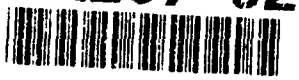
Quarterly Technical Report

for

Database System Studies in Fine Grain Optoelectronic Computing



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A.2. *Free- space interconnects*: Massively parallel processing requires large number of inter-processor data channels ($>10^4/cm^2$) each operating at high speed (.1-1 GHz) packaged in a small volume (10^3 cm^3). Free-space interconnects provide the potential to satisfy these stringent requirements. Our approach to free-space interconnects as shown in Fig. xx is based on vertical transmitters (VCSELs and/or MQW modulators) and receivers integrated with electronic logic circuits (Si and/or GaAs) forming smart pixel arrays that take advantage of the third dimension in contrast to A.1. The interconnection path between smart pixels as well as to guided wave long distance communication links and parallel access optical storage is established by means of efficient diffractive/refractive optical elements providing massively parallel high speed data channels.

However, to bring free-space interconnected systems to reality issues at material/device/system levels and their interfaces must be resolved. Our activities will be divided in two complementary halves. Part of the work will focus on establishing a generic technology and knowledge-base on material synthesis, component fabrication and testing, system packaging and assembly, modeling and characterization of free-space links. The other part focuses more on finding leverage for free-space interconnections within existing multi-processor architectures such as the Hughes 3-D computer and evaluating their commercial competitiveness. Special attention will be put on interfacing free-space interconnected systems to 3-D electronic processors, to guided wave communication links, and to parallel accessed optical storage devices to expand their applications span to image computation, database and multi-media applications, and sensor fusion.

Specific tasks in the materials growth and processing area include the development of active layer thickness control methods during MBE growth that will lead to better array uniformity for smart pixels and enable the repeatable fabrication of wavelength chirped transmitter arrays. Work will also be carried out to realize double-sided transmissive modulator based smart pixels to simplify system packaging using MQW modulators and detectors operating at longer wavelengths (e.g.1.06-1.3 um) where silicon and GaAs substrates are transparent. In addition, our present flip-chip bonding capabilities for integrating silicon logic with MQW modulator arrays will be extended to enable integration of silicon logic with VCSEL arrays. Furthermore, epitaxial lift-off, transfer and direct bonding technique (L-T-B) will be used to realize smart pixels by integrating Si or GaAs logic with GaAs light emitters. This technique may improve the operation speed of smart pixels while reducing their cost and improving their manufacturability. (Participants: L. Coldren, H. Wieder, E. Yablonovitch, S. Esener)

On the devices and circuits front simple electronic circuits performing XOR, 1bit memory and bypass and exchange switching operations will be incorporated at each pixel

of the smart pixels. To interconnect these pixels, smart multiplexed computer generated multi-level phase diffractive holograms as well as photorefractive static and dynamic holograms will be investigated for exploiting their high degree of volume multiplexing and reconfigurability for achieving more fault-tolerant systems. On the computer generated holograms (CGH) side, new fabrication procedures will be investigated including writing analog patterns by e-beam direct write and creating form birefringent structures. Studies will be conducted using different e-beam spot sizes to reduce exposure time and to achieve 3-D proximity compensation especially for grating periods less than 5μm. In addition, CGH's with several multiplexed impulse responses using polarization, wavelength or phase selectivity will be investigated for reconfigurability . For example, properly designed CGHs fabricated on birefringent substrates offer independent impulse responses for two orthogonal polarizations, effectively acting as a polarizing beam splitter with two diffractive optical elements. Modeling design, fabrication and testing of these interconnection devices will be carried out. On the other hand, volume holograms can also be used as efficient 2-D array generators to power-up light modulator arrays (with defect removal) and to achieve dynamically reconfigurable interconnections. Fixing of SBN and $LiNbO_3$ photorefractive crystals will be studied for their utilization in static interconnects. Dynamic reconfiguration characteristics of photorefractive interconnects eliminating fanout energy loss will also be investigated .(Participants: S.H. Lee, S Fainman, E. Hu, H. Craighead, P. Yeh)

On the architecture and packaging front, sub-system prototypes built on optical tables will be characterized and modeled. These prototypes will be used to understand the potentials of free-space optical interconnections in terms of bit-error rate, fan out, power and speed and determine new application areas. This characterization will be carried out for point to point interconnection topologies as well as topologies requiring larger fan-out. Experimental and modeling studies will be carried out to package such sub-systems into robust modules. Techniques such as flip-chip bonding and L-T-B will be used with various optical materials and adapted to the needs of free-space optoelectronic components. That is we will use these integration techniques as a further step in the hierarchy of integration and miniaturization at the system level rather than at the circuit level to realize integrated sub-systems. In addition, special sub-system architectures will be investigated to interface free-space systems with guided-wave communication links, parallel access storage and 3-D electronics. These interfaces are critical for architectures such as shared memory computing systems that require massively parallel data to be retrieved from storage systems and be transmitted at very high rate via fiber optic communication channels, while routing and processing of the data is carried out in parallel. Performing conversions between space division multiplexed (SDM) signals and wavelength division multiplexed (WDM) or time

division multiplexed (TDM) signals is then critical. Generic optoelectronic array interfaces compatible with microfabrication, high density electronics, mass manufacturing, and low cost assembly will be defined. These interfaces will be designed based on OTC technology including for example smart pixels with wavelength chirped optical outputs and diffractive and/or volume holograms to couple 2-D signals to fibers. In the future such parallel to serial data converters will also be useful for interconnecting free-space optoelectronic MCMs via fibers. (Participants: S.Fainman, S.H. Lee, E. Yablonovitch, P. Krusius, W. Chang, P. Yu and S. Esener)

These investigations will be carried out by a select team of researchers centered at UCSD together with researchers from UCSB and UCLA (focused on smart pixels integration), the packaging alliance at Cornell and UCLA (for array interfaces and system packaging) and our industrial partners including Hughes (for 3-D electronics and optical storage interfacing), Honeywell and Rockwell (for packaging), and AT&T (for diffractive optics).

In the past quarter we have investigated the architectural requirements for an intelligent optical memory interface for relational database applications. An intelligent memory interface will reduce I/O requirements to main memory by performing a portion of the database query directly at the secondary storage device. The Selection operator from the relational database model is an ideal candidate for implementation as an intelligent interface function. Selection examines individual data records, passing only those records which satisfy a query-dependent criterion. We have developed three increasingly complex architectures to support Selection and derivatives of Selection commonly found in practical database management systems.

Selection is an operation performed on a relation of data, as shown in Figure 1a. Each row of a relation is called a tuple, and corresponds to one record of data. Each column is called an attribute. Formally, Selection is a Boolean function of the results of simple comparisons, chosen from $\{<, \leq, =, \neq, >, \geq\}$, between tuple attributes and query constants. For example, the criterion

$$[\text{ Throws(T)=left(L) }] \text{ OR } [\text{ Innings Pitched(IP) } >200] \qquad [1]$$

yields the selected tuples shown in Figure 1b. Common augmentations allow comparisons between attributes in a tuple. For example, the criterion

$$\text{Wins(W)} \leq \text{Losses(L)} \qquad [2]$$

selects the tuples shown in Figure 1c. Moreover, most practical database management systems allow comparisons between simple arithmetic expressions of the tuple attributes and constants. The criterion

$$9 \cdot \text{ER/IP} < 3.00 \qquad [3]$$

yields the selected tuples in Figure 1d.

The architecture shown in Figure 2 was originally proposed to implement the formal definition of Selection. The tree-based digital comparator examines two bit-strings, D being the data recalled from memory and Q the query constant, yielding two bits at the root representing their equality relationship. If D>Q, then g=1 while l=0. If D<Q, then g=0 while l=1. From these two bits, any of the numerical comparisons can be determined. The bit string D may

represent several attributes. To perform a comparison between only one attribute and a constant, both the query bit q_i and its complement $\neg q_i$ are forced to zero if the bit location i is not in the queried attribute. Multiple comparisons on a tuple can be time-multiplexed. Unfortunately, this architecture does not allow comparisons between attributes, such as that in equation [2]. We have developed an improved architecture, shown in Figure 3a, which allows such comparisons. In this architecture, the tuple is optically loaded into a RAM, with each row of the RAM receiving one attribute. If the attribute value is large, several rows will be required. The RAM may also hold several query constants. Rows from the RAM are read into a smaller digital comparator. Hence, comparisons can be made between attributes of a tuple, or between an attribute and a query constant. The architecture in Figure 3b is similar, except that an ALU between the optically loaded RAM and comparator allows simple arithmetic calculations before the comparison. These architectural designs will be presented at the 1993 OSA annual meeting to be held this Fall in Toronto.

We are currently investigating the feasibility of implementing these architectures with optoelectronic GaAs fine-grain processors. The simple, regular structures of the digital comparator and optically loaded RAM should be amenable to optoelectronic implementation. Optoelectronic implementation of the ALU may pose a difficult challenge. Hence, we may find that database systems requiring comparisons on arithmetic expressions of data must store redundant information, in the form of precalculated expressions, if an optoelectronic intelligent interface is to be used. For certain applications, the increased retrieval rate may outweigh the increased use of storage capacity.

We are also beginning our investigation of GaAs optoelectronic technologies for digital free-space optical interconnects. This investigation will determine the application niche of these technologies according to system performance criteria such as bit rate, bit error rate, density, and optical fan-out. This investigation will include the effects of detector and transmitter design on the system performance parameters. This investigation will include both theoretical models of free-space optical interconnections as well as experimental evaluation of the predicted speed and reliability trade-offs.

1991 Dodgers Pitching Statistics

attribute

Name	T	W	L	SV	IP	ER	BB	SO	H
Tim Belcher	R	10	9	0	230.33	61	75	156	189
Orel Hershiser	R	7	2	0	112	43	32	73	112
Ramon Martinez	R	17	13	0	220.33	80	69	150	190
Kevin Gross	R	10	11	3	115.67	46	50	95	123
Bob Ojeda	L	12	9	0	189.33	67	70	120	181
Mike Morgan	R	14	10	1	236.33	73	61	140	197
Steve Wilson	L	0	0	2	20.67	6	9	14	14
John Candelaria	L	1	1	2	33.67	14	11	38	31
Roger McDowell	R	6	3	7	42.33	12	16	22	39
Jim Gott	R	4	3	2	76	25	32	73	63
Tim Crews	R	2	3	6	76	29	19	53	75
Jay Howell	R	6	5	16	51	18	11	40	39

tuple

(a)

Name	T	W	L	SV	IP	ER	BB	SO	H
Tim Belcher	R	10	9	0	230.33	61	75	156	189
Bob Ojeda	L	12	9	0	189.33	67	70	120	181
Mike Morgan	R	14	10	1	236.33	73	61	140	197
Steve Wilson	L	0	0	2	20.67	6	9	14	14
John Candelaria	L	1	1	2	33.67	14	11	38	31
Ramon Martinez	R	17	13	0	220.33	80	69	150	190

(b)

Name	T	W	L	SV	IP	ER	BB	SO	H
Tim Crews	R	2	3	6	76	29	19	53	75
Steve Wilson	L	0	0	2	20.67	6	9	14	14
John Candelaria	L	1	1	2	33.67	14	11	38	31
Kevin Gross	R	10	11	3	115.67	46	50	95	123

(c)

Name	T	W	L	SV	IP	ER	BB	SO	H
Tim Belcher	R	10	9	0	230.33	61	75	156	189
Roger McDowell	R	6	3	7	42.33	12	16	22	39
Mike Morgan	R	14	10	1	236.33	73	61	140	197
Steve Wilson	L	0	0	2	20.67	6	9	14	14
Jim Gott	R	4	3	2	76	25	32	73	63

(d)

Figure 1: (a) Relations are simply tables of similar data. Each row is called a tuple, while each column is called an attribute. (b) Selection produces a resultant relation from an input relation by accepting only those tuples satisfying a given criterion. That criterion can be expressed as a Boolean function of numerical comparisons between attributes and query constants. Here, tuples are selected from the relation according to [T=L]OR[IP≥200], which finds all pitchers who are either left-handed or pitched more than 200 innings. Common augmentations to Selection allow comparisons between attributes of a tuple or arithmetic expressions of these attributes. (c) The comparison W≤L illustrates a comparison between attributes of a tuple. (d) The comparison 9•ER/IP≤3.00 illustrates a comparison on arithmetic expressions.

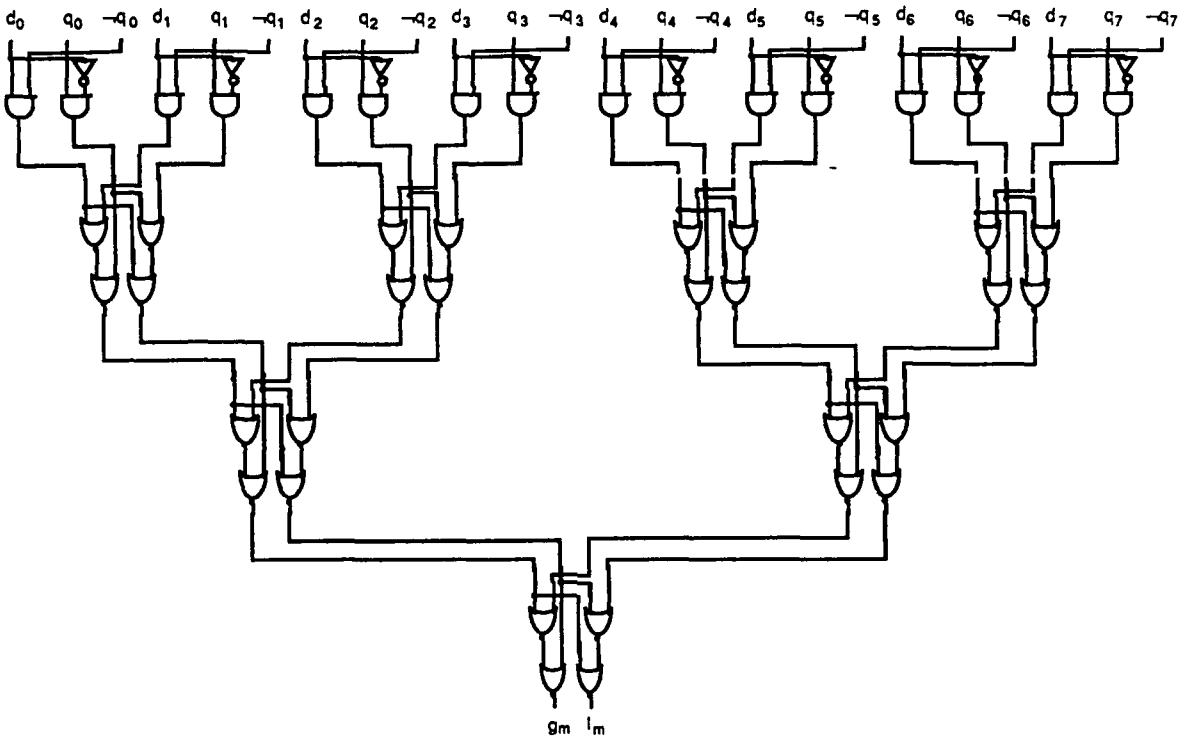

Figure 2: A tree-based digital comparator can support Selection. Leaf units compare two strings at each bit level. The bit-wise comparisons propagate through the tree, with the comparison at the most-significant-bit where the two strings differ arriving at the root of the tree. Bits can also be ignored in this architecture by forcing the local comparisons to zero.

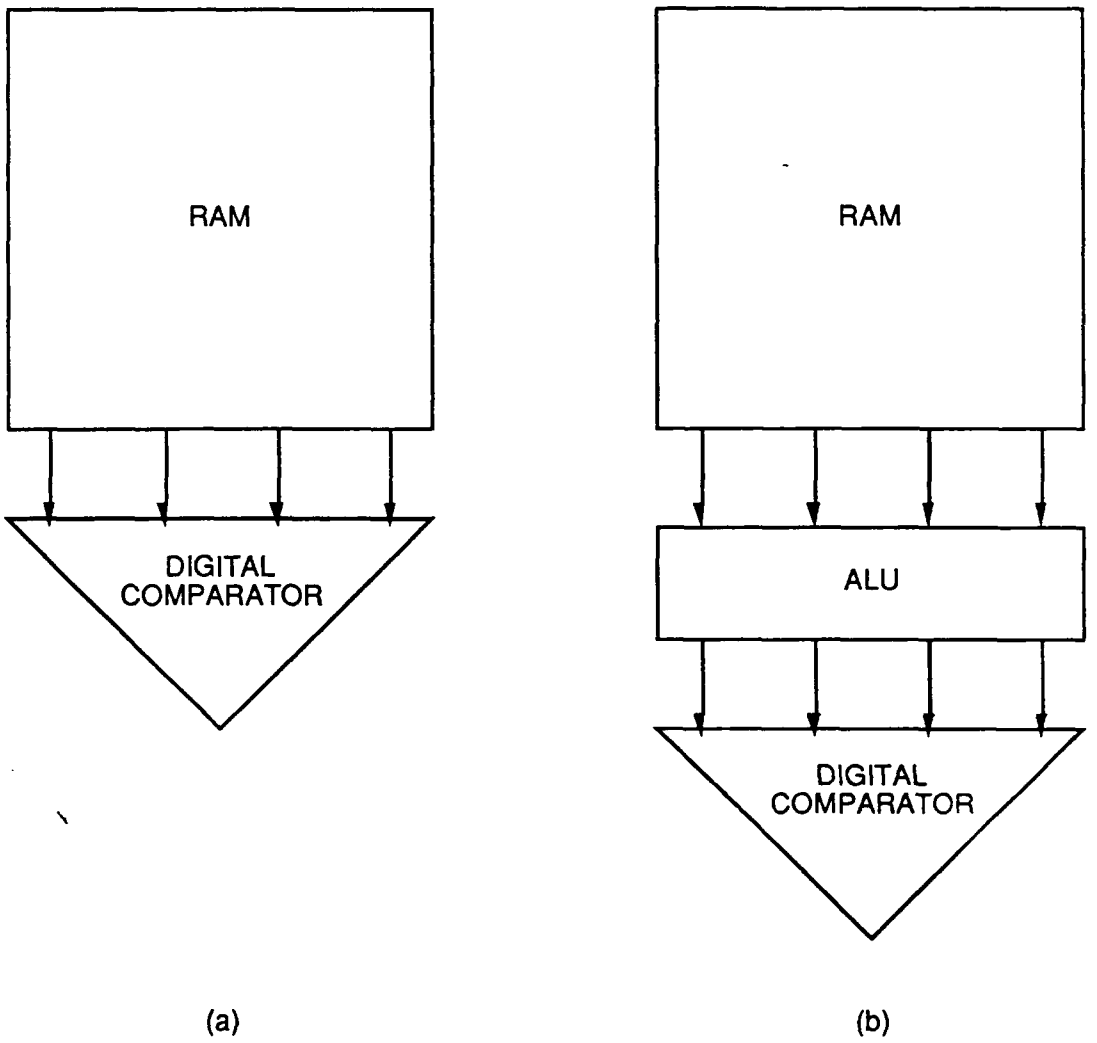

Figure 3: (a) For an augmented Selection which allows comparisons between tuple attributes, an optically loaded RAM precedes a smaller digital comparator. The RAM is loaded with a tuple and query constants. Each row of the RAM corresponds to one word. Attributes with multiple words are distributed over several rows. Attributes and query constants can be arbitrarily retrieved and compared. Comparisons on multi-word attributes can be time-multiplexed as smaller comparisons, with the most significant word comparison performed first. (b) For an augmented Selection with arithmetic expressions, an ALU is required between the RAM and digital comparator.