



NAVY Topic 113: Object Recognition Chip

A high-speed object recognition chip based on a biologically-realistic Hybrid Temporal Processing Element

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Progress Report # 2

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This report traces the progress made by Intelligent Reasoning Systems, Inc. (IRSI) on contract N00014-93-C-0118, from June 1, 1993 to July 31, 1993. The structure of this report is as follows: introduction and Phase I objectives, progress to date, projected progress, and appendices containing example programs.

Technical Objectives:

The technical objective of this Phase I effort is to evaluate the feasibility of a binocular object recognition system for the INtegrated Active VISION System (INAVISIONS) currently under development at IRSI. The INAVISIONS is based on a custom Very Large Scale Integration (VLSI) Hybrid Temporal Processing Element (HTPE) developed by IRSI (patent pending) [1-4].

Active vision implies that the image collection and processing operations form a single, integrated, adaptive system in which high-level processes, such as object recognition, can augment lower-level processes through feedback connections and can itself be controlled by higher levels. For example, the object recognition process can instruct the oscillating saccadic perception system to enhance the image resolution by a particular amount to assist in the object recognition process. Higher level perception systems can guide the object recognition processes by using expectations of what objects might be present in the image. Therefore, the INAVISIONS behaves a single image collection and processing system with coupled low- and high-level capabilities.

The IRSI INAVISIONS incorporates principles derived from experimental analysis of mammalian visual systems. Mammalian visual systems employ multiple concurrent, cross-coupled processing pathways to simultaneously infer location, motion, shape, color, and texture from images of an object obtained asynchronously and from multiple points of view (e.g. [5-6]). Processing occurs asynchronously, with continuous feedback between early and later processes. For example, low-resolution location and motion detection guide eye movement and visual attention through a fast feedback loop, while also contributing to slower, higher-resolution downstream motion, shape, and texture processing.

The INAVISIONS design is based on an asynchronous analog encoding of location and motion data, and the custom VLSI HTPE. The HTPE closely models the generic spiking neurons of the human brain [1-4]. Spiking neurons perform time-based processing using impulse-like Action Potentials (APs) and slowly time-varying Post Synaptic Potentials (PSPs). HTPEs can be used to encode and process information in terms of amplitude, frequency, phase, and time delay. In HTPE systems, transient and steady-state waveforms are used to provide real-time processing capabilities. The HTPE can operate on analog data at frequencies in excess of 100 MHz, allowing rapid oversampling methods to be used for resolution enhancement, motion detection, and multiple template matching. HTPEs have low device

intelligent machine tools, and other autonomous sensory-motor systems that require visible, IR, UV, or similar input. The basic architecture developed for the INAVISIONS will, however, also be useful for any sensory input that can be represented in a plane, and for which spatial continuity is a relevant constraint.

The initial stage of the INAVISIONS collects data asynchronously from the primary sensor, and provides a parallel analog encoding. This encoding allows preprocessing circuitry for tasks such as low-level resolution enhancement and motion-detection to be built into the retina, and to operate on data from each pixel or neighborhood of pixels in parallel. The preprocessed data is then encoded in asynchronous pulse streams and mapped, again in parallel, to hierarchical feature detection systems in which spatial relations between processing elements corresponding to pixels or pixel neighborhoods are preserved. The processing layers in this initial INAVISIONS stage correspond to the early processing stages in the retina of the Human Visual System (HVS). The initial stage of the INAVISIONS, from here on referred to as the INTe grated Saccadic Perception Image Resolution Enhancement System (INSPIRES), was developed under an Army Phase I SBIR effort and is currently in the Phase II review process.

6. In general, the optimal split between object recognition for attention and targeting and shape recognition needs to be identified, as do the points at which feedback from higher-level processing can be used to disambiguate objects and shapes.

Progress to Date:

SUMMARY OF FIRST WORK PERIOD

In the first work period, the overall structure of the Feature and Object Recognition SystEm (FORSE) was designed. The FORSE is intended for use in the complete INAVISIONS. The INAVISIONS, and hence, the FORSE are fully-parallel systems that are designed to be implemented in state-of-the-art three-dimensional VLSI circuitry. The structure of both systems will be examined in the following section on the projected progress for the final work period.

Conventional Cellular Neural Networks (CNNs) were examined in the first work period for use as spatial feature extraction and image transformation systems. CNNs require only spatially homogeneous, local connections and are amenable to analog VLSI implementation. The network structure is

Fig. 2: Non-Linear vs Linear Encoding Techniques.

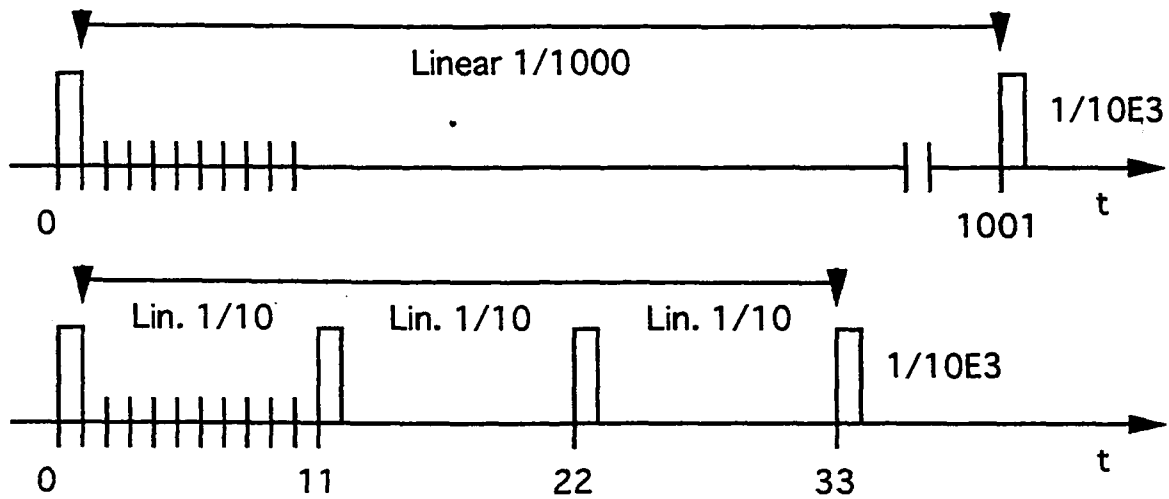


Fig. 3: HTPE Bias/Parameter Non-Linearity.

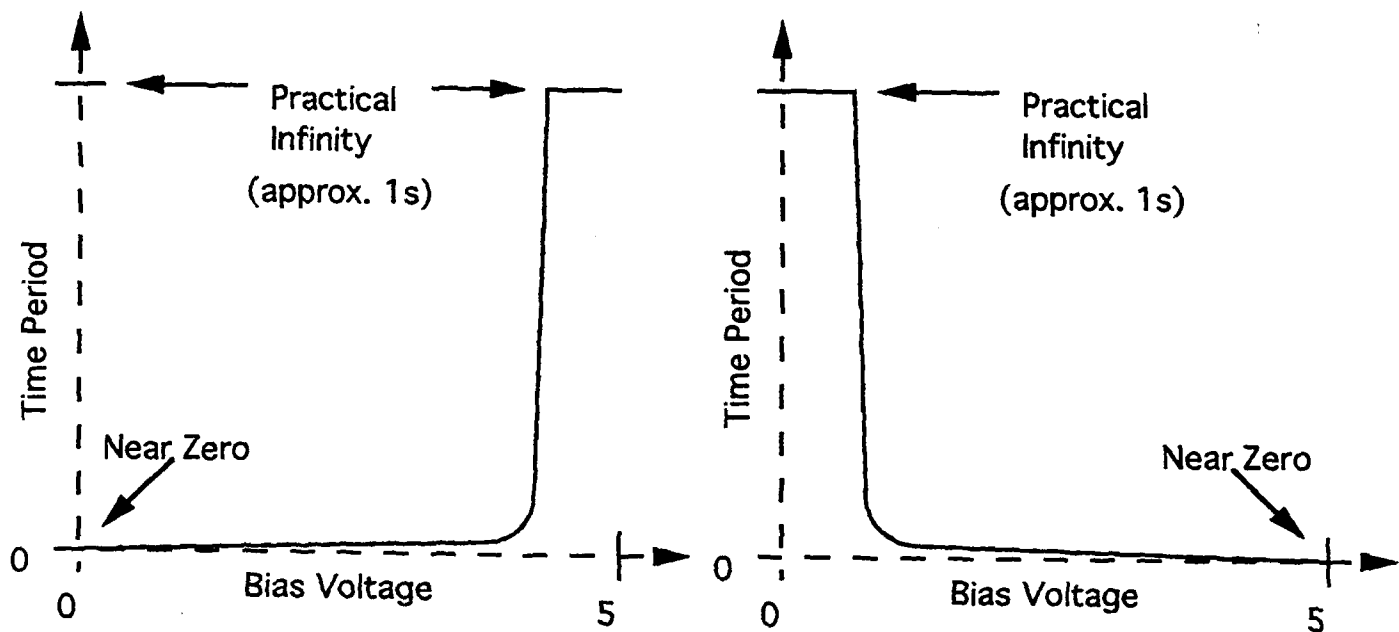


Fig. 4: HTPE Frequency/Pulse Width Oscillator.

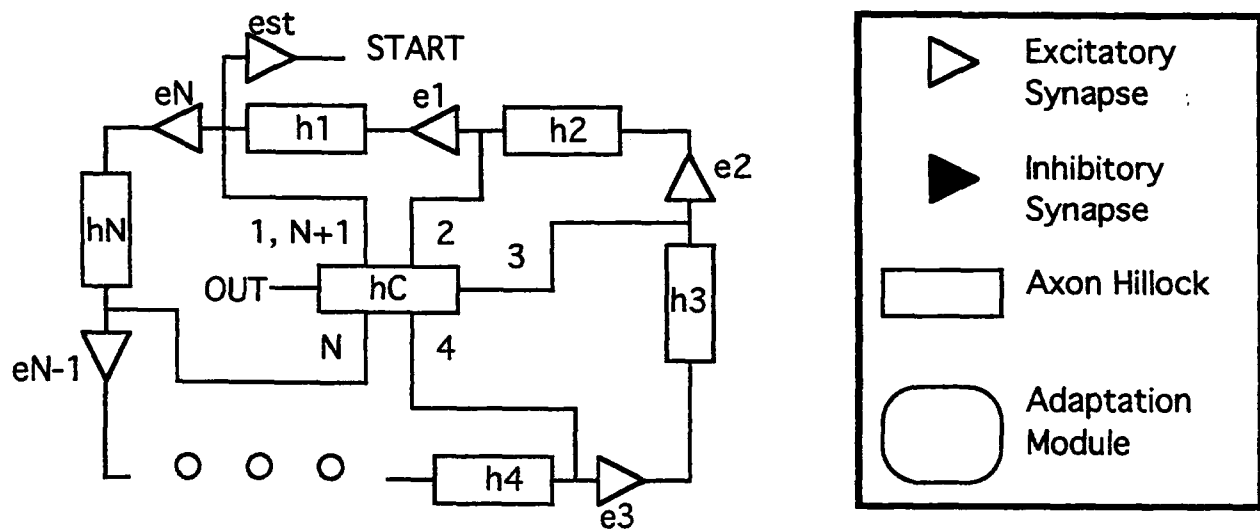


Fig. 5: Simulated Behavior of the HTPE Frequency/Pulse Width Oscillator.

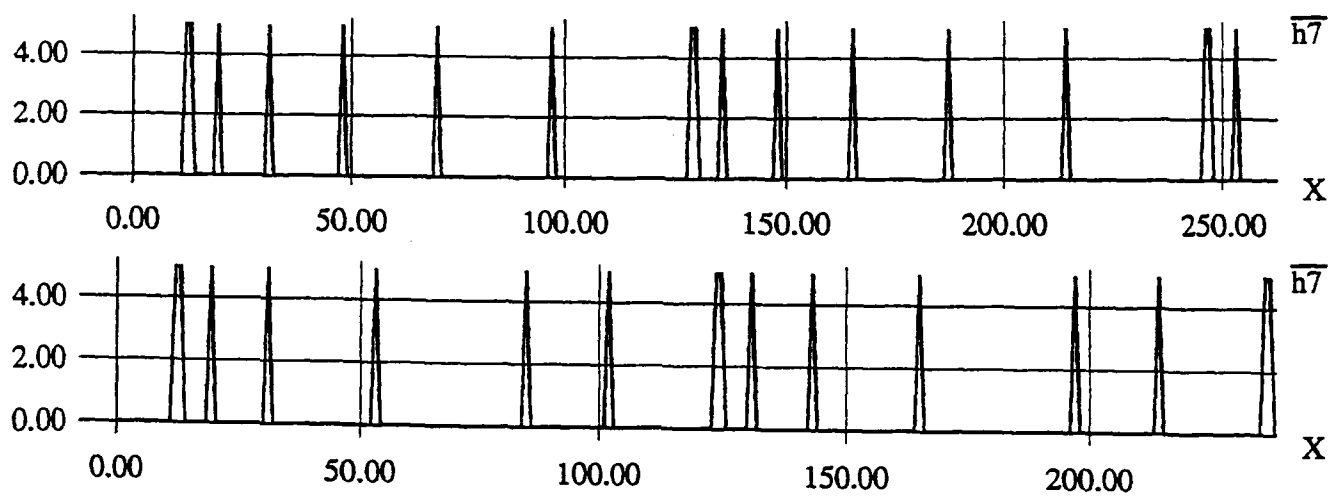


Fig. 6: HTPE Serial-to-Parallel Converter.

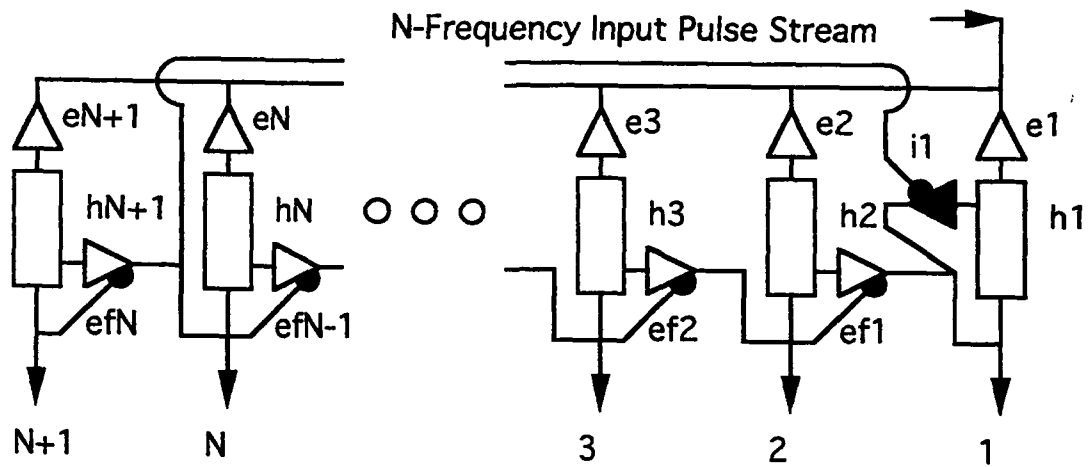


Fig. 7: Simulated Behavior of the HTPE Serial-to-Parallel Converter.

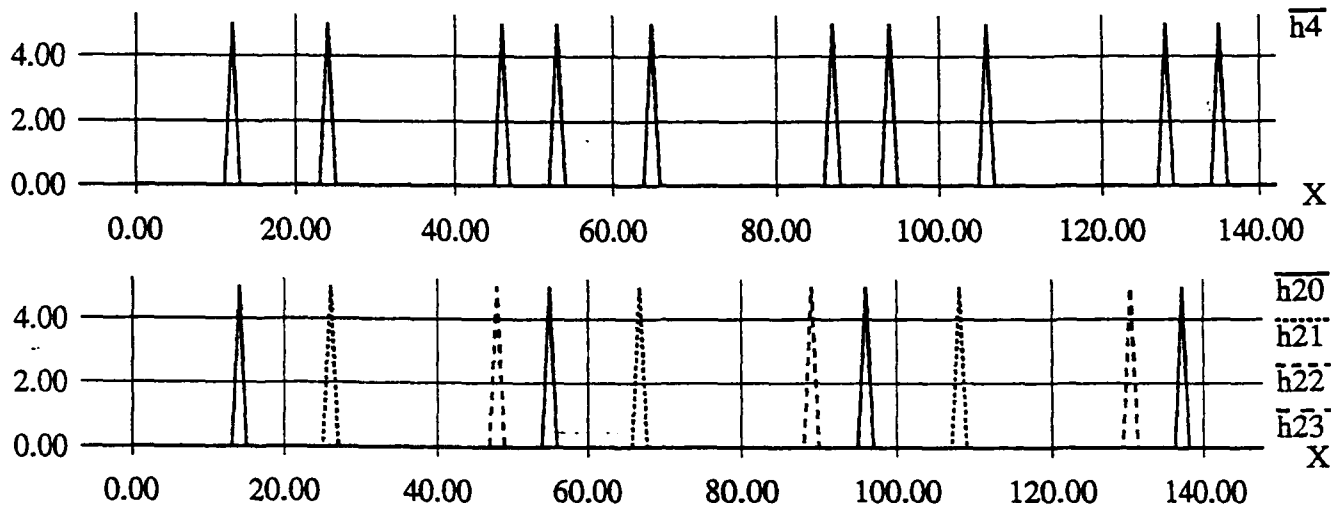


Fig. 8: Block Diagram of HTPE Relative Difference Network.

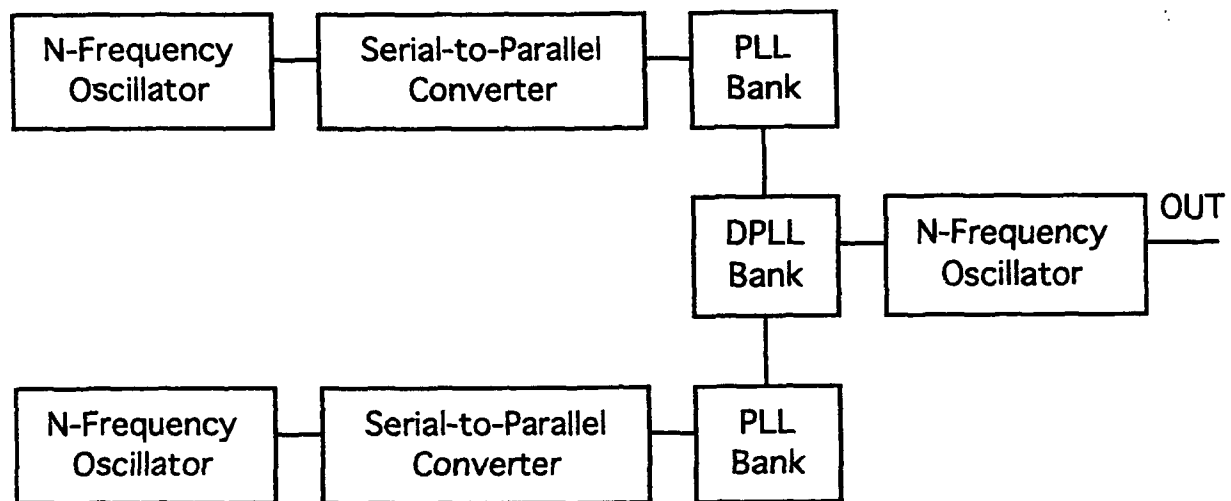


Fig. 9: HTPE Phase-Lock-Loop.

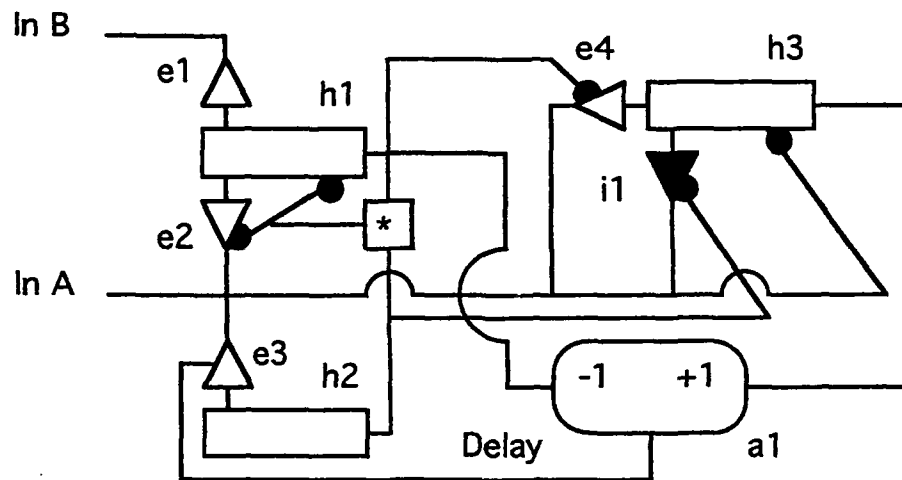


Fig. 10: Simulated Behavior of the HTPE Phase-Lock-Loop.

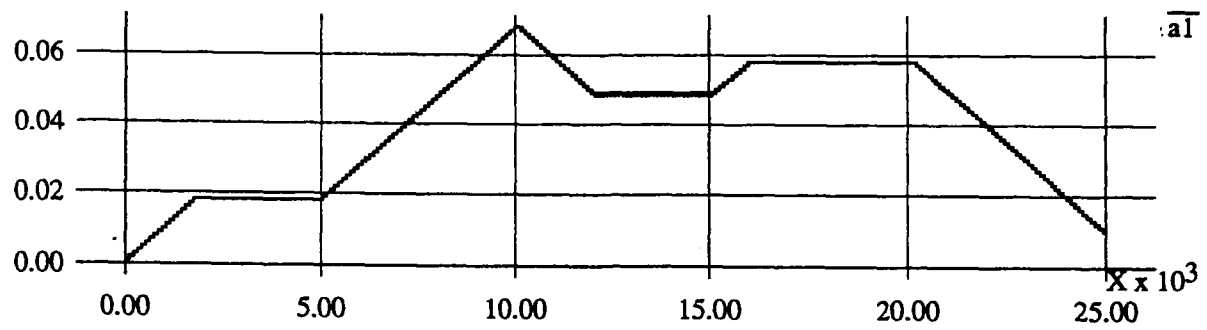


Fig. 11: Simulated Behavior of the HTPE Relative Difference Network.

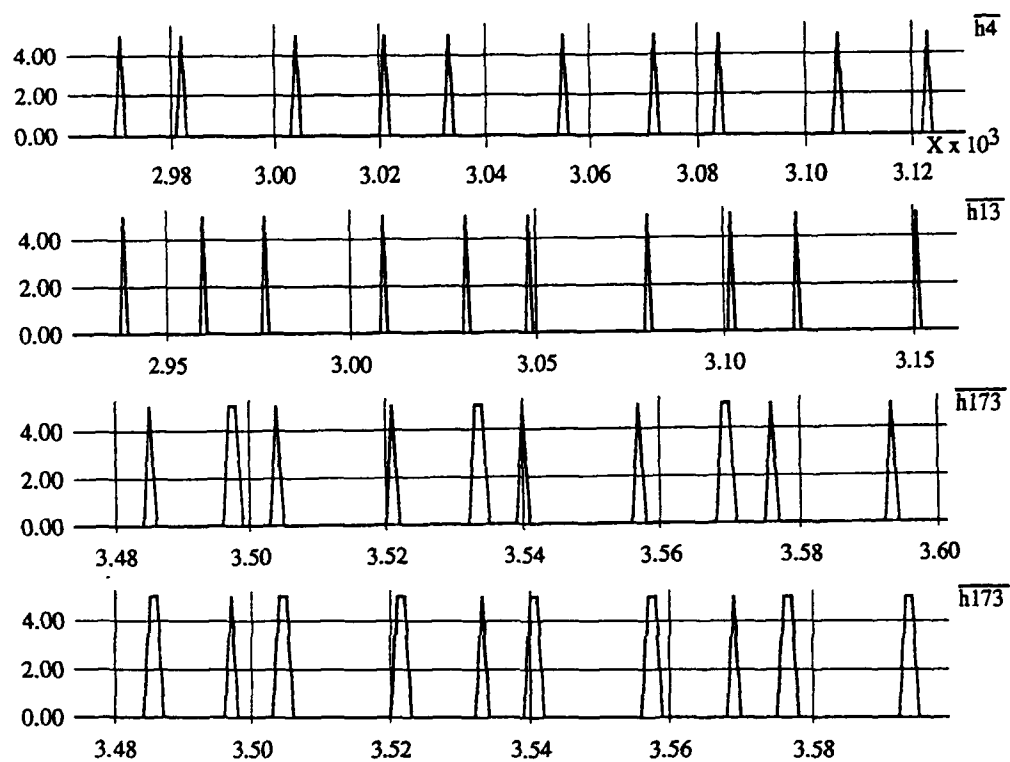


Fig. 13: Nearest-Neighbor Connection Scheme.

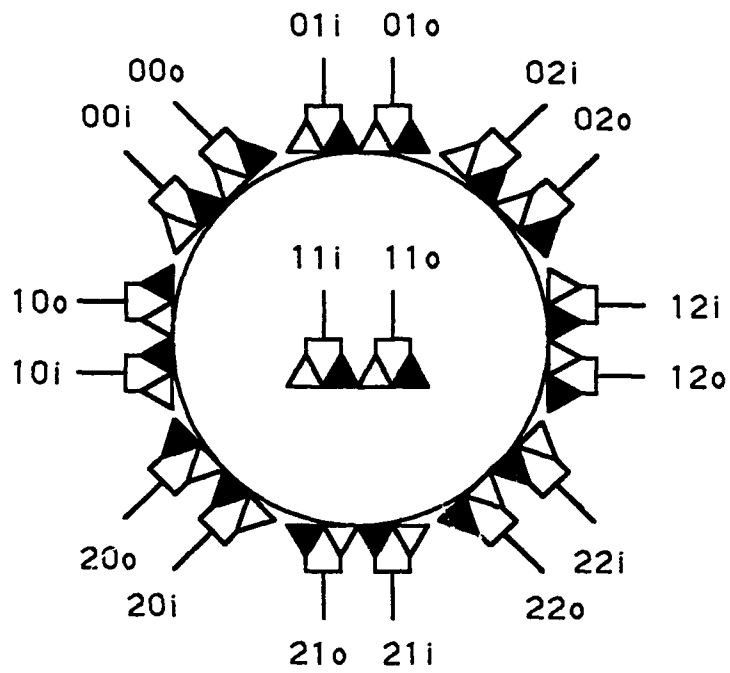


Fig. 14: Basic HTPE Waveforms and Operation.

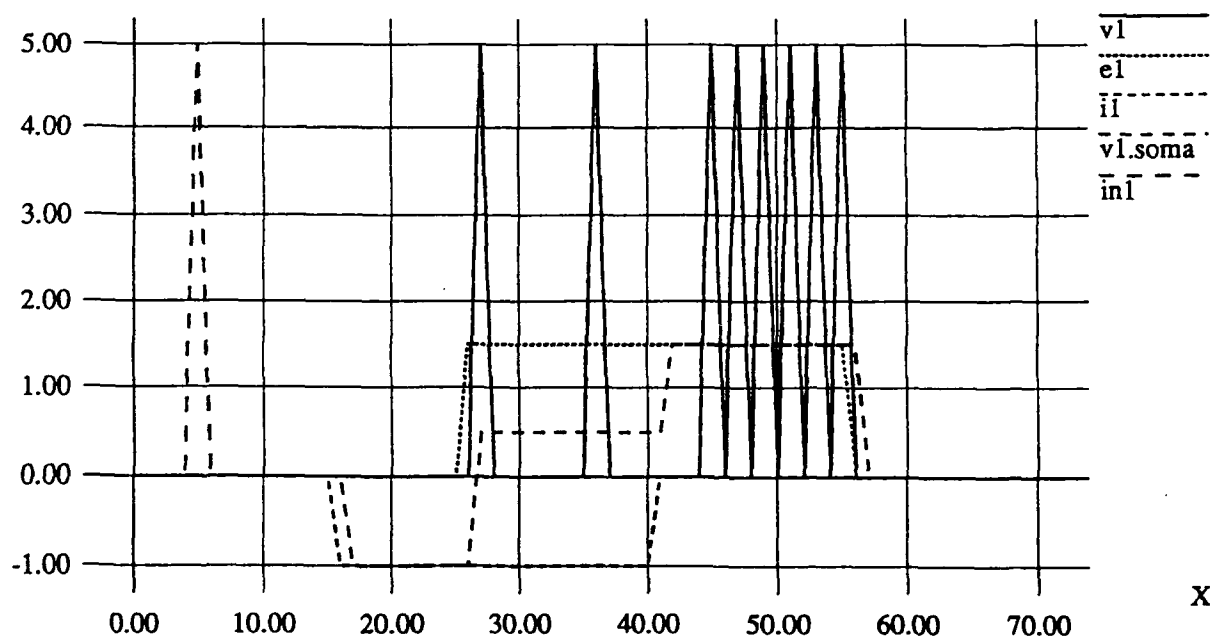
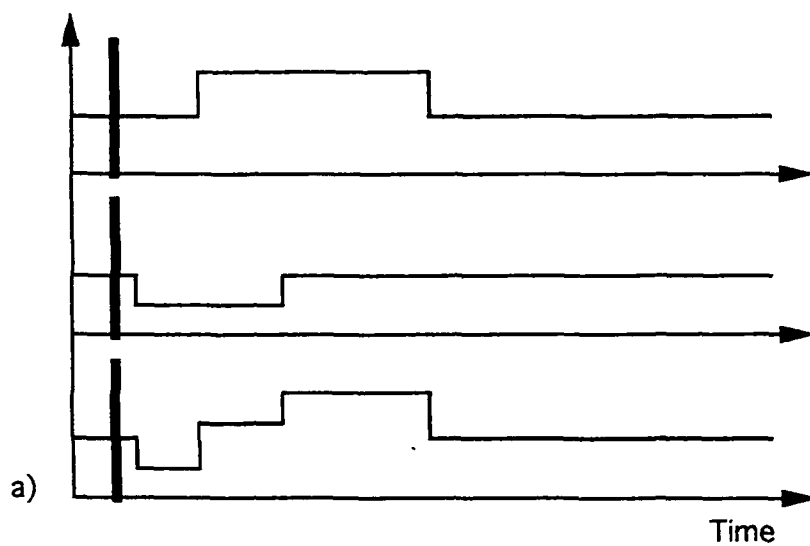


Fig. 22: Illustration of Depth-to-Disparity Mapping.

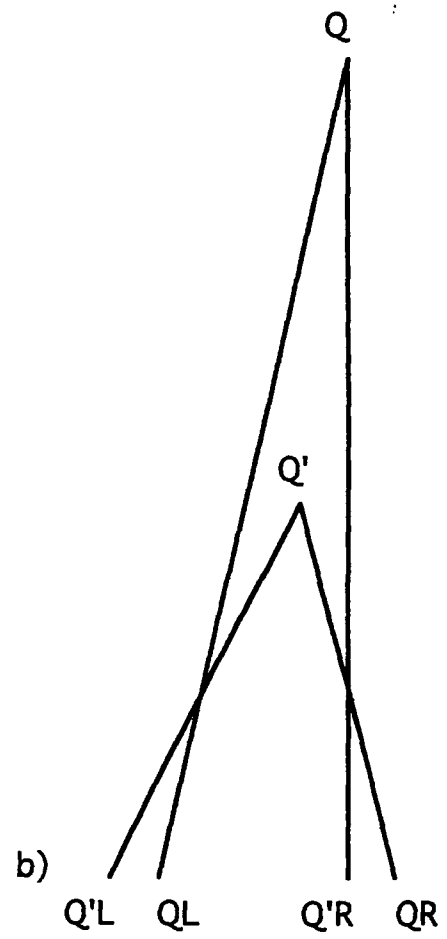
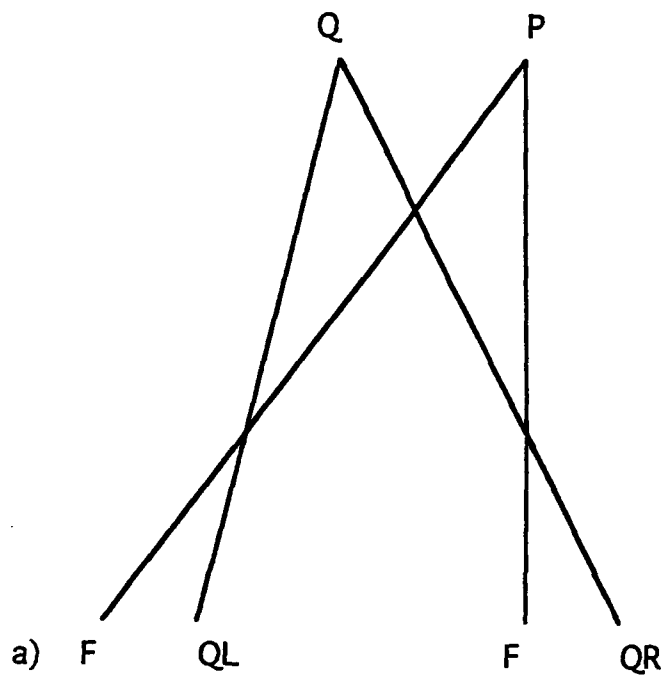


Fig. 23: Block Diagram of IRIS Integrated Active Vision System.

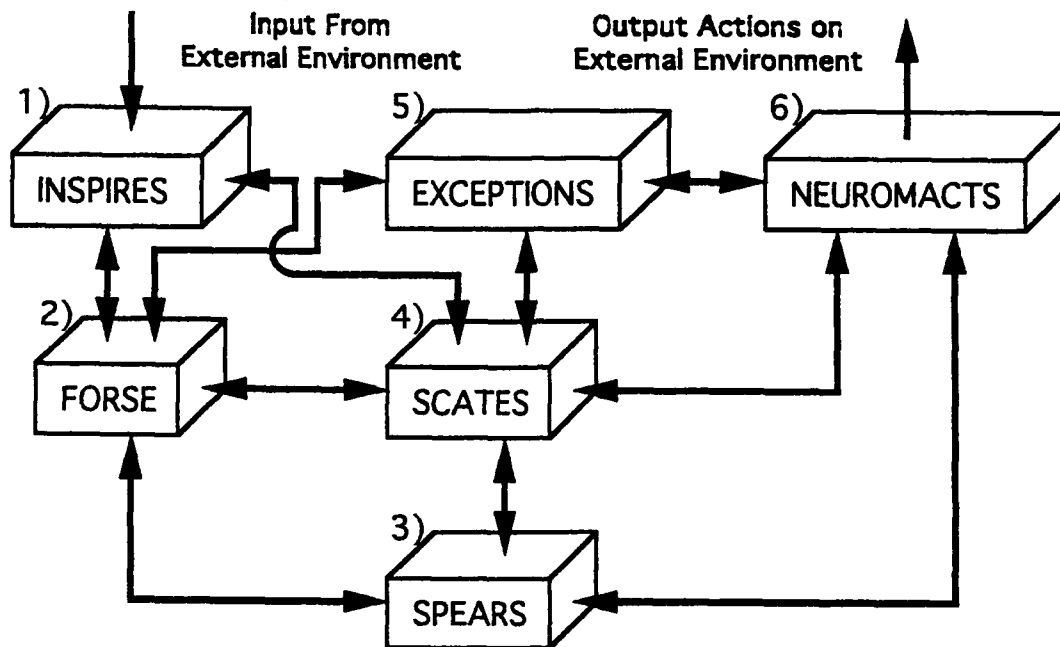


Fig. 24: Block Diagram of Feature and Object Recognition System Configurations.

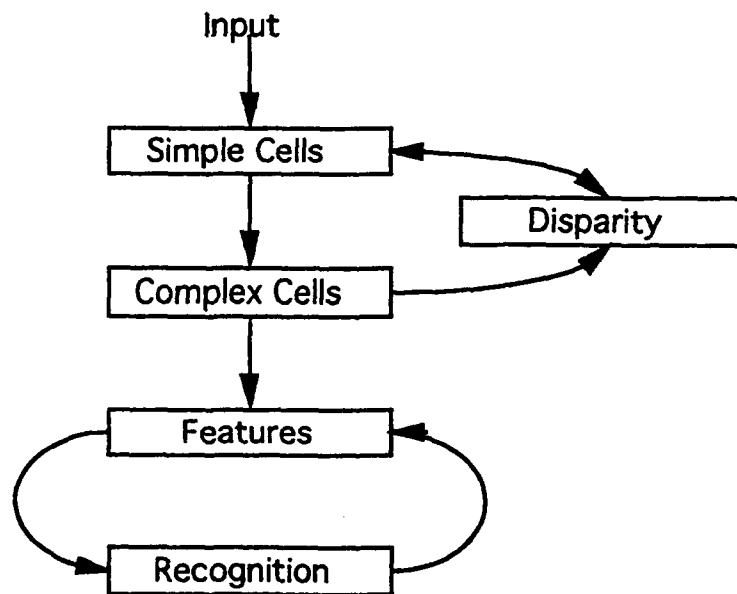
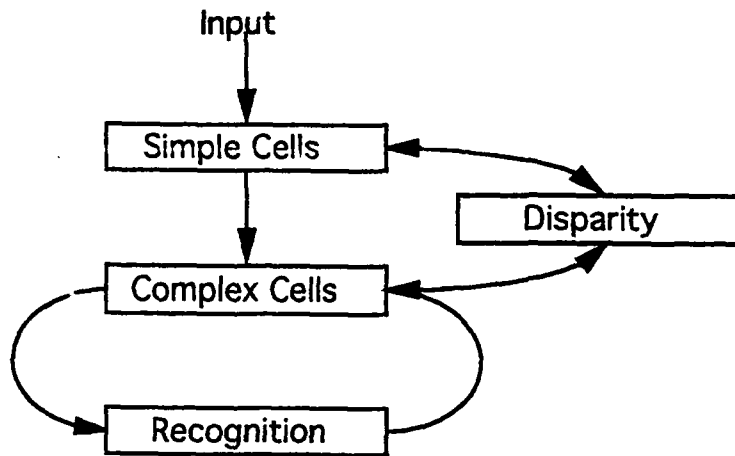


Fig. 25: Hierarchical Nature of the Grammar-Based Approach.

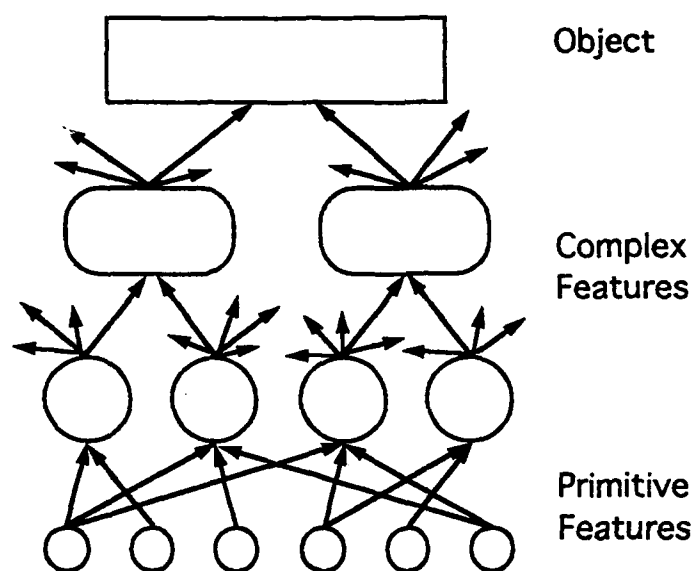


Fig. 26: EPSP, IPSP, SPSP, and AP Waveforms Produced by HTPe.

