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QUARTERLY REPORT NO. 4

FOR

ANALOG-TO-DIGITAL CONVERTER

CONTRACT NO. N00014-87-C-0314

1 JANUARY 1988 - 31 MARCH 1988

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Program Code Number: 7220

Name of Contractor: Texas Instruments Incorporated
13500 N. Central Expressway
P.O. Box 655936, M. S. 105
Dallas, Texas 75265

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Short Title of Work: GaAs A-to-D Converter

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23 May 1988

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FOR
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Contract No. N00014-87-C-0314
1 January 1988 - 31 March 1988

I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high sampling rate A/D converter and a high resolution GaAs A/D converter.

B. Baseline Process Development

During the past quarter, TI has directed its efforts toward improving HBT current gains and processing the first ADC test chip. HBTs have been fabricated with current gains higher than 50, although typical gains are in the 10 to 20 range. Using our overgrowth process, we have successfully demonstrated the first known integration of *n*-channel JFETs and *mpm* HBTs. Using our overgrowth process.

The ADC test chip includes a 5-bit ADC, a 4-bit ADC, and four sample-and-hold circuits, as well as various process monitors. The first ADC lot completed processing and was delivered to Hughes for characterization. Several additional lots of the new ADC test chip are being processed, and the current lead lot is expected to be completed in May.

C. A/D Converter Circuit Design

The Hughes ADC development effort this quarter has focused on two related efforts: (1) the design, layout, and test of a high speed 5-bit ADC and sample-and-hold (S/H); and (2) device modeling, a resistor trimming investigation, and process development support. The Hughes circuit design team attained a significant milestone by completing the circuit design and layout of both a 5-bit ADC and a S/H circuit. The Hughes portion of the test die was organized and released to TI for processing at the end of January. In

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custom thin-film test hybrid required to dynamically evaluate the 5-bit ADC and S/H. The primary device modeling achievements were the development of complete HBT overgrowth process bipolar and Schottky diode models and thermal characterization of the precision Cermet resistors. Development of a laser trimming methodology for on-chip Cermet resistors also began this quarter.

II. HUGHES-TI MEETING

A preliminary design review held on 21 January accomplished a number of important goals:

- (1) Questions concerning HBT modeling and projected device characteristics were discussed.
- (2) Critical performance-limiting device characteristics were discussed. Near-term processing goals, including reduced collector-base capacitance and improved current gain, were outlined.
- (3) We discussed a number of technical issues related to device development, including optimization of a Schottky diode structure, design of an improved capacitor technology, and design of a subsurface zener structure.
- (4) Layout of the partially completed 5-bit ADC was reviewed. Layout guidelines to enhance yield were discussed.
- (5) Issues related to the release of the January mask set were resolved.
- (6) Circuit design progress and projected performance for the 5-bit ADC and S/H circuit were reviewed.
- (7) Strategy and schedule were discussed for the May technical review.

III. HETEROJUNCTION BIPOLAR PROCESS DEVELOPMENT

Work is continuing on the baseline process in which the base layer is grown as part of the first epi, then selectively defined and etched before the emitter layer is grown. In addition to the emitter AlGaAs/GaAs n-epi layers, a thin (500 to 800 Å) p-epi GaAs layer is grown as the cap layer. This top p-epi layer forms the gate for the n-channel JFETs. It is selectively patterned and etched from the surface except in regions where the n-channel JFETs are to be formed. Utilizing this overgrowth process, we can integrate n-channel JFETs with the HBTs using only one additional mask level. Figure 1 illustrates the I-V characteristics of an n-channel JFET and an HBT

NPN CROSS SECTION

COLLECTOR BASE

TRENCH/
Si₃N₄ REFILL

EMITTER

P-GaAs

BORON
IMPLANT
DAMAGE

p+

n- p

n+

JFET CROSS SECTION

BACK GATE GATE P-GaAs

SOURCE

DRAIN

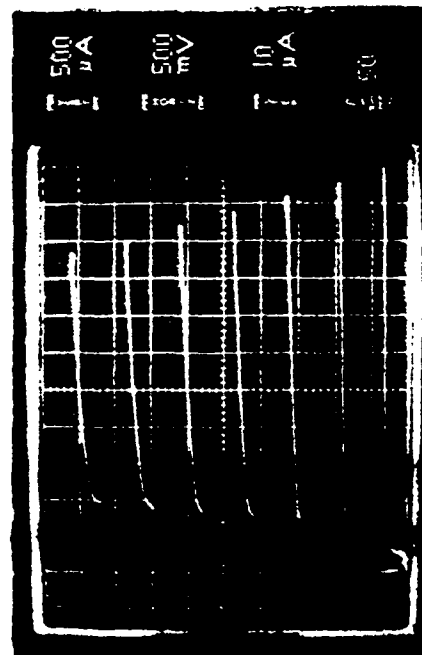
Si₃N₄

p+

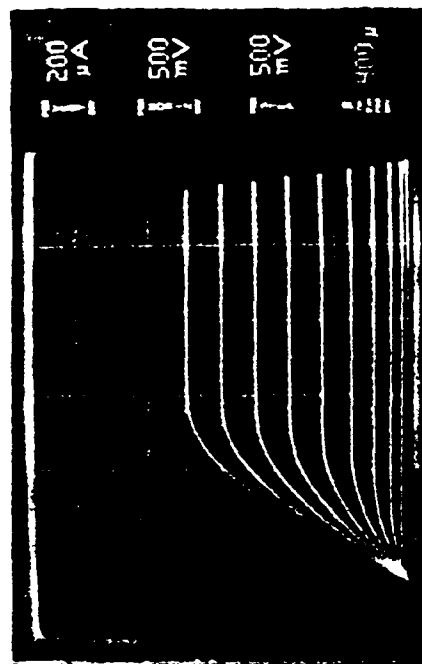
n- p

n+

SEMI-INSULATING GaAs



NPN HBT
I-V CHARACTERISTICS



N-CHANNEL JFET
I-V CHARACTERISTICS

Figure 1. Integrated npn HBT and n-channel JFET.

fabricated on the same chip utilizing this process. It can be seen that the HBT exhibits good gain and satisfactory Early voltage characteristics. The n-channel JFET with a gate length of 5 μm exhibits a transconductance of 25 mS/mm.

Despite these very positive results, some processing problems associated with the overgrowth process have been identified. The first of these problems involves the clean-up prior to overgrowth epi deposition. As a result of improper clean-up, the deposited AlGaAs/GaAs layers were polycrystalline. A new clean-up and inspection have been installed in the process, and the problem appears to have been eliminated. The second problem was encountered on several lots in which the concentrated HF used to strip a nitride layer attacked the AlGaAs in regions in which the GaAs cap layer had been selectively removed. The etching of the AlGaAs layer undercut the GaAs cap layer from the wafer, causing the emitter to be stripped from the HBTs. It is well known that for aluminum concentrations in excess of 30%, HF will etch AlGaAs; however, the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ used for these lots was not expected to be affected, since previous lots using this film had resulted in no etching in concentrated HF. Four lots were scrapped as a result of this problem, and additional lots were started. The HF stripping of the nitride has been replaced by a buffered oxide etch solution that does not etch AlGaAs, but does successfully etch the nitride. This process change has completely eliminated the etching of the AlGaAs.

The reticles for the new ADC test bar have been received. This mask set contains the designs for a 4-bit A/D and a 5-bit A/D, as well as four different sample-and-hold circuits. The first ADC lot fabricated with this mask set has been completed and delivered to Hughes for characterization. Initial test results suggest that the HBT current gains are low, which may prevent the circuits from operating successfully. Several additional lots are being processed with this mask set, and the next lot completion is scheduled for May.

Now that the process program has focused on a single overgrowth process, the emphasis during the coming months will be placed on identifying and eliminating the causes of the low HBT current gains. The goals for this

effort will be to routinely obtain uniform current gains > 50 while maintaining the large Early voltage required for the ADC circuits.

IV. CIRCUIT DESIGN PROGRESS

During the past quarter, the Hughes circuit design team attained a significant milestone by completing the architecture analysis, circuit design, and layout of the 5-bit ADC and high speed sample-and-hold (S/H). The Hughes portion of the test die (Figure 2) was organized and delivered to TI at the end of January. The 103 mil by 142 mil 5-bit ADC design requires only 800 active devices and has a projected maximum clock rate of 1 Gigasample-per-second (Gsps). Near-term process improvements, which include reduction of critical device parasitics, will allow the design to be extended to 2.5 Gsps. The high speed S/H design, which integrates a wideband hold amplifier and low distortion sampling gate, requires a die size of only 51.5 mils by 52 mils. The S/H circuit requires only 56 active devices and features a projected maximum clock rate in excess of 1 GHz.

The 5-bit ADC design efforts focused on optimizing the analog front-end for peak dc and dynamic linearity. Detailed computer simulations of the folding amplifiers, interpolation ladder, and comparator circuit were performed. A computer-generated "ideal" DAC was used to achieve high fidelity reconstruction of the ADC comparator threshold crossings. The DAC reconstruction allowed optimization of the ADC dc linearity and high frequency signal-to-noise performance. The 5-bit ADC was designed for minimum sensitivity to transistor current gain and V_{be} matching. To further minimize technical risk and maximize IC yield, the design was implemented with a single device type with a $7 \times 7 \mu\text{m}^2$ emitter size.

Detailed circuit design of the 5-bit decoder was completed. The chosen decoder architecture was optimized for maximum data clock rate and minimum data skew. The decoder design also includes on-chip latches and 50Ω output drivers. In addition, clock driver circuits for the comparator latches and output latches were designed and included on the final IC. Layout of the entire IC was completed near the end of January.

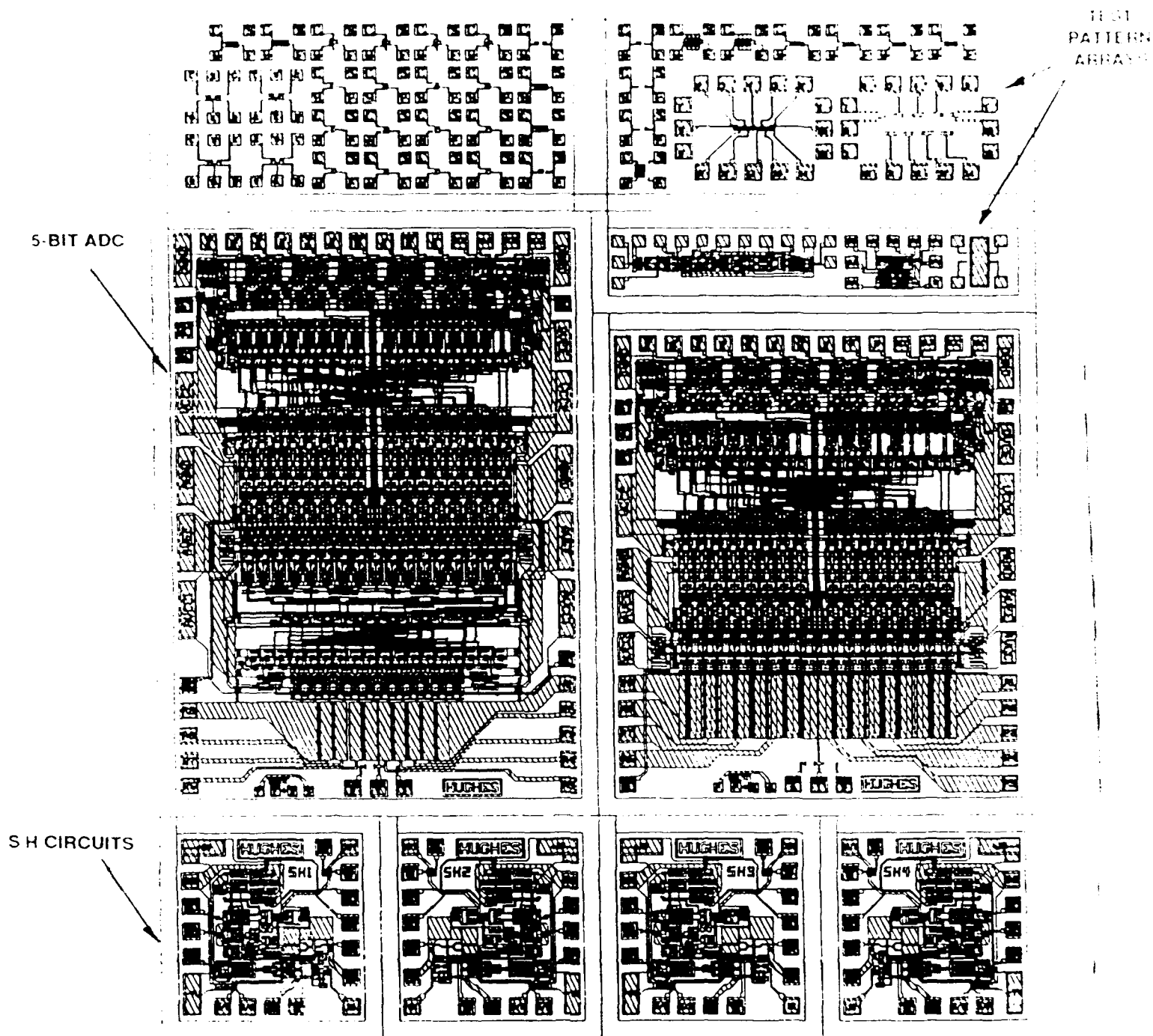


Figure 2. 5-bit ADC and S/H development bar.

The high speed S/H design was completed in parallel with the 5-bit ADC design. The HBT S/H is an open-loop, single-ended design that utilizes a Schottky diode sampling bridge. The S/H architecture consists of a sampling gate, gate driver, and hold amplifier. Computer simulations of the entire S/H circuit were performed. The Schottky diode gate and bipolar gate driver were optimized for minimum harmonic distortion, acquisition time, and pedestal error. The open-loop hold amplifier was optimized for dc linearity, droop, and settling performance. To minimize technical risk, four versions of the S/H circuit were designed. The two baseline designs incorporate devices with a $7 \times 7 \mu\text{m}^2$ emitter geometry; one version utilizes a Schottky diode sampling gate and the other, bipolar diodes for the gate. The other two designs incorporate higher risk devices with a $5 \times 5 \mu\text{m}^2$ emitter geometry. Although the lower capacitance $5 \times 5 \mu\text{m}^2$ devices are higher risk, they are expected to produce a S/H design with enhanced dynamic performance.

The layout of the S/H circuits was completed in January. The S/H pad connections were arranged to simplify dynamic interfacing of the S/H circuit with the 5-bit ADC, and care was taken to minimize performance-degrading crosstalk between the sampling clock and the analog input signal. To facilitate dynamic optimization of the circuit, the hold capacitor was designed to be laser-trimmable.

In February, Hughes received copies of the composed mask set from TI that included the Hughes circuit designs and the TI process characterization test patterns. Tapes of both the fractured and nonfractured database were compared for accuracy. A few problems associated with the fidelity of the data transfer were identified and subsequently solved. Procedures concerning database formatting, conversion, editing, and transfer are being defined to eliminate further database problems.

Mid-quarter, the Hughes circuit design team developed a test strategy for the 5-bit ADC and high speed S/H circuits released for processing at the end of January. Both ICs will be screened at the wafer with in-house special test equipment. Next, a custom hybrid and support test fixture will be designed to dynamically characterize the fully functional ICs. The 5-bit ADC will be tested for functionality at the wafer level with an Advantest analog

IC test system. The fully modular test system includes key subelements such as a precision voltmeter, programmable high accuracy voltage source, 1.8 GHz signal generator, and 1.8 GHz spectrum analyzer. Through the use of custom software programs written by Hughes specifically for testing the ADC, all pertinent dc and ac parameters will be measured and recorded. These parameters include dc linearity, code monotonicity, latch operation, power supply current, input bias current, and output signal voltage levels. The S/H circuits will be tested initially at the wafer level with the Lomac test system. The Lomac system is well suited for dc wafer testing of the S/H circuit, since only minor modifications of an existing test program are required to fully characterize the new IC. This quarter, all the key hardware elements required for probe testing, including custom probe cards, were identified, designed, ordered, and received from the vendors. Custom probe software required to test the 5-bit ADC was completed this quarter. Probe software required for S/H wafer-level testing is 50% complete.

Design and layout of a custom thin-film hybrid for dynamic evaluation of the 5-bit ADC and S/H were completed. The custom hybrid, shown in Figure 3, integrated both the 5-bit ADC and the high speed S/H circuits, thereby facilitating complete dynamic evaluation of both components at the projected > 1 GHz clock rate. Reference amplifiers have been included in the hybrid design to accurately set the ADC gain and allow trimming of the ADC dc linearity for optimum performance. A custom high speed latch IC has been included in the hybrid design to facilitate data handling at the > 1 GHz rate.

V. DEVICE CHARACTERIZATION

Test devices were designed and included on the 5-bit test bar mask tester released in late January. The test structures were designed to provide complete modeling of the overgrowth HBT devices. Patterns were designed for accurate characterization of device parasitic capacitance and S-parameter f_T measurement. Single base, multiple base, and multiple emitter bipolar structures were designed. In addition, test patterns were included to evaluate adjacent pair V_{be} and β matching, critical to successful high resolution ADC design. A family of Schottky diodes and subsurface

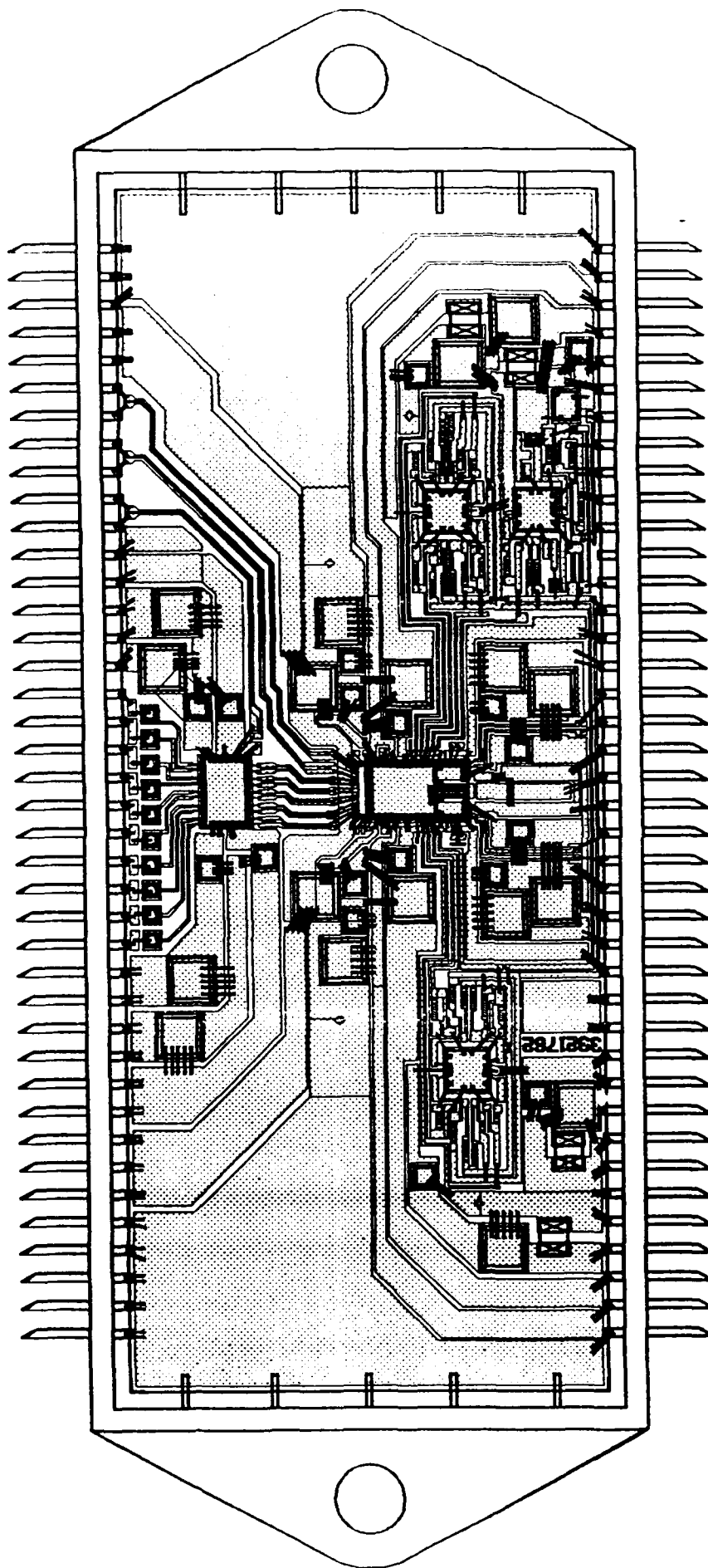


Figure 3. 5-bit ADC and S/H custom thin-film test hybrid.

zener structures was included for characterization. Resistor matching structures suitable for additional thermal dependence and resistor tracking measurement were included. The resistor patterns will also be used to study the effects of laser annealing as a means of trimming.

Thermal characterization of the 300 Ω /sq Cermet resistors was completed in January. Data were compiled from resist measurements at seven random die locations on a single wafer, and it was found that the Cermet material demonstrated an extremely linear thermal dependence of about +130 ppm/ $^{\circ}$ C (Figure 4). The measured wafer-wide spread in resistor value is on the order of 2%. This result includes the effects of contact, encroachment, and resistivity variations. A brief study of the resistor temperature tracking required for a high resolution ADC was completed. It is projected that for the accuracy-critical ADC application, the optimum resist is 150 Ω , 25 mils long and 50 mils wide (limited only by EM interference and area considerations). This would result in a noise error about one-third that of a 12-bit quantization error budget. Linearity error due to resistance variation under joule heating would be half that of the noise contribution.

The baseline Metal-1 to Metal-2 capacitor provides a capacitance per unit area of 0.057 fF/ μm^2 . At present, this is the only capacitor structure used in the 5-bit ADC and S/H circuitry. An alternative structure using the Ohmex and n^+ GaAs layers as plates can provide nearly four times the capacitance density because it has about half the dielectric depth, and nearly twice the dielectric constant (i.e., Si_3N_4 in lieu of SiO_2). The improved capacitor technology is required to reduce the die size of large capacitors. A test structure to fully evaluate this alternative capacitor structure has been included on the 5-bit ADC mask set.

The development of a laser trimming methodology for on-chip Cermet resistors began this quarter. Initial results indicate that resistor trimming through laser annealing is quite feasible. It was hoped that if a resistor temperature of approximately 450 $^{\circ}$ C could be maintained, the annealing technique would provide a nearly linear variation of resistance with time. However, since the actual temperature of the trimmed resistor is difficult to control, a nonlinear variation of resistance with time was

Normalized CERMET Resistance = F{Temperature}

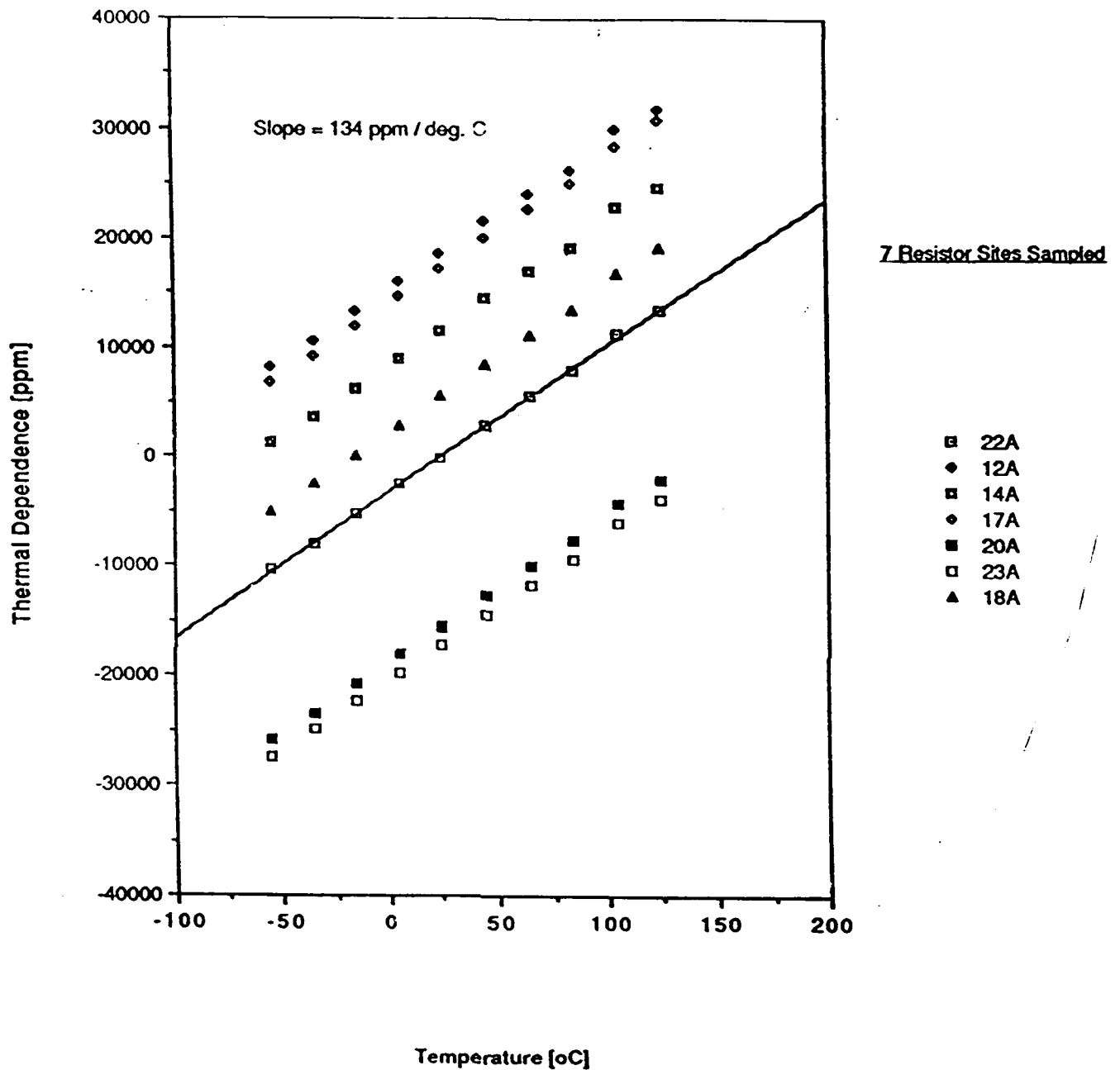


Figure 4. Cermet resistor temperature dependence.

found. The anneal tests were performed on a Florod Xenon laser station at Hughes. The width at half maximum power for the laser pulses is 1 mS, which corresponds approximately to the period of anneal. Unfortunately, continuous wave (cw) operation with the system used will damage the laser. Therefore, operating at 10 Hz, the anneal duty cycle is approximately 0.001%. Herein lies a difficulty. To obtain the desired 450°C anneal temperature, it could prove necessary to run the anneal for hundreds of hours on a single resistor. Clearly, such a requirement would be impractical. An alternative technique is to use higher power, annealing at a far faster rate per pulse. A number of data points have been compiled using a 10 μm laser spot size on 250 μm x 25 μm resistors. The results are shown in Figure 5. Here, on an uncalibrated but linear pulse energy scale, we see how a pulse energy of 150 brings an average variation of -0.6 m Ω /pulse. We also see that for a pulse energy of 175 (only a 17% increase) we have -400 m Ω /pulse. In comparison, TI processing data indicate we could expect on the order of only -0.2 m Ω /pulse change if the pulse provided a 450°C anneal temperature.

Even under these circumstances, laser anneal is still viable. However, a large resistor is required, so that a step-and-repeat annealing procedure could be followed. As seen from the nonlinearity of the Figure 5 curves, continuous anneal of the same spot will not yield a linear variation of resistance with the present laser configuration. It should be noted that variations in laser power during runtime of a 450°C cw laser technique may even render that approach nonviable, unless a step-and-repeat process is used.

Laser trimming has direct application to the proposed high-speed 8-bit ADC design. Trimming is desirable to improve transistor matching, which is critical to overall ADC linearity. High frequency requirements of the analog components in the 8-bit ADC restrict critical resistor size to approximately 30 μm x 10 μm . As this is about three spot sizes, a step-and-repeat technique is not practical. A trimming technique using smaller spot size with a longer series of low energy pulses will be investigated next quarter.

This quarter, a noise measurement box suitable for HBT measurement was designed and constructed. The noise test fixture demonstrates a 3 dB rolloff at 10 MHz, which is close to the 1/f corner expected theoretically.

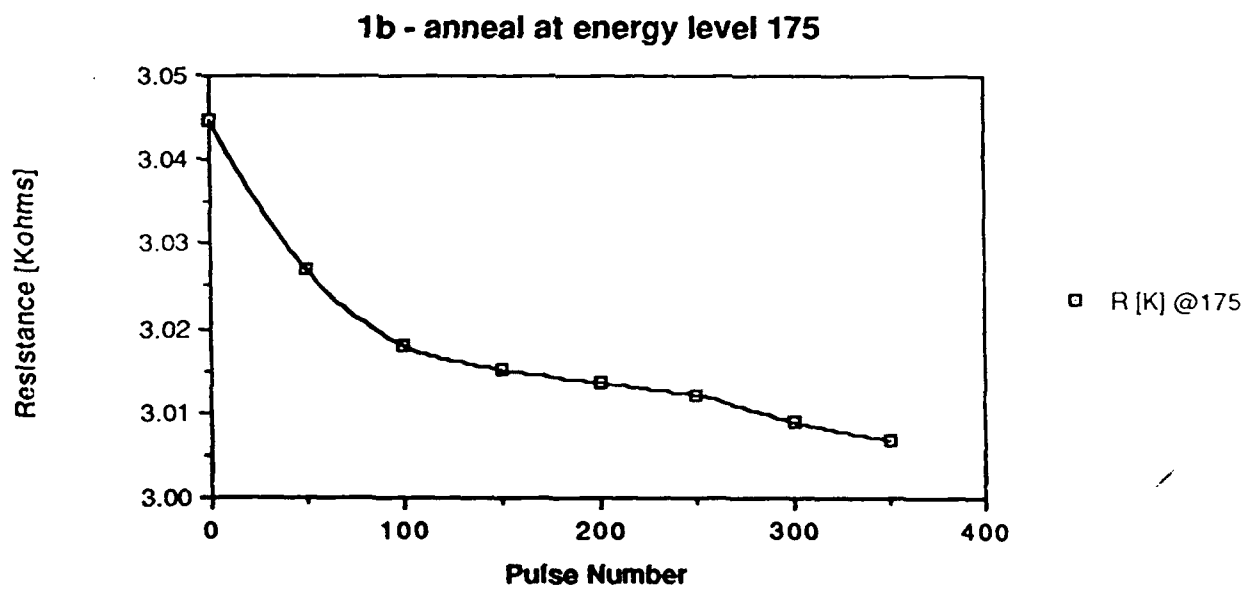
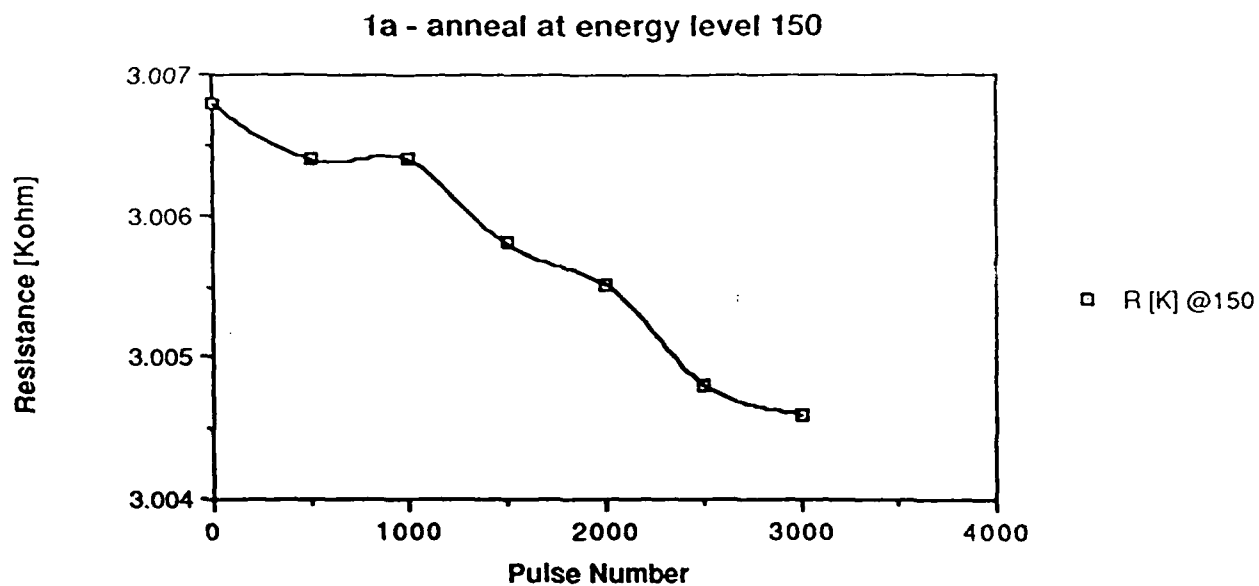


Figure 5. Preliminary Cermet resistor laser anneal results.

The corner frequency could be improved at the sacrifice of voltage gain, or the addition of an emitter-follower buffer stage prior to the output amplifier. Decreasing the voltage gains would make measurement more difficult, while addition of a buffer stage would create another noise source, thus complicating data analysis. Preliminary noise measurements will be performed on the test transistors on the 5-bit ADC mask set next quarter.

VI. PLANS FOR NEXT QUARTER

- (1) Investigate causes for low HBT current gains (10 - 20) and improve process to obtain gain > 50.
- (2) Complete fabrication of the custom thin-film test hybrid.
- (3) Complete the design of a dynamic test fixture required to evaluate the custom 5-bit ADC and S/H hybrid.
- (4) Complete wafer-level probe and dynamic evaluation of the 5-bit ADC and S/H circuits.
- (5) Begin detailed circuit design of the 8-bit ADC.
- (6) Provide a complete overgrowth model for both bipolar and Schottky structures based on measured data.
- (7) Continue laser annealing study. Determine the optimal technique for reliable and repeatable on-chip trimming.
- (8) Complete HBT $1/f$ noise analysis and measurement.
- (9) Complete HBT thermal resistance and V_{be} temperature dependence measurements.



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