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QUARTERLY REPORT NO 3
FOR
ANALOG-TO-DIGITAL CONVERTER
Contract No. N00014-87-C-0314
1 October 1987 - 31 December 1987

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I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high sampling rate A/D converter and a high resolution GaAs A/D converter.

B. Baseline Process Development

During the past quarter, a new baseline process was developed. Although HBTs had been successfully fabricated using our original base-implanted-through-the-emitter (BITE) process, the resulting base resistances were too large, and the Early voltages were far short of the design requirement of 50 V. The new baseline process, which utilizes two different epi deposition steps (overgrowth process), results in low base resistances and Early voltages that exceed our design requirement.

C. A/D Converter Circuit Design

The Hughes team has performed wafer-level measurements on the HBT wafers fabricated with both the original baseline process and the new overgrowth process. Test structures have been laid out by their design team and submitted to TI for inclusion in the second-pass process test bar. In addition, Hughes has begun a detailed design of the five-bit ADC as well as the sample-and-hold circuitry.

II. HETEROJUNCTION BIPOLAR PROCESS DEVELOPMENT

A. Baseline Process Development

After careful evaluation of eight lots of HBTs fabricated with the base-implanted-through-the-emitter (BITE) process, we have decided to replace this process with the "overgrowth" procedure. Although the BITE process resulted in HBTs with good gains, the resulting base resistances were too high, and

the Early voltages were too low. The overgrowth process had been scheduled to replace the BITE process early in 1988; however, based on our results for the BITE transistors and the positive results obtained using the overgrowth process, the transition was made during this quarter.

In the new baseline process the base layer is grown as part of the first epi, then selectively defined and etched before the emitter layer is grown. Three lots have been processed up through the ohmic metal process, which is the first point at which the transistors can be probed. The results were similar for all three lots. Two of the lots have been processed up to first metal. Figure 1 illustrates the output characteristics of a 7 x 7 μm^2 emitter transistor from one of these lots. It can be seen that the output characteristics are essentially parallel with the voltage axis, resulting in very high values for the Early voltage. The voltage gains varied from 5 to 20, depending on the operating points.

Seven additional lots are currently in process using this new baseline process. These lots are scheduled to be processed with all levels in order to evaluate the HECL circuits. The doping of the base level for several of these lots has been reduced from 1 x 10^{19} cm^{-3} for the three lots tested to date to 1 x 10^{18} cm^{-3}, as well as values between these extremes, to evaluate the trade-off between the Early voltage and the current gain. To optimize this process, the current gain must be increased to 50 and the emitter-base breakdown voltage must be increased. Lowering the base doping concentration from 1 x 10^{19} cm^{-3} should improve both of these parameters. In addition, the collector epi thickness has been increased and the doping decreased, which should give improved BV_{ceo} breakdown characteristics.

B. Back-up HBT Process

In addition to the overgrowth process described above, work is continuing on a second overgrowth approach that utilizes a base implanted prior to the second epi. This process, which has produced mixed results, was described in previous reports. This overgrowth process results in a more planar surface than the baseline process at the cost of higher base resistance. It represents our current back-up process and will continue to

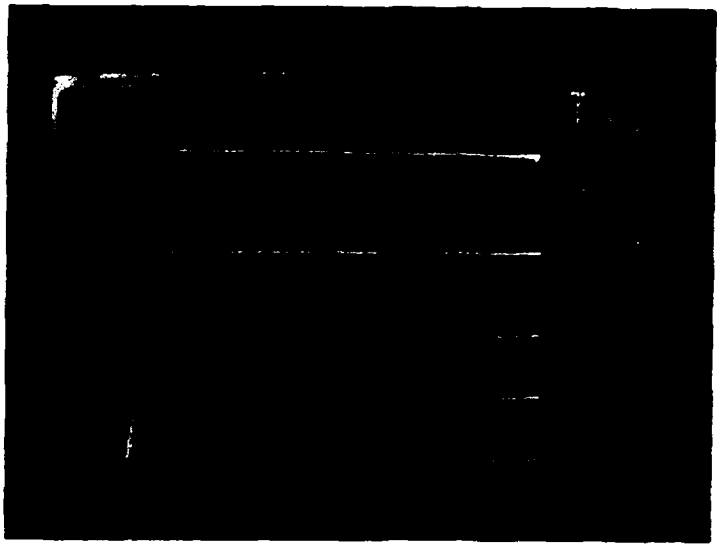

Figure 1. I-V characteristics for transistor fabricated using baseline process.

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be pursued at a reduced level of effort. Control of the base doping profile represents the major hurdle for this process. Results to date have ranged from transistors with current gains in excess of 1000 and low punchthrough voltage, to gains of 50 to 100 and reasonable punchthrough voltage. These latter transistors had Early voltages less than about 7 V resulting from low base doses. Different methods of increasing the base doping while maintaining a shallow reproducible base profile are under consideration. An attempt to use Zn implantation to obtain a shallow p-type base region resulted in poor Zn activation. A low energy Be implant, 5 to 10 keV, is desirable; however, it is difficult to maintain a good ion beam at such a low energy using our present ion source technology. Therefore, one of the molecular byproducts of our ion source, BeCl, will be used to effectively increase the mass of the Be ion from a shallow profile, similar to the use of BF_2^+ instead of B^+ for shallow boron implant profiles in the silicon IC technology.

Initial results indicate that BeCl implants result in less than half the junction depth of a Be implant at the same energy when implanted into semi-insulating GaAs. For example, at 170 keV the Be p-type active region extends to a depth of > 7000 Å, while BeCl gives a depth of only 3200 Å . For the npn HBT base a low energy, high dose implant is necessary. The BeCl complex at 30 keV and a fluence of $1 \times 10^{15}/cm^2$, implanted through 400 Å of nitride, resulted in ~ 1000 Å active region with a doping of ~ $1 \times 10^{18}/cm^3$. This is close to the HBT base doping requirement and will be pursued further.

C. Cermet Resistors

A lot composed of four GaAs wafers containing the Cermet resistor test patterns connected with first-level metal was shipped to Hughes for evaluation of the TCR. The devices were patterned using the ADC process test bar mask set. Initial measurements indicate that the TCR is less than 100 ppm/°C over the temperature range from 25 to 250°C. Only one test module in each bar contained resistor structures designed to be tested without additional circuitry. The first structure contains 25 µm to 2 µm wide resistors connected in series. The second structure is a 25 µm wide x 250 µm long Kelvin connected resistor.

The results of our multiprobe of 22 bars per wafer are given below.

Wafer No.		25 μm - 2 μm Resistors	Kelvin Connected Load Resistor
1	Mean	14116 ohms	3019 ohms
	Sigma	1035 ohms	49.2 ohms
	Sigma%	7.3%	1.6%
2	Mean	12245 ohms	2775 ohms
	Sigma	538 ohms	92.2 ohms
	Sigma%	4.4%	3.3%
3	Mean	14003 ohms	3062 ohms
	Sigma	601 ohms	71.7 ohms
	Sigma%	4.3%	2.3%
4	Mean	12938 ohms	3096 ohms
	Sigma	1276 ohms	43.7 ohms
	Sigma%	9.8%	1.4%

It can be seen that the resistance spreads for the Kelvin connected resistors are quite good, while the 25 resistors connected in series showed somewhat more spread. Both low TCR and the ability to laser-trim these resistors will be key to meeting the ADC requirements.

III. ANALOG-TO-DIGITAL CIRCUIT DEVELOPMENT

The first pass using the ADC process development mask set to build a circuit has resulted in a fully functional, 19-stage ring oscillator, 62 transistors (7 x 7 μm), with a propagation delay of 0.6 ns per gate. This circuit was fabricated in Lot 2627AB using the BITE process (base-implanted-through-the-emitter). The speed of this ring oscillator was limited by the RC response of the external circuitry and did not approach the transistor limiting frequency. The design of the ring oscillator was very conservative. Future designs will better test the limiting transistor speeds. The importance of this circuit was that it demonstrated for the first time our

fully integrated HECL planar technology, including trench isolation, the double-level metal process, and Cermet load resistors.

B. Device Characterization

Acting upon Hughes' request for higher Early and breakdown voltages, TI has made a successful jump to an overgrowth process. Though at present this process results in lower current gains, we anticipate that base profile adjustments will produce significant improvements. Hughes has received four half-wafers fabricated using the new baseline overgrowth process and has done some preliminary measurements that demonstrate lower emitter and collector resistances, current gains ranging from 1 to 20, and Early voltages in excess of 100 V. Improvements in the collector-emitter breakdown voltage, BV_{ceo}, to 7 to 10 V have also been noted, but there is some concern over the leakage current below breakdown for high accuracy circuits.

Hughes has prepared an updated model library for the overgrowth HBTs and a preliminary library for Schottky diodes based on earlier GaAs Schottky data provided by TI.

C. ADC Circuit Design

The Hughes circuit design team began detailed design of the five-bit ADC. Computer simulations of the input folding amplifier, interpolation ladder, and latching comparator were performed. In addition, cell layout of the folding amplifier and latching comparator were completed. Layout of the analog section of the IC is approximately 50% complete. The baseline design approach for the decode section of the five-bit ADC was chosen and dc circuit design initiated. Also, the detailed circuit design of a high speed sample-and-hold (S/H) circuit was begun. The S/H architecture selected employs a Schottky sampling gate and a unique bootstrapped hold amplifier. The S/H design is targeted to complement the five-bit ADC design.

To expedite layout of both the five-bit ADC and the S/H design, two custom layout tools were developed. A graphics program was written to automatically generate Cermet resistors, given user inputs of resistor value and desired width. In addition, a design rule check (DRC) program was

written to verify that the IC layout complies with the specified process design rules.

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