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13. ABSTRACT (Maximum 200 words) Issues related to designing configurable and fault-tolerant processor arrays such that even if some processors are faulty, a fault free array can be constructed using the healthy processors. The general models that have been explored consist of a set of identical processors embedded in a flexible interconnection structure that is configured in the form of a rectangular grid. In particular, models were studied that use multiple tracks along every grid line. Efficient scheduling algorithms were also developed for such processor arrays in the presence of communication delays.					
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Algorithms and Architectures for High Speed Signal Processing

FINAL REPORT

May 1, 1990 – April 30, 1993

by

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1 Introduction

This is the final report on our work under ARO-SDI Contract DAAL03-90-G-0108, May 1, 1990 through April 30, 1993.

The major results are in two areas:

1. Issues related to designing *configurable and fault-tolerant* processor arrays such that even if some processors are faulty, a fault free array can be constructed using the healthy processors. Such studies are motivated by applications of Wafer Scale Integration (WSI) where for example, a large number of processors, configured in the form of a square grid, can be put on a single wafer. Due to finite yield, some of the processors are likely to be faulty. In such a case, one can work around the faulty processors and reconfigure the remaining processors to form a healthy grid. Thus, reconfiguration methodologies can be viewed as tools to increase the effective yield of the WSI processing arrays. The general models that we have explored consist of a set of identical processors embedded in a flexible interconnection structure that is configured in the form of a *rectangular grid*. In particular, during this reporting period we studied models that use multiple tracks along every grid line and developed efficient algorithms for reconfiguration in such models. We have also developed efficient scheduling algorithms for such processor arrays in the presence of communication delays. Our results on this topic are summarized in Section 2.
2. Aspects of antenna array processing relating to methods for dealing with unknown or partially known noise field and the array manifold. Our approach to array processing problems such as directions-of-arrival (DOA) estimation has been based on the very successful *Subspace Method*. These methods however need explicit knowledge of the noise field and the array manifold. However, in many practical situations, this information may be unknown or only partially known and we have investigated several approaches to overcoming such limitations. In one approach, we used an instrumental variable method where the sample to sample temporal correlation of the signal is much larger than for the noise. Specifically, for a large enough differential delay, the covariance of the array outputs can show a finite signal component but has a zero contribution from noise. Thus the unknown noise covariance problem has been side stepped. We have provided a detailed analysis of this approach. Another area of investigation has

been the analysis of combined effects of finite samples and model errors on DOA estimation. This led to a doubly weighted subspace fitting approach where column weighting was used to optimize finite sample effects and row weighting for model errors. We also investigated techniques for incorporating prior knowledge of array response errors in the estimator using a *Bayesian approach* and an auto calibration procedure. The technique here is to allow the array response vectors to adapt to given data within the limits of the known error bounds on the array manifold. Our results on this topic are summarized in Section 3.

Two Ph.D. theses in these areas were completed during this contract and several papers published, accepted and submitted – see pp. 13.

2 Summary of Our Work on Reconfigurable Arrays

Many computations in matrix algebra can be conveniently carried out on an array of identical processing elements. WSI technology provides an inexpensive approach to building such arrays. However, during the fabrication process or during operation, some of the processing elements in a large array are inevitably going to be faulty. Spare PEs and extra routing hardware are often provided so that a fault-free array can be constructed; such reconfiguration capability can be used to increase the yield, and to guarantee fault tolerance in applications when failure is not permissible. Our work in this regard has been concerned with the design and analysis of such configurable fault-tolerant arrays and we have built on previous work within our group in this area. fault-tolerant arrays and we have built on previous work within our group in this area.

The general model considered by us is (see *e.g.* , [LSS89, Moo86, Ros83, SS86, SS82, Sny82]): it consists of a set of identical processors embedded in a flexible interconnection structure that is configured in the form of a rectangular grid. Each grid line in the mesh has a fixed number of data paths that can be routed along it (*i.e.* , the model has fixed channel width); switches can be placed at every grid point and at every location where a processor is connected to the grid. Furthermore, often the processors are divided into a set of non-spare PEs (say an $m \times n$ array) and a set of spare PEs that are distributed in a pre-determined fashion.

Given a set of faulty PEs, the objective is to reconfigure the connections

among the PEs such that a new rectangular *logical array* is formed comprising only the healthy PEs and demanding no more hardware resources (e.g., spare PEs, tracks, and switches) than available. It is clear that the more the additional hardware, the higher is the reconfiguration probability. Nevertheless, space and cost limitations place practical limitations on the amount of spare PEs, tracks and switches we can have. A question that now arises is: *Given a configurable architecture with fixed resources, are there efficient and simple algorithms for reconfiguring such architectures with high probability?*

It is also easy to see that if the number of faulty PEs is less than the number of spare PEs, then one can always define a set of compensation paths for successful reconfiguration. A compensation path is defined by the sequence of substitutions made to replace a faulty PE by a healthy one. However, the characteristics of the compensation paths (e.g., the geometrical distances between consecutive nodes, or the relative positions of the nodes in the grid) determine the amount of routing hardware needed to implement the necessary connections among the logical neighbors. It can be easily shown that if the number of routing tracks is fixed, then one cannot allow arbitrary sets of compensation paths. In other words, by limiting the hardware resources one limits the number of faulty patterns that one can reconfigure. *Hence, another natural question is how many tracks should one provide so as to allow a large enough class of compensation paths, and yet keep the hardware redundancy low.*

Yet another important question is: *given a network of healthy (reconfigured) processors and a task dependency graph with communication delays, what should be the schedule of the tasks so as to maximize performance.*

We summarize our answers to these questions/problems.

2.1 New Results

We developed reconfiguration techniques for a 3-track-1-spare model: this consists of a single row/column of spare PEs on the side of the array. There are three routing tracks running along the grid lines and multiple programmable switches placed at the intersections of the tracks. The faulty PEs are not assumed to be able to function as interconnection elements.

We developed a set of sufficient conditions for reconfiguration in our model. More precisely we proved that *if there exists a set of compensation paths subjected only to the constraints of continuity and nonintersection, then the 3-track-1-spare model can always accommodate such a set.* We must note here that the above result provides the first known theoretical

justification of the observations made by several researchers about the power of 3-track models (see [JLS88, YS89]).

We also developed *polynomial time algorithms* for determining such a set of continuous and non intersecting compensation paths (if it is possible to do so) for a given array with faulty PEs. If there is no such set of compensation of paths that covers all the faulty PEs, then the algorithm returns a set of paths to cover the maximum number of faulty PEs. Extensive simulations were carried out for the performance of our 3-track-1-spare model and we compared it to other reconfiguration models that use similar amount and kind of additional hardware. The results show that our model performs better than other models that use the same or greater hardware.

We also developed efficient algorithms for reconfiguration in a *neighborhood reconfiguration model* (see also [CF90, SS86]). In this model, the neighborhood reconfiguration consists of an $n \times k$ rectangular array with one column of spare PEs on one side. The routing hardware used for reconfiguration could either be a multiplexer based interconnection scheme or the routing is implemented by tracks and switches. The goal is to reconfigure the array *minimizing at the same time the geometric distances between logical neighbors* (i.e., PEs that are connected in the reconfigured array). This criterion is motivated by the fact that shorter interconnects reduce the communication delays among the PEs, and also might lead to less routing hardware. The algorithm that we present has 100% reconfiguration yield and performs provably better than other algorithms that use the same model (see for example [CF90, FR85]). We developed reconfiguration algorithms for the case of only one column of spare PEs along one side of the array. The algorithms are based on a simple procedure to reconfigure an $N \times (N + 1)$ array into an $(N + 1) \times N$ array and vice versa. We also derived time complexity of these new algorithms.

Finally we have new results on scheduling problems when there are communication delays in the routing network. The model that we consider consists of m identical processors $P_1, P_2, \dots, P_m$ where m is a parameter of the problem and bounded by a constant c . There exist n computational tasks $T_1, T_2, \dots, T_n$ that can be executed in any of the m available processors. There is a partial order among the tasks. This implies if $T_i \rightarrow T_j$ (i.e. T_j is dependent on T_i) then the computation of T_j in some processor P_j cannot start before task T_i is computed (say in processor P_i) and the results of this computation have been transmitted from processor P_i to processor P_j . The partial order among the tasks introduces a *precedence graph* associated with the scheduling problem. The tasks $\{T_i\}$ are the nodes of the graph and

we assume directed edges between the nodes $T_i \rightarrow T_j$ whenever there is a dependency between tasks T_i and T_j the way it is described above. We shall assume that the precedence graph is of the *out-forest* (or *in-forest*) form. All the tasks are of unit computational time, i.e. it takes one unit of time to compute any of the tasks $T_1, \dots, T_n$ in any of the processors $P_1, \dots, P_m$. The processors are fully connected, i.e. any processor can communicate with any other processor. Moreover, the computation of the tasks in the processors is independent of the communication among them. This implies that the processors can be running tasks at the same time that communication is taking place among them. The communication delay among any two processors takes unit time.

For such problems we have proved the following theorem:

Theorem *Given out-forest G , it can be determined in $O(n^{2m})$ time whether there exists a schedule for G of certain given length λ . If such a schedule exists then we can determine this schedule in $O(n^{2m})$ time.*

The analysis of In-forest precedence graph scheduling problem reduces to the Out-forest precedence graph scheduling problem by just inverting the direction of the dependencies between the tasks and then inverting the resulting optimal schedule. In the process of proving this theorem we developed efficient ways of transforming the given graphs that are subject to communication delays into *delay free* graphs that can be scheduled without taking into consideration communication delays between the processors, and whose optimal schedules *obey the precedence and communication delay constraints* of the original graph, and have *the same length* as the optimal schedule of the original graph. This allowed us to use dynamic programming to obtain polynomial time algorithms for computing the optimal schedule. Our algorithm is a generalization of the results presented in [DW85] for graphs with no communication delays.

Since the above work has resulted in one of the very few rigorous results on scheduling with communication delays, it has received considerable attention in the research community. For example, Prof. Eugene Lawler (of University of California at Berkeley) [Law93] has used some of the concepts first introduced in our work to design efficient polynomial time algorithms for determining *approximate* schedules; our algorithms on the other hand derive *optimal* schedules.

3 Summary of our Work in Array Processing

3.1 Introduction

In many practical signal processing problems, the objective is to estimate from noisy measurements a set of *constant* parameters upon which the underlying true signals depend. For example, estimating the directions-of-arrival (DOAs) of impinging wavefronts given the set of signals received at an antenna array is important in fields such as radar, sonar, electronic surveillance and seismic exploration. High resolution frequency estimation is important in numerous applications including Doppler radar and system identification. The quantities to be estimated are parameters (*e.g.*, DOAs of plane waves, cisoid frequencies) upon which the observations depend, and these parameters are assumed to be *constant* over the observation interval which is long enough to collect sufficient data to ensure parameter estimates of the desired accuracy.

There have been several approaches to such problems including the so-called Capon's maximum likelihood (ML) method [Cap69] and Burg's maximum entropy (ME) method [Bur75]. Though often successful and widely used, these methods have certain fundamental limitations (*esp.* bias and sensitivity in parameter estimates), largely because they use an incorrect model (*e.g.*, AR rather than special ARMA) of the measurements. Pisarenko [Pis73] was one of the first to exploit the structure of the data model, doing so in the context of estimation of parameters of cisoids in additive noise using a covariance approach. Schmidt [Sch79] and independently Bienvenu and Kopp [BK79] were the first to do this in the case of sensor arrays of arbitrary form. Schmidt, in particular, accomplished this by first deriving a complete geometric solution in the absence of noise, then cleverly extending the geometric concepts to obtain a *reasonable* approximate solution in the presence of noise. The resulting algorithm was called MUSIC (Multiple Signal Classification) and has been widely studied since its inception. The geometric concepts upon which MUSIC is founded form the basis for a much broader class of *subspace-based* algorithms and is the focus of this discussion.

Since the pioneering work of Schmidt, several new techniques based on the subspace approach have been developed. Notably, the ESPRIT technique (Estimation of Signal Parameters via Rotational Invariance Techniques) proposed by Paulraj, Roy and Kailath [PRK85], [PRK86], [RK89]. More recently, new results in multi-dimensional techniques such as the classical maximum likelihood method and Weighted-Subspace-Fitting (WSF) of

Ottersten and Kailath [VOK89] have attracted attention due to their potentially superior performance. In fact, an optimal choice of weighting can be shown to yield estimates that achieve the Cramer-Rao lower bound on the error variance [OVK92]. Techniques such as MUSIC, ESPRIT and WSF are collectively known as *subspace methods*. These methods assume that the noise field is spatially white and completely known to within a scale factor. Likewise, the response of the array to a wavefront from any given angle (also known as the *Array Manifold*) is also assumed to be known.

3.2 New Problem Areas

However there are in practice several situations where the above assumptions may not be true. Due to changes in weather, the surrounding environment, and antenna location, the response of the array may be significantly different than when it was last calibrated. Furthermore, the calibration measurements themselves are subject to gain and phase errors. For the case of analytically calibrated arrays of nominally identical, identically oriented elements, errors result since the elements are not really identical and their locations are not precisely known. Depending on the degree to which the actual antenna response differs from its nominal value, the algorithm performance may be significantly degraded. The requirement of known noise statistics is also difficult to satisfy in practice, since the surrounding environment and orientation of the array may be time-varying. In addition, one is often unable to account for the effect of unmodeled "noise" phenomena such as distributed sources, reverberation, noise due to the antenna platform, and undesirable channel crosstalk. Measurement of the noise statistics is complicated by the fact that there are often signals-of-interest observed along with the noise and interference. Because of these difficulties, it is often assumed by default that the noise field is isotropic, that it is independent from channel to channel, and that its power in each channel is equal. When the SNR is high, deviations of the noise from these assumptions are not critical since they contribute little to the array covariance. However, at low SNR, the degradation may be severe.

We briefly discuss below our results in handling cases where the above-mentioned assumptions of known array response and noise statistics is not correct. Earlier work has been previously reported in [Swi91], [Fri90], [SH91]. Several authors have also investigated DOA estimation algorithms that attempt to mitigate the effects of the antenna and noise model errors described above [PK85, PK86, PRSK86, FW88, WWL88, WF88, WOV91].

Main Results

A variety of models could be used to describe the perturbed array matrix. In practice, the response of a given sensor is typically known to within some tolerance in gain and phase that accounts for variations in the construction of the sensor and the conditions under which it is to operate. This tolerance may be specified as limits above and below some nominal response, or as an expected deviation around the nominal. Consequently, one might assume that $\tilde{\mathbf{A}}$ is specified in probabilistic terms (e.g., the mean and variance of the elements of $\tilde{\mathbf{A}}$ are assumed known), and that the sensor array is just one realization from the probability space of arrays. A particularly simple model of this type that has been widely used [Fri90, LV90, ZW88, Kur89] is to assume that the array response vectors are zero-mean, white, circular, and stationary: the errors are independent from sensor-to-sensor, its covariance is clearly diagonal. Off-diagonal terms indicate sensor-to-sensor correlations that result, for example, if there are uncalibrated mutual coupling effects, or if some sensors tend to perturb uniformly (such as identical or adjacent elements). We have derived [VS] exact expressions for the DOA estimation error covariance of several popular subspace based methods assuming the error model given above in the presence of finite data samples. In particular, this is done for a weighted version of MUSIC and subspace fitting algorithms using row and column weightings. An important outcome of our analysis is that, for a given error model, proper weightings lead to minimum variance DOA estimates.

Accurate signal parameter estimation from sensor array data is a problem which has received much attention in the last decade. A number of parametric estimation techniques have been proposed in the literature. In general, these methods require knowledge of the sensor-to-sensor correlation of the noise, which constitutes a significant drawback. This difficulty can be overcome only by introducing alternative assumptions that enable separating the signals from the noise. In some applications, the raw sensor outputs can be pre-processed so that the emitter signals are temporally correlated with correlation length longer than that of the noise. An *Instrumental Variable* (IV) approach can then be used for estimating the signal parameters without knowledge of the spatial color of the noise. We have developed [VSO93] a improved technique that can give significantly better performance.

As pointed earlier, the subspace methods require an exact characterization of the array, including knowledge of the sensor positions, sensor

gain/phase responses, mutual couplings, and receiver equipment effects. Unless all sensors are identical, this information must typically be obtained by experimental measurements (calibration). In practice, of course, all such information is inevitably subject to errors. Recently, several different methods have been proposed for alleviating the inherent sensitivity of parametric methods to such modeling errors. The technique proposed herein is related to the class of so-called auto-calibration procedures, but it is assumed that certain prior knowledge of the array response errors is available. This is a reasonable assumption in most applications, and it allows for more general perturbation models than does pure auto-calibration. The optimal maximum a posteriori (MAP) estimator for this problem has been formulated, and a computationally attractive large-sample approximation derived. We have shown [VS93] that our approach is statistically efficient, and verified this through computer simulation.

References

- [BK79] G. Bienvenu and L. Kopp. Principe de la goniometrie passive adaptive. In *Proc. 7^{eme} Colloque GRESIT*, pages 106/1-106/10, Nice, France, 1979.
- [Bur75] J. P. Burg. *Maximum Entropy Spectral Analysis*. PhD thesis, Stanford University, Stanford, CA., 1975.
- [Cap69] J. Capon. High resolution frequency wave number spectrum analysis. *Proc. IEEE*, 57:1408-1418, 1969.
- [CF90] M. Chean and J. A. B. Fortes. The full-use-of-suitable-spares (fuss) approach to hardware reconfiguration for fault-tolerant processor arrays. *IEEE Transactions on Computers*, 39:564-571, April 1990.
- [DW85] Danny Dolev and Manfred K. Warmuth. Profile scheduling of opposing forests and level orders. *SIAM Journal of Algorithms and Discrete Methods*, 6:87-92, October 1985.
- [FR85] J. A. B. Fortes and C. S. Raghavendra. Gracefully degradable processor arrays. *IEEE Transactions on Computers*, C-34, No. 11:1033-1044, Nov. 1985.

- [Fri90] B. Friedlander. A sensitivity analysis of the MUSIC algorithm. *IEEE Trans. on ASSP*, 38(10):1740-1751, October 1990.
- [FW88] B. Friedlander and A. J. Weiss. Eigenstructure methods for direction finding with sensor gain and phase uncertainties. In *Proc. ICASSP*, pages 2681-2684, 1988.
- [JLS88] L. Jervis, F. Lombardi, and D. Sciuto. Orthogonal mapping: A reconfiguration strategy for fault tolerant vlsi/wsi 2-d arrays. In *Proc. Int. Workshop on Defect and Fault Tolerance in VLSI Systems*, October 1988.
- [Kur89] A. R. Kuruc. Lower bounds on multiple-source direction finding in the presence of direction-dependent antenna-array-calibration errors. Technical Report TR-799, MIT Lincoln Laboratory, 1989.
- [Law93] E. Lawler. Scheduling trees on multiprocessors with unit delays. In *Workshop on Models and Algorithms for Planning and Scheduling Problems*. Villa Vigoni, Lake Como, Italy, June 14-18, 1993.
- [LSS89] F. Lombardi, M. G. Sami, and R. Stefanelli. Reconfiguration of VLSI arrays by covering. *IEEE Trans. on CAD of IC and Systems*, 8, No. 9:952-965, Sept. 1989.
- [LV90] F. Li and R. Vaccaro. Statistical comparison of subspace based DOA estimation algorithms in the presence of sensor errors. In *Proc. 5th ASSP Spectral Estimation Workshop*, pages 327-331, Rochester, NY, October 1990.
- [Moo86] W. R. Moore. A review of fault-tolerant techniques for the enhancement of integrated circuit yield. *Proc. IEEE*, (5):684-698, May 1986.
- [OVK92] B. Ottersten, M. Viberg, and T. Kailath. Analysis of subspace fitting and ML techniques for parameter estimation from sensor array data. *IEEE Trans. on SP*, SP-40, March 1992.
- [Pis73] V. F. Pisarenko. The retrieval of harmonics from a covariance function. *Geophys. J. Royal Astronomical Soc.*, 33:347-366, 1973.

- [PK85] A. Paulraj and T. Kailath. Direction-of-arrival estimation by eigenstructure methods with unknown sensor gain and phase. In *Proc. IEEE ICASSP*, pages 17.7.1-17.7.4, Tampa, Fla., March 1985.
- [PK86] A. Paulraj and T. Kailath. Eigenstructure methods for direction of arrival estimation in the presence of unknown noise fields. *IEEE Trans. on ASSP*, 34(1):13-20, February 1986.
- [PRK85] A. Paulraj, R. Roy, and T. Kailath. Estimation of Signal Parameters via Rotational Invariance Techniques - ESPRIT. In *Proc. Nineteenth Asilomar Conf. on Circuits, Systems and Comp.*, San Jose, CA, November 1985. Maple Press.
- [PRK86] A. Paulraj, R. Roy, and T. Kailath. A subspace rotation approach to signal parameter estimation. *Proceedings of the IEEE*, 74(7):1044-1045, July 1986.
- [PRSK86] A. Paulraj, V. U. Reddy, T. J. Shan, and T. Kailath. A subspace approach to determine sensor gain and phase with applications to array processing. In *Proc. 30th SPIE International Technical Symposium, Advanced Algorithms and Architectures for Signal Processing*, San Diego, CA., August 1986.
- [RK89] R. Roy and T. Kailath. ESPRIT - Estimation of Signal Parameters via Rotational Invariance Techniques. *IEEE Trans. on ASSP*, 37(7):984-995, July 1989.
- [Ros83] A. L. Rosenberg. The Diogenes approach to testable fault-tolerant array of processors. *IEEE Trans. on Computers*, pages 902-910, Oct. 1983.
- [Sch79] R. O. Schmidt. Multiple emitter location and signal parameter estimation. In *Proc. RADC Spectrum Estimation Workshop*, pages 243-258, Griffiss AFB, N.Y., 1979.
- [SH91] V. C. Soon and Y. F. Huang. An analysis of ESPRIT under random sensor uncertainties. *IEEE Trans. on ASSP (in review)*, 1991.
- [Sny82] L. Snyder. Introduction to the configurable, highly parallel computer. *IEEE Trans. on Computers*, 15:47-56, Jan. 1982.

- [SS82] D. P. Siewiorek and R. S. Swarz. *The Theory and Practice of Reliable System Design*. Digital Press, 1982.
- [SS86] M. Sami and R. Stefanelli. Reconfigurable architectures for VLSI processing arrays. *Proc. of the IEEE*, pages 712-722, May 1986.
- [Swi91] A. Swindlehurst. *Applications of Subspace Fitting to Estimation and Identification*. PhD thesis, Stanford University, Stanford, CA., 1991.
- [VOK89] M. Viberg, B. Ottersten, and T. Kailath. Direction of arrival estimation and detection using weighted subspace fitting. In *Proc. 23rd Asilomar Conference of Signals, Systems, and Computers*, San Jose, CA, November 1989. Maple Press.
- [VS] M. Viberg and A.L. Swindlehurst. Analysis of the combined effects of finite samples and model errors on array processing performance. In *Proc. of the Int'l. Conf. on Acoustics, Speech, Signal Processing*. Minneapolis, MN, April 1993.
- [VS93] M. Viberg and A. Swindlehurst. A bayesian approach to auto-calibration for parametric array signal processing. submitted to *IEEE Trans. Signal Processing*, 1993.
- [VSO93] M. Viberg, P. Stoica, and B. Ottersten. Array processing in correlated noise fields based on instrumental variables and subspace fitting. submitted to *IEEE Trans. Signal Processing*, 1993.
- [WF88] A. J. Weiss and B. Friedlander. Direction finding in the presence of mutual coupling. In *Proc. 22nd Asilomar Conf. on Signals, Systems, and Computers*, pages 598-602, 1988.
- [WOV91] B. Wahlberg, B. Ottersten, and M. Viberg. Robust signal parameter estimation in the presence of array perturbations. In *Proc. IEEE ICASSP*, pages 3277-3280, Toronto, Canada, 1991.
- [WWL88] A. J. Weiss, A. S. Willsky, and B. C. Levy. Eigenstructure approach for array processing with unknown intensity coefficients. *IEEE Trans. ASSP*, 36(10):1613-1617, October 1988.
- [YS89] H. Y. Youn and A. D. Singh. Bounded Channel Width Restructuring Algorithm for VLSI/WSI Arrays With Channel Faults.

Presented at HFTM, June 1989, University of Illinois, Urbana, IL, USA., June 1989.

- [ZW88] J. X. Zhu and H. Wang. Effects of sensor position and pattern perturbations on CRLB for direction finding of multiple narrow-band sources. In *Proc. 4th ASSP Workshop on Spectral Estimation and Modeling*, pages 98–102, Minneapolis, MN, August 1988.

ARO-IST/SDI Supported Publications
May 1, 1990 - April 30, 1993

Published Journal Papers

- [1] V.P. Roychowdhury, J. Bruck, and T. Kailath, Efficient Algorithms for Reconfiguration in VLSI/WSI Arrays, *IEEE Trans. Comput.*, 39(4):480-489, April 1990.
- [2] J. Chun and T. Kailath, Displacement Structure for Hankel, Vandermonde and Related (Derived) Matrices, *Signal Processing and Mathematics*, ed. L. Auslander, T. Kailath and S. Mitter, pp. 37-58, Springer-Verlag, New York, 1990.
- [3] A. Swindlehurst and T. Kailath, On the Sensitivity of the ESPRIT Algorithm to Non-Identical Subarrays, *Sadhana J.*, 15(3):197-212, November 1990.
- [4] J. Chun and T. Kailath, Divide-and-Conquer Solutions of Least-Squares Problems for Matrices with Displacement Structure, *SIAM J. Matrix Anal. and Appl.*, 12(1):128-145, Jan. 1991.
- [5] O. Farotimi, A. Dembo, and T. Kailath, A General Weight Matrix Formulation Using Optimal Control, *IEEE Trans. Neural Networks*, 2(3):378-394, May 1991.
- [6] J. Chun and T. Kailath, Displacement Structure for Hankel, Vandermonde and Related (Derived) Matrices, *Linear Algebra Appl.*, 151:199-227, June 1991.
- [7] J. Bruck and V. P. Roychowdhury, How to Play Bowling in Parallel on the Grid?, *J. Algorithms*, 12:516-529, Sept. 1991.
- [8] H. V. Jagadish and T. Kailath, Obtaining Schedules for Digital Systems, *IEEE Trans. Acoustics, Speech, Signal Process.*, 39(10):2296-2316, Oct. 1991.
- [9] T. Varvarigou, V. P. Roychowdhury, and T. Kailath, New Algorithms for Reconfiguring VLSI/WSI Arrays, *J. VLSI Signal Process.*, 3(4):329-344, Oct. 1991.
- [10] A. Dembo, T. Cover, and J. Thomas, Information Theoretic Inequalities, *IEEE Trans. Information Theory*, 37(6):1501-1518, Nov. 1991.
- [11] K-Y. Siu, V. Roychowdhury, and T. Kailath, Depth-Size Tradeoffs for Neural Computation, *IEEE Trans. Computers*, 40(12):1402-1412, Dec. 1991.
- [12] J. Chun and T. Kailath, Systolic Array Implementation of the Square Root Chandrasekhar Filter, *Int'l. J. Control*, 54(6):1385-1398, Dec. 1991.
- [13] R. Roy, B. Ottersten, L. Swindlehurst and T. Kailath, Multiple Invariance ESPRIT *IEEE Trans. Acoustics, Speech, Signal Processing*, 40(4):867-881, April 1992.
- [14] A. Swindlehurst and T. Kailath, A Performance Analysis of Subspace-Based Methods in the Presence of Model Errors, Pt. I: The MUSIC Algorithm, *IEEE Trans. Acoustics, Speech, Signal Processing*, 40(7):1758-1774, July 1992.
- [15] T. Varvarigou, V. P. Roychowdhury, and T. Kailath, A Polynomial Time Algorithm for Reconfiguring Multiple-Track Models, *IEEE Trans. Computers*, 42(4):385-395, April 1993.

Papers Accepted for Publication

- [1] A. Swindlehurst and T. Kailath, Azimuth/Elevation Direction Finding Using Regular Array Geometries, *IEEE Trans. Aerospace Electron. Systems*, Jan. 1993.
- [2] A. Swindlehurst and T. Kailath, A Performance Analysis of Subspace-Based Methods in the Presence of Model Errors, Pt. II: The MUSIC Algorithm, *IEEE Trans. Acoustics, Speech, Signal Process.*, Sept. 1993.
- [3] T. Kailath and J. Chun, Generalized Displacement Structure for Block-Toeplitz, Toeplitz-Block, and Toeplitz-Derived Matrices, *SIAM J. Matrix Anal. and Appl.*
- [4] D. Pal and T. Kailath, Fast Triangular Factorization and Inversion of Hermitian Toeplitz and Related Matrices with Arbitrary Rank Profile, *SIAM J. Matrix Anal. Appl.*
- [5] D. Pal, Gohberg-Semencul Type Formulas via Embedding of Lyapunov Equations, *IEEE Trans. Acoustics, Speech, Signal Process.*
- [6] V. Roychowdhury, K-Y. Siu, A. Orlitsky, and T. Kailath, A Geometric Approach to Threshold Circuit Complexity, *Information & Computation*
- [7] T. Varvarigou, V. Roychowdhury, and T. Kailath, Reconfiguring Processor Arrays using Multiple-Track Models, *IEEE Trans. Communication*
- [8] M. Genossar, H. Lev-Ari, and T. Kailath, Consistent Estimation of Cyclic Autocorrelation, *IEEE Trans. Acoustics, Speech, Signal Process.*, to appear March 1994.
- [9] D. Pal and T. Kailath, A Fast Matrix Factorization Approach Towards the Singular Cases of Tabular Form Root Distribution Procedures: The Imaginary Axis Case, *IEEE Trans. Circuits and Systems*.
- [10] D. Pal and T. Kailath, Displacement Structure Approach to Singular Root Distribution Problems: The Unit Circle Case, *IEEE Trans. Automatic Control*.
- [11] K-Y. Siu, V. Roychowdhury, and T. Kailath, Computing with Almost Optimal Size Neural Networks, *IEEE Trans. Info. Theory*.
- [12] T. Varvarigou, V. Roychowdhury, and T. Kailath, Scheduling In and Out Forests in the Presence of Communication Delays, *IEEE Trans. Parallel Computation*.

Papers Submitted for Publication

- [1] M. Viberg and A.L. Swindlehurst, Analysis of the Combined Effects of Finite Samples and Model Errors on Array Processing Performance, *IEEE Trans. Signal Processing*.
- [2] M. Viberg, P. Stoica, and B. Ottersten, Array Processing in Correlated Noise Fields Based on Instrumental Variables and Subspace Fitting, *IEEE Trans. Signal Processing*.

Conference Papers

- [1] T. Varvarigou, V. P. Roychowdhury, and T. Kailath, Some New Algorithms for Reconfiguring VLSI/WSI Arrays, Proc. Int'l. Conf. on Wafer Scale Integration, pp. 229-235, San Francisco, CA, Jan. 1990.
- [2] D. Pal and T. Kailath, A Generalization of the Schur-Cohn Test: The Singular Case, Proc. 33rd Midwest Symposium on Circuits and Systems, Canada, Aug. 1990.

- [3] D. Pal and T. Kailath, Approximate AR Modeling: A Schur Approach, Proc. 5th ASSP Workshop on Spectrum Estimation and Modeling, Rochester, NY, Oct. 1990.
- [4] T. Varvarigou, V. P. Roychowdhury, and T. Kailath, Reconfiguring Processor Arrays Using Multiple-Track Models, Proc. Int'l. Conf. on Wafer Scale Integration, San Francisco, CA, Jan. 1991.
- [5] K-Y. Siu, V. Roychowdhury, and T. Kailath, Computing With Almost Optimal Size Threshold Circuits, Int'l. Symp. on Information Theory, Budapest, Hungary, June 1991.
- [6] K-Y. Siu, V. Roychowdhury, and T. Kailath, Circuit Complexity for Neural Computation, Proc. 25th Annual Asilomar Conf. on Signals, Systems and Computers, Pacific Grove, CA, Nov. 1991.
- [7] D. Pal and T. Kailath, A Systematic Generalization of the Schur-Cohn Procedure for Root Localization with Respect to the Unit Circle: The Singular Cases, Symp. on Fundamentals of Discrete-Time Systems, Chicago, IL, June 1992.
- [8] K.Y. Siu, V. Roychowdhury, and T. Kailath, On the Complexity of Neural Networks with Sigmoidal Units, IEEE Workshop on Neural Networks for Signal Processing, Copenhagen, Denmark, Aug. 1992.
- [9] B. Khalaj, A. Sayed, and T. Kailath, A Unified Derivation of Square-Root Multichannel Least-Squares Filtering Algorithms, Int'l. Conf. on Acoustics, Speech, Signal Processing, Minneapolis, MN, April 1993.
- [10] M. Viberg, A.L. Swindlehurst, Analysis of the Combined Effects of Finite Samples and Model Errors on Array Processing Performance, Int'l. Conf. on Acoustics, Speech, Signal Processing, Minneapolis, MN, April 1993.

Theses

- [1] D. Pal, Fast Algorithms for Structured Matrices with Arbitrary Rank Profile Ph.D. Dissertation, Stanford University, Stanford, CA, May 1990.
- [2] T. Varvarigou, Fault Tolerance and Scheduling Issues in Multiprocessor Systems, Ph.D. Dissertation, Stanford University, Stanford, CA, December 1991.
- [3] M. Genossar, Spectral Characterizations of Nonstationary Processes, Ph.D. Dissertation, Stanford University, Stanford, CA, April 1992.

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