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ARMSTRONG LABORATORY

MINIATURE COLOR DISPLAY PHASE IV FINAL REPORT

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MAY 1993

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FOR THE COMMANDER

Kenneth R Boff

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May 1993 FINAL (October 1, 1992-May 31, 1993)

Miniature Color display
Phase IV Final Report

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A 400 x 300-pixel miniature color display with a resolution of 300 pixels/inch, yielding a 1.3 x 1.0-inch active area, has been demonstrated for helmet-mount applications. The display uses active-matrix subtractive-crystal technology. This approach produces high luminance and full color at each pixel without the loss in addressable resolution that is associated with conventional additive-color displays. A stack of three active-matrix twisted-nematic liquid-crystal light valves, sandwiching cyan, magenta, and yellow color polarizers, is used to generate full color. By spectral tuning of the xenon arc-lamp backlight and the color polarizers, a color gamut comparable to that of a shadowmask color CRT is achieved. Four bits of grayscale are provided for each of the three color primaries, yielding a total availability of 4096 colors. the display produces a peak white luminance of 3500 fL and has an inherent (i.e., dark-field) contrast ratio of 50:1. The preceding figures are sufficient to achieve a 2:1 contrast ratio against a 10,000 fL ambient scene, using typical helmet-mounted display optics. The display refresh rate is 68 Hz.

Liquid-crystal, display color, miniature, helmet-mounted

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Section I
Introduction and Summary

1.1 Background

The Miniature Color Display (MCD) Program is a four phase program. In the first phase we conducted research in design to verify concept feasibility, predict performance and specify design parameters, for the miniature subtractive color display. In Phase II, we fabricated a brassboard device that was used in Phase III to resolve problems and design issues. Phase IV involved fabricating, testing and delivering five demonstrator miniature color displays. This report is the final report for Phase IV activities.

Our effort during the fourth phase was to complete fabrication of active matrix substrates and subtractive color display panels. These subtractive color display panels (cyan, magenta and yellow) were then fabricated into subtractive color stack assemblies which were assembled into the MCD demonstrators. Each demonstrator was tested for performance. The five demonstrators, lamp and controller electronics were delivered to Armstrong Lab, Dayton, Ohio May 14, 1993.

The MCD Final Review and Demonstration of the subtractive color MCD image sources is scheduled for May 25, 1993, and is to held at Armstrong Lab, WPAFB, Ohio.

The Miniature Color Display program is now successfully completed.

1.2 Phase IV Accomplishments

1.2.1 Subtractive Color Gamut

Our original goal was to evaluate the color gamut achievable with the best dichroic dyes in a subtractive color stack of anti-parallel aligned guest host displays and neutral density polarizers. In a short time period we evaluated a twisted nematic guest host stack with color polarizers, and a promising color gamut with a test cell was achieved. The guest host approach (dichroic dyes in liquid crystals) was abandoned due to a slow electro-optic response time, high operating voltages, and low bulk resistivity of the dyed liquid crystal which caused a low RC time constant inadequate for 60 hz TFT driving. Early on in the program we began developing a subtractive color gamut utilizing dichroic color polarizers as the only color elements, and undyed twisted nematic liquid crystals (TFT grade liquid crystal) as the optical switching elements. In a subtractive color stack of single pixel test cells, backlighted with a notch filtered 300 watt xenon arc lamp we achieved a broad color gamut comparable to a CRT with a 50:1 dark state contrast ratio. With this technology and a 300 lpi aperture patterned subtractive color test cell we also achieved in addition to the reported color gamut and contrast, 3500 fL white, yielding calculated compliance with the required 2:1 contrast ratio at 10,000 fC forward scene ambient.

1.2.2 Gray-Scale Algorithm

The purpose of the gray-scale algorithm is to determine the cyan, magenta, and yellow display drive voltages necessary to obtain target Lu'v' coordinates. Initially, a Newton-type minimization method was implemented. At that time, the stack was constructed using guest host materials. Overall transmittance of the stack could be determined by the product of the individual and independent displays.

After converting to non-dichroic materials, we determined that a Jones matrix characterization of the stack was necessary if numerical optimization algorithms are to be used. To avoid measurement and modeling errors, we successfully implemented a straightforward approach in which the stack is directly measured at all possible combinations of a predetermined set of display voltages. These measurements result in a table of applied voltages and the resulting Lu'v' coordinates. To obtain a desired Lu'v' output, the drive voltages associated with the closest Lu'v' match found in the table are used.

1.2.3 Active Matrix Liquid Crystal Display

Fabrication and assembly of the five subtractive color demonstrators was the major accomplishment of this program. This was the direct product of the results achieved during the earlier phases.

Phase I concentrated on the design and fabrication of the AMLCD substrates. Although this critical phase of the program was delayed three months, we accelerated our efforts and completed this on schedule. The a:Si fabrication process was re-established by fabricating thin film transistors. These devices were subsequently characterized. Results of these measurements demonstrated that the 'on' currents, or 'drive' currents, exceeded design requirements by a factor of two. Further, the 'off' currents, or 'leakage' currents, are consistently less than 10pa. Both of these values are consistent with successful operation of AMLC displays.

Phase II was concerned with the fabrication and assembly of functional AMLCD panels. The first panel assembled and tested was for the color magenta. This panel was demonstrated during the CDR in May 1992. After successfully fabricating one panel, the next objective was to assemble the first subtractive color stack. This was accomplished during Phase III of the program.

This first fully functional subtractive color display was demonstrated at the final design review (FDR) in November 1992. The design was frozen at that time. Any further enhancements to the display's performance would be accomplished with subtle modifications to the substrate fabrication process.

Finally, once the functionality of the first subtractive color stack was demonstrated, the final phase of this contract could begin. The completion of the four remaining deliverable units was accomplished during Phase IV of the contract.

1.2.4 Drivers and Interconnect

Column drivers meeting the MCD voltage range and 16 grey-level requirements had to be identified and purchased. This proved a very difficult undertaking as almost all such drivers are used only in Japan are not available in the US due to various trade restrictions. However, prototypes of new column driver jointly developed by Honeywell and AMI/Gould became available in time for use on the MCD program. This device meets and exceeds the MCD electrical requirements.

A readily available row driver from OKI was used. No acquisition problems were incurred with this part. However, to be compatible with the AMI/Gould column driver, additional circuitry was required in the interface between the PC and the MCD display.

A flexible interconnect solution was developed to connect the row and column drive signals to the display glass. This interconnect, obtained from ElForm, has high resolution, low resistance conductor runs that are very thin and flexible.

1.2.5 Controller Electronics

To test and demonstrate the MCD, a flexible electronic interface was designed and constructed. A custom solution was required due to the non-standard resolution of 400 x 300 of the MCD, as well as the need to drive the three separate panels comprising the subtractive color stack. This custom electronics system used commercially off-the-shelf parts were possible including a IBM PC clone for the "host" and a Texas Instruments card for the graphics generator. The resulting system allow the display of arbitrary test patterns containing up to 256 simultaneous colors out of a palette of 4096 colors.

1.2.6 Illuminator

By using yellow and cyan notch filters and a xenon arc lamp illuminator, we have been able to achieve a useful color gamut and satisfy the 0.33 luminance requirement.

1.3 Summary

All activities and tasks associated with Phase IV have been completed. This completes the Miniature Color Display Contract.

Section II
Technical Achievements

2.1 Subtractive Color Gamut

2.1.1 Sub Color LC Technology

Our base technology for subtractive color is twisted nematic liquid crystal displays (TNLCD) utilizing only color polarizers as the subtractive color element. Color polarizers linearly polarize light. Unlike a neutral density polarizer which polarizes the entire visible spectrum, a color polarizer polarizes an isolated region of the spectra to yield it's characteristic color. As such, the magenta TNLCD modulates green light, the cyan TNLCD modulates red light, and the yellow TNLCD modulates the blue portion of the visible spectra. In the ideal case the color polarizers only polarize their assigned wavelengths of the visible spectrum. The light filtering characteristics of an ideal subtractive color polarizer is shown in Figure 1 for a cyan polarizer for the crossed, and the parallel polarizer conditions. A truth table, tracking the polarization states the development of colors through a subtractive color TNLCD stack utilizing cyan, magenta and yellow polarizers, is shown in Figure 2.

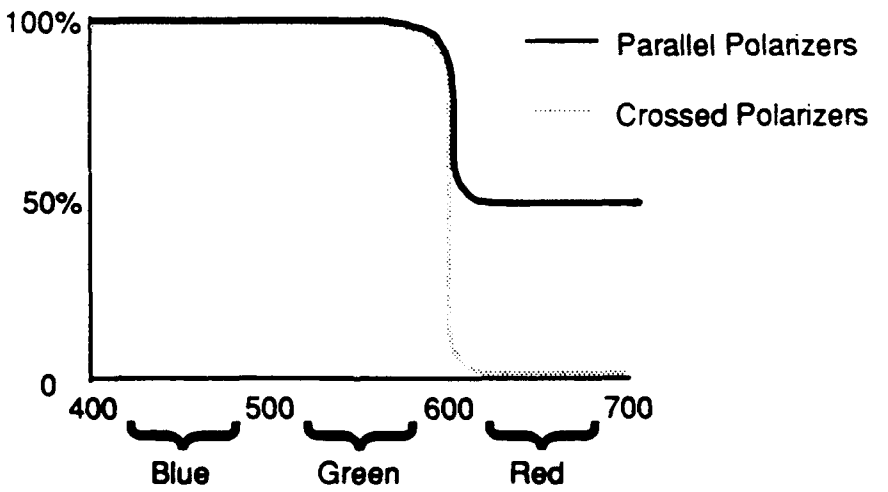
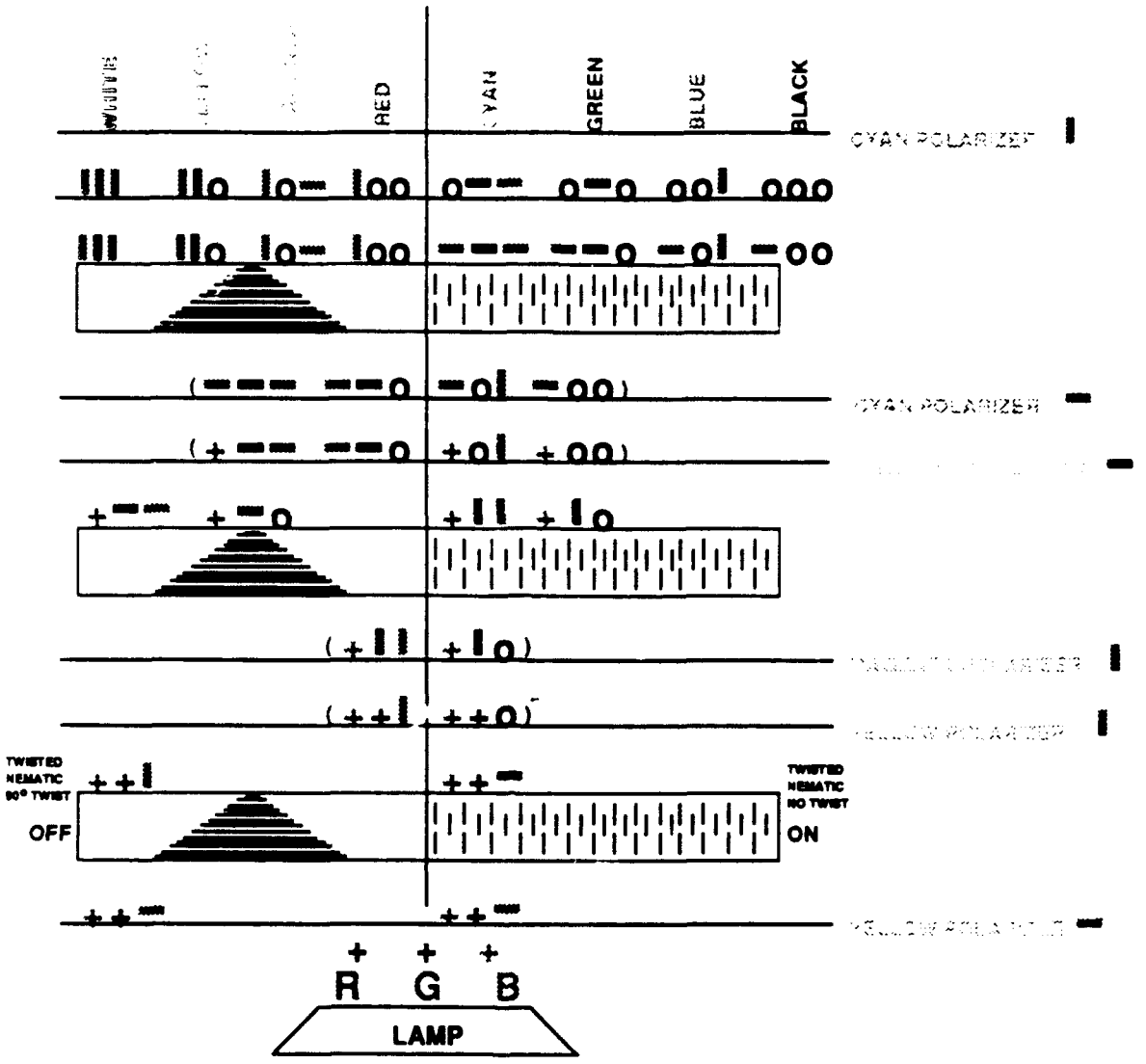


Figure 1. Light Filtering Characteristics of Ideal Cyan Polarizer for Crossed and Parallel Orientations that the Twisted Nematic Light Valve Modulates Between



Truth Table for a three cell twisted nematic subtractive color assembly utilizing yellow, magenta, and cyan color polarizers. The diagram tracks polarized light orientation for development of colors through a single stacked pixel. Crossed lines (+) indicate unpolarized light. (−) indicates x polarized light, (|) indicates y polarized light. Twisted nematic rotates polarization 90 degrees | → −, −→ | in twisted off-state. In no twist on-state, polarization orientation is maintained | → |, − → −. The order of colors in each subgrouping is RGB. Yellow polarizers polarize blue light RGB +++ → RGB ++−, or ++ − depending on polarizer orientation. Magenta and cyan polarizers polarize green and red light respectively transmitting x or y polarized light − or | depending on polarizer orientation. O represents no light. For example, yellow light is RGO or | | O, magenta is ROB or | O−. Yellow, magenta and cyan polarizers are oriented crossed for a transmissive (twisted off state), i.e., the output polarization from the input polarizers is rotated 90 degrees so that it is passed by the exit polarizer.

Figure 2. Truth Table

2.1.2 Illumination System

A 300 watt xenon arc lamp was selected as the illumination source, due to it's ability to satisfy the very high (exceeding 2500 fL) luminance output requirement of the subtractive color display system, for viewing under 10,000 fC of ambient background illumination. The lamp was filtered with notch filters to remove cyan and yellow wavelengths such that discreet red, green and blue (RGB) wavelength regions pass through the subtractive color light valve stack. The RGB tuned lamp increases the color separation efficiency of non ideal polarizers. The lamp peaks are tailored such that an isolated peak makes a saturated color. The RGB lamp peaks were tailored to effect a broad color gamut close to the NTSC standard when they are effectively separated by the TNLCD utilizing color polarizers. The Spectra of the notch filter tuned lamp is shown in Section 2.6 Figure 13.

2.1.3 Color Polarizers

Color polarizers are commercially available, as cyan, magenta, yellow, red, green, and blue polarizers. The polarizing activity of these polarizers is far from ideal. They transmit unequal portions of the colors they are supposed to transmit, and they transmit substantial quantities of the colors they are supposed to block. When these polarizers are utilized solely in a twisted nematic subtractive color stack, a much less than optimal color gamut results, even when the RGB tuned lamp is employed. To correct this problem, we developed color LC polarizing filters with dichroic dyes to correct these deficiencies.

These dichroic liquid crystal polarizers complement the sheet polarizers. A synergistic tuning of the polarizers and the lamp spectra decreased extraneous undesired wavelengths during color selection which greatly increased color purity, color saturation, and contrast ratio. An expanded view of the optimized subtractive color light valve (Assembly D) is shown in Figure 3. The effect of the polarizer and lamp improvements are shown in the color gamuts of Figure 4, and in the spectra for red, blue and black select in Figure 5.

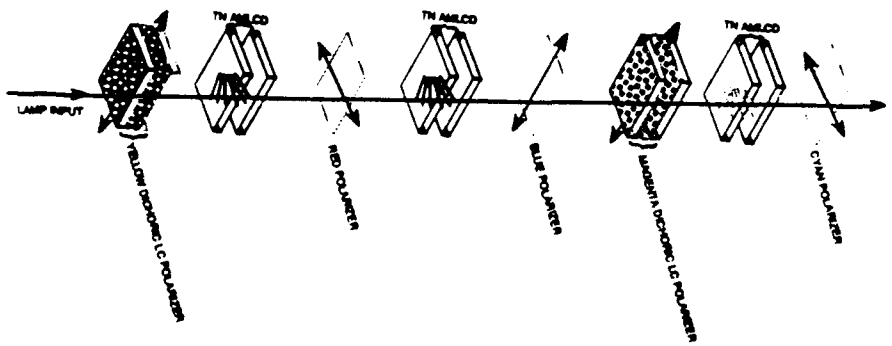


Figure 3. Expanded View of Normally White Optimized Subtractive Assembly D.
(Thickness of Elements is not to Scale)

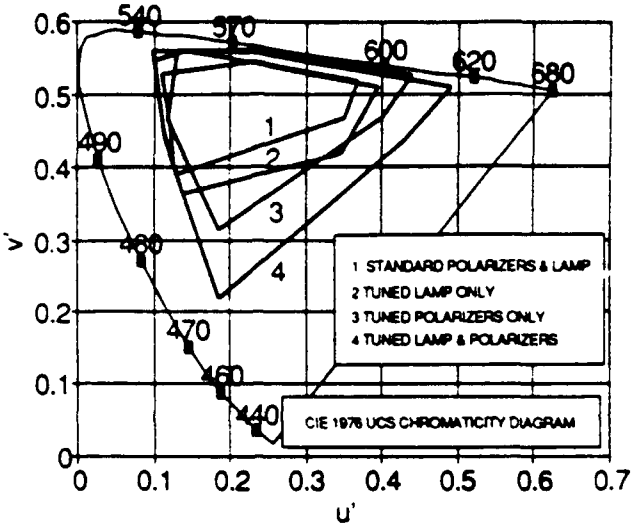


Figure 4. Color gamut comparison showing improvements due to notch filter tuned lamp, and tuned polarizers. Color gamut improvements are 1) no improvements (standard polarizers and xenon lamp) , 2) tuned lamp only, 3) tuned polarizers only, and 4) tuned lamp and tuned polarizers.

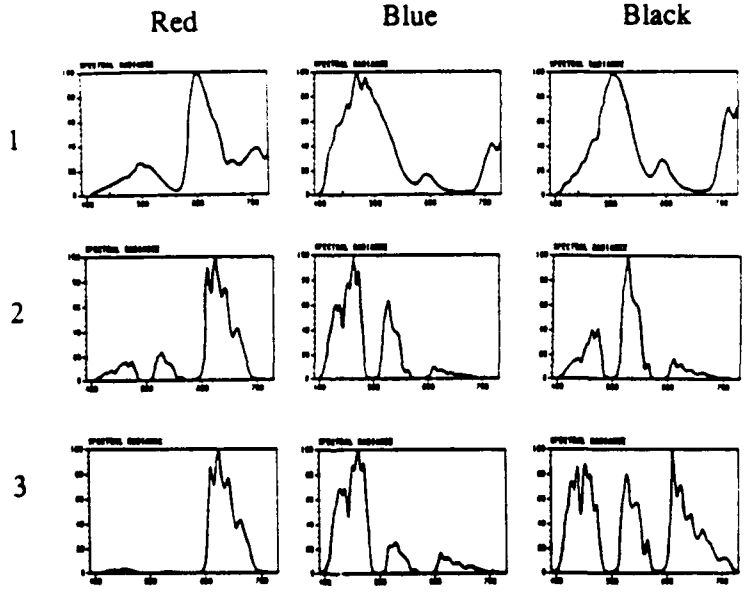


Figure 5. Improvements in Red, Blue, and Black Spectra with 1) Standard Polarizers Standard Xenon Lamp 2) Standard Polarizers and Tuned Xenon Lamp, and 3) Tuned LC Dichroic Polarizers and Tuned Xenon Lamp

2.1.4 Color Gamut

Assembly D is comparable to a shadow mask CRT. It has a balanced white state, and contrast ratio of 50. The color gamut of Assembly D, curve #4 of Figure 4, is shown in Figure 6 compared to the color gamut of a shadow mask CRT, and the NTSC standard. This optimized subtractive color gamut covers a larger area of color in its boundaries than either the shadow mask CRT or the NTSC Standard. A color gamut area comparison is shown in Figure 7.

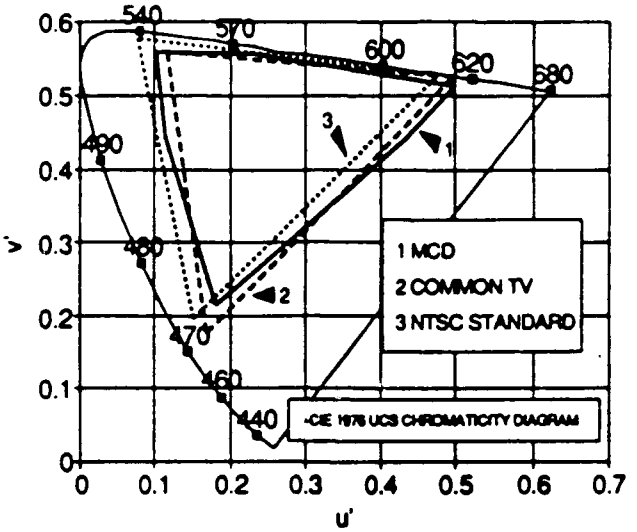


Figure 6. Color Gamut Comparison of Optimized Subtractive Color Assembly D vs. Shadow Mask CRT (Command TV) and NTSC standard.

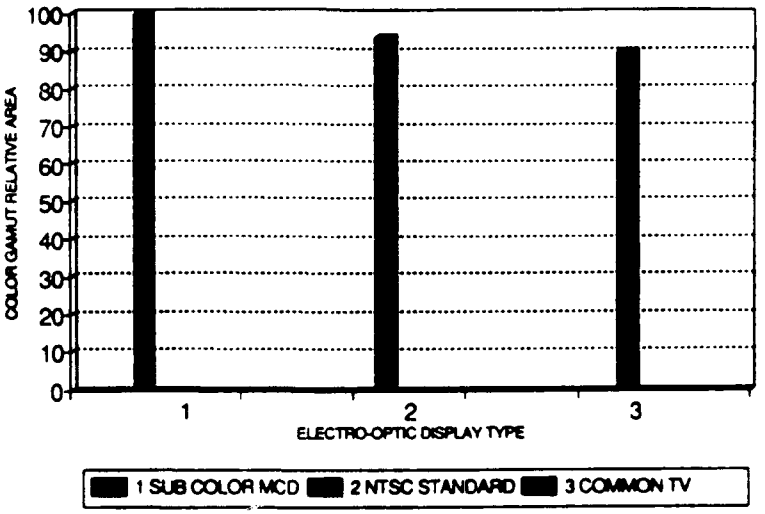


Figure 7. Color Gamut Area Comparison of Optimized Subtractive Color Assembly D vs. Common TV (Shadow Mask CRT) and NTSC Standard.

2.1.5 Luminance Compliance

The illumination system includes a Fresnel lens and a subsequent diffuser to facilitate adjustment of the output luminance profile. The Fresnel lens converts the fiber bundle output to a highly directional output in the forward direction while minimizing spatial non uniformity. The diffuser gain is selected to achieve the required forward luminance. The diffuser gain also affects the numerical aperture or viewing cone angle of the displayed image.

The color gamut and contrast ratio for the AMLCD image sources vary from the values published for the single pixel stack. The major reason for this is that when the driving electronics were designed they were designed for a single row voltage setting shared between cyan, magenta and yellow panels. In actuality the TFT's demonstrate differences in threshold voltage,"on" current, and "off" current between panels. Therefore, for a 300 lpi design using amorphous silicon TFT's, we need independent control over the row voltages to drive the pixel RMS voltage over the designated range for each panel. This will be corrected in future designs. Despite this restriction in voltage ranges we can still set up voltages to achieve a usable color gamut and comply with the high ambient contrast requirement.

For the 300 watt Xenon illumination system with a Fresnel lens, a high gain diffuser, and filters we measured 1,000,000 fL for the peak luminance. For AMLCD image source No. 5, a straight through transmission of approximately 2 % was measured, and an angular averaged transmission of approximately 1% was measured for a collection angle of approximately 5 degrees. A dark field contrast ratio of 25:1 was demonstrated with AMLCD image source No. 5. With the 300 watt Xenon lamp with Fresnel lens, high gain diffuser and filters the luminance of subtractive color AMLCD image source No. 5 was measured at 10,000 fL for a 5 degree collection angle, with the lamp at full power. *At the peak lamp luminance, when utilizing an equation provided by Dr. Dave Post, a contrast ratio in excess of 3 was calculated for high ambient 10,000 fC forward scene luminance, for AMLCD image source No. 5.* A plot of lamp system luminance vs. calculated contrast ratio at 10,000 fC forward scene luminance for AMLCD subtractive color image source No. 5 is shown in Figure 8.

If the notch filters are removed, a 300% luminance increase occurs. This produces a narrower but still useable color gamut. In this case, the diffuser gain could be reduced to increase the numerical aperture or viewing cone angle while maintaining luminance compliance.

In principal, the optical transmission of a subtractive color system can be much higher than a conventional additive color system using absorptive color filters. The optical efficiency of the subtractive color MCD is determined by the back light spectrum, lamp to fiber optic cable (FOC) coupling, FOC transmission, notch filter transmittance, degree of backlight collimation, color polarizer transmission characteristics, and pixel aperture ratio. These parameters were not optimized. These prototype MCD's limit the transmittance to approximately 2 %. This compares to a typical transmittance of about 3% in present state-of-the-art additive color AMLCD's.

By optimizing the MCD light valve and backlight parameters, we believe that we can increase

the optical transmittance by roughly a factor of five, yielding a peak luminance of approximately 6000 fL at a substantially increased numerical aperture with no loss in dark field contrast ratio. This will substantially reduce the lamp power requirement to as low as 50 watts, yielding a calculated peak contrast ratio of 3:1 with a substantially increased viewing angle.

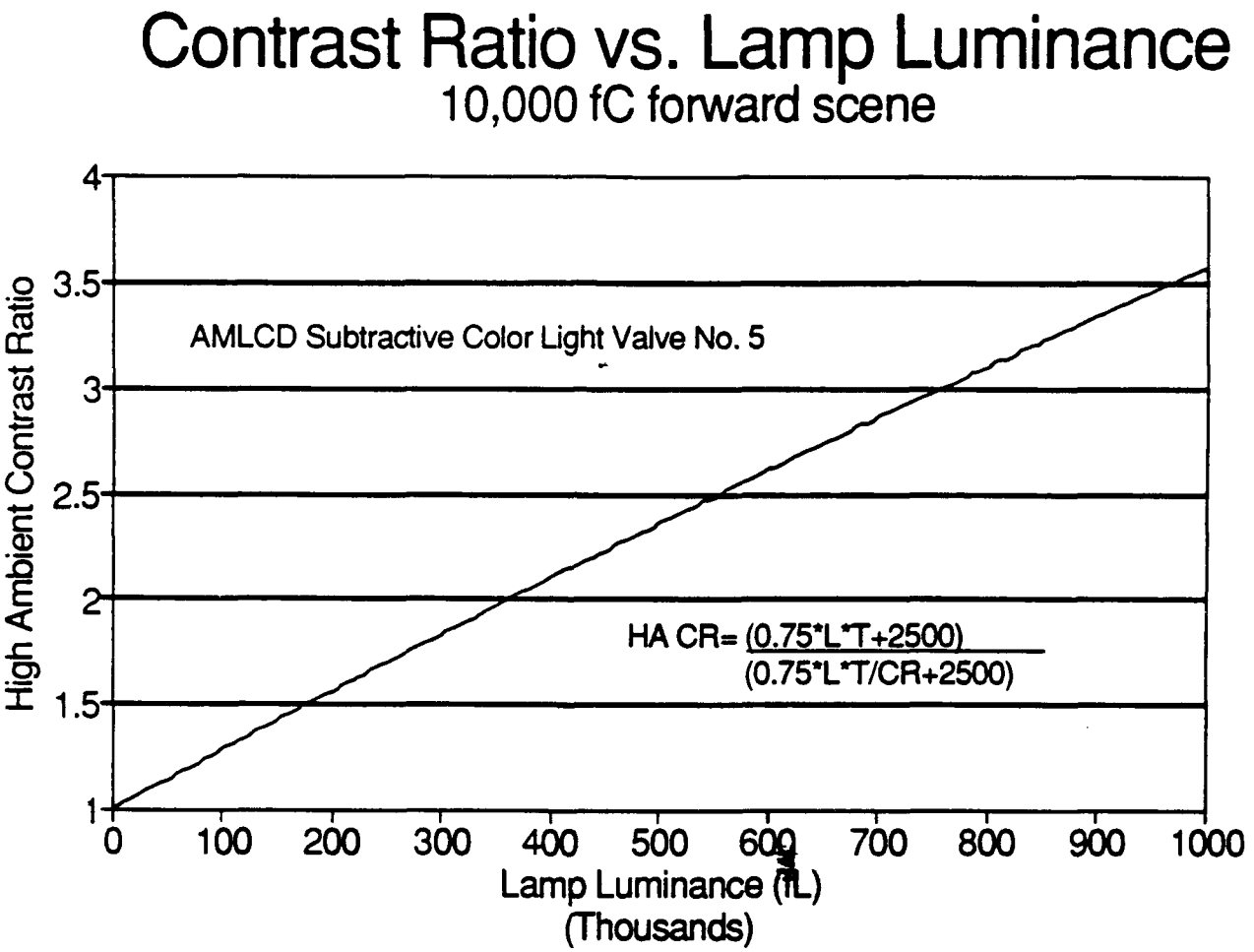


Figure 8. Illumination System Luminance vs. Calculated Contrast Ratio at 10,000 fL forward scene luminance is plotted for AMLCD Subtractive Color Image Source No. 5 for a 5 Degree Collection Angle. Maximum Illumination System Luminance is 1 Million fL.

2.1.6 Liquid Crystal

We are using a fast switching video rate super fluorinated liquid crystal with a high bulk resistivity for TFT video compatibility with our current subtractive color twisted nematic with color polarizers.

2.1.7 Guest Host

Our original plan was to use guest host technology for subtractive color. Guest host technology utilizes a dichroic dye dissolved in the active switching liquid crystal, providing a switchable (subtractive color to white) color polarizing layer. Guest host technology was evaluated as a subtractive color display medium with respect to satisfying the contract goals outlined above. We achieved a good color gamut with guest host technology, and color polarizers (Heilmeyer guest host). The response time of the guest host displays was too slow for video driving. In addition, guest host liquid crystals have low bulk resistivity. A high liquid crystal bulk resistivity is necessary for active matrix video driving. Due to these problems, The guest host approach to subtractive color was abandoned. Time was not wasted however, as we learned much about lamp tuning and color polarizer tuning during this phase of development.

2.1.8 Neutral Density Display

Our original plan called for the use of a neutral density twisted nematic AMLCD in addition to the cyan, magenta and yellow twisted nematic AMLCD's to independently control gray shading of all selected colors. The Transmission for this 300 lpi four cell subtractive color stack with 50 % aperture ratio was only 0.24 %. The calculated lamp luminance to achieve a contrast of 2 at 10,000 fL ambient forward scene luminance is 4 million fL. It would require a two kilowatt lamp to output this luminance. This was unacceptable. To increase the transmission of the subtractive color stack, the neutral density AMLCD was eliminated.

2.2 Gray-Scale Algorithms

The purpose of the grey-scale algorithm is to determine the CMY panel drive voltages necessary to obtain target Lu'v' coordinates, where the desired coordinates must be located within the obtainable Lu'v' space of the stack. The algorithm tries to find the minimum of the objective function

$$\min \left[(Lu'v')_{desired} - (Lu'v')_{obtained}\right] \quad (1)$$

where L, u', and v' are functions of independent variables which are the cyan, magenta, yellow, and neutral density panel drive voltages C, M, and Y, respectively:

$$\begin{aligned} L &= f_1(C,M,Y) \\ u' &= f_2(C,M,Y) \\ v' &= f_3(C,M,Y) \end{aligned} \quad (2)$$

All general numerical optimization algorithms require that the variables be independent of one another.

During the development of the proposal, we implemented a Newton-type minimization method. At that time, the stack was constructed using guest-host type panels so that the overall transmittance of the stack could be determined by the product of the individual and independent panels:

$$T_{stack} = T_{cyan} T_{magenta} T_{yellow} \qquad (3)$$

For the Newton method an explicit model of panel transmittance as a function of control voltages is required. The assumed model used was

$$T = Ae^{-bf(V)} \qquad (4)$$

where

A = maximum transmittance (wavelength independent)
b = wavelength dependent parameter
f(v) = function of applied voltage (wavelength independent)

We found that inaccuracies were caused by fitting the panel behavior with the simple function of Equation 4. Additionally, we encountered convergence problems that resulted in finding local, and not global, minima.

After award of the contract, we chose a new minimization approach and adopted the simulated annealing algorithm to replace the model of Equation 4 with sets of actual measurement data [1]. This combinatorial method utilizes a discrete set of measurement data to find the best solution to Equation 1. The best fit modeling errors inherent in Equation 4 are eliminated by using actual measurement data. However, since the solution is chosen from the set of measurement data provided, a large number of measurements is required for best results. The algorithm also excels at finding global minima in the presence of undesired local minima. The simulated annealing algorithm also uses the objective function of Equation 1 and the overall stack transmittance as a function of panel transmittance of Equation 3.

Problems with this technique occurred when the panel type was changed from guest-host to non-dichroic. Equation 3 no longer holds due to the wavelength dependent polarization phase retardation of the output luminance from each twisted neumatic panel, and the effect of this phase retardation on the transmission through subsequent stack elements [2]. Figure 9 shows an example of the differences between the actual stack transmittance performance and the calculated (per Equation 3) results using white light.

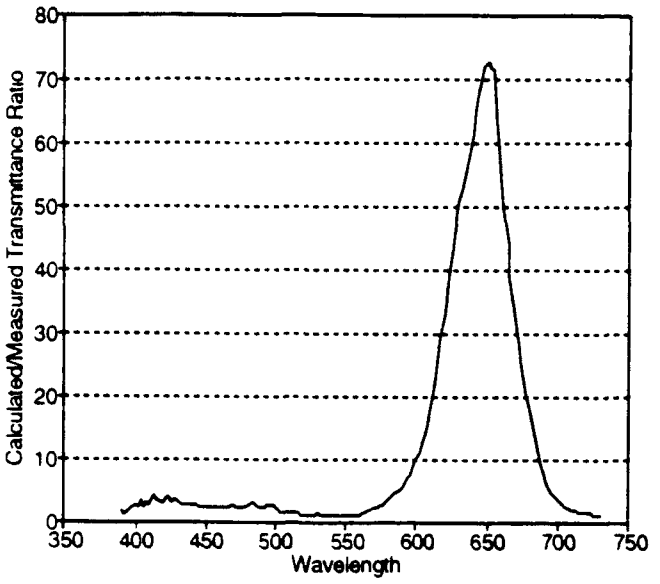


Figure 9. Measured/Calculated Stack Performance

To accurately characterize the stack, an equation similar to Equation 3 must be derived where the transmittance term of each panel is replaced by a Jones matrix [3,4]. Obtaining Jones matrices is a measurement intensive process that is subject to modeling and measurement errors. To avoid these errors, we implemented a technique wherein the stack is directly measured at all possible combinations of the panel voltages. This series of measurements yields a table which can later be scanned to locate closest Lu'v' coordinates to desired targets. The software used for these tasks is documented in the separate report , MCD Final Report Software.

2.3 Active Matrix Liquid Crystal Display

2.3.1 AMLCD Design and Fabrication

This section details the technical accomplishments that occurred during the AMLCD design and fabrication. The design and initial substrate fabrication was completed during Phase I. The first display panel was completed and demonstrated during Phase II. The first subtractive color stack was completed and tested during Phase III. Finally, during Phase IV the remaining deliverable subtractive color displays were completed.

Technical accomplishments are reviewed in the following areas. Active matrix design in section 2.3.1.1. Active matrix fabrication in section 2.3.1.2. Display design in section 2.3.1.3. Finally, display fabrication in section 2.3.1.4. Achievements relating to the assembly of the full subtractive color stack will be covered in section 2.3.2.

2.3.1.1 Active Matrix Design

The major accomplishments from this part of the program were the design and initial fabrication of the 300 x 400 pixel active matrix substrates. Resolution was set at 300 lines per inch. This design was thoroughly tested and evaluated to obtain estimates of the process stability and yields.

The starting point for the design was the determination of the specifications. These are summarized in Table 1. The design of the active matrix array used an 85 μm pitch for both rows and columns, leading to an aperture ratio of 56%. To accomplish this, the layout was completed utilizing a 6μm address bus width and a 5 μ space between this bus and the pixel edge.

Detailed drawing of the pixel architecture is shown in Figure 10. The scales are located on the bottom and left hand side of the layout indicate lengths in microns.

In addition, a photograph of a mini-array of completed pixels is shown in Figure 11. The source lines (column bus) and the gate lines (row bus) are clearly labeled.

Finally, Figure 12 shows a photograph of the entire substrate. This includes the active matrix and ten test structures positioned across the top and bottom of the substrate.

Table I. Specifications

Aspect Ratio	4:3
Resolution	400(H) x 300 (V)
Frame Rate	60 Hz
Pixel Pitch	85 μ (H) x 85 μ (V)
Aperture Ratio	56.7%
Active Matrix	a:Si
Drivers	Gould/AMI (Column) OKI (Row)
Mode	Subtractive Color
Substrates	22 mil thick

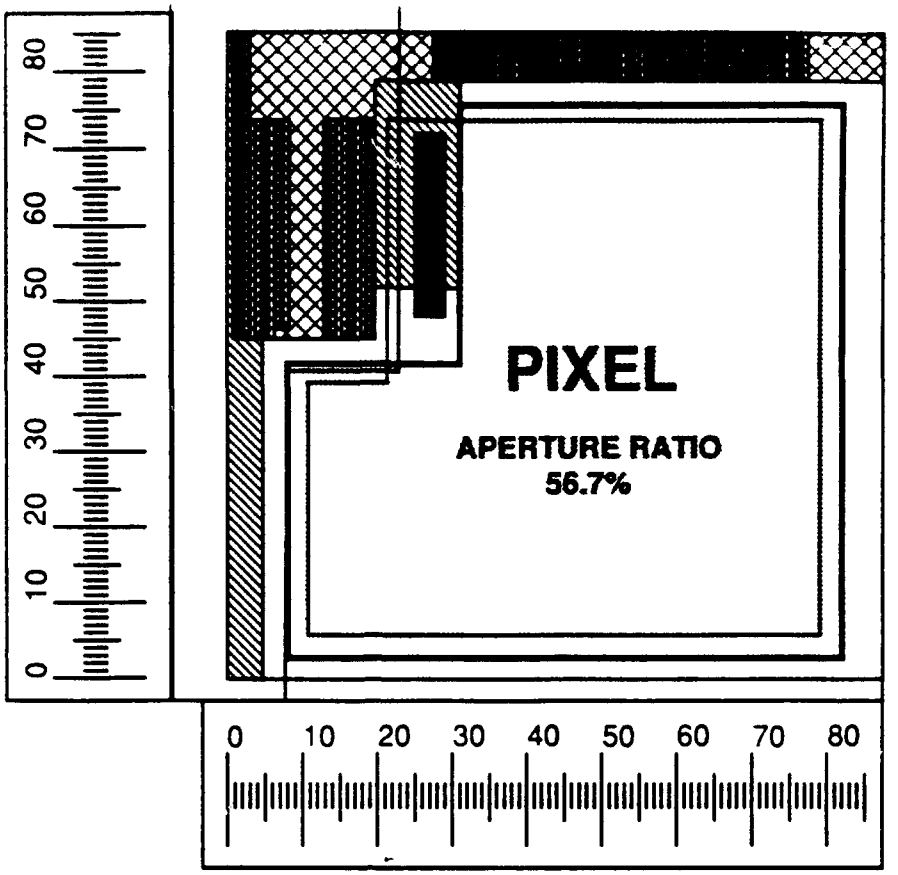


Figure 10. MCD Pixel Layout Dimensions/Scale in Microns

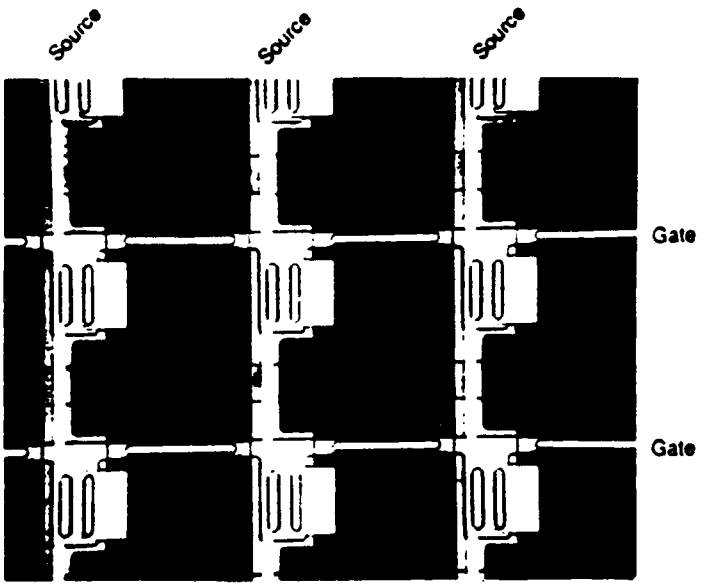


Figure 11. Photograph of a Small Section of the MCD Array Showing TFTs and Pixels (Pixel pitch is 85 μm).

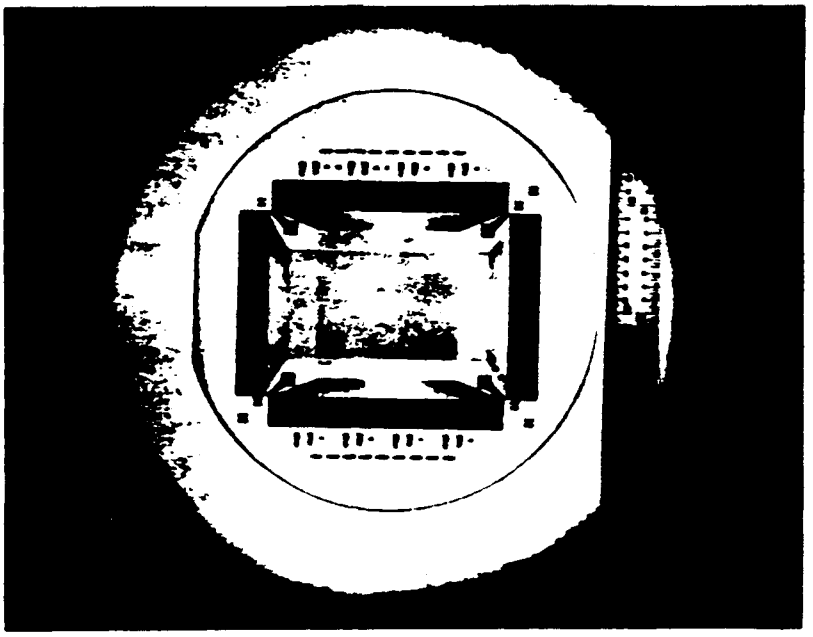


Figure 12. Photograph of the Entire MCD Substrate (Test Structures can be Seen Along the Top and Bottom)

To connect this display to external driving circuitry, bus connections were made to alternate rows and columns on each of the four sides. The row and column undergo further expansion until the final pitch of 305μ (0.012in.) is reached. At this point connection between the matrix and the driving circuitry is made with flexible cabling (El-Form).

Several test structures are included on the mask set. These allow for in-process monitoring of critical fabrication operations, validation of the active matrix design and determination of the stability of the substrate fabrication process to normal fluctuations in processing.

In-process monitoring is crucial for successful substrate fabrication. Deviations from expected results can be identified at the time of their occurrence. Poor quality material can be eliminated early in the process. Thereby reducing costs and improving quality.

The initial design of the active matrix substrates assumed certain thin film transistor performance. Validation of these assumptions is a crucial aspect of the overall design process. Test structures provide this type of feedback.

Finally, an understanding of the substrate fabrication process stability is crucial to the success of this program. This is determined by measuring electrical parameters on a family of thin film transistors specifically designed to simulate the impact of process variations on thin film transistor performance.

The greatest single factor determining the variability of transistor performance is the geometry of device. This is the ratio of the transistor width to its length. In order to characterize process stability, device geometry is intentionally altered by an amount significantly greater than that experienced during normal substrate processing.

After fabrication, these test structure devices are electrically characterized. The results of these measurements will indicate the sensitivity of transistor performance to normal process variations. In other words, the yield of the active matrix substrates.

2.3.1.2 Active Matrix Fabrication

The substrates were fabricated using amorphous silicon thin film transistors. This process was resurrected after several years of inactivity. The basic flow of the process is detailed in Table II.

The process begins with the deposition and patterning (masking layer 20) of the gate metal. This is followed by the deposition of both the silicon nitride gate dielectric and amorphous silicon layer. This is patterned using masking layer 30. Next comes the deposition and patterning of the inter-metal dielectric using layer 40. At this point, the thin film transistors have been defined and are ready for metal deposition and patterning (using layer 50). After completion of this step the transistors are ready for electrical parametric testing.

Table II. MCD - Active Matrix Process Sequence

1. Deposit 1200 A thick gate metal, pattern and etch	-L20
2. Deposit SiN_x dielectric and a:Si pattern and etch	-L30
3. Deposit 5000 A of IMD pattern and etch contact vias	-L40
4. Deposit Ti/Al source/drain metallization, pattern and etch	-L50
5. Deposit SiN_x passivation layer	
6. Pattern and etch pixel contact vias	-L70
7. Deposit ITO pixel electrode, pattern and etch	-L80
8. Pattern and etch bond pads	-L90
9. Deposit light shield layer, pattern and etch	-L60

Table III. Performance vs. Design

	Performance	Design
TFT I_{off} Requirement	2.5 pa - 4.5 pa	<3.3 pa
TFT I_{on} Requirement	>.3 μa	>.3 μa
TFT Channel Length	6 μm +/-.5 μm	6 μm
TFT Width	24 μm +/-.5 μm	24 μm

Table IV. TFT Process Stability

TFT Width	TFT Length	TFT I_{off}	TFT I_{on}
24	6	2.5 pa - 4.5 pa	>.3 μa
26	4	3.5 pa - 5 pa	> .3 μa
22	8	2 pa - 3 pa	>.3 μa

Once the devices have passed electrical testing the pixel contacts are defined using layer 70. After deposition and definition of the ITO layer (using masking layer 80) the substrates are ready to have their bond pads defined (layer 90). The last step in the process is the deposition and definition of the DARC material. This acts as both a light shield for the thin film transistor and as a spacer post.

A comparison of the measured performance of the devices with the design targets is found in Table III. These measurements were made in an enclosed test fixture, in the dark, and at room temperature. Critical parameters included in this table are the transistor drive current, referred to as the 'on' current and the leakage current, referred to as 'off' current. Actual measured device performance exceeded the design targets for both of these important device parametrics.

Also provided is the extracted length and width of the thin film device. The target width is 24 microns. As is seen from the table this value is achieved to within .5 microns. Therefore the width of an actual device is between 23.5 microns and 24.5 microns. The target length of the device is 6 microns. Once again, the actual value for processed devices is within .5 microns. The length of an actual device is between 5.5 microns and 6.5 microns. The .5 micron variation represents the limit of the photo-lithography equipment used in substrate fabrication.

Table IV summarizes data used to analyze the stability of the substrate fabrication process. These measurements were made in an enclosed test fixture, in the dark, and at room temperature. Included here are both the 'on' current and 'off' current for devices of various widths and lengths. Specifically, included here are results form the worst case variations that would occur during 'normal' processing.

For leakage current, that is 'off' current, this occurs when the width is larger than designed (26 microns) and the length is shorter than designed (4 microns). Consequently, one would expect the leakage current to increase for a device drawn with a width to length ratio of 26/4 as compared to the standard device of 24/6. As shown in Table 4, the leakage current does increase slightly. However not to a level that will degrade the performance of the display.

For drive current, that is 'on' current, the worst case variation occurs at the other end of the spectrum. That is, when the device is narrower and longer than the targeted design. This is shown in the table as the device with the width to length ratio of 22/8. The drive current for this device is greater than the .3 micro-amp design specification.

Summarizing the results on process stability the thin film transistors will operate at the targeted design specification for a range of width to length ratios from 26/4 to 22/8. As noted in Table IV, the typical variance in the width to length ratio, extracted from fabricated devices, is from 24.5/5.5 to 23.5/6.5. Therefore, the amorphous silicon fabrication technology utilized in this program will yield thin film transistors that have electrical operating characteristics, tested independent of environmental externalities, that are consistant across wide variation in substrate processing.

2.3.1.3 Display Design

This section focuses on the design of the individual display panels that were assembled into the subtractive color stack. Several accomplishments were achieved in the areas of cell gap spacing and in shielding the thin film transistors from exposure to light.

Starting with the spacing of the cell gap. In order for the cells to operate effectively, the cell gap spacing had to be controlled tightly. The design called for two different cell gap thicknesses.

The thickness on the yellow AMLCD cell was set to be 3.5 microns. The thickness of the magenta and cyan AMLCD cells was set at 4.5 microns. It was decided to utilize a polyimide material (DA C) as the spacer post. Processes were developed to fabricate cell gaps of 3.5 and 4.5 microns ing this material.

In order to meet the optical luminance requirements of this program a significant amount of light is incident upon the subtractive color stack. The response of the amorphous silicon thin film transistors to this environment was a potential problem area. In order to minimize these effects, the following three part light shielding strategy was implemented.

First, the individual panels were assembled utilizing a back plane patterned with the nickel-chrome gate metal covering the active transistors. In the final stack design the light passes through the patterned back plane first then through the active matrix. In this way, the gate metal on the back plane would protect the thin film devices from the deleterious effects of induced photo-conduction current.

Next, the DARC polyimide material was patterned into spacer posts that were placed over the active devices. This would provide a second level of protection. Primarily for reflected light.

Finally, since the thin film devices were designed utilizing the inverted stagger architecture the gate is underneath the active area of the device. The gate of the thin film transistor provides yet another level of protection from ambient light.

2.3.1.4 Display Assembly

This section details the process utilized to assemble individual active matrix panels that will comprise the subtractive color stack. Included is a summary of the operating conditions for each display.

Figure 13 is a high level block diagram of the AMLCD assembly process used to assemble the individual panels and to assemble the subtractive color stack. Blocks numbered 1 through 22 identify the single panel assembly process. Blocks numbered 23 through 25 identify the subtractive color stack assembly process.

This program presented several unique technical challenges. One was in the area of interconnection of the display to the external drive circuitry. The other was in the reduction of damage caused by electrostatic discharge occurring within the display. This results in regions characterized by a large number of individual pixel failures. Figure 14 describes the technique used to bond the display to the external drive circuitry. This method utilizes heat seal bonding between the display and a printed circuit board. Flexible interconnect material is used for this operation (El Form). This board is plugged into another printed circuit board containing the row or column drivers.

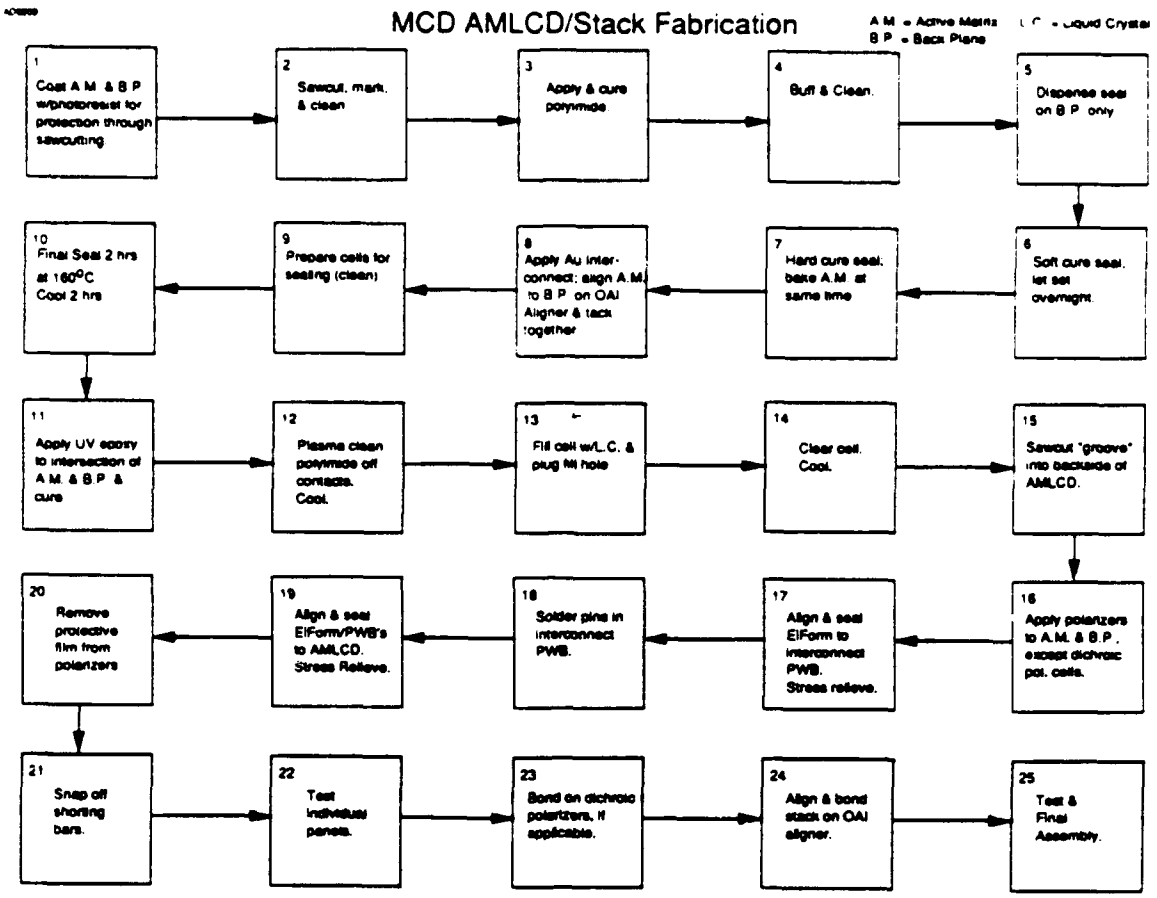


Figure 13. MCD AMLCD/Stack Fabrication

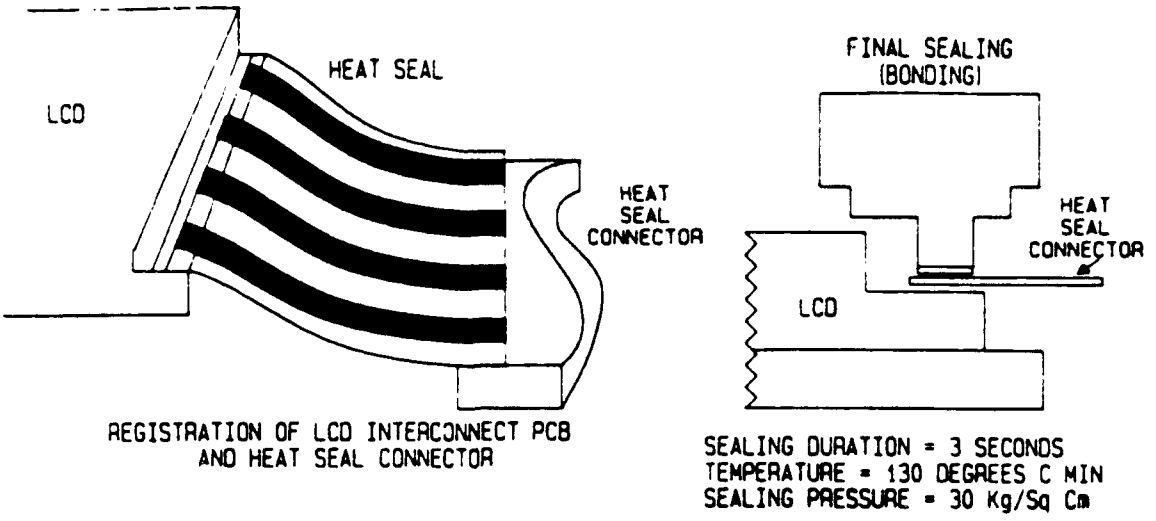


Figure 14. Interconnect Using Heat Seal Connector

As shown, the process requires heat and pressure to ensure a strong connection between the display and the El Form. Use of thin glass substrates required the development of a bonding process, including handling techniques, so as to avoid cracking the display during this operation.

Figure 15 shows an expanded view of the display connected to the boards containing the drivers. Following the interleaved design of the outputs on the active matrix, drivers are bonded to each of the four sides of the display. Column drivers are located along the top and bottom of the display. Row drivers are located on the left and right sides.

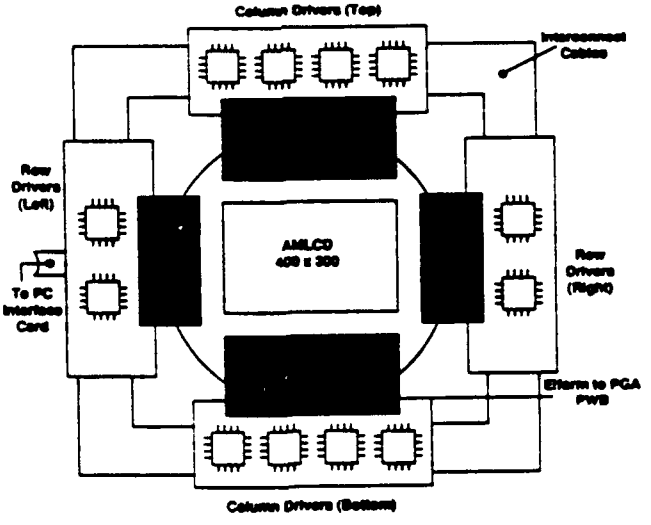


Figure 15. Driver CCAs and Display

Figure 16 shows the technique utilized to eliminate damage caused by electrostatic discharge. All of the rows and columns are connected together by a shorting ring. This provides a large area for dissipation the electric charges built up during AMLCD assembly, before they can cause significant damage to groups of pixels. After the bonding, described above, has been completed a groove is cut into the glass. The shorting bars are snapped off at this cut line. The bonded display remains in tact and ready for testing.

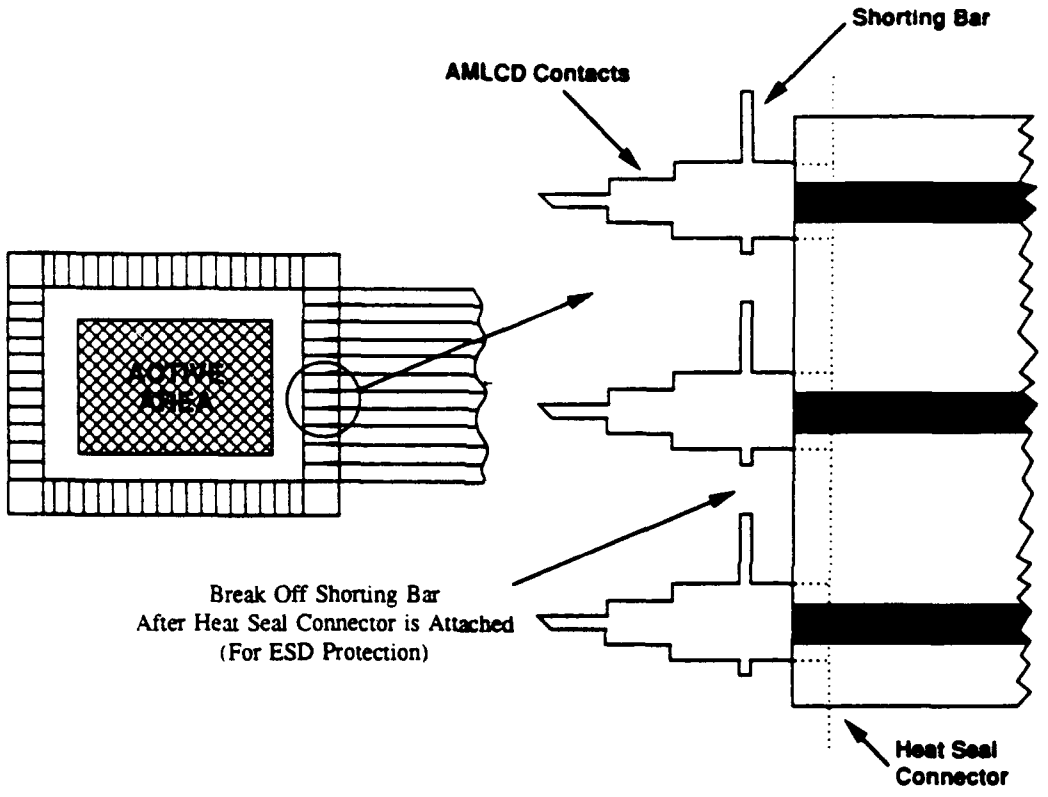


Figure 16. Interconnect with ESD Protection

Typical operating characteristics for a single panel are summarized in Table V. The row voltages, which are the gate voltage applied to the matrix transistors, operate between 0 volts and 20 volts. The column voltages, which are the source voltages applied to the matrix transistors, operate between 1.2 volts and 16.8 volts. The back plane voltage is typically operated in the range from 6 volts to 8 volts.

Table V. Operating Characteristics

Row Voltage	Ov → 20v
Column Voltage	1.2 → 16.8
Backplane Voltage	6 v → 8 v
Frame Rate	~ 60 Hz
Max. Gould/AMI Operating Frequency	9 MHz

2.3.2 Stack Assembly

Once the individual panels have been fabricated, assembled and tested they were ready for the final part of the program. Assembly into the final subtractive color stack.

The assembly process is reviewed in section 2.3.2.1. An operational summary of the five deliverable subtractive color stacks is provided in section 2.3.2.2. Finally, the packaging of the display is reviewed in section 2.3.2.3.

2.3.2.1 Assembly Process

A final subtractive color display consists of a stack of three active matrix panels and two passive dichroic cells. This section describes the process used to assemble the final stack.

Boxes numbered 23 through 25 on Figure 13 detail the block diagram flow for the stack assembly process. The yellow active matrix cell is used as the first layer, referred to as the base layer, of the alignment process. Next, the magenta active matrix cell is aligned and bonded to this base layer. Once this has been completed, the magenta dichroic cell is bonded to the magenta active matrix cell. The next step in the operation requires skill and patience. Aligning the cyan active matrix cell, through the magenta dichroic cell, to the magenta active matrix cell. Once aligned, the cyan cell is bonded to the magenta dichroic cell. Finally, the yellow dichroic cell is bonded to the yellow active matrix base. Opposite to the magenta active matrix cell. This completes the stack assembly.

The active matrix cells have the flex connectors and the driver boards attached at the time of stack assembly. Holding this in place during stack assembly is crucial. Figure 17 is a diagram of the holding fixture used in the process.

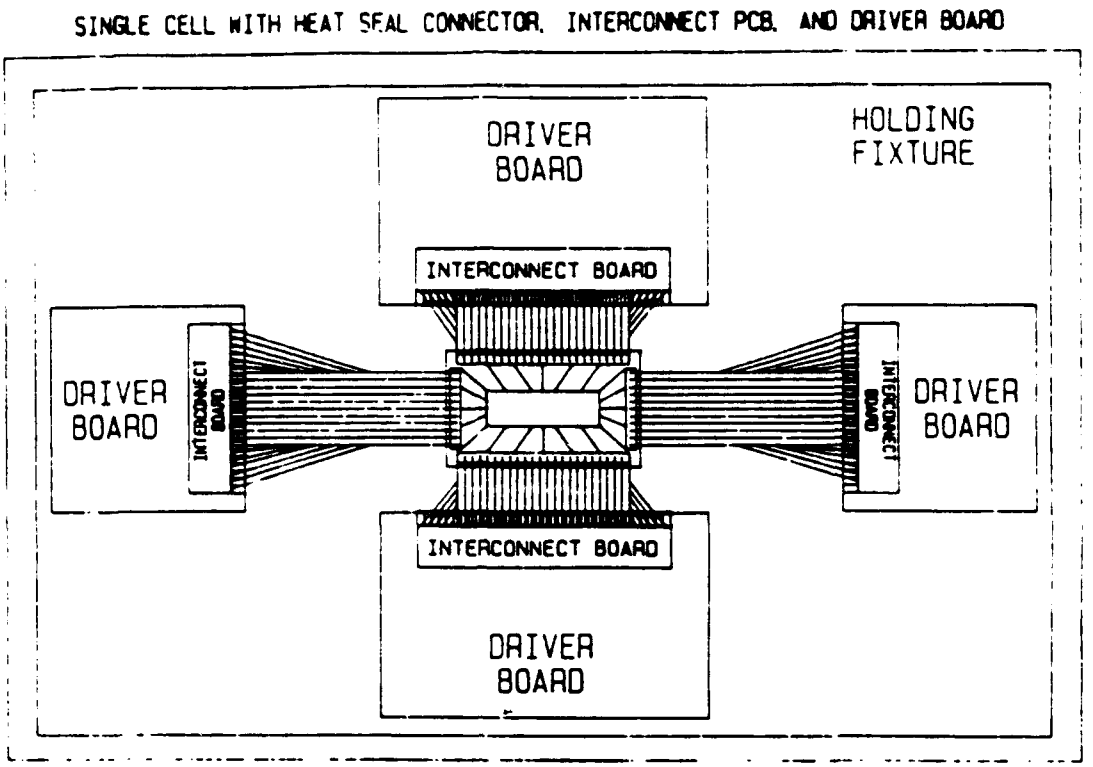


Figure 17. MCD Holding Fixture

2.3.2.2 Subtractive Color Stack Operation

This section summarizes the operation of the five subtractive color stack demonstrators. Included for each stack are the display's operating voltages and a description of the optical performance of the display. The stacks are reviewed in the order in which they were fabricated.

Stack One was the first demonstrator completed. The operating voltages for rows and backplanes are summarized below:

Vrow	Vcyan	Vmag	Vyellow
14.8	2.50	2.55	3.20

The individual AMLCD panels that comprise this stack had to be driven in an inverse mode of operation. That is, to turn on the thin film transistor the gate voltage had to be negative. To turn off the TFT the gate voltage was positive. Typically, the opposite is true. The gate voltage must be positive to turn on the transistors and negative to turn them off. After an investigation, it was discovered that the titanium target used to sputter the thin film transistor contacts needed to be replaced. Poor contact formation using titanium will cause an inversion in the type of transistor

being fabricated. The target change was accomplished and a new target monitoring system was instituted. This problem was not encountered again.

In order to drive this stack a software modification was made. This change recognizes that these transistors are to be inverse driven. The change is transparent to the user.

Color and dynamic images were reasonable considering that this was the first effort and that the inverse drive severely limited the ability to optimize the operating voltages of the individual panels. There were very few, less than 2%, row and column failures on this display.

Stack Two was the second demonstrator completed. The operating voltages for rows and backplanes are summarized below:

Vrow	Vcyan	Vmag	Vyellow
20.5	4.99	5.00	5.32

This stack was demonstrated at the final design review. The color was improved on this demonstrator as compared with Stack #1. However, a new problem was discovered. The magenta AMLCD panel smeared badly when displaying a dynamic image. The display also flickered. This was significantly reduced by changing the frame rate, in the driving hardware, from 60Hz to 72Hz.

Smearing was seen during the testing of the magenta panel at certain row voltages and not at others. After assembly into the stack, the best row voltage for the other two AMLCD panels, in terms of color, was at a value that caused the magenta to smear. Removing the magenta smearing, by altering the row voltage, leads to significant degradation of the color saturation of the other AMLCD panels.

The root cause for this dynamic smearing was found to occur in the design of the pixel. There is a parasitic overlap capacitance between the gate and the pixel contact. This results in unequal charge movement between the two parts of the drive cycle. The net result is a buildup of charge on the pixel, a DC voltagte across the pixel. Which appears as smearing during dynamic operation.

This problem could be resolved by allowing for independent control of the row voltage for each AMLCD panel or with a re-design of the pixel to eliminate this overlap capacitance. At the time that this smearing was discovered, there was not sufficient time or resources to implement either solution. This is an area for further work on subtractive color displays.

Stack Three was the completed next. The operating voltages for row and backplanes are summarized below:

Vrow	Vcyan	Vmag	Vyellow
19.4	4.36	4.20	4.88

The performance of this stack was improved over the previous two. Once again there was smearing in dynamic operation. This time it was the cyan cell. It is apparent that to minimize the smearing of a dynamic image the electrical performance of the AMLCD panels that comprised the stack would have to be matched as closely as possible.

Stack Four was the completed next. The operating voltages for row and backplanes are summarized below:

Vrow	Vcyan	Vmag	Vyellow
20.0	4.30	5.25	4.42

The performance of this stack was improved over the previous ones. Especially with respect to color. Once again there was smearing in dynamic operation. Since these AMLCD panels had been matched as closely as possible, the smearing was found to occur slightly in all panels.

Stack Five was the completed last. The operating voltages for row and backplane are summarized below:

Vrow	Vcyan	Vmag	Vyellow
18.6	4.00	4.00	4.00

The performance of this stack was the best of all of the displays. Especially with respect to color and dynamic imaging. Once again there was smearing in dynamic operation. These three AMLCD panels were the most closely matched electrically. Therefore the smearing was found to occur slightly only in the yellow AMLCD panel.

Several important conclusions can be drawn from our experience. First, each of the AMLCD panels that will comprise the final display must be matched as closely as possible with respect to electrical performance. Second, the driving hardware must be designed with the maximum flexibility to alter operating voltages supplied to each AMLCD panel in the subtractive color stack. Finally, it is possible to fabricate high density a:Si based pixels without redundancy and achieve high yields.

2.3.2.3 Packaging

Once the subractive color stack has been assembled it must be connected to the driver boards and mounted into supporting hardware. Figure 18 depicts a mechanical drawing of both the front and side views of this structure.

The front view shows the stacking of the row and column driver boards around the side of the display, Using the flex cable interconnection process. Row and column board stacking is three deep. One layer for each of the three active matrix panels within the subtractive color stack.

The side view shows how the back light is mounted. The fiber optic cable entered from the back and run straight into the back light. This is done to maximize luminance delivered into the back light.Once the subtractive color stack has been assembled it must be connected to the driver boards and mounted into supporting hardware.

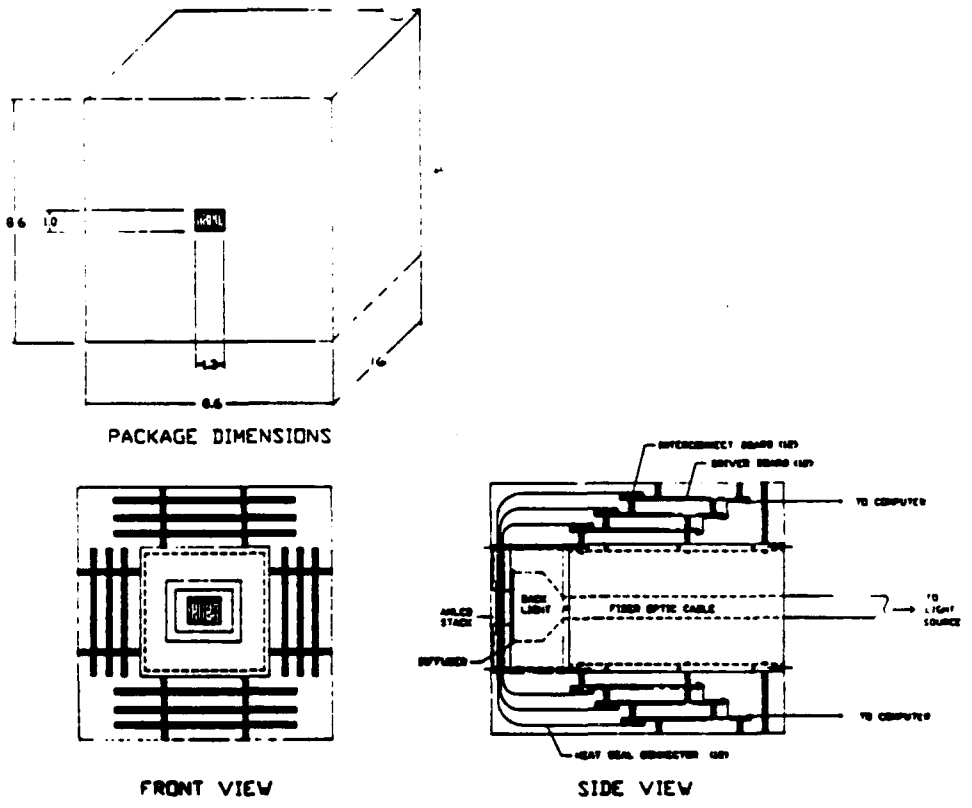


Figure 18. MCD Final Assembly

The front view shows the stacking of the row and column driver boards around the side of the display, using the flex cable interconnection process. Row and column board stacking is three deep. One layer for each of the three active matrix panels within the subtractive color stack.

The side view shows how the back light is mounted. The fiber optic cable entered from the back and run straight into the back light. This is done to maximize luminance delivered into the back light.

2.4 Drivers and Interconnect

To meet the contract requirements, the driver must provide a minimum of 16 grey-scale drive voltages to the active matrix based panels. Additionally, their output voltage range must be sufficiently large to produce the desired display contrast ratio.

To identify a suitable grey-scale source driver for the MCD program, numerous LCD electronics companies were researched. The offerings by Hitachi, NEC, OKI, S-MOS (Seiko-Epson), Supertex, Toshiba, Micro-Rel, and AMI-Gould were examined.

Although plentiful in Japan, gray-scale drivers are not readily available in the US., at least not in the small quantities required by the MCD program. Of the products researched, only three components emerged as viable possibilities: the Hitachi 66300T, the NEC 16453, and the AMI-Gould/Honeywell drivers. Problems with the Hitachi 66300T were tape automated bonding (TAB) packaging, a minimum 500 piece order, and a low accuracy TV-oriented design. The NEC 16453, also a TAB package, was custom developed for JAE for the Honeywell-produced Boeing 777 display; NEC is unwilling to supply this component to Honeywell for the MCD program and will shortly discontinue supplying components for 777. The AMI-Gould driver was developed in partnership with Honeywell to second source the NEC part.

The AMI-Gould source driver was chosen and ordered based on electrical specifications, availability, and access to AMI-Gould. This component meets and exceeds the requirements of MCD in that it is capable of supplying twenty-eight voltage drive levels and has a 0V to 18V output voltage range. The AMI-Gould component is a newly developed component. However, no problems were encountered.

The AMI-Gould column driver die was designed for eventual tape automated bonding (TAB) packaging. Thus, all outputs pads were placed on one size of the die. For conventional packaging, attaching bond-wires to the large number of outputs (64) requires a large package of approximately 2" by 2". This large package contributes heavily to the overall size of the MCD display.

To meet the panel testing schedule, a molded-ring-carrier quad-flat packaging (MRC-QFP) of the column driver was used in Phase II. This package was unsuitable for Phase III in that a bulky and costly socket is required to mount the part on the PWB. Therefore, a ceramic pin grid array

(CPGA) version of the part was used in the production assemblies to reduce packing size and socket costs.

Gate drivers manufactured by the above manufacturers were also reviewed in search of a mate to the AMI-Gould column driver. The OKI Semiconductor MSM6368 row driver was chosen as being the closest available match, although its supply voltages had to be level shifted to obtain output levels compatible with the AMI part.

2.5 Controller Electronics

To test and demonstrate the MCD, a flexible yet low development effort electronic interface was required. Where possible, low-cost commercially-off-the-shelf components were used. These included a Gateway 2000 PC "clone" for the platform and a Texas Instruments 34020 Software Developers Board (SDB) for the graphics generator/ However, to support subtractive color and the non-standard 400 x 300 resolution, additional custom electronic circuitry was required. Circuitry to interface the TI 34020 SDB card to the row and column drivers of the MCD was implemented. This circuity performed the following functions:

Color code to cyan, magenta, and yellow panel column drive code mapping: For each pixel on the MCD, the 34020 SDB has an associated image memory that is eight bits deep. Thus, each pixel has an associated color code ranging from 0 to 255. On image scan out, this code is obtained from the 34020 SDB card and supplied to a 256 entry by 12-bit wide random access memory (RAM). The 12-bit RAM output is split into three groups of 4-bits each, where each group is then sent to one of the cyan, magenta, or yellow panels. The 4-bits act to select one of the 16 available voltages available from the column drivers. The RAM is loaded via software to select 256 displayable colors out a palette of 4096 possibilities.

Sync separators: The 34020 SDB only provides composite sync whereas separate vertical and horizontal sync signals are required by the MCD drivers. Thus, a custom sync separator had to be included in the design.

Row driver power up/down sequencing: The row drivers require several voltage supply levels which must be turned on and off in proper sequence to avoid latch-up problems.
Column driver output level circuitry: Sixteen different drive voltage are provided to the column drivers, which in turn function as one-of-sixteen rotary switches at each column. For maximum flexibility, a separate set of 16 unique voltages is provided for each of panel thereby resulting in the need for a total of 48 reference voltages. Furthermore, to achieve a RMS voltage across the pixels, these voltages must be alternated plus/minus at 60 Hz. Twelve quad DACs were used to implement the 48 time-varying voltage levels.

Clocking and data load control: The number of outputs on available row and column drivers did not result in an integer number of devices per panel side. Therefore, special controller circuity

is necessary to load and clock the drivers such that unconnected driver outputs are bypassed and proper data alignment occurs between the top, bottom, left and right sides.

The software required to load the palette RAM is documented in the MCD Final Report Software Manual.

2.6 Illuminator

2.6.1 Lamp Requirements

We realized early on in the MCD program that in order to facilitate the optimization of the display color gamut and minimize lamp power requirements the lamp should have an emission spectra similar to that shown in Figure 1. Such a spectra may be obtained by means of a metal halide arc lamp. Unfortunately the lamp does not presently exist. Therefore we have obtained a 300 watt xenon arc lamp whose emission spectra appears as in Figure 19. In order to tailor this spectra to be more like the desired one we obtained two stop band multilayer dichroic filters. When the two filters are placed in series their transmittance appears as in Figure 20. The filters are placed on the input side of the MCD which results in an input spectra as shown in Figure 21.

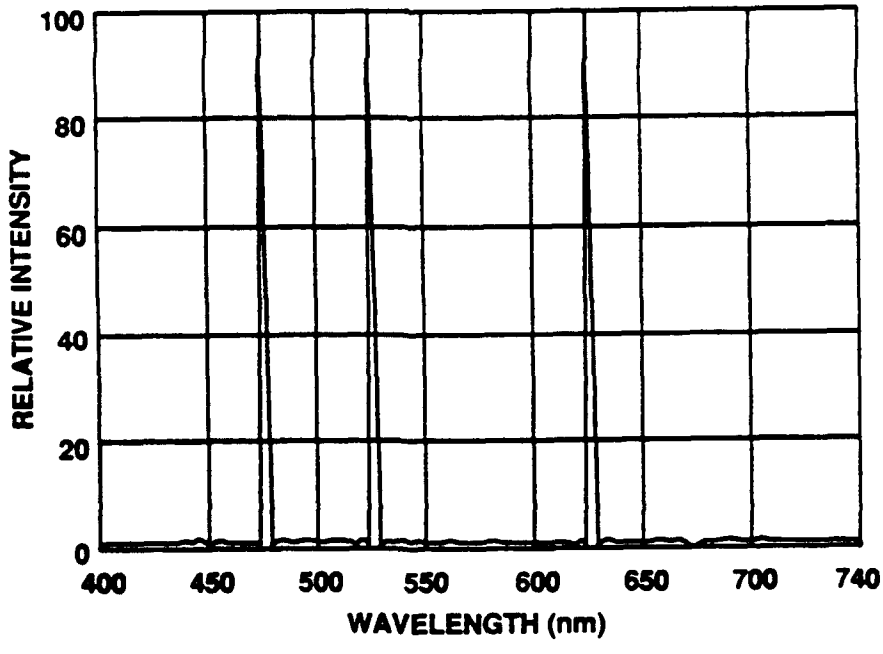


Figure 19. Spectral Distribution of Ideal MCD Illuminator

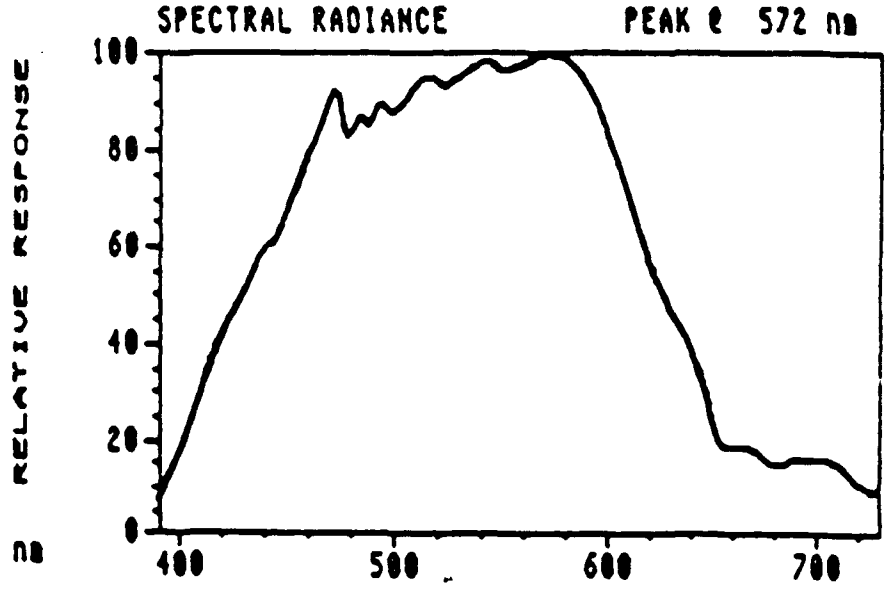


Figure 20. Spectral Distribution of a Xenon Arc Lamp

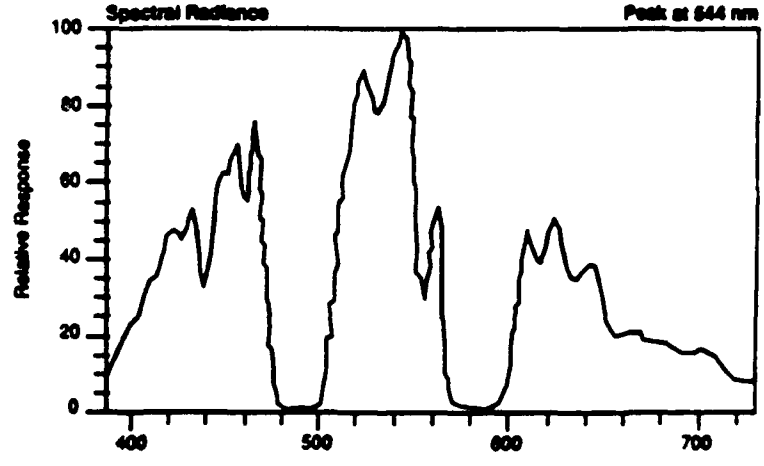


Figure 21. Spectral Radiance of the Xenon ArcLamp When Filtered by the Two Notch Filters

A new 300 watt xenon arc lamp will deliver as much as 1900 unfiltered lumens through a five foot fiber optic bundle to the MCD.

2.6.2 Thermal Tests

We have conducted an experiment to determine the thermal effects of a large amount of light on the MCD. The MCD consisted of a laminated stack of four cells with the appropriate polarizers. The cells were non-active dummy devices with a 50% clear aperture at 900 lpi. The setup was arranged with a ground glass diffuser on the lamp side of the MCD. The experimental arrangement is shown in Figure 22. The light source was a 300 watt xenon arc lamp with a cold mirror. The light was transmitted to the MCD through a ten foot long 3/8 inch diameter fiber optic cable which also served as a uv filter.

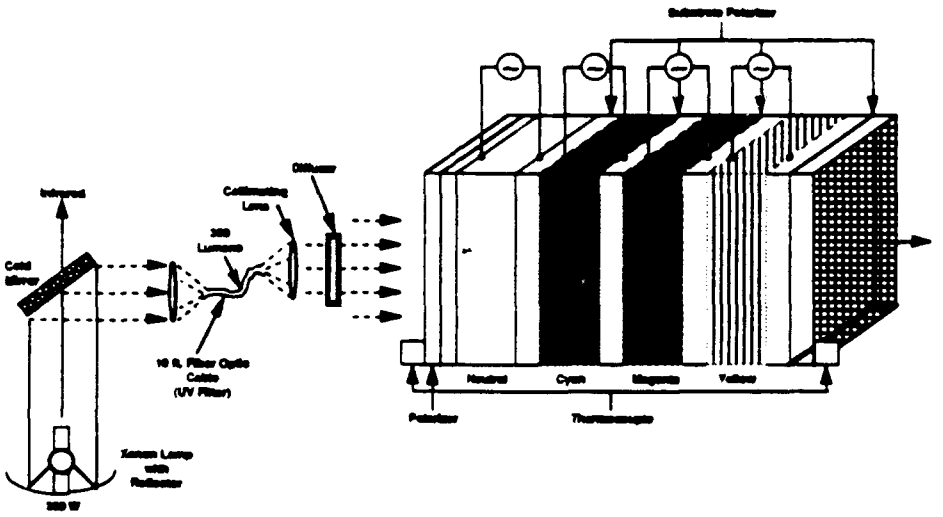


Figure 22 Experimental setup for thermal tests of MCD.

Thermocouples were cemented to the input and output surfaces of the MCD. A Pritchard photometer was used to measure the light transmitted through the diffuser and through the MCD stack. Two hundred forty thousand footlamberts were incident on the MCD, (330 lumens); 280 footlamberts were transmitted. The initial temperature of both sides of the stack was 25 degrees C. The three subtractive cells were turned on to transmit white light. In one hour a maximum temperature rise had been achieved; the input side reached 34.2 degrees and the output side reached 33.3 degrees C. The LC cells were then turned off. After one hour the input temperature had dropped to 30.8 degrees C and the output temperature had dropped to 29.8 degrees C.

Because of the failure to note the ambient temperature during the first tests we repeated them with a 30% increase in optical power. The setup was the same as that used before except for the following: a five foot fiber optic cable was substituted for the ten foot cable which resulted in 450 lumens to be delivered to the test stack, an increase of 100 lumens. In test #1 the subtractive

cells were powered on and the neutral cell was left in the off state (all cells transparent) See Figure 23 for these data. The lamp was turned on at time zero and other events occurred as shown on the data plots. Test #2 repeated these events with the cells all initially in the absorbing state. These results are shown in Figure 24. Tentatively, we conclude that the temperature rise will be manageable.

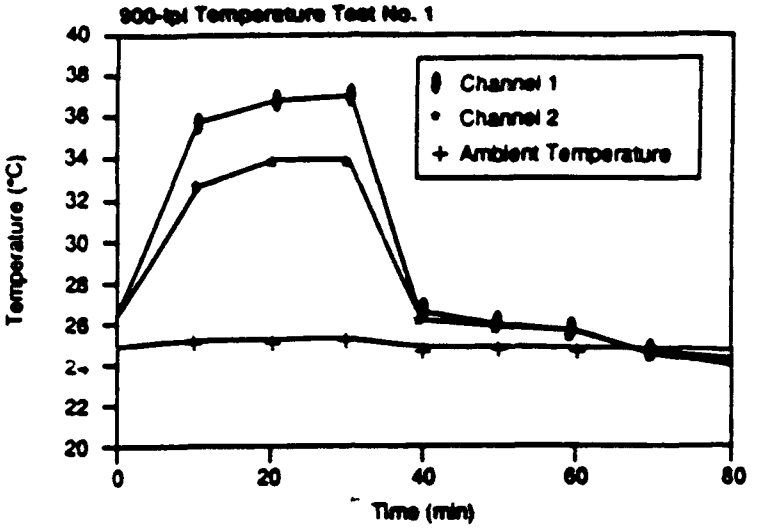


Figure 23. Thermal Test Results with all Cells in the Transparent.

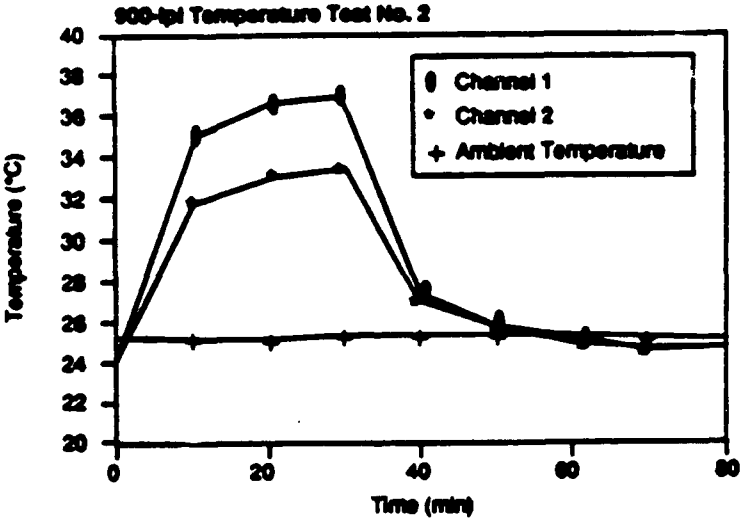


Figure 24. Thermal Test Results with All Cells in the Absorbing State

2.6.3 Angular Distribution of Transmitted Light

The MCD is intended to be viewed through helmet mounted display optics. The angular distribution of the transmitted light therefore affects the size of the exit pupil. Normally the image source for the HMD is a CRT which provides a Lambertian distribution. We have measured the angular distribution of the light exiting the MCD and is shown in Figure 25. The light is fairly collimated but the spread is sufficient to provide a 10mm exit pupil.

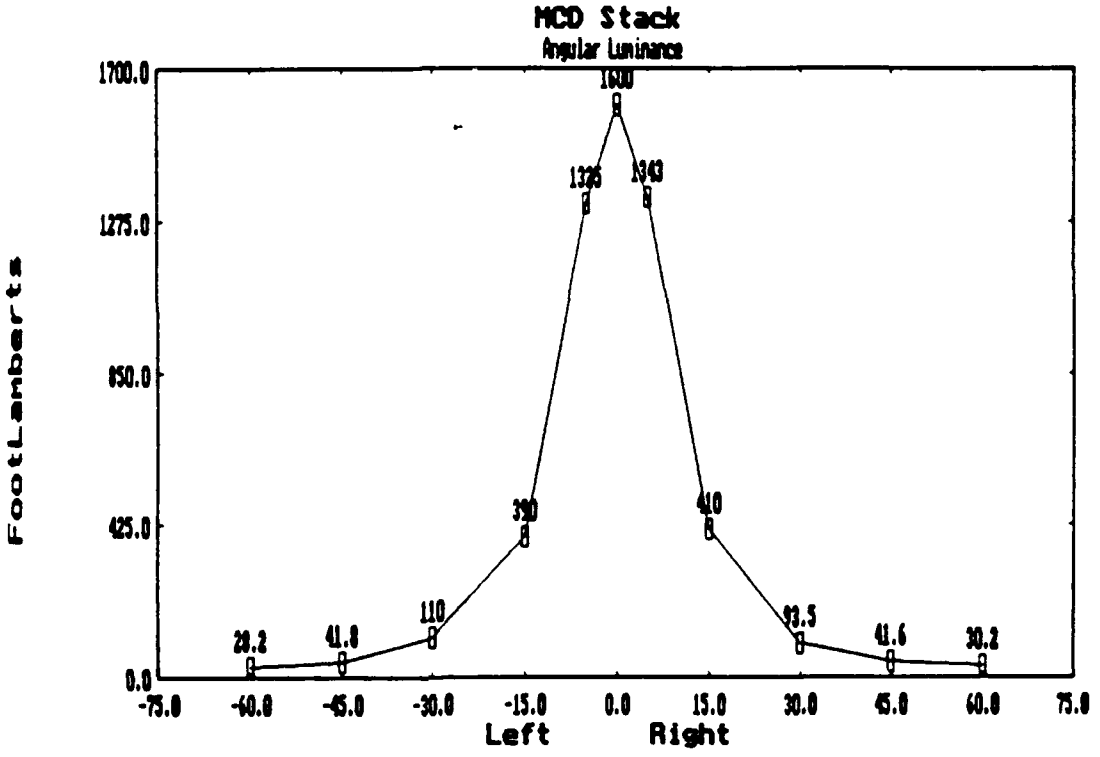


Figure 25. Angular Distribution of the Light Exiting the MCD