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13 ABSTRACT (Maximum 200 words)

This was a viewgraph presentation at the Government and Industry DMS Solutions Workshop. It explained the form, fit, function, and validation of the Generalized Emulation Microcircuit Program.

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GENERALIZED EMULATION MICROCIRCUIT PROGRAM

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GENERALIZED EMULATION MICROCIRCUIT PROGRAM

FORM, FIT, AND FUNCTION SPECIFICATIONS

COMBINATION OF:

ORIGINAL SPECIFICATION

MEASURED TYPICAL DEVICE CHARACTERIZATION

CHARACTERISTICS INHERENT TO ORIGINAL FABRICATION

TECHNOLOGY

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

FLEXIBLE APPROACH:

REDUCE NON RECURRING ENGINEERING

**MAINTAIN A SINGLE PROCESS SPANNING
MULTIPLE FAMILIES**

PROGRAMMABLE TECHNOLOGY

EXACT REPLACEMENT

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GATE ARRAY APPROACH

GENERIC MACROCELLS: NOR, NAND, ETC.

REUSABILITY

BICMOS TECHNOLOGY

MERGED BIPOLAR / CMOS PROCESS

BIPOLAR ELEMENTS IN I/O

CMOS FOR LOGIC FUNCTIONS

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GATE ARRAY CONFIGURATIONS

<u>ARRAY</u>	<u>I/O CELLS</u>	<u>CORE CELLS</u>
GEM1218	48	1218
GEM384	26 + 2 POWER	384
GEM120	16 + 2 POWER	120
GEM 120-24	24 + 2 POWER	120

TAILORED TO FIT INTO ORIGINAL PACKAGES

CORE CELL CONSISTS OF MULTIPLE TRANSISTORS, CAPS. ETC.

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

DEVELOPMENT PHASE - KEY ELEMENTS

DEVELOP BICMOS PROCESS AND DOCUMENTATION

DEVELOP GEM DESIGN LIBRARY

PROTOTYPE PARTS THAT SPAN OBSOLETE FAMILIES

TESTING

SUPPORT / INTERFACE STRUCTURE

APPLICATION / INSERTION PARTS

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM ROUGH SCREEN CRITERION - GEMABILITY

DIGITAL TECHNOLOGY

TECHNOLOGIES INCLUDE:

**TTL, STTL, LSTTL, DTL, RTL, ECL,
CMOS, PMOS, NMOS**

PIN COUNT $\leq$ 48

GATE COUNT $\leq$ 1000

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

PROTOTYPE DEVICES

ORIGINAL DEVICE

54LS00

LS TTL NAND

54LS107

LS TTL JK FLIP FLOP

CS720J

DTL NAND

MC955L

DTL JK FLIP FLOP

SH2100

CURRENT DRIVER

F10125

ECL TO TTL TRANSLATOR

C4485

TTL ARITHMETIC LOGIC UNIT

MM5060

PMOS SHIFT REGISTER

MC358A

ECL JK FLIP FLOP

54S181

S TTL ARITHMETIC LOGIC UNIT

DS8642

QUAD TRANSMITTER/RECEIVER

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

PART No.	ORGANIZATION
D3205	DESC ORDER
SW728-1P	DESC ORDER
SM-B-746395	ETDL/CECOM
SM-B-746396	ETDL/CECOM
SM-B-746131	ETDL/CECOM
AM2505/RM2505	CRANE
932046-501B SC15175FH-3	WR
932631-001B SC15180LH-3/MC2118	WR
8250	HILL/NUWES
54LS261	IBM
DS7836J	DESC DEMO
DS8642J	DESC DEMO
159202/SYC2534A/MIC2534/10197	NRAD/RAMP
A3012961-1/HC2135/9428-049	ETDL/SINGARS

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION

ONE YEAR BASE PERIOD

FOUR ONE YEAR OPTION PERIODS

TWO MAIN COMPONENTS

BASE EFFORT (CORE)

ENHANCEMENTS, SUPPORT

DELIVERY ORDER (IDIO)

IC RELATED PRODUCTION / SERVICES

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

VALIDATION PHASE (CORE ELEMENTS)

TECHNOLOGY ENHANCEMENTS

DESIGN (LIBRARY ELEMENTS, STRUCTURE)

PROCESS (YIELDS, PROCESS CONTROLS)

TECHNOLOGY SUPPORT

GEM DESIGN

GEM LIBRARY

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

VALIDATION PHASE (CORE ELEMENTS)

BASE LEVEL OF FABRICATION

INFORMATIONAL BRIEFINGS

ANNUAL CONTRACT BRIEFINGS

APPLICATION PARTS

PROGRAM MANAGEMENT

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION - CURRENT EFFORTS

SCHOTTKY ARRAY

HIGH VOLTAGE ARRAY

PROCESS MODIFICATIONS TO IMPROVE RUGGEDNESS

APPLICATION / INSERTION DEVICES

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION:

MENU APPROACH

MIX AND MATCH WORK ELEMENTS

CUSTOM TAILORING OF DELIVERABLES

LINE ITEM

DATA DELIVERABLES

PORTIONS OF REPLACEMENT TASKS POSSIBLE

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

VALIDATION:

STANDARD PROTOTYPE PART

40 PARTS

10 - 12 WEEKS

DATA PACKAGE RECEIPT

SAMPLES (IF AVAILABLE)

MINIMAL CUSTOMER INPUT REQUIRED

'REGULAR ORDER'

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION - EXAMPLES OF TASKS (NON INCLUSIVE)

CHARACTERIZATION OF OBSOLETE PARTS

TURNKEY IC DESIGN

DESIGN OF IC ELEMENTS

DESIGN OF NEW ARRAYS

CELL DESIGN NOTEBOOKS

MODIFICATION / EXTENSION OF GEM PROCESS

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

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GENERALIZED EMULATION MICROCIRCUIT PROGRAM

GEM VALIDATION - FUTURE PLANS

SMALLER GEOMETRIC FEATURE SIZE

SPEED

COMPLEXITY

VHDL CAPABILITY

EXPANDED DESIGN CENTERS

COST REDUCTION EFFORTS

STREAMLINING RESPECIFICATION PROCEDURES

GENERALIZED EMULATION MICROCIRCUIT PROGRAM

VALIDATION PHASE

KEY DELIVERY ORDER ELEMENTS:

MIPR TO DESC

SOW OR DESCRIPTION OF WORK

ASSISTANCE IS AVAILABLE / INTERACTIVE

WITHIN THE SCOPE OF THE EFFORT

ASSISTANCE / COORDINATION IS AVAILABLE