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This paper reports the first fabrication of active semiconductor and high temperature superconducting (HTS) devices on the same substrate. Complementary Metal-Oxide-Semiconductor (CMOS) transistors were fabricated on the same sapphire substrate as either YBCO flux-flow transistors (FFTs) or YBCO superconducting quantum interference devices (SQUIDs). All devices functioned as expected at 77 K without degradation, demonstrating that a compatible process has been found to monolithically integrate adjacent CMOS and HTS devices.

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Demonstration of Monolithic Co-fabrication of $Y_1Ba_2Cu_3O_{7-\delta}$ and CMOS Devices on the Same Sapphire Substrate

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We report the first fabrication of active semiconductor and high temperature superconducting (HTS) devices on the same substrate. Complementary Metal-Oxide-Semiconductor (CMOS) transistors were fabricated on the same sapphire substrate as either YBCO flux-flow transistors (FFTs) or YBCO superconducting quantum interference devices (SQUIDs). All devices functioned as expected at 77 K without degradation, demonstrating that a compatible process has been found to monolithically integrate adjacent CMOS and HTS devices.

In the seven years since the discovery of high-temperature superconductivity, the field of superconductive electronics has undergone explosive development. Due to difficulties in growing films directly on silicon, copper and oxygen contamination of the silicon layers during growth, and the high temperature environments seen in HTS growth, it has not been fully integrated with semiconductor based technology. Research has been focused on the use of superconducting interconnects between integrated circuits, which could lower chip power dissipation, reduce necessary interconnect width and pitch, and reduce dispersive loss. Several attempts have been made to fabricate HTS circuits or devices directly on Si or other semiconductor surfaces[1,2]; these layers were of low quality and were stress limited, and no devices were fabricated in the layers.

CMOS thin-film silicon on sapphire (SOS) devices utilizing improved silicon films have achieved performance equal to or better than bulk CMOS devices[3]. For low temperature, low power operation, CMOS SOS has a number of advantages over other silicon technologies[4]. Additionally, one of the best substrates for growth of YBCO layers for superconducting devices is sapphire.

Fabrication of the thin-film SOS CMOS on sapphire was performed first. Further details relating to the CMOS processing in SOS can be found in Offord[3]. Areas that were to later have HTS devices were initially protected from various silicon processing steps such as high energy ion implants by initially not removing the silicon layer from the area. In CMOS circuit fabrication, a layer of aluminum is typically used as the interconnect layer between devices. Aluminum, however, cannot withstand the processing temperatures incumbent in superconducting device fabrication. For short distances, this layer was replaced by a second polycide ($TiSi_2$) layer. After CMOS processing was complete, the silicon protective coating was removed in the HTS area and a 200 nm layer of Si_3N_4 was deposited and patterned over the CMOS devices as a final passivating layer against the oxygen plasma and copper environments seen during the YBCO growth.

YBCO devices were then fabricated on the bare sapphire adjacent to the test CMOS devices, aligned lithographically. Pulsed laser deposition (PLD) techniques were used[5] in conjunction with a series of buffer layers[6]. For the production of grain-boundary SQUIDs, these buffer layers include final MgO and CeO layers used to produce a 45° in-plane rotation where desired. YBCO deposited over the Si_3N_4 regions was not superconducting. An amorphous Al_2O_3 layer was used as a passivation of the YBCO devices. Openings for electrical contact to both the YBCO devices and the CMOS can be made using photolithography and RIE or ion milling and a final layer of metal can easily be patterned for a final interconnection layer.

Both bi-epitaxial and step edge SQUIDs were made with modulation voltages at 77 K as large as 40 $\mu V/\Phi_0$. I-V curves from both p- and n-MOS devices were measured and compared with devices which did not receive HTS processing. No significant difference was seen.

This demonstration opens up numerous other possibilities to explore the combination of these two well developed technologies. Circuits and devices that exploit the advantages of both HTS materials and SOS CMOS in order to mitigate the deficiencies of the other can be integrated together. For example, ultra-sensitive SQUIDs, bolometers, and ultra-high speed Flux-Flow Transistors and Josephson Junction based circuits (functioning at speeds of 100 GHz or more) can be combined with CMOS memories, latches, low noise amplifiers, silicon based sensors, and driving electronics.

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[5] K. Char, M.S. Colclough, S.M. Garrison, N. Newman and G. Zaharchuk. *Appl. Phys. Lett.* **59**, 733 (1991).
[6] L.P. Lee, K. Char, M.S. Colclough, and G. Zaharchuk. *Appl. Phys. Lett.* **59**, 3051 (1991).

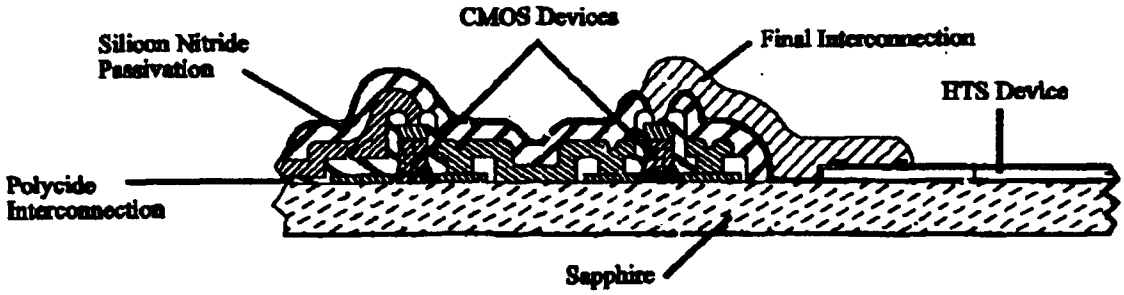
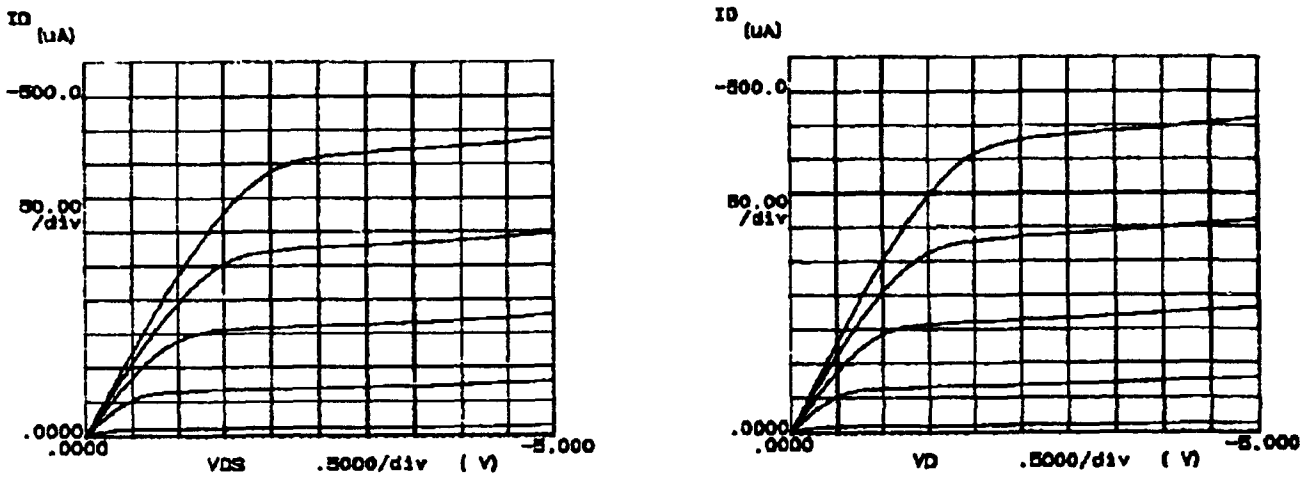


Figure 1. Cross-sectional Schematic View of Monolithically Co-fabricated HTS and CMOS Devices



(a) **(b)**

Figure 2. 3μm x 20μm PMOS I-V Curves at 300K (a) Before and (b) After Co-fabrication

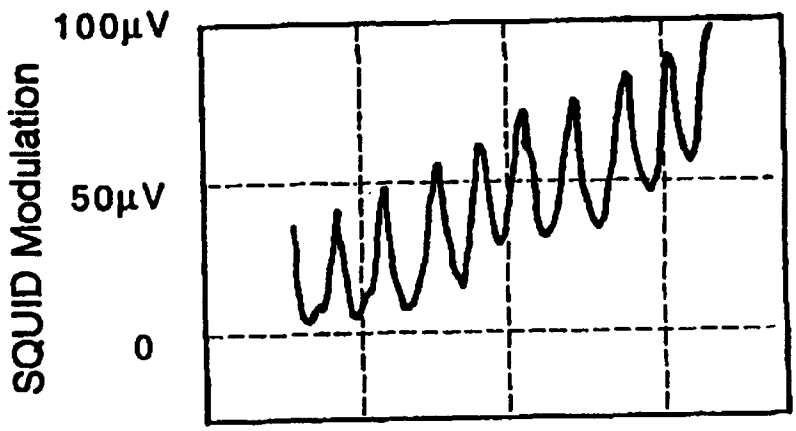


Figure 3. Functional Step-edge SQUID Monolithically Co-fabricated on CMOS/SOS