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TECHNICAL REPORT FOR GRANT No.:
N00014-93-1-1007

University of Maine

ADC TEST SUPPORT PROGRAM
1 Aug 93 through 30 Oct 93

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ADC TEST SUPPORT PROGRAM
Period of 1 Aug 93 Through 30 Oct 93

Principal Investigator: Fred H Irons
co-Investigator: Donald M. Hummels

Summary

This report summarizes accomplishments made under Grant No.: N00014-93-1-1007 for providing ADC Test Support to the ARPA HBT/ADC technology development program during the period of 1 Aug through 30 Oct 93. The following were accomplishments for this period. 1) Attended and participated in a planning meeting at the Mayo Foundation on 19 Jul 93 to discuss testing issues and develop an agenda for the September Workshop; 2) Attended and participated in the ADC testing workshop on 1 Sep 93 at Lincoln Laboratory. Information and example test results were presented for newly developed tests; 3) Started training a graduate research assistant on a program devoted to subject ADC architectures and relation to dynamic errors; 4) Performed initial tests to illustrate interaction of ADC error table models to generic ADC performance and interactions with input circuit VSWR and matching.

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1. Introduction

The subject grant was issued to initiate the participation of the University of Maine (UMaine) into the on-going ARPA HBT/ADC technology development program. It is planned that the Test Support program should probably be active for a duration of about two years through the scheduled product delivery phases of the ARPA program. The role of the UMaine participation is threefold: 1) To cooperate with MIT Lincoln Laboratory and the Mayo Foundation to provide recommendations for applicable tests, packaging, and expected properties for contractor ADCs; 2) to help prepare a seminar with Lincoln Laboratory to provide feedback from Task (1); and, 3) To document results and recommendations from both Tasks (1) and (2). This report provides a review of results and accomplishments for the first quarter participation in the program.

2. Planning Meeting at the Mayo Foundation

A one day meeting was held at the Mayo Foundation on 19 Jul 93 to initiate discussion on packaging issues and to plan the September workshop scheduled to be held at Lincoln Laboratory. The following people attended the meeting. From Mayo were B.Gilbert, W.Walters, D.Schwab, J.DeBarst, and B.Randal; From MIT Lincoln Laboratory were C.Martin and S.Broadstone; and D.Hummels was there from the University of Maine. Packaging and probing issues were discussed and demonstrated for various high frequency data structure examples that the Mayo Foundation had worked on in the recent past. It was useful to see setup methods and probing techniques actually used to achieve high frequency multiple chip testing and so it was decided to include this data into the scheduled workshop to share with the contractors. An outline for an agenda was then developed and agreed upon for the September workshop. A copy of the final agenda, coordinated and arranged by C.Martin, is shown in Table I. Areas of responsibility were divided as follows: Mayo would make recommendations for packaging design and layout for probe testing; Lincoln would perform high frequency testing, develop a probe capability for testing chips and developing prototypes through final packages; UMaine would concentrate on ADC Error Modeling, assist in the development of specific tests aimed at architectural features, and support testing of final packages.

Table I Workshop Agenda

HBT/ADC Testing and Packaging

MIT Lincoln Laboratory, September 1, 1993

- | | |
|----------------------|---|
| 8:30 - 9:00 | Opening Remarks
Walter E. Morrow, Jr., Director of MIT Lincoln Laboratory and
Zachary J. Lemnios, Program Manager ARPA/MTO |
| 9:00 - 9:30 | Performance Parameters for A/D Converters
Carol C. Martin, MIT Lincoln Laboratory |
| 9:30 - 10:30 | Testing Methods for A/D Converters
Steven R. Broadstone, MIT Lincoln Laboratory and
Fred H. Irons, University of Maine |
| 10:30 - 10:45 | Break |
| 10:45 - 11:45 | High Speed Packaging Approaches
Barry K. Gilbert and Daniel J. Schwab, Mayo Foundation |
| 11:45 - 12:15 | High Speed Package and Interconnect Simulations
Wayne L. Walters, Mayo Foundation |
| 12:15 - 1:00 | Lunch |
| 1:00 - 1:45 | A/D Converter Test Facility
MIT Lincoln Laboratory |
| 1:45 - 2:15 | Proposed Test Fixture
Mayo Foundation and MIT Lincoln Laboratory |
| 2:15 - 3:15 | Discussion of Proposal |
| 3:15 - 3:30 | Break |
| 3:30 - 4:30 | Testing Plans
TRW, Rockwell, Hughes |
| 4:30 - 5:30 | General Discussion |

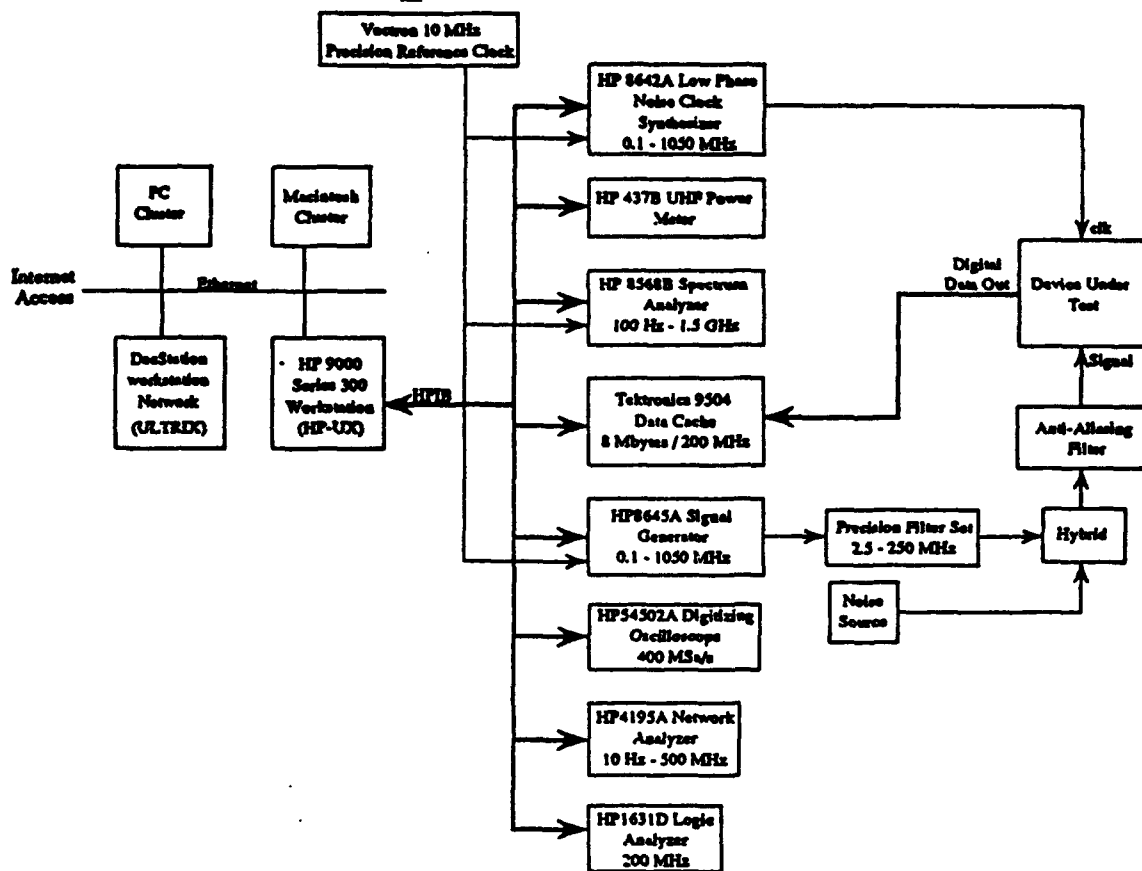
3. UMaine Contribution at the September Workshop

The UMaine contribution to the September Workshop held at MIT Lincoln Laboratory is reviewed here by including copies of the vugraphs presented at the workshop. The presentation emphasized that the University of Maine has a testbed comparable to the Lincoln Testbed. The tests that were described in this workshop were chosen to illustrate how customized tests could be designed to address specific types of errors and could compliment standard tests that have evolved for each test facility. In addition, data from recently developed experiments were presented to show that downsampling the output samples of an ADC does not compromise the full bandwidth performance data for the device. Finally data were presented to show how error models, in the form of lookup tables, can be used to correct dynamic errors for an ADC. It was pointed out that the error table models will be used to study how different error mechanisms can be made evident through the models so that error tables may provide useful tools to diagnose ADC performance. Brief descriptions are provided in the following paragraphs for each vugraph and subject area.

3.1 The UMaine ADC Test Facility

This first graph shows the instrumentation and the Local Area Network (LAN) control that exists for the testbed. The system is modeled after the test facility at Lincoln Laboratory which was also constructed under Dr. Irons' supervision. The heart of this system is a commercial high-speed data cache which is used to collect 16-bit data at rates up to 100 MSPS on each of two independent channels. The 8 MB cache capacity is quite adequate to handle all expected tests. Another feature of the system is the access through a LAN to a variety of work stations so that several users have access to the testbed. Outside contact is also available over Internet so that raw data could be shipped almost anywhere in the USA if required. The operating system is UNIX based and all programs are developed in C or C++ to provide a flexible and portable basis for evolving test programs.

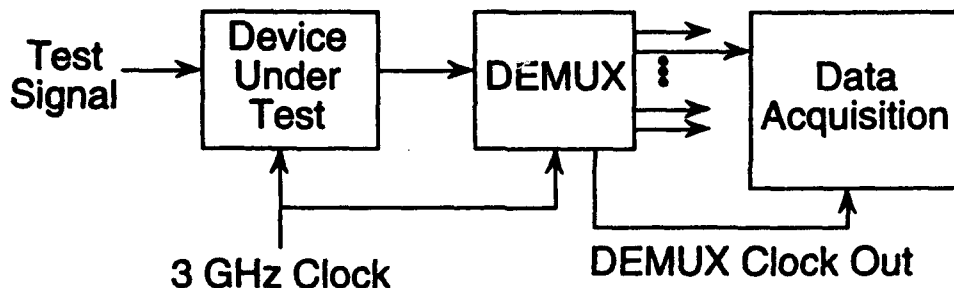
ADC Test Facility



3.2 Downsampling Test Results

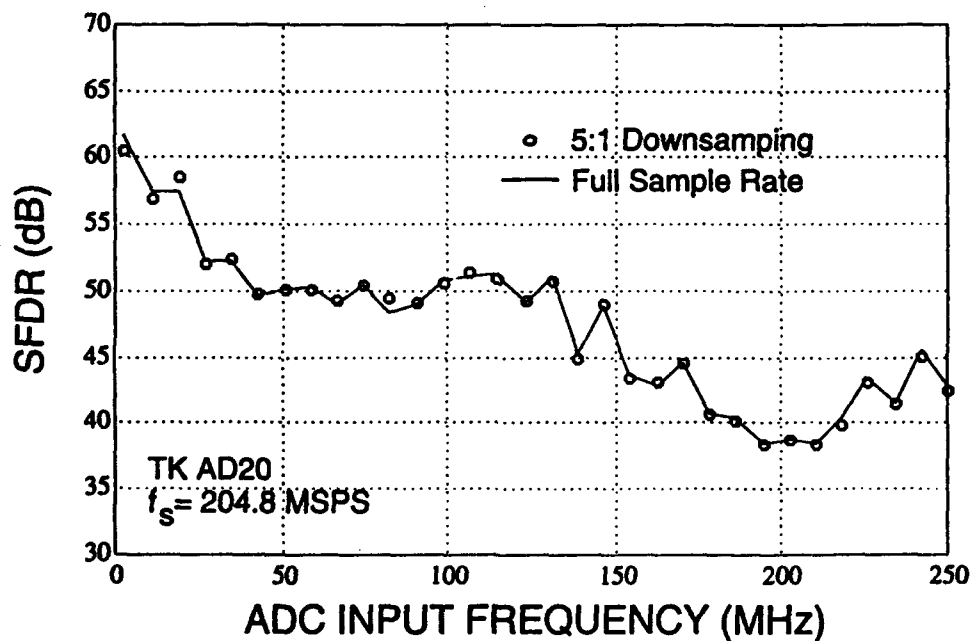
Two vugraphs are presented to illustrate measured downsampling results for a Tektronix AD20C 8-bit 250 MSPS ADC. The results are of interest because the 3 GPS ADCs planned for the ARPA program all have downsampled output data streams so as to accommodate the slower speed of commercially available data acquisition systems. The question was raised at the April design review about whether or not the full bandwidth performance was only aliased via the downsampling operation. Special tests were developed and run to answer this question. The AD20C was operated at a 204.8 MSPS clock rate in two-modes, namely; straight through and by a five-to-one downsampling ratio. The first graph illustrates the concept in block form and the second vugraph shows the results obtained from the experiment. The result shows that downsampled data provide identical results when compared to data obtained at a full sample rate for the standard SFDR test. It should be noted that the two sets of data were taken a day apart so the correspondence is even more assuring. Other standard tests that are unaffected by the downsampling operation are the Histogram and Residual Error tests since downsampled data sequences can easily be made to stimulate every possible ADC state.

Downsampling

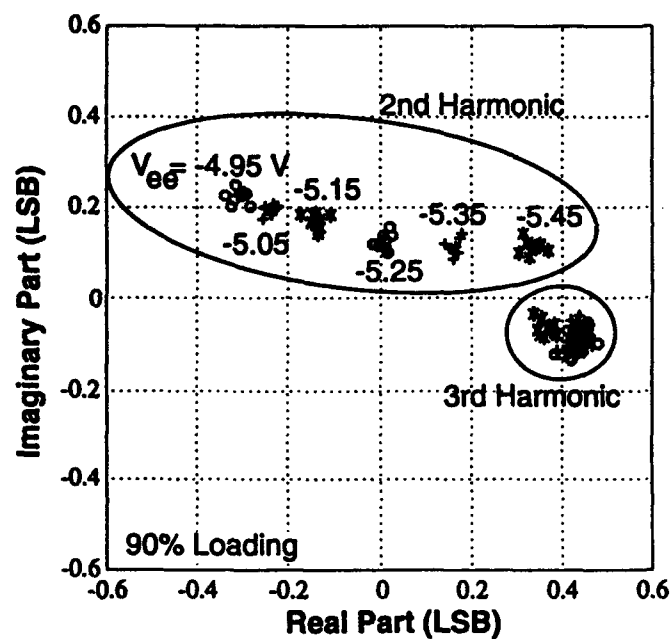


Full Bandwidth ADC Performance Can Be
Measured Using Downsampled Data

SFDR Via Downsampling Example



Harmonic Distortion Sensitivity



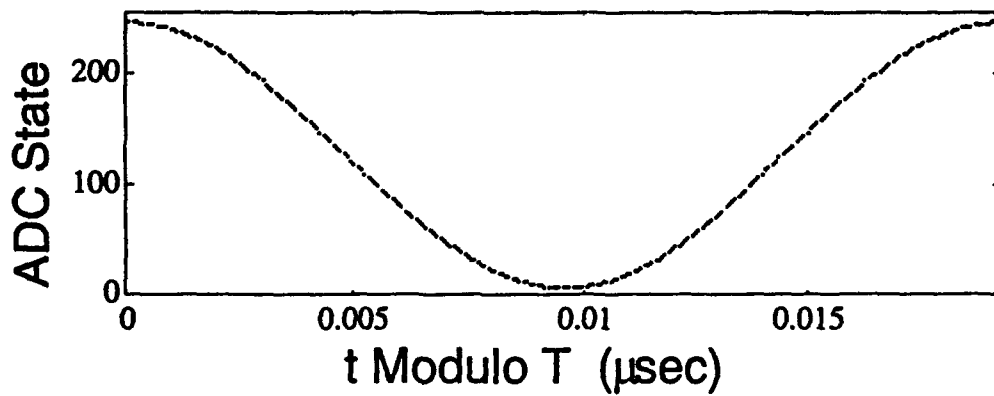
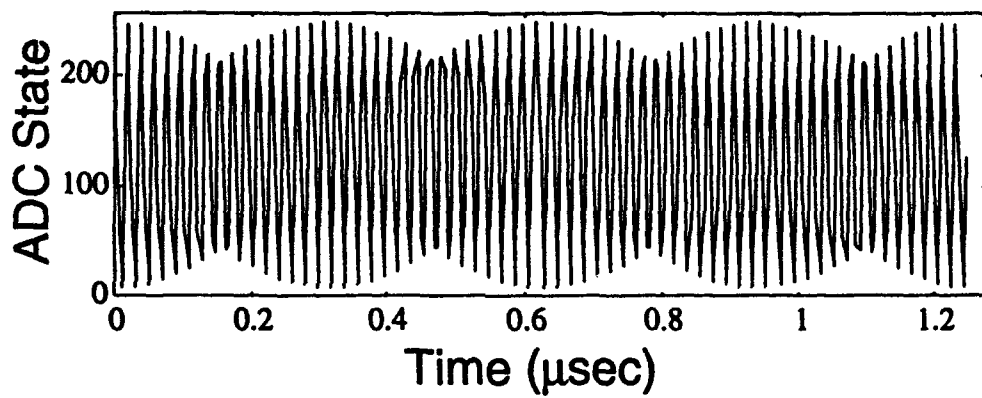
3.3 Harmonic Distortion Sensitivity

The previous vugraph illustrates that custom, non-standardized tests can be developed to obtain characterizing information for an ADC. The results shown in this example show second and third harmonic distortion components measured over ten minute intervals for an ADC subject to 90% sinewave loading. The results are shown as a function of a changing -5.2 V bias supply (V_{BI}) to the ADC. The supply is incremented in 0.1 V steps over the ADC rated bias tolerance range. The result shows that the odd harmonic is statistically repeatable whereas the even harmonic has a statistical bias that is correlated to the V_{BI} supply. Note that a ± 0.2 V 120 Hz ripple could easily be present on V_{BI} when it is delivering several Amps to a load. One has to be careful about power supply selection for biasing wide dynamic range ADCs. Since the distortion component represents a full LSB of error, the ADC could not be calibrated reliably to remove distortion without putting tighter restrictions on the V_{BI} supply or finding and correcting the source of error in the ADC circuit.

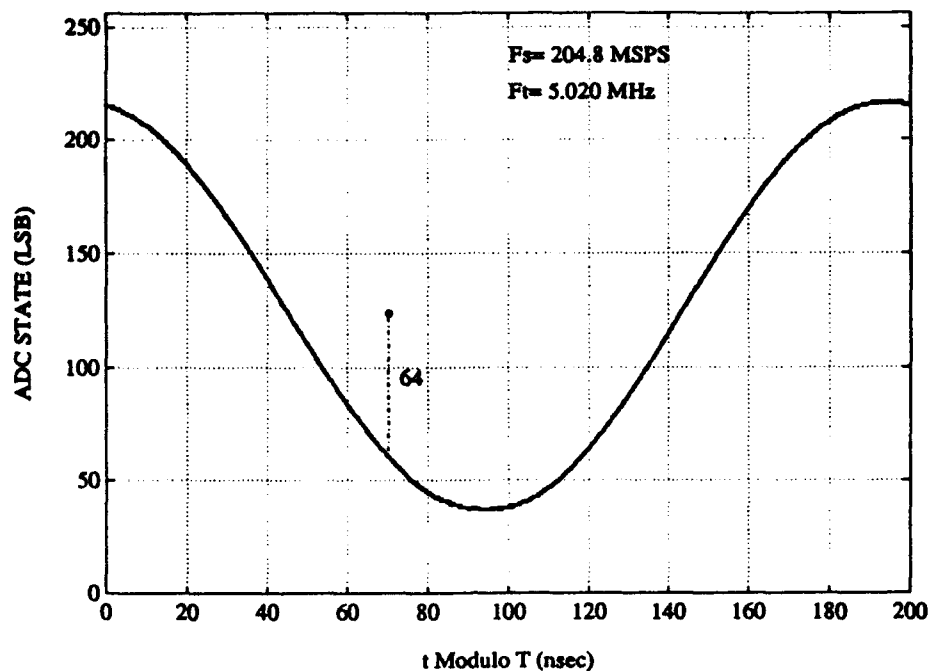
3.4 Modulo Time Plots

This series of vugraphs is used to show how time domain plots of sampled data can be used to obtain diagnostic results that are not evident through usual spectral analysis (DFT) procedures. The first graph shows a typical plot of samples taken and plotted versus sample time for a sinewave test signal. The result is an unintelligible sequence of data (normally looks like a solid bar of "grass") due to the modulation of the test signal frequency with the sum and differences of the ADC sample frequency. The data do not reveal much useful information in this form. However, when the data are reordered and plotted versus sample time modulo the period of the test signal, then the data form one full period of a sinewave (if everything is functioning properly). This plot clearly indicates the amplitude, phase, and offset of the test sinusoid but it should be noted that it is required to know the test frequency period very accurately. The requirement of knowing the period is not a problem for those test procedures that use synchronized synthesizers as is usually the case for these test systems. The next vugraph shows an example of the detection of a single bit error in a data set by means of a time modulo plot. The erroneous sample stands out clearly from the sinewave shape required by the test. Because the difference is exactly $64 = 2^6$, the error in the sample can be traced to a single bit error. In this case the error was caused by reflection mismatches of data on the interface to the data acquisition unit and was not due to the performance of the ADC. The corresponding spectrum for this data set is shown in the adjacent graph. The result looks quite clean for an 8-bit ADC and so it might normally be concluded that "all is well" if the spectral measure was the only method used to evaluate the ADC.

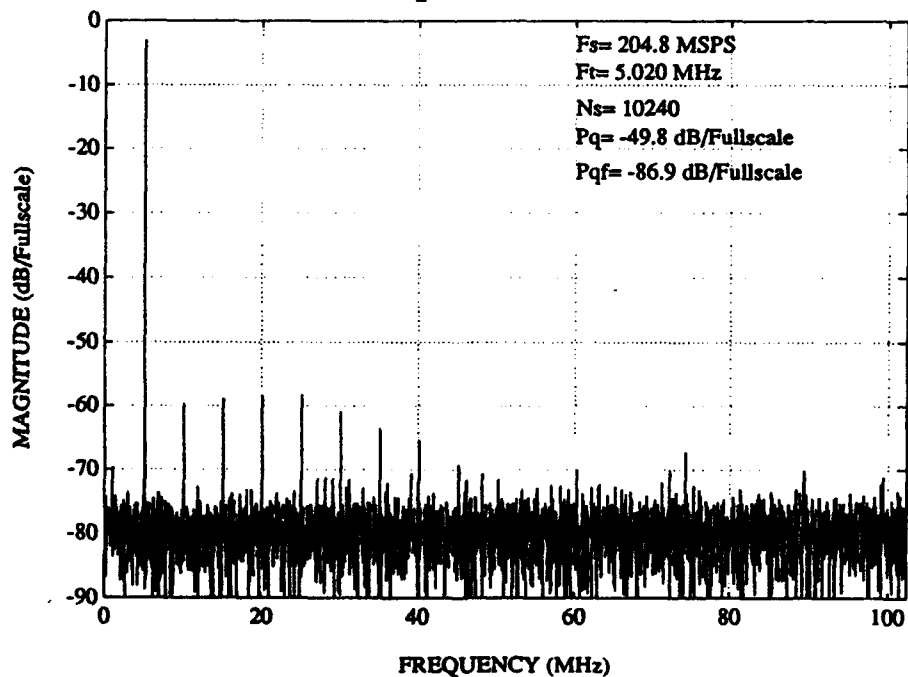
Modulo-Time Plots



Detection of Bit Errors



Spectrum For Single Error Sample Set

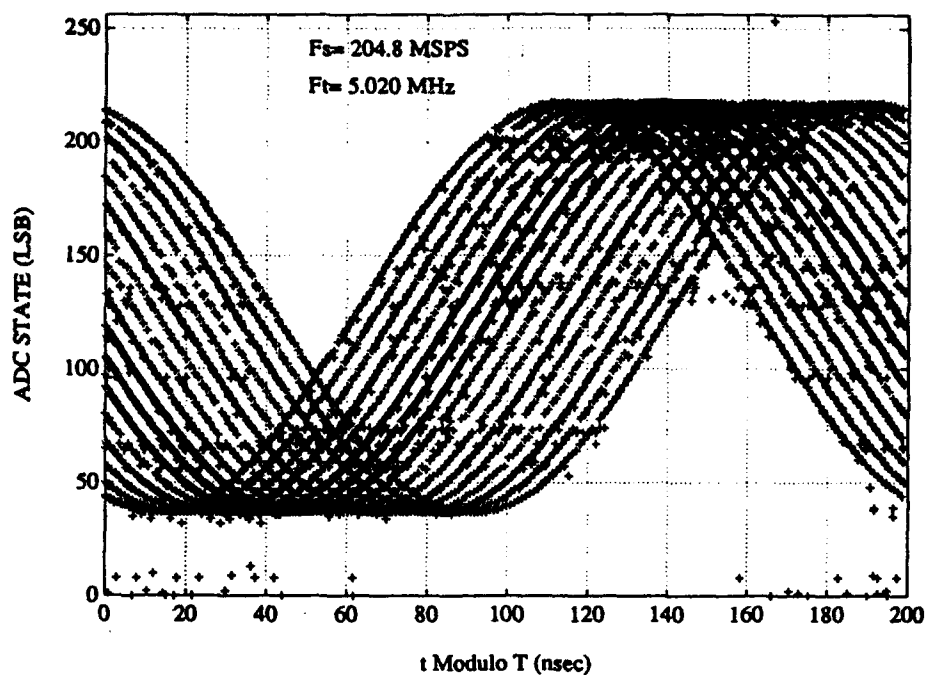


Note that neither a Histogram nor a Differential Non-linearity test would find anything wrong with this example set of data either. However, careful inspection of the spectrum shows that the "average" noise level is on the order of -80 dB/FS rather than the expected level of -86.9 dB/FS. Thus it is seen that the single bit error - which is similar to an impulsive error - has added a small amount of wide band noise across the full spectrum.

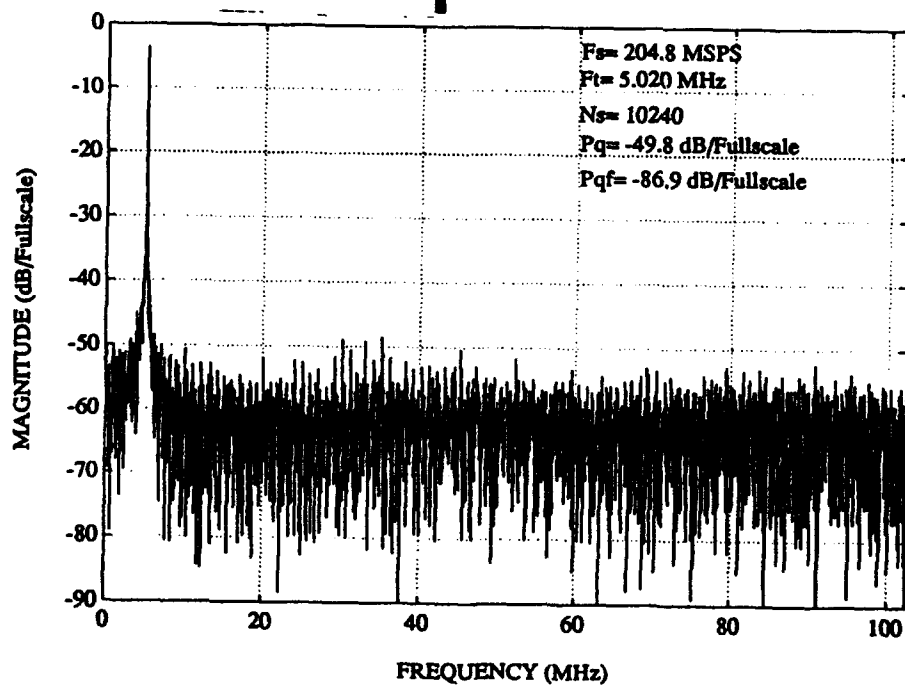
A final time domain example is shown in the following Detection of Timing Error vugraph. There it appears that the test sinusoid is "shifting" or "walking" across the plot; i.e., it keeps changing phase with respect to the clock. In addition, there are several samples that do not fit any of the sinusoids thus displayed. There are many data errors. The problem is traced to the clock driver on the buffer that drives the interface to the data acquisition unit at the output of the ADC evaluation board. The mismatched clock signal, with its attendant reflections, presents an unreliable waveform to the line receiver and so it periodically makes decision errors on whether or not it has seen a "high" or "low" logic level. The time-modulo plot unfolds what is otherwise an unintelligible data stream into the understandable result shown in the graph. The spectral response for this set of samples is shown in the adjacent graph for comparison purposes. The response is clearly a single tone response with little or no visible harmonic distortion, but the average noise level is nearly 27 dB above the expected level for an ideal 8-bit ADC with the given number of samples. The spectral response has a near 50 dB dynamic range, which is good for most 8-bit flash converters, and so one might conclude that the converter was working alright based on the spectrum data by itself.

The point of these examples is to show that both time and frequency domain responses are necessary tools to help determine completely proper operation for an ADC. This is especially true for high speed ADCs where the timing and matching of the signal lines is of high importance to reliability in the transmission and reception of digital data. The time modulo plot is a useful procedure to arrange the time domain samples into an expected shape so that it is possible to visually observe improper performance of both the ADC and the data acquisition system. Furthermore, the result which is easy to see in the modulo time domain is often not readily apparent by spectral analysis methods. The examples also serve to show that improper performance is not always due to just the ADC but it may be affected by interface circuitry in timing, terminations, and other line driver-receiver problems with high-speed data.

Detection of Timing Errors



Spectrum For Timing Error Sample Set



3.5 ADC Error Modeling

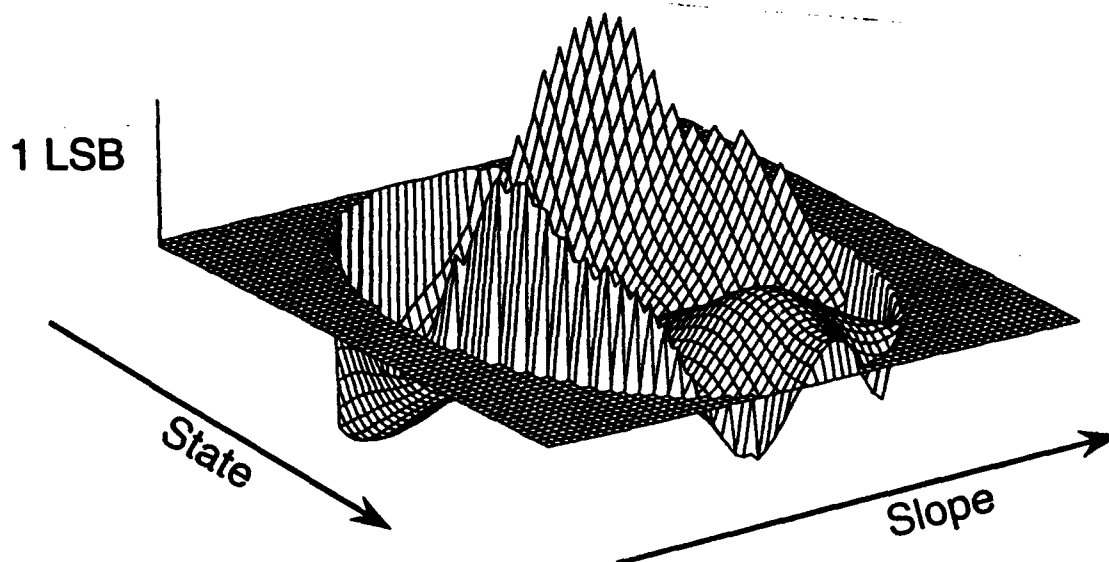
It has been known for some time (see D.Asta and FH Irons, "Dynamic Error Compensation of Analog-to-Digital Converters", The Lincoln Laboratory Journal, Vol.2, No.2, 1989, pp.161-182) that the dynamic performance of an ADC can be measured and corrected using lookup tables to store errors. The surface shown in the vugraph represents such a function for a 25 MSPS 12-bit ADC. Note that the error is stored as a function of the ADC state and slew rate (slope) at each sample time. A typical correction response for a near full scale loading is shown in the adjacent example Dynamic Compensation graph of SFDR versus operating frequency. An improvement of more than 6 dB (one bit) is achieved over about one half of the Nyquist bandwidth. It turns out that different error mechanisms, such as amplitude compression or amplitude dependent jitter, affect the error table in different ways. Thus it is expected that the use of measured dynamic error tables, together with ADC models, will provide a useful role in diagnosing ADC performance for different architectures and error mechanisms. The University of Maine is currently conducting research and training students in the measurement and use of dynamic error models so as to better understand how ADC nonideal performance is both measured and characterized. It is expected that these techniques will provide assistance and understanding for obtaining expected behavior for different architectures and phenomena.

4. Conclusion

This report has presented a full description for the results and accomplishments by the University of Maine under the subject grant for the period of 1 Aug through 30 Oct 1993. The report explains how the following objectives were accomplished.

- i. Meet with MIT Lincoln Laboratory and the Mayo Foundation to plan the September Workshop held at MIT Lincoln Laboratory. The purpose of the workshop was to address packaging and testing issues for the candidate ADCs being developed under the ARPA HBT/ADC program.
- ii. Participate in the workshop.
- iii. Document the accomplishments for the first quarter participation in the program.

ADC Error Characterization



Dynamic Compensation

