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13. ABSTRACT *(Maximum 200 words)*

Our results indicate that excellent passivation of SiN_x/GaAs and SiN_x/InP interfaces can be achieved using both liquid and gaseous sulfur treatments of the surface. It is important to note that the S-treated surfaces are stable in the presence of an 'soft' ECR plasma and are amenable to the environment of SiN_x growth. Annealing appears to be a crucial step in achieving lower defect densities at the SiN_x/III-V interfaces. A significant reduction in the interfacial defect density leads to unpinning of the Fermi-level at the interfaces. This permits fabrication of superior metal-semiconductor (both Schottky and ohmic) junctions and metal-insulator-semiconductor FETs. Furthermore, reduction of defects at the interface also reduces the surface recombination velocity, thus improving the performance of minority carrier based devices. We have demonstrated that such is indeed the case by passivating AlGaAs/GaAs based heterojunction bipolar transistors and surface-emitting lasers.

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Final Report

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1.0 Statement Of The Problem Studied

For numerous devices, it is imperative to fabricate surfaces and interfaces with a low number of electronic defect states located in the energy bandgap of the material. The presence of large defect state densities at the surface or interface causes Fermi level pinning and also results in high surface recombination velocity that adversely effects the performance of devices. In the case of GaAs, the surface defect density and the surface recombination velocity may be as large as 10^{13} cm^{-2} eV^{-1} and 10^{6} cm/s, respectively. Presently, acceptable device quality interfaces in GaAs are produced using epitaxial films of AlGaAs. However, there are several devices, including lasers and heterojunction bipolar transistors (HBTs), where a good quality 'passivated' interface between the semiconductor and an electrochemically robust dielectric material would greatly simplify the process flow and enhance the performance and reliability of ICs. Furthermore, for some devices such as metal-insulator field effect transistors (MISFETs) good dielectric/III-V interfaces are absolutely essential. Despite a tremendous research effort for many years, passivation of dielectric/III-V surfaces has been unsuccessful in the past.

Recently, novel sulfide solution treatments have been proposed which help improve passivation of III-V surfaces. However lack of understanding of the mechanism, the reproducibility and uniformity of the processes, and the stability of the treated surfaces have been severe bottlenecks with this technique.

During this research project, the main objectives were to develop reproducible, uniform, and stable processes for improved passivation of GaAs and InP surfaces and devices. Our approach and ideas for addressing the problems associated with the passivation of dielectric/semiconductor interfaces were outlined in the original proposal. In the next sections, a brief description of the tasks and a summary of the results and accomplishments are presented.

The areas that were explored during the project period were the following:

1. Development of novel GaAs and InP surface passivation techniques using sulfide solution and gaseous/plasma H_2S treatments.
2. Auger/XPS analysis and determination of the composition of the treated surfaces; identification of the chemical bonding nature of the S-GaAs surfaces.
3. Laser Raman spectroscopy measurements to determine the surface barrier height and the extent of surface Fermi-level "pinning" of the S-treated samples.
4. Development of processes for in-situ, low-damage SiN_x deposition using 'soft plasmas', and encapsulation of the S-treated surfaces with SiN_x. This was important because the beneficial effects of sulfur treatments, without a suitable encapsulation, deteriorate rapidly upon exposure to atmospheric ambient.
5. Fabrication and characterization of metal-dielectric-(S-treated) GaAs (or InP) structures.
6. Auger/XPS study of dielectric-(S-treated) GaAs (or InP). Identification and analysis of the effects of dielectric deposition on the chemical and electronic properties of the treated interfaces.
7. Passivation of the facets of AlGaAs/GaAs-based semiconductor lasers.
8. Passivation of mesa AlGaAs/GaAs-based HBTs.

2.0 Summary Of Results And Accomplishments

2.1 Passivation using sulfide solutions and H_2S

We have successfully developed processes, using sulfide solutions and H_2S treatments, which help passivate the surface defects in GaAs and InP. The 'wet' technique involves the use of liquid ammonium sulfide solutions with excess sulfur and phosphorous pentasulfide. Excellent passivation of dielectric/n-InP and metal/n-GaAs interfaces have also been achieved using gaseous H_2S treatments. The H_2S-treatments result in slightly higher defect densities at the SiN_x/InP interfaces compared to the 'wet' treatments. On the other hand, H_2S-treatments appear to be superior for the passivation of metal/n-GaAs interfaces.

The H_2S treatments provide considerably superior uniformity and reproducibility compared to the treatments involving liquid sulfide solutions. This is an important result because the use of these techniques, beyond the research laboratories, will depend upon these criteria.

Recently, we have also developed novel processes using selenium sulfide solutions and H_2/H_2S plasmas, both of which appear promising for the passivation of GaAs surfaces.

2.2 Angle resolved XPS and Auger analysis of S-treated surfaces GaAs and SiNx/GaAs interfaces

Sulfur bonding to etched GaAs surfaces which have an As/Ga ratio ranging from 0.6 to 6.0 were studied. The source of the sulfur was either a liquid solution of Na_2S or $(NH_4)_2S$ or gaseous H_2S applied in a N_2 purge glove box. XPS spectra was obtained from ~ 40 different samples in order to determine the concentration of the various surface chemical species and their bonding state. Most of the experiments were conducted with H_2S exposed samples at substrate temperatures from 30 to 350 C. These experiments indicate that sulfur bonds to both Ga and As. The amount of bonding to each depends on the As/Ga ratio. This is true for both H_2S and the liquid S solutions. Only one S-As bonding state (ΔBE = 1.6 eV) was observed, independent of the S treatment process. S was observed to bond to elemental As and substrate As with the same binding energy and concentrations. H_2S exposed surfaces had two to three times higher concentration of S than did those that were treated with Na_2S or the $(NH_4)_2S$. In H_2S atmosphere, elemental As is removed from the GaAs surface at a lower temperature than in a vacuum. We suspect that this is caused by the formation of AsH_3.

The AES sputter profile for the H_2S- and S-treated SiN_x/GaAs samples were also measured. The profiles show a significant S peak at the SiN_x/GaAs interface. The polysulfide treated sample showed only about 1/2 the amount of sulfur at the interface. Both profiles show a considerable amount of oxygen content in the SiN_x film and at the interface. XPS analysis of As and Ga 3d lines showed no evidence of As-O bonding. Sputter mixing and readsorption effects prevent our full confidence in the high resolution curve fits required to determine the sulfur bonding. However, the data seems to indicate that there are both As-S and Ga-S bonds at the interface.

2.3 Design and construction of class-100 clean room and ECR-PECVD system

To provide the appropriate laboratory space and infrastructure needed for research, the College/University appropriated funds to build approximately 400 sq. ft of class 100 clean room. During the year 1990-1991, the clean room was designed and built under the PI's supervision. During this time, we also designed and custom-built a multi-chamber, ECR-PECVD system. A schematic diagram of the system is shown in Fig. 1. The system has three vacuum chambers, two of which are pumped to ultra-high vacuum regimes. The surface preparation chamber is used for in-situ cleaning and gaseous (using hydrogen sulfide) passivation of III-V surfaces and devices. The deposition chamber allows the growth of dielectric thin films, such as SiN_x. With the present configuration of the system, films such as silicon oxide, silicon oxynitride and amorphous silicon can also be grown. The system is also equipped with probes for in-situ photoluminescence (PL) and electrical measurements.

2.4 Development of soft-plasma, low-damage SiN_x deposition processes using ECR-PECVD

Using the ECR-PECVD technique, we have developed processes for low temperature (< 200 C) growth of high-quality silicon nitride thin films on GaAs and InP. The process parameters have been carefully controlled to create 'soft' plasma conditions during deposition, thus permitting good quality SiN_x/GaAs and SiN_x/InP interfaces. We believe this has been a significant accomplishment, especially because conventional PECVD processes can cause severe plasma-induced damage to the surface. Ability to achieve passivation necessitates the use of soft plasmas with low ion energies, which then help fabricate smooth and defect-free interfaces.

The typical process parameters during the deposition of nitride films, which result in good SiN_x/III-V interfaces, are the following: plasma power ~ 200 W, SiH_4/N_2 flow rate ratio ~ 1:10, and chamber pressure ~ 20 mtorr. The deposition rate of the dielectric film under these conditions was found to be only 20 A/min. The refractive index at 632.8 nm, measured using Rudolph AutoEL IV ellipsometer, of the deposited films was ~ 1.87. The dielectric breakdown strength and the relative permittivity are approximately 3-5 MV/cm and 6.33, respectively. The etch rate of the films in 10:1 DI:HF solution is approximately 60 A/s. The AES, Rutherford Backscattering, FTIR and stress measurements were also carried out. This work was done in collaboration with Dr. K. L. Seaward at the Hewlett Packard Laboratory, Palo Alto, California. The AES data indicates Si, N and O content in the films to be 44 %, 53%, and 4 %, respectively. The stress in the films was found to be ~ 3.6×10^9 dynes/cm^2. FTIR spectroscopy measurements indicate the following : N-H ~ 2.1×10^{21} cm^{-3} and Si-H ~ 4.0×10^{21} cm^{-3}.

2.5 Stable, uniform, and reproducible passivation of InP

We have achieved excellent passivation of the InP surface using sulfide-treatments followed by the growth of an over-layer of ECR-PECVD silicon nitride; the conditions of SiN_x deposition are the same as described above. The

PL signal for the sulfide-treated SiN_x/InP interface is approximately 10 times larger than the untreated samples. The capacitance-voltage characteristics, as shown by the solid line in Fig. 2, of S-treated Al/SiN_x/InP devices indicate that the interface is indeed well-passivated. The characteristics exhibit excellent agreement with the ideal C-V characteristics, plotted using the vendor's suggested doping density of 5 x 10^{15} cm^{-3}. Accumulation and inversion at the InP surface were easily achieved, with the Fermi level scanning ~ 0.85 eV of the bandgap in the voltage range from -5 to 5 V. Excellent passivation of the InP surface has also been achieved using in-situ gaseous H_2S-treatment. The C-V characteristics of the Al/SiN_x/InP devices, where the InP surface was exposed to H_2S at 150 C prior to the SiN_x deposition, is also shown in Fig. 2 (dashed line). The defect densities, estimated using Terman analysis, at the passivated SiN_x/InP interfaces are in the range of low 10^{11} cm^{-2} eV^{-1}. *To the best of our knowledge, these values for SiN_x/InP interfaces are among the best reported in literature to date.*

2.6 Stable, uniform, and reproducible passivation of GaAs

Passivation of the GaAs surfaces has also been achieved using sulfur, selenium-based solutions and H_2S gaseous treatments. The Schottky diodes fabricated on S- and Se-treated GaAs surfaces exhibit considerable improvement in performance. The reverse leakage current in Au/n-GaAs diodes reduce by approximately two to three orders of magnitude. The Schottky barrier height is increased by a value ranging from 0.1 to 0.15 eV. Similarly, the Al/n-GaAs contacts fabricated using wet chemical treatments exhibit approximately three orders of magnitude increase in the reverse current and a reduction in barrier height from ~ 0.75 eV to ~ 0.58 eV. These results indicate that the sulfide- and H_2S-treatments are effective in improving the properties of Au (or Al)/n-GaAs interfaces.

Stable passivation of SiN_x/GaAs interfaces has also been achieved using a process developed in our laboratory. Historically, passivation of dielectric/GaAs interfaces have been very difficult. Fig. 3 shows the representative C-V data for a S-passivated Al/SiN_x/n-GaAs device. Using the quasi-static data, which exhibits a significant dip in going from accumulation to inversion, it is estimated that the Fermi-level scans approximately ~0.83 eV of the energy bandgap of the semiconductor. In addition, the high-frequency capacitance measured at both 100 KHz and 1 MHz are considerably superior compared to the untreated samples. The characteristics exhibit some frequency dispersion, and in the range of +7 to -7 V, the hysteresis (not shown in the figure) is typically about 2 V. The dopant density in the GaAs substrate, estimated using the theoretical best-fit of the minimum capacitance, is 2 x 10^{16} cm^{-3} which lies well within the range of values suggested by the vendor. The MIS devices that were not treated with the sulfide solution exhibit nearly flat quasi-static and high-frequency C-V characteristics suggesting that the Fermi-level is strongly pinned at the SiN_x/GaAs interface. Such a behavior is typical of SiN_x/GaAs interfaces which have very high density of electronic defects at the interface.

The electrical properties of the S-passivated SiN_x/GaAs interface strongly depend upon the annealing temperature. The effects of annealing at 220, 300, 400 and 500 C temperatures on the C-V characteristics are shown in Fig. 4. Although the figure shows the 100 KHz C-V data only, similar improvements in the 1 MHz and the quasi-static C-V characteristics are also observed. The devices show a substantial improvement with increasing temperature, with the

device annealed at 500oC exhibiting the least amount of 'stretch-out' and the largest change in capacitance. The data indicates lowering of the interfacial defect density due to increasing annealing temperature. Annealing appears to be a crucial and essential step in achieving passivation. The MIS devices which were not treated with the sulfide solution indicate worsening of the SiN_x/GaAs interface with increasing annealing temperature.

2.7 Passivation of AlGaAs/GaAs HBTs

We have passivated 36 x 36 μm^2 AlGaAs/GaAs HBTs, provided by HP Laboratories, Palo Alto, using the 'wet' sulfide solution treatments followed by the deposition of ECR-PECVD SiN_x overlayers. The sulfide-treatment and SiN_x deposition were done under similar conditions as those for the fabrication of MIS devices.

Fig. 5 shows the current gain, β, versus the collector current, I_c, characteristics at various stages of processing. The curve A is a for a device which did not receive any passivation treatment, whereas curve B is for the device after the S-treatment and the deposition of the SiN_x overlayer. It was observed that although there is a significant improvement in the gain of the device after dipping into the sulfide solution, this effect is completely lost after SiN_x is deposited. The curves A and B are practically identical. However, as a result of annealing at 300 C in N_2 ambient for 30 minutes, there is an improvement in the gain of the transistor, as shown by curve C. This device was then allowed to remain in room ambient and the characteristics were measured again after 1 day (shown as curve D) and then 10 days (shown as curve E). The same device was then annealed at 400 C, which resulted in further improvement of the device characteristics; the enhancement in the gain of the transistor in the low collector regime is shown by curve F. The increase in the gain of the transistor with increasing anneal temperature is consistent with the results obtained on MIS devices. As discussed earlier, annealing plays an important role in reducing the defect density at the SiN_x/S-GaAs interface.

Fig. 6 shows the Gummel plot of the device before and after passivation. The characteristics labeled as 'unpassivated' and 'S-passivated' are for the transistor exhibiting the curves A and F in Fig. 5, respectively. The ideality factors for the characteristics representing I_c and I_b are approximately 1.05 and 2.0, respectively. There is a significant reduction in the base current after passivation, with the ideality factor reducing by approximately a factor of 2 compared to the unpassivated devices. The data indicates superior passivation of the mesa surface walls of the transistor.

2.8 Passivation of Vertical-Cavity Surface-Emitting Lasers (VCSEL)

We have achieved excellent passivation of VCSELs using sulfide solutions and SiN_x overlayers. The unpassivated devices were obtained from the University of California, Santa Barbara, California. Fig. 7 shows the cross-section of the device, and also the L-I curves for four 8.0 μm diameter VCSELs which were subjected to different process treatments. Sample A was cleaned with dilute NH_4OH, and ~ 1500 A of SiN_x was then deposited at 200 C using the ECR-PECVD technique. Sample B, after the initial cleaning step, was treated with $(NH_4)_2S_x/P_2S_5$ solution prior to SiN_x deposition. Sample C underwent the same process as sample B, except that this device was also annealed at 300

C in N_2 ambient. In the case of Sample D, after the S-treatment, the device was also treated with (NH_4OH) solution containing 0.2 g of As_2S_3. As a result of this treatment, the sample was coated with a crust of As-S layer, which was then removed by heating the device at ~ 250 C in the ECR-PECVD system prior to the deposition of SiNx.

As seen in the figure, the threshold current was reduced for all the three passivation techniques, and the peak CW output power was increased over the control device for sample D. A minimum threshold current of 0.67 mA was observed for the best 8 micron device, while a power output of over 1.2 mW CW was achieved. The minimum published threshold current for a VCSEL is 0.65 mA, but this is for a device with very high reflectivity mirrors; a design which reduces the threshold current at the cost of reducing the peak power output to the microwatt range. The larger devices showed more substantial improvements in output power, with the peak CW power output of the 20 μm diameter devices increasing from 3.5 mW to over 5.0 mW for the best devices. Fig. 8 shows the dependence of the threshold current density on the perimeter/area ratio of the device. As seen in the figure, the threshold current density for the smallest devices (8 μm dia.) drops from ~ 2 KA/cm2 to ~ 1.5 KA/cm2 with passivation. Detailed analysis of the data suggests that 25 % reduction in the surface recombination velocity occurs as a result of passivation. Although detailed life-testing has not been carried out on these devices, the passivation appears to be stable for a period of several months.

2.9 Summary

In summary, our results indicate that excellent passivation of SiN_x/GaAs and SiN_x/InP interfaces can be achieved using sulfur treatment of the surface. It is important to note that the S-treated surfaces are stable in the presence of an 'soft' ECR plasma and are amenable to the environment of SiN_x growth. Annealing appears to be a crucial step in achieving lower defect densities at the SiN_x/III-V interfaces. A significant reduction in the interfacial defect density leads to unpinning of the Fermi-level at the interfaces. This permits fabrication of superior metal-semiconductor (both Schottky and ohmic) junctions and metal-insulator-semiconductor FETs. Furthermore, reduction of defects at the interface also reduces the surface recombination velocity, thus improving the performance of minority carrier based devices. We have demonstrated that such is indeed the case by passivating AlGaAs/GaAs based heterojunction bipolar transistors and surface-emitting lasers.

3.0 On-going research

Our on-going research involves development of superior processes for passivation of III-V surfaces, integration of these processes in conventional device fabrication technology, and detailed electrical and reliability characterization of the passivated devices. Due to the wide ranging application and significance of passivation in III-V ICs, there are several laboratories who have begun to collaborate with us on the project. A brief description of these projects are listed below:

a) HP Research Laboratory (Drs. S. Camnitz, K. L. Seaward and V. Malhotra): Passivation of HP's AlGaAs/GaAs HBTs and HBT-based integrated circuits. It is anticipated that this research will assist HP in the design and fabrication of high-performance AlGaAs/GaAs integrated circuits, including mixers and oscillators. In support of the work to be done at UH, HP has recently awarded an equipment grant to our group here at the University of Hawaii. This grant will help improve our capabilities for DC characterization of devices.

b) University of California, Santa Barbara (Drs. B. Young, L. A. Coldren and V. Malhotra): Passivation of GaAs-based near IR surface-emitting lasers. We are collaborating with this UCSB group for passivation of their surface-emitting lasers.

c) US Army Electronics Technology and Device Laboratory (Drs. J. Flemish and V. Malhotra): Passivation of GaAs MESFETs and MMICs. For the GaAs-based MESFETs, currently being developed at the US Army Research Laboratory, there is a need for the development of a suitable passivation technology for the devices. Due to the lack of suitable SiN/GaAs interfacial properties, a substantial reduction in the saturation current density and the gate breakdown voltage is observed. This is having an adverse impact on further development of MMIC-based technologies. A research collaboration with the scientists at the laboratory is underway and we hope to be able to assist the Army laboratories in SiN/GaAs interface passivation.

d) National Renewable Energy Laboratory (Drs. A. Nelson and V. Malhotra): Auger/XPS characterization of S-passivated SiN/InP interfaces. We are conducting experiments to study the chemical compositions of sulfur-passivated SiN/InP interfaces. A joint publication on our recent work is under preparation.

e) Colorado State University (Drs. C. W. Wilmsen and V. Malhotra): Passivation of a variety of optoelectronic devices such as MSM photodetectors and phototransistors.

4.0 Scientific personnel supported during the project period

1. V. Malhotra	Principal Investigator
2. A. Kapila	Research Assistant, completed M. S. degree in Electrical Engineering, Nov. 1993, Thesis: "Surface passivation of III-V compound semiconductors"
3. X. Si	Research Assistant, anticipated completion of M.S. degree, Jan 1994 Thesis title (tentative): "S-passivation of GaAs surface and GaAs-based devices "
4. Giles Thompson	Research Assistant
5. X. Chen	Post-doctoral fellow
6. C. Wilmsen	Subcontract to Colorado State University

5.0 Publications

Chapters in Books

1 V. Malhotra and C. W. Wilmsen, "Passivation of InP and GaAs" ed. G. E. McGuire and P. H. Holloway (to be published by Noyes Publications).

Other publications

2 A. Kapila, V. Malhotra, L. S. Camnitz, K. L. Seaward and D. Mars, "Passivation of GaAs surfaces and AlGaAs/GaAs HBTs using sulfide solutions and SiNx overlayer (in preparation).

3 D. B. Young, A. Kapila, J. W. Scott, V. Malhotra, and L. A. Coldren, "Reduced threshold vertical-cavity surface emitting lasers," submitted to Electronic Letters

4 A. Kapila, X. Si, and V. Malhotra, "Passsivation of dielectric- and metal-GaAs interfaces using (NH4)2Sx and gaseous H_2S," submitted to Appl. Phys. Lett.

5 A. Kapila, "Surface passivation of III-V compound semiconductors," M. S. Thesis, University of Hawaii, November, 1993.

6 A. Kapila, X. Si, and V. Malhotra, "Electrical Properties of SiN_x/InP interface passivated using H_2S," Appl. Phys. Lett., 62 (18), pg. 2259, 1993.

7 A. Kapila and V. Malhotra, "Passivation of the InP surface using polysulfide and silicon nitride overlayer," Appl. Phys. Lett., 62 (9), pg. 1009, 1993.

8 X. Chen, X. Si, and V. Malhotra "Measurement of reduced surface barrier in sulfur passivated InP and GaAs using raman spectroscopy, J. Electrochem. Soc., vol. 140, 7, pg. 2085, 1993.

9 A. Kapila, X. Si, V. Malhotra, "Effects of wet and dry S-treatments on the electrical properties of SiNx/InP interface" Proceedings of the SOTAPOCS, 183rd Electrochem. Soc. meeting., May 16-21, Honolulu, 1993.

10 X. Si, A. Kapila, V. Malhotra, K. M. Geib, and C. W. Wilmsen, "Properties of ECR-PECVD SiNx and sulfur-treated SiNx/GaAs interface", Proceedings of the SOTAPOCS, 183rd Electrochem. Soc. meeting., May 16-21, Honolulu, 1993.

11 A. Kapila, X. Si, V. Malhotra, "Sulfur passivation of InP and GaAs," presented (and published in the Proc.) Materials Research Society Spring Meeting, April 12-16, San Francisco, 1993.

12 J. Shin, K. M. Geib, and C. W. Wilmsen, "Sulfur bonding to GaAs," J. Vac. Sci. Technol. B 9 (4), pg. 2337, 1991.

13 X. Chen and V. Malhotra, "Reduced surface barrier heights in chemically passivated GaAs and InP," presented at the 38th American Vacuum Society symposium, Seattle, Nov. 11-15, 1991.

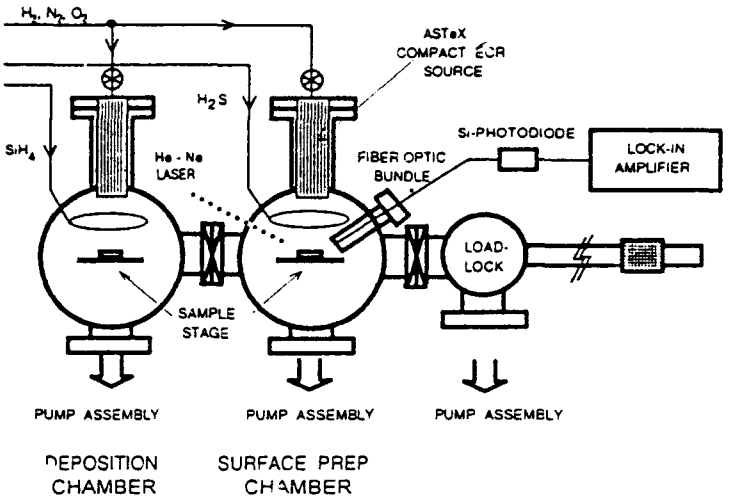
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Fig. 1

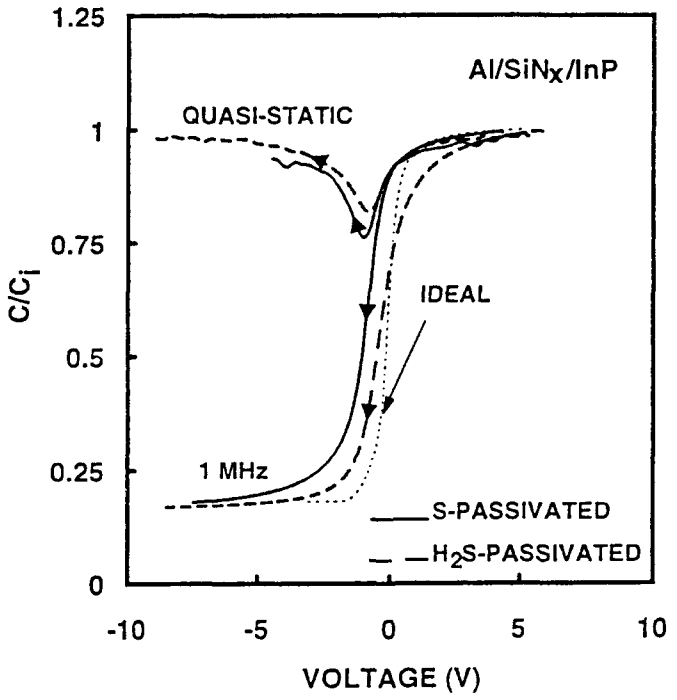
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Fig. 2

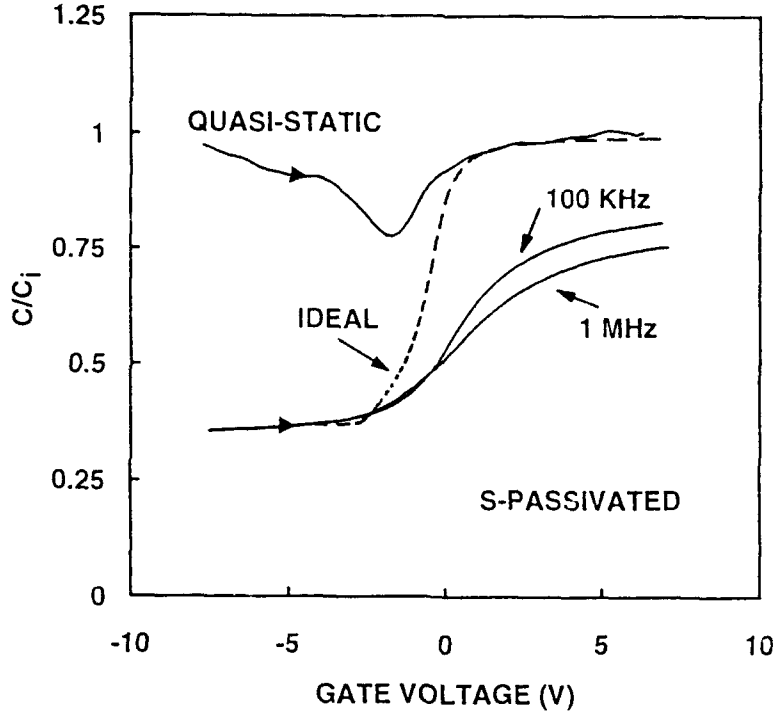
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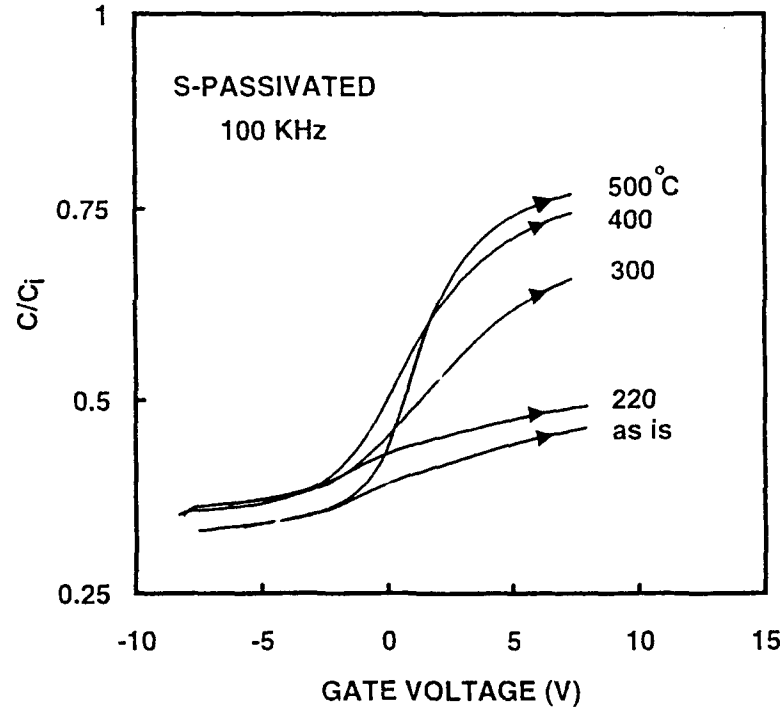
Fig. 3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GATE VOLTAGE (V)

Fig. 4

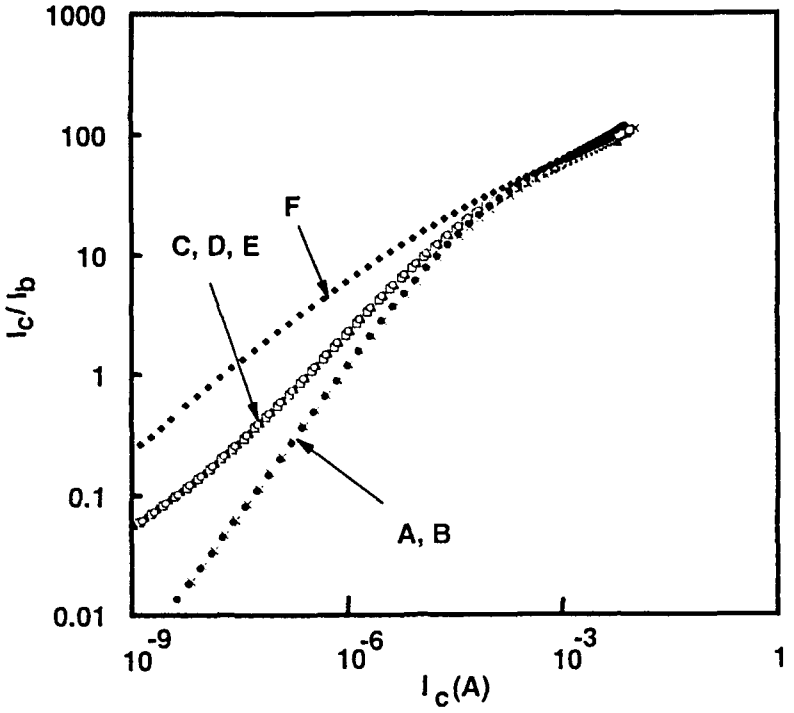
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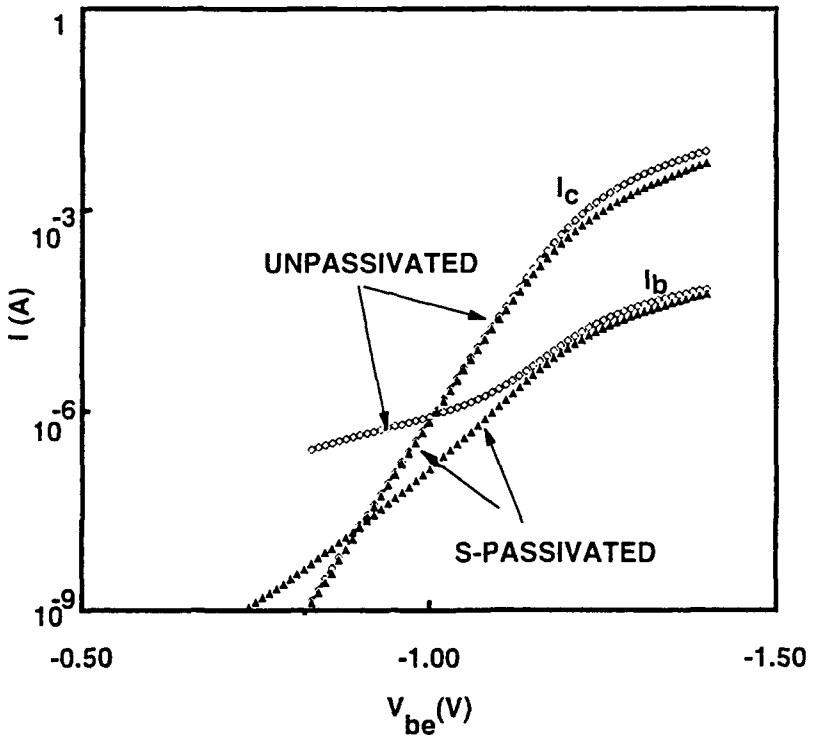
Fig. 5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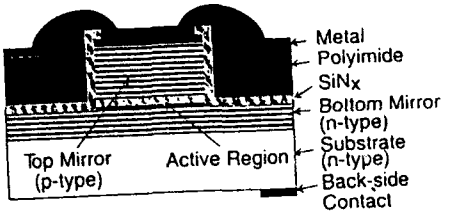
V_{be}(V)

Fig. 6


Metal
Polyimide
SiN_x
Boltom Mirror
(n-type)
Substrate
(n-type)
Back-side
Contact
Top Mirror
(p-type)
Active Region

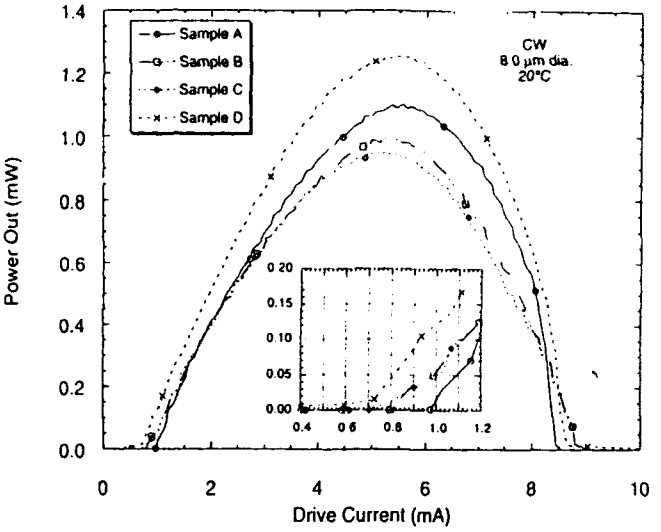

Sample A
Sample B
Sample C
Sample D
CW
8.0 μm dia.
20°C
Power Out (mW)
Drive Current (mA)

Fig. 7

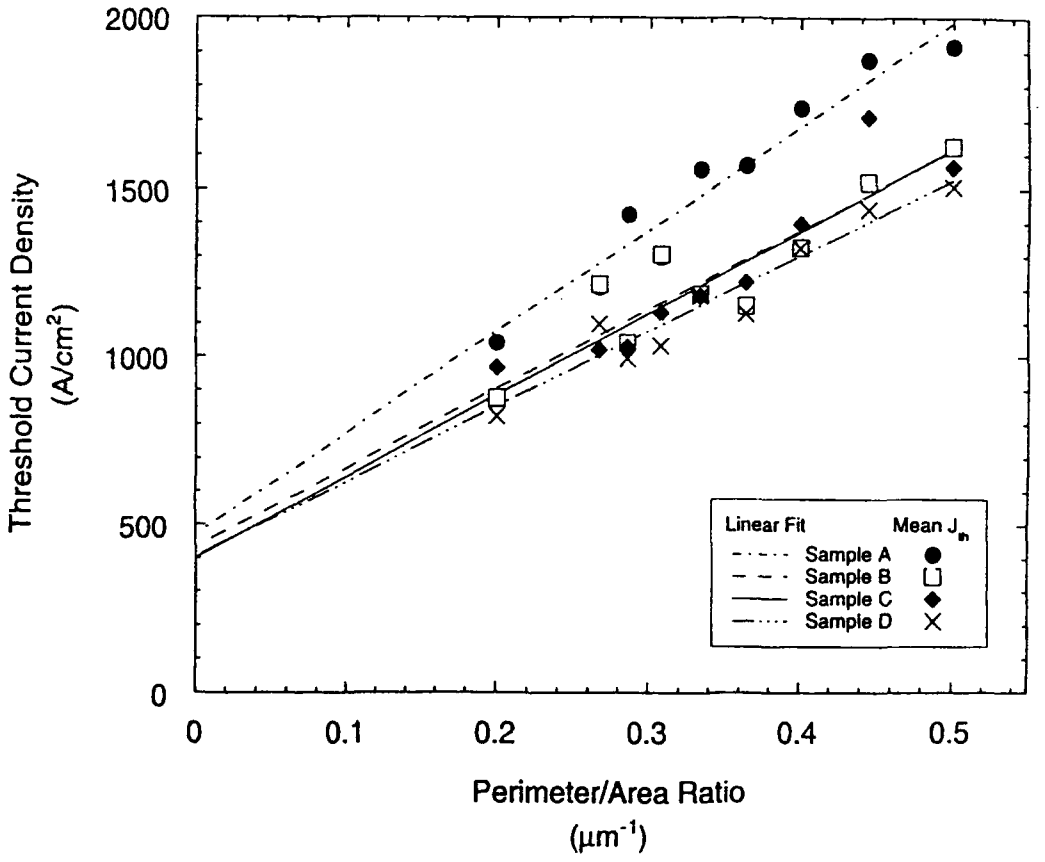

Threshold Current Density
(A/cm²)
Perimeter/Area Ratio
(μm⁻¹)
Linear Fit
Mean J_{th}
Sample A
Sample B
Sample C
Sample D

Fig. 8