AD-A277 158

RELIABILITY MANAGEMENT THROUGH SELF-TESTING

DTIC
S ELECTE
MAR 23 1994
F D

FINAL REPORT
January 1992

SDIO/IST
ONR

(4/1/1986-12/31/1991)

PI: Yashwant K. Malaiya

Colorado State University
Fort Collins CO 80523

94 3 18 062

94-08781

DTIC QUALITY INSPECTED 1

1

RESEARCH OBJECTIVES

- High degree of readiness in spite of system complexity

- Probability of an undetected fault must be extremely low

- Both testing and redundance can be very expensive

- Statistical Characterization

- Need to evaluate the effectiveness of approaches

2. PROJECT ACHIEVEMENTS

As discussed in the previous proposal, we have investigated some of the important problems associated with the challenging task of achieving very high readiness. Several significant results have been obtained and some major problems have been identified. We have regarded this as a multi-level problem. For convenience, the results obtained have been grouped into the following subsections:

1. Stuck-open and bridging faults in CMOS

2. Other major VLSI technologies (ECL and BiCMOS)

3. IDDQ based testing

4. Faults in storage elements

5. Fault handling at the register level

6. Design faults

A list of publications and reports since 1989 is included at the end of this section.

2.1 Stuck-Open and Bridging Faults in CMOS [P2,89.6,91.1,89.1,89.3,89.6,89.10]

Many physical failures in CMOS, now the dominant technology, cannot be characterized using the classical fault model. With the shrinking geometrics, bridging faults have now become even more important. Some of the major achievements include:

- A testable design scheme that allows stuck-open fault detection wiring a single test pattern, even in the presence of glitches and skews.

- Identification of the analomous reverse condition (ARC) phenomenon. Other researchers have now started taking this into account.

Many of the results of CMOS are also applicable for SOI, which is a special implementation of CMOS.

2.2 Other Major VLSI Technologies [P5,P6,91.4,19.12,90.3,90.8]

Recent advances have made it possible to achieve higher densities and lower power consumption in the high performance ECL technology. BiCMOS is expected to emerge as an important technology. Our achievements include:

- Modeling schemes for faults in simple and complex ECL cells.
- Results on how nove margins may be affected by high resistance bridging faults.
- A design-for-testability scheme.
- Examination of testability of BiCMOS.

2.3 IDDQ-Based Testing [91.5]

While IDDQ-based testing has been used for several technologies, it is especially suitable for a low quiescent supply-current technology like CMOS. It has now been recognized that for several failure modes, only IDDQ-based testing is effective. However, some significant problems need to be solved before IDDQ-based testing can be of general use in large VLSI chips in practice. We have presented:

- A simple statistical characterization of the problem of limited resolution.
- An information compression scheme to enhance resolution.

As discussed in the next section, some important problems yet remain to be examined.

2.4 Faults in Storage Elements [P4,89.9]

Most design-for testability (DFT) approaches involve the use of additional or more complex storage elements in order to convert the problem of testing sequential circuits into the easier problem of testing combinational circuits. The faults in storage elements are often not explicitly considered. This would be reasonable if faults in the storage elements appear only as output s-a-0/1.

We have examined several frequently used storage elements under stuck-open, stuck-on and bridging faults to identify the situations when complex behavior occurs. We have shown that some cases the storage element can become stuck-transparent causing both logical and timing problems. In some cases it can be shown that coupling between the clock-signal and the cell output can be effectively modeled as stuck-at 0/1.

2.5 Fault Handling at the Register Level [P3,91.2,91.6,91.8,90.5,90.6,89.8]

These results are concerned with BIST and PLAs. BIST has emerged as a very powerful and popular technique. BIST uses information compression by an LFSR to obtain a signature. In the past, the aliasing probability has usually been evaluated using the assumption that all error patterns are equally likely. Our contributions in this area include:

- Signature register designs to avoid aliasing due to double faults.

- Optimal BIST scheduling schemes.

- Schemes to evaluate effects of physical faults on the signature.

2.6 Design Faults [91.3,91.10,91.11,90.1,90.2,89.4]

Design faults may occur during the design of both hardware and software. The process of finding and fixing design faults is similar in both cases. Significant

numbers of data sets from different software projects are now available. We have focused on accurate measurement and projections of defect-detection-rate.

We have presented measures called Average Error and Average Bias to compare predictive capabilities of different models. We have shown that some models have significantly higher predictive capabilities. Projections based on neural-net approach can sometimes provide better accuracy than existing model-based approaches. We have also developed methods for a priori estimation of parameters.

2.7 SDIO/IST Supported Publications/Reports

Book

1. Software Reliability Models: Theoretical Development, Evaluation and Applications, Editors: Y.K. Malaiya and P. Srimani, IEEE Computer Society Press Technology Series, Dec. 1990.

Papers

[P1] Y.K. Malaiya, N. Karunanithi and P. Verma, "Predictability of Software Reliability Models," Technical Report, submitted for publication.

[P2] R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "Bridging Faults in MOS VLSI: Analysis and Characterization," submitted for publication.

[P3] S. Feng, Y.K. Malaiya and N. Karunanithi, "Predictability of Fault Coverage Models for Random Testing of Combinational Circuits," submitted for publication.

[P4] Y.K. Malaiya, W. Al-assadi and A.P. Jayasumana, "Fault Modeling for Storage Elements," to be submitted.

[P5] S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Fault Modeling for ECL for High Fault Coverage of Physical Faults," Technical Report, submitted for publication.

[P6] S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "BiCMOS Behavior under Stuck and Bridging Faults," Technical Report, submitted for publication.

[91.1] A.P. Jayasumana, Y.K. Malaiya and R. Rajsuman, "Design of CMOS Circuits for Stuck-Open Fault Testability," IEEE Journal of Solid State Circuits, Vol. 26, No. 1, Jan. 1991, pp. 58-61.

[91.2] Y. Min, Y.K. Malaiya and B. Jin, "Analysis of Detection Capability of Parallel Signature Analyzers," IEEE Trans. Computers, Vol. 40, No. 9, Sept. 1991, pp. 1075-1081.

[91.3] N. Karunanithi, Y.K. Malaiya and D. Whitley, "Prediction of Software Reliability Using Neural Networks," Proc. Int. Symp. on Software Reliability Engineering, May 1991, pp. 124-130.

[91.4] S.M. Menon, Y.K. Malaiya and A.P. Jayasumana, "Fault Modeling and Testable Design of 2-Level Complex ECL Gates," Proc. Fourth CSI/IEEE Int. Symp. on VLSI Design, Jan. 1991, pp. 23-28.

[91.5] Y.K. Malaiya and A.P. Jayasumana, "Enhancement of Resolution in Supply Current Based Testing for Large ICs," IEEE VLSI Test Symposium, Apr. 1991, pp. 291-296.

[91.6] S. Feng and Y.K. Malaiya, "Evaluation of Detectability in BIST Environment," Proc. IEEE VLSI Test Symposium, Apr. 1991, pp. 271-276.

[91.7] A.P. Jayasumana, W. Al-assadi and Y.K. Malaiya, "On Pass Transistor Logic Design," International Journal of Electronics, Vol. 70, No. 4, Apr. 1991, pp. 739-749.

[91.8] S. Feng and Y.K. Malaiya, "Optimization of Test Parallelism with Limited Hardware Overhead," Microelectronics and Reliability, Vol. 31, No. 2, 1991, pp. 271-276.

[91.9] Y.K. Malaiya, "Early Characterization of the Defect Removal Process," Proc. 9th Annual IEEE Software Reliability Symposium, May 1991, pp. 6.1-6.4.

[91.10] J. Bieman, Y.K. Malaiya, K. Olender, R. Oldehoeft and P. Srimani, "The Reliable Software Laboratory at Colorado State University," Proc. 9th Annual IEEE Software Reliability Symposium, May 1991, pp. 6.5-6.10.

[91.11] Y.K. Malaiya and P.K. Srimani, "An Introduction to Software Reliability Models," to appear in Proc. CMG-91, Dec. 1991.

[91.12] S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "On Bridging Faults in ECL Circuits," to appear in Proc. Fifth Int. Conf. on VLSI Design, 1992.

[90.1] Y.K. Malaiya, N. Karunanithi and P. Verma, "Predictability Measures for Software Reliability Models," Proc. IEEE 14th Int. Computer Software and Applications Conference (COMPSAC 90), Oct. 1990, pp. 7-12.

[90.2] Y.K. Malaiya, S. Sur, N. Karunanithi and Y.C. Sun, "Implementation Considerations for Software Reliability," Proc. 8th Annual IEEE Software Reliability Symposium, June 1990, pp. 6.21-6.30.

[90.3] S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Fault Modeling for ECL Devices," Electronic Letters, Vol. 26, No. 15, July 19, 1990, pp. 1105-1108.

[90.4]   R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "A New Testable Design of Field Programmable Logic Array," Proc. IEEE Int. Symp. on Circuits and Systems, 1990, pp. 436-439.

[90.5]   Y. Min, Y.K. Malaiya and B. Jin, "Aliasing Errors in Parallel Signature Analyzers," Journal of Computer Science and Technology, Vol. 5, No. 1, Jan. 1990, pp. 25-40.

[90.6]   R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "Reprogrammable FPLA with Universal Test Set," Proc. IEE, Vol. 137, Pt. E, No. 6, Nov. 1990, pp. 437-441.

[90.7]   A.P. Jayasumana, W. Al-assadi and Y.K. Malaiya, "Pass Transistor Logic Design," in VLSI System Design, Editors: L.M. Patnaik and A.D. Singh (Proc. Third International Workshop on VLSI Design), Tata-McGraw Hill, Jan. 1990, pp. 13-17.

[90.8]   S.M. Menon, A.P. Jayasumana and Y.K. Malaiya, "Gate Level Modeling of ECL Circuits," Proc. First Great Lakes Symposium on VLSI, Mar. 1990, pp. 330-331.

[89.1]   R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "CMOS Stuck-Open Fault Detection in Presence of Glitches and Timing Skews," IEEE Journal of Solid State Circuits, Vol. 24, No. 4, Aug. 1989, pp. 1055-1061.

[89.2]   R. Rajsuman, Y.K. Malaiya and A.P. Jayasumana, "Limitations of Switch Level Analysis for Bridging Faults," IEEE Trans. CAD, Vol. 8, No. 7, Jul. 1989, pp. 807-811.

[89.3]   Y.K. Malaiya, "On Inherent Untestability of Unaugmented Micro-programmed Control," Proc. 22nd ACM/IEEE Int. Work. on Micro-programming and Microarchitecture, Aug. 1989, pp. 88-96.

[89.4]   P. Verma and Y.K. Malaiya, "In Search of the Best Software Reliability Model," Proc. 7th Ann. IEEE Software Reliability Symposium, May 1989, pp. 76-92.

[89.5]   A.B. Kulkarni, Y.K. Malaiya and A.P. Jayasumana, "MESHNET: A New Fault-Tolerant Local Area Network for Industrial Environments," Proc. 15th Ann. Conf. IEEE Ind. Ele. Soc., Nov. 1989, pp. 537-542.

[89.6]   R. Rajsuman, A.P. Jayasumana and Y.K. Malaiya, "CMOS Stuck-Open Fault Detection Using Single Test Patterns," Proc. ACM/IEEE Design Automation Conference, June 1989, pp. 714-717.

[89.7]   Y.K. Malaiya, "On Inherent Untestability of Unaugmented Micro-programmed Control," Proc. 22nd ACM/IEEE Int. Work. on Micro-programming and Microarchitecture, Aug. 1989, pp. 88-96.

[89.8] Y. Min, Y.K. Malaiya and B. Gupta, "On the Computational Complexity of Test Generation for ETG PLAs," IEE Proceedings, Vol. 136, Pt. E, No. 2, Mar. 1989, pp. 107-111.

[89.9] Y.K. Malaiya, B. Gupta, A.P. Jayasumana, R. Rajsuman, M. Sankaran and S. Yang, "Functional Fault Modeling for Elementary Static Storage Elements," IEEE Design for Testability Workshop, Apr. 1989.

[89.10] B.Gupta, Y.K. Malaiya, Y. Min and R. Rajsuman, "On Designing Robust Testable CMOS Combinational Circuits," IEE Proceedings, Vol. 136, Pt. E, No. 4, Jul. 1989, pp. 329-338.