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CDRL No. 0002AB-8

Quarterly Technical Report - Report No. 8

October 1, 1993 - December 31, 1993

DARPA DICE Manufacturing Optimization

Linda J. Lapointe
Thomas J. Laliberty
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Raytheon Company

1994

DARPA
Defense Advanced Research
Projects Agency

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Attention: Mr. Donald Sharkus, Contracting Officer

Subject: Contract MDA972-92-C-0020;
Submission of Quarterly Technical Report, No. 8
Manufacturing Optimization
DARPA Initiative In Concurrent Engineering

Enclosure: (1) CDRL 0002AB-8, Quarterly Technical Report No. 8 for the period October-December 1993

Dear Mr. Sharkus:

In accordance with the CDRL requirements of the subject contract, Raytheon Company is pleased to submit Enclosure (1) for your records.

Should you require additional information in this regard, please contact this office at (508) 858-5294, by facsimile at (508) 858-5142 or by mail correspondence to M/S T3MA18.

Very truly yours,

RAYTHEON COMPANY

Karen D. Omobono

Karen D. Omobono
Contract Administrator
Missile Systems Laboratories

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Contracts Management Office

Arlington, VA 22203-1714

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1. Summary

This is the Quarterly Technical Report for the DARPA DICE Manufacturing Optimization. The goal of the Manufacturing Optimization (MO) system is to facilitate a two tiered team approach to the product/process development cycle where a product design is analyzed by multiple manufacturing engineers, and product/process changes are traded concurrently in the product and process domains. The system will support Design for Manufacturing and Assembly (DFMA) with a set of tools to model manufacturing processes, and manage tradeoffs across multiple processes. The subject of this report is the technical work accomplished during the final quarter of the contract.

The main thrust of the final quarter was test and demonstration of the MO software and the development of the MO final report. Highlighted in this report are the PWA/PWF process models and test case developed as the demonstration vehicle for the MO system, as well as the procedures for building new product/process models.

2. Introduction

This is the Quarterly Technical Report for the DARPA DICE Manufacturing Optimization. The concept behind the Manufacturing Optimization (MO) system is to facilitate a two tiered team approach to the product/process development cycle where a product design is analyzed by multiple manufacturing engineers, and product/process changes are traded concurrently in the product and process domains. The system will support DFMA with a set of tools to model manufacturing processes, and manage tradeoffs across multiple processes. The subject of this report is the technical work accomplished during the final quarter of the contract.

Raytheon spent the final quarter on the test and demonstration of MO software, and on the development of the final report. Highlighted in this report are the PWA/PWF process models and the test case developed as the demonstration vehicle for the MO system, as well as the procedures for building new product/process models.

3. MO Process Models and Test Case

The following sections are an overview of the typical manufacturing cycle for a standard through hole printed wiring board which highlight the inter-relationships among product design attributes and manufacturing processes. The manufacturing cycle provided the baseline for the MO process models that were developed. Figure 3-1 depicts a typical manufacturing process flow for printed wiring boards. At each step in the flow there are design attributes that influence the manufacturing process. Four of the manufacturing processes will be described as highlighted in the figure.

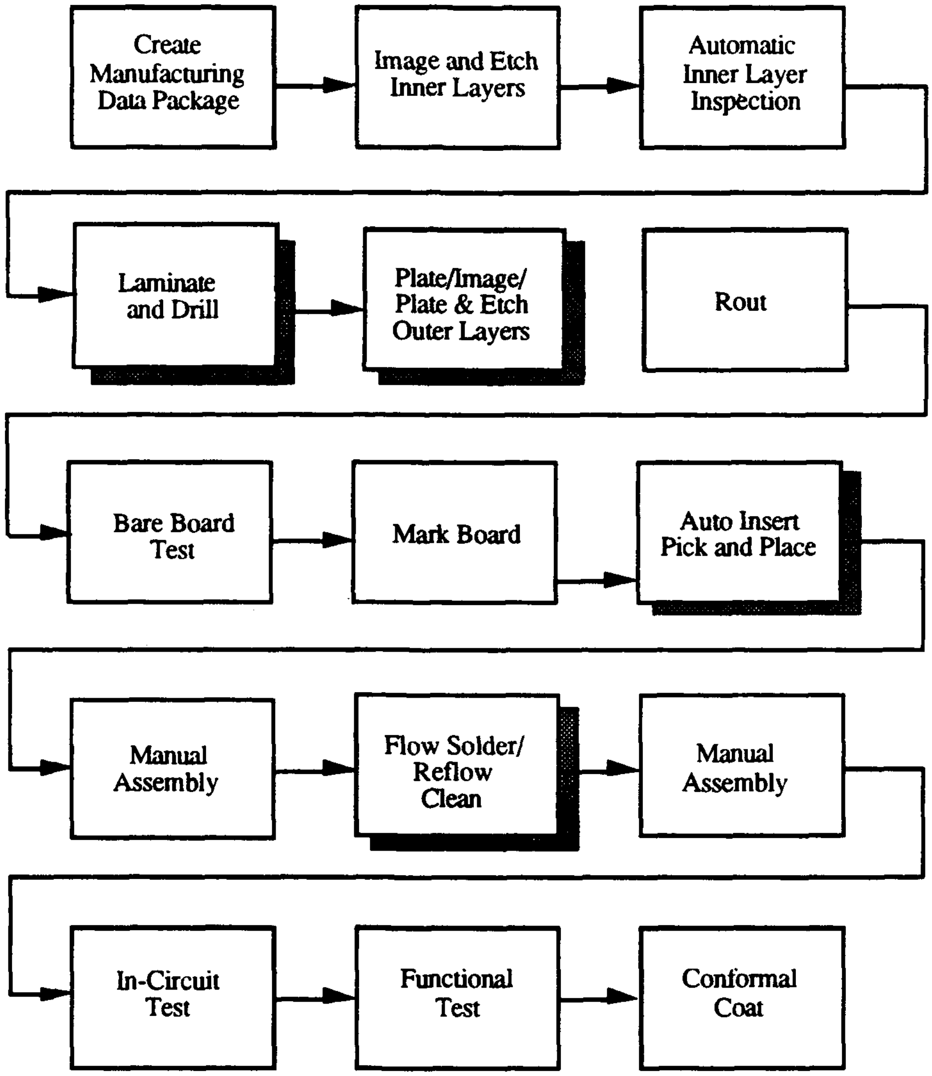

Figure 3-1. Printed Wiring Board Manufacturing Flow

Laminate and Drill are the processes where multiple circuit layers are laminated under heat and pressure, and the required holes are automatically precision drilled. The critical design attributes, which influence the lamination process include: blind/buried vias, number of layers, copper balance, layer stackup, board/laminate thickness, impedance control requirements, laminate/prepreg material, and board dimensions.

While the effect of design features upon the Laminate and Drill processes are many, one of the most profound influences upon cost and yield comes from the requirement for blind and/or buried vias. Traditional through-hole PWB construction requires a single lamination step, followed by precision drilling of the through holes. However, boards requiring blind vias (i.e., visible from one external surface only) or buried vias (i.e., completely blind from both external surfaces) will require multiple lamination, drilling, imaging, plating cycles. Additional costs include tooling, inspection, yield loss due to via fracturing, and multiple setups.

A more common occurrence is the adverse influence of non-uniform copper balance upon lamination, whereby warping of the laminated structure occurs, causing via and component attachment failures. Efforts to minimize warping result in added cost and are not always successful.

A third critical design attribute is that of impedance control. Stringent control of interconnect impedance is dependent upon distance between interconnect layers and their associated copper planes. This requirement translates into non-standard layer stackups and more precise control of the lamination processes.

Yet a fourth is the relationship between pad size, drill diameter, and board thickness whereby the requirement for close tolerance drilling of many "large" holes in small pads through thick panels, results in high inspection costs and low yields.

The Image, Plate, and Etch Outer Layers processes involves photographic imaging and chemical plating/etching operations. The critical design attributes, which influence these processes include: plated through-hole (PTH) diameter, PTH aspect ratio, available registration aids, feature sizes, spacing and tolerances, material selection, layer stackup (presence of interconnect on outer layers, position of ground planes, metal balance/density, outer laminate copper thickness), and length of parallel interconnect lines.

Again, many design feature/manufacturability relationships exist. One of the more notable dependencies is the aspect ratio of plated-through-holes whereby the greater the barrel length:hole-diameter (aspect) ratio, the more difficult it becomes to deposit copper inside the barrel. Proper plating and copper adhesion are imperative if the board is to ultimately withstand temperature cycling and vibrational stress.

The Auto Insertion/Pick and Place processes involve automatic insertion of through-hole components and the attachment of surface mount devices. The critical design attributes, which influence the auto insertion process, include: insertability of each component type, number of components by insertion type, component orientation by component type, component-component spacing, component-obstruction spacing, board thickness versus component lead length, lead diameter versus hole diameter, static sensitivity, sequencer compatibility of components, and component bonding/attachment method.

Fundamental to automated insertion is the inherent insertability of specific component types. A secondary, but similarly important criteria is the number of components of a given class (e.g., dual in-line IC or surface mount packages) that ultimately determines the economic feasibility of allocating and setting up a specialized insertion machine for a limited number of components. Even where the component type and count meet the required criteria, component orientation and component spacing become important factors. The best case occurs where all components are aligned in the same direction, less attractive is where components of a given type occur at zero and ninety degree rotations, and worst case is where components are aligned off-axis (i.e.,, 45 degrees or other).

The Flow Solder process is where through-hole components are soldered onto the board using a "wave" of molten solder and surface mount components are reflowed using a vapor phase, IR, convection, or combination. The critical design attributes, which influence the flow solder process include: board thickness/lead protrusion, thermal sensitivity of components, metal balance, component orientation, board geometry, presence of interconnect or ground plane on solder side, pad geometry, plated through-hole lead diameter, and aspect ratio of through-hole.

Thick boards, coupled with short lead protrusion, and improperly sized/shaped pads on the solder side create lead clinching problems. Pads that do not have proper thermal relief with respect to copper power and ground planes become heat sinks and promote poor solder joints.

Conductor paths on the solder side cause solder bridging. Heat sensitive components require special handling and solder-side ground planes cause a variety of problems associated with heat absorption.

3.1 Printed Wiring Board Assembly Model

Provided below is the printed wiring board assembly hierarchical tree model, and following it are the MO Process Modeler screens displaying various parts of this model.

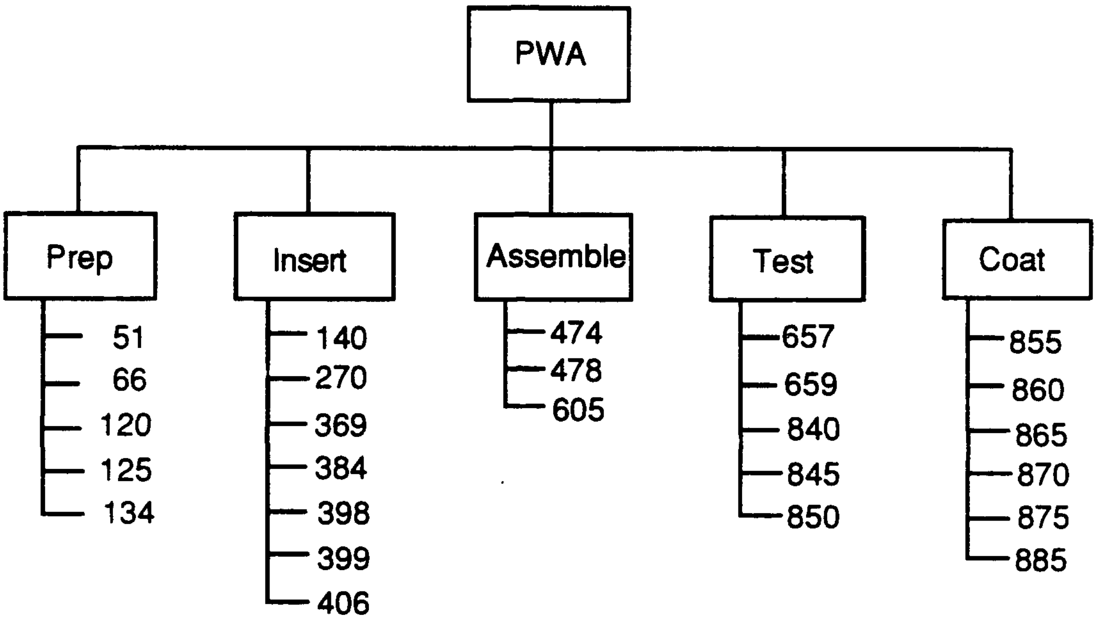

Figure 3.1-1. Printed Wiring Board Assembly Tree Model

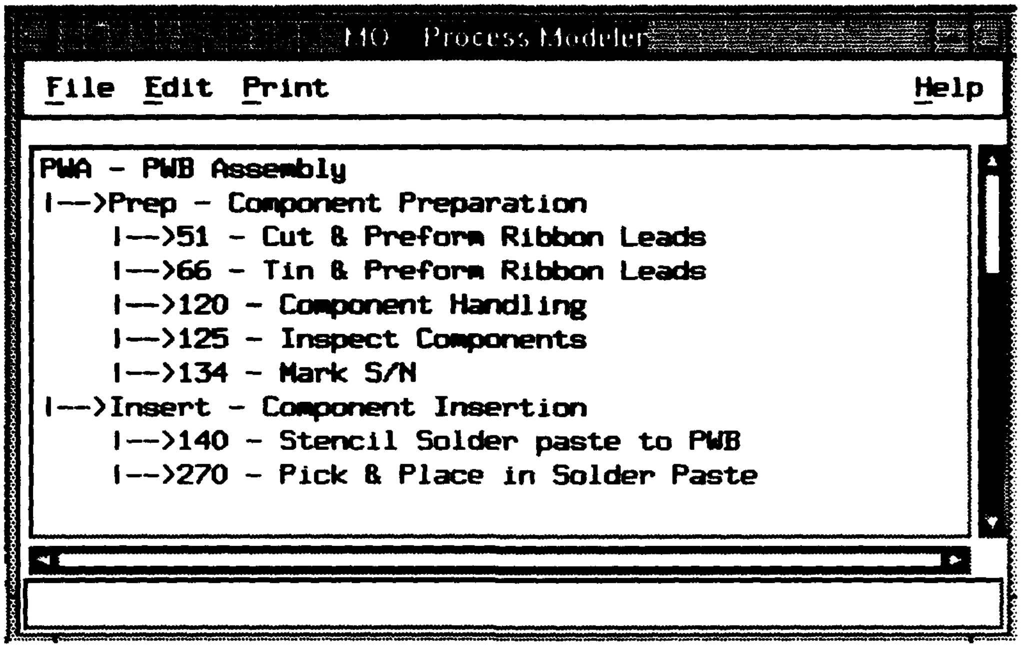

Figure 3.1-2. Printed Wiring Board Assembly Flow

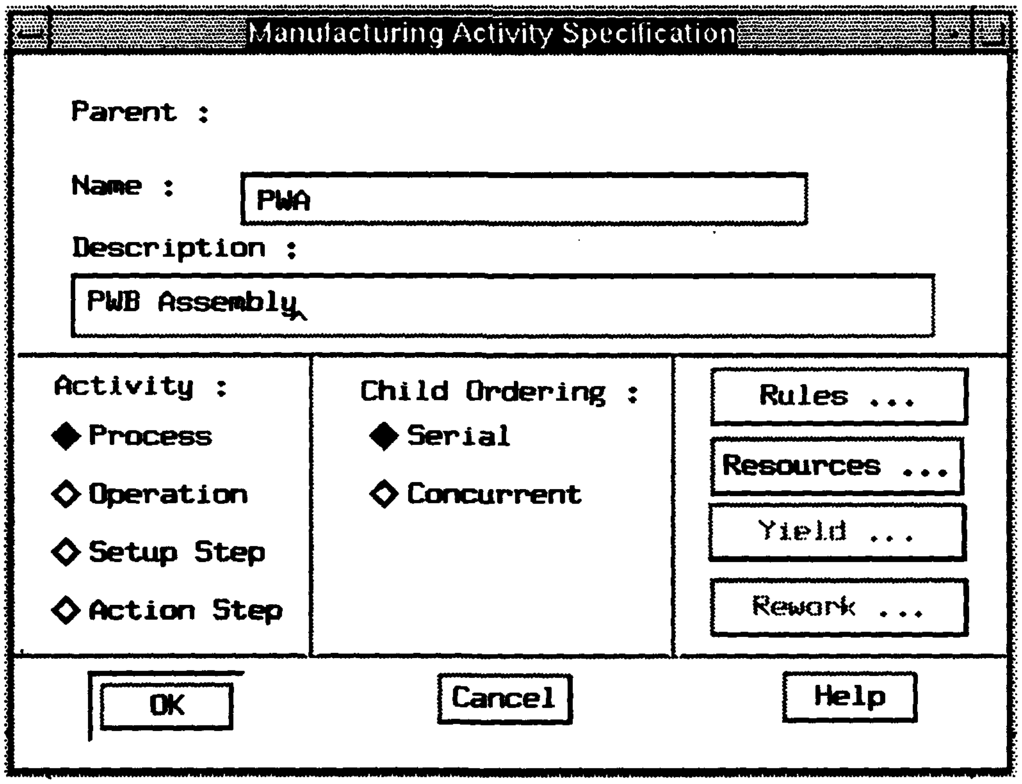

Figure 3.1-3. Process PWA Activity Specification

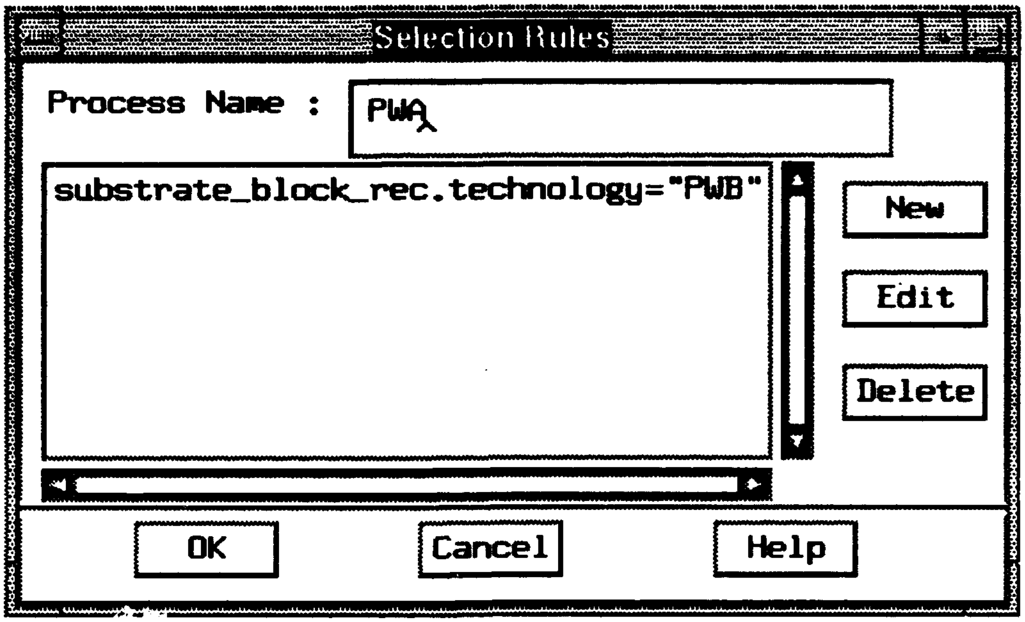

Figure 3.1-4. Process PWA Selection Rules

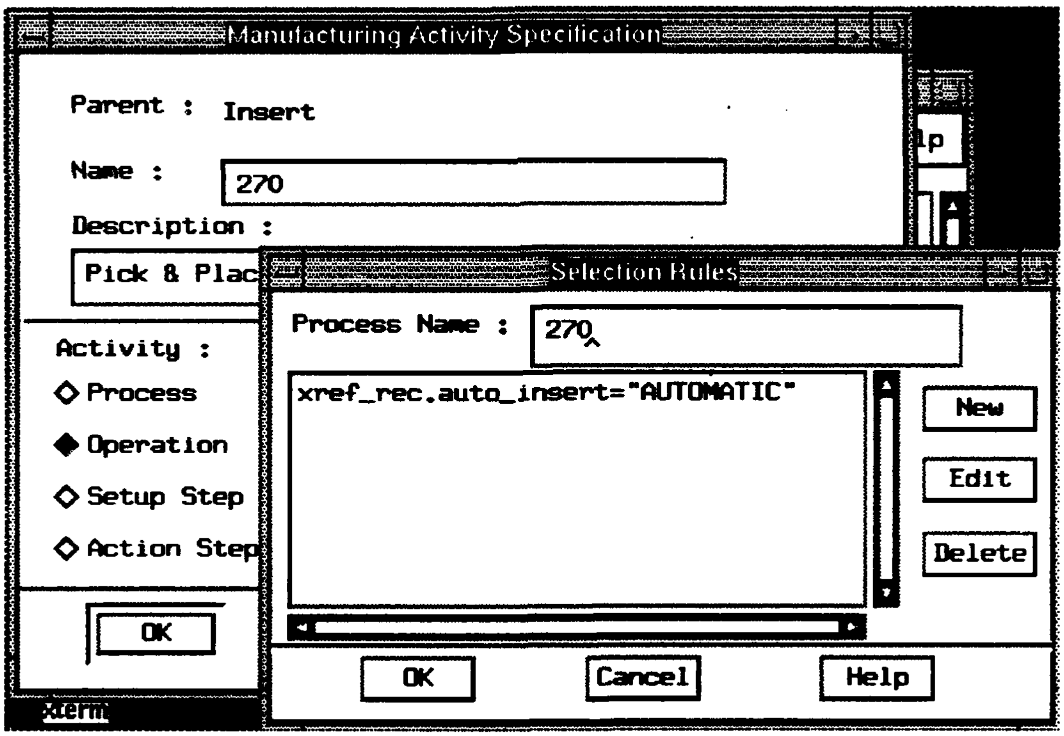

Figure 3.1-5. Operation 270 Activity Specification & Selection Rules

3.2 Printed Wiring Board Fabrication Model

Provided below is the printed wiring board fabrication hierarchical tree model, and following it are the MO Process Modeler screens displaying various parts of this model.

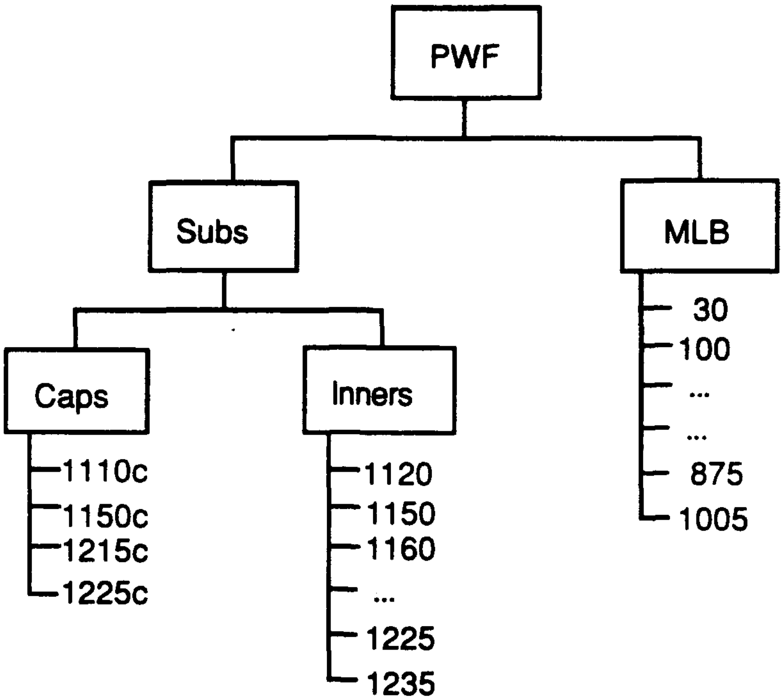

Figure 3.2-1. Printed Wiring Board Fabrication Tree Model

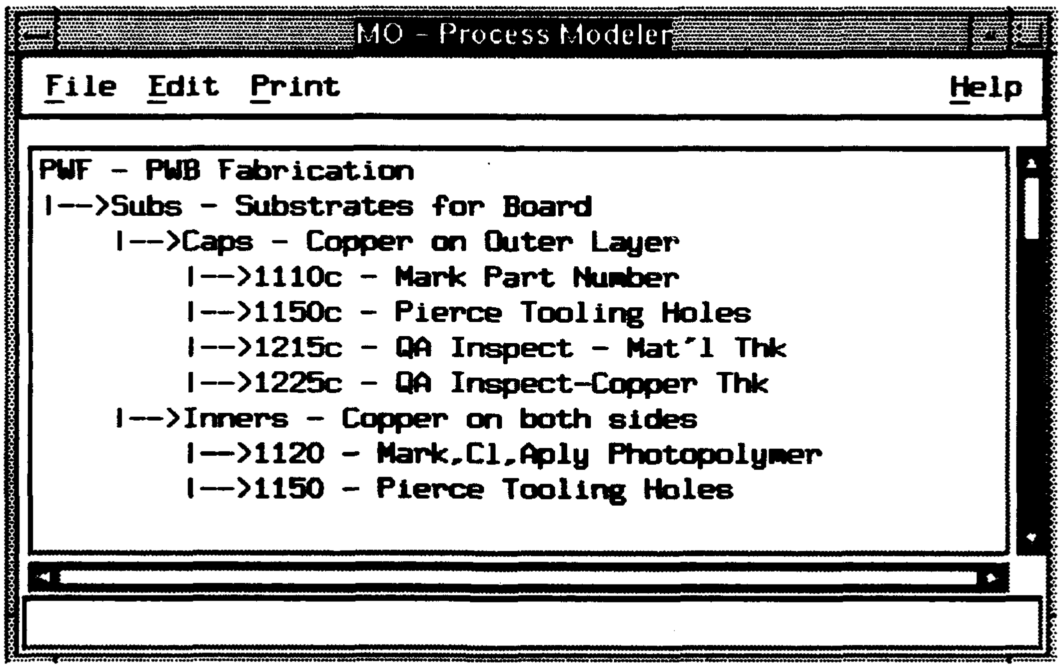

Figure 3.2-2. Printed Wiring Board Fabrication Flow

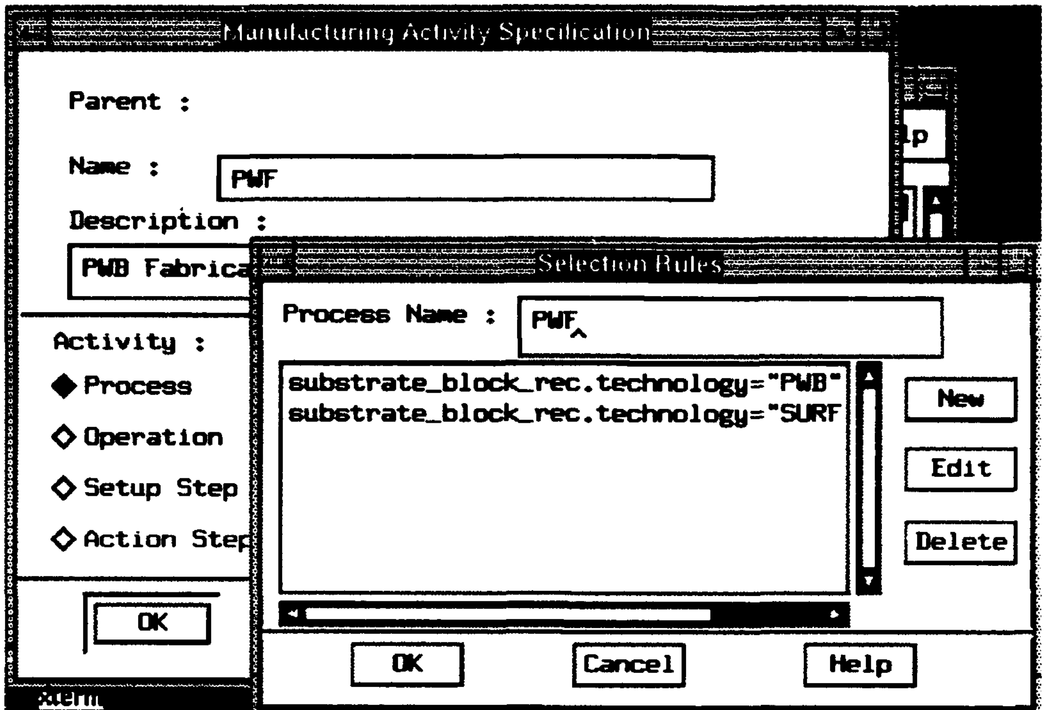

Figure 3.2-3. Process PWF Activity Specification & Selection Rules

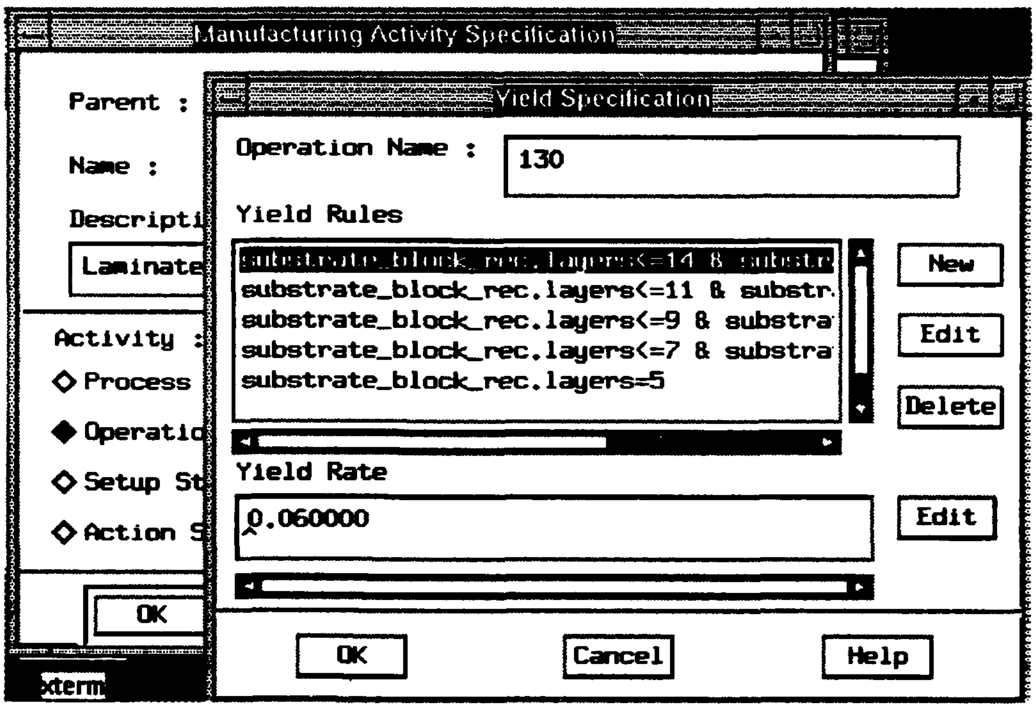

Figure 3.2-4. Operation 130 Activity & Yield Specifications

3.3 Test Case Demonstration Vehicle

The product demonstration vehicle for MO is a module from the Patriot System's Expanded Weapons Control Computer (EWCC). The system packaging concept stressed packaging density. The packaging technology selected for this system utilized leadless hermetic chip carriers on double sided modules. These modules consisted of two PWB's bonded back-to-back on a composite core.

Each PWB consisted of 13 layers: 2 outer pad layers, 7 interconnection wiring layers, and 4 power and ground planes. The wiring layers were configured as controlled impedance microstrip layers in order to support high speed digital signals. Very small feature sizes were utilized. For instance, the line widths were 0.005 ± 0.001 inch, the plated through hole diameter was 0.016-0.022 inch, and the inner layer land diameter was 0.030 inch. These boards had small features, small spacings, and tight tolerances throughout. They were difficult to manufacture.

In order to improve the producibility of the printed wiring boards, some fundamental changes were made to the packaging approach. First, the electronic devices were changed to leaded hermetic chip carriers. The modules were still double sided, but the utilization of leaded packages permitted simpler assembly. Second, the inner configuration of the printed wiring boards was changed from microstrip to stripline.

The boards now consisted of 2 outer pad layers, 6 interconnection wiring layers, and 4 power and ground planes. This, combined with the change to the leaded packages, permitted increasing feature sizes, spacings, and tolerances. Now the line widths were 0.006 ± 0.002 inch, the plated through hole diameter was still 0.016-0.022 inch, but the inner layer land diameter was increased to 0.052 inch. Spacings and tolerances were relaxed.

The EWCC module test case was loaded into MO and an analysis/optimization session was run to demonstrate the ability of MO to estimate cost and yield. Provided below are the assembly and fabrication analysis reports produced by MO.

3.3.1 PWA Analysis Report

MANUFACTURING PROCESS FLOW

	INDIVIDUAL TIME	TOTAL TIME

Name	Description	Ideal(hr)	Actual(hr)	Ideal(hr)	Actual(hr)
PWA	PWB Assembly	0.000	0.00	1.77	1.78
Prep	Component Preparation	0.000	0.00	0.154	0.15
51	Cut & Preform Ribbon Leads	0.000	0.00	0.000	0.00
66	Tin & Preform Ribbon Leads	0.008	0.01	0.008	0.01
120	Component Handling	0.007	0.01	0.007	0.01
125	Inspect Components	0.034	0.03	0.034	0.03
134	Mark S/N	0.104	0.10	0.104	0.10
Insert	Component Insertion	0.000	0.00	1.055	1.06
140	Stencil Solder paste to PWB	0.000	0.00	0.000	0.00
270	Pick & Place in Solder Paste	0.000	0.00	0.000	0.00
369	Reflow Solder	0.343	0.34	0.343	0.34
384	Clean & Put in Fixture	0.092	0.09	0.092	0.09
398	Touch-Up Solder	0.571	0.57	0.571	0.57
399	Clean	0.031	0.03	0.031	0.03
406	Inspect	0.019	0.02	0.019	0.02
Assemble	Mechanical Assembly	0.000	0.00	0.048	0.05
474	Assemble & Reflow	0.000	0.00	0.000	0.00
478	Clean	0.031	0.03	0.031	0.03
605	Final Inspect	0.018	0.02	0.018	0.02
Test	Board Testing	0.000	0.00	0.208	0.21
657	Thermal Shock	0.000	0.00	0.000	0.00
659	In-Circuit Test	0.047	0.05	0.047	0.05
840	Hot Solvent Wash	0.031	0.03	0.031	0.03
845	Water Wash & Bake	0.007	0.01	0.007	0.01
850	Omega Test	0.124	0.12	0.124	0.12
Coat	Board Coating	0.000	0.00	0.310	0.31
855	Mask	0.000	0.00	0.000	0.00
860	Attach Labels	0.124	0.12	0.124	0.12
865	Bake	0.007	0.01	0.007	0.01
870	Spray Coat (Circuit Side)	0.119	0.12	0.119	0.12
875	Demask	0.018	0.02	0.018	0.02
885	Inspect	0.043	0.04	0.043	0.04

YIELD AND REWORK BREAKDOWN

Name	Description	Yield	Rework($)	%Rework	ProdQTY
PWA	PWB Assembly	1.00	0.00	0.000	100
Prep	Component Preparation	1.00	0.00	0.000	100
51	Cut & Preform Ribbon Leads	1.00	0.00	0.000	100
66	Tin & Preform Ribbon Leads	1.00	0.00	0.000	100
120	Component Handling	1.00	0.00	0.000	100
125	Inspect Components	1.00	0.00	0.000	100
134	Mark S/N	1.00	0.00	0.000	100
Insert	Component Insertion	1.00	0.00	0.000	100
140	Stencil Solder paste to PWB	1.00	0.00	0.000	100
270	Pick & Place in Solder Paste	1.00	0.00	0.000	100
369	Reflow Solder	1.00	0.00	0.000	100
384	Clean & Put in Fixture	1.00	0.00	0.000	100
398	Touch-Up Solder	1.00	0.00	0.000	100
399	Clean	1.00	0.00	0.000	100

406	Inspect	1.00	0.00	0.000	100
Assemble	Mechanical Assembly	1.00	0.00	0.000	100
474	Assemble & Reflow	1.00	0.00	0.000	100
478	Clean	1.00	0.00	0.000	100
605	Final Inspect	1.00	0.00	0.000	100
Test	Board Testing	1.00	0.00	0.000	100
657	Thermal Shock	1.00	0.00	0.000	100
659	In-Circuit Test	1.00	0.00	0.000	100
840	Hot Solvent Wash	1.00	0.00	0.000	100
845	Water Wash & Bake	1.00	0.00	0.000	100
850	Omega Test	1.00	0.00	0.000	100
Coat	Board Coating	1.00	0.00	0.000	100
855	Mask	1.00	0.00	0.000	100
860	Attach Labels	1.00	0.00	0.000	100
865	Bake	1.00	0.00	0.000	100
870	Spray Coat (Circuit Side)	1.00	0.00	0.000	100
875	Demask	1.00	0.00	0.000	100
885	Inspect	1.00	0.00	0.000	100

COSTING BREAKDOWN

		INDIVIDUAL COST		TOTAL COST	
Name	Description	Ideal($)	Actual($)	Ideal($)	Actual($)
PWA	PWB Assembly	0.000	0.00	20.014	20.01
Prep	Component Preparation	0.000	0.00	1.683	1.68
51	Cut & Preform Ribbon Leads	0.000	0.00	0.000	0.00
66	Tin & Preform Ribbon Leads	0.088	0.09	0.088	0.09
120	Component Handling	0.077	0.08	0.077	0.08
125	Inspect Components	0.389	0.39	0.389	0.39
134	Mark S/N	1.129	1.13	1.129	1.13
Insert	Component Insertion	0.000	0.00	11.441	11.44
140	Stencil Solder paste to PWB	0.000	0.00	0.000	0.00
270	Pick & Place in Solder Paste	0.000	0.00	0.000	0.00
369	Reflow Solder	3.714	3.71	3.714	3.71
384	Clean & Put in Fixture	0.996	1.00	0.996	1.00
398	Touch-Up Solder	6.188	6.19	6.188	6.19
399	Clean	0.331	0.33	0.331	0.33
406	Inspect	0.212	0.21	0.212	0.21
Assemble	Mechanical Assembly	0.000	0.00	0.531	0.53
474	Assemble & Reflow	0.000	0.00	0.000	0.00
478	Clean	0.331	0.33	0.331	0.33
605	Final Inspect	0.199	0.20	0.199	0.20
Test	Board Testing	0.000	0.00	2.632	2.63
657	Thermal Shock	0.000	0.00	0.000	0.00
659	In-Circuit Test	0.540	0.54	0.540	0.54
840	Hot Solvent Wash	0.331	0.33	0.331	0.33
845	Water Wash & Bake	0.070	0.07	0.070	0.07
850	Omega Test	1.691	1.69	1.691	1.69
Coat	Board Coating	0.000	0.00	3.727	3.73
855	Mask	0.000	0.00	0.000	0.00
860	Attach Labels	1.691	1.69	1.691	1.69
865	Bake	0.070	0.07	0.070	0.07

870	Spray Coat (Circuit Side)	1.287	1.29	1.287	1.29
875	Demask	0.190	0.19	0.190	0.19
885	Inspect	0.488	0.49	0.488	0.49

3.3.2 PWF Analysis Report

MANUFACTURING PROCESS FLOW

		INDIVIDUAL TIME		TOTAL TIME	
Name	Description	Ideal(hr)	Actual(hr)	Ideal(hr)	Actual(hr)
PWF	PWB Fabrication	0.000	0.00	20.806	20.84
Subs	Substrates for Board	0.000	0.00	1.660	1.66
Caps	Copper on Outer Layer	0.000	0.00	0.621	0.62
1110c	Mark Part Number	0.391	0.39	0.391	0.39
1150c	Pierce Tooling Holes	0.018	0.02	0.018	0.02
1215c	QA Inspect - Mat'l Thk	0.173	0.17	0.173	0.17
1225c	QA Inspect-Copper Thk	0.039	0.04	0.039	0.04
Inners	Copper on both sides	0.000	0.00	1.040	1.04
1120	Mark,Cl,Aply Photopolymer	0.489	0.49	0.489	0.49
1150	Pierce Tooling Holes	0.018	0.02	0.018	0.02
1160	Expose Photopolymer	0.068	0.07	0.068	0.07
1170	Develop Photopolymer	0.050	0.05	0.050	0.05
1190	Etch Copper	0.046	0.05	0.046	0.05
1200	Strip Photopolymer	0.013	0.01	0.013	0.01
1215	QA Inspect - Mat'l Thk	0.173	0.17	0.173	0.17
1225	QA Inspect-Copper Thk	0.039	0.04	0.039	0.04
1235	QA Inspect Scanning	0.145	0.14	0.145	0.14
MLB	Build Multi-Layer Board	0.000	0.00	19.145	19.18
30	Oxide Treatment	0.133	0.14	0.133	0.14
100	Bake Panels	0.032	0.03	0.032	0.03
110	Lay up for lamination	0.342	0.37	0.342	0.37
130	Laminate	0.044	0.05	0.044	0.05
140	Lamination Teardown	0.323	0.32	0.323	0.32
160	Stress Relieve	0.006	0.01	0.006	0.01
170	Rout Excess Material	0.056	0.06	0.056	0.06
220	Drill	15.366	15.37	15.366	15.37
250	Pressure Blast	0.069	0.07	0.069	0.07
280	Bake	0.000	0.00	0.000	0.00
290	Plasma Desmear	0.239	0.24	0.239	0.24
300	Glass Etch	0.072	0.07	0.072	0.07
440	Electroless CU Deposition	0.048	0.05	0.048	0.05
460	Electrostrike Copper	0.042	0.04	0.042	0.04
480	Scrub	0.021	0.02	0.021	0.02
510	Apply Photopolymer	0.059	0.06	0.059	0.06
520	Expose Photopolymer	0.068	0.07	0.068	0.07
530	Develop Photopolymer	0.050	0.05	0.050	0.05
560	Copper/Tin Lead Plate	0.116	0.12	0.116	0.12
580	Mark Control Number	0.039	0.04	0.039	0.04
605	QA Inspect-Tin/Lead	0.016	0.02	0.016	0.02
620	Strip Photopolymer	0.023	0.02	0.023	0.02
680	Etch Copper	0.046	0.05	0.046	0.05
710	Bake	0.006	0.01	0.006	0.01
720	Reflow	0.034	0.03	0.034	0.03
770	Stencil	0.073	0.07	0.073	0.07

775	QA Inspect Scanning	0.054	0.05	0.054	0.05
780	Rout Boards and Coupons	0.094	0.09	0.094	0.09
795	QA Inspect	0.035	0.03	0.035	0.03
815	Coupon Prep	0.090	0.09	0.090	0.09
845	QA Inspect Final	1.465	1.47	1.465	1.47
875	QA Electrical Test	0.024	0.02	0.024	0.02
1005	MIR Inspect	0.060	0.06	0.060	0.06

YIELD AND REWORK BREAKDOWN

Name	Description	Yield	Rework($)	%Rework	ProdQTY
PWF	PWB Fabrication	0.94	0.00	0.000	100
Subs	Substrates for Board	1.00	0.00	0.000	100
Caps	Copper on Outer Layer	1.00	0.00	0.000	100
1110c	Mark Part Number	1.00	0.00	0.000	100
1150c	Pierce Tooling Holes	1.00	0.00	0.000	100
1215c	QA Inspect - Mat'l Thk	1.00	0.00	0.000	100
1225c	QA Inspect-Copper Thk	1.00	0.00	0.000	100
Inners	Copper on both sides	1.00	0.00	0.000	100
1120	Mark,Cl,Aply Photopolymer	1.00	0.00	0.000	100
1150	Pierce Tooling Holes	1.00	0.00	0.000	100
1160	Expose Photopolymer	1.00	0.00	0.000	100
1170	Develop Photopolymer	1.00	0.00	0.000	100
1190	Etch Copper	1.00	0.00	0.000	100
1200	Strip Photopolymer	1.00	0.00	0.000	100
1215	QA Inspect - Mat'l Thk	1.00	0.00	0.000	100
1225	QA Inspect-Copper Thk	1.00	0.00	0.000	100
1235	QA Inspect Scanning	1.00	0.00	0.000	100
MLB	Build Multi-Layer Board	0.94	0.00	0.000	100
30	Oxide Treatment	1.00	0.00	0.000	107
100	Bake Panels	1.00	0.00	0.000	107
110	Lay up for lamination	1.00	0.00	0.000	107
130	Laminate	0.94	0.00	0.000	107
140	Lamination Teardown	1.00	0.00	0.000	100
160	Stress Relieve	1.00	0.00	0.000	100
170	Rout Excess Material	1.00	0.00	0.000	100
220	Drill	1.00	0.00	0.000	100
250	Pressure Blast	1.00	0.00	0.000	100
280	Bake	1.00	0.00	0.000	100
290	Plasma Desmear	1.00	0.00	0.000	100
300	Glass Etch	1.00	0.00	0.000	100
440	Electroless CU Deposition	1.00	0.00	0.000	100
460	Electrostrike Copper	1.00	0.00	0.000	100
480	Scrub	1.00	0.00	0.000	100
510	Apply Photopolymer	1.00	0.00	0.000	100
520	Expose Photopolymer	1.00	0.00	0.000	100
530	Develop Photopolymer	1.00	0.00	0.000	100
560	Copper/Tin Lead Plate	1.00	0.00	0.000	100
580	Mark Control Number	1.00	0.00	0.000	100
605	QA Inspect-Tin/Lead	1.00	0.00	0.000	100
620	Strip Photopolymer	1.00	0.00	0.000	100
680	Etch Copper	1.00	0.00	0.000	100
710	Bake	1.00	0.00	0.000	100

720	Reflow	1.00	0.00	0.000	100
770	Stencil	1.00	0.00	0.000	100
775	QA Inspect Scanning	1.00	0.00	0.000	100
780	Rout Boards and Coupons	1.00	0.00	0.000	100
795	QA Inspect	1.00	0.00	0.000	100
815	Coupon Prep	1.00	0.00	0.000	100
845	QA Inspect Final	1.00	0.00	0.000	100
875	QA Electrical Test	1.00	0.00	0.000	100
1005	MIR Inspect	1.00	0.00	0.000	100

COSTING BREAKDOWN

		INDIVIDUAL COST		TOTAL COST	
Name	Description	Ideal($)	Actual($)	Ideal($)	Actual($)
PWF	PWB Fabrication	0.000	0.00	252.042	252.49
Subs	Substrates for Board	0.000	0.00	19.387	19.39
Caps	Copper on Outer Layer	0.000	0.00	7.269	7.27
1110c	Mark Part Number	4.625	4.63	4.625	4.63
1150c	Pierce Tooling Holes	0.234	0.23	0.234	0.23
1215c	QA Inspect - Mat'l Thk	1.970	1.97	1.970	1.97
1225c	QA Inspect-Copper Thk	0.440	0.44	0.440	0.44
Inners	Copper on both sides	0.000	0.00	12.118	12.12
1120	Mark,Cl,Aply Photopolymer	5.738	5.74	5.738	5.74
1150	Pierce Tooling Holes	0.234	0.23	0.234	0.23
1160	Expose Photopolymer	0.775	0.78	0.775	0.78
1170	Develop Photopolymer	0.567	0.57	0.567	0.57
1190	Etch Copper	0.584	0.58	0.584	0.58
1200	Strip Photopolymer	0.159	0.16	0.159	0.16
1215	QA Inspect - Mat'l Thk	1.970	1.97	1.970	1.97
1225	QA Inspect-Copper Thk	0.440	0.44	0.440	0.44
1235	QA Inspect Scanning	1.650	1.65	1.650	1.65
MLB	Build Multi-Layer Board	0.000	0.00	232.655	233.11
30	Oxide Treatment	1.689	1.81	1.689	1.81
100	Bake Panels	0.369	0.39	0.369	0.39
110	Lay up for lamination	3.892	4.16	3.892	4.16
130	Laminate	0.503	0.54	0.503	0.54
140	Lamination Teardown	3.678	3.68	3.678	3.68
160	Stress Relieve	0.064	0.06	0.064	0.06
170	Rout Excess Material	0.715	0.72	0.715	0.72
220	Drill	188.385	188.39	188.385	188.39
250	Pressure Blast	0.876	0.88	0.876	0.88
280	Bake	0.000	0.00	0.000	0.00
290	Plasma Desmear	3.031	3.03	3.031	3.03
300	Glass Etch	0.909	0.91	0.909	0.91
440	Electroless CU Deposition	0.604	0.60	0.604	0.60
460	Electrostrike Copper	0.534	0.53	0.534	0.53
480	Scrub	0.263	0.26	0.263	0.26
510	Apply Photopolymer	0.672	0.67	0.672	0.67
520	Expose Photopolymer	0.774	0.77	0.774	0.77
530	Develop Photopolymer	0.567	0.57	0.567	0.57
560	Copper/Tin Lead Plate	1.473	1.47	1.473	1.47
580	Mark Control Number	0.445	0.45	0.445	0.45
605	QA Inspect-Tin/Lead	0.184	0.18	0.184	0.18
620	Strip Photopolymer	0.289	0.29	0.289	0.29
680	Etch Copper	0.584	0.58	0.584	0.58

710	Bake	0.072	0.07	0.072	0.07
720	Reflow	0.387	0.39	0.387	0.39
770	Stencil	0.867	0.87	0.867	0.87
775	QA Inspect Scanning	0.656	0.66	0.656	0.66
780	Rout Boards and Coupons	1.069	1.07	1.069	1.07
795	QA Inspect	0.397	0.40	0.397	0.40
815	Coupon Prep	1.069	1.07	1.069	1.07
845	QA Inspect Final	16.689	16.69	16.689	16.69
875	QA Electrical Test	0.263	0.26	0.263	0.26
1005	MIR Inspect	0.685	0.69	0.685	0.69

3.4 How To Build a New Product/Process Model

The Manufacturing Optimization system was designed so that you could build process models against various product models. Provided below are the step by step procedures that a user would follow in order to build new product/process model. We tried sample MCM, EDIF, MMACE, and sheet metal Product Models. The sample sheet metal product is being used to demonstrate the procedures below.

1. Write a Product EXPRESS model to represent the new product area that you wish to build a Process Model against. An small example of a sheet metal product features is provided below (sheetMetal.exp) :

```
SCHEMA sheetMetal_features_schema;
  ENTITY sheetMetal_feature;
        reference_designator: STRING(50);
        quantity: INTEGER;
  END_ENTITY;

  ENTITY hole
   ABSTRACT SUPERTYPE OF ( ONEOF (rectangle,oval,single_diameter_hole))
   SUBTYPE OF (sheetMetal_feature);

        minimum _distance_to_edge_of_bend : STRING(50);
        tightest_lead_in_tolerance_plus_minus : STRING(50);
        tightest_hole_to_hole_tolerance_plus_minus : STRING(50);
  END_ENTITY;

  ENTITY rectangle
   SUBTYPE OF (hole);

        length : STRING(50);
        width : STRING(50);
        radius : STRING(50);
  END_ENTITY;

  ENTITY single_diameter_hole
   SUBTYPE OF (hole);
```

```
        minimum_hole_diameter : STRING(50);
        maximum_hole_diameter : STRING(50);
        blind_or_through_hole : STRING(50);
        depth_of_hole : STRING(50);
        drill_holes_at_assembly : STRING(50);
        is_the_bottom_of_the_blind_hole_flat : STRING(50);
        setup_rigidity : STRING(50);
  END_ENTITY;

  ENTITY oval
   SUBTYPE OF (hole);

        nominal_hole_length : STRING(50);
        nominal_hole_width : STRING(50);
        radius : STRING(50);
  END_ENTITY;
END_SCHEMA;
```

2. Run the 'express2c++' compiler on the new EXPRESS product model.
   The command to compile the sheet metal example is:
   express2c++ -noclasses sheetMetal

3. Run 'rose create' command on the new product schema in order to produce an instantiated version of the product. The command to run rose create on the sheet metal example is: **rose create -o sheetMetal_Test sheetMetal_features_schema**

4. Set the MO product/process model schemas environment variable.
   setenv MO_PRODUCT_SCHEMAS sheetMetal_Test

5. Make sure the compiled schema and product design file are located in the ROSE_DB environment variable path, or else update ROSE_DB to include the new directory.

6. Run 'mo', enter the 'Modeler', select the empty template process model, and begin building your Manufacturing Process Model for the new product.

4. Conclusions

During this reporting period, the main thrust was on the test and demonstration of the MO software system, as well as the development of the final report. Highlighted in this report are the PWA/PWF process models and the test case developed as the demonstration vehicle for the MO system, as well as the procedure for building new product/process models.

5. References

1. BR-20558-1, 14 June 1991, DARPA Initiative In Concurrent Engineering (DICE) Manufacturing Optimization - Volume I - Technical.

2. CDRL No. 0002AC-1, March 1992, Operational Concept Document For The Manufacturing Optimization (MO) System, Contract No. MDA972-92-C-0020.

3. CDRL No. 0002AC-2, March 1992, Description of CE Technology For The Manufacturing Optimization (MO) System, Contract No. MDA972-92-C-0020.

4. CDRL No. 0002AC-3, May 1992, Functional Requirements and Measure of Performance For The Manufacturing Optimization (MO) System, Contract No. MDA972-92-C-0020.

5. CDRL No. 0002AC-4, December 1992, Software Design Specification For The Manufacturing Optimization (MO) System, Contract No. MDA972-92-C-0020.

6. CDRL No. 0002AC-5, July 1993, System Description For The Manufacturing Optimization (MO) System, Contract No. MDA972-92-C-0020.

7. CDRL No. 0002AC-6, September 1993, User Manual For The Manufacturing Optimization (MO) System, Contract No. MDA972-92-C-0020.

6. Notes

6.1 Acronyms

ASEM	Application Specific Electronic Module
CAEO	Computer Aided Engineering Operations
CDRL	Contract Data Requirements List
DARPA	Defense Advanced Research Projects Agency
DFMA	Design for Manufacturing and Assembly
DICE	DARPA Initiative In Concurrent Engineering
MO	Manufacturing Optimization
MSD	Missile Systems Division
MSL	Missile Systems Laboratories
OSF	Open Software Foundation
PWA	Printed Wiring Assembly
PWB	Printed Wiring Board
PWF	Printed Wiring Fabrication
ROSE	Rensselaer Object System For Engineering
STEP	Standard for Exchange of Product Model Data

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