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ADVANCED DISTRIBUTED SIMULATION TECHNOLOGY ADVANCED ROTARY WING AIRCRAFT

SOFTWARE PROGRAMMER'S MANUAL VISUAL SYSTEM MODULE

Loral Systems Company
12151-A Research Parkway
Orlando, Florida 32826-3283

April 7, 1994

Contract No. N61339-91-D-0001
ARWA - Delivery Order No. 0048
CDRL A003

Prepared for:

Simulation Training and Instrumentation Command
Naval Air Warfare Center
Training Systems Division
12350 Research Parkway
Orlando, FL 32826-3224

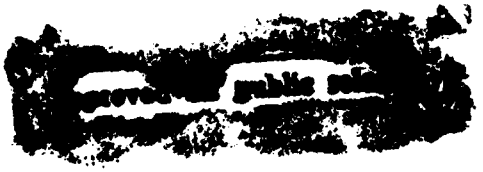

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TABLE OF CONTENTS

1. SCOPE

The scope of this Software Programmer's Manual (SPM) is discussed in the following subparagraphs 1.1, 1.2, and 1.3.

1.1 Identification

This document applies to the Advanced Rotary Wing Aircraft (ARWA) Visual System Module (VSM) Computer Software Configuration Item (CSCI). The host and target computer system for the VSM CSCI is the Harris NightHawk.

1.2 System Overview

The principal purpose of the Visual Module is to simulate out-the-window and sensor imagery and to display the imagery to the crew members of an ARWA device. The Harris NightHawk computer system runs the software which performs these functions.

1.3 Document Overview

The purpose of this document is to provide information needed by a programmer to understand the instruction set architecture of the specified host and target computers. The Software Programmer's Manual provides information that may be used to interpret, check out, troubleshoot, or modify existing software on the host and target computers.

Section 1 outlines the scope of the document.

Section 2 describes the documents referenced in this specification.

Section 3 outlines the software programming environment.

Section 4 describes the programming information relative to the host and target computers.

Section 5 provides general design notes.

2. REFERENCED DOCUMENTS

The following documents of the exact issue shown form a part of this specification to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of this specification, the contents of this specification shall be considered a superseding requirement.

Government:

MIL-STD-1815A

MIL-STD-1553B

Non-Government:

IEEE 754

IEEE 802.3

IEEE 488

Harris 0890114-060. CX/UX Programmer's Guide. October 1992.

Harris 0855004-030. Series 4000 Diagnostic Reference Manual. November 1991.

Harris 0830040-020. Series 4000 Architecture Manual. December 1991.

Harris 0890288-040. CX/UX HAPSE Reference Manual. March 1993.

Harris 0890240-020. CX/UX Hf77 FORTRAN Reference Manual. April 1991.

Harris 0891019-020 CX/UX Harris C Reference Manual. April 1991.

Harris 0890373. MC88100 Risc Microprocessor User's Manual. 1990.

3. SOFTWARE PROGRAMMING ENVIRONMENT

a. Equipment Configuration.

The computer system being used for the VSM host and target computer consists of a Harris NightHawk Series 4000 computer with 2 processors. The Series 4000 is based on the Motorola Reduced Instruction Set Computer (Risc) 32-bit MC88100 microprocessor with an integral Institute of Electronic and Electrical Engineers (IEEE) 754 Floating Point Unit. Virtual Memory and cache are provided by a Motorola MC88200 Cache/Memory Management Unit (CMMU).

The VSM computer consists of a NightHawk HN4402-AEN1 computer operating at 25 Megahertz (MHZ) requiring 120/208 Vac, 30A, 60 Hertz (Hz), two-phase input power. Included are 16 megabytes (MB) of local memory, 32 MB of global memory, a 12-slot Harris VME bus (9U), a 7 slot Versa Modular European (VME) bus (6U), two built-in RS-232 ports, 16 additional serial ports, four external interrupt receivers, a 100 MB/second memory bus, and a console processor with cathode ray tube (CRT) terminal. The HN4402-AEN1 has 2 central processing units (CPUs) and 128 kilobytes (KB) cache memory. Additional components of the computational system includes a 125 MB 1/4" Tape cartridge, a 1.2 gigabytes (GB) hard disk drive, and a 330 MB hard disk drive.

The VSM computer also houses a SCRAMNet interface board for communicating with the ESIG-2000 image generators, and an FDDI board for communicating with the Flight Station Module (FSM) and Simulation System Module (SSM) on the ARWA Global Bus. An ethernet connection allows a connection to developmental networks.

b. Operational Information.

The features and specifications summarized below apply to the Series 4400 computer system architecture.

CENTRAL PROCESSING UNIT

Longword Length - 32 bits

Processors (HN4400) - one, two, or four per system

System Bus - Harris VME (HVME)

Physical Address Space - 4GB

Floating Point - On-Chip Accelerator

Memory Management Unit - Implemented using Motorola MC88200CMMU, 25MHz 4 KB memory pages 56-entry Page Address Translation Cache

Cache Memory - Implemented using Motorola MC88200 CMMU, 25 MHz; both write-through and copy-back algorithms used; concurrent address translation and cache access.

MEMORY SUBSYSTEMS

Maximum Physical Memory - 144MB

Global Memory - 8 to 128MB (with parity)

Global Memory Config - Available in increments of 8-, 16-, 32-, and 64-MB per board; 0, 1, or 2 boards per system (note: cannot install two 8-MB boards)

On-board Memory - 0 or 16MB (with parity)

INTERRUPTS

HVME/VME - 7

High-Speed Edge-Triggered - 4

I/O Bus - 8-, 19-, or 21-Slot Harris VME (HVME), superset of VME with parity checking and synchronous burst mode performance enhancement; triple-height Eurocard (9U)

I/O Bus Performance - 40MB per second (with memory expansion); 10MB per second (without memory expansion)

COMMUNICATIONS

Serial Lines (Standard) - Two asynchronous RS-232C lines (console terminal, user)

Serial Lines (Optional) - 16-line asynchronous/ synchronous and 32-line asynchronous RS-232C multiplexers

Local-Area Network - Ethernet (IEEE 802.3), TCP/IP

Wide-Area Network - X.25 TCP/IP packet switching; Defense Data Network (DDN) conformance

Special Interfaces - MIL-STD 1553B Interface; Encore High Speed Data (HSD) channel; Digital Equipment Corporation (DEC) DR11; IEEE 488

Additional operational characteristics, capabilities and limitations of the computer system can be found in the MC88100 Risc Microprocessor User's Manual (0890373), paragraph 1.3 (Elements of the Computer System) and the Series 4000 Architecture Manual (0830040-020), paragraph 8 (Applications Information).

c. Compilations, Assemblies, and Linkages.

Equipment required for performing compilations and assemblies on the computer system consists of the HN4402-AEN1 computer and associated compilation software. All new VSM software will be written in Ada. C and FORTRAN code may be used in the case where reusable software is available. The Fortran, C, and Ada compilation software is stored on an internal hard disk. The standard Unix "edit" line editor and "vi" visual editor are standard source code editors on the NightHawk. A Harris visual editor is also available.

All C compilations and linking is performed under HARRIS C version 6.2. An overview of Harris C can be found in the CX/UX Harris C Reference Manual (0891019-020), paragraph 1 (Introduction).

All FORTRAN compilations and linking is performed under Harris FORTRAN version 6.2. An overview of Harris FORTRAN can be found in the CX/UX Hf77 FORTRAN Reference Manual (0890240-020), paragraph 1 (Introduction).

All Ada compilations and linking is performed under the Harris Ada Programming Support Environment (HAPSE) version 5.2. An overview of HAPSE 5.2 can be found in the CX/UX HAPSE Reference Manual (0890288-040), paragraph 1 (Introduction). The HAPSE tool, "ada", is a validated Ada compiler that supports the complete Ada language specification, as defined by MIL-STD-1815A. The compiler operates in several distinct phases, designed to meet the needs of the entire software development process. These phases include:

- Determination of compilation unit dependencies
- Syntax checking
- Semantic checking
- Code generation and optimization
- Instruction scheduling
- Machine-code assembly.

Various options can be invoked with "ada" that control compilation phases. For example, during preliminary software development it is often useful to limit the compilation phases to syntax and semantic checking. Errors from these phases can be automatically fed to a text editor for fast, iterative editing and compiling.

HAPSE provides several methods for generating executable programs from compiled sources. A prelinker, "a.ld", is provided that verifies and creates an executable image of all component units required for a given main unit. "a.ld" can either be invoked directly or called from the compiler "ada" or the dependency recompilation tool "a.make", if specific options are given. The HAPSE "a.make" tool provides for program generation after automatic recompilation of modified units. It operates in a similar fashion to the Harris

CX/UX operating system "make" tool, with the exception that all compilation/file depedencies are automatically determined/maintained by the tool.

The HAPSE debugger, "a.db", provides full Ada symbolic debugging facilities, including:

- Visual and line oriented screen presentation
- Symbolic access to Ada packages, variables, expressions
- Display of objects and their Ada source representation

Additional information regarding the equipment and software necessary to perform compilations and assemblies on the computer system are described in the CX/UX HAPSE Reference Manual (0890288-040), paragraph 1.3 (Compilation and Program Generation).

4. PROGRAMMING INFORMATION

a. Programming Features.

The computer's instruction set architecture is described in the MC88100 Risc Microprocessor User's Manual (0890373), paragraph 3.2 (Instruction Categories).

b. Program Instructions.

Instructions in the computer's instruction set architecture are described n the MC88100 Risc Microprocessor User's Manual (0890373), paragraph 3.4 (Instruction Set).

c. Input and Output Control Programming.

Input and output control programming of the computer system include:

(1) Initial loading and verification of computer memory.

Harris NightHawk initial loading is completed upon normal power-up booting of the system. The computer memory can be verified using the Harris Stand-Alone INTerface (SAINT). SAINT examines the system configuration and automatically determines which diagnostics should be executed. An options menu allows the operator to alter the number of passes, display options, error processing, the list of programs to be run, and the CPUs on which the programs should be executed. As each program is run, SAINT records the pass/fail status of the program and provides a comprehensive status report after all diagnostic programs have been run. SAINT is capable of running diagnostics on local, global, and HVME reflective memories.

Additional information on SAINT can be obtained in the Series 4000 Diagnostic Reference Manual (0855004-030), paragraph 2 (The Stand-Alone Interface (SAINT)).

(2) Serial and parallel data channels.

The processor motherboard has an Input/Output (I/O) port board connector that provides access to the system address and data bus, as well as some important control signals. This connector allows an I/O controller to directly connect to the processor board. Four bidirectional transceivers interface the backplane data bus to the backplane address/data

bus. Bidirectional transfers are controlled by flags that select the direction of data flow and enable the output.

(3) Discrete inputs and outputs.

The Harris NightHawk HN4402-AEN1 can communicate with discrete inputs and outputs through the HVME I/O bus.

(4) Interface components.

The Harris NightHawk HVME I/O bus is the backplane of the computer system. Attaching to the HVME board is a single processor board, a global memory board, a fixed and removable disk controller, a tape controller, an ethernet controller, a Fiber Distributed Data Interface (FDDI) interface, a SCRAMNet reflective memory interface, and a printer interface.

(5) Device numbers, operational codes, and memory locations for peripheral equipment.

Device numbers and memory locations within the HN4402-AEN1 can be allocated by the user. HVME Primary I/O is allocated from memory address 0xc1000000 to 0xd5ffffff. Third party A32 primary I/O is allocated from memory address 0xe0000000 to 0xfeffffff. Third party A24 primary I/O is allocated from memory address 0xff000000 to 0xfff6ffff and from memory address 0xfff80000 to 0xfffeffff. Third party A16 primary I/O is allocated from memory address 0xffff0000 to 0xffffffff.

d. Additional or Special Techniques.

I/O interfaces between the ESIG-2000 image generator and the NightHawk is performed via SCRAMNet reflective memory. Communication between the ARWA Global bus and the NightHawk is performed via an FDDI interface.

e. Programming examples.

Programming examples can be found in the CX/UX Programmer's Guide (0890114-060) as follows:

Appendix A	Message Queue Facilities examples
Appendix B	Synchronization Tools examples
Appendix C	Interval Timer examples
Appendix D	Signal Facilities examples
Appendix E	User-Level Interrupt Routines examples 1
Appendix F	User-Level Interrupt Routines examples 2
Appendix G	High-Speed Data (HSD(E)) examples
Appendix H	Harris Reflective Memory (HRM) examples

Programming examples can be found in the CX/UX HAPSE Reference Manual (0890288-040) as follows:

Paragraph 4	HAPSE Compiler examples
Paragraph 6	HAPSE Programming examples
Paragraph 9	Implementation-Dependent Characteristics examples
Paragraph 11	Shared Memory and Process Communication examples
Paragraph 12	Compiler Configuration examples
Paragraph 13	Real-Time Extensions examples

Paragraph 14	Additional Support Packages examples
Paragraph 15	Real-Time Event Tracing examples
Paragraph 18	Real-Time Ada Tasking examples
Paragraph 20	ARMS Configuration Control example examples
Paragraph 21	ARMS Task Interrupt Entries example examples
Paragraph 22	ARMS Cyclic Scheduling examples
Paragraph 23	ARMS External Interface Issues examples
Paragraph 24	ARMS Troubleshooting examples
Paragraph 27	Sample Line Mode Debugger Session examples
Paragraph 28	Sample Visual Mode Debugger Session examples

f. Error detection and diagnostic features.

The I/O Subsystem test verifies the CX/UX system I/O configuration. Functionality of I/O controllers and attached peripherals is verified by the tests in "cxio." The "cxio" diagnostic allows testing of the following I/O devices: disk drive, 1/2 inch (9-track) tape, 1/4 inch cartridge tape, CRT terminal, asynchronous I/O port turnaround (RS-232/RS-422), printer, plotter, X.25 port to port loop back, real time clock, edge triggered interrupt / programmable interrupt generator, HSD (high speed data interface) to HSD loop back, DEC DR11W emulator loop back, and shared memory.

5. NOTES

ACRONYM LIST

ARWA	Advanced Rotary Wing Aircraft
CMMU	Cache/Memory Management Unit
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CSCI	Computer Software Configuration Item
DDN	Defense Data Network
DEC	Digital Equipment Corporation
FDDI	Fiber Distributed Data Interface
FSM	Flight Station Module
GB	Gigabyte
HAPSE	Harris Ada Programming Support Environment
HRM	Harris Reflective Memory
HSD(E)	High Speed Data
HVME	Harris Versa Modular European
HZ	Hertz
IEEE	Institute of Electronics and Electrical Engineers
I/O	Input/Output
KB	Kilobyte
MB	Megabyte
MHZ	Megahertz

RISC	Reduced Instruction Set Computer
SAINT	Stand-Alone INTerface
SPM	Software Programmer's Manual
SSM	Simulator System Module
VME	Versa Modular European
VSM	Visual System Module

6. APPENDICES

Not Applicable.