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Quarterly Progress Report #5
10/1/92 - 12/31/92

Field Emitter Array RF Amplifier Development Project
Phase One, Cathode Technology Development
DARPA Contract #MDA 972-91-C-0028

Sponsored by:
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13. ABSTRACT (*Maximum 200 words*)

Fifth Quarterly R&D Status / Technical report for the Field Emitter Array RF Amplifier Development Project - Phase I, Cathode Technology Development. Electrical tests of field emitter arrays fabricated at MCNC have demonstrated modulation of the anode current at 1 GHz. DC testing continues at an aggressive pace. The vacuum bonder and test system is installed. The test chamber has been outfitted for DC and RF testing, with feedthroughs rated for 5 kV at 1 A DC, and 700 V at 1 A for high frequencies. The test chamber routinely gives vacuum levels in the low 10^{-8} torr range with overnight bakeout. Developments in device processing continue. New techniques for deposition of thick oxide layers are under development. In-house chem-mechanical polishing of wafers for planarization is time-consuming, but has proven more successful than polishing by external vendors.

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DARPA Contract #MDA 972-91-C-0028

MCNC Field Emitter Array RF Amplifier Development Program
Phase One, Cathode Technology Development - DARPA Contract MDA 972-91-C-0028

Fifth Quarter - December 1992

Key Ideas

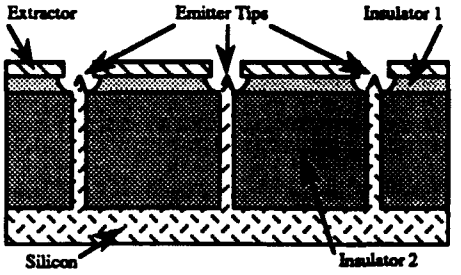
Develop microstructural field emission diodes and triodes with a cutoff frequency above 1 GHz, 5 A/cm^2 at < 200 V gate to emitter bias, and > 100 hour lifetime.

Reduce capacitance and increase transconductance of FEA devices to improve frequency response. Focus on development of tall emitter columns to minimize capacitance. Evaluate low work function materials for emitter surface coatings, reduce gate dimensions, and improve tip sharpening to increase transconductance.

Examine various test methods to permit characterization of more devices per test cycle. Evaluate test fixtures including controlled impedance RF test fixtures, vacuum tubes, and several methods of microencapsulation.

Develop a circuit model for our versions of the FEA device. Characterize the model for use in RF amplifier design and implementation. Establish model consistency across manufacturing methods and yield.

MCNC Silicon Field Emitter with Column



Major Accomplishments:

Demonstrated anode current modulation at 1 GHz on a field emitter array with gate to emitter bias < 200 V. Several devices have produced repeatable measurements.

Test chamber at MCNC outfitted for DC characterization and RF testing. Bakeout of the test chamber gives vacuum levels in the low 10^{-8} Torr overnight. Electrical feedthroughs installed, with ratings of to 5 kV at 1 A for DC, 700 V at 1 A for high frequency signals.

Gated columnar structures delivered to subprogram at Litton for further testing in amplifier modules. Samples with diamond-like coatings delivered to NRL for testing.

Major Milestones - This quarter and upcoming quarter:

Fabricate devices capable of meeting frequency response requirement and providing current density of 5 A/cm^2 for > 100 hours. Apply all acquired processing knowledge to a single run to produce the best devices possible.

Continue DC testing of field emitter arrays on an aggressive schedule. Screen arrays with acceptable perfomance for RF characterisitics. Automate data collection equipment for lifetime testing.

Construct thin-film microencapsulated FEA and test. Fully qualify vacuum bonding press to design specifications. Produce microencapsulated devices with vacuum test and microencapsulation system.

Field Emitter Array RF Amplifier Development Project
Phase 1, Cathode Technology Development

I. Executive Summary

Progress in research and development continues at all sites. MCNC's program continues at full speed with smooth transition of project leadership.

- Electrical tests of field emitter arrays fabricated at MCNC have demonstrated modulation of the anode current at 1 GHz. DC testing continues at an aggressive pace.

- Vacuum bonder and test system is installed. The test chamber has been outfitted for DC and RF testing, with feedthroughs rated for 5 kV at 1 A DC, and 700 V at 1 A for high frequencies. The test chamber routinely gives vacuum levels in the low 10^{-8} Torr range with overnight bakeout.

- Developments in processing continue. New techniques for deposition of thick oxide layers are under development. In-house chem-mechanical polishing of wafers for planarization is time-consuming, but has proven more successful than polishing by external vendors.

II. Milestone Status:

Task	Completion Date	
	Original	Complete Expected
Complete first diodes of each of the three device types: Horizontal, vertical, and trench. Deliver samples to NRL, NCSU, and Litton. (MCNC)	11/91	11/91
Prepare first pass device models and potential circuit models based on initial device IV data. (Duke, MCNC, and UNC-CH)	3/92	11/92
Down select RF FEA designs based on device performance predictions	3/92	12/91
Complete first generation of field emission IV curves for each of the device types fabricated along with initial electron trajectory data and electron time of flight data. (NCSU and MCNC)	3/92	3/92 & Continuing
Design and order vacuum sealing and test system (MCNC)	11/91	12/91
Modify Litton trajectory modeling programs for field emission. Initial macroscale high vacuum tube encapsulation of field emission cathodes. (Litton)	3/92	11/91
Complete second set of field emission diode device runs with column FEAs (MCNC)	3/92	3/92
Complete third series of gated column emitters with modifications for very low electric fields over gate emitter isolations to reduce gate leakage	-	5/92
Complete new mask set for half micron field emission devices. (MCNC)	5/92	3/92
Install vacuum sealing and test system (MCNC) MCNC set-up a temporary vacuum test system in a SEM (3/92)	3/92	10/92
Complete initial electron trajectory modeling and initial testing of macroscale tubes containing microstructural gated FEC diodes. (Litton)	7/92	10/92
Complete fabrication of first microencapsulated FEC transistors. (MCNC)	9/92	1/93
Generate first pass transistor data from microencapsulated FE transistors. (MCNC, Duke, and Litton)	9/92	2/93
Demonstrate microstructural FEA diode/open triode devices meeting device IV and g_m/C program requirements.	9/92	3/93
Determine priorities of future device development. Determine the primary amplifier design methodology from the three amplifier design approaches. (MCNC)	9/92	3/93
Complete design for first integrated FEC based RF amplifier and FEC tube RF amplifier based on device characterizations. (MCNC, Duke, and Litton)	3/93	3/93
Complete second level models for FEC emission from surfaces treated in various manners. (UNC-CH)	3/93	3/93
Complete testing of FEC electron trajectories, electron trajectory model verification. (NCSU, Litton)	3/93	3/93
Determine packaging and cooling requirements for the prototype RF amplifier. (MCNC and Litton)	3/93	3/93

III. Technical Progress:

1.0 Electrical testing and high-frequency performance measurements.

1.1 Field emitter arrays were tested at MCNC and NCSU that demonstrated modulation of the anode current at 1 GHz. The test fixture used for these measurements is shown in Figure 1. An oscilloscope with signal processing capability was used to eliminate the background signal due to the gate-to-anode capacitance. With the emission current off and a 1 GHz sine wave signal applied to the gate electrode, a sample trace of the background due to the gate-to-anode capacitance was acquired. The calibrated signal, defined as the live signal minus the background, was acquired. Any 1 GHz sinusoidal signal appearing in the calibrated signal is due to the modulation of the anode current.

A sample trace of the calibrated signal is shown in Figure 2. As expected, there is no sinusoidal signal present, but simply a band of noise around the ground level. A DC bias was then applied to the gate until emission current was observed. A trace of the resulting calibrated signal is shown in Figure 3. A sine wave 1 GHz with some added noise is clearly visible.

1.2 A limited amount of testing was done on a wafer from the thin-film encapsulation lot after the gate-to-anode insulating layer was complete and the emitter cavities opened. If no emission current could be obtained from the devices at this point, further processing of the devices would not be productive. Some promising results were obtained, and testing continues.

2.0 Device processing.

2.1 A new technique was developed to solve the "keyhole" problem described in the previous Quarterly Report. This effect had been noticed in earlier months after an insulating oxide had been deposited onto field emitter arrays with tight emitter tip-to-emitter tip spacing. A new deposition technique involving the repeated application of evaporated SiO_2 layers using photoresist to planarize layers between applications was developed This technique proved successful in eliminating the "keyholes" between the column structures.

The concept behind the technique is to fill in the areas between field emitter columns gradually by repeated applications of LPCVD oxide, followed by the appropriate etchbacks to build up a thick, even layer of insulator. First a layer of oxide is deposited over the arrays, thickly coating the studs as well as the areas in between. This is followed by an application of PC3-6000 (a brand of photoresist from Futurrex, Inc. in Newton, NJ) that covers everything with a very planar coating. The PC3-6000 is then partially etched back, exposing only the tops of the oxide-covered columns, taking advantage of the height difference between the oxide covering the field emitter columns and the oxide fill-in between columns. This enables the oxide to be stripped from the silicon columns by repeated immersions in BOE without effecting the base layer that still lies beneath the coating. After the oxide has been sufficiently cleared away from the columns, the remaining PC3-6000 can be removed and the whole process begun again with a higher base level of insulator to build on. The multi-step insulator fill-in technique is used in the current processing.

2.2 Wafers from several lots were prepared for chem-mechanical polishing (CMP), and sent to outside vendors contacted at the SRC topical research conference on CMP for Planarization in September 1992. Polishing was performed by two selected vendors with generally poor results. The first vendor tended to overpolish the wafers, leaving very little of the emitter structure on the wafer. Poor process control was cited as the reason, mainly the lack of accurate means to measure the remaining oxide layer during the polishing process. Mechanical measurement techniques were used on control samples. This method is not as accurate as optical methods used by the second vendor.

The second vendor consistently underpolished the wafers. This vendor had proper measurement equipment, but was overcautious about leaving enough oxide to prevent damage to the emitter

structures. The vendor also complained that there was no layer on the wafers to serve as a polish stop to let them know when polishing was complete. This lead to time-consuming iterations of polishing work by the vendor and inspection and measurement by MCNC.

Even when polishing was successful, both vendors suffered a significant yield loss due to wafer breakage. On the average, only 20% of the wafers sent out were returned with successful polishing. CMP is a new technique that may be applicable to future wafer processing. At this point, however, the uniformity and polish depth control as well as yield are unacceptable.

In-house experiments with CMP for wafer planarization showed that machine polishing with a soft pad was accurate but slow. A manual lapping technique using a glass substrate with water as the polishing compound slurry carrier significantly increased the speed of polishing. Despite the speed increase, the process is still extremely time consuming. If possible, an alternative method of planarization should be incorporated into the process flow.

3.0 Vacuum testing and microencapsulation bonding system.

3.1 A photo of the installed system is shown in Figure 4. In December of 1992, the process of qualification was begun on the bonder/tester double-chamber vacuum system delivered to MCNC on 21 October 1992. During this break-in period the testing chamber held up very well, consistently providing test environments in the low 10^{-8} Torr range on a routine basis. The addition of a heating jacket around its outer surface (applied 13 January 1993) has enabled the chamber to attain higher vacuum levels by driving some of the residual water vapor off the inner walls. Since that time the testing chamber has been used repeatedly, including a demonstration test set-up for the DARPA review at MCNC on 4 February 1993. A photo of the system control panel is shown in Figure 5.

In contrast, however, the bonding chamber has been undergoing some major problems. Qualification of the bonding chamber includes the verification of the temperature of the internal wafer press required for wafer bonding under vacuum. On 21 December 1992, the chamber was put through the most demanding test of this process: the interior temperature was driven to the upper limit of spec (800 °C) before system breakdown brought matters to a halt. A post-mortem examination of the chamber in mid-January 1993 revealed the primary cause of failure to be an electrical short in the internal wiring providing power to the heating coil. The high heat had in fact melted the Teflon insulation in many places, allowing electrical contact between the exposed wires. There was also a breakdown in the system's power distribution unit, possibly as a result of the short in the heating circuitry. A wire was burned out within a mechanical relay and was repaired on 11 January 1993.

As a possible solution to the major problem, an alternate method of routing the leads into the system was attempted, wherein ceramic insulation would be used instead of the Teflon, and the wiring would be fed into the chamber through a different port. This approach never proved entirely successful, especially at a later stage in the repairs when it became apparent that the original scheme would be much easier to put together.

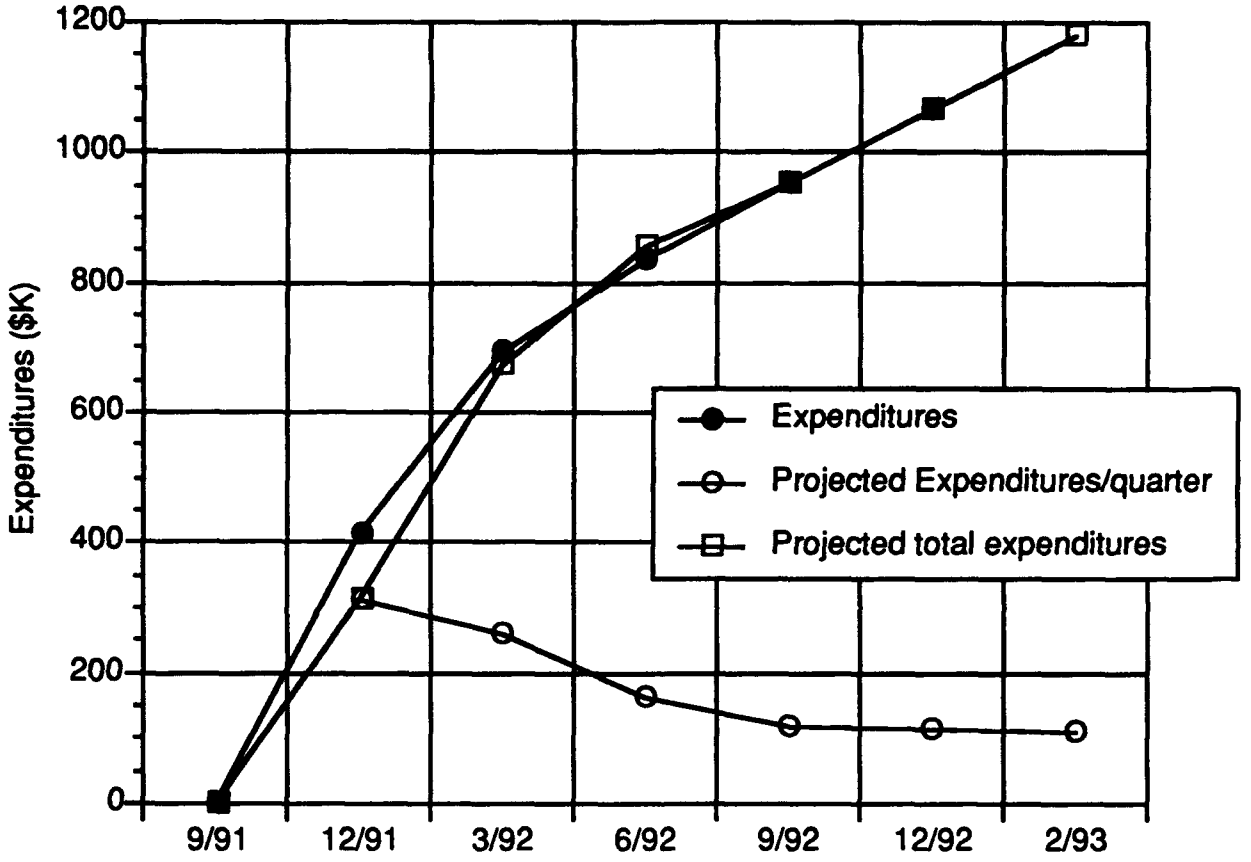
Complicating the process of repair to the system was the fact that, at first glance, the important connections needing to be made between the wiring and and the heating coil had to be done within the bonding chamber itself, with only a 10" diameter port providing working access, and where thermal shielding was often in the way. To overcome these problems, the internal shielding arrangement needed first to be disassembled, and the wafer press/heating coil assembly extracted from the constricted volume of the chamber, where it could be worked on much more easily. A new heating coil was then installed in the press and connected to a new set of Teflon-insulated leads with fiberglass sleeving. The rejuvenated wafer press was then carefully replaced within the bonding chamber and the thermal shielding intricately reassembled. This repair work was often quite tedious, and required several sessions involving MCNC personnel and the local vendor (LitCo Industries, Raleigh NC).

As a result of these repairs, the bonding chamber is currently back in its original condition, the only design change being that the heating circuitry that had previously melted and shorted together has now been sleeved in fiberglass. The range of the heating coil has not been tested with the new wiring. It may be necessary to limit temperature operations below a certain level (750 °C, for example) as further protection against insulation breakdown.

4.0 Other Developments

4.1 Researchers at MCNC theorized that the aluminum metalization on the backside of the wafers was forming a reverse-biased Schottky junction and limiting the emission current obtainable from our devices. Testing on a bare wafer with backside metal indicated that the contact was Ohmic in nature.

IV. Fiscal Status



Expenditures this quarter (10/01/92 - 12/31/92)	$116,514.43
Total expenditures to date (9/09/91 - 12/31/92)	1,067,744.61
Projected expenditures:	
1/93 - 3/93	110,691.39
Contract Amount (Basic)	$1,178,466.00

V. Problem Areas

A significant problem faced by the MCNC field emitter program is the identification and elimination of the causes of excessive gate current in gated emitter arrays. Current processing leaves the emitter tip well below the level of the gate metal. Since electrons are emitted in a volume that is roughly cone-shaped, many of the electrons intercept the gate metal before they can escape to the space between the gate and anode. If the peak of the emitter tip could be placed in the center of the thickness of the gate metal consistently, it is likely that the gate intercept of emitted electrons could be reduced. This consistent placement of the emitter tips drives efforts at planarization of the insulating oxide layer between the emitter substrate and the gate metal. These efforts have included CMP and multi-layer oxide deposition.

While the field emitter arrays produced at MCNC have shown anode current modulation at 1 GHz, the current density and total current of these arrays falls short of the targets set by DARPA. Other devices have demonstrated the necessary current per tip to produce the required current density at the tip packing density of MCNC's arrays, but none have shown the required total current. No single array of devices has demonstrated all the performance requirements. All the information gathered from processing done up to this point will be applied to future runs to produce the best possible devices.

VI. Visits and Technical Presentations

Numerous closed meetings were held between MCNC staff and its subcontractors. As indicated in the previous quarterly report, only two presentations on this project have been made outside the direct program participants during the contract time period covered by this report. Researchers from the program at MCNC and the subprograms attended the DARPA Vacuum Microelectronics Initiative Review on 14 & 15 October, 1992. Dr. Jiang Liu from the subprogram at NCSU presented a paper at the International Electron Devices Meeting (14-18 December, 1992, San Francisco, CA). A copy of this paper as it appears in the conference proceedings was given as Attachment G in the fourth quarterly report. No other outside presentations are planned at this time.

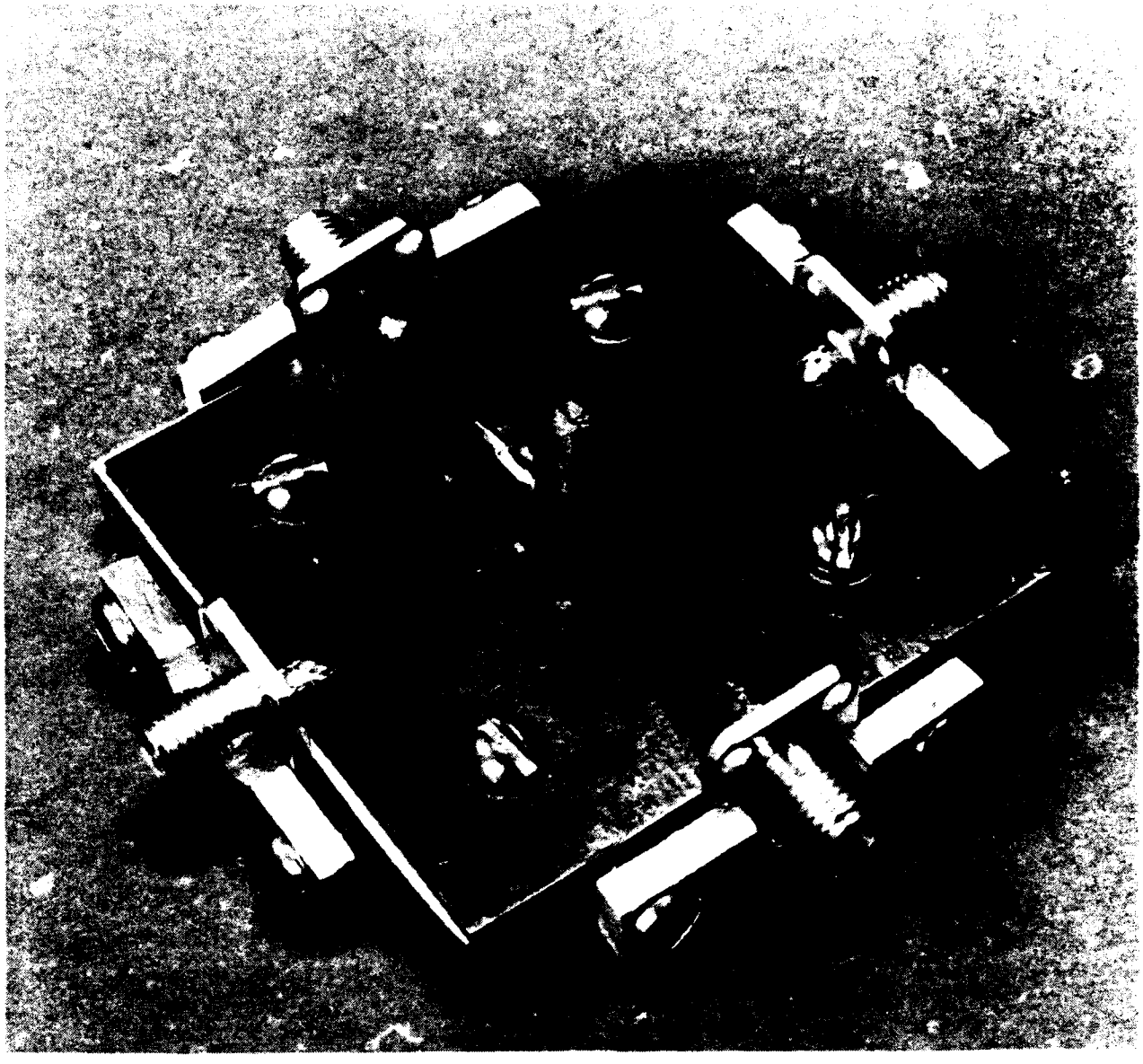


Figure 1: High-frequency test fixture.

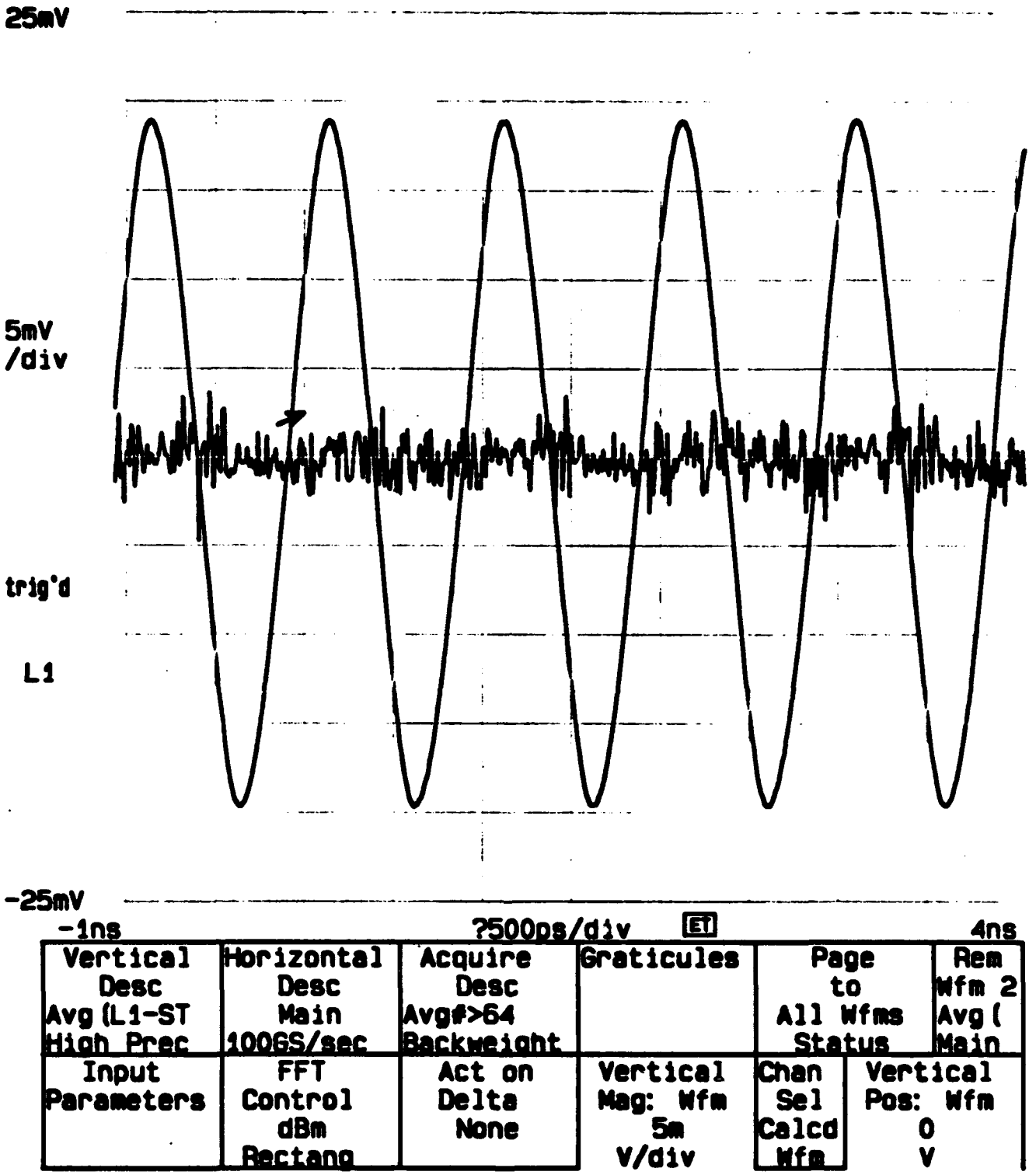


Figure 2: Calibrated signal with no emission current.

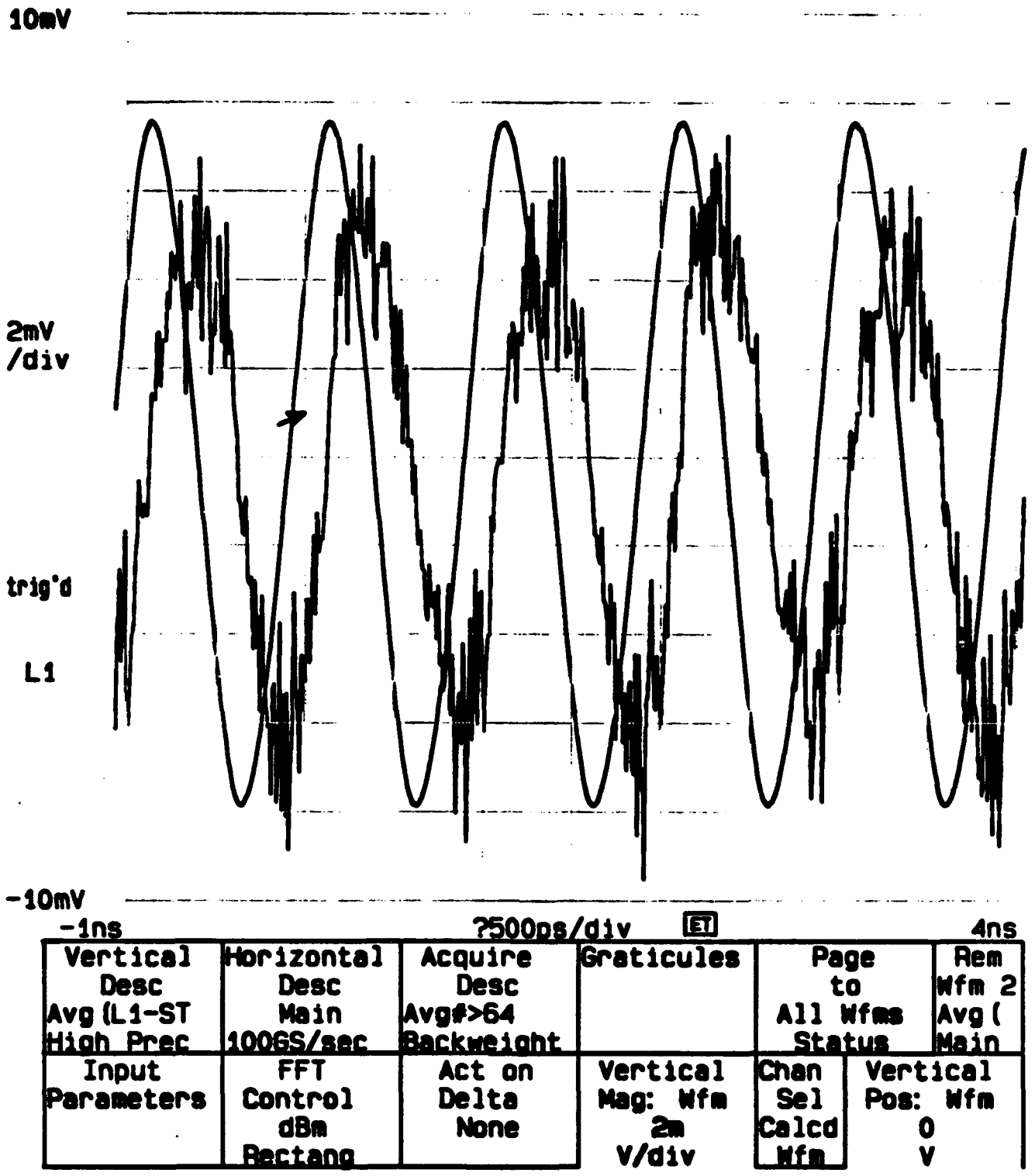


Figure 3: Calibrated signal, emitters on. 1 GHz sine wave clearly visible.

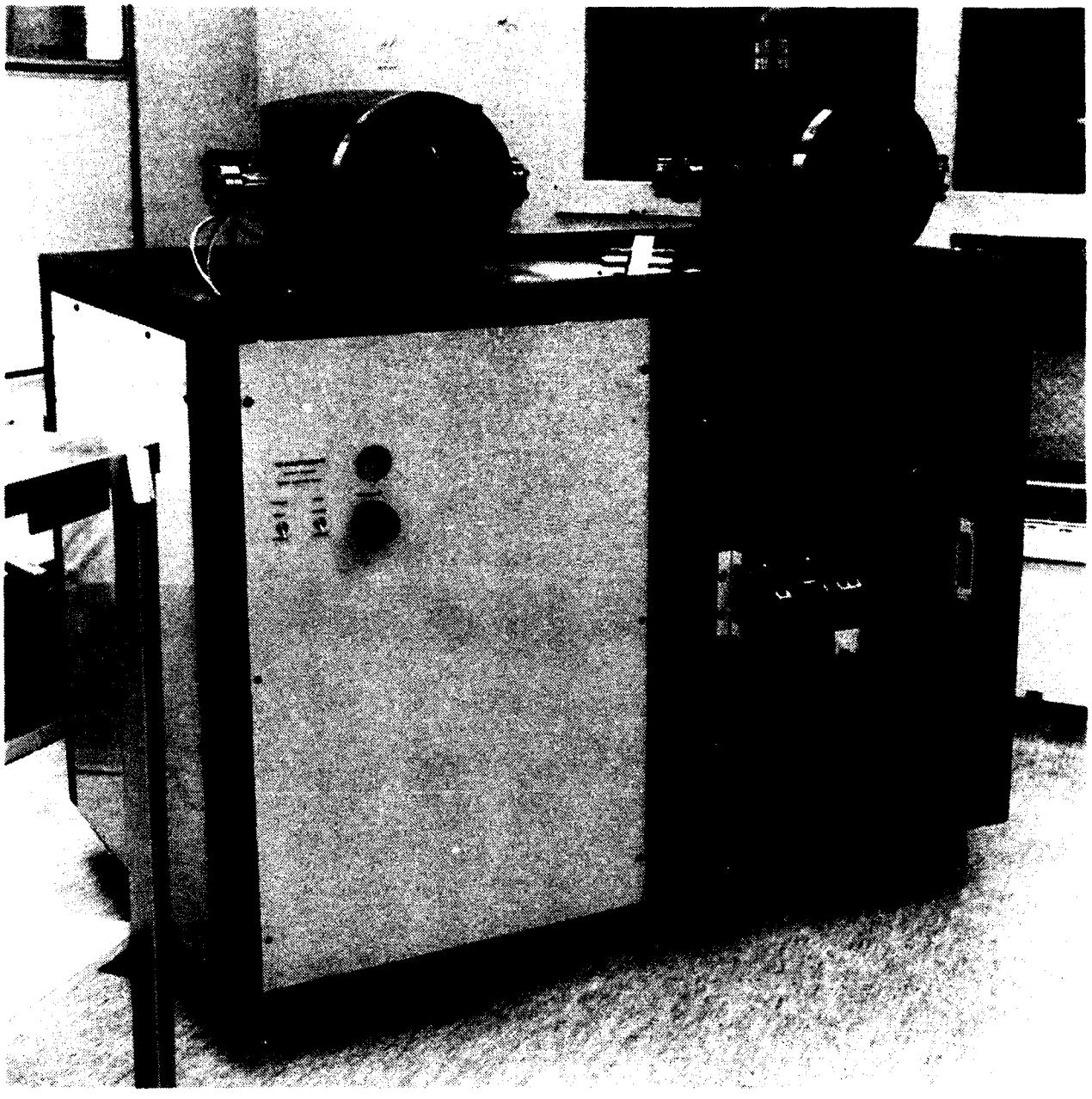


Figure 4: Installed vacuum bonder/test system at MCNC.

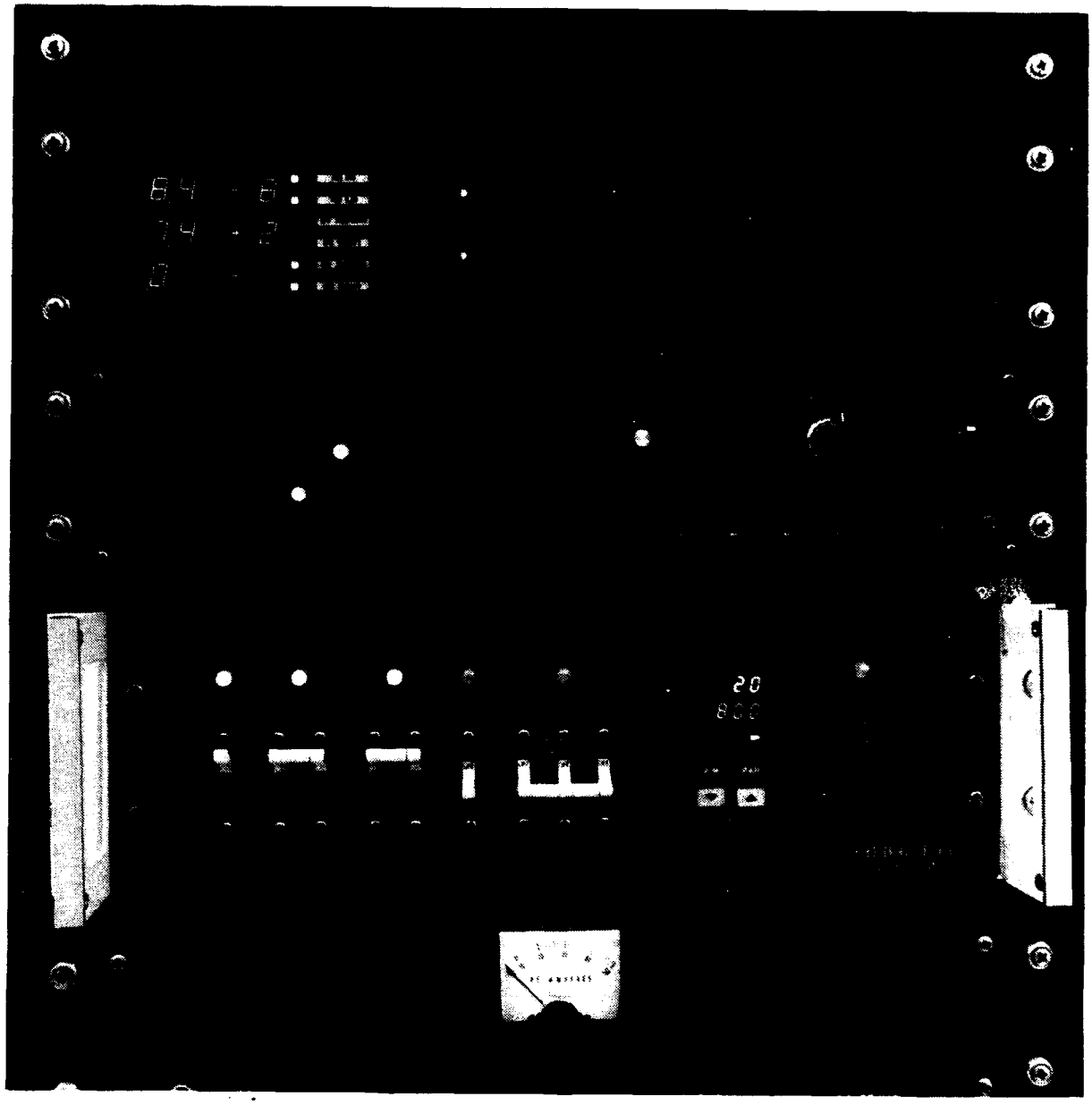


Figure 5: Control panel of vacuum system.