CAS Inc.
WEAPON SYSTEMS ANALYSIS

P.O. Box 11190
Huntsville, AL 35814
Telecopier (205) 895-8668

CAS ASD REPORT 921155
ADVANCED INTEGRATED AIRCRAFT SURVIVABILITY EQUIPMENT ANALYSIS
FINAL REPORT ADDENDUM

28 MAY 1992

"The views, opinions, and findings contained in this document are those of the author(s) and should not be construed as official Department of the Army position, policy, or decision, unless so designated by other official documentation"

Prepared By: _____ Contract No.: DAAJ09-89-D-0021/0022
Keith Zook

Classification and
Content Approved by: _____ Data Item No.: A002
A. Darryl Wortman

650 Discovery Drive • Huntsville, AL 35806 • (205) 895-8600
555 Sparkman Drive, Suite 1022 • Huntsville, AL 35816 • (205) 895-8800

TABLE OF CONTENTS

LIST OF FIGURES AND TABLES

1.0 SCOPE

This document provides detailed information which is in addition to, or a further explanation of, the information presented in Delivery Order 022, Contract DAAJ09-89-D-0021, Advanced Integrated Aircraft Survivability Equipment Analysis Final Report.

2.0 DETAILED INFORMATION

2.1 COMMUNICATION INTERFACE AND PROCESSOR COST

Defining individual component costs of processors and interconnects does not illustrate the true cost impact of the component. For example, VME and MIL-STD-1553B are the only two individual options for interconnects and processors with a significant per part cost savings. VME is undesirable for reasons other than cost, while MIL-STD-1553B was selected as the best Local Area Network (LAN) for AIASE. Per part costs for all of the other options, PI-Bus vs. Futurebus+ and R4000 vs. 80960MX, will be similar.

The average cost of a SEM-E module in the late 1990's has been estimated at $17,000 (1987 dollars used throughout). The primary driver in module cost is normally memory and manufacturing. A processor or interface device typically represents only 5% to 10% of the total module purchase cost. The High Speed Data Bus (HSDB) is an exception due to the high number of hybrid components. The HSDB interconnect components may represent more than 50% of the module's estimated $28,000 cost. In addition, a HSDB requires a coupler external to the module which is significantly more complex than a 1553 bus coupler (see Figure 2-1). The cost of the coupler is highly dependent on the number of terminals on the HSDB.

Rather than procurement costs, the more significant cost driver for most components is the level of integration and support difficulties introduced. Each component type must be designed, simulated, prototyped, integrated with a prototype module (including integration with software drivers, operating systems, and applications), tested, redesigned (usually), integrated with a production module, tested, and finally used in the system. At that time the component must be supported by field test equipment and the logistics system. This cycle must be followed for each component used. If common components are used, the development cost is paid only once or is shared among multiple modules. The support costs are minimized because fewer part types and less special test equipment is needed. If the components conform to an industry standard, then manufacturers may be willing to invest in the early stages of the cycle with the hopes of developing

a better, yet compatible, component. This would be similar to the current availability of 80X86 processors from non-Intel manufacturers.

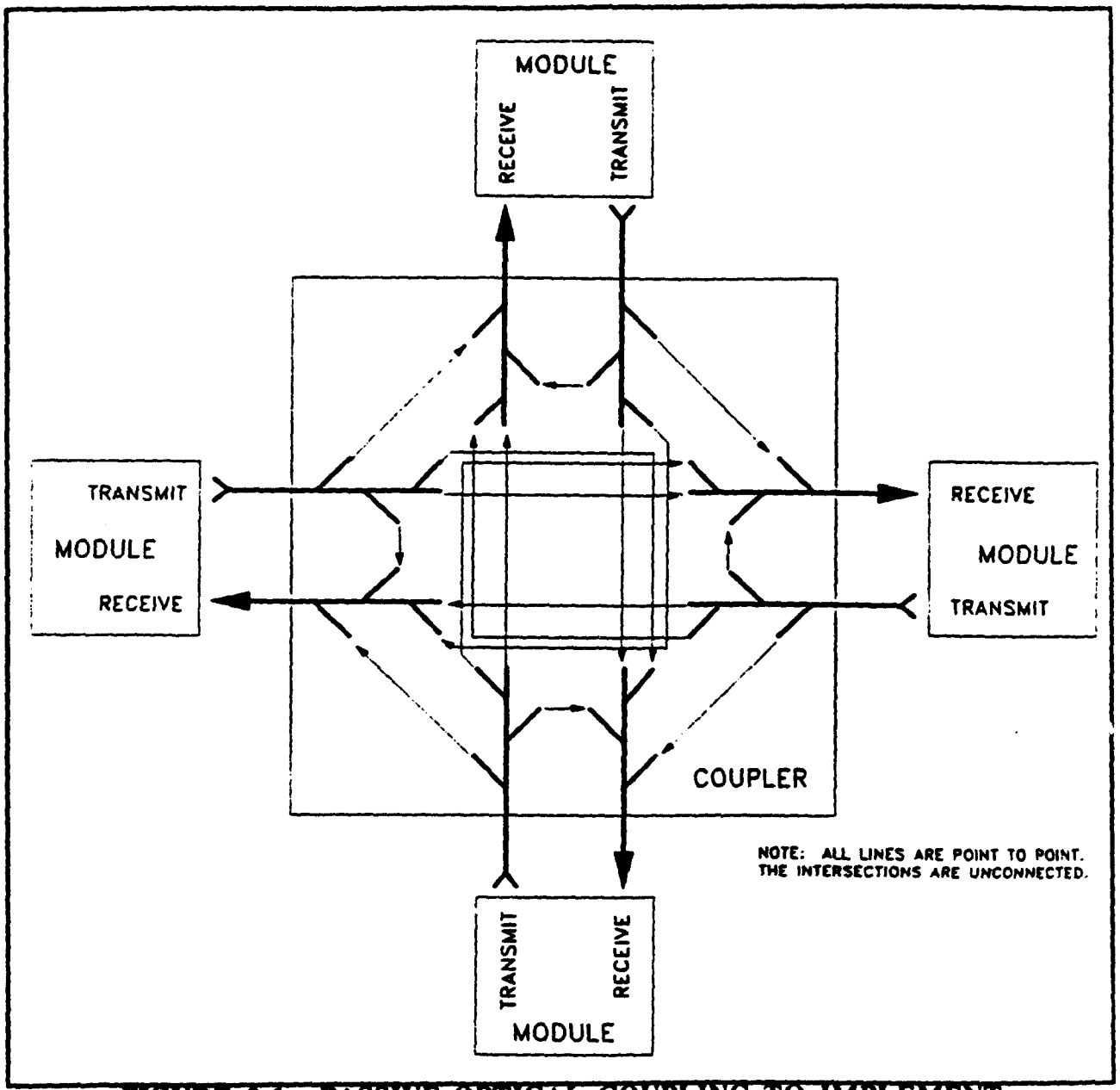

FIGURE 2-1. PASSIVE OPTICAL COUPLING TO IMPLEMENT A LINEAR BUS

The cost benefits of commonality are different for the different integration levels (component, module, subsystem, system, platform, service, DoD). The Institute for Defense Analysis (IDA) Commonality Study and the Comanche responses to the Office of the Secretary Of Defense (OSD) Commonality Questionnaire reveal that the life cycle cost benefits decrease as

commonality is applied to higher levels. For example, a common module within a subsystem provides a higher cost benefit than a common module applied between platforms. Although only commonality at the module level was studied, an extrapolation to the component level can be made. The reason for decreasing cost benefits as commonality is applied at higher levels is due primarily to the increased complexity of configuration management and the broadening requirements which must be met by the module.

The conclusion is that cost savings are best realized by selecting the most mature components that will meet similar requirements. The following paragraphs and Table 2-1 provide information on the development state of each option. The final report provides details regarding the capabilities of each option.

The PI-Bus market is tied directly to military aviation programs. With the uncertainty of Comanche production, production PI-Bus parts may be limited to the Delco chip developed for F-22 and the TI chip developed for the F-16 Modular Mission Computer (MMC). Any changes in these programs would have serious effects on the cost and availability of PI-Bus parts.

Futurebus+ is currently available only in small quantities as multi-chip implementations without full functionality. None of these implementations are currently qualified for the military environment. The market pressure from the Navy's Next Generation Computer Resources (NGCR) program will ensure the availability of military Futurebus+ parts, but the available protocol functions may be limited.

The VME-Bus is currently available. Although it is a clear winner on cost, it does not rate favorably in other criteria.

The MIL-STD-1553 Bus is currently available and is a much simpler technology than High Speed Data Bus. The costs of a 1553 bus implementation are significantly less (70% to 80%) than that of the HSDB.

TABLE 2-1. COMMUNICATION INTERFACE AND PROCESSOR COST FACTORS

	COMM PROGRAMS	MIL PROGRAMS	STANDARDS	SPEC LEVEL	PROTO-TYPED	PRODUCTION YEAR
1553	None	Very Many	MIL-STD-1553B, Many Handbook, Application, and Test Guides	Complete	Yes	Now
HSDB	None	F-22, RAH-66	SAE AS4074, SAE AIR 4288 Users Handbook, JIAWG	Complete	Yes	Mid/late 90's
PI-Bus	None	F-22, RAH-66, F-16	SAE, JIAWG	Complete	Yes	Mid/late 90's
Futurebus+	Work-stations	Many Expected	IEEE, NGCR, SAVA	SEM-E Profile Due in Late 1992	Yes	1992/1993 for Commercial
VME	Very Many	Many	VITA	Complete	Yes	Now
TM-Bus	Boeing 777, Test Equipment	F-22, RAH-66, F-16	SAE AS 4765, IEEE 1149.5, JIAWG	Nearing Completion	Yes	Early/mid 90's
IEEE 1394	Apple	None	NGCR, IEEE	Electrical Only	No	Mid/late 90's
R3000/R4000	Work-stations	F-16	ACE, JIAWG	Complete	Yes	Now
80960MX	None	F-22, RAH-66	JIAWG	Complete	Yes	Now

The High Speed Data Bus is in a situation similar to that of the PI-Bus. It is mainly driven by military aviation programs, with Comanche and F-22 the primary proponents. Production parts for a HSDB are tied to these two programs. Again, with the uncertainty of Comanche production, production HSDB parts may be limited to the Harris parts developed for the F-22.

The currently planned military TM-Bus implementations are an integral part of a maintenance controller function that resides within a Multi-Chip Module (MCM). There are commercially planned implementations that are separate devices that interface to a processor/controller. There are efforts underway to make the protocol and physical layer specifications for the commercial and military TM-Buses the same. If this occurs, the market will apply downward pressure on the cost and availability of a TM-Bus device. This will occur irrespective of the military demands.

The IEEE 1394 Serial Bus is currently an electrical specification without a protocol. The NGCR program is backing this interconnect and Apple computer is proposing to use it in their next generation of computers. There are currently no military platforms specifically backing the 1394 bus. There are no manufacturers publicly planning to make devices available, therefore no cost information is available.

The MIPSCO R3000 processor is used in multiple military configurations, including on a SEM-E module in the F-16 MMC. It is acknowledged as one of the commercial industry standards

in the workstation arena. The MIPSCO R4000 is a follow-on to the R3000 and is currently available in workstations from Silicon Graphics. The R4000 has been proposed for numerous military applications. Multiple manufacturers are working on a military qualified R4000. The commercial market forces will drive the cost and availability of this processor.

The Intel 80960MX processor is used on the F-22 and the RAH-66 and has been proposed on numerous military products. It is currently available from Intel only in small quantities. The cost and availability of the 960 is tied to the F-22 and RAH-66.

2.2 HIGH SPEED DATA BUS OPTICAL COUPLERS

Two LAN candidates were considered to support the inter-ASE communication between the Integration Processor, ATIRCMS, ATRJ, AOCMS, and AVR-2. MIL-STD-1553B is a well documented and understood linear protocol, implemented on a two wire electrical medium, and operating at a 1 MHz bit rate. The HSDB is a linear protocol implemented on an optical fiber medium which can operate at a 50 MHz bit rate.

Unlike electrical traces in a backplane, optical fibers do not naturally form a linear interconnect. Fibers transmit light unidirectionally from an emitter, such as an LED, to a light sensing receiver (photo-diode). Two fibers are required to facilitate duplex communication. To implement a linear protocol on an inherently point-to-point medium, a coupling device is required to "split" the light emanating from one light source into multiple fibers connected to the receiver pins of the terminals on the HSDB. This is logically depicted in Figure 2-1.

Two types of couplers are available. A passive coupler uses splices to ensure that all transmitters have optical paths to all receivers. They require no re-generation or re-timing of signals and are therefore simpler and less costly than a coupler that actively receives and re-transmits. There is a limited optical power budget bounded by the power available at the light source and the sensitivity of the optical receivers. Each splice and connector between the transmitter source and receiver represents a power loss. The more terminals on a HSDB, the more splicing required to implement the linear connectivity. Thus, passive couplers are generally limited to 6 or less terminals. For systems with a larger terminal count, active couplers are required to "boost" the optical power. The AIASE maximum terminal count would be 5 (i.e. 4 AT systems and 1 IP).

The type of coupler is a system decision based on the total optical budget available for the selected HSDB modules. In general, a given HSDB module will work with either an active or passive coupler, as long as the system power budget is not exceeded.

2.3 ARCHITECTURE EVALUATION CRITERIA

As stated in D.O. 022, paragraph 9.1.2, some criteria for the architecture evaluation were eliminated because they were not discriminating. This statement was made in the context of the architectural element discussion with the intent being that some architectural criteria are not discriminating because the options are being developed within the framework of the ongoing AT system programs. These options are evaluated by the AT system developers based on their perceived requirements. For instance, the AT system architecture's floating point capability is being designed to meet the resident algorithms' floating point requirement, and thus the capability will not be a discriminating factor between architecture options.

For the AIASE architecture, the evaluation criteria was categorized into processing, interconnect, enclosure, software, and front-end elements. In the system development cycle, pertinent criteria are used to assess the system elements. A draft list of potential criteria for each element is provided in Table 2-2.

TABLE 2-2. POTENTIAL CRITERIA FOR SYSTEM ELEMENTS

PROCESSING	MIPS rating, MOPS rating, MFLOPS rating, memory access time required, cache size, interrupt latency, context switch time, virtual addressing capability, security features, fault tolerance
INTERCONNECT	As provided in D.O. 022 Final Report
ENCLOSURE	Size, orientation, cooling method, environmental protection, module access, backplane access, harness access, power conditioning
SOFTWARE	Software development system tools (requirements to design and design to code traceability, language sensitive editor, host compiler-debugger-simulator-evaluator, target compiler, multiuser target debugger, target loader, etc), embedded processor support (run time system, metrics), compiler system expansion factor rating, compiler system optimization effectiveness
FRONT END	Specific to each front end but may include aperture size, mounting restrictions, shielding, A/D efficiency, digital data rate

2.4 LOWER LEVEL TRADE-OFFS

The architecture evaluation documented in the AIASE Final Report concentrated on the interconnects. The draft criteria were considered for the other architectural elements, but it was

ascertained that a detailed assessment is best performed at lower levels. As an example, an ATRJ algorithm developer may specify a worst case interrupt latency to service an RF pulse report. The module developer will assess designs against the interrupt latency requirement. The internal interrupt latency of a module, while very important to executing the algorithm, is not a crucial parameter for the system architect. The system architect relies on the algorithm developer and the module designer for their assessments of these elements. Similarly, enclosure, software, and front-end assessment is best performed by the experts in those areas.

The AIASE survey analysis identified areas that the AIASE architecture definition should address to arrive at common solutions. Among these issues were power, form factor, two-level maintenance support, general purpose processor type, software development systems, operating system services, maintenance controller operation, and interconnects. Early coordination between the AT system architects and the AIASE system designers will mitigate future interoperability and integration problems. In addition, the AIASE study includes an integration process not investigated by the current ATASE programs. General purpose processing requirements were assessed based on the integration process algorithm requirements.

The selection of interconnects was identified as the most important task of the system architect. In any open architecture definition, the first step to facilitating interoperability is to ensure that standard interconnects are used. A system architect can select interconnects that meet the expected functional communication requirements. The requirement to use these standard interconnects are then levied on the module designers. The benefit of this is threefold.

1. The system integration will be easier because all modules have been designed to use standard interconnects.

2. The module supplier is allowed freedom in the internal module design to apply their particular expertise. Specifying down to the lower levels tends to take the system engineer out of his area of expertise and waste the suppliers' expertise.

3. The life cycle costs are reduced because all module interfacing is performed on standard interconnects.

As an example of this process, a system architect specifies appropriate standard interconnects for modules required to interoperate. The EW processing expert builds the optimal processor while communicating off-module via the standard interconnect. This minimizes

integration risk and simplifies module I/O. Open architectures also facilitate easy insertion of state-of-the-art technology. A rigid common module definition, however, tends to shackle the supplier's innovation and eliminates functionality from any competition.