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Ferroelectric **Oxide** Memory FET (FEMFET) Development

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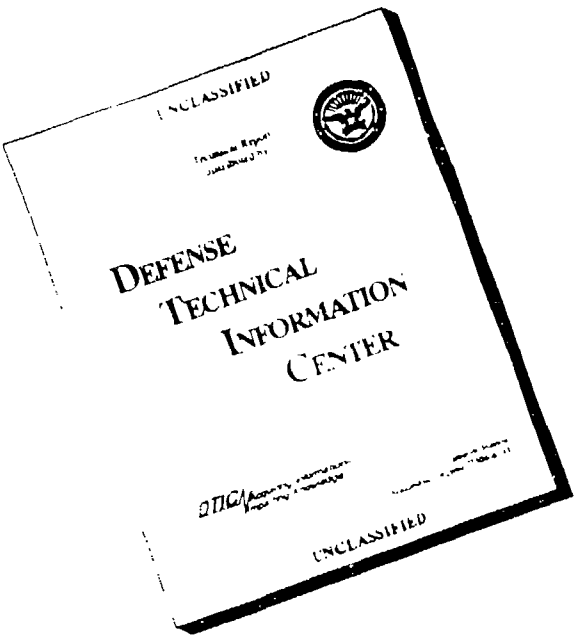

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This Final Technical Report covers the integration of oxide ferroelectric thin films (e.g. bismuth titanate = $Bi_4Ti_3O_{12}$ = BTO or lead zirconate titanate = PZT) into the gate dielectric of a metal-insulator-silicon field effect transistor (MISFET), capable of functioning in a non-volatile, non-destructive readout (NDRO) ferroelectric random access memory (FERRAM). Also provided is a detailed description of the test vehicles implemented for the study of fabrication process integration and optimization and the resultant properties of "ferroelectric/(semiconductor) memory FET (FEMFET) and related structures". The Interim Report covering the first phase of this contract described an investigation of UHV-deposited ferroelectric "fluoride" ($BaMgF_4$ = BMF) films as gate insulators; however, BMF transistor structures exhibited rather poor reproducibility, and electrical instability manifested as poor retention capability. Results of the second phase of this program are presented in this report, which focuses on exploration of oxide ferroelectric films for the FEMFET gate dielectric. There is growing evidence that layers of ferroelectric oxides, when suitably processed may possess switching and stability properties that are far superior to those attainable with BMF layers.

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19. ABSTRACT

Multi-layer MISFET gate-stack test structures, incorporating crystalline oxide ferroelectric films with SiO_2 buffer and cap layers, Si_3N_4 diffusion barriers and TiW or Al gate electrodes, were fabricated using our pulsed laser deposition (PLD) apparatus (scaled under the program to allow coating 4-inch wafers compatible with IC processing) to demonstrate memory storage capability, and to establish the basis for a FEMFET-FERRAM thin-film technology using an oxide ferroelectric material. C-V measurements indicated excellent memory-window characteristics, suggesting that underlying (p-) type silicon could be driven to deep depletion with switched remanent polarization (P_r) values of less than 0.2 $\mu C/cm^2$. Early device wafers were fabricated using these gate structures, and switchable ferroelectic memory transistors were successfully demonstrated. However, transistor memory retention measurements yielded poor retention times similar to those attained with BMF. Destructive readout measurements of ferroelectric remanent polarization vs. time for these gate structures suggested excellent remanent polarization (P_r) memory retention and that the rapid decay of the C-V memory window observed (in transistor gate structures) was due to a progressive build-up of charge caused by ion migration within the ferroelectric layer.

A unique, highly sensitive, non-destructive method of determining charge migration behavior in the ferroelectric layer from CV measurements was developed, which provided a powerful new analytical tool for the characterization of fatigue and aging effects in both FEMFET and (modified) ferroelectric capacitor memory structures. Using this testing method, a factor of approximately 1000 improvement in the retention of BTO gates was demonstrated through the use of Nb doping. Gates fabricated with undoped PZT and Al top electrodes gave extrapolated memory retention exceeding 10 years! As a consequence of this latest work with new materials, compatible buffer-layer and cap-layer incorporation into the memory gate structure, low-stress metallization techniques, and lithography appropriate for delineation of the oxide ferroelectric gate dielectric, we feel that most of the issues associated with a high retention FEMFET demonstration are now essentially under control. However, because of funding and time constraints a transistor device wafer lot employing these improvements was not fabricated.

Despite the fact that high-performance memory device arrays with high yield have not yet been obtained, the intrinsic merits and practical potential of the technology have been successfully demonstrated using ferroelectric oxide thin film materials. As a consequence of results achieved on this program, and of several related studies reported in the literature, exciting opportunities now exist for significant further improvements in the performance and stability of FEMFET-FERRAM transistor arrays.

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1.0 EXECUTIVE SUMMARY

The Westinghouse contract is aimed towards the development of a 4-inch silicon wafer technology for FERRAM/FEMFET (Ferroelectric Memory FET) ,memory arrays. The memory cell structure involves a ferroelectric layer as the gate dielectric of the FET, where the candidate ferroelectric materials identified for evaluation were a fluoride (BaMgF4 = BMF) or oxide (Bi4Ti3O12 = BTO or other). The key aspects of the program address the following: (a) development of Integration Compatible / Accelerated Lifetime (ICAL) test vehicles incorporating prototype FEMFET structures, (b) optimization of integrated fluoride or oxide films as low-coercivity ferroelectrics, (c) demonstration of long-term device stability (i.e. evaluation of retention, fatigue, and aging effects) in optimized transistor structures, and (d) development of large-area manufacturing processes compatible with 4-inch FERRAM/FEMFET technology.

The Interim Report[1] covering the first phase of this contract described an investigation of MBE-grown ferroelectric 'fluoride' (BMF = $BaMgF_4$) films as gate insulators for NDRO ferroelectric memory FET device structures based primarily on (100) oriented silicon, and to some extent on GaAs wafers. Although devices showing large programmable memory windows were obtained, using relatively low address voltages, the BMF transistor structures exhibited rather poor reproducibility, and electrical instability manifested as poor retention capability. The test transistors fabricated exhibited good transistor curves; however, retention time was on the order of one to five hours. Measurements using the Radiant Technology RT-66A ferroelectric test system of the stored ferroelectric remanent polarization were inconclusive (values were too small to measure reliably because films on silicon had the polar axis oriented mostly in-plane instead of the

desired orientation out-of-plane). Further studies, including temperature-bias-stress evaluations, indicated that mobile charges (ionic conductivity) were a significant factor in producing a fast decay of the memory window (i.e. loss of retention). These results were the major reason in deciding to shift the study of ferroelectric FEMFETs from BMF to other 'oxide' ferrolelectric materials such as bismuth titanate (BTO). Additional problems encountered with BMF gate insulator structures included high coercive fields, and film cracking arising from the high differential thermal expansion between BMF and Si. Also, thin BMF layers, when electroded with Al films, exhibited large internal clamping fields (presumed to be of piezoelectric origin) which suppressed polarization switching.

Results of the second phase of the program are presented in this report, which focuses on exploration of ferroelectric bismuth titanate (BTO) films for the FEMFET gate dielectric, since there is growing evidence that layers of BTO and certain other ferroelectric oxides, when suitably processed, may possess switching and stability properties that are far superior to those thus far obtained for BMF layers. This evidence has emerged primarily from our recent effective development of pulsed (excimer) laser deposition (PLD) as a growth method for BTO (as well as several other mixed oxides) that is markedly superior, in control of film composition and structure, to previously used sputtering techniques. However, it is also strongly supported by a re-evaluation of key device and materials parameters (from work at Westinghouse and elsewhere), and by recent findings on the successful chemical doping of ferroelectric oxide films to achieve significant improvements in electrical quality.

An 8K FERRAM Test Vehicle was created for evaluation of FEMFET baseline process integrity. This mask set featured a full complement of test structures for evaluation of the

process integrity of the FEMFET process. These test structures address such issues as performance, reliability, producibility, radiation hardness, and uniformity of the baseline technology. Wafer fabrication on this program phase used short-loop gridded wafers for ferroelectric capacitor fabrication and evaluation and fully processed device wafers for FEMFET fabrication. During this program phase 111 gridded wafers were processed and 15 device wafers were processed up to FEMFET formation using oxide ferroelectric materials.

Under Westinghouse IRAD efforts before the start of the present program, we had demonstrated operation of an integrated oxide-type gate structure with 5V programming using BTO films prepared by pulsed laser deposition (PLD). Optimum deposition parameters for preparing BTO films on small substrates were established prior to the start of the present program. The focus of our oxide-ferroelectric thin film deposition efforts on the present program was on scaling the already established BTO process to allow coating 4-inch silicon wafers to be compatible with our existing 1μm CMOS very large scale integrated circuit (VLSIC) fabrication.

Multi-layer MIS test structures, incorporating crystalline BTO films with SiO_2 buffer and cap layers, Si_3N_4 diffusion barriers and metal (and alloy) gate electrodes, were fabricated using our scaled PLD apparatus to demonstrate memory storage capability, and to establish the basis for a FEMFET-FERRAM thin-film technology using an oxide ferroelectric material. C-V measurements indicated excellent memory-window characteristics, suggesting that p-type silicon electrodes could be driven to deep depletion with switched remanent polarization (P_r) values of less than 0.2 $\mu C/cm^2$.

Early device wafers were fabricated using these gate structures, and switchable ferroelectric memory transistors

were successfully demonstrated. However, transistor memory retention measurements yielded poor retehtion times similar to those attained with BMF. Measurements of ferroelectric remanent polarization vs. time of gate structures suggested excellent memory retention and that the rapid decay of the C-V memory window observed (in both gates and transistors using BTO layers) was due to a progressive build-up of fixed positive charge caused by ion migration (within the BTO layer) to the semiconductor interface.

In order to eliminate the possible effects of measurement fields on the stability of the stored C-V window condition, a unique indirect, non-destructive electrical measurement approach has been developed at Westinghouse, whereby the memory window threshold voltages were imputed from zero-bias values of the gate capacitance C_g, using SONOS C-V reference plots. This highly sensitive, non-destructive method of determining charge migration behaviour in the ferroelectric layer provides a powerful new analytical tool for the characterization of fatigue and aging effects in both FEMFET and (modified) ferroelectric capacitor memory structures.

Significant improvements in C-V window retention have been demonstrated on this program with new ferroelectric oxide-type memory gate stack structures (having buffer- and cap-layers and metal top electrodes of Ti-W or Al) and new ferroelectric oxide materials (e.g. doped BTO and PZT). In particular, a factor of approximately 1000 improvement in the retention of BTO gates was demonstrated through the use of Nb doping; and, gates fabricated with undoped PZT and Al top electrodes gave extrapolated memory retention exceeding 10 years! As a consequence of this latest work with new materials, compatible buffer- and cap-layer incorporation in the memory gate structure, low-stress metallization techniques, and lithography appropriate for deliniation of the oxide ferroelectric gate dielectric, we feel that most of

the issues associated with a high retention FEMFET demonstration are now essentially under control. However, because of funding and time constraints a transistor device wafer lot employing these improvements was not fabricated.

Despite the fact that high-performance memory device arrays with high yield have not yet been obtained, the intrinsic merits and practical potential of the technology have been successfully demonstrated using ferroelectric oxide thin film materials. As a consequence of results achieved on this program, and of several related studies reported in the literature, exciting opportunities now exist for significant further improvements in the performance and stability of FEMFET-FERRAM transistor arrays.

2.0 INTRODUCTION

Nonvolatile memory is an essential requirement for all computer systems. It is especially important for military systems where vital information has to be stored in some type of a nonvolatile memory (i.e. memory that does not forget when power is lost in a hostile environment). Among the available nonvolatile memory technologies, disk memories offer large capacities, and are widely used in such items as personal computers. However, they are slow, bulky, and susceptible to breakdown because of their mechanical nature. Magnetic core and magnetoinductive plated wire memories are very limited in capacity, very bulky, have large power requirements, and are very expensive. Erasable programmable read-only memories (EPROM) and electrically erasable programmable read-only memory (EEPROM) have slower write speeds, are susceptible to radiation damage, and fatigue faster than either core or silicon random access memories. Silicon oxide-nitride-oxide silicon (SONOS) memory is a nonvolatile memory option that is fast to read and can be radiation (RAD) hard. Unfortunately however, SONOS is yet to be programmed for long retention (over five years) with programming pulses of 1μs or shorter. Another memory option currently under development is the magnetoresistive random access memory (MRAM), which has the potential to provide high density, radiation hardness, and nondestructive readout (NDRO) operation with unlimited endurance. Major disadvantages of this device are its slower read cycle time and larger cell design.

Key characteristics of some of the military nonvolatile memory technologies as they existed near the middle of 1991 are listed[2] in Table 1-1. When one considers all the selection requirements for a nonvolatile memory, namely fast read/write, radiation hardness, cost effectiveness via compatibility with currently used integrated circuit (IC)

Table 1-1: MILITARY NONVOLATILE MEMORY TECHNOLOGIES †

	FLOATING GATE EEPROM	FLASH EEPROM	SNOS (SHADOWnvRAM)	SONOS EEPROM	DRO FERRAM	NDRO FERRAM	MRAM	CORE	PHOENIX™ (SRAM&EEPROM)	SRAM with Hypercap™
STATUS	1 Mbit Production	1 Mbit Production	Samples Available Prod. by '92, 8K x 8	Limited Production in '92 8K x 8'	Limited Commercial Production 512 x 8	Development 1K x 8 in '92	Limited Production by 1992 16K x 1	Mature Tech. 64K/128K Word Modules	Mature Tech. 128K/256K Word Modules	Hypercap in Dev.
SPEED (ACCESS TIME)	150 nsec	120 nsec	35 nsec	150 nsec	100 nsec	200 nsec	Density Dependent 200 nsec - 2 μsec	350 nsec	50 nsec	SRAM Dependent: 50 nsec Typical
WRITE TIME	10 msec Byte/Page	High	SRAM write: 35 nsec; Download: 11 msec	10 msec Byte	100 - 200 nsec	100 - 200 nsec	100 - 250 nsec	900 nsec	50 nsec	SRAM Dependent: 50 nsec Typical
ENDURANCE	10^4 - 10^5 Write Cycles	10^6 Write Cycles	10^5 Power Cycles	10^6 Write Cycles	10^{10} Read/Write	10^{10} Write Cycles	No known Limitations	No Limits	10^5 Power Cycles	No Limits
RADIATION HARDNESS	Low-Moderate	Low-Moderate	Moderate (Potential)	High (Potential)	High (Potential)	High (Potential)	High (Potential)	Moderate to high	SRAM Dependent	SRAM Dependent
GROWTH POTENTIAL	Moderate	High	Moderate	Moderate	High	High	Moderate	Limited	Low to Moderate	Moderate to High
LIMITATIONS	Write Speed Endurance	Write Speed Endurance	Density	Write Speed	Endurance DRO	(none)	Read Speed, Density	Speed, Density Power	Density	SRAM Standby Current
COST	Moderate	Low	Moderate to High	Moderate	Potentially Low	Potentially Low to Moderate	Potentially Moderate	High	Moderate	Low
SOURCING	Xicor Atmel Seeq	Intel Atmel AMD	Simtek	Westinghouse (with SNL)	Rasetron (SHADOWnvRAM) / Raytheon	Westinghouse (with SNL)	Honeywell NVE	Quadri Ampex SCI	Quadri	Quadri

†Modified version of table in Reference 2.

processing technology, high endurance and retention, and nondestructive readout (NDRO) capability, the ferroelectric memory stands out as the logical choice for all applications where submicrosecond programming is needed.

The basic characteristics of a ferroelectric material that make it suitable for memory device application include primarily its ability to retain two stable remanent polarization ($\pm P_r$) values at zero field, thus providing nonvolatility. The second basic aspect relates to the control and sensing of the remanent polarization state, including a means for polarization reversal from up (+ 1) to down (0) or vice versa. For compatibility with standard silicon complementary metal-oxide semiconductor (CMOS) ICs, the ferroelectric memory element must switch at an applied voltage of less than 5V. The first ferroelectric memory transistors were fabricated in the 1950's and 1960's; however, all of these early devices used bulk ferroelectric material with a thin film of semiconductor on top, thus requiring higher than acceptable switching voltages. The first thin film ferroelectric memory device was fabricated by S.Y. Wu[3] at Westinghouse in 1974. The structure of this device, called metal-ferroelectric-semiconductor transistor (MFST) by Wu was identical to the standard silicon metal-insulator-semiconductor field effect transistor (MISFET), except that the insulator in the MISFET was replaced by a thin (3 to 4 μm) layer of sputter-deposited ferroelectric bismuth titanate. Although the device was stable and functional, it required a very large switching voltage, thus making it incompatible with silicon ICs. In addition, it was slow (switching time of the order of microseconds). The slow speed was attributed by Sugibuchi et al[4] to tunnel-injection effects, i.e., charge injected from the silicon surface into traps in the ferroelectric film through a thin native SiO_2 barrier layer. This resulted in injection-type on/off switching (similar to SONOS) dominating over the desired

polarization-type switching. Sugibuchi eliminated injection and demonstrated ferroelectric memory operation by using a thick (500A) barrier layer which required high voltage to operate. Recently, Buhay et al[5] demonstrated operation at low voltage using a thin barrier layer. In this work bismuth titanate films were fabricated by the pulsed laser deposition (PLD), which provides a much better control of stoichiometry compared to sputter deposition used in earlier Westinghouse work. This latest thin film development work with bismuth titanate was performed under Westinghouse IR&D funding prior to the start of this second phase of the contract, and provided the motivation to pursue further development of our ferroelectric memory using ferroelectric oxide materials.

3.0 TECHNICAL EFFORT

3.1 Ferroelectric Memory Integration Schemes

Two basic types of integration schemes are being pursued by the ferroelectric memory community at this time: (1) destructive readout (DRO) where the information must be rewritten after every read operation, and, (2) nondestructive readout (NDRO) where the information can be read over and over again until the next write operation. Integrated ferroelectric random access memory (FERRAM) using the DRO scheme closely resembles dynamic random access memory (DRAM).

The description and background of the various DRO FERRAMs are available from many other sources and will not be covered here. The recent surge in interest in ferroelectric nonvolatile memories can be traced to the development of thin film technologies in the 1970's and 1980's allowing the fabrication of thin film ferroelectric capacitors at temperatures compatible with semiconductor processing, and the successful integration of these capacitors into demonstration DRO FERRAM chips by Ramtron and Krysalis in the mid 1980's. A good description of these developments can be found in the review article by Scott and Araujo[6] .

The NDRO scheme makes use of a ferroelectric memory FET (FEMFET), in much the same manner as the "floating gate memory transistor" or the "SONOS" memory transistor, which is widely used in many large, commercial, fast-read EEPROMs or in RAD-hard nonvolatile RAMs, to provide nondestructive readout, in addition to fast read. Also of great importance in this device is the fast write characteristic, which derives from the use of special high quality ferroelectric films within the gate stack of the FEMFET. Switching of the polarization state of the ferroelectric gate structure caused by a "write" pulse results in a "permanent" modulation of the

FET's channel conductivity to a "one" or "zero" condition. The cross section of the FEMFET, shown in Figure 3-1 is achieved using an "add-on" process module engineered to be compatible with existing 1μm CMOS very large scale integrated circuit (VLSIC) fabrication. Before an 'oxide' ferroelectric gate stack is grown, specific preparatory steps are used to insure the absence of a "tunneling-trapping barrier" layer of the type observed by Wu[2] at the interface between the semiconductor and the 'oxide' ferroelectric. The gate structure is also "capped" with a thin layer of SiO_2 to achieve a more robust MISFET gate dielectric capable of handling larger electric fields. Additionally, the capping layer provides better memory gate adhesion and facilities memory-gate stack photoengraving.

The advantages of the FEMFET are inherent amplification built into the device, unlimited read cycles (the device fatigues only during reprogramming and not during routine reading), and potentially very high packing density associated with the two devices per cell format. Thin films of ferroelectric barium magnesium fluoride (BMF) and bismuth titanate BTO) are being used in the FEMFET development program at Westinghouse.

3.2 'OXIDE' FEMFETs / Background and History

The basic charge-storage mechanisms of FEMFET devices have been discussed, for example, in papers by Wu[3] , Sugibuchi et al.[4] , and more recently by Sinharoy et al.[7] Various mechanisms can operate to provide a sheet of (space) charge in the vicinity of a semiconductor-insulator interface. The occurrence and field-induced migration of contaminant alkali ions in SiO_2 layers is a well-known example[8]. Another example, which has been studied and exploited extensively in oxide-nitride (SONOS) memory structures, is the tunneling of injected charge into traps - primarily at the interface between two dielectric layers. Figure 3-2 shows the shift in

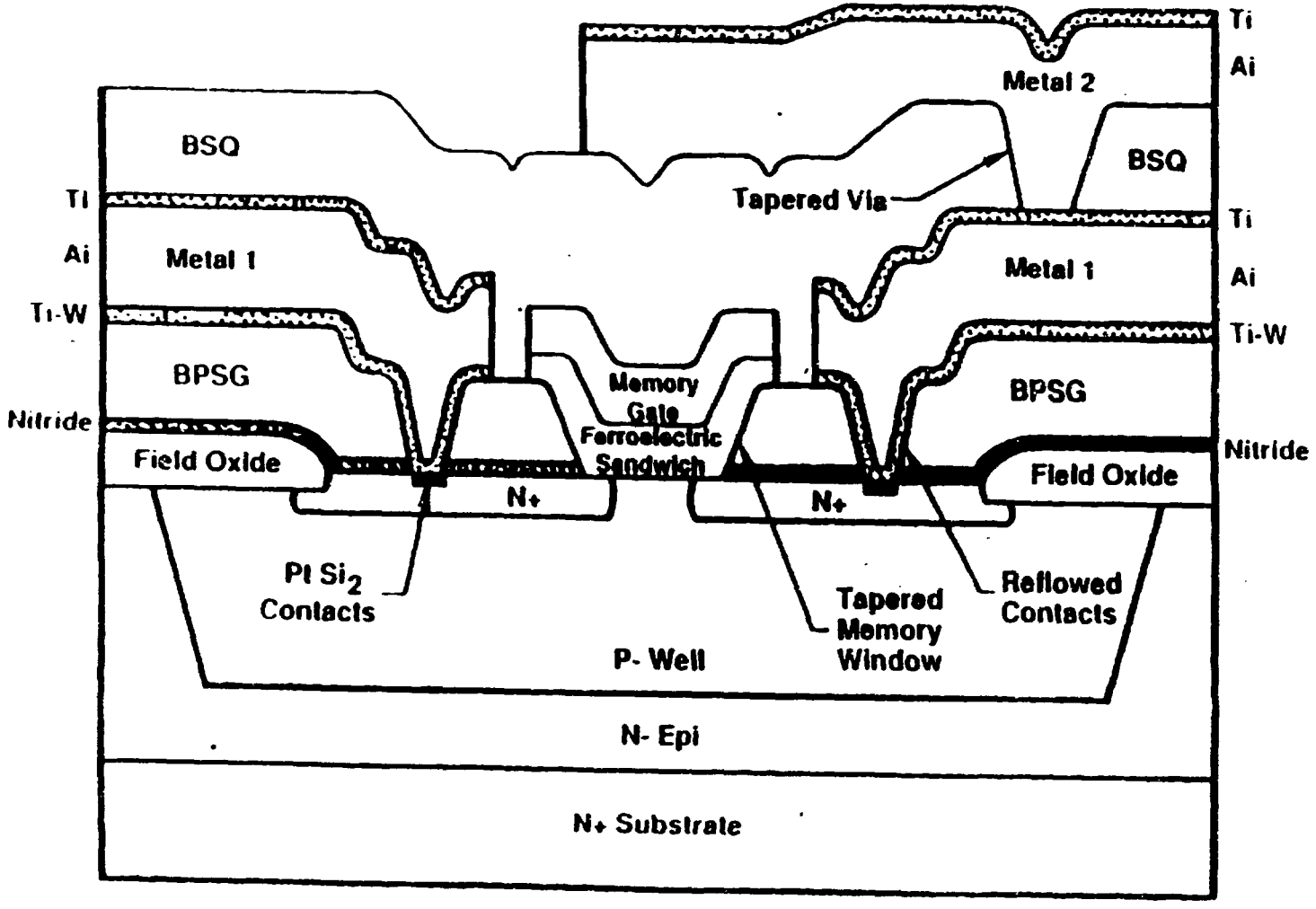

Figure 3-1: Westinghouse One-Micron CMOS FEMFET Cross-Section.

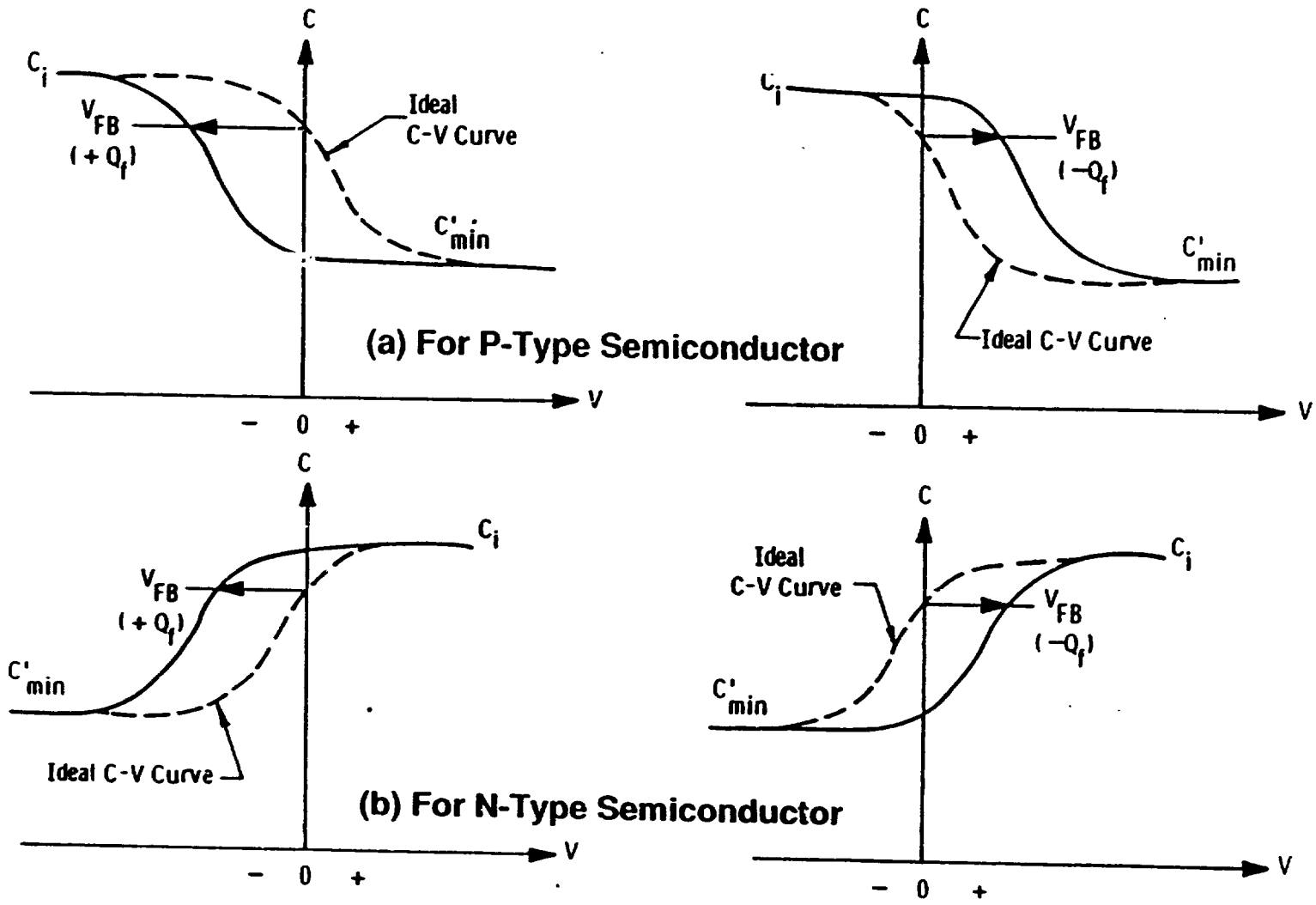

Figure 3-2: CV Curve Shift Along the Voltage Axis Due to Positive or Negative Fixed Oxide Charge.[7]: (a) For P-type Semiconductor, (b) For N-type Semiconductor.

voltage of a high-frequency C-V curve when positive or negative charge, Q_f, is present at the interface, measured relative to an ideal C-V curve where $Q_f = 0$. A positive Q_f causes the C-V curve to shift towards more negative gate (metal electrode) bias values for both *n*- and *p*-type semiconductors, and conversely for a negative Q_f. Next, the charge Q_f can be identified with the effective reversible surface charge of a polarized thin film of ferroelectric material, and in fact Figure 3-3 suggests[9] the programming method for a ferroelectric memory FET (FEMFET). As illustrated in Figure 3-3, when the gate is positive, the reversible ferroelectric spontaneous polarization (P_S) switches orientation so that the negative electric dipole charges are adjacent to the positive gate, forcing the positive electric dipole charges to be at the silicon interface, and conversely. The shift in the flatband voltage indicated in Figure 3-2 can be related to the change in the insulator space charge (or the effective change in P_S near the semiconductor interface) by an expression[7] of the form

$$\Delta Q_f = -C_i \Delta V_{FB} \qquad (3\text{-}1)$$

The first successful achievement of a FEMFET device employing a ferroelectric film as the gate dielectric was obtained by Wu[3] at Westinghouse. Using metal-ferroelectric-semiconductor-transistor (MFST) structures comprising 2 - 4 μm thick BTO gate dielectric layers sputtered on silicon, he was able to demonstrate reversible changes in channel conductance by changing the voltage on the gate. In these devices, however, the simple switching mechanisms depicted in Figures 3-2 and 3-3 were not observed. Under gate voltages high enough to produce memory storage, carriers were injected into the ferrroelectric from the silicon, and these charges led to the attraction of carriers of opposite polarity to the semiconductor surface. It seems probable that these effects arose from the formation of a thin mixed oxide

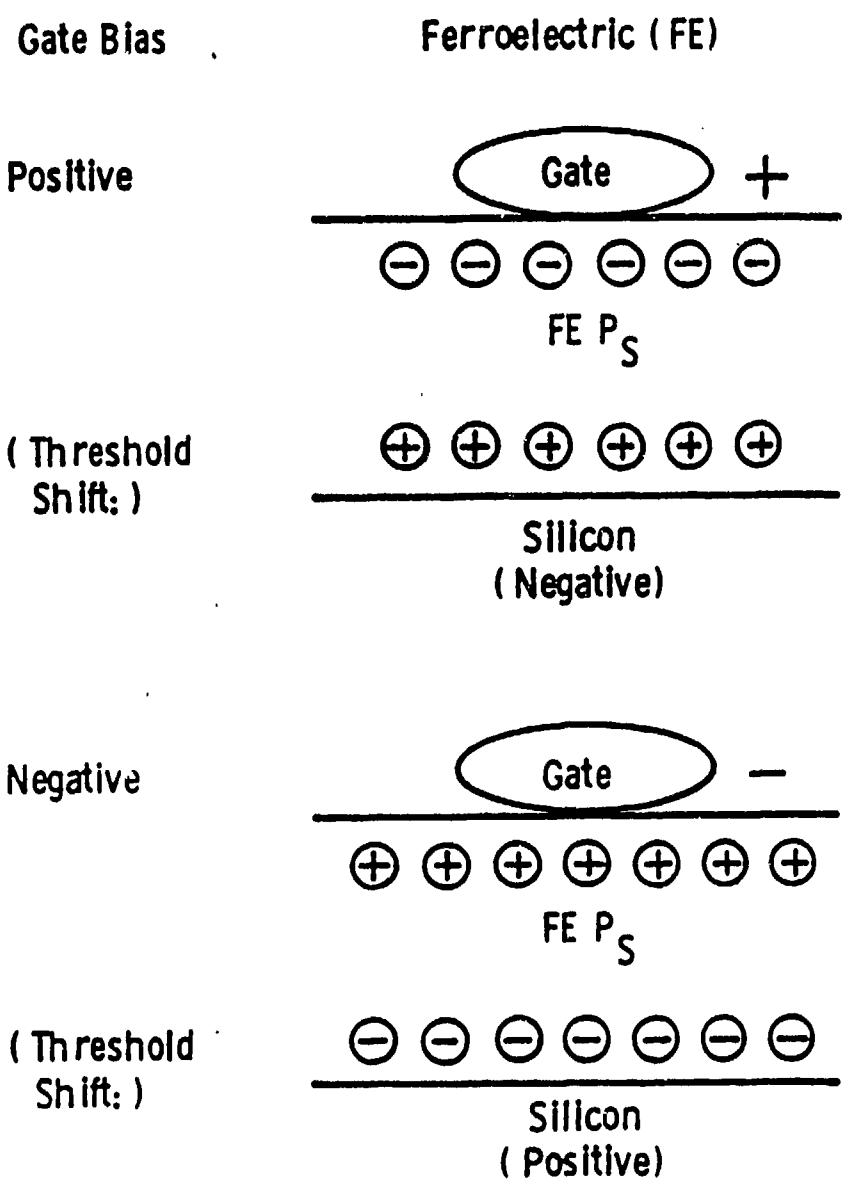

Figure 3-3: Ferroelectric Memory FET Programming[7].

layer at the interface, because of the oxidizing environment during BTO deposition and the necessity for extended sputter deposition times at elevated temperature.

In subsequent work by Sugibuchi et al.[4], the titanate layer was formed by annealing (at 650°C) amorphous films deposited on unheated Si substrates. This procedure reduced stress and cracking prevously induced in the films by differential thermal contraction. The results obtained indicated that charge injection could be avoided by operating at gate voltage frequencies higher than 1 kHz, or by adopting a structure in which a thin (500A) thermal oxide buffer layer was interposed between the titanate and the silicon. In these situations, modulation of the silicon surface potential occurred only through polarization reversal in the ferroelectric film. The switching time for a 0.7 μm thick BTO film was found to be exponentially dependent on the applied voltage, typically 10 msec at 25 V and 300 msec at 15 V. Considering the early state of development and the primitive passivation approaches used in these studies, the retention characteristics of these *p*-channel devices were rather promising. The "on" and "off" states were relatively stable even at 100°C and no fatigue effects were observed up to 10^5 write and erase cycles.

Few published studies have yet appeared on FEMFET device structures with other ferroelectric oxides as the gate insulator. An early attempt was made by Higuma et al.[10] to develop FEMFET structures on *n*-type GaAs substrates (N_D = 2-9 x $10^{17}/cm^3$), using RF sputtered lead lanthanum titanate (PLT) films as the gate dielectric. The films were grown at temperatures below 500°C and subsequently annealed at temperatures up to 750°C to develop the crystalline perovskite-type ferroelectric structure. This yielded ferroelectric hysteresis loops with typical values of P_r = 7.7 $\mu C/cm^2$ and E_c = 120 kV/cm. Transistor structures were

fabricated , using Zn diffusion to produce the *p*-type source and drain regions. Well-defined "on" and "off" states were observed, but with operating power levels about an order of magnitude lower than those reported by Wu[3] and Sugibuchi[4] for structures on Si with BTO gates. However, the I_D vs. V_G characteristics for these PLT devices on GaAs indicated clearly defined switching thresholds consistent with the normal ferroelectric polarization reversal mechanism (i.e. no evidence of charge injection into the ferroelectric).

More recently, Rost et al.[11] produced FEMFET structures by RF magnetron sputtering of ferroelectric $LiNbO_3$ films on (111) silicon substrates. The potential advantages of $LiNbO_3$ gate structures, on this orientation of Si, derive from the ease with which the polar *c*-axis can be grown normal to the substrate, the low chemical reactivity of the niobate, and the extremely high value of P_S (71 $\mu C/cm^2$) reported for this material. A novel molybdenum lift-off process was used to delineate the 25 μm square FET structures. Using niobate films 2700A thick, grown at 600°C, low leakage values (34 pA) were obtained and an amplification factor of 64 was reported. Also, in operation hysteresis of parameters of the device were altered in a way which was consistent with ferroelectric switching being the dominant effect. Below we describe results achieved under the present program using BTO and other oxide ferroelectric materials in the development of oxide-type FEMFETs.

3.3 Critical Parameters for Optimum FEMFET Performance

From the above discussion it is clear that the primary mechanism for channel conductance modulation during FEMFET operation (i.e. the desired polarization reversal in the ferroelectric layer, or undesired charge injection into the ferroelectric) depends sensitively upon the compositional profile in the vicinity of the semiconductor-dielectric

interface. We shall discuss this more fully later in relation to thin film deposition and annealing conditions for the gate dielectric, and the interposition of buffer-barrier and capping layers for reduction of injection and leakage. Next, we consider the dependence of the polarization switching process and memory retention characteristics on the intrinsic electrical parameters of the metal-dielectric-semiconductor structure.

3.3.1 Ferroelectric Film Quality

First, consider the ferroelectric polarization process and its dependence on film quality. This process, and the threshold switching fields and polarization values involved, are sensitive to ferroelectric film composition, crystallinity, orientation and stress condition (as described in later discussion). In particular, earlier studies by Luke[12,13] on crystals of BTO, showed that switching- and coercive-fields (E_S and E_C) and also switching speed were extremely sensitive to chemical purity. Optical evaluation of depoling effects showed that in crystals grown from high-purity oxides, nucleation and propagation of reverse domains occurred from a few fixed sites near the electrode interface. BTO crystals grown from reagent grade (RG) materials of lower purity, however, display reverse nucleation from many sites throughout the crystal, and also require an order of magnitude higher field to attain the same switching speed as high purity crystals. The key role of impurities such as Fe_2O_3 in influencing E_C and switching speed was demonstrated by Luke[12] . Also, a strong anisotropy in conductivity (at least two orders of magnitude between the *a*- and *c*-axes of the crystal) was noted in RG material.

In general, the switching and coercive fields measured in thin film ferroelectrics range from one to two orders of magnitude higher than those found for crystals of the

equivalent bulk materials. The higher fields required in films have been a source of concern in relation to power requirements for memory operation, but can be offset to a large extent by using lower film thicknesses. A high E_c parameter (coupled if possible with the pseudo-threshold *c*-axis switching characteristic of BTO) is attractive for another reason, viz. it tends to neutralize the effect of depolarizing fields inherent in the metal-ferroelectric-semiconductor geometry, as discussed below.

3.3.2 Interrelation of Device Operating Fields and Dielectric Parameters

Consider briefly the key operating (and intrinsic) field conditions required for FEMFET devices, and their dependence on the electrical properties of the ferroelectric layer and semiconductor substrate. We begin by defining the threshold field E_{th} required to change the surface potential of the semiconductor from flat band to strong inversion, and hence the condition of the channel conductance from "0" to "1". Following the recent discussion by Petrovsky et al.[14] this can be expressed as

$$E_{th} = [4kTN \ln(N/n_i)/(\varepsilon_0 \varepsilon_s)]^{1/2} \qquad (3\text{-}2)$$

where k is the Boltzmann constant and N, n_i , ε_s are concentration, intrinsic concentration and dielectric constant respectively of silicon. Also, modifying equation (3-1), for the field strength caused by spontaneous polarization to be sufficient for effective modulation of the semiconductor surface potential, one has

$$P_s/(\varepsilon_0 \varepsilon_s) > E_{th}. \qquad (3\text{-}3)$$

The P_s term in this expression also corresponds to the saturated value of polarization achieved at the switching

voltage. After switching, the polarization condition relaxes to the remanent value P_r, which when inserted in equation (3-3)defines a "holding field" for retention of the stored "1".

Returning to the treatment by Petrovsky et al.[14] , one can also express a relation for the values of the characteristic fields in the FEMFET device, as follows

$$P_s/(\varepsilon_0\ \varepsilon_i) < E_C < E_A < E_B\ , \qquad 3\text{-}4)$$

where E_C is the coercive force, E_A is the field in the ferroelectric created by the applied voltage, and E_B is the breakdown voltage. The expression $P_s/(\varepsilon_0\ \varepsilon_i)$ has been suggested as a figure of merit for FEMFET type devices. This expression appears to be more appropriate than the ratio $P_s/(\varepsilon_0\ \varepsilon_i\ E_C)$ proposed by Scott et al.[6] for capacitor memories, which characterizes the ratio of non-linear switching response to linear non-switching response.

Petrovsky et al.[14] have used relations (3-2), (3-3) and (3-4) to derive the representation shown in Figure 3-4, which shows limits of the permissible area of FEMFET operation, assuming different values of permittivity for the ferroelectric film. The area shown is for $E_B = 5.10^6$ V/cm, $E_A = 10^6$ V/cm, $E_C = 5.10^5$ V/cm, E_s (E_{th}) $= 4.10^3$ V/cm ($N = 10^{14}$ cm^{-3}), for the range $P_s/(\varepsilon_0\ \varepsilon_i) = 4.10^3 - 5.10^5$ V/cm.

3.3.3 Origin and Role of Depolarizing Fields

It has been pointed out[15,16] that the metal-ferroelectric-semiconductor (MFS) configuration, despite its advantages for low-power NDRO operation, is extremely susceptible to instabilities due to high built-in depolarizing fields. This situation has been studied theoretically and experimentally, especially with reference to ferroelectric TGS layers on silicon substrates. In the conventional metal electroded

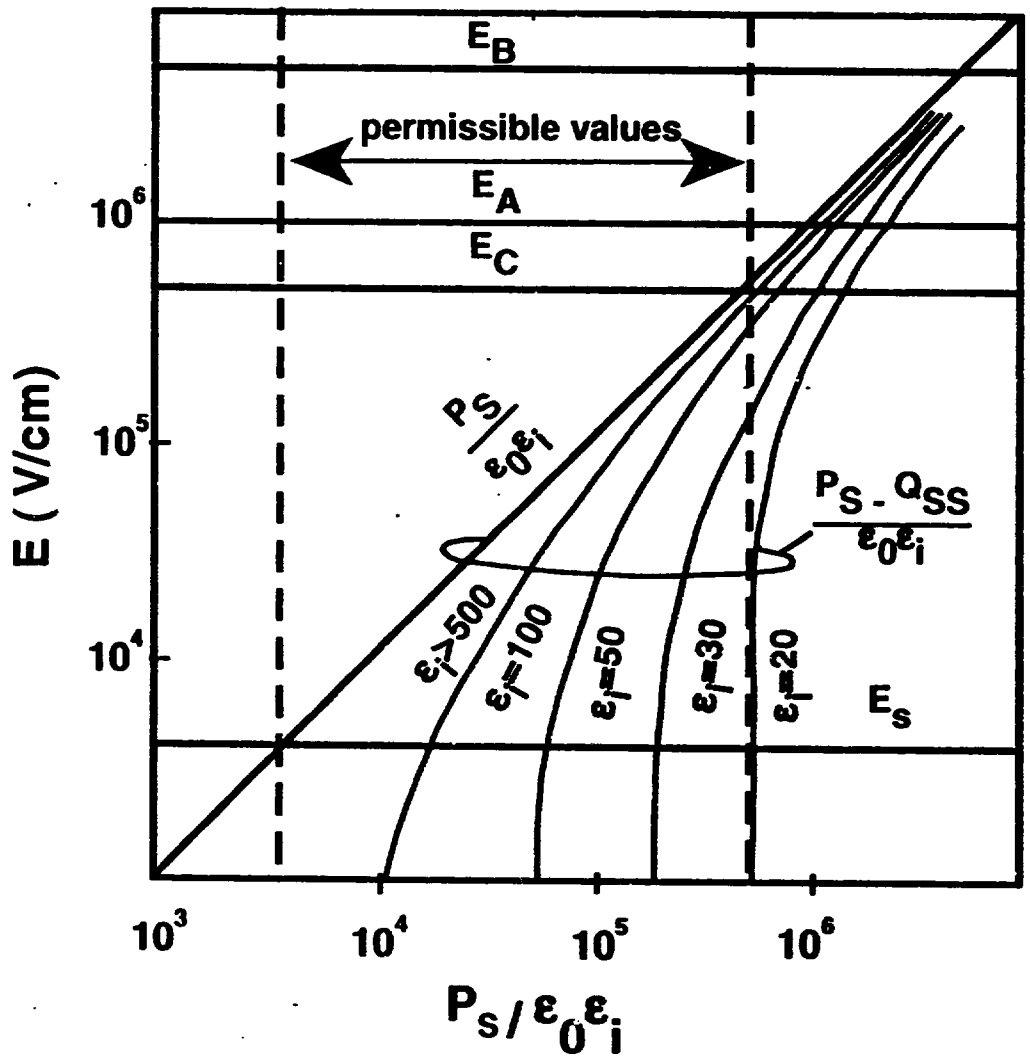

Figure 3-4: Representation of Requirements for Metal-Ferroelectric-Semiconductor Memory[14].

ferroelectric capacitor geometry, the reverse depolarizing field which tends to reduce the polarization, is largely compensated by charges in the electrodes. However, when one of the electrodes is a rather lightly-doped semiconductor (as is the case with FEMFET devices) band bending qV_b (see Figure 3-5) near the surface gives rise to a depolarization field in the ferroelectric, which under short-circuit conditions is given by the band bending divided by the thickness of the ferroelectric. For majority-carrier depletion, V_b is related to the total charge σ_s in the space charge region and can be shown to be given by

$$V_b = 2\pi(\sigma_s)^2/\varepsilon\, q\, N_A \,, \qquad (3\text{-}5)$$

where $\varepsilon = 6$ is the dielectric constant for silicon, q is the magnitude of the electronic charge, and N_A is the acceptor density in the Si electrode. Using photo-illumination to vary the compensation-charge extension in the silicon electrode, Wurfel and Batra[16] were able to confirm modeling predictions that the depolarization fields can reduce the intrinsic polarization, and for sufficiently thin films lead to polarization instability. Also, calculations by Batra and Silverman[17] for TGS-based structures would suggest that the values of depolarizing field can range from about 10^4 V/cm for carrier concentrations of 10^{17} /cm^3 to 10^7 V/cm or higher for uncompensated conditions arising from doping levels around 10^{15} /cm^3. The latter field values are in excess of the dielectric breakdown strength for most ferroelectric materials.

It is clear that the situation just described does not apply to gate voltages which lead to majority carrier accumulation at the semiconductor surface, or in other words to an "off" or "0" memory state. For this condition, as shown by Sugibuchi et al.[4] , the value of the depolarizing field is well below the activation field needed for film switching.

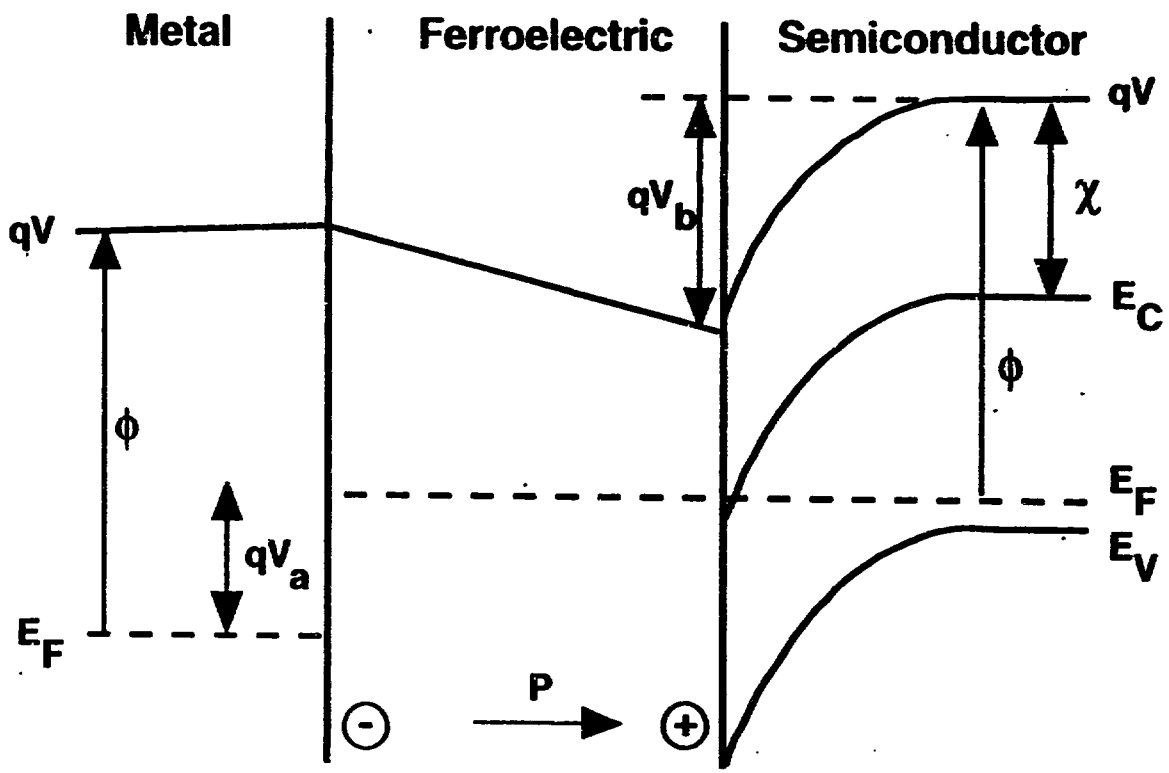

Figure 3-5: Distribution of the Potential V in a Ferroelectric Thin Film Sandwiched Between a Metal and Semiconducting Electrode of Equal Work Functions (Φ) for an Applied Bias V_a. The Valence and Conduction Band Energies E_v and E_c Undergo a Band Bending eV_b, and V is Drawn Parallel to the Bands but Displaced From Them by the Electron Affinity (χ). E_F is the Fermi Level[16].

Also, under low-frequency test conditions or under photo-illumination, where thermal generation of minority carriers or photo-generation of carriers, can enhance the total surface charge density in the silicon, the depolarizing field is effectively compensated. A simplistic application of the above arguments to our experimental structures, comprising a ferroelectric BTO film sandwiched between an aluminum gate electrode and a lightly-doped silicon substrate, leads to some additional operating limits with reference to those indicated in Figure 3-4. Thus, the depolarizing field in the ferroelectric, E_f , must lie significantly below the E_C limit (in Figure 3-4) in order for the remanent polarization and stored information to be stable. The fact that E_C values for thin films of BTO tend to be uniformly higher than those for bulk crystals by two to three orders of magnitude helps this situation, but also increases gate operating voltages and power requirements.

In the present studies (see section 3.6.4, we have seen instabilities (loss of retention) in charge stored in metal-ferroelectric-semiconductor test structures based on both BMF and BTO layers; however, these effects have usually been observed as shifts of threshold voltage in CV plots and not as loss of remanent polarization (P_r) in the ferroelectric films. For this reason, we feel that the actual depolarizing fields present in our structures must be significantly smaller than those estimated in the studies of Batra et al.[16,17] on TGS based structures. Before discussing the experimental data (see section 3.6.4) obtained in this phase of the program, we briefly consider some possible reasons for the apparent low values of depolarization field, E_f, in our test devices.

3.3.4 Some Aspects of Practical FEMFET Structures

The practical FEMFET designs and test structures that have

emerged during this program now contain features (or operating conditions) that may invalidate models such as those developed by Batra et al.[17] to explain depolarizing effects in TGS-based MFS structures. These features are described in greater detail below, where the properties and electrical optimization of multi-layer devices are considered. Suffice to say at this point, that in practice we are dealing not with a simple ferroelectric sandwich structure, but with a three- or four-layer structure of the type metal-electrode/cap- layer/ferroelectric/(diffusion-barrier)/buffer- layer/silicon. Each of these layers plays a key role in successful device operation. Thus, the buffer layer (SiO_2) suppresses tunnel-injection of carriers from the silicon, which would otherwise allow slower SONOS-type operation to dominate. The diffusion barrier (e.g. Si_3N_4) blocks migration of mobile species associated with electrical instability. The ferroelectric layer stores polarization which modulates the surface potential of the silicon, and the cap layer (SiO_2) blocks intergranular leakage under electrical bias from the gate. While the detailed consequences of such multi-layer configurations are discussed later, we now consider briefly the general effects to be expected, particularly with reference to depolarization and stability of stored charge.

First, extending on the points raised above, the significance of depolarizing effects in a simple metal/ferroelectric/semiconductor structure will clearly depend upon the mode and speed of operation. For applied field polarity leading to the depletion condition illustrated in Figure 3-5, at frequencies higher than 10 Hz, positive values of polarization are completely unstable due to the high depolarizing field. To obtain symmetrical, and completely saturated loops under dark conditions, frequencies of about 0.1 Hz must be employed, to allow time for thermal generation to build up charge near the surface of the

silicon. Translating this to FEMFET operation, an undesirable long write-pulse of several seconds duration would have to be sustained in order to invert the channel region to a level necessary to compensate the depolarizing field.

Next, consider why depolarizing effects appear not to be significant in our BTO (and BMF) multi-layer structures? We believe that this may be attributable to differences in the ferroelectric film microstructure (cf. the TGS structures Wurfel et al.[16]) and to the presence of several additional interfaces in our devices. The TGS films produced by melt- or solution-growth methods, contain large-area continuous single-crystal regions, with very pronounced shape anisotropy. Long-range cooperative interaction of the dipoles in such structures (which conform more closely to the idealized film model) might be expected to generate and sustain depolarizing fields approximating the theoretical value ($4\pi P_s$). In our BMF and BTO films, we are dealing with roughly equi-axed granular structures, with the individual grains approaching 1 micron in size. Due to the large thermal expansion mismatch relative to silicon, the grains are frequently separated by cracks or fissures. Thus, we have a loosely-coupled granular array, with only weak long-range interaction (and no domain coupling) occurring during polarization switching. The depolarizing field for each individual grain is of course very small, and may be completely overwhelmed by other internal field effects such as stress-induced (or piezo-electric) fields.

Even if strong ferroelectric coupling were possible in these granular film structures, the interfaces present in multi-layer structures of the type considered here might be expected (as discussed by Lines and Glass[18]) to lead to space-charge accumulation at boundaries with the ferroelectric layer, and thus to compensation of the depolarizing field. The specific roles of component layers, for example, in

enhancing breakdown strength, reducing tunnel injection and modifying the field in the ferroelectric, are considered in Section 3.2 above.

3.3.5 Stability Effects, Mobile Ions, Etc.

As mentioned above, our results on both BMF-based (see Interim Report[1]) BTO-based (see section 3.6.4) FEMFET structures thus far have indicated that, while retention of remanent polarization P_r is in many cases adequate, the width of the C-V memory window shrinks with time, leading to poor retention. The mobile-charge drift mechanisms which appear to be causing these degradation effects[19] are not yet properly understood. Large shifts in flat-band voltage produced by drift of alkali ions to the oxide-silicon interface, were observed early in the development and passivation (with thermal SiO_2) of silicon devices[7] , and were eliminated by resorting to high-purity fabrication practices. However, relatively little is known about mobile ion effects in multi-layer dielectric structures in which the component films are processed primarily by vapor deposition approaches.

The results presented in this report (see section 3.6.4) show that striking improvements in (C-V window) retention are achieved by substituting more refractory ions in the ferroelectric oxide crystal structure. Exploration of such "doping" effects for ferroelectric memory films was prompted by earlier studies on ceramic ferroelectrics by Jaffe et al.[20] which showed that addition of Nb to perovskite-type lead-based ceramics resulted in a marked reduction in conductivity. More recently, the basis for such doping , using e.g. La^{3+} to substitute for divalent A-site cations and Nb^{5+} to substitute for tetravalent B-site cations in perovskite ferroelectrics, has been analyzed by Smyth[21] . Several workers[22,23] have successfully applied the approach to PZT ferroelectric films used for capacitor-type memories, and

were able to demonstrate significant reduction in fatigue. Substitution with higher-valence dopants seems in particular to lower the occurrence of positively charged mobile oxygen vacancies, which can readily develop in thin films at elevated thin film deposition temperatures due to chemical reduction and loss of volatile oxide constituents.

If mobile positive charges are in fact present in the as-deposited ferroelectric BTO layers fabricated in our FEMFET device structures, the work by Smyth[21] suggests that they could readily migrate under the action of the internal fields (10^4 -10^5 V/cm) that probably exist during memory storage. In our case, this could lead to progressive build-up of trapped fixed positive charge at the ferroelectric/buffer interface, which is expected to cause the observed (see section 3.6.4) asymmetric shrinkage of the C-V memory window. The internal fields arise from Pr dipole alignment (cf. Figure 3-18) but may also be attributable to depolarizing fields and/or to piezo-electrically induced effects. In particular, we have found that residual stress in aluminum gate electrode films on BMF layers[1] can be high enough to completely suppress formation of a C-V memory window.

Although our experimental observations in this report suggest that loss of retained memory is primarily due to field-induced charge migration within the ferroelectric layer, instabilities caused by other components in the multi-layer FEMFET structure cannot entirely be ruled out. For example, we have observed that both the methods of fabricating buffer-, capping- and barrier-layers, and the choice of materials for these layers, can have a significant influence on switching and memory storage properties. As a case in point the dielectric leakage and breakdown behavior of SiO_2 thin films used for capping the ferroelectric, are markedly superior for layers prepared by LTCVD than for layers prepared by plasma- or sputter-deposition. An extensive

literature exists on the mechanisms of charge trapping and bias-stress-induced instabilities in oxide-nitride type FET structures.[24,25] While these studies are useful in defining gate-bias and temperature conditions, and mobile chemical species (e.g. hydrogen), that may initiate current leakage effects, it is important to remember that they pertain only to high-field (> 1 MV/cm) gate-bias modes that exist briefly when the memory device is being addressed. Here, the dramatic retention improvements achieved by doping the ferroelectric layer, and the fact that the original charge migration must have occurred at much lower residual fields (with no externally applied gate bias), imply that the intrinsic dielectric quality of the ferroelectric plays the key role in relation to memory window retention. This, of course, is only true provided that the remaining SiO_2 and Si_3N_4 layers in the FEMFET are adequate to perform their functions.

3.4 Materials and Device Structures Considerations

In the program originally proposed, two thin-film ferroelectric approaches for FEMFET devices were described, the first based on barium magnesium fluoride (BMF) and the second on bismuth titanate (BTO). Previous Westinghouse efforts on MIS test structures had indicated that BMF films were not only highly compatible with the silicon surface, but could yield excellent memory window properties with long-term operation stability. It was already known that in the case of BTO films, further efforts would probably be required to overcome certain interface problems and to control ferroelectric switching behavior. Thus, the BTO technology initially was relegated to a backup role on this program.

Due to parallel recent Westinghouse-supported IRAD efforts (see Appendix D) on bismuth titanate (BTO) in MIS device

structures, the device potential of BTO films (relative to BMF films) appeared promising, so that we focused on this material and other oxide ferroelectrics for our FEMFET memory development efforts during a second phase of the subject contract. Recall, from earlier research on BTO structures by Wu[3] at Westinghouse and Sugibuchi et al.[4] at Nippon Electric, in addition to recent studies by the present authors[5] and Kalkur et al.[26] , that in MI(Si) devices based on BTO films deposited or annealed at high temperatures, polarization reversal (at least at lower frequencies, i.e. < 1 kHz) is dominated and rate-limited by charge injection and trapping from the semiconductor into the ferroelectric. To suppress this tunneling injection, so that normal high-speed polarization switching can dominate, it is necessary to insert a high-quality dielectric buffer (or barrier) between the silicon and the ferroelectric layer. In operation, part of the voltage applied to the MIS gate electrode is now dropped across this dielectric buffer layer, so that the field available for switching the ferroelectric is reduced. The development of high-quality SiO_2 and Si_3N_4 layers for SONOS-type memories and for control of interface states, is a technology in which Westinghouse is a pioneer and world leader. The key issues in the oxide-type FEMFET device structure considered here are to maintain the control and perfection of such buffer layers, while also incorporating a high-quality switchable ferroelectric oxide layer on top.

During the past three years, rapid progress has been made in the deposition and optimization of a wide variety of ferroelectric oxide film compositions[27] , using growth techniques such as rf sputtering, ion-beam sputtering, MOCVD, pulsed laser deposition (PLD) and sol-gel growth. Most of these approaches have been developed in response to the needs for relatively rugged ferroelectric capacitor structures in integrated DRO memory arrays. Insertion of ferroelectric films by such techniques into NDRO FEMFET structures requires

more careful control of thermal and chemical processing conditions in order to avoid degradation of both the semiconductor interface and the ferroelectric layer itself. As indicated in the following discussion, if such control can be achieved ,the FEMFET approach might readily be extended to a much wider range of oxide ferroelectrics, and in particular to materials offering easier processing together with a more attractive combination of chemical stability and ferroelectric and dielectric properties.

3.4.1 Ferroelectric Thin Film Material Options

Table 3-1 shows a brief listing of ferroelectric materials which have been prepared recently in thin film form, by both vapor deposition and sol gel techniques, to yield materials displaying varying degrees of ferroelectric activity. The data shown for permittivity , remanent polarization and coercive field are for selected film samples described in the literature. These numbers are not intended to be representative either of the material or the deposition technique, and in some cases differ widely from bulk values. They are used here simply to develop some criteria by which the relative merits of materials for insertion into FEMFET devices can be evaluated.

To compare the effect of polarization and dielectric parameters on the magnitude of the memory window, we assume an MIS structure with a total buffer layer thickness (including silicon oxide and nitride) of about 300A, and a cap layer thickness of 500A, typical of what were used. The ferroelectric film thickness is assumed to be 5000A (which also is reasonably typical of BTO films used). With an a.c. or pulse signal applied to the gate, the voltage will divide between the ferroelectric and non-ferroelectric layers of the gate insulator in inverse proportion to their effective capacitance. For simplicity, we assume an applied signal of

TABLE 3-1: Electrical Properties for Selected Ferroelectric Oxide Films Considered for Use as Gate Dielectric With Oxide Buffer and Capping Layers in FEMFET Device Structures.

COMPOUND	ε	P_r (C/cm^2)	E_c (kV/cm)	C_f/C_{nf}	E_f (kV/cm)	FOM (E_f/E_c)	FOM (P_s/ε) $(x10^{-1})$
$LiNbO_3$	35	4.5	10	1.4	83.4	8.3	1.3
$Pb_5Ge_3O_{11}$	30	2.5	55	1.2	91.0	1.65	0.8
$KNbO_3$	100	20	20*	4.0	40.0	2.0	2.0
$Bi_4Ti_3O_{12}$	140	30	20-150	5.6	30.4	1.52-0.2	2.1
$BaTiO_3$	200	5	15	8.0	22.2	1.48	0.3
SBN	50	34	51	2.0	66.6	1.31	6.8
PZT	300	35	35	12.0	15.4	0.44	1.2
PLT(15%)	280	38	34	11.2	16.4	0.48	1.4

Footnote:

* - Data estimated from electro-optic switching fields.
f - Ferroelectric
nf - Non-Ferroelectric

+10V or - 10V. The ratio of ferroelectric layer to non-ferroelectric layer capacitances, C_f/C_{nf} , can be derived from the permittivity and thickness values, and is listed in the table. From these data we obtain the voltage , V_f, and field E_f across the ferroelectric, which can be compared with the coercive field E_c (usually listed for a fully saturated loop). With the exception of bismuth titanate and lithium niobate, few experimental data are yet available for MIS or FEMFET structures incorporating these thin film dielectrics as a gate insulator.

Although in all the cases listed in Table 3-1 the need for a separate oxide barrier to suppress tunneling is assumed, this assumption may not be valid. For example, in the case of $LiNbO_3$ the recent studies by Rost et al.[11] using sputtered films as the gate dielectric, have claimed that switching proceeds by the normal polarization reversal process, without occurrence of charge injection into the ferroelectric film. To explain this observation it is asserted that the lithium niobate film , during deposition, is relatively unreactive towards the silicon surface, and thus there is a reduced tendency to generate a thin oxide tunneling barrier at the semiconductor/dielectric interface. It is clear from results emerging in the literature that each ferroelectric oxide film material, depending on deposition conditions, will probably generate its own set of interfacial chemical and electronic artifacts when grown directly on silicon. In recognition of this problem, Westinghouse has sought to simplify the interface situation by using , for all ferroelectric oxide films studied in this program, a standard buffer structure approach based on silicon oxide/nitride.

3.4.2 Influence of Processing and Structure / Critical Parameters

Using the data in Table 3-1, we derive a preliminary summary

of expected relative performance, comment on the usefulness of the parameters listed, and suggest directions of research on processing and the device structure which should lead to optimization of FEMFET performance. At first sight, for the buffered and capped structures assumed here, a combination of low permittivity , low coercive field and reasonably high polarization appear to offer the best performance. From the first two of these parameters, the ratio of the field across the ferroelectric to the coercive field, E_f/E_c, can be estimated as a switching figure of merit. This field ratio is highest for $LiNbO_3$, but also exceeds unity for five of the other materials (although the situation for BTO varies widely with the reported values of E_c). It is lowest for the $PbTiO_3$ -based ferroelectric films, due to the higher values of permittivity. Although the ratio E_f/E_c defines the ease of storing information in the memory during operation, it ignores the problem of retaining the information. For good retention, as discussed above, E_c should be higher than the depolarizing field. With this problem in mind, in Table 3-1 we list additionally estimated values of the operational figure of merit P_r/ε.

A high switching FOM value, as defined by the field ratio E_f/E_c, should ensure that the effective P_r displayed by the ferroelectric gate dielectric will be equal to, or approach , the numbers listed in Table 3-1. However, it should be remembered that to obtain these values of P_r in practice, we must apply a total switching voltage which significantly exceeds E_c. Thus, it is important that the value of the switching voltage needed for saturation also should be low. In materials with high values of P_s, such as $LiNbO_3$ (71 $\mu C/cm^2$) and BTO (50 $\mu C/cm^2$), partial switching of the polarization probably is adequate for operation of the FEMFET. In the case of the hysteresis loop, this would correspond to a minor loop condition (see e.g. the family of loops shown for BMF films in the Interim Report[1]. The numbers

quoted in Table 3-1 for several cases clearly correspond to partial switching situations. In Figure 3-6 we illustrate a plot of remanent polarization (after switching) vs. switching field, Esw, for a recent BTO film deposited (by pulsed laser deposition; see Appendix D) on a platinum-coated substrate. Although the highest value of P_r recorded for this randomly oriented film structure was about 25 $\mu C/cm^2$, the lowest value, corresponding to a switching field of 225 kV/cm (and E_c = 43 kV/cm) was about 2.5 $\mu C/cm^2$. This number is still somewhat higher than that required to operate the FEMFET device (see Section 3.6.4). However, the switching field of 225 kV/cm would correspond to a required gate address voltage of about $\pm$ 70 V , if buffer and capping layers of the type assumed for Table 3-1 were to be employed. In view of this analysis it is surprising that our MIS measurements with BTO have yielded significant CV memory windows with address voltages of $\pm$ 20V. We can only conclude that sufficient switching of the low coercive-field c-axis component of the polarization may be occurring at much lower applied field values.

From the analysis just given for BTO gate dielectrics it is clearly desirable to develop processing approaches, both for BTO and for the other ferroelectrics listed in Table 3-1, to increase the field in the ferroelectric film component and/or to decrease the switching fields needed to reverse the polarization. One approach to increase the field in the ferroelectric, would be to replace the silicon oxide/nitride buffer and cap component layers with high-permittivity layers (such as amorphous ferroelectric films). Unfortunately, most of the candidate materials are known to exhibit markedly inferior properties in relation to current leakage and breakdown strength. Lowering the switching field, and/or changing to another ferroelectric such as $LiNbO_3$, which in c-axis oriented films seems to show unusually low values of coercive field (cf. Table 3-1) would appear to be the main

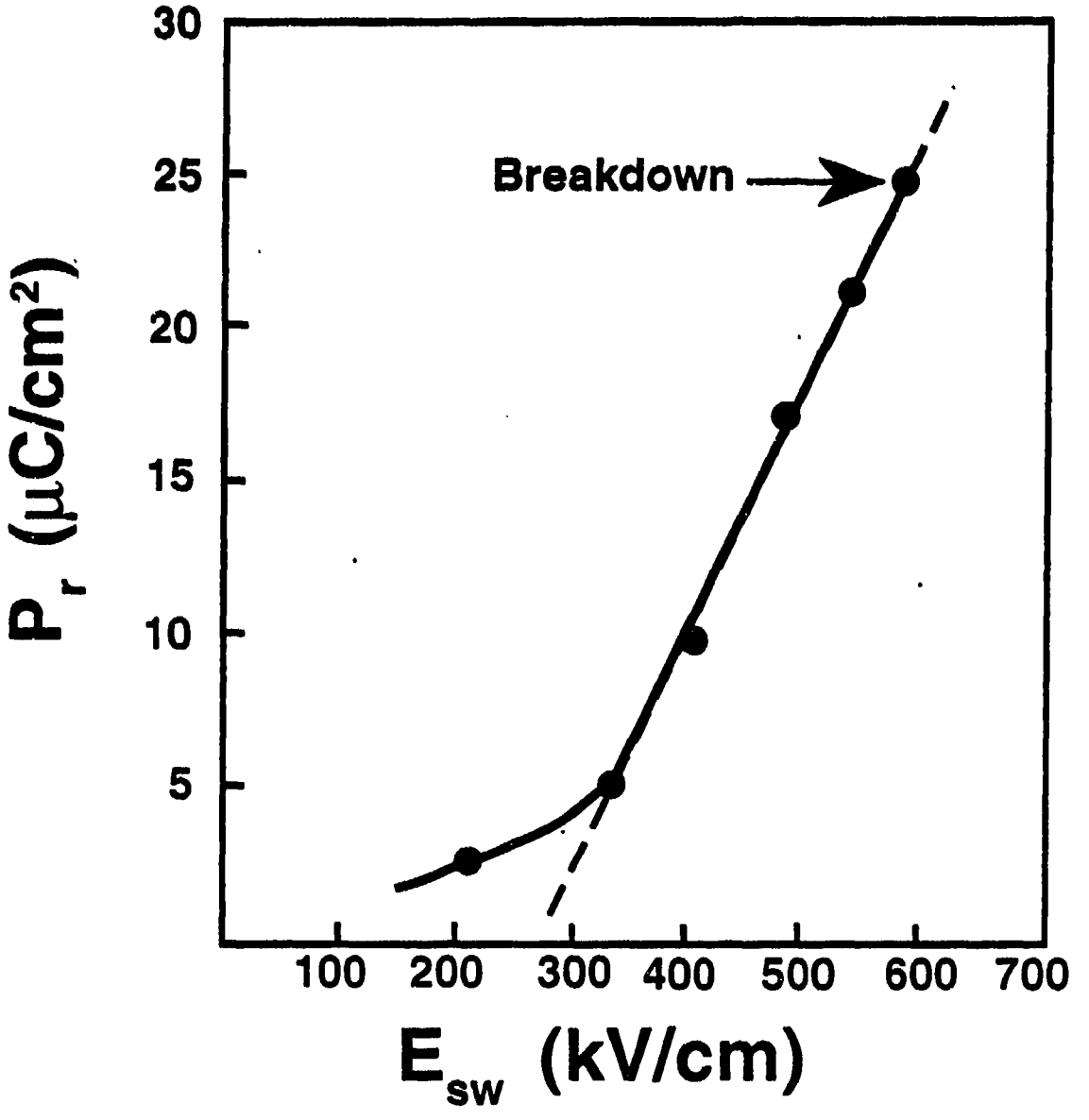

Figure 3-6: Hysteresis Loop Data for Ferroelectric Bismuth Titanate (BTO = $Bi_4Ti_3O_{12}$) Film Grown by Pulsed Laser Deposition (PLD) Remanent Polarization (P_r) Values are Plotted vs. Switching Field E_{sw}.

option available to us. However, c-axis films of $LiNbO_3$ are only achieved on (111)Si, which is not used in standard CMOS processing. It is well known that some ferroelectric films, such as $PbTiO_3$, PZT, PLT and BTO, can exhibit significantly lower coercive fields in epitaxial structures, as summarized in Reference 27. However, to incorporate this concept in the FEMFET device we would need to employ epitaxial buffer layers such as YSZ, MgO or $MgAl_2O_4$, which would also have to function as effective tunneling barriers. Preliminary experiments with high dielectric constant and epitaxial buffer layers and alternate oxide ferroelectric materials were attempted late in this program. No success has yet been achieved with the alternate buffer approach. MIS structures with lead germanate (PGO) gave the largest memory windows but retention was poor. Large memory windows and good retention were achieved with PZT used in FEMFET gate stacks (see section 3.6.4 for details of these results).

3.4.3 Retention Properties and Device Optimization

At the start of this effort on MIS BTO structures it was shown that, although greatly superior to that of BMF structures, retention properties with BTO in general still fell far short of the program goals. In the latest work near the end of the program, two aspects were targeted in an effort to improve retention. The first of these involved an effort to reduce mobile charge migration in the BTO layers through the La and Nb doping approaches referred to above. Although this approach has not yet been optimized, it has already led to marked improvements in retention[19]. The second approach involved a change in the process used for fabricating the capping layer, from LPCVD to rf magnetron sputtering. It had been suspected for some time that the release of atomic hydrogen in the silane-based LPCVD process might be causing deleterious chemical reduction of the BTO film surface. These changes have resulted in startling

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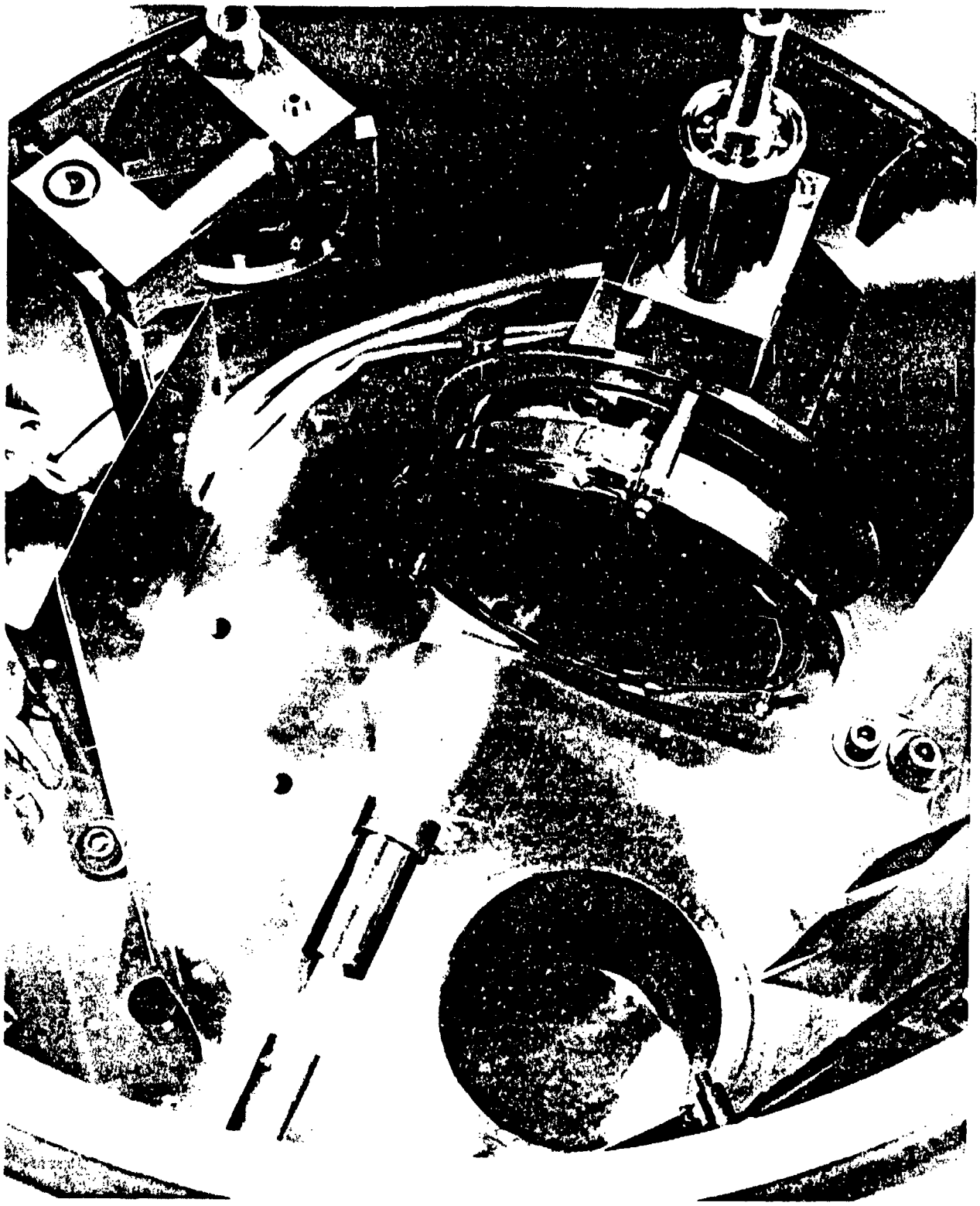


Figure 3-8: Scaled Pulsed Laser Deposition(PLD) Deposition Chamber Showing Capability to Coat 4-Inch CMOS Wafers.

Figure 3-9: 4-Inch Silicon Wafer with Visible Interference Fringes Displaying Coating Thickness Uniformity.

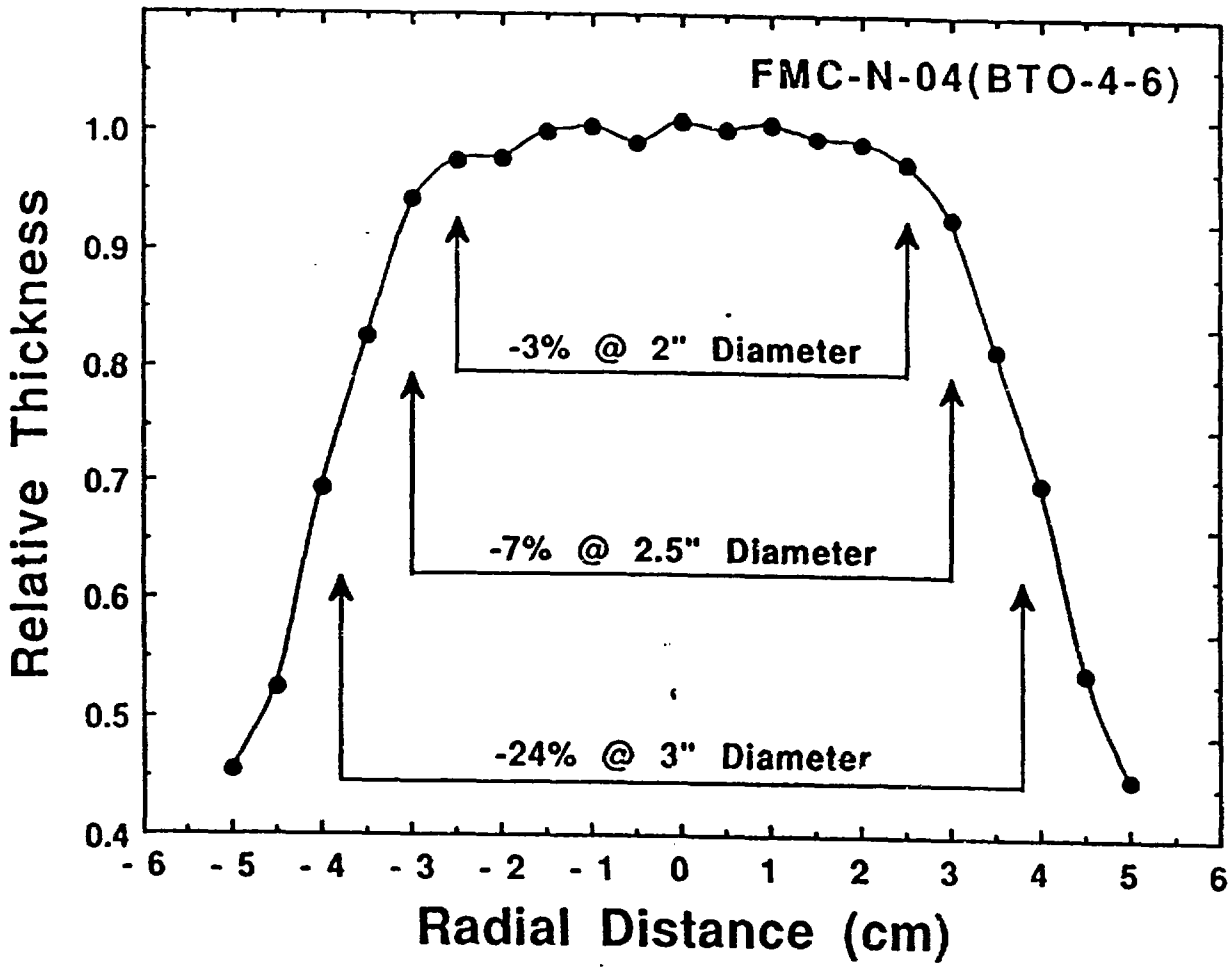


Figure 3-10: Typical Ferroelectric Thin Film Thickness Uniformity Profile on a 4-Inch Silicon Wafer.

the uniformity was -3%, -7%, and -24% over 2-, 2.5-, and 3-inch diameter areas, respectively. The drop in thickness at approximately 3-inch diameter is consistent with the observation of the interference fringe observed in Figure 3-8. Further improvement of uniformity could have been achieved, at considerable expense, by automatically scanning the laser beam over the target surface, but was determined not to be necessary for the present program. See section 3.6.3 below for good results of electrical measurements (CV memory windows) of BTO gate stacks, suitable for FEMFET devices, fabricated on a 4-inch wafer; where the BTO layer was deposited using the above large-area PLD apparatus.

Typical PLD deposition parameters used to deposit oxide-ferroelctric films on 4-inch wafers were laser energy density of 1-2 J/cm2, pulse repitition rate of 10-30 Hz, and partial O2 pressure of 200mTorr. Most of the films were deposited using a one-step temperature process involving depsoition at 450-550C to achieve crystallization as-deposited, without the need for a post-deposition oven anneal. Some films were prepared using two-step temperature processes involving deposition of an amorphous film at low temperature (25-350C) followed by a rapid thermal anneal (RTA) at high temperature (600-750C) for a few seconds. Appendix A lists details of the PLD deposition parameters for oxide-ferroelectric films deposited on 4-inch wafers used for various device processing evaluations (see section) and electical testing (see results in section 3.6.4).

3.6 Electrical Testing

3.6.1 Generic Ferroelectric Memory Gate Structure

The conductor (metal)-insulator-semiconductor (MIS) device is an extremely useful tool for the development of semiconductor integrated circuits. Since the reliability and stability of

all semiconductor devices are intimately related to their surface conditions, an understanding of the surface physics with the help of MIS devices is very important during device development. The MIS structure of Figure 3-11 has d as the thickness of the insulator and V as the applied voltage of the conductive plate. In this discussion we use the convention that the voltage V is positive when the conductive plate is positively biased relative to the semiconductor body via the ohmic contact, and conversely. The total capacitance C of the series combination of the insulator capacitance C_i ($=\varepsilon_i/d$) and the semiconductor depletion-layer capacitance C_D is:

$$C = \frac{C_i * C_D}{C_i + C_D} \qquad (3\text{-}6)$$

For a given insulator thickness d, the value of C_i , is constant and corresponds to the maximum capacitance of the series combination.

Figure 3-12 illustrates typical CV behavior in N-channel devices with a p-type body. Where the gate is negative relative to the p-type body, there is an accumulation of holes and a high differential capacitance for the semiconductor. As the negative voltage is reduced sufficiently, a depletion region that acts as a dielectric in series with the insulator is formed near the semiconductor surface, and the total capacitance decreases. For cases where the mobile electrons are able to follow an applied ac signal, the combined series capacitance goes through a minimum and then increases again as the inversion layer of electrons forms at the surface. Note that this increase of capacitance only happens at very low frequencies where the recombination-generation rates of minority carriers (electrons, in our example) can keep up with the small ac signal in step with the measurement signal. Consequently,

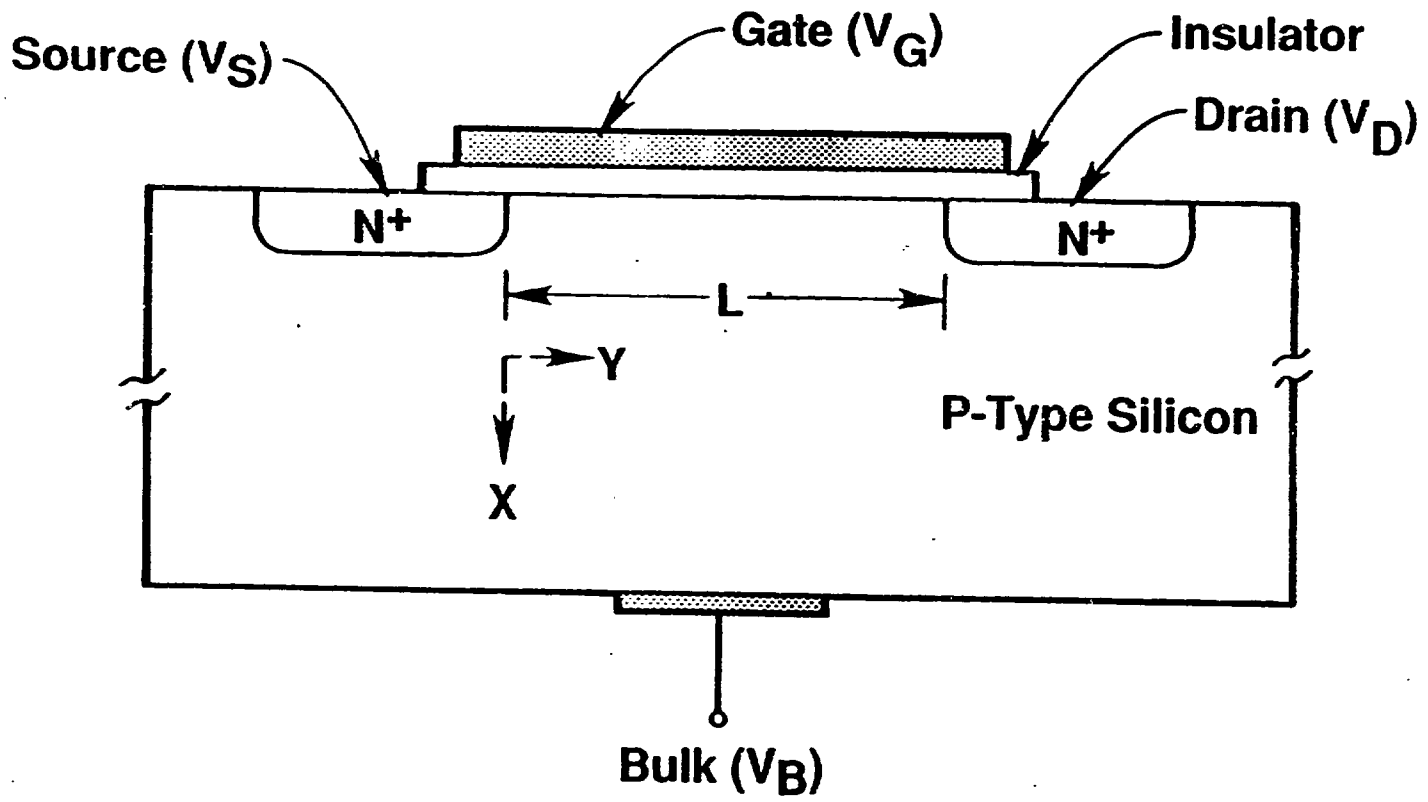


Figure 3-11: The MISFET Cross-Section.

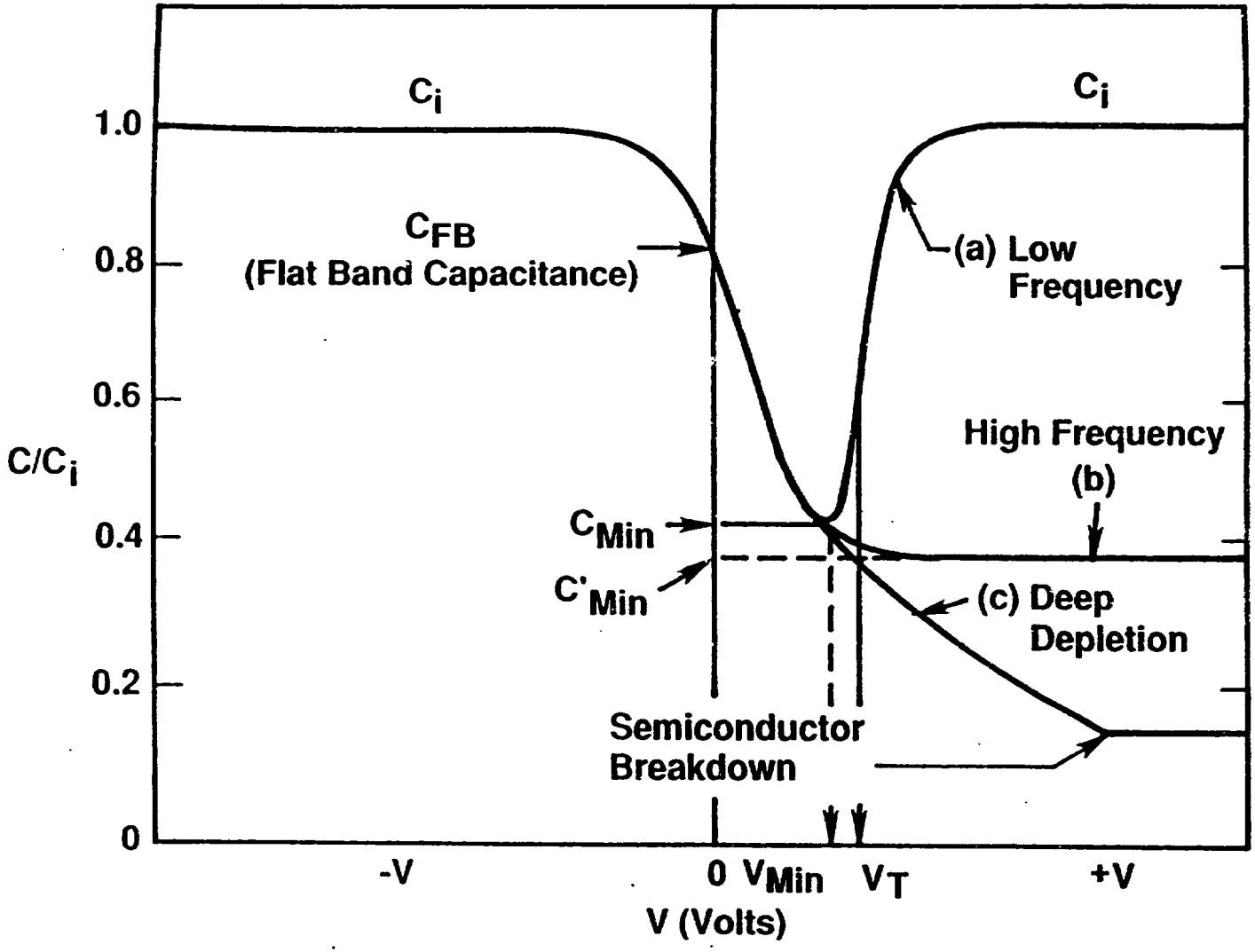


Figure 3-12: MIS Capacitance-Voltage (CV) Curves: (a) Low Frequency, (b) High Frequency, (c) Deep Depletion.

for higher frequencies, MIS curves do not show the increase of capacitance as the gate voltage goes positive relative to the p-body, as in curve (b) of Figure 3-12. For the deep depletion condition, usually associated with pulse operation as in a CCD, curve (c) of Figure 3-12 shows an even further reduction of capacitance due to a greater depletion depth.

Various mechanisms operate to provide the equivalent of a sheet of charge in the vicinity of the silicon-dielectric interface. Figure 3-13 (Figure 3-2 repeated for convenience of the reader) shows the shift along the voltage axis of a high-frequency C-V curve when positive or negative charge Q_f is present at the interface, measured relative to an ideal C-V curve where $Q_f = 0$. A positive Q_f causes the C-V curve to shift toward more negative gate bias values for both n- and p-type transistor bodies, and conversely. Identifying the charge Q_f with the effective reversible surface charge of a polarized thin film of ferroelectric material, Figure 3-13 directly suggests the programming method for a ferroelectric memory FET (FEMFET); illustrated schematically, in Figure 3-14 with emphasis on the ferroelectric spontaneous polarization (P_s). When the gate (conductive plate of Figure 3-11) is positive relative to the transistor body, the reversible ferroelectric spontaneous polarization switches orientation so that the negative electric dipole changes are adjacent to the positive gate forcing the positive electric dipole charges to be at the silicon interface, and conversely. Switching the ferroelectric dipoles in the gate region of the FEMFET is equivalent to super-imposing the right and left curves of Figure 3-13, and is shown at the top in Figure 3-15.

Early investigation of the FEMFET used the test cross section shown in Figure 3-15 to evaluate the behavior of highly-oriented ferroelectric films on silicon for use in nondestructive readout (NDRO) nonvolatile memories. In the

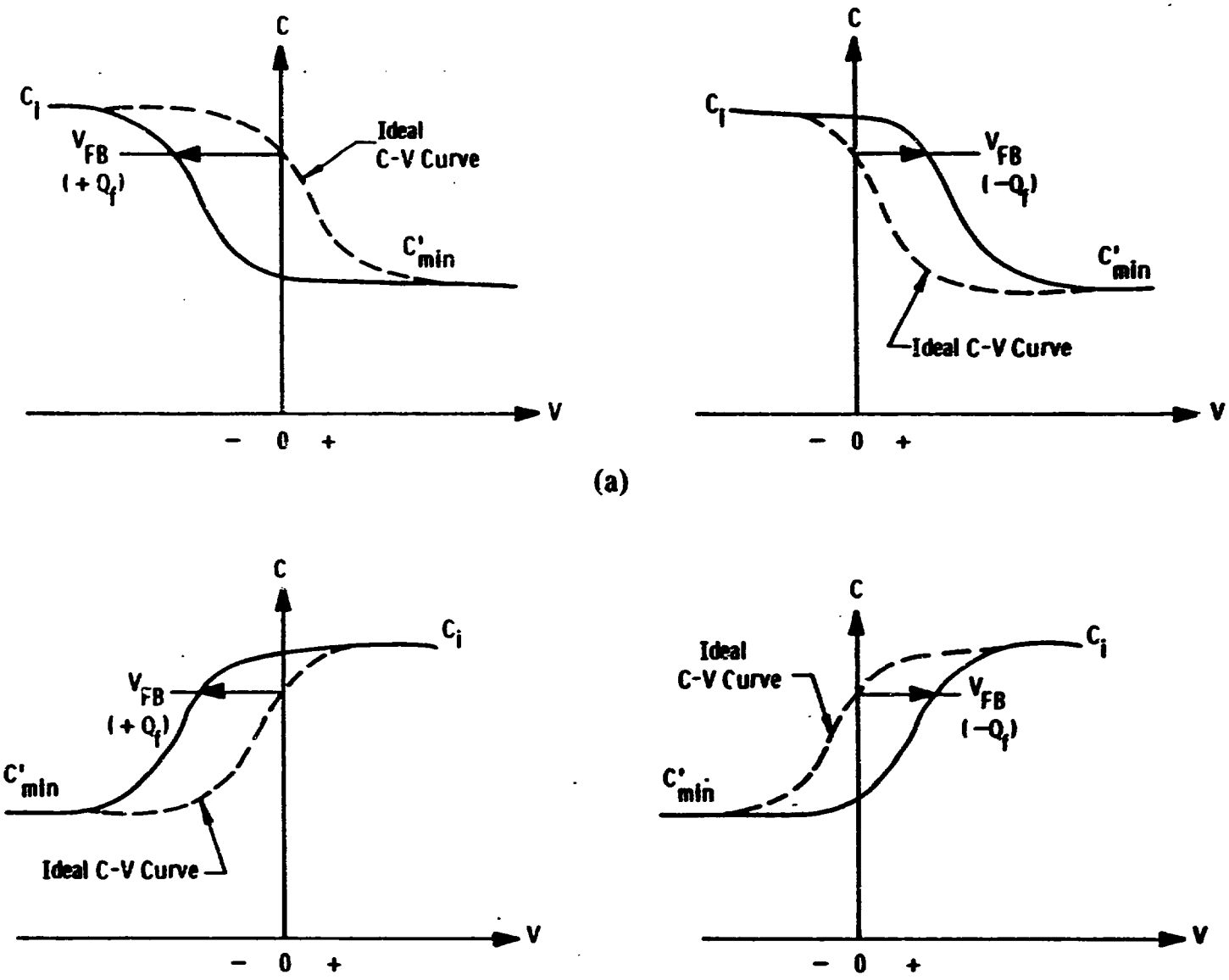


Figure 3-13: CV Curve Shift Along the Voltage Axis Due to Positive or Negative Fixed Charge. (a) For P-type Semiconductor, (b) For N-type Semiconductor.

Memory FET Programming

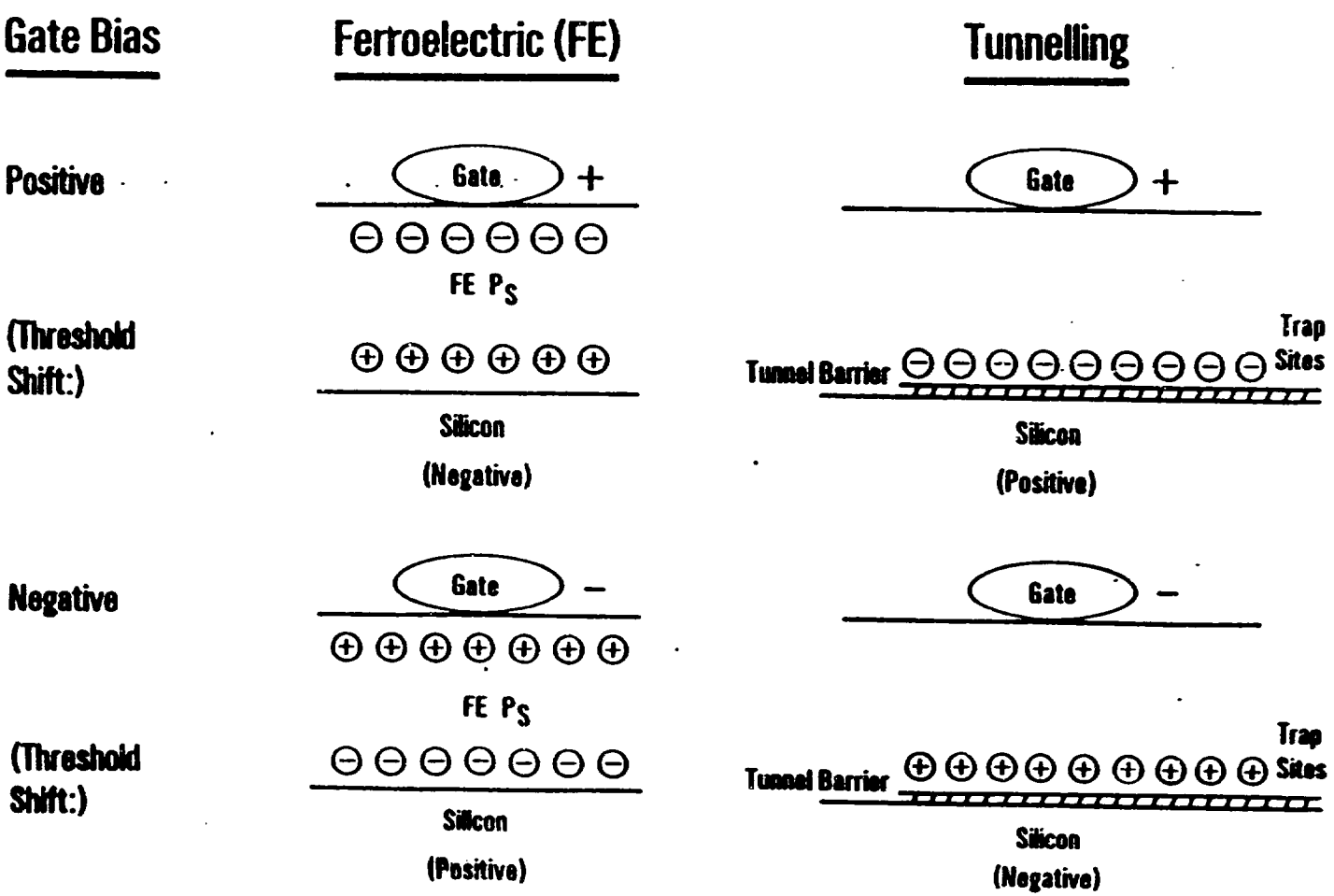


Figure 1-14: Ferroelectric Memory FET Programming.

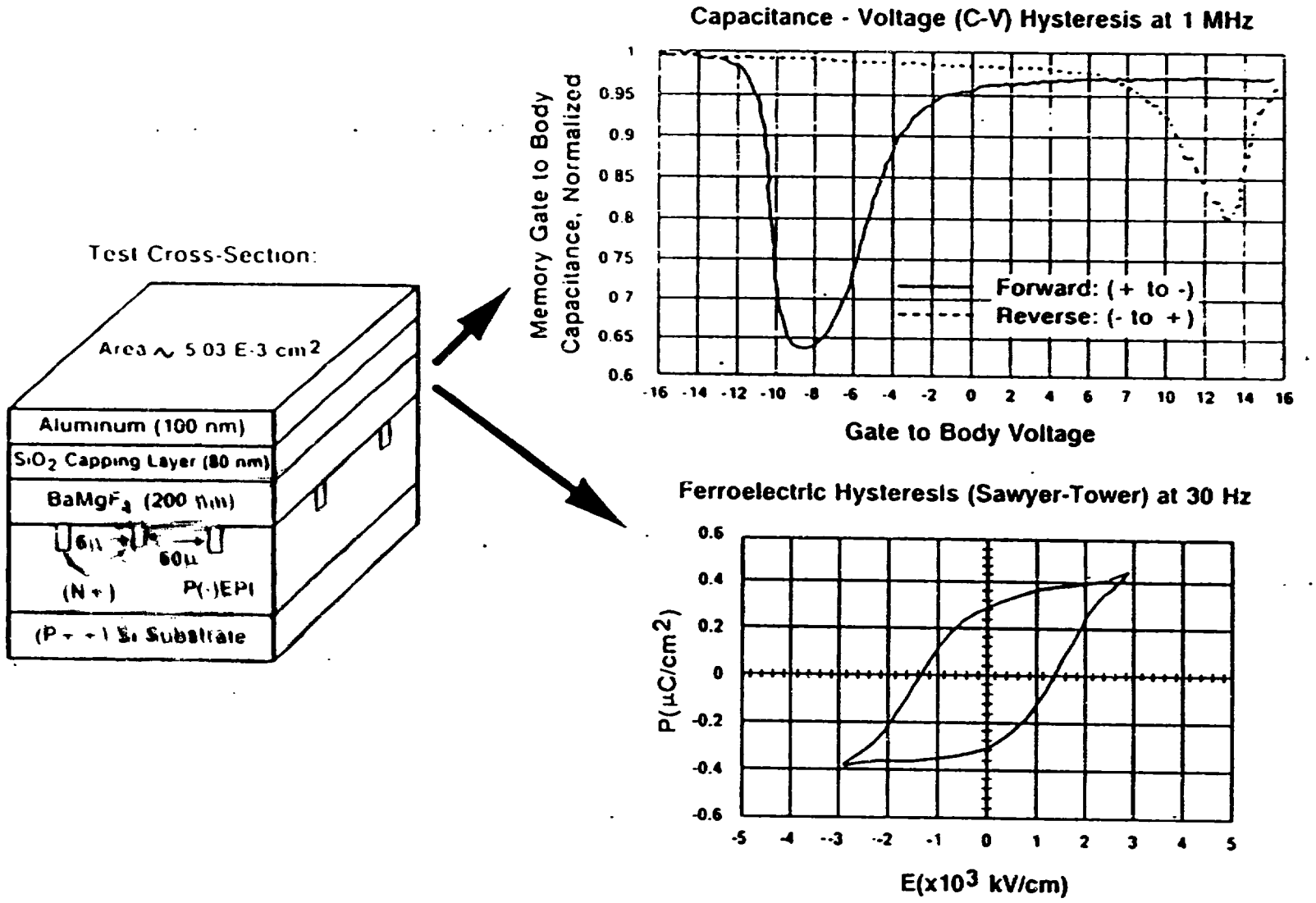


Figure 3-15: Cross-Section and Typical Hysteresis Curves Measured on a FEMFET Gate Stack With an Al-Dot Top Electrode: (a) Top Right-CV Hysteresis; (b) Bottom Right-Polarization Hysteresis.

upper right corner of Figure 3-15 typical results are shown of an unstressed BMF ferroelectric film without any annealing or other processing after film growth. It incorporates many features of the C-V curves of the preceding description. The most prominent attribute is the 10.8V threshold shift (generally called the "memory window") in response to the ±10V programming. The C-V hysteresis loop was scanned at the rate of 75mV/s at room temperature, with its clockwise trace indicated by arrows. The (-10V) bias polarizes the ferroelectric film with negative sheet charge near the silicon, turning "off" the associated N-channel MISFET, and conversely. Combining the 10.8V threshold shift with the (maximum) dielectric capacitance and the area of the memory capillary gives a charge change of about 10^{12} electrons per square centimeter. Although that charge density of about 0.16 μC per cm^2 is much smaller than typical ferroelectric spontaneous polarization values, the net effect on the FEMFET is more than adequate for fast-read (50 nsec) nonvolatile memories. Also, note that the 10.8V memory window results from the application of ±10V programming bias. The 10V programming shown in Figure 3-15 derives mainly from the film thickness exceeding 400 mm for an approximate programming field around 250 KV/cm. The FEMFET structure, however, is quite amenable to scaling. That is, a thinner ferroelectric film should allow reducing the programming bias to lower values, e.g. 5 V for ferroelectric films around 200 mm or less in thickness. Because of the scan rate of 75mV/s, all of the above results are representative of saturated rather than partial programming that might occur in the case of programming pulses of shorter duration and/or lower fields.

3.6.1.1 Novel Testing Approach for Predicting Data Retention in Nonvolatile Memory Transistors

In Figure 3-15, there are two types of hysteresis curves: at the top right in the figure is the the C-V hysteresis loop

(characteristic of semiconductor nonvolatile NDRO memory) and at the bottom right is the field-polarization hysteresis plot (of the Sawyer-Tower kind). Notice that the C-V hysteresis curve goes through two minima: first as the gate voltage sweeps from negative to positive, increasing again as the inversion layer of electrons forms at the surface, then also with the opposite sweep applied to the gate. For the traditional C-V dot structure, the increase in capacitance in both directions from the minimum occurs only at very low frequencies or other conditions where the generation rate of minority carriers (electrons, in our case) can keep up with the small signal variation and lead to charge exchange with the inversion layer in step with the capacitance measurement signal. Another way of providing adequate minority carriers for that interaction with the inversion layer is to incorporate a grid of the opposite type of doping (cf. Figure 3-15). Such a grid is essentially the same as the regular "source-drain" doping used for the associated FETs. This gridded wafer configuration for testing nonvolatile memory gate stacks by means of C-V dots provides significant advantages over unpatterned wafers for that application. Figure 3-16 illustrates a typical hysteresis curve using gridded wafers with an earlier bismuth titanate (BTO) ferroelectric memory gate stack. Notice that the minimum during the forward sweep from +10V to -10V occurs at about -3V, while that for the reverse sweep occurs just below +3V for an approximate memory (threshold) window of almost 6V. Typically this memory window collapses (loss of retention) at a very slow rate (about 0.25V to 0.33V per decade of time for a 10V-programming SONOS EEPROM memory gate stack at room temperature). That is, the depletion threshold moves toward the enhancement state and the enhancement threshold moves toward the depletion state with some characteristic closure rate. This is illustrated in Figure 3-16 with the arrows labelled "Probable V_{th} Shifts". The associated memory stack capacitance, C_g, shifts are likewise indicated in the figure

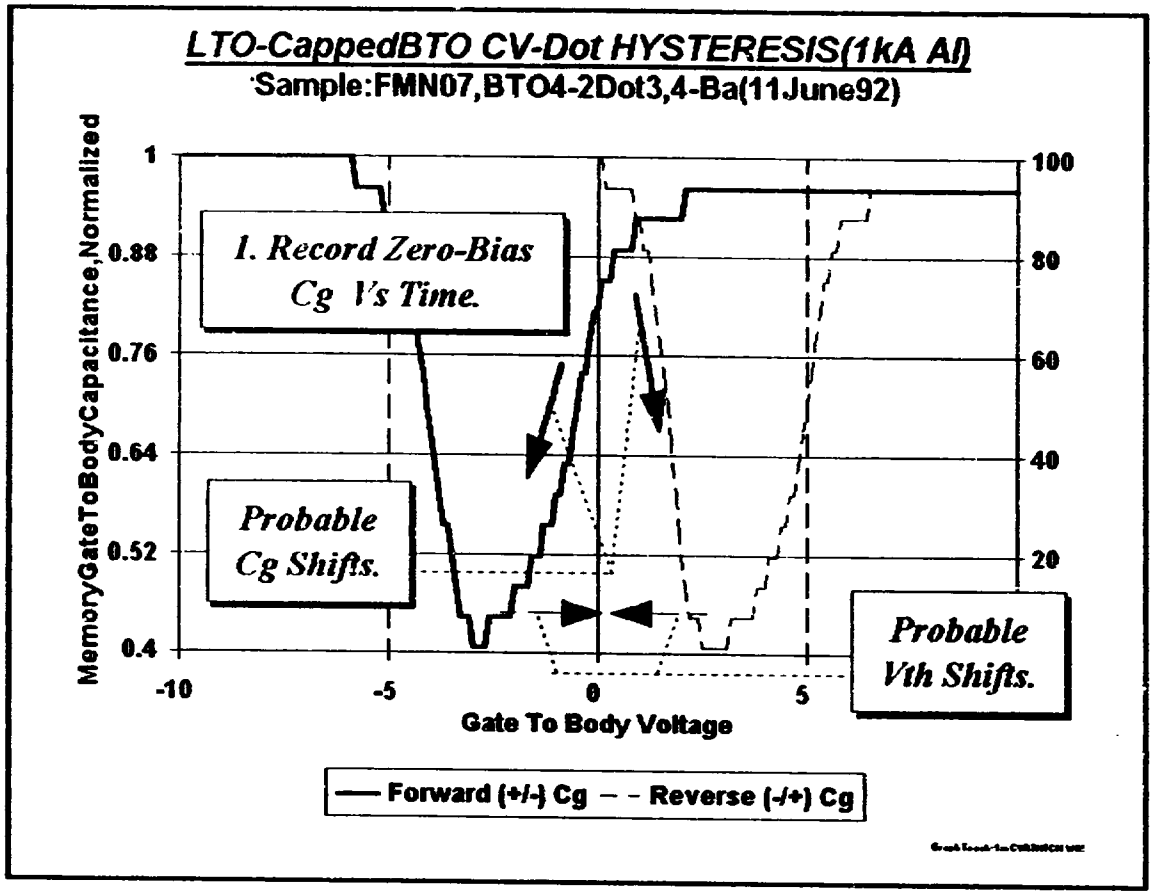


Figure 3-16: Ferroelectric Capacitance Versus Gate Voltage (CV) Hysteresis Results on a Gridded VLSIC CMOS Wafer, Indicating Likely Drifts as a Function of Time.

with the labels "Probable C_g Shifts".

In a traditional NDRO nonvolatile memory chip, the memory stacks (where the data are stored) experience NO externally applied or internally generated voltage bias during the long periods of time when data are not being written into or read from the storage locations. Consequently, any retention test should use the same bias conditions during the waiting times between programming and readout. That is, the overlying conductive gate is DC biased to the same potential as the underlying semiconductor during those waiting times. Applying this boundary condition requirement to the case of using C-V dots to predict retention means that the C-V dot capacitance is measured at zero bias as a function of time. Indeed, this is the action indicated in Figure 3-16 by the instructional label "record Zero-Bias C_g versus time".

3.6.1.2 Conversion From Cg to Apparent Gate Voltage Shift and Thence to Inputed Flatband Shift

The data recorded in the manner indicated in Figure 3-16 are simply time histories of the capacitance of the C-V dots for the two oppositely programmed states of the memory stack at the temperature at which the device was held during the time of the tests. We further assume that the time required to record the hysteresis curve was extremely short compared to the duration of the C-V time histories; so that any recorded threshold drift caused by the measurement represents a truly negligible perturbation on the hysteresis curve. Consequently, the hysteresis curve can be used to transform the timed sequence of zero-bias capacitance values into a timed sequence of "apparent gate voltages", or equivalently a history of apparent gate voltage shifts as a function of time, as implied in Figure 3-17. In reality, of course, the bias across the capacitor has remained steady at zero volts. As illustrated in Figure 3-18, a "historical record of

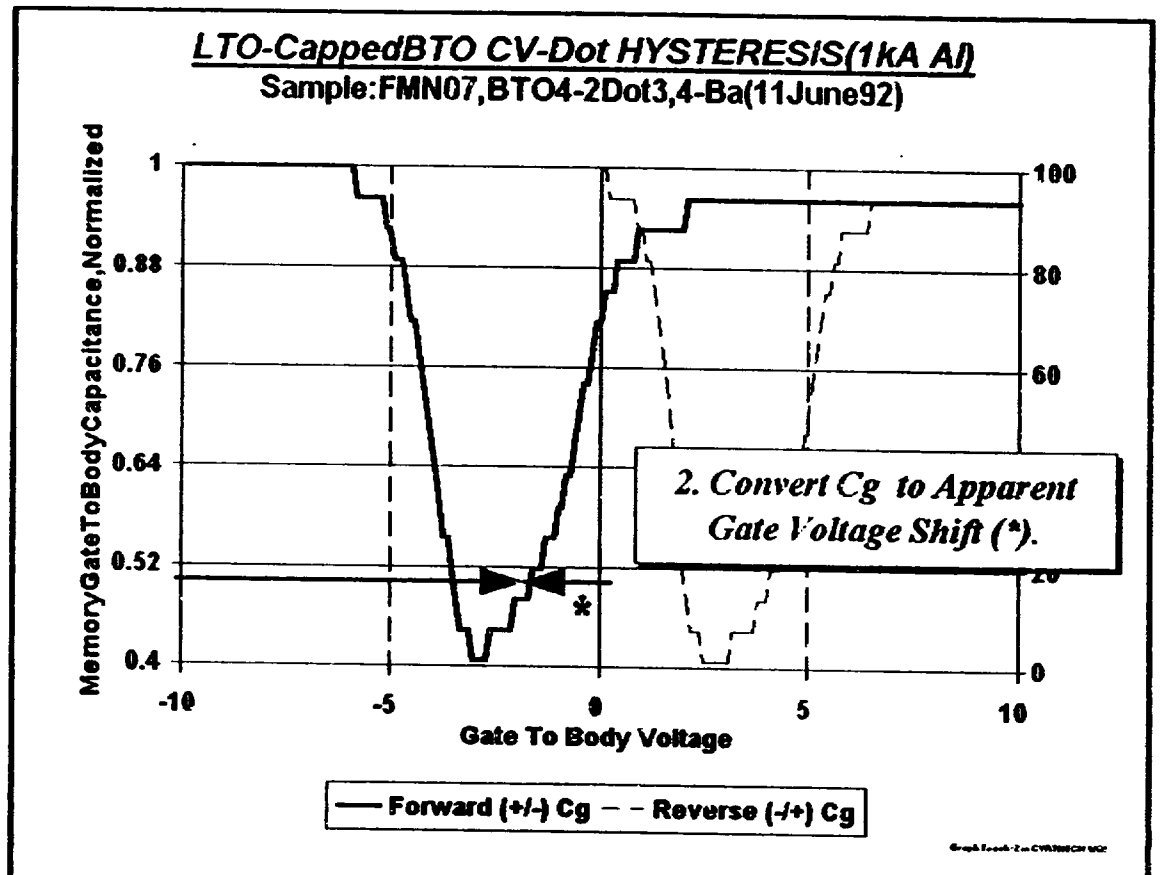


Figure 3-17: The Conversion From the C_g Values to the Apparent Gate Voltage Shift.

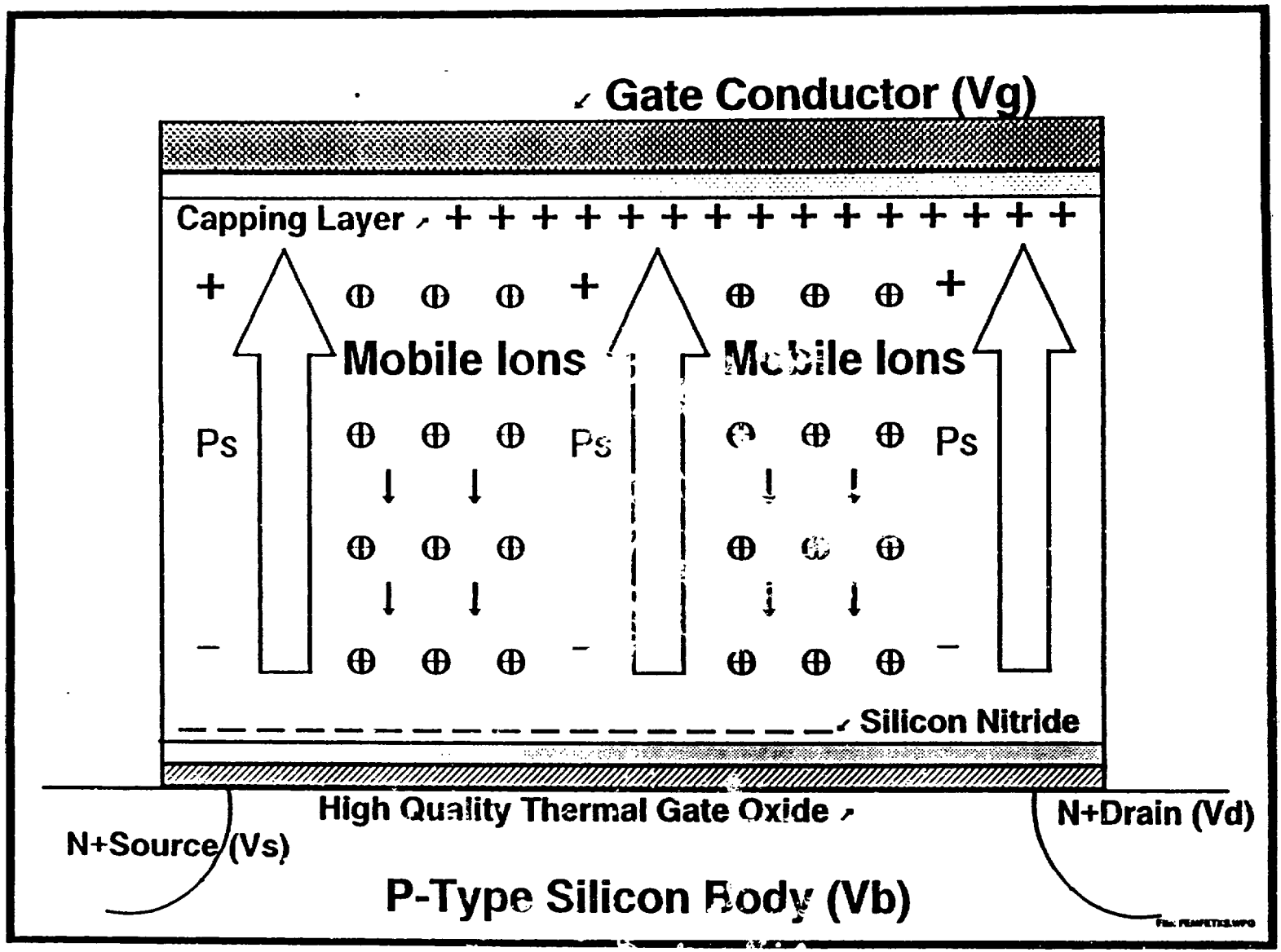


Figure 3-18: Illustrative Distribution of Charges and Polarization Within a Ferroelectric Memory Stack.

apparent gate voltage shifts" is actually the measurement of the effects of mobile charge within the memory stack structure. Notice that the ferroelectric polarization direction has been programmed UP by applying a negative bias to the overlying conductive gate. This results in a POSITIVE charge sheet near the top of the ferroelectric layer and a NEGATIVE charge sheet near the bottom of the ferroelectric layer. Often, mobile charges include more than one species; but an important one in many oxide-type ferroelectrics is the oxygen vacancy, which behaves like a positive mobile ion. The resultant internal electric field tends to move these positive mobile ions toward the semiconductor, as indicated with the smaller arrows. As more and more such positive mobile ions migrate and come to stay near the surface close to the semiconductor, they compensate the negative sheet of charge associated with the ferroelectric polarization direction. Compensation of some of the charges in that negative charge sheet nearest the semiconductor by the positive mobile ions tends to shift the threshold voltage negatively from enhancement toward depletion for an N-channel MISFET.

Next, Figure 3-19 illustrates calculating the imputed flatband voltage (versus time) by subtracting the apparent gate voltage shift from the initial flatband voltage. This step is a simple subtraction and gives two numerical sequences as functions of time: one describing the imputed flatband after positive programming and the second describing the imputed flatband after negative programming. Plotting both on a logarithmic time scale immediately reveals the rate at which the memory window (the difference between the two lines) is decaying. A typical result from the above process is illustrated in Figure 3-20. These early results for a bismuth titanate (BTO) memory stack imply that a FEMFET with that characteristic could not be read to discriminate the memory state originally programmed after about 1,000 minutes,

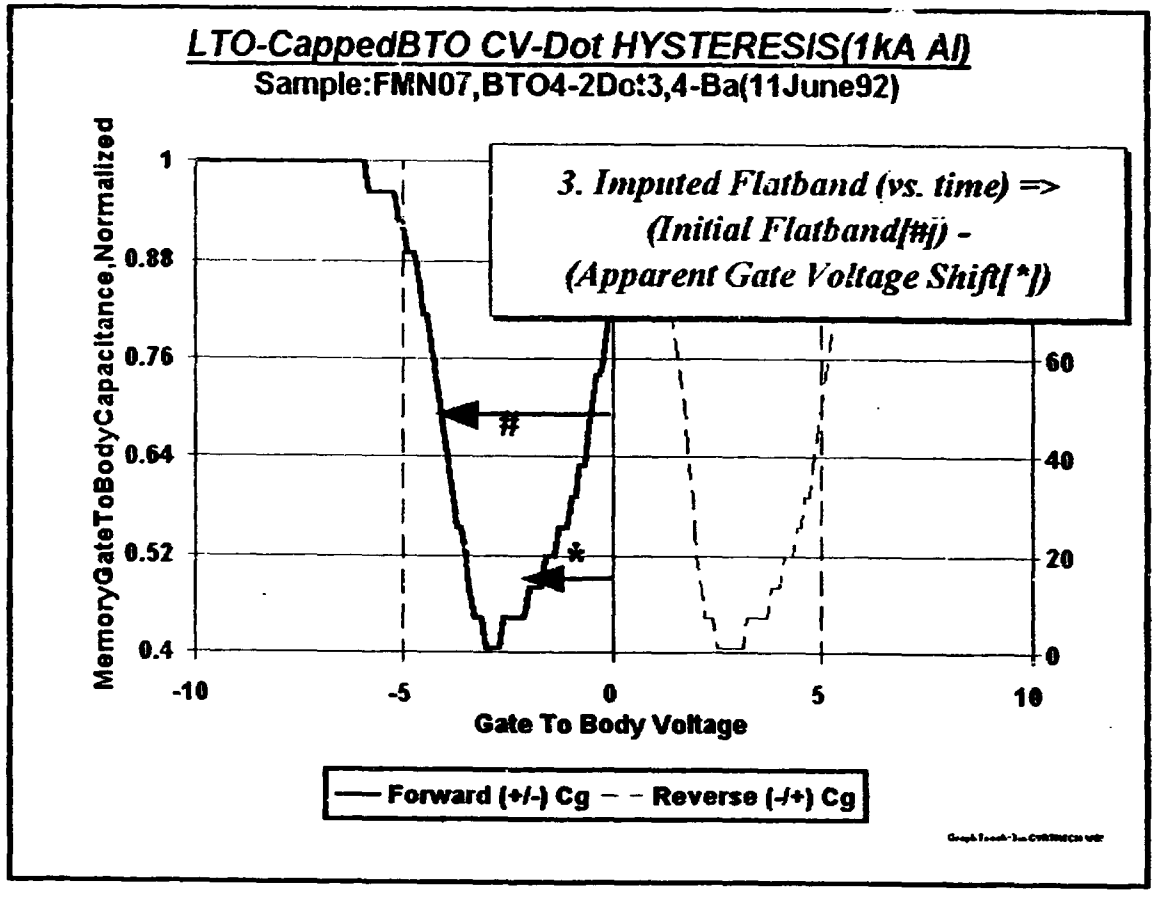


Figure 3-19: Calculating the Imputed Flat-Band Voltage as a Function of Time.

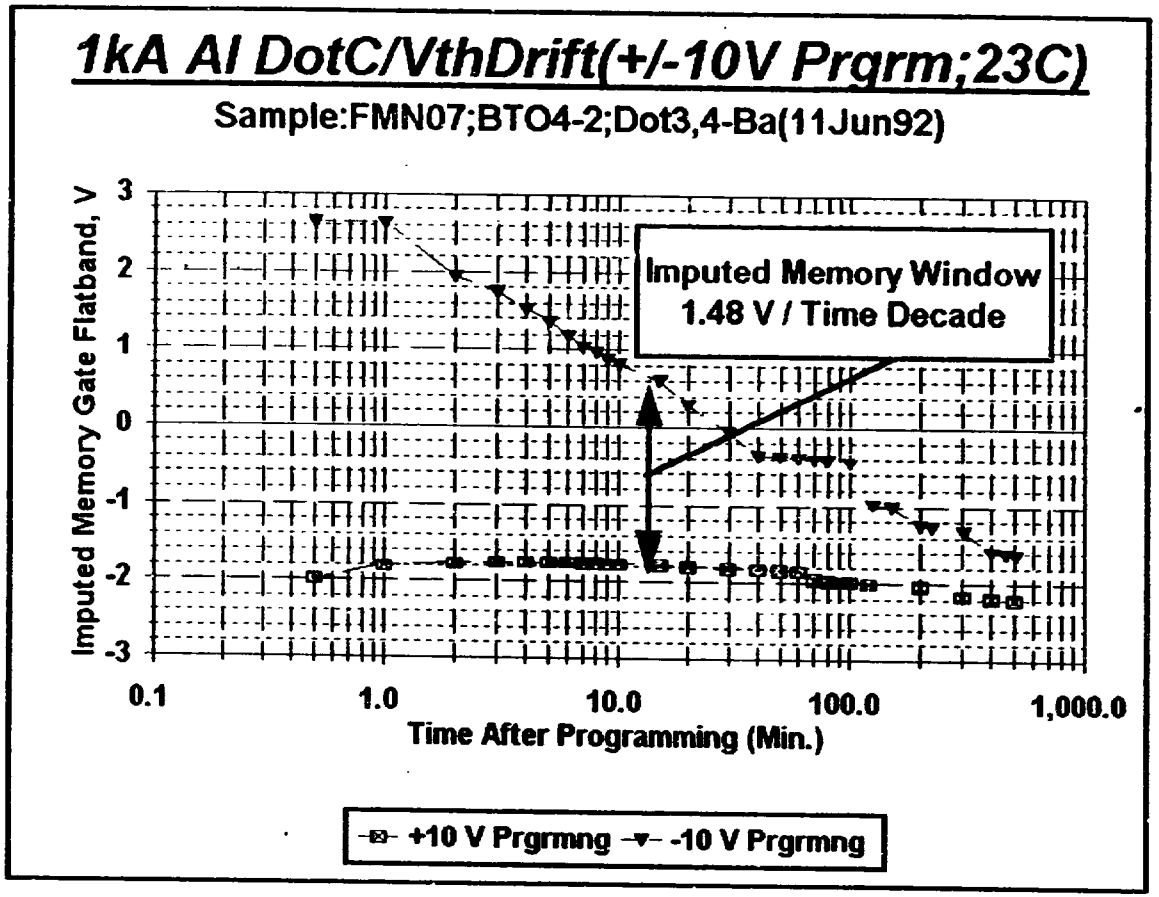


Figure 3-20: Example Resultant Imputed Threshold Drift for an Early Buffered BTO Gate Stack Implying Fast Memory Window Decay (1.48 V/Time Decade).

because the two states had essentially drifted to within less than 0.1 volt of each other.

3.6.1.3 Validation Using SONOS EEPROM Product

To determine whether the above method of imputing memory window decay is valid or not, a known and well-documented reference must be measured by the above technique. The technique then can be assumed valid if the results and conclusions from the new technique agree with the memory retention results obtained using EEPROM industry standard test techniques. Westinghouse ATD, Baltimore, MD manufactures SONOS EEPROMs for various United States government users. These are thoroughly tested by Sandia National Laboratories, under a variety of stringent conditions involving elevated ambient temperatures and high-energy irradiation. The technique described above was applied to a memory stack capacitor fabricated over a "N-" tub characteristic of a P channel SONOS FET. The results are given in Figure 3-21. The negative threshold state corresponds to the "CLEAR" state in the usual N-SONOS EEPROM, while the positive threshold state corresponds to the "WRITE" state in the usual N-SONOS EEPROM. Notice that the drift of the "CLEAR" state was imputed to be 114mV/decade of time, while the drift of the "WRITE" state was imputed to be 252mV/decade of time.

Because of the very slow scanning of the CV instrument, the resultant programming of the memory stack and the imputed drift must be associated with "saturated" programming, in contrast to the faster programming used when the EEPROMs are built into fieldable equipments. The latter scheme uses 10V for 7.5 msec. for "clearing" and 2.5 msec for "writing". When these pulses are used for testing transistors identical to those in the core of the EEPROM memory array for times out to 100 seconds, the retention measurements by Sandia National

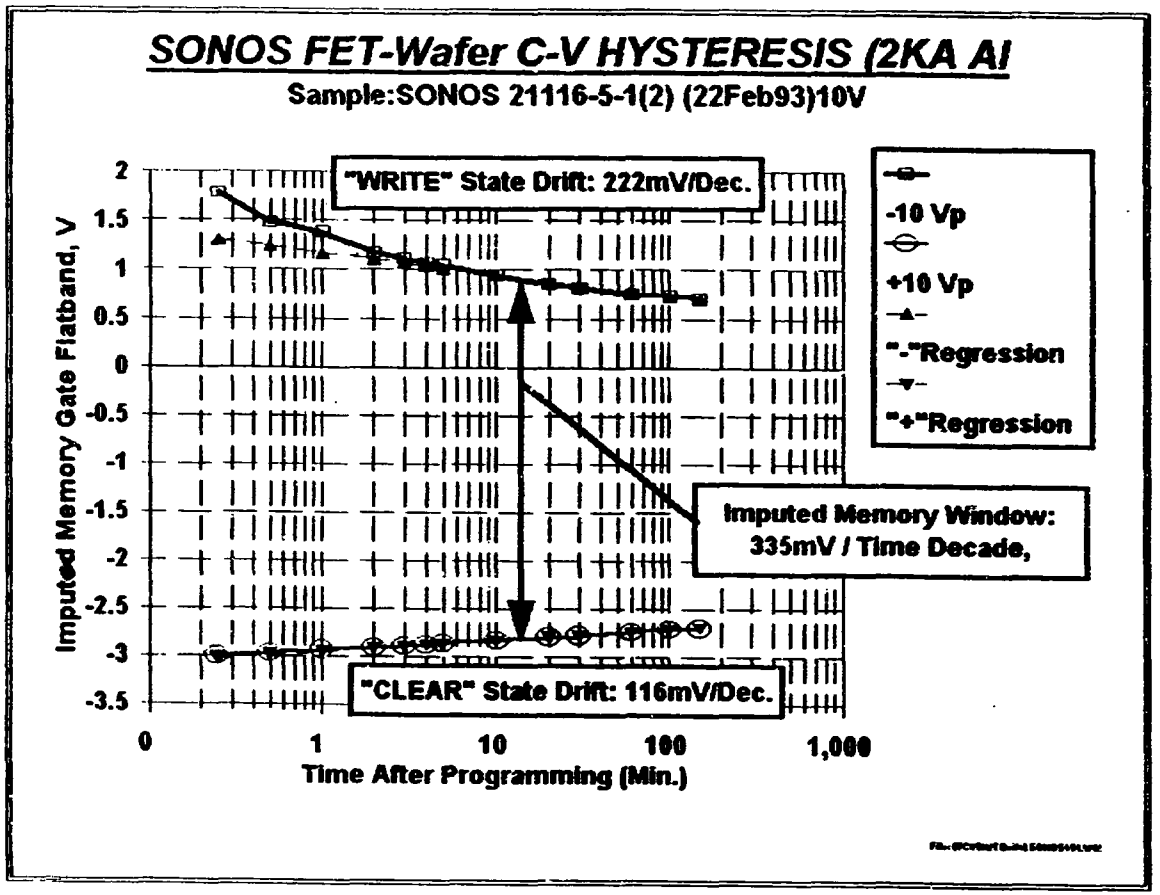


Figure 3-21: Validation of "CV Hysteresis Imputed Memory Window Decay" Using SONOS Lot 21116, Wafer 5.

Laboratories gave a memory window of 1.74 V. ± 0.123 V., with a decay rate of 120 mV/decade of time ± 28 mV/decade of time. The threshold voltages for the time dependent memory window decay are the gate-to-source voltages needed to give a drain-to-source current of 10μA. Substantial previous experience on similar devices show that decay rates from saturated programming invariably exceed those arising from the above programming pulses described in the product data sheets. These observations support the hypothesis that saturated programming gives more charge in shallow traps. Such more weakly bonded charge can be more easily effected; thus resulting in a faster threshold drift when compared to the case of the pulsed programming. The 335 mV/time decade total memory window decay rate shown in Figure 3-21 for saturated programming is certainly consistent with the experimental data and the above hypothesis, too. Indeed, measurements on the same SONOS EEPROM wafer but involving a slightly different memory-FET gate configuration gave a decay rate of nearly 350 mV/time decade (as measured in one laboratory using a semiconductor parameter analyzer, yet only 120 to 140 mV/time decade when measured in another laboratory using dedicated SONOS EEPROM test equipment).

In conclusion, the test results described above strongly suggest that retention predictions based on the new CV hysteresis drift technique are indicative of actual device retention measurements using traditional well-documented schemes. Consequently, NDRO NVM retention predictions based on the new CV hysteresis drift technique can be used for statistical process control during ongoing manufacturing as well as for preliminary development of new NVM gate stacks or for modifying existing NVM gate stacks.

3.6.2 Application to Ferroelectric Memory FETs (FEMFETs)

The above novel technique for predicting data retention in

nonvolatile memory transistors, using memory gate-stack CV-dot hysteresis, was developed after recording some early FEMFET retention data for a BMF FEMFET, illustrated in Figure 3-22. Notice that in less than 100 minutes the memory window has decayed to values which would be impractical to use in an actual memory chip. Parallel related evidence, shown in Figure 3-23, further confirms a memory retention problem for the BMF FEMFET gate stack. Based on considerable experience with SONOS, such a rapid memory window decay was not anticipated. In order to correct the problem indicated in Figures 3-22 and 3-23, immediate action was taken in two directions: 1) Identify the cause of the problem; 2) Devise alternatives to work around the problem.

The first and simplest test to help pinpoint the cause of the problem is the experimental measurement of the spontaneous ferroelectric polarization as a function of time, independent of other mechanisms that can affect the memory gate stack. This is most expediently done by the specialized ferroelectric measurement instrument, the "RT66A" by Radiant Technology, Inc. The RT66A can measure ferroelectric capacitors using pulses in much the same way that DRAMs measure data stored on their internal core capacitors. The charge needed to "reset" the spontaneous ferroelectric polarization to a known direction by means of a known pulse is recorded. A small charge value means the ambient spontaneous ferroelectric polarization vector is nearly aligned with the "reset" vector. A large charge value means the ambient spontaneous ferroelectric polarization vector is nearly aligned opposite to the "reset" vector. Since the realignment pulse duration is on the order of microseconds, only the reorientation of the spontaneous ferroelectric polarization vector occurs in that time period. Such mechanisms as "charge tunnelling and trapping" or "mobile charge migration" all take much longer times and often need the assistance of very large applied electric fields and/or

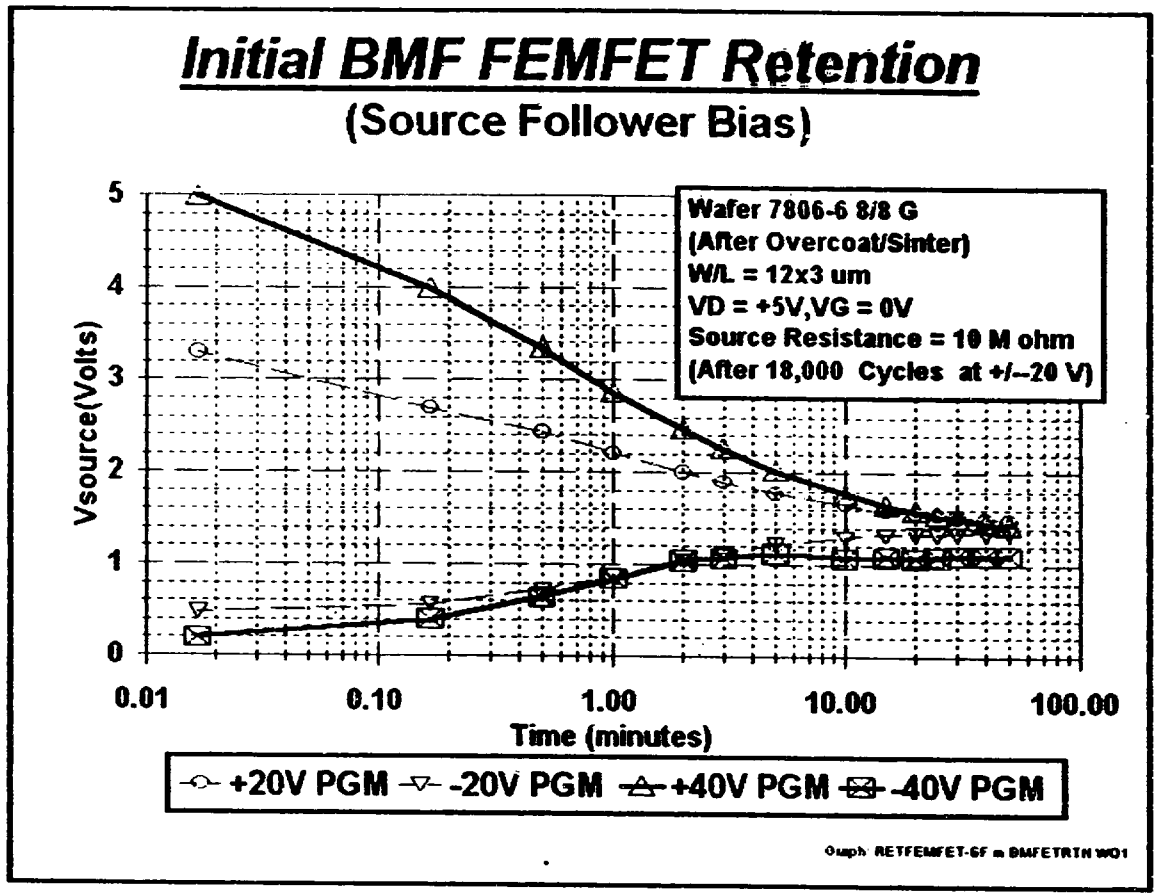


Figure 3-22: BMF FEMFET Retention Measured in Source-Follower Mode.

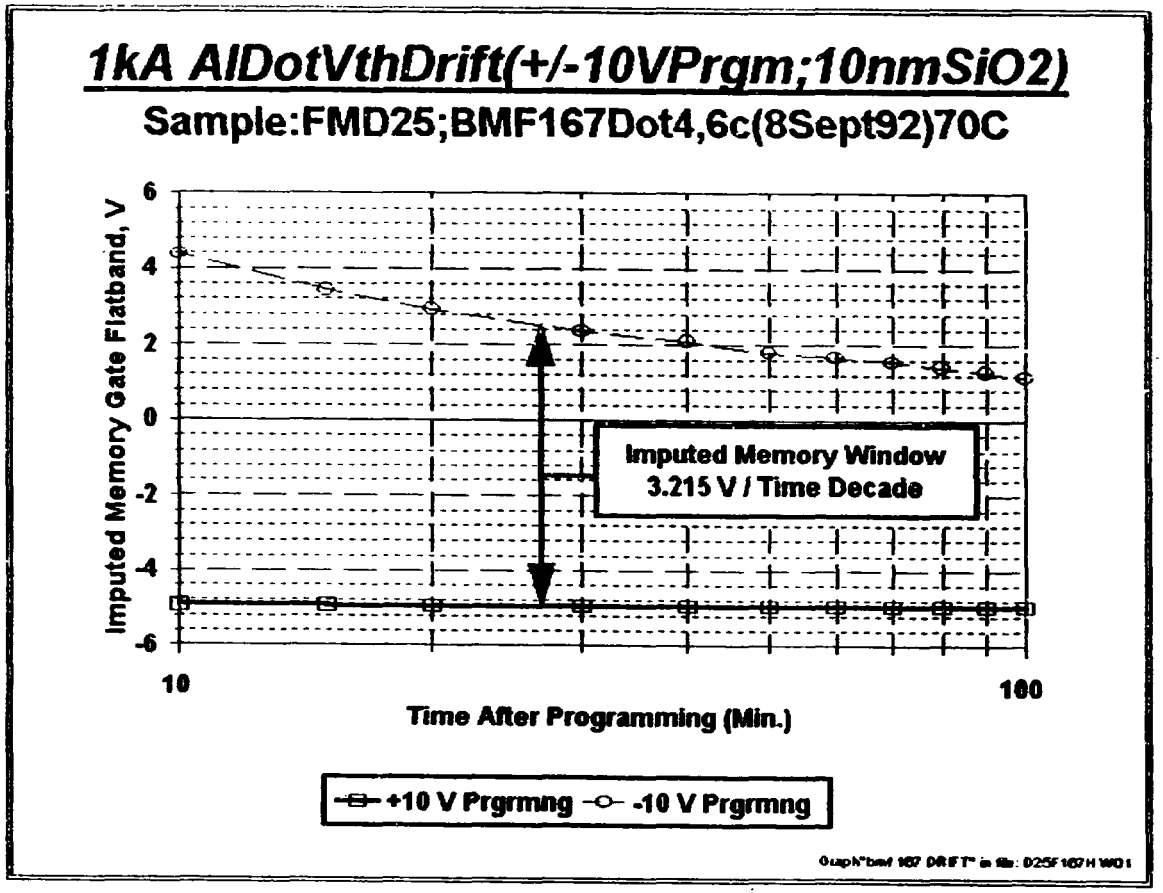


Figure 3-23: Corresponding "CV Dot" Memory Window Decay in the BMF Gate Stack of the BMF FEMFET of Figure 3-22.

elevated temperatures. Results shown in Figure 3-24 were obtained from such a measurement taken on a BMF film. Indeed, the data of Figure 3-24 seem very noisy and are of little value for conclusively identifying the cause of the CV memory window drift. These poor results are probably due to the small polarization achieved for a BMF film on silicon (see the Interim report[1]) under the test conditions, which is beyond the measurement accuracy of the RT66A test equipment.

Meanwhile, alternatives to work around the problem were initiated. The main thrust of the alternatives was to investigate the use of oxide ferroelectrics (starting with bismuth titanate) in lieu of the fluoride ferroelectric BMF.

3.6.3 Initial Oxide-Type Ferroelectric Memory Gate Stack Development

As discussed earlier in this report, ferroelectric memory gate stack structures containing SiO2 buffer layers between the ferroelectric and the semiconductor, are capable of exhibiting more than one type of switching behavior depending on their mode of operation. Thus, as originally demonstrated by Sugibuchi et al[4], tunnel-injection (SONOS) type switching which is confined to low gate operation frequencies can convert to ferroelectric switching at significantly higher frequencies. Similarly, our IRAD studies on such buffered devices revealed a strong dependence of CV hysteresis behavior on the magnitude of the programming voltage.

Figure 3-25 shows typical CV data for an early gate stack structure in which the thickness of the SiO2 buffer layer was 100A, while that of the BTO layer was 5000A. An approximate estimate, based on the bulk values of permittivity for these oxides, suggests that the buffer and ferroelectric layers would have roughly equal capacitances, and that any a.c. voltage applied to the gate would therefore divide equally

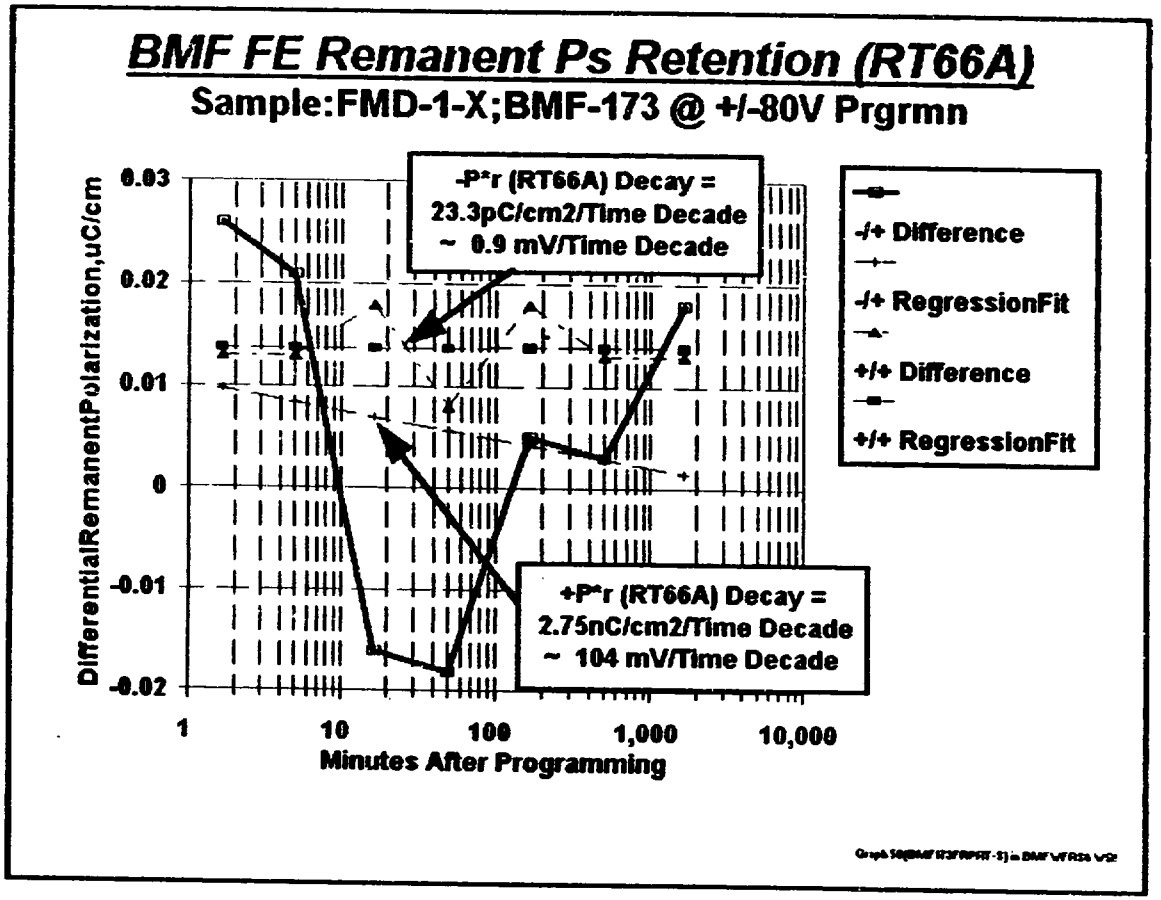


Figure 3-24: Remanent Ferroelectric P_r Retention of BMF Film Measured on the Radiant Technology RT66A Ferroelectric Test Equipment.

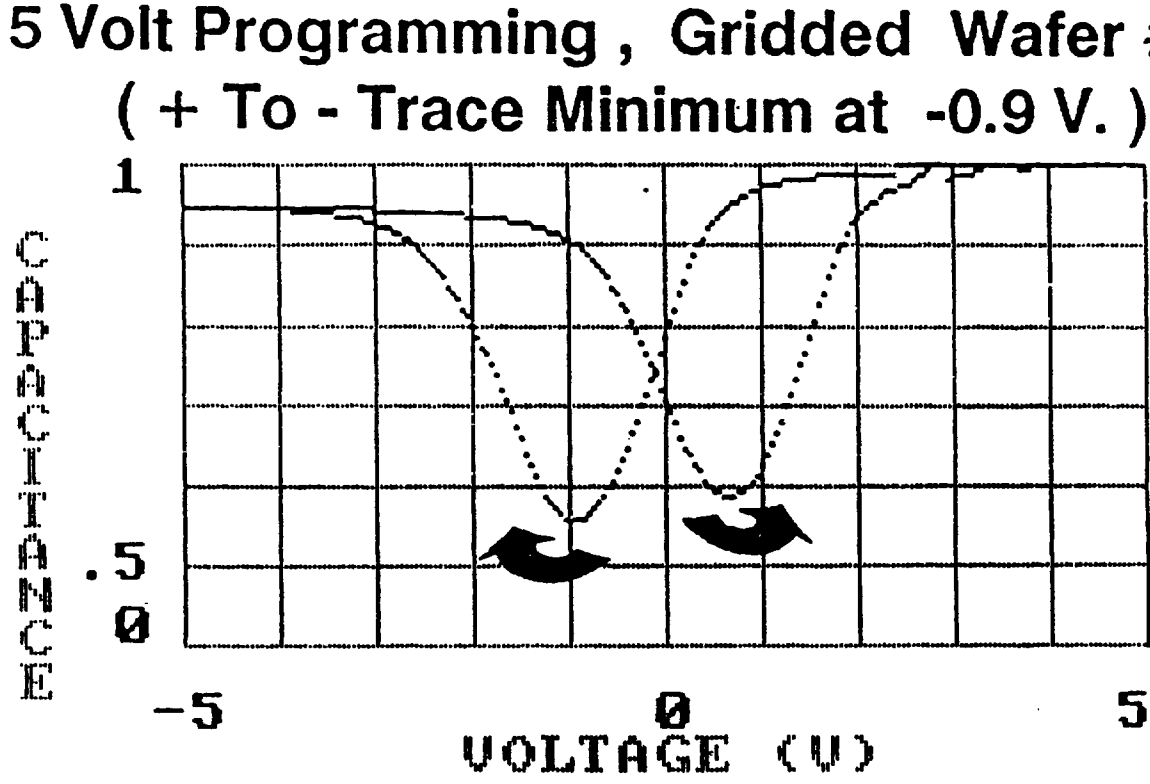


Figure 3-25: Ferroelectric Capacitance Versus Gate Voltage (CV) Hysteresis Results for an SiO_2-Buffered BTO Gate Stack on a Gridded VLSIC CMOS Wafer for $\pm$5V Programming. The Sweep Direction Indicated by Arrows in the Figure is Consistent With a Ferroelectric Mode of Operation.

between the two layers. Figures 3-25 through 3-27 demonstrate that as the gate programming voltage is increased from 5V to 15V, the mode of switching first is dominated by ferroelectric polarization reversal in the ferroelectric, and later by SONOS-type tunnel-injection of charge through the buffer layer. Thus with increasing voltage, the CV memory window decreases from a value of about 0.9V (mainly of ferroelectric origin at 5V programming in Figure 3-25), through approximately zero (when the charge from the two mechanisms compensates in Figure 3-26), to about 0.3V (Figure 3-27) when the SONOS mechanism dominates. Note the reversal of the CV sweep directions indicated by arrows in the figures which is consistent with this interpretation.

The observation of ferroelectric switching at low voltages (corresponding to a field of about 50 kV/cm in the BTO layer), can probably be attributed to the presence of a small amount of low-coercivity, c-oriented component in the BTO film. At a 5V address voltage (corresponding to a field of about 10^6 V/cm in the SiO2) less charge is generated by SONOS-type tunnel-injection, and polarization charge dominates. At higher voltages, the polarization of the small amount of low-coercivity BTO material is probably already saturated, and its charge contribution does not further increase. However, the SONOS charge contribution does increase with higher tunneling field, and now dominates the CV hysteresis behavior.

These results are highly significant, in that they illustrate the feasibility of obtaining ferroelectric memory switching at low power levels required for oxide-type transistor arrays. If the quantity of low-coercivity, c-oriented BTO component could be further enhanced by suitably modified film processing, such films would offer exciting advantages for low-power, high-speed memory systems. In view of the retention problem encountered with BMF in the first phase of

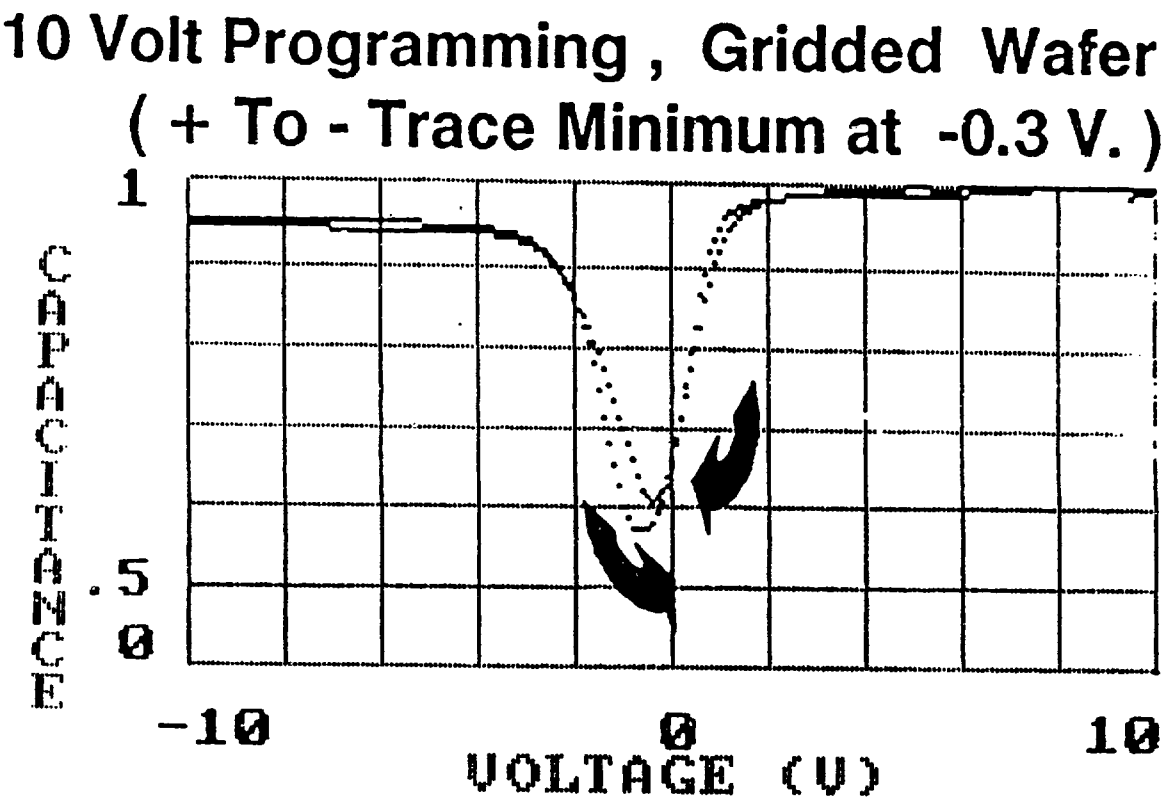


Figure 3-26: The Caption of Figure 3-25 Obtains but for ± 10V Programming. The CV Sweeps Nearly Overlap (Injected Charge is Dominating Ferroelectric Polarization Induced Charge) and the Direction Indicated by Arrows is Opposite from Figure 3-25 and Consistent With a Dominant Charge-Injection Mode of Operation.

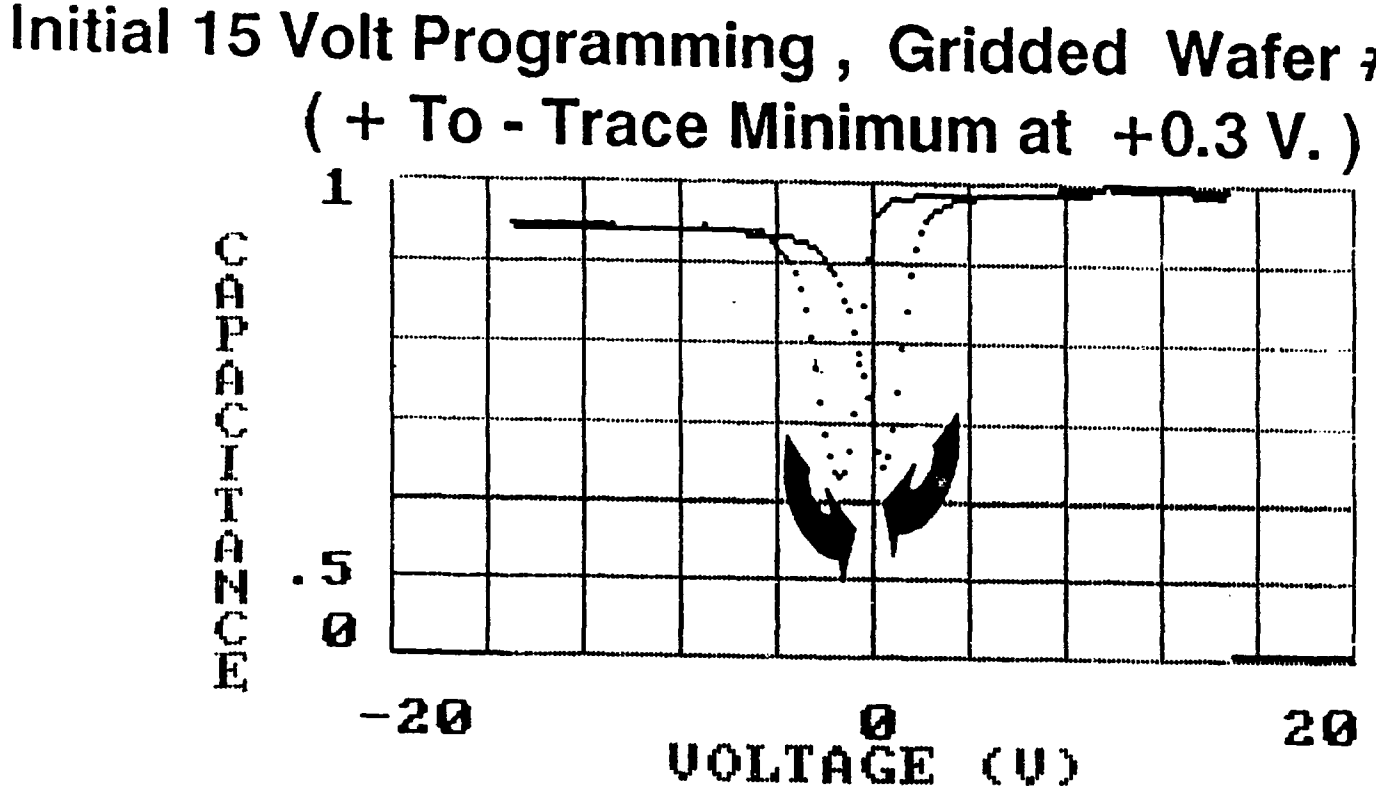


Figure 3-27: The Caption of Figure 3-25 Obtains but for ± 15V Programming. The Sweep Direction Indicated by Arrows in the Figure is Consistent with a Dominant Charge-Injection Mode of Operation.

the program, these results (along with the growing evidence that doped ferroelectric oxides may possess properties far superior to those thus far obtained with BMF) provided motivation to further consider oxide-type ferroelectrics in a buffered-type gate structure in our search for a stable FEMFET device in the present program.

As was mentioned above, the early buffered ferroelectric gate stack memory results above were obtained prior to the start of the present program on a Westinghouse IRAD effort and have been reproted elsewhere[5]. The BTO films used in these devices were prepared using our PLD apparatus in existance prior to starting the present program, capable of coating small wafer pieces, and BTO deposition conditions already established[30]. In section 3.5 above we described modifications under the present program to our PLD apparatus to allow coating 4-inch wafers compatible with our existing one micron CMOS VLSIC fabrication. The next step in qualifying the scaled PLD process for wafer scale FEMFET device fabrication was to examine the uniformity of CV memory windows obtained for buffered ferroelectric oxide gate stacks fabricated across a 4-inch wafer. Figure 3-28 shows the good results obtained. At the right in the figure is a schetch of a wafer and map of the array of memory gate stacks (Al top electrodes) tested. In this case the wafer was stationary (no rotation) and solid curved lines on the wafer sketch indicate interference fringes due to thickness variation across the wafer. Memory windows measured for each dot indicated on the map were determined from CV measurements and plotted in the bar graph in the figure. A reasonably uniform 2V memory window across the wafer was obtained for 5V programming, which was determined to be acceptable for use in device fabrications required for the program.

3.6.4 Oxide Ferrolectric Memory Gate Stack Continuing Developmencs

CV Memory Windows for 5Volt Programming

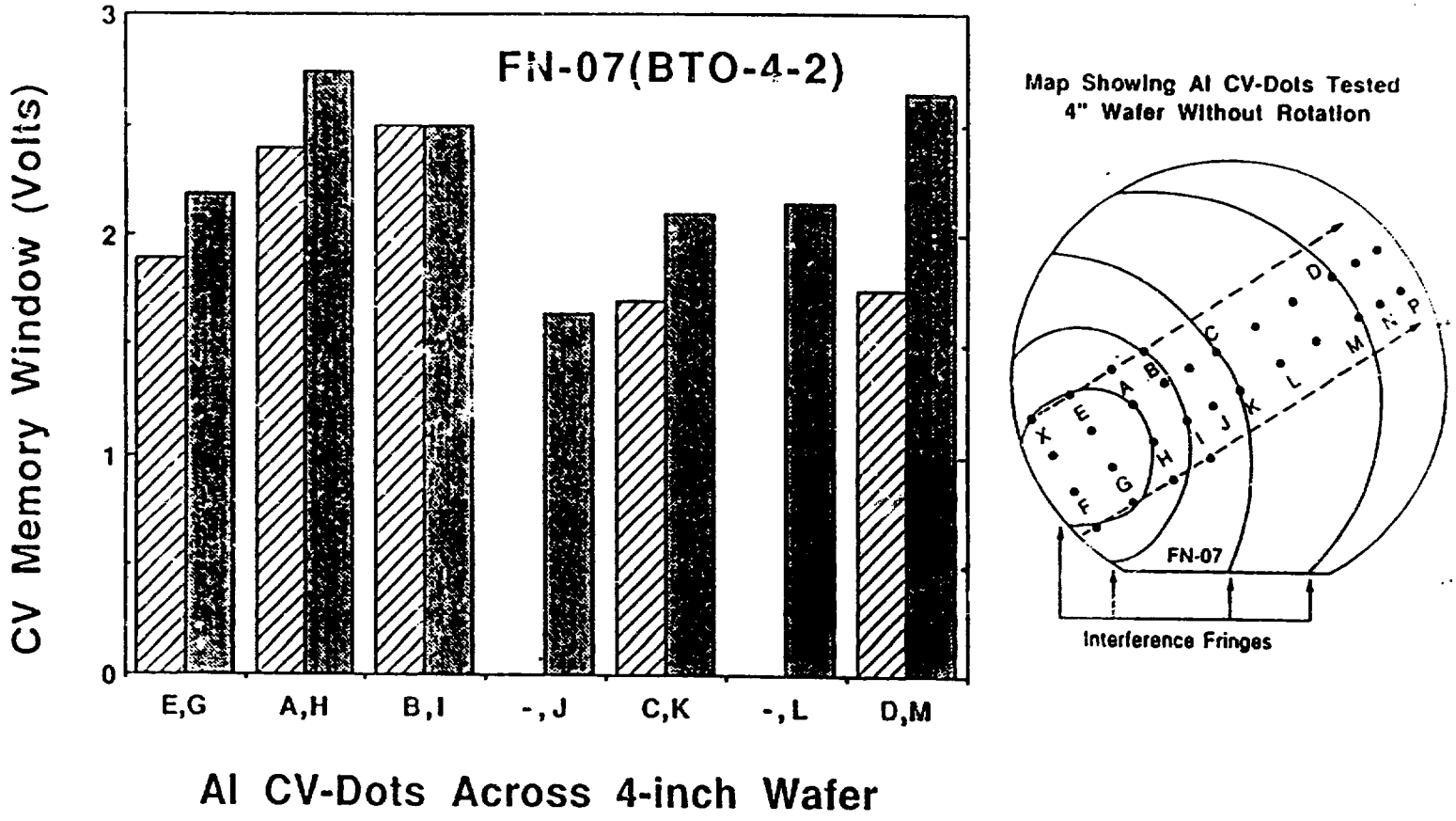


Figure 3-28: Uniformity of CV Memory Windows for a BTO (Deposited Using Our Scaled PLD Apparatus) Gate Stack Measured Across a 4-Inch Wafer as Indicated in the Insert at the Right in the Figure.

Before discussing our approach to reducing or eliminating mobile charge drift effects, it is useful to consider how the data obtained from the CV hysteresis drift (retention loss) technique may be influenced by the mechanisms of charge generation and migration. First, consider the ideal situation where the charge modulated during ferroelectric switching is sufficient to cycle the semiconductor surface between states of complete accumulation ('0') and deep depletion ('1'). Further, assume that there is no mobile ion drift, but that retention loss occurs only through reductions in stored polarization (Pr). If the ferroelectric hysteresis is symmetrical, i.e. not distorted by depolarization or stress-induced piezoelectric field effects, then the threshold values ('0' and '1' states) in the CV hysteresis plots should converge symmetrically with time, with equal or opposite slopes. Next, suppose that no decay in P_r occurs, but that retention loss is due solely to positive mobile ion effects (cf. Figure 3-18). In this case, only the positive threshold voltage (corresponding to enhancement for an N-channel MISFET) is affected, and is driven negatively towards depletion. The negative threshold voltage should be unaffected. This type of behaviour is in fact observed in most of the CV drift data obtained for BTO devices, and appears to confirm our mobile ion hypothesis. Deviations from this behavior may probably be explained on the basis that polarization decay may also occur in some cases, or that the initial programming state was not fully saturated.

Because of our experience with the BMF FEMFETs, we started using the CV hysteresis drift analysis technique (developed on this contract) to predict and monitor memory retention as soon as the method had been validated. Indeed, the memory threshold drift shown in Figure 3-20 is truly the earliest result for one of our initial BTO FEMFET gate stacks. The data clearly suggest that particular gate stack was not likely to achieve a retention of 10,000 minutes.

Furthermore, the hypothesis pictured in Figure 3-18, where the mobile charges are likely to be oxygen vacancies, surely obtains for the case of oxide ferroelectrics in the FEMFETs. Indeed, upon seeing the evidence of mobile charge as presented in Figure 3-20, a search for reducing or eliminating that mobile charge problem in oxide based ferroelectrics was initiated.

The first steps involved reviewing our previous considerable ferroelectric experience as well as discussions with our consultants, including Drs. Francombe, Krupanidhi, and Don Smyth (of Lehigh). The overwhelming consensus involved a multi-pronged approach: The first approach was to focus on reducing the number of oxygen vacancies by eliminating any "reducing environment" exposure of the ferroelectric film itself. An example of that is the following: In the previous section we showed how a suitably chosen sandwich of silicon oxide plus silicon nitride between the silicon and the oxide-type ferroelectric is needed to eliminate the "tunnelling-trapping" mechanism which opposes the FET threshold settings by the ferroelectric polarization. The silicon nitride layer, however, incorporates large quantities of hydrogen ions, potentially capable of reducing part of the ferroelectric in intimate contactact with that silicon nitride layer. For this situation, the corrective action consisted of thoroughly oxidizing the silicon nitride layer before depositing the ferroelectric upon it. Other steps were taken to reduce the numbers of oxygen vacancies, such as annealing the ferroelectric films in oxygen atmospheres.

The second main approach for eliminating mobile charges was the use of specific dopings in the ferroelectric materials themselves. Two candidate dopants were lanthanum and niobium, based on their well documented behavior of holding/entrapping oxygen ions in the crystal lattice.[20-23] The third main approach for eliminating mobile charges was

the use of other oxide ferroelectrics which may be less susceptible to incorporating mobile charges. Some examples of materials other than BTO that were tried included PZT and lead germanate. The results of these various experiments are now presented. Eliminating any "reducing environment" exposure of the ferroelectric film itself became the standard routine.

Lanthanum-doped bismuth titanate (LBTO) was first to be tried. Some of the early favorable results are shown in Figure 3-29, where the lanthanum doping reduces mobile charge effects significantly. From the figure one can see that an initial memory window of 1.25V decays quickly in 20 minutes and then the memory window decays slowly at a rate of 25 mV/ time decade. With niobium-doped BTO (NBTO) a large initial memory CV window was achieved; however, the decay rate (Figure 3-30) of 349 mV / time decade was faster than for LBTO

Meanwhile, efforts were made to discriminate between the effects of the mobile charges and the decay of the ferroelectric spontaneous polarization, P_s. This is illustrated in the combination of Figures 3-31 and 3-32. These two figures show the decay of the memory window from two different points of view: That of Figure 3-31 represents the FEMFET, and shows the total window decay as the combination of both the ferroelectric remanent polarization, P_r, and the mobile charge. That of Figure 3-32 represents the ferroelectric capacitor, and shows only the window decay arising from the ferroelectric remanent polarization, P_r, relaxation but not the much slower motion of the mobile charge. The latter was explained in section 3.6.2 in connection with Figure 3-24. The same Nb-doped BTO (NBTO) film measured both ways gave results of 146mV/time decade for the ferroelectric remanent polarization, P_s, as measured by the RT6A "for capacitors only", with microsecond type

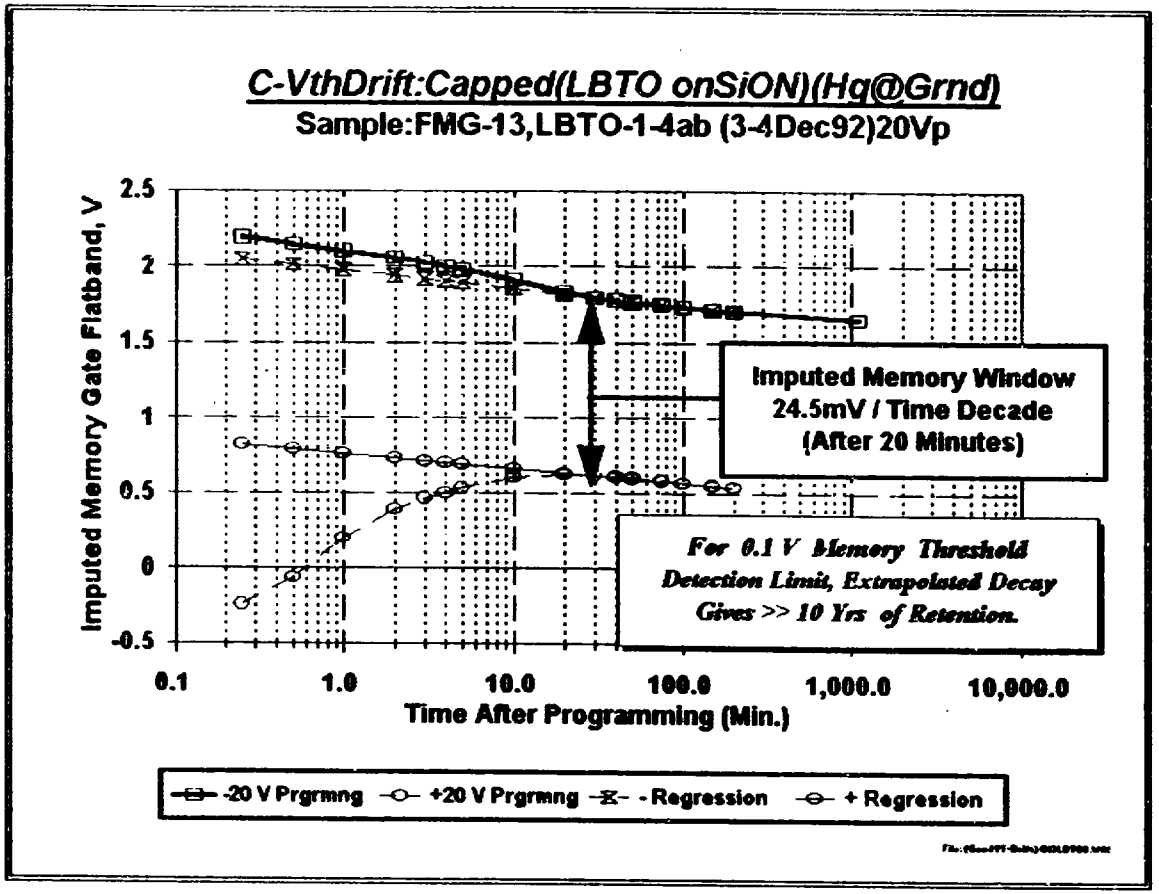


Figure 3-29: CV Memory Window Decay (Extrapolated >>10 Years Retention) for a Gate Stack with a Lanthanum-Doped BTO (LBTO) Layer and Mercury Top Electrode. Lanthanum Doping Significantly Reduces the Effects of Mobile Charge Relative to Undoped BTO.

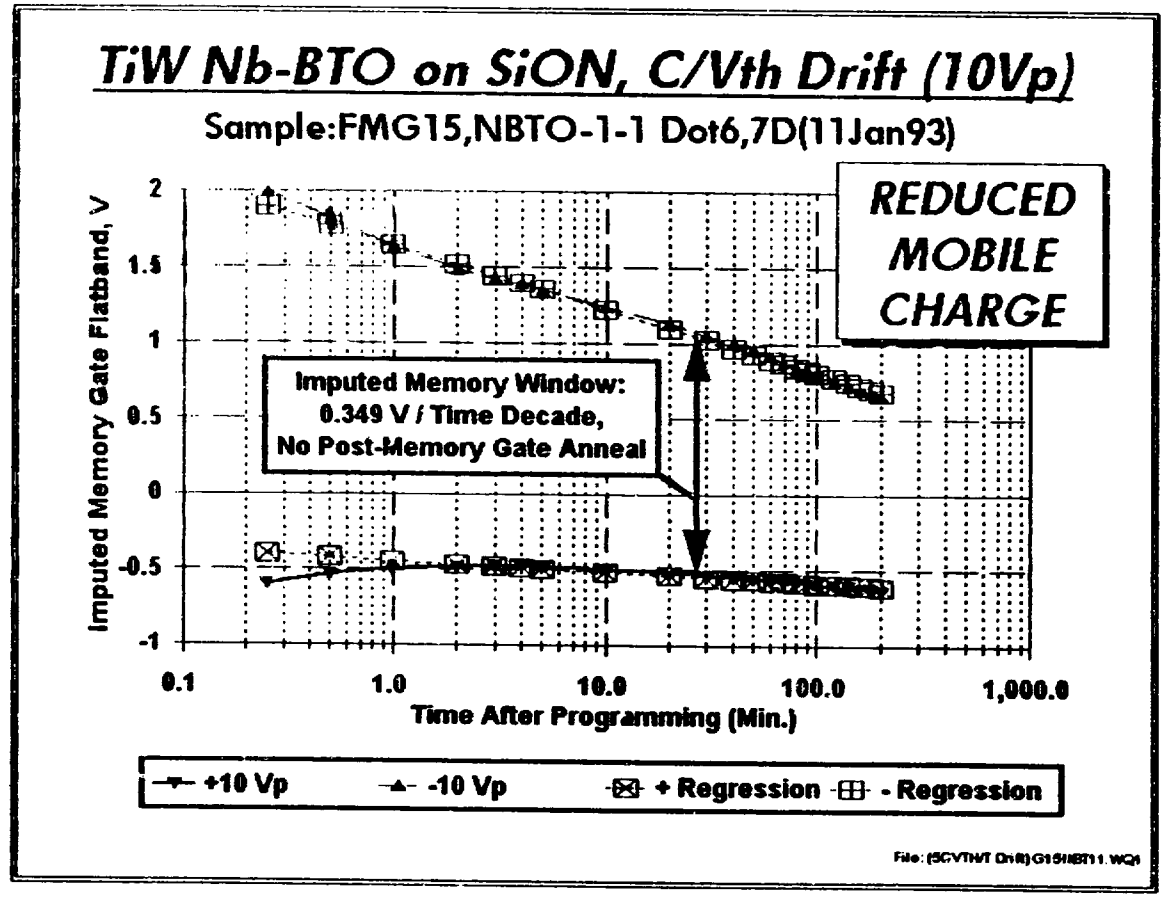


Figure 3-30: CV Memory Window Decay (0.349 V/Time Decade) for a Gate Stack with a Niobium-Doped BTO (NBTO) Layer and TiW Top Electrode. Niobium Doping Yields x1000 the Retention Time Compared to Undoped BTO Gates with Al Top Electrodes (see Figure 3-20).

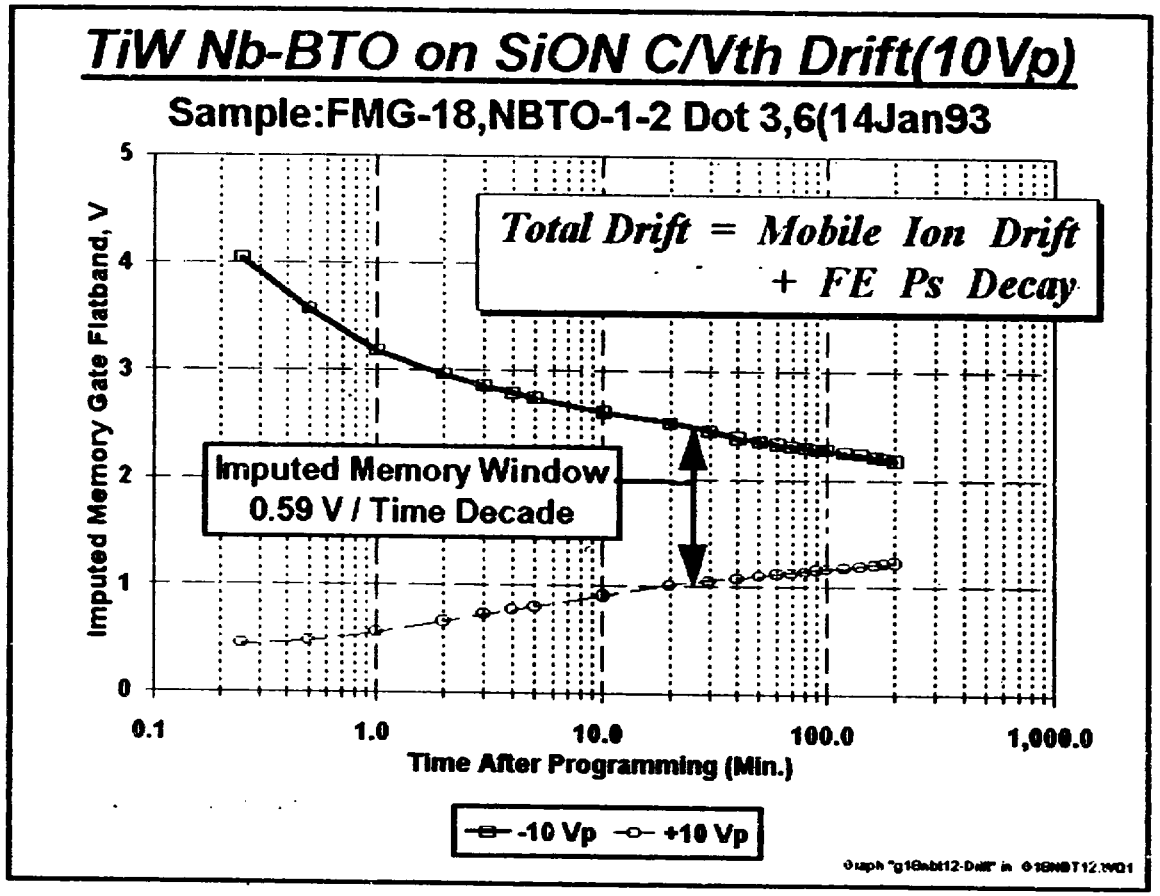


Figure 3-31: CV Memory Window Decay of Niobium-Doped BTO (NBTO) Gate With a Fast Decay Rate (0.59V/Time Decade) Used to Evaluate the Relative Contributions of Mobile Ion Drift and Ferroelectric Remanent Polarization P_r Decay (See Figure 3-32).

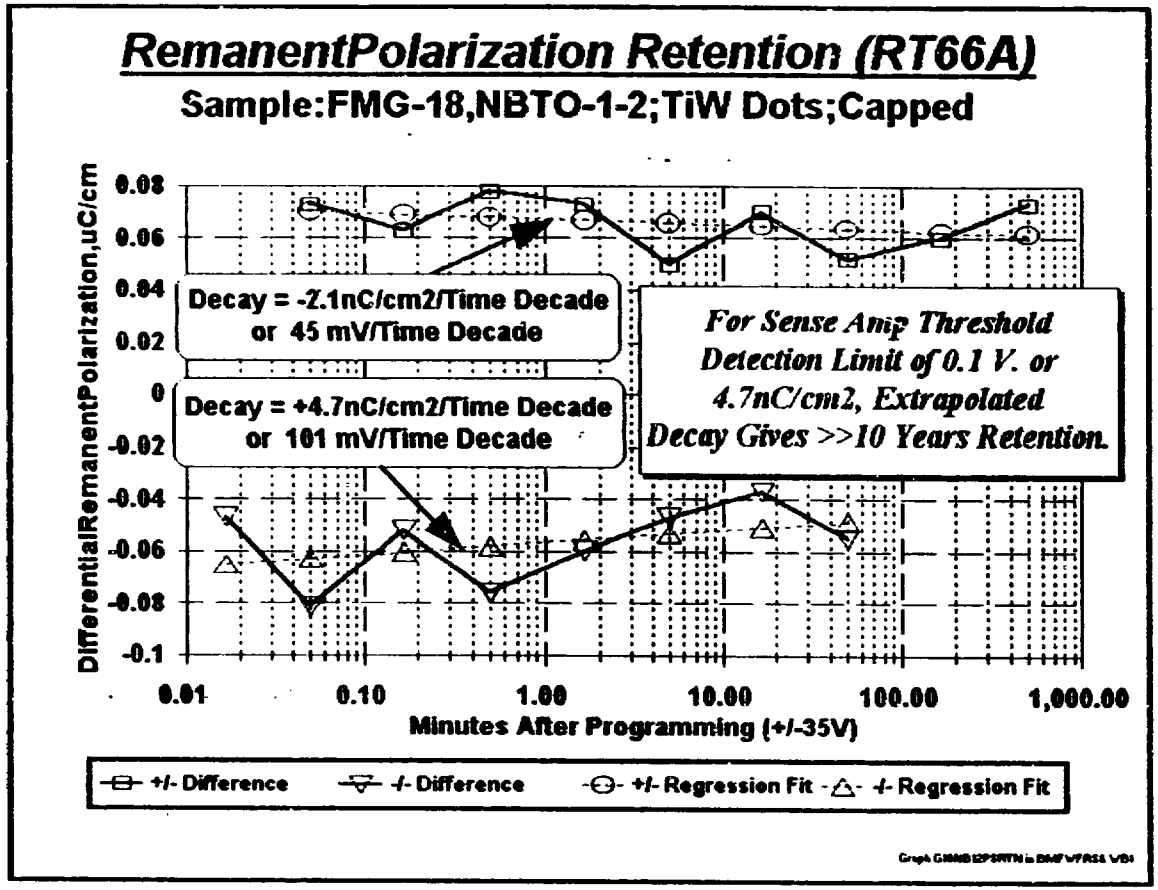


Figure 3-32: Independent Measurement, Using the Radiant Technology RT66A Ferroelectric Polarization Test Equipment, of the Remanent Polarization Decay Rate (Extrapolated >> 10 Years) of the Same Sample of Figure 3-31. Niobium-Doped BTO (NBTO) Shows Good P_r Retention.

switching times, but 590mV/time decade when the effects of mobile charge were included. Indeed, the results of Figure 3-32 show a retention time >> ten years for the capacitor, if the sense amp has a detection limit of 0.1Volt or 4.7nC/cm^2. Thus, even a partial elimination of mobile charges to reduce the decay rate to the neighborhood of 250mV/time decade would yield a reliable memory product usable for numerous applications.

In parallel with the above experiments, investigations of other ferroelectric materials were going on. Figure 3-33 shows the decay rate for an early undoped lead zirconate titanate (PZT) FEMFET gate stack suggesting good retention and considerable promise for subsequent development.

Switching speed was expected to be dependent on the dopant as well as other fabrication parameters based on both our previous experience and advice from consultants. Dr. S. B. Krupanidhi, at Penn State, made numerous switching speed measurements on many samples of memory stacks fabricated on this program. Figure 3-34 illustrates typical switching speed measurements as recorded on a BMF memory stack. Dr. S. B. Krupanidhi's measurements on representative samples of the oxide ferroelectric memory stacks, given in Figure 3-35, show the incorporation of either lanthanum or niobium has the effect of increasing the switching time over the undoped bismuth titanate, while undoped PZT has the fastest switching speed.

3.7 8K FERRAM Test Vehicle

An 8K FERRAM Test Vehicle was created for evaluation of FEMFET baseline process integrity. This test vehicle was created by modifying an existing 4 um test vehicle from a Westinghouse/Sandia National Laboratories 8K EEPROM program. This program employed a SONOS (Silicon Oxide Nitride Oxide

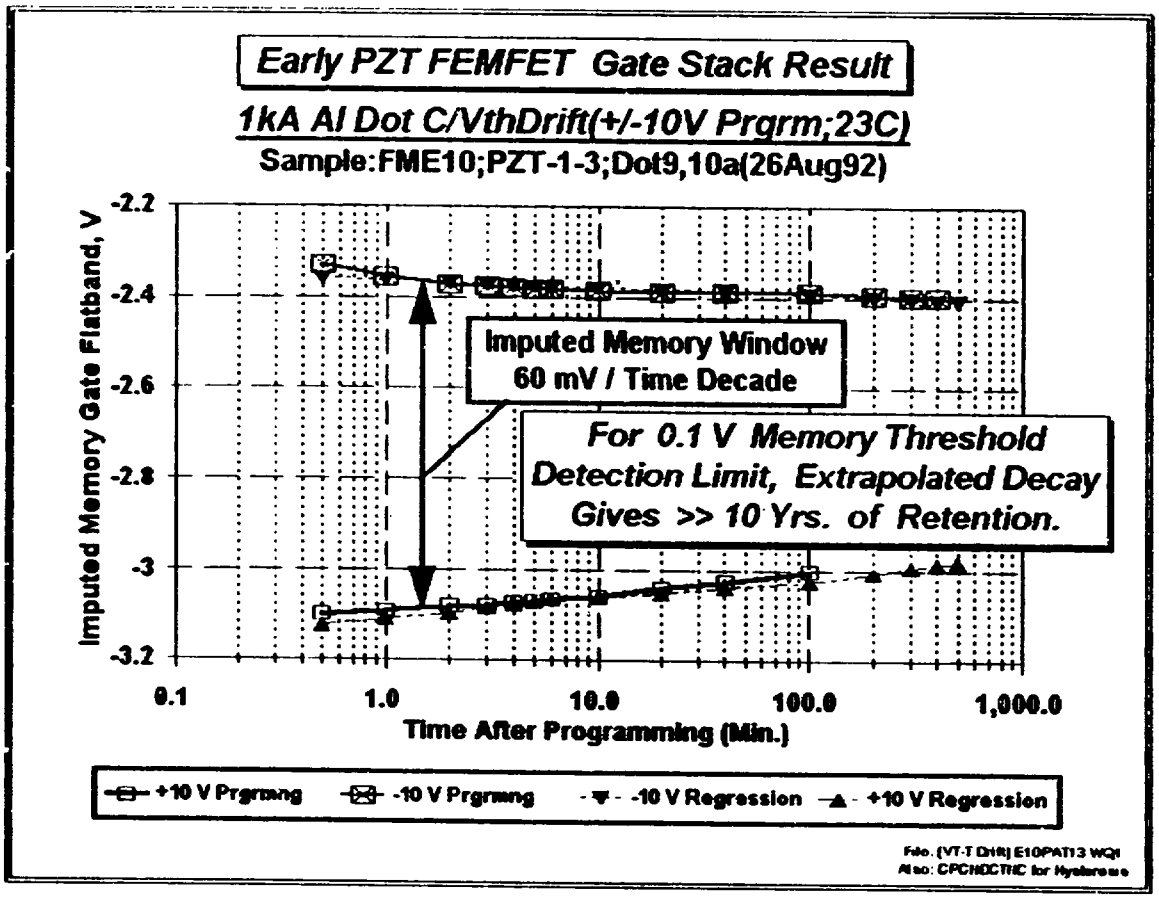


Figure 3-33: CV Memory Window Decay (Extrapolated >> 10 Years Retention) for a Gate Stack with a Lead Zirconate Titanate (PZT) Layer and Al Top Electrode. Undoped PZT Shows Significantly Reduced Mobile Charge Effects and Good Retention.

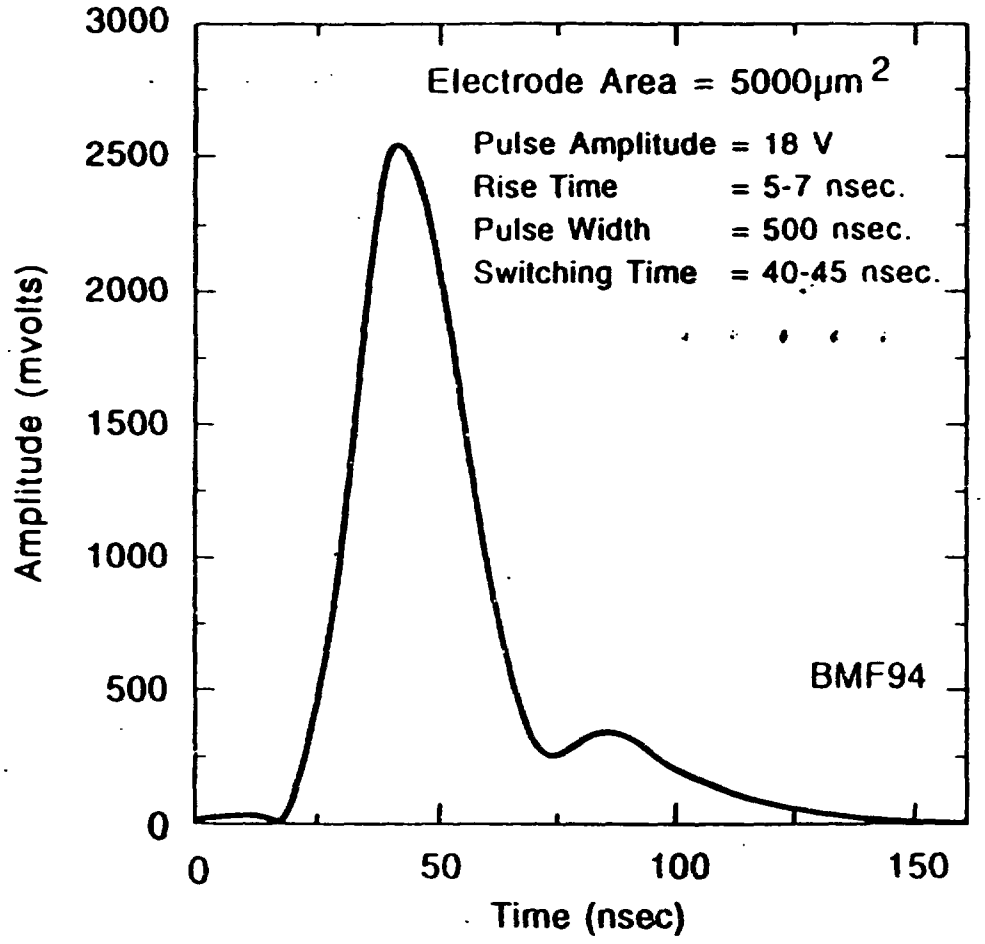


Figure 3-34: Example High-Speed (Pulsed) Polarization Reversal Switching Measurement for a BMF Memory Stack (Measured by Professor Krupanidhi, Penn State University).

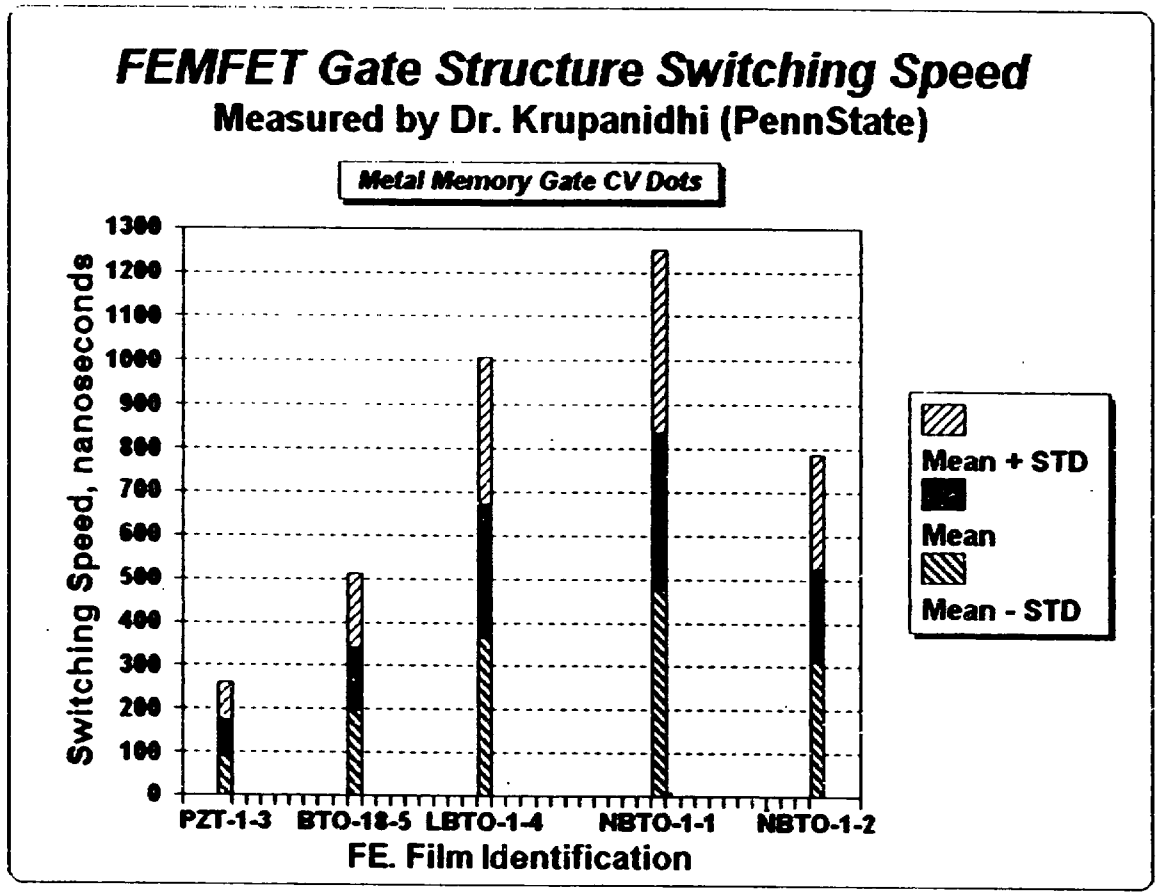


Figure 3-35: Comparison of Switching Speeds (Measured by Professor Krupanidhi, Penn State University) for BTO (Doped and Undoped) and PZT.

Semiconductor) nonvolatile memory transistor approach. The Westinghouse FEMFET baseline process was designed to be compatible with this SONOS technology.

A detailed description of the 8K FERRAM Test Vehicle is included in Appendix C. Included in this description are:

- Mask design rules
- FEMFET cross section
- Mask polarity information
- Mask alignment sequence/tolerances
- Wafer map
- Test structure description/probe pad information
- Plots of test structures

1X projection print photolithography was used for the FEMFET process. This allowed multiple devices to be placed on each FEMFET wafer. The 8K FERRAM Test Vehicle maskset was comprised of the following devices:

Device	# per wafer
- 8K FERRAM EEPROM	62
- WEC Process Test Pattern	56
- SNL Process Test Pattern	56
- SNL Self Stress Test Pattern	06
Total die =	180

This maskset featured a full complement of test structures for evaluation of the process integrity of the FEMFET process. These test structures addressed such issues as performance, reliability, producibility, radiation hardness, and uniformity of the baseline technology. The key test structures were:

- CMOS transistors of varying widths and lengths

- FEMFET transistors of varying widths and lengths
- Gated diodes
- Metal contact structures
- Sheet resistivity test structures
- Field parasitic MOSFETs
- Area capacitors
- SCR test structures

The 8K FERRAM was designed using a four transistor memory cell. Each memory cell has two FEMFET memory transistors and two NMOS access transistors. The dual memory transistor approach results in a much more robust design and is commonly used in military nonvolatile memory applications. Differential sense amplifiers are used which can detect differences in memory transistor threshold voltages as small as 50 mV. Figure 3-36 shows a diagram of the FERRAM memory cell. This cell has dimensions of 40 um x 60 um. Design rules were selected to maximize the producibility of the FEMFET. The general approach selected was to make design rules as conservative as possible to allow for flexibility in processing. This approach allowed a wider tolerance for wet versus dry chemistry processing. The resulting memory cell could then be used as a demonstration vehicle for a wide range of ferroelectric materials. The plan for this program was to demonstrate a FEMFET process suitable for military nonvolatile memory applications. Upon successful completion of this task, design rules would be evolved to allow for high density memories in the future.

Based on a detailed process review, the following changes to the original 4 µm memory cell were instituted which should result in significant improvements in producibility and memory transistor drain breakdown. These changes were:

1. Memory gate metal overlaps all ferroelectric material to allow the baseline VHSIC metal etch to be

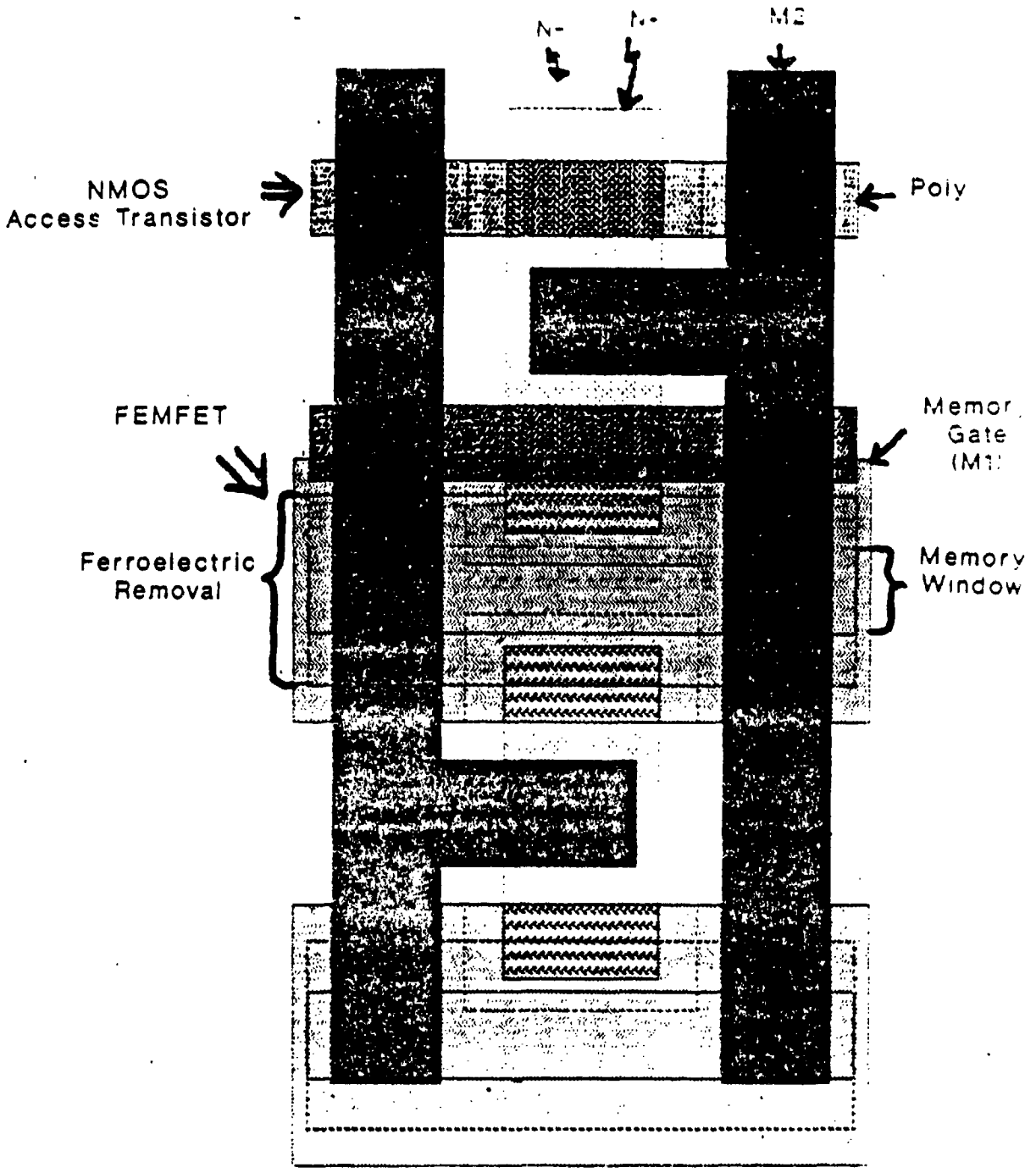


Figure 3-36: 8K FERRAM Memory Cell.

done. By overlapping the ferroelectric memory gate over the ferroelectric stack, the ferroelectric should be completely shielded from attack during the baseline M1 etch. This should avoid some of the more complicated approaches considered for this step. The ferroelectric removal mask overlaps the memory window by 2.7 μm (0.5 μm single misalignment tolerance, 1.0 μm MW etch, 0.25 μm ferroelectric stack etch, plus 0.95 μm safety = 2.7 μm). [This was achieved by reducing the MW overlap of N- extender from 1.7 μm to 1.0 μm.] This is needed to ensure that no bare silicon exists inside the memory window when the memory gate is deposited. In order to guarantee that memory gate (M1) overlaps the ferroelectric stack, a design rule of 1.9 μm was selected for M1 overlap of the stack (0 μm for ferroelectric stack etch, 1.0 μm for 4 misalignment tolerances, plus 0.9 μm safety = 1.9 μm). This results in a minimum M1 spacing of 2.0 μm in the memory array, which is approved for projection printing at Westinghouse ATL.

2. N- extender overlaps N+ extender in all directions to increase memory transistor drain breakdown from roughly 17V to 22-24V. This should allow the FEMFETs to be characterized at 20V. The ferroelectric memory transistors were modified so that the N-extender overlaps the N+ source-drain in all directions by 2.0 μm. (For the Sandia 4 μm design, it presently only overlaps the N+ in the channel region.) This will eliminate breakdown problems associated with the edge of the N+ drains. This change increases the FEMFET effective width from 8.0 to 12.0 μm. This also reduces the N- to P+ guardband space from 8.0 to 6.0 μm.

3.7.1 Low Risk Complementary or Differential Data Storage Technique

The Westinghouse two-FEMFET per bit approach, with differential detection, offers a low risk design for enhanced retention and NDRO sensitivity. The two-FEMFET cell corresponding to a bit is shown in Figure 3-37, where the two FEMFETs per bit are used in a complementary fashion to achieve reliable differential writing and sensing. Included in Figure 3-38 is a first metal strap used on the word line to reduce delay and improve speed. After erase/write, one element is in the depletion mode threshold state ($V_t > 0$ for a p-channel device) and the other is in the enhancement mode threshold state ($V_t < 0$ for a p-channel device).

The differential data storage increases the signal input to the sense amplifier and speeds data detection. Figure 3-39 illustrates the differential or complementary NDRO sensing scheme. Typically the nodes used for writing data (BLw and BLw) are used as current sources during the read operation. Only that row in the central memory array activated by the selected word line (WL) can be conductive. Thus, during the read operation, one FEMFET of a pair will be conducting while the other is nonconducting by virtue of the opposite or complementary ferroelectric polarization states within the gate dielectric of the two FEMFETs. The complementary column read nodes (BLr and BLr) are precharged to midway between the power supplies so that the one conducting FEMFET pulls its associated sense amp input column toward that power supply attached to the sources of the FEMFETs. The sense amp shown has cascaded stages with negative feedback to rapidly drive the circuit into saturation. SPICE simulations including approximate models for the memory FETs suggest read cycle times in the range of 50 nsec to 100 nsec.

The differential data storage and sensing of the two FEMFETs per bit assures balanced data sensing and minimizes the effects of prompt dose photocurrents which affect both bit

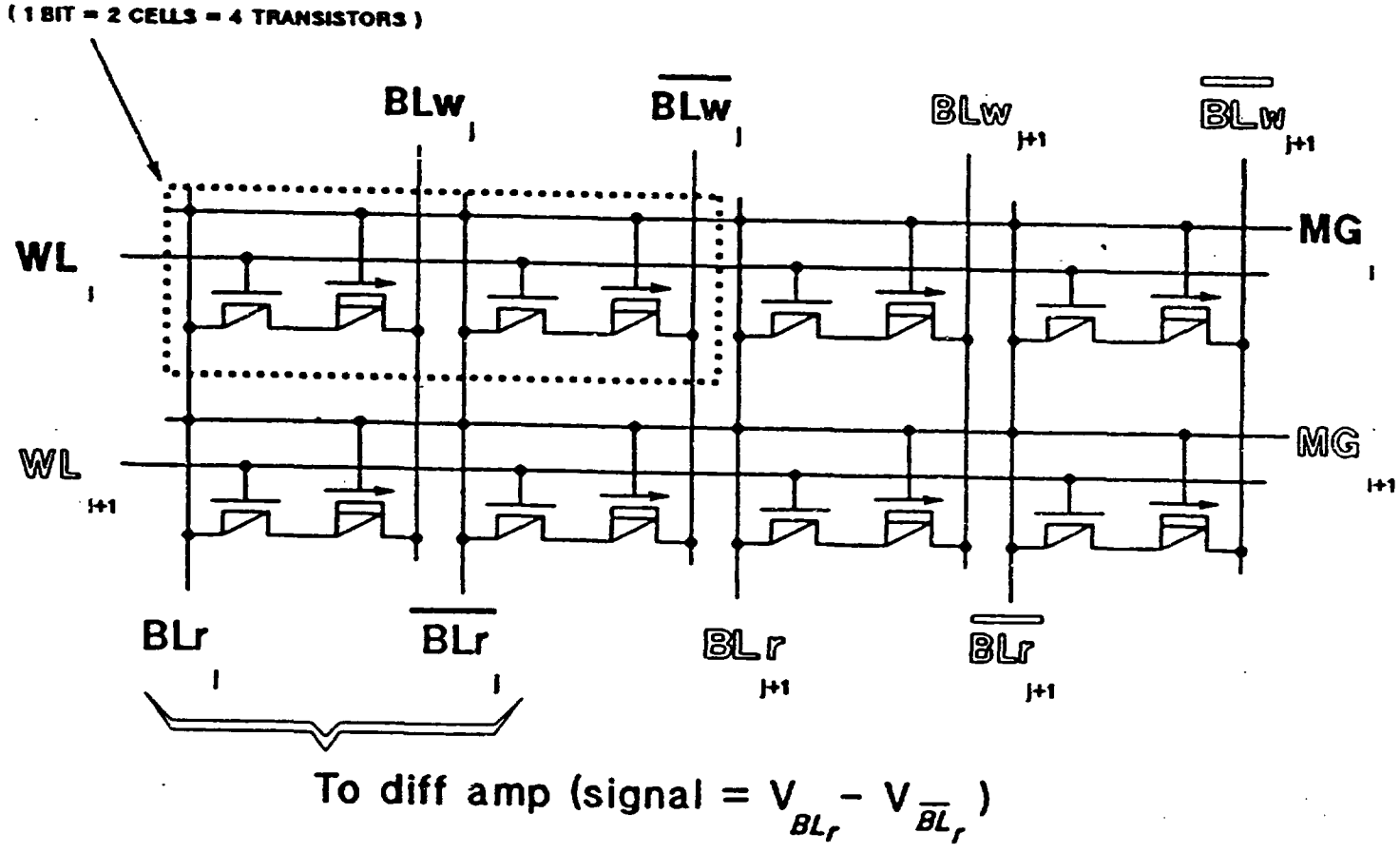


Figure 3-37: Complementary Data Storage Schematic for Central Array.

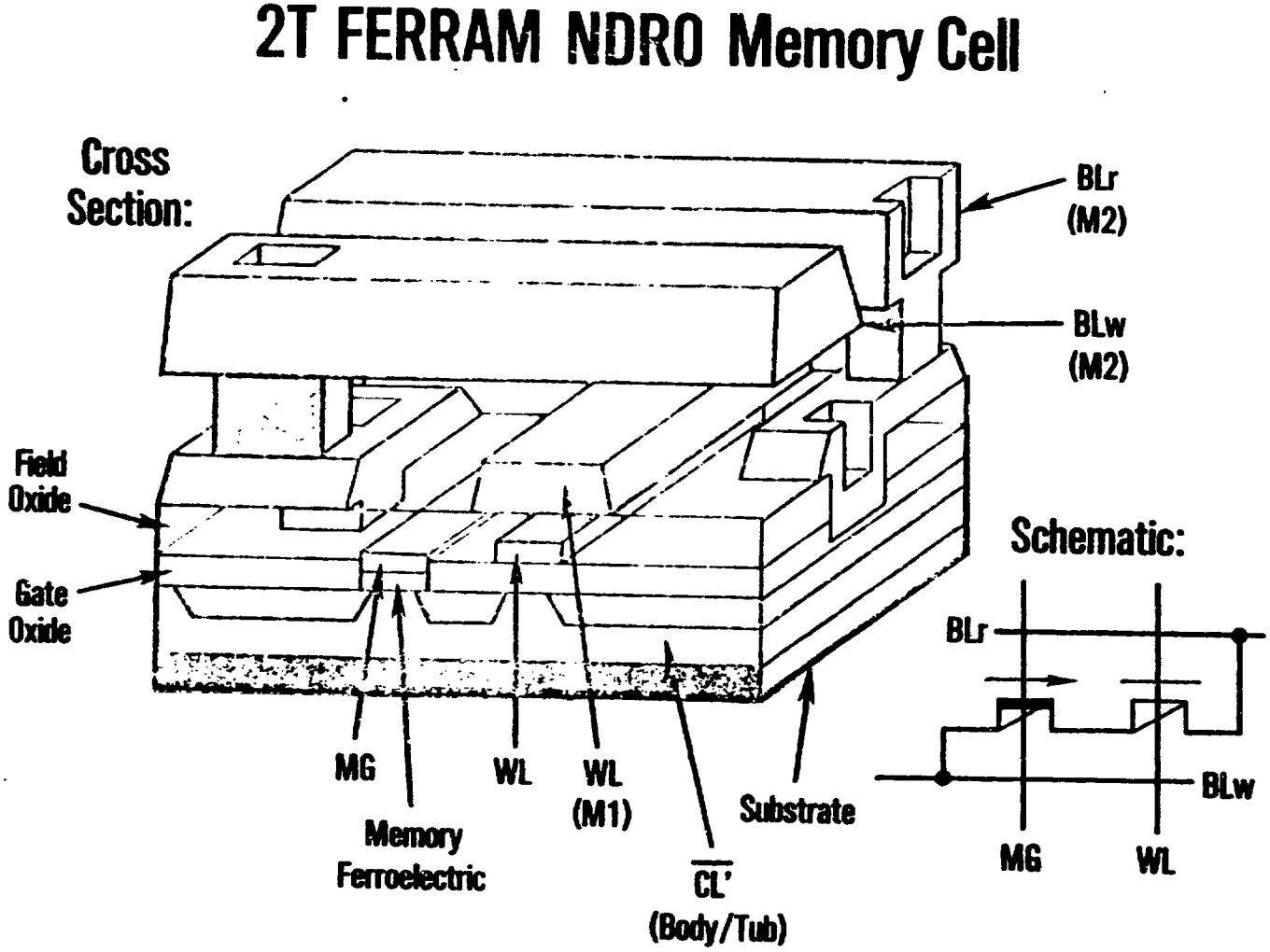


Figure 3-38: A 3-D View of the 2T FERRAM NDRO Memory Cell.

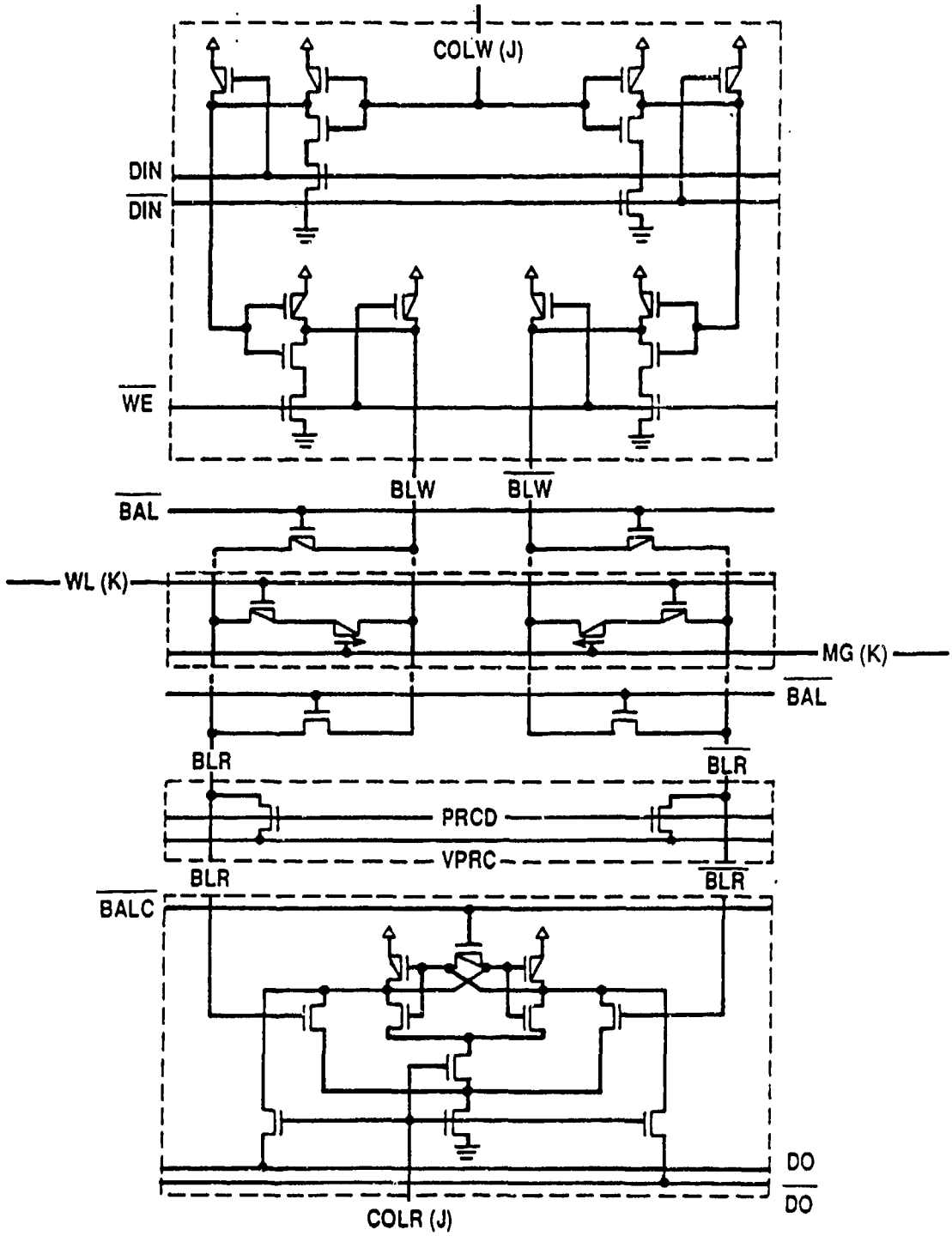


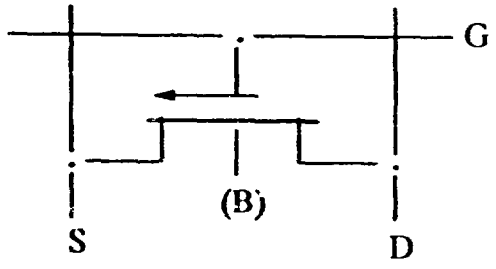
Figure 3-39: High-Speed Complementary / Differential NonDestructive ReadOut (NDRO) Sensing Scheme (Illustrative).

lines equally. These cause a common mode voltage which the differential sense amplifier ignores. The two FEMFETs corresponding to a bit are physically adjacent in the array for best matching so that the only difference between them corresponds to the data stored. This scheme also contributes to good operating margins (noise immunity, tolerance to supply variations, etc.) in much the same way as differential data transmission does in differential line drivers and receivers. Although it is possible, in principal, to store data using one FEMFET per bit, Westinghouse feels the radiation hardened, high reliability applications require a solid proven approach.

3.7.2 CMOS-Compatible Programming of the FERRAM

FEMFET programming modes are well suited to rad hard nonvolatile memory applications and are compatible with the 1-micron CMOS process. In typical NDRO EEPROM applications, all the memory transistors reside in a common well. This configuration provides the best density, and easily accommodates bulk erase/write (all words), page erase/write (a group of words), or single word erase/write. Erasure (to an indeterminate state) is done by pulsing the well to the appropriate voltage (0 volts for a well) while the memory gates are held at the program voltage, V_p (+5 volts for the p-channel case). This places all the selected memory transistors in the same V_t state (depletion mode for a p-channel array). During the write cycle the selected sites are then written with the desired data. In writing, the selected word line is pulsed (to 0 volts for a p-channel), the well and the bit line are at V_p (+5 volts for p-channel), and the memory gate is held at ground. This shifts one of the two FEMFETs to the opposite V_t state (enhancement mode for the p-channel case) while the other inhibits writing by holding the bit line at the memory gate potential ($V_{gs} = 0$). These erase/write modes are presented in Table 3-2.

TABLE 3-2: FEMFET Transistor Programming Modes.



		Column Access: Body and Source/Drain	
		Selected	**Unselected**
Row Access: Memory Gate	Selected	Write (L,H, H) Clear (H, L. L)	Write Inhibit (L, H, L) Clear Inhibit (H, H, L)
	Unselected	Write Inhibit (H, H, H) Clear Inhibit (L, L, L)	Write Inhibit (H, H, L) Clear Inhibit (L, H, L)

FEMFET Bias Key: Mode (VG, VB, VSD) where:

VB = body potential, VG = gate potential, VSD = source and drain potential:
L = low = 0V = ground,
H = high = $+V_p$ = program voltage

For writing, the selected row has MG at 0 volts, while the unselected rows have MG at V_p. The selected column has data applied complementary fashion to the HLw (bit line write) and BLw (bit line write bar) nodes. All unselected columns and one side of the selected column have the source and drain at 0 volts versus V_p for the source/drain of the other side of the selected column. At a selected bit location, one FEMFET structure sees the situation labeled "write inhibit."

Page erase (a group of words), single word erase, and byte erase make use of the clear inhibit mode of the FEMFET transistors where the clear is inhibited by holding the gate line of uncleared words at 0 volts when the well is pulsed to 0 volts so that $V_{gb} = 0$. Cleared words will have $V_{gb} = V_p$. Virtually all these variations have been done in the past by Westinghouse using multiple-dielectric nonvolatile memory FETs with modes comparable to those of Table 3-2.

3.8 Oxide FEMFET Baseline Process Description

Wafer fabrication on this phase of the program used short-loop gridded wafers for ferroelectric capacitor fabrication and fully processed device wafers for FEMFET fabrication. During this program phase, which employed ferroelectric oxide thin film materials, 111 gridded wafers and 15 FEMFET device wafers were fabricated. In addition, a reserve of device wafers were processed up to FEMFET formation and were held pending results from gridded wafer CV tests. Tables summarizing the processing history of gridded and device wafers, prepared during this phase of the program using oxide ferroelectric thin films, are presented in Appendix A.

Gridded wafers consisted of P on P+ starting wafers with an orthogonal grid of 6 um wide N+ diffusions at 100 um spacing. These N+ grids provide a source of minority carriers during electrical testing and result in more accurate evaluation of

ferroelectric film properties. The gridded wafers were used as an effective tool for evaluating suitability of oxide ferroelectric films deposited in a variety of ways for FEMFET fabrication. Ferroelectric dielectrics were first deposited on these gridded wafers for capacitance-voltage (CV) electrical evaluation. These measurements provided a rapid assessment of important ferroelectric properties such as memory window size, position, endurance and retention. Typical throughput time for these wafers was about 1-2 weeks. This allowed for rapid evaluation of various different candidate materials used in fabrication of the gate stack such as: different oxide ferroelectric materials and layer thickness, different buffer layers and deposition methods and layer thickness, post-deposition rapid thermal anneal (RTA) or oven anneal temperature, capping layer deposition methods and layer thickness, top electrode materials and layer thickness.

Upon successful completion of gridded CV tests, ferroelectric films were selected for use on fully processed device wafers. These device wafers were processed with a 4 um dual well CMOS process developed for Sandia National Laboratories for their SONOS 8K EEPROM fabrication. The design rules for that EEPROM formed the basis of the design rules for the 6083 8K FERRAM test vehicle and are given in Table 3-3. The Sandia EEPROM SONOS process was modified such that the FEMFET transistor would replace the SONOS memory transistor in this design. A baseline process was selected at the beginning of the program with the following objectives:

- minimization of high temperature operations
- processes compatible with VLSI double metal processing
- processes must not risk fab line contamination
- design rules compatible with dry or wet chemistry

The FEMFET baseline process cross section and sequential

TABLE 3-3: Design Rules for the 6083 8K NDRO FERRAM ICAL Test Vehicle.

Level		Design Rule	
#	Name	Feature / Item	Value, μm
7	N-	+ Overlap of memory gate/M1	> 0.7
		+ Minimum space (channel length)	> 2.6
8	N+	+ Space to MG/M1	> 1
10	Contact	+ Minimum contact	3 x 3 (2.5 x 2.5 on Mask)
		+ Space to memory window	> 4
11	Memory Window	+ Overlap of MG/M1	> 1
12	Ferroelectric Removal	+ Overlap of M W	> 2
13	Memory Gate/M1 (MG/M1)	+Minimum width	4 (5.6 on mask)
		+ Minimum space	4 (2.4 on Mask)
		+ Overlap of Contact	0.5 (1.55 on Mask)
14	Via	+ Minimum via	3 x 3 (2.5 x 2.5 on Mask)
15	M2	+ Minimum width	4 (5.6 on mask)
		+ Minimum space	4 (2.4 on mask)
		+ Overlap of via	0.5 (1.55 on masks)

process steps are shown in Figure 3-40 and Table 3-4. The ferroelectric memory transistor steps are highlighted in bold text in the table. The key process elements for FEMFET transistor fabrication involve:

- memory window formation
- ferroelectric deposition and etch
- memory gate deposition and etch

Figure 3-41 is a photograph of a 4-inch diameter wafer containing the multiple test chips comprising the 8K FERRAM test vehicle described in section 3.7 above and in Appendix C. The photograph was taken after the ferroelectric BTO layer deposition step, using the scaled pulsed laser deposition method (PLD) described in section 3.5 above, and before etching the ferroelectric BTO layer using the processes described below.

FEMFET processing was incorporated as the last processing steps prior to first metallization in order to minimize the number of high temperature cycles to which the ferroelectric material was exposed. The FERRAM process adds two additional masks to a conventional CMOS process in order to define FEMFET memory transistors. Since two additional masks are also required to make SONOS memory devices, both technologies require 16 masks.

A series of unit semiconductor compatible process development experiments were conducted to optimize the processes selected for FEMFET fabrication. A memory window process was identified which allowed this window to be reflowed along with the normal contact window reflow. This approach resulted in a near ideal contour of the FEMFET memory window, eliminating any subsequent concerns about metal step coverage. Figure 3-42 is an SEM of the reflowed memory

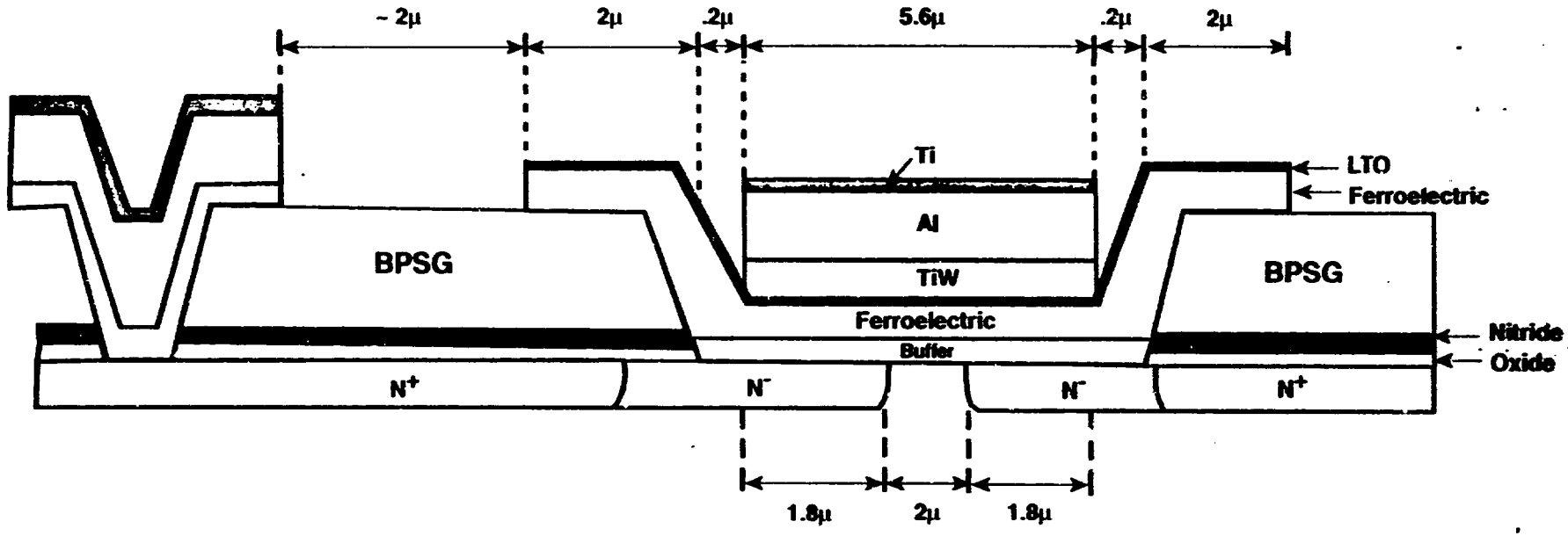


Figure 3-40: Cross-Section Westinghouse FEMFET Fabrication Process.

TABLE 3-4: FEMFET Baseline Fabrication Process.

Step #	Fabrication Process	Step #	Fabrication Process
1	Wafer issue	42	Phos. implant
2	Laser oxide	43	Resist strip
3	Laser #	44	N+ photo (8)
4	Strip oxide	45	Phos. implant
5	Pad oxide	46	Resist strip
6	Alignment photo (0)	47	P+ photo (9)
7	Oxide/silicon etch	48	Boron implant
8	Strip oxide	49	Resist strip
9	Pad oxide	50	Reoxidation
10	N-well photo (1)	51	Nitride dep.
11	Phos. implant	52	BFSG dep.
12	Resist strip	53	Densification
13	P-well photo (2)	54	Contact photo (10)
14	Boron implant	55	Contact etch
15	Resist strip	56	Memory window photo (11)
16	Oxide strip	57	BPSG etch
17	P/N-well drive	58	Reflow
18	Oxide strip	59	Oxide etch
19	Pad oxide	--	(H2 anneal omitted)
20	N-guard band photo (3)	60	Platinum dep.
21	Phos. implant	61	Silicide anneal (Contacts silicide, MW not silicided)
22	Resist strip	62	Platinum strip
23	P-guard band photo (4)	* 63	Memory window photo (11)
24	Boron Implant	* 64	Nitride/oxide etch
25	Strip resist	* 65	Ferroelectric removal photo (12)
26	Strip oxide	* 66	LTO dep.
27	Pad oxide	* 67	Ferroelectric removal photo (12)
28	Nitride dep.	* 68	Ferroelectric etch
29	Device window photo (5)	69	First metal dep. (TiW/Al/Ti)
30	Nitride/oxide etch	70	M1 photo (13)
31	Field oxidation	71	M1 etch
32	Nitride/oxide	72	Sinter
33	Sac. oxide	73	BSQ dep.
34	Oxide strip	74	Via photo (14)
--	(SNOS steps omitted)	75	Sloped via etch
35	Gate oxide	76	M2 dep. (Ti/Al)
36	Poly dep.	77	M2 photo (15)
37	Poly dope	78	M2 etch
38	Poly photo (6)	79	Overcoat dep.
39	Poly etch	80	Overcoat photo (16)
40	Pad oxide	81	Overcoat etch
41	N-extender photo (7)	82	Sinter

* = Ferroelectric-Unique Process Steps Are Shaded.

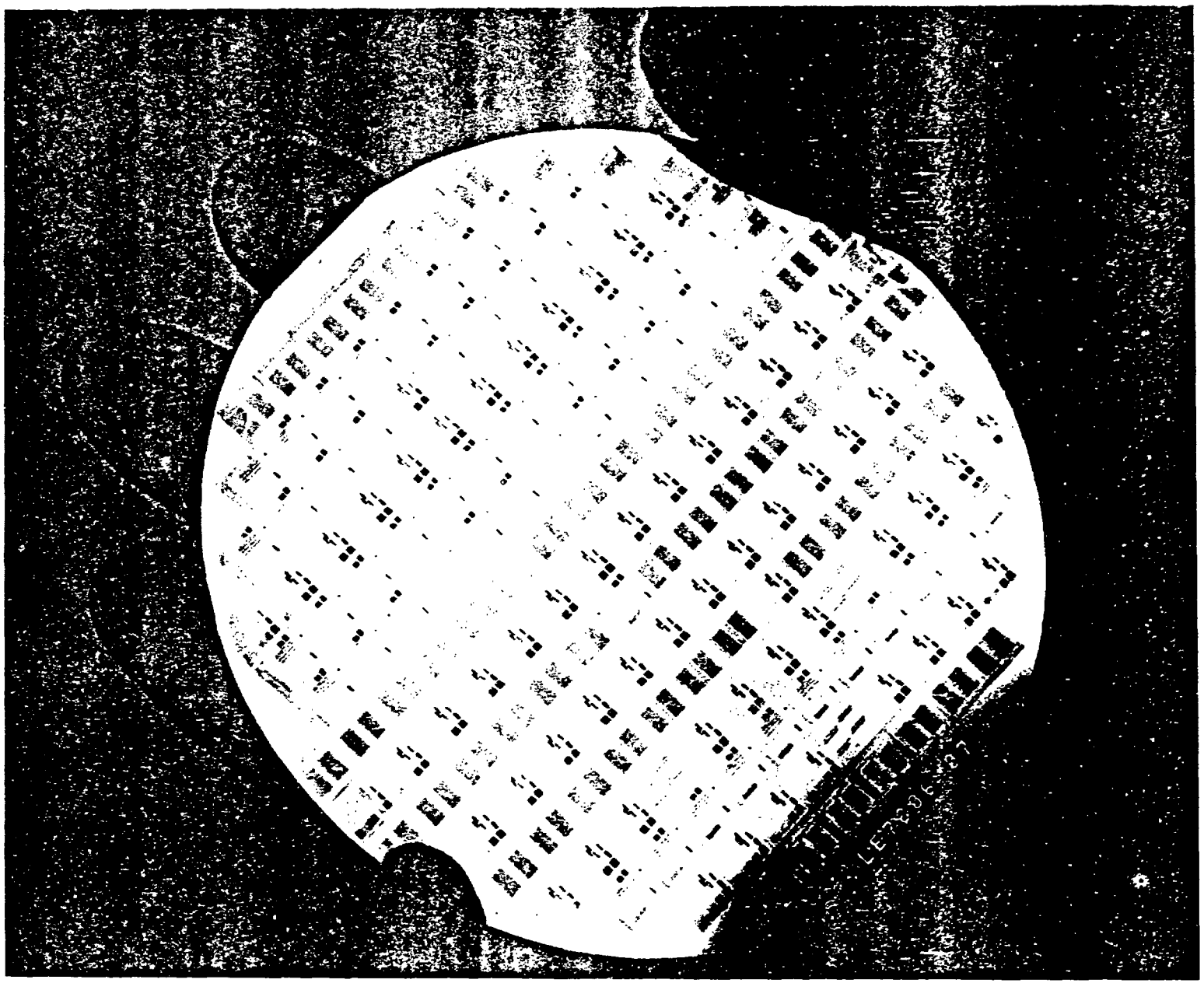


Figure 3-41: Photograph of 4-Inch FERRAM Wafer Coated With BTO By Pulsed Laser Deposition(PLD) Prior to Processing Transistors for Electrical Testing.

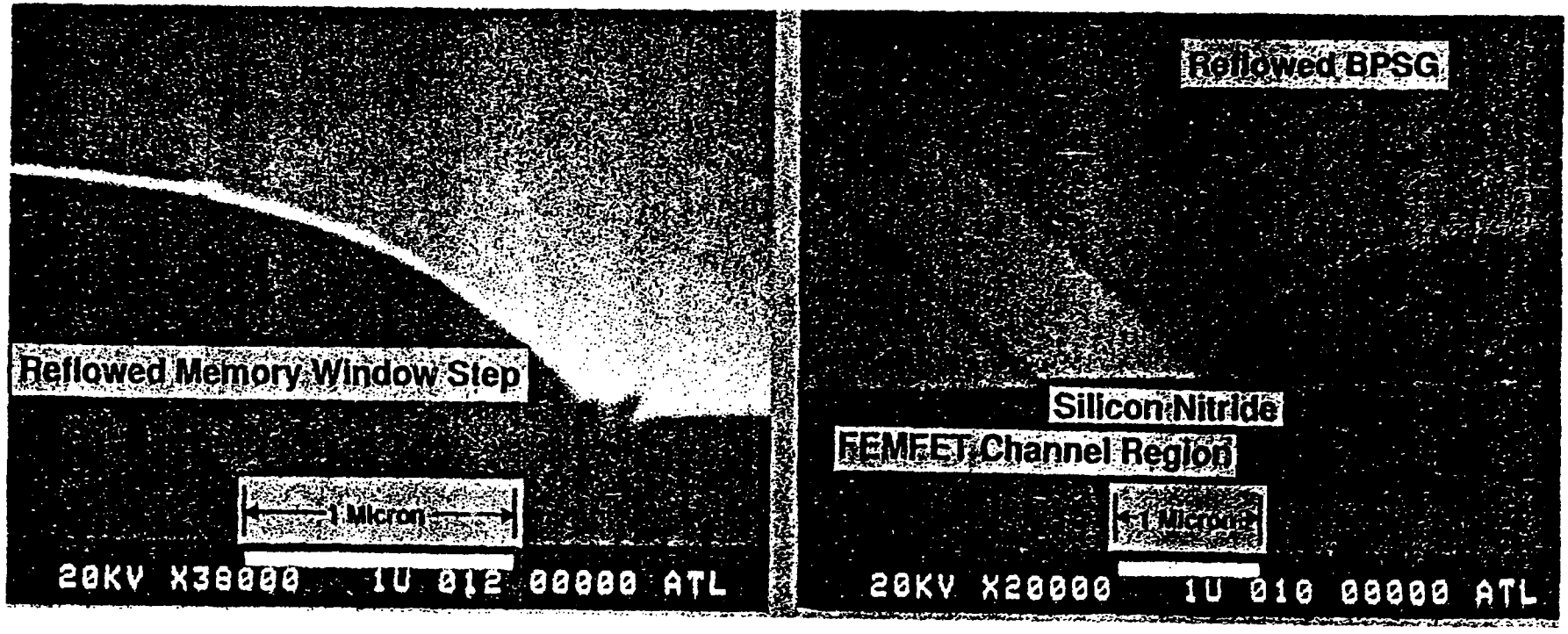


Figure 3-42: SEM Cross-Section of Reflowed Memory Window Shows Smooth Profile for Improved Metal Step-Coverage.

window and shows that the process provides a smooth profile for good metal step coverage.

Both wet and dry etch processes were developed to define the ferroelectric layer pattern. Figure 3-43 is an SEM cross-section of a BTO FEMFET gate before top electrode metallization; where definition of the BTO ferroelectric layer was accomplished using a photoresist mask and wet chemical etch. Figure 3-44 is an SEM cross-section of an ion milled BTO layer which was successfully patterned using a resist mask. Figure 3-45 is an SEM cross-section of the BTO layer of Figure 3-44 after removal of the resist mask. Note the tapered edge achieved which improves metal step coverage. No damage to the ferroelectric layer is apparent as a result of the ion milling process. Ion milling offers the advantage over wet etching of being suitable for etching many different compound ferroelectric oxide materials like the various candidates considered for use in FEMFET fabrications in the present program.

With baseline fabrication processes established, operational FEMFET memory transistors were successfully produced with BTO ferroelectric films. Although wet and dry etch processes were used to fabricate FEMFET devices only those fabricated by wet etching yielded transistors with measurable memory windows. However, the latter was probably a consequence of factors other than the etch process step. In the next section the electrical measurements made on the operational devices are discussed.

3.9 BTO FEMFET Electrical Testing

Process optimization for such parameters as oxide dielectric buffer thickness, oxide ferroelectric film thickness/deposition ambient, oxide dielectric capping, ferroelectric film anneal, and metal thickness was performed

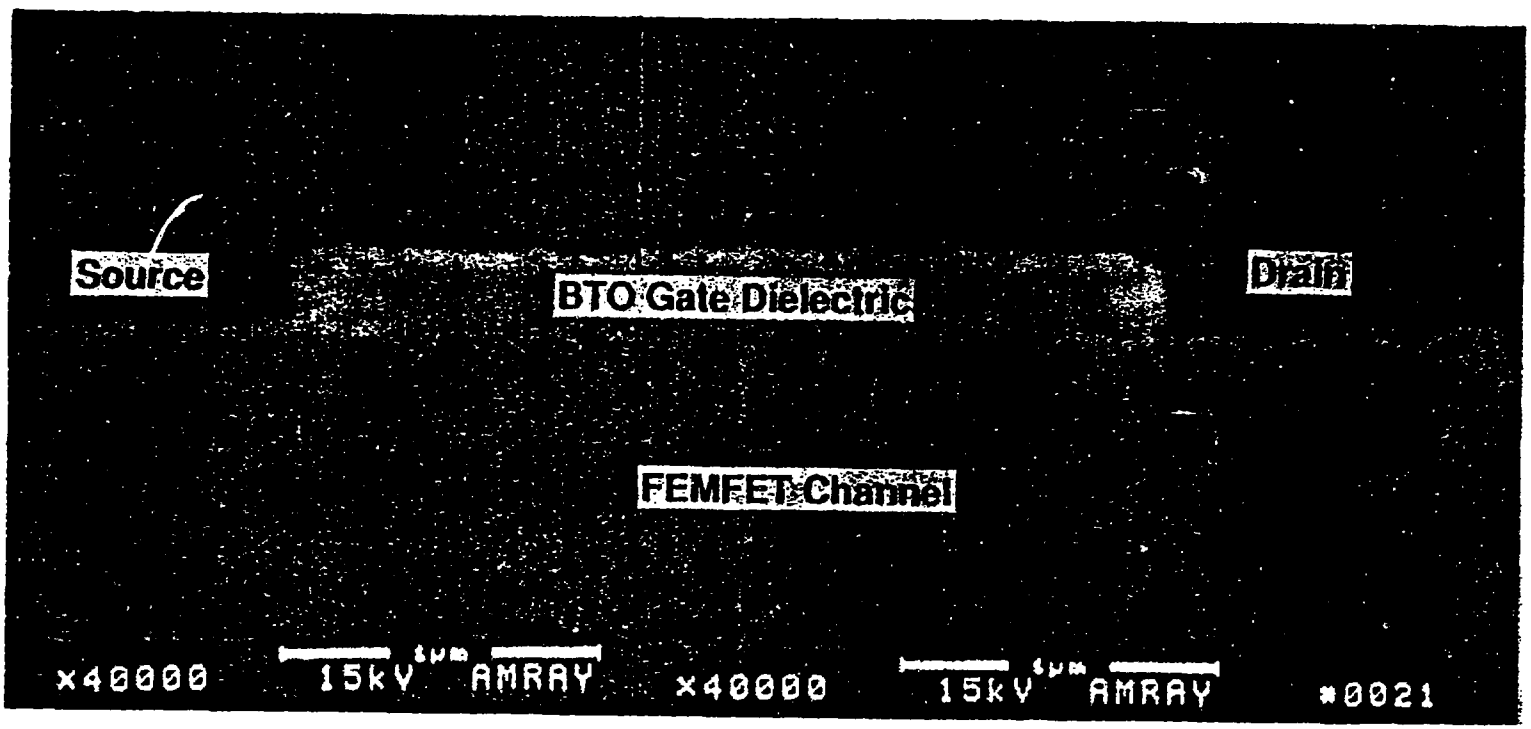


Figure 3-43: SEM Cross-Section of BTO FEMFET Gate Before Metallization; Where Definition of the BTO Layer Was Accomplished Using a Wet Chemical Etch.

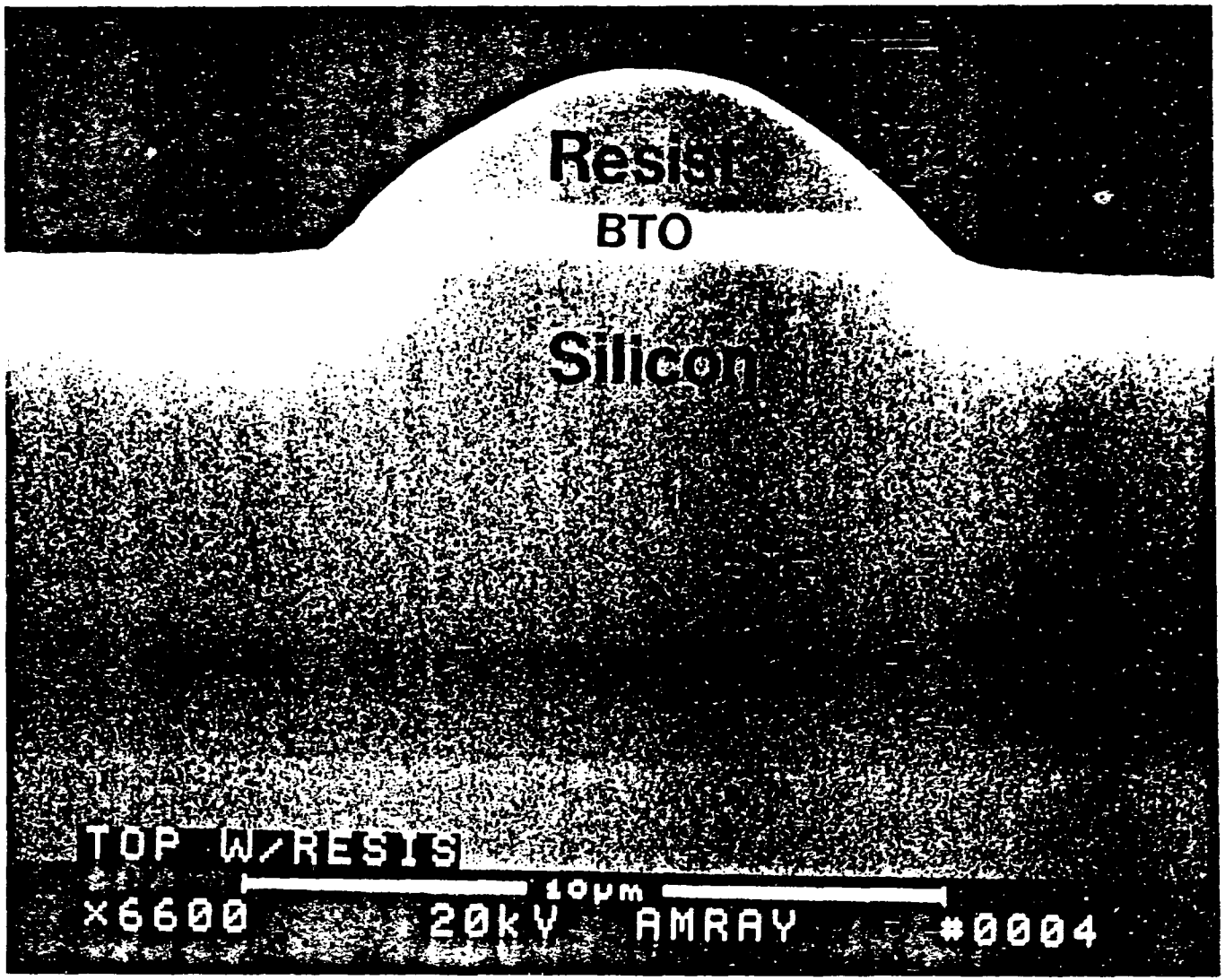


Figure 3-44: SEM Cross-Section of BTO Layer and Resist Mask Successfully Patterned Using Ion Milling.

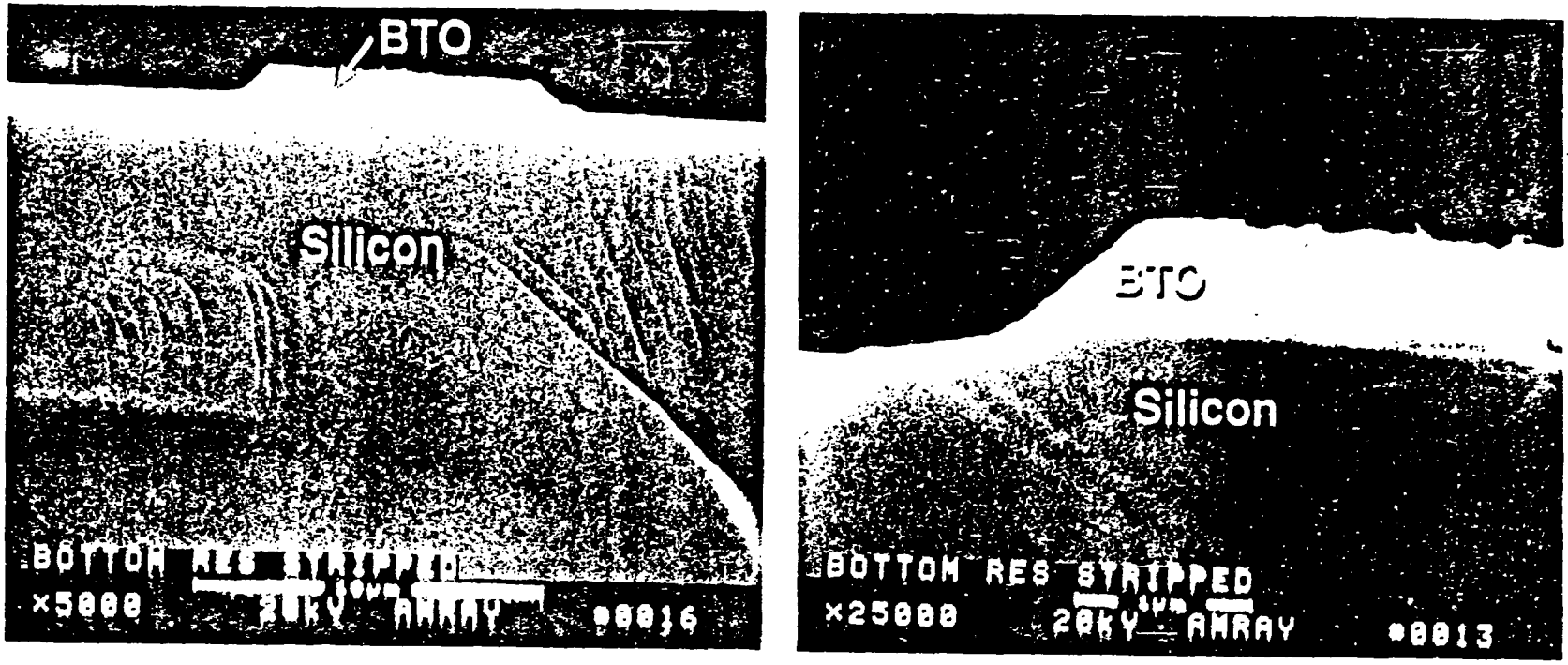


Figure 3-45: SEM Cross-Section of BTO Layer of Figure 3-44 (Patterned By Ion Milling) After Removal of Resist Mask.

in short-loop CV hysteresis and retention measurements, summarized in Appendix B, on gridded-wafer capacitors. During the course of this phase of the program 111 gridded wafers were processed. The tables in Appendix A summarize the key materials, processes, and gate structure parameters evaluated with these gridded wafers. In addition a total of 15 transistor device wafers were processed. ID numbers of FEMFET device wafers fabricated in this phase of the program using a variety of oxide feroelectric materials (BTO, Nb-doped BTO, La-doped BTO, PZT, and Nb-doped PZT) are (LE)7786-02,07,08,09,10 and (LE)7806-07,08,09,11 and (LE)7869-01,02,04,06,07,09. Details of the different oxide ferroelectric materials and key processing parameters evaluated with these devices are summarized in the tables listed in Appendix A. Results of electrical characterizations of gridded wafers and FEMFET device wafers are summarized in the tables in Appendix B.

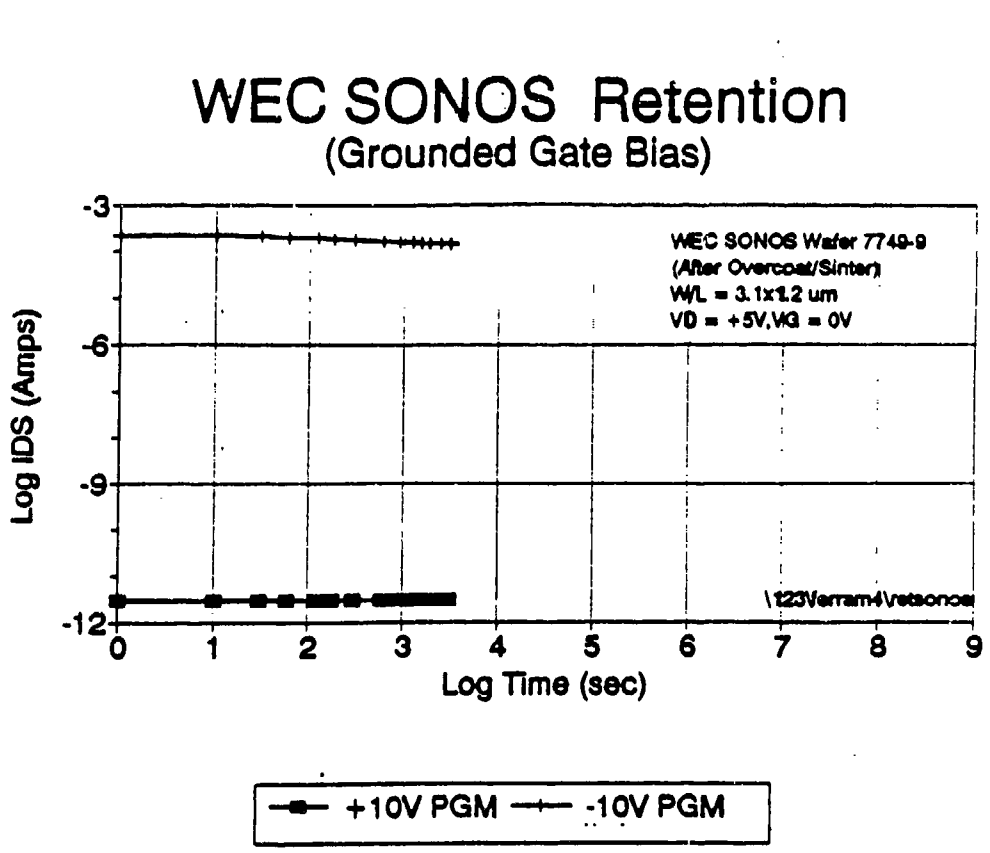
To electrically characterize FEMFETs, it was decided that the best approach would be to use conventional log of drain current (IDS) versus gate voltage (VGS) I-V curves. By plotting log of drain current, OFF state FEMFET leakage can be seen with picoampere accuracy. The threshold voltage and peak ON current are also easily seen on these plots. FEMFETs were tested by performing DC gate voltage sweeps typically with $\pm$ 5, $\pm$ 10, $\pm$ 20, or $\pm$ 40V. Typical sweep rate was approximately 2 Volts per second. Multiple sweeps were generally performed to assess such issues as threshold voltage versus maximum programming voltage, threshold voltage repeatability, and voltage polarity effects. An HP Model 4145B Semiconductor Parameter Analyzer (SPA) was used to make these measurements.

Early in this program phase the novel testing approach (cf. section 3.6.1.1) for predicting data retention in nonvolatile memory transistors from capacitance measurements at zero bias

as a function of time using CV dots had not been developed. During this time the only way to characterize retention was by programming processed FEMFETs. Later, significant time and effort was saved by evaluating retention of CV dots, rather than processed FEMFETs.

Retention characterization of oxide ferroelectric FEMFET devices involved establishing test procedures for these memory transistors. Procedures similar to those used for SONOS nonvolatile memory transistors were used as a starting point. Typically, FEMFET programming was accomplished with gate voltages between 10 and 40 volts for 10 seconds. Then, retention was determined by monitoring drain current (I_{ds}) versus time for 0 volt gate bias (VDS = 1 to 5V). This bias replicates the bias that would be seen in an EEPROM application and allows data to be retrieved nondestructively. To verify validity of the FEMFET retention measurements, Westinghouse SONOS transistors were measured using the proposed FEMFET tests. Figure 3-46 shows the resulting SONOS drain current data. For retention the drain current with 0V gate bias and 5V drain bias was monitored versus time. Note that excellent retention was observed, with minimal change in drain current after 4000 seconds. Also, note that this memory device had a 4V memory window with a 10V program voltage. These measurements confirmed that our retention measurement techniques were valid for memory transistors.

An example of a BTO FEMFET I-V characteristic for an early device wafer (ID LE7786-10) is shown in Figure 3-47. Note that when gate voltage is ramped from positive to negative voltage, the transistor threshold tends to be pushed negatively (toward depletion mode operation). Conversely, ramping gate voltage from negative to positive voltage shifts transistor thresholds positively (towards enhancement mode operation). These shifts are opposite in direction to what is observed for SONOS memory devices (see Figure 3-46) which



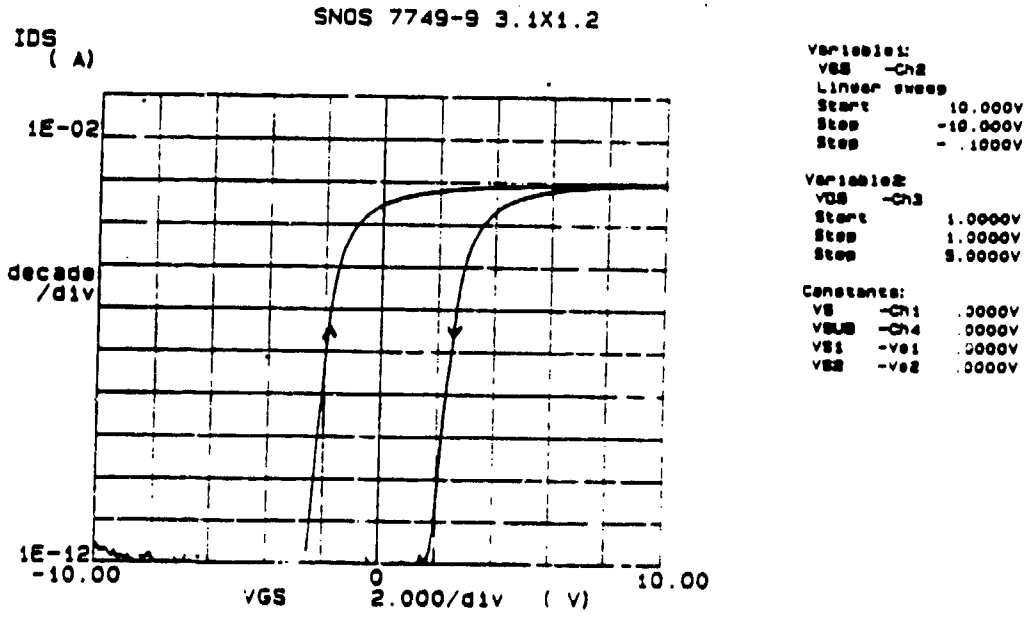


Figure 3-46: Westinghouse SONOS Transistors Show Excellent Retention to Validate FEMFET Retention Measurement Techniques.

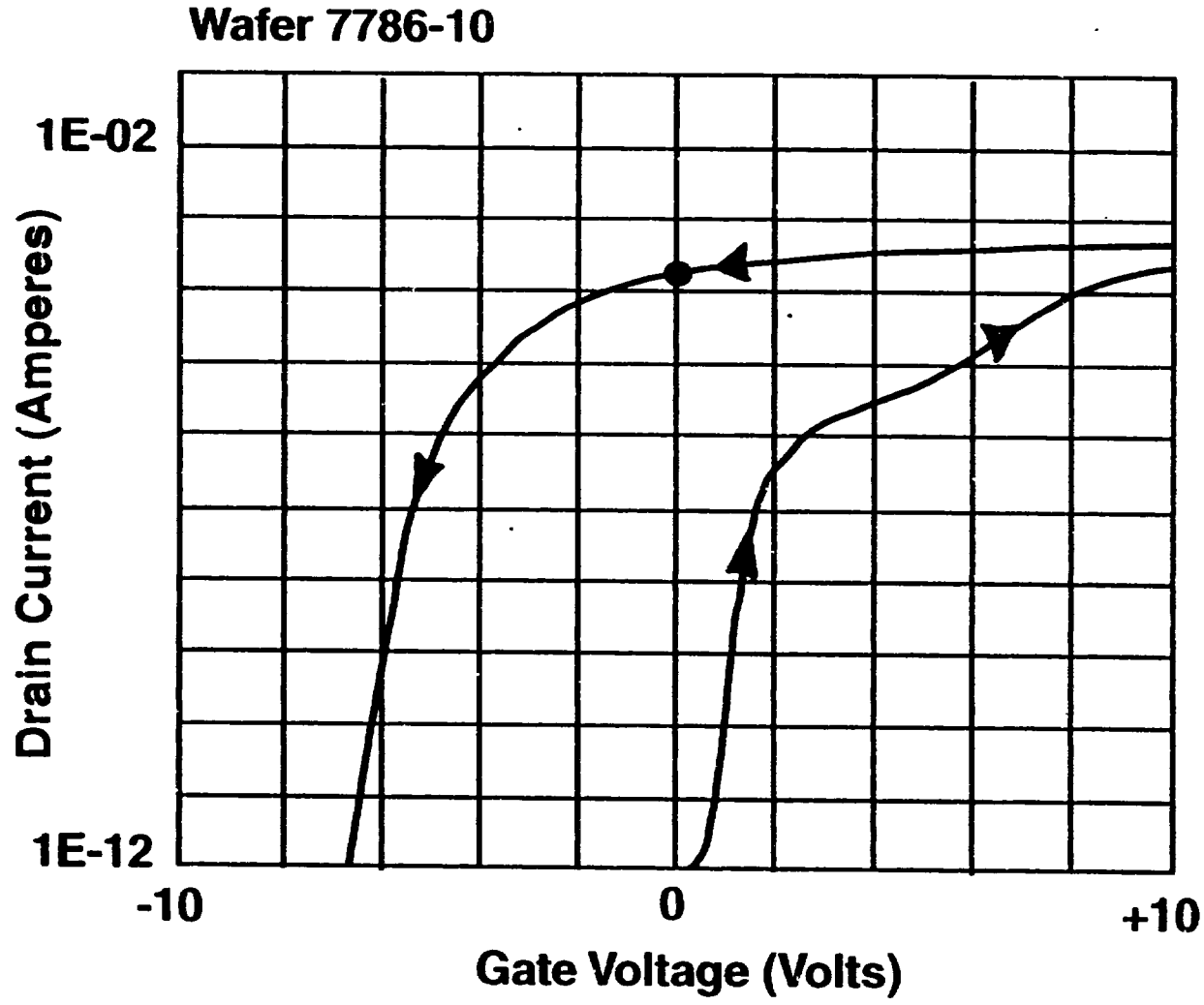


Figure 3-47: I_{ds} vs V_{gs} for Early BTO Transistor.

operate based on charge-trapping for memory operation. The opposite nature of these shifts confirmed that ferroelectric operation was accomplished in this oxide ferroelectric type FEMFET.

The retention characteristics of this oxide-type FEMFET are shown in Figure 3-48. Note that the differential in the ON and OFF state drain currents decays quickly in the first 1000 seconds from the large initial differential. After 1000 seconds the decay in the drain currents is slower with a one decade residual differential at 5000 seconds. This result is typical of what was measured on oxide-type FEMFET devices processed early in this program phase. The cause for the decay was presumed to be due to mobile oxide charge in the ferroelectric layer, which could be related to the quality of the ferroelectric layer, the physical gate structure, or other FEMFET processing steps. Possible processing steps which were identified which could cause this problem are the CVD processes used for the buffer and capping layer, which produces hydrogen bonded in the layers. This source of hydrogen could reduce the ferroelectric layer during its deposition producing a mobile charge. These critical processes were replaced in all subsequent FEMFET device wafer fabrications. To examine other possible causes it was decided to evaluate retention of CV dots using a novel testing technique (cf section 3.6.1.1) , developed for this purpose, in short-loop CV dot experiments. Thus, the focus of the program shifted to demonstrating long memory gate retention, which was accomplished (cf. section 3.6.4). Although additional FEMFETs were processed with different oxide ferroelectric materials and gate structures identified in the CV dot short-loop experiments, none yielded transistors with as good performance as for the FEMFET of Figure 3-47. This probably was a consequence of different processing steps used to fabricate these FEMFETs. Because of time and funding constraints we were unable to prepare

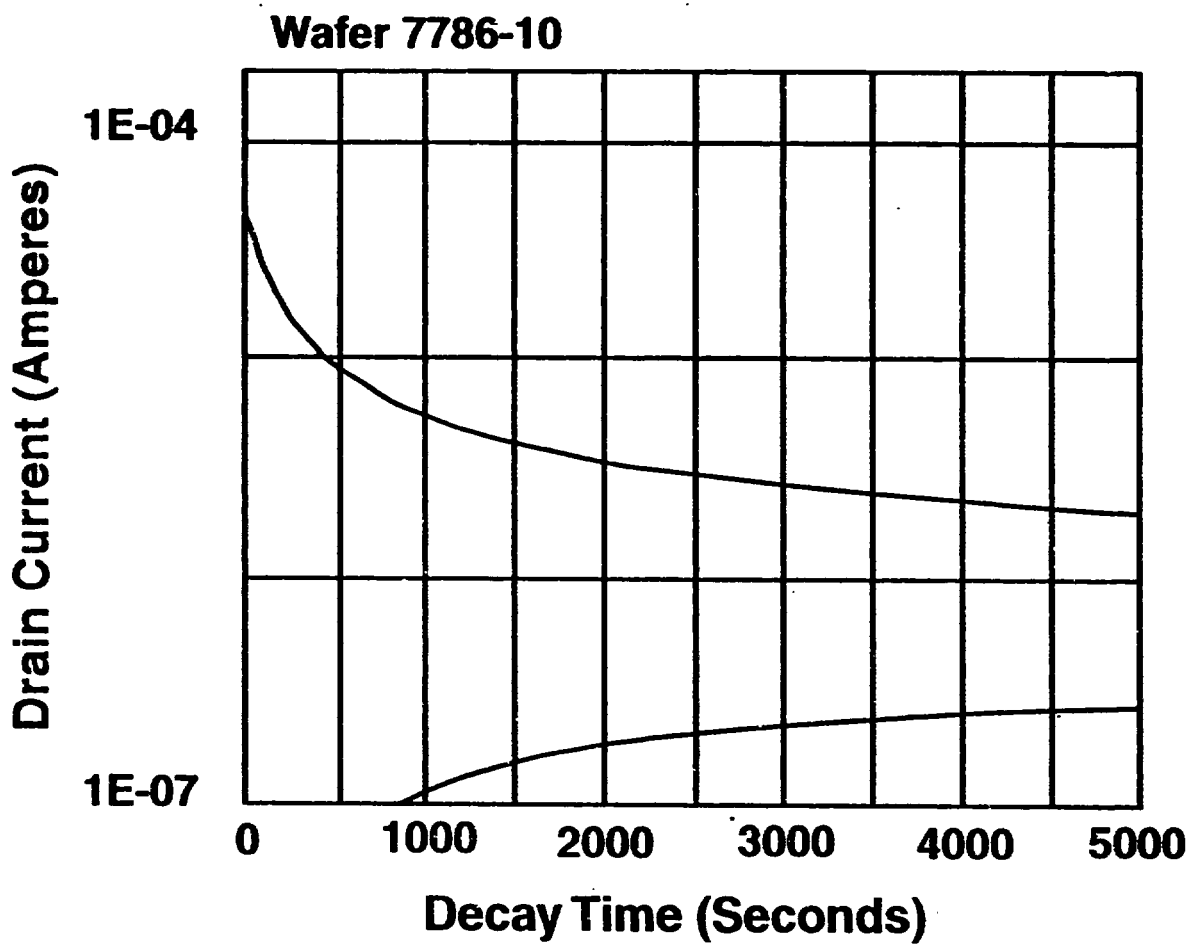


Figure 3-48: Retention Result for Early BTO Transistor Device Wafer.

additional device wafers to demonstrate long transistor retention using the improvements which showed long retention in memory gate tests.

4.0 DISCUSSION OF BTO RESULTS AND CONCLUSIONS

This phase of the program has focussed on the development of BTO-based thin-film technology as a superior, and potentially more stable, FEMFET-FERRAM memory fabrication approach. Despite the fact that high-performance memory device arrays with high yield have not yet been obtained, the intrinsic merits and practical potential of the technology have been successfully demonstrated. The following key results were achieved.

1. Pulsed laser deposition conditions were established for the successful deposition of high-quality ferroelectric films of BTO on a wide variety of substrates, including silicon, oxide single crystals and epitaxial films of superconducting YBCO. Both polycrystalline and epitaxial BTO film structures were achieved.

2. Multi-layer MIS test structures, incorporating crystalline BTO films with SiO_2 buffer and cap layers, Si_3N_4 diffusion barriers and metal (and alloy) gate electrodes, were fabricated to demonstrate memory storage capability, and to establish the basis for a FEMFET-FERRAM thin-film technology. C-V measurements indicated excellent memory-window characteristics, suggesting that p-type silicon electrodes could be driven to deep depletion with switched remanent polarization (P_r) values of less than 0.2 $\mu C/cm^2$.

3. Although our measurements of P_r vs. time suggested excellent memory retention, the rapid decay of the C-V memory window observed on these structures indicated a progressive build-up of fixed positive charge due to ion migration (within the BTO layer) to the semiconductor interface. Similar tests with lead titanate based ferroelectric gate dielectrics showed a similar behaviour which could be attributed to mobile ion effects.

4. In order to eliminate the possible effects of measurement fields on the stability of the stored C-V window condition, a unique indirect, non-destructive approach has been developed at Westinghouse, whereby the window threshold voltages were imputed from zero-bias values of the gate capacitance C_g, using SONOS C-V reference plots. This highly sensitive, non-destructive method of determining charge migration behaviour in the ferroelectric layer provides a powerful new analytical tool for the characterization of fatigue and aging effects in both FEMFET and (modified) ferroelectric capacitor memory structures.

5. Significant improvements in C-V window retention have been demonstrated on this program with new ferroelectric oxide-type memory gate stack structures (having buffer- and cap-layers and metal top electrodes of Ti-W or Al) and new ferroelectric oxide materials (e.g. doped BTO and PZT). In particular, a factor of approximately 1000 improvement (compare Figures 3-20 and 3-30) in the retention of BTO gates was demonstrated through the use of Nb doping; and, gates fabricated with undoped PZT and Al top electrodes gave extrapolated memory retention (see Figure 3-33) exceeding 10 years! As a consequence of this latest work with new materials, compatible buffer- and cap-layer incorporation in the memory gate structure, low-stress metallization techniques, and lithography appropriate for deliniation of the oxide ferroelectric gate dielectric, we feel that most of the issues associated with a high retention FEMFET demonstration are now essentially under control. However, because of funding and time constraints a transistor device wafer lot employing these improvements was not fabricated.

As a consequence these results achieved on this program, and of several related studies reported in the literature, exciting opportunities now exist for significant further improvements in the performance and stability of FEMFET-

FERRAM transistor arrays. Before summarizing these future potential research directions, we consider briefly some key aspects of the present BTO FEMFET structure and processing which impose limitations on optimum transistor fabrication and performance.

(a) Present BTO layers display high coercive and switching fields (relative to single crystals), coupled with rather low breakdown fields (see Figure 3-6), attributable probably to poorly crystallized structure and micro-cracking (electrode penetration) due to thermal mismatch between the BTO film and Si substrate. The electrical leakage caused by the cracking is effectively alleviated by the SiO_2 cap layer, but the low relative permittivity of this and the buffer layer, require that high operating gate voltages be applied in order to achieve a sufficiently high switching field across the BTO part of the structure (refer to Table 3-1).

(b) Despite the observation of square-loop properties and sharp switching thresholds in c-oriented crystals of BTO, crystalline films invariably display very rounded loops with the E_C values of constituent crystallites covering a very wide range of values. The resulting P_r values for partially switched films of the type operated in our test structures are marginally sufficient to provide a semiconductor surface potential suitable for long-term stable memory storage. However, to ensure better memory retention it would be preferable to develop film structures exhibiting c-oriented textures, with good crystal perfection and associated square loops, low coercive field and high P_r characteristics. (There is a trade-off here between the coercive field and depolarizing field, and if E_C becomes too low the stored charge may become unstable.)

(c) Our studies to date (particularly on BMF test structures[1]) have revealed that application of thin-film

metal top electrodes to the ferroelectric layer can generate interfacial stress values high enough to suppress almost completely the C-V memory window formation. These effects, which point to the existence of strong piezoelectric fields, are highly sensitive both to the nature of the metal electrode and to the thickness of the ferroelectric layer. Little is yet known about these relationships in the case of BTO device structures, and thickness parameters needed for optimum C-V window properties have yet to be established.

(d) Although doped BTO layers, prepared by pulsed laser deposition (PLD) have been successfully produced in this study, and demonstrated for high-retention memory use, optimum compositions of La- and Nb-doped films have not yet been developed. Little is known about the influence of such doping on dielectric quality and ferroelectric properties of PLD layers (cf. related studies[21-23] on doped films of lead titanate based compositions).

5.0 RECOMMENDATIONS

Some key aspects of FEMFET device processing using BTO-based structures still require further development. These include, but are not confined to, optimization of buffer- and cap-layer growth conditions, and development of high-resolution photolithography procedures. In particular, low-temperature fabrication of high-quality cap layers is needed, and a suitable differential-etch or rejection procedure for the doped BTO gate dielectric is essential.

Here, we consider plausible solutions to address the key problems listed above, based partly upon experiments performed on this program and partly on developments described recently in the ferroelectric literature. We offer these in order of priority, dealing first with steps that in the short term are likely to result in an effective demonstration of a stable FEMFET-FERRAM NDRO memory array, and which are based primarily upon proven technologies. Alternative materials and processing approaches are also presented , however, which should lead to much higher-quality devices with significantly lower power requirements and further improved memory stability.

(a) As a first priority, we re-address the short-term application of our high-retention BTO(La,Nb) MIS test-vehicle results, in a high-performance FEMFET-FERRAM memory array. To reiterate, the C-V window retention properties of these doped BTO structures are the most promising[19] to appear to date; and, if they can be successfully and reproducibly exploited in a complete device array we will have established a new and highly significant NDRO memory technology. The key to all of our suggested research in this area is the urgent and rapid development of photo-lithographic approaches that can be applied generally to every ferroelectric film FET structure considered here. The importance of this problem has been

discussed by Rost et al.[1] who were able to develop a molybdenum film liftoff process uniquely suited to the etch chemistry of $LiNbO_3$-based transistors. Our present work is focussed on etch delineation processes for BTO-based structures, using primarily HCl-based etches for the BTO layers, which we found to be successful in our original studies of BTO transistor[3] and epitaxial display arrays[31].

(b) Predicated on the successful outcome of the photolithography studies, short-term effort also is needed in the area of BTO(La,Nb) film crystal quality development, so as to achieve layers displaying lower E_c and higher P_r properties. In the later stages of this contract, we have emphasized the use of lower PLD deposition temperatures, coupled with subsequent RTA treatment as a means of attaining better homogeneity and crystal quality, without risking significant interdiffusion with other film (or substrate) components in the FEMFET memory cell structure (Such approaches[32,33] have recently proven highly effective in the crystallization of both PZT and BTO layers). Successful application to our BTO(La,Nb) films will depend critically on the control of phase structure and orientation by systematic adjustment of deposition and annealing conditions, using correlation with XRD and hysteresis measurements. As discussed above, this task would also involve systematically varying the doping level in the BTO films to achieve optimum overall ferroelectric and retention performance.

(c) As a somewhat longer-range objective, attention should be focussed on the development of alternative , higher-permittivity buffer- and capping-layers. The recent successful activity on $SrTiO_3$ paraelectric layers[34] and PLZT for high-performance capacitors[35] in DRAM devices, leads us to believe that adequate quality high dielectric constant buffer- and cap-layers could readily be processed using available technology. A capacitance increase of one or two

orders of magnitude in these layers would greatly increase the field available for switching in the ferroelectric BTO layer (cf. Table 3-1), significantly reducing the operating power requirements. The resulting drop in the field across the buffer- and cap-layers, would reduce tunnel injection from the silicon and also place less stringent leakage requirements on these layers. If the use of a more crystalline cap layer results in intergranular (upper) electrode penetration, this might be offset by using[36] a vitreous binding additive to the cap material to enhance its dielectric breakdown. Incorporation of such vitreous additives directly into the BTO(La,Nb) layer is an interesting alternative, and might enable the capping layer to be eliminated entirely from the structure. Chemical passivation of the devices (i.e. minimizing potential interaction with atmospheres during processing) could be achieved through low-temperature application of vapor-grown SiO_2 after the gate electrodes are fabricated.

(d) Recall from the discussion above, the generation of interfacial stress during the gate metallization step, can have a profound effect on the C-V window behaviour and on the ferroelectric switching properties in general. Our studies at Westinghouse, and information gleaned from the ferroelectric film literature, suggest that both the choice of electrode metal, its method of application, and thickness play critical roles in this respect. Clearly, this aspect requires more careful attention in future FEMFET development studies.

(e) Finally, we turn to the question of all-epitaxial FEMFET structures which, while appearing somewhat esoteric in relation to presently accepted VHSIC fabrication procedures, could offer greatly improved memory transistor array performance and long-term stability. Recent efforts at developing lattice-matched epitaxial sandwich structures, have emphasized the potential of top electrode layers in the

FEMFET structure with reduced stress comprising, for example, superconducting oxides[5,37] such as YBCO or metallic oxides[38] like (La,Sr)CoO3 or SrRuO3. Capacitor test devices using these materials for top and bottom electrodes, grown epitaxially on YSZ-buffered (100) Si, have been shown to display greatly improved memory fatigue properties, compared to those made with polycrystalline ferroelectric films on metal electrodes.

No studies have yet been described on the C-V properties of epitaxial YSZ, $SrTiO_3$, BTO or PZT on silicon substrates. An investigation of this type is long overdue, and could easily be undertaken, since suitable samples are readily available. We strongly suggest that C-V measurements on epitaxial structures of the type - SrRuO3/BTO(or PZT)/YSZ/(100)Si be undertaken at the earliest opportunity.

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APPENDIX A: TABLES SUMMARIZING OXIDE FERROELECTRIC WAFER HISTORY

Wafer ID	Buffer Thickness	Date	Target ID	STC ID	Temperature(°C)	Pressure (mT)	Rotation (RPM)	Power (mW)	Rep Rate (Hz)	Time (Min)	Thickness(nm)	O_2 Anneal (°C/Min/S)	COMMENTS
FN-07	TO/10	11-20-91	BTO-4-2	383-23	660	200	0	300	10	30	400-200	none	To ATL 11/21/91, 500A LTO cap
FN-08	TO/10	11-22-91	BTO-4-3	383-24	660	200	0	300	10	30	500-200	none	To ATL 02/17/92
FN-09	TO/10	12-13-91	BTO-4-4	383-27	660	200	20	300	10	30	260	none	To ATL 12/19/91
FP-06	TO/10	01-02-92	BTO-5-1	383-28	600	200	20	300	10	30	260	none	To ATL 01/07/92
FP-07	TO/10	01-06-92	BTO-5-2	383-30	600	200	20	300	10	30	260	none	To ATL 01/07
FP-08	TO/10	01-08-92	BTO-5-3	383-31	660	200	20	300	10	30	260	none	To ATL 01/16
FP-09	TO/10	01-10-92	BTO-5-4	383-32	600	200	20	300	10	30	260	none	To ATL 01/16
FMC-N-01	TO/10	01-13-92	BTO-5-5	383-33	460	200	20	300	10	30	260	none	To ATL 01/16
FMC-N-02	TO/10	01-15-92	BTO-5-6	383-36	460	200	20	300	10	30	260	none	To ATL 01/16
FMC-N-04	TO/10	01-17-92	BTO-4-6	383-38	600	200	20	300	10	30	260	none	To ATL 01/16
FMC-N-05	TO/10	01-20-92	BTO-4-7	383-37	460	200	20	300	10	30	260	none	Cut and X-ray
FMC-N-06	TO/10	01-31-92	BTO-4-8	383-38	630	200	20	300	10	30	260	none	Cut and X-ray
——	——	02-04-92	BTO-4-9	383-39	630	200	20	300	10	4	?	none	Laser Failed
FMC-N-07	TO/10	02-26-92	BTO-6-1	383-40	600	200	20	300	10	11	?	none	Laser Failed
FMD-01	LTO/15.3	02-26-92	BTO-6-2	383-41	660	200	20	300	10	30	?	none	Thin Due to Heavy Deposit on Window
LE7808-07	LTO/16.1	02-27-92	BTO-6-3	383-42	660	200	20	300	10	30	210	none	To ATL 02/26
LE7808-08	LTO/16.1	02-28-92	BTO-6-4	383-43	660	200	20	300	10	36	260	none	To ATL 02/27
FMD-02	LTO/15.3	03-02-92	BTO-6-5	383-44	660	200	20	280,320,360	10	40	280-230	none	To ATL 02/28
FMD-03	LTO/15.3	03-03-92	BTO-7-1	383-45	660	200	20	280,320,340	10	45	300-260	none	To ATL 03/03
LE7788-02	LTO/08.7	03-06-92	BTO-7-2	383-46	660	200	20	280,320,340	10	45	300-260	none	To ATL 03/03
FMC-N-08	TO/10	03-06-92	BTO-7-3	383-47	660	200	20	300,320,360	10	40	280-230	none	To ATL 03/06
FP-10	TO/10	03-09-92	BTO-7-4	383-48	660	200	20	280,315,340	10	40	280-230	none	To ATL 03/06
FMD-04	LTO/15.3	03-12-92	BTO-7-5	383-49	660	200	20	280,315,340	10	40	280-230	none	To ATL 03/09
FMC-N-09	TO/10	03-13-92	BTO-7-6	383-50	600	200	20	280,315,340	10	40	280-230	none	To ATL 03/16
FMC-N-10	TO/10	03-16-92	BTO-8-1	383-51	600	200	20	280,315,340	10	40	280-230	none	To ATL 03/18
FMC-N-11	TO/10	03-18-92	BTO-8-2	383-53	300	200	20	280,315,340	10	40	260	none	To ATL 03/18
FMC-N-12	TO/10	03-27-92	BTO-8-3	383-54	300	200	20	280,310,330	10	40	230	600/60M	To ATL 03/19
FMC-N-13	TO/10	03-30-92	BTO-8-4	383-55	300	200	20	280,306,330	10	40	250-230	600/10S	To ATL 03/31
FMC-N-14	TO/10	03-31-92	BTO-8-5	383-56	300	200	20	280,310,330	10	40	250-230	650/10S	To ATL 03/31
——	——	04-01-92	BTO-8-6	383-57	300	200	20	280,315	10	30	——	——	——
FMC-N-15	TO/10	04-10-92	BTO-9-3	383-60	660	200	20	260,280,310	10	60	410-380	600/10S	To ATL 04/08
FMC-N-16	TO/10	04-13-92	BTO-9-4	383-61	300	200	20	270,290,310	10	60	460	none	To ATL 04/10
FMC-N-17	TO/10	04-14-92	BTO-10-1	383-62	300	200	20	270,290,320	10	60	460	600/10S	To ATL 04/13
FMC-N-18	TO/10	04-15-92	BTO-10-2	383-63	300	200	20	270,300,330	10	60	460	none	Broken
FMC-N-19	TO/10	04-23-92	BTO-10-4	383-65	660	200	20	270,300,320	10	60	460	650/10S	To ATL ?
FMC-N-20	TO/10	04-24-92	BTO-11-1	383-66	300	200	20	270,300,320	10	60	460	none	To ATL 04/28
LE7788-08	TO/48.6	04-28-92	BTO-11-2	383-67	660	200	20	270,300,320	10	60	450	600/30M	To ATL 04/28
LE7788-07	TO/24.2	05-04-92	BTO-11-3	383-70	660	200	0	300	10	30	460	none	To ATL 04/28
FMD 14 X	TO/60.6	05-06-92	BTO-11-4	383-71	660	200	20	280,300,330	10	30	?	none	To ATL 05/04
FMD 08 X	TO/26.6	05-08-92	BTO-12-1	383-72	660	200	20	280,310,330	10	60	460	none	To ATL 05/06
FMD 09 X	TO/26.6	05-08-92	BTO-12-2	383-73	660	200	20	280,300,320	10	60	460	none	To ATL 05/06
FMD 15 X	TO/60.6	05-13-92	BTO-12-3	383-74	660	60	20	270,290,310	10	60	450	none	To ATL 05/11
FMD 16 X	TO/60.6	05-14-92	BTO-12-4	383-76	610	60	20	280,300,320	10	60	450	none	To ATL 05/13
FMD 10 X	TO/26.6	05-16-92	BTO-13-1	383-78	480	60	20	290,310,330	10	60	450	none	To ATL 05/14
FMD 11 X	TO/26.6	05-18-92	BTO-13-2	383-77	610	200	20	280,320	20	30	450	none	To ATL 05/18

Wafer ID	Buffer Thickness	Date	Target ID	STC ID	Temperature(°C)	Pressure (mT)	Rotation (RPM)	Power (mW)	Rep Rate (Hz)	Time (Min)	Thickness(nm)	O_2 Anneal (°C/Min/S)	COMMENTS
FN-07	TO/10	11-20-91	BTO-4-2	383-23	550	200	0	300	10	30	400-200	none	To ATL 11/21/91, 500A LTO cap
FN-08	TO/10	11-22-91	BTO-4-3	383-24	550	200	0	300	10	30	600-200	none	To ATL 02/17/92
FN-09	TO/10	12-13-91	BTO-4-4	383-27	550	200	20	300	10	30	260	none	To ATL 12/19/91
FP-06	TO/10	01-02-92	BTO-5-1	383-29	600	200	20	300	10	30	260	none	To ATL 01/07/92
FP-07	TO/10	01-06-92	BTO-5-2	383-30	600	200	20	300	10	30	260	none	To ATL 01/07
FP-08	TO/10	01-08-92	BTO-5-3	383-31	550	200	20	300	10	30	260	none	To ATL 01/15
FP-09	TO/10	01-10-92	BTO-5-4	383-32	600	200	20	300	10	30	260	none	To ATL 01/15
FMC-N-01	TO/10	01-13-92	BTO-5-5	383-33	450	200	20	300	10	30	260	none	To ATL 01/15
FMC-N-02	TO/10	01-16-92	BTO-5-6	383-35	450	200	20	300	10	30	260	none	To ATL 01/15
FMC-N-04	TO/10	01-17-92	BTO-4-6	383-36	600	200	20	300	10	30	260	none	Cut and X-ray
FMC-N-05	TO/10	01-20-92	BTO-4-7	383-37	450	200	20	300	10	30	260	none	Cut and X-ray
FMC-N-06	TO/10	01-31-92	BTO-4-8	383-38	630	200	20	300	10	4	?	none	Laser Failed
——	——	02-04-92	BTO-4-9	383-39	630	200	20	300	10	11	?	none	Laser Failed
FMC-N-07	TO/10	02-26-92	BTO-6-1	383-40	600	200	20	300	10	30	?	none	Thin Due to Heavy Deposit on Window
FMD-01	LTO/16.3	02-26-92	BTO-6-2	383-41	550	200	20	300	10	30	210	none	To ATL 02/26
LE7806-07	LTO/16.1	02-27-92	BTO-6-3	383-42	550	200	20	300	10	35	260	none	To ATL 02/27
LE7806-08	LTO/16.1	02-28-92	BTO-6-4	383-43	550	200	20	300,320	10	40	280-230	none	To ATL 02/28
FMD-02	LTO/16.3	03-02-92	BTO-6-5	383-44	550	200	20	290,320,350	10	40	280-230	none	To ATL 03/03
FMD-03	LTO/16.3	03-03-92	BTO-7-1	383-45	550	200	20	290,320,340	10	45	300-260	none	To ATL 03/03
LE7786-02	LTO/08.7	03-06-92	BTO-7-2	383-46	550	200	20	290,320,340	10	45	300-260	none	To ATL 03/06
FMC-N-08	TO/10	03-06-92	BTO-7-3	383-47	550	200	20	300,320,360	10	40	280-230	none	To ATL 03/06
FP-10	TO/10	03-09-92	BTO-7-4	383-48	550	200	20	290,316,340	10	40	280-230	none	To ATL 03/09
FMD-04	LTO/16.3	03-12-92	BTO-7-5	383-49	550	200	20	290,316,340	10	40	280-230	none	To ATL 03/16
FMC-N-09	TO/10	03-13-92	BTO-7-6	383-50	600	200	20	290,316,340	10	40	280-230	none	To ATL 03/16
FMC-N-10	TO/10	03-16-92	BTO-8-1	383-51	600	200	20	290,316,340	10	40	260	none	To ATL 03/19
FMC-N-11	TO/10	03-19-92	BTO-8-2	383-53	300	200	20	290,316,340	10	40	230	600/60M	To ATL 03/19
FMC-N-12	TO/10	03-27-92	BTO-8-3	383-54	300	200	20	280,310,330	10	40	260-230	600/10S	To ATL 03/31
FMC-N-13	TO/10	03-30-92	BTO-8-4	383-55	300	200	20	280,306,330	10	40	260-230	650/10S	To ATL 03/31
FMC-N-14	TO/10	03-31-92	BTO-8-5	383-56	300	200	20	280,310,330	10	40	——	——	——
——	——	04-01-92	BTO-8-6	383-57	300	200	20	280,315	10	30	410-360	600/10S	To ATL 04/06
FMC-N-16	TO/10	04-10-92	BTO-9-3	383-60	550	200	20	260,280,310	10	60	460	none	To ATL 04/10
FMC-N-18	TO/10	04-13-92	BTO-9-4	383-61	300	200	20	270,290,310	10	60	460	600/10S	To ATL 04/13
FMC-N-17	TO/10	04-14-92	BTO-10-1	383-62	300	200	20	270,290,320	10	60	460	none	Broken
FMC-N-18	TO/10	04-15-92	BTO-10-2	383-63	300	200	20	270,300,330	10	60	460	650/10S	To ATL ?
FMC-N-19	TO/10	04-23-92	BTO-10-4	383-65	550	200	20	270,300,320	10	60	460	none	To ATL 04/28
FMC-N-20	TO/10	04-24-92	BTO-11-1	383-66	300	200	20	270,300,320	10	60	460	600/30M	To ATL 04/28
LE7786-08	TO/48.5	04-28-92	BTO-11-2	383-67	550	200	20	270,300,320	10	60	460	none	To ATL 04/28
LE7786-07	TO/24.2	06-04-92	BTO-11-3	383-70	550	200	0	300	10	30	?	none	To ATL 06/04
FMD 14 X	TO/60.6	06-06-92	BTO-11-4	383-71	550	200	20	280,300,330	10	60	460	none	To ATL 06/06
FMD 08 X	TO/26.6	06-06-92	BTO-12-1	383-72	550	200	20	290,310,330	10	60	460	none	To ATL 06/06
FMD 09 X	TO/26.6	06-08-92	BTO-12-2	383-73	550	200	20	280,300,320	10	60	460	none	To ATL 06/11
FMD 15 X	TO/60.6	06-13-92	BTO-12-3	383-74	550	50	20	270,290,310	10	60	460	none	To ATL 06/13
FMD 18 X	TO/60.6	06-14-92	BTO-12-4	383-75	510	50	20	280,300,320	10	60	460	none	To ATL 06/14
FMD 10 X	TO/26.6	06-16-92	BTO-13-1	383-76	490	50	20	290,310,330	10	60	460	none	To ATL 06/18
FMD 11 X	TO/26.6	06-18-92	BTO-13-2	383-77	510	200	20	290,320	20	30	460	none	To ATL 06/18

Wafer ID	Buffer Thickness	Date	Target ID	STC ID	Temperature(°C)	Pressure (mT)	Rotation (RPM)	Power (mW)	Rep Rate (Hz)	Time (Min)	Thickness(nm)	O_2 Anneal (°C/Min/S)	COMMENTS
FMD 12 X	TO/26.6	06-19-92	BTO-13-3	383-78	510	200	20	300,340	30	20	460	none	To ATL 06/19
FMD 13 X	TO/26.6	06-21-92	BTO-13-4	383-79	490	200	20	310	30	20	460	none	To ATL 06/21
FMD 03 X	TO/13.6	06-28 92	BTO-13-5	383-80	510	200	20	310	30	20	460	none	To ATL 06/28
FMD 04 X	TO/13.6	06-01-92	BTO-14-1	383 81	550	200	20	300	30	20	460	none	To ATL 06/01
FMD 05 X	TO/13.6	06-03-92	BTO-14-3	383-83	550	200	0	300	10	30		none	To ATL 06/04
FMD 06 X	TO/13.6	06-06-92	BTO-14-4	383-84	550	500	0	300	10	30		none	To ATL 06/09
FMD 07 X	TO/13.6	06-09-92	BTO-14-5	383-85	550	10	0	300	10	30	see comment	none	To ATL 06/09; Estimate 2400A at center fringe (green)
FMD 19 X	TO/50.8	06-09-92	BTO-15-1	383-86	550	50	0	300	10	30	see comment	none	To ATL 06/09; Note 604A step up at grids
FMD 20 X	LTO/48.7	06-10-92	BTO-15-2	393-87	550	200	0	150	10	30	see comment	none	To ATL 06/17; Measured 2077A @ Clip mark near center fringe
FMD 21 X	LTO/48.7	06-11-92	BTO-15-3	383-88	550	200	0	100	10	40	see comment	none	To ATL 06/17; 2000A at center fringe
FMD 23 X	LTO/48.7	06-12-92	BTO-15-4	383-89	550	200	0	100-140	30	30	see comment	none	To ATL 06/17; Increases at higher rep rates
FMD 24 X	LTO/48.7	06-16-92	BTO-15-5	383-90	550-550	200	0	150-176	30	25	see comment	none	To ATL 06/17; center fringe
FMD 25 X	see comment	06-22-92	BTO-16-1	383-92	550	0.8	0	300-315	30	30	see comment	see comment	To ATL 06/26; pre-cleaned before loading wafer; pressure O_2, 30 min at 450-440C
FME-01	see comment	06-23-92	BTO-16-2	383-93	550	see comment	0	300	30	30	see comment	none	To ATL 06/26; Start deposition in vacuum; Measured 2183A near clip mark near the center fringe
MVE-100P06	none	06-24-92	BTO-16-3	383-94	550	see comment	0	150	30	30	see comment	none	To ATL 06/26; Start deposition in 50 mTorr Ar; Measured 2468A near clip mark near the center fringe
FME-02	TO/20	06-26-92	BTO-16-4	383-95	470	200	20	300	30	20		none	To ATL 06/26
FME-03	TO/20	06-26-92	BTO-16-5	383-96	450	200	20	300	30	20		none	To ATL 06/26
FME-08	TO(10)/N(40)	06-29-92	PZTO-01-1	383-97	550	300	0	300	10	30		none	To ATL 07/08
FME-09	TO(10)/N(40)	06-30-92	PZTO-01-2	383-98	550	300	0	150	10	30		none	To ATL 07/08
FME-10	TO(10)/N(40)	07-02-92	PZTO-01-3	383-99	550	300	20	150	30	40		none	To ATL 07/08
FME-11	TO(10)/N(40)	07-07-92	PZTO-01-4	383-100	500	300	20	150	30	40		none	To ATL 07/08
FME-15	TO/20	07-30-92	BTO-17-1	383-102	470	10	20	275	30	19	see comment	none	To ATL 08/07; No edge-thickness or color recorded
FME-16	TO/20	08-04-92	BTO-17-2	383-103	450	10	0	290	10	30	see comment	none	To ATL 08/07; Measured 1227A at clip mark near edge of wafer
FME-17	TO/20	08-08-92	BTO-17-3	383-104	450	10	0	285	10	30	see comment	none	To ATL 08/07; Highly non-uniform thickness
FME-18	TO/20	08-13-92	BTO-17-4	383-107	450	50	0	250	10	30	see comment	none	To ATL 08/13; Measured 4085A at clip mark near edge(yellow-green) of wafer
LE 7786-09	TO/20	08-17-92	BTO-18-1	383-109	450	200	20	250	30	20		none	To ATL 08/17
LE 7786-10	TO/20	08-18-92	BTO-18-2	383-110	450	50	20	250	30	20		none	To ATL 08/18
FME-19	TO/20	08-31-92	BTO-18-3	383-111	550/300	50/200	20	250	30	20/3		none	To ATL 08/31
FME-20	TO/20	09-01-92	BTO-18-4	383-112	550	10	20	250	30	20	see comment	none	To ATL 09/03; Estimate 7A at the center of the wafer
FME-12	TO(10)/N(40)	09-03-92	PGO-01-1	383-113	550	50	0	250	10	30	see comment	none	To ATL 09/03; Measured 4692A at clip mark near fringe
FME-21	TO/20	09-04-92	BTO-18-5	383-114	470	10	0	250	10	30		none	To ATL 09/06
FMF-09	TO(10)/N(20)	09-17-92	BTO-19-1	383-116	450	50	0	250	10	30		none	To ATL 09/17
FMF-10	TO(10)/N(20)	09-18-92	BTO-19-2	383-116	450	50	0	240	10	30		none	To ATL 09/18
FMF-11	TO(10)/N(20)	09-22-92	BTO-19-3	383-117	450	50	0	230	10	30	see comment	none	To ATL 09/24; Measured 3347A at clip mark near fringe of wafer
FMF-12	TO(10)/N(20)	09-23-92	BTO-19-4	383-118	550	50	0	230	10	30		none	To ATL 09/24
FMF-16	TO(10)/N(20)	09-26-92	PGO 02-1	383 119	26	50	0	250	10	30		650C/120M	To ATL 09/30

Wafer ID	Buffer Thickness	Date	Target ID	STC ID	Temperature(°C)	Pressure (mT)	Rotation (RPM)	Power (mW)	Rep Rate (Hz)	Time (Min)	Thickness(nm)	O_2 Anneal (°C/Min/S)	COMMENTS
FMF-17	TO(10)/N(20)	09-28-92	PGO-02-2	383-120	25	60	0	260	10	30		600C/10S	To ATL 09/30
FMF-18	TO(10)/N(20)	09-30-92	PZTO-02-1	383-121	660	300	0	260-240	10	30	see comment	none	To ATL 09/30; Measured 1592A at clip mark near fringe
FMF-19	TO(10)/N(20)	10-01-92	PZTO-02-2	383-122	660	300	0	260	30	40	see comment	none	To ATL 10/01; Measured 8036A at clip mark near fringe
FME-22	TO/20	10-02-92	BTO-19-5	383-123	660	200	0	260	10	30	see comment	none	To ATL 10/02; Measured 1106A at clip mark near fringe
FME-23	TO/20	10-06-92	BTO-20-1	383-124	660	10	0	260	10	40	see comment	none	To ATL 10/06; Too thin(why?) to make thickness measurement
FME-24	TO/20	10-06-92	LBTO-3-1	383-125	660	60	0	240	10	40	see comment	none	To ATL 10/06; Measured 1388A at clip mark near fringe
FMF-05	TO(10)/N(20)	10-07-92	LBTO-3-2	383-126	660	60	0	260	30	20	see comment	none	To ATL 10/07; Measured 2201A at clip mark near fringe
FMF-10 + 3	TO/20	10-08-92	LBTO-3-3	383-127	660	60	0	260-200	5	76 + 44	see comment	none	To ATL 10/08; Measured 1571A at clip mark near fringe
FMF-06	TO(10)/N(20)	10-09-92	BTO-20-2	383-128	460	200	0	260	10	40	see comment	none	To ATL 10/13; conducting by probe test
		10-12-91	YBCO-18-1	383-129	660	200	0	240-220	10	30	----------	none	
FMF-07	TO(10)/N(20)	10-13-92	LBTO-3-4	383-130	460	200	0	260-230	5	60 + 60		none	To ATL 10/13; for second applied YBCO top electrode test. Re-send to ATL 10/19
-------		10-16-92	YBCO-18-2	383-133	660	200	0	240-230	10	30	----------	none	
FMF-08	TO(10)/N(20)	10-14-92	BTO-20-3	383-131	460	200	0	260-210	5	60 + 60		none	To ATL 10/19
FMG-01	TO(10)/N(20)	10-15-92	LBTO-2-1	383-132	460	200	0	260-200	5	60 + 60	see comment	none	To ATL 10/19; correlation between alignment of focused beam and haze pattern.
FMG-02	TO(10)/N(20)	10-19-92	BTO-20-4	383-134	460	200	0	260-200	5	60 + 60		none	To ATL 10/19
FMG-03	TO(10)/N(20)	10-20-92	BTO-21-1	383-135	460	200	0	260-240	10	5		600C/120M	To ATL 11/17
-------		10-20-92	PGO-02-3	383-136	25	60	0	260-240	10	30			
FMG-04	TO(10)/N(20)	10-21-92	BTO-21-2	383-138	25	200	0	260-240	10	40		550C/60M	To ATL 11/17
FMF-20	TO/20	10-22-92	YSZ-01-1	383-137	460	0.6	0	240-230	10	22		none	To ATL 10/23
-------		10-23-92	BTO-21-3	383-138	460	0.6	0	230-220	10	26			Set O_2 @ 0.6mTorr 1 min after start
FMF-21	TO/20	10-26-92	LBTO-2-2	383-139	660	60	0	260	10	40	see comment	none	To ATL 12/01; purity O_2 tank; Measured 1241A @ royal blue fringe near clip mark
FMF-22	TO/20	10-29-92	LBTO-2-3	383-140	460	60	0	260	10	40	see comment	none	To ATL 11/18; Measured 1178A @ royal blue fringe near clip mark; Diode sputter 1406A Ti:W dot electrodes
FMG-12	TO(10)/N(20); R060 oxidized	10-30-92	LBTO-2-4	383-141	460	60	0	260	10	40	see comment	none	To ATL 11/17; Haze nearly completely eliminated!; Measured 1109A @ royal blue fringe near clip mark
FMF-23	TO/20	11-02-92	LBTO-1-1	383-142	460	200	0	260	10	40	?	none	To ATL 11/06; pattern; First ITO CV-dot deposition too thin (estimate <400A); Second ITO CV-dot pattern 750-1000A thick and clearly visible
FMF-24	TO/20	11-03-92	LBTO-1-2	383-143	460	60	0	260	10	40	see comment	none	To ATL 11/06; @ 60mTorr (but not needed at 200mTorr); Measured 2316A @ carnation pink fringe near clip mark; Diode sputter 1125A ITO dot electrodes
FMF-26	TO/20	11-06-92	LBTO-1-3	383-144	460	60	0	260	10	66	see comment	none	To ATL 11/17; Diode sputter 698A Ti:W dot electrodes
FMG-13	TO(10)/N(20); R060 oxidized	11-06-92	LBTO-1-4	383-145	660	200	0	260-270	10	30	see comment	none	To ATL 11/18; Alignment checked during dep and appeared to be off; Estimate 4200A at light orange central fringe
01-X	TO/20	11-11-92	BTO-21-4	383-146	460	200	0	260	10	30		none	To ATL 11/17
02-X	TO/20	11-12-92	BTO-21-5	383-147	460	60	0	260	10	30		none	To ATL 11/18
03-X	TO/20	11-13-92	BTO-21-6	383-148	460	60	0	260	10	30		none	To ATL 11/17
04-X	TO/20	11-18-92	BTO-21-7	383-149	460	60	0	326	10	30		none	To ATL 11/30
05-X	TO/20	11-20-92	LBTO-2-5	383-150	660	200	0	320	10	30	?	none	To ATL 12/06; Magnetron sputter 607A SiO_2 cap layer
06-X	TO/20	11-24-92	BTO-22-1	383-151	660	200	0	320-300	10	30		none	To ATL 12/01
FMG-14	TO(10)/N(20); R060 oxidized	12-08-92	LBTO-1-6	383-152	660	200	0	260	10	33		none	To ATL 12/08

Wafer ID	Buffer Thickness	Date	Target ID	STC ID	Temperature(°C)	Pressure (mT)	Rotation (SPM)	Power (mW)	Rep Rate (Hz)	Time (Min)	Thickness(nm)	O_2 Anneal (°C/Min/S)	COMMENTS
FMG-15	TO(10)/N(20); R060 oxidized	12-14-92	NBTO-1-1	383-163	660	200	0	260	10	30		none	To ATL 12/14
FMG-16	TO(10)/N(20); R060 oxidized	12-16-92	NPZT-1-1	383-164	RT	200	0	260	10	30		?	To ATL 12/16
FMG-17	TO(10)/N(20); R060 oxidized	12-17-92	NPZT-1-2	383-166	660	300	0	260	10	30		none	To ATL 12/18
FMG-18	TO(10)/N(20); R060 oxidized	01-04-93	NBTO-1-2	674-02	660	200	20	270	10	40		none	To ATL 01/04
FMG-19	TO(10)/N(20); R060 oxidized	01-06-93	NBTO-1-3	674-03	660	200	20	275-300	30	20		none	To ATL 01/06
07-X	TO/20	01-06-93	NBTO-2-1	674-04	660	200	20	270	10	40		none	To ATL 01/06
FMG-20	TO(10)/N(20); R060 oxidized	01-08-93	NPZT-1-3	674-05	RT	200	0	260	10	15		?	To ATL 01/08
7869-1	TO(10)/N(20); R060 oxidized	01-14-93	NBTO-2-2	674-06	660	200	20	260	10	40		none	To ATL 01/14
7869-2	TO(10)/N(20); R060 oxidized	01-16-93	NBTO-2-3	674-07	660	200	20	260	10	80	?	none	To ATL 01/16;???To ATL 01/20; Diode sputter 1774A TEW
7869-4	TO(10)/N(20); R060 oxidized	02-02-93	NBTO-3-1	674-10	660	200	20	260	10	30		none	To ATL 02/05
7869-9	TO(10)/N(20); R060 oxidized	02-04-93	NBTO-3-2	674-11	660	200	20	260	10	40		none	To ATL 02/04
7869-11	TO(10)/N(20); R060 oxidized	03-12-93	NBTO-3-3	674-12	660	200	20	260	10	40		none	To ATL 03/18
FMG-21	TO(10)/N(20); R060 oxidized	03-17-93	NBTO-3-4	674-13	660	200	20	260	10	40		none	To ATL 04/01
FMG-22	TO(10)/N(20); R060 oxidized	03-18-93	NBTO-3-5	674-14	660	200	20	260	10	40	?	none	To ATL 03/18; Magnetron sputter 387A SiO_2 cap layer
LE 7869-06	TO(10)/N(20); R060 oxidized	05-10-93	LBTO-4-1	674-16	660	200	20	260	10	40		none	To ATL 05/10
LE 7869-07	TO(10)/N(20); R060 oxidized	05-13-93	PZTO-3-1	674-18	660	300	20	225-220	30	40		none	To ATL 05/18
LE 7869-08	TO(10)/N(20); R060 oxidized	05-20-93	NPZT-1-4	674-17	660	300	20	225-200	30	40		none	To ATL 05/27

Appendix B: Table Summarizing Experimental C-V/ G_p-V TEST Results

Wafer #	Experiment	Test Results	Comments
7779FMB2; BMF-Si-73	Barrel Etched	Will not hold voltage, flat response, large and variable conductivity in dielectric	
7779FMB4; BMF-Si-75	Post Sputter	Dielectric blistered and peeling, does not hold voltage, no C-V data	
7779FMB14; BMF-Si-83	Broken top half of wafer Mercury probe, ~500Å LTO	Showed 12.5 volt window on ±10V sweep; (Files B14uc11 & B14uc13)	24 OCT 91
7779FMB7; BMF-Si-77	Simulated premetal Clean by 2 minute Sputter etch	± 20V sweep showed 19 - 20 Volt window; No ± 10 volt window.	
7779FMB13; BMF-Si-82	Aluminum dots and low temperature sinter in H_2/N_2 After 450°C sinter in H_2/N_2	± 20 Volt sweep showed a small window ~ 2 volts No Ferroelectric Window	
7779FMB17; BMF-Si-85	1000Å LTO	± 20V sweep gives No Window; +20 to -50V sweep shows a 14 volt window	
7779FMB22; BMF-Si-89	500Å LTO on 100nm BMF (File FMB22C5)	± 20V sweep gives 24V. window	7 NOV 91
7779FMB9; BMF-Si-79: 100nm 500Å LTO, 3KÅ TIW, Wafer cut into 4 quarters	T_{ess} Etch of TIW, Plasma Strip of Resist; (Files: B9TESPLS; B9BRLPLS) Barrel Etch TIW, Plasma Strip of Resist T_{ess} Etch TIW, Positrip Resist(File: B9BRLPOS) Barrel Etch TIW, Positrip Resist Anneal at 400°C for 30 min. H_2/N_2	Dot measurements showed no window. Dots tended to breakdown at 20V. Mercury Probe: ± 20V sweep showed 24.4 volt window, G_p: +25, -40μ℧. Dot showed no memory window and showed High conductance. Mercury Probe: ± 20V sweep showed 20 volt window: G_p = +500, -530μ℧ Dot breaks down at -20V. shows no window. Mercury Probe: breaks down at ± 20 volts. (Unexplained Misbehavior → Fluke) Dots showed no ferroelectric window and breakdown ~ 20V. Mercury Probe: ± 20V sweep showed a 23.2 window & G_p = +430, -470μ℧ No significant improvement	T_{ess} seems to give less leaky results than Barrel Plasma; (14 NOV 91)
7779FMB18; BMF-Si-86	1000Å LTO, 1000ÅFilament evaporated Al through Mask Anneal at 400°C for 30 min. in H_2/N_2	Aluminum dots showed no ferroelectric window at ± 50V. Aluminum dots showed no ferroelectric window at ± 50V. Mercury probe showed a 63 volt window at ± 50V real time sweep and a 59 volt window on C-V plot.	
7779FMB24; BMF-Si-91	500Å LTO, Full Clean	± 20V scan shows 26 volt window G_p = +5/-12μ℧ (av. 2)	(15 NOV 91)
7779FMB25; BMF-Si-92	500Å LTO, Degrease, No RCA clean	± 20V scan show 24.8 volt window (av of 2); G_p = +30/-37 (av 2)	(15 NOV 91)
7779FMB23; BMF-Si-90	500Å LTO, 1K Al evaporated through mask from filament source Silver Print deposited from cotton fiber on Q-Tip, Air dried 1½ hrs. Coated 4 Al dots with silver print	Al Dot - ± 20V scan showed 0.6 volt window. Small Indium foil electrode at ± 20V scan showed a 24.6 volt window (av. 2) (B23ind1) Silver Print Dot at ±10V can showed a 12.3 volt window. Silver Print dots breakdown 10 to 20V. Al-Ag dots showed no Ferroelectric window at ± 10V sweep. Dots broke down > 10V < 20V	(15 NOV 91) (19 NOV 91) (20 NOV 91)
7779FMB21; BMF-Si-88	500Å LTO Deposited then subjected to 60 min. Plasma Strip. (FILE /B21PLSTP)	± 30V C-V Scan Used To Pole Dielectric. ±20V Scan Showed Window Of 29.3 volts (av4), G_p = +6/-12 μ℧(av 2)	(21 NOV91)
FMN-22; BMF-Si-93	No RCA Preclean, 1kA Thick; 480°C FG Anneal, 1hr., 800Å LTO	Good Hysteresis With Memory Windows Often Exceeding the Programming Voltage. After trip to Sandia & return showed deterioration.	Pulsed CV Measurements: Hg Probe = > 6.65V Memory Window at 100μs, ±16V Needs Explanation
FMC-N12; BMF-Si-94	Complete Fluoridation Preclean; 480°C FG Anneal, 1hr., 2kÅ Thick, 800Å LTO	Good Hysteresis With Memory Windows Often Exceeding the Programming Voltage.	3 Dec to STC for Retention Measurements (File # 3CN12F94A) (26 NOV 91)

Wafer #	Experiment	Test Results	Comments
FMC-N11; BMF-Si-95	Complete Fluoridation Process; 480°C PG Anneal, 1hr.,2.1kÅ Thick, 800Å LTO	Backsputter Prumetal-Clean Ruins FEMFET Behavior On Top Half of Wafer. Bottom Half of Wafer ±20v,-3.2/9=12.2Window.	3 Dec for TiW-Al CV Dots With Presputter Clean ♣
FN-07 (w/10nm SiO_2); BTO-4-2	5 to 8kÅ in Sweet Spot; 2 to 4kÅ beyond second interference ring, No Cap.	Very Leaky Capacitors Showing Both FE & Tunnelling/Trapping Hysteresis.	3 Dec for Al Dot Removal; 500Å LTO Deposition; Filament Masked Al Dots.
FN-07 (w/10nm SiO_2); BTO-4-2	5 to 8kÅ in Sweet Spot; 2 to 4kÅ beyond second interference ring, No Cap.	VIRGIN DOT: ±16V Sweep→1.4V Window; Showed Poling @20V giving larger window; ±20V Sweep→6.4V Window; ±10V Sweep→6.1V Window	(Files N7BT42C5 & C6 on 2 JAN 92)
FMC-N21; BMF-Si-96	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C PG Anneal, 1hr.;2000Å Thick		4 Dec for 800Å LTO. The Bubble Defects Were Observed In The Film.
FMC-N23; BMF-Si-97	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C PG Anneal, 1hr.;2050Å Thick	±16V Sweep→0.3V Window; ±20V Sweep→7.5V Window; ±50V Sweep→53V Window; 50V Seems To Partially Lock P_s; Sodium Contaminated Drug Ahem Dep.	4Dec For 800Å LTO. For 1μ Al Shadow Dots. (Files $N23F97_{50}$ & $N23F97_{20}$ on 2 JAN 92)
FMC-N16; BMF-Si-98	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C PG Anneal, 1hr.;1875Å Thick	20V sweep Repeated 5x: Window = 4V, 7.4V, 11.2V	4 Dec for 500Å LTO. For 1μ Al Shadow Dots.
FMC-N15; BMF-Si-99	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C PG Anneal, 1hr.;2125Å Thick		4 Dec for 500Å LTO for FE Removal Experiments
FMC-N25; BMF-Si-100	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C PG Anneal, 1hr.;2125Å Thick		4 Dec for 500Å LTO for FE Removal Experiments
FMC-N20; BMF-Si-101	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C PG Anneal, 1hr.;2125Å Thick	(Files C20F96Ac & C20F96Af on 18 DEC 91) ±20V Sweep→12.6V Window; ±16V Sweep→8.9V Window; ±10V Sweep→3V Window (Files C20f101H, M, & L > 6JAN92)	11 Dec For 800Å LTO & Ti WAl CV Dots With NO Presputter Clean (Mate To FMC-N11) ♣
LE7620A-6; BMF-Si-102	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C PG Anneal, 1hr.;2000Å Thick		11 Dec for 800Å LTO
LE7620A-5; BMF-Si-103	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C PG Anneal, 1hr.;2000Å Thick		11 Dec for 800Å LTO
LE7620A-2; BMF-Si-104	No RCA; Buffered HF, DI H_2O, Alcohol Degrease; 480°C PG Anneal, 1hr.;2000Å Thick		11 Dec for 800Å LTO
LE7620A-3; BMF-Si-105	No RCA; Buffered HF, DI H_2O, Acetone Degrease; 480°C PG Anneal, 1hr.;2000Å Thick		11 Dec for 800Å LTO
FMC-N19; BMF-Si-107	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in PG @ 480°C 1hr.	PRE SPUTTER & SINTER, ±20V. SWEEP SHOWED NO WINDOW	532Å LTO(13Jan92)
FMC-N17; BMF-Si-108	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in PG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N01; BMF-Si-109	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in PG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N09; BMF-Si-110	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in PG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N13; BMF-Si-111	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in PG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N10; BMF-Si-112	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealled in PG @ 480°C 1hr.		532Å LTO(13Jan92)

Wafer #	Experiment	Test Results	Comments
FMC-N06; BMF-Si-114	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealed in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N08; BMF-Si-115	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealed in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N18; BMF-Si-116	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealed in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FMC-N05; BMF-Si-117	Buffered HF, DI H_2O, Degrease With Acetone, HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealed in FG @ 480°C 1hr.		532Å LTO(13Jan92)
FN-09; BTO-4-4 (Rotated)	PLD BTO: 500nm Center, 200nm Edge, Greenish; 18 Dec 91; 500°C Edge, 650°C Center, PRE SPUTTER ETCH.	TOP HALF OF WAFER , ±10v, Cp=155pF, Gp=1315/1520 Window=2.4/4.16=1.76v, ±5v, Window=1.62/2.2=0.58v	532Å LTO (13Jan92), Al/TiW dots, pre-sputter etch, dots Zylite/Barrel etch
FP-06; BTO-5-1 (Rotated)	PLD BTO: 250nm Center, 150nm Edge, Greenish; 2 Jan 92; 500°C Edge, 650°C Center	PROBED 5 CAPACITORS, ±20V., CONDUCTANCE OVER SCALE.	532Å LTO(13Jan92)
FP-07; BTO-5-2 (Rotated)	PLD BTO: 250nm Center, 150nm Edge, Greenish; 6 Jan 92; 500°C Edge, 650°C Center	MERCURY PROBE, ±20V. C-V WINDOW 11.6V.; ±10V. C-V WINDOW 3.8V.	532Å LTO(13Jan92)
FP-08; BTO-5-3	PLD BTO: 250nm Center, 150nm Edge, Rotating; 15 Jan 92; 550°C (readout)	MERCURY PROBE C_{MAX} 143.8pF, ±10V. SWEEP , DEP.-4.6V., ENH.2.0V., WINDOW 6.6V., G_p125\140μ Ω.BREAKS DOWN AT 20V.	492Å OF LTO 20JAN92
FP-09; BTO-5-4	PLD BTO: 250nm Center, 150nm Edge, Rotating; 15 Jan 92; 500°C (readout)	HIGH CONDUCTANCE.NO WINDOW,LOOKED AT SMALL CAPACITOR DOTS	492Å OF LTO 20JAN92
FMC-N01; BTO-5-5	PLD BTO: 250nm Center, 150nm Edge, Rotating; 15 Jan 92; 450°C (readout)	BREAKSDOWN AT 20V.;NOT FERROELECTRIC	492Å OF LTO 20JAN92
FMC-N02; BTO-5-6	PLD BTO: 250nm Center, 150nm Edge, Rotating; 15 Jan 92; 450°C (readout)	Used forFE etch experiment.	492Å OF LTO 20JAN92
FMC-N07; BMF-Si-118	Buffered HF, DI H_2O, Degrease With Acetone , HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealed in FG @ 480°C 1hr.	±20V., Gp=45μ Ω, Window -14.4/6=20.4 V. ±10V, Window=-8.35/1=9.35V. ±5V, Window=-3.3/-1.2=2.1V.	492Å OF LTO 20JAN92 No Preclean; 10kÅ Al evap.; A 100μs pulse change
FMC-N14; BMF-Si-119	Buffered HF, DI H_2O, Degrease With Acetone , HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealed in FG @ 480°C 1hr.	±20V.SWEEP,NO RESPONSE	492Å OF LTO 20JAN92
FMC-N22; BMF-Si-120	Buffered HF, DI H_2O, Degrease With Acetone , HF Dip, 200nm BMF @ 200°C, Prebaked @ 520°C, Annealed in FG @ 480°C 1hr.		492Å OF LTO 20JAN92
FMC-N04; BMF-Si-122	2 Step chem clean	MERCURY PROBE, ±20V.SWEEP DEP.-13.2V., ENH.11.0V., WINDOW 24.2V.; G_p80/120 μΩ; ±10V.SWEEP, DEP.-16V., ENH.-2.4V., WINDOW 13.6V.	No difference between 1 step and 2 step clean
FMC-N24; BMF-Si-123	1 Step chem clean	MERCURY PROBE; ±20V. SWEEP, G_p18/25, DEP.-14V., ENH.14.4V., 28.4WINDOW	See Above
FN-01; BMF-Si-124	1 step chem clean,2 hr. anneal	MERCURY PROBE, ±20V.SWEEP ,WINDOW 22.6V., G_p65/53μΩ, NOT NORMAL DIP CURVES, IS THIS A GRIDDED WAFER? ±10V. WINDOW12.5V.	See Above
FN-02; BMF-Si-125	1 Step chem clean ,2 hr. anneal.	MERCURY PROBE,DOES NOT BEHAVE LIKE GRIDDED WAFER? ±20V., G_p40/68μΩ, WINDOW 18.4V.; ±10V.: G_p38/75, WINDOW8.4V.	See Above
FN03; BMF-Si-126	2 Step chem clean,2 hr. anneal.	MERCURY PROBE, DOES NOT BEHAVE LIKE GRIDDED WAFER? ±20V., G_p38/72, WINDOW17.2V.; ±10V., GP36/72, WINDOW 8.2V.	

Wafer #	Experiment	Test Results	Comments
FN-04; BMF-Si-127	2 Step chem clean,1 hr. anneal.	±20V,Gp=109/247,Cp=50/107,window=14.4;±10V,window1.8V; HgProbe: ±20V,Gp=55/63,Cp=41/72 window = 25.2, ±10V, window = 9.8V. Wafer does not behave as a gridded wafer.	9kÅ evap. Al dots. (See Comments On FP-1)
FN-05; BMF-Si-128	2 Step chem clean,1 hr. anneal.	Wafer used for FE etch experiments.	
FP-01; BMF-Si-129	2 Step chem clean;9KA Al DEPOSITED THROUGH MASK	C-V ON DOT, ±20V. Gp152/31, Cp79/100pF, WINDOW: 13.7/0.5 = 14.2V.; ±10V: -3.6/-2.4 = 1.2V.; MERCURY PROBE, ±20V: Gp122/17, Cp76.5/66.9, WINDOW -13.7/6.6= 20.3V.; -15/10 C-V, WINDOW = -10/1.3= 11.3; ±5V., WINDOW = -2.3/0.35= 2.65; -25/20C-V, WINDOW= -19.8/7.5 = 27.3	9KA AlDOTS DEPRESS MEMORY WINDOW ,INCREASE CONDUCTANCE, REQUESTED STC TO INCREASE BMF THICKNESS FROM 2KA TO 2.5/2.8 KA.
7806-1; BMF-Si-131	1 step chem clean		
7806-2; BMF-Si-132	1 step chem clean		
7806-3; BMF-Si-133	1 step chem clean		
7806-4; BMF-Si-134	1 step chem clean		Delivered to HDL
7806-5; BMF-Si-135	1 step chem clean		
FN-07; BTO-4-2	GRIDDED WAFER ,100 A SiO_2,1K A Al DOTS EVAP.	MEMORY WINDOW 6.6V.@10V.,WORKS AT 20V.&5V.	GOOD RESPONSE OVER LARGE PART OF WAFER
FN-08; BTO-4-3	GRIDDED WAFER,100 A SiO_2,10 K A Al DOTS EVAP.	MEMORY WINDOW @10v MAX 2.8 V.BTO ABOUT 20%THINNER THAN FN-07, BREAKDOWN 10 TO 20 V.	OVERALL DOES NOT LOOK TOO GOOD. ONLY SMALL PART OF WAFER HAD RESPONSE
FMD-01; BTO-6-2	GRIDDED WAFER,153 A LTO	MERCURY PROBE, ±5V., Gp 468/571 μΩ. WINDOW= -0.5/0.1= 0.6V.; ±10V., Gp 500/600, WINDOW= 0/1.5= 1.5V., Cmax 367pF.	
7806-7; BTO-6-3	LTO 161Å sub.		
FP-02; BMF-Si-136	1 step chem clean,2.5KÅ nom.	±10v, Cp= 53/86pF,Gp= 66/56 no memory window. ±20v, SONOS Type	1KÅ LTO Cap, no presputter etch no grid visible, Ti/Al/TiW dots
FP-03; BMF-Si-137	1 step chem clean	DA'd for bubbles.	
FP-04; BMF-Si-138	1 step chem clean	DA'd for bubbles.	
FMD-06; BMF-Si-140	1 step chem clean		
FMD-07; BMF-Si-141	1 step chem clean		
FMD-08; BMF-Si-142	1 step chem clean		
7806-6; BMF-Si-143	1 step chem clean		
FMD-23; BMF-Si-139	1 STEP CHEM CLEAN,500C 1Hr.ANNEAL,250-150nm	Al Dot(13): Cp=196.7, Gp=43/66; ±5, =0.8, ±10=-7.4/-5= 2.4, ±20: -11.88/-0.08= 11.8. Hg C: Cp= 173.1, Gp= 81/110; ±5: =2.2, ±10: -9.2/0=9.2, ±20, broke down	
LE-7806-08; BTO-6-4	161A LTO ON Si	3 Transistors Showed no Memory @25 V.	
FMD-02; BTO-6-5	153A LTO , 550C 40MIN.	Hg Probe, breaks down at 20 V. ±10v, Gp= 30/70, window= 0.4/1.4= 1V. Cmax= 211pF, ±5V, window = -0.95/-0.4 = 0.55V, Cmax= 199pF.	BTO Deposit not uniform, spots
FMD-03; BTO -7-1	153A LTO, 550C 45 MIN.	Hg Probe; Breaks Down at 20V. ±10v.: Gp= 70/145, Window= -0.2/1.8 = 2V, Cmax= 277pF, ±5V: Window = -0.15/1.95= 2.1, Cmax= 274pF.	
FN09; BTO-4-4	Thermal Oxide 100Å	Bottom Half of Wafer; ±10v, Cp = 167pF, Gp = 1398/1375, Window = 1.2/4.3 = 3.1v, ±5v, 2.5/3.32 = 0.82v.	4KÅ Al 1.3kÅTiW;pre sputter clean;dots were Zylin/Barrel etched.Sinter 400 C H_2/N_2
FP06; BTO-5-1	Thermal Oxide 100Å	One dot showed no window one dot showed 0.5v window, one dot non ferroelectric.	As Above
FP07; BTO-5-2	Center 2500Å, edge 1500Å. Thermal Oxide 100Å	Hg Probe: center ±20v, 11.6V window; ±10V, 3.8V window	
FMC-N-08; BTO-7-3	550 C, 40 min., 200 mTorr.10H_2, 20 rpm.100Å Thermal Oxide	±5v, Cp = 466/451pF, Gp = 214/472, Window = 0.48/1.38 = 0.9v, ±10v, Cp = 478, Gp = 411/1146, Window = 1.2/2.9 = 1.7v.	500Å LTO, no presputter, grid visible, Ti/Al/TiW dots.
LE7786-02; BTO-7-2	550 C, 45 min., 200 mTorr.10H_2, 20 rpm.LTO 187Å.		

Wafer #	Experiment	Test Results	Comments
FMD-09; BMF-Si-144	2.5KÅ nom.	±10v, Cp = 130/135pF, Gp = 25/40μ Ω Window = -4.4/-0.8 = 3.6v ±5v, Window = 0.9v	500Å LTO Cap, no presputter, grid visible, Ti/Al/TiW dots
FMD-10; BMF-Si-145	250-150nm.	Al Dot(4, 6): Cp = 164.5, Gp = 24/47: ±5, -4.2/-3.8 = 0.4, ±10, -4.3/-2.6 = 1.7, ±20, broke down. ;Hg C: Cp = 195.5, Gp = 37/69;±5, ≈2.2, ±10, -7.84/3 = 10.84, ±20, -19.2/5.2 = 24.	
FMD-11; BMF-Si-146	280-180 nm.	Al Dot(4, 6): Cp = 101.9, Gp = 11/50; ±5, ≈0, ±10, 2.2/6.0 = 3.8, -6.56/10.2 = 16.76;Hg C : Cp = 127.2, Gp = 10/31, ±5, 2.1/3.9 = 1.8, ±10, 0.5/ 7.3 = 6.8, ±20, broke down.	
LE7786-01; BMF-Si-147			
LE7786-04; BMF-Si-148			
FP-10; BTO-7-4	550°C, 10%H_2, 200 mTorr, 40min. Thermal Oxide	±5v, Cp = 128/369pF, Gp = 820/970, SONOS Type Window at±10@5 v.	500Å LTO, pre sputter etch, no grid visible, Ti/Al/TiW dots. Used in etch experiment
FMD-04; BTO-7-5	550°C, 10%H_2, 200 mTorr, 40min. Thermal Oxide; LTO suboxide	±10v, Cp = 460/440, Gp = 1179/1078, SONOS type displacement ±5v, Window = 0.3v.	500Å LTO, no pre sputter etch; grid visible, Ti/Al/TiW dots. Used in etch experiment.
FMC-N-09; BTO-7-6	600°C, 10%H_2, 200 mTorr, 40min. Thermal Oxide; Thermal Suboxide	Hg Probe;Cp = 109.5pF, Gp = 68/82μΩ, ±10v = 2.7/3.76 = 1.06v, ±5v = 1.3/3.65 = 2.35v	Possible Cu Contaminatioe
LE7786-05; BMF-Si-149			
FMD-24; BMF-Si-150	3.3KÅ nom.	±10v, Cp = 99/96, Gp = 28/48, Window = -1.24/1.84 = 3.08 ±5v, Window = 2.3v.	500Å LTO Cap, no presputter, grid visible, Ti/Al/TiW dots
FM-N-16; BMF-Si-151		Wafer used for FE etch experiments.	
FM-N-19; BMF-Si-152	4.9KÅ nom.	±10v, Cp = 72/69pF, Gp = 14/153μ Ω, No window Can be measured, at ±20/10/5v, Too spread out	500Å LTO, no presputter, grid visible, Ti/Al/TiW dots
FM-N-20; BMF-Si-153		Used for FE etch experiments.	
FP-05; BMF-Si-154	2.8KÅ nom.	±10v, Cp = 21/126pF, Gp = 8/102μ Ω, dot no window, Hg = 0.8v window ±20v, Window = 6.2v, Hg = 6.0v.	
FMC-N-10; BTO-8-1	600 C Dep.	Hg Probe; Cp = 137pF, Gp = 101/120μ Ω, ±10v Window = 3.6v, ±5vWindow = 3.67v	468Å LTOCap
FMC-N-11; BTO-8-2	300 C Dep, 600 C 1 Hr Anneal	Hg Probe;Cp = 223.9pF, Gp = 63/107μ Ω, ±10v SONOS WINDOW, ±5vWindow = 1.1v Window, Breaks Down at20v.	468ÅLTO Cap
FMD-12; BMF-Si-155	Thickness = 250-400 nM	Al Dot(13): Cp = 82.5, Gp = 11/108; ±5, ≈2.7, ±10 = 1.6/6.5 = 4.9, ±20, -0.2/10.8 = 11;Hg C: Cp = 74.9, Gp = 41/51;±5, -0.1/2.5 = 2.6, ±10, (-0.9)/4.7 = 5.6, ±20, -5.52/9.6 = 15.1	534Å LTO, 3/27/92
FMD-13; BMF-Si-156	Thickness = 250-400nM	Used for FE etch experiment.	534Å LTO Cap, 3/27/92
FMD-14; BMF-Si-157	Thickness = 190-290 nM	Al Dot(4, 6): Cp = 136.2, Gp = 12/31; ±5, ≈0.6, ±10, ≈1.3, ±20, -14.8/ 8.2 = 23;Hg C: Cp = 72.8, Gp = 10/40; ±5, 0.4/2.15 = 1.75, ±10, (-7)/1.8 = 7.8, ±20, -16/10.2 = 26.2.	534Å LTO Cap, 3/27/92
FMD-15; BMF-Si-158	Thickness = 360-610 nM	DA'd for bubbles.	534Å LTO Cap, 3/27/92
FMD-16; BMF-Si-159	Thickness = 360-610 nM	Al Dot(12): Cp = 61.8, Gp = 11/14; ±5, ≈1.4, ±10, 1.0/8.2 = 7.2, ±20, 0/11.6 = 11.6;Hg C: Cp = 63.6, Gp = 19/ 15;±5, -1.92/1.3 = 3.2, ±10, (-1.2)/7.0 = 8.2, ±20, -8.8/9.8 = 18.6. 500 Rad Si X-Ray: Al Dot(12): Cp = 61.5, Gp = 8/11;±5, ≈1.7, ±10, 0.1/ 7.68 = 7.58, ±20, (-1.5)/13.4 = 14.9	534Å LTO Cap, 3/27/92 Conclusion of rad test at 500 Rad Si is that there was no significant change. Therefore the wafer sent to SANDIA was not damaged by airport X-ray.
FMC-N-12; BTO-8-3	300C DEP . RTA 600C, 10SEC.	±10v.Cp = 359.8pF, Gp = 334/435, Wind = 1.4/4.1 = 2.7v, ±5v, Wind = 1.35/3.05 = 1.7v.Broke Down 20v.	
FMC-N-13; BTO-8-4	300C DEP, RTA 650C, 10SEC.	±10v, Cp = 270.9, Gp = 25/101, Wind = 3.6/4.56 = 0.96v. ±5v Wind = 3.3/3.6 = 0.3v., Broke down 20v.	
FMD-17; BMF-Si-160	300-200NM, H_2, 480C, 1Hr.	Al Dot(8): Cp = 132.1, Gp = 43/75; ±5v, Wind = ≈0.25v, ±10v = -0.76/1.5 = 2.26, ±20v, -1 5.8/8.6 = 24.4v. Hg C: Cp = 115.5, Gp = 34/50;±5, 0.25 /1.15 = 0.9v, ±10, -1.74/2.2 = 3.94, ±20, -17/8.12 = 25.12	
FMD-18; BMF-Si-161	300-200NM, H_2, 480C, 1Hr.		
FMD-19; BMF-Si-162	Degrease Only, H_2, 480C, 1Hr., 100Å buffer oxide 300-200 nm. BMF	Al Dot(12): Cp = 105.4, Gp = 69/80; ±5, -1.8/-0.5 = 1.3, ±10, -2.5/0.98 = 3.5, ±20, -4.12/9.4 = 13.5. Hg C: Cp = 86.6, Gp = 55/60;±5, -0.6/ 0.85 = 1.45, ±10, (-1.5)/2.4 = 3.9, ±20, -5.1/10.8 = 15.9.	

Wafer #	Experiment	Test Results	Comments
FMD-20; BMF-Si-163	Degrease Only, H_2, 480C, 1Hr., 100Å buffer oxide 300-200 nm. BMF		
FMD-21; BMF-Si-165	3-Step Growth, 250-360 nm.	Al Dot(4, 6): Cp = 141.5, Gp = 27/45; ±5v, Wind. = ≈0.7v, ±10v, Wind = 4.1/7.6 = 3.5, ±20v, Wind = 4.68/9.68 = 5 Hg C: Cp = 97.02, Gp = 9/18, ±5v, 2.65/4.25 = 1.6, ±10v, 1.5/5.96 = (4.46), ±20v, -15/7 = 22	
FMD-22; BMF-Si-166	3-STEP GROWTH, 300-200 NM.	Al(12), Cp = 160.3, Gp = 44/19, ±5v Wind ≈1.5v, ±10 Wind = 2.4/6.1 = 3.7, ±20v Wind = -2.8/9 = 11.8.Al(9);Cp = 148.7, Gp = 20/40, ±5v Wind ≈1.4, ±10v, Wind = 2.8/6.44 = 3.64, ±20v, Wind = -2.8/8.8 = 11.6.Hg(c);Cp = 168.7, Gp = 74/100, ±5v, Wind = -0.6/2.4 = 3.0, ±10v, Wind = -2.8/4.3 = 7.1, ±20v, -14.8/8.4 = 23.2.Hg(E); Cp = 185.4, Gp = 106/134, ±5v, Wind = -0.6/2.3 = 2.9, ±10v, Wind = (-2.44) /4.74 = 7.18, ±20v, Wind = Broke Down.	
FMC-N-14; BTO-8-5/6	RTA 600C/10SEC., 410-360 NM.	Al(4, 6);Cp = 299.6, Gp = 96/173, ±10v, Wind. = SONOS: Hg(C);Cp = 303.6, Gp = 34/97, ±5, 10, 20v, All Have SONOS response. Hg(E); Cp = 281.6, Gp = 250/294, ±5, 10, 20v All Have SONOS response.	
FMC-N-15; BTO-9-3	550C-60MIN. GROWTH	Al(4, 6);Cp = 345.6, Gp = >1.8E3, ±5, 10, 20v, Too High GP for C-V Hg(C);Cp = 118.3, Gp = 11/77, ±5v, (-1.85) /1.45 = 3.3, ±10v-0.96/2.2 = 3.16, ±20v, 2.28/4.32 = 2.0v, .Hg(E);Cp = 136.4, Gp = 14/27 ±5v, (-0.62) /2.85 = 3.47, ±10v, -0.8/2.64 = 3.44, ±20v, Broke Down	
FMC-N-16; BTO-9-4	300C-60 MIN.;RTA 600C/10SEC.	Al(12);Cp = 412.6, Gp = 539/417, ±5v, ≈0, ±10v, 4.16/4.7 = 0.54. Al(11);Cp = 423.4, Gp = 188/353, ±5v, ≈0, ±10v, 4.3/4.6 = 0.3, ±20v, SONOS. Hg(C): Cp = 321.5, Gp = 108/190, ±5v, ≈2, ±10, 20v, SONOS. Hg(E): Cp = 268.7, Gp = 319/342, ±5v, ≈2.1, ±10, 20v, SONOS.	
FMC-N-18; BTO-10-2	300C-60MIN.;RTA 550C/10SEC.	Al(4, 6);Cp = 304.6, Gp = 126/217, ±5v, 3.36/3.5 = 0.14, ±10v, 4.01/ 4.56 = 0.55, ±20v, SONOS. Hg(C): Cp = 330.7, Gp = 32/112, ±5v, ≈1.4, ±10v, 3.64/4.5 = 0.86, ±20v4.6/8.4 = 3.8.Hg(E);Cp = 298.1, Gp = 27/88, ±5v, ≈1.28, ±10, 20v, SONOS.	
FMD-25; BMF-Si-167	100ÅBuffer Oxide	Al(4, 6)Cp = 61, Gp = 10/13, ±5 = -2.45/1.2 = 3.65, ±10 = (-3.5) /3.2 = 6.7, ±20 = 5.2/10.72 = 5.52;Hg(C)Cp = 78, Gp = 6/11, ±5 = -2.55/1.92 = 4.47, ±10 = (-2.64)/4.24 = 6.88, ±20 = (-7.12)/12.48 = 19.6	
FMC-N23; BMF-Si-168	100Å Buffer Oxide		
7786-6; BMF-Si-170	133Å Buffer Oxide		
W-1; BMF-Si-164	STRESS SAMPLE 162-245nm	Deposited 500Å LTO	SENT TO VA TECH 5/1/92
[illegible]	[illegible]		
[illegible]	DEP [illegible]	SONOS RESPONSE	
[illegible]	BU[illegible].5nm. [illegible]		
[illegible]	[illegible]FER [illegible]	Al(12) Cp = 109, Gp = 120/202, ±5 = -3.33/ (-1.3) = 2.03, ±10 = (-5.16) /2.5 = 7.66, ±20 = -5.92/10.48 = 16.4; Hg(C) Cp = 93, Gp = 6/11, ±5 = -1.1/1.69 = 2.79, ±10 = (-3.2) /5.38 = 8.58 ±20 = -9.2/12.68 = 21.28	
FMC-[illegible]	BUFFER [illegible] TO. [illegible] -200nm.		
FMD02X; BMF-Si-173	BUFFER [illegible] TO. [illegible] -200nm.	Al(4, 6)Cp = 80.7, Gp = 3/7, ±5 = -3.35/-1.35 = 2.0, ±10 = -5.1/1.9 = 7.0, ±20 = -8.32/8.88 = 17.2; Al(4, 4): Cp = 87.6, Gp = 4/8, ±5 = -1.1/1.2 = 1.92, ±10 = -5.1/1.9 = 7.0, ± 20 = -8.56/8.88 = 17.52, Hg(C): Cp = 92, Gp = 4/10, ±5 = -2.02/1.4 = 3.4, ±10 = -3.84/4.2 = 8.04, ± 20 = -8.76/11.4 = 20.16; Hg(EB): Cp = 88, Gp = 5/11, ±5 = -0.15/2.1 = 2.25, ±10 = -2.0/7.1 = 9, ± 20 = -9/11 = 20.0	
FMD02X; BMF-Si-174	BUFFER 135Å TO. 300 -200nm.	Al(4, 6) Cp = 81, Gp = 3/7, ±5 = -3.35/-1.35 = 2.0, ±10 = -5.1/1.9 = 7.0, ±20 = -8.32/8.88 = 17.2;Hg(C) Cp = 92, Gp = 4/10, ±5 = -2.02/1.4 = 3.4, ±10 = -3.84/4.2 = 8.04, ±20 = -8.76/11.4 = 20.16.	
LE7786-07; BTO-11-3	550C/30MIN. STATIC RUN, 242Å TO BUFFER		

Wafer #	Experiment	Test Results	Comments
FMD14X; BTO-11-4	550C/60MIN., 20RPM, TO = 506Å	Al(4, 4)Cp = 173, Gp = 24/60, ±5 = 0.45, ±10 = 0.9, ±20 = -2.72/-0.96 = 1.76 . Hg(ES)Cp = 98, Gp = 9/18, ±5 = -2.18/-0.82 = 1.36, ±10 = -2.3/-0.2 = 2.1, ±20 = -3.2/-0.3 = 2.9	
FMD-08X; BTO-12-1	550C/60MIN., 20RPM, TO = 256Å	Al(12) Cp = 358, Gp = 170/294, ±5 = -2.39/-1.86 = 0.53, ±10 = -2.34/-1.08 = 1.26, ±20 = -1.28/0.8 = 2.08, Hg(EE) Cp = 98, Gp = 10/18, ±5 = -2.9/-1.7 = 1.2, ±10 = -3.6/-0.8 = 2.8, ±20 = -5.2/2.3 = 7.5,	
W-2; BMF-SI-169	Va. TECH. STRESS MEAS.	SENT TO Va.TECH 5/22/92	700Å LTO CAP
FMD-09X; BTO-12-2	550C/60MIN., 20RPM, TO = 256Å	Ti(4, C): Cp = 225/222, Gp = 41/94, ±5 = ≈1.1, ±10 = -1.2/0.52 = 1.72, ±20 = -0.3/3.6 = 3.9, ;Ti(4EW): Cp = 221/218, Gp = 45/103, ±5 = 0.38/0.1 = 0.48, ±10 = (-0.6)/ 0.36 = 1.0, ±20 = 0.2/2.8 = 2.6; Hg(CC): Cp = 157/137, Gp = 102/376, ±5 = -0.05/0.1 = 0.15, ±10 = 0.1/0.2 = 0.3, ±20 = (-0.2)/ 0.6 = 0.8, ; Hg(EE): Cp = 137/134, Gp = 65/51, ±5 = -0.2/0.42 = 0.62, ±10 = (-0.26)/ 0.72 = 0.98, ±20 = 0.2/1.8 = 1.6; Hg(EW): Cp = 119/114, Gp = 13/70, ±5 = 0.35/1.65 = 2.0, ±10 = 0.66/1.9 = 1.24, ±20 = -0.8/0.2 = 1.0;	
FMD-15X; BTO-12-3	550C/60MIN., 20RPM, TO = 506Å, 50mTORR	Ti(4, C): Cp = 146/149, Gp = 38/60, ±5 = ≈0.1, ±10 = -2.7/-1.9 = 0.8, ±20 = -3.2/(-0.6) = 2.6; Ti(4EW): Cp = 130/148, Gp = 84/58, ±5 = 0, ±10 = 0, ±20 = ≈0.4;Ti(4, EE): Cp = 75/147, Gp = 41/54, ±5 = 0, ±10 = 0, ±20 = 0;Hg(CC): Cp = 119/126, Gp = 41/42, ±5 = SONOS, ±10 = SONOS, ±20 = SONOS; Hg(EW): Cp = 115/118, Gp = 20/30, ;±5 = ≈0.6, ±10 = ≈1.2, ±20 = -4.4/(-2.2) = 2.2; Hg(EE): Cp = 100/106, Gp = 31/28, ±5 = ≈0.5, ±10 = ≈1.2, ±20 = -4.72/ (-1.2) = 3.52	
FMD-16X; BTO-12-4	510/60MIN., 20RPM, TO = 506Å, 50mTORR		
FMD-10X; BTO-13-1	490C/60MIN., 20RPM, TO = 256Å, 50mTORR	Al(4, 6): Cp = 203/204, Gp = 51/60, ±5 = -2.88/-1.4 = 1.48, ±10 = -3.2/ (-2.0) = 1.2, ±20 = -4.4/-2.56 = 1.84; Al(4, 4): Cp = 191/191, Gp = 27/64, ±5 = -2.7/-2.2 = 0.5, ±10 = -2.96/-1.8 = 1.16, ±20 = -2.8/(-1.2) = 1.6; Hg(CC): Cp = 146/145, Gp = 16/35, ±5 = -2.8/-1.4 = 1.4, ±10 = (-3.24)/ (-0.64 = 2.6, ±20 = Broke Down; Hg(ES): Cp = 158/154, Gp = 18/39, ±5 = -4.2/-3.4 = 0.8, ±10 = -5.6/-1.56 = 4.04, ±20 = (-8.2)/ 5.2 = 13.4;Hg(EE): Cp = 147/142, Gp = 34/51, ±5 = -2.92/-1.42 = 1.5, ±10 = (-3.9)/-0.5 = 3.4, ±20 = -4.88/0.88 = 5.76	
FMD-11X; BTO-13-2	510C/30MIN., 20RPM, TO = 256Å .	Al(4, 6): Cp = 239/238, Gp = 40/99, ±5 = -2.8/-1.9 = 0.9, ±10 = -3.1/-1.3 = 1.8, ±20 = (-2.2)/0.6 = 2.8; Al(4, 4): Cp = 241/240, Gp = 44/103, ±5 = ≈0.8, ±10 = -2.9/-1.4 = 1.5, ±20 = (-2.32)/0 = 2.32; Hg(CC): Cp = 126/122, Gp = 12/26, ±5 = -3.9/-3.1 = 0.8, ±10 = -4.6/-1.8 = 2.8, ±20 = (-8)/-1.2 = 6.8; Hg(EN): Cp = 103/95, Gp = 3/12, ±5 = -2.93/(-0.05) = 2.88, ±10 = -3.36/0.6 = 3 96, ±20 = -2.72/(-0.2) = 2.52; Hg(Ek): Cp = 112/105, Gp = 10/19, ±5 = -2.2/-0.4 = 1.8, ±10 = -2.6/0 = 2.6, ±20 = (-2.4)/0.6 = 1.8; Hg(EW): Cp = 92/81, Gp = 5/10, ±5 = ≈1.5, ±10 = -4.76/-1.56 = 3.2, ±20 = (-8.4)/(-0.8) = 7.6;Hg(ES): Cp = 140/121, Gp = 14/22, ±5 = (-2.28)/ 0.62 = 1.66, ±10 = -2.36/-0.2 = 2.16, ±20 = -3.28/0.32 = 3.6	
FMD13X; BTO-13-4	490C/20MIN, 256Å BUFFER	Al(3, 12): Cp = 310/312, Gp = 38/142, ±5 = -3.0/-2.7 = 0.3, ±10 = -3.2/-2.4 = 0.8, ±20 = -3.8/-1.6 = 2.2;Al(3, 9): Cp = 338/339, Gp = 53/171, ±5 = -3.0/-2.65 = 0.35, ±10 = -3.24/-2.36 = 0.88, ±20 = -4.2/-1.4 = 2.8, ;Al(6, 11): Cp = 73/65, Gp = 59/173, ±5 = -3.1/-2.65 = 0.45, ±10 = -3.5/-2.24 = 1.26, ±20 = -4.72/-1.16 = 3.56; Hg(CC): Cp = 73/65, Gp = 8/11, ±5 = -3.9/-1.6 = 2.3, ±10 = -4.8/-0.3 = 4.5, ±20 = -6.32/2.0 = 8.32; Hg(ES): Cp = 73/63, Gp = 8/11, ±5 = -4.4/-2.6 = 1.8, ±10 = -4.84/-0.64 = 4.2, ±20 = -8.6/0.4 = 9.0; Hg(EW): Cp = 138/128, Gp = 112/111, ±5 = -2.55/-0.62 = 1.93, ±10 = -2.98/-0.1 = 2.88, ±20 = -3.6/0 = 3.6;	
FMD03; BTO-13-5	510C/20MIN, 135Å BUFFER	Al(12): Cp = 409/404, Gp = 113/254, ±5 = -2.23/-1.38 = 0.85, ±10 = -2.26/-0.8 = 1.46, ±20 = BrokeDown, ;Al(9): Cp = 406/402, Gp = 109/248, ±5 = -2.3/-1.45 = 0.85, ±10 = -2.38/0.84 = 1.54, ±20 = BrokeDown;Al(2, 13): Cp = 401/397, Gp = 106/245, ±5 = -2.3/-1.4 = 0.9, ±10 = -2.3/0.8 = 1.5, ±20 = BrokeDown;Hg(CC): Cp = 110/97, Gp = 42/43, ±5 = -1.35/-0.4 = 0.95, ±10 = -1.4/-0.2 = 1.2, ±20 = BrokeDown;Hg(ES): Cp = 101/86, Gp = 12/16, ±5 = -1.68/-0.32 = 1.36, ±10 = -2.0/0 = 2.0, ±20 = Broke Down;	

Wafer #	Experiment	Test Results	Comments
FMD-04X; BTO-14-1	550°C/20 MIN.;135Å BUFFER, 10K Al 150°C Dep &Photo Lith.	Al(C): Cp = 284/280, Gp = 42/145, ±5=0.1, ±10 = 1.0/1.36 = 0.36, ±20 = SONOS;Al(ES): Cp = 293/288, Gp = 47/154, ±5=0.1, ±10=1.2/1.6 = 0.4, ±20 = SONOS;Al(EN): Cp = 283/277, Gp = 47/157, ±5=0.1, ±10=0.1, ±20 = 4.8/6 = 1.2;Hg(ES): Cp+314/307, Gp = 66/146, ±5 = 0.05/0.72 = 0.67, ±10 = 0/0.7 = 0.7, ±20 = SONOS;Hg(CC): Cp = 189/184, Gp = 24/59, ±5 = SONOS, ±10 = SONOS, ±20 = SONOS.	
FMD-05X; BTO-14-3	550°C/30 MIN.;135ÅBUFFER;NO ROTATION;277 nm AT EDGE, 200mTORR	Al(4, 9): Cp = 384/374, Gp = 217/341, ±5 = -1.18/0.35 = 1.53, ±10 = -1.3/0.7 = 2.0, ±20 = 0.6/2.32 = 1.72;Al(6, 6): Cp = 438/425, Gp = 195/352, ±5 = -0.25/0.75 = 1.0, ±10 = -0.3/ 1.08 = 1.38, ±20 = SONOS, Al(3, 12): Cp+393/384, Gp = 154/294, ±5 = -0.87/0.65 = 1.52;±10 = -1.2/1.2 = 2.4, ±20 = SONOS; Hg(1R): Cp = 107/99, Gp = 182/168, ±5 = 0, ±10 = SONOS; Hg(2R): Cp = 249/149, Gp = 229/39, ±5 = -0.7/1.8 = 2.5, ±10 = -0.96/2.3 = 3.28, ±20 = 0;Hg(3R): Cp = 142/140, Gp = 17/36, ±5 = -3.1/2.1 = 5.2, ±10 = -0.8/1.6 = 2.4, ±20 = Break Down.	
FMD-06X; BTO-14-4	550°C/30 MIN.;135ÅBUFFER;NO ROTATION;500mTorr	Al(4, 4): Cp = 338/328, Gp = 58/238, ±5 = 0.2/1.52 = 1.32, ±10 = SONOS;Al(4, 5): Cp+321/ 308, Gp+58/354, ±5 = 0.3/1.45 = 1.15, ±10 = SONOS;Al(4, 2): Cp+321/314, Gp = 74/189, ±5 = 0.6/1.0 = 0.4, ±10 = SONOS;Hg(1R): Cp = 74/63, Gp = 30/11, ±5 = SONOS, ±10 = SONOS; Hg(2R): Cp+86/79, Gp = 8/72, ±5= 0.7, ±10 = 2.6/5.8 = 3.2, ±20 = SONOS; Hg(3R): Cp = 131/ 122, Gp+15/47, ±5 = 0.22/1.08 = 0.86, ±10 = 0.56/1.26 = 0.7, ±20 = Broke Down.	
FMD-07X; BTO-14-5	550°C/30 MIN.;135Å BUFFER;NO ROTATION;10 mTorr	Al(12, 13): Cp+315/311, Gp = 122/226, ±5 = -1.35/-1.15 = 0.2, ±10 = -4.01/0.2 = 4.21, ±20 = -1.52/1.8 = 3.32;Al(18, 12): Cp+319/314, Gp = 177/275, ±5 = -1.65/-0.5 = 1.15, ±10 = -3.9/0.76 = 4.66, ±20 = -3.8/1.8 = 5.6;Al(12, 14): Cp = 322/319, Gp = 104/215, ±5 = -1.48/-1.34, ±10 = -3.5/-0.9 = 2.6, ±20 = -2.92/2.4 = 5.32;Hg(R): Cp+170/168, Gp = 31/62, ±5 = -2.05/-0.85 = 1.2, ±10 = -3.7/0.7 = 4.4, ±20 = -2.2/1.2 = 3.4;Hg(G): Cp+111/97, Gp+18/21, ±5 = -1.85/0.85 = 2.7, ±10 = -3.3/2.0 = 5.3, ±20 = -3.6/1.8 = 5.4; Hg(Y): Cp+150/142, Gp+27/46, ±5 = -2.25/-1.25 = 1.0, ±10 = -4.4/-0.8 = 3.6, ±20 = -1.1.8/1.0 = 2.8;	
FMD-19X; BTO-15-1	550°C/30 MIN.;506Å BUFFER;NO ROTATION;50mTorr	Al(3, 10): Cp = 165/165, Gp = 29/57, ±5 = -3.1/-2.45 = 0.65, ±10 = -3.41/-1.88 = 1.52, ±20 = -2.88/-1.0 = 1.88;Al(3, 7): Cp = 144/102, Gp = 24/229, ±5 = -3.3/-2.9 = 0.4, ±10 = -3.7/ -2.4 = 1.3, ±20 = -4.32/-1.52 = 2.8;Hg(2R): Cp = 133/131, Gp = 14/29, ±5 = -2.28/-1.78 = 0.5, ±10 = -2.5/-1.56 = 0.94, ±20 = -3.8/-1.2 = 2.6; Hg(4R): Cp= 133/128, Gp = 24/41, ±5 = -2.38/ -1.94 = 0.44, ±10 = -2.6/-1.76 = 0.84, ±20 = -1.4/-1.0 = 3.4.	
FMD-20X; BTO-15-2	550°C/30 MIN.;487Å LTO BUFFER;NO ROTATION;200mTorr	Al(9, 12): Cp = 285/285, Gp = 48/124, ±5=0.15, ±10=0.4, ±20 = -3.12/-1.8 = 1.32; Al(5, 12): Cp = 279/278, Gp = 47/125, ±5=0, ±10=0.2, ±20=0.4;Hg(2R): Cp = 117/114, Gp = 20/21, ±5 = -1.58/-1.05, ±10 = -1.7/-1.0 = 0.7, ±20 = -2.6/-1.0 = 1.6;Hg(G): Cp = 199/ 191, , Gp = 132/159, ±5 = -1.65/-1.20 = 0.45, ±10 = -2.0/1.0 = 1.0, ±20 = -2.72/0 = 2.72	
FMD-21X; BTO-15-3	550°C/40 MIN.;487 LTO BUFFER;NO ROTATION;200mTorr	Al(3, 20): Cp = 249/247, Gp = 22/76, ±5=0.3, ±10 = -2.1/-1.4 = 0.7, ±20 = -2.48/-0.4 = 2.08 Al(3, 16): Cp = 285/283, Gp = 34/108, ±5=0, ±10=0, ±20=0;Hg(1R): Cp = 196/183, Gp = 141/102, ±5 = -1.15/-0.65 = 0.5, ±10 = -1.4/-0.44 = 0.96, ±20 = -2.4/0 = 2.4; Hg(1B): Cp = 187/176, Gp = 52/81, ±5=0.3, ±10 = -1.44/-0.6 = 0.84, ±20 = Broke Down.	
FMD-23X; BTO-15-4	550°C/30 MIN.;487ÅLTO BUFFER;NO ROTATION;200mTorr	Al(7, 5): Cp = 238/237, Gp = 30/73, ±5=0.25, ±10 = -2.3/-1.64 = 0.66, ±20 = -3.4/-2.08 = 1.32;Al(5, 5): Cp = 250/249, Gp = 38/92, ±5=0.4, ±10 = -2.4/-1.76 = 0.64, ±20 = Broke Down;Hg(2R): Cp = 89/80, Gp = 12/15, ±5 = -2.2/-1.6 = 0.6, ±10 = -2.4/-1.5 = 0.9, ±20 = -2.72/-1.4 = 1.32;Hg(3R): Cp = 121/116, Gp = 74/81, ±5=0.5, ±10 = -1.2/-0.16 = 1.04 ±20 = -1.96/1.2 = 3.16.	
FMD-24X; BTO-15-5	650°/550°C/25 MIN.;487ÅLTO BUFFER;NO ROTATION;200mTorr	Al(4, 9): Cp = 221/220, Gp = 43/95, ±5=0.1, ±10=0.2, ±20=0.4;Al(5, 7): Cp = 238/237, Gp = 47/105, ±5=0.1, ±10=0.2, ±20=0.4;Hg(2R): Cp = 103/101, Gp = 28/37, ±5 = -1.4/-0.5 = 0.9, ±10 = -1.44/0.4 = 1.04, ±20 = -1.6/0 = 1.6;Hg(3R): Cp = 130/127, Gp = 32/47, ±5 = -1.62/ -0.9 = 0.72, ±10 = -1.7/-0.8 = 0.9, ±20 = -2.0/-0.48 = 1.52;	

Wafer #	Experiment	Test Results	Comments
FMD 25X; BTO-16-1	550°C/30 MIN., NO BUFFER;0 RPM 7 KÅ Al Dots	Al(G): Cp = 265/264, Gp = 570/566, ±10&±20 Flat No FERROELECTRIC BEHAVIOR;Al(P): Cp = 345/343, Gp = 825/811, NO FERROELECTRIC RESPONSE;Hg(G): Cp = 229/228, Gp = 707/707, NO FERROELECTRIC RESPONSE;	
FME 01; BTO-16-2	550°C/30 MIN., NO BUFFER; 0 RPM, 1KÅ Al Dots >	±10;Cp = 357/355, Gp = 176/170, N) Ferroelectric Response At ±10 V&±20 V, Broke Down At -40 V.	
FME 02; BTO-16-4	470°C/20 MIN., BUFFER 200Å TO, 20 RPM, 200mTorr	Al(4, 6): Cp = 152/225, Gp = 42/79, ±5 = 1.3, ±10 = 3.5, ±20 = 3.6; Al(4, 4): Cp = 117/184, Gp = 28/57, ±5 = 1.4, ±10 = 2.6, ±20 = 3.6; Hg(CC): Cp = 132/115, Gp = 109/86, ±5 = 1.6, ±10 = 1.7, ±20 = 3.6; Hg(ES): Cp = 74/62, Gp = 9/7, ±5 = 1.4, ±10 = 4.2, ±20 = 19.6.	
FME 03; BTO-16-5	450°C/20 MIN., BUFFER 200Å TO, 20 RPM, 200mTorr	Al(12): Cp = 141/258, Gp = 25/76, ±5 = 1.3, ±10 = 3.5, ±20 = 7.12; Al(9): Cp = 146/251, Gp = 31/80, ±5 = 1.5, ±10 = 3.7, ±20 = 7.2; Hg(CC): Cp = 128/172, Gp = 92/37, ±5 = 1.7, ±10 = 2.8, ±20 = 3.4; Hg(ES): Cp+105/166, Gp = 17/33, ±5 = 2.3, ±10 = 4.5, ±20 = 3.6;	
------; BTO-16-3	550°C/30 MIN., NO BUFFER, 0 RPM	±10 V, Cp = 459/26, Gp = 175/3, Al(4, 15): SONOS;Al(9, 18): ±10 = 0.76, ±20 = SONOS.	
MVE-100P06	SPUTTERED BTO, Rm.Temp.120 W, 20μ, 3Hr , ANNEALED 650°C	±10 V;Cp = 514/18, Gp = 543/14, Al(4, 7) &Al(4, 9) Dots SHOWED NO FERROELECTRIC RESPONSE.	
FME-08; PZT-01-1	TO(10), N(40), PZT, 550°C/30 MIN., 300mTORR, RPM 0, 1 KÅ Al	Al(5, 11): Cp = 59/72, Gp = 11/13, ±5 = =0.6, ±10 = 1.9, ±20 = 2.2; Al(8, 14): Cp = 51/59, Gp = 9/11, ±5 = 0.35, ±10 = 1.3, ±20 = 2.4; Hg(1B): Cp = 46//48, Gp = 10/12, ±5 = 1.3, ±10 = 2.3, ±20 = 2.2; Hg(2B): Cp = 62/69, Gp = 9/10, ±5 = 0.6, ±10 = 1.7, ±20 = 2.0;	
FME-09; PZT-01-2	TO(10), N(40), PZT 550°C/30 MIN., 300mTORR, RPM 0	Al(A): Cp = 61/61, Gp = 129/232, ±5 = 0.1, ±10 = 0.3, ±20 = Broke Down, Al(B): Cp = 61/59, Gp = 140/464, ±5 = 0, ±10 = 0.2, ±20 = Broke Down; Hg(C): Cp = 52/52, Gp = 6/8, ±5 = 0.7, ±10 = 2, ±20 = 0/2.6 = 2.6, Hg(E): Cp+50/50, Gp = 6/8, ±5 = 0.7, ±10 = 2.2, ±20 = 0/2.88 = 2.88.	
FME-10; PZT-01-3	TO(10), N(40), PZT 550°C/40 MIN. , 300mTORR, RPM 20,	Al(8, 9): Cp = 46/56, Gp = 5/7, ±5 = 0.45, ±10 = 1.8, ±20 = 2.8; Al(3, 6): Cp = 60/66, Gp = 9/10, ±5 = 0, ±10 = 1.1, ±20 = 2.4; Hg(C): Cp = 27/36, Gp = 6/3, ±5 = 1.5, ±10 = 3.4, ±20 = 6.8; Hg(ES): Cp = 41/42, Gp = 4/4, ±5 = 0, ±10 = 3.0, ±20 = 4.6;	
FME-11; PZT-01-4	TO(10), N(40), PZT 500°C/40 MIN. 300 mTORR , RPM 20	Al(4, 6): Cp = 40/68, Gp = 12/7, ±5 = 0.6, ±10 = 1.6, ±20 = SONOS, Al(3, 5): Cp = 46/61, Gp = 6/8, ±5 = 0.6, ±10 = 1.4, ±20 = SONOS, Hg(C): Cp = 38/52, Gp = 32/4, ±5 = 2.2, ±10 = 4.5, ±20 = 6.2; Hg(ES): Cp = 46/53, Gp = 4/5, ±5 = 2.2, ±10 = 3.8, ±20 = 4.8.	
FME-04; BMF-Si-178	DEP 150°C, 3000Å, ANNEAL 480°C 1 KÅ Al Dots.	Al(4, 6): Cp = 58/81, Gp = 12/14, ±10 = 2.0, ±20 = 6;Al(4, 4): Cp = 65/87, Gp = 13/15, ±10 = 1.4, ±20 = 3.2;Hg(C): Cp = 56/97, Gp = 33/53, ±5 = 2.5 ±10 = 3.4, ±20 = 6.8;Hg(ES): Cp = 65/82, Gp = 16/21, ±5 = 1.9, ±10 = =3.1, ±20 = 8.2;	
FMD-12X; BTO-13-3	510°C/20 MIN., 256Å BUFFER TO, 200mTorr, 20 RPM, 450nM BTO	Al(4, 12): Cp = 284/286, Gp = 42/129, ±5 = =0.2, ±10 = -2.8/-1.9 = 0.9, ±20 = -2.4/-0.2 = 2.2, ;Al(4, 9): Cp = 287/288, Gp = 42/128, ±5 = =0.2, ±10 = -2.8/-2.6 = 0.7, ±20 = -2.6/-0.6 = 2.0, Al(1, 10): Cp = 283/285, Gp = 43/126, ±5 = =0.2, ±10 = -2.6/-1.6 = 1.0, ±20 = -2.48/-0.08 = 2.4, ;Hg(CC): Cp = 148/123, Gp = 111/26, ±5 = -1.98/-1.02 = 0.96, ±10 = -2.2/-0.7 = 1.5, ±20 = -2.32/-0.2 = 2.12, ;Hg(ES): Cp = 116/111, Gp = 12/21, ±5 = =1.1, ±10 = -4.7/-1.8 = 2.9, ±20 = -7.6/-0.88 = 6.8, ;Hg(EN): Cp = 118/117, Gp = 164/161, ±5 = -1.85/0.82 = 1.06, ±10 = -2.04/-0.6 = 1.44, ±20 = -2.4/-0.48 = 1.92;	
P⁺/P⁺; BMF-Si-183	DEP 200°C, 2500Å, ANNEAL 480°C IN H_2, 1 KÅ Al Dots.	Al(C): Cp = 78/87, Gp = 160/148, ±10 = FLAT, ±20 = 6.4, Al(E): Cp = 76/85, Gp = 157/144, ±10 = FLAT, ±20 = 4.88, Hg(C): Cp = 66/80, Gp = 110/116, ±5 = 0.7, ±10 = 1.5, ±20 = -16/3.4 = 19.4;Hg(EN): Cp = 72/85, Gp = 131/130, ±10 = 1.2, ±20 = -17.7/-2.6 = 15.2.	
P⁺/P⁺; BMF-Si-180	LARGE PIECE, BEST POLY, 200°C, 2800Å, ANNEAL H_2, 1 KÅ Al Dots.	Al(A): Cp+105/40, Gp = 15/5, ±10&20 = FLAT;Al(B): Cp = 47/50, Gp = 30/27, ±10&20 = FLAT;Hg(C): Cp = 72/54, Gp = 32/40, ±5 = 0.6, ±10 = 1.3, ±20 = 12.4;Hg(EN): Cp = 58/59, Gp = 35/73, ±5 = 0, ±10 = 1.0, ±20 = 10.8.	

Wafer #	Experiment	Test Results	Comments
FME-15;BTO-17-1 [383-102]	200ÅTO, 470 C°/19 MIN., 20 RPM, 10 mTORR	Al(9, 10): Cp = 68/227, Gp = 31/63, ±5=0.25, ±10=1.7, ±20=3.5; Al(9, 7): Cp = 137/242, Gp = 28/75, ±5=0.2, ±10=0.6, ±20=2.5; Hg(CC): Cp = 84/142, Gp = 55/233, ±5=0.4, ±10=2.7, ±20=8.0; Hg(ES): Cp = 100/205, Gp = 43/136, ±5=0.5, ±10=2.9, ±20=10.2;	
FME-16;[383-103] BTO-17-2	200 Å TO, 450°C/30 MIN, 0 RPM, 10 mTORR.	Al(2, 10): Cp = 208/207, Gp = 37/69, ±5 = -2.68/-2.38 = 0.3, ±10 = -2.7/-1.6 = 1.1, ±20 = -10.72/-4.48 = 6.24; Al(2, 9): Cp = 181/181, Gp = 32/58, ±5=0.15, ±10 = -5.4/-3.2 = 2.2, ±20 = -11.0/-2.88 = 8.12;Hg(EN, G): Cp = 204/199, Gp = 189/216, ±5=0.25, ±10 = -4.44/-1.7 = 2.74, ±20 = -7.4/2.4 = 9.8;Hg(EN, B): Cp = 211/208, Gp = 31/63, ±5=0.3, ±10 = -5.96/-3.1 = 2.65, ±20 = -9.4/-0.2 = 9.2;	
FME-17;[383-104] BTO-17-3	200 Å TO, 450°C/30 MIN, 0 RPM, 10 mTORR.	Al(3, 14): Cp = 238/237, Gp = 27/68, ±5 = -4.77/-4.52 = 0.25, ±10 = -5.36/-3.84 = 1.52, ±20 = -10.72/-4.48 = 6.24;Al(4, 12): Cp = 256/255, Gp = 43/89, ±5=0.18, ±10 = -3.9/-2.3 = 1.6, ±20 = -6.56/-2.08 = 4.48;Hg(G): Cp = 86/80, Gp = 21/23, ±5 = -1.4/-1.18 = 0.22, ±10 = -3.1/0 = 3.1, ±20 = -6.2/5.0 = 11.2;Hg(P): Cp+163/158, Gp = 25/44, ±5=0.1, ±10 = -1.44/-0.8 = 0.64, ±20 = -6.2/1.4 = 7.6;	
FME-18;BTO-17-4	200Å TO, 450°C/30 MIN, 0 RPM 50 mTORR.	Al(5, 2): Cp = 269/266, Gp = 58/115, ±5 = -1.5/-0.75 = 0.75, ±10 = SONOS, Al(5, 4): Cp = 264/263, Gp = 55/113, ±5 = -2.35/-1.65 = 0.7, ±10 = -2.7/-1.0 = 1.7, ±20 = BROKE DOWN; Al(3, 2): Cp = 266/264, Gp = 59/115, ±5 = -1.85/-1.0 = 0.85, ±10 = SONOS, Hg(2R): Cp = 88/83, Gp = 49/50, ±5 = -0.86/-0.1 = 0.76, ±10 = SONOS, Hg(3R): Cp = 182/165, Gp = 114/120, ±5 = -1.58/-0.65 = 0.93, ±10 = -1.78/-0.5 = 1.28, ±20 = BROKE DOWN;	
LE7786-09;BTO-18-1	200ÅTO, 450°C/20 MIN., 200mTORR 20 RPM.		ION MILLED AT STC
LE7786-10; BTO-18-2	200Å TO, 450 °C/20 MIN., 50m TORR, 20 RPM.	(4, 9): Cp = 199/186, Gp = 240/314, ±5 = -0.4/1.05, ±10 = -0.76/1.6 = 2.36, ±20 = 1.28/5.2 = 3.92; (4, 7): Cp = 200/196, Gp = 253/283, ±5 = 0/1.15, ±10 = -0.36/1.76 = 2.12, ±20 = 1.92/5.68 = 3.76; (3, 6): Cp = 201/198, Gp = 201/229, ±5 = 0.65/1.65 = 1.0, ±10 = -0.1/2.3 = 2.4, ±20 = 2.88/7.0 = 4.12.	ION MILLED AT STC
FME-19;BTO-18-3	550°C/20 MIN. 50 mTorr, 300°C/3 MIN. 200mTorr, 20 RPM.	Hg(CC): Cp = 116/111, Gp = 18/24, ±5 = -0.3/0.05 = 0.35;±10=0.2, ±20 = SONOS;Hg(EN): Cp = 146/141, Gp = 114/125, ±5 = -0.25/0.05 = 0.3, ±10=0.05, ±20 = SONOS;Hg(ES): Cp = 89/141, Gp = 45/95, ±5=0.4, ±10=0.2, ±20 = SONOS.	
FME-20;BTO-18-4	550°C/20 MIN., 10 mTORR, 20 RPM, TO 200Å.	Al(4, 6): Cp = 211/211, Gp = 0.5/57, ±5 = -3.65/-2.95 = 0.7, ±10 = -4.9/-2.84 = 2.06, ±20 = -7.0/-0.2 = 6.8;Al(5, 5): Cp = 55/193, Gp = 8/50, ±5=0.4, ±10=1.76, ±20=6.0;g(CC): Cp = 127/121, Gp = 10/22, ±5 = -2.85/-0.4 = 2.45, ±10 = -3.9/0.1 = 4.0, ±20 = -3.56/-0.2 = 3.36;Hg(ES): Cp = 156/155, Gp = 239/57, ±5 = -4.15/-2.05, = 2.1, ±10 = -5.38/-1.0 = 4.38, ±20 = -5.52/-0.2 = 5.32.	
FME-12;PGO-1-1	100Å TOX/400Å NITRIDE, 0 RPM.	Al(4, 12): Cp = 54/59, Gp = 15/8, ±10&±20&±50 NO FERROELECTRIC Al(8, 11): Cp = 65/75, Gp = 17/13, ±10&±20 NO FERROELECTRIC Hg(C): Cp = 62/69, Gp = 8/8, ±10&±20 NO FERROELECTRIC WINDOW	
FME-21;BTO-18-5	470°C/30 MIN., 10 mTORR, 0 RPM	Al(6, 2): Cp = 122/175, Gp = 30/54, ±5=0, ±10=2.1, ±20=6.2 Al(6, 3): Cp = 96/176, Gp = 23/62, ±5=0.2, ±10=1.1, ±20=6.8 Hg(C): Cp = 88/84, Gp = 29/26, ±5=0, ±10=2.6, ±20=6.4 Hg(CC): Cp = 77/80, Gp = 41/48, ±5=0, ±10=2.7, ±20=7.2	
FMMF-013;BMF-Si-185	G.T. = 150°C, RTA 600°C, 10 SEC., IN $H2/N_2$, 270 aM AT CENTER	Al(9, 10): Cp = 108/101, Gp = 14/56, ±5 = 1.12/3.0 = 1.88, ±10 = -0.1/3.5 = 3.4, ±20 = -1.2/10.8 = 12.0, Al(8, 8): Cp = 114/107, Gp = 16/63, ±5 = 0.85/2.65 = 1.8, ±10 = -0.5/3.44 = 3.94, ±20 = -2.88/9.2 = 12.08, Hg(CC): Cp = 88/85, Gp = 25/43, ±5 = -1.6/3.52 = 5.12, ±10 = -3.62/4.44 = 8.06, ±20 = BROKE DOWN, Hg(ES): Cp = 106/102, Gp = 34/61, ±5 = -1.72/2.95 = 4.67, ±10 = -3.32/4.24 = 7.48, ±20 = -14.8/6.48 = 21.28	
FMF-09;BTO-19-1	100Å TO/200Å NIT., 450°C/30 MIN., 50 mTORR, 0 RPM	Al(5, 2): Cp = 209/209, Gp = 0.5/52, ±5 = -3.6/-2.15 = 1.45, ±10 = -4.36/-1.36 = 3.0, ±20 = -2.4/2.88 = 5.28, Al(5, 3): Cp = 185/185, Gp = 54/92, ±5 = -3.25/-2.2 = 1.05, ±10 = -3.8/-1.5 = 2.3, ±20 = -1.0/2.36 = 3.36, Al(4, 2): Cp = 203/202, Gp = 28/61, ±10 = -3.56/-0.72 = 2.84.	LASER FOCUS PROBLEM.

Wafer #	Experiment	Test Results	Comments
FMF-10;BTO-19-2	100Å TO/200Å NIT., 450°C/30 MIN., 50 mTORR, 0 RPM.	Al(15/14): Cp = 240/240, Gp = 55/101, ±5 = -4.25/-3.78 = 0.47, ±10 = -4.7/-3.4 = 1.3, ±20 = BK DOWN, Al(16, 16): Cp = 207/206, Gp = 48/80, ±5 = -3.48/-1.75 = 1.73, ±10 = -3.96/-0.74 = 3.22. Hg(C): Cp = 77/68, Gp = 6/11, ±5 = -2.7/-1.05 = 1.65, ±10 = -3.44/ -0.56 = 2.88, ±20 = -0.6/3.8 = 4.4, Hg(E): Cp = 172/171, Gp = 37/57, ±5 = -2.8/-2.3 = 0.5, ±10 = -3.8/-1.3 = 2.5, ±20 = -5.2/2.6 = 7.8.	
FMF-11;BTO-19-3	100ÅTO/200ÅNIT., 450°C/30 MIN. 50mTORR, 0 RPM	Al(5, 3): Cp = 214/213, Gp = 46/80, ±5 = -3.8/-1.9 = 1.9, ±10 = -2.36/-0.8 = 1.56, ±20 = -1.72/3.8 = 5.52, Al(4, 2): Cp = 220/219, Gp = 54/92, ±5 = -4.05/-2.2 = 1.85, ±10 = -5.36/-1.24 = 4.12, ±20 = -2.88/3.6 = 6.48, Hg(A): Cp = 120/112, Gp = 12/20, ±5 = -2.4/-1.3 = 1.1, ±10 = -2.7/-0.84 = 1.86, ±20 = -0.4/2.4 = 2.8, Hg(B): Cp = 143/139, Gp = 17/28, ±5 = -2.05/-1.38 = 0.67, ±10 = -2.3/-1.1 = 1.2, ±20 = BK DOWN.	
FMF-12;BTO-19-4	100ÅTO/200Å NIT., 550°C/30 MIN., 50 mTORR, 0 RPM.	Al(13, 17): Cp = 382/380, Gp = 65/192, ±5=0.25, ±10 = -2.1/-1.2 = 0.9, ±20 = BROKE DOWN, Al(11, 14): Cp = 421/421, Gp = 239/239, ±5 = -2.6/-2.1 = 0.5, ±10 = -2.84/-1.6 = 1.24, ±20 = BK DOWN, Hg(1R): Cp = 270/152, Gp = 84/38, ±5 = -2.55/-0.95 = 1.6, ±10 = -2.8/-0.3 = 2.5, ±20 = BK DOWN, Hg(2R): Cp = 117/117, Gp = 61/52, ±5 = -1.3/0.3 = 1.6, ±10 = -1.86/-0.2 = 1.66, ±20 = -1.12/0.2 = 1.32.	
FMF-16;PGO-2-1	100ÅTO/200ÅNIT., RT, 50mTORR, 30 MIN., 0 RPM, FURNANCE ANEAL	Hg(R): Cp = 44/51, Gp = 16/9, ±10=0.6, ±20 = -9.28/-8.2 = 1.0	
FMF-17;PGO-2-2	100ÅTO/200Å NIT., RT, 50 mTORR, 30 MIN., 0 RPM, RTA	Hg(R): Cp = 61/66, Gp = 13/46, ±5 = -2.8/-2.62 = 0.18, ±10 = -3.0/-2.56 = 0.44, ±20 = -6.8/-0.64 = 6.16	
FMF-18;PZTO-2-1	100ÅTO/200ÅNTT. 550°C/30 MIN. 300 mTORR, 0 RPM	Al(3, 3): Cp = 114/114, Gp = 22/49, ±5 = 0.4/1.7 = 1.3, ±10 = 0.56/1.5 = 0.94, ±20 = SONOS; Al(2, 2): Cp = 101/100, Gp = 19/34, ±5 = 0.52/1.88 = 1.36, ±10 = 0.8/1.7 = 0.9, ±20 = SONOS, Hg(A): Cp = 45/43, Gp = 3/9, ±5 = -1.3/3.0 = 4.3, ±10 = -2.56/4.6 = 6.66, ±20 = SONOS; Hg(B): Cp = 50/48, Gp = 4/8, ±5 = 0.45/4.1 = 3.65, ±10 = -2.1/4.5 = 6.6, ±20 = 2.88/4.2 = 1.32.	
FMF-19;PZT-2-2	100Å TO/200 NIT. 550°C/40 MIN. 300 mTORR, 0 RPM	Al(10/15): Cp = 60/46, Gp = 12/23, ±10=0, ±20=0; Al(9, 9): Cp = 82/56, Gp = 26/24, ±10=0.2, ±20=0.2; Hg(A): Cp = 37/31, Gp = 8/12, ±5=0, ±10=3, ±20=3, Hg(B): Cp = 59/49, Gp = 35/27, ±5=0, ±10=1.2, ±20=3.2.	
FME-22;BTO-19-5	550°C/30 MIN., 200 mTORR, 0 RPM	Al(5, 3): Cp = 273/271, Gp = 59/132, ±5 = -1.7/-0.85 = 0.85, ±10 = -2.1/-0.4 = 1.7, ±20 = 0.2/1.28 = 1.48, Al(4, 5): Cp = 272/284, Gp = 312/138, ±5 = -3.6/-3.22 = 0.38, ±10 = -4.2/-2.98 = 1.22, ±20 = BROKE DOWN, Hg(1R): Cp = 162/157, Gp = 176/190, ±5 = -1.5/0.15 = 1.65, ±10 = -1.84/0.4 = 2.24, ±20 = -0.72/2.08 = 2.8, Hg(2R): Cp = 63/156, Gp = 11/38, ±5=1.4, ±10=3, ±20 = BROKE DOWN.	
FME-23;BTO-20-1	550°C/40 MIN. 10 mTORR, 0 RPM	Hg(C): Cp = 189/187, Gp = 143/173, ±5 = -1.5/-1.3 = 0.2; ±10 = -3.0/ -1.24 = 1.76; ±20 = SONOS	
FME-24;LBTO-3-1	550°C/40 MIN., 50 mTORR, 0 RPM	Al(10, 16): Cp = 311/310, Gp = 28/116, ±5 = -2.38/-1.48 = 0.9, ±10 = -2.8/-0.76 = 2.04, ±10 = -2.8/-0.76 = 2.04, ±20 = -2/4.4 = 6.4, Al(9, 13): Cp = 361/361, Gp = 44/164, ±5 = -2.15/-1.5 = 0.65, ±10 = -2.8/-0.76 = 2.04, ±20 = -2/4.5 = 6.5, Hg(1R): Cp = 102/100, Gp = 25/31, ±5 = -2.4/-0.35 = 2.05, ±10 = -2.64/0.3 = 2.94, ±20 = BROKE DOWN, Hg(2R): Cp = 111/108, Gp = 93/98, ±5 = -2.55/-0.62 = 1.93, ±10 = -4.6/0.44 = 5.04, ±20 = -7.56/4.08 = 11.64; AFTER 400°C/1 Hr. BAKE 250mTORR O_2: Al(10, 13): Cp = 311/308, Gp = 30/114, ±10 = -2.6/2.2 = 4.8, Hg(1R): Cp = 151/244, Gp = 31/205, ±10 = -2.8/1.8 = 4.6, Hg(2R): Cp = 83/83, Gp = 7/14, ±10 = -3.1/1.1 = 4.3.	
FMF-5;LBTO-3-2	100ÅTO/200ÅNIT., 550°C, 50mTORR, 0 RPM.	Al(10, 15), Cp = 175/175, Gp = 72/74; ±10 WINDOW = 0; Al(10, 9); Cp = 218/218, Gp = 174, ±10 WINDOW = 0. Hg(1R); Cp = 111/111, Gp = 12/20, ±5 = -3.7/-1.92 = 1.78, ±10 = -4.92/-1.0 = 3.92, ±20 = -9.04/1.6 = 10.64	
FAMFF-10, 3; LBTO-3-3	200Å TO, 559°C, 50mTORR, LONG DEP. 0 RPM.	Al(6, 5): Cp = 112/112, Gp = 48/46, ±10 WINDOW = 0; Al(5, 5): Cp = 124/124, Gp = 53/53, ±10 WINDOW = 0.	

Wafer #	Experiment	Test Results	Comments
FMF-6;BTO-20-2 / CJYBCO-1B	450°C/40 MIN., 200mTORR, 0 RPM , SUPER COND, 550°C/30 MIN 0 RPM	Sent Back To STC	
FMF-7;LBTO-3-4 YBCO	450°C/2 Hr(5Hz), 100ÅTO/200Å NTT, 200mTORR, 0 RPM .	Sent Back To STC	
FMF-08;BTO-20-3	100ÅTO/200ÅNTT., 450°C/2Hr., 5Hz., 200mTORR, 0 RPM.	Al(15, 10): Cp = 238/238, Gp = 95/95, ±20 Window = 0; Al(11, 10): Cp = 218/218, Gp = 74/74, ±20 = Window = 0.	
FMG-02;BTO-20-4	450°C/2Hr., 5Hz., 200mTORR, 0 RPM	Al(5, 6): Cp = 271/271, Gp = 114/114, ±20 Window = 0; Al(7, 8): Cp = 252/252, Gp = 100/100, ±20 Window = 0	
FMG-01;LBTO-2-1	450°C/2Hr., 5Hz., 200mTORR, 0 RPM	Al(6, 4): Cp = 158/158, Gp = 37/37, ±20 Window = 0; Al(4, 5): Cp = 176/176, Gp = 50/50, ±20 Window = 0.	
FMF-20;BTO-21-3	YTTRIUM BUFFER-YSZ-1-1;450°C/20 MIN., 10 Hz, 0 RPM, 5E-4 O_2, BTO 450°C/25 MIN., 10 Hz, 0 RPM, 5E-4 O_2.	INDIUM DOTS ON TOP BTO HAD HIGH CONDUCTIVITY; ±2 VOLTS =0.1 V WINDOW	
FMF-23;LBTO-1-1	450°C/40 MIN., 200 mTORR, ITO DOTS ON LBTO, 0 RPM.	ITO(3, 4): Cp = 185/174, Gp = 1034/1006, ±5 = 0/0.43, ±10 = -0.2/0.64 = 0.84, ±20 = 0.8/2.36 = 1.56; ITO(3, 6): Cp = 210/201, Gp = 1257/1218, ±5 = -0.2/0.35 = 0.55, ±10 = -0.4/0.5 = 0.9, ±20 = 1.0/2.8 = 1.8; Hg(1R): Cp = 275/264, Gp = 576/619, ±5 = -, ±10 = 0.1, ±20 = BROKE DOWN, Hg(2R): Cp = 202/198, Gp = 99/133, ±5 = 0.1, ±10 = 0.2, ±20 = SONOS, Hg(OR): Cp = 347/327, Gp = 496/554, ±5 = 0.1, ±10 = 0.2, ±20 = SONOS.	
FMF-24;LBTO-1-2	450°C/40 MIN., 50mTORR, 0 RPM, ITO DOTS.	ITO(4, 5): Cp = 183/189, Gp = 1223/1203, ±5 = 0, ±10 = 0, ±20 = 0, ITO(3, 3): Cp = 285/275, Gp = 677/706 ±5 = 0, ±10 = 0, ±20 = 0. Hg(1R): Cp = 487/452, Gp = 1520/1589, ±5 = 0, ±10 = 0, ±20 = 0. Hg(OR): Cp = 130/129, Gp = 62/79, ±5 = 0, ±10 = 0.1, ±20 = 0.2.	
FMF-25;LBTO-1-3	450°C/66MIN., 50mTORR, 10Hz, 0 RPM, TiW 700Å DOTS ON LBTO	TiW(5, 4): Cp = 275/263, Gp = 1078/1098, ±10 = 0, ±20 = 0; TiW(3, 6): Cp = 189/177, Gp = 1587/1551, ±10 = 0, ±20 = 0; Hg(OR): Cp = 153/151, Gp = 176/195, ±10 = 0, ±20 = 0; Hg(3R): Cp = 164/162, Gp = 61/83, ±10 = 0, ±20 = 0;	
FMG-3;BTO-21-2 / PGO-2-3	BTO 450°/5 MIN. 200 mTORR, 0 RPM		
FMG-4;BTO-21-2	R.T./40 MIN. 200mTORR, 10Hz, 0 RPM	Hg(G);Cp = 12.6, ±20 = 2.0, Hg(E); Cp = 19, ±20 = 1.4, Hg(B); Cp = 13.7, ±20 = 1.4.	
FMG-12;LBTO-2-4	450°C/40 MIN. 10Hz, 50 mTORR, 0 RPM		
FMG-1X;BTO-21-4 (FMG-25)	450°C/30 MIN., 200mTORR, 10Hz, 0 RPM	Hg(R);Cp = 201.4, ±10 = 2.45, Hg(Q); Cp = 200.4, ±5 = 1.8, Hg(N); Cp = 202.3, ±20 = 2.4, Hg(L); Cp = 146.6, ±10 = 11, Hg(K); Cp = 144.8, ±5 = 1.8, Hg(E);Cp = 146, ±20 = 14.8, Hg(D); Cp = 223.3, ±5 = 1.68, Hg(C); Cp = 225.3, Hg(B); Cp = 225, ±20 = 2.9.	
FMG-3X;BTO-21-6	450°C/30 MIN., 50mTORR, 10Hz, 0 RPM	Hg(F);Cp = 488, ±10 = 0.45, Hg(E);Cp = 395, ±20 = 0.8, Hg9C); Cp = 293, ±10 = 0.3, Hg(A);Cp = 290, ±20 = 0.7.	
FMF-22;LBTO-2-3	450°C/40MIN., 50mTORR, 0 RPM, 1400Å TiW DOTS ON LBTO	TiW(3, 4): Cp = 490/460, Gp = 1005/1155, ±10 = 0, ±20 = 0, TiW(2, 4): Cp = 637/599, Gp = 850/1139, ±10 = 0, ±20 = 0 Hg(1R): Cp = 344/332, Gp = 652/782, ±10 = 0, ±20 = 0; Hg(2R): Cp = 432/412, Gp = 652/782, ±10 = 0, ±20 = 0;	
FMG-13;LBTO-1-4	550°C/30MIN., 200mTORR, 0 RPM, 600Å QUARTZ CAP (SPUTTERED)	Hg(1R): Cp = 103/103, Gp = 16/27, ±5 = 1.32/2.08 = 0.76, ±10 = 1.06/2.2 = 1.14, ±20 = 1.4/3.52 = 2.12, Hg(2R): Cp = 97/96, Gp = 16/25, ±5 = 1.25/1.92 = 0.67, ±10 = 1.1/2.2 = 1.1, ±20 = 0.8/3.12 = 2.32;	
FMG-2X;BTO-21-5	450°C/30MIN., 50mTORR, 0 RPM, 600Å QUARTZ CAP	Hg(1R): Cp = 213/210, Gp = 158/205, ±5 = 0.2, ±10 = 0.1, ±20 = 0.2, Hg(2R): Cp = 148/148, Gp = 66/108, ±5 = 0.5/0.65 = 0.15, ±10 = 0.5/0.9 = 0.4, ±20 = 0.4.	
FMG-5X;LBTO-2-5	550°C/30MIN., 200mTORR, 0 RPM, 200Å OX BUFFER----AFTER 600Å SPUTTERED QUARTZ CAP	NO CAP: Hg(C);Cp = 151/150, Gp = 16/37; ±5 = -3.22/2.58 = 5.8, ±10 = -2.2/3.2 = 5.4, ±20 = BOOKE DOWN; Hg(1R);Cp = 239/233, Gp = 173/227, ±5 = -0.65/0.1 = 0.75, ±10 = -0.05/0.45 = 0.4, ±20 = BROKE DOWN;-----CAPPED: Hg(CC);Cp = 89/89, Gp = 35/18, ±5 = -1.1/0.35 = 0.75, ±10 = -1.2/0 = 1.2, ±20 = 1.0/1.88 = 0.88, Hg(R);Cp = 114/114, Gp = 16/29, ±5 = -1.68/-0.38 = 1.3, ±10 = -1.84/0 = 1.84, ±20 = -1.0/1.0 = 2.0.	

Wafer #	Experiment	Test Results	Comments
FMG-4X;BTO-31-7	450°C/30 MIN., 50 mTORR, 0 RPM	Hg(C); Cp = 152/147, Gp = 77/98, ±5 = -0.78/3.05 = 3.83; ±10 = 0.6/2.01 = 1.41; ±20 = SONOS; Hg(1R); Cp = 312/298, Gp = 633/689, ±5=0, ±10 = SONOS.	
PENN. ST. BTO ON Si		NO OBSERVABLE HYSTERESIS	
PENN. ST. BTO ON NITRIDE		Hg(L); Cp = 166.5, ±10=0.6, Hg(A); Cp = 180, ±20=5.6.	
PENN. ST. PGO ON Si LG-31		Hg(A); Cp = 34.36/36.27, Gp = 2.3/4.5, ±5=2.6, ±10=5.6, ±20= 7.8, AFTER ANNEAL 500°C/2Hr. 250 mTORR OX. Hg(AA);Cp = 70.84/65.17, Gp = 20/17, ±5=0, ±10=5.5, ±20=8.8	
PENN. ST. PGO ON Si LG-32		Hg(G);±50=25, Hg(F);Cp = 32.42, ±42=22.5, Hg(E);Cp = 32.22, ±35=17.5, Hg(D);Cp = 31.53, ±20=8.5, Hg(C);Cp = 30.32, ±10=3.6 ANNEAL 500°C/2Hr. 250mTORR OX. Cp = 45.64/42.15, Gp = 14/8, ±5=0, ±10=1.9, ±20 = SONOS.	
PENN. ST. PGO ON Si LG-33		NO OBSERVABLE HYSTERESIS	
PENN. ST. PGO ON Si LG-34		Hg(E);Cp = 39.72, ±50=4, Hg(C);±50=6.1	
FMG-6X; BTO-22-1	550°C/30MIN. 200mTORR, 0 RPM.	Hg(C); Cp = 184/120, Gp = 246/342, ±5=6.1, ±10 = 2.1/8.8 = 6.7, ±20 = SONOS; Hg(1R); Cp = 207/198, Gp = 255/355, ±5=0, ±10 = SONOS	
FMF-21; LBTO-2-2	550°C/40MIN. 50mTORR, 0 RPM	Hg(C); Cp+529/507, Gp = 401/622, ±5 = 0.62/0.9 = 0.28, ±10 = 0.4/0.96 = 0.56, ±20 = 2/3.2 = 1.2; Hg(1R); Cp = 208/205, Gp = 16/56, ±5 = 0.15/0.52 = 0.37, ±10 = 0/0.76 = 0.76, ±20 = BROKE DOWN.	
FMG-14; LBTO-1-5	550°C/33MIN. 200mTORR, 0 RPM, BUFFER Ox/NITRIDE OXIDIZED	Hg(1R); Cp = 292/285, Gp = 515/562, ±5=0.25, ±10=0.5, ±20 = 1.0/1.92 = 0.92, Hg(C); Cp = 459/457, Gp = 351/478, ±5=0.3, ±10 = -1.6/-1.06 = 0.54, ±20 = 1.0/2.52 = 1.52.	
FMG-15; NBTO-1-1	OX/NIT. BUFFER, 550°C/30 MIN. 200 mTORR, 0 RPM.; TIW Dots Deposited Through Mask	Hg(C);Cp = 146/146, Gp = 14/29, ±5 = -0.93/0.07 = 1.0, ±10 = -1.24/0.36 = 1.6, ±20 = 0.2/2.6 = 2.4; Hg(R); Cp = 186/185, Gp = 90/119, ±5 = -0.88/-0.28 = 0.6, ±10 = -1.1/0.05 = 1.15, ±20 = 1.0/2.6 = 1.6. TIW(6, 8);Cp = 705/632, Gp = 778/1498, ±5 = -0.55/-0.1 = 0.45, ±10 = -0.8/0.2 = 1.0; TIW(6, 7); Cp = 596/570, Gp = 668/889, ±5 = -0.5/0.2 = 0.7, ±10 = -0.8/0.64 = 1.44, ±20 = -0.48/2.2 = 2.68	
FMG-16; NOPZT-1-1	R.T./30 MIN, 200mTORR, 0 RPM, RTA 650°C/10 SEC O_2.	Hg(C); Cp = 14/13, Gp = 0/1.4, ±5=7.2, ±10=14, ±20 = -0.2/19.2 = 19.4, Hg(1R); Cp = 14/13, Gp = 0.7/1.1, ±5=8.6, ±10 = -3.3/9.5 = 12.8, ±20 = BROKE DOWN	
FMG-17; NOPZT-1-2	550°C/30 MIN, 300 mTORR, 0 RPM	Hg(C); Cp = 36/29, Gp = 6.7/14.3, ±5=1, ±10 = -2.6/7.1 = 9.7, ±20 = BROKE DOWN; Hg(1R); Cp = 66/62, Gp = 10/44, ±5 = -0.95/1.1 = 2.05, ±10 = -1.5/3.6 = 5.1, ±20 = -0.2/4.6 = 4.8	
FMG-18; NBTO-1-2	550°C40 MIN, 200mTORR, 20 RPM QUARTZ CAP = 624Å, TIW DOTS-1620Å	Hg(C); Cp = 275/269, Gp = 365/912, ±5=0.3, ±10=0.6, ±20 = BROKE DOWN, ; Hg(EN); Cp = 161/159, Gp = 14/39, ±5=0.15, ±10=1.0, ±20 = SONOS. TIW(3, 6), Cp = 274/271, Gp = 135/190, ±5 = 0.49/1.61, ±10 = 0.5/1.9 = 1.4, ±20 = 1.6/3.52 = 1.92; TIW(7, 9); Cp = 385/380, Gp = 341/400, ±5 = -3.38/-2.58 = 0.8, ±10 = -3.44/2.16 = 1.28, ±20 = -2.2/-0.2 = 2.0.	
FMG-19;NBTO-1-3	550°C/20 MIN, 200mTORR, 20RPM, 30Hz	Hg(EN); Cp = 193/191, Gp = 46/82, ±5 = -0.2/0.7 = 0.9, ±10 = 0.2/0.7 = 0.5, ±20 = BROKE DOWN; Hg(EEN); Cp = 187/184, Gp = 76/103, ±5 = -0.75/0.48 = 1.23, ±10 = -0.9/0.6 = 1.5, ±20 = -0.2/2.08 = 2.28.	
07X;NBTO-2-1	550°C/40MIN, 200mTORR, 20RPM, 10 Hz, BUFF. = 200Å TO.	Hg(C); Cp = 250/271, Gp = 904/1562, ±5 = -0.1/0.1 = 0.2, ±10 = 0.05/0.76 = 0.71, ±20 = BROKE DOWN, Hg(EN); Cp = 602/561, Gp = 339/705, ±5=0.2, ±10 = -1.0/-0.64 = 0.36, ±20 = BROKE DOWN	
FMG-20;NPZT-1-3	R.T./15MIN. 200mTORR, 0RPM, 10Hz, RTA 650°C/10SEC.	Hg(C); Cp = 41/41, Gp = 0.3/15, ±5=1.75, ±10 = 1..3/3.8 = 2.5, ±20 = SONOS; Hg(1R); Cp = 50/49, Gp = 4/6, ±5=2.4, ±10 = 2/4.6 = 2.6, ±20 = BROKE DOWN.	
7869-1;NBTO-2-2	550°C/40MIN. 200mTORR, 20RPM, 10Hz.		
7869-2;NBTO-2-3	BUFF.OX/NIT/OXIDATION; 500°C/60MIN., 200mTORR, 20RPM, 10Hz.		

Appendix C: Westinghouse 8K FERRAM Test Vehicle Design Description

The 6083 FERRAM maskset consists of four different designs incorporating ferroelectric technology. These four designs are the 6081, 6082, 6084, and 6085 chips. the 6081 chip is the 8K SONOS EEPROM designed by Sandia National Labs (SNL) and successfully built at ATL as the 6071 chip. The 6082 and 6084 chips are the SNL test pattern chip and the Westinghouse- designed test pattern chip, respectively. They were also included on the 6073 maskset as the 6072 and 6074 chips. The 6085 is a SNL-designed test chip consisting of various "SELF-STRESSING" circuits.

The modifications to the 6071, 6072, and 6074 designs consisted mainly of "Biteching" to the new process/ mask layer sequence, and changing the appropriate SONOS-ferroelectric-related layers in the memory devices as well as adding Via and Metal-2 to the designs (the original 4μM SONOS process is a single level metal process). On the 6081 chip, the only modifications made were in the core memory array, where it was necessary to change the poly-memory-gate shapes to Metal-1, and add Via and Metal-2. The following pages describe the design rules, projection plate composition, and contents of the test chips.

C.1 Sandia Design Rules Extracted from "SA3776 DWG" (CALMA L6070)

1) 1.0 P-well
a) min. width . . . . . 22 um
b) min. space . . . . . 26 um
c) rec. space to L2 . . . . . 1 um; butting OK
d) space to L6 . . . . . 19 um

2) 2.0 P+ G.B.
a) min. width . . . . . 4 um
b) min. space . . . . . 16 um

3) 3.0 Thin oxide cut (device window)
a) min. width . . . . . 8 um
b) min. space (n+) . . . . . 8 um
c) min. space (p+) . . . . . 12 um

4) 4.0 Poly 1
a) min. width . . . . . 4 um
b) min. space . . . . . 4 um
c) overlap of L3 (n-ch) . . . . . 0 um
d) overlap of L3 (p-ch) . . . . . 4 um

5) 5.0 N- implant (extended-drain)
a) min. width . . . . . 8 um
b) overlap of L4 (channel length direction) . . . . . 2 um

6) 6.0 P+ implant

a) min. width	8 um
b) min. space	8 um
c) overlap of L3	3 um

7) 7.0 Contact window

a) min. width	3 um
b) min. space	4 um
c) enclosed by L4	2.5 um
d) enclosed by L15	3 um
e) enclosed by L6	2.5 um
f) enclosed by L16	2.5 um
g) space to L4	2.5 um
h) enclosed by L3	2 um
i) enclosed by L8	0.5 um

8) 8.0 Metal

a) min. width	4 um
b) min. space	4 um

9) 9.0 Bond pad etch

a) enclosed by L8	4 um

10) 12.0 Memory gate

a) overlap of L16 (channel width direction)	3.75 um
b) overlap of L15	4 um

11) 15.0 Poly 2

same as for poly 1 (4a-d)

12) 16.0 N+ implant

a) min. width	8 um
b) min. space	8 um
c) space to L2	4 um

13) 18.0 Poly 2 stringer etch

a) min. space	4 um
b) overlap of L15	2 um
c) space to L4	2 um

14) 23.0 Field adjust implant

a) min. space	4 um
b) overlap of L3 (p-ch)	5 um
c) overlap of L1	11 um

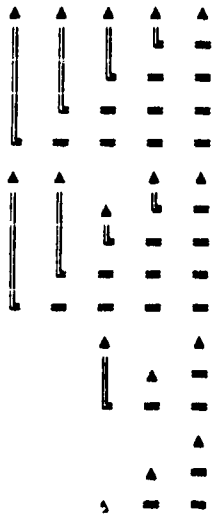
C.2 Westinghouse 4 um FE/SONOS/CMOS CALMA and Mask Levels for Ferroelectric Version of Sandia EEPROMs. (Calma Libraries L6080, L6081, L6082, L6084)

WEC CALMA	Fill Code	Mask Level	Mask Polarity	Description
0	NA	0.0	Clear	Alignment
†1	12	1.0	Clear	N-well
2	16	2.0	Clear	P-well
3	NA	3.0	Opaque	N+ Guard band
4	71	4.0	Clear	P+ Guard band
5	11	5.0	Opaque	Device window
6	104	6.0	Opaque	Non-mem poly
7	5	7.0	Clear	N- implant
8	NA	8.0	Clear	N+ implant
9	90	9.0	Clear	P+ implant
*10	10	10.0	Clear	Contact
11	91	11.0	Clear	Memory window
12	83	12.0	Opaque	FE removal
*13	76	13.0	Opaque	Metal 1
14	96	14.0	Clear	Via
*15	NA	15.0	Opaque	Metal 2
16	82	16.0	Clear	Overcoat

† The N-well layer (L1) is generated by DRC program.

* DRC sizing required.

C.3 Alignment Tolerances



L#	Level Name	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	Alignment		1	1	1	1	1	2	2	3	2	2	3	4	3	4	5	6
1	N-Well			2	2	2	2	3	3	4	3	3	4	5	4	5	6	7
2	P-Well				2	2	2	3	3	4	3	3	4	5	4	5	6	7
3	N+ G.B.					2	2	3	3	4	3	3	4	5	4	5	6	7
4	P+ G.B.						2	3	3	4	3	3	4	5	4	5	6	7
5	Dev. Window							1	1	2	1	1	2	3	2	3	4	5
6	Poly								2	3	2	2	3	4	3	4	5	6
7	N-Implant									3	2	2	3	4	3	4	5	6
8	N+Implant										3	3	4	5	4	5	6	7
9	P+Implant											2	3	4	3	4	5	6
10	Contact												1	2	1	2	3	4
11	Mem.Window													1	2	3	4	5
12	F.E.Removal														3	4	5	6
13	Metal 1															1	2	3
14	Via																1	2
15	Metal 2																	
16	Overcoat																	

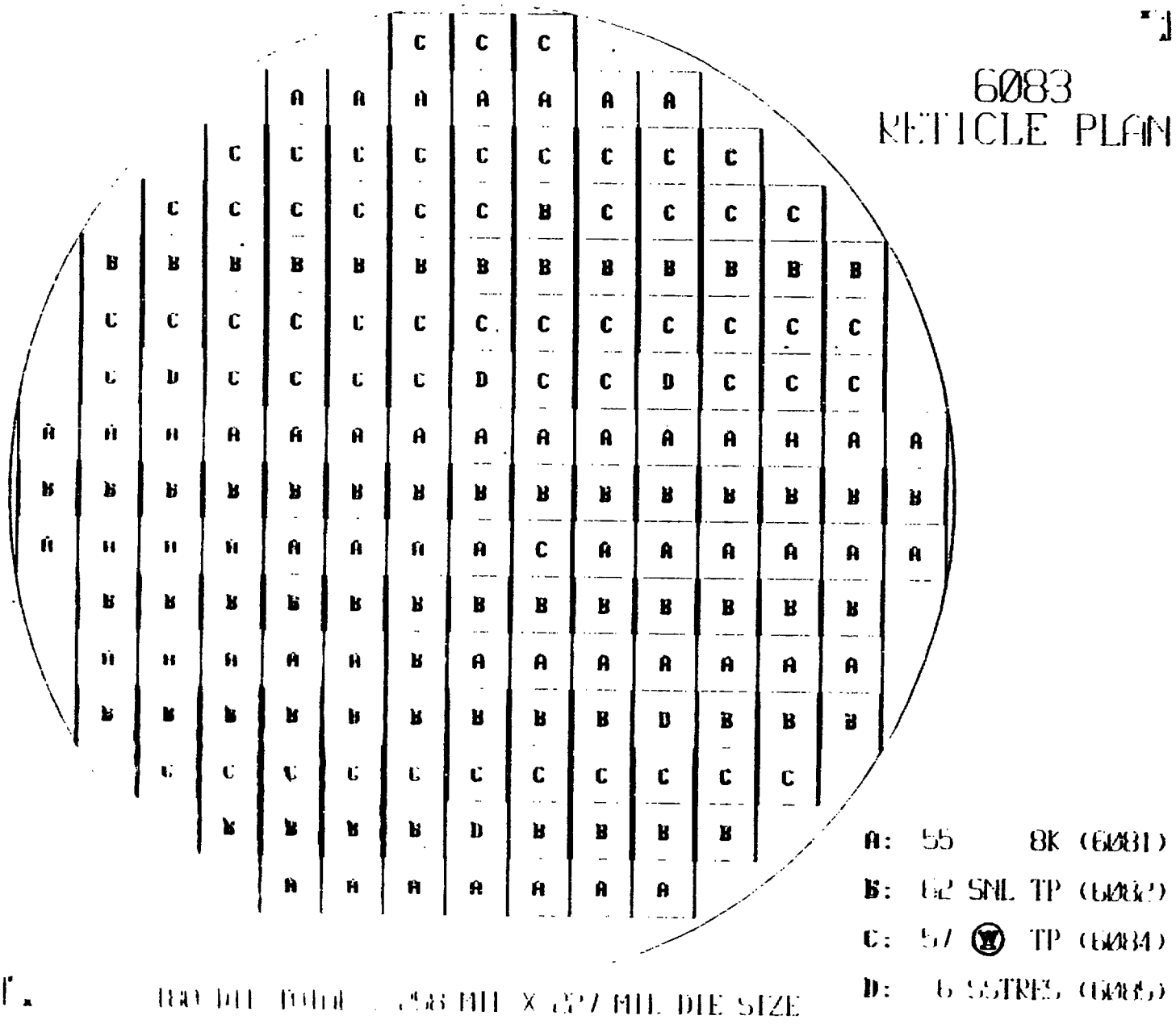


Figure C-1: FERRAM ICAL Test Vehicle Reticle Plan

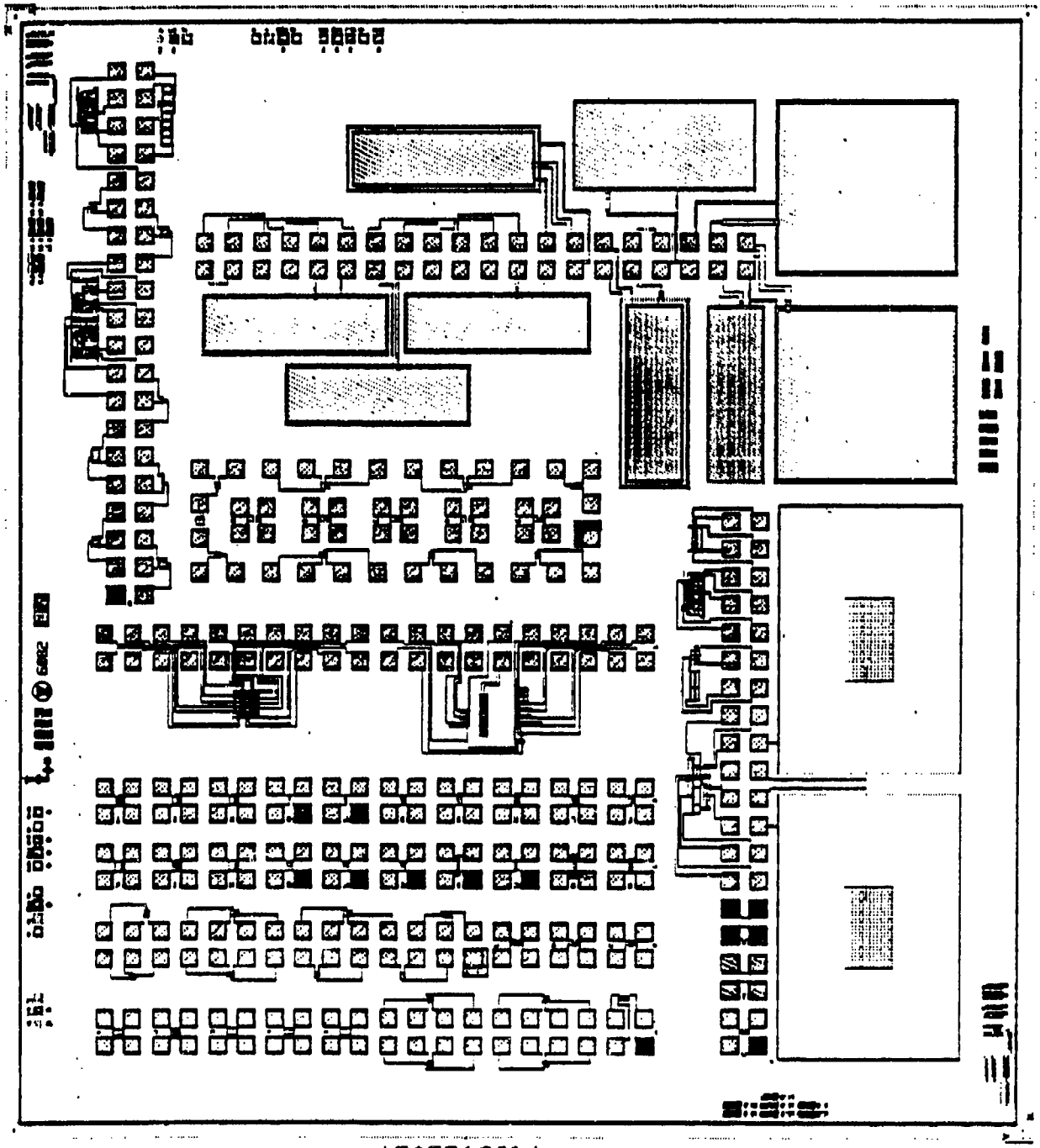


Figure C-2: The 6082 FERRAM/SNL ICAL Test Chip

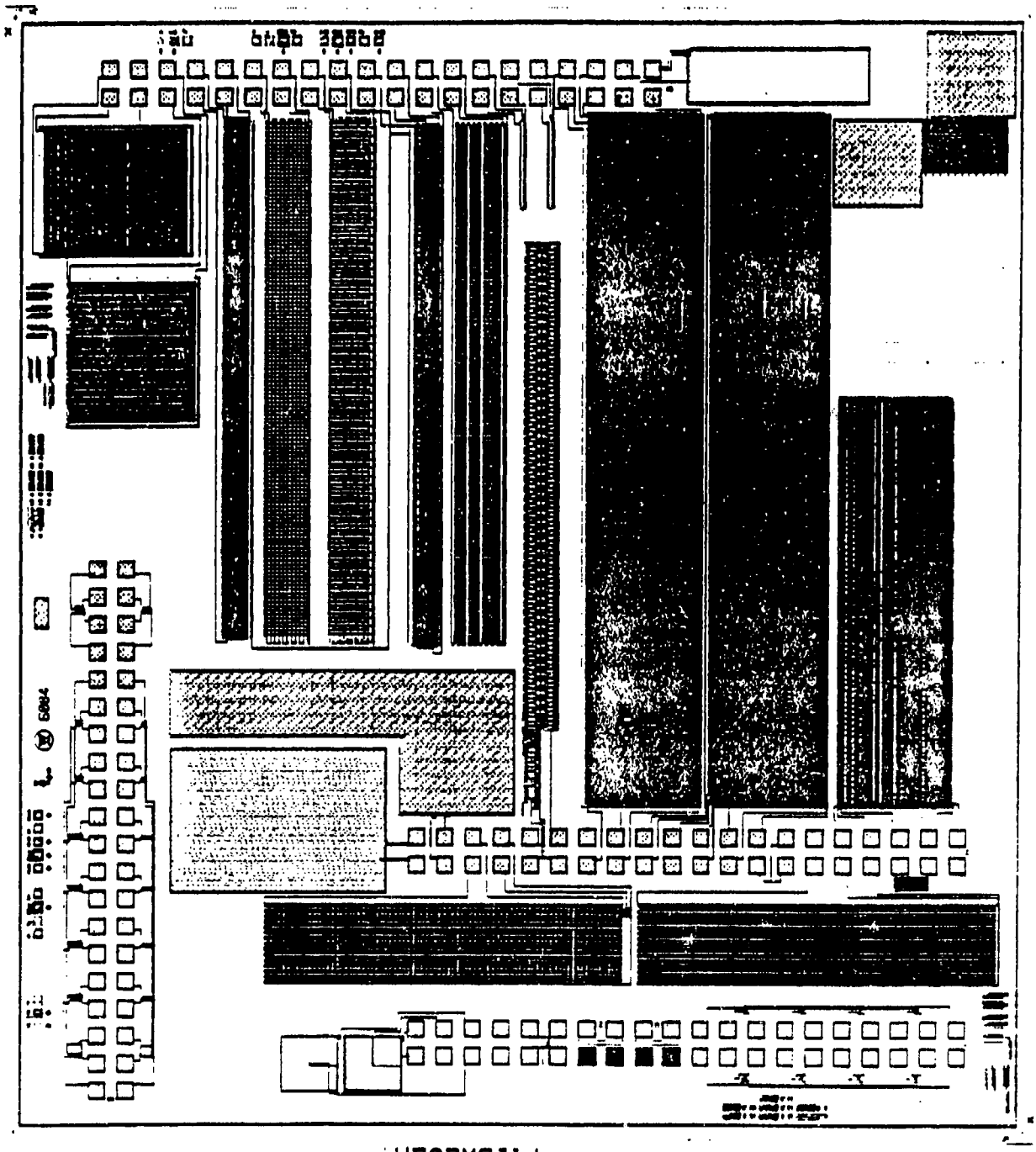


Figure C-3: The 6084 FERRAM/WEC ICAL Test Chip

C.4 Description of "TA751_ATL" 4 μm FENV/CMOS Test Chip

CALMA Library : L6082
CALMA Structure : TA751_ATL

Following is a listing of test structures included in the nine padsets:

(1) TP13_ATLP

This padset consists of SNL Module-13 structures (eight 8/4 FENV transistors) and also SCR structures C, D, and E (Tx= 13, 10, and 8 μm, respectively). See figures 1-1 and 1-2.

FENV pinouts (one pin for source and P-well)

Source	Gate	Drain	P-well
20	18	19	20
23	21	22	23
13	11	12	13
10	8	9	10
34	32	33	34

FENV pinouts (separate pins for source and P-well)

Source	Gate	Drain	P-well
16	14	15	17
26	24	25	27
30	28	29	31

N-substrate pin 7

SCR C:	N-sub 5	P+ 6	P-well 36	N+ 35
SCR D:	N-sub 3	P+ 4	P-well 38	N+ 37
SCR E:	N-sub 1	P+ 2	P-well 40	N+ 39

(2) RESIST_CAP_ATLP

This padset consists of the six SNL capacitors (A, B, C, D, E, and F), poly Van der Pauw (pins 27-32... see figure 10), metal Van der Pauw (pins 21-26), N+ resistor (pins 19, 20), P+ resistor (pins 36, 37), and the current mirror circuit.

A. Capacitor A is a metal gate capacitor in p-well with P+/P+ GB under gate. Its area is 0.5 x 10^6 μm^2. (Pins 4,3).

B. Capacitor B is a metal gate capacitor in p-well with P+/P+ GB under gate. Its area is 0.3 x 10^6 μm^2. (Pins 4,5,6 P-well).

C. Capacitor C is a metal gate capacitor in p-well with P+ GB under gate and a P+ halo around gate. Its area is 0.3 x 10^6 μm^2. (Pins 34,33,7 P-well).

D. Capacitor D is a poly 1 capacitor in a blanket p-well and guardband substrate with P+ halo. Its area is 0.3 x 10^6 μm^2. (Pins 2,1).

E. Capacitor E is a poly 1 capacitor in p-well with P+ halo. Its area is 1.0×10^6 μm^2. (Pins 40,1).

F. Capacitor F is a poly 1 capacitor in n-well with N+ halo. Its area is 1.0×10^6 μm^2. (Pins 39,38).

(3) A_TO_J_ATLP

This padset consists of SNL transistors A to J (ten total).

A. An NMOS transistor with W/L of 40/4 (C4810_CEL).

source 2 gate 40 drain 39 P-well 1

B. An NMOS transistor with W/L of 100/10 (C4820_CEL).

source 4 gate 38 drain 37 P-well 3

C. A PMOS transistor with W/L of 40/4 (C4830_CEL).

source 6 gate 36 drain 35 N-sub 5

D. A PMOS transistor with W/L of 100/10 (C4840_CEL).

source 8 gate 34 drain 33 N-sub 7

E. A PMOS poly field oxide transistor with W/L of 22/14 (C4850 CEL).

source 10 gate 32 drain 31 N-sub 9

F. A PMOS metal field oxide transistor with W/L of 22/14 (N+ GB under gate) (C4860_CEL).

source 12 gate 30 drain 29 P-well 11

G. A PMOS metal field oxide transistor with W/L of 22/14 (no N+ GB under gate) (C4910_CEL).

source 14 gate 28 drain 27 N-sub 13

H. An NMOS metal gate transistor with W/L of 26/18 (no GB under gate) (C4920_CEL).

source 16 gate 26 drain 25 P-well 15

I. An NMOS poly transistor with W/L of 26/18 (no GB under gate). (C4930_CEL).

source 18 gate 24 drain 23 P-well 17

J. An NMOS metal gate transistor with W/L of 26/18 (GB under gate). (C4940_CEL).

source 20 gate 22 drain 21 P-well 19

(4) K_TO_T_ATLP

This padset consists of SNL transistors K to T (ten total).

K. An N-FENV transistor with W/L of 8/4 (C4950_CEL).

P-well 1 source 2 drain 39 gate 40

L. An NMOS poly field oxide transistor with W/L of 26/18 (no GB under gate) (C4960_CEL).

P-well 3 source 4 drain 37 gate 38

M. An NMOS N-extender transistor with W/L of 40/4. This transistor differs from A in that the area of the source and drain is larger. Space from oxide to poly is 11 microns instead of 8 microns(C5010_CEL).

source 6 gate 36 drain 35 P-well 5

N. An NMOS N-extender transistor with W/L of 30/3 (C5020_CEL).

P-well 7 source 8 gate 34 drain 33

O. An NMOS N-extender transistor with W/L of 20/2 (C5030_CEL).

P-well 9 source 10 gate 32 drain 31

P. A PMOS transistor with W/L of 30/3 (C5040_CEL).

N-sub 11 source 12 gate 30 drain 29

Q. A PMOS transistor with W/L of 20/2 (C5050_CEL).

N-sub 13 source 14 gate 28 drain 27

R. An NMOS metal field oxide transistor with W/L of 26/18 (no GB under gate) (C5060_CEL).

P-well 15 source 16 gate 26 drain 25

S. An NMOS metal field oxide transistor with W/L of 26/18 (GB under gate) (C5070_CEL).

P-well 17 source 18 gate 24 drain 23

T. An NMOS poly field oxide transistor with W/L of 26/18 (GB under gate) (C5080_CEL).

P-well 19 source 20 gate 22 drain 21

(5) C3542C_ATLP

The following structures are included:

* analog cell C
* exploded CM5X_CEL (from analog cell B)
* exploded TRIGGER_CEL (from analog cell B)
* n-channel transistor (from analog cell A)
* N- implant only transistor (from analog cell B)

a) 18/30 N- implant only:	source 6	gate 8	drain 7
b) 7/11 P+ xtr:	source 12	gate 14	drain 13
c) 7/90 P+ xtr:	source 15	gate 17	drain 16
d) 9/30 N- implant only:	source 18	gate 20	drain 19
e) 18/30 N- implant only:	source 24	gate 22	drain 23
f) 18/60 N- implant only:	source 27	gate 25	drain 26
g) 10/30 NMOS:	source 36	gate 34	drain 35

N-sub 21

(6) DIODES_ATLP

This padset consists of the following:

* C2210C_CEL (p-channel 40/4 metal transistor with no memory cut)
  N-sub 20 source 19 gate 21 drain 22
* N+ to P-well diode
  N+ 10 P-well 9
* P+ to N-sub diode
  P+ 11 N-sub 12
* Metal Van der Pauw (structure Y)
  pins 17, 18, 23, 24
* Poly Van der Pauw (structure W)
  pins 15, 16, 25, 26
* INV_CEL (from analog cell A)
* CM5X_CEL (from analog cell A)
* LSHIFT_CEL (from analog cell A)
* TRIGGER_CEL (from analog cell A)

(7) TP3_9_ATLP

This padset includes SNL Module 3 (small memory array) and Module 9 (n and p-channel transistors). Module 3 is a 4 row by 3 bit memory array. The schematic for Module 3 is shown in figure 7-1. It contains a "dummy" row as can be found in the SA2099, SA3612, and SA5182. In this case, however, both the MNOS and NMOS gates are tied to the p-well, whereas in the actual array it is just the MNOS gates. The sizes, in microns, of the transistors are shown in parentheses. The width of the transistor is shown before the '_' whereas the length of the transistor follows the '_'. The alpha character is the transistor type; P for P-channel, N for N-channel.

	Drain	Gate	Source	P-well
8/2.4 N-FENV	9	10	31	36
8/4 NMOS	3	37	31	36
100/10 NMOS	2	37	31	36
50/5 NMOS	1	37	31	36
40/4 NMOS	40	37	31	36
2 series				
4/16 NMOS	39	37	31	36
4/16 NMOS	38	37	31	36

	Drain	Gate	Source	N-sub
100/10 PMOS	32	35	31	6
40/4 PMOS	34	35	31	6
40/4 PMOS	33	35	31	6

with 2x drain contact-to-gate space

(8) TP14_ATLP

This has the same structures as SNL Module 14 except for two fewer of transistors C2210A_CEL and C2210_CEL, it also includes transistors 1-5 below. See figure 8.

1. An NMOS poly gate oxide transistor with W/L of 26/26 (GB under gate) (C5081_CEL).
   source 21 gate 19 drain 22 P-well 20
2. An NMOS metal field oxide transistor with W/L of 26/18 (GB under gate) (C5082_CEL).
   source 23 gate 17 drain 24 P-well 18
3. An N-FENV metal gate oxide transistor with W/L of 26/20.6 (GB under gate) (C5083_CEL).
   source 25 gate 15 drain 26 P-well 16
4. An NMOS metal gate oxide transistor with W/L of 26/20.6 (GB under gate) (C5084_CEL).
   source 27 gate 13 drain 28 P-well 14
5. An N-FENV metal gate oxide transistor with W/L of 26/26 (no GB under gate) (C5085_CEL).
   source 29 gate 11 drain 30 P-well 12

FENV N-channel transistors

source	gate	drain	P-well
8	10	9	7
33	31	32	34
4	6	5	3
37	35	36	38

FENV P-channel transistors

source	gate	drain	N-sub
40	2	39	1

(9) C2200_CEL

This is kept exactly as SNL Module 13, it is NOT padded out to 2x20 padset per SNL's request. TP13 ATLP is the Westinghouse-testable version of this Module.

C.5 Description of L6084 " WECPM_ATL" 4 μm FENV/CMOS Test Chip

List of structures placed in L6084 "WECPM_ATL":

1) M_POL_CWSTR_ATL : a metal to poly contact string consisting of 4800 3μm X 3μm
(padset A) contacts (pins 4,5), and tap for 160 contacts (pins 5,6)

2) M_NPL_CWSTR_ATL : a metal to N+ contact string consisting of 4800
(padset A) 3 μm X 3 μm contacts (pins 23, 24), and a tap for 160 contacts (pins 18, 23). P-well contact is pin 17.

3) M_POL_RSCT_ATLP : a poly resolution/continuity structure consisting of vertical
(padset A) poly serpentine inside poly comb (LW-4μm, LS-4μM) over horizontal device window stripes (LW-8μm, LS-8μM) over P-well with P-well contact.
poly combs : pins 36, 38
poly serp : pins 37, 39
P-well : pin 40

4) MOVERP_RSCT_ATL : a metal over poly resin/cont structure consisting of vertical
(padset A) metal serpentine inside comb (LW-4μm, LS-4μm) over horizontal poly serp/comb (LW-4μm, LS-4μm)
poly serp : pins 12, 33
poly combs : pins 29, 30
metal serp : pins 9, 10
metal combs : pins 31, 32

5) M_RSCT_NOM_ATL : a vertical metal serp/comb structure (LW-4μm, LS-4μm)
(padset A) metal serp : pins 13, 14
metal combs : pins 27, 28

6) DCHAIN_ATL : a gate delay chain consisting of 100 inverter gates
(padset A) (Wp-32μm, Wn-15μm)
in 26 out 16 vdd 15 vss 25

7) MODEL_XTRS_ATLP : various sized NMOS and PMOS transistors for modeling
(padset B) purposes, common source and common substrate connected 50x50, 50x5, 50x4, 50x3, 50x2, 12x4, 8x4

NMOS

W/L	G	D
50/50	22	23
50/5	24	25
50/4	26	27

PMOS

W/L	G	D
50/50	19	18
50/5	17	16
50/4	15	14

50/3	28	29	50/3	13	12
50/2	30	31	50/2	11	10
12/4	32	33	12/4	9	8
8/4	34	35	8/4	7	6
source 36			source 5		
P-well 21			N-sub 20		

*40/4 NMOS annular transistor:
source 40 drain 39 gate 38 P-well 37

*40/4 PMOS annular transistor:
source 1 drain 2 gate 3 N-sub 4

8) SONOS_XTRS_ATLP (padset C) : various sized N-FENV transistors, common source and common substrate connected:
10x5, 10x4, 10x3, 10x2
a P+, an N+, a Poly, and a Metal 1 Kelvin contact a 26x26 PMOS transistor with N+ G.B. under gate

N-FENV			P-FENV		
W/L	G	D	W/L	G	D
10/5	2	3	10/5	39	38
10/4	4	5	10/4	37	36
10/3	6	7	10/3	35	34
10/2	8	9	10/2	33	32
source 10			source 31		
P-well 1			N-sub 40		

* P+ : pins 11, 12
M1 : pins 30, 29

* poly : pins 13, 14
M1 : pins 28, 27

* M2 : pins 15, 16
M1 : pins 26, 25

* N+ : pins 17, 18
M1 : pins 24, 23

* 26/26 PMOS : source 20 gate 22 drain 21 N-sub 19

9) SRP_ATL : spreading resistance probe structure (N-well, P-well, N+G.B. P+ G.B., N-implant, N+implant, P+implant; all 125μm x 800μm

10) JC_TBS : TBS structure (a 25 x 25 array of 8μmx4μm PMOS transistors)

11) JC_VERTNPN : a vertical NPN device
(padset A) N-sub : pin 7
P-well : pin 9
N+ : pin 24

12) JC_MPCAP : a 1000μmx1000μm poly (pin 21)
(padset A) to metal one (pin 20) capacitor.

APPENDIX D: PULSED LASER DEPOSITION (PLD) PUBLICATIONS

Integrated Ferroelectrics, 1992, Vol. 1, pp. 213–222
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PULSED LASER DEPOSITION (PLD) OF ORIENTED BISMUTH TITANATE FILMS FOR INTEGRATED ELECTRONIC APPLICATIONS

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Abstract In this paper we describe recent successes of growth of epitaxial bismuth titanate (BTO) films by pulsed laser deposition (PLD) suitable for electro-optic and electrical switching device structures, and fabrication of an improved gate structure for a ferroelectric memory FET (FEMFET). TEM and x-ray results indicate that excellent crystalline quality BTO films were achieved on $LaAlO_3$. Polarization switching was demonstrated for BTO capacitors with epitaxial superconducting $YBa_2Cu_3O_7$ as the lower electrode. Using an SiO_2 buffer layer, a BTO/Si structure was fabricated and direct charge modulation in the Si by polarization reversal in the BTO was demonstrated.

INTRODUCTION

Since the growth of stoichiometric[1] and epitaxial[2] films of ferroelectric bismuth titanate, $Bi_4Ti_3O_{12}$ (BTO), by rf sputtering was demonstrated in these laboratories, it has become apparent that films of this material offer several important and unique application opportunities in integrated electronics. These potential applications derive from an unusual combination of several useful properties, such as high electro-optic contrast switching effects under low address fields, demonstrated feasibility of direct integration in silicon FET's as a gate dielectric, and the capability of high specific capacitance associated with low dielectric loss.

The unique electro-optic switching behaviour of BTO crystals has already been duplicated in sputtered epitaxial films to achieve an X-Y addressed display.[3] For this purpose, single-domain film

structures were required with the spontaneous polarization and optic axis lying in the plane of the film. Similarly, experimental Si-based memory structures were successfully fabricated in which switching between the "zero" and "one" states was produced by reversing the ferroelectric polarization in the BTO gate dielectric of an FET.[4] Finally, high-value (0.3 $\mu F/cm^2$) and low-loss (tan δ = 0.005) capacitors were fabricated on metallized silicon substrates at growth temperatures of about 550°C.

Despite these early successes with sputtered films of BTO, serious growth problems were often encountered due to the low deposition rates available, to the Bi_2O_3-rich composition needed in the target, and to the influence of ion bombardment at the substrate. These effects led to particle formation in the films,[1] cracking of epitaxial layers and interdiffusion with the substrate material.[4] In particular, the the interdiffusion with Si surfaces produced tunneling barriers which promoted anomalous, injection-dominated switching in ferroelectric FET memories (FEMFETs).

Recent studies by Buhay et al.[5,6] and also by Ramesh et al.[7] have demonstrated that high-quality films of BTO can be grown on a variety of substrates, and epitaxially on MgO, by pulsed laser deposition (PLD), using approaches similar to those developed for growth of oxide superconductor layers. We have shown that, unlike the situation with sputtering, stoichiometric targets can be used to yield particle-free films of excellent structural and electrical quality, displaying essentially bulk ferroelectric properties. Moreover, growth could be achieved at high rates and low substrate temperatures under conditions compatible with the processing needs of semiconductor integrated circuits. In the present paper we describe recent extensions of the PLD method to epitaxial growth of BTO films suitable for electro-optic and electrical switching device structures, and to fabrication of improved gate dielectrics for FEMFET arrays.

EXPERIMENTAL

Film deposition was carried out using a Lumonics HyperEx-460 industrial laser operating on the KrF transition at 248 nm at pulse energies up to 300 mJ, with pulse durations of 20-30 nsec and repetition rates up to 65 Hz. The films were prepared, as previously

described,[5,6] with an estimated laser fluence, on the stoichiometric BTO ceramic target, of 2 J/cm^2, laser pulse rate of 10 Hz, and oxygen flowing at a pressure of 200 mTorr. For these conditions, and for nominal substrate temperatures used in the range 500-700°C, films were grown to a typical thickness of 1 micron, at a rate of about 30 nm/min. Structural characterization was performed using X-ray diffractometry and rocking curve measurements, X-ray oscillation and Weissenberg patterns, electron diffraction and transmission electron microscopy (TEM). The composition of the layers was evaluated using electron microprobe techniques. Capacitance and conductance measurements were made over the frequency range 10-500 kHz using a Boonton bridge, and ferroelectric hysteresis studies were carried out with a modified Sawyer-Tower circuit.

The epitaxial BTO films studied here included BTO/$LaAlO_3$(001), bi-layer structures of the type BTO/YBCO/$LaAlO_3$(001) and BTO/YBCO/YSZ(100) and tri-layer structures of the type BTO/$SrTiO_3$/YBCO/$LaAlO_3$(001) and BTO/$SrTiO_3$/YBCO/YSZ(001). MIS structures involving BTO deposits on thin (100-200A) buffer layers of CaF_2 and SiO_2 on (001)Si were also prepared for electrical C-V measurements. In the bi- and tri-layer structures the epitaxial films of YBCO ($YBa_2Cu_3O_7$) and $SrTiO_3$ were pre-deposited in a separate vacuum system by rf magnetron sputtering. In the case of silicon substrates, CaF_2 and SiO_2 were pre-deposited by vacuum sublimation and thermal oxidation respectively.

RESULTS

Epitaxial Structures on (001)$LaAlO_3$ and Zirconia (YSZ) Substrates

$LaAlO_3$(001) substrates provide an excellent lattice match to the paraelectric (high-temperature) tetragonal (001) face of BTO (~1% compared to 2% for $SrTiO_3$ and 10% for MgO). BTO films were grown at nominal substrate temperatures of 600, 675, and 750°C. Examination by X-ray diffractometry indicated in each case primarily the ferroelectric orthorhombic phase with a very strong c-axis (normal) crystal orientation. X-ray Weissenberg patterns confirmed a well-oriented epitaxial structure with BTO(001) // $LaAlO_3$(001), and with a-b twinning in the (001) plane of the substrate, i.e. BTO[100] and [010] // $LaAlO_3$[110] (see Figure 1). X-ray rocking curve studies

FIGURE 1 X-ray Weissenberg pattern of BTO film grown at 750°C on $LaAlO_3$(100).

yielded FWHM values depending sensitively on growth temperature. Increasing the growth temperature from 600 through 675 to 750°C produces a dramatic improvement in film quality, with the corresponding FWHM widths changing as shown in Figure 2.

TEM studies performed on the 750°C sample gave confirmation of the twinned structure (Figure 3). Small area diffraction (SAD) measured in the twinned areas (different contrast regions in Figure 3a and 3b) showed the orientations of the a-b axes differ by 90° rotation and the twin boundaries are parallel to the film axes. Two types of boundaries observed were: (a) straight boundaries (Figure 3a) probably associated with formation of twins directly at the growth temperature near the Curie point (Tc) transition, and (b) curved boundaries (Figure 3b) tentatively attributed to formation of ferroelectric domains on cooling below Tc. These results suggest that the true film growth temperature may differ from that measured at the heater surface by as much as 60-80°C. However, single domain film structures of quality adequate for optical waveguide modulators can probably be achieved by growing further above the Tc transition.

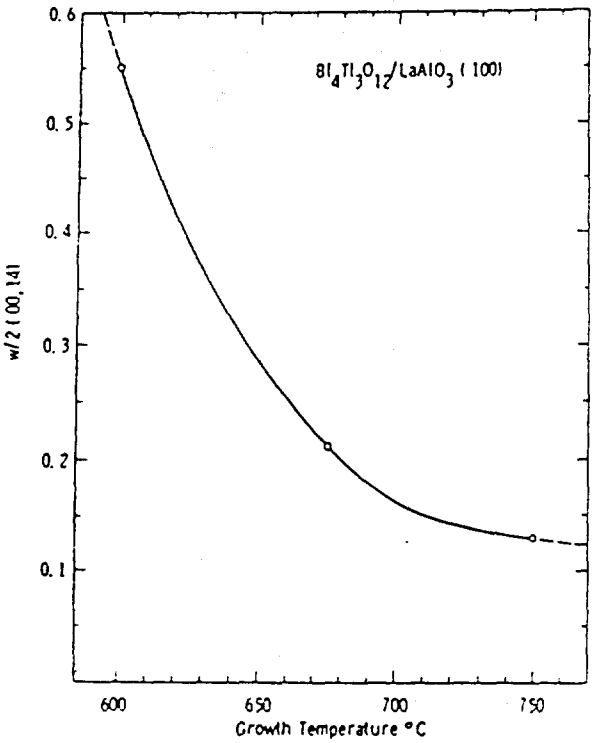

FIGURE 2 FWHM of X-ray rocking curve about (0014) versus temperature for BTO film of Figure 1.

Good-quality epitaxy of BTO was also obtained in the various bi- and tri-layer, (001) oriented samples on $LaAlO_3$ and yttria-stabilized ZrO_2. In each case, the BTO c-axis was normal to the substrate plane. In the case of the structures with YBCO, a narrow temperature window was established for BTO growth which led to ferroelectric behaviour without degradation of the superconducting transition at 90K in the YBCO. Using gold top electrodes, hysteresis loops of the type shown in Figure 4 were displayed. The measured polarization at partial saturation (4.3 $\mu C/cm^2$) agrees well with the bulk crystal value parallel to the c-axis, but the coercive field (200-300 kV/cm) is anomalously high. These structures provide a unique example of highly-ordered, lattice-matched electrode/ ferroelectric interfaces, which should possess high stability and reduced fatigue, for example, in semiconductor memory configuration.

(a)

(b)

FIGURE 3 TEMs of same BTO film of Figures 1 and 2: (a) straight twin boundaries; (b) curved twin boundaries.

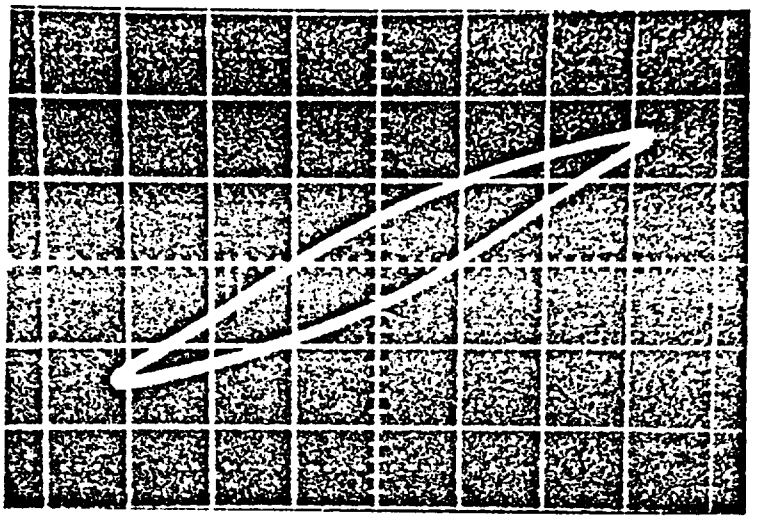

FIGURE 4 Hysteresis loop measured at 2 kHz for BTO/$SrTiO_3$/YBCO/YSZ structure. Scale: Vertical, 3.5 $\mu C/cm^2$ per large division; Horizontal, 310 kV/cm per large division.

MIS Structures on Silicon

These structures were explored with the aim of establishing whether PLD films of BTO on Si (with or without dielectric buffer layers) might exhibit switching behaviour free from the charge injection effects encountered previously with sputter-deposited BTO layers. BTO structures prepared by PLD without such buffer layers were in fact found to display injection effects, and will not be discussed further here. The results for BTO structures using CaF_2 or SiO_2 as a buffer layer are discussed further below. The BTO/CaF_2 dielectric structure was deposited on a standard VHSIC CMOS wafer (4-8 Ohm-cm p^-Si epi-layer grown on 0.005-0.02 Ohm-cm p^{++}Si substrate). The BTO/SiO_2 structure was deposited on a gridded (6 μm wide N^+ lines spaced 60 μm apart) standard wafer. In both cases a mercury probe having an area of 0.64×10^{-3} cm^2 was used as the top electrode. The BTO/CaF_2 and BTO/SiO_2 test structures and C-V plots are shown in Figures 5 and 6 respectively.

The test structure of Figure 5 was intended to simulate a FEMFET that is incorporated in á P-well CMOS VLSIC memory, i.e., an N-channel FEMFET. Thus, as the gate voltage sweeps from +5 volts to -5 volts in the C-V hysteresis curve of Figure 5, the capacitance of the gate dielectric stack increases as the depletion-region "inversion charge

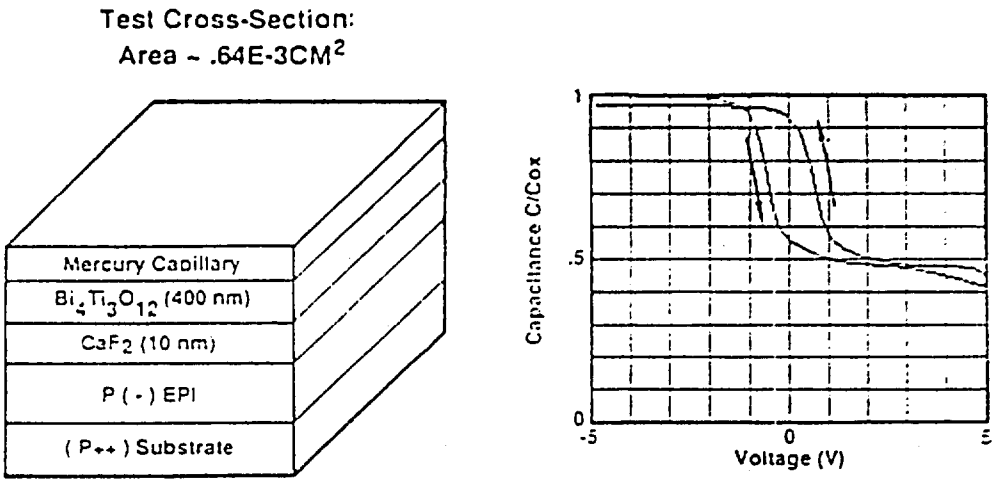

FIGURE 5 Test structure and C-V hysteresis result for a CaF_2-buffered BTO film on a standard VHSIC CMOS Si wafer.

layer" becomes an "accumulation charge layer", with the disappearance of the series depletion-region capacitance at approximately the threshold voltage. The shift of the threshold from enhancement mode toward depletion mode in response to negative programming (V_{gate} = -5 volts) indicates positive charge trapped near the semiconductor-gate-dielectric interface rather than a negative sheet of charge that would arise if the negative gate reoriented the ferroelectric dipoles to the positive end adjacent to the negative gate. Thus, the polarity of the threshold shift of the C-V plot (arrow directions shown in Figure 5) for the BTO/CaF_2 structure is consistent with the interpretation that charge is being injected from the Si surface into traps near the BTO/CaF_2 interface (injection type on/off switching).

The test structure of Figure 6 includes more of the FEMFET (namely, the NMOST source/drain implants) to greatly facilitate both pulsed and endurance C-V measurements. Consequently, in the C-V plot of Figure 6, the lower apparent capacitance is shunted back to its higher value by an inversion layer whose source of electrons is the source/drain grid implant that is shorted to the substrate. Only during the transition from an accumulation layer (arising from a negative gate bias) to the inversion layer (associated with a positive gate bias) does the gate capacitance drop to a minimum value at a gate voltage near the effective threshold voltage. Thus, from the gridded-

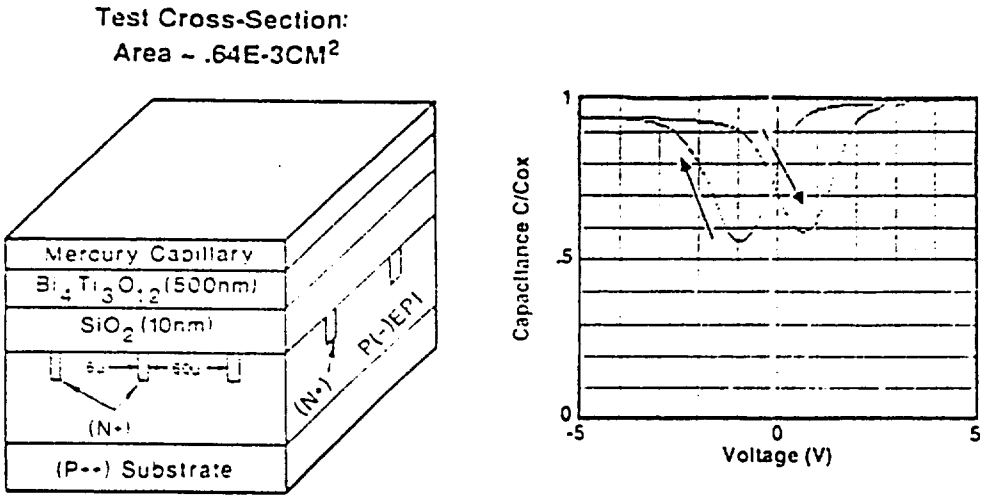

FIGURE 6 Test structure and C-V hysteresis result for a SiO_2-buffered BTO film on a gridded wafer.

wafer C-V hysteresis curve of Figure 6, the negative memory-gate programming gives the enhancement mode (normally OFF) while the positive memory gate programming gives the depletion mode (normally ON). The polarity of the threshold shift of the C-V plot (arrow directions shown in Figure 6) for the BTO/SiO_2 structure is opposite of that in Figure 5 and is indicative of ferroelectric switching. That is, for 5-volt programming, the reversible ferroelectric polarization dominated when charge tunnelling and trapping was inhibited by the good quality SiO_2 buffer layer. The CaF_2 buffer layer, however, permitted so much charge tunnelling and trapping that it completely dominated over any likely ferroelectric polarization switching. The faster BTO ferroelectric switching is the desired goal for NDRO FERRAM operation.

SUMMARY

Pulsed laser deposition has been used, in conjunction with a stoichiometric target, to deposit a variety of BTO epitaxial structures on (001) crystal substrates of $LaAlO_3$ and YSZ. By controlling the growth temperature, it was possible to form high-quality BTO capacitors with epitaxial superconducting YBCO as the lower electrode, and to demonstrate polarization switching. Using

SiO_2 buffer layers, BTO/Si MIS structures also were grown, and the feasibility of direct charge modulation in the Si by polarization reversal in the BTO was demonstrated.

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Pulsed laser deposition and ferroelectric characterization of bismuth titanate films

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Stoichiometric films of bismuth titanate, $Bi_4Ti_3O_{12}$, have been grown for the first time by the technique of pulsed excimer laser deposition. Ferroelectric films were obtained at temperatures as low as 500 °C on Si(100), MgO(110), and Pt-coated Si(100) substrates. Hysteresis measurements using a Pt-coated Si sample yielded a saturation polarization value of about 28 $\mu C/cm^2$, consistent with a randomly oriented titanate film structure. A preliminary metal-insulator-semiconductor sandwich structure of the form $Bi_4Ti_3O_{12}$-CaF_2(100 Å)-Si was grown and used to examine polarization induced memory switching effects.

In previous studies[1,2] it has been demonstrated that films of bismuth titanate, $Bi_4Ti_3O_{12}$, with high structural, electrical, and optical quality can be prepared by rf sputtering. For sputtered films it was not possible to grow crystalline films of the ferroelectric composition at elevated substrate temperatures without using excess bismuth oxide in the ceramic target. Also, since sputtering is a slow process, interdiffusion with the substrate can occur at the high temperatures needed for single-phase growth. Recently, laser deposition has emerged as a promising technique for the stoichiometric growth of perovskite-type high-temperature superconductor films.[3,4] Efforts have also been made to apply this deposition approach to ferroelectric mixed oxides, such as lead zirconate titanate (PZT), but composition control difficulties have arisen due to the high volatility of the PbO constituent.[5] No reports have yet appeared on the use of this technique for the growth of $Bi_4Ti_3O_{12}$ films.

The fact that ferroelectric $Bi_4Ti_3O_{12}$ displays a *c*-axis polarization component with a low coercive field renders it attractive as a gate dielectric film in ferroelectric field-effect transistor (FET) semiconductor memories requiring low drive power. Earlier attempts were made by Wu[6] and by Sugibuchi *et al.*[7] to achieve such FET structures using rf sputtering to deposit the titanate film. However, the high processing temperatures (~675 °C) and low deposition rates used for titanate film growth led to interdiffused structures characterized by the appearance of oxide tunneling barriers at the semiconductor interface. A key motivation for the present study was to explore the feasibility of using pulsed laser deposition for rapid growth of the titanate at low substrate temperatures, in order to obtain optimum semiconductor/dielectric interface properties.

The pulsed laser used was a Lumonics Hyper EX-460 industrial excimer laser operating on the KrF transition at 248 nm at pulse energies up to 300 mJ, with pulse durations of 20–30 ns and repetition rates up to 65 Hz. The laser beam entered the metal vacuum chamber (base pressure 5×10^{7} Torr) via a quartz window and was focused to a rectangular spot (1.5 mm×3.5 mm) on a hot-pressed stoichiometric $Bi_4Ti_3O_{12}$ ceramic target supplied by Pure Tech, Inc. The beam was incident on the target at an angle of 45°, and the target was rotated at 10 rpm to reduce cratering. Substrates were bonded with conductive epoxy to the substrate holder, which was radiatively heated, and were positioned at a distance of 3.5 cm from the target surface. The samples were placed within a 2-cm-diam area centered on the plume axis, and were expected to receive material removed from the target mainly by ablation. All films were prepared with an estimated laser fluence on the target of 2 J/cm^2, laser pulse rate of 10 Hz, and oxygen flowing at a pressure of 200 mTorr. For these conditions the deposition rate was about 30 nm/min. Films were prepared at different substrate temperatures in the range 500–700 °C, and were grown typically to thicknesses of about 1 μm. Structural characterization of the films was performed using x-ray diffractometry, x-ray oscillation patterns, and texture camera photographs, while surface morphology was determined by means of scanning electron microscopy. The composition of the layers was examined using energy-dispersive x-ray (EDX) and electron microprobe techniques. Capacitance and conductance measurements were made over the frequency range 10–500 kHz using a Boonton bridge, and ferroelectric hysteresis studies were carried out with a modified Sawyer–Tower circuit.

Preliminary depositions were made on MgO(110) and Si(100) substrates at 675 °C in order to provide a basis for comparison with previously grown rf sputter-deposited films prepared at the same temperature. In all samples studied compositions of the deposited films were determined to be the same as that of the target within the precision of the EDX and electron microprobe measurements. This result was confirmed by the phase composition data obtained by diffractometry, as shown in Fig. 1. This figure also emphasizes the strong differences in orientation between layers grown on the two substrate materials. The diffractometer trace for the film on silicon [Fig. 1(a)] indicates a randomly oriented polycrystalline structure, while that for the film on MgO [Fig. 1(b)] confirms a highly oriented texture with the orthorhombic *c* axis normal to

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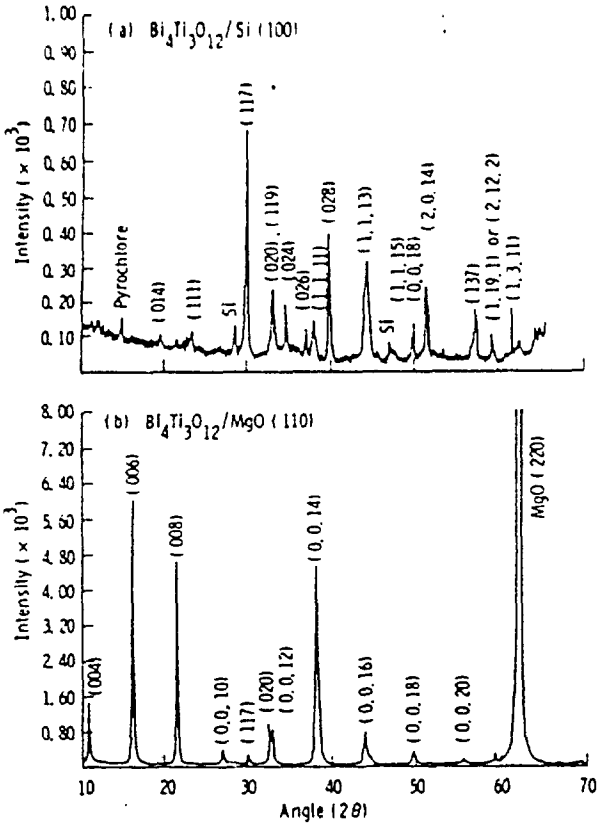

FIG. 1. X-ray diffraction patterns for (a) a film deposited at 500 °C on Si(100) and (b) a film deposited at 675 °C on MgO (110).

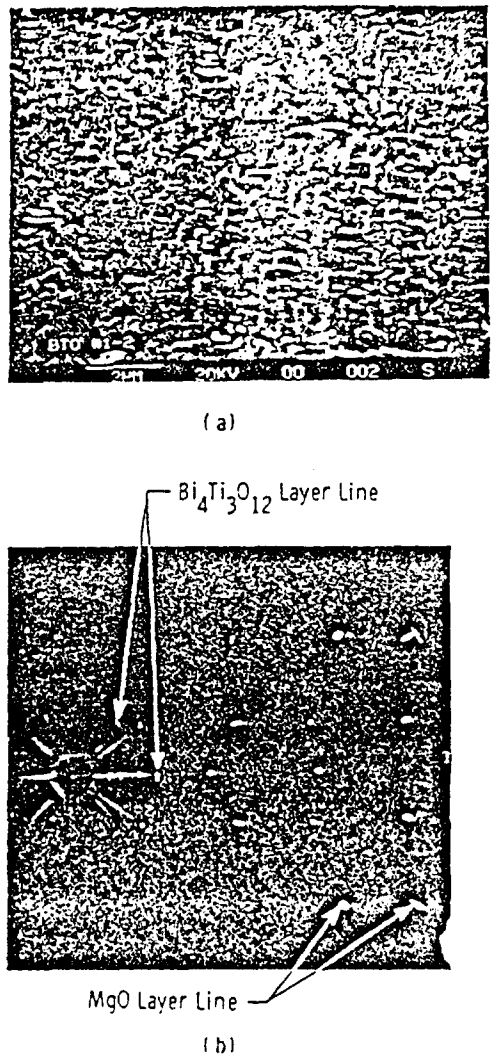

FIG. 2. (a) Scanning electron micrograph of a fiber textured film on an MgO(110) substrate; (b) x-ray diffraction oscillation pattern of the same sample.

the substrate surface. [The reflections in the pattern shown in Fig. 1(a) were indexed on an orthorhombic unit cell with dimensions $a = 5.453$, $b = 5.403$, $c = 32.83$ Å, cf. the values for bulk crystals of $Bi_4Ti_3O_{12}$, i.e., $a = 5.448$, $b = 5.410$, $c = 32.84$ Å).] These results on film orientation differ markedly from those reported previously from our laboratories[1,2,6] on sputtered films of $Bi_4Ti_3O_{12}$. Sputtered layers on Si(100) were shown usually to display a strong c-axis texture (at least for films about 3 μm thick), while those on MgO(110) grew with the c axis (and either the a or b axis) in the plane. One possible explanation for this difference is the fact that the surface structure of the MgO(110) substrate may be modified at the high oxygen pressure and temperature at which the pulsed laser deposited films were prepared.

Scanning electron microscopy (SEM) micrographs of the laser-deposited titanate films showed them to be virtually free from particulate deposits (a problem especially associated with laser deposition of high T_c superconducting films, and often with sputtered films) with no evidence of cracking. The surface structure of the highly textured deposit on MgO(110) showed the formation of rectangular platelets (consistent with the habit of bulk crystals) with edges aligned parallel to the sides of the MgO substrate [see Fig. 2(a)]. Confirmation of this alignment was obtained from x-ray oscillation patterns such as that illustrated in Fig. 2(b) which indicates a weakly epitaxial (double-positioned) structure of the type (001) $Bi_4Ti_3O_{12}$// (110)MgO; with the [100] and [010] cell edges of the titanate lying at approximately 45° to the in-plane [001] and [1$\bar{1}$0] axes of the MgO. This azimuthal alignment is readily explained by recalling that the titanate film is deposited at temperatures slightly above the Curie point, where the structure is tetragonal[8] and can be referred to a unit cell with an a_T parameter of about 3.86 Å (cf. $a = 4.21$ Å for MgO). It is these shorter tetragonal axes (oriented at 45° to the orthorhombic axes of the ferroelectric phase) which align parallel to the [001] MgO axis during growth.

Hysteresis measurements were performed on metal-ferroelectric–metal-semiconductor sandwich structures in which the ferroelectric comprised a bismuth titanate layer about 1 μm thick deposited at 500 °C. The substrate was low-resistivity p-type Si(100), which was coated with 50 nm of SiO_2 prior to application of a sputtered Pt(Ti) contact layer. X-ray diffraction measurements showed that the $Bi_4Ti_3O_{12}$ film possessed a randomly oriented polycrystal-

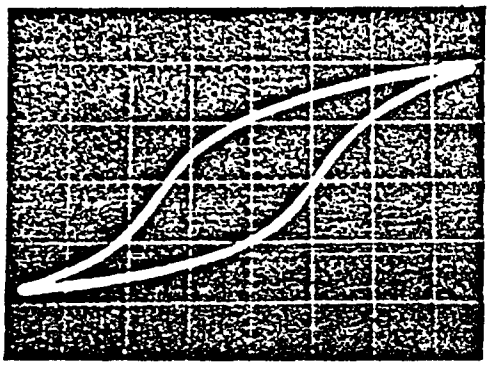

FIG. 3 Hysteresis loop measured at 2 kHz for a 1050-nm-thick polycrystalline bismuth titanate film. Scale: vertical, 17.5 $\mu C/cm^2$ per large division; horizontal, 181.8 kV/cm per large division.

line structure, similar to that of the films grown on Si(100), shown in Fig. 1(a). Figure 3 shows a hysteresis loop obtained at 2 kHz from such a structure with a circular gold counterelectrode having area 5×10^{-3} cm^2. The polarization is nearly saturated, and at slightly higher applied voltage dielectric breakdown occurred. The inability to fully saturate the polarization may have been due to poor counterelectrode contact or shorting via grain boundaries in the film. Annealing of the electrodes or use of lower growth temperatures is expected to reduce or eliminate this problem. The estimated saturation polarization and remanent polarization were 28 and 19.3 $\mu C/cm^2$, respectively. The saturation polarization is consistent with the value ($\sim 32\ \mu C/cm^2$) anticipated for a random angular distribution of the resultant polarization ($\sim 50\ \mu C/cm^2$) typical of bulk crystals. The estimated coercive field is 200 kV/cm, and is comparable to values measured for randomly oriented $Bi_4Ti_3O_{12}$ films prepared by sputtering.

Capacitance and conductance measurements yielded a dielectric constant (for the sample depicted in Fig. 3) of approximately 138 which is independent of frequency. The dissipation factor varies somewhat with frequency, displaying a minimum value of 2.2×10^{-2} at 500 kHz. Both the dielectric constant and dissipation factor fall within the range measured for sputtered films of $Bi_4Ti_3O_{12}$.

In an attempt to test the feasibility of using the laser-deposited films of bismuth titanate as the gate dielectric in a ferroelectric FET memory device we prepared metal-insulator-semiconductor (MIS) structures on *p*-type silicon substrates. A 10-nm-thick film of CaF_2 grown by molecular beam epitaxy (MBE) was interposed between the silicon epitaxial layer and the ferroelectric layer (grown at 500 °C) in order to suppress tunnel-injection effects observed previously with MIS samples in which the gate dielectric comprised a sputtered titanate layer grown directly on the silicon.[6] The counterelectrode was the mercury capillary of a standard mercury probe having a contact area of 0.64×10^{-3} cm^2, which was used to measure the *C-V* curve. However, the polarity of the threshold shift of the curve was the same as that observed by Wu,[6] consistent with the interpretation that charge is being injected from the silicon surface into traps in the ferroelectric film (injection type on/off switching). A threshold shift opposite in sign to the injection type is expected from induced charge compensation on the Si surface by the polarization of the film (polarization type switching). Apparently, the fluoride layer thickness used here was too thin to prevent charge injection. Further work is currently in progress, using barrier layers of either a thicker CaF_2 film or a layer of SiO_2 to prevent charge injection.

In conclusion, stoichiometric transfer from a $Bi_4Ti_3O_{12}$ target to a variety of single-crystal substrates has been achieved by the technique of pulsed excimer laser deposition. The deposited ferroelectric titanate phase remains stable during growth at substrate temperatures up to 675 °C or higher, and films deposited at temperatures down to 500 °C are shown to display bulk-type ferroelectric behavior. A preliminary version of a ferroelectric MIS structure failed to demonstrate polarization type switching of the type required in ferroelectric FET memory devices. However, it may yet be possible to overcome this problem by using lower growth temperatures or thicker dielectric barrier layers.

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