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Advanced Packaging Concepts for Digital Avionics

(Les Techniques avancées de mise sous boitier)

Papers presented at the Avionics Panel Symposium held in San Diego, CA, USA, 6-9 June 1994.

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- Recommending effective ways for the member nations to use their research and development capabilities for the common benefit of the NATO community;
- Providing scientific and technical advice and assistance to the Military Committee in the field of aerospace research and development (with particular regard to its military application);
- Continuously stimulating advances in the aerospace sciences relevant to strengthening the common defence posture;
- Improving the co-operation among member nations in aerospace research and development;
- Exchange of scientific and technical information;
- Providing assistance to member nations for the purpose of increasing their scientific and technical potential;
- Rendering scientific and technical assistance, as requested, to other NATO bodies and to member nations in connection with research and development problems in the aerospace field.

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Theme

A critical impediment to significantly improving the performance of digital airborne electronics or avionics is the limitation posed by current electronics packaging concepts. This symposium will bring together experts from seemingly diverse, but interlocking disciplines ranging from logisticians to digital designers to mechanical engineers and will establish the current baseline in digital packaging, failure modes of the electronics and support problems. Trends in both supportability and processing will be described for early 21st century application. Along with the projections of asymptotic increase in signal, image and data processing, dramatic increases in thermal densities, chip interconnects, connectors and backplane traffic will be described. Current packaging approaches will then be shown to be totally inadequate, both from performance and supportability perspectives. A system solution for packaging light weight, ultra-durable and high-performance real-time digital processing will then be presented. Papers will be presented on how diverse new technologies could be applied to be integrated to provide a system solution. The technologies to be examined in this symposium include micro-circuit and nano-circuit device technology, hybrid wafer/wafer level packaging, three-dimensional packaging, advanced cooling approaches including flow through module designs and phase change (replacements for failure prone and data-rate limiting metallic connectors and backplanes) and line weight enclosures that can also reduce vibration and EMI effects.

Avionics currently comprise almost one-third of the flyaway costs and over one-third of the support costs of modern day fighters. These percentages are expected to steadily grow unless fundamental changes are made in the manner in which avionics are designed, manufactured, packaged, tested and supported: advanced packaging technologies hold promise for achieving greater performance while holding down costs.

Thème

Les limitations imposées par les concepts courants de mise sous boitier des composants électroniques représentent un obstacle majeur à l'amélioration sensible des performances de l'électronique numérique embarquée (c'est-à-dire l'avionique). Ce symposium réunira des experts d'horizons apparemment divers mais en réalité connexes, tels que des logisticiens, des concepteurs d'équipements numériques et des ingénieurs mécaniques. Il jettera les bases des techniques actuelles de mise sous boitier, des modes de défaillance de l'électronique et des problèmes de soutien.

Les grandes tendances en matière de traitement et de capacité de soutien seront décrites pour une application de l'an 2000, ainsi que des extrapolations d'augmentations asymptotiques dans le domaine du traitement du signal, de l'image et des données, et l'évolution dramatique des densités thermiques, des interconnexions de puces, des connecteurs, et du trafic des fonds de panier.

Il sera ensuite démontré l'inadéquation totale des approches adoptées actuellement aux problèmes de mise sous boitier, tant du point de vue des performances que des capacités de soutien. Une solution «systèmes» aux problèmes de la mise sous boitier d'un ensemble de traitement numérique léger, ultra-fiable, temps réel à hautes performances sera ensuite présentée. Des communications seront présentées sur l'intégration de diverses technologies nouvelles pour permettre une solution systèmes. Parmi les technologies qui seront examinées lors du symposium on distingue : les technologies des dispositifs à micro-circuits et à nano circuits, la mise sous boitier tridimensionnelle, les concepts avancés de refroidissement y compris les modules à écoulement libre et à changement de phase (à substituer aux connecteurs métalliques et aux fonds de panier susceptibles aux pannes et limités en débit), ainsi que les boitiers légers qui permettent d'atténuer les vibrations et les effets des perturbations électromagnétiques.

A l'heure actuelle, l'avionique représente presqu'un tiers des coûts de sortie d'usine et plus d'un tiers des coûts de soutien des avions de combat modernes. A moins que des changements fondamentaux ne soient opérés au niveau de la conception, la fabrication, la mise sous boitier, les essais et le soutien de l'avionique, il est vraisemblable que ces pourcentages augmenteront progressivement. Les technologies avancées de mise sous boitier devraient permettre d'obtenir de meilleures performances tout en limitant leurs coûts.

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TECHNICAL EVALUATION REPORT

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SUMMARY

The Symposium was convened to bring together a diverse group of experts in the various disciplines involved in the design, integration, production, and logistics support of advanced avionics systems. The overall theme was the challenges and alternative approaches in the packaging, installation, and interconnection of avionics employing rapidly evolving electronic technologies while promoting commonality and controlling cost.

The Symposium was highly successful both in presenting a comprehensive survey of progress and areas of continuing technical development and in defining and generating discussion of the key issues which must be dealt with in future avionics system designs. The organization of the 30 papers which were presented permitted a logical flow, beginning with the current avionics packaging situation and progressing through discussion of the technical and programmatic aspects of packaging increasingly dense and high performing electronics in military aircraft environments. Every session was notable for the free and candid exchange of views between audience and authors, as documented in the Discussion section following each paper. As a result, the value of the Symposium extended beyond the purely technical content and achieved very useful quantification of the alternatives for dealing with packaging, thermal management, standardization, and other issues and the merits of the various approaches.

Among the primary topics discussed during the Symposium were:

- Module size and form factor for efficient and reliable packaging of VLSI-based, as well as RF and analog, circuitry with steadily increasing density and performance.
- Architectures and designs for power distribution and regulation.
- Methods for cooling densely packaged avionics as module dissipations reach and exceed 100 W.
- Alternatives for interconnecting modules and functional clusters, both on the backplane and among racks, sensors, displays, and other locations, including optical schemes.
- Alternatives to conventional aluminum enclosures, especially advanced composite materials.
- The overarching imperative to control costs and the importance of effective standardization and innovative design methods in achieving that goal.

In four days of concentrated presentations and discussions, the Symposium yielded both a useful exchange of views among experts in the field of avionics packaging and a body of results which will serve as an important reference. These results can and should be a major contribution to the resolution of questions about standards, architectures, and designs which must be settled if the potential of avionics to maintain the superiority of NATO air forces is to be realized.

TECHNICAL CONTENT

Opening Ceremony

Following opening remarks by Dr. Yarmovych, AGARD Chairman, on the changing role of NATO and of its technical organizations, the theme of the symposium was presented by the Technical Program Chairman, Dr. Krueger. Avionics packaging was selected from the many

Papers presented at the Avionics Panel Symposium held in San Diego, CA, USA, 6-9 June 1994.

proposed topics due to its importance for the cost, performance, reliability, maintainability, and commonality of avionics systems. The tremendous growth in avionics functionality, the importance of upgrades to extend the lifetime of existing systems, and the need to control costs all contribute to the critical importance of packaging and make this topic especially timely.

Keynote Address

In his remarks, Honorable R. Noel Longuemare, Principal Deputy Under Secretary of Defense for Acquisition and Technology, US. Department of Defense, reinforced the importance of avionics packaging and discussed a number of trends in the environment confronting NATO which make this such a critical area, including:

- The overall importance of controlling cost to maintain defense capabilities in the face of declining budgets.

- The leverage of packaging advances on avionics performance, reliability and cost.

- A growing emphasis on commonality, interoperability and international cooperation, with packaging and associated standards as a key element of progress toward these goals.

Mr. Longuemare stressed the importance of treating packaging in a complete *system* context. It is essential that not only digital circuitry, but also analog, RF, EO, and mixed signal functions be supported with reliable, affordable, high performance packaging and interconnection.

He then described a number of initiatives being undertaken by the US DOD:

- A Common Systems Working Group has been formed to pursue avionics commonality. The emphasis is on architecture rather than common modules, reflecting the limited success achieved to date in applying common modules in multiple systems. Technology transparency is an important goal, and the Group is addressing both digital and analog functions.

- A new Defense Manufacturing Council has been formed to accelerate the implementation of acquisition reforms in DOD system programs.

- An overall acquisition reform initiative is underway to eliminate non-value added functions and to help maintain a healthy defense industry base. Attention is being paid to use of commercial parts and adoption of best commercial practices as part of an overall strategy of using commercial-off-the-shelf (COTS) and dual-use products.

Finally, Mr. Longuemare mentioned a number of specific programs which explicitly include considerations of commonality, interoperability, and international cooperation, including:

- The recently released RFP for the MIDS program includes the recommendations of a five-nation team working on modularity, interoperability and cost control.

- The AIM-9X short range air-to-air missile program stresses international cooperation.

- A NATO CALS office has recently been opened.

In conclusion, Mr. Longuemare reiterated the importance of AGARD and urged the attendees to seek ways to apply advanced technology to support the priorities and imperatives facing NATO in the post-cold war environment.

Session I - Current Packaging Designs and Limitations

The six papers in the opening session served to establish a basis for the symposium's consideration of trends and requirements in avionics packaging. Overview papers described both US and European packaging programs (PAVE PACE, SHARP, and FASTPACK) which are aimed at defining current and future system needs and determining the optimum packaging strategies to meet those needs. Other authors described modeling and analysis tools which have been developed to implement next-generation designs.

Themes.

- Packaging today must be considered as a consistent technology ensemble which provides for component mounting and protection, a full hierarchy of interconnections and information transfer, power and thermal management, support for maintenance and failure management, and compatibility with commonality and standardization. Packaging in this broad sense is often a limiting factor in the system designer's ability to exploit advances in components and other enabling technologies.

- Avionics systems now in development, with the F-22 as the outstanding example, are based on

the complementary concepts of integration and modularity. However, the corresponding packaging baseline, involving line replaceable modules (LRMs) with 2-D printed wiring boards (PWBs) installed in integrated racks and interconnected via a variety of parallel electrical data paths, is approaching serious limits. Problems include the complexity, cost and reliability of rack backplanes and connectors; achievable data rates; and the ability to extract heat. At the same time, demands for increased information processing throughput, data storage, complex cockpit display generation, and so forth continue unabated. Realistic projections call for super-computer levels of performance, in the range of 1000 MIPS of general purpose data processing and several GFLOPS of signal processing, on board a tactical aircraft. Data transfer speeds in the accompanying network must be in the range of several GBPS.

- As the complexity and level of integration of avionics systems has increased, packaging has become intimately connected to architecture and to the overall system engineering process that seeks to optimize a weapon system as a whole. Packaging must support a logical functional partitioning, must provide the necessary signal and data paths and speeds, must be adaptable to airframe volumes and structures, and must not impose unacceptable penalties in weight, power, cooling, or other system characteristics. The packaging scheme must effectively deal with all types of avionics functions, including digital, analog, RF and EO signals.

- Technology transparency, implemented through form/fit/function/interface (F^3I) specifications and standards, is essential to deal with the continued rapid evolution in electronics technologies.

- Growing use of computer modeling and analysis tools is an integral part of modern avionics practice. Tools for evaluating fault tolerance, thermal and mechanical design, logic validity, built-in test coverage, and other critical design aspects are essential in dealing with modules that contain tens of millions of transistors and dissipate as much as 100 W or more.

- For many reasons, including cost and assured availability, military avionics will increasingly be driven to use commercial or dual-use products. Ways must be found to achieve reliable operation in military system environments, with obvious implications for packaging.

Issues.

- The primary issue discussed in Session I proved to be pervasive through the meeting. It concerns the preferred size (format) of a basic avionics module. US systems have settled, for the present, on the SEM-E format (149 by 162 mm) defined under the US Navy's SHARP program, while there is a consensus among European developers that a somewhat larger (150 to 160 by 233 mm) format is preferable. The FAST (French ASAAC Study Team) module, which is close to the Double Europe module form factor, has been proposed as preferable to SEM-E, and two papers in Session I presented results supporting this view, based on parametric studies of cooling, power distribution, EMC, and mechanical design, as well as impact on the platform aircraft. The SEM-E format, on the other hand, is being successfully employed in the F-22 and is the basis for packaging in other systems such as the RAH-66 Commanche helicopter.

- A related issue which strongly affects the decision on module form factor is that of the power distribution and conditioning architecture. If the final, or "point of use," power regulation is performed on-module, giving the highest quality and greatest redundancy, then the required PWB area has made it difficult to fit all the required circuitry into a SEM-E. If, on the other hand, dedicated power conditioning modules are employed in the avionics rack, a SEM-E can contain both typical functional blocks such as a data or signal processor and the required bus interface, built-in test, and other circuitry.

- Another issue is the maximum module power dissipation which is both required and achievable. The SEM-E is nominally rated for 35 - 50 W with conductive cooling through the module ribs to the rack structure. This can be increased significantly with liquid flow through (LFT) cooling, at the cost of providing reliable coolant connections and a module cold plate with fluid channels. The FAST module can handle up to 80 W with conductive cooling and more with LFT. Advanced module designs with more than 100 W power dissipation will become increasingly common as levels of integration and performance continue to rise, with much of that power associated with the transceivers required to drive backplane capacitance at high clock rates. Use of LFT is therefore likely to be required.

- Still other issues concern the module cooling scheme (conduction vs. liquid flow through),

rack cooling (air vs. various fluid coolants), EMI/EMC shielding (module case vs. integrated rack vs. airframe structure), and the suitability of a given module format for installation in variously shaped avionics bays. The FASTPACK study concluded that, in general, the larger FAST module format, use of coolanol, use of distributed EMI/EMC shielding, and a variety of rack configurations are preferred.

Session II - Requirements for Advanced Packaging Technology

The 10 papers in this session dealt with a broad spectrum of technologies which determine the feasibility, cost, and performance of various advanced packaging concepts. It is clear that the Multi-Chip Module (MCM) "supercomponent" is now a fundamental ingredient in the packaging hierarchy, and several papers dealt with aspects of assuring MCM quality and reliability and with the advantages and disadvantages of the various MCM families. In a related area, a convincing summary of data on plastic encapsulated microcircuits (PEMs) was presented which shows that their early reliability problems have been solved.

At the same time, many groups are exploring extension of traditional 2-D circuit structures to 3-D, both for increased packing density and to shorten interconnect paths, and several authors discussed such designs. Two recurring issues here are the ability to extract heat from such structures and the best approach to vertical connections among circuit layers. Unfortunately, several of the projects described were terminated prematurely due to budget constraints.

Themes.

- MCM packaging, and variants such as chip-on-board, are rapidly replacing traditional hermetic single-chip packages as the preferred first level interconnection scheme for digital, analog, mixed signal, and, increasingly, RF and EO circuitry. For example, one paper described an active substrate which provides both monolithic memory blocks and the interconnects for additional active components which are mounted on top. MCMs approach the density of wafer-scale integration (WSI) while reducing the yield problems associated with WSI. Several authors reported work on aspects of reliability and manufacturability of such approaches. The last paper in the session extended these ideas to RF and mixed digital-RF modules.

- A number of innovative schemes for passing signals among the layers of a 3-D stack of circuit planes have been demonstrated. One example uses elastomeric "columns" or "buttons" with embedded wires which make reliable contact when the stack is mechanically compressed, while another paper described a combination of conductive paths diffused through a silicon wafer with microbridge contacts between wafers.

- Both the functionality and the power dissipation of digital modules continue to rise. As a benchmark, the URDA processor design puts 200 MIPS of data processing and 800 MFLOPS of signal processing in a single liquid cooled SEM-E which is compatible with the F-22 backplane. 3-D schemes will take the functional density and speed higher still, but may call for greater module thickness.

- There is growing evidence that commercial-off-the-shelf (COTS) parts, including plastic packages, are compatible with military avionics, if the required operating temperature range is attained.

Issues.

- The overall issue which emerges from this session concerns the need to find new packaging techniques which circumvent the limitations of current module/connector/backplane/enclosure designs. Connector pin counts, backplane complexity, achievable data transfer rates, and other factors affecting system performance and reliability loom as fundamental constraints on the designer's ability to exploit the benefits of ever-improving electronics technologies. At the same time, decisions about new packaging and interconnection schemes will profoundly affect the extent to which standardization and backward compatibility with existing inventory systems can be achieved. There is presently no consensus on the direction to take.

- Although MCMs, chip-on-board, and other advanced packaing concepts are becoming widely used, their limited production and, especially, field service history means that continued attention to the identification, measurement, and mitigation of failure mechanisms is important.

- Another important question is the extent to which high density packaging, by reducing the capacitance which an output circuit must drive at high clock speeds, in combination with reduced power supply voltage, may help offset the rise in module power dissipation that comes with increasing gate and device counts.

Session III - Advanced Packaging Technologies

The eight papers in this session fell into two groups, each dealing with a major packaging issue. The first three authors reported work on advanced cooling methods, while the remaining five discussed aspects of interconnections.

Each of the three leading candidates to replace conventional conduction cooling of modules was the subject of a paper. Those approaches are:

- Liquid flow through (LFT), with associated questions of choice of coolant, pressure and mass flow rate, design of the flow path for maximum thermal transfer, and so forth.

- Immersion cooling, involving flooding the volume above the active components with a fluid which may or may not be intended to boil (single phase vs. two phase cooling).

- Heat pipes embedded in the module cold plate for beater spreading and extraction of heat from high power components.

The papers on interconnection inevitably treated aspects of system architecture as well, since the partitioning and topology of a system are intimately bound up with the requirements and design for the associated data paths. Various authors discussed current and projected data rates, the merits of optical (photonic) vs. electrical transmission, schemes to reduce connector pin counts, and other related issues.

Themes.

- Although today many modules can remain within the power dissipation limit imposed by simple conduction cooling via the module's ribs, there is a clear trend to higher power associated with increasing circuit density and speed. Anticipated reduction of the standard logic bias voltage from 5 to 3.3V will help, but will not eliminate the problem. LFT is gaining in acceptance, e.g., on the F-22, and early problems with leakage, inefficient heat transfer, etc. are being solved. However, more work on effective, maintainable, affordable cooling techniques is needed.

- Reasonable extrapolations of avionics information processing needs lead to projections of data transfer rates of at least several GBPS. At the same time, there is a strong desire to reduce the complexity and improve the reliability and maintainability of interconnection hardware.

- A number of papers in this session reflect the widespread interest in optical techniques to supplement or even replace electrical data transmission. Progress was reported on both planar and conventional optical waveguides, high speed sources and detectors, and connectors and other components. This may be an area where worthwhile savings are possible through use of COTS products.

Issues.

- Although there is general agreement on the need for improved module heat extraction, the papers in this Symposium reflect the diversity of opinion on how best to achieve it. Any method which involves plumbing coolant to individual modules will entail an additional maintenance burden for system users. Heat pipe structures compatible with planar modules would eliminate this, but have historically been expensive. Any liquid cooling system, but especially immersion cooling and integral heat pipes, exhibits at least some dependence on aircraft orientation and g-forces, which is a potentially serious concern in maneuvering flight. A standard cooling design is obviously a prerequisite to module and enclosure standardization.

- The discussion of interconnection technology raises the issue of whether fundamental changes in avionics architecture are in order. A "unified" architecture in place of the current partitioning into sensors, signal and data processors, several kinds of networks, etc. has attractions in terms of system integration, system control, and long term upgrading, and might be possible with a universal interconnection approach like the IEEE Scalable Coherent Interconnect (SCI). A related question is whether to replace current parallel multiplex and switched data paths on the backplane with very fast serial channels in order to reduce pin count, simplify the backplane, and reduce susceptibility to noise and crosstalk.

- There is a clear difference of opinion over the need to migrate from electrical to photonic data paths. One paper presented data which argue that electrical backplanes are already capable of ≥2 GBPS and can be pushed to 5 - 10 GBPS, with the limit being the bandwidth of the connectors. Other authors reported progress on optical components which promise to solve problems with reliability (especially of connectors) and bring down cost. Within the optical backplane community, a variety of approaches have been explored using point-to-point channels, star

couplers, and reflective or transmissive couplers at the module connector. Once again, this is an area where much more work and experience is needed to determine the best approach and which has a fundamental impact on commonality and standards.

Session IV - Advanced Packaging Applications

Session IV's 6 papers dealt with several additional topics of importance to avionics packaging. The first two described extensive studies on materials, fabrication methods, and designs for enclosures built partially or completely of composite materials. The next two described work on power distribution for modular, integrated systems. The final papers presented results of studies on electromagnetic compatibility (EMC) and on the basic architectural questions associated with optimum design of a modular communications/navigation/identification (CNI) suite.

Composite enclosures offer the potential of reduced weight and resistance to corrosion, but have, in general, poorer thermal and electrical conduction than metal structures. The papers in this session considered a wide range of materials and provided data on the selection, design, and manufacture of composite enclosures ranging from small component housings to full integrated racks. In particular, metallization techniques were described which produce the required level of EM shielding.

The two authors addressing power distribution presented results which suggest greatly increased feasibility and utility for on-module power supplies to generate and regulate bias voltages. This scheme would replace central rack power supplies or partially distributed designs in which some fraction of the modules in a rack are dedicated power regulators. The power density, size, planar form factor, and efficiency of these recent designs, based on novel components and clever circuitry, make fully distributed power regulation appear much more attractive than was the case a few years ago.

The final two papers illustrated the complexity of the modular avionics design challenge and the multiple subtleties which must be taken into account. The first was an in-depth consideration of the EMC problems brought on by increases in module size, density, and operating frequency and gave guidance on ways to minimize them. The second illustrated the importance of careful system engineering and optimization in achieving the potential benefits of modular electronics for high reliability, cost control, and performance. The author presented a series of studies leading to an overall optimized CNI architecture.

Themes.

- There appears to be agreement that composite enclosures are now a legitimate option in situations where their light weight and resistance to chemical attack are attractive and where their limited thermal conductivity can be accepted through the use of some metal structures, low power electronics, or other cooling method. Today, they cost more than metal enclosures, but this should improve as composite use in general and aircraft applications in particular grow in volume.

- There is also consensus on the attractiveness of moving to fully distributed power regulation architectures, given that the on-module power supply can be made small and efficient enough. In addition to very high redundancy and fault tolerance, this approach allows power distribution in the rack at high voltage, hence lower current, with both lower electrical wiring losses and relaxed tolerances on ripple, voltage sag, and other power quality specifications. It also greatly simplifies the task of getting power into a module, since the lower current level requires fewer pins in the edge connector. The value of on-module voltage regulation increases as the final bias voltage goes down, and the trend toward 3.3V as the standard logic supply voltage may make this approach indispensable due to the difficulty of centrally generating and distributing high quality power at this low voltage.

- The power supply papers illustrated the ingenuity and careful development effort which has gone into components and circuits for planar power supplies. Switching frequencies in the range of 1 MHz are an important design feature. Magnetic components in particular have come a long way in both performance and form factor, allowing designs as small as 2"x 2" with high power densities and efficiencies of 90% or more.

- The EMC problem in avionics systems of the class discussed at this Symposium is generally recognized. As clock frequencies reach hundreds of MHz and as backplanes increase in complexity, potential coupling mechanisms among components and circuit traces multiply. Even small apertures in shielding enclosures may admit signals adequate to produce upsets. Careful

design using accurate modeling tools, along with thorough testing, are clearly essential.

Issues.

- The progress made in miniaturizing module power supplies has obvious implications for the issue raised previously about module form factor. The results shown in this session may indicate that even the smaller SEM-E size can accommodate on-module power conditioning, since the design presented might occupy as little as 1/8 of the available PWB area. A related issue concerns the power distribution architecture itself. It might be possible to have the advantages of both fully distributed and partially distributed designs by converting rack prime DC power to AC with a few dedicated modules, then using a simplified on-module circuit to step down and regulate the actual bias voltage without the need for a complete DC-DC converter. Any such scheme would eliminate backward compatibility with existing modular avionics designs which rely on dedicated power supply modules.

- With respect to composite enclosures, the issue would seem to be simply one of carefully matching the choice of enclosure type to the specific application. For example, designs with some metal or metal matrix composite members might be used in cases where moderate to high power modules are to be installed.

- A final general issue is that of accounting for the full consequences of moving to the fast, dense avionics systems of interest to this Symposium. EMC and an optimum architecture for redundancy are two of many such considerations. Once again, comprehensive, high quality system engineering is of the utmost importance.

DISCUSSION

Viewing the Symposium as a whole, a picture emerges of a military avionics community grappling with problems which are different, in important ways, from those which were dominant as recently as a few years ago. On one hand, the inexorable march of electronic technology, and the growing importance of avionics in determining the cost and operational effectiveness of combat aircraft, put a premium on design methods which can seize the opportunities offered by avionics to maintain the qualitative superiority of air forces. On the other hand, severely constrained budgets and shrinking force structure compel the designer to hold down costs, promote interoperability among systems, and provide for modernization over system lifetimes of 30 years or more.

Technologies such as VLSI/VHSIC, MMIC, and MCM packaging, together with advanced sensors and displays and other elements of a state-of-the-art avionics suite, make it technically feasible to equip a fighter or other aircraft with greatly enhanced mission capabilities. Built-in test and redundancy for failure management create equally exciting possibilities for systems with very high mission reliability and reduced maintenance requirements. To an unprecedented degree, packaging and interconnections represent limiting factors on the ability to realize these improvements and on the cost of the resulting systems. For example, the combination of multiple high resolution sensors with a central fusion and target recognition processor generates multi-GBPS data rates within and among the major elements of the avionics system. Processor throughputs and data storage volumes which would, quite recently, have been the envy of a scientific computing facility are now routinely projected for tactical aircraft. The current generation of interconnects, typically involving 50 - 100 MBPS serial links between racks and sensors and 16 or 32 bit parallel data paths clocked at 25 MHz on the backplane, is becoming marginal to support the needs of sensors, processors, and other system elements. The next generation of avionics would thus present a daunting packaging challenge even without the need for cost control and standardization. With all these things taken into account, it seems clear that some fundamentally new packaging and interconnection approaches are essential.

As was emphasized throughout the meeting, any packaging solution must be part of a complete system design, meaning that it must account for all aspects of the avionics system, its interaction with the platform aircraft, its long term logistics support, and its contribution to a balanced weapon system that delivers maximum operational capability for the resources invested. For example, the issue of preferred module form factor should begin with fundamental questions of architecture and functional partitioning – the basic module package should be as small as possible while accommodating both an information processing or other complete function and the required infrastructure circuitry for backplane interfaces, power conditioning, and so forth.

There is a packaging hierarchy, from the individual chip to the MCM or other

"supercomponent," to the PWB and module, to the rack or other enclosure, and finally to the entire system. Associated with this packaging taxonomy is a hierarchy of data rates and timing which is the prime determinant of requirements for the various interconnects. At the same time, the level of functionality integrated in a module tends to drive the power dissipation and thus the required cooling which must be supplied by the aircraft environmental control system (ECS), with implications for weight, cost, engine power penalty, and other critical factors. In short, avionics packaging involves a search for an optimum solution in a design space of very many dimensions.

The often elusive goal of widespread commonality within and among a variety of aircraft and avionics systems has taken on a new coloration in the post-Cold War environment. New starts on aircraft systems are now so rare that one or more generations of electronic technology must be expected to turn over between opportunities for entirely new designs. The greatly reduced quantities of systems in production hampers both the ability to maintain a robust, competitive industrial base and the opportunity for cost savings from economies of scale. The obvious, but difficult, implications of the situation include:

- The importance of standardization within a given system, so that common hardware and software items are used wherever possible for equivalent purposes to minimize development cost and maximize production runs.

- The need for technology transparency in a given configuration item like a module, achieved through F^3I standards and careful attention to architectural issues of timing and interconnection, so that a given item remains producible over time and can take advantage of technological improvements.

- The practical reality that the most frequent opportunities for commonality may be with commercial aircraft avionics and other non-military systems, at least at the level of components.

One interesting concept for promoting greater numbers of fewer hardware types is that of the multi-purpose or "metamodule." The basic idea is to take advantage of the tremendous functionality that can be packaged in a module by including multiple processing repertoires in a single unit. Results like the URDA module design may be harbingers of modules which can, as required, serve as general purpose data processors, pipeline or vector signal processors, etc. A single meta-module type might then be used repeatedly, with software written to employ an appropriate subset of the total inventory of instructions for any specific task. A major side benefit would be great flexibility for reconfiguration to recover from failures or battle damage by reprogramming surviving modules with the highest priority tasks.

If the investments made in perfecting new avionics components and systems are to yield full benefits, ways must be found to incorporate them in retrofits and upgrades to existing systems. An important consideration here is that replacing the contents of avionics bays is far easier and less expensive than installing new cabling within an airframe, since the latter may require removing skin and modifying primary structure. This may require that advanced processors and other modules and components be supplemented with input/output devices able to communicate over existing cables and optical fibers. For example, even a first-generation multimode fiber like those being designed into aircraft like the F-22 can support far high data rates than those now used, given suitable transceivers. It must also be remembered that new technology which places unachievable demands on the platform aircraft, e.g., types or levels of cooling not available from the ECS, will be effectively precluded as upgrade options.

Having due regard for the magnitude of the packaging challenge, it must be emphasized that the situation is far from hopeless. Results like those presented at this Symposium show that innovations ranging from advanced materials to entirely new avionics architectures promise to provide the means to develop and build systems with the required performance, reliability, and maintainability. Achieving desired levels of cost and commonality is more problematical, making it essential that these be given equal or higher priority in both technology development and system design.

RECOMMENDATIONS

- Programs like PAVE PACE and the ASAAC architecture study which examine the basic issues of functional partitioning, scalability, network topology and performance, system operating modes, and the like should be a continuing high priority. A searching examination of the current modular, integrated architectural framework in

light of advances in technology and system requirements is very much in order. One prominent area of inquiry must be the feasibility of replacing the current miscellany of buses and other interconnects with a universal data transmission scheme like the SCI. Another must be development of interfaces that allow simplification of connectors and backplanes. Questions such as preferred module size, bus bandwidth, failure management, and so forth should be *derivatives*, not *drivers*, of the underlying architectural paradigm.

- A similar reexamination of the basic strategy of commonality and standardization is now called for. Opportunities for use of common hardware and software items across weapon systems are limited by shrinking numbers and stretched out program schedules. There may be more value from emphasizing commonality within individual systems and between military and commercial applications. Standards should be based on F^3I descriptions of configuration items with continuing attention to technology transparency and unambiguous definition of interfaces. The standardization strategy and the architecture within which the standards will be applied must be mutually supportive, e.g., in establishing system timing requirements that are consistent with periodic insertion of faster processors.

- As one of the most powerful means of attacking these issues, greater use of simulation and modeling tools is essential. The power of simulation in everything from standards compliance verification to system integration is well established. Work is underway on replacing conventional specifications with executable models that eliminate ambiguities and support design automation. A common simulation and modeling environment would be a great foundation for progress on common avionics hardware and software.

- The excellent work on enabling technologies that was reported in this Symposium, as well as related efforts in many companies and countries, is, ultimately, the key to solving the packaging problems that have been discussed. AGARD can play an important role in coordinating these developments, advocating continued funding for important projects, and disseminating results through publications and meetings like this one. Many of the issues discussed at this Symposium can only be settled by data from thorough evaluation and testing of alternative proposed approaches.

- Although the subject of this Symposium was explicitly packaging for digital avionics, it is clear that equal or greater challenges exist in packaging for RF, EO, analog, and mixed-signal hardware. Problems with backplane blind-mate coaxial and optical connectors, power supplies, and cooling are just a few of the issues that must be dealt with in a complete system solution for next-generation systems.

CONCLUSION

This Symposium was very effective and useful in generating a focused consideration of an area which is of enormous importance to the future of NATO air power. The issues which must be addressed are well defined. Encouraging progress in the enabling technologies was reported, and the openness of the debate among the participants argues well for future cooperation in dealing with these admittedly formidable challenges. The combination of accelerating change in electronic technology and shrinking defense resources make it especially critical that the questions raised in this meeting receive continuing, concentrated, and well coordinated attention.

DISCUSSION ISSUES

I. Module Form Factor – two fundamentally different module sizes have been put forward:

- SEM-E is derived from the 3/4 ATR box/rack packaging system and is the basis for major US military avionics systems such as the F-22 and RAH-66.
- FASTPACK and ASAAC-A formats are supported by a consensus of European avionics developers.

Related Issues:

- Power distribution architecture – see following issue.

- Maximum power dissipation – a larger module can handle more power, but may also contain more circuitry, generating more heat dissipation.

- Platform integration – a smaller form factor may be easier to accommodate in the sometimes constrained volumes of tactical aircraft avionics bays; on the other hand, the FASTPACK study concluded that the larger format has advantages in platform integration.

- Dual use – the FASTPACK module is close to the Double Europe standard and may be more conducive to arriving at a packaging scheme of interest to both military and commercial aircraft; commercial avionics tends to use larger formats than SEM-E.

II. Power Distribution Architecture – basic questions about the best way to distribute and regulate power in an integrated rack have existed since the first studies of modular avionics; among the continuing issues addressed in this Symposium were:

- Should power regulation be central at the rack, partially distributed via dedicated power supply modules (typically on the order of one power supply to seven functional modules), or fully distributed with on-module generation and regulation of the circuit bias voltage(s)?
- Should rack power distribution be AC or DC and at what voltage?
- What should be the standard supply voltage(s) for logic, analog, and RF circuitry; in particular, what are the benefits of dropping the logic bias voltage from 5 to 3.3 V?
- What levels of size reduction and efficiency are feasible in planar, miniaturized converters and regulators?

Related Issues:

- The answers to the above questions appear to depend critically on the final regulated voltage; at 5 V or above, a centralized or semi-distributed architecture may have advantages, but at lower voltages a fully distributed approach may be required. A key question is the ability to supply the increasing power supply current levels required as bias voltages drop without consuming an excessive fraction of the edge connector pinout.

- Results reported at the Symposium suggest that suitable module-level power supplies may be achievable which occupy perhaps 1/8 of the PWB area of a SEM-E module. Highly innovative designs for planar magnetic components, control circuits, power devices, and the like promise continued improvements in power density, hence size reduction.

III. Cooling – opinion among Symposium authors is split on the need for greater power dissipation than can be accommodated by purely conductive cooling (≤ 50 W for SEM-E and ≤ 80 W for FASTPACK) and on the preferred approach to cooling higher power modules (liquid flow through, air flow through, heat pipe cold plates, immersion cooling, etc.)

Related Issues:

- Maintainability impact – any scheme which requires plumbing a cooling fluid to individual modules will represent an additional maintenance burden (refilling and bleeding coolant reservoirs, maintaining pumps and other hardware, handling fluid-filled components, etc.)

- Immersion cooling has been shown to extract very high heat loads, but questions remain on feasibility, especially for RF modules.

- Long term reliability of conductive cooling has been questioned due to deterioration of rib clamping force with wear in the mechanism.

- Module bias voltage – the trend to reduced voltage, from 5 V to 3.3 or 3.5 V, is an important reliability consideration due to reduced hot electron and other effects in sub-micron geometry chips and perhaps 25 - 40% lower overall power dissipation on a module. However, it requires backplane interconnects able to work reliably with smaller logic swings and will do little for the thermal management problems of RF and mixed-signal module types. It also tends to require on-module voltage conversion to avoid very high power supply current levels on the backplane.

IV. Optical vs. Electrical Interconnect – interesting work has been presented on extending the performance of "conventional" electrical backplanes (up to ≥2 GBPS) and on replacing electrical backplanes with optical paths; also, both optical and electrical channels have been demonstrated for "long distance" (inter-rack, sensor-rack, and rack-cockpit) data transmission. At present, the designer has available at least prototype demonstrations of both optical and electrical solutions to achieve the data rates required for compatibility with projected high performance modules.

Related Issues:

- Cost – there is, as yet, little production history for optical transceivers, connectors, etc. to allow an assessment of the cost impact of replacing electrical backplanes with optical. This question should (but will not) be addressed from a life-cycle cost, rather than an initial acquisition cost, perspective.

- Reliability and maintainability – high data rate serial channels using either optics or electrical schemes such as SCI promise significant reductions in connector pin counts compared to the current 360 pin JIAWG SEM-E connector.

- Hybrid networks – backplanes will always have some electrical connections for power and RF modules require either coaxial cable inputs or high bandwidth RF-optical transducers at the antennas; there is no intrinsic bar to mixed optical and electrical signal paths if it can be shown that such a design is optimum.

- Commonality and dual use – if true exchangeability of modules among platforms and between military and commercial systems is to be achieved, the backplane and long distance interconnection scheme will have to support this.

V. Architecture – although most authors at the Symposium addressed refinements to the "conventional" architecture as embodied in systems like the F-22, a number of papers raised, implicitly or explicitly, the prospect that a fundamentally new paradigm is required:

- The PAVE PILLAR/JIAWG Advanced Avionics Architecture (A^3) is based on partitioning into apertures, preprocessors, sensor data network, core processors (signal and data or integrated), high speed data bus, cockpit, video data network, and vehicle management system.
- Alternatives include "unified" architectures in which multiple processor categories and bus types become conponents on a single "logical backplane" and distributed architectures in which significant digital processing is collocated with sensors, antennas or actuators rather than being concentrated in the core processing area.

Related Issues:

- Connectivity – it seems to be a continuing trend that information collection and processing outstrips the ability to transmit that information among system elements.

- Operational requirements – there seems to be no end in sight to the demand for more information processing and display capabilities to deal with beyond visual range combat, automatic target identification, sorting of dense EM environments, etc. nor to the ability of electronics technologies to pack ever greater amounts of such capability into a given volume.

VI. Enclosures – two important aspects of the enclosures to be used with high density modular avionics were discussed during the Symposium:

- Composites – significant progress has been made in evaluating materials, metallization, thermal management, and other aspects of the use of composite materials to reduce the weight and improve the reliability of racks and other enclosures. This is clearly a viable option, subject to trade-offs of cost, repairability, and other parameters between composite and conventional metal designs.
- EMI/EMC – increased packaging density and rising clock speeds complicate design to deal with both internal interference and resistance to external EM threats, including NEMP and high power microwave weaponry. This must be a fundamental design consideration, along with performance, environmental tolerance, and other requirements.

THE IMPACT OF ADVANCED PACKAGING TECHNOLOGY ON MODULAR AVIONICS ARCHITECTURES

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The recent integration of advanced VLSI digital microcircuits with advanced multichip packaging and liquid flow through cooling has resulted in a significant increase in functional computing density and system processing speed for military avionics. A computing function accomplished previously by an entire line replaceable unit (black box) can now be done in a line replaceable module measuring 15 by 15 by 1.5 centimeters (approximate dimensions of the SEM-E module). Further advances in commercially available microcircuit packaging, including wafer scale packaging, will result in another major step in functional density and speed that will be equally as profound as progress made to date. The way forward has been found for developing reliable, highly compact and affordable supercomputer modules to meet burgeoning processing demands for future applications.

This paper explores how advances in digital packaging will impact network requirements at the system level. Two main issues connected with modular digital packaging for avionics were investigated: 1. Can conventional electrical designs continue to handle the information network speed and wirabilitiy requirements needed at the backplane to efficiently utilize advanced modular data and signal processors? 2. Considering projected network requirements for future sensors, displays, etc, (which are made possible because of digital packaging advances), what type of system architecture will be needed?

The paper concludes that: 1. Beyond the module (PCB) interface, a new type of backplane implementation will eventually be needed to support the flexibility and growth needs of modular processing. Several new approaches other than a passive electrical backplane could be employed; however, a switched, photonic-based approach is proposed for information distribution between digital processing modules as well as for interconnection between peripherals. Digital packaging advances will result in I/O speeds of about 2 Gigabits/sec. 2. Advanced integrated RF and EO sensors and display technologies will require network data rates in the range of 2 Gigabits/sec in order to communicate in real time with the high speed signal and graphics processor modules in the common integrated processor racks. Many of these "peripheral" functions will require virtual point-point links because continuous, streaming data is involved.

This resulting system architecture recommended is a switched optical network which interconnects sources and sinks of information to the modular processing assets, as well as providing a network for intermodule intercommunication within the rack. Issues of protocol control of this network remain. Further, several advances in photonic packaging and connectors will be required to make this new architectural approach a reality. Although photonics offers the best long-range solution, significant technology difficulties must be overcome.

INTRODUCTION

It is interesting to trace how architectures have evolved over the last 30 or so years and correlate this evolution with digital packaging. Figure 1 shows the chronology of the evolution from the dedicated analog (black box) systems to the digital/federated (black box) approach. The integrated digital (modular) approach shown as the third generation architecture is just beginning to find its way into US weapon systems (F-22, RAH-66). The advanced integrated/modular analog and digital system is still in the R&D stage and will not available for system use until after 2006. The last three architectures track closely with the work done in the Avionics Directorate under the Digital Avionics Information System (DAIS), Pave Pillar, and the current work being done under the Pave Pace thrust. All these architectures have been substantially shaped by advances in digital packaging technology.

The second generation architecture shown in Figure 1 (digital/federated) initially required a 1 Megabit/sec interconnection (MIL STD 1553). This low network speed and low interconnectivity requirements resulted from two basic, inter-related factors: 1. Only the outputs of relatively slow (eg 0.5 MIPS) data processing black boxes and very low bandwidth controls were interconnected. 2. Fast signal processors did not exist in this pre-VLSI era. Signal processors were usually hard-wired to their sensor and communicated with A/D converters and data processors across a local, dedicated backplane. Hence, "high speed" speed signalling (slow by today's standards) was "hidden" from the system network. As the speed and number of processors increased however, several of these low bandwidth busses were added to accomodate increased network speed requirements.

The third generation, utilizing VLSI packaging, permits the use of flight-line replaceable modular (ie PCB level) multi-function data and signal processors which communicate across a common backplane.

The speed and interconnect requirements of the network architecture dramatically changed with the advent of the third generation processing capability. Fiber optic networks are used to interconnect various sources and sinks (eg sensors to processing racks, racks to racks and racks to

displays) because of high signalling rates.

Some time soon after the turn of the next century, a fourth generation architecture will be needed for advanced avionic systems. Not only are several advanced applications projected that will require "GigaFLOP/Sec or higher" speeds, but advanced digital circuitry and packaging technology will allow the realization of a practical modular supercomputer. This architecture will be a natural extension of the third generation.

Why did these architectures change with time? Figure 2 attempts to provide a top-level model of the process that explains the basic forces at work in affecting architectural changes over the four generations shown in Figure 1 (note however that wherever possible, each new architecture is made backward compatible with the previous one to exploit off-the-shelf hardware or software where desirable.) Figure 2 portrays how the desire for improved performance, lower cost, mission growth and flexibility, improved availability, reduced aircrew workload and reduced manpower are always present over the life of any weapon system. The threat changes so the weapons system must change. Budgets are continually being reduced. Changes to the avionics is the most practical means of satisfying these desires. A steady stream of new avionic technologies are seemingly always becoming available to support these changes. It could be argued that the desires for affordability and increased performance are inherent "requirements" and that the availability of the technology is the enabling event that begins the process of weapon system modification.

Referring to Figure 2, new avionic sensors, displays, weapons, etc are added to military aircraft because digital processing technology can now support new performance features. This technology insertion process (Figure 2) continues until network bottlenecks occur. Eventually, the existing input-output information transfer mechanism on the aircraft (ie, the network, including connectors and protocol) cannot cope with the interconnect and speed demands of the new sensors, nor can it satisfy the processing I/O capability of the digital microcircuits. In other words, processing capability advances are occuring at such a fast pace that the existing system architecture cannot provide the real-time interconnect and bandwidth capability needed to efficiently exploit the processing capability.

Improvements in microcircuit-level circuitry and its attendant packaging and interconnect structure (pin grid arrays, flip-chips, high density laser patterning, multi-chip modules, etc) has outstripped progress made at the board, backplane or system network level. This problem is becoming acute for parallel processing systems, where problems with growth, scalability/transportability of various parallel program software and all-around poor execution efficiency is occurring. Quoting from Reference 1, "In some cases, a processor speed increase of 100 may only produce a 5 fold improvement in completion time due to time taken in local memory accesses or cache misses."

One reason for this disparity is the current lack of technology to build high-yield photolithographic patterns on low dielectric substrates for large backplane structures.

DIGITAL PACKAGING TECHNOLOGY TRENDS : THE PACKAGING HIERARCHY

Figure 3 shows how modular digital avionics is currently being employed in an advanced avionic system. The modular assets are housed in racks and are interconnected via an electrical backplane. Data and signal processing PCBs which would normally be contained within "black boxes" for a second generation, federated architecture are interconnected across a common backplane within the rack for third generation avionics. Analog to digital conversion circuits remain at the sensor locations, requiring high speed digital networks to communicate with the modular processor complex. This architecture will be considered the baseline. Figure 4 shows the packaging hierarchy involved in this avionic network system. We will briefly look at each tier of the hierarchy.

Microcircuitry Packaging Trends

Strides made in digital packaging over the last two decades have been enormous. Within the shadow cast by a single transistor used in avionics during the 1960s, Intel Corporation's Pentium chip can now be placed. It has over 3000000 transistors. Further, the pace at which commercial microcircuit performance improvements is occurring is equally impressive. For example, although Pentium was introduced in early 1993, four years after Intel's 486 chip, Intel recently announced that the new "P6" chip will be shipped in early 1995. The P6 will have 6000000 transistors and operate at 300 million instructions per second. Several other companies, including Power PC (backed by several computer companies), Motorola and Apple Computer are working on competitive designs. These chips will be used in future military avionics, although they will frequently be packaged in multi-chip packages interconnected to high performance substrates and cooled with liquid flowing between or over PCBs.

Multi-Chip Module (MCM) Packaging Trends

Digital packaging technologists are also working to increase system processing speed and functional densities through the development of multi-chip modules (MCM) which utilize Hybrid Wafer Scale Integration (HWSI). This relatively new approach to packaging is currently being used on the F-22 and RAH-66 weapon systems for data and signal processing modules. Primarily, MCMs allow more circuits to be employed per unit board area. Here, individual bare chips are mounted close together on a thin film substrate that provides a high wiring capacity/high speed interconnecting media. For example, the speed of a PCB signal is around 17 cm per ns, where MCM circuit speeds are 3-4 times as great (Ref2). Since packaging efficiences of over 90% can now be achieved in area utilization inside the MCM, their performance is similar to the "ultimate" processor built as a monolithic wafer. Future modular supercomputers for avionics applications will be built by interconnecting several MCMs together at the board level to accomplish parallel processing in excess of 2 GigaFLOPS.

Backplane Packaging Trends

The advent of modular processors allows a small family of modules (data, signal and graphic processors, global memories, power supplies and I/O modules) to be interconnected across a common backplane. The advantages of this backplane connections are many: 1. data and signal processing assets for the avionics system are tightly interconnected, allowing sensor fusion and all forms of information integration to be "easily" accomplished, 2. reconfiguration of failed assets is made much easier because

of tight system control over processing assets, 3. fewer total modules of fewer different types result, with attendant cost and weight savings, because processing assets can now be shared, 4. integrated test and maintenance is now made much easier, resulting in fewer "cannot duplicate" problems; this capability enables flight-line removal of the failed modules with the result that the intermediate repair shop at the airbase is no longer needed and 5. inter-module bussing and network switch functions are accomplished across a common backplane, again saving weight and cost.

However, one significant drawback (which cannot be avoided with today's technology) results from this approach. The backplane is required to grow in complexity to accomodate the routing of all digital signals from diverse sensors, mass memory and mission load devices, controls and displays, inter-rack signals and digital data to and from the stores management and vehicle management systems. The resulting system network is, necessarily, made up of a collection of dissimilar types of networks.
The wirability of the backplane must grow dramatically to accomodate this increased signalling in addition to accomodating the speed demands of advanced microchips and MCMs. The combined functionality of the low bandwidth busses used to interconnect black boxes for the second generation system must now be supported by a (higher speed) bus function embedded in the backplane. In addition, error correction of backplane control signals is needed to ensure proper reception of key signals in an "EMI-rich" environment. The modular backplane must now mediate streaming data traffic between sensors, displays memories and processors, as well as enable the control of the system assets and pass processed data to the appropriate modular assets within and between processor racks. Finally, a test and maintenance bus function is needed to identify failed modules in order to support reconfiguration and flight-line maintenance. Over 20000 embedded networks will be required for a typical two tier rack.

Given that the designer does not want to exceed 300-400 pins at the SEM-E card edge for reliability reasons, the reader can appreciate that the digital system designer is beset with further difficulties in providing the needed wirability via the backplane. For example, a representative modular data processor will require the following pin counts, as shown in Table 1.

Table 1
Typical Signal List for Data Processor Module

Signal Function	No. Pins	Comments
Power	16	+5V
Digital Ground	72	
Frame Ground	1	
Reserved	35	Committed to other Modules
PI Bus	58	32 bit, error Correcting
Module I.D.	6	
TM Bus	4	
Control	8	System Reset, Clock
IEEE-488 Bus	19	
Discretes	20	Fault det/Pwr trans/ Overtemp/etc Protection
Interrupts	6	
Local Mem. Bus	48	
Spare	23	Growth
Total	316	

Table 1 shows that the designer of this module has been forced to make several difficult decisions because of pin limitations. For example, the Joint Integrated Avionics Working Group Module Interconnect Document recommends one power ground pin per power pin, yet only a frame ground was used. Plus, this document recommends that one signal pin per ground signal pin be used (the ratio of 4 to 1 as shown in Table 1 is acceptable however, but not preferred). Also, a dual redundant PI bus would be preferred instead of only one (requiring another 58 pins). And, the designer is likely restricted from using more sophisticated cache coherent busses such as Future Bus + (instead of the PI bus) because 91 pins would be required for a 32 bit implementation. As the width of the data field increases from 32 to 64 to 128 bits over time, the use of parallel traces throughout the electrical backplane becomes virtually impossible. The use of parallel data lines brings on more problems than increased pin counts and increased number of layers. The problem of data skewing for parallel traces is significant for clock rates of several Megahertz and higher and requires traces to be of equal length regardless of the separation of the source and sink modules. One recent design required the use of equal-length PI bus traces 120 cm long, which is over twice the dimension of the physical backplane.

Let us now look at the interconnect, speed and topology issues of this packaging hierarchy now that its basic building blocks are described.

BACKPLANE IMPROVEMENTS NEEDED

The most severe limitation in maintaining system speed and reliability occurs at the backplane. Photolithography advances applied at the chip and MCM level are no longer appropriate. The backplane must achieve needed wireability through multiple layering and/or through the use of larger areas. One recent backplane design which supports modular avionics has a 22 layer construction which can connect 40 SEM-E modules through its electrical traces. The backplane is 0.4-0.5 cm thick and its size is 40 cm by 50 cm. A 300 pin card-edge connector is used. In order to minimize the number of layers and improve routing, 8600 blind vias were used (the failure of just one of these vias will cause the backplane to malfunction.) MIL-HDBK-217-E analysis revealed an MTBF of just over 6500 hours. This failure rate is considered serious in that it is less than the reliability of each module (at around 10000-15000 hours), yet removal and replacement of the backplane at the flight line is a tedious, time-consuming maintenance action. (In addition, such "paper" MTBFs are usually 2-3 times higher than what is later reported in the field).

The main driver for this low MTBF is the quantity of plated-through-holes which are needed to support the large number of connector pins (discussed above) and the backplane signal density required.

Improvements in electrical backplane technology has reached a point of diminishing returns in that only marginal improvements in wirability and speed can be achieved and then only after great effort. "Custom" designs can be imagined that use point-point lines or coax ribbon cables to increase backplane speeds but these designs fail to support the concepts of module interchangeability and growth.

The advanced backplane needed must simultaneously possess improved reliability, increased wirability over longer distances, higher speeds along with no restrictions being placed on module placement within the rack. Looking just at the PI bus, its functional replacement by non-electrical means would reduce the number of layers from 22 to 14 and most of the blind vias would be eliminated. The reliability of the backplane would then be more than doubled. Further, if this bus function could be accomplished without requiring signal amplification when the signal must travel more than about 50 cm (eg for a 12.5 MHz signal), interface modules could be eliminated.
No new electrical backplane material on the horizon simultaneously possesses the needed properties of low dielectric constant (high signal speed), strength, machinability and high glass transition temperatures to make the quantum improvement needed. A new type of backplane is needed.
A summary of the speed problems connected with the packaging hierarchy is shown in Figure 5 (Ref 3). Note that "RC" effects limit the use of metallic interconnections as we go from the chip to the system level.

The next section of the paper describes a baseline architecture which will help put the upper two tiers of the packaging hierarchy in perspective. Later on, projected modifications to this architecture that will be brought on by further packaging advances will be described, along with an advanced system-wide network to solve the above-described bottle-neck.

BASELINE ARCHITECTURE

Figure 6 shows a representative implementation of the Pave Pillar architecture at a more detailed level than shown in Figure 3 in order to compare its performance with what is expected for the fourth generation. The specific attributes of the building blocks shown in Figure 6 are as follows. Avionic functions such as sensing, processing and crew information presentation and control are interconnected through point-point photonic networks with speeds of 400 Megabits/sec (the Sensor Data Distribution Network-SDDN and the Video Data Distribution Network-VDDN). Stores and vehicle management functions, although not shown, are also connected to the core processing function through Mil Std 1553B (STANAG 3838) busses. Common Processing supports both data and signal processing through a tightly-coupled family of common modules which contains sufficient built-in-testability to accomodate flight-line removal.

Communications between racks and access to mass memories and mission load cartridges is through a high speed, serial fiber optic-based data bus. This bus operates at 50 Mbits/sec and uses a token passing protocol.

The dominant backplane networks are a data network switch and the PI bus discussed earlier. Both networks use 32 bit-parallel wide words with added control lines. The data network is required to handle streaming data for sensors and displays. For example, this switch network would take digitized radar signals, buffer a frame in a memory module and then send it to a signal processor module. Backplane limitations limit the speed of the switched signals to 25 Mhz, resulting in a total bandwidth of 800 Mbits/sec for the 32 bit parallel data words. Along with the PI bus (400 Mbits/sec), current state-of-the-art processor modules can be adequately supported. Representative data processing modules (SEM-E) operate at around 20-30 MIPS and signal processing modules run at around 200-300 MFLOPS.

High speed digitized photonic data from the sensors interface to a Fiber Network Interface Unit module which changes the serial, optical signal to a 32 bit parallel electrical signal that is then controlled by a data network switch located in the global bulk memories. PI bus signalling may be required to be amplified by a gateway module if inter-rack distances are significant, or be converted back to an serial, optical signal by the Gateway module for transport on the HSDB for messages destined for another rack (or coming from a peripheral such as the mass memory). The current-day digital designer is forced into converting data back and forth several times between serial, opto-electronic signals and parallel, electrical signals. This layered, hierarchical hardware design, in turn, results in custom, layered software interfaces to handle associated latencies.

If photonics could be extended to the backplane for data signalling and control (resulting in two adjacent backplanes, where the electrical backplane is used primarily for electrical power and ground functions), a more unified network would result. Not only would software interfaces be simplied, but the bandwidth advantages of photonics over electrical backplanes could then be exploited. However serial/parallel and parallel/serial conversions must now take place at the module, requiring low cost, compact transceivers. Figure 7 shows an early prototype version of an optical backplane built by Harris Corporation in 1992. The objective of this effort was to demonstrate the state-of-the-art of photonics hardware. Here the fibers were encapsulated in a polyeurathane stiffner and was shown to be extremely rugged. Note the use of the passive star coupler facilitates a broadcast network which could be used for the control function. The network ran at 1 Gigabit/sec. Significant packaging advances will be needed to make the transceiver practical however. Further, the use of a passive star has limited use for a backplane in that streaming data from sensors and to displays cannot be accomodated.

PAVE PACE SYSTEM REQUIREMENTS

Several Pave Pace system studies have been accomplished to project post-2005 avionic architecture requirements for advanced military aircraft. In part, the studies (McDonnell-Douglas Corp, Boeing Corp and Lockheed Corp) investigated network requirements for advanced avionic sensors and displays and forecast network and processor capabilities from technology forecasts of photonics and digital packaging available for laboratory demonstration in the 1998-99 time frame. This section of the paper presents summary findings of these studies.

As shown in Figure 8, the Pave Pace architecture continues to employ modular digital processing assets, albeit with much faster modular processors. The studies projected that the highest signalling rates would come from advanced integrated radio frequency (RF) system that is expected to integrate communications, electronic combat and radar functions through a set of shared apertures and modular RF assets. The aggregate transmit data rate (RF suite to processors) was estimated at 7 GBits/sec and would be accomodated by several fiber networks operating at a speed of around 2 Gbits/sec. The integrated electro-optical (EO) system

and the advanced displays each required 2 Gbits/sec of data. The backplane required 2 Gbits/sec.

Figure 9, derived from the McDonnell-Douglas study, shows an artist's conception of the how dramatically different the processing system is expected to be between the third and fourth generation system. The system network and processing system was modelled, using VHDL and ADAS computer-based simulations for CNI, Electronic Combat (EC), Radar and EO functions. Real algorithms were assumed. The McDonnell design showed that the ratio of network speed (Megabits/Sec) to processing speed for the module (MegaFLOPS) were as follows: EC-1:1, Radar:0.2, EO:0.75. CNI did not require ultra-high network speeds. The projected single-width, SEM-E size modular processor which could be packaged by 1998 is described in Table 2 below. It operates at 2400 MegaFLOPS (peak). In order to reduce software control complexity, increase processor throughput and save weight, the data, signal and graphics processing for (at least) the major functions of Integrated RF and Integrated EO systems should be computed with parallel processors contained within a SEM-E module (or double-width SEM-E if necessary). Even after de-rating the average speed of the processor by a factor of 0.35 (simulation results) to account for non-perfect parallelization, operating system overhead, etc,
growth and "design error protection" requires the 2 Gigabit/Sec data rate referenced above.

For a multi-role fighter system postulated for the study, about 17 Gigaflops of processing power is needed. Consideration of various application inefficiencies and I/O bottlenecks states required for real time avionic processes, the study concluded that a total of 48000 MegaFLOPS peak processing power was needed to yield the 17 Gigaflops. Note the relative comparison of third and fourth generation modular processing capability where a ten to one reduction in module count is predicted over one decade of time. In addition, the study concluded that a two-fold reduction in cost, ten-fold reduction in volume and a ten-fold improvement in system reliability should result with the new digital packaging technology. For technology mature in the 1998 time frame, the study predicted the characteristics shown in Table 2.

Table 2
1999 Modular Processing Characteristics

	Data Processor	Signal Processor
Speed (peak) MFLOPS**	450MIPS*	2400
Data Storage (MBytes)	48	32
Data Cache (MBytes)	120	512
Inst. Cache (MBytes)	120	128
Chip Clock Freq (MHz)	150	75
MCM Clock Freq (MHz)	75	75
PCB Clock Freq (MHz)	50	50
Power (Watts)	95	115

*3 CPU MCMs **16 DSPs plus graphics processor

Note that even though these estimates are highly time-sensitive. The assumption made here is that microcircuitry available for purchase in 1996-97 would be used to arrive at a packaged, working modules in 1999. As such, the projected data could be considered to be conservative.

PHOTONIC NETWORK

Now that the network and associated processing requirements for an advanced military aircraft have been defined, this section of the paper will describe the general attributes of the photonic network needed to support these requirements. A composite of the results provided by the above Pave Pace contractors, as well as findings of Harris Corporation, which has been deeply involved in investigating such networks will be discussed.

For advanced processing networks such as Pave Pace, all four contractor team's basic conclusions were in close agreement; however, their specific design recommendations for the network varied. In general, all recommended a switched, photonic network to support high speed digital processing. All agreed that this switched network should unify and interconnect streaming data between sensors and racks and displays and racks and that inter-module signal transfers should also be accomplished over this network. Over time, the parallel switched electrical data network currently employed in the backplane should be replaced with a serial, switched photonic network. As of Feb, 1994, the Scalable Coherent Interface/Real Time (SCI/RT) has been selected by the SAE as the real-time network for future use. Work is underway to validate this standard for a Pave Pace type architecture using the optical-switched network implementation.

Figure 10 provides some general guidelines that shows a switched network is preferred when the number of system terminals approach 64 (this is an upper bound since bus contention problems usually reduce effective bandwidth). Connectivity needs in the past have been small. However, as architectures evolve into distributed systems, hundreds of nodes are possible. Further, Figure 10 shows that photonics is the preferred solution when system speeds peak above around 50 MHz.
It is realized however that alternative backplane designs based on electrical components could be made to work at the data rates required. These designs include the use of point-point links, coax, limited-use buses or ring bus designs where the signal is amplified at each module before being transmitted to the adjacent module. However, the view of the authors is that when factors such as network growth, flexibility, weight, EMI immunity and uniformity are considered, photonics appears to offer the best overall solution for the future.

TECHNOLOGY ADVANCES REQUIRED

In order to field a reliable, compact and affordable photonic network to meet the challenges posed by strides in digital packaging, several technology advances are required. These technologies can be grouped in four areas:
1. Backplane The backplane itself is viewed as posing the fewest technology problems since a working prototype (Figure 7) has been developed and tested for the military environment by Harris Corp. Techniques for stiffening and mounting either clad or unclad fiber are understood. More advanced optical backplane designs are being developed, including the use of free-space hologram reflections between modules and the use of Polyguide (Trademark of the Dupont Corp). This latter approach photolitographically constructs

fine-line patterns on the substrate. This latter type of approach is preferred because it promises to provide electrical backplane-like wirability with fiber-like signalling speeds. However, the insertion loss currently being experienced with this approach is much too high for practical use. Should the Photonics R&D community fail in making this approach feasible over the next few years, encapsulated fiber backplanes can be used.

2.Connector In order to exploit the ease of maintenance that modular avionics offers, it is highly preferred that all module to rack/backplane connectors be "blind-mated" (ie. all electrical, optical and fluid connection matings/dematings are simulateously accomplished by the simple action of inserting/retrieving the module). Such a design allows maintenance personnel to simply insert or retrieve the module to/from the rack without any special tools or time-consuming procedures, even while wearing "Artic" or Chemical Defense apparel. A highly successful, blind-mate card-edge fiber-optic connector has been developed by AT&T Corp and is being used on the F-22 aircraft. This connector supports the use of multi-mode fiber having a core diameter of 100 microns and exhibits impressive insertion loss much less than 1 dB. This connector will allow photonic signalling to/from sensors and to/from the photonic-based HSDB to interface to appropriate I/O modules in the rack. For optical switches that can accept multi-mode fiber, the existing AT&T connector should be adequate. This class of switch converts optical energy into an electrical signal, performs the switch function and then re-converts the signal back to the optical domain. The major components of such a switch has been tested at the US Navy's Naval Air Development Center-Warminster and shown to work at 1 Gigabit/sec. However, the majority of photonic technologists advocate an all-optical switch approach because it is potentially faster, more reliable and smaller (and at present, unobtainable). This type of switch requires single-mode polarization-preserving fiber. The blind-mate connector must now accomodate an 8 micron diameter fiber core (reducing initial module/rack misalignments, possibly a thousand times greater than the fiber size which is one-tenth the diameter of a human hair) and ensure that the polarization of the electric field is preserved. Currently AT&T is working on the development of such a connector. However, it is uncertain that a reliable single-mode blind mate connector can be built due to the immense technical challenges involved.

3.Optical Switch As stated above, an all-optical switch is preferred, but several difficult technical factors remain. In addition to the limitations stemming from the use of single-mode fiber, the size of the cross-bar switches achieved to date have been limited due to excessive losses and manufacturing complexities. Work is proceeding to determine if these problems are surmountable.

4.Transceiver Each module involved in the use of the photonic backplane will require a Network Transmitter/Receiver Unit (NTRU) on each PWB for redundancy. Transmit, receive, clock recovery, serial to parallel and parallel to serial conversion and protocol functions are imagined to make up the NTRU MCM. The main difficulty is in building a small, temperature-rugged laser that can fit inside a small area/height profile available (the goal is to build a NTRU with an area of around 5 square cm and a height of 0.3 cm) and not require a thermo-electric cooler at a data rate of at least 2 Gigabits/sec. Figure 11 shows a sketch of the optical network, along with the connector.

CONCLUSIONS

Advances in digital packaging will make possible impressive improvements in situation awareness and automation processes on future military aircraft. These advances will make extreme demands on connectivity and data rates at the printed circuit board and backplane tiers of the packaging hierarchy. Further, advanced digital packaging makes possible the continued use of a common pool of modular data, signal and graphics processors in support of integrated RF, EO and displays. Sensor-based data rates in turn, are driven into the Gigabit/sec range, dictating that network advances must be made to efficiently use the high-performance digital processors. The network solution recommended is to use a photonic-based switched network that extends from the module card edge to the various peripherals of the network. Many technology issues however remain before such a network can be fielded.

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1."Shared-Memory Multiprocessor Trends and the Implications for Parallel Program Performance", E.P. Markatos and T.J. LeBlanc, U of Rochester Tech Report 420, May 1992.

2."Multi-chip Modules Aim at Next-Generation VLSI", J. Lyman, Electronic Design Magazine, 9 Mar, 89

3. J. Dennis Seals, AT&T Corp.

DISCUSSION

Question: Is it a limit or a constraint to imagine that the next generation of avionics, from a network point of view, would be made using LRMs interconnected with a backplane?

Answer: I really think using an electrical backplane does place limits on LRM intercommunications. At this time, however, all alternative approaches I've heard about require further development and hence, aren't available to replace the electrical backplane.

The problem is a practical one. If we try to speed up backplane signaling (electrical) speeds, we need to figure out a way to preserve signal to noise (S/N) at the receiver as clock rates increase. Going to differential signaling (elimination of common ground) allows speeds to go up, but only at the expense of 100 or so more module pins, which drives down reliability at the connector and results in a more complex, failure-prone electronic backplane. Currently, the F-22 backplane has 24 layers, about 20,000 plus networks, and about 8,500 - 9,000 blind vias, any one of which could fail and destroy the capability of the backplane. Adding more pins/circuits brings on more layers, more barrel cracking of the vias, less reliability, and a bad maintenance problem in removing the backplane at the flight line.

If, on the other hand, we can replace the PI bus through photonics, we eliminate about 7 - 8 backplane layers and 58 pins in each connector. If we eliminate the switched data network in the backplane, we save five layers and 40 pins. The most important thing to do is eliminate the electrical Data Network and use a "unified" photonic network (switched) between sensors/clusters and clusters/displays for streaming data. Here we eliminate several switch modules, I/O modules and gateway modules. The cost of the network is roughly halved if the photonics can be built properly. Eliminating the PI bus, TM bus, etc. doesn't make a big change in cost and weight, because the high cost of optical transceivers required for *each* module overrides other benefits. (We do get much better reliability, however.)

So, I advocate photonic, switched networks (laser based, running at $\geq$ 2 GBPS) for "external rack" communications and leave the backplane for electrical power, PI bus and TM bus. Some day, further downstream, we'll eventually see an all photonic network.

Question: The goals for your optical scheme are met today by SCI. Why not adopt this concept? SCI can operate with 64k nodes without switches. SCI uses differential signals at 0.25V to reduce power and improve performance. 10^{-13} error rates [have been] demonstrated with experimental hardware. Modules can be built with less than 100 connections. No conversion to optical is required. Between nodes, 18 twisted pairs inside a single shield can be used between racks or other nodes. Multi-loops of SCI can provide redundancy or reconfiguration capability.

Answer: Excellent question! I cannot say your idea is wrong or won't work, but rather point out concerns. Work planned with Harris Corp. on with SCI and SCI/RT will hopefully put these issues to bed. Here are some of the concerns with an all-electrical SCI approach.

Our studies have shown the need for a switched network between sensors/racks and racks/displays (streaming data) in order to achieve fault tolerance. Can we build a small, rugged switch for an electrical/parallel network? What is the weight delta relative to photonics? Can we get EMI low enough to support stealthy platforms? For the backplane, what is the reliability impact of SCI in that more connector pins are involved? What is the reliability impact on the backplane in that more lines are required? Will SCI provide the

capability to guarantee low BER for signals across a small, fighter-type backplane in a high EMI environment?

I don't know for sure what the answers to these questions are. We'll start with SCI and see where we go. We'll compare with SCI/RT regarding the protocol. It may turn out that your approach is right for some applications and mine for others. I'm betting that photonics is needed for streaming data over "long" distances of a few 10s of feet and that the electrical solution will be the first pursued at the backplane (despite the problems encountered with the additional pins). Or it may be that you're right for the next several years and I'm right over the longer term. All I know is that the photonic approach is not ready now. Thanks!

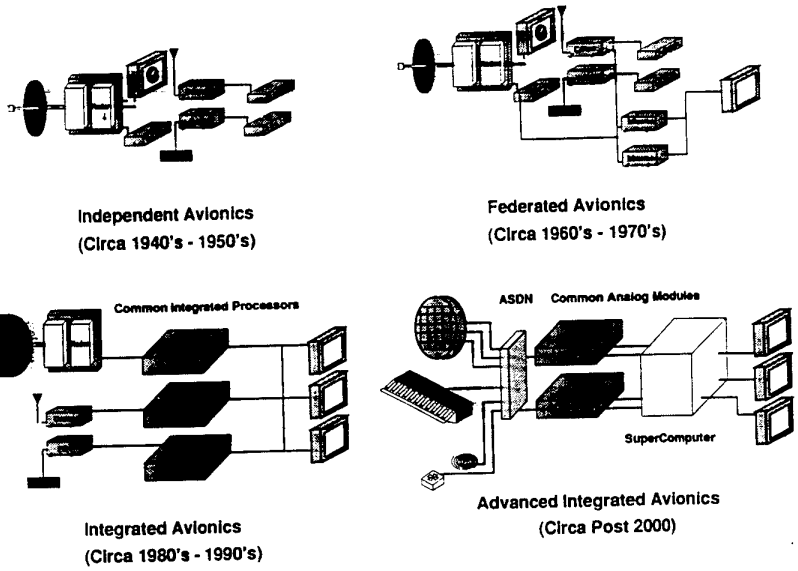


FIGURE 1
AVIONICS ARCHITECTURE EVOLUTION

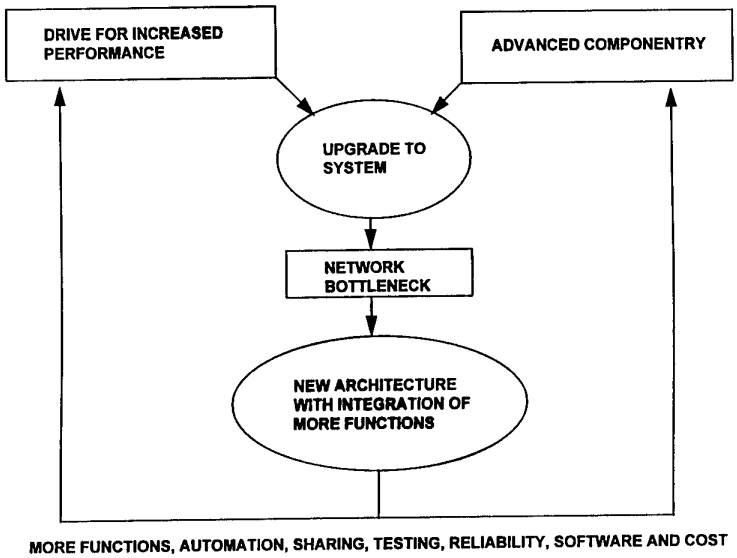


FIGURE 2
THE ARCHITECTURAL CHANGE PROCESS

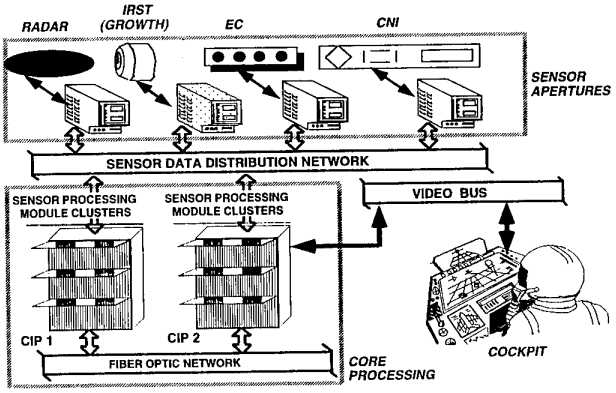


FIGURE 3
REPRESENTATIVE MODULAR AVIONICS ARCHITECTURE
(THIRD GENERATION - 1990 AVAILABLE TECHNOLOGY)

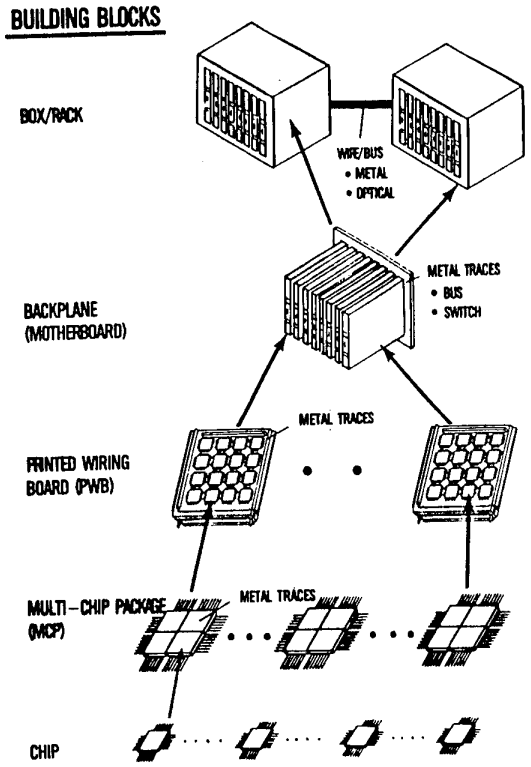
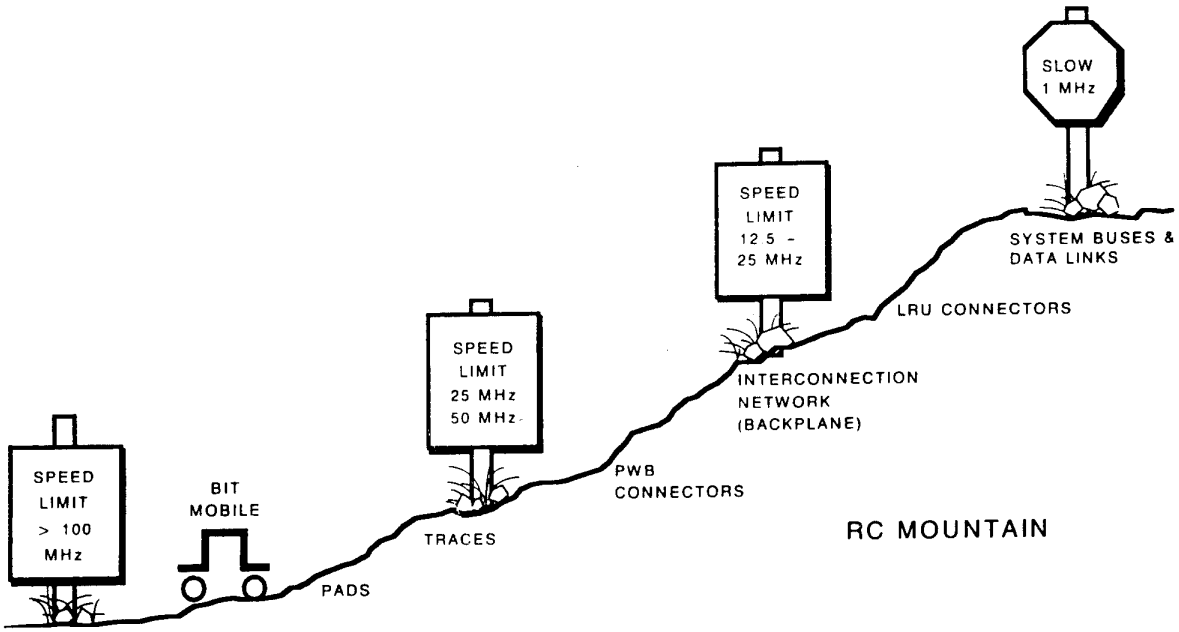


FIGURE 4
DIGITAL SYSTEM PACKAGING TECHNOLOGY



ON-CHIP	CHIP TO CHIP (MCP)	PWB - PWB	SUBSYSTEM TO SUBSYSTEM
CONDUCTOR FEATURE SIZE: .5 μm	10 - 25 μm WIDE 5 μm HIGH 25 - 50 μm PITCH	125 μm WIDE 125 μm PITCH	

FIGURE 5
SPEED LIMITATIONS OF PACKAGING HIERARCHY FOR METAL INTERCONNECTS (REF 3)

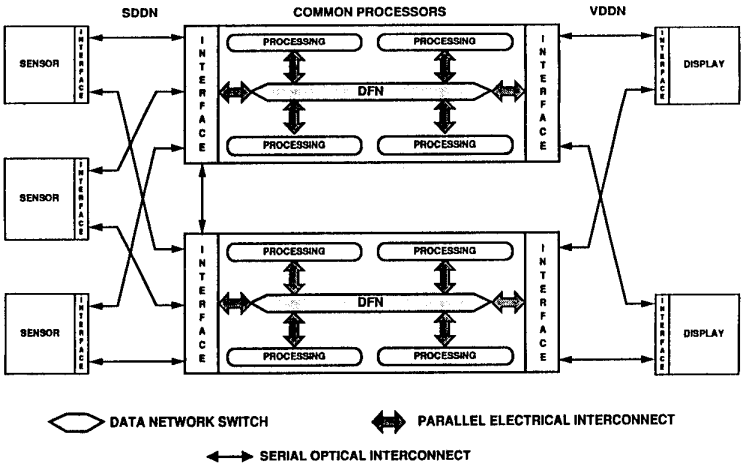


FIGURE 6
REPRESENTATIVE PAVE PILLAR NETWORK

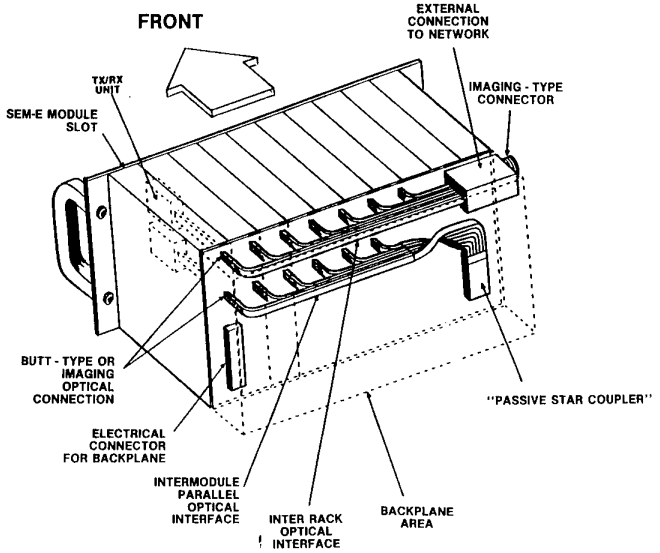


FIGURE 7
PROTOTYPE OPTICAL BACKPLANE

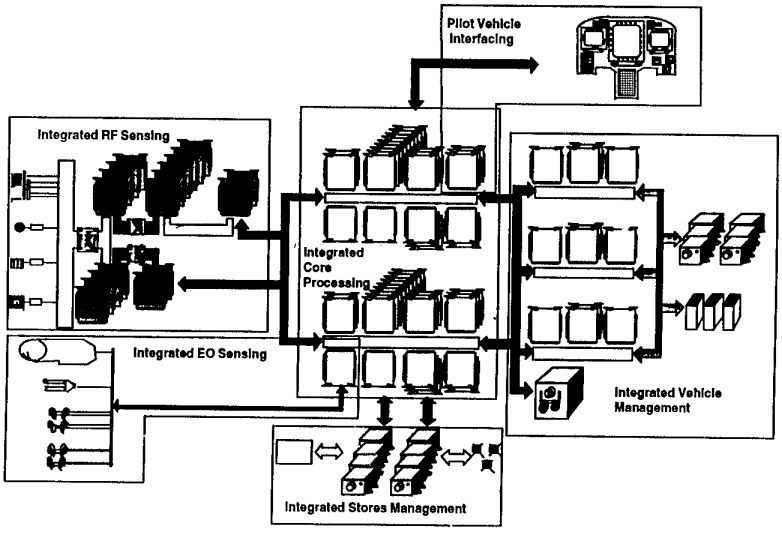


FIGURE 8
PAVE PACE ARCHITECTURE

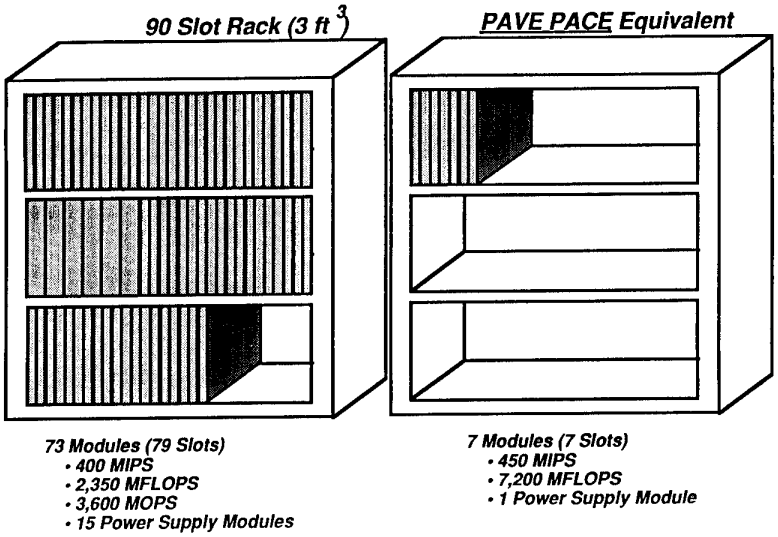


FIGURE 9
COMPARISON OF DIGITAL PROCESSING CAPABILITES
1990 VERSUS 1999 TECHNOLOGIES

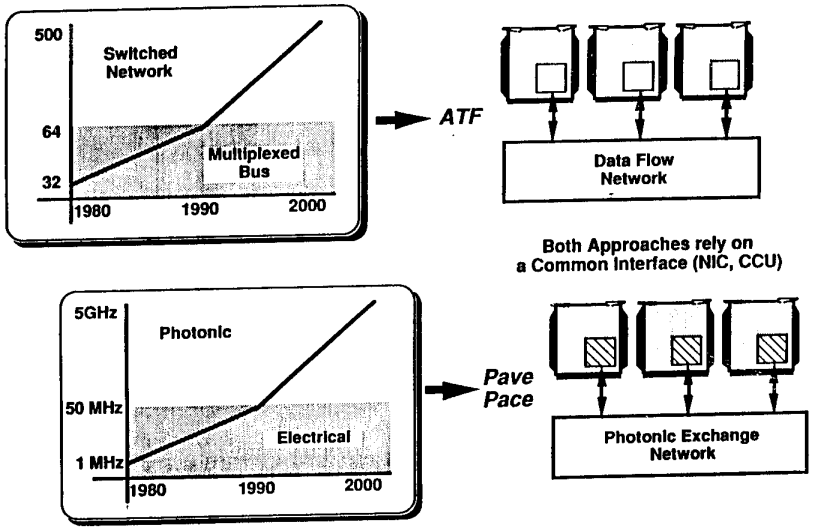


FIGURE 10
ADVANCED NETWORKS REQUIRED FOR
FUTURE PROCESSING

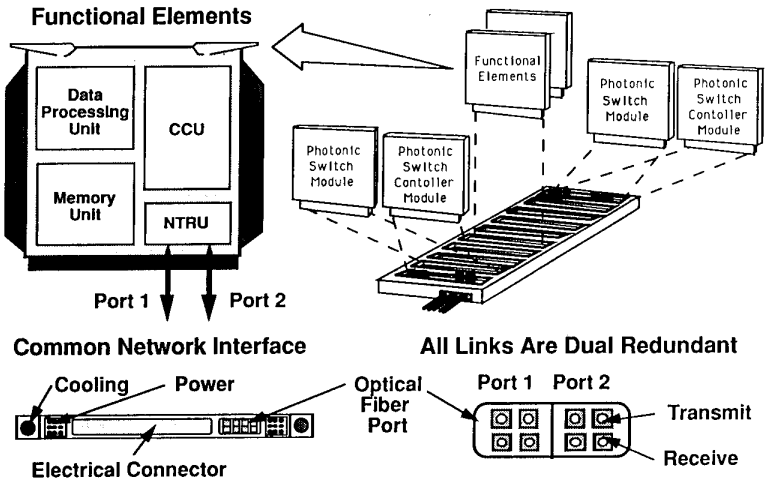


FIGURE 11
FUNCTIONAL ELEMENTS OF A
PHOTONIC BACKPLANE SYSTEM

Standard Hardware Acquisition and Reliability Program (SHARP) Advanced SEM-E Packaging

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SUMMARY

The objective of the "Advanced SEM-E Packaging" is "To identify existing SEM-E and modular avionics characteristics; delineate where they are not defined; and document consensual requirements and guidance for military and commercial applications to provide a framework for open systems architecture implementation." SHARP has teamed with the Air Force Modular Avionics Systems Architecture (MASA) Program to bridge Industry and government agencies in defining and documenting Standard Electronic Module (SEM) format E advanced packaging requirements. The baseline for the working group has been identified, but SHARP and MASA are soliciting participation and input from Industry, other agencies, and NATO.

1 INTRODUCTION

SHARP is a Navy-wide logistics technology development effort aimed at reducing the acquisition costs, support costs, and risks of military electronic weapon systems while increasing the performance capability, reliability, maintainability, and readiness of these systems. The SHARP consists of a joint program between the Naval Surface Warfare Center (NSWC), Crane Division and the Naval Air Warfare Center (NAWC), Aircraft Division - Indianapolis. NAWC AD, Indianapolis is the primary activity for the avionics related efforts. And NSWC, Crane is the primary activity for submarine and shipboard electronics related efforts.

Lower life cycle costs for electronic hardware are achieved through military and commercial technology transition, standardization, and reliability enhancement to improve system affordability and availability, as well as enhancing fleet modernization. Advanced technology is transferred into the fleet through Standard Electronic Modules, Standard Power Supplies, Standard Battery Systems, Standard Enclosure Systems, and Standard Interconnect Systems.

The SHARP's success and credibility is based on the deployment of 8 million products in over 250 different systems using over 350 hardware standards with 50% of those standards used in 8 or more systems. The SHARP research and development initiatives have provided a proven return on investment of 5 to 1 and an increase in reliability of 2 to 13 times. SHARP has established an excellent military and commercial technology transition vehicle and achieved a dramatic reduction in development time of electronics.

SEM processes originated with the Standard Hardware Program in 1965. This logistics program has operated under the name of Sharp since 1987. However, the program functions have been in existence and have operated with the same philosophy for over twenty-five years.

2 BACKGROUND.

The Standard Electronic Module (SEM) was first defined over twenty-five years ago, and is currently documented in MIL-STD-1389 (current revision is MIL-STD-1389D). The first format defined was a module 2.62 x 1.95 inches. The initial format "A" was followed by additional larger formats, the most recent addition being format "E", 5.88 x 6.68 inches, documented in 1988. See Figures 1. and 2. The philosophy driving the program has been the same throughout. Package electronics to a standard form, fit, and function. Develop quality control to produce high reliability and maintainability in military environments. Use standardized packaging, documentation and quality control to reduce system

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life cycle cost. The "SEM E" format, one of five SEM formats of SHARP, is becoming widely accepted as the preferred method of packaging avionics circuit assemblies for the DOD. The SEM E format is also beginning to appear in the ruggedized commercial product sector of industry's products. The SEM E requirements can be found in both MIL-STD-1389 and IEEE 1101.4 and 1101.5

SEMs have been proven successful in meeting the objectives of improving reliability and reducing cost. The use of SEMs have brought about cost savings of millions of dollars over and above the cost of implementing the SEM discipline into system design and development process. Considering SEM cost as an investment during development, and life-cycle-cost savings as a return on investment, typical ROI's for SEM average 8:1 over a 10 to 15 year system life.

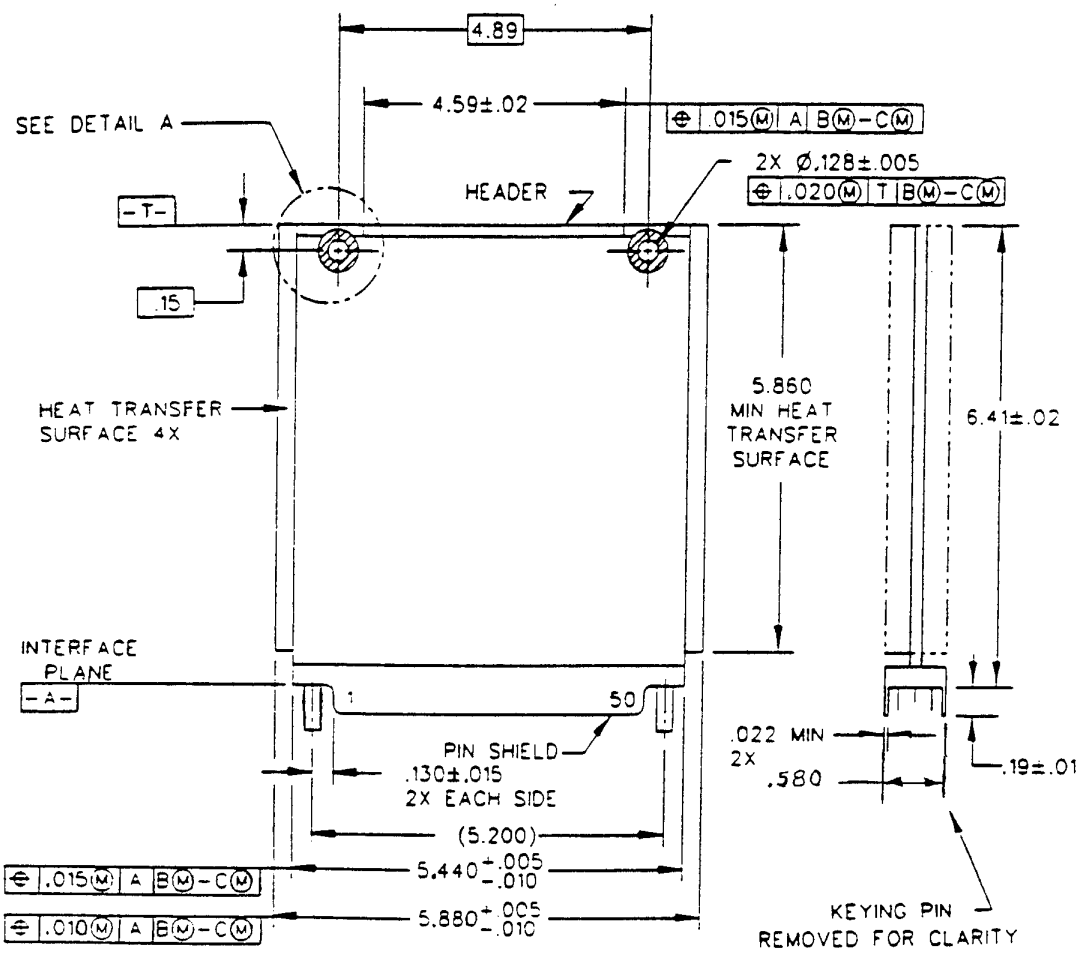


Figure 1. SEM E Format. MIL-STD-1389D, 1989.

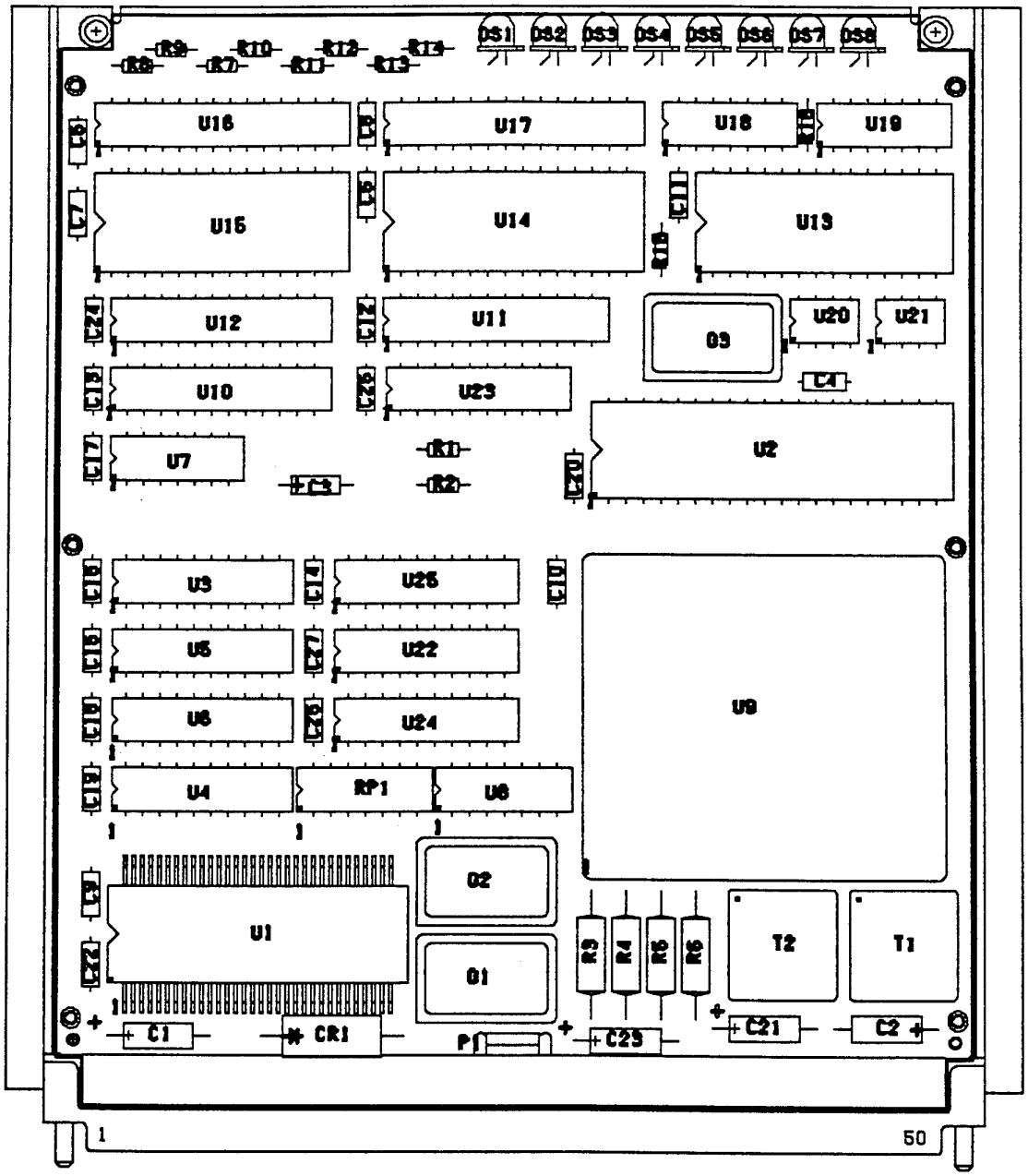


Figure 2. A SEM E Module. Standard Avionics Processor, Key code: ESAP. A processor with MIL-STD-1750A architecture and a MIL-STD-1553 Interface.

3 STANDARDIZATION.

A standardization program can focus at multiple levels. The physical packaging of electronic modules can be standardized, with common hardware, physical form, fit, and interface, achieved across many systems and different platforms. Electronics can be functionally standardized, with each module serving as a building block in the electronic function, and, preferably, as a building block in many different systems. On a higher level, electronic modules can meet architecture standards by conforming to one bus standard or a set of limited operating codes making them electrically and logically standard at the module interface. In all three cases, documentation and test procedures can be standardized, to make all modules meeting the standard capable of operating in same environment, with all modules being described in the same manner. The SHARP SEM, including the SEM-E format, is standardized in the first way, physical form, fit and interface, and an effort is being made to bring the electronically complex SEM-E modules into architectural standardization as well.

This approach creates a building block approach for system development. Figure 3. shows the packaging aspect of standardization. SEM-E is just that, one format. The module, with a documented envelope (physical size and shape, clamping surfaces, heat conduction path), is made with one of a limited number of connector designs, and mates with a backplane connector (also made from a limited number of connector designs), within an enclosure with a specific exterior dimension and mounting points.

There is nothing magic about the precise physical form, fit and interface of many of these parts. Some were developed for SHARP, but most have been adopted from other military programs or industrial use. The important thing about the physical form and fit is that a standard has been set, and then built upon. (For instance, the growth of SEM format sizes can be directly traced to the 1/4 size gradations of the Air Transport Rack (ATR), MIL-E-85726, an item not originally developed for SHARP.)

Each of these parts has an associated documentation package with drawings of the physical envelope, design requirements, and testing or other certification procedures. The documentation is intended to be detailed enough to permit the manufacture of the parts by multiple vendors, but not so detailed as to specify the process by which the item is manufactured. In the case of SEM multiple vendors may produce a part using a variety of different circuits and components. using a variety of different circuits and components. As long as the connector pin outs produce the same signals to the rest of the system, the internal differences do not matter; the part can appear with the same part number if made by two or twenty vendors.

The result of the physical standardization becomes obvious. What was the development time and cost spent on packaging for the first SEM? No savings over any other comparable design. But what is the savings on the second developed module? The list of tested parts is already there. The list of qualified vendors is already there. The drawings of heat sinks, connectors, an enclosure to put it in; they are there already, and are already documented. And the more modules are packaged in this format, the more associated hardware costs and risks become defined, predictable, and thus, reduced. This does not mean that there would be no risks, after all, it is a different module, the circuitry and electronic components are different, but the packaging is a known quality. There is less chance that $100K worth of circuitry and development time are jeopardized by a $100 connector.

The effect of such physical standardization on maintainability, and on retrofit and upgrades, also becomes obvious using the building block approach. If a modules fails, it is not always necessary to go back to the original vendor, hoping that the replacement is available. There can and usually is more than one vendor. There is, at the very least, a documentation package to be followed for items either out of production or to be second sourced. The enclosure itself can reduce the risk of retrofit and upgrades. New avionics, making use of new technology can be packaged in the same format. Introducing a new enclosure, with higher EMI protection, or lighter weight structure? Package it to the same outside and inside envelop. You remove the old enclosure, and insert the new one in its place. You remove the old modules and insert the new ones or any combination of on original and updated items. A well documented, standard system can accommodate it. Even if the original manufacturers are long gone and/or the technology is new. By using a standard packaging plan, new technology can be transitioned into existing electronic systems or new developments.

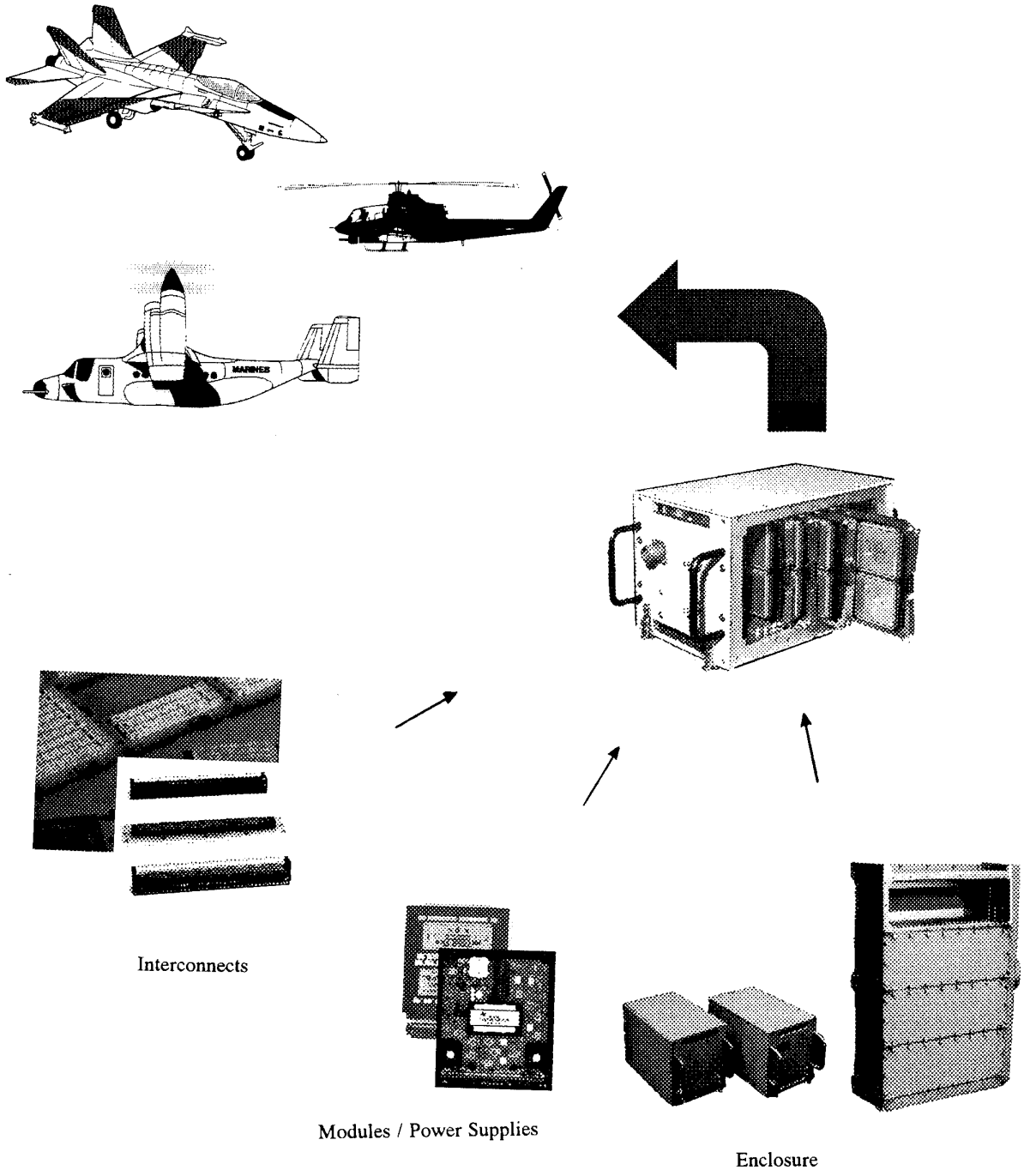


Figure 3. SHARP Avionics Building Blocks.

The use of electronically functional modules also aids this reduction in development time. Obviously, it may be impossible to make an entirely new system out of previously developed standard functions. (Although, with the technology level of the original Format A and B modules, used in the Polaris and Poseidon programs, it was possible. In such small physical formats modules might contain a single Op-Amp, or a selection of resistors, or a few gate arrays.) But development cost savings are achieved in even a few of many modules are functional standards. In current SEM-E configurations, there are computers on a single module, system bus converters on one module, power supplies on one module, etc. Magnitudes of additional payoffs are realized when there becomes a base of SEMs that have a number of different functions. These functions become functional electronics circuit building blocks that are standardized physically for off-the-shelf procurements.

The standard documentation, including the qualification processes, that specify the SHARP system have produced reliable parts and systems. The qualification program not only provides a periodic check of the production quality of vendors, it provides a common point of control and pool of information. The Qualified Products List (QPL) that provides access to multiple, qualified vendors is just one example. The acquisition burden of assuring quality is reduced when using a QPL based on independent testing or other certification. The burden of researching manufacturers, searching for sources, and sorting technological capability from "slick advertising", is all done away with, when the buyer can refer to a well run QPL. The common pool of knowledge produced by QPL maintenance provides users and manufacturers with an opportunity to learn from the mistakes of others, and provide positive feedback to the research and development of new technology to be introduced into the standards program.

4 STANDARDIZATION AND ACQUISITION PROGRAMS

In the development phase of a system there is a reduction in cost and time by reducing redundant engineering circuit design and packaging, some performance verification testing, and documentation preparation. SHARP has also seen more credible contractor pricing in R&D proposals due to the wide visibility of SEM development and production costs. SHARP also has resources and facilities available to assist in evaluation, specification and design of electronic systems.

During production the use of a standards program aides in increasing production competition. There are existing qualified sources for many of the items needed for procurement; in general, the more standard items used in the system, the more existing sources. Common test equipment and program sets can be used to support many systems that use SEM. The equipment can be acquired as "Government Furnished Equipment" or as directed "Contractor Furnished Equipment".

In operation of the system, the level of documentation and high reliability results in reduced maintenance costs. SHARP has seen improved system reliability through monitoring of module vendor quality, and a system to feedback field failure data. The interchangeable "module building block" parts, reduce the variety of spares, tools, and test equipment required. Functional specification of SEM allows the use of non proprietary replacements, and reduces the dependence on any one vendor. Lastly, a system following SHARP has a less risk associated in a system upgrade or retrofit, due to documented design, functional specifications, and multiple sources.

5 STATE OF MILITARY STANDARDIZATION.

These reductions in cost and improvements in reliability are certainly the goals of standardization. With SHARP we have reached many of these goals in a wide variety of systems within items documented in SHARP are used the situations we have only heard of through vendor feedback. For instance, SHARP connectors and backplanes and used in missile applications, ground based vehicles, US Navy shipboard systems, and avionics (in US military platforms, commercial jets, and European fighter aircraft).

We have also seen limits to the use of the SEM. The standards are designed to meet the requirements of a wide range of environmental and functional needs, but there are special situations where SEM cannot cover all requirements.

What is much more common, is the misuse of the term "standard", and the ability of system designers, program management, and suppliers to bend standard

requirements until they are meaningless. If the goal of standardization is commonality of products within multiple systems and platforms, there are very few standardization programs which have contributed major savings throughout DOD.

Referring to just the physical form, fit and interface of SEM-E, the SEM-E requirements are fully defined in the current issue of MIL-STD-1389 and IEEE 1101.4 and 1101.5. Yet everywhere one can see "SEM E" modules which do not meet these requirements. Industry has produced a plethora of "SEM-like" modules, most roughly 6 x 6.5 inches in size, but with a wide variety of exact dimensions, pitches, connectors.

In Figure 3., each building block fits together in a proscribed manner. A change in physical dimension can make a product unfit for use within this system. Modules too wide or tall will not fit into the enclosure. Modules of various pitches must be matched by changes to enclosure card guides. Most obvious is the use of different connectors on "standard modules". If two vendors produce the same function on their modules, capable of use in a variety of systems, what good is this commonality if each vendor uses a different connector that equates to differences in frames, circuit boards, etc.? Will the supply system be able to contact both sources for a spare? No, not without carrying each vendor's product as a separate part single source item.

How much money has DOD invested on these "less than an inch" variations? How many "standardization" documents have been written with size requirements so loose that two modules meeting the requirements cannot fit into an enclosure also built to the same requirements? How many "standard systems" include so many variations and formats as to make the exercise in standardization pointless?

What drives these endless variations in electronic packaging? Obviously there is sometimes a real technologically based need for a specific packaging variation. SHARP has long recognized that SEM is not appropriate in all situations.

In the final analysis, standardization programs in military electronics, have not lived up to their potential, failed, or have never been tried because the military has not insisted that it be done. Many of the less than successful "standardization" documents have been either written by the government, or written under the direct influence and review of the government.

The success of SHARP, and SEM in specific, can be attributed to the long continuity of the program, the advocacy of the navy and the care taken in the less exciting aspects of logistics, documentation and certification. In order to increase the future use of standards where appropriate, and avoid trying to custom standardize all future improvements to modular electronics, SHARP has built on over a quarter of a century of experience. This can only be done by increasing contact and discussion with our end users, and bridging government and industry to have consensus on Advance SEM-E standard packaging.

6 ADVANCED SEM-E PACKAGING.

If you examine the currently documented SEM E Format in MIL-STD-1389, you will see a very basic module, but one with which there is much data regarding design, production, and testing. It does not have attached clamps on the heat conducting rib, or insertion and extraction levers. (Requiring these items would directly force the user to put the module in his system in a specified manner.) Its maximum thickness is 0.580 inches thick. (Only limited vibration, shock and thermal testing has been done on thicker modules.) It is designed to conduct heat away from the circuitry through the guide rib. (Still the most common method of cooling modular electronics.) Its maximum recommended power output is 35 W. (Although many designs exceed this maximum recommendation with large success.) The documented connector design is for digital signals of up to 250 pin outs. (Other connector designs are in process.)

This design is still adequate for many systems. However, SHARP research and development programs are already working to expand the capability of SEM E packaging. The program has and is examining the efficiency of module clamps, and insertion and extractor levers. Power supplies are being developed in greater module thicknesses, with analysis on the reaction to greater mechanical stress. Changes to enclosure and module design are being studied in order to increase heat disapation. A 396 contact connector has been developed, and is being documented. SHARP is also moving to insert RF capability and fiber optics into our standardization program.

SHARP has updated its documents and inserted new technologies in the past. But the number and variety of technologies requested for inclusion in SHARP has never been as large as it is today. The program does

not wish to try to include "something for everyone", and it may well be that some of these technological improvements will prove inappropriate for standardization at this time. SHARP also wishes to include technologies appropriate for current use and future development. In order to accomplish these goals, SHARP needs the aid of our users.

SHARP is collaborating with the Air Force Modular Avionics Systems Architecture (MASA) program to bridge industry and government agencies in defining and documenting SEM format E advanced requirements. The baseline for the working group has been identified, but SHARP and MASA are soliciting participation and input from industry, other agencies, and NATO.

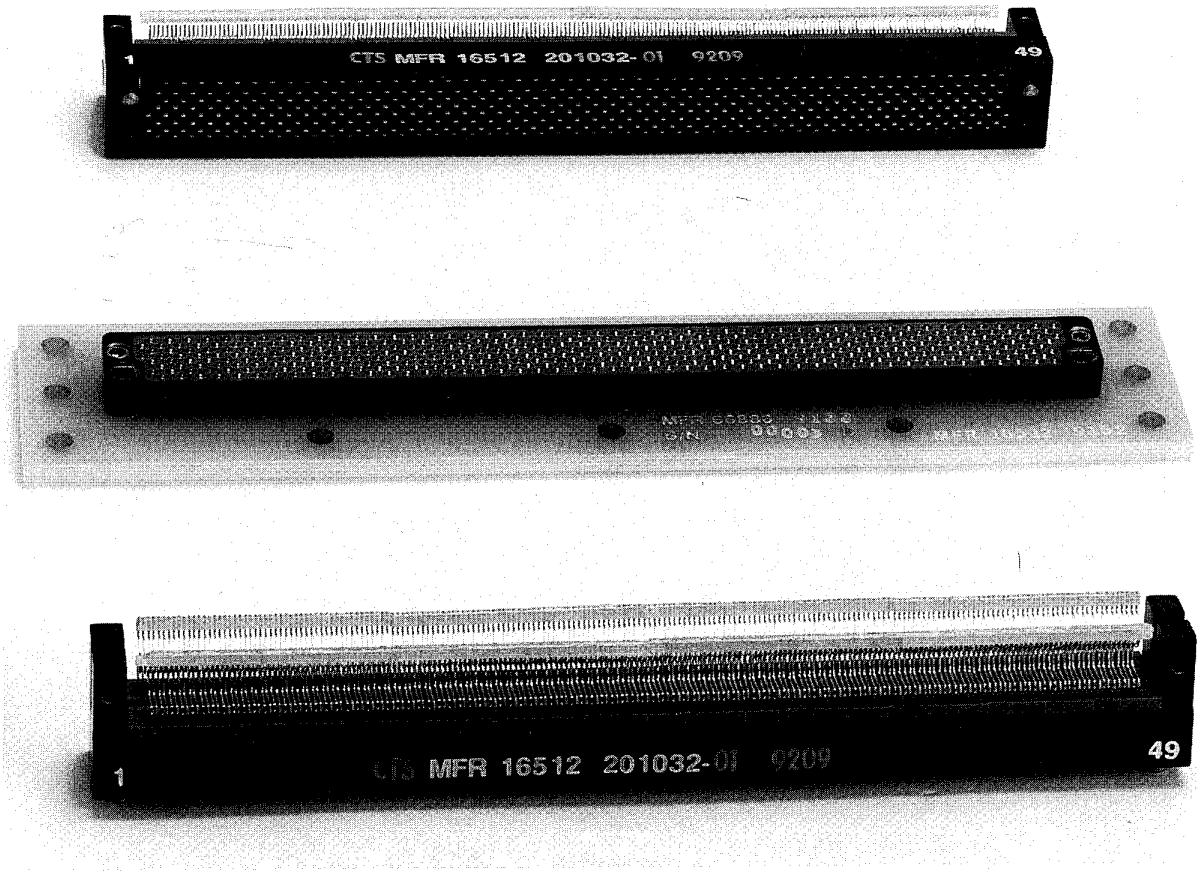


Figure 4. 396 pin High Density Connector. Meets SEM E Format requirements, while increasing pin-out density, and making room for specialized contacts, including photonic termini, RF contacts, and coax.

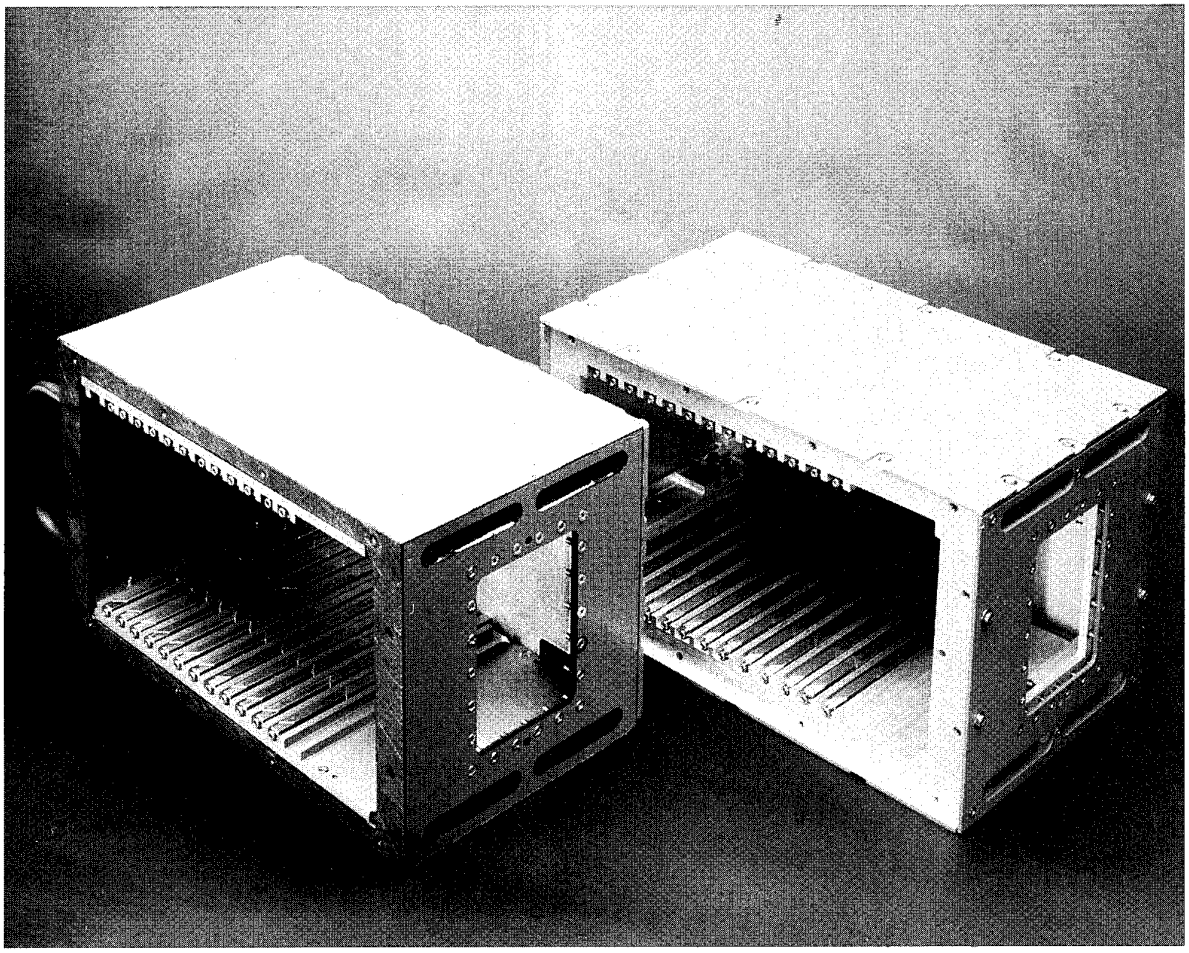


Figure 5. Standard Enclosure meeting 3/4 ATR requirements. An aluminum design (weight: 11.5 lb.), right. A composite design (weight: 7 lb.), left. Each enclosure is designed for SEM E modules and could accommodate the same backplane, or fit in the same space in an aircraft.

DISCUSSION

Comment: ASAAC proposed a larger format (150 x 233 mm).

Author's Reply: NATO has not selected or endorsed a standard format at this time.

Question: What are the reasons for having "SEM-E – like" modules and not SEM-E modules?

Answer: There are several reasons why these variations exist. Some variations in "SEM-E" formats result from the education and awareness process. Many separate committees and groups are responsible for documenting variations on SEM-E; some groups [are] working without information from other standards bodies. In addition, there are profit advantages for industry in creating a new format or a variation from a standard format. Most of the variations that exist were driven by industry, either working in an industry group or a military group.

Question: Commercial avionics have chosen very large formats. Cost reduction is an important parameter. How [are we] to be dual use if the military avionics adopts a small format?

Answer: The military adopted SEM-E based on platform requirements and the support of multiple architectures that also produce supportability gains for the military operating environment. There is some concern over the effect of vibration and shock (military operation) on the longer connectors of larger modules. Dual use does not result from only the direct use of specific modules. Dual use can be at the component, technology and process levels, resulting in reduced time and cost. SEM-E is starting to be used in the ruggedized electronics area and is documented in an industry standard.

Question: Is the SEM-E format a constraint on the introduction of commercial technology into modules – would a larger format allow the earlier incorporation of commercial technology?

Answer: No, the inclusion of COTS items in SEM-E or any military format is not precluded by size of format. The inclusion of COTS is more dependent on environmental requirements, both of vibration in small military aircraft, and salt and corrosives on aircraft on shipboard. The military acquisition process also influences the use of COTS. Aspects of COTS and dual use will be discussed in greater detail in Mr. Hawkins' paper tomorrow, which will also deal with planned changes to SHARP to make the development and approval process quicker and more cost efficient.

Question: The available circuit area of the SEM-E format is one limitation. Another is the nominal 35W passive cooling limit. Is this a significant limitation and is SHARP considering some more "exotic" cooling technologies to raise the P_{MAX} limit?

Answer: The requirements of MIL-STD-1389 only advise 35W and request information on cooling methods for higher power. There are examples of successful methods for higher power. NAWC is studying additional cooling methods: advanced heat sinks, flow-through cooling, etc. Any of these methods may be incorporated in SHARP in the future. SHARP has seen that applying good Systems Engineering and design processes typically produces modules of less than 100W. These can be adequately cooled by air-flow-through or conduction. The typical air conduction cooled SEM-E can dissipate up to 50W, and air-flow-through up to 80 - 100W. There has been very little, if any, requirement for liquid flow through cooling and immersion cooling outside of the F-22 program.

FASTPACK : Solutions optimisées pour le conditionnement de l'avionique modulaire issues d'une étude paramétrique. Part I : Aspects Porteur.

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1. RESUME

• L'avionique modulaire est l'un des concepts majeurs qui s'appliquera aux systèmes avioniques futurs dans un objectif de coût (LCC) abordable et d'amélioration de la disponibilité opérationnelle. Les objectifs associés à un tel concept sont nombreux : l'amélioration de la fiabilité, la standardisation, l'interchangeabilité, l'interopérabilité... C'est pour atteindre ces objectifs qu'il est nécessaire de définir des caractéristiques standards au niveau des modules (LRM).

• La définition de ces standards de LRM a un impact direct sur les modules et leur conditionnement. Le choix du meilleur concept passe alors par une étude précise des répercussions de chaque solution à tous les niveaux (racks, soutes et porteurs) et dans tous les domaines techniques (thermique, électrique, mécanique, protection électromagnétique, connectique). Cet article présente donc les résultats de cette étude paramétrique porteur/système-avionique et plus particulièrement l'incidence sur le porteur, avion ou hélicoptère, des choix possibles de concepts.

• La méthode utilisée définit les contraintes porteurs à paramétrer et leurs interactions mutuelles. Les répercussions sont d'abord intégrées dans un modèle représentatif de missions types. Ainsi les résultats, domaine par domaine, montrent l'importance des effets sur les systèmes de servitudes porteurs. Enfin, un processus de dimensionnement complet du porteur incluant les aspects fiabilité et les besoins fonctionnels aboutit à la synthèse. Celle-ci tant quantitative que qualitative permet de vérifier la robustesse des compromis effectués.

• En conclusion, la maîtrise du compromis global porteur/système-avionique, par une approche d'ingénierie simultanée, permet de justifier une solution de conditionnement de l'avionique modulaire dans l'optique d'un système futur.

(Cette étude a été réalisée avec le support du Service Technique des Télécommunications et des Equipements aéronautiques (STTE), département avionique du Ministère Français de la Défense, dans le cadre des travaux nationaux accompagnant le programme multinational ASAAC).

2. LISTE DE SYMBOLES

- ASAAC : **A**llied **S**tandard **A**vionics **A**rchitecture **C**ouncil.
- ECS : **E**nvironment **C**ontrol **S**ystem.
- FASTPACK : **F**rench **A**saac **S**tudy **T**eam for **PACK**aging.
  Part I : Aspects Porteur
  Part II : Aspects Avionique
- LRM : **L**ine **R**eplaceable **M**odule.
- LCC : **L**ife **C**ycle **C**ost.

3. INTRODUCTION

L'architecture de l'avionique des avions et hélicoptères de combat futurs se caractérisera par une structure modulaire. Des fonctions élémentaires d'un système sont conçues chacune dans un module différent et l'association d'un ensemble de modules permet de créer une fonction complète de l'avionique. D'un point de vue physique, cette conception se traduit par un nombre donné de modules, dénommés LRM placés dans un rack.

Les principales caractéristiques demandées à cette architecture et aux modules la constituant sont :
- l'interopérabilité et l'interchangeabilité,
- la fiabilité,
- la modularité,
- la maintenabilité,
- la minimisation des masses, volumes et coûts.

L'objectif du conditionnement de l'avionique modulaire est donc de définir des concepts et des standards d'interfaces capables de répondre à ces caractéristiques dans les six domaines suivants :
- la distribution électrique,
- le contrôle thermique,
- la compatibilité électromagnétique,
- la mécanique,
- la connectique,
- la compatibilité avec les porteurs.

Dans le but d'avoir des concepts prenant en compte, d'une part, ces six domaines simultanément et, d'autre part, les technologies futures, le groupe FAST a mené une importante étude paramétrique du conditionnement, nommée FASTPACK, rassemblant trois industriels équipementiers (Thomson-CSF, Sextant Avionique et Dassault Electronique) et 2 avionneurs (Dassault Aviation et Eurocopter France).

La démarche suivie dans FASTPACK consiste, pour chacun des domaines, à isoler l'ensemble des paramètres influents et à les

faire varier entre des valeurs classiques et des valeurs prospectives (horizon 2005). Ces paramètres sont ainsi liés à la physique des phénomènes et non à une technologie donnée. Les résultats de cette étude paramétrique sont obtenus par une utilisation importante de simulations numériques.

FASTPACK permet donc de déterminer les limites d'une solution ou d'un concept en fonction des hypothèses faites par le concepteur de l'architecture de l'avionique modulaire. L'étude permet aussi d'étudier de nouvelles solutions ou configurations si certaines caractéristiques de l'avionique évoluent. De plus, il est fondamental de noter que FASTPACK permet la prise en compte réciproque d'éléments allant du composant électronique jusqu'au porteur.

4. METHODES

4.1. Méthode Générale

La méthode utilisée dans cette étude est une application de la notion de traçabilité sur la définition des standards dans le domaine du conditionnement. Son but est d'identifier un chemin entre les standards (caractéristiques des modules, règles de conception, ...) et les besoins opérationnels. Dans une première phase, on définit des standards répondant à des besoins opérationnels génériques. Les différents concepts retenus sont issus d'une optimisation au niveau des solutions de conditionnement pour les aspects quantitatifs et d'une réflexion qualitative pour le reste (voir FASTPACK Part II). Dans une deuxième phase, ces standards sont utilisés pour définir des applications types et ainsi justifier les choix et leur robustesse dans un contexte plus large. Il s'agit ici de l'optimisation globale que l'on étudiera aux chapitres 4.2.4. et 6.1. La Figure 1 illustre schématiquement l'enchaînement des différentes parties du processus d'optimisation.

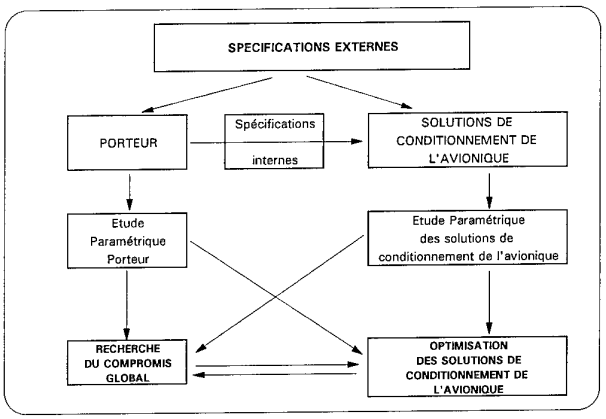


Figure 1 : Schéma de principe de l'étude

C'est dans ce cadre qu'il a été possible d'étudier l'impact de choix dans le domaine du conditionnement à la fois sur les composants électroniques et sur le porteur.

Enfin, il est important de noter que les objectifs de l'étude sont de comparer plusieurs solutions entre elles et que par conséquent, les résultats présentés ont été établis grâce à des calculs d'influences relatives par rapport à une référence et de taux d'échanges entre les différents paramètres.

4.2. Méthode au niveau porteur

Au niveau des porteurs, on peut décrire la méthode utilisée par les quatre grandes étapes suivantes :

4.2.1. Identification des contraintes et des degrés de liberté.

Le système avionique se trouve soumis aux contraintes du porteur qui sont de trois types :
- les exigences systèmes,
- les contraintes d'environnement,
- les contraintes d'installation.

Dans ces trois catégories, les contraintes ont été déclinées à l'horizon 2005 pour extraire un ensemble de spécifications donnant un cadre à la définition des concepts de conditionnement et identifier les paramètres dont les variations ont un impact important sur le dimensionnement du porteur.

Les exigences systèmes ont seulement été quantifiées pour être compatible avec les définitions et les besoins des systèmes avioniques futurs et n'ont pas fait l'objet de variation paramétrique. Ces aspects concernent :
- la fiabilité, la sécurité et la disponibilité,
- la testabilité,
- la maintenabilité,
- l'aptitude à la personnalisation,
- la standardisation.

Les contraintes d'environnement ont été décrites de manière détaillée mettant en évidence les évolutions possibles de certains paramètres par rapport à des spécifications actuelles. Ces paramètres touchent divers domaines : la température, le type, et le débit du fluide, la puissance à dissiper pour l'aspect thermique, le type d'alimentation et la puissance à fournir pour l'aspect électrique et le niveau d'agression électromagnétique. L'ensemble des autres paramètres est resté homogène à des niveaux de spécifications des programmes Rafale ou Tigre.

Enfin, les contraintes d'installation telles que le montage avec ou sans amortisseur, l'installation électrique, les problèmes d'accessibilité de ségrégation, de répartition en zones, de maintenance, ... ont fait l'objet d'études qualitatives permettant l'élaboration de recommandations quant à l'installation des racks.

4.2.2. Prise en compte des contraintes et répercussions sur le porteur pour un système d'armes donné.

Dans chaque domaine et pour chaque paramètre identifié au chapitre précédent, une modélisation de leur influence sur la masse et le volume a été faite. Les lois obtenues sont ensuite intégrées à un modèle d'avant-projet complet représentatif du dimensionnement nécessaire à la réalisation de missions dont les caractéristiques ont été définis à partir de schémas types. Ce modèle permet de prendre en compte l'effet "boule de neige" provoqué par l'interaction des différents paramètres entre eux et l'interaction des différents systèmes entre eux. Il agit ainsi sur les variables d'interface avec le porteur : la masse, le volume et le débit prélevé sur les moteurs pour les avions et la masse et la puissance prélevée sur l'installation motrice pour les hélicoptères.

Afin que les comparaisons recherchées soient significatives, le dimensionnement doit être réalisé pour un même niveau de performances. Les itérations successives permettent ainsi de converger sur le dimensionnement de la masse à vide du porteur en prenant en compte les effets intermédiaires sur la poussée des moteurs, la quantité de carburant nécessaire et la taille pour les

avions et l'installation motrice et la masse porteur pour les hélicoptères.

Ce processus est illustré sur la Figure 2 pour les avions et sur la Figure 3 pour les hélicoptères.

Chaque domaine est dans ce chapitre étudié de manière isolée afin d'identifier les différents effets mis en jeu dans le bouclage.

Domaine Thermique :
Les paramètres variables sont la température d'entrée du fluide dans les racks, le type de fluide utilisé (Air ou Coolanol (COOLANOL 25R (MONSANTO)), la différence de température entre l'entrée et la sortie du rack et la puissance totale à dissiper.

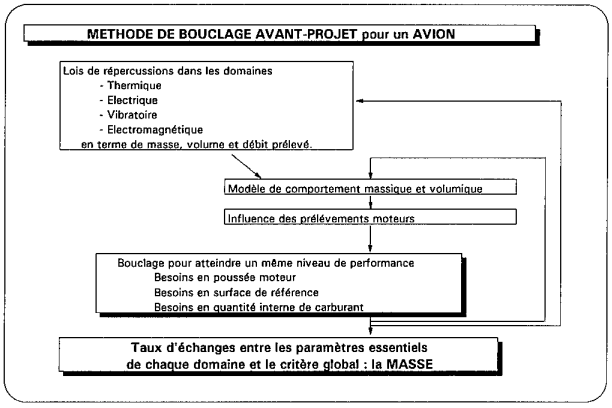


Figure 2 : Processus de dimensionnement pour les avions

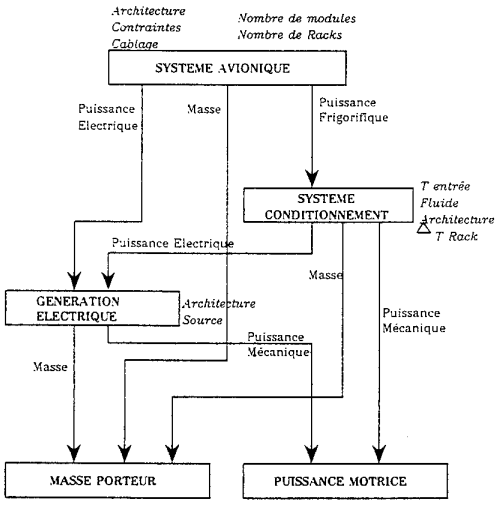


Figure 3 : Processus de dimensionnement pour les hélicoptères

Domaine Electrique :
Les paramètres variables sont le type d'alimentation (270 Vdc ou 115 Vac (fréquence fixe pour les hélicoptères et variable pour les avions) et la puissance totale à fournir.

Domaine Electromagnétique :
Pour les avions seulement, l'existence ou non d'une métallisation de la peau de l'avion et d'un blindage sur les câblages associé à un certain niveau d'atténuation de la cellule a été étudié.

Dans cette partie de l'étude, les interactions entre les paramètres du conditionnement et le dimensionnement du système d'armes ne sont pas prises en compte. De ce fait, sa masse et son volume sont supposés constant. Des variations du système d'armes autour du point de référence sont décrites dans le chapitre 4.2.4.

4.2.3. Recommandations qualitatives

En parallèle de ces aspects quantitatifs issus des modèles mis en place, un certain nombre de domaines ne peuvent pas être modélisés simplement. Ces aspects correspondent essentiellement à l'intégration mécanique et électrique et aux aspects systèmes du dimensionnement. Ils font l'objet de recommandations pour la conception et le choix des solutions.

La méthode décrite jusqu'à présent pour les aspects porteurs couplée avec une méthode similaire pour les autres domaines du conditionnement (FASTPACK Part II) permet de retenir quelques concepts dont les solutions sont techniquement cohérentes vis à vis d'une intégration réaliste au porteur.

4.2.4. Intégration complète en tenant compte des problèmes de fiabilité et des aspects besoins fonctionnels.

Le but de cette étape est de prendre en compte simultanéement tous les domaines cités précédemment ainsi que le rebouclage avec les besoins fonctionnels et la fiabilité.
Les besoins fonctionnels représentent une hypothèse de départ pour dimensionner le système avionique. Par la suite, les objectifs de fiabilité, jumelés avec les études sur les températures d'entrée du rack et les débits de fluide, permettent d'aborder les aspects de redondance. En fonction de ces différents paramètres, les répercussions porteurs sont différentes et un premier critère global peut être atteint : la masse à vide d'un avion réalisant les missions préalablement définies.

Les calculs réalisés par cette méthode sont simplifiés par rapport à la complexité de l'ensemble du problème. En effet, certains aspects n'ont pas été pris en compte (ségrégation, reconfiguration, architecture système, ...). Des variations technologiques ou des évolutions de spécifications sont possibles grâce à la méthode mise en place mais ces variations n'ont pas été entreprises à ce jour.

La Figure 4 décrit l'ensemble du processus ainsi que les interactions avec l'optimisation de solution technique cohérente dont le principe a été détaillé au chapitre précédent. La méthode s'applique aussi bien aux concepts retenus dans l'étude qu'à des concepts dont les paramètres d'interface sont connus par ailleurs.

Il est essentiel de noter que les différentes études paramétriques du projet FASTPACK (Part I et II) interviennent à chaque étape du calcul pour définir les paramètres d'échanges.

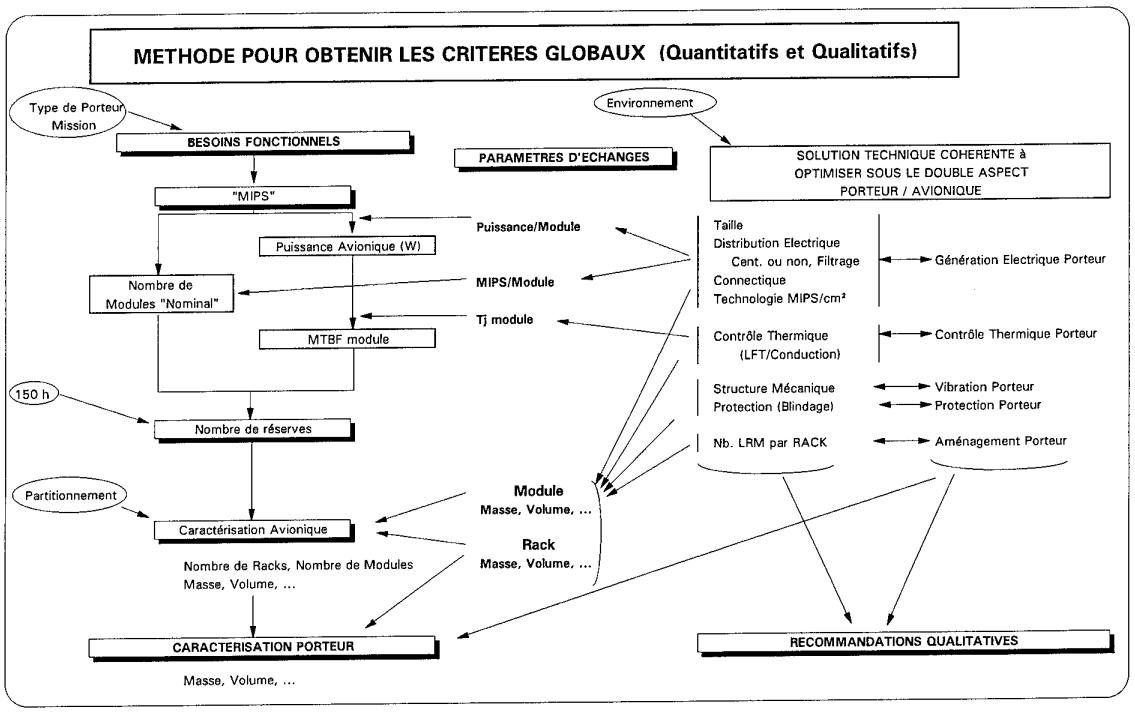


Figure 4 : Processus global de recherche de compromis avec prise en compte des aspects fiabilité et besoins fonctionnels

5. RESULTATS

5.1. Résultats Avions

Dans ce chapitre, on reprend la logique de la méthode décrite ci-dessus pour la décliner sur un avion de combat. Le point de référence de toute l'étude est un avion de type Rafale.

5.1.1. Répercussions Avions

Autour du point de base, on fait varier l'ensemble des paramètres identifiés lors de la phase de définition des contraintes porteur.

Domaine Thermique :
Les plages de variations des paramètres sont les suivantes :

Paramètre	Domaine
Température entrée rack	de 10 à 50°C
Fluide	Air ou Coolanol
Puissance à dissiper	de 10 à 60kW
ΔT rack (°C)	de 10 à 60°C

Les hypothèses principales sur l'ECS sont :
• Tous les racks avioniques sont refroidis par des circuits en parallèle (avec la même température et le même débit). Cette hypothèse est assez pénalisante pour le dimensionnement du circuit de contrôle thermique mais permet de mener le raisonnement jusqu'au bout sans être arrêté par un choix d'architecture.
• La température dimensionnante pour le circuit de contrôle thermique est la température maximale permanente, elle est égale à la température moyenne d'entrée du rack (utilisée pour les calculs de fiabilité) + 10°C pour prendre en compte des profils de missions standards.
• Dans le cas d'un circuit utilisant du coolanol, un échangeur air-coolanol est ajouté et refroidi par de l'air à 5°C, la température de sortie de l'air est voisine de celle du coolanol chaud.
• On définit la notion de potentiel avionique pour couvrir la part de la capacité calorifique effectivement utilisée par le fluide pour refroidir les racks. On considère qu'une température de sortie de 70°C correspond à un potentiel de 0%.

Les résultats obtenus sont de deux types. Les premiers sont un balayage systématique des différents paramètres et les seconds sont des évaluations ponctuelles sur un certain nombre de cas de calculs depuis le composant jusqu'au porteur.

Un ensemble de réseaux a été obtenu en faisant varier les différents paramètres de l'étude thermique. Les deux exemples des Figures 5 et 6 illustrent les résultats de la première famille. L'exploitation de ces réseaux permet d'extraire des influences intéressantes :
• L'impact sur le dimensionnement de l'avion est **important**, de l'ordre de plusieurs centaines de kg. A titre d'exemple, une variation de 20kW à 40kW sur la puissance totale à dissiper induit une répercussion de 350 kg en utilisant de l'air et de 600 kg en utilisant du coolanol (Figure 5).
Ce niveau de répercussion rend l'installation de tels systèmes difficile voire irréaliste par rapport au niveau d'intégration déjà atteint aujourd'hui.
• Vis à vis de la fiabilité, le paramètre essentiel est la température de sortie du rack. Un gain sur ce paramètre a ainsi pu être chiffré. Le passage de 70°C à 50°C pénalise l'avion d'environ 200 kg. Cette pénalité s'accentue pour des températures basses (voir Figure 5).

• Grâce à cette paramétrisation, il est possible d'identifier des domaines d'utilisations de l'air et du coolanol pour minimiser la répercussion en masse sur l'avion. Pour des forts débits (ou faibles ΔT), le coolanol est plus intéressant. Pour des faibles températures d'entrée, c'est plutôt l'air qui est intéressant. Cette conclusion, physiquement logique, doit être pondérée par la notion de potentiel avionique et par le choix d'alimentation en parallèle des différents racks. En effet, le potentiel du fluide primaire (l'air) est mieux utilisé grâce à l'utilisation d'un échangeur Air/Coolanol que dans le cas de l'utilisation d'un seul fluide (l'air) (Figure 6). Mais, d'autre part, des aspects de vulnérabilité peuvent nécessiter une redondance pénalisante sur le circuit coolanol.

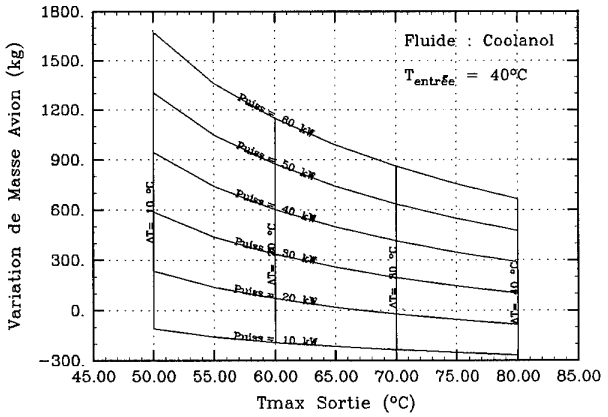


Figure 5 : Réseau Contrôle Thermique Δ(Masse Avion) = f(Tsortie,P,ΔT)

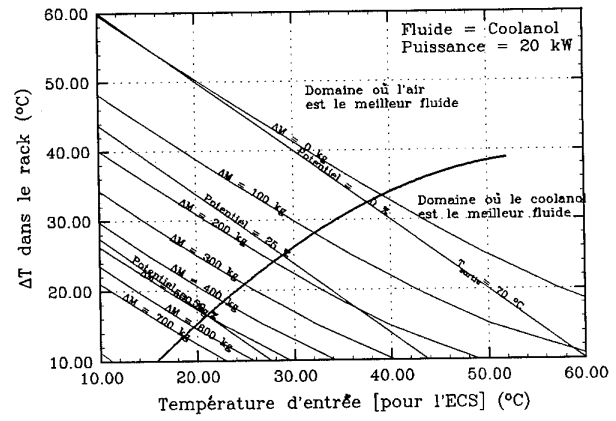


Figure 6 : Réseau Contrôle Thermique (Tentrée, ΔT) dans lequel figurent les iso-ΔMasse Avion (ΔM) et les iso-potentiels

Un deuxième type de résultat est présenté sur les tableaux ci-dessous et illustre sur 8 cas ponctuels l'étude thermique depuis le composant jusqu'au porteur. Tous les gradients depuis le composant jusqu'à l'entrée du rack sont étudiés et présentés dans l'article FASTPACK Part II. L'objet de ce chapitre est donc de passer de l'entrée du rack au porteur en terme de dimensionnement et de répercussions sur l'avion.

L'ensemble des calculs effectués a couvert une centaine de cas :

- 2 Types de fluide : Air et Coolanol.
- 2 Formats : FAST (160x233 mm²) et SEM-E (149x162 mm²).
- 2 Puissances par carte : 40 et 80W.
- 2 Epaisseur de drain conducteur : 2 et 3 mm.
- 2 Types de répartition de puissance : uniforme et avec points chauds.
- 3 Débits de fluide dans le rack correspondant à 10, 15 et 20°C de variation de température.

A titre d'exemples, les tableaux ci-dessous illustre quelques-uns des résultats obtenus.

Fluide : Air; Drain : 3 mm; Points Chauds; ΔT : 10°C				
	Fast-40W	SEM-40W	Fast-80W	SEM-80W
Tentrée	33°C	25°C	11°C	2°C
ΔM Avion	**338 kg**	**447 kg**	**801 kg**	Impossible
Potentiel	**63 %**	**71 %**	**80 %**	Impossible
Puissance	**37kW**	**55kW**	**86kW**	Impossible

Fluide : Cool; Drain : 3 mm; Points Chauds; ΔT : 10°C				
	Fast-40W	SEM-40W	Fast-80W	SEM-80W
Tentrée	35°C	27°C	13°C	4°C
ΔM Avion	**241 kg**	**348 kg**	**690 kg**	Impossible
Potentiel	**27 %**	**42 %**	**67 %**	Impossible
Puissance	**8kW**	**16kW**	**45kW**	Impossible

Tentrée est la température du fluide à l'entrée du rack. Ces valeurs sont issues de l'étude thermique de FASTPACK Part II avec un objectif de 85°C de température de jonction. Cette valeur agit sur l'ensemble de la puissance avionique (c'est à dire 20kW).

ΔM Avion est la variation de Masse à Vide Avion (Répercussions sur l'ECS et Effet boule de neige sur l'avion) par rapport au point de référence : Air; Puissance Avionique de 20kW; T (in Rack) de 20°C et ΔT de 40°C.

Potentiel représente le potentiel restant du fluide utilisé. 40 % signifie que le fluide pourrait refroidir globalement une avionique dont la puissance de référence (20kW) représenterai 60% de la puissance totale.

Puissance représente la puissance avionique équivalente (théorique) qu'il serait possible de conditionner avec l'utilisation de tout le potentiel du fluide.

Impossible signifie que la demande en température d'entrée ne peut pas être satisfaite avec l'architecture système choisi.

On peut facilement remarquer un impact considérable sur la masse de l'avion. Il faut cependant rappeler que sur l'ensemble des cas balayés, la masse peut varier dans de moindres proportions, la valeur de ΔM allant de 50 à 800 kg et le potentiel avionique de 0 à 80 %.

En moyenne, on constate les valeurs suivantes :

	Δ Masse	Potentiel	Puissance
Air	238 kg	43 %	25 kW
Coolanol	193 kg	26 %	10 kW
SEM-E	292 kg	39 %	21 kW
FAST	212 kg	30 %	14 kW

L'ensemble des tableaux présentés montre clairement l'intérêt de l'utilisation du format FAST par rapport au format SEM-E du seul point de vue thermique exposé dans ce chapitre :

- Pour une même température d'entrée, la température de jonction obtenue est inférieure de 10°C permettant a priori une meilleure fiabilité.
- Pour une même température de jonction (85°C) l'impact sur le porteur est diminué de **plusieurs dizaines de kg**, alors que le potentiel avionique est du même ordre de grandeur.

Par contre, la comparaison Air/Coolanol est beaucoup moins évidente du double fait du faible écart de variation de masse en faveur du coolanol et d'une variation conséquente du potentiel avionique en faveur de l'air. Cette conclusion est logique si on fait référence à la Figure 6 puisque l'écart de température, entre l'entrée et la sortie du rack, utilisé dans les calculs ci-dessus est faible (de 10°C à 20°C). On retrouvera ce phénomène au chapitre 6.1. mais cette fois en faveur de l'air, ce qui illustre bien l'ambiguïté du choix.

En conclusion, l'étude thermique montre l'intérêt du format FAST et la nécessité de construire une architecture du système de contrôle thermique adaptée à l'avionique embarquée et aux fluides utilisés afin d'exploiter au mieux l'énergie potentielle de ces différents fluides et de minimiser l'importance des répercussions sur le porteur.

Domaine Electrique

Le but de ce chapitre est de comparer l'impact du choix du réseau électrique embarqué :

- Alternatif à fréquence variable
- Continu à 270 V

Aucune modification importante de l'architecture de la génération électrique n'a été faite, seul les convertisseurs ont été comptabilisés pour garder les mêmes hypothèses de dimensionnement et de sécurité.

La Figure 7 traduit pour les deux types de génération, l'écart de masse avion obtenu pour différentes puissances à fournir.

• L'impact de la puissance est important : 60 kg pour 10 kVa de plus sur chacun des 2 alternateurs.

• Par contre, la différence entre le continu et l'alternatif est très faible (≈ 15 kg) et ne permet pas dans l'état actuel des réflexions de privilégier l'une ou l'autre des solutions. Ce choix ne pourra être fait qu'à un stade plus avancé de la définition du système embarqué et en prenant en compte l'ensemble des consommateurs électriques de l'avion.

Domaine Electromagnétique

Dans ce domaine, la difficulté consiste à trouver le meilleur compromis de répartition des protections électromagnétiques entre le porteur, la soute, le rack et le module. Dans ce but, il a été étudié sur un avion l'impact de la métallisation et du sur-blindage.

Pour obtenir une atténuation correcte au niveau de la peau externe de l'avion, la variation de masse qui en découle est de l'ordre de 130 kg. Cette variation importante associée à un gros problème de validation et de contrôle de cette atténuation nous amène plutôt à envisager une protection directement sur les racks ou éventuellement dans des zones bien identifiées du porteur particulièrement critiques et contenant un grand nombre d'éléments à protéger.

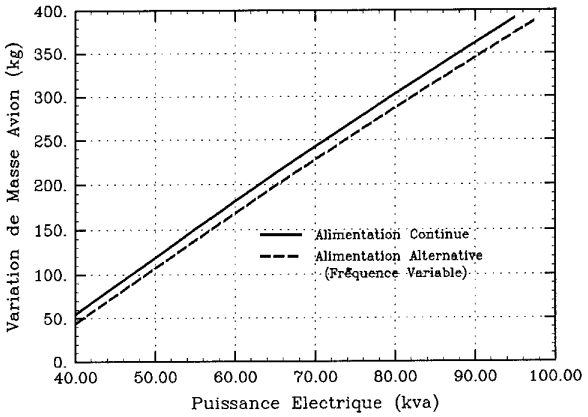


Figure 7 : Influence du réseau électrique sur un avion

5.1.2. Recommandations qualitatives et Installation

Dans le présent article, il a été défini un rack générique pour permettre l'étude complète du conditionnement de l'avionique. Cependant, un grand nombre de limitations sont apparus et ont été rassemblés dans ce chapitre vis à vis d'une définition figée d'un rack, la mise en place de spécifications d'emploi et d'intégration des modules dans le porteur devant être réalisée au préalable.

• Les racks sont le plus souvent placés de telle sorte que les LRM soient situés dans un plan quasi-vertical.

• Ils peuvent être fixés par l'une quelconque des cinq faces autres que la face avant, mais préférentiellement sur les faces de dessus et de dessous. Les différents raccordements entre le rack et l'avion (électriques, optiques et fluidiques) sont situés sur la face arrière du boîtier car cette configuration est celle qui présente le meilleur compromis en termes :

- d'accessibilité aux LRM
- d'utilisation optimale des volumes de soute disponibles
- de protection mécanique et électromagnétique des câblages.

• Le nombre de LRM par rack dépend de la configuration géométrique exacte. Cependant, on peut noter que le nombre de LRM souhaitable est assez important, de l'ordre de 25 par rack.

• Une étude de faisabilité a montré qu'il était possible de supprimer les suspensions pour certains racks avec des restrictions dans le cas de porteurs très spécifiques.

⇒ La présente étude ne permet pas de définir ou de figer une interface standard entre le rack et l'avion.

Enfin, une étude qualitative sur les pertes de charge a montré qu'aussi bien dans le cas du coolanol que dans le cas de l'air et avec les hypothèses faites dans le cadre de l'étude (racks en parallèle), la notion de perte de charge n'est pas critique au premier ordre pour un dimensionnement initial du circuit. Quelques limitations pourraient apparaître dans le cas d'équipements refroidis par air, en série ou ventilés au sol.

5.2. Résultats Hélicoptères

L'étude a été menée suivant le schéma de la Figure 3. Chaque étape a donné lieu à des résultats intermédiaires quantitatifs sous forme de sorties graphiques dont deux exemples sont donnés ci-après (Figure 8 et 9) et des résultats qualitatifs sous forme de recommandations.

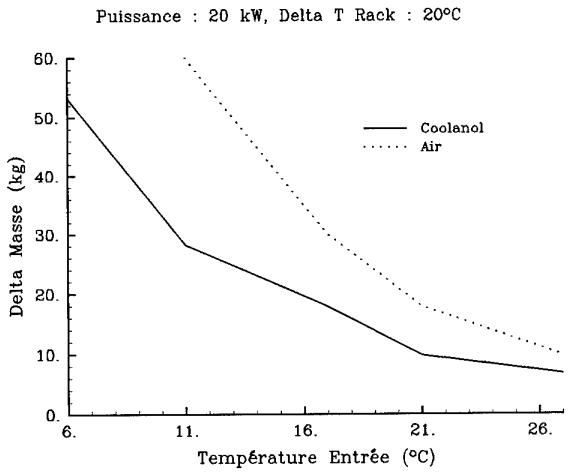


Figure 8 : Influence de la Température d'entrée sur la masse d'un hélicoptère

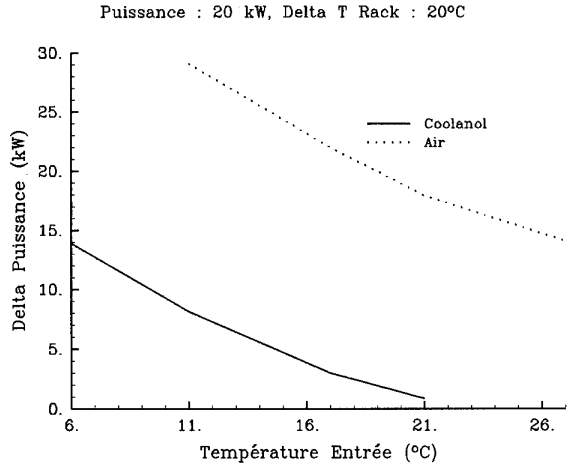


Figure 9 : Influence de la Température d'entrée sur la puissance motrice d'un hélicoptère

5.2.1. Répercussions Hélicoptères

Hypothèses et domaines de variations des principaux paramètres :
Comme le montre la Figure 3, l'étude prend en compte un certain nombre de paramètres et leurs domaines de variation.

• Système Avionique :

Paramètre	Domaine
Puissance	10 à 30kW
Architecture	Basée sur des missions types dimensionnantes
Modules	40 et 80 W
Racks	15 à 30 modules
Contraintes	Répartition du nombre de modules suivant les puissances. Installation de baies dans le porteur.
Câblages	Réduit, Utilisation de la fibre optique

• Système de contrôle thermique :

Paramètre	Domaine
Température entrée rack	7 à 27°C suivant le fluide utilisé
Fluide	Air ou Coolanol
Architecture du système de contrôle thermique	Simplex, Duplex, Mixte (air, coolanol). Echange Air-Fréon, Fréon-Fluide
ΔT rack (°C)	20, 40 et 60°C

• Génération électrique :

Paramètre	Domaine
Architecture	Mono-tension, Bi-tension Distribution
Sources	115 Vac @400 Hz ou 270 Vdc 28 Vdc en secours

Résultats globaux :
Les résultats de l'étude font apparaître que la masse de l'hélicoptère sera d'autant plus faible que la température d'entrée du fluide est élevée.

D'autre part, un fort gradient de température du fluide à l'intérieur des racks sera aussi un élément favorable à la diminution de la masse et de la puissance motrice de l'hélicoptère.

Enfin, l'utilisation de coolanol pour les fortes puissances d'avionique (> 15kW) ou les fortes densités de puissance par unité de surface de silicium semble être l'alternative au choix de l'air. Nous avons pu notamment constater que les diamètres de canalisations pour l'air devenaient très importants aux fortes puissances et que l'installation de telles canalisations posent des problèmes complexes à résoudre.

Résultats par domaine :
• Système de contrôle thermique :
Les études d'architecture du système de contrôle thermique montrent que les paramètres de sortie les plus significatifs, à savoir la masse et la puissance prélevée :
- sont proportionnels à la puissance de l'avionique,
- sont inversement proportionnels à la température du fluide de refroidissement,
- sont inversement proportionnels au gradient de température du fluide de refroidissement à l'intérieur des racks,
- présentent de meilleurs résultats grâce à l'utilisation de coolanol.

ASPECTS FIABILITE et BESOINS FONCTIONNELS

Liste des cas testés :
CAS A et B : Format SEM-E et FAST / Air
CAS C et D : Format SEM-E et FAST / Coolanol

Ce processus de dimensionnement a été effectué sur un avion de combat

Hypothèses :
Ecart de température dans le rack = 20 °C et Température entrée Rack Variable (Autour de 20°C) = = > Tj=85°C
Autres Hypothèses homogènes avec les propositions FASTPACK
Hypothèses technologiques identiques en MIPS/cm², W/MIPS et kW/l (Alimentation)
Quantité totale de MIPS nécessaires = 10000 MIPS et MTBF LRM à 85°C = 5000 h

CAS		A (SEM-E / Air)	B (FAST / Air)	C (SEM-E / Cool)	D (FAST / Cool)
DONNEES	Masse d'un module (kg)	0,68	1,00	0,68	1,00
	Masse d'un rack (kg)	7,20	8,90	8,75	10,55
	Volume d'un rack (dm3)	9,14	12,70	9,14	12,70
RESULTATS	Puissance d'un module (W)	50	85	50	85
	Nombre total de modules	250	150	250	150
	Nombre de modules de réserves	17	12	17	12
	Potentiel du fluide de contrôle thermique	60%	60%	40%	40%
	Masse Avionique LRM + Racks (kg)	**280**	**230**	**305**	**245**
	Masse à installer (*) (kg)	1905	1810	1960	1845
	Volume à installer (*) (m3)	4,47	4,47	4,55	4,55
	Débit d'air prélevé (kg/mn)	41	41	24	24
	Variation de Masse à Vide Avion (kg)	**160**	**0**	**210**	**25**

(*) La masse et le volume à installer incluent la masse avionique et l'ECS (Contrôle Thermique, Génération Electrique, ...)

Figure 10 : Tableau de synthèse des aspects fiabilité et besoins fonctionnels

• Système de génération électrique :
Les études menées sur les architectures de génération électrique font apparaître que l'utilisation de 270 Vdc est légèrement plus favorable que l'utilisation de 115 Vac @400 Hz.
Les paramètres dimensionnants pour la génération électrique sont la puissance avionique, bien sûr, mais aussi le gradient de température à l'intérieur des racks. En revanche, la température d'entrée n'influe que très peu sur le dimensionnement de la génération électrique.

En cas de source mono-tension 270 Vdc, les équipements de production électrique présentent un meilleur rendement au kilogramme que pour des tensions plus faibles, ce qui avantage la solution 270 Vdc.

En cas d'utilisation de tensions mixtes, 270 Vdc et 115 Vac @400Hz, ces gains peuvent devenir moins significatifs jusqu'à s'annuler à cause de la complexité et du nombre plus important d'équipements mis en oeuvre.

5.2.2. Recommandations qualitatives et Installation

Les racks seront installés horizontalement dans les hélicoptères et l'accès aux LRM se fera par l'avant.

Les interconnexions pourront être faites sur différentes faces des racks en fonction de la configuration des baies de l'appareil.
Les racks ne seront pas suspendus.

Les racks seront accessibles soit à l'intérieur du porteur, soit à l'extérieur par des portes d'accès aux soutes.

6. SYNTHESE PORTEUR

6.1. Intégration complète quantitative avec prise en compte des problèmes de fiabilité et des besoins fonctionnels.

Les résultats présentés dans ce chapitre suivent la logique décrite au chapitre 4.2.4. et sur la Figure 4 pour un avion de combat.
4 cas de calculs ont été retenus pour étudier l'impact du fluide de contrôle thermique et du format des cartes sur le dimensionnement complet de l'avion :

Cas A : SEM-E / Air
Cas B : FAST / Air
Cas C : SEM-E / Coolanol
Cas D : FAST / Coolanol

Dans le modèle utilisé, on calcule la surface disponible pour les composants pour en déduire le nombre de modules nécessaires vis à vis du pur besoin fonctionnel. Puis, grâce à une modélisation de la fiabilité en fonction de la température et à un modèle de dimensionnement des réserves nécessaires pour respecter les besoins de disponibilité, on aboutit ainsi à la spécification du système d'armes complet. La masse et le volume de ce dernier, ajouté à l'ECS et à la génération électrique permettent de dimensionner le porteur vis à vis des objectifs essentiels d'un tel système : **le besoin fonctionnel et la fiabilité**.

Dans le tableau de la Figure 10, la démarche et les résultats sont présentés pour les quatre cas d'études afin d'obtenir un critère global de choix : la Masse à vide Avion.

La Figure 10 illustre parfaitement l'avantage du format FAST par rapport au format SEM-E avec un gain de 150 à 200 kg sur la masse à vide et déjà environ 100 kg sur la masse à installer (sur

1900 kg) dans le cas de l'utilisation du format FAST. Cet écart s'explique par une meilleure efficacité thermique et par une surface réelle disponible plus importante (hors connecteur, hors convertisseur opto-électronique, hors système de gestion et de tests des processeurs). De plus, les convertisseurs de tension limitent le niveau d'intégration à partir d'un niveau élevé de puissance, et la surface restante pour les composants fonctionnels est là encore en faveur du plus grand format.

Aucune conclusion significative ne ressort du tableau présenté pour le choix du type de fluide (voir le chapitre 5.1.1. et la Figure 6). En effet, l'équilibre entre la température d'entrée, l'écart de température, le gain de masse des racks avec de l'air, le débit prélevé plus important sur l'air, le potentiel avionique, ... est très délicat à obtenir et à valider. Il faut aller plus loin encore et optimiser dans chaque cas la température de jonction (Tj) et les conditions de fonctionnement de l'ECS.

A titre d'exemple, la Figure 11 montre le type de résultat que l'on pourrait obtenir en faisant varier la température de jonction dans la logique de la Figure 4. Il apparaît clairement un minimum correspondant à un équilibre entre le dimensionnement de l'ECS et le dimensionnement du système d'armes.
Il faut cependant noter que la position du minimum est très dépendante du critère choisi et des hypothèses technologiques ou fonctionnelles.
En effet, si on remplace la masse du porteur par le coût, le minimum devrait se déplacer vers des températures plus faibles.
Si on modifie la loi d'évolution de la fiabilité en fonction de la température, l'optimum se déplacera également.

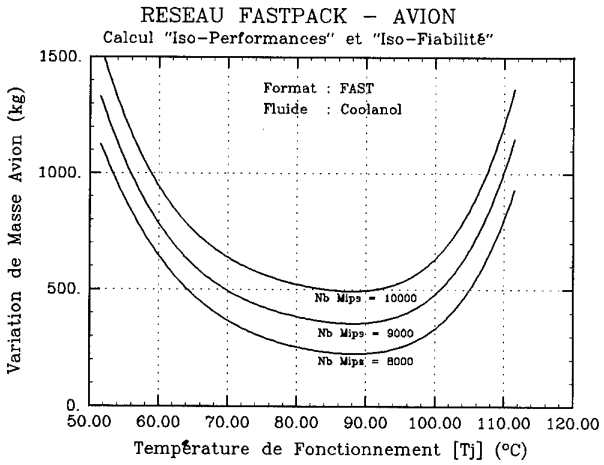


Figure 11 : Réseau Optimisation de la température de jonction

La seule certitude est l'existence de ce minimum dont la maîtrise est le point de passage obligé du dimensionnement des systèmes futurs.

6.2. Comparaison Air-Coolanol qualitative

L'étude comparative montre que l'utilisation du coolanol peut permettre la réduction de la masse du porteur et de la puissance consommée ou prélevée. La présente étude montre que cela est théoriquement possible dés les faibles puissances d'avionique (pour un hélicoptère) et pour la gamme de débits de fluides envisagée dans l'étude.

Mais les contraintes d'installations nous amènent à pondérer ces résultats.

Pour un hélicoptère, dans le cas de porteurs possédant une climatisation de la cabine de pilotage ou des équipements existants devant être refroidis par circulation d'air, l'utilisation du coolanol comme liquide de refroidissement de l'avionique modulaire, aurait pour conséquence la cohabitation de deux systèmes de contrôle thermique. Il est clair que dans ce cas, les gains théoriques en masse et en puissance consommée seraient réduits et voire même annulés. De plus une telle solution mixte coûterait plus cher en fabrication et en utilisation.

Dans le cas d'un avion, le circuit primaire est toujours alimenté par de l'air et l'utilisation du coolanol dans l'avionique nécessite le rajout d'un circuit d'échange avec l'air et donc une certaine pénalité. L'utilisation du coolanol n'est favorable que dans certaines conditions détaillée au chapitre 5.1.1..

Les taux d'échanges obtenus sur l'ensemble de la chaîne Porteur / Rack / Module ne doivent pas occulter d'autres aspects qualitatifs qui ont pourtant souvent été à la base des choix dans les programmes précédents :

- Vulnérabilité
- Communauté à des moyens existants
- Maintenance
- ...

Enfin, le type, l'architecture et la disposition des différents racks dans le porteur entraînent des contraintes spécifiques devant être examinées au cas par cas.

Il est donc essentiel de poursuivre les réflexions menées dans le cadre de cette étude par la validation des concepts retenus, de leur faisabilité et de leur intégration complète au porteur.

7. CONCLUSIONS

Cette étude a permis de définir une position française sur le conditionnement de l'avionique modulaire dont les éléments concernant le porteur sont rassemblés ci-dessous. Les autres choix sont présentés et justifiés dans l'article FASTPACK Part II.

Domaine thermique :

- Pour les gammes de débits de fluides envisagés et pour des puissances avioniques fortes, l'utilisation d'un liquide de type coolanol semble plus favorable.
- L'influence des différents choix thermiques — notamment de la température de jonction ou de la puissance totale à dissiper — sur le dimensionnement du porteur est très important. Il est par conséquent impossible de figer l'architecture de l'ECS sans étudier chaque cas isolément pour optimiser les flux thermiques mis en jeu.

Domaine électrique :

- Le choix du réseau de bord ne peut pas être arrêté dans le cadre de cette étude. Cependant, dans tous les cas, les modules — grâce à une conversion éventuelle à l'entrée du rack — devront être capables des deux types de génération 270 Vdc et 115 Vac à fréquence fixe ou variable.
- La tension secours des LRM critiques sera de 28 Vdc ou de 270 Vdc.

Domaine électromagnétique :
Les protections seront réparties entre les modules (vis à vis des modules voisins) et le rack (vis à vis de l'environnement avion). Dans certains cas particuliers, l'avion, grâce à des soutes spécifiques, pourra apporter une légère atténuation permettant un dimensionnement des racks plus favorable.

Format des modules :
L'étude thermique (du composant jusqu'au porteur) ainsi que l'ensemble des réflexions qualitatives menées par FASTPACK part I et II montre l'intérêt d'un module de grand format, appelé **FAST : 160x233x20 mm³**.

Intégration au porteur :
Etant donné,
- les interactions fortes entre le porteur et les racks vis à vis des interfaces connectiques,
- l'installation de racks dans des soutes (ou baies) de formes et de natures différentes (en terme de protection, de suspension, d'orientation géométrique, ...) et dans des porteurs différents,
- le niveau de connaissance des porteurs concernés,
- la complexité des contraintes de ségrégations, des problèmes d'intégration,

la spécification et la définition des racks n'ont pas pu être faites dans cette étude.

Outre la définition et la justification de concepts correspondant aux objectifs et exigences des systèmes avioniques futurs, cette étude a permis de mettre en place des outils dont l'utilisation a abouti à des résultats passionnants de trois types :
• L'étude de la chaîne complète de dimensionnement depuis le composant électronique jusqu'au porteur pour un environnement et des niveaux technologiques donnés,
• La transparence à la technologie grâce à la robustesse de la méthode. En effet, en s'appuyant sur l'étude des phénomènes physiques et non sur une technologie particulière, les résultats obtenus ne sont certes pas directement transposables mais l'exploitation des outils associés permet de consolider les choix proposés,
• La mise en évidence des difficultés et des points durs lors de la prise en compte et de l'intégration de l'avionique modulaire au niveau du porteur.

Enfin, les critères qualitatifs, la validation des concepts ou la prise en compte de nouveaux sauts technologiques sont autant de domaines qu'il faut continuer à explorer pour élargir le champ d'application.

FASTPACK a suivi une approche d'ingénierie simultanée permettant de couvrir en parallèle l'ensemble des domaines du conditionnement. C'est la porte ouverte à la recherche de compromis pluridisciplinaires et plus généralement à des études d'optimisation globale du système.

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Nous tenons à remercier Maurice GUIOT (BNAE) et Arnaud DEMICHELIS (STTE/AVI) pour leurs contributions tout au long de l'étude FASTPACK.

DISCUSSION

Question: Can you please explain the reason why the aircraft's weight will increase again with increasing the junction temperature above 85 °C after a minimum at the junction temperature of 85 °C?

Answer: To compensate for the loss of reliability with increasing junction temperatures, additional redundant modules have to be provided. This explains the increase of necessary aircraft weight for junction temperatures above 85 °C.

Question: What is the maximum heat density of your hot spots in your calculations?

Answer: 1000 W/dm^2.

Question: From the viewpoint of reliability, is there an advantage for liquid vs. air cooling?

Answer: The answer to this question was not directly one of the objectives of the study. But one can see that for the global optimization, there is no significant difference between air and liquid cooling. You have to adapt the cooling parameter to the specific design you are looking for.

For the reliability aspect directly linked to choice of fluid, this study gives no specific element, but this aspect was taken into account in the global optimization by variation of junction temperature connected directly to reliability.

FASTPACK : OPTIMIZED SOLUTIONS FOR MODULAR AVIONICS DERIVED FROM A PARAMETRIC STUDY Part II : AVIONICS

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SUMMARY

The main requirements for modular avionics have a strong influence on the Packaging solutions for the Line Replaceable Modules (LRMs) and the rack. Packaging is here including: mechanical concepts, cooling, power supplies, interconnections and electromagnetic compatibility. To define the packaging solutions for the next generation of avionics, a parametric study, FASTPACK, has been performed at the platform and avionics levels (for platform, see FASTPACK Part I).
The present paper deals with the avionics part and shows how the FASTPACK parametric study has been conducted in order to define a synthesis in each domain, used to derive Packaging concepts. The main results include the choice of a LRM format, called FAST, a distributed power supply network within the rack, conduction and liquid flow through cooling, shielding on the rack against external electromagnetic threats and shielding on the LRM for rack internal interferences and, finally, the first definition of the LRM connector.

1. INTRODUCTION

The architecture of modular avionics for combat helicopters and aircrafts, as defined in programmes such as ASAAC (Allied Standard Avionics Architecture Council) or EUCLID CEPA 4, is characterized by a structure in which elementary functions of a system are designed each in a different module and the association of modules allows to create a complete avionics function. From a physical point of view, this design is characterized by a given number of modules, called LRM for Line Replaceable Module, placed in a rack. Figure 1 shows the rack and LRMs of future modular avionics.

The major requirements for this architecture and its modules are:

- interoperability and interchangeability by a standardisation of the interfaces,
- reliability,
- modularity,
- maintainability,
- weight, volume and cost minimisations.

The objective of the Packaging of modular avionics is to define concepts able to fulfil these requirements in the six following domains:

- power supplies,
- cooling,
- electromagnetic compatibility,
- mechanics,
- interconnections,
- compatibility with platforms.

To fulfil the interoperability requirement, the concepts must apply to aircrafts as well as helicopters.

In order to have concepts taking into account, on the one hand, simultaneously the six domains and, on the other hand, the future technologies, FAST (French ASAAC Study Team) has conducted a large Packaging parametric study, called FASTPACK. FAST, for Packaging, is constituted of the following companies:

- electronic manufacturers: THOMSON-CSF, SEXTANT AVIONIQUE and DASSAULT ELECTRONIQUE,
- aircraft manufacturers: DASSAULT AVIATION and EUROCOPTER FRANCE.

Papers presented at the Avionics Panel Symposium held in San Diego, CA, USA, 6-9 June 1994.

The main driver of FASTPACK is, for each of the Packaging domain, to determine the key parameters and to give them different values from present technologies to future technologies (2005 time scale). These parameters are then linked to the physics of the phenomena and not to a dedicated technology. The results of this parametric study are derived by an extensive use of numerical simulations, for the domains where software tools are existing. FASTPACK allows to determine the limits of a solution or a concept as a function of the hypotheses made by the modular avionics designer. Moreover, FASTPACK allows to investigate new solutions or configurations if some avionics requirements are changing. Another key feature of FASTPACK is the fact that it takes into account the complete system, from the electronic device to the platform (aircraft or helicopter). It is then possible to determine the consequences, for instance, at the platform cooling system of any modification of the maximum junction temperature of the electronic devices, or to determine, in the opposite way, the consequences at the device level of any modification in the platform mechanical environment. The FASTPACK presentation is divided in two parts: Part I deals with the Platform Aspects and Part II, with the Avionics and is the subject of the present paper.

For the user, FASTPACK / Avionics is presented as five design tools for the five domains of Packaging. The aim of the present paper is to describe the main concepts of each domain with an emphasis on the choice of the LRM format for which two candidates are envisaged:

- SEM E (149 x 162 mm),chosen in US programmes such as Pave Pillar,
- FAST (160 x 233 mm), which is almost the Double Europe format, widely used.

2. COOLING CONCEPTS

2.1 The design tool

The thermal design tool for the rack and LRMs of FASTPACK allows to determine the temperature gradients, on the one hand, between the LRM edges and the components junction and, on the other hand, between the rack input and the LRM edges. The tool is dedicated to LRMs having a maximum power dissipation of 120 W. Heat transfer from LRM to rack is conduction from the component, through a substrate and the LRM central plate, to the LRM edges, in contact with the rack upper and lower cooling plates, where a coolant is circulating. The assembling materials (adhesives, solders) are taken into account.

The tool has been derived in such a way that it can be used by a modular avionics designer at the beginning of a project with its limited amount of information. The main inputs of the tool are, for the LRMs : the total power density (power divided by the LRM useful area), the maximum power density (power divided by the LRM dissipation area, i.e. hot spots) and the size of the LRM format. For the rack, the main inputs are the LRM format and the number of LRMs. The results are then the maximum temperature gradient in the LRM as a function of the components position (the gradient is minimum when all the components are placed near and along the LRM edges and is maximum when they are along an axis perpendicular to the LRM cooled edges). The complete result for the LRM includes also an isothermal surfaces drawing, the nature of the substrate and assembling materials, the thickness of the LRM central plate and the quality of the thermal clamps. For the rack, the result is the coolant type, its flowrate, the temperature gradient in the rack, the cooling plates internal structure and the pressure losses.

Knowing the desired level of reliability for the LRM and the technology used, one can derive a maximum junction temperature for the components and, by the use of the tool, a first thermal design of a rack with all the main characteristics. Two important results are finally obtained: the coolant rack inlet temperature and the rack pressure losses. These values can then be discussed with the platform manufacturer to get a global optimization. The following paragraphes present typical results at the rack and LRM levels: FASTPACK Part I paper discussed the global optimization process with the platform.

2.2 Rack air cooling

Figure 2 shows, in the case of a rack cooled by air, the results of the thermal design tool for a 16-LRM rack, in which the LRM power dissipations are 40 and 80 W. The power is dissipated on a limited number of components (hot spots). Each result shows the temperature gradients in the component, in the LRM and in the rack cooling plates.

The results are presented as a comparison of the FAST and SEM E formats. The bottom of the tables shows, for a maximum junction temperature of 85°C for the components, the air temperatures at the rack inlet. The pressure losses in the rack are also given.

The power dissipation applies on 8 (for 40W-LRMs) or 16 (for 80W-LRMs) surface areas of 1 cm^2 (representing the electronic components). The differences between the two format reach 10°C junction temperature, for a similar air temperature at the rack inlet. Another way to present this difference is to fixed the junction temperature at 85°C (as done in the tables): the SEM E format requires, from the platform, a lower air temperature. The requirement implies, at the ECS level, an increase of several tens of kilograms, as shown in FASTPACK Part I.

2.3 Rack liquid cooling

The results concerning liquid cooling are given on Figure 3 and presented as for air cooling. The liquid chosen in the calculations is the COOLANOL 25R (MONSANTO): the conclusions would be similar if any other liquids used on aircraft were considered. The internal structures of the rack cooling plates are here optimized for air and for liquid, but different in terms of thickness (5mm for liquid and 12mm for air) and fins arrangement (compact heat exchangers). Thus, the results between the two types of coolant are similar and can be summarized as: for LRM power dissipation lower than 80 W, the benefit in using a FAST format (almost Double Europe) is about 10°C, compared to a SEM-E.

The pressure losses of the liquid network within the rack are mainly outside the cooling plates, in the distribution part of the network. The LRM format has then no influence on the pressure losses.

2.4 Liquid Flow Through Cooling for LRMs

In the case of high power dissipation, i.e. 200 W, conduction cooling is no more possible. It is then necessary to have the coolant just near the electronic devices: the solution is to use liquid cooling inside the LRM central plate, which is called Liquid Flow Through (LFT) cooling. The internal structure of the LRM central plate is of the compact heat exchanger type, in order to get a high heat transfer coefficient.

Results of numerical simulations using the FLOTHERM computer code (from FLOMERICS), show that the gradient in the components is 15 °C, in the substrate, 10 °C and between the fluid and the LRM heat sink, 5 °C. This solution presents the interest of being able to have a 85°C junction temperature for the components with a coolant at 40°C, with a relatively low pressure loss (15000 Pa). Nevertheless, this solution implies the main following constraints in the design of LRMs:

- the use of low pressure loss and dripless quick-disconnect couplings for the supply of coolant to the LRM,
- the need to absorb the volume variation of the coolant contained in the LRM when exposed to temperature changes outside the rack,
- the installation of the quick disconnect couplings and the volume variation absorbing devices in a limited space.

2.5 Conclusion on the cooling concepts

LRM cooling concepts

Conduction : for modules less than 80W (FAST format).
Liquid Flow Through : for modules from 80 to 200 W.

LRM format

The choice is the FAST format. The main reasons from a thermal point of view are:

- in conduction cooling, the FAST format allows junction temperatures 10°C lower than the SEM E: the reliability of a FAST format LRM is better;
- in conduction cooling, the pressure losses at the rack level are much lower in the case of the FAST format, reducing the consequences at the platform level;
- the consequences in terms of weight on the platform ECS are lower for the FAST format (benefit of several tens of kg - see FASTPACK Part I paper).

3. POWER DISTRIBUTION CONCEPTS

The aim of this chapter is to define the best power supply network architecture between the platform voltage at the rack input and the electronic devices voltage. Two types of platform voltages are considered: 270 Vdc and 115 Vac, fixed frequency (400 Hz) or variable frequency (around 400 Hz). They are specified in the following standards: MIL STD 704 D and Pr EN 2282. The power supply network architecture of the rack and LRMs must take into account two functions: the voltage conversion (from the platform one to the components one) and the filtering, including for alternative currents, the voltage rectifying.

The architecture can take the five following forms:

(a) CPS : for Centralized Power Supply where one power supply is placed in the rack and distributes the necessary component voltage to all the LRMs;
(b) PSM : for Power Supply Module or single stage modular architecture where one or several power supplies, being physically identical to digital function LRMs, are placed in the rack. These power supply LRMs distribute the necessary component voltage to all the other LRMs;
(c) PSM + PCM : for PSM and Power Conversion Module or double stage modular architecture where a first conversion of the platform voltage is realized by one or several PCMs, which output voltage is in the range 50 - 100 V. The latter is then distributed to PSMs which supply the digital function LRMs;
(d) PSE : for Power Supply Element or single stage distributed architecture where the platform voltage is directly delivered to digital function LRMs which have their own converters (PSE). The latter converts the platform voltage to the component one in a single conversion;
(e) PSE + PCM : for PSE and Power Conversion Module or double stage distributed architecture where, as for the double stage modular architecture, one or several PCMs are realizing the first conversion, resulting in a moderate level voltage on the backplane (personel safety). This intermediate voltage (50 - 100 V) is then directly delivered to the digital function LRMs having, each, a PSE.

Before determining the best power supply network architecture for modular avionics, it is necessary to define where are located, in the rack, filtering and rectifying (for alternative currents).

3.1 Filtering and rectifying

The conducted emissions (CE) for the power supplies are characterized by a spectrum ranging from few tens of Hz to several tens of MHz. The low frequencies are linked to the rectifying of the fixed or variable frequency 3-phase voltage, producing odd harmonics. The high frequencies are due to diodes commutation spikes of the Graetz bridge (used to rectify the alternative currents),perturbations generated by the dc-dc converters (at their switching frequencies and harmonics) and perturbations coupled to the power supply lines, by conduction, cross-talk or radiation (processor clock frequencies or data buses). It is then necessary to filter the perturbations as near as possible of their source.

It should be noticed that, first, the size of the filtering passive components are related to the square of the current passing through them and to the cut-off frequency of the filter they are

constituting (the lower the frequency is, the larger they are). Second, to let the external conducted perturbations entering the rack obliges to use large filters at each digital function LRMs. Moreover, these filters may not be installed in the defined LRM envelop.

Hence, the filtering and rectifying concept is based on the following points :

- the rectifying of the alternative currents and the filtering of the resulted low frequencies (2400 Hz for instance), as well as the external perturbations, are taken into account in a filtering and rectifying chamber, shielded, line replaceable (as a LRM) and placed directly at the rack input;
- the filtering of the high frequencies (greater than 30 MHz) is realized in each LRM.

For example, for a 200 W LRM and a single stage distributed architecture (PSE), the volume and weight for the high frequency filtering, are respectively 8 cm^3 and 20 g.

A consequence of the chosen concepts is that the voltage at the PCM, PSM, CPS or PSE input is 270 Vdc.

3.2 Power supply network architecture

The concept for filtering and rectifying being defined, the best architecture can now be determined using the following criteria: weight, volume, consumption, reliability, cost.
A software, called ACDE, has been developed to allow comparisons between the five architectures, based on these five criteria, with the technological integration, expressed in W/l, being the main input data.

3.2.1 Electrical and physical performances

As in the chapter on the cooling concepts, three examples are considered: a rack of 16 LRMs of 40 W each, a rack of 16 LRMs of 80 W each and a rack of 16 LRMs of 200 W each. In each case, the power supply function includes the energy conversion with its management and control circuits. Figure 4 shows the volume (in liter) and the weight (in kilogram) obtained for the FAST format.

Results for modules of 40 and 80 W

The results described here do not take into account the necessary redundancy to fulfil the reliability requirements: the latter is discussed in paragraph 3.2.2.

For the modules of 40 and 80 W, the best solution in terms of weight and volume is the single stage distributed architecture (PSE). Its volume is 3 times lower than a centralized architecture (CPS) and 43 % lower than a single stage modular architecture, as proposed in the PAVE PILLAR programme. The comparison on weight follows the same conclusion: 33 % less for the PSE architecture compared to PSM. Nevertheless, for the efficiency, the PSM architecture is better by about 5 %.

Results for modules of 200 W

The discrepancies between the single stage modular and distributed architectures reach 60 % in volume and 50 % in weight to the benefit of the distributed version.

In the case of a modular architecture, to deliver 3200 W (16 LRMs of 200 W), one needs 9 power supply modules (PSM): the number of digital circuit LRMs is then only 7. But these 7 LRMs do not need 3200 W but 1400. In order to be coherent, the main data is the total dissipated power of 3200 W. This choice implies that the number of LRMs may overpass 16. A comparison of the distributed and modular architectures shows that the number of LRMs is then respectively, 22 and 16: this difference indicates that to have a 16 LRM rack with a modular architecture (PSM), the technological integration effort to conduct is very important and probably too important for a year 2000 objective.

3.2.2 Reliability and cost

The reliability aspect is considered by taken into account as an input, the mission requirements of the ASAAC programme. Moreover, to have realistic calculations, the avionics system is supposed to be made of 300 LRMs distributed in 20 racks of 15 LRMs.

The mission success probability derived for the power supplies, in the case of 2 hour missions, is:

$$R = 0.99984 ,$$

with the hypothesis of 4 missions of an average of 2 hours, per day and per aircraft.

The objective being fixed, a mission success probability calculation is done for each of the 5 power supply network architectures, assuming that the probability for the digital circuits is 1. When no redundancy is considered, the conclusion is that no architecture satisfies the objective. When a (n+1) redundancy is envisaged, the 5 architectures satisfy the objective: the minimum value for the mission success probability is 0.99998. The (n+1) redundancy implies obviously consequences on the power supply network design and on the rack volume. In the case of a Centralized Power Supply (CPS), the increase in the power supply volume is 100 %. For a distributed network, the increase is 7 % (for a 15 LRM rack).

The cost aspect is considered by taken into account a very large number of power supplies: it does not include the development costs. The relative costs of each architecture (the reference being the lower cost) are:

- PSM : 1,
- PSM + PCM : 1.6,
- PSE : 1.14,
- PSE + PCM : 1.74,
- CPS : 1.1 .

The single stage distributed architecture (PSE) is higher in cost by 15 % compared to a single stage modular architecture (PSM), which is the cheapest option. The solutions with pre-regulators (PCM) imply a 50 to 60 % overcost.

- the growth capability of current solutions,
- the technological need .

This connector shall interconnect :

- electrical and optical signals: the number of pins is around 32 electrical and 24 optical (except for the optical switch module),
- power distribution: 4 pins.

The connector has to be modular to adapt the number of interconnections to the LRM families (e.g., data processing, graphic processing or memories).

The electrical pin pitch shall be compatible with automatic implementation means. Mechanically it shall be designed to reduce the insertion force while having a pin redundancy. It is characterized by a contact resistance and micro-cut-offs compatible with electronic circuit technology. It is inserted in an isolating material to have good breakdown voltage at high altitudes. It shall be issued from a basic metal and protected in order to satisfy the severe environments.

The optical points shall be protected against external pollutions and mechanical shocks when not engaged. Each optical point shall be able to interconnect mono or multimode fiber with a minimum of reflection coefficient and transmission loss. The optical transmission shall not be influenced by vibrations.

This connector shall also :

- satisfy the mechanical stresses between the LRM and the rack and be manufactured to the tolerances necessary to mount a LRM in a rack,
- be removable and pluggable without special tools, i.e. the insertion and extraction force is less than 20 daN,
- be equipped with adapted insertion/extraction devices and keying mechanisms,
- have the following make-first/break-last coupling sequence: ground contact, power supply, electrical and optical signals,
- be shielded against electromagnetic threats,
- sustain when plugged in, the hazards usually encountered in embedded electronics,
- characterized by a limited height, with tight tolerances (to fit in the LRM pitch in the rack).

Figure 12 shows a scheme of a connector with such an arrangement.

7. CONCLUSION

The present document has described the FASTPACK study, on the packaging of modular avionics, in which five systems have been developed from sensitivity analyses to design tools, for the five domains of packaging (cooling, power distribution, EMC, mechanics and interconnections). The interests of such a study are multiple :

- FASTPACK is based on a parametric approach to be linked to the physics of the phenomena, not to a specific technology (technology transparency),
- the tools developed in FASTPACK are re-usable because their application domain varies from classical technologies to future technologies,
- FASTPACK is not limited to the avionics part but takes into account the complete system (equipments/platform) or, in other words, the analyses is done from the electronic device to the platform ECS (see FASTPACK Part I paper),
- FASTPACK is following a concurrent engineering approach to cover, in parallel, all the packaging domains.

The present aim of FASTPACK is to choose a LRM format and to present packaging concepts of modular avionics in order to fulfil the ASAAC programme requirements.

LRM format

FAST format: **160 x 233 x 20 mm**. This choice is based on a synthesis of all the packaging domains with the following main reasons:

- integration of Power Supply Element on the LRM,
- cost optimization by use of mixed or dual technologies,
- rack level retrofit (direct interchangeability with ATR enclosures,
- provision for forecasted increase in power density,
- inclusion, for Liquid Flow Through LRM, of quick-disconnect couplings within the format (compatibility with Conduction Cooled LRMs),
- Finite Element Analysis indicates no detrimental effects in strong mechanical environment.

Cooling

Conduction cooling for modules up to 80 W.
Liquid Flow Through cooling for modules over 80 W.
Use of liquid cooling at rack level.

Power distribution

Single stage conversion distributed architecture for the power supply network in the rack.
Backplane voltage distribution by redundant buses.
A (n+1) redundancy allows to fulfil the required reliability.

Electromagnetic compatibility

Concept of distributed shielding against radiated modes:

- protection against rack internal fields : shielding on the LRMs ;
- protection against external threats : shielding on the rack.

Filtering of conducted modes :

- for low frequencies (< 50 MHz) : use of a filtering box at the rack input, including rectifying;
- for high frequencies (> 30 MHz) : use of local filters at each LRM level.

Interconnections

Modular electro-optical connector in order to satisfy the needs

3.3 Integration of filtering

The aim of this paragraph is to make a synthesis of the results on the filtering and on the power supply network architectures by taking as an example, the case of a rack of 16 LRMs of 200 W.

Figure 5 presents this synthesis by giving, for each architecture, the volume and weight (in absolute and relative values) of the filtering part and of the power supply part, for a 270 Vdc platform voltage. This figure shows that the complete architecture, integrating the filtering, with the lower volume and weight, is the single stage distributed architecture (PSE). If, to avoid a 270 Vdc distribution to all the modules, one wishes to add one or more pre-regulators (PCM), the 2 stage distributed architecture (PSE + PCM) is always an interesting solution because it is comparable to a single stage modular architecture (PSM), with the technical benefit of a distributed architecture. A comparison on a final result between the PSE and PSM concepts shows that the choice selected in the PAVE PILLAR programme has a higher weight, by 80 , and a higher volume, by 110 %, if the LRM powers are 200 W.

3.4 Conclusion

Electrical distribution concepts in the rack and LRMs

Single stage distributed architecture (PSE)

Each digital function LRM has its own power supply which converts the 270 Vdc coming from, after filtering and sometimes rectifying, the platform voltage to the components necessary voltage. The advantages of such an architecture are:

- lower weight and volume compared to the other types of architecture,
- a possible graceful degradation of the PSE function by a separation in 2 or more converters allowing to pursue the use of a LRM in the case of a failure of one converter,
- low backplane currents,
- a local filtering of the high frequency perturbations, on the LRMs,
- a rack of n LRMs contains n digital function LRMs,
- the input voltage of all the LRMs being identical, the PSE function permits to adapt the necessary voltages of each LRM.

LRM format

In order to integrate the PSE in the digital function LRM, the best choice for the format is FAST, compared to SEM E, when performances and costs are taken into account.

4. ELECTROMAGNETIC CONCEPTS

This chapter concerns the protection against the radiated modes and the perturbations on the cables: the conducted modes have been treated in the previous paragraph.

4.1 Radiated modes

Two types of radiated modes are considered: internal fields and external threats.

4.1.1 Protection against internal fields

The results presented here are based on measurements, on the one hand, of radiated emission (RE) and, on the other hand, of radiated susceptibility (RS) of digital circuit and power supplies.

The measured values of susceptibility are 100 mV/m in terms of electrical field (plane wave) and 100 µV at the components inputs. The shielding thickness to be placed between two LRMs is determined in such a way that the voltage at the components inputs is lower than the value of 100 µV. The table of Figure 6 shows for racks of 15, 20, 25 and 30 LRMs, with SEM E and FAST formats, the necessary aluminium weight. These weight values can be expressed as a total metallization on a shielding cover of the order of 100 µm per LRM. Thus, the LRM covers, needed also for handling purpose, can be metallic, with a thickness greater than 100 µm, or in composite materials. The metallization thickness is compatible with the use of organic composites which allow to minimize the cover weight.

4.1.2 Protection against external threats

Among the various external electromagnetic threats, two are selected to determine the necessary shielding thickness:

- the plane wave: electric field E = 200 V/m,
- the wave linked to the High Altitude Nuclear ElectroMagnetic Pulse.

On the basis of these two threats, an analytical computation gives the weight and consequently the shielding thickness. The results are presented on Figure 6 for the 200 V/m plane wave and 7, for the NEMP threat, for racks of 15, 20, 25 and 30 LRMs, with SEM E and FAST formats. The main question for the protection against external electromagnetic threats is to know if the shielding has to be placed on the rack or on every LRM, with the fundamental hypothesis that the aircraft or the helicopter is made of transparent composite structures, characterized by no electromagnetic attenuation.

For the 200 V/m wave, the results show that if the shielding is only placed on the rack, the total necessary weight is lower than 2 g. If the shielding is only placed on the LRMs, the total weight is lower than 20 g. These values are extremely low, especially compared to those for the protection of the LRMs against internal fields. This plane wave is not a sizing parameter for the radiated modes. Its influence is more on the cables between the racks.

For the NEMP wave, the results are completely different. If the shielding is only placed on the LRMs, the total weight is 6 (for 15 LRMs) to 10 (for 30 LRMs) times higher compared to a shielding only placed on the rack. That is why the optimized weight of the shieldings, given in the last column of the table, considers a shielding against external threats placed

on the rack and the shielding against internal fields placed on the LRMs. It should be noticed that the shielding placed on the rack takes into account, in the optimized weight column, the presence of the shielding on the LRMs.

4.2. Perturbations on the cables

The present chapter concerns the protection of the electronic circuits against the perturbations brought by the cables between the racks placed on the platform.

The two protection modes are :
- shielding : to protect the cables in such a way that the perturbations are lower than the equipments susceptibility level,
- filtering : to use cables strictly needed for signal transmission and to filter the perturbations at the equipments input.

The recommendations relative to the cables are:
(a) the use of pig tails at the cable-rack interface makes impossible to fulfil the requirement of component susceptibility level (100 µV), for all types of threats ;
(b) the lightning and NEMP threats are much more critical than the 200 V/m plane wave. They must be treated by extremely heavy shieldings in the cases where the electronic equipements have to keep on running. Filtering is, for these cases, impossible because it would imply filter cut-off frequencies not compatible with the bandwidth necessary to transmit the signals. In the cases where only a non destruction of the equipments is expected, the protection against NEMP and lightning has to be done by clamping systems ;
(c) the 200 V/m plane wave can be handled by filtering or shielding of the cables. The filtering solution is less heavy than shielding. Nevertheless, it can only be applied if the bandwith of the signals to transmit does not exceed a certain value. In the case where the platform brings an attenuation of the order of 20 dB, this frequency is 15 MHz. In the case where the platform does not guarantee any attenuation (transparent composite structures), this frequency is 4 MHz. Above these frequencies, the only possible solution is cable shielding, with a weight penalty.

4.3 Conclusion on EMC concepts

The main conclusion for the protection against radiated electromagnetic modes is that, for a finite volume of electronics, the best solution in terms of weight is to shield a single volume rather than n smaller volumes.

Concept of protection against radiated electromagnetic fields

The concept is based on a **distributed shielding**.
Protection against internal fields: shielding on the LRMs.
Protection against external threats: shielding on the rack.

5. MECHANICAL CONCEPTS

The objectives are to define, by the use of numerical simulations:
- the dynamic behaviour of the rack,
- the transfer functions from the LRM to the platform,
- optimized weight and volume based on the different configurations.

5.1 General approach

From the platform to the components, three different mechanical level are considered:
- from the platform to the rack,
- from the rack to the module,
- from the module to the electronic components.

The criteria for the validation of a defined configuration, from the structural point of view , is the level of acceleration seen by the components (for example, 100 g can be considered as a maximum value for typical component assembly).

Six families of parameters are selected to cover all the configurations:
- input specifications (platform levels),
- rack external interfaces (location and number of attachment points, dampers),
- definition of the rack (LRM format, walls thicknesses),
- material properties (stiffness, density, damping),
- number of modules (size of the rack),
- LRM contribution (weight, resonant frequency).

The rack response is defined by its acceleration transfer function which links the levels applied to the rack (platform level) to the levels induced on the module interfaces. The impact of all the previously defined parameters on the dynamic response of the rack is evaluated in terms of predominant frequency and transmissibility. Taking into account the number of parameters (14 at least), it is almost impossible to analyse all the possibilities. The preferred approach is to define a reference configuration and to study the influence of each parameter operating separatly (sensibility analysis), on:
- resonance frequency variation (dF/F),
- transmissibility variation (dQ/Q),
- weight (dM/M) and volume (dV/V) variations.

Combining this different effects allows to answer the question "what will happen if" (for example : if the thickness of the wall is doubled). The same approach used on the LRM level allows to get the whole chain from platform to components (see Figure 8).

5.2 Rack simulation

5.2.1 Reference configuration

This reference configuration is:
- 25 FAST format LRMs (600 g, Fr = 200 Hz),
- 4 attachment points (2 front bottom - 2 rear up),
- no suspension,
- aluminium rack (weight = 4.4 kg, walls = 2mm),
- dimensions : 394 x 262 x 183 mm.

5.2.2 Reference behaviour

X Axis : 196 Hz (modules) - 1460 Hz (rack)
Y Axis : 480 Hz . Z Axis : 345 Hz

5.2.3 Parametric results

A - Rack external interface : attachment point location
Four positions have been considered, the highest frequency one being the reference (see Figure 9).
B - Rack external interface : number of attachment points
The results, on the main axis, show a limit reached after one intermediate added point.
C - Impact of LRMs size on the rack
The result is about 10 % of predominant frequency increase in the main direction for a SEM-E size rack (see Figure 10).
D - Wall thickness
The predominant frequency is proportional to the wall thickness in the main direction.
E - Impact of the material properties
For a Young modulus of 150 GPa, the resonance frequency is out of the range of specifications (> 2000 Hz) for the main direction. The density of the walls, the Young modulus of the cold-walls and damping ratio have also been analysed.
F - LRM number
The number of LRM has a direct impact on the rack length. The frequency decreases if the number of LRM increases.
G - LRM contribution
Depending on the selected technology and materials, the LRMs will have different dynamic response and by consequence, a different impact on the rack.
To take into account the effects of the LRMs on the rack, the finite element sub-structuring technique is used and the different LRM configurations (see para.5.3), integrated in the reference rack.

5.2.4 Conclusion on the rack simulation

The rack level is the first step to analyse the complete chain from the platform to the components. The impact of the variation of one parameter can be foreseen and also the combined effect of different independant ones.

5.3 LRM simulation

In order to make an evaluation of the interferences between the rack and the LRM in a modular avionics structure, the dynamic mechanical behaviour of a LRM is analyzed by using a finite element method with results applicable to the components.

5.3.1 LRM modelisation

The mechanical behaviour of a LRM is obtained by numerical simulations based on the following parameters :

- LRM format (FAST, SEM-E),
- heat sink type and thickness,
- material type,
- number of stiffener,
- heat sink-substrate adhesive (shearing stiffness),
- connector attachment point number,
- components size,
- thermal clamps equivalent stiffness.

5.3.2 Simulation

(a) Reference congiguration

As for the rack, a reference case is defined:

- FAST format with aluminium heat sink of 1mm,
- FR4 substrate (thickness 1,6mm x 2),
- no stiffener, connector with two attachment points and rigid thermal clamps,
- small components,
- weight of 600g.

This simulation points out that the LRM first vibration mode is a tile like bending mode, with a maximum displacement on the smallest side, opposite to the connector. The resonance frequency associated to this first deformation mode is around 300Hz and the associated Q-factor is around 25.

With the following vibration levels applied to the clamps:

- sine vibrations : +/- 8 g peak,
- random vibrations : PSD = 0.03 g^2 / Hz - frequency range: 10 - 2000Hz,

the results show a 0-peak displacement less than 0.6 mm (for the sine) and 0,2 mm (3 sigma, for the random).

(b) Other simulation cases

Figure 11 presents the results obtained when some parameters values are modified from the reference case. The main conclusion concerns the LRM format: because the predominant mode is a tile like one, the difference between the FAST and the SEM E formats is not very important, especially when compared to the influence of the substrate-heat sink adhesive characteristics or of the clamping mechanisms.

5.3.3 Conclusion

The results show that the dynamic behaviour of the module fulfil the usual levels of vibrations.
Nevertheless, additional attachment points are required in the case of great components and the motion of the LRM covers have to be limited. The study points out that the LRM mechanical behaviour is not a dimensioning point. The main parameter is the global stiffness linked to the heat sink-adhesive-substrate assembly. This parameter is more and more important if the substrate is rigid (e.g., alumina), or if the heat sink is thick or if the bonding is rigid.
The use of stiffeners is a good solution but brings an overhead of weight. The other parameters,such as the LRM format, are not considered as fundamental.

6. INTERCONNECTION

In order to define the LRM connector, the study takes into account different aspects :

- the functional requirements,
- the environmental requirements,
- the technical parameters of a connector,

of each LRM family. The typical configuration of such a connector is :

- 24 optical contacts,
- 32 electrical pins,
- 4 power pins.

For Liquid Flow Through (LFT) modules, quick-disconnect couplings are added on both sides of the electro-optical connector.

ACKNOWLEDGEMENTS

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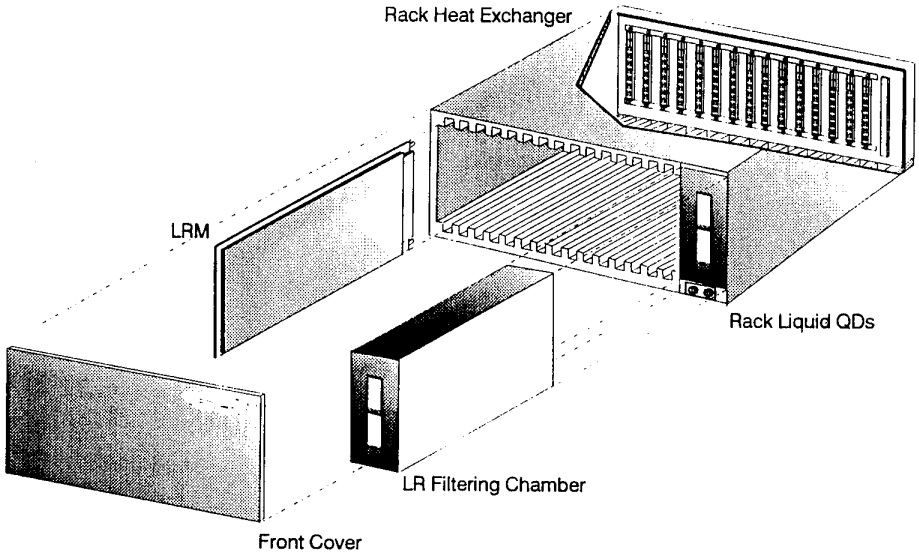


Figure 1 : Rack and LRMs for future modular avionics

LRM power and air flowrate	FAST format *40 W - 64 g/s*	SEM E format *40 W - 64 g/s*	FAST format *80 W - 128 g/s*	SEM E format *80 W - 128 g/s*
Gradient in : (°C)				
Component	5	5	5	5
LRM	32	38	50	57
Rack	15	17	19	21
For a maximum junction temperature of **85 °C**, the fluid temperature at the rack inlet is (steady state):				
Pressure loss (Pa)	**33** 330	**25** 550	**11** 715	**2** 1150

Figure 2 : Temperature gradients in the components, LRM and rack and coolant temperature
Air cooled rack
Rack of 16 LRMs with power dissipation on components of 1 cm^2 (on each LRM)

	FAST format *40 W - 35 g/s*	FAST format *80 W - 70g/s*	SEM E format *40 W - 35 g/s*	SEM E format *80 W - 70g/s*
For a maximum junction temperature of **85 °C**, the fluid temperature at the rack inlet is (steady state):				
Coolant Temperature (°C)	**35**	**13**	**27**	**4**
Pressure loss (Pa)	9700	15400	9800	15700

Figure 3 : Temperature gradients in the components, LRM and rack and coolant temperature
COOLANOL cooled rack
16 LRMs with components of 1 cm^2 on 3 mm thick heat sink

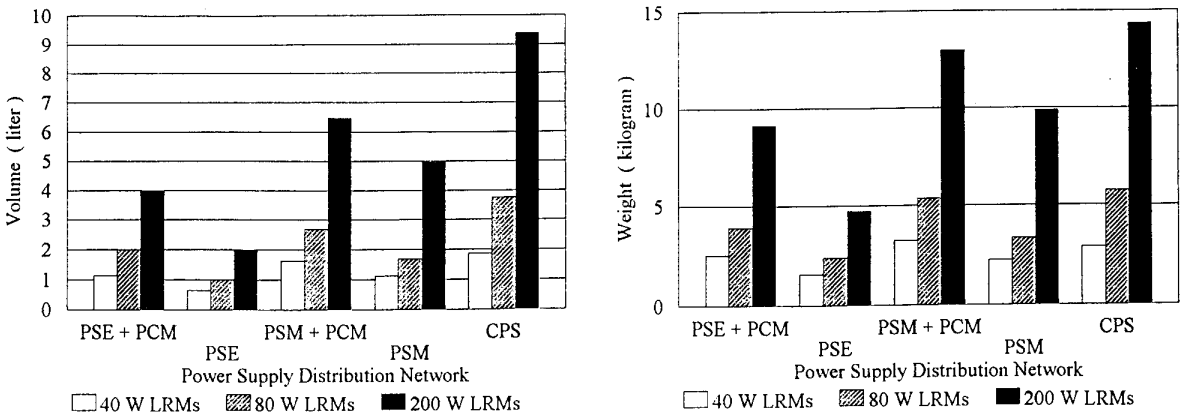


Figure 4 : Comparison of the 5 Power Supply Distribution Network (PSDN) Architecture
Rack of 16 LRMs

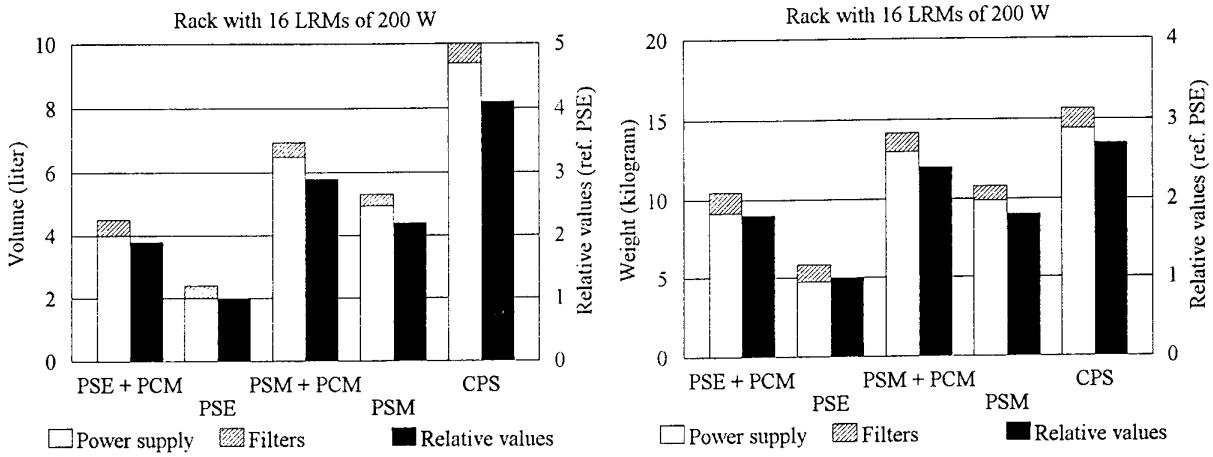


Figure 5 : Comparison of the 5 PSDN Architecture including the filtering function

Rack type	Number of LRM	200 V/m			
		LRM/LRM (1)	→ rack (2)	→ LRM (3)	weight (4)
FAST	15	930	1.4	8.5	930
	20	1240	1.5	11	1240
	25	1550	1.7	14.5	1550
	30	1860	1.9	18.4	1860
SEM E	15	630	1.2	7.3	630
	20	840	1.3	9.6	840
	25	1050	1.5	12.9	1050
	30	1250	1.7	16.5	1250

(1) necessary weight to shield LRM to LRM perturbations (grams)
(2) necessary weight to shield against external threat, when shielding is on the rack (grams)
(3) necessary weight to shield against external threat, when shielding is on the LRMs (grams)
(4) total weight for the best shielding distribution (grams)

Figure 6 : Shielding weight for protection against internal electromagnetic interferences and the 200 V/m plane wave threat

Rack type	Number of LRM	Nuclear EleectroMagnetic Pulse					
		LRM /LRM (1)	Rack (2)	LRM (3)	Optimized weight distribution		
					Rack	LRM	Total
FAST	15	930	346	2104	261	930	1191
	20	1240	427	3146	323	1240	1563
	25	1550	509	4352	384	1550	1934
	30	1860	590	5696	445	1860	2305
SEM E	15	630	259	1575	196	630	826
	20	840	323	2380	244	840	1084
	25	1050	388	3317	293	1050	1343
	30	1250	452	4364	341	1260	1601

Legend for (1) , (2) and (3) : see Figure 6

Figure 7 : Shielding weight for protection against internal electromagnetic interferences and the Nuclear ElectroMagnetic Pulse threat

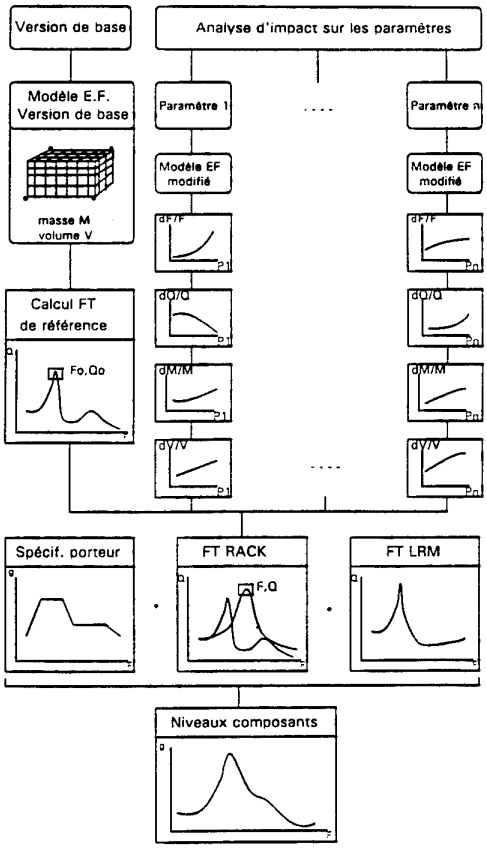


Figure 8 : Mechanical analysis procedure

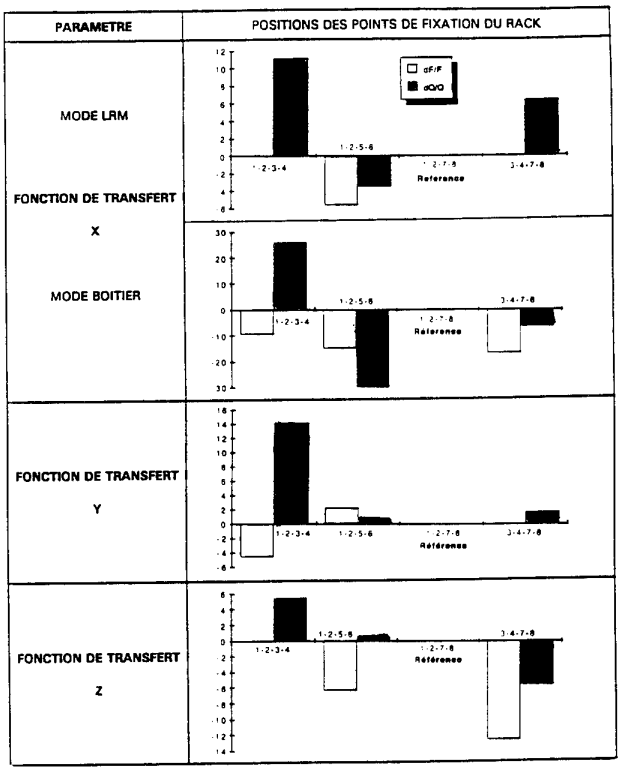


Figure 9 : Attachment point location influence on the Rack mechanical behaviour

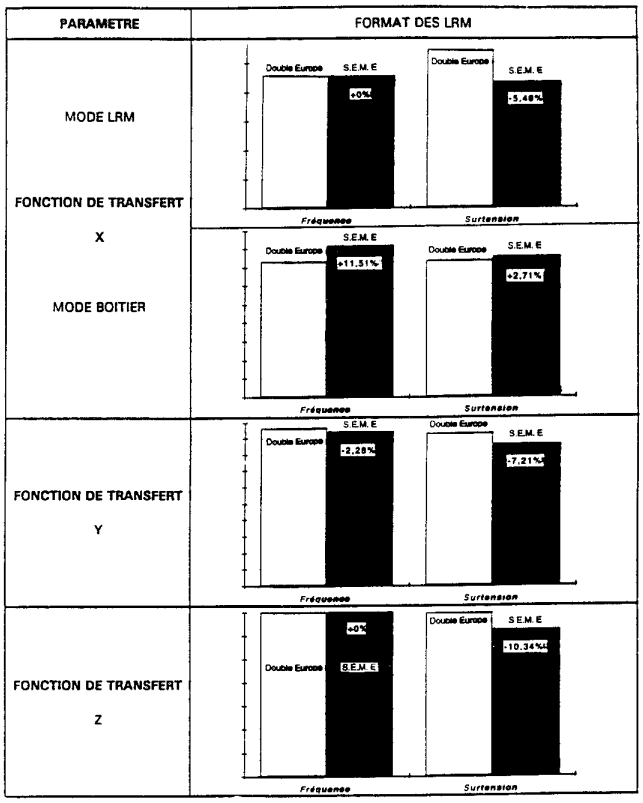


Figure 10 : LRM format influence on the (Rack + LRM) mechanical behaviour

Parameter	New value	F / F0	Q / Q0	RMS / RMS0
Format	FAST --> SEM E	[1.12 , 1.17]	1.15	[0.83 , 0.90]
Heat sink	1 mm --> 3 mm	1.6	1.15	0.45
Heat sink	Conduction --> LFT	1.05	1.15	1
Substrate	1.6 mm FR4 --> 1 mm alumi	2.2	1.1	0.35
Adhesive	Semi-hard --> soft	0.45	0.6	[2 , 3]
Stiffeners	0 --> 3	1.25	1	0.60
Connector	2 fixation points --> 3 points	1	1.13	1.05
Components	15 x 15 mm --> 50 x 50 mm	1.33	1	0.6
Thermal clamps	hard --> "soft"	[0.35 , 0.55]	0.7	[3 , 5]

Figure 11 : Influence of parameter changes on the LRM mechanical behaviour
F = resonance frequency - Q = transmissibility factor - RMS = displacement rms value

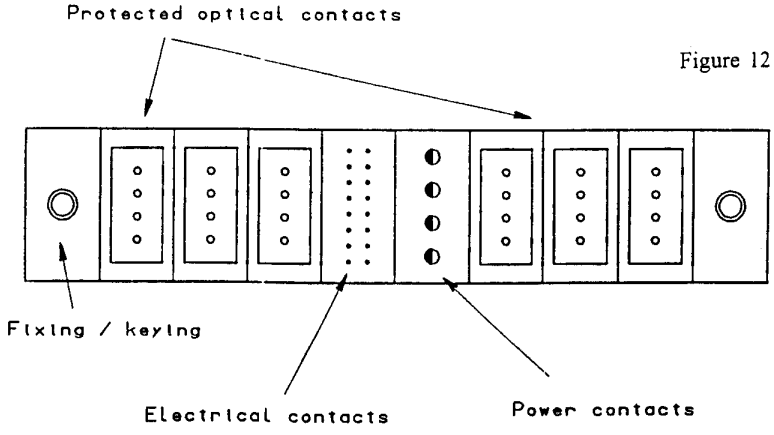


Figure 12 : Typical connector arrangement

DISCUSSION

Question: In what way to you handle the RF-input/output signals?

Answer: The connector is of modular type, i.e., it is constituted of different elements including photonic element (with 2 or 4 optical points), electrical points element (with 8 or 16? pins) and power elements. It is then possible to have an RF element with conventional technologies. It *will* also be possible to use photonics in the field of RF signals (but, please, wait some years!)

In the FASTPACK study, we focused mainly on digital equipments. This explains why the possible RF element has not been included.

Next meeting. . .

Question: Was air-flow-through considered for study comparison?

Answer: Only at the beginning. We stopped because for high power modules, LFT allows thinner heat exchanges and lower pressure losses. The last point was (and is) a major concern when the platform aspects (ECS) are considered.

Question: What aircraft platforms were used to define the environment baseline both operational and performance?

Answer: A Multi Role Fighter aircraft and a combat helicopter. Some additional data were taken from transport and utility, and maritime (or seat) patrol, aircraft and helicopters.

The Advanced Avionics Subsystem Technology Demonstration Program

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Abstract

The Navy's Advanced Avionics Subsystem Technology (AAST) Fault Tolerant program is clarifying the Navy's fault tolerant avionics specifications methods and acceptance tests. The goal of the program will be clarify the Specification and Statement of Work language needed in future procurements and to demonstrate fault tolerant validation tools on an avionics design. A set of tool features will then be developed that spans the needs of fault tolerant computer system design from early concept studies to full scale production and operational support, both hardware and software. The paper will give an overview of the AAST Fault Tolerant Demonstration and focus on two tools that are being used in the demonstration: FERRARI - a software fault injector that will be used to validate the fault tolerance of the Common Integrated Processor (CIP), the F-22 Mission Processor and GRIND a concept evaluation tool that will be used to evaluate the overall CIP architecture.

Index Terms: Avionics, Fault tolerance, Fault injection, error injection.

1 Introduction

The DoD is entering a radically new era of systems procurement. The Cold War is over and new scenarios and radical force structure changes are changing the requirements of the next generation of weapon systems. Other factors in the "new world order" of weapon system procurement are: budgets are decreasing, development cycles are being stretched out, prototypes and demonstrations are being emphasized, open systems standards will dominate, and the next generation of systems will be intensively modeled and simulated before any hardware is built. Future complex weapon systems will increasingly rely on digital systems and the dependability of these digital components will play a critical role in the effectiveness of those systems in the field.

The key issue that the AAST Fault Tolerant Demonstration is addressing in this new era of defense procurement is - how can the Navy manage and procure dependable and cost effective, computer-based weapon systems? The demonstration program will investigate the timely and practical application of fault tolerant technology early in the design cycle before major resources are committed to a particular design. This application of fault tolerant technology will be balanced against the extreme time pressures of modern avionics system development.

2 The Advanced Avionics Subsystem Technology Fault Tolerant Demonstration

Funds for the research, development, transition and insertion of new technologies into the fleet are divided into 6.1, 6.2, 6.3A and 6.4 funds. The 6.1 and 6.2 funds are focused on exploring the feasibility of new technologies. The 6.3A funds are aimed at demonstrating those technologies so that program offices can specify them with confidence. In 1990, ONR's 6.1 research started the Ultradependable Multicomputers and Electronic Systems Research Initiative. This research initiative addresses a wide ranging number of fault tolerance topics including measurement and modeling of expected system fault modes, fault injection, simulation and modeling techniques, software fault tolerance approaches, as well as compiler, algorithm and hardware-based fault-tolerance techniques. ONT's 6.2 exploratory development, computer block has an effort called the "Engineering of Complex Systems Technology" whose aim is to explore the entire design and development of advanced real-time systems. The fault tolerance portion of the block plan is aimed at integrating fault tolerance into the design process of complex systems. The Advanced Avionics Subsystem Technology (AAST) Fault Tolerance Demonstration is a 6.3A project that takes the 6.2 Engineering of Complex Systems effort the next step and demonstrates the fault tolerance metrics and acceptance tests at each stage of an evolving contractor's design. The AAST work will also transition some

of the ONR 6.1 developed tools (fault injection, fault tolerance benchmarks and fault tolerance simulation techniques). The goal of the AAST Fault Tolerance Demonstration is to demonstrate the necessary and sufficient dependability metrics and validation techniques of a fault tolerant system. These requirements will be documented so that program offices can use them in their specifications and SOW packages according to their various fault tolerance and dependability needs.

3 Language and Fault Injection Tools

The two key thrusts of the AAST Fault Tolerance Demonstration program are: what legal language needs to be in the Statement of Work (SOW) and Specification to clarify to the contractor the exact fault tolerant and dependability requirements that the government expects to see in the system? And what tools and fault injection techniques are needed to validate that language?

Legal, formal, requirements are the only way the government can define computer performance and dependability requirements. More precise fault tolerant requirements would specify the system's fault containment regions, the specific faults the system will guard against, and the types of analysis and fault injection testing that shall be done at each stage of the system design.

The SOW is the requirements for the contractor design team to fulfill at each stage of the system design. Generally, the SOW should require that the error handling features of the system shall be validated at each stage of the systems evolution. The validation should be a functional fault analysis which will map the specified fault set onto each identified fault containment region and then identify the fault detection, isolation, removal and recovery mechanisms of the system that will enable the system to maintain the mission services in the presence of faults. This validation should be demonstrated with fault injection techniques on the current simulation or breadboard of the evolving design.

This precise legal language, dealing with dependability and fault tolerance, should include clear and quantifiable validation techniques to be performed at each stage of the system's design that will allow Navy to be informed customers able to quantify a design's dependability and reasonably ensure that the evolving system will be a dependable system for the Navy to own and operate. Thus, the Navy needs to support the development of fault tolerant validation tools. The following two sections describe two of the tools to be used in the laboratory demonstration of the AAST Fault Tolerant program.

4 Fault Injection Tools Supporting the AAST Fault Tolerant Demonstration

The two two tools that are used in supporting the AAST Fault Tolerant Demonstration. The first is DEPEND, which is a simulation environment tool that is used in the design phase of a system before an actual hardware has been built. The second is FERRARI, which is a fault and error injection tool that injects errors into a prototype of a system to measure its ability to detect, locate and recover from errors while it is executing real application.

5 DEPEND/GRIND Overview

Commercial systems for air, ground, and space applications require innovative solutions to dependability problems. To meet these needs, we have developed a highly instrumented, simulation-based CAD environment, called DEPEND, which allows designers to study a system in detail. The CAD tool provides an object-oriented framework that allows the evaluation of highly dependable systems. The tool provides facilities to rapidly model components typically found in fault-tolerant systems. It provides an extensive, automated fault injection facility which can simulate realistic fault scenarios. For example, the tool can inject correlated and latent errors, and it can vary the injection rate based on the workload on the system. In addition, it provides several key features that are necessary for fault simulation:

1. It provides ways to signal a change in the status of the components due to a failure, so that remedial actions can be simulated.

2. It provides mechanisms to halt on-going processes due to faults/errors/failures. This is an extremely needed feature for fault simulations. It is also useful for incorporating importance sampling methods.

3. It has the capability to model the inter-component dependencies under fault conditions. For example, a failed server may not be able to initiate re-integration without control from a healthy control server. Such dependencies can be easily modeled with DEPEND.

4. It provides several automatic fault statistics collection facilities that can provide measures such as MTTF and availability. They can also provide a detailed list of every fault injected, repair action attempted and their status.

DEPEND is a powerful tool capable of modeling complex systems, but using it may be difficult for those who are new to the tool or who are unfamiliar with C++. Though the object library reduces the amount of programming that the user has to perform, models often turn out to be hundreds of lines of code. GRIND, a GRaphical INterface for DEPEND, provides an alternative to coding C++ directly. GRIND

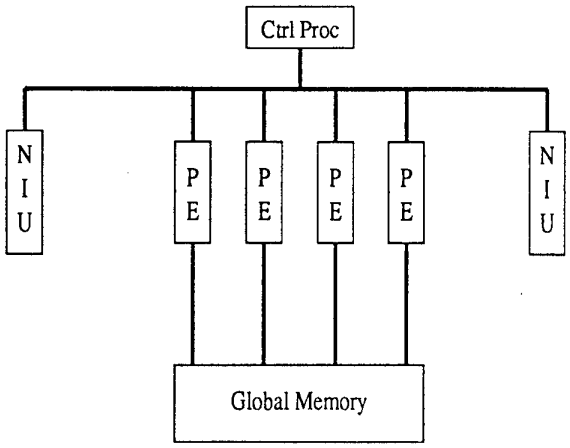


Figure 1: Common Integrated Processor block diagram.

is a menu-driven X-Windows application which facilitates the creation of DEPEND models. With this interface, one is able to visualize the architecture of the system being modeled and how it functions. Hardware components are represented using icons while the software aspects of the system are specified using a graphical flow-chart representation. Development of models can also be performed quicker because GRIND's menu structure presents most of DEPEND's features to the user so that less time is spent referring to the manual and debugging typos. While a graphical interface provides a quicker and more intuitive way of entering models, much of DEPEND's power can not be harnessed graphically, which means that direct C++ coding must be used to create especially complex models. However, since GRIND's output is a file containing a well-formatted C++ program, one can speed up the creation of a complex model by first using GRIND to create a simpler, more abstract model, and then extending it by jumping directly into the C++ code generated by GRIND.

5.1 Example Application

As an example application of GRIND, this section will present a model of a system similar to a processing module found in Hughes Common Integrated Processor (CIP). The system is a fault-tolerant element consisting of four processing elements (PEs), two redundant network interfaces (NIs), a global memory (GM), and a control processor (CP).

Refer to Figure 1. Either NI can be used by any of the PEs in order to send data to or get data from the outside world. We will assume that one NI has sufficient bandwidth to support the system, so that if one fails the system can continue to function. The CP is responsible for distributing tasks among the four PEs which communicate with each other using the GM. The reason for having multiple processing elements is for fault-tolerance as well as for increasing computing power. Let's say that three of the four processors are needed to maintain the minimum throughput requirements. Since tasks are likely to be running on a PE when it fails, the process of reconfiguring to use only three PEs is likely to be complex and itself prone to failure. Thus, the model will include a reconfiguration coverage for the processing elements. Given the failure rates of each of the subcomponents, an interesting analysis would be to see how sensitive the reliability of the module as a whole is to this reconfiguration coverage. This would give engineers an idea of how much effort needs to be invested in designing a robust reconfiguration process.

Constructing this model using GRIND was a straightforward process. The first step was to create a derived class for each of the different types of subcomponents in the model. GRIND allows the user to create derived objects from the classes within the DEPEND object library so that more specialized functionality can be added to the default objects. Once a derived class is created, one can create variables and methods for that class in addition to those inherited from the parent class. In this example model, a `PE` class was derived from the `FT_kofn` object. Because `FT_kofn` is the parent of `PE`, `PE` inherits all of `FT_kofn`'s functionality making it able to model the processing-element k-out-of-n system. Similarly, a `GM` class was derived from a `FT_memory` object, as well as a `CP` class from a `FT_server2` object and a `NI` class from a `FT_link2` object. Since no workload (such as processor utilization, message passing, memory access, etc.) is incorporated into this model, there was no need to further specialize the derived classes. The derived classes were added here to demonstrate that this model can be readily extended within the GRIND environment.

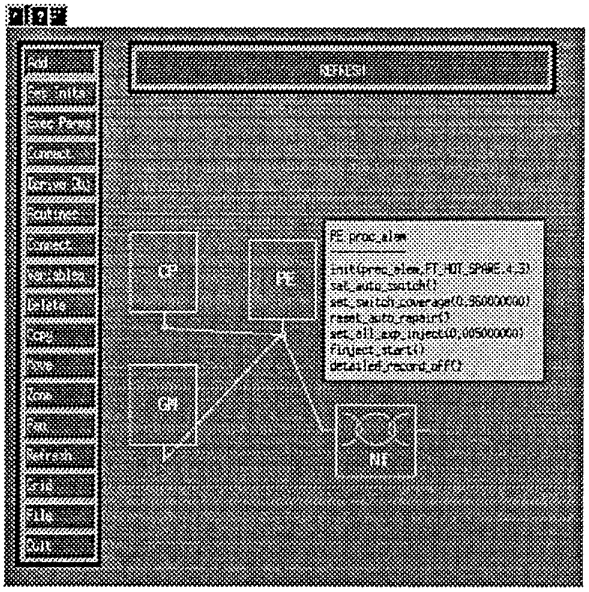


Figure 2: GRIND hardware display showing the initializations methods for the processing elements.

Once the derived classes were established and objects from these classes where added to the model.

the initialization methods of these objects were set through the *Set Inits* menu. Through this menu, the fault injection rates were set as well as some of the configuration parameters. Through these 'configuration parameters', we specified that the `proc_elem` object was to be 3-out-of-4 system with a 96% reconfiguration coverage and the `net_interface` object was to have one spare.

See Figure 2 for a GRIND display showing the objects of the model and a listing of the initialization methods of `proc_elem`, an object of the class `PE`. The GRIND environment also allowed us to specify that the executable was to run the simulation one thousand times, outputting the time-to-failure after each run. With this information, GRIND was able to create a C++ program which could be compiled and then run. The output of the executable is simply a listing of one thousand times to failure; so with the aid of a standard statistical analysis package, one could generate a curve estimating the reliability of the system. The parameter for the reconfiguration coverage can easily be changed within GRIND so that multiple scenarios may be simulated and a sensitivity analysis can be performed.

The next tool that will be discussed is FERRARI.

6 Design and Implementation of FERRARI For the Hughes Common Intergrated Processor (CIP) Module

Fault and error injection has been recognized as a powerful technique which allows the evaluation of a prototype system under faults, in particular, the measurement of the effectiveness of its error detection and correction capabilities. Another advantage of this technique is that the effects of faults in the system can be studied when it is executing realistic programs.

Hardware and software techniques have been proposed for fault injection. The motivation behind our work was the development of a a flexible and an automated fault and error injection system. We concluded that hardware fault injection would be cumbersome and would not allow us to inject faults and errors inside chips, for example, change a bit or bits in an internal register of a processor. On the other hand, it was clear that simulation would be too time consuming. Our approach, therefore, is to emulate hardware faults and errors through software, by corrupting the program execution state while it is executing, so that the behavior of the system would be the same as if the internal fault had been present.

Our studies showed that the behavior of a system varies with the type of faults and errors injected. (This is described in more detail in Section 8.) We also wanted the ability to inject faults while executing a variety of applications or system functions. The injection techniques described in this paper provide the necessary flexibility.

These techniques have been incorporated into FERRARI a Fault and ERRor Automatic Real-time Injector. The main contributions of FERRARI are its ability to inject transient errors as well as permanent faults so that it can be used to test the effectiveness of concurrent error detection and correction mechanisms, and its capability to perform the injection on object code. The current version of FERRARI is implemented to emulate a large number of faults and errors in the CPU circuitry, in memory, and in peripheral drivers.[1] Hardware faults as well as control flow errors (including bus errors, memory errors and processor control line errors) are emulated through software. FERRARI allows control over the time, location, type and duration of the fault or error. It can measure coverage and latency (in instruction cycles or microseconds) and is able to locate the source of a detected error or one which caused failure. It is able to automatically control a large number of experimental runs.

The current version of the CIP module was not built to be fault tolerant. Our aim in injecting fault to this module is not to evaluate its dependability properties but rather to test the capability of FERRARI to inject faults and errors on the hardware prototype. This will give us the ability to add new features to FERRARI that will be used on future versions of the CIP module which are build to be fault tolerant.

Figure 3 depicts the hardware configuration of the fault and error injection process. In this figure, a microvax workstation is connected to the CIP through the high speed data link. The microvax is configured as the host machine where the fault and error tool is executing.

The CIP contains the general purpose processing elements (GPPE's), the special signal processing elements (SPE's), and the global memory. The GPPE's execute the ADA applications while the SPE's execute the signal processing applications. Communication between the GPPE's and the SPE's is attained through the global memory shown in Figure 3. Each GPPE's has its own local memory which contains the program that is running on that GPPE and the data needed for the successful execution of the program. The "interface module" is a special purpose hardware that controls the communication between the microvax and the CIP module.

As mentioned earlier, the fault and error injection tool (FERRARI) is executing on the host microvax workstation which is running the vms operating system. The procedure for injecting errors into the CIP module is depicted in Figure 4. The "user console" is a program that can access the low level functionality of each component residing on the CIP module. It can insert software breakpoints, access any of the internal registers for any of the GPPE's, and read/write into the local memory of the GPPE's. FERRARI can inject fault and ERRORS in the CIP modules by sending a sequence of commands to the "user console" program that is running concurrently with FERRARI. This communication is attained through the use of mailboxes [2]. After receiving the sequence of commands from FERRARI, the "user console" pro-

[1] More rigorous studies to obtain the actual high level fault/error models of a particular processor should be conducted prior to using FERRARI. An example is the study undertaken in [5] where a technique for mapping real hardware failures to high level error models is presented.

[2] Mailboxes are used to send streams of data from one process to another.

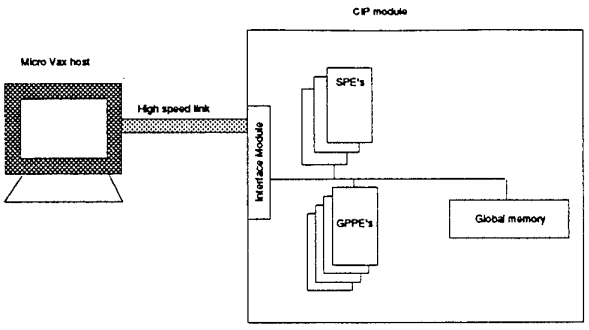


Figure 3: Hardware configuration of error injection on the CIP module

gram executes this sequence one command at a time by sending the command through the high speed link to the CIP module as shown in Figure 4. The operating system running on the CIP module will interrupt and modify the running application accordingly.

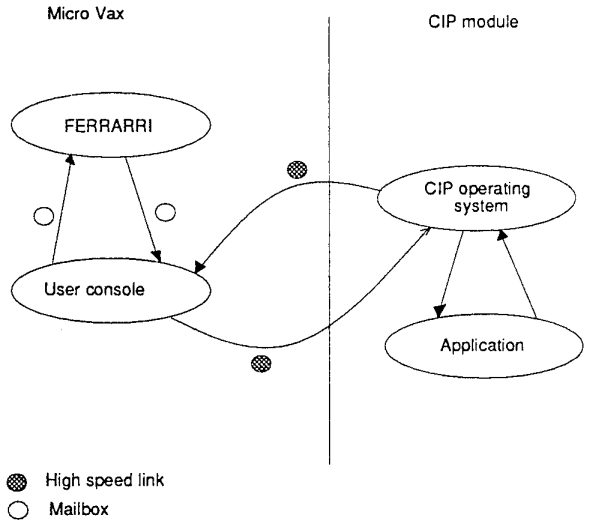


Figure 4: Procedure of error injection on the CIP module

At the end of the fault injection experiment, the CIP module operating system will send error messages through the high speed link to the "user console" program running on the microvax workstation which, in turn, transfer these messages to FERRARI. This error message contains information that describes the execution state of the application running on the CIP module when the error was injected. FERRARI uses this information to evaluate the final coverage of the system.

6.1 Initialization and Activation Module

This module prepares the test program[3] for fault and error injection. The tasks of this module are: 1) it parses the test program executable file to determine the starting address location and size of the text and data segments of the file, and 2) it extracts the execution behavior of an error free run of the test program. Extracted information includes the output of the program, referred to later as *reference*, execution time, and the address space traversed during program execution.

6.2 User Information Module

This module obtains experiment parameters supplied by the user which include: 1) the type of the dependability measurement (coverage vs. latency), 2) the duration of the fault/error (transient error vs. permanent fault), 3) the mode of the experiment which selects between user vs. random selection of the address bit position and time instance at which the fault/error is injected, 4) the fault/error type which selects one of the five types supported by FERRARI (these are XORing a bit with logic "1", resetting a bit, setting a bit, resetting a byte, and setting a byte), 5) the fault and error model (explained in the next subsection), 6) the method of fault/error injection (also explained in the next subsection).

6.3 Fault and Error Injection Module

FERRARI supports the injection of both permanent faults and transient errors. The mechanisms for fault and error injection are identical, and the only difference is the duration of the injected fault and error. For transient error injection, the duration is defined to be one instruction cycle. On the other hand, the duration of permanent faults may be several instruction cycles, or may span the entire execution interval of the application.

One of the design features of FERRARI is its capability to inject a variety of fault/error models. This feature was established when we observed the target system responding differently when different error models were injected in the system. (An example of this behavior is shown in Figure 13.) In addition, the design of FERRARI allows the inclusion of other models to its set of fault/error models.

A detailed discussion of the mechanism of some of the transient errors and permanent faults that are injected through FERRARI follows in the next two subsections.

6.3.1 Transient Errors

FERRARI supports three methods of transient fault/error injection, Memory Corruption, Spatial and Temporal. In the "Memory Corruption" method, a fault is injected in the task memory image before program execution starts. In the "Spatial" method, the

[3] We refer to the program whose code is mutated by FERRARI during the course of the fault/error injection process as the "test program".

fault/error injection is triggered after N occurrences of a randomly selected address line. The value of N is defined by the user. Once the program uses the erroneous value, the error is removed. Finally, in the "Temporal" method, the execution of an application is interrupted at a randomly selected instant of time and the value of the next element fetched or stored into memory is modified. An experiment to compare the three different methods will be presented later in Section 8.

Table 1: Selected Transient Error Models

	Model	Description
1	AddIF	address line error resulting in executing a different instruction
2	AddIF2	address line error resulting in executing two instructions
3	AddOF	address line error when a data operand is fetched
4	AddOS	address line error when an operand is stored
5	DataIF	data line error when an opcode is fetched
6	DataOF	data line error when an operand is loaded
7	DataOS	data line error when an operand is stored
8	CndCR	errors in condition code flags

Some of the transient errors supported by FERRARI are presented in Table 1 and are emulated as follows. When the execution reaches a specified address, the program is trapped. A selected error is injected and the current instruction is executed. The injected error is then removed and the program is allowed to resume execution. The reason for this procedure is to avoid injecting the error more than once if the selected address was in a loop. Of course, if the single execution of the instruction under the error resulted in a change of internal state, this erroneous state would remain, and may cause other execution errors subsequently. This section will present the mechanism for injecting two of the error models presented in Table 1, the AddIF and the AddOF. The mechanisms for injecting the other error models in Table 1 were presented in [1].

- Address line error while the processor is fetching an instruction

  Figure 5 illustrates the mechanism to inject this error. The processor is interrupted when it reaches the selected address to be modified. The next instruction to be executed is fetched from the address pointed to by the current program counter having one of its bits (bytes) modified. After the execution of the wrong instruction, the program is trapped on the following instruction. The previous program counter value is restored before the program is allowed to proceed.

- Address line error when the program is fetching an operand

  When execution reaches the address where the error is to be injected, the program is trapped (Figure 6). In SPARC machines, for example, only *load* and *store* instructions access memory.

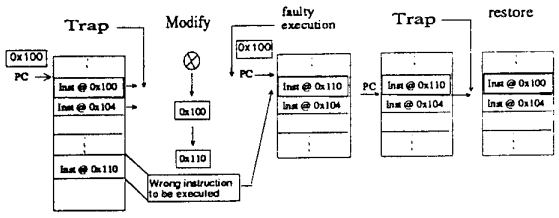


Figure 5: Address line error when an instruction is fetched

All the other instructions use registers as their source and destination operands. The load and store instructions use registers to access memory. The effective address of the operand, for the selected load/store instruction, is modified. After the execution of the faulty instruction, the program is trapped again to restore the content of the previous program counter.

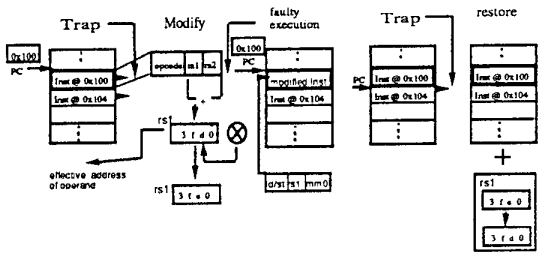


Figure 6: Transient address line error when an operand is fetched

In addition to the error models listed in Table 1, FERRARI allows the user to mutate the contents of an internal register. In addition, the user may select a combination of some of the transient errors in the Table 1. For example, it was found in [5] that a significant percentage of the injected faults inside a sample processor are manifested as "address and data line errors while fetching an operand".

6.3.2 Permanent Faults

Permanent faults supported by FERRARI are: 1) address line fault; 2) data line fault; 3) fault in condition code flags. These faults are emulated as follows:

- Address line fault

  When the program execution reaches the address of the selected instruction, a bit/byte in the program counter is modified. The instruction at the modified address is executed. If the executed instruction is a branch instruction, the value of the program counter becomes the target address of the branch instruction, otherwise its value is the previous program counter, before fault injection, incremented by four. Figure 7. This procedure is

repeated N times where N is a number that determines the duration of the fault in instruction cycles. If any of the executed instructions accesses memory (load/store instructions), the effective address of the operand may be modified in the same bit/byte position used to mutate the address of the executed instruction.

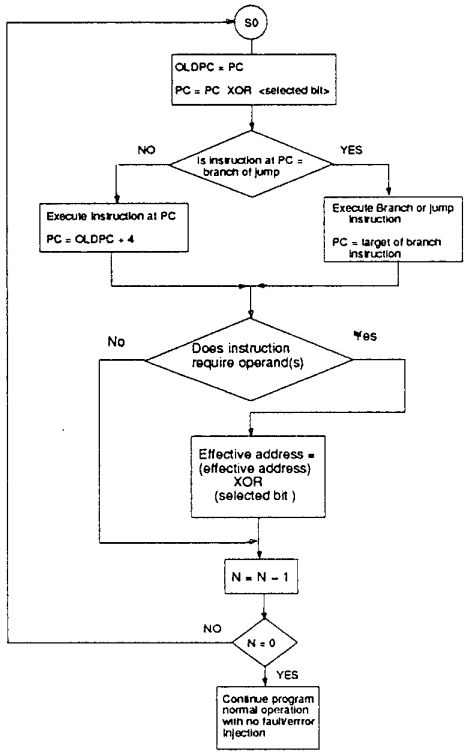


Figure 7: Mechanism for permanent address fault injection

- Data line fault

  When the program execution reaches the address of the selected instruction, the processor is interrupted. The value of the instruction at that address is modified. The program is then trapped N times where N is a number that determines the duration of the fault in instruction cycles. If any of the executed instructions accesses memory (load/store instructions), the operand values may be modified in the same bit/byte position used to mutate the executed instruction.

- Fault in condition code flags

  This fault emulates a stuck-at fault in the condition code register. When the program execution reaches the address of the selected instruction, the selected condition code bit is modified. The program in then trapped N times where N is a number that determines the duration of the error in instruction cycles.

6.4 Data Collection and Analysis Module

This module measures and records the response of the system for every injected fault/error. For each run, the location of the fault/error (virtual address), the affected bit, and the affected register, if any, are recorded. Terminating conditions for every run are also appended to the logfile. Terminating conditions indicate whether the resulting error: 1) was dormant (did not lead to a failure and did not produce wrong output during the lifetime of program execution), 2) had led to a failure (the test program either produced wrong output, or was terminated after it timed-out, or 3) was detected. Terminating conditions that result in detected errors are due to: 1) executing "exit(*cause*)" statements in the test program code, where *cause* is a value that either indicates the nature of an error detected by a user detection mechanism, or signals the end of the program execution, 2) an error triggering one of the built-in error detection mechanisms of the system. Note that when the test program terminates abnormally, it returns to its parent (in this case the fault/error injection process) a flag indicating the nature of the error that caused the system to abort the execution of the test program.

The data analysis module also records the identity of the error detection mechanism and the error detection latency if the error was detected. Finally, a flag used to indicate the results of the *compare* function utilized to compare the output produced by the current run and *reference* (explained in Section 6.1) is appended. The function *compare* utilized in all the experiments presented in Section 8 uses the UNIX *cmp* function that performs a byte-by-byte comparison of two files. The user may decide to utilize another *compare* function more suitable to the test program. For example, for non-deterministic applications, *compare* would check whether the difference between corresponding elements from two files is within a specified limit. FERRARI may also be used to test systems that utilizes spatial redundancy techniques. For example in a TMR system, FERRARI can inject faults/errors into one of the TMR modules and the output of the voter is considered to be the *compare* function output.

At the end of the experiment, the collection and analysis module collects these results along with the associated status flags and calculates percentages with respect to coverage, latency, and type of error detection mechanism for each experiment.

7 Experiment Description

Experiments presented in this paper were conducted on SUN SPARC workstations running SUNOS 4.1. These experiments provide an insight of the type of faults and errors that can be injected into the CIP module. These experiments were selected to demonstrate the capabilities of FERRARI, as well as to study the behavior of the target system when injected with faults and errors. In addition, a variety of faults and errors were injected to measure and compare the effectiveness of several of the error detection and correction techniques that are either built into the operating system or are embedded into the test programs.

For every experiment, the user selects the fault type and fault model to be injected and 6.4) injection runs. In each run, the bit position(s), the selected register to be faulted (if any), and either the location (address inside the program code, including library codes) or the instance at which a fault/error is injected[4] were randomly selected.

Results for over one million runs are presented in this paper. The criterion adopted when selecting the number of runs per experiment was based on obtaining a consistent average behavioral response of the system (e.g. percentages of "No Error", "Undetected Errors", and "Error Coverage" including the distribution of the contribution of each of the error detection mechanisms). For some of the conducted experiments, the response of the system became consistent at 10,000 runs, while for others, the behavior of the system became consistent at 20,000 runs.

The guideline followed when selecting test programs was to maintain an automated injection environment while making fault/error injection runs. This feature resulted in conducting a large number of runs for each experiment, thus providing confidence in the measurement of the response of the system. Another factor considered when selecting test programs was to evaluate several of the concurrent error detection and correction techniques that were embedded at the application-level code. As a result, test programs used in our experiments were application-level programs.

An advantage for injecting faults/errors in the system at this level is that many of these faults/errors generate traps (error conditions and exceptions) which are later detected by the built-in error detection mechanisms of the system (e.g. detecting an "illegal instruction"). Once these errors are detected, the system aborts the execution of the program and returns to its parent shell, which is in this case FERRARI.

When those same errors, on the other hand, were trapped while the system is executing in the supervisor (kernel) mode[5], the processor enters either an endless "wait" state, or a "diagnostic" state[6]. In both cases automating the fault/error injection process becomes impossible since the system has to be reset manually in order to continue the fault/error injection experiments. The study in [6] has shown that injecting faults/errors in the system while executing in either mode generates the same traps but differs in the action taken once the error is detected. Note that injecting the system with faults/errors while it is running in the kernel mode is accomplished by running FERRARI as a daemon process[7] in the supervisor mode. As a result, FERRARI will have access to supervisor allocation tables and would thus be able to modify the processor state while it is executing operating system code.

The procedure of fault/error injection in FERRARI is shown in Figure 8. In each experiment conducted, a selected application is first run without injecting an error in the system. The output, named *reference*, is written to a file for future comparisons. A fault or error is injected into the system while running the application. If no error detection mechanism is triggered, the output of the current run is compared to *reference*. A difference between the two outputs indicates an error has resulted in a wrong output and that the error was not detected by any of the error detection mechanisms. This would contribute to the lack of coverage of the mechanism.

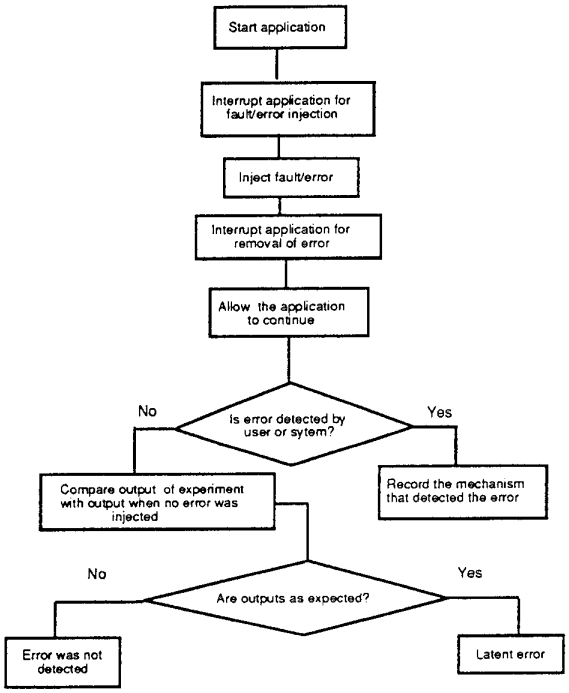


Figure 8: Fault/error injection procedure

The following is a list of the test applications utilized in our experiments.

1. Matrix multiplication using checksums [4].
2. Quicksort with assertions [9].
3. Robust data structures applied to modular robust binary (MRB) trees [7].

8 Empirical Results

In this section we present the results of fault/error injecting SUN SPARC1 workstations while running the above applications. Both permanent faults and transient errors were injected in our extensive studies. The results of the experiments presented in this paper, however, concentrate on transient errors, since the results were more interesting, and since we found that errors due to faults which were active for more

[4] during the course of execution of the test program

[5] The SPARC processor supports multi-tasking which requires the processor to be able to operate in two modes: a supervisor and a user mode.

[6] In this mode, the system dumps all its memory to a swap area and later reboots the machine.

[7] In Unix, a daemon process is one which is running silently until awakened by a request.

than a few instruction cycles were very likely to be detected by one of the error detection mechanisms. This is consistent with previous work done on permanent faults [10].

The first experiment was designed to evaluate the coverage of error detection mechanisms under different types of fault and errors. The next experiment attempted to determine the percentage of injected errors which remained latent for a particular application. The coverage sensitivity to different error models and the effect of system error detection mechanisms was studied in the next two experiments. Finally, the tradeoffs between error detection capability and performance overhead were measured.

8.1 Effect of different fault/error injection methods

Experiments were conducted to compare three different methods of fault and error injection. These are: 1) corrupting the task memory image, 2) spatial transient error injection, 3) and temporal transient error injection. In these experiments we injected over 15,000 errors in the system while running the quicksort application for two different data sizes. The purpose of these experiments was to study the variation of error coverage with data size when using these three injection techniques. Figure 9 presents coverages for the three experiments. In the first experiment, a fault was injected in the task memory image before program execution started. This was referred to previously as the "Memory Corruption" method. The injected fault, as explained earlier, remained throughout the execution sequence of the program and the faulty value was potentially used many times. This is referred to as a "memory error" in the figure. In the second experiment, an address line was randomly selected before program execution started. Once the program used the erroneous value (in this experiment a data line error), the error was removed. This is referred to as a "spatial transient error" in the figure. The "temporal transient error" injection method was used in the third experiment. In this experiment, the error injection was accomplished by interrupting the execution of an application at a randomly selected instant of time, and changing the value of the next element fetched from memory.

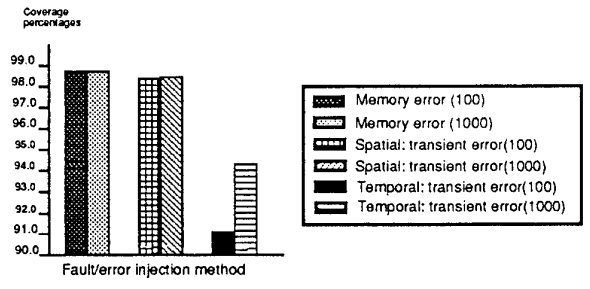


Figure 9: Error detection for quicksort application on different data with different injection methods

Results presented in Figure 9 demonstrate the variability of the error coverage of the detection mechanisms under different injection methods. From these results we deduce the following.

- Errors injected in the task memory image exhibited the highest coverages since the error, as argued before, was exercised more than once if the corrupted instruction was in a loop.
- The coverage was insensitive to the size of the sorted data when faulting the memory image of the test program and when using the spatial injection method. The coverage, on the other hand, increased as the size of the sorted elements increased from 100 to 1000 elements for the temporal error injection method.

This behavior becomes clear when one realizes that the quicksort application was embedded with "assertions", a data value error detection mechanism. The quicksort application is composed of three segments: 1) initialization, 2) data loop, and 3) file closing. In the "data loop" segment, the program reads and sorts data elements in ascending order. When the size of the sorted elements increases, the execution time inside only the data loop segment is increased whereas the execution time inside the other two segments is not affected. As a result, the probability that a data error is injected inside the loop and consequently is detected by the "assertion" mechanism increases when the "temporal" injection method is employed. This behavior, however, was not observed in the other two injection methods. In those methods, the data error is injected at the first incident when the value of the "program counter" matches the value of the preselected address location, including any address inside the data loop segment. Consequently, the response of the system for the memory corruption and spatial injection methods is independent of the execution time of the application. Therefore, the temporal injection method would challenge the error detection mechanisms to a higher degree.

8.2 Effect of latent errors

Figure 10 shows the result for the matrix multiplication application using the checksum technique for error detection. Errors from every error model shown in Table 1 were injected into the system while running the matrix multiplication of two matrices each has 20 by 20 elements. For this experiment, we first injected the transient errors at all legal addresses traversed during the course of execution of the test program. Later, we utilized the pseudo-random number generator to select the address at which an error will be injected. We started with 1000 runs and kept incrementing the number of runs by 1000. After 10,000 runs, the system exhibited the same behavior (measured in terms of the distribution of the responses of the system, as explained later) to that observed when the test program was injected exhaustively.

A large percentage(41%) of the injected transient errors were latent ("No Error") and did not affect the program output. Latent errors include erroneous values that are overwritten before they are used in subsequent computations, and errors in the condition code

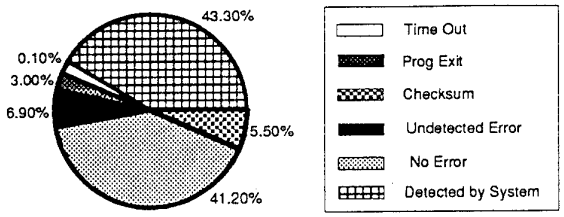


Figure 10: Distribution of errors for matrix multiplication application

that do not affect the expected course of execution of the test program. In Figure 11, we list a segment of code, shown in both C++ and the corresponding low-level SPARC assembly language, mutated to emulate the injection of an error. In the C++ code, the algorithm checks whether the value of the variable "argc" is less than 4. In this example, the injected error modified the "immediate" operand of the instruction to the value of zero. When the "cmp" instruction is executed, the value of the internal register "O0" was greater than zero and the program branched to location "main + 120". Thus the injected fault did not cause the program to deviate from its normal execution.

```
/* C++ code */

if(argc < 4){
  cout << "usage <qsort> <array_size> <input_file> < output_file>";
  exit(user_exit_code);
  }

/*assembly code */

0x2ad8  <main +68>:   ld  [%fp + 0x44], %O0
0x2adc  <main +72>:   cmp %O0, 3
0x2ae0  <main +76>:   bg 0x2b0c       <main +120>
0x2ae4  <main +80>:   nop
0x2ae8  <main +84>:   call 0x3108 <op$alshift__7ostreamPCc>
0x2af0  <main +88>:   nop
0x2af4  <main +92>:   ld [%fp +0x48], %O0
0x2af8  <main +96>:   call 0x50fc <exit>
```

Figure 11: An example of a latent error

43% of the errors were detected by the built-in error detection and protection mechanisms in the SPARC system. These mechanisms, which are triggered before any application-level error detection techniques, trap illegal instructions, bus errors, segmentation faults, bad system calls, interrupts, arithmetic exceptions, etc. In Section 8.4 we present the contribution of these built-in error detection mechanisms.

Of the remaining errors, 5.5% were detected by the checksum technique and 3.0% by program exit conditions ("Prog Exit" in the figure). Program exit conditions were features added to increase program robustness, such as checking the status of I/O operations when opening and closing files, and were found to enhance the error detection capabilities of the system. The "Time Out" value in Figure 10 and in all other figures indicates the percentage of errors which caused the system to enter a *wait* state. This case was observed when the injected fault caused the program to start executing a system *wait* call. Apparently the arguments passed to this system call (*wait*) were set to produce an infinite loop. For such cases, a timer was used to abort program execution. In this particular application, 6.9% of the errors were not detected ("Undetected Error"), and produced incorrect results. *Undetected Errors* are errors that are not detected by the application program error detection mechanisms, yet they do not cause the execution of the application to terminate prematurely. The nature of such errors and techniques to prevent them will be described later in the paper.

As shown in Figure 12, the response of the system is confined to only a few categories (*Detected by the system, No Error, Undetected Error, Checksum* or *User, Prog Exit*,and *Time out*). These categories are not limited to the SPARC system; they are similar to others reported in the literature. Results from other studies have also confined the responses of the targeted system to only few categories based on service outages [3], statistical distribution of responses [8], or error manifestation of fault injection experiments [2]. Note, however, the system responses obtained through our experiments do not include the category "system crash", which is a very common error manifestation reported in other studies. As argued previously, we decided to avoid system crashes (consequently the time delay to reboot the machine once it crashes), by fault/error injecting while the processor is in the "user" mode.

In order to concentrate on detectable errors, the rest of the figures in this paper show the coverages of errors when latent errors are excluded from the calculations. Figure 12 shows the distribution of coverages for matrix multiplication using checksum only when excluding the latent errors.

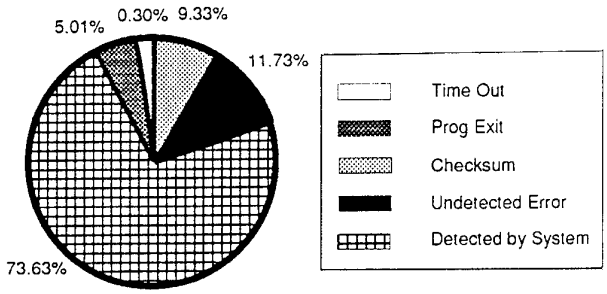


Figure 12: Percentages of errors detected in the matrix multiplication application when latent errors are excluded from the calculations

8.3 Coverage sensitivity to different error models

The purpose of this experiment was to study the response of the system when injected with faults/errors that are representative of failures in the real hardware[8][5]. Figure 13 shows the system behav-

[8] As mentioned earlier, injecting faults/errors that emulate hardware failures and are 100% accurate requires conducting a

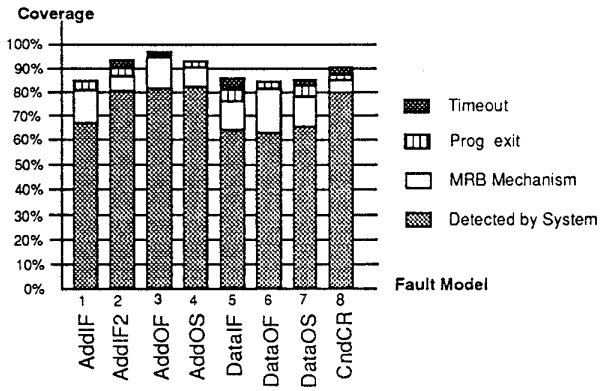


Figure 13: Error coverage of the MRB tree as a function of the injected transient error model(10,000 runs).

ior when transient errors presented in Table 1 where injected into the system while running the MRB tree test program.

Over 60% of the detected errors were trapped by the built-in system error detection mechanisms. In Figure 13, the highest coverage was obtained when address line errors were injected while loading/storing operands (AddOF and AddOS) where the system detection techniques (elaborated in Section 8.4), the assertion technique, and other program robustness techniques have contributed to the overall coverage. The lowest coverage was obtained when data line errors were injected (models DataIF, DataOF, and DataOS). Note that although the MRB tree error detection mechanism is a data value checking technique, it was still effective for other errors caused by the injected errors. The effectiveness of the MRB tree error detection, however, was the highest when errors were injected into the data bus when operands were either fetched or stored (error models DataOF and DataOS).

8.4 Effect of system error detection mechanisms

The SPARC system has built-in error detection mechanisms that monitor address, data and control buses, Figure 14. In this experiment, the system was injected with the eight different error models (see Table 1), while running the matrix multiplication application using checksums. These coverages were found to be comparable to those obtained with the quicksort and robust data structures applications. In this figure, most of the illegal instructions produced were caused by injecting transient errors from models AddIF, AddIF2, DataIF (when the processor is fetching different instructions) and model CndCR. Segmentation faults were triggered by memory access exceptions which occur when a data memory access or an instruction prefetch fails to complete normally. Although this response is anticipated when address line errors were injected, it is less intuitive when data errors were injected (models DataOF, DataOS). Further analysis has shown that the majority of these errors were modifying operand values that specify the memory address of a data element directly or indirectly (an example is the case when the contents of the destination register for a "load" instruction is mutated). In Figure 14, "Bus error" is due to a memory misaligned access which occurs when a load, store, or exchange instruction attempts to access a memory address that is not consistent with the size of the access. An example of a misaligned access is when a half-word access is attempted to an odd byte address.

study to map low level hardware failures to these fault/error models.

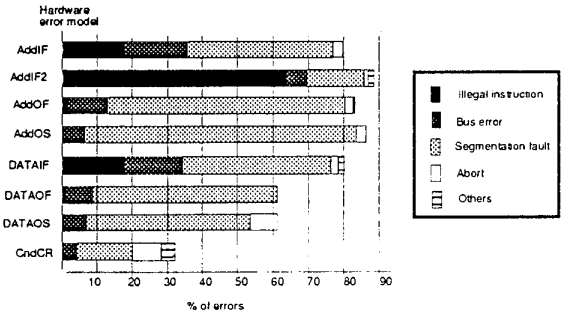


Figure 14: Percentage of errors that were detected by the SPARC built-in error detection mechanisms. "others" = hangup, bad system calls, arithmetic exceptions (20000 runs).

8.5 Measurement of error detection latency

Figures 15 shows the average user, system, and overall error detection latency for the quicksort application. In this figure, latency is shown for selected transient error models presented in Table 1. The sorted list for this experiment consisted of ten integer elements. As shown in the Figure, the latency for the user detection mechanism was several thousands of instruction execution time compared to a few hundreds for the system error detection mechanisms. The reason is that user assertions (elements are monotonically increasing) are applied near the end of the execution of the program, whereas the system error detection mechanisms are triggered at every instruction. A timeout interval at the beginning of the experiment was set to 5000 instruction cycles. If an error was not detected during this interval, it was labeled as an "Undetected Error".

As shown in the figure, latencies for address line errors were in general smaller than those for other injected error models. This behavior is expected since most the injected address line errors (80%), as was shown in the previous experiment, were detected by the built-in system error detection mechanisms such as "segmentation faults", "illegal instructions", and "bus error". The system error detection mechanisms trap these illegal conditions in one or few instruction

cycles. Note that since the *quicksort* application occupies a small address space, the probability of inducing a "segmentation fault" exception increases, and is detected by the memory management unit in the few cycles. Similar arguments holds for "bus error" and "illegal instruction" exceptions. Also note in the figure that the latency for AddIF2 model is smaller than that for AddIF since more than one bit of the instruction address is mutated in the AddIF2 error model.

Regarding data line errors when operands are accessed, DataOS has higher latency than that of DataOF, as shown in Figure 15. A principal reason for this behavior is that some of the corrupted data operands are used in the address calculation of other operands. For the DataOF model, these corrupted data are immediately used to fetch other data, whereas for the DataOS model , some of these corrupted data are only used at a later stage during the course of execution of the test program, depending on the control flow of the program.

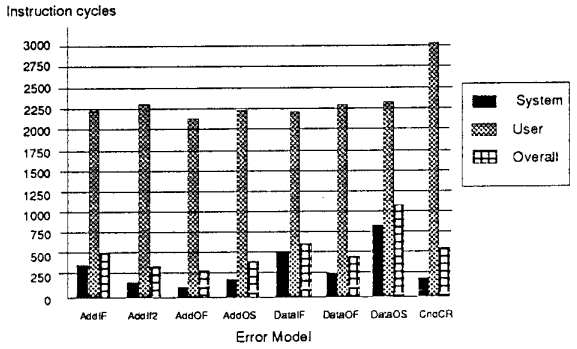


Figure 15: Error detection latencies for matrix multiplication utilizing checksum techniques (10,000 runs).

9 Conclusion

This paper outlined the Navy's AAST Fault Tolerant Demonstration program and described two tools being used in the demonstration. This program will clarify the precise legal language needed in future Specifications and SOW of complex, computer based weapon systems and what validation techniques are needed to support that contract language.

During the Gulf War, Naval aircraft sustained high Full Mission Capable (FMC) rates (in the high 90% range), but these high FMC rates were sustained at the cost of high Maintenance Man Hours per Flight Hour (MMH/FH), (30 to 65 MMH/FH), high spares usage and high false alarm rates, (consistently in the 30% to 35% range). Future complex weapon systems will increasingly rely on digital sub-systems and the dependability of these digital designs will play a critical role in the effectiveness of those systems in the field. In future combat situations, the rate of spares usage, the time to isolate and repair the equipment, and the false alarm rates will play a critical role in the effectiveness of those systems. As budgets decrease, fewer systems are purchased and commercial parts are used, the dependability of those systems will be a critical factor in the effectiveness of the next generation of computer based combat systems.

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DISCUSSION

Question: How do you assure the correctness (reliability) of your fault injection system, i.e., that its assessment of the response of the fault tolerant system (error detected/not detected) is correct?

Answer: It is difficult to guarantee the correctness of any software. Since we are injecting faults and errors, the target system should be able to handle even "incorrectly" injected faults. We use an initial run of the application without any fault/error injection as the "gold" result (even this cannot be guaranteed to have no errors in the application code), then compare every fault injection run with the baseline result to tell whether the target tolerated the fault.

IMPROVING MULTICHIP MODULE (MCM) DESIGN AND RELIABILITY USING THE INTELLIGENT MCM ANALYZER

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1. SUMMARY

The Intelligent MCM Analyzer (IMCMA) is a software tool which allows the designer to concurrently assess the reliability of an MCM design based on operational parameters. Traditionally, this type of assessment takes days to accomplish and is performed after the design phase. The Intelligent MCM Analyzer does not require the designer to be a thermal/reliability expert and gives an assessment in minutes depending on the complexity of the design and the speed of the computer. IMCMA assists the designer in achieving a robust design which will improve both quality and reliability. The software uses object-oriented data representation, a blackboard architecture and heuristic expertise to perform lower level reasoning associated with finite element thermal analysis techniques that are normally very tedious and labor intensive. A test case will be presented comparing results from IMCMA with the results from a general purpose finite element code. The ultimate payoff will be the manufacturers' ability to build higher quality, higher reliability MCMs at a lower cost.

2. INTRODUCTION

An electronic package generally contains one or more integrated circuits (ICs) combined into a functional unit. A Multichip Module (MCM) is a style of electronic packaging which incorporates multiple IC die in a single package. An electronic package has four major functions: circuit protection, signal distribution, power distribution and thermal management. The main concern of this paper is with thermal management during MCM design. The advantage of MCM technology is a reduction in size, weight and power. The overall power for an MCM can be lower but the power density can be quite high. This can easily lead to a thermal management problem which will lower the reliability of the module if the higher operating temperatures were not accounted for in the design process. Complex multichip modules usually provide high performance, and given their typical low production levels, MCMs are often quite expensive. MCMs come in three basic types: MCM-C (Ceramic dielectric), MCM-L (Laminated, reinforced organic dielectric), and MCM-D (Deposited, unreinforced low dielectric). Each type of MCM has an associated set of materials that can be used for its construction and a selection of die from which to choose to meet the specific application's requirements. Consequently each MCM design has a unique type, set of materials, number of die, and size. All of these factors affect the thermal management of an MCM.

The engineer has a variety of MCM design considerations to address. The design process determines the thermal profile and reliability for a given MCM. From this baseline the reliability and thermal performance will only degrade due to defects that arise from the manufacturing process. For this reason the designer should be given the ability to see the thermal profile of the design before manufacturing begins. This will allow the design to be changed in order to improve the thermal performance and consequently the reliability.

Reliability through design is a methodology which addresses reliability issues throughout the course of the design process. To this end, tools must be available which allow the designer to enter into and operate in technical areas where they may have limited expertise. This is because of the multidisciplinary requirements associated with the design of most modern electronics. Rome Laboratory has addressed this problem through the use of a blackboard framework which allows the thermal evaluation of a MCM design even when the designer may lack technical experience in thermal modeling.

3. DESIGN BASED THERMAL ASSESSMENT

Rome Laboratory was one of the originators of microelectronic reliability assessment using finite element methods[1]. Assessments of new designs have included MMIC modules[2], the Hughes 3D computer[3], and multichip modules. The Finite Element Analysis (FEA) method has become a standard practice at Rome Lab for the thermal assessment of new electronic designs. This assessment is based on environmental and operational stresses induced during the production and operation of advanced electronics. This process is described in Rome Lab Technical Report, RL-TR-91-251, "Reliability Assessment of Wafer Scale Integration Using Finite Element Analysis"[1]. A flow chart of this process is shown in Figure 1. The process can be quite time consuming (e.g., days) and requires qualified personnel. If this technique is going to be used by a designer, its efficiency must be dramatically increased.

There are three areas in which this process needs to be improved: Finite Element Model Generation, Ensuring Accuracy of the Model, and Remeshing or Sub modeling. The largest bottleneck is the amount of time required for the finite element model generation. At this step, a 3D geometric representation of the MCM is created. This process takes disproportionately more time than the actual analysis

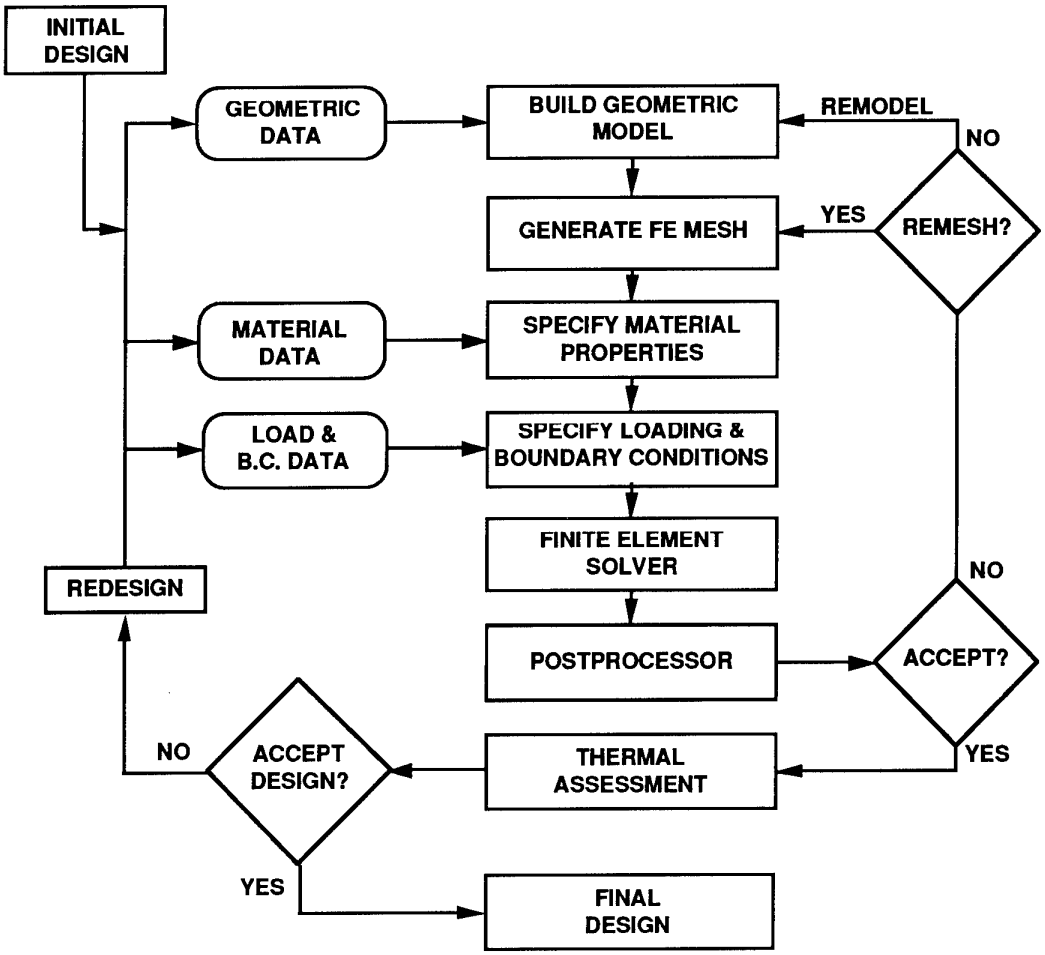


Figure 1. FEA Thermal Assessment Process

because of the complexity of multichip modules. Second, a method is needed to ensure the accuracy of the numerical analysis. Since finite element analysis is a numerical method, checks must be done to ensure its proper usage. Finally, the remeshing or sub modeling must be automated to the extent that remeshing of the original model or sub modeling of critical areas can be performed without engineer interaction. The FEA thermal assessment must be integrated into the design process if design choices are to translate into highly reliable products. To this end Rome Laboratory has developed IMCMA, an automatic analyzer that incorporates our knowledge of finite element analysis and multichip modules in a form that can be integrated into the design process[4].

4. IMCMA OVERVIEW

The software architecture used for IMCMA is based on the blackboard problem-solving paradigm developed by the artificial intelligence community. A blackboard system performs problem solving by using three basic components. The first is a global database containing input, domain and run-time generated data. The second is a collection of independent modules, called Knowledge Sources (KSs), which contains the domain knowledge needed to solve the problem. The third is a control mechanism, separate from the individual KSs, that makes dynamic decisions about which KS to execute next. This approach provides a framework for integrating diverse software components, allows specialized knowledge representations, supports multi-level reasoning, and is conducive to incremental, evolutionary software development.

IMCMA has automated approximately ninety percent of the FEA thermal assessment process. IMCMA performs much of the lower level reasoning associated with the development of a finite element model. Features include the use of both numerical and symbolic knowledge sources, the use of heuristics to determine the mesh density of the finite element model, the use of objects in conjunction with the blackboard framework to allow for examining and reasoning about the model and the analysis, the evaluation of the numerical accuracy of the model, and the use of simplifying

assumptions to reduce the complexity of the analysis. The savings in modeling and analysis time that IMCMA exhibits comes about principally through the use of knowledge sources that control the various steps in the process. These knowledge sources supply the type of information and make the same type of design simplifications a knowledgeable engineer would. The designer must provide the following information as input to IMCMA:

Size of Package
Package Material
Size of Substrate (length, width, thickness)
Substrate Material
Substrate Attach (material, thickness)
Chip (size, location, power dissipation)
Chip Material
Chip Attach (material, thickness)
Boundary Conditions

5. IMCMA OPERATION

This input information can be entered either through a Graphical User Interface (GUI) or translated from electronic information previously stored in a library or generated by another design tool. At this time the user can specify several run-time parameters before invoking the "run" command. From this point the rest of the process is automatic. A detailed view of the software architecture is shown in Figure 2.

IMCMA begins by doing the most time consuming task in the FEA thermal assessment, finite element model generation. The time required for building the model is greatly reduced by the various knowledge sources making design simplifications. These include modifying the models dimensions to simplify the mesh density, making use of symmetry, and extruding the various components with the correct materials and thicknesses.

The Adjust Model KS is used to optimize the 2D geometric mesh density that will be used by the finite element model. There are three aspects to this optimization: reducing the number of elements, developing elements with good aspect ratios, and allowing a higher mesh density in areas of special interest. The number of elements needs to be kept low in order to keep the finite element analysis time sufficiently low for the analysis to be accomplished during the modules design phase. This is accomplished by the Adjust Model KS moving the location of the corners of the various integrated circuits a slight amount, so that they are in alignment. This modification does not affect the accuracy significantly and has the effect of greatly reducing the number of elements. For the example presented, the unmodified model has 700 elements per layer while the modified one has 26 elements. After this modification is made, the other two aspects of the KS are activated, and the model is then meshed with the two mesh parameters controlling the mesh generation. The auto meshing makes sure that each integrated circuit is comprised of at least 4 elements, while allowing the areas of lower heat flux (e.g. the substrate and package) to be divided into a lower mesh density. The aspect ratio also is controlled so that no element has an aspect ratio greater than 8 to 1. The results of this KS is a mesh that is optimized for the fastest analysis time for the thermal analysis of the MCM.

The Symmetry KS can reduce the problem size by a factor of four where the integrated circuits are similar and are laid out in a symmetric pattern. This frequently occurs in memory modules. With this KS, the location of the lines of symmetry are found and the geometric model is then reduced

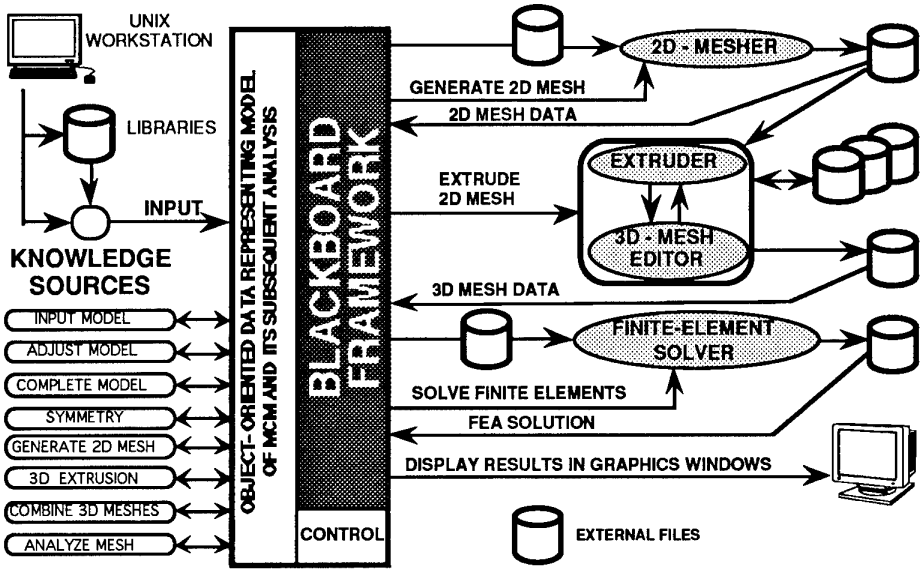


Figure 2. Software Architecture

to one half or one quarter of the original, depending on the level of symmetry. The correct adiabatic boundary conditions are then applied to the newly formed boundaries, so the solution will be the same as that of the original problem. This KS also significantly reduces the amount of time for the modeling and analysis because of the reduction in the number of elements used in the problem.

The Extrusion KS and the Complete Model KS are used to build up the 3D mathematical model that reflects the physical reality of the MCM. These KSs have built into them the knowledge and understanding for assembling the basic structures associated with a multichip module. This includes items like: the chips are located on top of the substrate and are the heat producers, the substrate is attached to the package with an attachment material, the nodes of the various components that are attached to one another have to be merged into one node. These are the types of things that are normally accomplished by the engineer building the finite element model.

Finally, the Analyze Mesh KS is activated which adds the boundary conditions and invokes the finite element solver. The solver yields a description of the behavior of the physical system, including thermal profiles and the stresses and strains associated with the temperature distribution. A color coded temperature profile of the module is displayed for the user. IMCMA has an "inspector" capability, which gives the user the ability to browse the common, object-oriented database containing both the descriptive and analytical data associated with the analysis. At this point the designer has several options:

Continuing the Design Process Without Changes
Changing the Design and Rerunning IMCMA
Sub modeling an Area of Concern

6. TEST CASE

The multichip module used as the test case is a test vehicle from a MCM reliability program. The test vehicle is a MCM-D that has an alumina substrate with 10 milled cavities for die and a polyimide/copper interconnect on top. The test vehicle is about 1.6 inches by 1.6 inches in size.

The MCM was modeled using a generic commercial finite element software code. The finite element model generation took two days to create and contains about 16,000 elements and 10 layers. The analysis of the model takes about four hours to run on a workstation. The thermal profile from the analysis is shown in Figure 3.

The same MCM was modeled and analyzed using IMCMA (see Figure 4). The input file took about five minutes to prepare. After the input file was prepared, the software built the finite element model and performed the analysis in about 20 minutes. The model contains 768 elements and 3 layers. The difference in the temperature profile of the two analyses is minor. However, the difference in time is tremendous. IMCMA gives the user a thermal profile of the MCM design quickly and does not require the user to be an expert in thermal modeling.

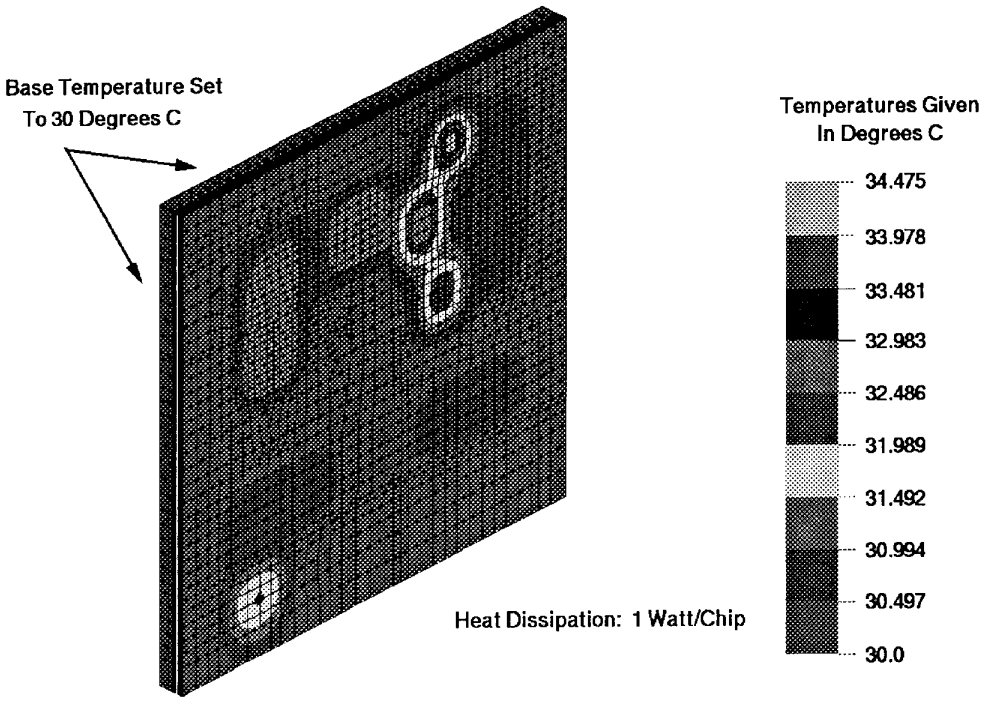


Figure 3. Thermal Profile From Commercial FEA Code

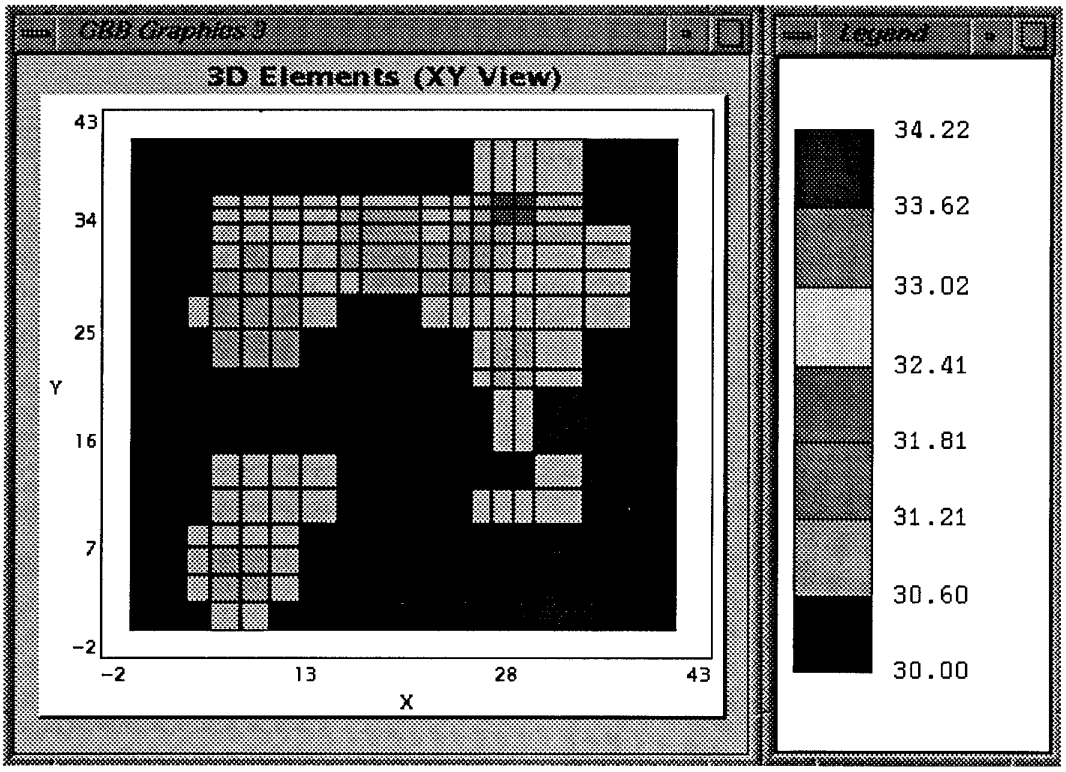


Figure 4. Thermal Profile From IMCMA

6. CONCLUSION

Thermal assessment of multichip modules is now an affordable capability for the designer. The IMCMA software allows for the thermal evaluation of a MCM design even when the designer may lack technical experience in thermal modeling. The designer has the ability to perform this type of analysis during the design phase, which leads to better designs and lower cost. Potential users of this technology include government organizations requiring independent assessment of contractor's designs for new multichip modules as well as the manufacturers of MCMs. This will increase multichip module usage and ensure them a place in the high volume electronic components market.

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DISCUSSION

Comment: DELPHI is a European project (ESPRIT) to develop electronic component models (including MCM) using reduction techniques. Information is available. It is always surprising to develop easy tools for electronic engineers or designers, because it usually gives easy results, certainly, but far from reality, when the components are installed in a module.

Author's Reply: Verification and validation is always important – and sometimes difficult.

Question: Will you consider convection?

Answer: Yes, it is a possible addition to the software capabilities.

Question: For avionics applications, sensor data streaming is usually stochastic in nature and software driven. In addition, the power dissipation of many common devices (such as CMOS or BiCMOS) is linear with the data rate and therefore also stochastic in nature. This is a first order effect on the results of a thermal analysis. If analysis is performed at only steady state, then which power level is used? Using maximum power levels will lead to overdesign of the MCM with high cost penalties. Does Rome [Lab] have a program to statistically model power dissipation vs. software or data streaming to come up with a realistic mean and standard deviation?

Answer: Power dissipation values are chosen by the user. They can assume worst case, or model several input values and interpret the collective results.

ULTRA-RELIABLE DIGITAL AVIONICS (URDA) PROCESSOR

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SUMMARY

Texas Instruments Incorporated (TI) developed the URDA processor design under contract with the U.S. Air Force Wright Laboratory and the U.S. Army Night Vision and Electro-Sensors Directorate. TI 's approach couples advanced packaging solutions with advanced integrated circuit (IC) technology to provide a high-performance (200 MIPS/ 800 MFLOPS) modular avionics processor module for a wide range of avionics applications. TI 's processor design integrates two Ada-programmable, URDA basic processor modules (BPMs) with a JIAWG-compatible PiBus and TMBus on a single F–22 common integrated processor-compatible form-factor SEM-E avionics card. A separate, high-speed (25-MWord/second 32-bit word) input/output bus is provided for sensor data. Each BPM provides a peak throughput of 100 MIPS scalar concurrent with 400-MFLOPS vector processing in a removable multichip module (MCM) mounted to a liquid-flowthrough (LFT) core and interfacing to a processor interface module printed wiring board (PWB). Commercial RISC technology coupled with TI's advanced bipolar complementary metal oxide semiconductor (BiCMOS) application specific integrated circuit (ASIC) and silicon-on-silicon packaging technologies are used to achieve the high performance in a miniaturized package. A Mips R4000-family reduced instruction set computer (RISC) processor and a TI 100-MHz BiCMOS vector coprocessor (VCP) ASIC provide, respectively, the 100 MIPS of scalar processor throughput and 400 MFLOPS of vector processing throughput for each BPM. The TI Aladdin ASIC chipset was developed on the TI Aladdin Program under contract with the U.S. Army Communications and Electronics Command and was sponsored by the Advanced Research Projects Agency with technical direction from the U.S. Army Night Vision and Electro-Sensors Directorate.

1. URDA PROCESSOR MODULE[1]

As shown in Figure 1, the URDA processor module is implemented in a SEM-E, liquid-flow-through avionics card form factor. The URDA module combines data processing, signal processing, memory, and system interfaces on a single avionics module. Two URDA BPMs, each with 100-MIPS and 400-MFLOPS throughput capability, are integrated with a processor interface module (PIM) to provide a single SEM-E module with 200-MIPS and 800-MFLOPS throughput, JIAWG-compatible PiBus and TMBus interfaces, and a 100-MByte/second input/output port for high-speed sensor data transfer. The URDA BPMs are repackaged implementations of the TI Aladdin BPMs. To provide such high throughput in such a small volume, they are fabricated using TI's silicon-on-silicon packaging technology coupled with commercial RISC technology and TI's advanced BiCMOS ASIC technology.[2] The URDA processor is supported by TI-developed and commercially available tools for software development, software/system integration and test, and system design.

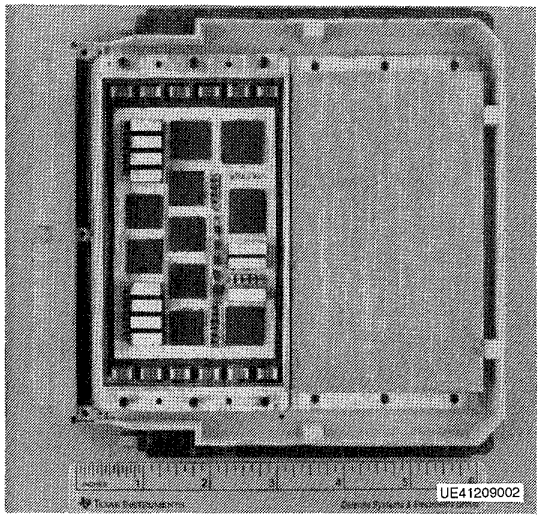


Figure 1. URDA Processor Module

The URDA architecture is shown in Figure 2. TI's approach provides a common processor kernel implementation in an MCM package (the URDA BPMs) integrated with an interface module that provides system-specific interfaces and functionality. Each URDA BPM has an Aladdin system bus (ASB), an input/output bus (IOBUS) port for communication and data

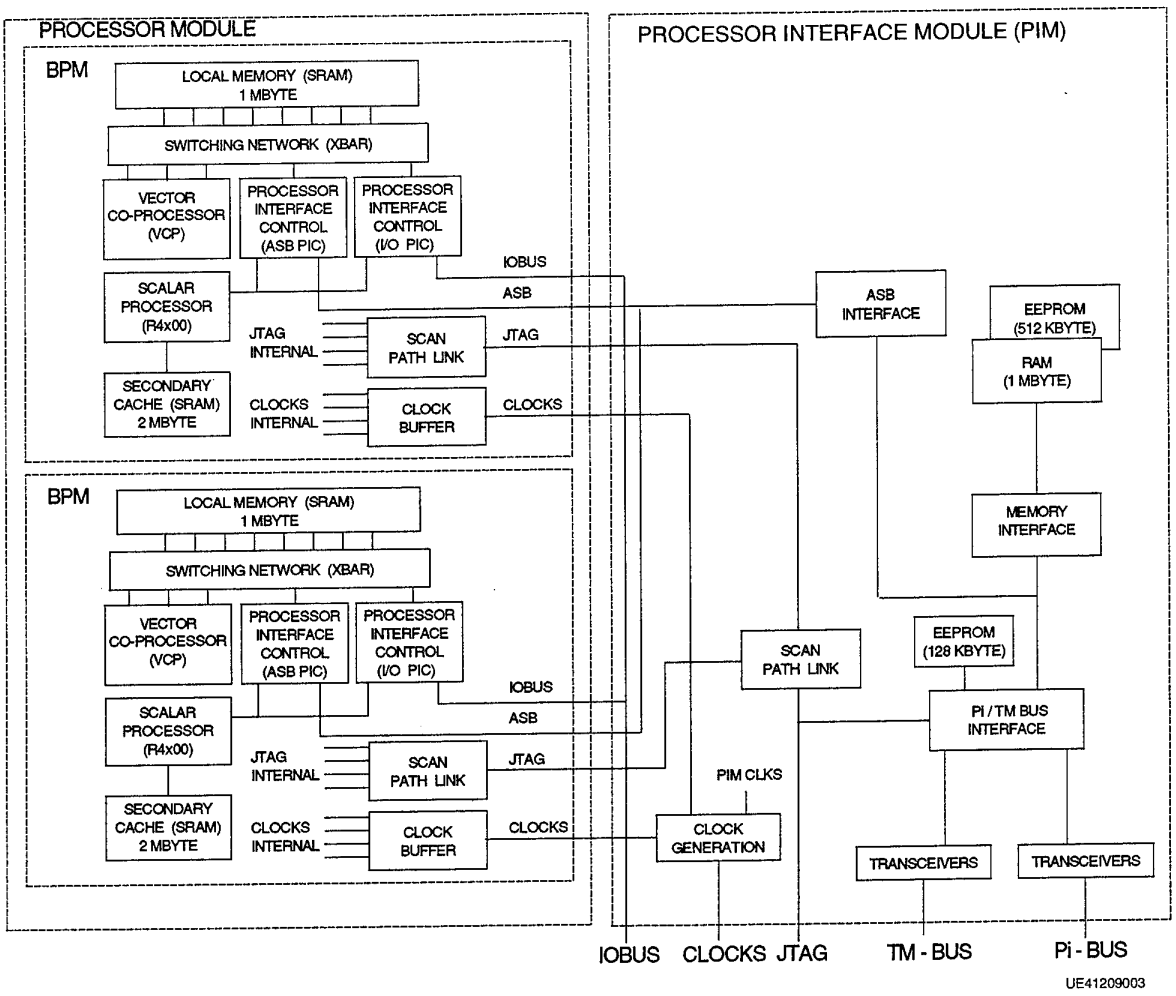


Figure 2. URDA Processor Module Architecture

transfer, and a JTAG interface for test and maintenance control. The PIM provides a personalization of the kernel processor to the specific system and application, including the interfaces to the backplane and support circuitry for the BPMs. This approach allows the common processor kernel MCM to be used in a variety of systems and module form factors without requiring mechanical or electrical design changes to the kernel processor functions, interfaces, or package.

The URDA system requirements include JIAWG standard PiBus and TMBus backplane interfaces to the module and a separate 100-MByte/second, high-speed IOBUS for sensor data transfer. The IOBUSs are routed to the PIM backplane connector, providing a common 100-MByte interface to both URDA BPMs. Circuitry on the PIM implements the PiBus and TMBus interfaces to the backplane, a TMBus-to-JTAG translation, a separate JTAG interface to the backplane, clock generation, interrupt and discrete control support, on-module nonvolatile memory for program store, and on-module ran dom-access memory (RAM) that acts as a store and forward interface between the PiBus and the BPMs. Both BPMs interface to the PIM store and forward memory via a common ASB interconnect. Because of design information availability and schedule compatibility, the F–16 modular mission computer (MMC) JIAWG PiBus and TMBus chipset was selected for use on the URDA PIM. A field-programmable gate array (FPGA) provides the interface between the ASB and the local memory bus of the MMC chipset.

1.1 BPM Architecture[1,3]

The URDA BPM architecture is shown in Figure 2. The local memory is implemented using TI custom 16K × 9 static random-access memory synchronous (SRAMS) devices

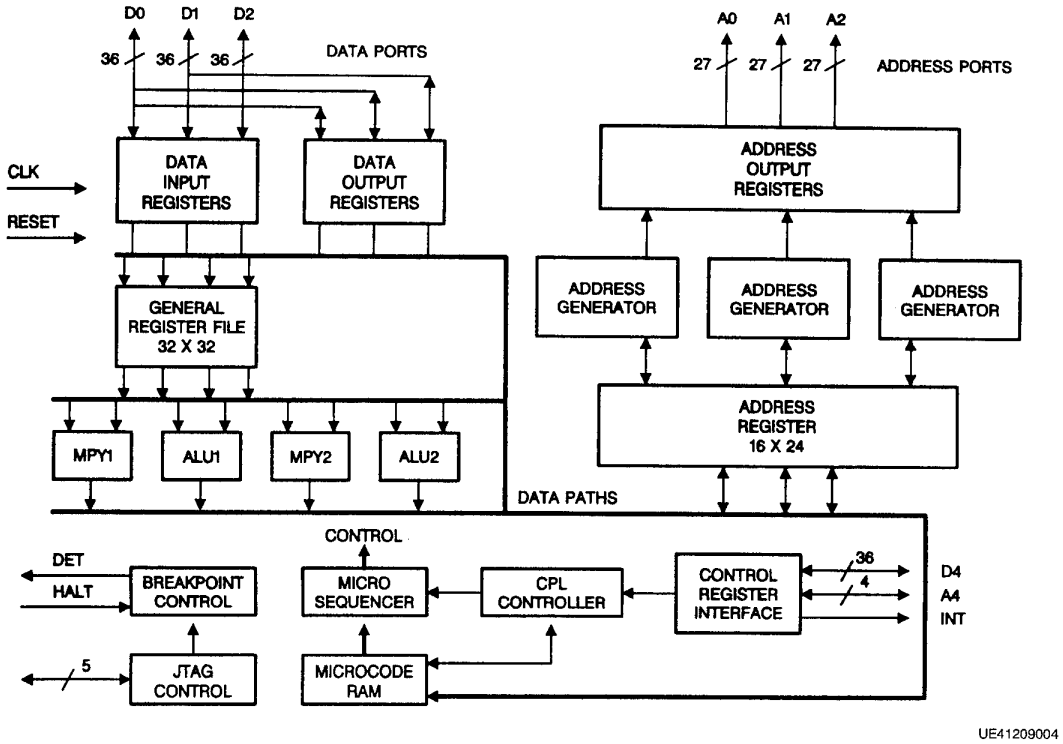


Figure 3. Vector Coprocessor Block Diagram

designed for 100-MHz synchronous operation. Local memory is divided into eight 32-Kword (32 bits plus byte parity) banks, accessible via six crossbar processor ports. The VCP has access to the local memory via three independent data ports connected to the crossbar devices. Access to local memory from the scalar processor and the two 25-MWord/second (100-MByte/second) buses (the ASB and IOBUS) is provided by the two processor interface control (PIC) devices. The sixth crossbar processor port is configured to provide real-time monitor access via probe points to internal crossbar trans- actions. All activity can be monitored by external test equip- ment at the 100-MHz BPM clock rate, clock by clock, for any memory port or any processor port, selectable via JTAG. A commercial scan path linker device provides the interface between the JTAG port and the JTAG test rings internal to the BPM. Each ASIC, except for the SRAMS, is designed with JTAG logic for test, debug, and fault isolation to the device level on the BPM. The scalar processor, a Mips R4000, provides 100-MIPS scalar processor throughput and accesses local memory at a 100-MWord/second burst rate (in eight-word cache blocks) via either of the PIC devices. Also provided for the R4000 are 512 Kwords (2 MBytes) of secondary cache memory implemented with commercial 128K × 8 SRAMs. Buffering and fanout of the 100-MHz clock is provided by a TI clock distribution circuit (CDC) that has been designed to minimize clock skew across multiple clock driver outputs. The VCP, PIC, crossbar, SRAMS, and CDC devices are all semi-custom BiCMOS devices designed for the TI Aladdin program and fabricated using TI's EPIC2B 0.8-micron process.

1.2 Vector Coprocessor (VCP)[1,3]

The VCP is a microprogrammable, pipelined processor containing multiple arithmetic resources, as shown in the block diagram in Figure 3.[2,4] All resources are controlled by an on-chip microsequencer executing from a 256 instruction by 192-bit, on-chip microcode RAM.

Two 32-bit multipliers and two 32-bit arithmetic logic units (ALUs) provide a peak processing throughput of 400 MFLOPS/MOPS at a 100-MHz BPM clock rate. The arithmetic resources support 32-bit integer fixed-point and single precision IEEE-754 floating-point formats. A four-stage pipeline implementation allows 100-MHz operation of the arithmetic units. A 32-word register file is available for use by the arithmetic units. The data paths also support passing data between the data register file and the address register file.

Three bidirectional data ports (coupled with three independent address generators) provide a peak I/O capacity of 1200 MBytes/second. A 16-word by 24-bit address register file supports operation of the three address generators. Three index

registers, a loop counter, and an accumulator register provide extensive indexing and window addressing capability. Each address generator provides a 24-bit address plus control signals to the crossbar devices, supporting sustained 100-MHz memory accesses on all three VCP ports.

Two loop counters are available for nested looping and can be loaded from microcode fields or the data register files. A program counter stack supports eight levels of nested subroutines, and several sources can be used to provide branch destinations for conditional or unconditional branching. Conditional branch decisions can be based on 30 arithmetic resource conditions, as well as loop counter status.

A command parameter list (CPL) controller provides on-chip operating system functionality in hardware. The CPL controller handles loading and execution of microcode routines as directed by Command Parameter Lists[4] implemented as application data structures loaded into the local BPM memory. Code executing on the R4000 scalar processor builds the appropriate CPLs and initiates action by the CPL controller. CPLs consist of two words and identify to the CPL controller the type of command to be executed (application, jump, microcode download, or microcode read) and can be chained together for execution of successive microprograms with no intervention required by the R4000 scalar processor.

Special consideration has been given to support for testability and software debug in the VCP design. A JTAG interface provides full boundary scan, internal scan of over 1300 data path flip-flops, and software access to debug support hardware. A signature register and signature compare logic in the VCP also provide support for software built-in test (BIT) routines and a microcode download checkpoint. Breakpoint logic consisting of two 20-bit counters with separate microcode address comparators provides multiple-event detection on micro- code instruction access. The breakpoint logic is initialized via JTAG and allows event detection on "n" occurrences of address 'A' followed by "m" occurrences of address 'B,' Once the VCP is halted, JTAG commands can single-step VCP execution, access register contents, and resume operation.

With four on-chip arithmetic resources, the VCP has a maximum processing throughput capability of 400 MFLOPS executing at a 100-MHz clock frequency. This performance far exceeds the capabilities of other existing processors. Table 1 shows the performance of the VCP for some typical signal processing algorithms as compared to the performance of two popular digital signal processors (DSPs): the TI TMS320C40 and the INTEL i860. A general-purpose library of algorithms implemented in microcoded routines is available for use in developing programs for execution in the VCP.

2. SOFTWARE SUPPORT[1,3]

TI's URDA software toolset supports URDA target parallel processing applications by providing:

- Application partitioning/mapping support
- Code translation tools for the R4000
- Code translation tools for the VCP
- Run-time environment (i.e., operating system support)
- Debug support.

Application partitioning/mapping support is provided through either the ADAS toolset or Teamwork/SIM tools. A uniprocessor Ada toolset is used to generate code for the scalar processor, and a VCP toolset is used for generating microcode for the VCP. The runtime environment provides the basic operating system (OS) functions such as multitasking, interrupt handling, Ada exception handling, timer management, and virtual memory management. Additionally, the URDA runtime environment includes support for initialization, VCP interface, and interprocessor messaging. Programs for either the R4000 or the VCP can be downloaded independently to the target processors for execution and debug or can be downloaded, executed, and debugged as cooperating programs in a multiprocessor system.

2.1 VCP Programming[1,3]

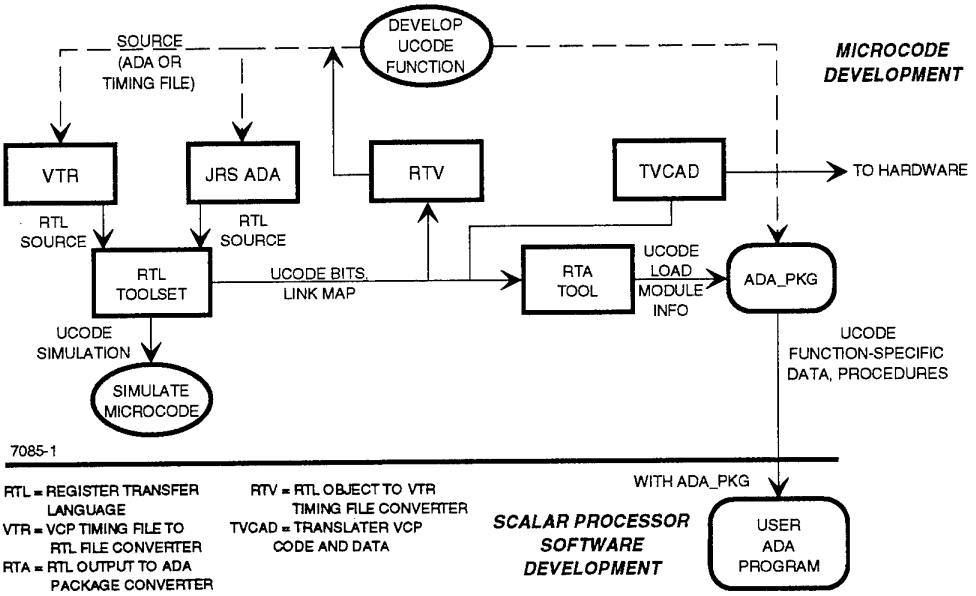
The VCP tool suite (Figure 4) is centered around the TI Register Transfer Language (RTL) toolset, which provides the core assembler, linker, simulator, and bit generation capabilities. Source RTL programs for the VCP can be written directly or, with the aid of a VCP-timing-file-to-RTL (VTR)

TABLE 1. VCP PERFORMANCE COMPARISON

Algorithm	VCP (ms)	TMS320C40 (ms)	Intel i860 (ms)
Complex fast Fourier transform (FFT), radix 2, 1024 points	0.23	1.55	0.74
Vector inverse, 1024 points	0.08	0.36	0.06
Vector multiply and add, 1024 points	0.01	0.05	0.12
Convolution, 128 × 128 array, 5 × 5	2.5	25.4*	13.1
3 × 3	0.7	13.5*	4.6
Matrix multiple 128 × 128	21.8	110.6*	77.2
Vector square, 1024 points	0.01*	0.05*	0.06
Histogram, 1024 points, 8-bit data	0.03*	0.35*	0.50

*Estimated timings

- AUTOMATES INCLUSION OF MICROCODE RELATED INFORMATION REQUIRED BY SCALAR PROCESSOR ADA PROGRAM
- PROVIDES PROCEDURE CALL INTERFACE FROM SCALAR PROCESSOR ADA TO MICROCODE



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Figure 4. Ada Interface to Microcode

two-dimensional programming utility or, with the aid of an Ada-to-microcode compilation system. VCP object files can be reverse assembled into two-dimensional source code using an RTL-object-to-VTR (RTV) or can be converted to Ada packages for interfacing to R4000 Ada programs using RTL-object-to-Ada (RTA). Each VCP programming tool is described in more detail below.

1. Ada—The JRS Research Laboratories Inc. (JRS) Ada compilation system is VAX-hosted and allows writing VCP programs in Ada, testing the Ada implementation using the VAX Ada debugger, and compiling the Ada to produce VCP microcode in the form of a source RTL program. The compiler supports all VCP hardware features, including multiple arithmetic units and multiple address generators. Built-in functions have been implemented to allow the Ada programmer to use specialized VCP hardware features such as window addressing, bit reverse addressing, and special ALU and multiplier opcodes. As a result, the Ada programmer can write very stylized code, which typically will result in more efficient microcode. Average execution time ratios between compiler generated microcode and hand-generated microcode have proven to be 2.2 for stylized Ada and 5.0 for unstylized Ada.

2. RTL—The RTL tools are also VAX-hosted and allow for complete development- and instruction-level simulation of the VCP with its associated memory. The RTL tools let system architects and designers define a custom programming language, simulation environment, and bit generation utilities for any programmable part, not just the VCP.

3. VTR—The VCP-timing-file-to-RTL file converter is a VAX-hosted tool that simplifies the generation of handwritten VCP microcode by providing the VCP microprogrammer with a bird's-eye view of the two-dimensional code being developed. It also allows VCP code to be written using shorter mnemonics than those supported by the RTL toolset. These two things combined will result in more efficient hand-generated VCP microcode.

4. RTV—The RTL-object-to-VTR source translation utility executes on the IBM PC in interactive or command line mode and disassembles VCP object files to produce two-dimensional VCP source code files. Information about the number of loops, length of each loop, and efficiency of each VCP part within each loop is written to the bottom of each file. This utility was designed to analyze VCP microcode generated by the JRS Ada compiler. It also has been used to provide a two-dimensional view of hand-generated microcode that was not generated using VTR.

5. RTA—The RTL-object-to-Ada package translation utility is VAX-hosted and reads VCP object files, VCP link map files, and user preference information to generate an Ada package

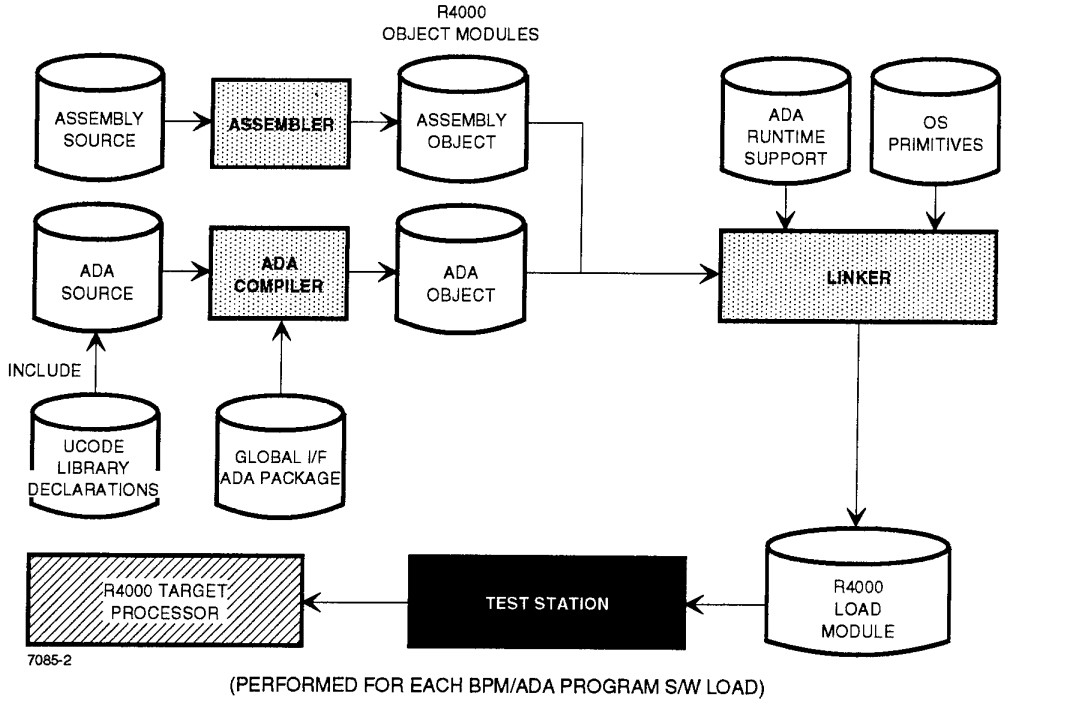


Figure 5. R4000 Code Development Flow

for interfacing VCP applications to R4000 Ada. RTA uses the link map file, microcode slice file, and a modified simulation control file output by the VCP RTL toolset. RTA reads the modified simulation control file and link map file to generate an Ada record type representing the CPL chain. The VCP link map provides CPL names and link addresses while the simulation control file provides CPL execution order, which dictates CPL chain record structure. Load module information is extracted from the VCP link map and translated into Ada load module constants, including start address and length of each load module and of each CPL within each load module.

6. TVCAD—The translate VCP code and data utility converts VCP object files, CPL chain, and data information into one file that can be downloaded into the hardware. The download file contains three columns of information including address, data to be written at the specified address, and a comment pertaining to the type of data being written.

2.2 Ada Programming[1,3]

Programming for the URDA ADM processor is based on a uniprocessor programming paradigm with either shared memory accesses or message passing providing the inter-BPM communications. Applications targeted to the URDA architecture are statically partitioned into the software units allocated to each logical BPM. Each partition allocated to the scalar processor on a BPM is developed using a traditional uniprocessor Ada toolset, as shown in Figure 5. Using the RTA tool described previously, R4000 code used to initialize data structures for VCP routines can be generated automatically for inclusion in the scalar processor program. Additionally, any data packages that are global to the BPMs within an URDA processor may be "with'd" into the application program for each of the BPMs. Then, standard compilations/assemblies generate object modules that can be linked with the necessary runtime and OS primitives to form a load module.

Likewise, the VCP toolset generates microcode for execution on the VCP. The microcode can be included as data within the scalar processor program load module or may be loaded independently under user control to the appropriate BPM local memory. From the Ada program on the scalar processor, the VCP can be invoked using either blocking or nonblocking remote procedure calls. Communications between applications on different BPMs are supported through shared memory access or through message passing primitives provided by the runtime environment.

2.3 Runtime Environment[1,3]

The TI URDA ADM runtime environment is based on a TI-produced Ada runtime and executive developed on the TI Aladdin program to support embedded, real-time applications targeted to the R4000 scalar processor. In addition to a standard Ada runtime, the TI URDA runtime supports uniprocessor counting semaphores, dynamic modification of task priorities, additional timer support (delay until a future time, read and set system time), uniprocessor locks, and physical/virtual memory management routines. The physical/virtual memory management routines allow a virtual address/window to be assigned dynamically to a physical address and also allow for the physical address associated with a virtual address to be returned. Support also is included in the runtime environment for BIT, application software interfaces to the VCP, and inter-BPM messaging. The BIT capability includes processor startup, system initiated, and periodic BIT functions, which are used for fault detection and isolation.

The VCP interface function manages the invocation of the microcode from the Ada program executing on the scalar processor. To the scalar processor Ada programmer, the interface appears as either blocking or nonblocking remote procedure calls. This allows for either polling or event-driven synchronization between the R4000 and the VCP. The interface also provides access to the VCP status and configuration registers.

The messaging function provides task-to-task communications, where tasks send messages to "message queues" that may be assigned or shared by different tasks. The messaging function is an R4000 target/ASB bus implementation of the TI Common Network Operating System. Extensions to the Aladdin messaging function comprehend inter-ADM communications across the PiBus using the store and forward memory of the PIM. Messages may be sent logically, without requiring the sender to know who or where the destination is. Application tasks may request messages from a queue in either a blocked or nonblocked mode. The blocked receive mode allows the application task to be blocked until either a message is received or a specified time-out occurs. The nonblocked receive mode allows the requesting task to poll for receipt of a message. The store and forward memory on the PIM allows PiBus messages to be received into the PIM memory. Interrupts notify the scalar processors that a message has been received into the store and forward memory and is available for processing. Messages targeted for transfer across the PiBus are sent to the PIM memory first; then a PiBus transfer is initiated by the scalar processor to send the message from PIM memory to the appropriate PiBus receiving node. Both read and write PiBus transfers can be initiated, allowing data to be sent from or fetched into the initiating ADM.

2.4 Integration and Test Support[1,3]

Extensive integration and test support is provided for the URDA processor. Test and debug tools provide debug support at several levels. Support is provided for system-level functions, BPM debug, VCP debug, and scalar processor debug support.

System-level functions include utilities for downloading VCP and R4000 programs, as well as supporting software and hardware test and debug. The BPM debugger provides BPM-level control and supports VCP test and integration. The BPM debugger provides access to local memory and allows user access to the ASB and the IOBUS from the BPM under debug control. Breakpoint management also is provided at the BPM level. VCP instruction execution, crossbar processor or memory port transactions, and ASB or IOBUS activity can be defined as events to be detected. VCP operation then can be halted upon detection of breakpoint conditions. The VCP debugger allows the user to halt VCP execution for stepping through CPL execution at the instruction level or the CPL level (i.e., clock by clock or on CPL boundaries). While in a VCP halt state, access is provided for inspection and modification of internal VCP register values. The SP debugger is based on the Mips R3000 debug monitor. Debug monitor code executes on the target, providing program execution control, access to memory and variables, and breakpoint management.

3. PACKAGING TECHNOLOGY

The TI URDA module packaging concept is shown in Figure 6. TI's concept incorporates a silicon-on-silicon technology MCM mounted to a liquid-flowthrough (LFT) core. The MCM is connected to a standard surface-mount PWB via compressible contact connectors. The module form-factor is compatible with the F22 common integrated processor (CIP) LFT module form factor.

3.1 LFT Module

The CIP LFT module form factor is a modification to the JIAWG SEM-E standard, extending the dimension between the module guide rails to provide a quick-fluid-disconnect (QFD) coupler on each side of the module. The couplers on the module connect to corresponding couplings in the chassis walls when the module is inserted into the chassis. The MCMs are mounted directly onto the LFT core on one side of the module, and the PWB (with standard surface-mounted components) is mounted on the other side of the core. Cutouts in the LFT core allow the compressible connectors to interconnect the MCMs to the PWB on the opposite side of the core. As shown in the figure, a serpentine path is provided through the module core underneath each MCM. A fin pattern

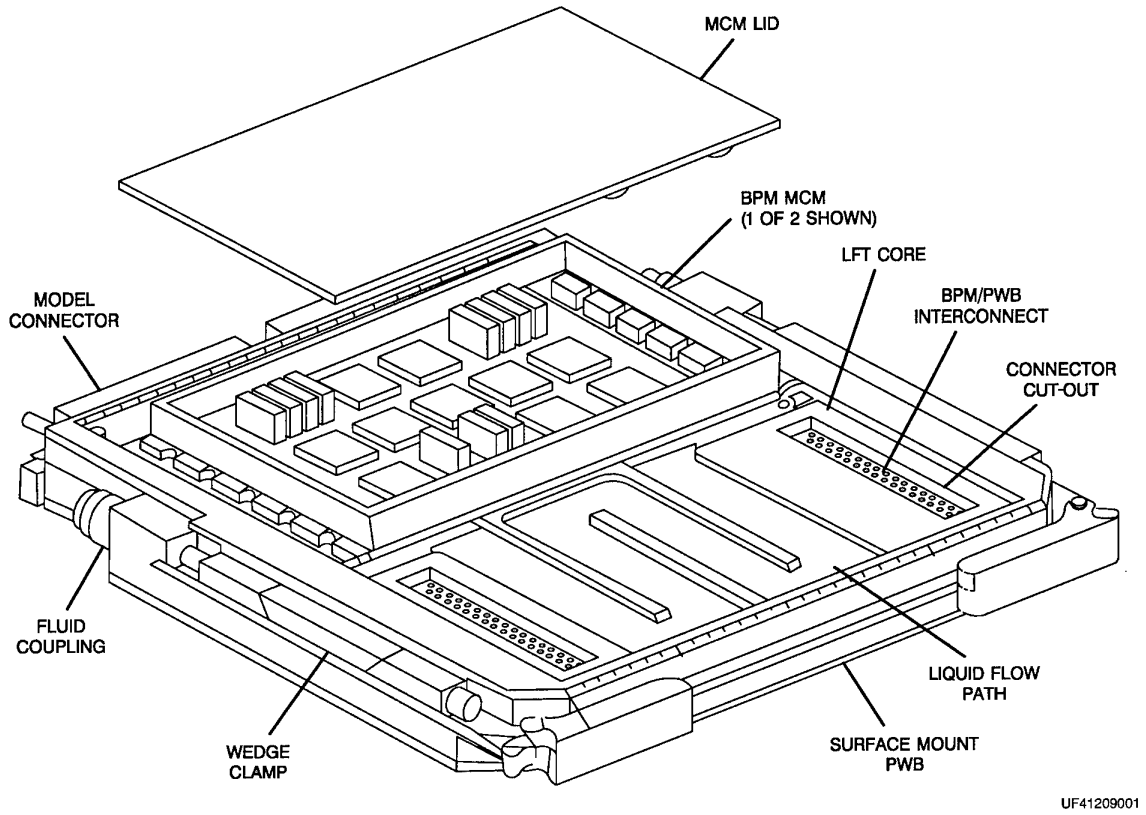


Figure 6. URDA SEM-E Module

in the flow path provides the heat exchange mechanism for transferring the heat from the module to the fluid. Fluid cannot flow directly across the module from side to side because of the cutouts in the core for connectors. Thus, the fluid path runs from the inlet QFD to a point between the connector cutouts for each MCM and then splits into two serpentine paths, one under each MCM. The separate paths then recombine between the MCMs on the exit side of the module and empty the fluid via the exit QFD.

A compressible interconnect provides a Z-axis connection between pads on the PWB backside surface and the bottom surface of the MCMs. The pad pattern is compatible with either a button contact or elastomeric connector approach. In either case, the PWB is mounted to the core with its pad pattern aligned with the core cutouts. Connectors are placed in each cutout and the MCMs then are bolt-mounted to the core. Alignment features on the core and the MCMs ensure proper pad-to-connector alignment. As the MCM mounting bolts are tightened, the connectors are compressed in the Z-axis, making contact between the pads on the PWB and the pads on the MCMs. Signal, signal shield, power, and ground connections are all provided from the backside PWB to the MCMs via the compressible connectors.

3.2 MCM Packaging

TI's URDA MCM packaging integrates flip-tape-automated bond (TAB) technology with TI's 3-D memory packaging technology (Figure 7) to mount the ICs to a silicon substrate. This approach mounts 10 large ASICs, three small ICs, 88 memory ICs, and several small passive components onto a 2.3-inch × 3.6-inch silicon substrate for an effective packaging density of approximately 1.8 (IC silicon area divided by substrate silicon area). The populated substrate resides inside a 5-inch × 2.7-inch ceramic package that is bolted directly to the LFT core.

As shown in Figure 7, the fabrication process flow includes substrate fabrication, TAB processing, and 3-D memory assembly. The substrate is fabricated with an iterative process that builds successive polyimide dielectric and metal routing layers on top of a silicon wafer. Power, ground, three signal

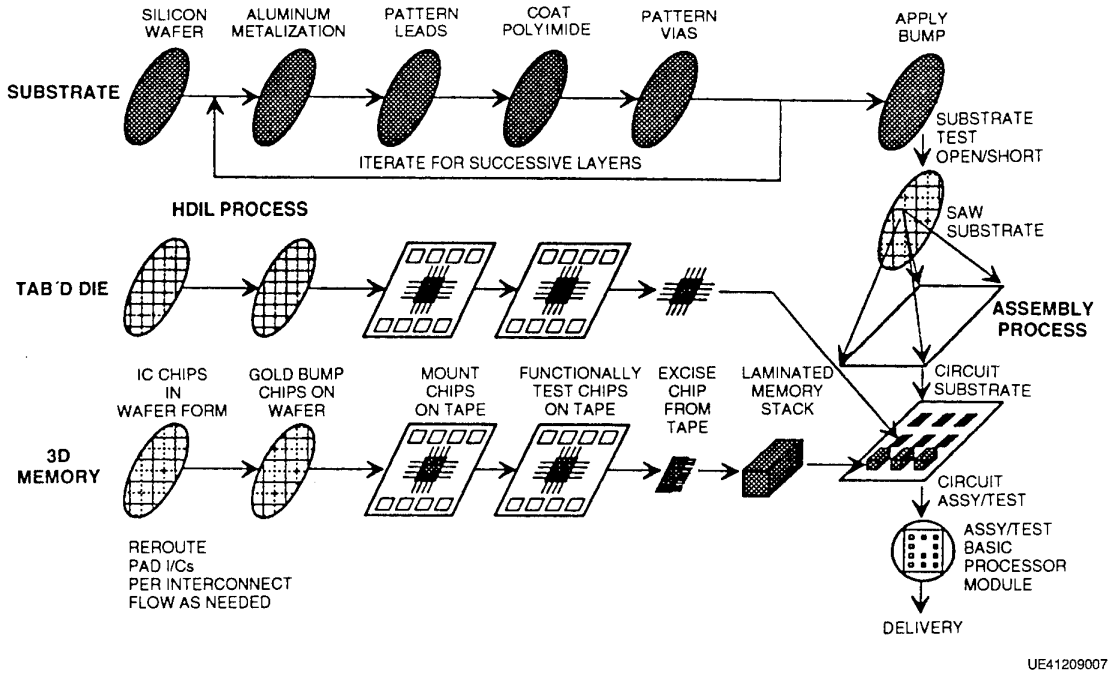


Figure 7. MCM Fabrication Process Flow

layers, and a top pad layer are built in this iterative process. The TAB process starts with devices in silicon wafer form and adds gold bumps to the pads on each IC. Bumped devices are sawed into individual die, and a TAB lead frame is bonded to the pads on each die. Each TAB'd device is tested and burned-in before assembly on the substrate. Tested TAB'd die are excised from the lead frame with 20-mil leads extending from the device for bonding to the pads on the substrate. The excised TAB'd die are "flipped" upside down and the leads bonded to gold-bumped pads on the substrate. The 3-D memory devices are essentially TAB'd devices that undergo two additional process steps. A reroute is performed on each device in wafer form to route the signals only along the "long" sides of the memory device. The TAB lead frame then is bonded to these rerouted leads, and the TAB'd memories are tested and burned-in the same as the other TAB'd devices. After excise, TAB'd memory devices are laminated into "cubes" with the signal leads aligned in a grid pattern on the "top" and "bottom" surfaces of the cubes. Leads on the "top" of the cube provide test points for each memory device. The leads on the "bottom" are soldered to pads on the substrate.

Figure 8 shows a schematic cross section of a flip-TAB device and 3-D memory cube. Thermal management for the flip-TAB devices is provided by the thermally conductive epoxy placed under each device. Heat from the memory devices is conducted through the leads soldered to the substrate. Thermal vias in the polyimide layers under the flip-TAB devices and underneath the memory TAB lead pads conduct the heat to the substrate.

4. CONCLUSIONS[1]

TI's URDA processor is ideally suited to advanced radar and signal processing applications. The TI URDA processor combines data processor, signal processor, memory, and system interface functions on a single SEM-E module. Advanced BiCMOS ICs, silicon-on-silicon packaging, and commercial RISC scalar processor technologies have provided the capability to implement a single SEM-E avionics card form-factor signal processor with 200-MIPS/800-MFLOPS throughput. The TI URDA processor's modularity, scalability, Ada programmability, high performance, and extensive software development and debug support environment provide a powerful, general-purpose processor for use in Department of Defense (DoD) embedded signal processing systems.

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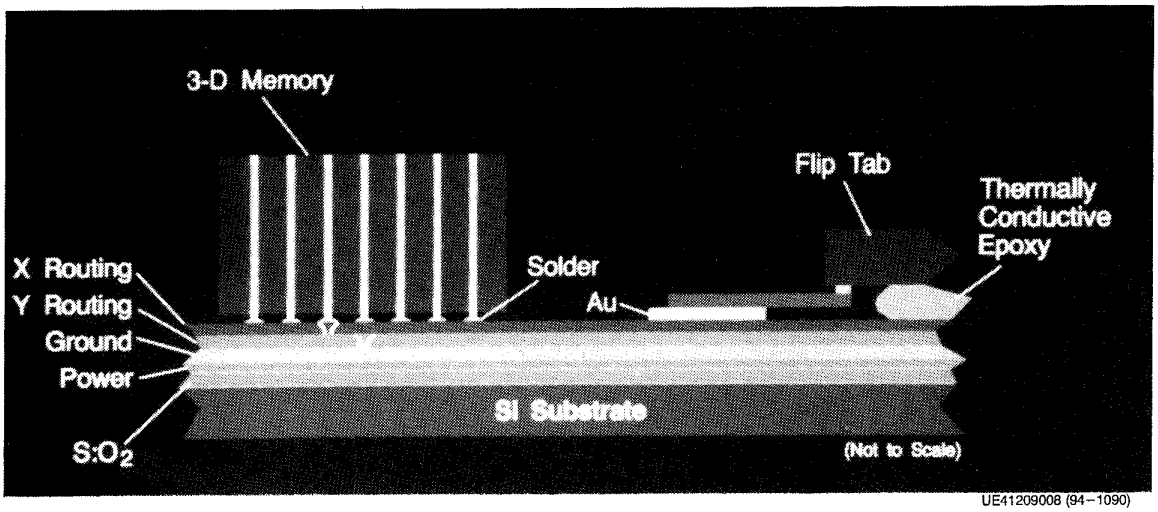


Figure 8. MCM Cross Section

DISCUSSION

Question: What is the power dissipation of the URDA module?

Answer: The nominal power dissipation is estimated to be on the order of 65 - 75 W. A worst case estimate could be in the range of 86 - 90 W.

Question: Where are the power supplies?

Answer: The power supplies are modular power regulators in a SEM-E form factor and are plugged into the same backplane as the SEM-E processor module.

Question: Will you have enough space to include the power supplies on a SEM-E module already full with URDA processors?

Answer: If the interface circuitry was also packaged in an MCM, there would be room for a power regulator on the interface side of the SEM-E module. There is not room on the side of the module with the basic processor modules. The current design does not have room for power regulators on the module.

Packaging the MAMA Module

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1. SUMMARY

The MAMA (Mixed Arithmetic, Multiprocessing Array) module is being developed to evaluate new packaging technologies and processing paradigms for advanced military processing systems. The architecture supports a tight mix of signal, data, and I/O processing at GFLOP throughput rates. It is fabricated using only commercial-of-the-shelf (COTS) chips and will provide a high level of durability. It's attributes are largely the result of two new interconnection and packaging technologies. Chip-in-board packaging is used to reduce local x-y communication delays and solder joints, while significantly improving board-level packaging density. A unique 3-D interconnection technology called a cross-over cell has been developed to reduce board-to-board communication delays, drive power, glue logic, and card-edge pin-outs. These technologies enables true 3-D structures that are form, fit and connector compatible with conventional line-replaceable modules. The module's design rational, packaging technology, and basic architecture will be presented in this paper.

Note: This work was sponsored in part by the Air Force's Wright Laboratories (AAAS-1) and Army Night Vision Labs under the Ultra-Reliable Digital Avionics (URDA) program F33615-92-R-1019.

2. INTRODUCTION

The MAMA module is one of several advanced technology demonstration models that are being developed under the URDA—a joint Army and Air Force program. The goal of this program is to demonstrate and evaluate technologies that could lead to more reliable and lower-cost military processors. The MAMA module was designed to efficiently execute computationally-complex algorithms requiring a mix of signal, data, and I/O processing.

The design requirements for the MAMA module were derived from a number of computationally complex processing algorithms. Temporal IRST, FLIR, automatic target recognition, electronic warfare, virtual reality simulators, and adaptive radar were the major performance drivers. Each of these applications require processing throughputs well in excess of a billion floating point operations per second (one GFLOP)—a result that was not unexpected. The surprising result was the mix of processing. Previous sensor processing streams have exhibited an orderly transition of sensor, signal, data, and symbolic processing, with distinct boundaries between each class of processing. However, many of the advanced algorithms exhibited a greater mix of processing classes. Data and symbolic processing in the form of heuristic pruning, cueing, and dynamic control is being used to keep sensor and signal processing tractable at even GFLOP levels. Functions such as situation assessment that have traditionally been pure data and symbolic processing applications now required signal processing to efficiently execute complex tracking and linear programming calculations. This tight coupling of different processing classes suggests that future processing modules will have to employ a several different classes of processing units within a hybrid multiprocessing architecture.

Cost was another major design driver. Our cost studies showed that the government may not be able to afford full-custom solutions for each studied applications. While the cost of personal computers has dropped dramatically over the last ten years, the cost of military processing systems has risen. This is largely due to the use of expensive custom hardware and software solutions. The military has a long history of developing its own CPUs, DSPs, interface protocols, physical form factors, operating systems, application support systems, and test equipment. This practice has been justified from the standpoint of reliability and performance density, but commercial systems have made major strides in both areas. It is clear that the military can no longer ignore the cost-savings potential of commercial hardware and software.

This realization has created a mounting pressure to use commercial-of-the-shelf (COTS) modules in future military systems. At first glance, the use COTS modules appears to be an attractive and cost-effective solution. Commercial CPU and DSP modules are now more powerful than many of the custom modules being developed for military systems. The performance/cost ratio of a COTS data processing module can be a hundred times greater than its military counterpart. Interface chips and protocols are expensive to develop and standardize, even in the commercial world. The potential cost benefits are even greater when one considers the availability of good low-cost support software and test equipment. However, there are some potential drawbacks with using COTS modules for many military applications, such as combat vehicles.

Few COTS modules are able to meet the configuration

management, form/fit factors, testability and reliability standards required for harsh military environments and combat vehicles. COTS manufacturers build modules for a highly-competitive and high-volume market. They cannot afford to provide strict configuration control and long-term support for a low-volume military market. Commercial connectors and modules form/fit standards are invariably different from military standards (e.g., VME vs. SEM-E) and repackaging can be expensive. The military uses its own interfaces and protocols, few of which are compatible with commercial CPUS and DSPs. Ruggedized commercial modules may be suitable for some land-based military applications, but it is unlikely that they will survive the severe environmental stresses encountered in a military helicopter, tank, or jet aircraft. These factors, coupled with practical problems with long-term support, security, and military standards cast doubt on the widespread applicability of commercial modules for military applications.

3. A PARTIAL COTS SOLUTION

These problems led the AT&T design team to consider using COTS components (chips) rather that assembled modules. This approach was arrived at by noting that much of the cost associated with developing a full-custom module was directly attributable to custom processing units (CPUs, DSPs) and interface chips. Special packaging and interconnection technology would allow the device to be packaged in the required form/fit factor and meet military specifications. This approach would be more costly that purchasing COTS modules, but much less expensive than a full custom design. There was the additional advantage that one can usually assemble a reasonable emulator of the target module using COTS modules, allowing the software developers to work concurrently with the hardware development.

Our proposed approach is to package and interconnect COTS devices in such a manner as to achieve a reliability and performance density on par with full custom module designs. Our biggest hurdle was to bring devices closer together without compromising reliability. It quickly became apparent that one could not use commercially packaged parts to achieve the desired reliability and performance density. Most COTS devices are available only in plastic quad flat-pack or pin-grid array packages. Plastic packaging is a poor thermal conductor and does not adequately protect the devices in harsh environments. Pin-grid arrays have large stack profiles and often compromise military module pitch requirements. As a result, AT&T has developed several new interconnection and packaging solutions.

4. THE PACKAGING APPROACH

Packaging and interconnection designers have to deal with two conflicting design goals. They need to move devices closer together to reduce signal delays and improve packing density. At the same time, they must minimize thermal problems related to this denser packaging. One solution that address both problems is chip-in-board (CIB) technology. CIB technology effectively eliminates device level packaging, reducing board area and interconnection delays in the circuit board plane. Basically, bare chips or multichip substrates are mounted into cavities cut into the circuit board. These devices are wire or tab bonded, and sealed with metal lids. This packaging approach reduces the signal path length and improves signal integrity. This structure is more reliable as a result of eliminating a two levels of connections and a major thermal barrier. The stack profile of the packaged board is less than half that of a conventional surface mount board.

This CIB circuit board is formed from a stack of low-temperature, cofired ceramic sheets. Each sheet in the stack starts a thin, flexible ceramic material called green tape. Cavities and vias are easily cut or punched while this material is in its green state. Signal traces and vias are then added to each sheet by screening on gold metallization. This assembled stack is fired under controlled pressure and temperature, resulting in a hard ceramic board. Yields are high since each sheet in the stack is inspected prior to firing. Devices and multichip assemblies are attached into the cavities with a thermal conductive adhesive. Electrical connections are made with either wire or coplaner tab bonding. The cavities are sealed with a conventional metal lid after board-level testing. AT&T is also experimenting with a ceramic cover board that provides an excellent thermal expansion match to the circuit board and another level of board interconnects.

Figure 1 shows a partial cross-section of a typical chip-in-board cavity. Our first test board contained eight 2.5 x 2 cm cavities in a 170 square centimeter board. The total stack thickness of the sealed board assembly was approximately 4 mm. This packaging approach yields a number of reliability benefits. The number of physical interconnections is reduced by a factor of two since the chip or multichip assembly is now bonded directly in the circuit board. Signal integrity is improved by eliminating a level of packaging capacitance. The thermal resistance between the devices and the cooling medium is reduced by eliminating a ceramic package. The higher cost of the circuit boards will be offset by the elimination of device-level packaging costs.

Although chip-in-board techniques significantly reduce interconnect delays in the x-y plane, any significant improvement in system level performance will require a complimentary improvement in board-to-board (z-axis) interconnections. Z-axis interconnections are typically implemented by way of a backplane or soldered flex-circuit crossovers that wrap around the edge of the

frame. Both techniques require an long, indirect path to implement z-axis interconnects. They place restrictions on the device placement, interconnect density, and use valuable board real estate.

AT&T has developed a new Z-axis interconnection technology called the crossover cell. Connections are made between neighboring circuit boards through special elastomeric buttons that conduct only in the z-axis. Each silicone button consists of a dense matrix of uniformly spaced vertical conductors. Pressure contact connections are made when the button is compressed between pad sites located on the back side of two circuit boards (see figure 2). The connections are solder-less, compliant, and tightly sealed. Cells can be located anywhere on the backside of the board surface and therefore do not require valuable device real estate. Interconnect densities of up to 50 interconnections per square centimeter are readily achievable. The exact positioning of the buttons is not critical and a good connection requires only that the respective board pads have a seventy-five percent alignment. Pad dimensions can be adjusted to accommodate different alignment tolerances, eliminating the chance of a short circuit.

The first prototype module contained 28 cells distributed over 170 square centimeters of board area. Each cell had a 7 mm square footprint and provided 16 bonding pads. Two alignment pins were used to register the board faces for accurate pad-to-pad center alignment. A pad-to-pad alignment accuracy of less than a tenth of a millimeter can be achieved with this technique. The most critical aspect of this assembly is the selection of proper bonding materials and procedures for attaching the circuit boards.

The techniques described above have successfully undergone preliminary electrical and environmental tests.

5. THE MAMA MODULE

The MAMA module architecture consists of four basic functional blocks: I/O scheduler, data management, symbolic/data processing, and signal/image processing (see figure 3). The I/O scheduler block handles all external I/O control, task scheduling, and local fault management. This block controls high-level synchronization and data flow control among other processing functions. The data management block serves as a large elastic data buffer. Its function is to decouple task setup, breakdown, and execution, reducing the level of synchronization needed between functional blocks. The data management block also performs basic data manipulation functions such as packing, unpacking, sorting, scaling, reformatting, and reordering. These functions are performed on the data as it is moved between functional blocks. The data processing function operates on data structures containing numeric and categorical information (symbolic processing). These are the structures requiring sorting, searching, and decision logic normally associated with situation awareness and decision support applications. The signal processing function operates on regular numeric structures such as vectors, arrays, and matrices. These operations include Fourier transforms, cross and dot products, digital filters, complex demodulation, and beamforming.

The MAMA FE supports a concurrent execution paradigm where data for task N+1 is setup (input) while task N is being processed and task N-1 is being broken down (output). Specifically, the I/O control block can input or output a block of data while the data management block is formatting data setup for the next executable task. Concurrently, the data and signal processing blocks can operate on data setup previously by the data management subsystem. The setup operations, as well as the task execution are scheduled by the I/O control subsystem.

The flow of data and control information is often a major performance bottleneck. The MAMA architecture has been carefully designed to minimize internal and external bus conflicts and latencies. External control and data movement is accomplished over four separate busses: the tactical control bus, the test and maintenance bus, the user control bus, and the high-speed data bus.

The Tactical Computer Interface (TCI) is used to communicate command and control data with other functional elements and sensors. This interface function is characterized by the movement of small messages or data blocks that must be delivered with high integrity and low latency. It supports functions such as system-level task management and synchronization, module ID assignment, power-up, power down interrupt, warm start, and secure data flush. Reliability and performance analysis require this bus to be dual-redundant and support a sustainable, aggregate I/O transfer rate of not less than 0.25 Mbytes/sec (measured using 32-bit data blocks).

The Test and Maintenance Interface (TMI) is used to support of testing and to communicate fault management (health status, fault isolation, reconfiguration, fault recovery) data between the MAMA module and other computers/sensors in the test bed. Test data is characterized by the random transfer of small messages or data blocks. Therefore, the TMI will designed to support a sustainable I/O bandwidth of at least 0.1 Mbytes/sec.

The High-speed Data Interface (HDI) is used to move large blocks of sensor and output data between the MAMA module and other modules/sensors in the system. This interface will support a sustained I/O

bandwidth of at least 40 Mbytes/sec. This requirement was driven by the sensor data rate required to support future targeting FLIR and adaptive radar applications.

The User Control Interface (UCI) is required only for prototype testing and evaluation. It is used to remotely control the MAMA functions during test and debug. Its main functions are: (1) initialization and termination of software routines, (2) hard and soft Reset, (3) off-line diagnostics operation, and (4) execution modes. Data movement is not time-critical and characterized by a wide range of block sizes. This interface will support a sustained, aggregate I/O bandwidth of at least 0.25 Mbytes/sec.

The data channel is used to route information among the various functional blocks. It contains a number of data bridges that allows sections of the data channel to be used concurrently. For example, data can be routed from a sensor to data management block while information is also be moved into the signal processing block. This design can effectively double the instantaneous bandwidth. The data channel bandwidth has been chosen to match the bandwidth of the external high-speed data bus

Command and control messages must be transmitted and received in a few tens of clock cycles. The MAMA design provides a physically separate command and status path is provided to communicate internal high-priority (commands and machine status) messages. It can operate concurrently and independently of in external or data channel transfer.

6. PHYSICAL IMPLEMENTATION

The MAMA module is physically implemented as a double SEM-E module. It consists of two frame assemblies (SEM-E modules) that are pinned together and secured in the rack by opposing wedge-locks. Each frame assembly is a structural frame sandwiched between two ceramic boards. Cross-over buttons implement the connection between these two boards. Z-axis connections between the frame assemblies are made with a high-profile, elastomeric strips. The module conforms to SEM-E standards and requires no special maintenance or insertion procedures. The structural frame can be designed to use conventional, edge-conduction, air-flow-through, or liquid flow-through techniques for thermal management.

Figure 4 shows the basic architecture and its physical mapping onto four circuit boards. The first frame assembly consists of two identical signal processing circuit boards. These boards are ceramic and incorporate both chip-in-board and crossover cell technology. Each board contains cavities for the three DSP MCMs, a control DSP, clocks, local memory, and an FPGA for the glue logic. The two boards provide a peak signal processing throughput of 0.8 Gflops and 3 Gops. Each DSPs has its own local memory and six DMA channels. These DSPs are interconnected in a toroidal network consisting of 36 point-to-point DMA channels. The board-to-board connections for the system buses and DMA channels are made with multiple z-axis crossover cells.

The I/O and Data processor boards form the second frame assembly. The I/O board contains a 30 MIP RISC processor and local memory for control and scheduling. Three chips provide high-speed data, tactical control, and test/maintenance interfaces. The data processor board contains a 60 MIP RISC processor and local memory, plus two large global memories. Z-axis crossover cells provide the system bus interconnects.

Although the system and control busses spans all four boards, the maximum path length is less than 10 centimeters. The electrical and physical design of this unique module has been completed and assembly will begin in a few months. Preliminary electrical and environmental tests on test coupons and prototype structural frames have demonstrated the reliability of this structure.

7. POTENTIAL BENEFITS

During the course of this program, we have identified numerous cost and development benefits with using commercially available devices. Device documentation was exceptionally complete and accurate. There have been no proprietary agreement problems, and most questions were readily answered over the telephone. Schematics, behavioral, and logic models were available in standard formats and evaluation parts were frequently provided at little or no cost. Emulators, simulators, test vectors, test problems, and monitoring equipment were available for test and debug. There were multiple vendors for most parts, eliminating the second sourcing problems. However, the most significant cost benefits appears to be in the software support arena. Compilers, cross-compilers, linkers, loaders, and debuggers are available from multiple sources. It was even possible to purchase a host development system based on the same processing units as our target design. The support software was stable and relatively bug-free. It was interesting to note that Ada compilers and support systems tended to cost five to ten times more than an equivalent C++ software system. This price difference shows the dramatic cost savings afforded by large volume sales. Still, an COTS Ada support system cost only a fraction of what it would cost to develop this software from scratch. Vendor support has been strong and custom code modifications could be obtained for a reasonable cost. We have also noted a higher level of software commonalty and portability, due largely to emerging commercial standards. This portability was particularly apparent for open real-time operating systems.

8. CONCLUSIONS

The experience to date suggests that it is possible to build a cost-effective and reliable module that can meet future military requirements. The key is to marry commercially available CPUs and DSPs with right packaging and interconnection technologies. Simulations show that the MAMA module will have a performance density on par with many custom 3-D structures. Furthermore, the MAMA module conforms to standard SEM-E form-fit factors and require no special tools or maintenance. Apart from a reduction in hardware procurement costs, there are significant cost benefits to be accrued through the use of commercially available real-time operating systems and support software packages. It is unknown what the COTS cost-saving will be for integration and field support, but preliminary studies are promising.

9. ACKNOWLEDGMENTS

The work presented in this paper represents the collective efforts of AT&T's AAAPT and URDA project teams. The author also wishes to acknowledge the contributions of the AAAS-1 branch of Wright Laboratories and the Army's Night Vision Laboratories. Much of the research and material described in this paper was funded under their programs. I am particularly indebted to John Ostgaard, Greg Rubertus, Paul Brewer, Lynda Graceffo, Kristina Le, and Reed Morgan for their continuing support.

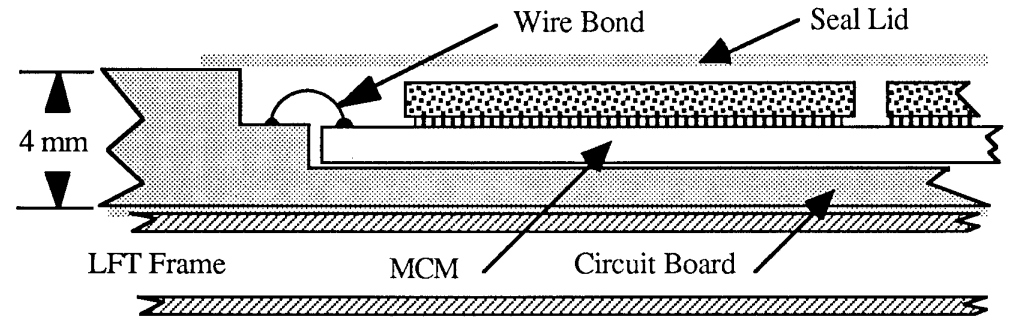


Figure 1 - Chip-in-Board Packaging

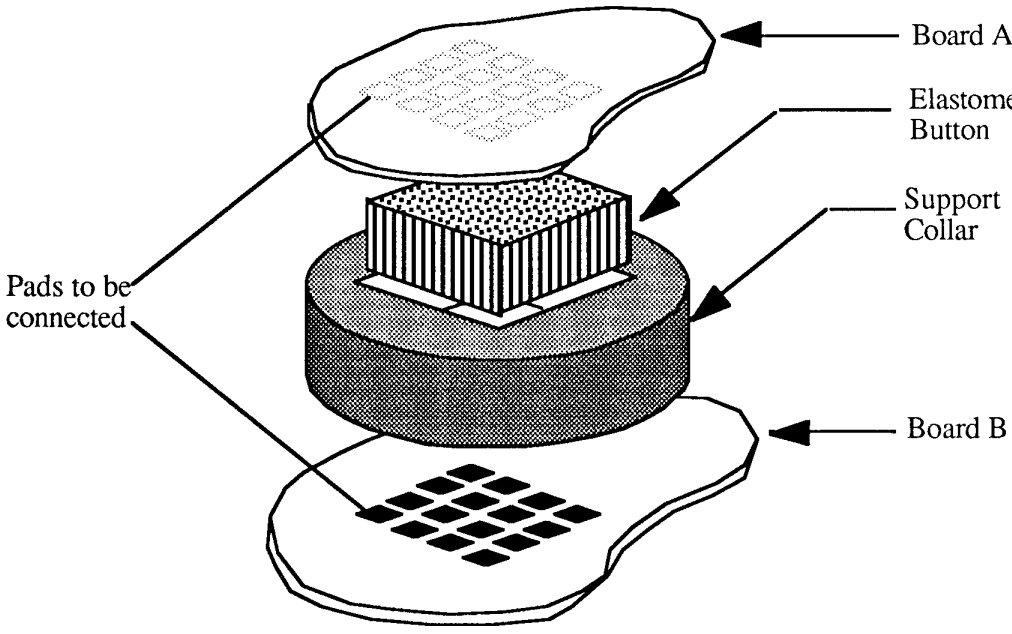


Figure 2 - The Z-axis Crossover Cell

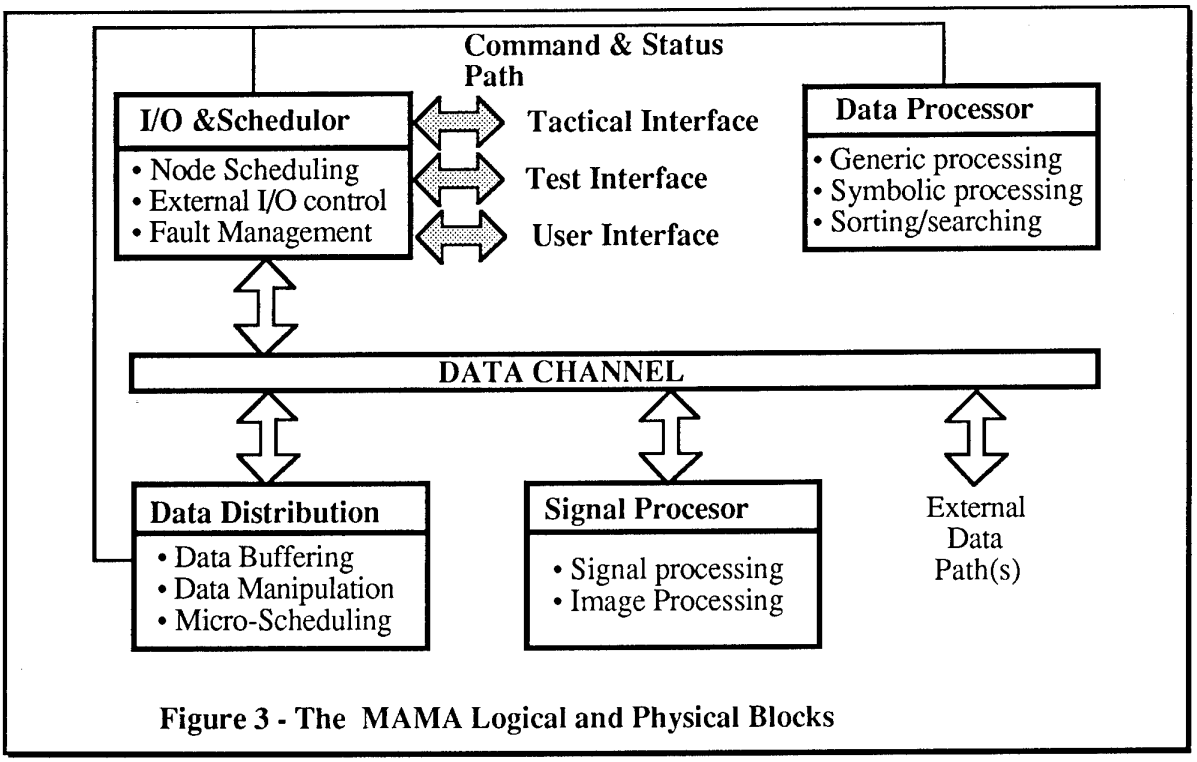


Figure 3 - The MAMA Logical and Physical Blocks

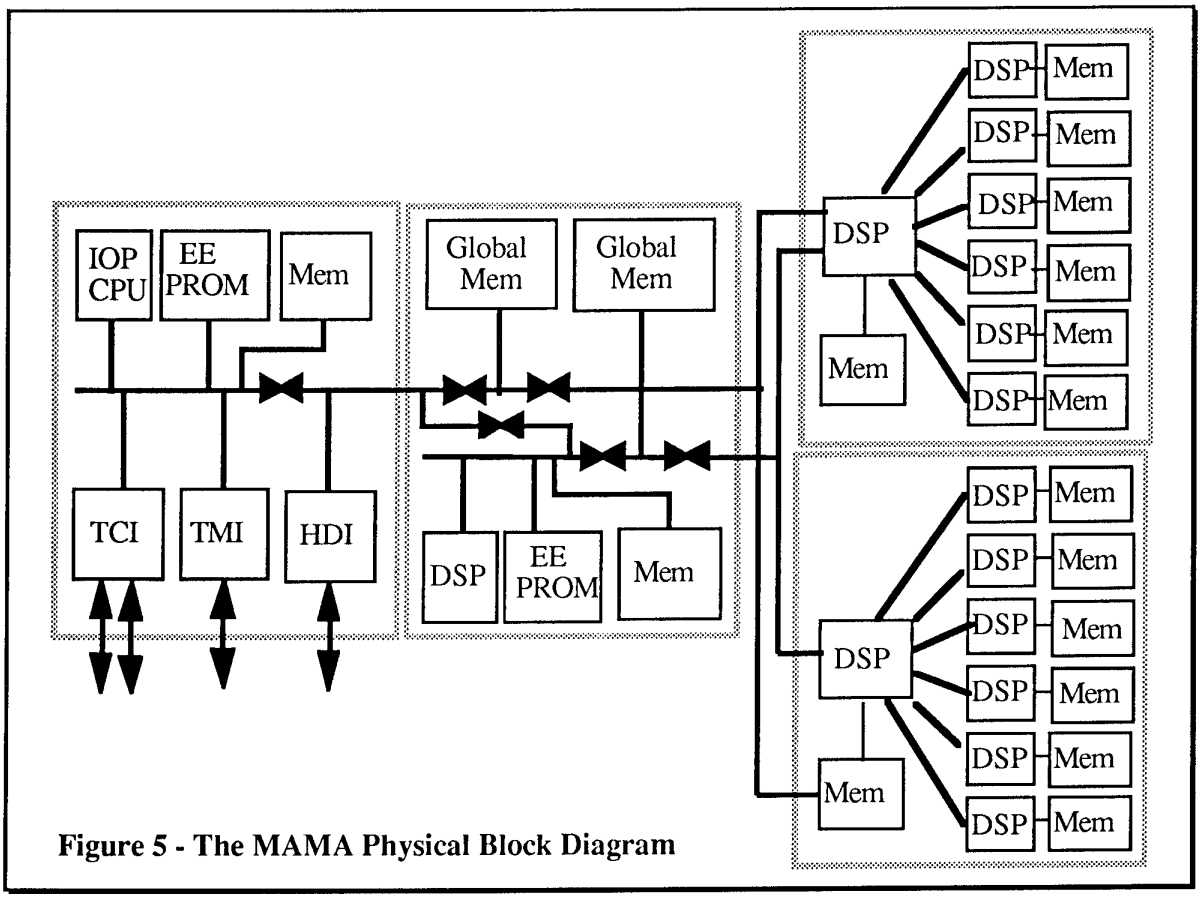


Figure 5 - The MAMA Physical Block Diagram

DISCUSSION

Question: How is hermetic sealing realized when using ceramic lid on ceramic substrate?

Answer: The ceramic cover is an experiment to explore the possibility of incorporating wiring (and possibly a second level of electronics) in the cover seal. We do not have any test data on the level of hermetic sealing.

Question: How to handle with COTS products the military requirement of a storage temperature range of -55 to +125 °C?

Answer: We recognize this as a potential problem and that is why we have elected to use the chip-in-board packaging. It essentially duplicates a ceramic hermetic package – the standard for military device packaging.

Question: Does your work have an impact on long term support of COTS components?

Answer: Yes; it will impact long-term support in two ways. First, the functional design focuses on reducing both the number of unique types of modules needed to populate a system. This allows a more economical sparing and long-term storage. More importantly, commercial CPU, DSP and bus interface chip vendors strive to maintain upward compatibility with the existing software base. This may make it economical (and viable) to upgrade systems on a shorter life-cycle (every five to eight years vs. ten to fifteen).

Question: Considering that the devices used (C-40s) are commercial, the level of integration, and the fact that the module is sealed, what test methodology is used, especially self-test to support maintainability after assembly?

Answer: We are still exploring the best assembly and test procedures, but our objective is a test-before-you-seal strategy. The prototype design has a number of test buses and test points. Several jigs have been assembled to test the MCMs before they are mounted into the board cavities. Certainly, the board structure will be tested before the final cover seals are attached.

Question: What will be the maintainability of the proposed MAMA module, if any, and with what cost (relative)?

Answer: Our goal is to make modules that are highly reliable and cost effective, so that the occasional failed module can be discarded.

Question: What is the status of qualification, especially for vibration, for this technique?

Answer: This module was designed under a technology demonstration program (URDA). The various components (chip-in-board, z-axis crossover cells, etc.) have undergone a number of environmental and electrical tests (including shock and vibration). Funding for the project was canceled before a fully assembled unit could be tested.

The Demise of Plastic Encapsulated Microcircuit Myths

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Summary

Production of microelectronic devices encapsulated in solid, molded plastic packages has rapidly increased since the early 1980s. Today, millions of plastic-encapsulated devices are produced daily. On the other hand, only a few million hermetic (cavity) packages (Figure 1) are produced per year. Reasons for the increased use of plastic-encapsulated packages include cost, availability, size, weight, quality, and reliability. Markets taking advantage of this technology range from computers and telecommunications to automotive uses. Yet, several industries, the military in particular, will not accept such devices. One reason for this reluctance to use the best available commercial parts is a perceived risk of poor reliability, derived from antiquated military specifications, standards, and handbooks; other common justifications cite differing environments; inadequate screens; inadequate test data, and required government audits of suppliers' processes.

This paper describes failure mechanisms associated with plastic encapsulation and their elimination. It provides data indicating the relative reliability of cavity and solid-encapsulated packaging, and presents possible approaches to assuring quality and reliability in the procuring and applying this successful commercial technology.

1. Introduction

Plastic-encapsulated microcircuits (PEMs) have been used primarily in commercial, industrial, automotive, and telecommunications electronics. Consequently, they have a large manufacturing base. With their major advantages in cost, size, weight; performance; and near-instant availability, plastic packages have attracted widespread attention for government and military applications. Although this is a major opportunity for PEMs, they have met formidable challenges in adapting to the high-reliability demands of these markets. While the major impediment to PEM application has been a perception of lower reliability, problems also arise as a result of the military's small procurement and production volumes, the predominance of manual package-assembly operations used by military suppliers, and the defense department's outdated standards and handbooks.

Some of the first semiconductor devices were encapsulated in plastic. These early devices used molding compounds plagued by thermal intermittence problems.[1] Because of the difference in the coefficients of thermal expansion (CTE) of the bond wires and the encapsulant, these devices exhibited open-circuit failures at the bond pads at temperatures above ~100°C. As temperatures decreased, compressive forces restored the contact of wire to bond pad. Moisture-induced failures, like corrosion, cracking, fracture and interfacial delamination, were also significant [2]. This problem has been largely resolved; testing at 85°C/85% relative humidity in 1974 produced 25% cumulative failures at 1,000 hours, compared with 0.1 in 1990[3]. The nearly exclusive use of hermetically sealed microcircuits in military, aerospace, and other high-reliability, high-criticality applications is a direct result of the problems associated with early plastic packaging.

The decade of the 1980s brought revolutionary changes in electronics technology in general, and in plastic packaging in particular. Earlier plastic- encapsulated transistors and diodes were fabricated by dispensing a small amount of room-temperature vulcanizing silicone or flexible epoxy material over the die and bond wires (glob-topping). Later, various molding techniques were attempted, including transfer, injection, and potting. Hundreds of variations in epoxies, silicones, and phonemics variations were evaluated for cost, performance, implementation, shelf life, repeatability, flammability, and reliability. Also evaluated were various additives for heat removal, adhesion, viscosity, mold release, flame retardation, and appearance. Protecting the die surface prior to molding by coating it with silicone elastomers, varnish, or spun-on glass (SOG) was a popular procedure. To reduce voiding between encapsulant and package leads, silicone resin was forced into these voids under a vacuum, a process known as "back filling."

The progressive improvement in plastic packaging integrity has been effected by improved materials, increased plastic purity, high-quality device passivation, improved lead frame designs, and manufacturers' quality programs. In general, the failure rate of plastic packages has decreased from about 100 failures per million device hours in 1978 to about 0.05 per million device hours in 1990[4]. Hermetic cavity packaging does not appear to have kept up with these advanced requirements in either performance or cost, as is obvious from the curves in Figure 2; worldwide sales of commercial microcircuits in 1995 are projected to be $100B. Military sales projections are down to $1.6B, a decrease to 1.5% of the total market share from a high of 16% in 1975.

2. Advantages of Plastic Packaging

2.1 Performance

A plastic package has advantages of light weight and small size, compared with its ceramic counterpart; commercial plastic packages generally weigh about half as much as ceramic packages. A 14-lead plastic dual in-line package (DIP), for example, weighs about one gram, versus two grams for a 14-lead ceramic DIP. Although there is little difference in size between plastic and ceramic DIPs, smaller configurations, such as small-outline packages (SOPs) are only available in plastic, because their size provides higher packing density and shorter propagation delays. At the printed circuit board level, the use of SOPs allows smaller, fewer, and higher-performing circuit boards. Figure 3 illustrates the impact plastic encapsulation is having on microcircuit assembly and packaging. Today, 72% of ICs are produced by surface-mount technology (SMT)—non-cavity assemblies. With the introduction of ball-grid arrays (BGAs), the percentage of SMT packages is projected to increase significantly.

2.2 Cost

The cost of a packaged electronic part is determined by several major factors: die, package, volume, size, assembly and assembly yield, screening, pre-burn-in and its yield, burn-in, final test and its yield, and the specified qualification test. Because more than 90% of the IC market is plastic-packaged, cost has been lowered by

automated volume manufacturing and low off-shore labor expenses, hermetic packages are usually fabricated using more expensive materials and labor-intensive manual manufacturing processes (JAN military requirements specify on-shore manufacturing). Moreover, there is little cost difference between plastic surface-mount components and plastic DIPs, whereas ceramic surface-mount components are more expensive than ceramic DIPs. Thomson - CSF reports a 45% purchase cost reduction for each of twelve printed circuit boards (PCBs) in a manpack transceiver application implemented with PEMs rather than ceramic components [5].

It may be argued that hermetically packaged ICs may cost up to ten times more than plastic-packaged ICs because of the rigorous testing and screening required by the user for hermetic parts[6]. However, ELDEC[7] estimated that plastic ICs cost 12% less than their hermetic counterparts when both types were screened to customer requirements.

High yields and low assembly costs are achieved with plastic-packaged parts because they lend themselves well to automatic assembly techniques, thereby eliminating manual handling and operator error. On the other hand, automated pick-and-place machines reportedly can crack hermetic seals or chip the package. Moreover, costs of PEMs become lower with a higher level of integration and higher pin-count devices, because of the high price of the die in relation to the total cost of the packaged device. While these benefits may not be realized for complex monolithic VLSIs, great cost advantages may accrue for complex package styles, such as multichip modules.

The price per part to the user will include the above costs, and a significant price adder for the military. This adder, a built-in fact for the military market, includes the cost of the supplier's military infrastructure, the absence of competition price will be what the market will bear; and a need for a favorable profit margin.

2.3 Availability

Plastic-encapsulated microcircuits are much more available than hermetic devices. First, because non-cavity plastic devices are assembled and packaged on continuous production lines, as opposed to the on-demand production of hermetic parts, acquisition lead times are significantly shorter and problems associated with the restart of a hermetic line are not encountered. Second, some parts are simply not available from major manufacturers in cavity form. Most designs are developed first as plastic-encapsulated microcircuits. Suppliers estimate that, at any given time, 30% more part functions are available in plastic than in ceramic. Hermetic packages are developed only in response to sufficient market interest, performance requirements, and cost benefits: the military, the major purchaser of hermetic parts, has become a small portion of the total electronics market. With the current technology transition toward SMTs, interest in ceramic devices has lagged in the market, making adaptation of plastic ICs to military applications more critical.

2.4 Reliability

The reliability gap between cavity-packaged devices and solid PEMs has decreased in the last decade. Figure 4 summarizes published improvements in plastic encapsulated microcircuit reliability since 1976[7]. Two major contributions to this trend are encapsulating materials and passivation. Modern encapsulating materials have low ionic impurities, good adhesion to other packaging materials, a high glass transition temperature, high thermal conductivity, and CTEs matched to both die and leadframe. Advances in passivation include better adhesion to the die, fewer pinholes or cracks, low ionic impurity, low moisture absorption, CTEs better matched to substrates, and the use of such techniques as spun-on glass.

Figure 5 presents comparative failure-rate data between 1978 and 1988 of plastic-encapsulated microelectronics and hermetically packaged devices from a commercial source[8]. The database for this figure is from first-year warranty information on commercial equipment operating primarily in ground-based applications (office, laboratory, and transportable equipment); these failure rates are for the same part (or part function) over time. As Figure 5 shows, during this period both types of packaged devices improved more than an order of magnitude in early-life failure rate. For PEMs, the current value for this type of reliability is ~ $0.02/10^6$ hours, definable or 20 FIT. However, it should be noted that the use environment is not precisely known for either type of device; this data cannot be isolated to the package without knowing the changes in die reliability during the period.

To compare common device types, Condra, et. al[9] tested the same mature custom bipolar IC in both plastic (commercial part) and hermetic ceramic DIP (military part) versions on twelve circuit-card assemblies. They ran 1,000 temperature cycles, from -55^0 to $+85^0$C, to compare the functional reliability of the two types of packages. No differences were observed in any of the twenty-six measured parametric values. They then added these parts to an untested group of about a hundred of the same devices, half plastic and half hermetic, in another set of circuit-card assemblies, along with an older discrete version of the card as a control. All these were subjected to 1,000 hrs. of 85^0C/85% relative humidity condition with 28 volts of intermittent bias (30m on, 30m off). The previously thermally cycled parts (both ceramic and plastic) could only be tested up to 650 hrs. before failing. Among the new group, no failures of either type of component were observed. Conservative lifetime estimates for both package types in avionic applications were well over thirteen years, even for combined severe testing.

The big question is why DoD isn't taking advantage of this superior technology and reaping the same benefits as the rest of the industry. The answer lies in history and tradition. In the 1960s, reliability and quality issues plagued the new electronic device called the integrated circuit. Government documents were subsequently generated to regulate ICs because military applications were the driver for these products. These documents included:

- 1962: MIL-STD-217, Military Handbook on Reliability Prediction of Electronic Equipment;
- 1963: MIL-STD-454 (Requirement 64-Microelectronic Devices), General Requirements for Electronic Equipment;
- 1963: MIL-STD-781, Reliability Testing for Engineering Development, Qualification and Production;
- 1965: MIL-STD-785, Reliability Program for Systems and Equipment Development and Production;
- 1968: MIL-STD-883, Test Methods and Procedures for Microelectronics;
- 1969: MIL-M-38510, General Specification for Microcircuits;

A decade later, the world market for military-approved microcircuits was well below the industrial/commercial demand for ICs. Current projections indicate the market for military and industrial hermetic devices will be only about 1% of the world production of microcircuits by 1995.

As did the integrated circuit, low-cost encapsulation processing required a period of learning and experimentation. By the early 1980s, the failure mechanisms that caused quality and reliability concerns had been researched and essentially reduced to background noise. Aluminum interconnect metallization corrosion was controlled by improvements in passivation composition and reduced defect density. Ionic contaminants on the die and in the encapsulant had been reduced to insignificant levels, eliminating bond-pad corrosion in field-use environments. Material and structural designs controlled thermal mismatch issues.

As technology advances, new failure mechanisms can evolve, but they are immediately addressed and controlled, as was the case with surface-mount technology delamination or "popcorning" resulting during assembly soldering from the vaporization of absorbed moisture in very thin packages containing very large dies.

Reliability data from many sources, including Texas Instruments, the ITT Research Institute, Honeywell, Rockwell International, Hamilton Standard, and Litton, indicate that PEMs are equally or more reliable than hermetic parts. This is not surprising, considering the microelectronics market trends depicted in Figure 2. Device manufacturers are improving their competitiveness in world markets by automating and modernizing their industrial and commercial facilities at the expense of their military assembly and packaging facilities.

The DoD isn't taking advantage of this high-quality market because it is held captive by the military specifications generated three decades ago. MIL-HDBK-217, for example, is still used to predict the reliability of a system, even though it is thirty years old. These predictions have been biased so that only military-approved parts will meet specified reliability goals. Other factors—such as MIL-HDBK-217's dependence on steady-state temperature, which incurs system penalties of size, weight and cost; ignorance of design impact; and current field-return failures, which have no relevance to the 217 model—make this document a deterrent to sound scientific judgment. Program managers for system developments, which typically require use of the 217 model, fear a substantial risk if they use PEMs. Other military standards also support this perceived risk and bias program managers in their choice of parts. MIL-STD-454, Requirement 64, includes the order of precedence by which an equipment developer must select microcircuits; only a military-approved part is permitted.

MIL-STD-217 is based on the assumption that part failures are the cause of equipment failure. What it does not take into account is that, since the early 1980s, parts have become extremely reliable and are not generally the cause of equipment failure. Field-failure returns from OEM repair facilities, microcircuit suppliers, and DoD depots universally indicate that less than 5% of all failures are chip- or package-related. The vast majority of returns are retested and pass, while the remaining 30 to 40% fail because of operator-printed circuit-board assembly or design-related reasons.

3. What The Army Is Doing

Since the late 1960s, the Army has been using plastic-encapsulated devices (transistors, diodes, microcircuits) in systems for which program managers realized the advantages of the technology. In one case study, an Army Panama Canal Zone field study was initiated in 1970 to assure that helicopter radios using these devices would not have reliability problems. Ten years later, with 5,000 transistors and integrated circuits on test and a quarter-billion device hours accumulated, the verdict supported the use of PEMs[10].

The Army has since used this technology in a few select development systems. These include the Platoon Early Warning System—where one million PEMs were used—and numerous electronic fuze applications, the most recent being the M762, which is now in production using surface-mount technology.

The Army is taking advantage of cost savings resulting from the procurement of non-developmental items (NDI). This equipment is procured without the restrictions imposed by military documents. Most microcircuits for this NDI equipment are PEMs purchased to assure that the system meets performance and reliability requirements. The DoD, in most cases, does not specify or even know what devices are used or how they are procured. The environmental uses for these NDI systems range from temperature/humidity controlled enclosures to hand-held, uncontrolled, anywhere-in-the-world applications.

Army document HDBK-179(ER) - Microcircuit Application Handbook dated October 1993, lists among other things the equipment environments in which PEMs can be used and how an OEM can assure the government that selected microcircuits will surpass system quality and reliability requirements.

The newest DoD qualification system, MIL-I-38535, the Qualified Manufacturer List (QML), embraces many of the ideas of best commercial practices (BCP). Commercial suppliers of high-volume PEMs produced for users who demand quality, reliability, and low cost have incorporated a methodology which assures these goals: control of incoming materials, in-line process control, statistical process control (SPC), in-line process monitors, continual periodic testing, and so forth.

Today, the six certified QML manufacturers produce wafers on lines used by both their military and industry customers. In addition, the DoD now permits off-shore QML lines after vendors argued that maintaining on-shore production was financially untenable. However, QML still demands that the IC supplier support a military organization in addition to its commercial organization, which is a non-value adding proposition for most companies.

While liberalizing QML is a move in the right direction, maintaining separate military lines is no longer justifiable, even to satisfy the environmental requirements of the military customer. Packaging and assembly for non-military industrial markets is done on high-volume plastic-encapsulation lines that are more efficient and cost-effective than their military counterparts. These lines are high-yield, high-quality, have a low defect rate, and provide a highly reliable product to demanding customers.

4. Summary

The quality and reliability of high-volume, best-commercial-practice parts are no longer an issue. Data is available showing that this technology is equivalent to traditional hermetic cavity packages. The challenge is how to procure them to meet equipment requirements cost-effectively. The Army has developed HDBK-179(ER), Microcircuits Application Handbook and has applied this methodology to several key programs, including the Comanche helicopter, the Battlefield Combat Identification System (BCIS), and the Single Channel Ground & Airborne Radio System (SINCGARS). The projected savings secured for each program by the use of PEMs are substantial.

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DISCUSSION

Question: What are the prospects of using plastic MCM parts in future for the military?

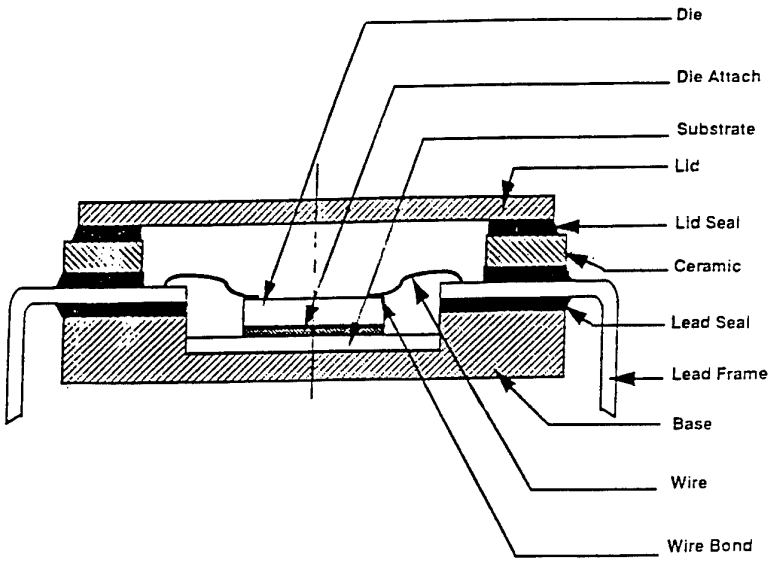
Answer: Very good. [The] desire to use best commercial practice parts must lead to the use of chip-on-board (COB). Many of the restrictions to the use of non-military parts (microcircuits) which are being lifted now for single chip[s] will make [the] transition to MCM easier.

Comment: The use of plastic components is not really a problem for the designer but in many cases for the customer, who has to be convinced.

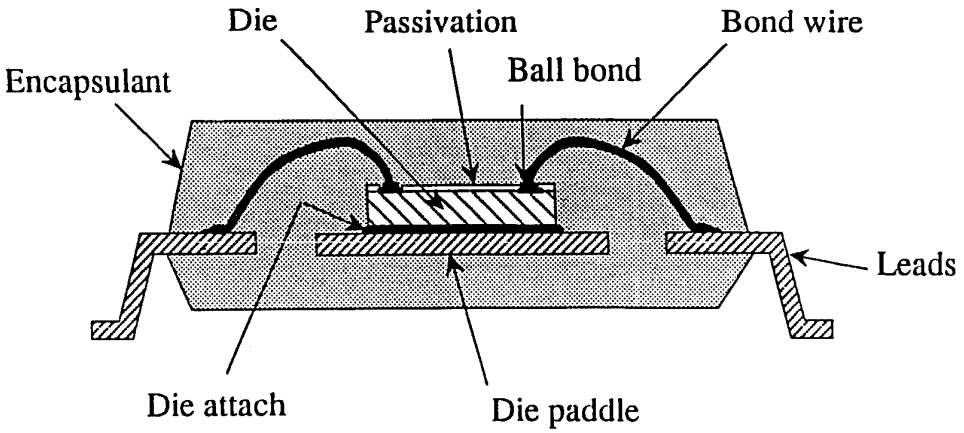
Author's Reply: there are changes coming, pushed down from OSD, which will make the customer a believer.

Question: Do you recommend standard 70 °C commercial parts or should the military stick with -55 °C to +125°C parts?

Answer: Environmental (system) requirements must be specific. Most will not be -55°C to +125°C. Non-military parts are now specified from -40°C to +85°C and from -55°C to +125°C.



(a) Cross-section of a typical ceramic single-chip package



(b) Plastic package construction

FIGURE 1. Comparison of cavity vs. non cavity (PEM) package construction

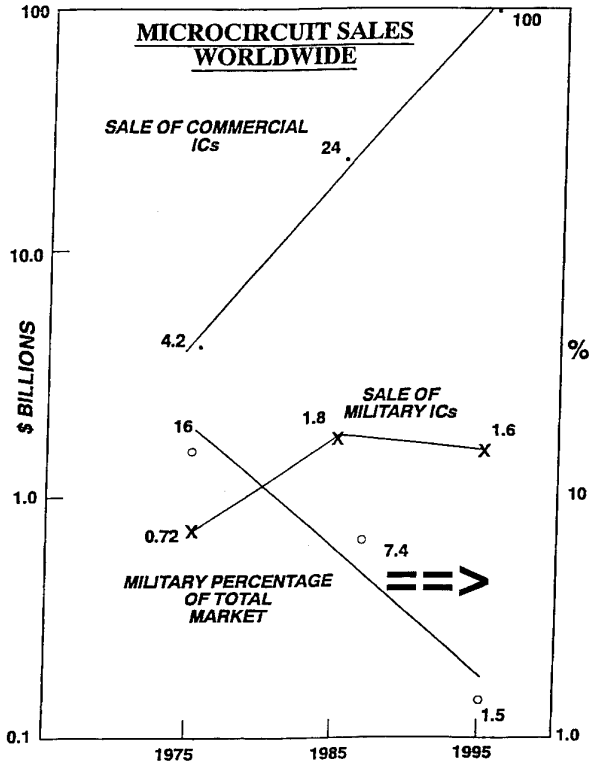


FIGURE 2. Market sales of commercial vs. military microcircuits
(Data provided by Texas Instruments)

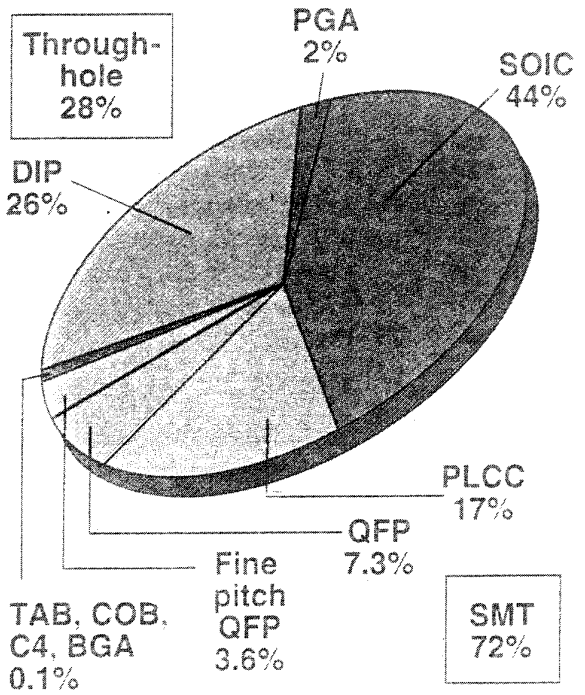


FIGURE 3. Package mix for integrated circuits
(Source: "Design Benchmarks and Activity Metrics," CEERIS International, Old Lyme, Connecticut)

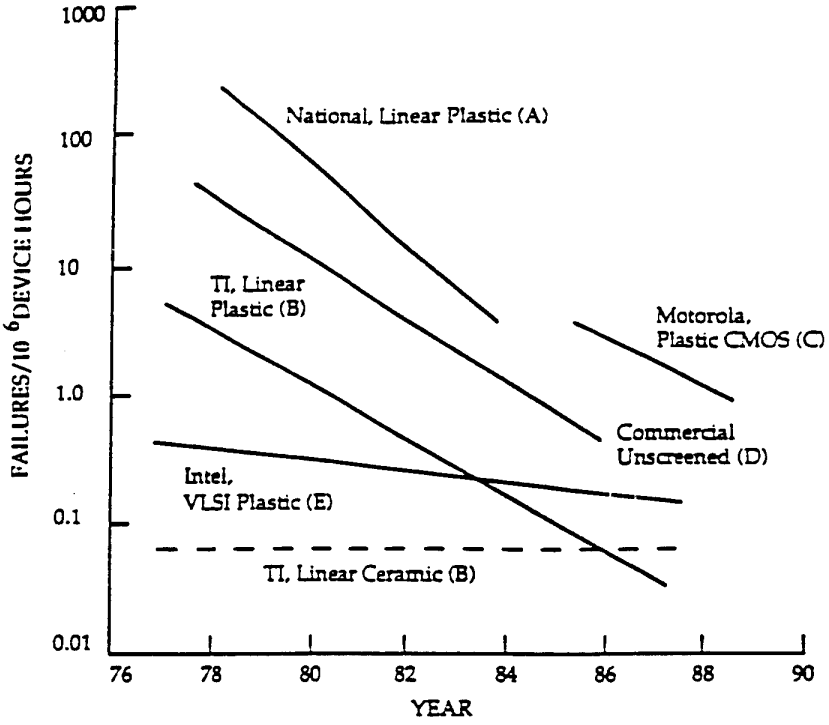


FIGURE 4. Microcircuit reliability improvement trends
(Condia, L. and Pecht, M., "Options for Commercial Microcircuits in Avionics Products," Defense Electronics, July 1991)

(Reference letter is in parenthesis)

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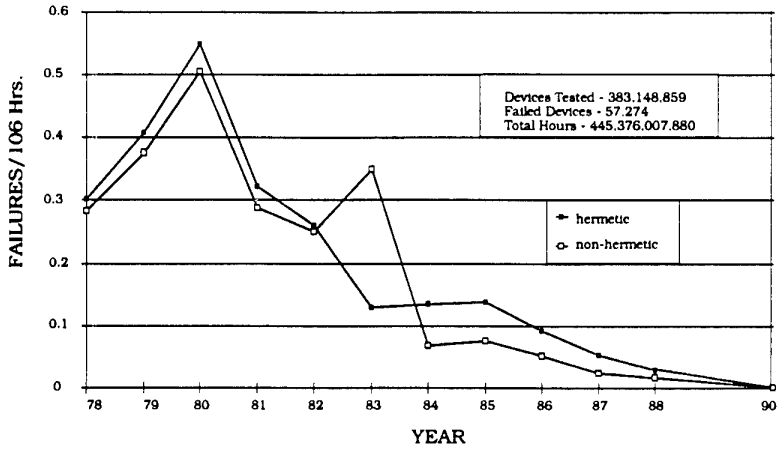


FIGURE 5. IC failure rate as a function of year

MCMs for Avionics - Technology Selection and Intermodule Interconnection

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1. SUMMARY

There are already several Multi Chip Module (MCM) technologies suitable for avionics applications, and new variations and updates are continually being added. The optimum technology choice for each avionics application will depend on many factors, including the electrical and thermal requirements, the operating environment, size, weight, quantity, cost etc.

This paper will compare the attributes of the various MCM technologies, both at present and future trends, including 3D assembly/packaging and the use of active substrates for MCM-Ds. The means of mounting MCMs and interconnecting them into the system using electrical or optical interconnection will also be compared. Some of the methods used to remove very high levels of power dissipation will also be discussed, in relation to the different technologies.

The requirements of electronic modules in different parts of avionics systems may be sufficiently different that alternative solutions are optimal for the various parts. The paper will briefly review the range of requirements across military (and comparable civil) avionics systems and, by considering the technology options, indicate how the optimum choice can be decided, both for the MCMs themselves and for the means of interconnection between MCMs and from MCMs to other parts of the system.

2. INTRODUCTION

The aim of this paper is to help designers to decide which of the several types of Multi Chip Module (MCM) are satisfactory for a particular task and how to choose the most appropriate one, particularly for digital avionics; with additional information on the way such MCMs should be mounted into a system and connected together.

We start by considering the requirements of different types of avionics systems, indicating what distinguishes them from one another in terms of functionality or operating environment and how the requirements change over time, from simpler to more complex systems. We then compare the various MCM technologies, their assembly techniques and thermal management options and the means of incorporating them into the system. This enables us to discuss the technology options in terms of how they can satisfy the system functionality requirements. We also refer to other factors which may affect the choice of technology for a particular MCM requirement. Finally, we give two examples of MCM selection and design from subsystems presently in development in GEC-Marconi Avionics.

3. AVIONICS REQUIREMENTS AND IMPLICATIONS FOR ADVANCED PACKAGING TECHNOLOGIES

Functional Requirements

The operational trends affecting avionics seem to have had the same ineluctable progression for some time. Simply put, however much functional capability can be provided will be used, and however much processing capability there is, it will be "not quite enough". Having rehearsed this simple truth, it is worth looking, in more detail, at where the growth is forecast to occur, and why, in order that any packaging implications can be teased out.

Figure 1 gives some indication of the growth in digital functionality based on a fairly limited dataset but one which is representative and whose trends are likely to be fairly common. The conclusion is that the traditional hierarchy of functional demand remains unchanged in order that there may be some move in relative values. However, the key drivers for given systems are likely to remain unchanged; radars will always be processor hungry, flight controls will always stress reliability and availability, stores will always focus on cost. Thus, even present rankings will give a fair indication of the more appropriate MCM technologies in each case.

Radar

To take a few specific examples, in its relative infancy of simple non-coherent systems, a radar employed a processor of a "mere" 1 million operations per second. The transition to FMICW pushed that up by two orders of magnitude and

current "state of the art" radars are up at a few thousand MOPs. Moving towards active E scan will add yet another order of magnitude to the demand. It is small wonder, then, that radar is one of the key application areas foreseen for MCM and the demand is for the most sophisticated.

Digital Map Systems

Unlike the other examples chosen, digital maps and map based navigation systems have not been driven so much by processor throughput demand as by memory size. As one might expect, the demand has easily kept pace with the increasing size of memory devices made available by commercial processing pressures. In 1984, a typical digital map system employed 8 Megabytes of store. This had grown to 32 Megabytes by the latter half of the decade and today's systems are up around 300 - 500 Megabytes.

However, the future trends are not quite so simple to forecast. As operational scenarios widen, the increase in memory demand is greater than a simple increase in map area coverage would suggest. Memory demand has been kept in check by data compression techniques, but at least some of these techniques are less appropriate to some of the map databases needed to provide true "out of area" coverage. The move from CRT displays to LCD surfaces also places new constraints on presentation which may lead to greater data requirements for a given map area.

Set against this is the increasing use of vector databases which require much smaller memory sizes for a given area and offer greater flexibility with the possibility of generating multiple scales from a single database.

There may also be a rapidly approaching upper limit to the size of memory which can be practically employed dictated by the mission loading time. Selective reloading helps but the problem is that even modern flash EPROM devices take a relatively long time to write. It is difficult to see how much more than 1 gigabyte will be useful in the medium term.

Displays

Cockpit display systems have grown in processing requirements from the early HUDs at about 4 kbytes and 0.25 MOPs to the present 10 megabytes and 4 MOPs. However, it is very difficult and, indeed, misleading to attempt to characterise display waveform generation in this way since the boundary between what is true data processing and what is symbol generation is a very blurred and somewhat arbitrary one. Indeed, solutions which physically segregate these functions exist side by side by those which do not.

Where the particular demands of displays systems emerge is not in the processing or memory requirements but in data communications. Current systems are still limited by having to operate over 1553 between systems and PI bus internal to modular avionics racks. Designers would welcome the opportunities which much higher bandwidth communications would open up.

Flight Control

Although the growth in computational demand required for flight control systems has been fairly dramatic in its own right, it has not been exceptional when viewed in comparison with other systems. The key requirement for flight control has always been high integrity, which has made its own demands on the reliability of the hardware used to implement it. The additional complexity given to the discussion by any attempt to co-host high integrity software with lower integrity software on the same hardware is beyond the scope of this paper. However, any hardware used to perform FCS functions, whether a general computing resource or a dedicated one, must meet the availability required and, with aircraft which can become divergently unstable in a matter of milliseconds, provision for error recovery can create disproportionate resource requirements, unless lane error rates are low enough to ignore "simultaneous" errors. High reliability will therefore continue to be a driving requirement.

Integrated Systems

The above referenced trend towards the use of common computational resources hosting a diversity of functional requirements might lead us to suppose that the sum of all the most rigorous demands is inevitably destined to be the specification placed on the common resource. This "highest common factor" view is a little pessimistic, however. Reconfiguration and dynamic scheduling have the potential to smooth out peak loadings, for example, driving down the total processing throughput needed. Likewise, an integrated system produced from common modules is likely to be placed in an avionics bay, the environment of which, while not benign, is certainly not the worst on the aircraft.

Operating Environments

Not only must we consider the functional demands placed on individual avionics systems, we have to consider the environmental conditions in which that functionality must be provided. It is not sufficient to examine the environment currently "on offer" for equipment bays; the diversity of mounting possibilities increases with more advanced architectures and their improved digital communications. Some systems, like the radar antenna, are more likely than others to stay in their traditional locations but, for other systems, no such geographical claims can be considered sacrosanct.

If we consider that the datum case is the Avionics bay, then the other environments to be considered include, but are not limited to, the following:-

Cockpit Mounted Equipment

Traditionally, the cockpit was thought of as providing a relatively benign environment for equipment because of the needs of the pilot. However, the reality was a lot less benign than at first appeared. Hot soak conditions, with the aircraft parked in the desert with the ECS turned off, tended to drive the temperature spec. The potential for contamination is high, both from natural sources and NBC weapons. There is a significantly higher exposure potential to EMC given the large apertures. Now, even the slight residual advantage enjoyed by cockpit mounted systems may be about to disappear with the move to liquid cooled suits, which potentially obviate the need for air conditioning.

Wing Mounted Equipment

The range of equipment mounted in the wings has thus far been associated with such systems as fuel management and surface position measurement plus the more complex and higher integrity weapon station interface units. These systems already represent between them a very wide range of performance requirements but the range is set to increase still further with the growing move to "smart" or "intelligent" actuators. The wing already encompasses a wide variation of environment with flight condition but the need to mount equipment next to hot hydraulic oil exacerbates this.

The driving operational requirement for wing mounted systems is likely to be reliability, given the difficulty of removing systems or, indeed, maintaining them in situ.

Engine Mounted Equipment

The only real change in engine mounted equipment is the increasing amount of it. However, for MCM to be accepted in this arena, they themselves must withstand the very severe environment and be able to keep abreast of the improvements in high temperature semiconductors, and that may dictate the types of MCM which are applicable.

Stores

Externally mounted disposable stores (i.e. weapons, fuel tanks etc.) are beyond the scope considered in this paper. However, the particular needs of externally carried podded systems are considered.

Discussion

The view emerging is that it will be a case of what is more appropriate rather than discounting some technologies as inappropriate because, in common with many evolutionary technologies, avionics are converging towards a set of common requirements, not only because there is usually a single optimum solution to a particular problem, but also because, for logistic and scale benefits, the user would like to see a move towards commonality, as evidenced by the whole modular avionics scene and JIAWG in particular.

Perhaps the greatest single fact to emerge in considering appropriate technologies for future avionics systems, not just in the choice of MCM, will be the question of economy of scale. Cost has emerged over the last few years in particular as the single common thread of the defence world and of procurement in particular. Whereas the customer has been slow to back off on the requirements side, the old axiom that "The bitterness of poor performance will endure long after the sweetness of low price has been forgotten" has been relegated firmly to the realm of old wives' tales. Today, low cost is the watchword and, if one cannot achieve it by intrinsically low cost technology *per se*, then achieving it by the scale effect of volume production is one major potential avenue for cost reduction. This implies not only commonality within systems, but at all levels, including between programmes.

4. MCM TECHNOLOGIES FOR DIGITAL AVIONICS

Because MCMs enable many components made by different technologies to be combined in a single package, they bring many benefits:

- System Performance: by increasing speed and functionality, and reducing crosstalk and losses.
- Miniaturisation: which maximises functionality, reduces size and weight, facilitates reconfigurability and contributes to cost savings.
- Power efficiency: by reducing parasitics, distributing power conditioning circuitry and reducing the size and cost of power supplies.
- Reliability: by reducing the number of connections, decreasing the stresses and strains and including Built-In Test circuitry.
- Reconfigurability: both at manufacture (which improves yield) and in-service (which improves fault tolerance, extends unattended operation and increases versatility).
- Cost cutting: due to increased automation of fabrication and assembly processes; reduced sizes or quantities of substrates, packages, connectors, thermal management structures, chassis, etc.; less frequent and easier maintenance.

But because the different types of MCM have different attributes, different trade-offs can be made to decide which to use. This section therefore compares the various substrate, assembly and cooling techniques, with regard to digital avionics. Detailed quantitative comparisons are given in Section 6.

MCM-C

MCM-Cs have ceramic substrates made by either a thick film or a co-firing technique (at either "low" or "high" temperatures). The thick film and low temperature techniques have the advantages of being able to include the familiar wide range of printed resistor values and of having tracks more conductive than the high temperature co-fired variant. Recent developments in materials and process technology have greatly improved the interconnection density per layer and will no doubt continue to improve. The use of substrates having higher thermal conductivity (such as aluminium nitride) will greatly improve the thermal performance of MCM-Cs. New high permittivity materials are being developed, to make capacitors of reasonably large values within the substrate; in digital applications these will principally be for decoupling. Lower permittivity materials (typically glass-ceramics) will increase the operating speed of MCM-Cs. The alternative approach is to add one or more layers of organic dielectric as in MCM-Ds (see below). Such substrates are sometimes called MCM-C/Ds. A ceramic substrate can also serve as the base of a non-metallic package, with cost and performance advantages.

MCM-D

MCM-D substrates use deposition techniques for dielectric and metal layers, in a manner similar to silicon device fabrication. The dielectric layers can be either inorganic, such as silicon dioxide, or organic, such as a polymer. At present inorganic dielectrics can be deposited only in thin layers, therefore to reduce capacitance or provide a useful characteristic line impedance the tracks must be narrow. This combination of thin and narrow dimensions gives rise to relatively high resistance. The organic dielectrics can be applied in much thicker layers if desired, so the tracks can be significantly wider and hence more conductive. There are several organic dielectrics, the majority being a variant of polyimide, with different combinations of features such as permittivity, water absorption, thermo-mechanical properties, etc., and new materials (or variants) will continue to emerge. Another variable is the means of patterning the dielectric (mainly to create the via-holes between layers), either by removal (e.g. by plasma or laser) or by photo-imaging. The latter promises to be by far the cheaper method but at present forces compromises in other properties of the dielectrics.

Most commonly the underlying substrate for MCM-Ds is silicon, because of its smoothness (which facilitates ultra-fine feature patterning) and its thermal coefficient of expansion (TCE). Silicon is also an extremely good thermal conductor. The thin-film technology also enables resistors (of moderate value) to be included, at very small size, as well as very fine spiral inductors. Developments are also in progress on high permittivity material deposition processes to provide reasonably high values of capacitance. An MCM-D can also use a ceramic substrate, to take advantage of higher values for resistors and capacitors or to use as the package base, with components on one or both sides. MCM-Ds can also have metal substrates, as the package base and for electrical screening.

The use of a semiconductor substrate, however, gives the MCM-D the unique advantage of being able to incorporate circuitry into the underlying substrate. This can be a "standard" wafer, such as memory, or a custom wafer including, for example, logic circuitry, protection devices, power devices, etc. Figure 2 shows an active substrate MCM-D presently under development at GEC-MRC which incorporates memory in the silicon substrate as well as memory and interface ICs assembled onto the substrate. The next step will be a more ambitious self-contained processor module incorporating an active substrate. An active substrate can increase the overall packing density in two ways: firstly by the obvious addition of a "layer" of devices; secondly (in the future) by enabling the removal of driver circuits from the added-on ICs into the active substrate, so allowing the added-on ICs to be smaller or to contain more electronic circuitry. Another use for the active substrate is to incorporate test circuitry, either to pre-test the interconnection on the substrate before committing to the assembly of the added-on ICs, or to test the circuit after assembly or for in-service testing/reconfiguration. In the future, the substrate could perhaps be made from alternative semiconductors such as gallium arsenide, silicon carbide or diamond.

Opto-MCM

MCMs can include optical or optoelectronic components and/or optical interconnection media. A silicon substrate is an ideal base for a silicon dioxide layer into which optical waveguides are incorporated and, of course, the ubiquitous anisotropically etched features can be used for aligning optical fibres and optoelectronic components. Its thermal conductivity is also useful for removing heat from the high power-density optical transmitters. Figure 3 shows an opto-MCM being developed at GEC-MRC incorporating silica waveguides on an integrated optoelectronic chip which is flip-chip mounted onto a silicon substrate with alignment grooves for devices and fibres. The use of optical interconnect, either within a module or between modules, can greatly increase the data rate, reduce crosstalk and interference, and eliminate the effects of line capacitance. Optical interconnections are likely to be particularly useful for providing accurate clock distribution with very low skew. As an alternative to guided optics (fibres or waveguides), a form of "free-space" optical interconnection using holograms is being developed. This technique promises greater flexibility and reconfigurability but it is not yet mature and may not be suitable for conditions of high shock or vibration.

MCM-L

MCM-L substrates use lamination techniques to combine organic dielectrics and bulk metal layers, essentially the same techniques as for advanced flexi-rigid printed circuit boards (PCBs) but with considerably finer features [1]. The main technological innovation is the use of very tiny holes, an order of magnitude smaller than in PCBs, cut by non-mechanical means. The finer features result in a dramatic reduction in the number of layers compared to a PCB. The dielectric layers are several times thicker than in a typical MCM-D, which results in low capacitance. The thin fine-feature layers are supported by a base, usually a reinforced polymer (such as a PCB) or, alternatively, a metal or ceramic plate. As well as providing mechanical support, these bases can also be used to adjust the TCE, to extract heat or to provide any other features normally associated with a PCB, a metal box or a ceramic substrate (e.g. package base, resistors and capacitors). In the future, resistors will also be available within the fine-feature MCM-L layers. High permittivity layers may also be available for integral capacitors. Figure 4 shows two examples of cross-sections of MCM-L substrates, Figure 5 shows a compact memory module using an MCM-L substrate mounted in a ceramic package.

The copper conductors in MCM-Ls are relatively thick (compared to MCM-Cs and MCM-Ds). They therefore have a much lower resistance and are more robust, for test-probing, wire-bonding and soldering assembly processes. They can therefore readily accept not only unpackaged ICs assembled by wire-bond, Tape Automated Bonding (TAB) or solder-bump flip-chip but also packaged components.

MCM-Ls are presently the lowest cost form of high density interconnect [2 to 5], partly because of the nature of the materials and processes and partly because they can be made in relatively large panels. As materials continue to improve, the panel sizes will increase, hence further reducing cost as well as enabling still larger MCM-Ls to be made. The same

technology can also be used to make the next level of interconnection for MCMs (of whichever technology) and for individual ICs, etc., large or small (see Section 5).

Assembly and Thermal Management

MCMs contain generally unpackaged (but not necessarily bare) ICs. They may also contain packaged ICs or other devices (such as oscillators) if they are not available (at acceptable cost or timescale) in unpackaged form. At present, another reason for using packaged ICs may be that the vendor is unable to guarantee the functionality or the performance of an unpackaged IC. Much effort is being spent worldwide to develop means to provide "Known Good Die" (KGD), since a good yield at MCM level demands KGDs, especially for high IC counts. A detailed discussion of the various assembly methods is outside the scope of this paper; a brief description will suffice for the comparison of the various types of MCM and methods of removing heat.

The vast majority of ICs are presently assembled in two-dimensional arrays on one or both sides of substrates. With wire-bonded or conventional TAB, the working surface of the IC faces away from the substrate and heat is most conveniently extracted via the substrate. If the dielectric layers present too high a thermal impedance, they can be pierced by thermal vias (in all types of MCM) or removed locally to allow the hotter components to be mounted directly onto the more highly thermally conductive substrate below. However, only a few can be so mounted before the interconnection density suffers. With flip-TAB (i.e. ICs mounted face-down) or flip-chip (C4) the heat is most conveniently removed from the exposed back surface, leaving the maximum interconnect density in the substrate. Although it requires high precision and careful design, it is possible to arrange for a solid heatsink to contact many ICs even though the ICs may not be of exactly equal thickness or mounted absolutely parallel. This can be facilitated in the case of flip-TAB by including a shallow gullwing in the TAB frame. Whether face-up or face-down, the ICs can be thermally connected to the substrate or to a separate heatsink, or both, by thermally conductive pastes. These materials can have very high thermal conductance, particularly those loaded with diamond particles. Diamond is also being developed for use as a deposited layer, to spread heat along a substrate. In addition to helping thermal management, polymer based coatings or encapsulants are able to provide a measure of environmental protection for the ICs. One aim of such developments is to remove the need for hermetic packaging for high reliability applications, to save cost, size and weight. The indications are that this will be successful in the near future [6, 7].

The more complex mechanical arrangements of pistons, springs, etc. for heat extraction are almost certainly too bulky, too heavy and too expensive for avionics use. There are mechanically simpler solutions which use fluids (either liquids or gases) to remove heat from the ICs while avoiding the need for high precision assembly. The two principal such methods are directed-jets of air (or gas) and immersion in a dielectric fluid. In the latter case, the fluid can cool by convection (and a little by conduction) and by using the latent heat of boiling, i.e. a phase-change. Not only can very high power densities be managed, but stable operating temperatures can be maintained even while power densities vary from one IC to another or with time. The substrate is also maintained at essentially the same temperature so thermo-mechanical stresses and strains are minimised. The technique is improved if the fluid is cooled below its boiling point (called "sub-cooling"). The fluid can be contained within an MCM (i.e. a self-contained sealed unit) so to the user it appears like any other module cooled externally (by conduction, convection or plumbed liquid coolant).

3D assemblies can take a variety of forms. For modular avionics, let us consider only the following (see Figure 6):

(a) ICs assembled sequentially in layers on top of each other, whether using wire-bonding, TAB, flip-chip or whatever,

(b) ICs pre-assembled into stacks of cuboids and then mounted onto the MCM substrate or a sub-carrier, most likely by a flip-chip or TAB technique,

(c) ICs mounted onto one or both sides of an MCM substrate and several such substrates stacked in parallel and interconnected at one or more edges,

(d) ICs mounted onto one or both sides of relatively narrow MCM substrates and several such substrates mounted orthogonally onto a "motherboard", which could also be an MCM substrate.

In spite of an overall reduction in power consumption, the power density in 3D is likely to be high. In many cases, particularly (a), (b) and (d), it will be possible to extract heat by one of several routes, or by a combination of two or more thermal paths. The selection of substrate type and assembly method will obviously be affected by the thermal impedances as well as by electrical and mechanical considerations. Clearly, the thermal design of all MCMs, but particularly with 3D assembly, must be considered at the outset and the choice of substrate type and assembly method should take into account the assembly sequence and the heat extraction, both while under test (not necessarily at the finished module stage) and in-service.

5. INTERMODULE INTERCONNECTION TECHNOLOGIES

Many present MCMs are similar in size and pincount to large packaged single ICs. In the future, many MCMs will remain of small or moderate size (30 to 80 mm) either because they can simply be made small or to maximise yield and facilitate testing. As pincounts rise to many hundreds per MCM and data transfer rates rise to hundreds of megabits/second and ultimately gigabits/second, new packages and higher performance PCB motherboards and backplanes will be needed.

As pincounts continue to rise, the traditional perimeter-connected packages (e.g. gullwing quad flatpacks) will become difficult to place and to solder and will be replaced by array-connected techniques. Array-connected packages, known as Land Grid Arrays (LGAs) or Ball Grid Arrays (BGAs) are already available and being used in some military systems, although presently more for single chip packages rather than MCMs. Their advantages include easier placement (due to larger pitch connections than equivalent perimeter-connected packages) and a much higher limit on the total number of contacts per package, whether for signals

or for power and ground (to reduce noise and resistance). Solder-free connections are of increasing interest, both to avoid the use of lead and cleaning solvents and to evade the thermo-mechanical problems of solders. One alternative is to use electrically conductive adhesives, but these are not yet widely considered acceptable for military use and are not readily removable for repair purposes. Another option is to use an array of miniature pressure-contacts, held in place mechanically and forced into reliable connection by clamping the packages to the next level of interconnection. This approach is referred to as Solder Free Interconnect (SFI). Removal and replacement is simply effected by removing the clamps and the offending component, using simple hand-tools. Examples of such connector-arrays are available from a number of sources, either in production or development, potentially suitable for military use. The densest array connections are used for applications such as displays, but these are presently for non-military products.

While the use of array connections will give some respite in terms of joint pitch, the interconnection pitch within the motherboard and/or backplane will still need to be very fine, which conflicts with the need for low crosstalk at ever increasing bit-rates. The materials and processes developed for MCM-Ls will be adaptable with advantage for electrical intermodule interconnection media, having lower permittivity and loss tangent, tight tolerance on line impedance, good high temperature performance and the ability to conduct heat away from the MCMs (if the latter are not cooled directly). In order to save cost and weight, the fine features used in the motherboards and backplanes will greatly reduce their layer counts and thicknesses which in turn will allow any TCE-restraining cores to be similarly lighter and thinner. If pressure contact arrays are used, TCE matching is not needed. Further weight reductions will be gained by using new materials such as the metal-matrix composites (e.g. aluminium/silicon carbide) in place of copper/Invar/copper or copper/molybdenum as used today.

Ultimately, optical interconnection will be needed to provide the high data transfer rates, up to gigabits/second. Optical backplane systems employing multimode operation are well established and in some cases commercially available. Singlemode backplane systems are now emerging. The use of optical interconnections at the backplane, on-board and module levels will allow new processor and switching network architectures to be realised, overcoming existing limitations. The optical pathways will need either lower loss materials than those presently commercially available or a means to compensate for losses, such as the doping of the optical medium to provide laser amplification. Improved optoelectronic interface components will consume less power and take up less space. Recent developments in packaging techniques have presented new opportunities for producing very small interface units, through the use of micro-etched silicon.

Point-to-point fibre links are already employed in non-military applications, for example, as embedded fibre ribbons, but they need ruggedising for military use. Optical connectors are compatible with DIN 41612 electrical connectors. Crosstalk is excellent but point-to-point links are not the most flexible in terms of system use. Another possibility is polymer waveguides, in which the losses are reducing to acceptable levels, but these also need further ruggedisation. A board-backplane connection would be more flexible if it could be readily connected/disconnected and allow a board to couple to optical signals wherever it was placed in the rack. One such method uses a D-fibre connector (see Figure 7), which promises to be very cost-effective [8]. The D-shaped singlemode fibres provide alignment tolerances much more relaxed than conventional singlemode connections. The optical signal is transferred between D-fibres on a card or module and on an optical backplane rail. This technique permits variable optical power taps which facilitates point-to-multipoint bus architectures as well as point-to-point optical links. Holographic backplane techniques would be still more flexible, possibly even permitting remote reconfigurability, but are likely to be complex. Direct free-space optical links provide a high capacity path, can be implemented with simple, low-cost components and avoid the use of a backplane. This could be useful for fault tolerant architectures for which rapid memory updates to back-up processors are needed. Another use would be for 3D architectures (such as processor arrays in torodidal or hypercube configurations) in which each MCM or module can have one or more free-space optical interfaces.

Optical interconnection of course fits very well with Opto-MCMs, offering a clear interface specification and reproducible communication characteristics.

6. TECHNOLOGY SELECTION

In many respects the different parts of avionics systems all share the same drivers in performance and cost and the move towards commonality and modular avionics both reflect and reinforce this. There are still, however, differences which can affect both the technology and the architecture selection. Very large amounts of data need to be processed at very high speeds for radar and image processing systems. Navigation systems need ever more memory capacity and faster access, hence very short interconnection paths to all the large memory. Optical interconnection provides very large bandwidth for intercommunications, as required by high data-rate buses and particularly by displays. Flight controls must be extremely reliable and modules in inaccessible locations (e.g. within the wings) should not need frequent maintenance. High temperature survival and operation are needed for avionics mounted near the engine or affected by hot fluids, by the heated areas of the aircraft skin or in the cockpit. The latter also need excellent protection from contamination and EMI. At the system level, the ability to reconfigure and to schedule work dynamically can benefit from the high bandwidth and high speed switching capabilities of optical interconnection.

Miniaturisation is the most visible benefit of MCMs and often the most important for military applications. Table 1 shows density data for MCMs available now (at least in prototype or limited availability) and as predicted for early in the next century, but these must be interpreted with caution. For example, the amount of silicon which can be physically compressed onto a given area of substrate or into a given volume can depend either on the IC assembly processes (2D or 3D) or on the interconnection density within the substrate. Of these two, at present it is almost always the former which is the limiter. It is notoriously difficult to devise a general means to compare MCM technologies, because different systems and modules have different needs and each MCM

technology can be manipulated to provide different trade-offs. With regard to interconnection density, for example, the requirement is considerably affected by the mix of ICs. Clearly, chip-sets having predominantly nearest-neighbour connections are relatively undemanding and designers can exploit this particularly with ASICs. We must also consider, however, other factors such as heat extraction and high speed performance, including crosstalk and parasitics incurred by the very fine geometries. Key electrical parameter values are given in Table 2 together with figures for the thermal conductivities of substrate materials. Clearly the electrical and thermal characteristics of a given type of substrate, and of a particular example of that type, will depend crucially on the detailed construction, which the designer can adjust to exercise the various trade-offs in performance, miniaturisation and cost. Advanced electrical and thermal modelling techniques are widely available for this purpose.

Each of the MCM substrate technologies has characteristics which promote its selection. MCM-C substrates can offer the largest range of integral resistor and capacitor values. The layer count can be extremely high, although the relatively high permittivity may limit the speed unless short paths are used or lower permittivity materials are introduced (such as polymer layers, to create MCM-C/Ds). For microwave applications, however, higher permittivity is an advantage since it helps to increase the miniaturisation. Small matching resistors can readily be integrated into the MCM-C. The ceramic substrate can readily be used as the base for the package, with consequent reductions in size, weight and cost. The avoidance of ferromagnetic materials, throughout the MCM-C and its package, is advantageous in applications in which the magnetic permeability must be minimised. The absence of organic materials makes them attractive for high temperature use. The ceramic substrates can also accept either unpackaged ICs or packaged devices or both, which makes them versatile and helps keep costs down, and they are compatible with a wide range of connectors and sockets for installation and for testing purposes.

MCM-D substrates can offer the highest interconnection density, should it be necessary, and the smallest integral passive components. Their unique advantage is the active substrate which, in addition to increasing the packing density, can provide the means to test the substrate before any ICs are assembled. MCM-D substrates are also the most attractive for opto-MCMs, although the other types of substrate can also be used. Opto-MCMs provide the most user-friendly photonic/electronic interfacing, for module-module or module-backplane connections.

MCM-L substrates are the most versatile option, being able to accept virtually any format of unpackaged or packaged device as well as other types of component. They can offer the lowest parasitics, they are resistant to damage, either from shock or from repair activities, and are the lowest cost option. They are probably the easiest type to incorporate into systems, being compatible with the widest range of connectors or sockets and capable of having integral flexible circuits. Their metal-cores can also be used as package bases.

For interconnection between modules, the first concern is the pincount and pitch of the modules, i.e. how easy it is to connect the modules reliably to the next level of interconnect. Next come the signal speed (crosstalk and propagation delay) and thermal management. The ability to remove and replace individual MCMs will be more important if testing them is either inherently difficult or inadequate in the context of the surrounding electronics. This can determine the choice of the method of assembly/connection and hence the choice of MCM substrate. The selection of electrical or optical interconnection between MCMs or to other parts of the system is still very application-specific. Multiplexing signals onto optical interconnections can clearly overcome problems such as high pincount and unacceptable crosstalk or interference but it is even more likely that optical interconnection will be favoured when intrinsically high signal bandwidths are present.

3D assembly is very promising as a means to achieve further miniaturisation and higher speed, due to having short path lengths. High density memory is a very good candidate for 3D assembly, since the pincounts and power dissipations of memory ICs are modest and the architecture simple, in comparison to other types of IC. Cuboid stacks of memory (see Figure 6(b)) are inherently dense and particularly appropriate for large memories but it would be counter-productive to have substrates widely spaced in order to accommodate only a few tall stacks. 3D assembly in the form of Figure 6(c) but using solder-free interconnects between the individual substrates would be robust and easy to build and maintain.

As with all technologies, however, particularly ones which are still developing, none of these issues will stand still long enough to be permanently pinned down, all the attributes including cost will vary with time and by different rates for the different options.

There are several factors which may affect the technology selection. Firstly, it may be desirable, or unavoidably necessary, to keep some ICs in individual packages: to facilitate product variants or mid-life updates; to allow late decisions on IC selections; to ease repair and replacement; or to maximise the electrical screening or environmental protection of particularly sensitive components, particularly analogue or mixed analogue/digital devices. The designer would need to decide whether to mount the packaged component(s) on the MCM substrate or to repartition the circuit into MCM and PCB/packaged devices; each of these could affect the choice of MCM substrate type. Secondly, previous experience or capabilities (such as in-house technology investment or software development) may determine what is the most cost-effective solution. Thirdly, the need for optical interconnection and the best option for the case in question may influence the choice of assembly method (whether in 2D or in 3D) and subsequently the MCM substrate type.

To illustrate the selection of MCM technologies, let us now give two examples. The first is an Arithmetic Processor Unit (APU) for an airborne radar. The present embodiment (in production) uses Surface Mounted Technology (SMT) on a Microwire™ board, see Figure 8(a), approximately 23 cm × 15 cm (9" × 6"). (We have developed a new fine-feature PCB which is thinner, lighter and cheaper than

Microwire™ and is called MICROTRACE. This PCB uses the same technology as MCM-L (see Figure 4) and will serve firstly for SMT boards then as motherboards for MCMs or mixtures of MCMs and packaged VLSICs.) To increase the processing speed of the APU and provide an adequate memory capacity in close proximity for rapid access, an active silicon substrate MCM-D has been chosen. The silicon substrate is a slice from a memory wafer, the individual memory blocks being accessed by the metallisation at the first stage of fabricating the high interconnection density layers of the MCM-D processing. In the first instance the assembled ICs will be wirebonded. The technique is essentially the same as shown in Figure 2. The schematic for the APU MCM-D is shown in Figure 8(b). The MCM is an order of magnitude smaller than the SMT version. In addition to the removal of memory ICs into the substrate, the number of remaining ICs has been further reduced by integrating some of the smaller ICs into larger ones. The reduction in assembly cost contributes to the cost-effectiveness of this approach. The circuit design incorporates built-in test (by boundary scan) and some reconfigurability.

The second example is high density memory for digital maps. As mentioned above, the densest memory assembly, taken separately, would be a 3D cuboid, but in practice it is often preferable that the memory assembly is similar to that of the neighbouring circuitry. The MCM technology which has found favour for implementing memory for digital maps thus far has been MCM-C with memory devices packaged on one side of the substrate and drivers on the other. Power management, whereby power has been applied only to the active device(s), has kept module dissipations modest. Multiple cavity packages have offered increases in packing density as have the capacities of the individual memory devices. Although 3-D stacks have been put forward in some cases, the upper limit of memory size discussed previously means that this packaging technique will not be necessary in many cases. The current problems are obtaining "known good die" and keeping the driver technology up to the standards compatible with the advances in memory devices.

7. CONCLUSION

The case for using MCMs in future avionics is ultimately irresistible. In addition to improving system performance, they confer benefits in size, weight, reliability, power efficiency and cost. They also facilitate changes in system architecture by enabling reconfigurability and dynamic scheduling of workload between the various modules in the system. Although the major MCM substrate technologies have much in common, and there are undeniably other drivers towards more commonality in avionics modules, there remain significant differences between the MCM technologies (substrates, assembly and packaging techniques) which enable each of them to claim particular advantages which promote their selection in specific cases.

We have briefly described the avionics requirements and the major MCM technologies and intermodule interconnection media, showing where each MCM substrate technology has particularly favourable attributes. When more than one option can fulfil the requirement, the deciding factor is likely to be cost. However, the cost of each technology will vary with quantity and with time, at different rates. The choice may therefore be influenced by the economy of scale at which the various vendors operate, but for many of them the scale will be determined by their popularity in other market sectors. In view of the way in which the modules and their interconnection media fit together to make up the system, it will become ever more important to consider the overall cost as a whole, not just the cost of each part in isolation.

8. ACKNOWLEDGEMENTS

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TABLE 1. MCM DENSITY COMPARISONS

	NOW				FUTURE (>2000 AD)			
	MCM-L	MCM-C		MCM-D	MCM-L	MCM-C		MCM-D
		Fine Line Thick Film	Co-fired			Fine Line Thick Film	Co-Fired	
Min. Practical Track Pitch (µm)	80	150	200	40	50	80	125	30
Typ. Via-Hole Diameter (µm)	50	100	150	30	<30	40	50	<20
Max. Interconnection Density/Layer (cm/cm^2)	80	40	30	160	100	100	75	200
Max. No. of Signal Layers	>12	6	60	4 (fine feature layers)	>20	6	>60	>5
Max. Interconn. Density (cm/cm^2)	>960	240	1800	640	>2000	600	>4500	>1000
Max. Area Ratio Silicon: Substrate (%)	~50 single side ~100 double side >100 (3D)	<80 >100 (3D)	<80 >100 (3D)	<80 (passive) 120 (active) >100 (3D)	75 single side 150 double side >200 (3D)	90 >200 (3D)	90 >250 (3D)	90 (passive) 150 (active) >250 (3D)
Max. Substrate Size* (cm^2)	>400	100	>200	100	>600	200	400	>200

* The finest features cannot necessarily be used for the largest substrate sizes of any particular substrate technology.

TABLE 2. MCM PERFORMANCE COMPARISONS

	NOW				FUTURE (>2000 AD)			
	MCM-L	MCM-C		MCM-D	MCM-L	MCM-C		MCM-D
		Fine Line Thick Film	Co-fired			Fine Line Thick Film	Co-Fired	
Electrical Dielectric Constant	3.5	4	5 - 10	3 - 4	2.6 - 10	4	<5 - 10	2 - 4
Propagation Delay (ps/cm)	60	70	80 - 120	60 - 70	50 - 120	70	70 - 100	40 - 70
Track Resistance (Ω/cm)	0.06	5	0.5 - 1	1 - 7	0.06 - 0.15	8	0.5 - 1	1 - 3
Track Capacitance (pF/cm)	1	2	2.5	2	1	2	2.5	<2
Thermal Thermal Conductivity (substrate material)	<1 - 390	30 - 200	2 - 30	36 - 200	<1 - 390	30 - 220	30 - 220	30 - 220

DISCUSSION

Question: With VLSI/VHSIC, it has proved to be the case that semicustom or fully custom chips have been essential to meet individual system requirements. In your view, will we need a similarly "foundry" capability for MCMs in avionics?

Answer: Yes – such a facility is essential. I think that most MCMs that will be used for avionics applications will be "semi-custom" or "full custom."

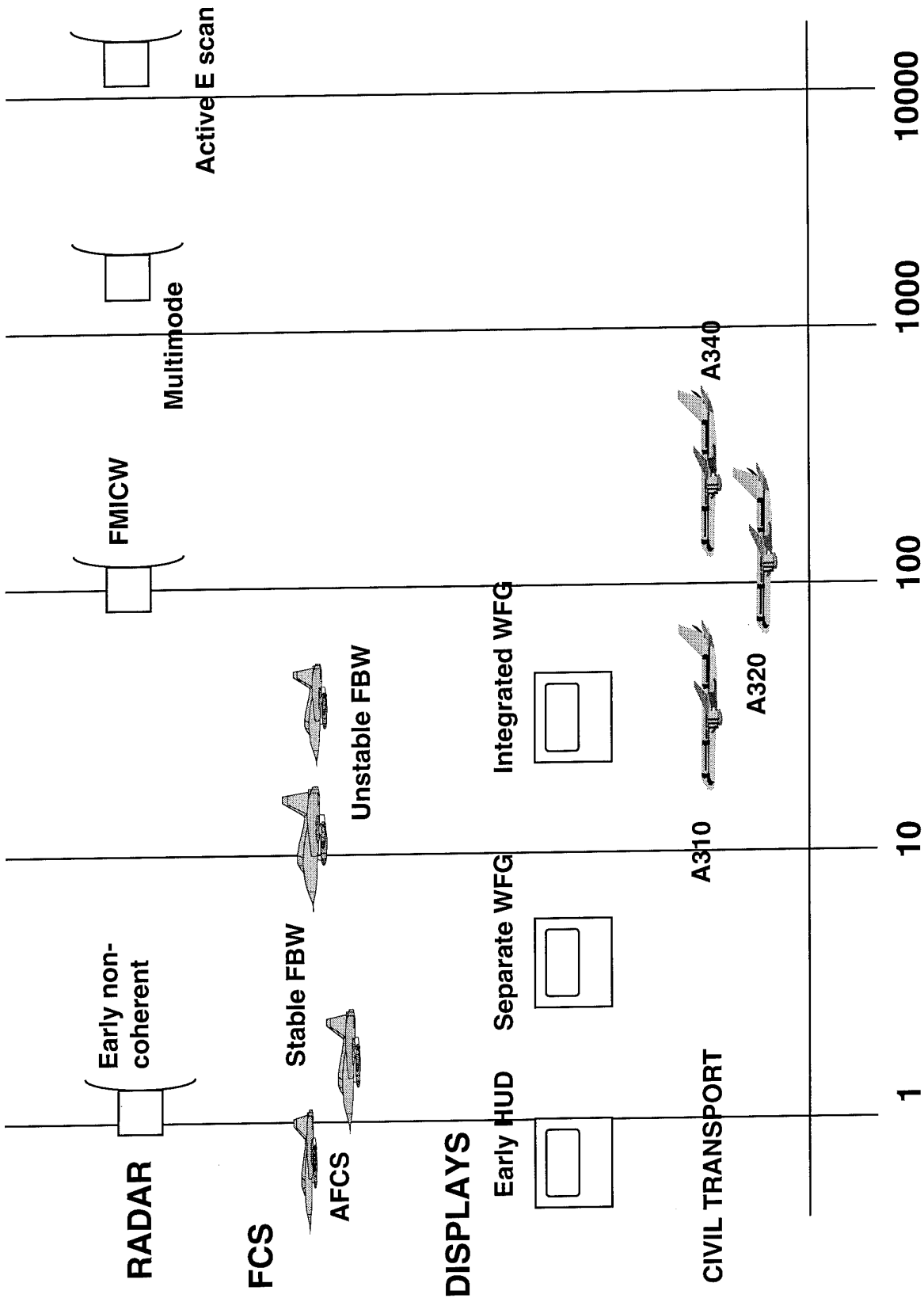


Figure 1 The growth in avionic systems' demand for processing

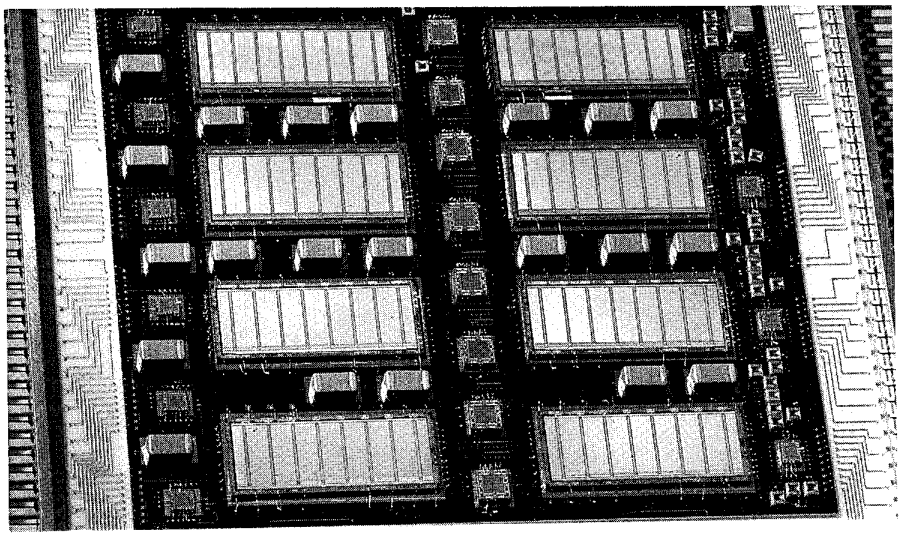


Figure 2 Active substrate MCM-D, based on a memory wafer slice (GEC-Marconi)

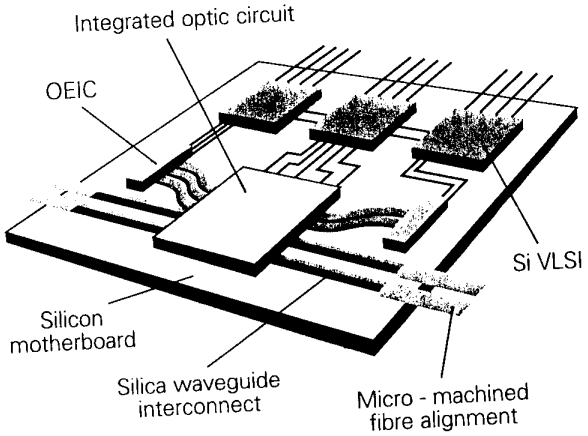


Figure 3 Opto-MCM incorporating flip-chip assembly, silica waveguides and alignment grooves in the silicon (GEC-Marconi)

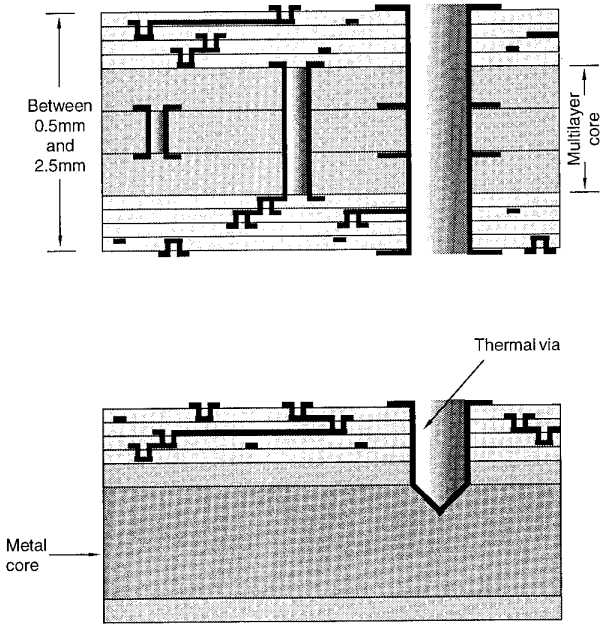


Figure 4 Two examples of the build-up of MCM-L substrates (GEC-Marconi)

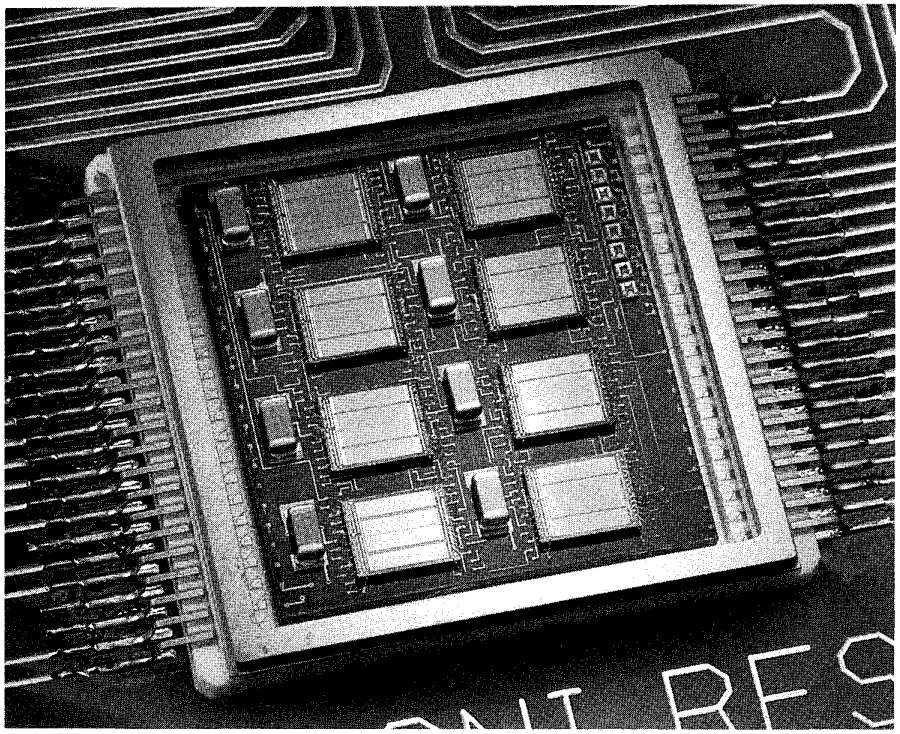


Figure 5 A compact memory module using MCM-L in a ceramic package (GEC-Marconi)

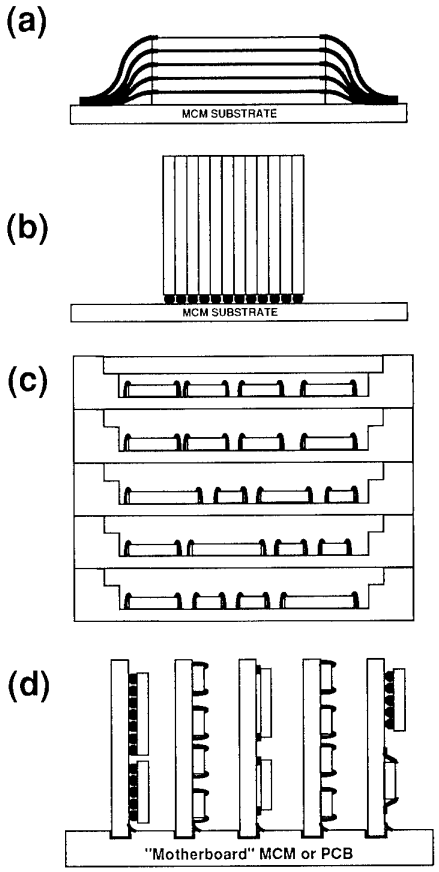


Figure 6 Some examples of 3D assembly schemes suitable for avionics use

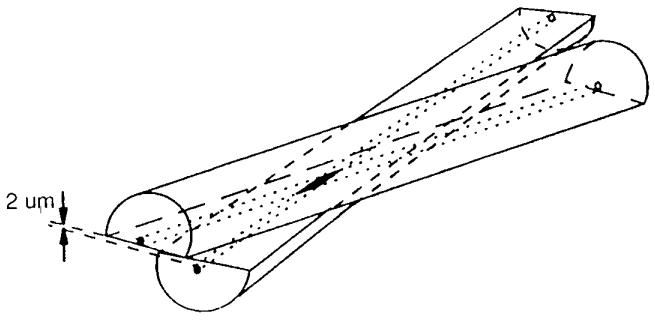
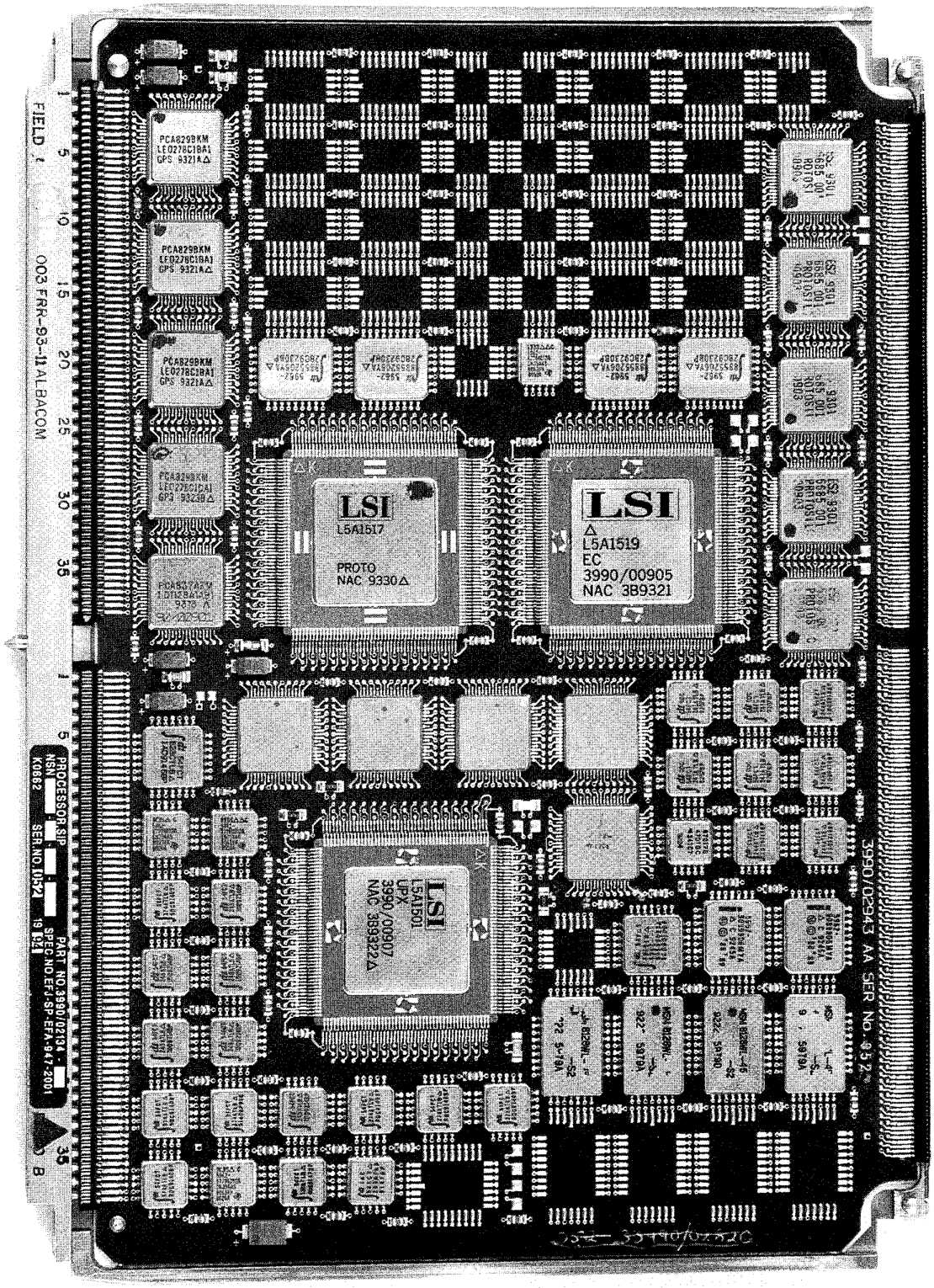
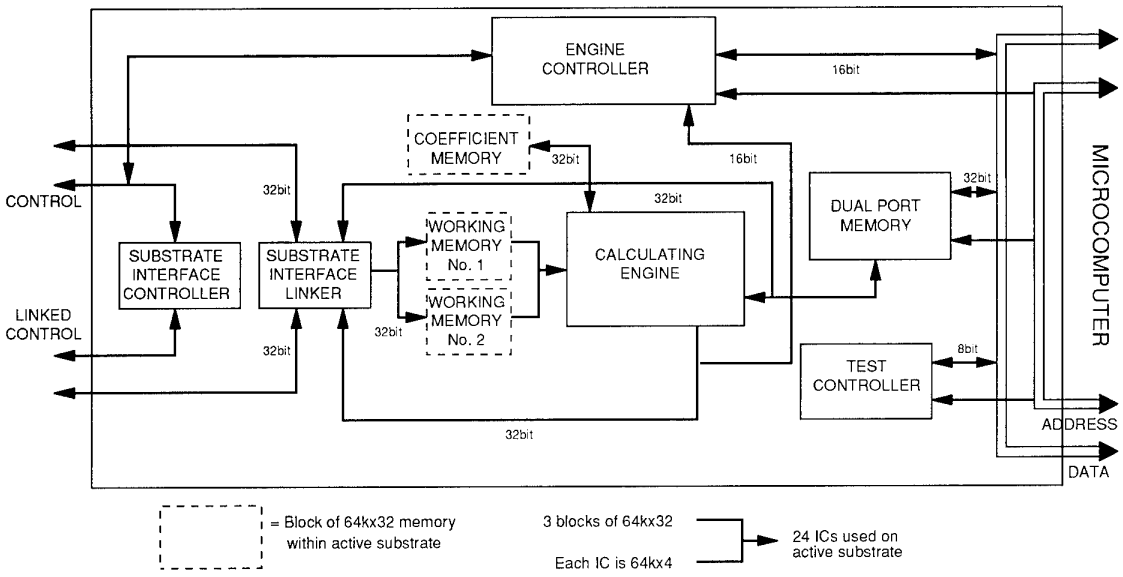


Figure 7 D-fibre connector: a cost-effective method for optical connection between modules, boards and backplanes

Figure 8 An avionics Arithmetic Processor Unit: (a) using SMT PCB technology (9" x 6")





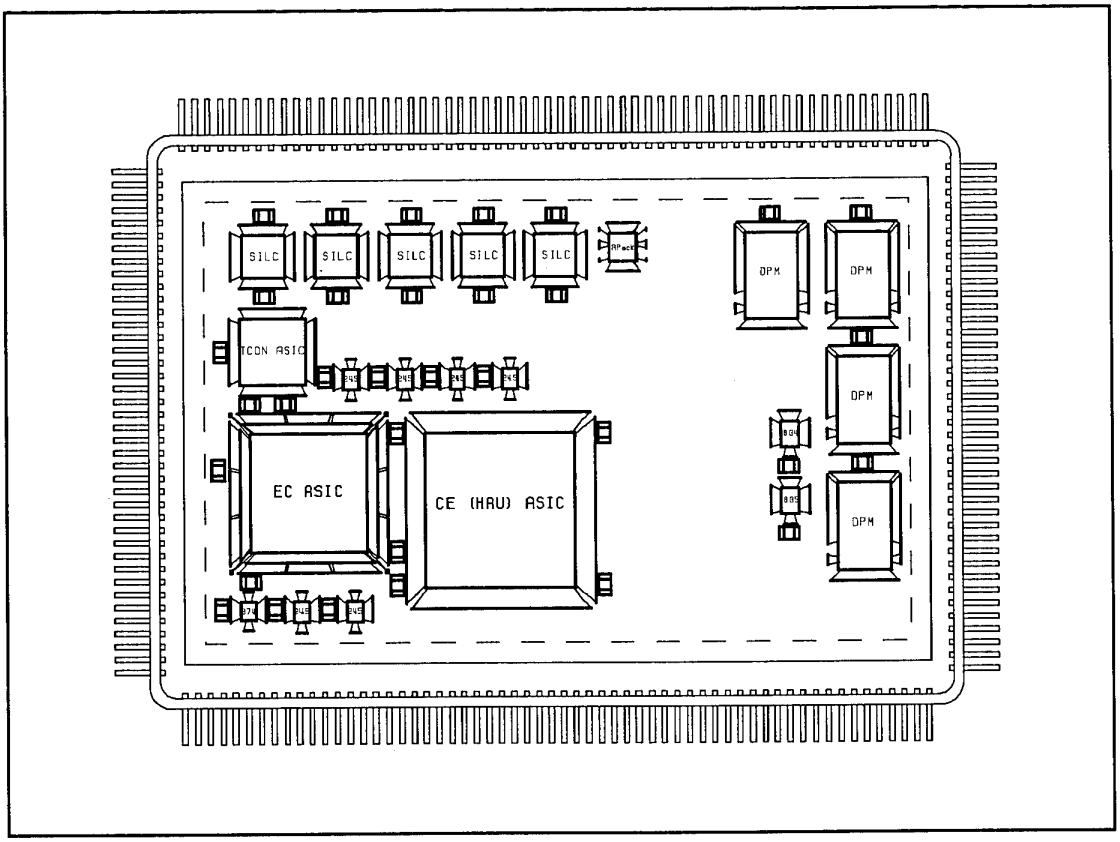


Figure 8 An avionics Arithmetic Processor Unit:
(b) schematic for active substrate MCM-D technology (3" x 2")

ADVANCED STANDARD ELECTRONIC MODULES FORMAT-E (SEM-E) PROCESSES FOR RAPID PROTOTYPING

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Abstract.

The objective of the "Advanced SEM Processes" effort is to simplify the development and qualification processes and reduce the related process times and costs from the current way of doing business. Advanced technology developments and qualifications typically are completed in three to five years from conception. The Standard Hardware Acquisition and Reliability Program (SHARP) is working in conjuction with the Advanced Research Project Agency (ARPA) Application Specific Electronic Modules (ASEM) effort, Raytheon and the Electronics Manufacturing Producibility Facility (EMPF) Manufacturing Technology efforts to define new processes for development and qualification that leverage commercial and military technology in applying "MultiChip Modules" (MCMs) to Standard Electronic Module format E (SEM-E) packaging. These processes are anticipated to have applicability to the development and qualification of SEM-E packaging, using multiple state of the art technologies in addition to MCMs. The primary objective is to reduce the current cycle time from three / five years to twelve months and costs from $500,000 / $1,000,000 to $100,000 / $250,000, therefore providing a baseline for standardizing electronics hardware acquisition processes into the twenty first century and beyond.

Introduction.

The Standard Hardware Acquisition and Reliability Program (SHARP) is a Navy-wide logistics technology development effort focused on reducing the acquisition costs, support costs, and risks of military electronic weapon systems while increasing the performance capability, reliability, maintainability, and readiness of these systems. The SHARP consists of a joint program between the Naval Surface Warfare Center (NSWC), Crane Division and the Naval Air Warfare Center (NAWC), Aircraft Division, Indianapolis. NAWC AD, Indianapolis is the primary activity for avionics related efforts with NSWC, Crane as the primary activity for submarine and shipboard electronics related efforts.

Lower life cycle costs for electronic hardware are achieved through military and commercial technology transition, standardization, and reliability enhancement to improve system affordability and availability as well as enhancing fleet modernization. Advanced technology is transferred into the fleet through Standard Electronic Modules, Standard Power Supplies, Standard Battery Systems, Standard Enclosure Systems, and Advanced Interconnect Systems.

The SHARP's success is based on the deployment of 8 million products in over 250 different systems using over 350 hardware standards, with 50% of those standards used in 8 or more systems. The SHARP research and development initiatives have provided an average return on investment of 5 to 1, an increase in reliability of 2 to 13 times, an excellent transition vehicle for military and commercial technology and dramatic reduction in development time of electronics.

Papers presented at the Avionics Panel Symposium held in San Diego, CA, USA, 6-9 June 1994.

SHARP's processes originated with the Standard Hardware Program in 1965. This logistics program has operated under the name of SHARP since 1987. However, the program functions have been in existence and operated with a similar philosophy for over twenty-five years.

Background.

Since 1965, the Navy has been trying to encourage the use of existing packaging to limit the number of times we have re-invented the electronic systems. At the same time our focus has been on improving process and produce quality. Our goal has been to reduce the cost of electronics in the Fleet. This effort was carried on under several names and system command sponsorships. The effort, through the same resource sponsorship, (Chief of Naval Operations, N403) emphasis and management, had different names including the Standard Hardware Program, Standard Electronic Modules Program, Naval Avionics Facility Indianapolis Modules, and the Standard Hardware Acquisition and Reliability Program. System command sponsorship has been from the Strategic Systems Project Office, the Naval Electronic Systems Command, the Naval Space and Warfare Systems Command and the Naval Supply Systems Command.

In the past the Navy planned to support a piece of equipment for 20 years or more. The whole cost of ownership or life cycle cost, as we call it, including development, production, operation and support, upgrades and disposal was the target of cost reduction. The method of cost reduction and reliability improvement came together when a more reliable equipment was found to be less expensive to maintain. Typically, it costs ten times more to maintain equipment than it does to initially procure it. Standardization allows for the elimination of redundant processes and reduction in spares through economies of scale.

The mechanism of this standardization has been functional documentation, a qualification process, and early design review to verify no redundant designs were used and that quality was designed in early in the development process. Careful consideration of the system requirements were necessary to make the best of these processes or the decision to use the existing design or not would be ineffective. The functional documentation made it easier to develop multiple sources, based on competition. The qualification assured the reliability and interoperability for which it was developed. The challenge was that no one wanted to pay for it. It was difficult to get everyone to "do it smartly". However, a notable commonality was achieved and standard modules were four to ten times more reliable then other similar modules.

Old Paradigm New World.

These achievements were based on levels of circuit integration at the Medium Scale Integration and lower. They were based on smaller module formats (about 4 vice the current 45 square inches circuit area). They were also based on a cold war scenario and a long time build up for deterrent sake. Although the military had a small part of the electronics market, it had, never the less, an impact on the direction and trends of the market place. Under these circumstances, the posture was correct and effective. Unfortunately or fortunately depending on your perspective, all of this has changed!

The use of commercial technology, products and processes has become a major emphasis for the Department of Defense. The life cycle profiles of military verses commercial products provide a very different life expectancy and levels of technology insertion. Figure 1. shows a comparison of military vice commercial life cycle. The commercial sector provides a more rapid technology insertion capability than the military. Even though state of the art technology can be rapidly inserted into

electronics by leveraging the commercial sector, commercial products have not typically been supported long enough to allow complete and direct usage of commercial products, without additional creativity being applied on the part of the Department of Defense (DoD). Commercial technology, products and process can all be applied to military electronics. Success lies in not only a smart idea, but in smart application.

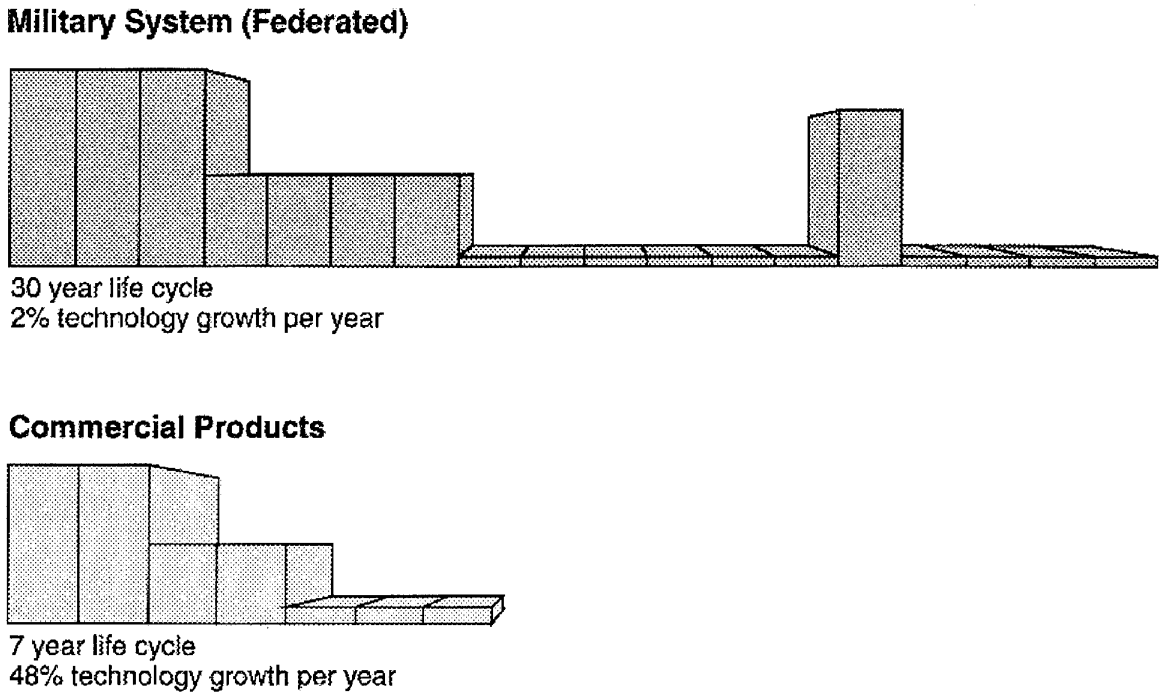


Figure 1.

Modeling and Simulation.

Modeling and simulation, virtual reality, these terms are becoming as much a part of our life as automobiles and house hold appliances have in the past. Virtually every major electronics firm has considered modeling. A recent article headline in a local paper stated "U.S. automakers speed up their car design process - Increased productivity and the latest computers reduce the time it takes Big 3 to develop models." "It took ... only $4^1/_2$ days, not the customary 13 weeks, to design and build a hood for the initial prototypes of its new midsize cars, ..." Simply stated, modeling and simulation reduces the number of prototype iterations due to faulty design and can be applied to reduce the lead time preparing for product qualification. This reduces development time and cost. The idea is to do as much design verification before you get to the laboratory as possible. An extra printed circuit board fabrication run means extra time for the designer to debug the board. Printed circuit boards are getting denser, include blind and buried vias, and have more layers. A trace routed on an internal layer can not be cut and jumpered. It is almost impossible to add a wire to a 132+ pin component because of the small spacing between pins and the half ounce fine pitch copper traces. Besides all this, lets face it, everybody would like to stay away from the laboratory. Even the best engineers have problems with test equipment and other miscellaneous laboratory setup concerns.

Finally, in the past, designers have only simulated blocks of circuitry. These blocks were never simulated together. The problem of integrating an Application Specific Integrated Circuit into a board design is well known. Designers may also have problems integrating a Programmable Logic Device into a board design. Unless you simulate the entire board, you cannot be sure that the board will work. The bottom line is that you save money and time by reducing the number of prototype board iterations. According to the latest estimate, between seven and ten billion dollars are lost annually because of this multiple prototype iteration strategy. The effort being discussed in this paper is addressing ways to apply simulation and modeling to electronics applications for rapid prototyping and generation of test vectors for verification and validation of designs.

Utilizing a complete suite of CAE/CAD tools with a standard design environment provide a key to time and cost reduction in prototyping SEM-Es. The idea is not to impose specific CAE/CAD tools and design on designers, but to apply a standard design methodology based on principles of maximizing the use of industry standard data formats for the exchange of design information between fabricator and designer. This allows designers and fabricators to use CAE/CAD tools of their choosing, as long as the required design data is provided in the specific industry standard formats when released for fabrication.

The purpose of the standard data package is to provide designers with necessary information on design rules, requirements, and required design release data and formats. This information includes thermal characteristics, mechanical dimensions, minimum feature spacings, device footprint specifications, etc. This standard data package will provide the designer all of the necessary information to provide first success designs in fabrication based on maximizing the efficiency and success of the design efforts transferred to fabrication in a rapid time frame. The important set of issues are to address the availability, use and correlation of device models for CAE/CAD design functions without imposing proprietary tools and formats. In doing so, maximum use of commercially available models for design and simulation will be applied.

Checking routines and procedures will assure that a viable, quality product results from the design process. Design verification will play an important role, and will include assuring that required design data and information are available and that there is compliance with data format requirements, fundamental electrical design rules and requirements, SEM-E mechanical packaging design rules and requirements, simulation and test program rules and requirements including fault directories and test diagnostics data (when possible), and target design technology (feature spacings, layer and via restrictions, device footprints, etc).

The use of modeling and simulation data to generate and transfer test vectors and related test data is just as important as applying modeling and simulation during design. This process is also a key element in the cycle reduction time compared to the generation of Test Program Sets after the module is designed and fabricated. The format for test vectors is expected to be the Test Systems Strategies Inc., Standard Events Format. Test Requirements Specification Language is planned for basic electrical characteristics with Fault Dictionary Language used for transfer of diagnostic data.

PEMs, ICs, ASICs, Chip Sets, and FPGAs.

Plastic Encapsulated Microcircuits (PEMs) are one avenue for leveraging commercial technology and products. PEMs are defined as an integrated circuit physically attached to a leadframe, interconnected to leads and molded in a plastic vice mounted in a metal or ceramic cavity, and hermetically sealed. Plastic

encapsulation originated in the 1950s with the first commercial transistors because of failures from corrosion or intermetallic growths. Military and other high reliability users opted for improved hermetic packages and refinements to the packaging processes. The results were hermetically sealed components to solve moisture induced problems. The direct use of high volume plastic ICs or die packaging via Hybrid and MCM technology can mean cost savings because of the declining availability of military ceramic ICs. More part numbers are available in plastic ICs (30% more) which drastically assist in the low DoD IC volume that has continued to produce decreasing military part numbers and suppliers. The Semiconductor Industry Association (SIA) predicts that in 1995 ceramic ICs will be 2% of world volume, the military market in dollars will be less than 1% of the market and the military market by volume will be too low to measure. In addition, some leading edge technology is only available in plastic packages. The goal is to leverage PEMs directly or through MCM packaging to provide a transition of commercial components into the next assembly level (SEM-E/Circuit Assembly). The application of PEMs is smart, but requires a smart application during the systems engineering and design process, not a blanket approach, to be successful.

Integral to the leverage of PEMs is the use of Off The Shelf (OTS) chip sets. These chip sets will include both commercial and military technology. Commercially available die and military die can be integrated and packaged via Hybrid or MCM technology without trading off the past problems with plastic encapsulation. This provides a drastic reduction in technology development time when combined with Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs). These technologies, combined with modeling and simulation tools, provide a rapid insertion of both commercial and military technology to the next assembly level. This approach also brings to light the real application of Dual Use technology.

MCMs, MMICs, Distributed Power.

Technologies developed from commercial and military electronics industry efforts are making unprecedented levels of performance, upgradability and supportability for modular electronics achievable through the increased use of industry standards and advanced dual use processes. Integral to achieving a cost effective implementation of these technologies is to provide a packaging and supportability process which provides for the full potential of the technology, while leveraging the best industry processes. The current technological challenge is to increase the performance and to reduce the amount of logistics support of Navy electronics while physically increasing the integration of the electronic functions. This requires a standard packaging approach below the electronic circuit assembly level to increase the density. The process for increasing the available real-estate for integrated circuits is to apply a new technology, MCMs. The scope of this effort is intended to also include Microwave Monolithic Integrated Circuit (MMIC) and Distributed Power (DP) technologies, but for the pilot process demonstration the focus is primarily on MCM technology and limited DP.

MCM technology allows for the equivalent of multiple integrated circuits to be packaged in one device, thus reducing the non-electrical part of the package. MCM technology is a derivative and subset of Hybrid technology. A Hybrid is defined (ISHM Design Guidelines) as "an electronic circuit manufactured by a combination of technologies which includes at least two components, at least one of which must be an active semiconductor device, in conjunction with a substrate manufactured by a film technology" A MCM is "a module in which the ratio of the area of active devices to substrate area is greater than 30 percent". See Figure 2. MCM technology

provides vast gains in real-estate for the module designer. In addition to real-estate gains, MCM technology provides a designer with modular building blocks below the board or module level. This approach provides standard functions that used to be at the circuit card assembly level but is now in a package small enough to provide multiple functions on a single board. Thermal issues can be solved for the most part by advanced composites materials (see SEM-E section) and good mechanical and thermal engineering. MCM technology is maturing to include three dimensional (3-D) packaging technology that will allow the mix and match of two dimensional 2-D MCMs. 3-D MCM technology will provide the vehicle to reduce the interconnect boards from two to one with a SEM-E approach.

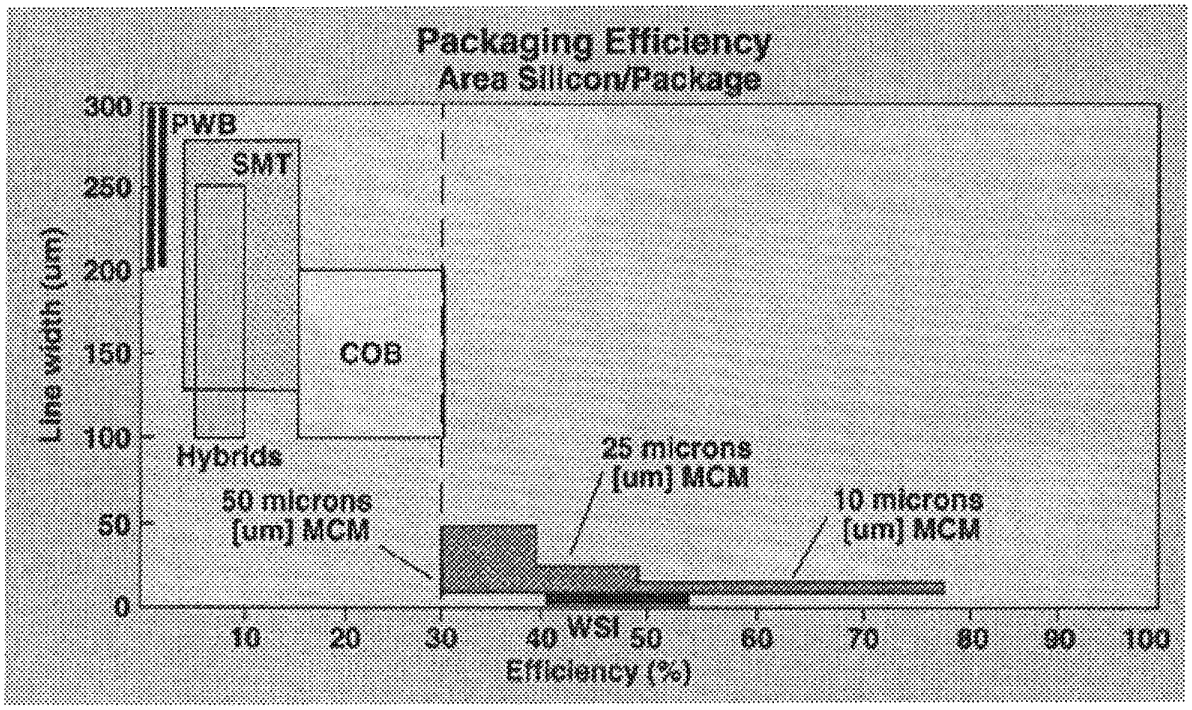


Figure 2.

DP provides each board or module in a digital system with its own local dc/dc converter that is physically located next to the point of load. The advantage with DP deals with the mechanical aspects of typical power supplies and converters. DP provides the designer with converters that are "components" with placement directly on the modules. Past power supplies have been typically large mechanical assemblies installed as bricks or stand alone modules. DP provides significant advantages in modular electronics that use rack type enclosures. Voltages in the two to five vdc range at high current have provided the baseline for distribution to the modules. DP disperses power at a higher voltage in the range of 48 to 300 volts dc or ac to provide lower current. This lower current results in reduced amounts of copper and fewer backplane connector pin usage, allowing pins typically reserved for power to be used for data transfer or special optical or radio frequency. DP can also reduce development cycles by providing converter selections for each board or module developed, vice specific power supply module design and testing. DP supplies can therefore be integrated with your design. System upgrades using DP

provides a way to upgrade modules in a system without requiring power supply module development. Modular power supplies that are packaged as components provide an excellent base for providing on module power conversion or mix and match building blocks for SEM-E packaged power supplies. A number of these components are beginning to be available as off the shelf items from industry.

Standard Electronic Modules.

The SEM effort, as a subset of the larger SHARP, has had to adapt to the changing requirements of a new world order and a new set of conditions. This adaptation is more revolutionary in nature than evolutionary. As a result, the algorithm of standardization has changed to provide faster development while concurrently decreasing the associated costs.

The SEM was first defined over twenty-five years ago, and is currently documented in MIL-STD-1389. Figure 3 and 4. provide basic diagrams of the SEM E format. The first format defined was a module 2.62 x 1.95 inches. This initial format "A" was followed by additional larger formats, the most recent addition being format "E", 5.88 x 6.68 inches, documented in 1988. The philosophy driving the program has been the same throughout: package electronics to a standard form, fit, and (physical) interface, and to develop quality control to produce highly reliable and maintainable electronics for military environments. Use standardized packaging, documentation and quality control to reduce system life cycle cost. The "SEM E" format, one of five SEM formats of SHARP, has become widely accepted as the defacto preferred method of packaging *avionics* circuit assemblies for the DoD. The SEM E format is also beginning to appear in the ruggedized commercial product sector of industry's products. The SEM E requirements can be found in both MIL-STD-1389 and IEEE 1101.4.

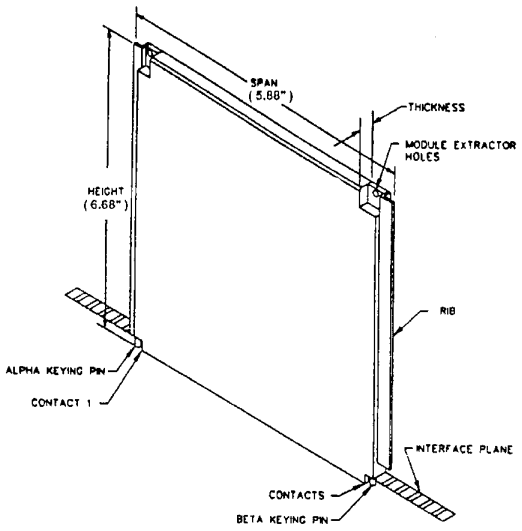


Figure 3.

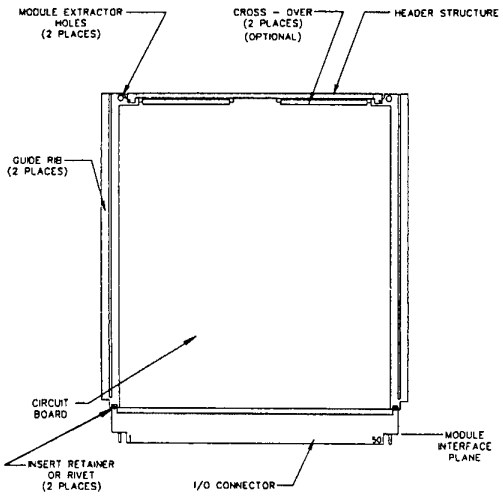


Figure 4.

SEMs have been proven successful in meeting the objectives of improving reliability and reducing cost. The use of SEMs have brought about cost savings of millions of dollars over and above the cost of implementing the SEM discipline into system design and development process.

Considering SEM cost as an investment during development, and life-cycle-cost savings as a return on investment, typical ROI's for SEM average 8:1 over a 10 to 15 year system life.

SEM-E hardware has provided a major advantage in packaging both in the technical sense as discussed previously and also in the OTS procurements. Available SEM-E hardware consists of standard frames, wedge clamps, extraction levers, cross-overs, connectors, covers and interconnect boards. Se Figure 5. The frame serves as a mechanical support and as the basis of the module's other components. For conduction cooled and air flow-through modules the frame provides the major thermal transfer path for heat dissipation from the electrical components. Frames are available in metal, metal matrix and composite matrix materials. The wedge clamps provide the retention of the frame to the chassis and card guide of the enclosure. The wedge clamps also serve to transfer heat from the frame and to provide the structural link to the enclosure card guide. Extraction/insertion levers provide extraction/insertion of the module without requiring external hand tools for removal. Extraction/insertion levers are available in either single piece metal or two piece cam action. Interconnect boards provide the interconnect system for the electrical components. The typical SEM-E is in .4 inch pitch or .6 inch pitch. The .4 inch pitch typically consists of a single interconnect board on one side of the frame. A .6 inch pitch typically consists of a set of two interconnect boards, one on each side of the frame. Interconnect boards are available in either multilayer printed wiring boards or thick film ceramic copper conductors. In the .6 inch pitch modules, a cross over is required to provide signals from one interconnect board to the other. An alternative to cross-overs is a rigid-flex-rigid interconnect board that provides a higher reliability as a single piece. Standard connectors are available that range from 100 pin blade and tuning fork to 396 pin high density blade and tuning fork. The number of pins require matching the pitch of the module because of availability of connectors in matching module pitch. The most common connector for a .6 inch pitch SEM-E is the 396 pin high density blade and tuning fork with the 150 pin blade and tuning fork for the .4 inch pitch SEM-E. Module covers are available that provide electro-static discharge and electro-magnetic interference protection. Standard covers are available in either graphite matrix composite or metal. These standard module components provide a quick turn-around in designing with SEM-E as OTS products.

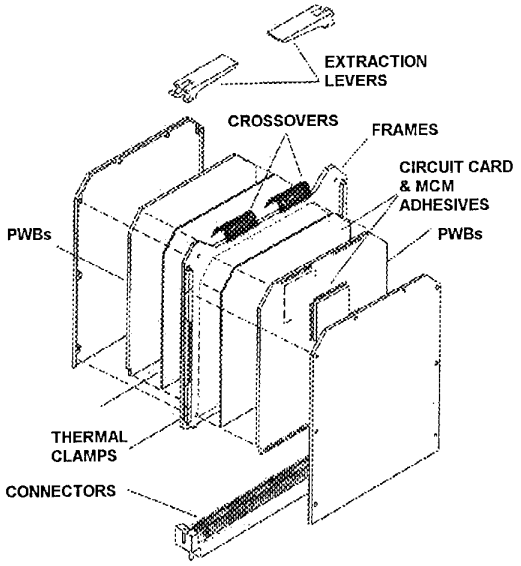


Figure 5.

The Glue.

With the increase in component size and large number of connection pins with MCMs, DP and MMIC technology, single step adhesives become more important. At the same time these adhesives must provide a good thermal transfer of heat from the component to the interconnect

board and onto the frame. Circuit card attachment and component attachment to the circuit card are very important and require experience in these areas. In addition to adhesives, "hot bar soldering" is important with the increasing number of leads the electrical components and connectors employ. Providing a single step soldering process in combination with the adhesive of the component to the circuit card and interconnect board are challenges being addressed.

SHARP has teamed with the EMPF to address the adhesive and soldering challenges through the large working relationship that the EMPF has with industry. In the circuit card to frame attachment arena, extensive contacts in the adhesive community are being leveraged through the EMPF from work on conductive adhesive technology efforts. The EMPF and both of the parent organizations have extensive knowledge in conductive adhesive technology and film and paste/liquid adhesives analysis and formation. For MCM to circuit card attachment, work on device attachment of large flat packs for thermal and mechanical improvements are being applied along with Hybrid Microelectronics module attachment technology to the next level assemblies. Mass lead, connector and cross-over solder attachment is being resolved through expertise in surface mount technology device attachment and connector and wire attachment technology. Both mass and hand reflow expertise is extensive with the EMPF and both parent organizations allowing leverage of EMPF contracts with equipment manufactures for a synergistic improvement to reflow.

The EMPF and parent organizations are working with Raytheon to improve current adhesive and soldering processes and materials through:

- Material suppliers on improved films,
- Investigative development of Ball Grid Array (BGA) technology to negate the need for package attachment adhesives,
- Raytheon and equipment vendors to optimize the equipment and processes,
- Standard reflow processes to integrate cross-over and connector attachment, and
- Investigate development of BGA technology components and processes to negate the need for special parts processes.

Prototyping and Processes.

As part of the ARPA ASEM program, ARPA has initiated efforts to enhance the industry's ability to produce MCM technology in a time efficient and cost effective manner. The major challenge with MCMs in the past has been the lack of accurate data on bare die logical behavior and physical properties that created a major impediment to MCM design and development. The targeted solution and goal is to help develop an industry infrastructure that efficiently provides the necessary bare die information needed to support MCM design and application to electronic circuit assemblies. The objectives of the ASEM are to 1) reduce non-recurring engineering costs by 10 fold, 2) reduce design to product cycle time by 10 fold, 3) routinely achieve first-pass success on new designs, 4) develop applications to stimulate the use of MCM technology, and 5) provide the DoD access to robust manufacturing capabilities.

The missing transition link was packaging those MCMs into the next assembly level. A down select to have an electronics board foundry established and demonstrated was completed. Based on that selection process, an ARPA contract was awarded to the Raytheon Equipment Division. Raytheon is establishing an ASEM Board Foundry to demonstrate the ability to quickly develop, build and test a high density MCM based packaging approach. ARPA and Raytheon felt that the SHARP SEM philosophy of the

development of standard common modular based electronics on a systematic approach to define physically interchangeable and integrated common module building blocks was ideal for this pilot implementation.

The SHARP program, through leveraging 6.2 R&D, IR&D, and 6.3A R&D initiatives with other military and private industry, provides for the packaging technology leaps necessary to fully achieve the performance benefits of MCM technology. The SEM-E format developed and standardized on during the 1980s has become the defacto preferred method of packaging electronics for airborne applications. SEM-E allows for the flexibility in upgrades and new applications based on the module support of either a federated, hybrid or integrated architecture. The SHARP is leveraging this opportunity to increase electronics density and functionality, while reducing the weight, thermal dissipation, development time and cost, and module count of electronics. Raytheon will build and test two SEM-E boards to validate successful implementation of the foundry. A process to evaluate and select the two SEM-E boards is in process. The likely candidates will include avionics applications from the Naval Air Systems Command. The Naval Air Warfare Center Aircraft Division, Indianapolis and the Crane Division of the Naval Surface Warfare Center have been jointly working in support of the SHARP to establish pilot transition of the evaluation boards into acquisition programs.

Old Values, New Techniques.

As discussed earlier, SHARP has been very successful in the standardization (commonality) arena. The same basic concepts, combined with creativity and leverage of industry and the commercial sector, can provide a large change in reducing cycle times and costs for SEM-Es. The concept of providing standard packaging for electronics is being taken a step further in the quest for decreased cycle times and cost for high performance electronics.

This effort reduces the risk in application of dual use technology to military systems and the associated risks of applying high performance packaging techniques, either by revealing discrepancies which are then accommodated, or validating conformance with military usage. Additional benefits include maintaining the dual use application benefits of rapid insertion of technology, decreased development times and costs, increased flexibility, and transition of state of the art commercial technology and processes to military applications.

The keys to this process are applying modeling and simulation at all levels of development and qualification, providing standard chip sets, standard sub-module packaging, and standard SEM-E components to rapidly insert and transition technology to the Fleet. To advance successful rapid prototyping with SEM-E to even higher levels, the following are some keys for further advancement:

- Continued application of standard SHARP SEM-E physical building blocks,
- Standardizing a family of electrical and logical interfaces at the module, MCM and MMIC levels using a consortium of military and industry organizations and users groups, and
- Modeling and simulation improvements to reduce proprietary issues, design verification time and translation to test vector for qualification.

In summary, SEM-E provides the leverage benefits for application of state of the art technology by:

- Supporting Implementation of Multiple Architectures to Meet User's Operational Requirements,
- Allowing Full Application of an Open Systems Architecture,
- Encouraging Application of Existing, Published Military & Commercial

Standards to Foster Competition & Lowered Costs,

- Utilizing An Established Modular Approach to Lowering Life Cycled Cost of Electronics,
- Transistioning Commercial as well as Military Technology,
- Supporting Involvement of Joint Service Technology Demonstrations,
- Allowing Pre-Planned Product Improvement for Rapid Technology Insertion, and
- *Fostering Application of a Standards Based Approach to Lowering Life Cycle Costs of Military Electronics When Appropriately Applied During the Systems Engineering Process.*

RELIABILITY ASSESSMENT OF MULTICHIP MODULE TECHNOLOGIES VIA THE TRI-SERVICE/NASA RELTECH PROGRAM

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INTRODUCTION

Multichip Module (MCM) packaging /interconnect technologies have seen increased emphasis from both the commercial and military communities as a means of increasing capability and performance while providing a vehicle for reducing cost, power and weight of the end item electronic application. This is accomplished through three basic Multichip module technologies, MCM-L that are laminates, MCM-C that are ceramic type substrates and MCM-D that are deposited substrates (e.g., polymer dielectric with thin film metals). Three types of interconnect structures are also used with these substrates and include, wire bond, Tape Automated Bonds (TAB) and flip chip ball bonds. Application, cost, producibility and reliability are the drivers that will determine which MCM technology will best fit a respective need or requirement. With all the benefits and technologies cited, it would be expected that the use of, or the planned use of, MCMs would be more extensive in both military and commercial applications. However, two significant roadblocks exist to implementation of these new technologies; the absence of reliability data and a single national standard for the procurement of reliable/quality MCMs. To address the preceding issues, the Reliability Technology to Achieve Insertion of Advanced Packaging (RELTECH) program has been established. This program, which began in May 1992, has endeavored to evaluate a cross section of MCM technologies covering all classes of MCMs previously cited. NASA and the Tri-Services (Air Force Rome Laboratory, Naval Surface Warfare Center, Crane IN and Army Research Laboratory) have teamed together with sponsorship from ARPA to evaluate the performance, reliability and producibility of MCMs for both military and commercial usage. This is done in close cooperation with our industry partners whose support is critical to the goals of the program. The following manufacturers/technologies are presently, or planned to be evaluated as a part of this program.

nChip Al/SiO2 substrate	MCM-D wirebond
General Electric Cu/polyimide/overlay	MCM-D wirebond
Texas Instruments	3D Cube wirebond
IBM Cu/polyimide	MCM-D wirebond, TAB, C4
Martin Marietta Thick film/SCOB	MCM-C wirebond
Motorola Laminate/COB	MCM-L wirebond
Hughes LTCC/HDMI	MCM-C/D wirebond
ISA Cu/polyimide	MCM-D wirebond, ball grid array

Several tasks are being performed by the RELTECH program and data from this effort, in conjunction with information from our industry partners as well as discussions with industry organizations (IPC, EIA, ISHM, etc.) are being used to develop the qualification and screening requirements for MCMs. Specific tasks being performed by the RELTECH program include technical assessments, product evaluations, reliability modeling, environmental testing, and failure analysis. The following sections will describe the various tasks associated with the RELTECH program, status, progress and a description of the national dual use specification being developed for MCM technologies.

TEST VEHICLES

The RELTECH key tasks described in Figure 1 are focused around the definition of a suitable technology test vehicle. The features defined on the test vehicle are such that a thorough characterization of the MCM technology can be performed during the product evaluation phase, the accelerated and environmental testing phase, and the reliability modeling phase of the respective technology under investigation. The technical assessment tasks of the program help define industry areas of concern related to design, fabrication, assembly and material issues.

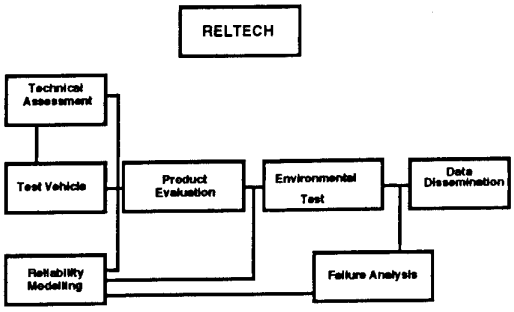


Figure 1. Flow of Work

TEST VEHICLE DEVELOPMENT

The reliability test vehicle is defined by the RELTECH program team working in conjunction with the technology manufacturer. In general, the test vehicles used on the RELTECH Program are designed such that the following attributes are achieved.

. the test vehicle shall examine all major failure modes anticipated.

. structures' representative of the worst case design rules shall be included on the test vehicle.

. the test vehicle shall be representative of production processing.

. the test vehicle shall be packaged in a manner representative of the intended usage.

An existing test vehicle will be used, if possible, however, if all test structures of interest are not addressed, a new test vehicle is proposed. The test vehicle, when finished, is produced in a manner that is characteristic of the MCM manufacturer's production process, and provided to the testing organization in a screened/preconditioned state thus assuring known good test vehicles prior to reliability testing. Correlation of equipment and test procedures are stressed to insure that the support activities and technology manufacturers have test set ups of a comparable nature to the lead activity. As a minimum, forty (40) test vehicles are specified with more added, cost permitting. Though statistically invalid, the sample's size is sufficient to allow the RELTECH program insight into the quality and reliability of the MCM technology under evaluation and screening/qualification tests necessary to exploit any of the potential failure mechanisms. Examples of some of the test vehicles used and the characteristics being addressed are as follows: (I) via chain/kelvin structures for measuring via integrity; (2) triple tracks for measuring corrosion; (3) ring oscillator for performance; (4) Heaters/High Power devices for measuring thermal characteristics; (5) parallel plate capacitor to measure substrate dielectric constant; (6) random access memory for functionality/density assessment; and (7) wire bonded/TAB/Flip-chip devices to evaluate interconnect and die attach integrity.

TECHNICAL ASSESSMENT

The technical assessment task has two primary components including a design review and a process survey. The objective of this task is to develop the baseline knowledge needed to tailor the RELTECH evaluation for the technologies of interest. The design review includes an assessment of the design process to insure that design for reliability, manufacturability, testability, and quality assurance were key components in the development of the technology. In addition, the test and qualification procedures used by the technology manufacturer during the development of the MCM structure is reviewed. The process survey is conducted for each technology selected. The survey provides the baseline necessary to execute the remainder of the RELTECH tasks. The survey also includes a review of all key process steps, process controls, and quality assurance procedures used by the MCM technology manufacturer. This task is performed first before delivery of the test vehicles and subsequent tasks of the RELTECH program.

PRODUCT EVALUATION PLAN

The primary objective of this RELTECH task is to characterize the products, develop a baseline understanding of the test vehicle and MCM process, characterize the thermal performance, and to assess potential quality problems and issues. In addition, materials characterization tests will be performed when possible and as necessary. A multi-technical approach to product evaluation (PE) is used to assess the issues cited previously. The RELTECH product evaluation task builds on the knowledge obtained during the in-depth survey of the technology manufacturer's process lines, accomplished during the technical assessment, and tailors a specific PE flow for that technology and test vehicle. For example, in performing the product evaluation on the nChip process, the following test/inspections would be performed; (1) external visual/photo; (2) Gross/Fine Leak; (3) Residual Gas Analysis (RGA); (4) Internal visual/photo; (5) Bond strength; (6) Die shear/stud pull; (7) Xray or Acoustic Microscopy; and finally on a special PE sample (8) IR Thermal analysis. The IR Thermal analysis is performed using a Barnes Computherm or equivalent infrared imaging system. The imaging system allows for the determination of isolated hot spots as well as measuring the temperature rise on the devices as influenced by the packaging and interconnect technology. Correlation with the modeling task will be performed as a result of the test, to verify the integrity of the respective finite element models.

Materials tests are performed, when needed, to fill critical gaps necessary to successfully model the test vehicle and its respective baseline process. For example, tests would include such things as an evaluation of nonlinear behavior (creep and stress relaxation) expected in polymer constituents for a Cu/polyimide MCM-D process.

All results of this task are documented in Product Evaluation Reports, with detailed materials test reports submitted to the RELTECH team members and the MCM industry partner for their review.

RELIABILITY MODELING

Implementation of the reliability modeling task is designed to achieve two critical objectives. First, develo0p finite element models that allow prediction of the limits of temperature, temperature range, thermal gradients, and vibrational environments necessary to induce over stress in MCM structures and to develop constitutive models and geometric finite element models that predict stresses, strains and temperatures occurring in the respective MCM structures.

CLOSED FORM DAMAGE MODELING

Potential wear out mechanisms will be assessed and a list of available damage models will be developed. Model parameters will be obtained from literature, initial destructive physical analyses, and materials test results. Based on this, a preliminary analysis to bound conditions necessary for failure to occur in NASA and DOD environments will be performed. In addition, minimum test requirements for accelerated environmental testing, necessary for the validation of structural performance, will be evaluated. Results of the closed form modeling and accelerated environmental testing will be used to predict operating life of the MCM structures for various DoD/NASA user environments.

FINITE ELEMENT MODELING

A generic coarse 3-D finite element model of the baseline test vehicle will be developed to allow for the calculation of thermal and structural responses of the MCM structure to various environments. Parametric studies for various environments and material characteristics will be performed to bound stresses and temperatures in major package elements. Upon completion, the models will allow users to select inputs for various boundary conditions including:

(1) Geometric configurations;

(2) Material properties; and

(3) Chip/Device power placement

Generic sub-models of sites of interest or of critical elements within the MCM structure will also be developed, attributes such as these will be developed:

. Vias

. Machined sites within substrate

. Interfaces

- Dielectric to substrate
- Interlevel dielectric
- Via to Chip interconnect
- Chip to substrate

Results of this effort will be correlated with failure analysis and environmental test results to assure robust/accurate models are developed. To date, coarse finite element (FE) models have been accomplished on the General Electric 2-D High Density Interconnect (HDI) structure, the nChip nC1000 substrate/die attach technology and the Texas Instruments 3D-Cube MCM technology. Also detailed models have been accomplished on a via/dielectric structure for the GE-2D HDI and nChip nC1000 substrate. In the area of Closed Form Damage Models, models have been developed for the GE-HDI via/dielectric interface, nChip nC1000 RELTECH Test Vehicle, and the TI-3D Cube. Correlation of closed form models with environmental test results on the 2D GE-HDI test vehicle as well as a coarse FE model on the IBM Copper/polyimide MCM-D test vehicle are in progress.

ACCELERATED AND ENVIRONMENTAL TESTING

The purpose of this task is to define and implement the reliability test portion of the RELTECH program. Other functions of the RELTECH program are used to provide constraints to the test plan proposed for the specific MCM technology. For example, the technical assessment task will provide the necessary information such as defining process details, access to existing test data, and other details that will help determine the basic test matrix established for each technology. The product evaluation phase of the program will assess the physical and electrical characteristics of the technologies to be tested and form the baseline metrics for comparison during and after environmental testing. The modeling portion of this program will provide guidance in the selection of test conditions and fixturing conditions. The actual test matrix, that the selected technologies will be subjected to, will be based on the survey findings, product evaluation results, preliminary modeling, and the technology manufacturer's experience with the selected technology. The test plan will, when completed, define the organizational interfaces, discuss product acceptance and preconditioning required prior to reliability testing, define in a broad sense the types of tests that could be selected for inclusion in the technology specific test matrices, and define documentation requirements. The accelerated environmental tests will be designed to manifest technology failure modes and thus provide a detailed understanding of the failure physics for the technology being tested. The following aspects of long term reliability will be addressed:

. Technology strengths and weaknesses

. Acceptable field use environments

. Process/Material variation affects

. Realistic failure mechanisms

. Fielded hardware expected lifetimes

The RELTECH Steering Committee and their industry partner will determine technology specific failure modes which will be tested in an accelerated manner consistent with material or other limits of the relevant technology, thus forcing failures in a reasonable amount of time. These accelerated stress tests will be designed to minimize the introduction of unrealistic failure modes. Specific test matrices are developed for each MCM technology evaluated, using a variety of tests as shown in Table I.

TABLE I - POTENTIAL TEST METHODS

TEST	BASELINE METHOD
Thermal Cycling	MIL STD 883 TM 1010
Vibration	MIL STD 883 TM 2005
Thermal Shock	MIL STD 883 TM 1011
Mechanical Shock	MIL STD 883 TM 2002
Constant Acceleration	MIL STD 883 TM 2001
Power/Temperature Cycling	JEDEC TM A105-A

High Temperature Storage	MIL STD 883 TM 1006
Radiation	MIL STD 883 TM 1019, 1020, 1021
Steady State Life	MIL STD 883 TM 1005
Salt Atmosphere	MIL STD 883 TM 1009A
Temperature/ Humidity/Bias	JEDEC TM A101-A
HAST	RwoH Test Sequence
Stepped Stress Tests: High Temperature-Bias Pressure-Humidity-Temp. Bias	TBD

Before and during the environmental testing phase of the effort, a log is maintained documenting all actions related to each test vehicle. The technology manufacturer will provide information, as necessary, for each vehicle delivered to the testing organization that details the processing, screening, preconditioning, and any other manufacturing actions the test vehicle experienced. The testing organization will keep detailed logs of all test conditions, chamber adjustments, and test data for each test vehicle. This manufacturing and test data will then be stored in a manner that will allow the RELTECH team to detail all manufacturing and testing actions on each test vehicle such that a detailed environmental history of the test vehicles can be constructed at any time. Furthermore, control samples will be maintained in an unstressed condition to verify basic test equipment/methodology correlation in the event of marginal performance of samples under test. The exact number of control samples is defined in the individual test matrices and the samples shall be randomly selected. The logging of test data and test conditions shall be maintained in a test log. An example of the test matrix for the General Electric High Density Interconnect MCM-D technology is shown in Table II.

TABLE II - GE HDI ENVIRONMENTAL TEST MATRIX

	LOT#			
Environmental Test	1	2	3	4
Control	2	1	2	2
High Temp Storage 150C, 1000+	2		1	1
Power/Temp Cycle -40C to 125C	2	2	2	2
Temp Cycle (-65 - 150C)		2	1	1
Thermal Shock -65C to -150C		2	1	1
Mechanical Shock/ Vibration	2		1	1
Steady State Life	2	2		
Sequential (Thermal/Mech-TBD)			2	2

At the time of this writing environmental testing has been completed on a small lot (3 devices) of General Electric 3D stacked HDI substrates and 22 General Electric 2D HDI test vehicles. Environmental test of the nChip nC1000 test vehicle is scheduled to begin in April 94, followed by the IBM Copper/Polyimide MCM-D test vehicle scheduled for a late 1994 start.

POST TEST PHYSICAL ANALYSIS AND FAILURE ANALYSIS

The general plan that has been in practice at RELTECH member facilities will continue to be followed. After testing and evaluation of the parts, failures will be analyzed for the cause of the failure. The objective will be to identify the specific reason for failure and then feed this information back to the technology manufacturer for possible corrective action.

Basic failure analysis techniques such as ESCA , cross sectioning, Auger, SEM, etc. will be used, as appropriate, to ascertain the cause of failure or to determine the cause of any degradation which may have occurred in the structure. Based on the tests and measurements performed during the product evaluation and environment test phases of

the program, an analysis of the acquired data will be performed to provide a complete reliability assessment, with appropriate technical rationale, for each MCM structure. This analysis will include the following areas as applicable:

a. A description of the MCM screen tests/procedures to ensure quality of materials, processing methods and performance integrity.

b. Determination of the MCM failure sites/elements and types of failures, catastrophic/degradation, classified as they relate to critical parameters in operational use.

c. The establishment of activation energies associated with identified failure mechanisms and mean time between failure (MTBF) extrapolations versus temperature to confidence levels commensurate with the sample size.

d. AC performance versus life (time) and temperature data for each MCM structure.

e. Electrical, mechanical and environmental limitations of the industry process.

f. An attempt shall also be made to correlate DC or AC testing results to establish operating behavior and characteristics under both electrically applied excitation, determine equivalent stress levels (DC vs AC) and using appropriate factors, provide reliability predictions at use temperatures for each MCM structure.

g. Based on failure mechanism analysis, provide and document the necessary corrective actions for MCM reliability improvement.

DUAL-USE MICROELECTRONICS MANUFACTURING SPECIFICATION FOR SINGLE AND MULTICHIP PACKAGING TECHNOLOGIES.

The Dual-Use specification is based on the Qualified Manufacturer's List (QML) philosophy which provides a system designed to demonstrate manufacturer process control. The intent is to extend to MCM technology the QML approach described in MIL-I-38535, the General Specification for Integrated Circuits (Microcircuits) Manufacturing, and Option 4 of MIL-H-38534, the General Specification for Hybrid Microcircuits. Basically, the QML approach is based on the premise that products and services consist of a sequence of processes overseen by a management system. It is a significant departure from the traditional military specification requirements in that it minimizes how-to-requirements and encourages the use of best practices. A management commitment to quality, similar to the ISO 9000 requirement, is to be demonstrated for a given technology. A Technology Review Group (TRG) is to be responsible for insuring that a total quality management approach is used to continuously improve process and product quality. A Quality Management Plan is also required similar to that for ISO 9001 which documents the procedures used to maintain controlled processes and product. The TRG and QM plan are essential to the QML philosophy.

Although the QML is very similar to ISO 9000 by requiring a quality system and documentation, it is specific to microcircuit manufacturing. Emphasis is placed on the areas of design, fabrication, packaging/assembly and testing using a failure mechanism identification/correction action (up front), not a stress test driven (end of line) procedure. Demonstration of technology understanding and process control through use of surrogate vehicles are used to ensure quality, reliability and consistency prior to the fabrication of a particular product is encouraged. These vehicles include: Technology Characterization Vehicle (TCV), to demonstrate control over known failure mechanisms of a technology; a Standard Evaluation Circuit (SEC) to determine long term reliability of product; and Parametric Monitors (PMs) used to insure continuous process control. The QML provides the basis for vendor and product/service selection and demonstration necessary for device performance, quality and reliability, and customer satisfaction.

The processes by which an organization achieves a manufacturing line or technology flow listing on the QML are validation and verification. Through the validation and verification a company demonstrates that the

quality and reliability system it has in place can provide end products or services which ensure customer satisfaction. Validation is the recognition of evidence that the manufacturing line or process is capable of producing high quality and compliant product. The validation team, consisting of industry and government technology experts, measures and evaluates a manufacturers' manufacturing processes against a baseline for that technology. This baseline can include innovative and improved processes that result in a more competitive and higher quality product, provided that the processes are evaluated and approved by the manufacturer's TRG, and documented in the Quality Management (QM) Plan. Again, the proposed procedure is not "how to" oriented but allows candidate organizations the flexibility to describe how his process flow insures quality and reliable product. Verification is the actual demonstration of the validated manufacturing line/process capability. Demonstration device(s) are run through the process and then tested to prove the reliability and quality of the technology. After QML certification of a technology flow, the TRG must strive to meet or improve the established baseline of certified processes, the QM program, and quality and reliability assurance requirements for all products.

TASKS

The following major tasks were established at the onset of the specification development:

- Establish an Industry Coordinating Working Group (ICWG) and hold technical interchange meetings to develop, review and coordinate the new specification, with heavy emphasis on addressing MCM concerns. This approach will strive to maximize usage of expertise from varied technologies and reliability testing.

- Review of applicable documents and specifications. (e.g. ISO9000, MCC/SEMETACH KGD Guideline Documents, JEDEC-26, etc.)

- Prepare Strawman Specification

- Prepare coordination draft

STATUS

The development and coordination of this specification will attempt to assure wide acceptance through the generation and use of an ICWG. This group includes military, industry and academia participants with a broad area of microcircuit background with maximum expertise in the areas of MCMs, hybrid microcircuits and plastic packaging. This team of industry representatives is currently developing the MCM requirements for this specification. Task groups are developing MCM-C,D,L screening and qualification requirements, flip-chip requirements, element evaluation, plastic packaging technologies, and general requirements for the specification.

STRAWMAN SPECIFICATION

The document review has begun and significant progress has been made based on this effort. The effort began with a review of the MIL-I-38535 and MIL-H-38534 documents. These specifications provide the requirements for single chip and hybrid technologies. They also share a common quality system and could be easily merged. A strawman specification is being developed to accomplish this merger and provide a single level of product assurance. The resulting specification, titled "Dual Use Microelectronics Manufacturing Specification for Single and Multichip Packaging Technologies", will contain the quality system requirements that are applicable to all technologies. As stated previously, this is essentially the ISO 9001 quality system with microelectronic concerns provided. The structure for the new specification is based on MIL-I-38535. This merged document provides a complete document for all microelectronics. MIL-I-38535 provided requirements which emphasize fabrication and design control, and addresses Si, GaAs, and preliminary provisions for plastic packaging technologies. More detailed plastic packaging technology requirements are currently being developed by JEDEC 26. MIL-H-38534 provided the hybrid assembly and packaging requirements and the framework for developing MCM requirements. These technology specific qualification and screening baselines will be provided in appendices. The specification format consists of these parts:

- General requirements to be addressed (quality system)

- Technology specific appendices (screening and qualification baseline)

- Supplemental guidelines (background information, e.g., "QM Plan outline")

Although the strawman specification provides a quality system for MCM manufacturing, several MCM specific issues remain to be addressed. To resolve these issues, the following criteria changes/additions are anticipated as a minimum:

- Known Good Die

- Known Good Substrates

- Standard Evaluation Circuit (SEC) Definition (i.e., MCM, plastic)

- Screening and Sample Testing Requirements (i.e., hermetic, plastic)

- Rework (i.e., hybrid, MCM)

- Packaging (i.e., hermetic, plastic)

SUMMARY

This paper has described a joint military/commercial effort to evaluate MCM structures and represents a model for future reliability studies for other technologies. This effort established a government/ind6ustry infrastructure with the intent to discover possible failure mechanisms associated with MCM interconnect structures and substrates, design and implement appropriate cost effective reliabilty and quality assurance procedures and propose corrective actions where applicable. DoD/NASA facilities and personnel have been brought together in a combined effort to evaluate and assure that these devices will meet their application requirements. The reliability data generated through this effort will be supplied to the MCM manufacturers so that they may implement design and process practices which will produce robust structures. Screening and qualification procedures developed under this effort will be documented in a national dual-use specification for MCMs and coordinated with a variety of industry organizations (e.g., ISHM, IEPS, IPC, IEEE, JEDEC, etc.).

REFERENCES:

1. Fayette, D.F., et al. "Reliability Technology to Achieve Insertion of Advanced Packaging (RELTECH) Program," 1993 Proceedings, International Conference on Multichip Modules, Page 514.

2. Gorniak, M., Farrell, J. and Fayette, D., "Dual Use Microelectronics Manufacturing Specification for Single and Multichip Packaging Technologies," 1994 Proceedings, International Conference on Multichip Modules.

DISCUSSION

Question: In the case of temperature cycling data, for example, how did you determine the number of cycles and the temperature range, both being subject[s] of discussion when technology qualification is considered?

Answer: The Multichip Modules under test are tested to failure (either parametric of catastrophic); therefore there is no preset number of cycles to be run. We will, however, record the number of cycles to failure or terminate tests at an appropriate point (e.g., 1500 cycles) if no failures occur. Also, we will attempt to benchmark the various MCM technologies to see how they compare under the same stress conditions. After testing a number of MCM technologies, we will propose a qualification limit for industry acceptance for temperature cycling, as well as other tests such as thermal shock, random vibration, etc.

Question: Do you have any elements on the comparison between COTS and MIL technologies, from the reliability point of view?

Answer: Not specifically. The majority of the MCM technologies being tested are hermetically sealed in KOVAR or ceramic packages. However, nChip, who are predominately commercial, offer their product this way. So, *de facto*, we are looking at a COTS technology. The ISA MCM technology is also commercial driven, however they are non-hermetic and have pad grid array interconnect to the board. Bottom line may not be a difference between COTS and MIL except the final packaging (hermetic vs. plastic). Hopefully, there will be no difference.

ASSURING KNOWN GOOD DIE (KGD) FOR RELIABLE, COST EFFECTIVE MCMs

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SUMMARY

A key requirement for achieving high yield multichip modules (MCMs) is assuring that the individual dice are known good devices (KGD). A KGD is defined as a bare die available at the same quality and reliability as the equivalent single chip packaged parts. Integrated circuits (ICs) that are Known Good will function over a specified temperature range, are compatible with the MCM approach utilized, and contain no short-term or long-term reliability hazards. The application of reliability and testability techniques at all levels of MCM development, particularly at the chip level, will maximize MCM yield. Today's testing and qualification requirements, defined by MIL-STD-883 Methods 5008 and 2010, are not capable of assuring KGD as defined above.

The development of cost effective requirements for achieving 99.9% yields poses a challenge which requires new and novel approaches and better methods for bare die testing, wafer level burn-in, tape automated bonding (TAB), temporary packaging, at-speed device testing at the wafer, die, and MCM level. Also of great importance are the methods for built-in self test (BIST), built-in test (BIT), and boundary scan. New standards in very large scale integration (VLSI) device testing must be developed in order for MCMs to be reliable and economical. Rome Laboratory (RL) has funded a program to address and develop these requirements.

The objectives of the RL program are to: research and evaluate current and proposed burn-in, electrical and interconnect test techniques for assuring known good VLSI circuits at wafer and die level; and evaluate various methods of incorporating testability features which will decrease test time and cost. In addition, MCM-level reliability and performance assessment procedures will be evaluated to determine appropriate testing concepts and procedures that will assure the procurement of reliable, cost effective MCMs for DoD/ NASA applications. The program consists of two phases:

Phase One will be a study phase to evaluate, analyze, trade-off, and select best techniques for test and burn-in of wafers, bare die and MCMs. Also during this phase, techniques for applying BIST, BIT, and boundary scan testability features to die and MCMs will be evaluated to determine their effectiveness in assuring KGD. Analysis of design for testability (DFT) techniques will be heavily emphasized in the study phase. Testability features which will be designed in at the die level and features which can be added at the module level will both be considered. Two VHDL models will be created and simulated. One will involve the testability features added through the redesign of an application specific integrated circuit (ASIC) (i.e., testability at the die level), and one model will contain testability features added at the module level. The study phase will also include a comparison of the advantages and disadvantages of MCM technologies and MCM assembly techniques.

Phase Two will be a demonstration of a cost effective procedure for assuring high quality/reliable production of MCMs based on the KGD methods developed in Phase One. The program, as a whole, is intended to provide a methodology which will provide the industry with cost effective

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qualification procedures for MCMs which can be integrated into the Qualified Manufacturers List (QML) procedures.

The expected results of this program can be summarized as follows:

1. High quality, reliable, and testable KGD.

2. High yielding, reliable, testable, and cost effective MCMs.

3. Standards and specification changes reviewed with commercial manufacturers and Joint Electron Devices Engineering Council (JEDEC) JC-13 committees.

4. QML expansion, and new QML sources for KGD and MCMs.

5. Continued improvement in cost, quality and available sources of KGD.

MCM TECHNOLOGIES

MCMs provide the interconnections for several surface mounted, unpackaged, and active integrated circuit chips, which are subsequently protected by a coating or an enclosure. MCMs offer high performance because their conductors are short, their ICs don't have the surrounding packaging and pins, and the dielectric constant of the interconnect structure is low. As a result, inductance and capacitance are reduced. MCMs can be categorized by the type of substrate that they use; there are three general types. MCM-C is co-fired ceramic. These are MCMs which use thick film technology such as fireable metals to form the conductive patterns, and are constructed entirely from ceramic or glass-ceramic materials. The use of MCM-C can compromise performance because the dielectric constant of the ceramics (generally Er > 5) used is much higher than that of the dielectrics in MCM-L or MCM-D (where Er < 3 are available).

MCM-L (L for laminate), are MCMs which use laminate structures and employ printed circuit board (PCB) technologies to form predominantly copper conductors and vias. The maturity of PCB technology makes MCM-L a good low cost solution for applications involving ICs of relatively low pin counts with moderate performance and thermal requirements. The technology is not appropriate for designs incorporating multiple high pin count ASICs or processor ICs because the technology has limited routing capacity and performance. Currently, there is much activity in making MCM-L more viable for more demanding MCM designs (for high density, high power, high speed applications).

MCM-D (D for deposited), are MCMs on which the multilayered signal conductors are formed by the deposition of thin film metal on unreinforced dielectric materials over a support structure of silicon, ceramic, or metal. MCM-D offers substantially greater interconnect density since the interconnect lines are defined by high resolution IC-like photolithography[1]. Higher routing density allows ICs to be placed closer together, thereby reducing interconnect lengths.

With the development of MCMs comes the development of assembly techniques and processes for these devices. Various assembly techniques for MCMs, methods for connecting chips to the interconnect substrate, include wire bonding, TAB, and flip chip. These three major techniques will be evaluated, and one process selected to be used in the Demonstration Phase. Topics which will be examined in the study phase include premount electrical test and burn-in capability, process maturity, chip availability, high frequency performance, development cost, process complexity, maximum die I/O count the process can handle, reworkability, power dissipation capability, reliability, and flexibility.

WIRE BONDING

Wire Bonding is a technique where bond wire is used to connect the pads of the bare die to corresponding pads on the ends of the substrate interconnection paths. The bonding wire is identical to that used for IC assembly, as are the bond formation methods. Wire bonding is most practical

for low lead count devices. It is a labor intensive process, as it requires two bonds to be made per connection. There are three methods used to create wire bonds: thermocompression, ultrasonic, and thermosonic. In thermocompression bonding, the wire is pressed against the bond site metal at an elevated temperature. As gold deforms easily at elevated temperatures, and will have no surface oxide to inhibit bonding, it is typically used. During the bonding process, the bonding surface is heated to approximately 400 degrees C. A major advantage of thermocompression bonding is that the bonding head may move in any direction to make the second bond, once the first bond is completed. This allows for bonding of all pads around the periphery of the die without rotating the substrate. Also, no unique fixturing is required.

Ultrasonic bonding uses ultrasonic energy to bond wires to die and substrates. Aluminum wire is generally used, and the bonding is performed at room temperature. Insensitivity to surface contamination is the major advantage of ultrasonic bonding. Another advantage is the fact that aluminum alloy wire is approximately twice as strong as the annealed gold wire which is used for thermocompression and thermosonic bonding. Ultrasonic bonding has two primary disadvantages. One, the process is unidirectional. The bond head can only move in one direction from the first to the second bond. Therefore, the substrate must be rotated numerous times to create all the bonds around the entire device. Acoustical energy is hard to measure. This makes the ultrasonic bonding process hard to characterize and control.

Thermosonic bonding is a combination of ultrasonic and thermocompression bonding. The substrate temperature is lower than that used with thermocompression bonding, as a burst of ultrasonic energy is used when each bond is formed. Its disadvantages include the necessity of a special fixture, and the requirement of acoustical energy[2]. Wire bonding, in general, is a proven technology with a long history of field reliability. Many manufacturers offer equipment and supplies for it, its processes are well characterized, and its limitations are well known. Several disadvantages to wire bonding include bond wires that are inductive at high frequencies, and limiting of density due to the space needed by assembly equipment.

TAB

TAB is a bonding technique which uses a tape having plated, single of multilayer conductive pattern(s) etched onto it. The tape has a central cutout for each die, with pads located around the periphery of the cutout that match the die bonding pads. These pads are termed inner leads, and bonding them is referred to as inner lead bonding. The gold plated leads on the TAB tape are joined to the gold bumps on the die via pulse tip thermocompression bonding. A gold bump is simply a deposit of gold on the die which is used to ensure accurate placement. With TAB, the die are in contact with, but not directly affixed, to the substrate. Therefore, there is no material between the back of the dice and the substrate which can be used to conduct heat. Heat must be dissipated to the ambient through the TAB tape or directly to the ambient from the surface of the die. The advantages of TAB include increased numbers of dice per unit area, and reduced cost of the substrates. Signal line connections in TAB tapes exhibit parasitic capacitance, resistance, and inductance. The inclusion of a ground plane into a multilayer TAB tape structure can greatly improve performance, especially at high frequencies[3]. TAB's disadvantages are costly materials, and the fact that the assembly equipment is designed for a specific application. The equipment is inflexible, and therefore only practical for manufacturing in large volume.

FLIP CHIP

Flip chip refers to the bonding of dice directly to pads on the substrate in a face-down orientation. Flip chip provides the shortest interconnection path from die to substrate, and thus is excellent for high frequency applications. Flip chip dice are

prepared by using multiple plating operations that place a specific thickness of a tin lead composition on the bonding pads of each die. These, then, mate with matching pads on the MCM substrate. Precision alignment during bonding is a requirement. Assembly throughput is quite high, as all the connections are made simultaneously. Die-to-die spacing for flip chip MCMs are the smallest of any assembly technique. This is the case because all interconnections are within the substrate. Thus, no bonding wire or TAB tape interconnect is required. However, this adds cost as precise manufacturing of substrates is necessary. Another disadvantage is that the flip chip devices are difficult to inspect since the dice are face down and the bonds are under the dice.

A critical issue facing all MCM packaging approaches is the yield of the chips in the module. Wafer testing is generally not a full functional test, not at temperature, and not at device operating speeds. These tests are not done until the wafer has been diced and the separate chips have been packaged. However, the die which are to be used in MCMs are unpackaged - "bare die". This has created the need for "Known Good Die". Semiconductor manufacturers came to market with KGD starting in 1992. The screens applied to these die ranged from wafer level test at room temperature, to high temperature tests, to die level burn-in. MCMs will benefit from KGD by an improvement in both module yield and reliability.

KGD ASSURANCE TECHNIQUES

A great deal of time and money have been spent to improve device level test and burn-in (DLBI), to assure KGD. The complete DLBI system is comprised of several parts: the bare dice, carrier, lid, socket, and test board. In order to perform DLBI, the bare die is placed in a carrier. Carrier types include permanent, semipermanent, and temporary. Permanent carriers are a form of package that is integrated into the next level of assembly. In semipermanent carriers, the die is forcibly removed from the carrier before assembly. The carriers present the challenge of removing the die, after test and burn-in, without damage to the die. With a temporary carrier, the die can easily be released from the carrier before assembly. Temporary carriers have the potential to provide the most generic solution.

A DLBI method recently developed jointly by Texas Instruments and MicroModule Systems provides a good example of a KGD carrier system. The bare die carrier holds the die to the high density interconnect. The die is placed face down in the carrier and is held in place by the lid, which also acts as a heat sink. The die carrier is then placed in a socket. Signals travel from the die contact points through the high density interconnect to the sockets contact points. No visual or automated alignment is necessary as a "fence" - a die holding mechanism assures the alignment of the die with the contact points. A temporary die carrier and a reusable socket are used to drive down the system cost[4].

In general, a number of experiments are used to prove the feasibility of such a system. Die contact to carrier and carrier to socket resistance should be monitored. To show that the contacts are maintained, the resistance measurements should not vary. Another concern is contact durability, this can be defined as the constancy of contact resistance when using different die in the same carrier. Reliability of the system also needs to be analyzed. Die related reliability concerns include environmental contamination, damage to bond pads, and damage to die passivation layers. Carrier reliability factors include contact point reliability and durability, and substrate integrity. Wire bond pull test, combined contact resistance measurement, and vibration testing are several of the methods used in evaluating the reliability of the system.

For MCMs, the approach used to produce the KGD is unimportant to the users of the die. However, for semiconductor manufacturers, providing KGD places a growing burden on the final manufacturing operation. Equipment for the test, burn-in, and handling of the bare die each add

to the cost of assuring a KGD. Considerable simplification, at least from the manufacturers point of view, would be possible if the product of the wafer fabs were "Known Good" wafers. This has created great interest in the technology of wafer level test and burn-in (WLBI). Semiconductor manufacturers will continue to drive WLBI technology development because of the anticipated reduction in cost and cycle time. MCMs have not only created a need for KGD, they have also brought about the need for new testing methodologies and advanced methods of design for testability (DFT). MCMs stress the limits/capabilities of chip, substrate, module, and system test. To be cost effective, MCMs must be designed with test and fault isolation as a critical design requirement.

DESIGN FOR TESTABILITY (DFT)

Incorporating BIST is one way of enhancing testability. BIST simply lets the chip test itself. Part of the chip contains test circuitry which generates inputs to the functional circuitry. The output of the functional circuitry is captured and checked to verify the results. There are two basic categories of BIST, on-line and off-line. On-line, or concurrent BIST, runs concurrently with the normal mode of operation of the circuit. Off-line BIST requires the stopping of normal operation to perform the test. Redundant logic, self-checking logic, and built-in logic block observer (BILBO) registers are among the most common approaches to BIST. Redundant logic involves using duplicate circuitry. The duplicate circuitry runs in parallel with the functional circuitry, and the outputs are compared. When the outputs differ, an error has occurred. Voting and error correction can be implemented through the use of multiple redundant logic. The large amount of extra circuitry, slower speed, and increased power dissipation are disadvantages of this method. Self-checking circuitry operates in parallel with functional circuitry, and is used to monitor parity or error correcting logic. A parity check acts on a wide data, address or command bus to detect one or more errors. Error correction also acts on the bus but has the ability to detect which bit or bits are in error and corrects them. Substantially, more circuitry is involved in error correction than error detection. BILBO registers are linear feedback shift registers which implement prime polynomial dividers to generate pseudorandom patterns. These patterns are applied to the functional logic to initiate a test sequence.

Boundary Scan is a structured digital DFT technique which places a scan path around the periphery of a device's logic. Its main purpose is to provide test access for verifying the integrity of the bond wires and interconnect at the MCM level, by means of a 4-wire serial bus. Boundary scan is structured by IEEE standard 1149.1. Boundary scan involves associating memory cells with each input and output of every device, so known signals can be sent across intervening interconnections and captured for observation. Having access and control of IC boundaries allows for control of input/output signals. It also provides a gateway to internal device logic.

The following sentences give a general description of a boundary scannable device. First, boundary scan cells are attached to each device I/O pin. The serially connected boundary scan cells form a shift register from the test data input (TDI) pin, around the device, to the test data output (TDO) pin. The boundary scan logic is composed of an instruction register (IR), instruction decode logic (IDL), and a test access port (TAP). Under normal operating conditions, the boundary scan circuitry is in reset mode. This allows the device logic to operate unimpeded. During its test mode, boundary scan logic responds to a test access protocol through the test mode select (TMS) and test clock (TCK) input pins[5].

Boundary scan allows for three main types of testing, external, internal, and sample mode testing. Verifying the connection between the IC and the external test equipment or other ICs is known as external test. Stuck-at, bridging, and open circuit faults can be detected. Internal test allows individual components to be tested

as if they were free standing devices. Boundary scan by itself does not test the logic, it only provides access to the IC. The scan path will allow serial vectors to be applied statically to the device. This is very time consuming. Boundary scan in conjunction with at-speed BIST circuitry would be extremely more effective. Sample mode provides monitoring of the device I/O pins during normal operation of the system, without affecting operation.

MCM TEST

The testing of MCMs is a difficult task because of the complexity of MCMs and the fact that there is no established infrastructure to support MCM testing. The testing of an MCM requires combining the features of a multilayer board tester and an IC tester. An IC tester performs functional, at-speed testing, and has full parametric capability. A board tester must be able to test an assembly of 100 or more ICs. A board tester does not test function-ality at the gate level, but only insures that components were successfully interconnected to the board. This testing is not done at-speed. The board test does sufficient testing to verify that 100% of the component I/Os are functioning[6]. An MCM tester must be able to test the assembly at full clock and data rates. With MCM test development, a model is needed of the whole MCM function. In order to get such a model, one needs models of the individual chips, models in a common format, and a simulation platform that can merge the chip models together. These requirements need to be considered when developing the test strategy.

TEST STRATEGY

The characteristics of the particular module determines which test procedures are most applicable. The optimal test strategy will be created using three basic steps. First, decide what test to perform. Second, generate the test vectors, and Third, apply the test vectors. MCM test approaches can be considered to be based on either board or IC testing. The IC testing approach is basically a full functional test. Through the use of a chip tester, an MCM can be fully tested in a matter of seconds. Chip testing provides no fault isolation or diagnostic information, and if the chip contains passive analog devices, it will be impossible to test using the chip tester. Therefore, the IC testing approach is effective only for simple nonrepairable MCMs[7]. Board testing includes such techniques as boundary scan testing, built-in test, and partial functional testing. These techniques require the use of DFT techniques to be used when the module is being designed. The degree to which DFT was incorporated in the module will affect how the test is performed.

After a test strategy has been selected, the next step is to develop the test vectors. Board testing systems can be used to automatically generate tests for boundary scan. However, functional tests normally require some vectors to be written manually. In many cases, a large number of the test vectors can be borrowed from the test code for the printed circuit board (PCB) that the MCM is replacing.

How to apply the test vectors is the final step in the test development process. Very large scale integrated (VLSI) IC testers are very expensive. As most IC manufacturers already own them, they would like to use them in testing the MCMs. In many cases the testers can be used to test circuits with boundary scan. It is more difficult to test circuits that contain BIST. Board testers often have pattern libraries that support many common IC types, but chip testers do not. This adds difficulty to getting the vectors in the proper format. Also, when using BIST the chips must be tested individually. This means that the other chips must be isolated. With board testers, software can be used to apply isolating patterns. Chip testers do not have this capability; they require the development of a special set of vectors to handle the chip isolation problem.

To save on equipment cost, it is desirable to pick a test strategy that can be performed with existing equipment. In many cases this results in a less than "optimal" test strategy. For now, there is no generalized or optimal solution to MCM testing. With

increased production of MCMs is expected to come the availability of more MCM specific test equipment in the near future.

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The Design and Manufacturing Development of an Active Silicon Substrate MCM.

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ABSTRACT

The demand for engine control systems with reduced weight, size and cost, increased integration, improved reliability and higher temperature operation drives the system designer to the use of advanced hybrid assembly technologies. This paper describes the design and manufacturing development of a silicon based 'D' type multichip module, MCM, containing an active substrate of memory. This CPU module is one of the building blocks for a range of generic engine control systems. The active substrate approach potentially gives higher packing density than wafer scale due to its 3D configuration.

The active substrate comprises 12 SRAM 128K × 8 bit of diffused memory arranged in groups of three. The design is organised so that a 'memory manager' ASIC selects pages of good memory from the substrate die thus obtaining the best possible yield.

A single wafer contains 4 silicon hybrid substrates, each approximately 40mm sq, which will be processed before separating into discrete circuits. The MCM structure is comprised of four aluminium metallization layers with benzocyclobutene, BCB, as the dielectric.

Approximately 16 other devices including a processor, the memory manager ASIC, a Processor Support ASIC and EEPROM, plus resistor network chips and decoupling capacitors will be added to the silicon substrate using adhesive and wire bond interconnection. The 'memory manager' ASIC tests the RAM on power-up, reject areas of bad memory and configures the good areas such that a continuous block of functional RAM is available to the processor. The RAM is configured as 16 bit wide with both 16 bit and 8 bit read/write accesses being supported.

The total module is to be assembled in a high temperature co-fired ceramic package with 200 I/O. After test and any rework that may be necessary the package will be sealed with a Kovar lid ready for final test.

This program of work was carried out within the European EUREKA Project JESSI T9 Silicon Hybrids.

1.0 Introduction

The demand for engine control systems with reduced weight, size and cost, increased integration, improved reliability and higher temperature operation drives the system designer to the use of advanced hybrid assembly technologies. This report describes the design and manufacturing development of a silicon based 'D' type multichip module, MCM, containing an active substrate of memory. This CPU module is one of the building blocks for a range of generic engine control systems. The active substrate approach potentially gives higher packing density than wafer scale due to its 3D configuration.

The active substrate comprises 12 SRAM 128K × 8 bit of diffused memory arranged in groups of three. This gives a possible available memory of 1.5M bytes, at 100% yield wafer, against a requirement of 1M bytes. The design is organised so that a 'memory manager' ASIC selects pages of good memory from the substrate die thus obtaining the best possible yield.

A single wafer contains 4 silicon hybrid substrates, each 40mm sq, which will be processed before separating into discrete circuits. The MCM structure is comprised of four aluminium metallization layers with benzocyclobutene. BCB, as the dielectric.

Approximately 16 other devices including a microprocessor. the memory manager ASIC, a CPU ASIC and EEPROM will be bonded on to the top layer of the substrate using adhesive and aluminium wire bonding for interconnection. Also resistor network chips and decoupling capacitors will be added to the module using adhesives.

The Memory Management ASIC will provide the interface between a 68020 microprocessor and an array of 128k X 8 static RAM devices fabricated in the silicon substrate of a multi-chip module.

The ASIC will test the RAM devices on power-up, reject bad memory areas and configure the good areas such that a continuous block of good RAM is available to the processor. The RAM will be configured as 16 bit wide with both 16 bit and 8 bit read/write accesses being supported. The RAM interface will not require the use of processor wait states.

Error correction techniques will be used to continuously correct single bit errors and detect double bit errors occurring within the selected good RAM areas.

The total module is to be assembled in a high temperature co-fired ceramic package with 200 I/O. After test and any rework that may be necessary the package will be sealed with a Kovar lid ready for final test.

2.0 Active Substrate

The active substrate selected for this module was the MHS/Temic 65608 SRAM memory device. This device is currently being developed by MHS/TEMIC using the new 0.5μm technology. Each device on the wafer has available 128K × 8, 1Mbit SRAM. The wafer is 125mm diameter which enables four substrates of approximately 40mm sq to be made on it using the Industrial Microelectronics Center, Sweden, (IMC) benzocyclobutene, (BCB) dielectric process. Each substrate will have an array of six by two (12) memory die which will be interconnected to form the active substrate memory.

3.0 Memory Management

3.1 RAM Configuration

The ASIC will interface with twelve 128k X 8 static RAMs connected to provide four blocks of 128k X 22 (16 data bits plus 6 error detection/correction bits). Each RAM block will have an independent address, data and control interface with the ASIC. If any RAM block is totally unusable then all the ASIC outputs to that block will set to a high impedance state. The RAM will be configured as 512 pages of 1k X 22.

On power-up the external RAM will be tested under control of the ASIC. There will be a two bit register associated with each page. One bit will indicate that the page is unusable due to addressing faults or uncorrectable multiple bit errors, the other bit will indicate that the page contains one or more correctable single bit errors.

Following completion of the external RAM tests the RAM will be configured to provide a continuous block of RAM for use by the processor. This will be achieved by using a block of internal RAM to provide a look-up table to translate the processor address into the actual RAM page address. The internal RAM will contain 384 X 15 bit words (9 data bits plus 6 error correction bits). Thus a maximum of 768k bytes of RAM will be available to the processor. The internal RAM will initially be filled with the addresses of totally error free external RAM pages, if there are less than 384 of these then the remainder will be filled with the addresses of pages containing single bit errors. The numbers of error free pages and pages containing single bit errors, the total number of usable pages, and the current state of the testing/configuration process will be made available in processor readable registers.[1]

The RAM testing and configuration will be completed within 50ms of power-up.

Once the external RAM is configured it will be available for read and write access by the processor with zero wait states. Byte writes will be accommodated by use of a read-modify-write cycle controlled by the ASIC, this will be transparent to the processor.

3.2 Error Detection and Correction

Error detection and correction will be performed continuously on both the external and internal RAM. Error correction code will be generated on every RAM write and checked on every RAM read. The codes used will be able to detect and correct all single bit data errors and detect all double bit errors. An error will also be generated if the processor attempts to access RAM outside of the usable configured area.

All errors will be flagged to a processor readable register, this register will be cleared by the ASIC following a processor read or by a hardware reset.

If a double bit error is detected (either on the External RAM or the Internal RAM), or if the processor attempts to access RAM outside of the usable configured area, a hardware output will be asserted to put the system into a safe state.

4.0 External RAM Testing

4.1 Overall Description

On power-up (or when requested by the processor) the four blocks of RAM will be tested in parallel. Addressing tests will be performed to check the address decoders within the RAM devices and detect stuck address lines. All data locations will then be tested to detect stuck-at-zero and stuck-at-one faults.

4.2 Addressing Tests

These addressing tests will not make use of the error detection/correction circuits.

The ten LS address bits used to select between the 1k words in each page will first be tested since failure of any of these bits results in the entire block of RAM being unusable. If more than two data discrepancies (to allow for single data bit errors) are found at any address then the RAM block will be declared unusable and no further testing will be performed on the block.

Once the testing of the LS address bits has been completed successfully the seven MS address bits used to select between pages will be tested in a similar way. Failure of a particular address will cause that page to be declared unusable by setting the appropriate error bit.

4.3 Data Tests

The error detection/correction circuits will be used during these tests to detect faulty data bits.

Data will be written to the entire block of RAM. For the lower half the address of the data location will be written to each data word, for the upper half the inverse of the address will be written. All the data will then be read back and single or multiple bit errors recorded by setting the appropriate error registers. The test will then be repeated with inverse data (to ensure that both stuck-at-one and stuck-at-zero faults are detected).

If "Test Mode" is selected the data tests will be shortened by only testing every 128th data word. This is to facilitate simulation of the ASIC design.

5.0 Design

5.1 Substrate Design Philosophy

The substrate technology to be used for MCM substrate is the IMC four metal layer/BCB process. This involves depositing a passivation layer of BCB, benzocyclobutene over the SRAM active substrate wafer and curing. BCB has an excellent planarising capability over relatively rough surfaces such as the steps in the die structure and the scribe tracks. This enables subsequent layers to be easily deposited and processed over the basic dielectric passivation layer. Photolithography techniques are then used to etch holes through the BCB so that contact can be made to the wire bond pads on the memory die. The wafer is then coated with an aluminium layer by sputtering and again photolithograph and etch processes are used to make contact to the memory die bond pads and form the first tracking layer. This procedure is repeated a further three times to create three more tracking layers. The top layer of the structure having the wire bond pads for the die which will be assembled on the top surface. A passivation will be deposited over the rest of the surface of the MCM for protection purposes. See Figure 1 showing general cross section of the structure.

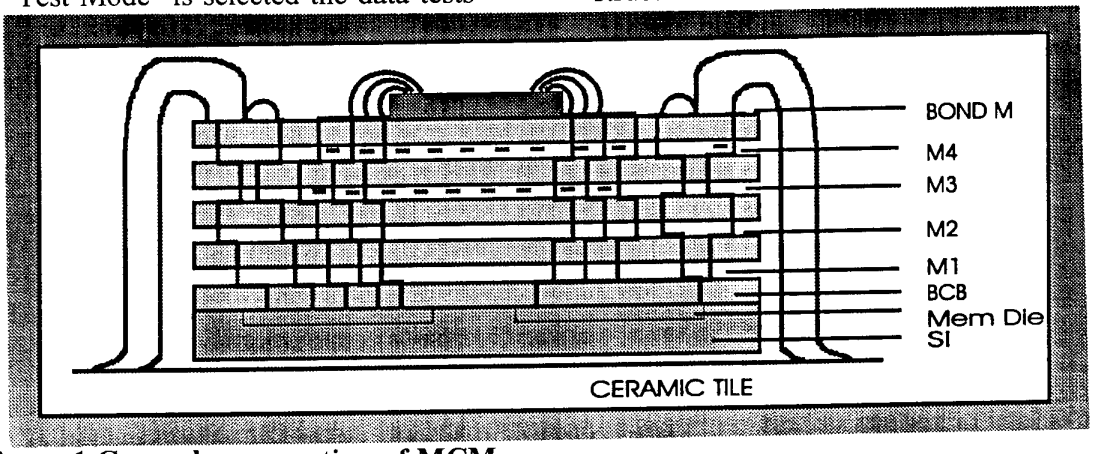


Figure 1 General cross section of MCM.

So that this MCM can be used in a variety of applications the strategy of the design has been formulated so that part of the structure is general to the memory and part specific to the Lucas CPU application. The SRAM memory die on the substrate are grouped in blocks of three and are connected to the memory manager ASIC in regular arrays. Thus the total MCM substrate contains four blocks of three SRAM die. The first two metallization layers of the MCM are used specifically to interconnect all the bond pads on the SRAM die and bring them to a convenient point so that they can be readily wire bonded to the memory manager ASIC, (MM ASIC), on the top surface. Also in the first two levels the power and ground rails are connected in groups of three and taken to a suitable position on the substrate so that they can be bonded to the external package. To avoid the problem of any possible shorts in the SRAM die the power rail from each individual die will be taken to a wire bond pad adjacent to the power rail. Thus when the substrate is completed the individual die will be probed and powered up to see if any short circuits exist. If not a wire bond interconnection from the bond pad to the rail will be made during the final assembly stages.[1] See Figure 2. As redundancy has already been built into the design by use of the MM ASIC, this creates a generic MCM memory substrate which can be used in a variety of applications.

In this case the top two layers of interconnection are application specific to this CPU and will interconnect all the other components on the top surface. This includes the Processor Support ASIC, the 68020 processor, the flash memory and other components.

5.2 Layout Strategy

The circuit was laid out using the Cadence MCM Allegro software directly from the schematic capture of the circuit diagram.[2] Signal tracking was designed using 25μm lines and spaces whereas ground and power tracks were at least 50μm wide.

The high density of the signal tracks is illustrated in Figure 3. The individual substrates on the wafer were approximately 40mm square so that four circuits could be manufactured from a single active substrate wafer.

Physical symbols were prepared using Cadence's Allegro layout system. These symbols were derived from component data sheets for the die and by importing GDSII files from an external system for the embedded components. Contained within symbols are connection points, wire bonds and bond pads, symbol geometry and restricted areas for connections, vias and component clearance. The substrate outline was generated and used as the base

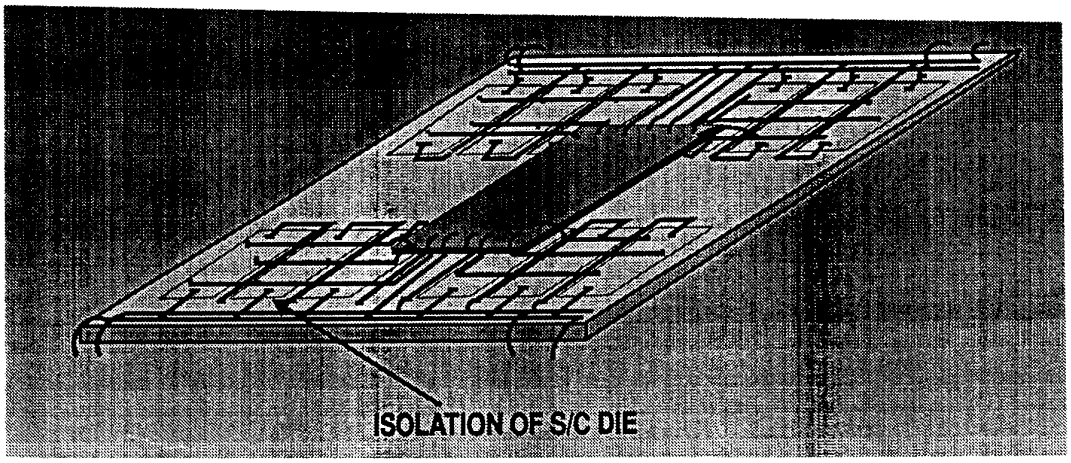


Figure 2 Organisation of memory on the with unconnected S/C block of SRAM.

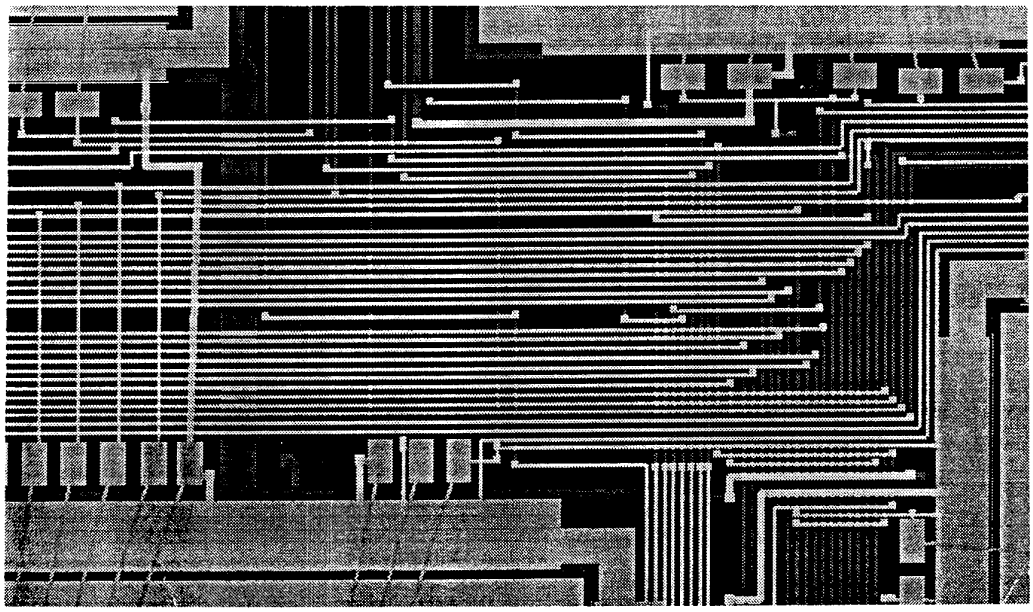


Figure 3 Illustration of high density 25μm lines on 50μm pitch.

file for the layout to be started. Physical, spacing and electrical rule sets are generated for component and signal groups within this database.

Once the front-end data and physical symbols were created, the physical layout could be started. Manual placement was used to position the die on the substrate due to the positional requirement of the MM ASIC and its relation to the other components on the top surface. The cross section was defined, detailing materials used, metal layers, dielectric layers and passivation coverings. Prior to routing, the layout was evaluated to identify potential bottlenecks for via placement or routing channels. This analysis referenced the cross section, physical, spacing and electrical rules and via sizes to produce a density map across the design.The map provides a visual check and any trade- offs to be determined, such as adding or deleting layers, modifying design rules and so on. The benefit to the layout designer is the ability to determine potential design changes before routing begins.

Critical signals were identified and routed, either automatically or interactively. These signals used then verified to ensure that noise sources and timing characteristics were acceptable. The remaining signals were then automatically routed, using a combination of blind and buried vias to conform to the design process rules. The benefits of constraint definition at the schematic capture stage are realised during this phase of the design process. Both automatic and interactive editing continually checked these constraints, highlighting all violations that occur. This methodology, known as correct by design (CBD), ensures that both manufacturing requirements and electrical performance are satisfied, culminating in right first time design.

This design strategy was carried out by tracking the metal 1 and metal 2 first, these being specific to the SRAM memory wafer. This area was then locked for further tracking so that only tracking for the application specific functions of the CPU section were carried out in metal 3 and metal 4 layers.

6.0 Manufacture and Assembly

The active substrates will be processed at IMC to create the four layer aluminium/BCB interconnect structure. After capacitive testing the substrates will then be assembled into high temperature co-fired ceramic packages. These will be in

the flat pack form for surface mounting with 200 I/O. The substrates will be attached using an epoxy film adhesive. The package has a 45mm × 45mm cavity and has been designed to take some additional components which were not suitable for mounting on the silicon active MCM substrate. At this stage all other components will be assembled onto the silicon substrate using a thermoplastic adhesive so that rework can be carried out readily if required. Wire bonding will be carried out using an automatic aluminium wire bonder. Test will then be carried out prior to lid seal. When satisfactory the total assembly will be vacuum baked at 125°C and then seam sealed with a Kovar lid in a dry nitrogen atmosphere.

Environmental testing will then take place over the full miliary specification range to prove the technology prior to introducing into product.

7.0 Summary

The design and manufacturing development of this MCM using an active substrate and redundancy in the memory has produced a module which has reduced the real estate taken by conventional technology by a factor of at least four. By eliminating a level of interconnection, the solder joints of the conventional components, the reliability of this design has increased by at least an order. This is essential for the modern technology now required with increased integration and functionality in the safety critical systems needed for today's and future aircraft both in the military and civil fields.

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HIGH DENSITY MONOLITHIC PACKAGING TECHNOLOGY FOR DIGITAL/MICROWAVE AVIONICS

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SUMMARY

There has been a need for generic technologies and common approaches in design, development, and manufacturing of military and commercial products. This need is more pronounced and pressing today than ever before. With the objective to dramatically enhance avionics reliability, maintainability and availability (RM&A), an integrated, generic technology for packaging, cooling, and interconnection of high density and high performance circuits was developed. It is named High Density Monolithic Packaging (HDMP). Under the sponsorship of Wright Laboratory, a two-part complementary program (1990-1994), named Advanced Radio-Frequency Packaging/ARFP was contracted to Westinghouse. Under the ARFP program, the HDMP technology is being applied and its promising capability is being assessed for its ability to reduce the low power RF avionics life-cycle cost. Being better than half way through the program, the results and projections have been extremely promising. The technology assessment is approximately 50% complete and initial results have been extremely successful.

Although the focus of the development effort has been on RF subsystems, the basic elements of HDMP technology have applications beyond RF/microwave subsystems. As digital processing speeds increase, RF/microwave design techniques must be applied to maintain high speed digital signal integrity. The basic elements of the HDMP technology are: low temperature co-fired ceramic (LTCC), solderless interconnects, multichip modules (MCMs), and composite heatsink materials. The key technology element, in this avionics availability enabling technology, is LTCC.

LTCC material technology is a monolithic multilayered ceramic and conductor/metallization structure used as a substrate to support dense co-habitation of high density electronic circuits, their interconnections, and the electromechanical integrity of the integrated constituents. Based on the intended application, LTCC/HDMP technology can be used as a generic vehicle and the means for:

1. Packaging and interconnection of high density circuits (monolithic microwave integrated circuits/MMICs and the very high speed integrated circuits/VHSICs) in the form of MCMs. To distinguish the specialized nature of RF/microwave MCMs, this packaging configuration is referred to as an integrated microwave assembly, or IMA.

2. The assembly and interconnection of IMAs and MCMs onto planar or into large multicavitied substrate/motherboards to form higher integrated assemblies. HDMP technology has also demonstrated the ability to support built-in-test (BIT) capability for RF SEM-E modules. This capability is consistent with the two level maintenance concepts that have typically been applied to digital systems to reduce life cycle costs.

Results have shown that HDMP is capable of dramatically reducing the weight, volume, and life cycle costs of RF subsystems. Based on these results and technically sound projections, the technology can provide a vehicle for the common use of the basic technology elements (MMIC, VHSIC, high density hybrid circuits) and approaches in design, development, and manufacturing of military and commercial products.

BACKGROUND

There is a need in existing and future avionics systems for a dramatic increase in reliability and maintainability (R&M), reduced weight/volume and life-cycle cost (LCC). Future systems are continuing to require advanced capabilities within the existing electronic volume. Beyond the need for performance enhancements, a greater emphasis is being placed on the need for high reliability and a two-level maintenance concept for improved availability and overall system cost effectiveness.

In the past decade, tremendous progress has been made in reducing the volume required for digital electronics, while also improving reliability and maintainability. The emergence of highly integrated, high speed digital device technology has been key for advancing digital systems packaging. The availability of these technologies has enabled integration standards to evolve at all electronic packaging levels. Standard Electronic Module (SEM-E) sizes and interfaces, in conjunction with enhanced BIT capabilities, are directives that are being imposed on digital electronics suppliers in an attempt to ensure that future systems are more reliable, maintainable, and cost effective.

Given recent advancements in digital packaging, new technologies must also evolve to advance RF/microwave electronic integration. In response to these needs, great strides have been made in developing and integrating equivalent RF technologies such as monolithic microwave integrated circuits (MMICs) to reduce parts count, interconnects, and improve the reliability, maintainability and cost associated with high frequency electronics. While these generic monolithic devices can satisfy many RF design needs for specific functions, an overall SEM-E level packaging concept needs to be developed to successfully integrate MMIC devices and associated components in a manner that is consistent with future packaging goals. This concept must set a standard for improving reliability, maintainability, weight, volume, and cost of avionics packaging without sacrificing performance.

The highly specialized nature of RF subsystems, particularly radar subsystems, has slowed the progress toward standardization and modularity in military avionics. The packaging constraints of microwave components include precise physical

arrangements of transmission media, specialized low loss materials, and tightly toleranced, impedance matched interconnects. In addition to general packaging constraints, the highly specialized electrical functions with narrow bandwidths have traditionally made MMIC development difficult and expensive, with limited applications. As a result, the reliability and maintainability of RF subsystems have traditionally been limited by the performance driven nature of RF design. In order to meet the demanding performance and cost requirements associated with RF assemblies, a wide variety of materials, components, and manufacturing capabilities are needed for both design and fabrication. The packaging is further complicated by the fact that each material exhibits unique and dissimilar mechanical, thermal, and electrical properties.

As a result of developments sponsored by the PAVE PACE program, a packaging approach that promises a reliable, efficient RF subsystem design and low life cycle costs has emerged. A high density microwave based packaging (HDMP) design has been developed to comply with the long term avionics objectives put forth by the PAVE PACE architecture. The specific technologies inherent in the HDMP approach are highly visible within the electronics industry, however the unique fashion in which the technologies are applied provides the key system benefits being sought in advanced architectures. The PAVE PACE program has provided overall system requirements that enable a systems approach to the design/development process and subsequent application of key technologies that provide the best overall solution to the packaging objectives.

HDMP DESIGN

RF subsystems, particularly radar, have evolved into discrete functional elements based on performance and testability needs. The subsystem functional partitioning has been optimized for a blind mate, ATR/module packaging architecture commonly found on modern aircraft weapons systems. The packaging architecture has supported a 3-level maintenance concept common to current fielded systems, where the ATR unit is flight-line replaceable. This hardware packaging approach correlated well with the loosely coupled federated subsystem avionics architectures commonly used in current system design. The evolution of avionics system architecture has demanded a change to RF subsystems that can be integrated in both function and hardware configuration.

The hardware configuration of next generation, integrated systems relies heavily on the SEM-E standard module format. Since the electrical functional partitioning has been optimized, the challenge has become one of packaging current functions within the relatively small SEM-E format, which is beyond what conventional packaging techniques allow. The additional constraint of a 2-level maintenance concept dictates that additional BIT functions be contained within the module so that the modules can become flight-line replaceable, thereby eliminating the intermediate shop facility. In addition to flight-line replaceable modules, module repair must also be simplified if significant life cycle costs are to be reduced. Figure 1 compares current and next generation maintenance concepts.

Given the fundamental architecture constraints imposed by an integrated architecture, it is clear that significant advances must be made in RF module packaging techniques to adapt to the inevitable changes in RF hardware configurations. Figure 2 contrasts the assembled module configurations for current and HDMP packaging approaches. Through the application of several emerging packaging technologies, the HDMP concept transitions current RF functional partitioning into the SEM-E size (including added BIT capability), and improves life cycle costs through improved reliability and maintainability. A key objective in the mechanical design of the HDMP module was to address the failure mechanisms associated with typical RF modules. Typical sources of failures include solder joints, substrate attach, and interconnect media between various substrates. These interfaces develop stresses imposed by thermal expansion mismatches that exist between the various components. Interface failures can be effectively eliminated with the use of LTCC as an integrated RF and digital interconnect media, and solder free interconnects (SFI) to eliminate solder joints normally used for electrical interconnection. MMIC devices not only reduce packaging volume, but also improve performance and reliability over discrete components. The synergy provided by the HDMP concept represents a major step forward in RF subsystem design.

The HDMP design consists of a large cavitied LTCC motherboard, LTCC IMAs housing various devices to provide discrete functional elements, improved BIT, solder free interconnects, and a SEM-E housing. Figure 3 graphically illustrates the elements of HDMP design. Each motherboard cavity is designed to allow for the insertion of a particular IMA. Opposing RF electrical interfaces are provided in the motherboard cavity ledge and in the IMA ledge. The solder free interconnect device bridges the small gap between the IMA and motherboard. Since the SFI device is a separate item unattached to the motherboard or IMA, modularity is provided and any suitable interconnect device can be readily implemented, or substituted at any time in the system's life cycle.

The assembly of the module is unique in that all electrical interconnects are provided by the mechanical assembly of the module. The clamping force provided by the module covers provides a sustained load on the interconnects and ensures connectivity. Screws hold the module components together without the added complexity and cost of solder or adhesives. The clamping force also provides a thermal interface between the IMA and the heatsink. The IMA "floats" within the motherboard cavity, and a mechanical spring between the motherboard and IMA provides the thermal interface and electrical interconnect loads. The "float" also accommodates the mechanical tolerances inherent in the manufacturing processes for the interfacing components. Figure 4 shows a cross section of the module assembly. It is easy to conceptualize a module housing that functions much like a wired chassis assembly with module components (IMAs, motherboard) being "inserted" into the housing in "blind-mate" fashion. In fact, the module I/O connections to the motherboard are also solder free and become part of the module housing at the top level assembly. The extension of modularity to a lower level of assembly greatly improves the maintainability potential of the RF SEM-E design.

The HDMP design places no special constraints on the SEM-E heatsink design. The interface with the heatsink is merely a flat surface. Since no adhesive is used to assemble components or boards to the heatsink, CTE (coefficient of thermal expansion) mismatches do not cause the stresses within the assembly that typical packaging approaches incur. This fact, coupled with

the need to reduce module weight, prompted the design study to include lightweight composite heatsinks as an option for improved reliability. One key aspect of the composite heatsink design that requires special attention is the local heat flux capability at the IMA/heatsink interface. The MMIC devices produce extremely large heat fluxes, even at the case of the IMA. Most composite heatsink designs consider low local heat fluxes, which limits their effectiveness with the heat fluxes encountered with MMIC packaging. Generally, transverse (or Y-direction) conductivity becomes important with high localized heat fluxes to spread the heat as it flows toward the cold-plate interface. This characteristic can be achieved, but must be specifically addressed in the design.

The life cycle cost advantages of the HDMP module design come from two primary features. The added BIT capability allows for an improved 2-level maintenance scheme, and the elimination of solder and bonding processes from the module level assembly greatly simplifies the second level depot processes. In addition, to improved life cycle costs, the design meets the objectives for a SEM-E based packaging concept for RF subsystems and supports the long term avionics architectures that rely on increased levels of hardware integration.

ENABLING TECHNOLOGIES

LTCC

Typical RF assemblies are composed of a variety of materials to suit the unique properties of RF signal transmission. Each material must be recognized individually and accommodated by the designer by considering the complex interactions between these materials within an assembly over the environmental extremes imposed by the manufacturing processes, storage, usage, and repair/maintenance environments. Innovative assembly techniques are also required to package these materials because the performance of an RF assembly is very sensitive to the mechanical interrelation of the housing, components, bonding methods, and assembly process control. The stresses imposed by the complex assembly often have detrimental effects on reliability, with interfaces being common points of failure

The RF performance requirements of mission avionics systems are typically key to weapons system effectiveness. This has forced performance to take priority over the reliability, maintainability and producibility requirements given traditional RF packaging techniques. Consequently, in cases where materials, components, and packaging techniques are known to limit reliability and maintainability, they are often used in spite of this limitation. This has become an acceptable practice because alternative methods for achieving the desired performance do not exist. Therefore, design guidelines and screening requirements for RF subassemblies are often tailored to meet the capability of the materials and components employed, rather than imposing predefined standards to ensure a level of reliability and maintainability. As a result, RF subsystems tend to be more costly to produce and maintain as well as less reliable and more expensive when compared to digital microcircuit assemblies.

Low temperature co-fired ceramic (LTCC) materials enable the cost effective production of complex, integral (i.e., monolithic substrate/housing) packages that perform the chip-to-chip interconnect and transmission media functions, as well as the housing input/output connections traditionally served by large digital and coaxial RF connectors. The use of commercially available LTCC materials provides the means to design and fabricate complex, 3-D multilayered structures. One material characteristic that is key to good electrical performance at RF frequencies is that of low dielectric loss. Current and emerging LTCC materials have dielectric losses that are low enough to make them useful for a variety of RF packaging applications. Closely coupled with dielectric losses in RF circuitry are conductor metallization losses. The inherent low firing temperature of LTCC allows the use of high conductivity noble metals as conductors within the substrate. The thick film metallizations typically used in LTCC based designs, however must be characterized for their electrical loss properties as they are not pure metals. The combined loss properties of the LTCC and the metallizations used enable the integration of multiple packaging elements into a single multilayered structure with overall losses that are acceptable at a wide range of RF frequencies.

In addition to the materials properties themselves, the fabrication techniques available for LTCC can also be used to enhance RF performance. The basic manufacturing processes involved in producing LTCC structures are via punching, via filling, printing and cavity formation using thin layers of unfired or "green" dielectric tape. These layers are then collated, laminated and "co-fired" (meaning that all layers are fired together) to create a monolithic body during a single firing cycle. Figure 5 provides a more detailed process flow for the fabrication of LTCC products.

Because LTCC can be fabricated to yield three-dimensional structures, cavities are readily incorporated. Advanced RF components can later be assembled into these cavities as illustrated in figure 6, such that all RF interconnect transmission lines from the device to the substrate remain planar. In much the same way, RF isolation walls between the circuits in the cavities can also be formed in the ceramic. Furthermore, vias can be designed into the walls to provide greater electrical isolation where needed. The multilayered nature of LTCC also supports the integration of stripline, microstrip, and digital routing (see figure 7).

All of the above mentioned techniques were combined in the two applications of LTCC in the HDMP concept. These applications included the integrated microwave assemblies (IMAs) and a motherboard. The IMAs serve to house the electronic devices (i.e., MMICs) as well as to provide interconnections between devices and to the external environment. The motherboard, in turn, houses a number of IMAs for which it provides interconnection. This concept yields a module having increased reliability and lower costs by reducing piece part count and eliminating interfaces which therefore reduces variability during the assembly process.

Interconnects

Solder free interconnects provide a means of greatly reducing maintenance costs for avionics systems. The application of solder free interconnects within the HDMP module allows the replacement of packages (in the case of RF subsystems, IMAs) without the need for soldering processes and equipment. The solder free interconnect (SFI) device utilizes a planar beryllium copper (BeCu) spring finger system for low loss RF performance to approximately 6.0 GHz. The interconnect configuration consists of a center signal conductor, with ground

interconnects on either side. The planar configuration provided reasonable RF performance using simple manufacturing processes. A similar multiplane system has been used for higher frequency performance. Alternate interconnect approaches could easily be implemented within the HDMP interface design, and several have been tested with considerable success. BeCu was used initially because it is a common interconnect material with well-understood properties making it ideal for proof of concept testing.

A modular overall packaging design was developed that maintained a simple interface between the SFI, IMA, and motherboard. The design of the SFI device did not require that special features be incorporated into the IMA or LTCC motherboard, and more importantly, no special manufacturing processes were dictated specifically for the use of SFI. The SFI device uses BeCu spring fingers for both signal and ground interconnections. The BeCu spring fingers were etched from sheet material. The etching process provides for exceptionally precise tolerancing of small intricate parts at a low manufacturing cost. Once etched, the array of spring fingers was attached to a carrier for overall assembly durability. The carrier is a fiberglass/epoxy frame with an integral compliant silicone rubber insert. The carrier/spring finger configuration provides a simple cantilever loading on the BeCu spring when compressed. The silicone rubber does not provide the interconnect load, but does provide a compliant support for the array of spring fingers during handling. Once assembled, the SFI device could be inserted between the IMA and motherboard to provide an interconnect that performed well to approximately 6 GHz (see figure 8), well beyond the requirement for most RF subsystem components.

MMIC (Monolithic Microwave Integrated Circuit) Technology

Monolithic components offer tremendous advantages in terms of reliability, maintainability, and manufacturing complexity. MMIC technology incorporates many complex electrical functions onto a single die. Using a combination of both active and passive circuit components, MMIC devices can range from simple amplifiers, oscillators, or mixer circuits, to large functional blocks. Given this opportunity, systems designers have continued to incorporate highly sophisticated functions, often at a rate that has pushed the envelope of available MMIC technology. The increased level of integration provided by MMIC technology allows for large functional blocks to be incorporated onto a small die, enabling a drastic reduction in packaging volume (often as high as 10 to 1). As MMIC device and design technology become increasingly available, their impact dominates module design, and evolving packaging approaches must be tailored to take advantage of the significant benefits associated with this technology.

The advantages of using MMICs are low cost, improved reliability, small size and weight, and consistent performance from die to die. Because of this decreased size, many die can be put on a single wafer. Thus, in large quantities, the cost per die is significantly reduced. Also, the higher level of integration reduces part count, circuit path length and the number of wire bonds needed for circuit assembly. Wire bonds are a source of uncontrolled parasitic interactions within the circuit. Performance variations will be reduced when the number of wire bonds used is decreased. Reduced part count and wire bond count also reduces manufacturing costs and improves reliability. However, for small scale production (< 100's) the MMIC design expense is usually prohibitively high. For this reason an attempt must be made to tailor each IMA design to use existing/generic monolithic components as a cost targeting approach. MMIC devices often require special attention for proper thermal management. A drawback of the increased circuit density is an increase in heat dissipation per unit area (referred to as heat flux) in the region of the device junction. The high heat fluxes produce severe thermal gradients which can result in extremely high junction temperatures. Special attention must be paid to thermal management in the design process, and proper design tools must be employed to achieve successful results.

Composite Heatsink Materials

RF modules are generally conductively cooled via a central web that contacts coldplates along two opposing edges of the module. Wedgelocks are typically used to provide a high contact pressure between the coldplate and heatsink. Conductive cooling provides a simple, low maintenance, robust module/rack configuration, and is therefore a preferred method if module heat loads permit its use. In typical systems that use conductive cooling, considerable weight is dedicated to the cooling web or thermal plane. Lightweight, high conductivity composite materials were utilized in the HDMP baseline design to address the growing need for system weight reduction. These composite materials have evolved from the development of high conductivity carbon fibers. The carbon fibers can be combined with a variety of matrix materials to yield composite materials with a wide variety of thermal and mechanical properties. Typical composite heatsink materials include carbon/PEI, aluminum/graphite, copper/graphite, and carbon/carbon. Each material can be designed for a specific usage, however in developing the HDMP design some fundamental limitations were identified.

Most composite materials exhibit properties that are highly directional. In the case of a SEM-E module heatsink, the conductivity can usually be tailored to coincide with the primary direction of heat flow (generally referred to as the module X-direction). When packaging MMIC devices, the high heat fluxes produced require that considerable spreading must occur within the heatsink material to achieve low junction temperatures. This phenomenon places additional constraints on the design of the heatsink material to include some transverse (Y-direction) conductivity to accommodate heat spreading. The IMA packaging technique produced heat fluxes at the surface of the heatsink of approximately 15 watts per cm^2. If adequate spreading of heat is not achieved, localized "spikes" occur in the temperature distribution across the surface of the heatsink, and unacceptable junction temperatures can result. These results can be seen in figure 9 for a SEM-E module with an array of heat sources of the type produced from IMAs that house MMIC devices. Carbon/carbon heatsinks as well as the metal matrix variety will usually have adequate spreading capability due to the contribution of the matrix material conductivity. Organic or polymer matrix heatsinks are viable as well, but conductivity constraints based on the heat flux environment needs to be identified in the packaging design phase.

Thermal Design Tools

While it is common to find a wealth of information on specific material or device technologies, often overlooked are the design-oriented techniques that enable the utilization of these technologies in functioning systems. Considerable credit for

the successful implementation of MMIC and LTCC materials must be given to the unique design/analysis tools developed specifically for the packaging design effort.

Device technology in recent years has begun to outpace the capability of most analytical tools available to perform thermal management analysis at the device level. Junctions within the MMIC devices are the regions that actually dissipate heat. These junctions are extremely small, and although the total heat dissipation may be relatively small, the minute junctions still produce heat fluxes (heat dissipation per unit area) in excess of 400 Watts per cm^2. Analytical tools are essential in developing reliable packaging techniques. Analytical techniques must be capable of resolving junctions of the size found in current MMIC devices, while also including the effects of the surrounding package, which for large integrated microwave assemblies (IMA's), is several orders of magnitude larger than the junction being resolved. Using a Westinghouse proprietary software package based on direct numerical simulation (DNS) techniques, thermal management optimization was made possible, and was accomplished for each IMA as well as the module.

The DNS approach uses finite difference techniques that provide the packaging designer with the capability to process thermal simulations that include several hundred thousand nodes in a matter of hours. An automatic meshing feature that is built into the DNS software allows the user to enter simple text data files which define the IMA or module geometry. This analysis capability was required to resolve the MMIC junctions in the presence of the surrounding package and to develop a specific package design that minimized the θjc (junction to case temperature rise). A thermal analysis output example is shown in figure 10. The grid is representative of the fidelity of the analysis. The sharp spikes are tiny MMIC junctions where temperature gradients often become severe. Arrays of thermal vias and planes of metal within the LTCC IMA package as well as heat spreaders just beneath critical components were all used to draw the heat from the devices through the base of the packages to a spreader which was attached to the back of the IMAs. Through the use of thermal spreaders, or backplates, heat was distributed evenly at the base of each IMA, thus maximizing the total area available for the thermal dissipation into the heatsink below.

RESULTS

Emerging systems architectures provided the framework in which the HDMP design was developed. HDMP technology:

- Supports the latest advances in monolithic components.
- Demonstrates a significant reduction in system weight and volume.
- Enables modular architecture (SEM-E) for improved maintainability.
- Uses Solder Free Interconnects to improve maintainability/repairability and reliability.
- Improves thermal conductivity, while accommodating dense packaging for reduced weight and volume.
- Increases reliability through an increase in component integration.
- Incorporates advanced BIT/FIT technology that enables 2-level maintenance.
- Reduces life cycle cost.

Extensive environmental testing has been performed on passive, and active HDMP modules. The results demonstrate the feasibility of the variety of concepts applied to the module to meet emerging systems requirements. L-band radar receiver functions have been implemented in SEM-E form (including BIT to facilitate 2-level maintenance) with the HDMP technology. Radar functions provide difficult design challenges, and are generally categorized as performance driven designs. Projected benefits of HDMP include a 3 to 1 module reliability improvement, and a 5 to 1 MTTR (mean time to repair) improvement at the module level repair shop.

DISCUSSION

Question: To what extent should airplane designers plan to mix RF and digital on the same module and in the same rack? Also, would liquid flow through cooling be good for the combined RF/digital modules? Could you comment on whether or not SEM-E modules are the right size and right pitch (0.6 in.) for use in RF circuitry?

Answer: (1) Mixture of RF and digital will become a necessity both on and off the module. They should be separated on the backplane and isolated by planes once in the module. (2) Use of liquid is only a last resort or if available out of necessity for other reasons. Conduction cooling with air plenum, conduction with liquid plenum, air flow through, then liquid flow through should be the sequence. Liquid adds cost, volume, and weight. (3) SEM-E for both digital and RF is too restrictive (in my opinion). A taller module (like the FASTPACK) would be better. A digital module with 0.65 in. pitch would be much better. At present, RF SEM-E pitch is at 0.90 in., driven by the availability of RF components and the standard allows for increments of 0.30 in. pitch.

Question: Fault localization to LRM level can be difficult using BIT, especially given the NATO goal of "No first line test equipment." What degree of localization has been achieved for RF modules?

Answer: It depends on the type of RF application, but in [the] HDMP application, we attained ≈95%.

Question: How did you do the MMIC thermal simulation?

Answer: Westinghouse has developed proprietary FEA thermal analysis tools. For GaAs applications, we obtain power dissipation and junction geometry information from the GaAs manufacturer to create the FEA model. We then look for a converging solution by going to finer FEA grids and stability of the final answer.

Question: What is the difference in occupied area between the RF ribbon interconnections and the SFi?

Answer: In the HDMP application, the SFI contact strip measured ≈5 mm, but can be as short as 2.5 mm. Ribbon band can be much shorter, but is less repairable, requires heat, and is not as automated as conventional wire bonding.

Question: What is the means to compensate for the thermal expansion mismatch for the hot spots of greater than 400 W/cm^2?

Answer: Maintain close match of CTE between GaAs, spreader, epoxy bond, and LTCC. Keep dimensions (x,y) small.

Question: What is the spreader made of?

Answer: Thermal spreader [is] made of copper/moly alloy (CM-15).

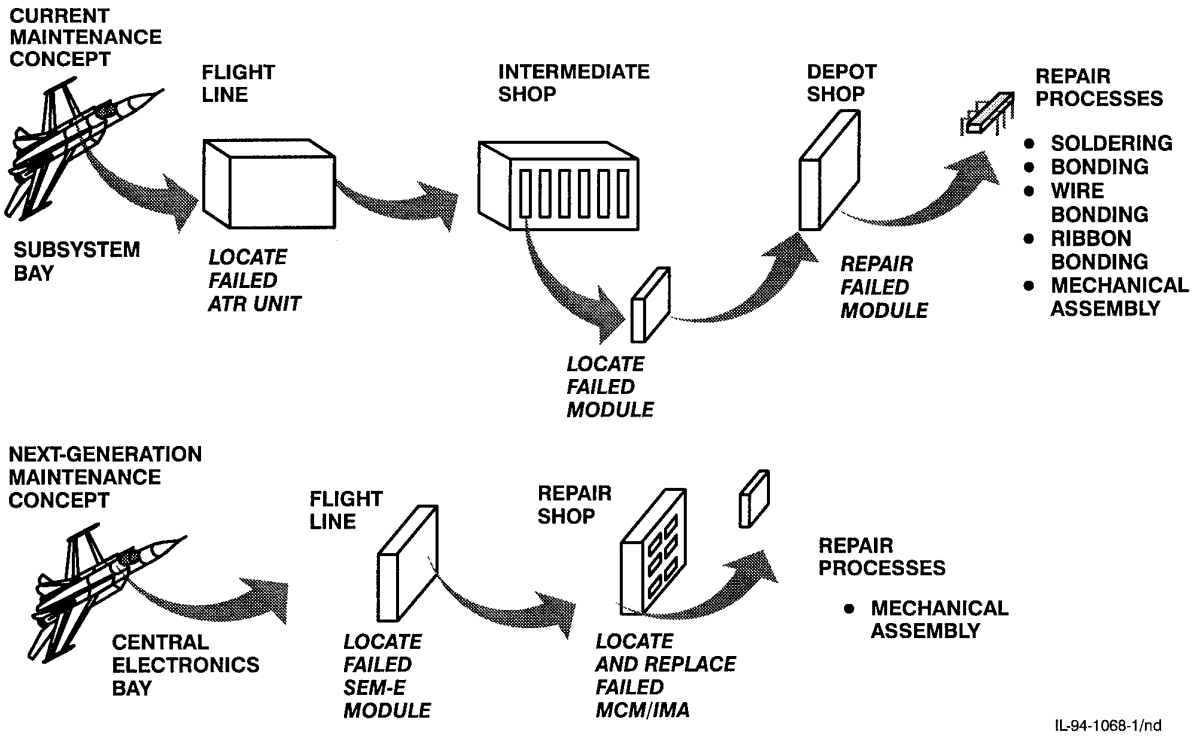


Figure 1. Next-Generation Systems Will Require Significant Reductions in Maintenance and Repair Complexity

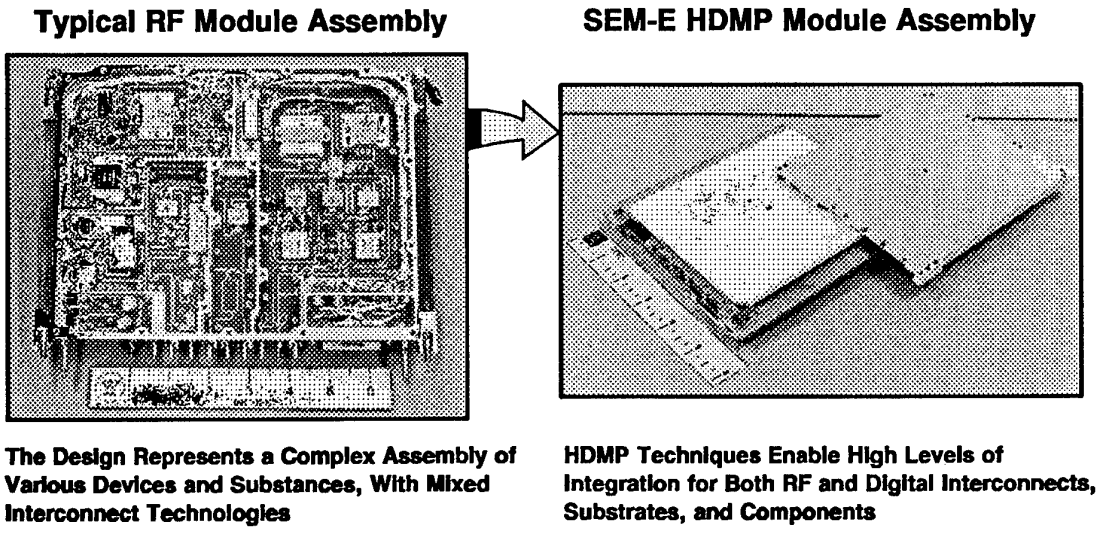


Figure 2. The Application of Advanced Module Packaging Technologies Result in Simplified Module Assembly

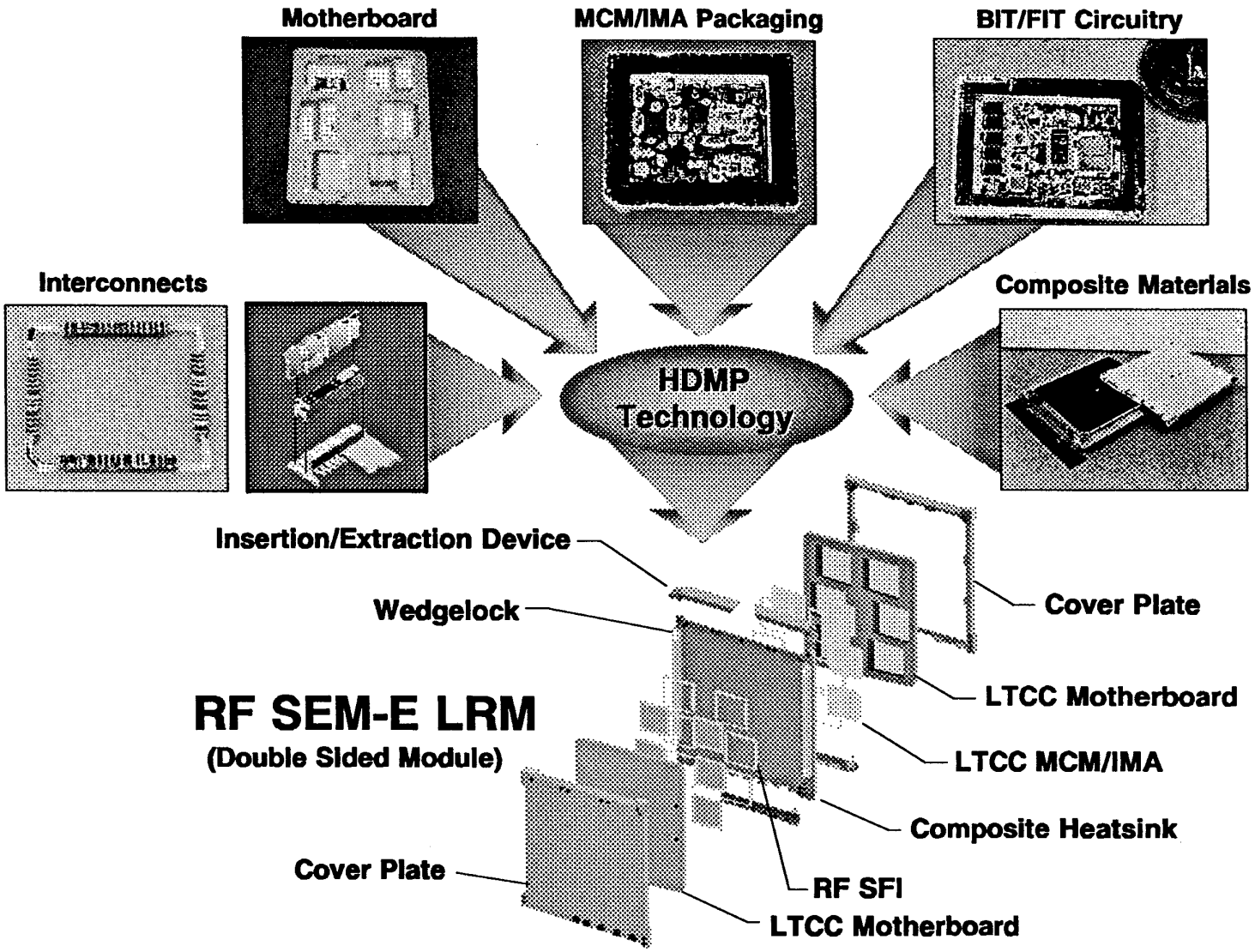


Figure 3. Elements of HDMP

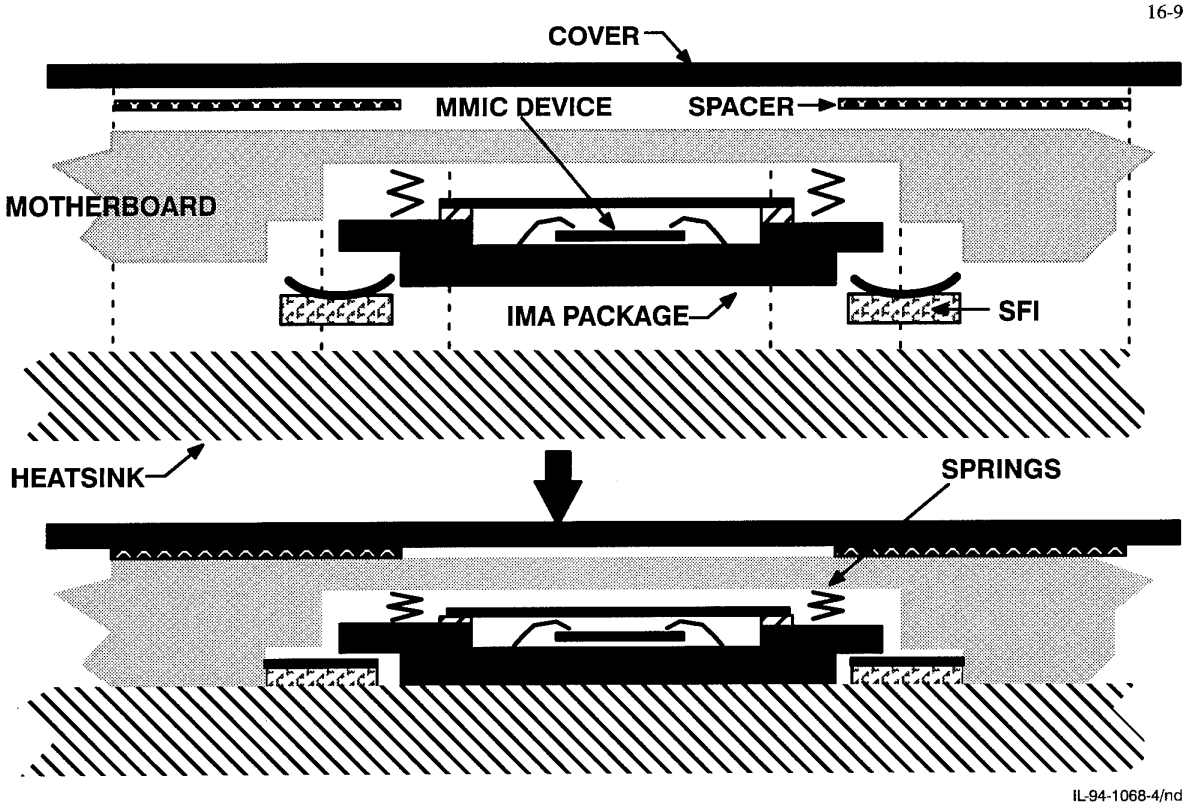


Figure 4. HDMP Module Assembly

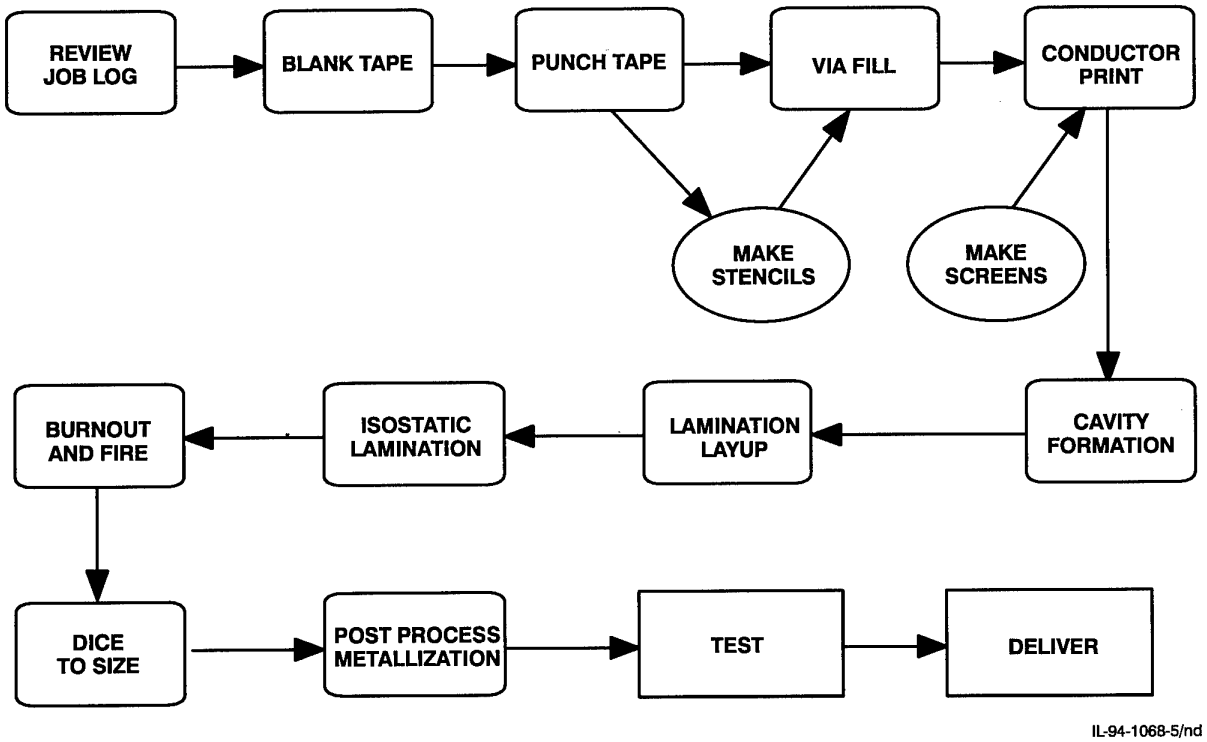


Figure 5. LTCC Manufacturing Process

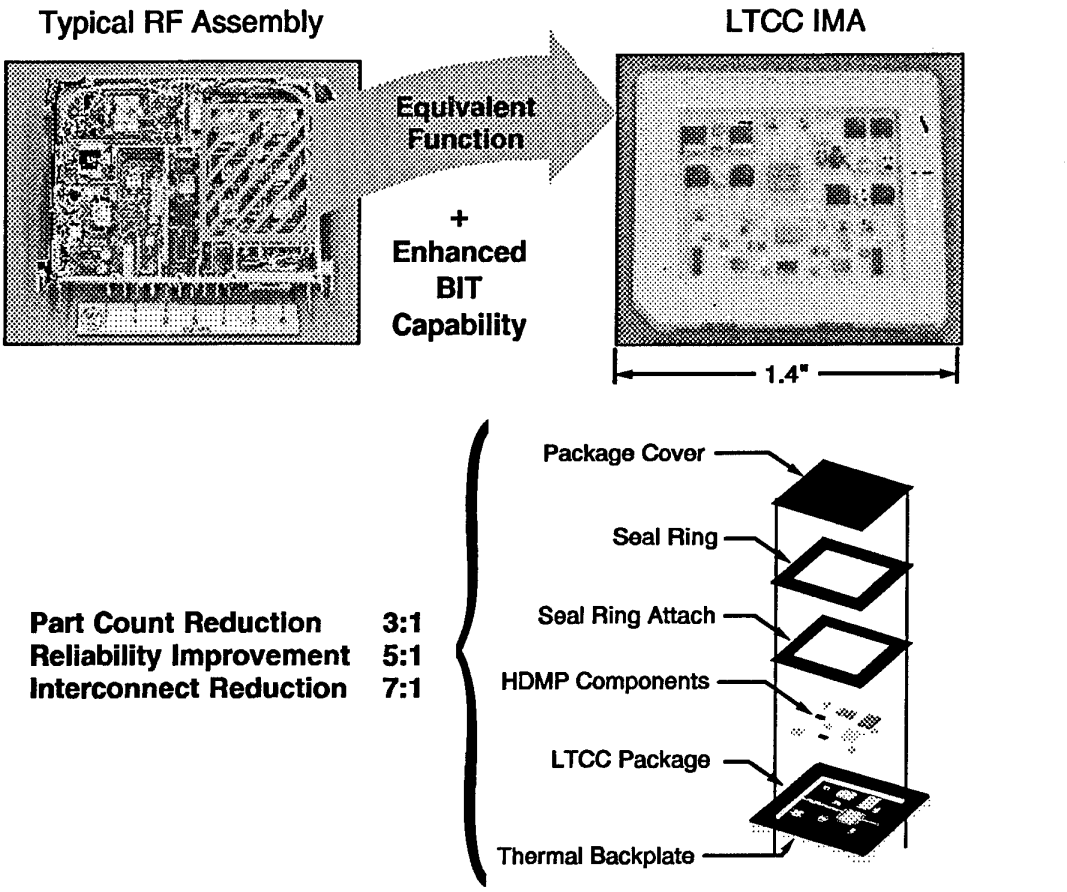


Figure 6. High Integration Densities Achieved With LTCC Offer Improvements in Reliability, Performance, Manufacturing Complexity, and Packaging Volume

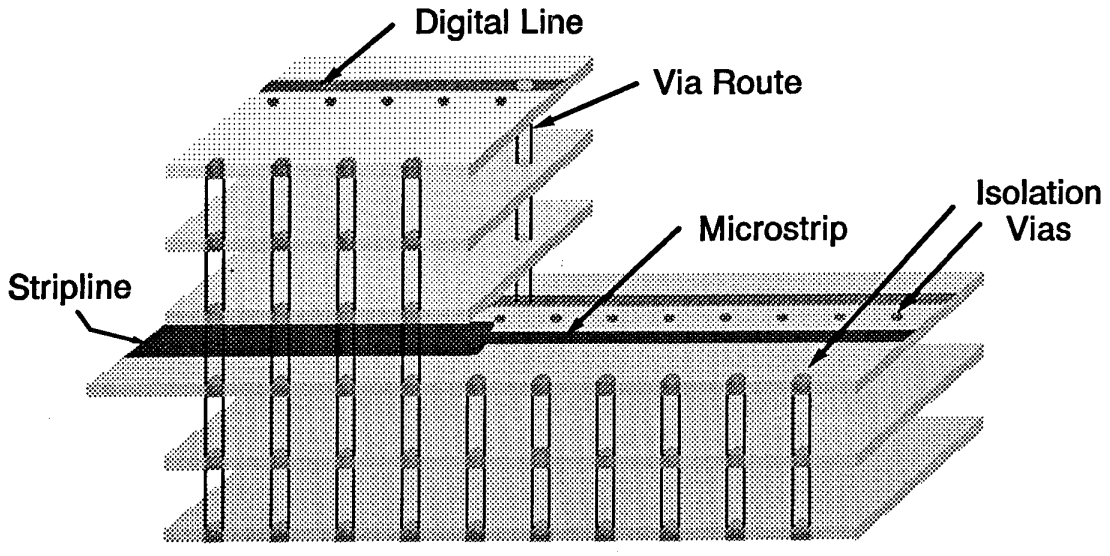


Figure 7. LTCC Substrate Cross Section Exploded View

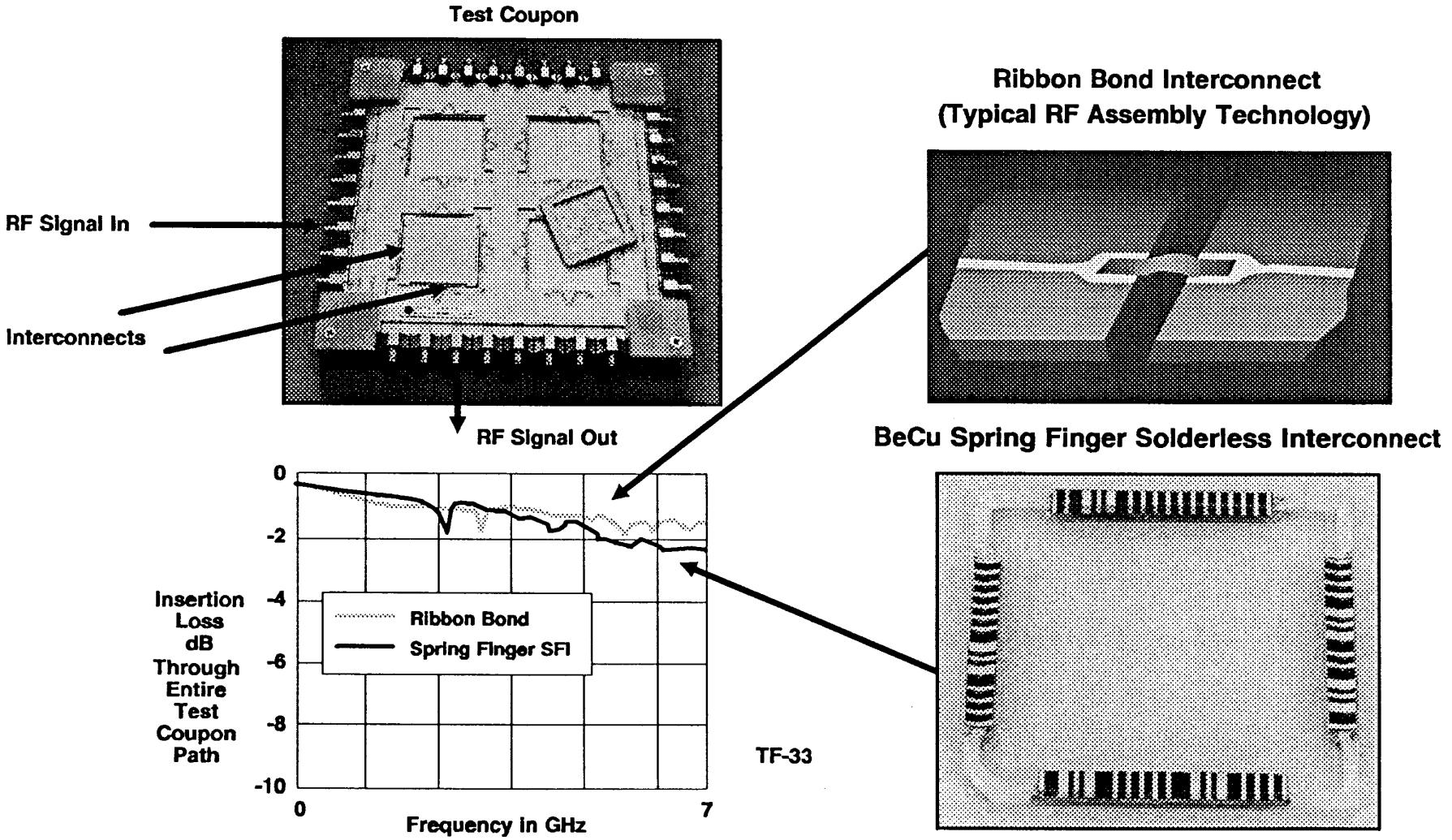


Figure 8. Solder Free Interconnects Offer Comparable L-Band Performance to Conventional Techniques

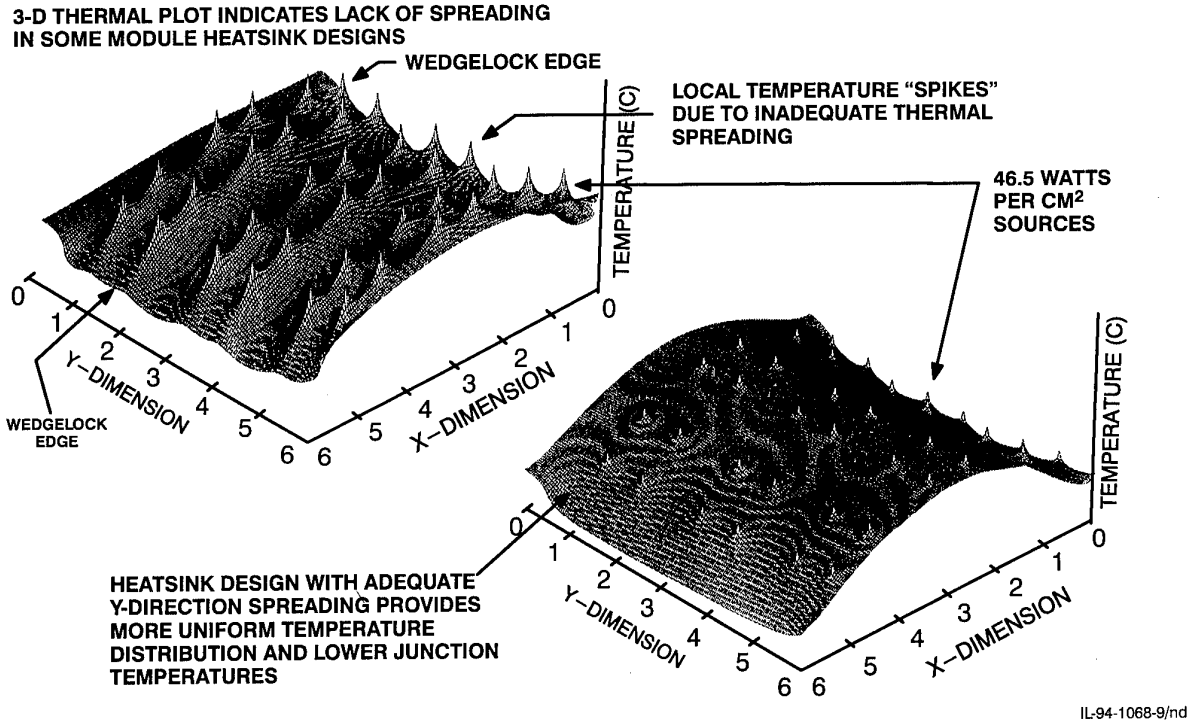


Figure 9. Y-Direction Conductivity Is Key to Improved Thermal Efficiency

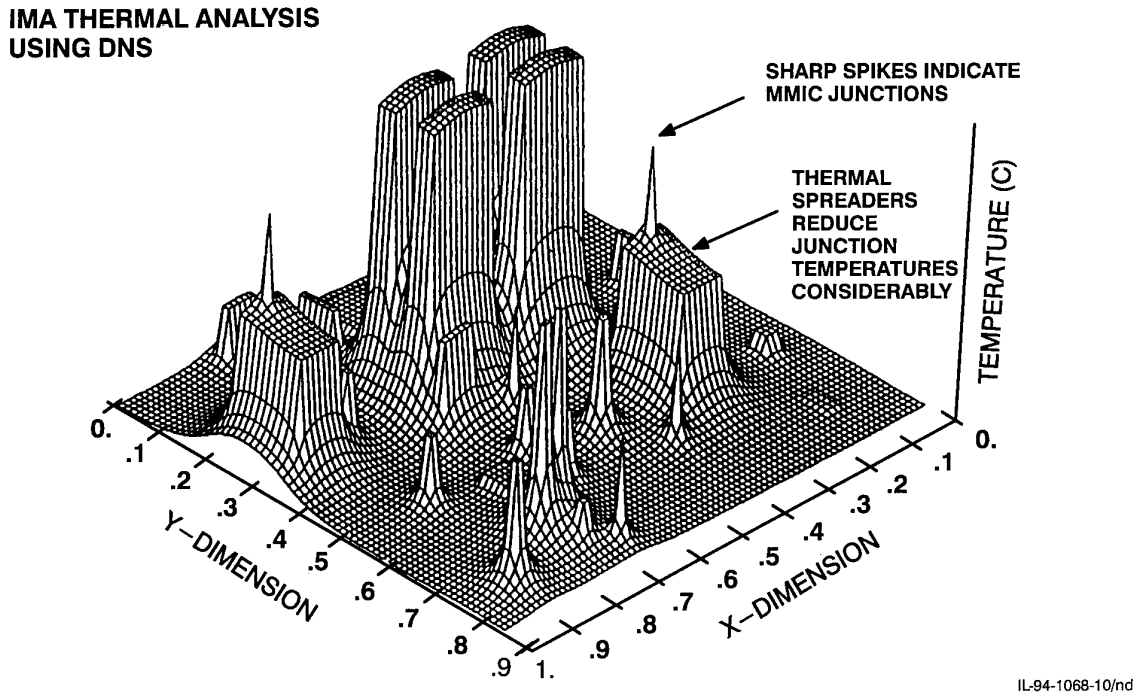


Figure 10. Thermal Analysis of IMA Containing MMIC Devices

Liquid Flow-Through Cooling of Electronic Modules

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Abstract

Thermal management of future avionics modules will be a critical design issue. New advances in integrated circuit technology and electronic packaging will allow the design of densely populated electronics modules with potential power dissipation levels in excess of 1.0 W/cm^2. While the module power level trend will be to increase, the maximum allowable junction temperature for integrated circuits may be lowered to provide more benign thermal environment for electronics. This negates the use of conventional thermal management techniques in new avionics applications. A number of trade studies were performed to determine which cooling technique would be best suited to meet the anticipated reliability and performance requirements for the year 2005 and beyond. The approaches to module cooling technologies considered were: edge cooled conduction, immersion, and hollow core flow-through. The technology selected was the hollow core flow-through. This paper discusses the results of flow-through cooling investigations on both single-pass cold plates and SEM-E modules.

Introduction

As a part of a comprehensive program on electronic packaging issues, electronic cooling techniques are being studied at the CALCE EPRC (Electronic Packaging Research Center). This work has included testing, modeling and model validation as key parts of the development of the CALCE software package which is an electronic packaging software toolbox. The CALCE EPRC is an NSF (National Science Foundation) sponsored consortium of organizations with an interest in electronic packaging.

The CALCE electronic cooling work has included forced and natural convection air-cooling, conduction cooling and flow-through cooling. Current work in the CALCE EPRC includes CFD (computational fluid dynamics) modeling of air cooled electronic multi-board chassis, flow-through cooling of SEM-E modules and the use of phase-change materials in thermal management. This paper describes the results of the flow-through cooling studies and the experience in integrating these results into the CALCE software.

The flow-through cooling efforts have included heat transfer and pressure drop measurements on both single-pass cold plates and SEM-E modules. For both heat exchanger geometries, tests were done with both water and PAO (polyalphaolefin) as the heat transfer fluid. Although water is not a practical heat transfer fluid for applications because of corrosion and fouling problems, it was included in the testing because its heat transfer characteristics are excellent and the performance of these devices with water represents a limit on performance. PAO, a synthetic oil, is available in a range of viscosity grades. The fluid used here is sold as 2cSt which represents the nominal viscosity of the PAO at 80°C. PAO was found to be a good fluid with reasonable heat transfer characteristics and reasonable materials compatibility.

We were first attracted to the field of liquid-cooled finned heat exchangers when we realized that very few investigators have published data on the subject. Although liquid cooling is widely used in avionics and other high performance rack-mounted systems, there is essentially no design data available in the literature. Thus, although many companies have in-house expertise, the technology is not well documented. A key objective of our work was to characterize the liquid-cooled performance of these devices and to arrive at predictive models useful for design.

The literature on liquid-cooled offset-fin heat exchangers is quite limited. Brinkmann et al. (1987) have studied liquid cooling of an offset-fin heat sink added to a component. Roberstson (1979) did experiments using liquid nitrogen as the cooling fluid. These two studies, while interesting, are not directly applicable to the problem of interest here. Hou (1988) studied liquid-cooled offset-fin cold plates and found that air correlations do not predict the performance of liquid coolants. LeVasseur (1991) studied the flow-through SEM-E configuration and documented increased heat rejection potential. The studies listed above represent a meager source of design information. To address this, we undertook an experimental and modeling study in 1991 (Hu and Herold, 1993a;Hu and Herold, 1993b;Hu, 1993). Since that time, we have initiated the SEM-E work (Herold et al., 1992).

Offset-Fin Technology

The geometry of typical offset-fins is shown schematically in Figure 1. The fin stock is manufactured by rolling thin sheet metal through a toothed die which cuts and bends the material into the offset shape. The fin stock is then brazed between two cover plates. The heat transfer fluid flows through the open spaces in the fin stock created by the die. As the fluid flows past the fins, the interruptions in the boundary layers that form on the fins lead to increased heat transfer and increased

pressure drop. For many electronic cooling applications, this tradeoff between pumping power and cooling performance is beneficial to the overall system design. Another benefit of the offset fins is that they provide significant structural rigidity for the heat exchanger which would tend to burst without the strength provided by the fins.

Flow-Through Cold Plates

Liquid-cooled cold plates are widely used as the heat sink for electronic assemblies. Although more complex configurations are sometimes used, a single pass design is quite common where the liquid coolant enters one end and exits at the other. The overall dimensions of the single-pass cold plates tested in our study were 8 x 0.3 x 30 cm. Seven cold plates were tested with the fin geometries listed in Table 1. Each of the plates was tested with both water and PAO. A modeling approach based on the work of Joshi and Webb (1987) was used to interpret the data. Comparisons were made against standard correlations (which exist only for air) and serious deviations were found which indicate that designs based on the air correlations would be undersized by a factor of two.

Because of the relatively high fin density in such a device, the flow passages between the fins are quite small (approximately 1.5 mm). Furthermore, the viscosity of the liquid coolants is relatively high. As a result, the flow between the fins tends to be laminar for the range of flow rates of interest. Higher flow rates would also be possible, but the maximum pressure drop requirement of most systems constrains the flow to the laminar range with Reynolds number typically from 10-100.

A typical cold plate temperature distribution is shown in Figure 2. The data points are from a particular test run and the solid lines represent our numerical models of the same run. As can be seen, the data are predicted quite well. The model includes the end effect conduction to the unheated section which is significant in many designs. Large temperature gradients occur near the inlet and outlet and this drives conduction in the cover plates. The end effect analysis is particularly important to understand when trying to interpret the overall heat transfer driving potential for the system since the temperatures near the ends should not be used. Instead, temperatures from the central section give a much better picture of the overall heat transfer process. The relatively large temperature difference of approximately 20°C is due to a heat flux of 7.6 W/cm^2.

A typical comparison between our experimental data and our models is shown in Figure 3 for one plate geometry. The plot includes both the heat transfer and pressure drop characteristic in the form of Colburn factor, j, and friction factor, f. The model of the liquid performance is seen to match the data quite well. This model takes into account the realities of liquid applications that include the importance of entry effects. The j values reported represent an average heat transfer performance over the entire device (as is needed in design). Our models take the length of the finned section as an input and account for the entry length where needed.

Flow-Through SEM-E Modules

The SEM-E (standard electronic module, size E) module exists in both a solid core version, with conduction cooling, and a flow-through core with offset fins designed for liquid cooling. Flow-through SEM-E technology has grown out of the needs of the avionics community for higher power on a given size board. The power limitation for a conduction cooled SEM-E is approximately 25 W while the liquid cooled SEM-E can easily achieve 200 W (while maintaining the same junction temperatures). This factor of 10 in thermal performance, when combined with the accelerating miniaturization of electronic components, means that liquid cooling provides for an otherwise unobtainable performance to weight ratio. Advanced high density electronic systems, necessary for both navigation and weapons, require flow-through technology.

Flow-through SEM-E designs represent an extension of liquid-cooled cold plate technology that has been used in avionics for 50 years. From a heat transfer standpoint, the SEM-E configuration is just a complicated cold plate due to the internal flow baffles needed to distribute the coolant evenly. Our heat transfer tests indicate that the performance of the SEM-E can be well predicted based on the models developed from the cold plate tests.

The SEM-E size boards were selected for their wide application to present and future Air Force avionics design. Several different liquid flow-through modules were designed and tested under extreme environmental conditions. The designs consisted in variations of the internal fin geometries and number of flow passes. Tests were conducted with water and PAO (Polyalphaolefin) as coolants. The coolant flow rates and the power dissipation levels were varied to study the module thermal performance under different conditions. Performance predictions were also obtained with CALCE software and correlated with experimental results.

Representative results from a series of heat transfer tests are shown in Figure 4. This figure is for a single module tested over a range of flow rates and power levels with PAO as coolant. The surface temperature at the outlet is plotted versus flow rate. In addition, the figure shows the CALCE prediction for the same case. The deviations represent scatter in the experimental results.

Summary and Conclusions

A series of experimental and modeling efforts dealing with liquid flow-through cooling of offset-fin structures are described. These finned systems are widely used in electronic cooling but little data has been published for liquid heat transfer fluids. The high heat transfer performance provided by these systems is the key to their

market penetration. Our comprehensive program has documented the heat transfer and pressure drop performance of such systems and applied the results to the modeling of the complex flow patterns in the flow-through SEM-E. Excellent results are obtained which provide the user with design tools for such technology.

Acknowledgements

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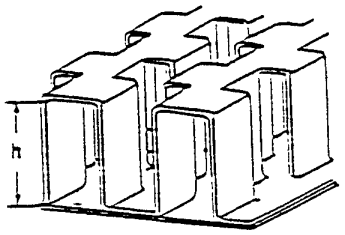
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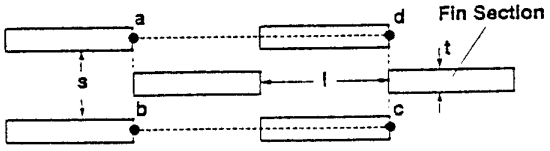
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a. Perspective View



b. Cross Section View at Half Fin Height

Figure 1 Offset Fin Geometry

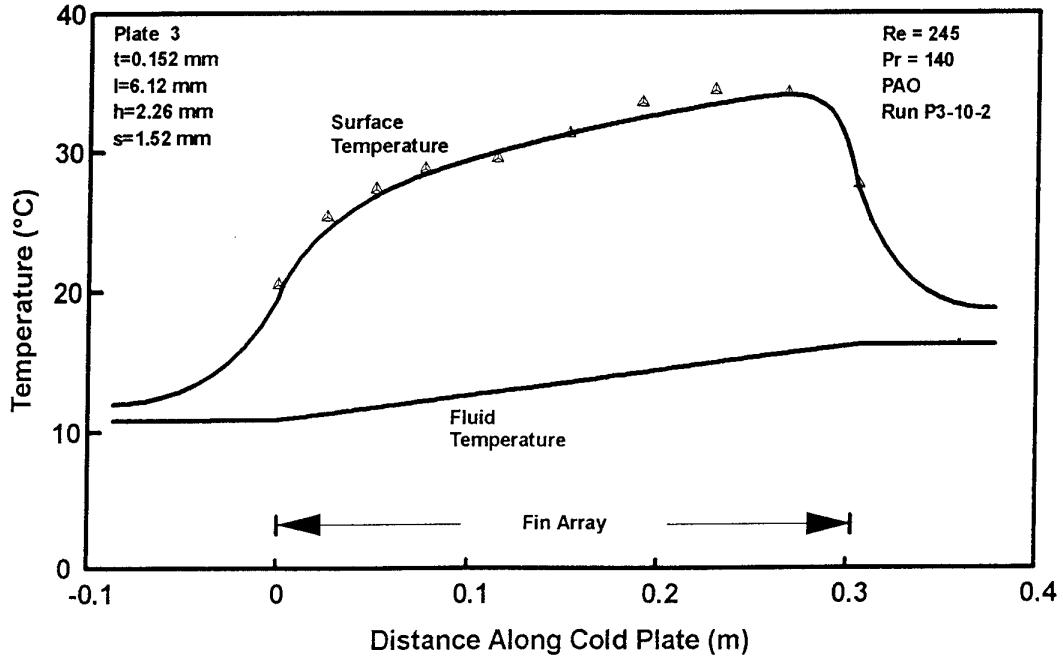


Figure 2 Cold Plate Temperatures from Numerical Model and Experiment

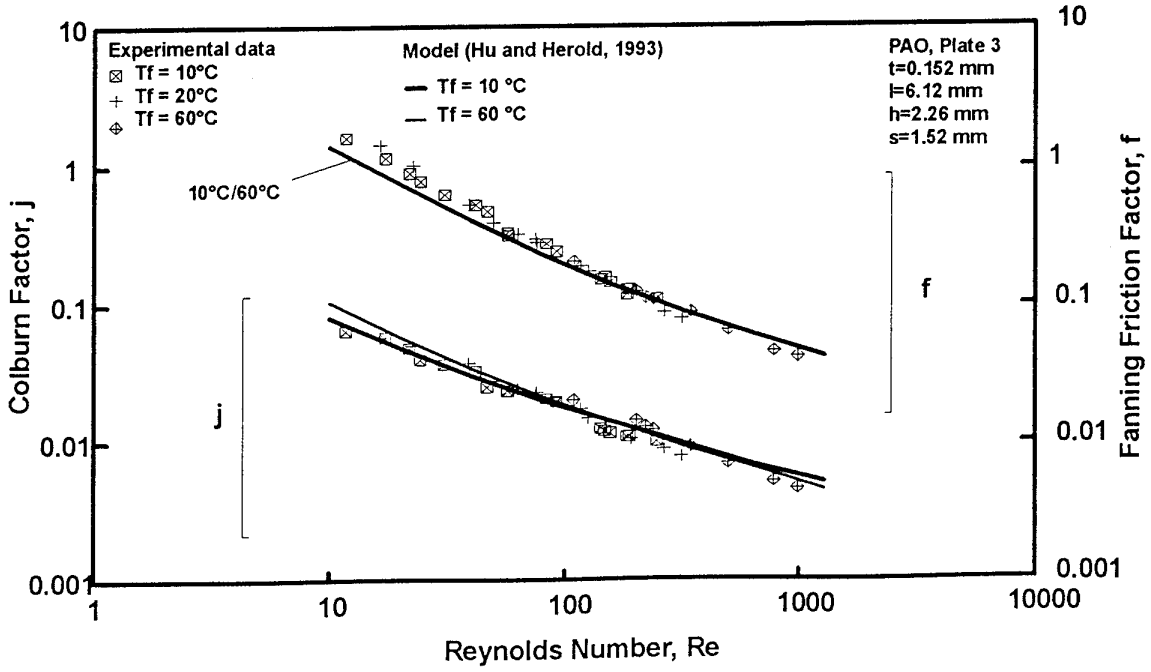


Figure 3 Effect of Fluid Temperature on Performance of Offset Fin Cold Plate

Table 1. Cold Plate Fin Geometry

Cold Plate	Fin thickness, t mm (inch)	Fin length, l mm (inch)	Fin height, h mm (inch)	Fin spacing distance, s mm (inch)
1	0.152 (0.006)	3.20 (0.126)	2.39 (0.094)	0.99 (0.039)
2	0.152 (0.006)	3.18 (0.125)	2.34 (0.092)	1.65 (0.065)
3	0.152 (0.006)	6.12 (0.241)	2.26 (0.089)	1.52 (0.060)
4	0.152 (0.006)	3.33 (0.131)	3.84 (0.151)	1.28 (0.050)
5	0.152 (0.006)	3.40 (0.134)	2.36 (0.093)	1.26 (0.049)
6	0.102 (0.004)	3.33 (0.131)	2.36 (0.093)	1.55 (0.061)
7	0.152 (0.006)	3.33 (0.131)	3.84 (0.151)	1.62 (0.064)

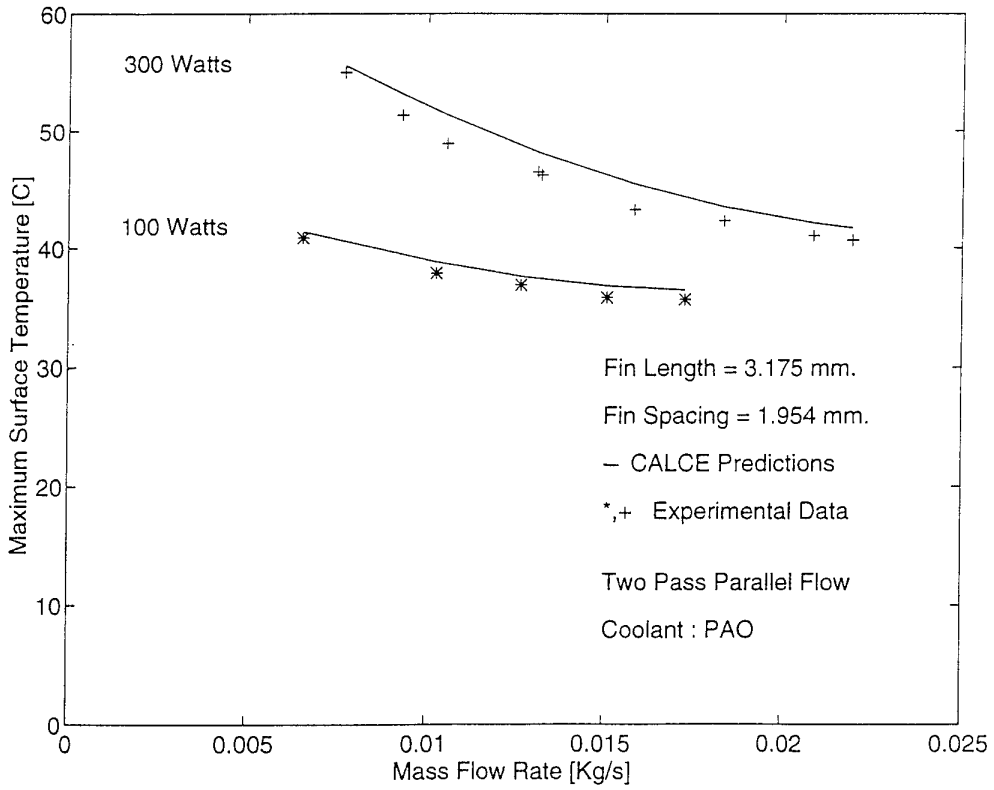


Figure 4 SEM-E Surface Temperatures from CALCE Predictions and Experiment

DISCUSSION

Question: The Colburn [factor] is dangerous to use to compare two fluids, because Nu = f(Re,Pr) divided by $ReDv^{1/3}$, [which] extremely reduced the effect of the fluid.

Answer: The object of the definition of the Colburn factor was to do just that; i.e., to collapse the data for all fluids into a single curve. However, in this application, the Colburn factor is not independent of the Prandtl number.

Question: Entry effects are much more important on real LFT modules.

Answer: Complex geometries such as the LFT SEM-E have very complex flow patterns that do affect performance somewhat.

Question: How far in power dissipation can we go with LFT modules? 100 W? 500 W? 1000 W?

Answer: The answer depends on which variables remain. Maximum power depends strongly on fluid flow rate which is usually constrained by pressure drop limitations.

Question: Have you investigated the effect of different coolant fluids on fin optimization with the aim of creating a semi-optimum fin design that works efficiently with many fluids?

Answer: Our models are specifically designed to allow extrapolation to other fluids and other geometries, as long as they are close to the properties of those systems tested. The model should work with Coolanol, for example.

Question: Have you investigated the effects of PAO's highly viscous state at -55°C on fin and LFT HE performance?

Answer: The lowest temperature we have tested is -10°C.

Question: Which alternative fin geometries should be investigated? (BAe results from 10 years ago on racks with circular perpendicular pins, no flow straightening on entry or exit, were not encouraging.)

Answer: Many alternative fin geometries have been proposed over the years. Offset fins appear to be the best configuration to me. within the offset fin geometry, there is considerable room for fin optimization. In my opinion, this optimization should lead to a fin design that will be difficult to beat. Another advantage of offset fins is the simplicity of fabrication (assuming the vacuum brazing process has been perfected).

IMMERSION/TWO PHASE COOLING

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ABSTRACT

Due to increasing heat dissipation requirements, the need for an advanced cooling technique in current military avionics has been recognized. Immersion cooling with phase change has been demonstrated in a Format E clamshell module as an alternative. This module is capable of dissipating more than 700 Watts. From the development of the Format E clamshell module the AAS&T (Advanced Avionics Subsystems and Technology) Program has began an effort to utilize the clamshell module in the development of a 3/4 ATR Format E Standard Avionics Enclosure utilizing immersion/change of phase cooling. The power dissipation requirement for the enclosure is 6500 Watts minimum. The cooling medium for both efforts is a Fluorinert (FC-72). The FC-72 is an environmentally safe coolant. As the need for greater heat removal and reliability increases, cooling technology must become more advanced to meet the needs of next generation aircraft.

PREFACE:

AAS&T is a unique Navy 6.3A advanced avionics technology insertion program. AAS&T is not associated with specific platforms, but rather with solving Navy unique problems. Many of Naval avionics problems stem from the environment in which they must operate. However, temperature is believed to be the largest cause of avionics failure. AAS&T under the leadership of the Naval Air Systems Command Code: AIR-546T, Washington, DC, is developing method of improving avionics through improvements in the advanced avionics packaging and thermal management of the electronics.

BACKGROUND:

Thermal management of military avionics has a long history. Electronic modules have progressed from simple convection cooling, to conduction cooling of aluminum modules, conduction cooled composite modules, and liquid flow through (LFT) modules now being planned for use on future aircraft. Each design is trying to eliminate failures and low reliability caused by inadequate electronic cooling. Fluorinert liquid cooling has been used in military systems since the 1960s. Military Specification MIL-H-81829 defines the requirements for a heat transfer fluid having superior electrical insulating and dielectric properties; several existing Fluorinert liquids meet the requirements of this specification. Immersion cooling of electronics has even been used as early as the Vietnam War, but this technology was not used to its fullest extent. Entire electronic enclosures were immersed in coolants, but the coolants were not dielectrics and could not be put in direct contact with the source of the heat; the electronics. Materials, technology, and resistance to change have limited the induction of immersion cooling into mainstream avionics. It is not easy to convince people that it is a safe idea to have a liquid in direct contact with electronic circuitry.

Without education into the technology, many people think that the coolant, like water, would destroy the electronics or be a safety hazard. This is not the case. Coolants selected for direct immersion cooling are considered dielectrics; which means that they do not conduct electricity. Since the coolants are dielectrics they are harmless to electronics. Many of these coolants will completely disappear when spilled, thereby not causing any maintenance problems. These coolants are almost completely inert. Many are safe enough for human ingestion, although not recommended.

Fluorinert liquids are currently being used in many commercial applications. Fluorinert liquid cooling gained acceptance with the introduction of the CRAY-2 supercomputer from Cray Research, Inc., in 1985. Cray Research is also using the Fluorinert in a direct immersion cooling application. Several other common Fluorinert liquid cooling applications are: radar transmitters, radar klystrons, high voltage transformers, power supplies, high end laptop computers, fuel cells and lasers. Fluorinert liquids have many other uses. Fluorinert is used in vapor phase reflow soldering to replace freon because of the ban on chlorofluorocarbons (CFCs). Fluorinert liquids are also used in liquid burn-in component testing, hermetic seal/gross leak testing, magnetic disk surface lubricants, foam blowing additives, and many other varied uses.

INTRODUCTION:

Current cooling technology is not keeping pace with the thermal requirements of electronics. Electronic systems designers are creating more densely packaged electronics that are producing higher heat fluxes (power per surface area, Watt/cm^2). Some heat fluxes are expected to exceed 50 watts/cm^2. Simple aluminum framed, conduction cooled, electronic modules are still the most prevalent modules in use. The Navy SEM-E specifications determine that a module cooled by this design shall not require heat dissipation of greater than 35 Watts (750W max. per 3/4 ATR). These conduction cooled modules, even with liquid cooled heatsinks, are unable to cope with the heat fluxes being produced.

Efforts to improve the heat dissipation of these modules, without redesign of the avionics enclosure or cooling system have begun. Module frames are also being made of several different types of composite materials. The composites are selected for their heat transfer capabilities, survivability, stiffness, and cost. A high end composite frame can safely dissipate 60 Watts. But, 60 Watts will not satisfy the needs of future aircraft.

The next generation platform Air Force , F-22, contains modules that far surpass this 60 Watt heat load. The F-22 program has decided to use LFT cooled module frames to alleviate the thermal problems. LFT is a method of cooling the module by passing liquid coolant directly through the center of the supporting structure of the module. The LFT cooling system is reaching its reliability limits at approximately 90-100 Watts. While this is adequate for the current avionics set, any modifications or additions in the future will be limited or impossible. Even natural degradation of the cooling system and thermal conduction paths may cause failures without an increase in the heat load on the system.

Technological advances in integrated circuit technologies has led to increasing circuit integration. This integration develops a great amount of heat at the chip level. Further development will lead to larger heat dissipation. Increases in component temperature greatly reduces the component reliability. This creates a need for better cooling techniques to increase the reliability of current and future electronic systems. The immersion cooled clamshell module AAS&T developed along with the immersion cooled enclosure currently under development shall be capable of filling the needs for cooling circuitry where other methods fail.

The largest source of stress put on an electronic module in today's avionics is temperature. Temperature causes approximately fifty-five percent of the stress endured by electronics, followed by vibration, humidity and dust. Adequate electronic cooling is necessary for future electronics to function and will help to greatly increase the mean time between failures of standard electronic systems. Increases in component temperature greatly reduces the component reliability. This creates a need for better cooling techniques to increase the reliability of current and future electronic systems.

IMMERSION COOLING:

The AAS&T program is addressing immersion cooling; this cooling method is capable of filling the needs for circuitry where other methods fail for the military as well as commercially. The goal is to demonstrate an alternative for LFT via immersion cooling.

Immersion cooling is a method of cooling by immersing the heat source in a coolant pool or bath. The heat source (i.e. the electronics) is in direct contact with the cooling liquid. Two phase immersion cooling occurs when the heat source being immersed causes the coolant to boil. This boiling is the phase change. The change from liquid to vapor removes more heat from the source and is a more efficient form of cooling than single phase immersion cooling. AAS&T's efforts also include forced convection to increase the efficiency and cooling capacity of immersion cooling.

Future uses of electronics will be of ever increasing density and will have requirements of increased reliability. Both of these goals will demand a better form of electronic cooling. Knowing that liquid coolants already exist on current military and commercial aircraft. Given the acceptance of LFT cooling; immersion cooling is the next logical step in evolution for advanced electronic packaging and thermal management.

Seeing the need for immersion cooling; AAS&T published a request for proposal in the field of immersion cooling within the SEM-E envelope. Purdue University was the contractor that was awarded the contract to investigate this form of electronic cooling. This effort was for thermal tests only, no environmental testing was performed. Many sections of this paper are taken from the deliverables of this contract and can be obtained from Naval Air Warfare Center, Aircraft Division, Indianapolis [Mudawar, 1992].

IMMERSION COOLED CLAMSHELL MODULE:

Purdue University's Two Phase Boiling Lab, under the direction of Prof. Issam Mudawar suggested using immersion cooling with boiling, or two phase immersion cooling, to accomplish our goals. Prof. Mudawar had already done a great deal of research in this area and he believed that our goal of 500 Watts in a SEM-E clamshell module could easily be met using this method. Cooling several modules in a coolant bath was suggested, but maintenance problems, and the ability to use a standard module envelope lead to the use of a previously designed clamshell module.

From Purdue's previous ventures into electronic cooling with immersion cooling, and a library of data that had been assembled from previous experiments; a specific Fluorinert liquid was shown to be very suitable for our needs as a coolant. The coolant was the 3M Fluorinert liquid, FC-72. FC-72 is an inert dielectric with beneficial thermal conductive properties. FC-72 is not a CFC, which are being banned for military and commercial use. FC-72 poses no threat to the environment. FC-72 is a Fluorinert, which means that it is essentially inert with all other substances. The thermal conductivity of FC-72 at 25°Cis 0.00057 Watt/(cm)^2*(°Ccm) [0.033 Btu/(hr)(ft^2)(°Fft)] and it has a specific gravity of 1.7. FC-72 will have no problems with lower temperatures (-55°C to 125°C), since its pour point is -90°C. To accomplish the desired two phase cooling and allow the nucleate boiling without reaching burnout; the coolant will be subcooled and the temperature will be kept below, but near, the boiling point of 56°C.

PREPERATIONS AND PRELIMINARY TESTS

Purdue began by evaluating the Navy's requirements for the module before beginning any testing or fabrication. The Navy's statement of work (SOW) called for the module design to be direct immersion cooled with liquid coolant entering and exiting through quick disconnect couplers from the bottom of the module as shown in figure 1. As a worst case condition the simulated module shall dissipate not less than 500 watts. The operational requirements for this module are an ambient temperature of 71 +/- 2°Cand the maximum module guide rib temperature shall not exceed 85°C. The flow rate of the coolant shall not exceed 0.668 ounces per minute and the subcooled inlet temperature will have a minimum of 27°C. The maximum outlet temperature and pressure drop shall be at the contractor's discretion.

Several general requirements were placed in the SOW ensure the best possible product for the Navy. The design was to minimize the operating pressure and the pressure drop through the module to lessen the load on the coolant system and allow

the maximum amount of modules in a given system. The design should also minimize the coolant flow rate also to lessen the load on the coolant system. To make the module design as attractive as possible it was a requirement to maximize the chip area. The larger the chip area, then the more modules that can be consolidated into one clamshell module, thereby saving weight and space.

It was decided to make one entire half of the module out of Lexan, so that the flow characteristics inside the module might be observed and recorded; thus making half of the module a window . This change also required a change in the minimum cooling capacity of the module. The new minimum dissipation required was 250 Watts (1/2 the original since it is only half of a module). The Lexan module half was required to be designed such that the inner surface of the window would simulate the same chip protrusions that existed on the opposite half for proper flow characteristics.

One of the goals of this effort, although not written into the SOW was the use of two phase cooling. Purdue suggested that two phase immersion cooling be used instead of only using single phase cooling. By allowing two phase cooling the cooling capacity of the clamshell module could be greatly increased. Two phase immersion cooling occurs when nucleate boiling is permitted to form on the surface of the chips. The heat removed from the chip through the heat of vaporization is much greater than the heat removed from simple conduction into the coolant or radiation. The boiling is controlled to such an extent by subcooling the inlet temperature, that no vapor is allowed to collect inside the module. The bubbles recondense into liquid before they reach the next chip in the module.

The next obstacle was how to create heat fluxes of such magnitude, accurately, and without destroying the heaters or chips each time they were used. Purdue had come across this difficulty in earlier cooling experiments. After having searched all available commercial off the shelf equipment available, they decided to design their own heaters. The heater consists of sixteen individual heaters that simulate sixteen chips on a printed wiring board. The simulated chips are made of oxygen-free copper, a thermocouple was embedded beneath the chip surface in the center of the copper block, an a thick-film resistive heater will be soldered to the underside of the copper block and supplied the heat. Each simulated chip was 0.5in x 0.5in and arranged in the module as shown in figure 2.

Before fabrication began on the immersion cooled clamshell module, Prof. Mudawar felt that the study of flow over protruding chips, as the SOW required, should be investigated. Previously Purdue had completed research on immersion cooling nine in-line chips in a linear flow channel, but they did not protrude into the flow. The equipment from the previous experiment was redesigned to accommodate simulated chips that protrude 1mm into the flow stream.

Critical Heat Flux (CHF) values were measured during the experiment. The CHF occurs when the heat flux increases and the interference between densely populated bubbles inhibits the motion of liquid near the surface of the heater. The lack of liquid causes a localized dry out and can quickly spread to the entire chip. This is the point at which the heat transfer coefficient (**H**) is a maximum. At this point **H** begins to decrease with increasing surface temperature of the chip over the saturation temperature of the coolant or excess temperature, although heat flux, which is the product of **H** and the excess temperature, continues to increase. This trend results because the relative increase in excess temperature exceeds the relative reduction in **H**. At CHF further increase in excess temperature is exactly balanced by the reduction **H**. Any increase in heat flux beyond this point will induce a sharp departure from the boiling curve in which surface conditions change abruptly; generally exceeding the melting point of the solid, destruction or failure of the system may occur. For this reason CHF is often termed the burnout point or the boiling crisis, and accurate knowledge of the CHF is important. [Incropera, 1985]. Even after adjusting for the difference in surface area between the flush mounted and the protruding chips, the protruding chips had a higher CHF.

The testing with the linear chip array and the immersion cooled clamshell module were both conducted on the same flow loop. There are two main sections of the flow loop that were used in the thermal and hydraulic testing. The first section shown schematically in figure 6, is a flow loop currently housed in the Boiling and Two-Phase Flow Laboratory at Purdue University. The different components of the flow loop are connected with plastic tubing. A magnetically coupled, centrifugal pump was used to circulate the fluid through the loop. Immediately downstream from the pump is a heat exchanger that extracts heat from the fluid generated by the clamshell module and the fluid friction along the pipe walls. The flow is then split, allowing some of the fluid to travel to the module sub-loop while the remainder of the fluid is routed though a by-pass line to the condenser/reservoir. The portion of the flow entering the module sub-loop is then passes through a 5-micron charcoal-activated filter and another heat exchanger. This heat exchanger is connected to a constant temperature bath and is used for fine tuning of the fluid temperature prior to entering the module sub-loop. After exiting the module sub-loop, the flow combines with the by-pass flow in the condenser/reservoir. The combined fluid then returns to the pump. The condenser/reservoir holds several gallons of FC-72 and helps maintain thermal and hydrodynamic stability in the loop by offering a large reservoir of liquid and vapor for the flow from the module sub-loop to interact with.

The second section of the flow loop is the module sub-loop shown in figure 7. The various components of the module sub-loop are connected with stainless steel tubing. A regulating valve located upstream from the clamshell module is used to control the flow rate through the module with the remainder of the flow going through a by-pass line in the module sub-loop. Immediately downstream from the regulating valve is a pressure gauge that is used to monitor the pressure at the clamshell module inlet. Temperature and pressure sensors are located at the inlet and outlet ports of the clamshell module to measure the inlet and outlet temperatures and pressures of the liquid, respectively. After exiting the module the flow combines with the module sub-loop by-pass line before being fed into the condenser/reservoir.

The pressure in the flow loop will be maintained by the condenser/reservoir and the pressurization/expansion located in the main flow loop. A secondary condensate tank attached to the expansion tank is used during deaeration of the fluid to insure that all noncondensable gases were removed from the fluid at the start-up of the experiments. The condenser/reservoir contains a submerged water-cooled condenser, an immersion heater, and a pressure relief valve. The cold water flow in the submerged condenser is controlled by a solenoid valve actuated by the data acquisition system. Pressure is controlled in the flow loop by regulating the energy from the immersion heaters in the pressurization tank and by introducing cold water into the submerged condenser. As mentioned earlier, the flow loop utilizes FC-72 as the coolant for this effort.

TESTING

The immersion cooled clamshell module to be tested was within the SEM-E format. Fluorinert liquid was introduced into the module cavity thorough quick disconnects (Hydraflow DC2004) located at the connector end of the module. Side A of the module consisted of the normal aluminum design, simulated chip heaters, and all of the instrumentation, while side B consisted of the Lexan window and simulated chip protrusions. Both covers are shown in figures 3, 4, and 5 with all sixteen simulated chip heaters clearly visible. Also visible are the four posts in the module. The posts were required to reduce the deflection of the thin module covers while the module was pressurized; even though the maximum internal pressure used was only 22.11 psia. Future module designs will probably not need four posts, and if made of a stiffer and stronger material than aluminum; the module may not need any internal posts.

The testing was initially divided into four main stages, the preliminary testing with the linear chip array. Initial thermal optimization testing and module testing will determine the capabilities of the simulated immersion cooled clamshell module to dissipate a minimum of 250 Watts. The thermal optimization testing examined various flow parameters and inlet coolant temperatures which influenced the performance of the immersion cooled clamshell module. Finally different methods of modifying the clamshell module with flow directors and fillers to increase the coolant flow directly over the chips and lessen the weight of the module. The final step was determined to be outside the scope of this effort, but Purdue would be free to pursue this vein, after they have proven the module's ability to dissipate 250 Watts or more.

To obtain boiling data, the power to the chips was incremented slowly while maintaining the module inlet pressure and inlet coolant temperature constant. Steady state was assumed to occur when twenty consecutive readings had standard deviation less than 0.10°C. At power levels well above 250 Watts, the testing was terminated due to vapor build up and fear of damaging the module. CHF was never reached during any of the tests performed on the immersion cooled clamshell module during this effort.

The module was tested at inlet flow rate between 0.073 to 1.84 kg/minute and inlet temperatures ranging from 27°C, the minimum inlet temperature allowed by the SOW, to 47°C in order to investigate its thermal capabilities. The inlet module pressure was maintained as close to 22 psia as was possible, while the pressure drop across the module ranged from 0.65 to 4.20 psi depending on the flow rate. Data was recorded for inlet and outlet coolant temperatures, guide rib temperature, inlet pressure, differential pressure across the clamshell module, four chip temperatures , and the chip heat fluxes.

RESULTS

All of the module tests exceeded the required heat dissipation level of 250 Watts except for two test performed at an inlet temperature of 47°Cwith flow rates of 0.73 and 1.16 kg/minute. These two test were ceased at 221 and 211 Watts, respectively. As stated earlier, none of the chips reached CHF or dryout of the liquid, but were halted for the safety of the module against vapor buildup. A summary of the pertinent data obtained during the immersion cooled clamshell module testing can be seen listed in Table 1.

Purdue graduate students and Prof. Mudawar made several significant observations while performing the tests on the clamshell module. When testing at the coolest inlet condition, the inlet temperature was 27°C, and flow rates below 1.61 kg/min., the vapor from the chips quickly condensed before reaching the surrounding chips. At approximately 15 to 20 Watts/chip, vapor began to coalesce into small pockets at the top of the module cavity, and as the heat dissipation level was increased to approximately 18 to 22 W/chip (i.e., 288 to 352 W/module), the vapor pockets grew steadily, but no vapor was observed exiting the module. Higher chip heat dissipation levels caused the vapor accumulation to accelerate more rapidly, until the lower edge of the coalescent vapor mass was level with the opening of the outlet port. Once this occurred, Small amounts of vapor were observed exiting the outlet port. The accumulation of vapor in the module never caused the chips to dry out because the chips were located below the module outlet port. The fluid level became stable at the level of the outlet port even with power increases, and vigorous boiling was observed on the chips located on the top row of the module. Increasing the flow rate served to increase the heat dissipation level at which the rapid vapor accumulation occurred. Vapor coalescence at the top of the module was inhibited, at all heat dissipation levels, by increasing the mass flow rate above 1.61 kg/min.

Vapor accumulation was also observed at the inlet temperatures of 37°Cand 47°C, but at lower heat dissipation levels. For the 47°Cinlet temperature, the leas subcooled inlet condition, vapor pockets began to for at the top of the module cavity at 5.5 to 7.5 W/chip.

Initially, it was feared that the coolant might flow inside the module cavity directly from the inlet port to the outlet port, but the trajectories of bubbles emanating for some of the chips, and the waviness induced by gradients in the index of refraction of the coolant proved the coolant circulated adequately within the cavity prior to exiting the module. Throughout the testing of the module, Chips 1 and 2 nucleated, began boiling, first. At high heat dissipation levels, larger amounts of vapor generation by Chips 1 and 2 were observed. This phenomenon may be the result of a relatively

poor liquid circulation in that reign of the module. Also, in the fully developed nucleate boiling regime, the chip surface temperatures reached steady state quicker and the inlet pressure was more stable.

Pressure drop across the module can be an important value when developing an entire system. The pressure drop for the clamshell module never went above 4.2 psi. Several examples of the pressure drop can be observed in Table 1; taken at various test conditions throughout the testing.

Even though only half of a module was tested, the module half dissipated over 400W. When the module is fully built, it will safely dissipate over 700W. Several test conditions are shown in Table 1 that illustrate the dissipation of over 400W, even up to 411W in one case.

The effort to develop and test the two phase immersion cooled clamshell module with Purdue University was a complete success. The minimum heat flux dissipation of 250W was shattered by dissipations of over 400W and none of the tests caused CHF or chip burnouts. These test proved that in today and tomorrow's military avionic environments, two phase immersion cooled clamshell modules have a place. This effort proved that two phase immersion cooling is feasible and has a promising future in military as well as commercial electronics.

With over 410 watts demonstrated on half a module and an estimated 800 watts plus for a complete module this effort demonstrates an alternative for high power dissipation problems. This effort clearly gives a solution to conduction cooled module issues. Flow and cooling characteristics indicate that several thousand watts may be dissipated from one clamshell module when flow channeling is utilized.

ON-GOING/FUTURE EFFORTS

The AAS&T program has taken the two phase immersion cooled clamshell module effort on to the next phase. A contract has been placed with Sparta Inc. of San Diego, CA, to produce a 3/4 ATR (Air Transportable Rack) that will accommodate the two phase immersion cooled clamshell modules. Sparta is to design, develop, test, and evaluate a liquid cooled, 3/4 ATR (air transport rack) standard avionics enclosure. The 3/4 ATR will house thirteen modules and is required to dissipate a minimum of 6500 Watts. The enclosure will be designed and tested to meet or exceed the requirements of MIL-E-85726 (Specification for Standard Avionics Enclosures) and the environmental requirements called out by the SHARP (Standard Hardware Acquisition and Reliability Program) hardware documentation for modules and enclosures. The contract is divided into two contract options. Option one encompasses the design and documentation of the enclosure. Option two encompasses the manufacture, testing and evaluation of the enclosure. The enclosure will be designed and tested to meet or exceed the requirements of MIL-E-85726 (Specification for Standard Avionics Enclosures) and the environmental requirements called out by the SHARP (Standard Hardware Acquisition and Reliability Program) hardware documentation for modules and enclosures. Sparta has decided to build the enclosure out of composite materials instead of the standard aluminum materials. This effort is due to be completed in FY-94.

AAS&T engineers have already been approached by designers who wish to use the immersion cooling technology. A joint effort between SHARP and AAS&T on two phase immersion cooling's first practical application demonstration is being discussed. SHARP engineers have designed a radio frequency module that will produce heat loads that far surpass current electronic cooling technologies. Immersion cooling is needed to make this module function for any length of time. All previous efforts with immersion cooling were all digital equipment. The effects of a nonhomogeneous environment, such as two phase cooling, on microwave circuits are unknown.

CONCLUSION

Although some unknowns still exists two phase immersion cooling has proved its worth in actual testing. Purdue University has proven that two phase immersion cooling can handle greater than 700 Watts in a format E module envelope. Sparta is currently proving that a 3/4 ATR can dissipate 6500 Watts. Immersion cooling is on its way to being capable of functioning in all Navy standard enclosures. Simple modifications can adapt the current design to thousands of other platforms if standardization is not required.

Purdue is also taking the immersion effort further, with several thousand watts to soon be dissipated from a single format E module. This technology will soon be available to solve thousands of thermal dissipation and reliability problems. The immersion cooled clamshell design is capable of: lowering circuit junction temperatures, reducing humidity and dust contamination, reducing electromagnetic interference in and out of the module, and reducing vibration. Future electronics will utilize more multi-chip-modules, wafer scale integration, and chip-on-board technologies. There is no question that current cooling technologies will not be able to handle these super dense circuits and the need for such a cooling technology will arise.

The future will call for two phase immersion cooling to have a role in: optical, digital, radio frequency, and power applications. This technology may also leverage new advances in other fields besides electronics. Where ever an object has overheating problems, immersion cooling with FC-72 could be a viable solution.

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DISCUSSION

Question: Do you have in mind any applications where 500W are dissipated in a small SEM-E module?

Answer: No, we have made this design with future requirements in mind. Liquid flow through cooling was claiming a 500 W capability, we anything lower would have been redundant. Our contract required 500 W minimum and had the contractor take the technology as far as they could.

Question: Do you have elements on chemical compatibility?

Answer: The FC-72 coolant is a very inert substance and shouldn't cause any problems. But it could carry a contaminant from an area where it wouldn't cause any problems to a more dangerous area. This cannot be avoided, but hopefully the filters, maintenance procedures, and even the manufacturing procedures would help to avoid this problem.

Question: Have you taken into account the complete coolant circuit in your contamination analysis?

Answer: The complete coolant circuit has always been considered. But, no, it has not been involved in any of our analysis. The cooling systems currently in existence were utilized for the contract requirements for temperature and pressure ranges, even though FC-72 is not found there . . .yet.

Question: With 250 W per module side, boiling should be distributed on the surface. How do you control the phenomena due to Critical Heat Flux?

Answer: The critical heat flux was not spread across all of the chips at the same time. Due to the irregularities of the coolant flow, it would initiate on, usually, one chip at a time. Even though we controlled each chip as close to the others as possible, they would not reach critical heat flux at the same time. In an actual system, you would know which chip would be your hot chip, and it could be the driver for your cooling system design. Again, I wouldn't recommend designing two phase cooling into a system, except for your worst case scenario.

Question: For fluorinert liquid:

a) What is the cost of the fluid?
b) Are there leaks? Could you use the Aeroquip connector?
c) Are you thinking about using non-clamshell module cases?
d) Are there any RF dielectric constant effects?

Answer:

a) The last time I heard a price for FC-72, it was $300/gal. This price would probably reduce with bulk purchases.

b) We are currently putting the quick disconnects through environmental testing in our 3/4 ATR, and have had no problems reported yet. As for using the Aeroquip connector, there should be no real problem. I would have to verify that the outer diameter and the pressure drop were within our tolerances.

c) No, we are not thinking of using any different type of module than we are already testing.

d) We believe that the temperature gradients in the coolant might cause problems with the required constant density for RF circuits. However, we had one of our experts

"run the numbers," and he felt that it shouldn't be a problem. I would want to see an actual test.

Question: What is the operating pressure and what does that do to the thickness of the clamshell?

Answer: The maximum operating pressure was 22 psia, but the module was tested for leakage at 44 psia. The clamshell thickness is 0.1 in.

Question: How much space is left for the electronics?

Answer: This leaves 0.38 in. for circuits and boards. If designed properly, short components could be put opposite tall components and allow the most room.

Question: Have you considered the burnout issue and formation of fluoric acid and contamination of your reservoir? (Work has been done at Supercomputing Inc. which did jet impingement [cooling] with flourinert.)

Answer: We have not done any work on burning FC-72, the byproducts, or how this would be handled. The material safety data sheets do not indicate any acid byproducts. They indicate that the FC-72 will first turn to gas. Most likely, your chips would fail before reaching the required temperature to break down the FC-72 and would probably cause many other problems. It is a topic which should be investigated.

Question: Please address the contamination problem of allowing fluid to impinge onto the electronics; also, [please address] sealed cards in storage going through storage temperature cycles of -55 to +125 °C.

Answer: A filter would be a requirement in the cooling system. Our current 3/4 ATR design only flows coolant over one module before returning to the pump and filter. Since FC-72 is very inert, it should flush, without mixing, the contaminants away. Also the module is almost always sealed and it would be very difficult for contaminants to get inside. Storage is an interesting problem since FC-72 boils at 56 °C. We have done tests by inserting empty modules into the cooling system; it had no problem with the influx of air. The module quickly filled with coolant. I would suggest storing the module empty.

W kg/min	Tin deg. C	Max. qtot W	Max. T1 deg. C	Max. T2 deg. C	Max. T3 deg. C	Max. T4 deg. C	Max. Tguide deg. C	Max. Tout deg. C	Pressure Drop psi
0.73	27	356.4	78.7	76.5	76.9	77.5	46.3	49.6	0.72
0.91		369.7	78.9	76.8	77.1	77.6	45.7	46.1	1.01
1.16		402.7	79.6	77.2	77.5	77.9	47.7	44.1	1.58
1.39		411.1	79.2	77	77.4	77.8	46.3	41.4	2.16
1.61		403.2	78.8	76.5	76.9	77	47.3	39.6	2.93
1.84		351.6	76.4	75.1	75.4	75.1	43.3	36.9	3.75
0.73	37	254.6	76.2	74.3	74.3	75.2	51.4	51.4	0.72
1.16		271	76.3	74.3	74.5	75.3	51.6	47.4	1.62
1.84		287.8	75.6	72.9	73.5	74.1	51.1	44.2	3.87
0.73	47	221.6	76	74.6	74.6	75.2	57.1	58.7	0.79
1.16		210.6	74.8	74	74	74.9	56.7	54.8	1.69
1.84		261.2	74.7	73.1	73.3	73.6	56.6	53.3	4.2

Table 1: Various Test Results

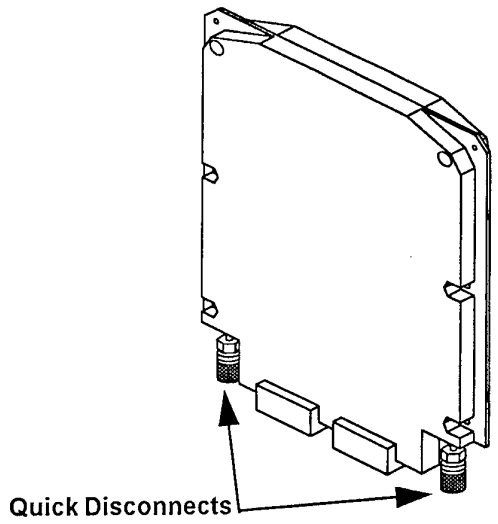


Figure 1: Sketch of Immersion Cooled Clamshell Module, with quick disconnects.

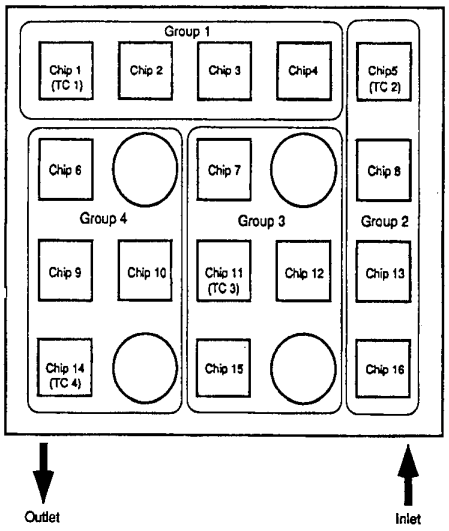


Figure 2: Module Chip Layout

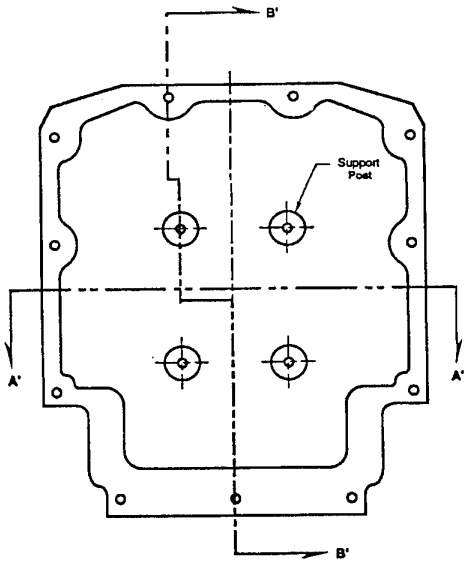


Figure 3: Immersion Clamshell Module Cover B, inside. Cover B was Lexan.

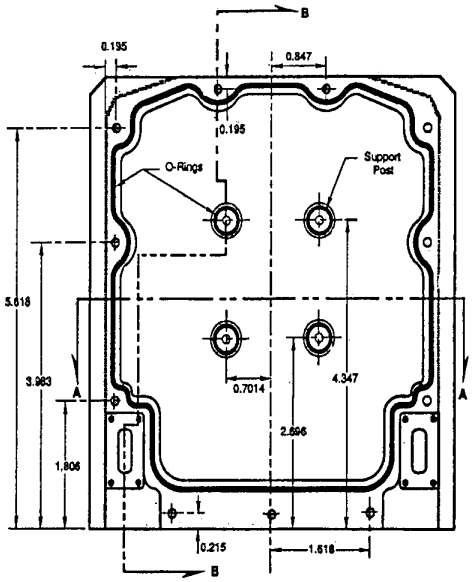


Figure 4: Immersion Cooled Clamshell Module Cover A, inside.

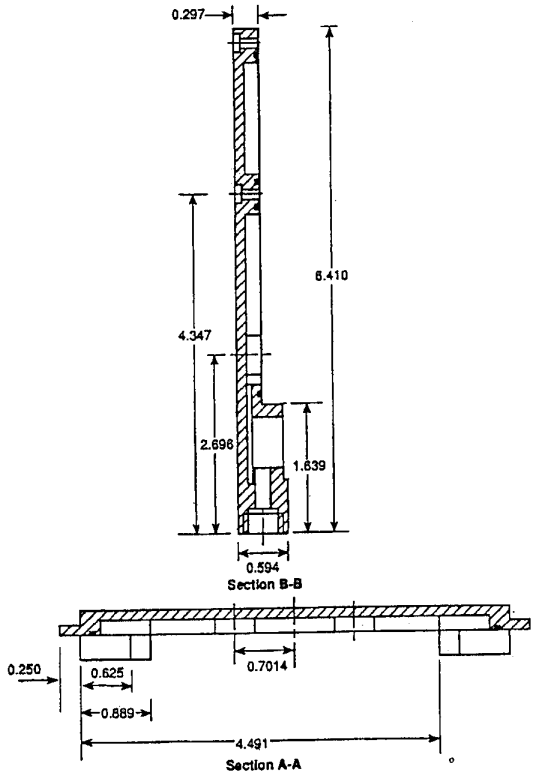


Figure 5: Cross-sectional Views of Cover A

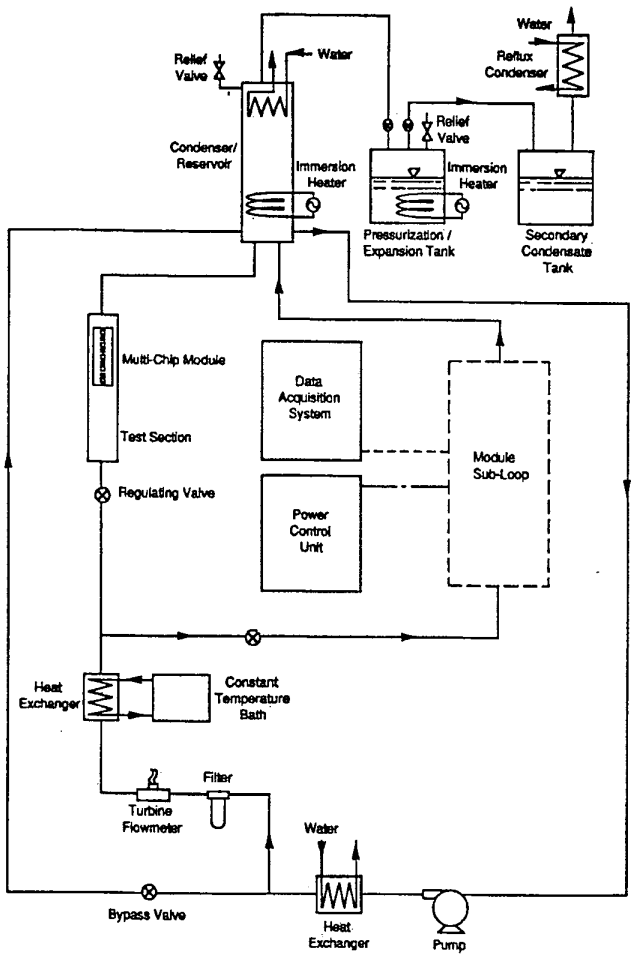


Figure 6: Schematic of Purdue's Flow Loop

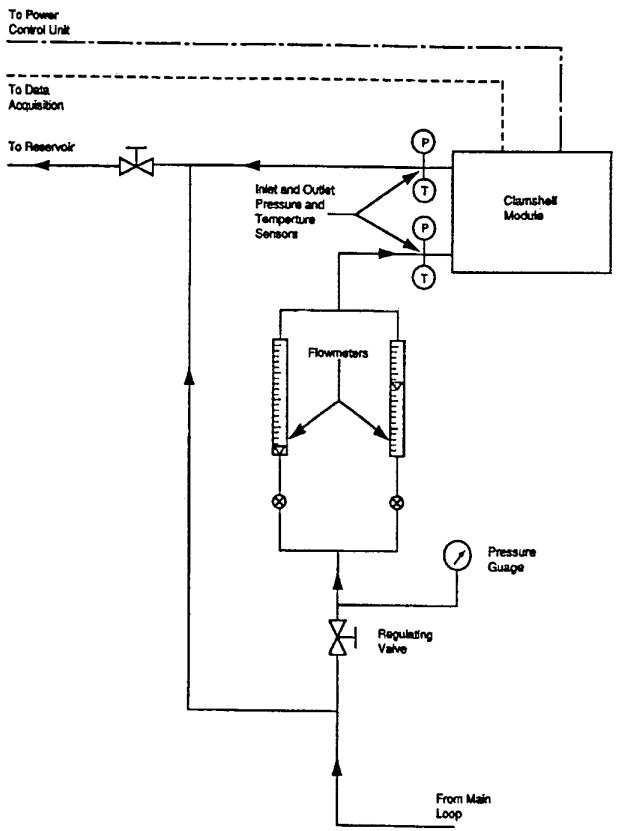


Figure 7: Schematic of Purdue's Module Sub-loop

Microchannel Heat Pipe Cooling of Modules

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SUMMARY

Purpose of this presentation is the proposal of a novel, high sophisticated cooling technique with a promising performance, but with a very early status of development, the microchannel heat pipe cooling.

This technique can be directly adapted to the basic idea of Modular Avionics resulting on the hardware side in a modular packaging design with interchangeable modules.

Due to the early status of the development and of the basic research some of the very stringent requirements for military airborne equipment are not met yet (or information is missing) like the impact of acceleration and orientation, nevertheless the normal performance capability is highly compliant with the dramatically increasing local maximum heat densities and total maximum heat dissipations, which are forecast for future avionic applications.

The presentation shall highlight the status of the development and the benefits of this technique; the latter is done by a comparison to the well established cooling methods for the module like Liquid Flow Through (LFT) and conduction cooling, in order to provide a clear impression of the cooling capabilities. Especially if the microchannel heat pipe is combined with a micro heat exchanger for the heat transfer off the module, the performance with respect to the maximum local heat density, the most challenging requirement for the future, is high in excess of the LFT method.

1. INTRODUCTION

In the past a lot of work has been performed at Dasa (formerly: MBB) to investigate on and to develop for the technologies necessary for introducing Modular Avionics.

As figure 1 indicates the programmes contained theoretical as well as experimental investigations on packaging and especially on cooling aspects for the modules and the rack aimed at implementing in military aircrafts.

This implies that these technologies for Modular Avionics have to be adapted and optimised for a combination of most severe requirements for airborne equipment as

- low weight/volume,
- high efficiency of power and thus low cooling demands,
- high reliability/failure tolerance,
- improved maintainability/repairability,
- durable towards excessive environmental stress (i. e. vibration, acceleration, EMC/EMI, ambient temperature, humidity and pressure, NBC – threat),
- low cost during life cycle.

The investigations conducted for the cooling aspect have revealed, that for today's avionics, packed in a modular manner and with a maximum total heat dissipation of 50 W for a SEM-E-module and a maximum local heat density at component (= heat source) level of 10 W/cm^2, the adequate and proper adapted cooling method is given by:

- conduction cooling on module side combined with
- thermal efficient mechanical clamping of two opposite module edges to the rack and
- forced air (or liquid) cooling of the rack by the means of two cold plates on top and bottom of the rack.

Since future electronics developments will lead to

- dramatically increased total heat dissipations
- dramatically increased heat densities at component level (forecast see fig. 2)

a cooling method different from conduction cooling has to be found, also capable of best accomplishing the above mentioned severe requirements for military aircraft usage.

Microchannel heat pipes (also named miniature heat pipes) as a novel derivative from macro heat pipes (with wicked material or with macro grooves) promise to show these capabilities though they are at the starting point of their development.

In the following the status of development together with the main characteristics of the microchannel heat pipes will be presented in comparison with a conventional, more or less just-to-adapt cooling method, the Liquid-Flow-Through (= LFT) cooling technique.

For further orientation also the basic properties for conduction cooling as the appropriate cooling method for today's avionics are evaluated.

2. METHOD

Two variants of microchannel heat pipe cooling for modules are envisioned differing mainly

- in the capability of total heat transfer and of heat density and
- in the interface to the rack, being a wet respectively a pure dry, mechanical one.

Both variants are depicted in the physical design configuration where the components of the two circuit boards per module face each other, since the circuit boards and the associated cooling layers form an enclosure being turned around to build up the outside of the module.

This design is looked upon to be superior to the conventional module layup, where two circuit boards are arranged in the

middle of the module embodying cooling layers and with components on both sides of this compound; main advantages are:

- flexibility with respect to component height
- cooling layers plus circuit boards form the cover layers of the module and therefore they take over the three functions: cooling, mechanical and electrical protection of the module.

Variant 1 (see fig. 3) with the best properties for total heat removal and for heat density is mainly composed of

- heat transfer inside the module by flat microchannel heat pipe layer
- heat transfer off the module and off the heat pipe layer by micro heat exchanger at one edge of the module supplied by quick connect couplings ("wet interface") with the rack and the platform's cooling fluid

The heat transfer path for Variant 2 (see fig. 4) is formed by

- also flat microchannel heat pipe layers inside the module and
- conduction cooling across the thermal clamping ("pure dry interface") to the rack thus replacing the module's micro heat exchangers of Variant 1 and
- (macro) forced convection cooling to the cooling fluid inside the rack's coldplate.

The envelope of usage regarding total heat load and heat density is inferior to Variant 1, but within these limits the benefits of Variant 2 lie in the interchangeability with the conduction cooled module due to the identical physical interfaces.

This is an important advantage, since though the trend of avionics goes for dramatically increased total heat dissipations and heat densities there will also be a number of modules with minor cooling requirements allowing the usage of conduction cooling.

3. RESULTS

3.1 Data Base

The theoretical and experimental data base for these cooling methods for modules are derived on results of a long-lasting cooperation between Dasa and the Karlsruhe Nuclear Research Center (Kernforschungszentrum Karlsruhe = KfK).

One of the central test series up to now has been the evaluation of the performance for the two different types of microchannel heat pipes:

a.) type I with transversal channels (grooves) and longitudinal arteries (see fig. 5)
b.) type II only with longitudinal channels (grooves) (see fig. 6)

and both with identical outer dimensions (see fig. 7).

Fig. 8, which is scanned by an electron micrograph, can provide a feeling for the physical miniature and quality of the microchannels forming the capillary structure (instead of conventional used wicked or poreous material or macro grooves) and thus the main new feature of this kind of heat pipe.

The curves in the diagram of fig. 9 show the thermal performance, especially the thermal resistances, of the type II microchannel heat pipe (longitudinal channels) and the dependency from the orientation.

It should be noted that

- the differential temperature ΔT was obtained by measuring the surface temperatures of the heat pipe at the location of the heat input and of the heat output to the heat pipe and thus the overall efficiency of the heat pipe inclusive the contact resistances of the temperature sensors are presented,
- the maximum measured heat power of 120 W stands for a maximum local heat density of 60 W/cm^2 for the surface both for heat input and for heat output to the heat pipe, leading to an overall thermal resistance of only 0.4 K/W
- the properties of a copper bar with the same outer dimensions and conduction as the heat transfer method are given for comparison.

In the following these test results are used to derive characteristic performance data for cooling of a module in SEM-E-format, and this is done in comparison with conventional cooling methods as Liquid Flow Through and conduction cooling.

3.2 Characteristic Performance Data in Comparison to LFT and Conduction Cooled Modules

Thermal resistances between heat source (die) and heat sink (cooling fluid) are used to assess the performance of the different cooling methods.

The main assumptions the calculation is based upon are worst case cooling conditions for future envisaged usage for this thermal path to zoom the capabilities and differences of the cooling methods:

For this purpose only a die forming a part of a MCM (= Multichip Module) is considered with:

- die's heat density: 100 W/cm^2
- die's cross section: 5 x 5 mm^2 leading to
- die's heat dissipation of 25 W
- die's location on the module to result in the worst case, i. e. longest possible, path for heat transfer associated with the encountered cooling method

The modules physical dimensions are taken to be (as a good approximation for the SEM-E-format)

- length: 150 mm, width: 150 mm, thickness: ≈ 15 mm
- with two circuit board integrated to the module

The total heat dissipation of the module is assumed to be 200 W with each of the two circuit boards producing 100 W.

With this approach the utmost forecast for the avionics of the year 2000 (100 W/cm^2 as the maximum local heat density and 200 W as the maximum heat dissipation for a SEM-E-module) is the basis for the comparison.

The thermal resistances between die and the appropriate module's cooling method in form of the contact resistances and the conduction through the MCM and the circuit board are not subject of this comparison here and thus not considered.

Fig. 10 to fig. 13 summarize the results obtained in showing the associated module's cross section, the belonging model for the thermal resistances and a table quantifying these thermal resistances.

The main characteristic figure for the effectiveness of the cooling method, the total thermal resistance, is graphically provided in fig. 14 for all the four methods, clearly showing the superiority of the microchannel heat pipe cooling method, even in the version (Variant 2, see fig. 4) with thermal clamping and thus dry interface to the rack.

As detailled investigations reveal there are several reasons leading to these rather great differences in total thermal resistance with respect to the different cooling methods:

1. Heat transfer coefficient:
   This coefficient is drastically increased for the micro structures as used for micro-channel heat pipes and micro heat exchangers due to the thermally very effective process of evaporation and condensation for the microchannel heat pipe and due to improved hydraulic performance for the micro heat exchanger and due to a fin efficiency of almost 1.0 (0.98!) for both.
   Values verified by experiment lie in the range of 40000 W/m^2K, instead of 2000–3000 W/m^2K for Liquid Flow Through module cooling; these figures of heat transfer coefficients are refering to the cross section for the heat transfer and not to the enlarging wetted surface for the heat transfer.

   Also the heat transfer coefficient for the contact resistance of the thermal clamping needed for Variant 2 (instead of the micro heat exchanger for Variant 1) is not a limiting factor as assumed up to now:
   It can reach values of 10^4 W/m^2K (see ref. 3) for a conduct pressure of 25 bar which is achievable with state-of-the-art clamping devices.

   Since the heat density distribution across a module of the future will look like the example of fig. 16, cross-section A–A, with very high peaks and a lot of areas inbetween with a heat density equal to zero, it is quite evident, that priority has to be laid on the cooling method's capability for coping with extreme heat densities, which is characterised by the heat transfer coefficients.
   The average heat density – as depicted in the cross-section of fig. 16 – will be very low, but it must be neglected for selecting and designing the cooling method.

2. The length of associated conductive pathes can be kept very low due to the micro structures the microchannel heat pipe and micro heat exchanger are based on. This also leads to lower thermal resistances for conduction through walls compared to macro structures.

3. The heat transfer inside the heat pipe is performed by mass transfer (of vapour) resulting in a neglectible temperature difference (due to pressure loss of the vapour) despite the length of the heat transfer path.

4. Due to the heat transfer by mass transfer inside the heat pipe the spreading of the heat density can be performed without adding an extra thermal resistance for this purpose which would be the case for LFT or for conduction.
   Fig. 15 depicts schematically this spreading function using the example with the die of 5 mm x 5 mm basic area and producing 25 W and with a total heat load of 200 W for the module, distributed equally to the two contained circuit boards (leads to 100 W per circuit board).
   The original heat density of 100 W/cm^2 at the die's side is spread by the means of the mass (vapour) transport to 13.3 W/cm^2 at the micro heat exchanger's side for Variant 1 respectively at the clamped module edge's side for Variant 2.

Another, more practical comparison of the different cooling methods can be gained by assessing their capabilities with respect to the allowable maximum local heat density combined with the allowable maximum total heat dissipation for instance for a module in SEM-E format and for the cooling requirements for a military aircraft.

These characteristic data can be derived from the obtained total thermal resistances under the assumption of identical cooling conditions.

The data is expressed in fig. 17: Dots stand for data quantitatively derived from the aforementioned total thermal resistances for the four cooling methods.

The associated, section lined area shall be looked upon to show in a qualitative form the tendencies of the limitations of these cooling methods.

It can be seen that the LFT method can cope – due to its direct way of cooling – a huge range of heat dissipation at a constant, but rather low level of local heat density. The value of 18000 W for the total heat dissipation of the module is a theoretical, virtual value either neglecting an increase of the temperature of the cooling liquid or assuming an infinite amount of cooling mass flow.

For the purpose of only comparing different cooling methods for the module this is a legitime way to keep the boundary conditions equal and identical; nevertheless further investigations should incorporate this interface to the aircraft's infrastructure and the infrastructure itself to see the limitations which are superimposed by them to the overall cooling design.

4. CONCLUSION

The presentation should have revealed two main points:

a. Because of the excessive effort for higher integration and higher tacting frequency for future avionics the thus dramatically increased local heat densities will become the overwhelming driving factor for selecting the appropriate cooling method.
b. Microchannel heat pipes provide a promising and adequate cooling method to be capable to cope with these future high density heat sources for mainly two reasons
   - high performance with respect to high local heat densities and
   - ability of spreading, of lowering heat densities with neglectible penalties (i. e. thermal resistance) by heat transfer by mass (vapour) transfer

Due to the very early state of development of this cooling technique even a lot of principle effects need further clarification and investigation such as:

- making use of and optimise for nuclear boiling for evaporation
- introducing droplet condensation instead of nowadays film condensation
- optimising of geometries of grooves and the heat pipe's plenum
- selecting the proper working two-phase fluid
- using (micro-) pumps for making the heat pipe insensitive towards orientation and acceleration
- developing of accurate simulation tools

These investigations will also allow a better understanding of the influence of orientation and acceleration on the effectiveness of the microchannel heat pipe combined with methods to compensate for these deteriorating effects.

As module cooling is only one step of the thermal ladder in the overall cooling path between heat source (die) and ultimate heat sink (e. g. the environmental control system of an aircraft), it has to be optimised for the boundary conditions which are given in form of the interfaces to the adjacent steps of the thermal ladder.

Nevertheless the whole thermal path has to be adjusted to the same level of thermal effectivness to prevent an uneven overall design with implicated bottle necks.'

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Program	Period	Content
NAS - Phase I	5/87 - 3/88	general survey study on the properties of Modular Avionics
NAS - Phase II ***+ ASAAC Feasibility Study Phase I***	10/89 - 2/94	special topics of NAS I
inhouse R+D activities	6/87 - 12/92	experimental program in cooperation with the supplier industry; subjects: modular components, bus structures, packaging

NAS = Neue Avionik Struktur (= New Avionics Structure)

Figure 1: History of Modular Avionics Programmes at DASA

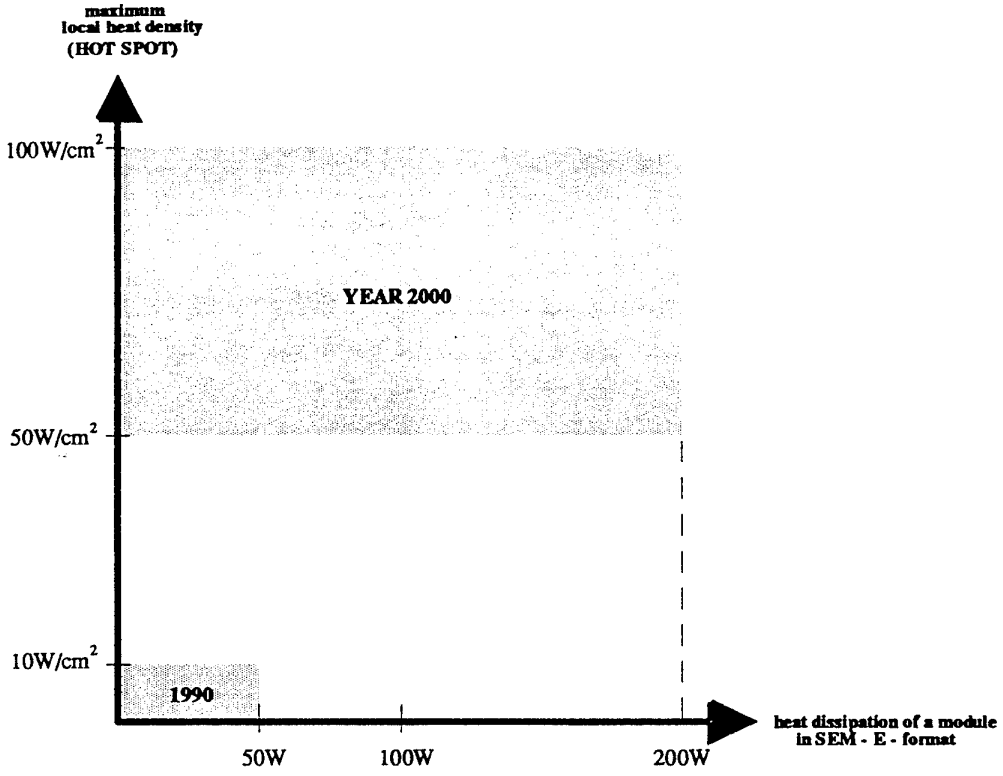


Figure 2: Trends in Avionics Heat Loads

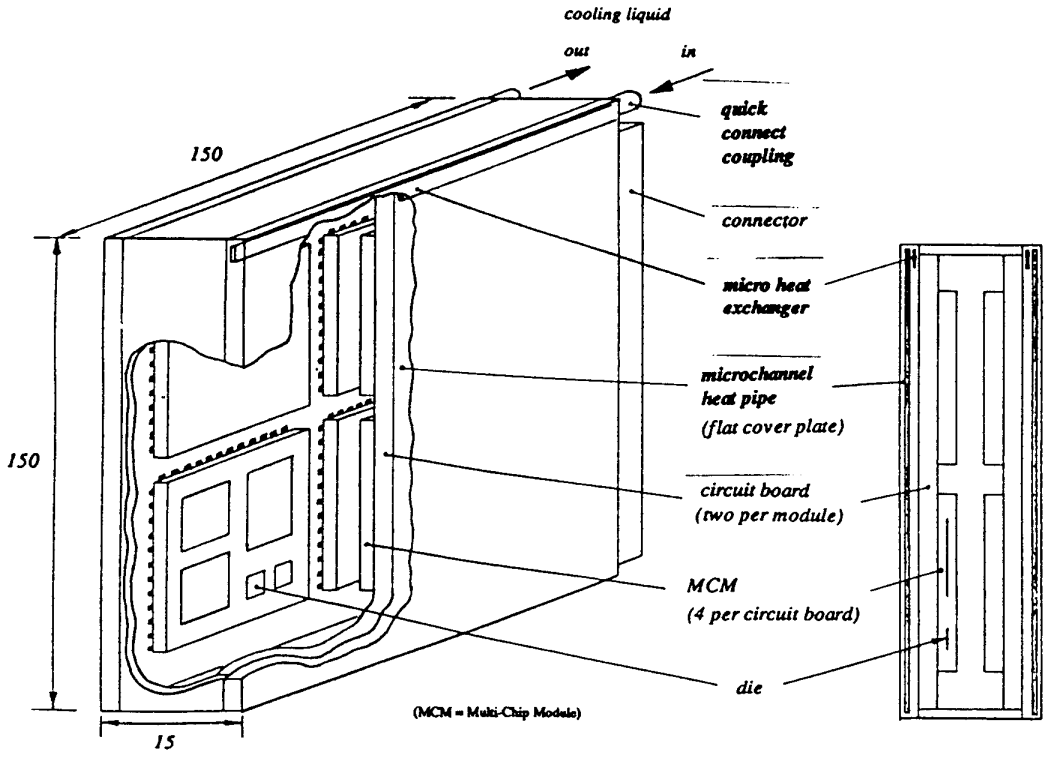


Figure 3: Variant 1 for Module Cooling:
Microchannel Heat Pipe (Flat Cover Plate) combined with
Micro Heat Exchanger and Quick Connect Couplings

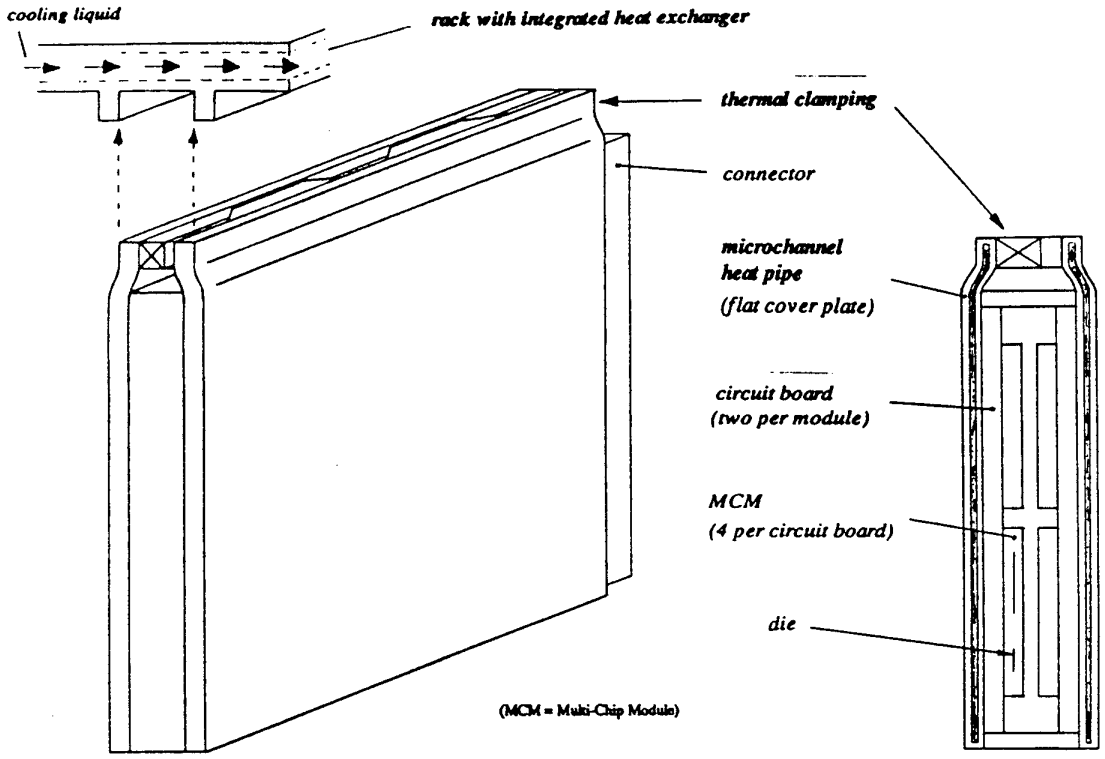


Figure 4: Variant 2 for Module Cooling: Microchannel Heat Pipe (Flat Cover Plate) combined with Thermal Clamping and Rack Heat Exchanger

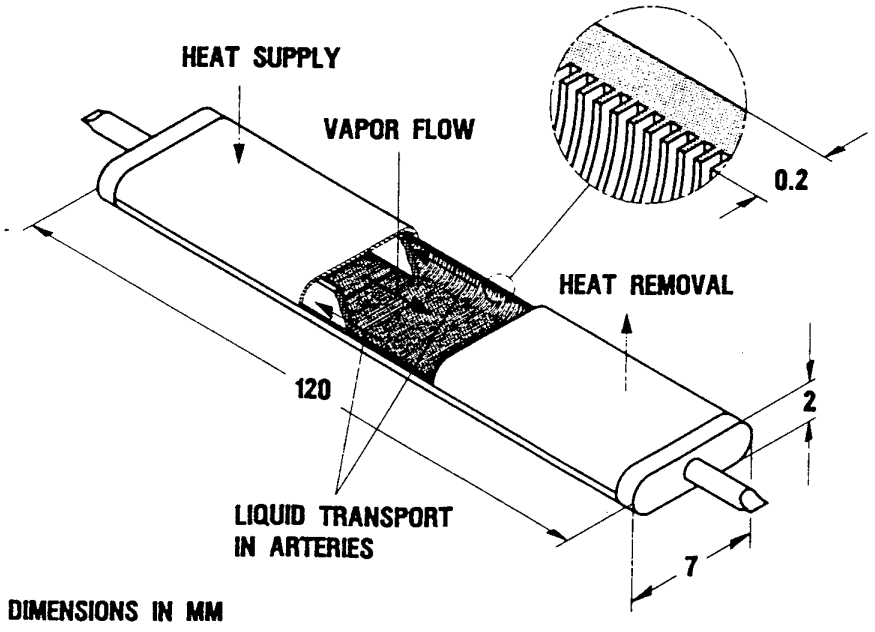


Figure 5: Microchannel Heat Pipe, Type I, with Transversal Grooves and Arteries (from ref.1)

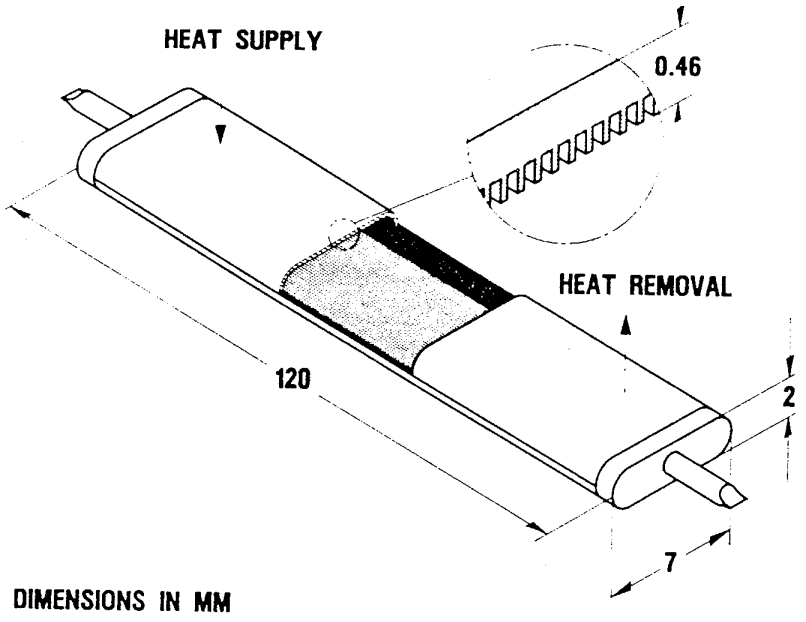


Figure 6: Microchannel Heat Pipe, Type II, with Longitudinal Grooves (from ref.1)



Figure 7: Specimen for Testing the Microchannel Heat Pipes: Type I on bottom, Type II on top. Material Cu; length 120 mm; cross section ca. 2mm x 7 mm (from ref. 1)

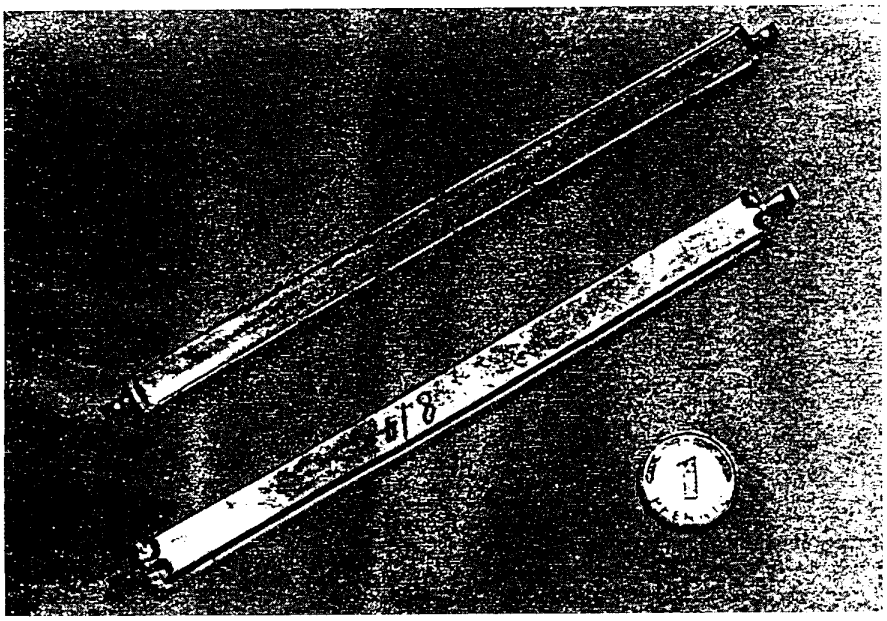


Figure 8: Scanning Electron Micrograph of an Example of Micro Structures (from ref.1). Foil Thickness: 100 µm; cross sections of the channels: 85 µm x 70 µm; bottom thickness: 30 µm; fin width: 30 µm

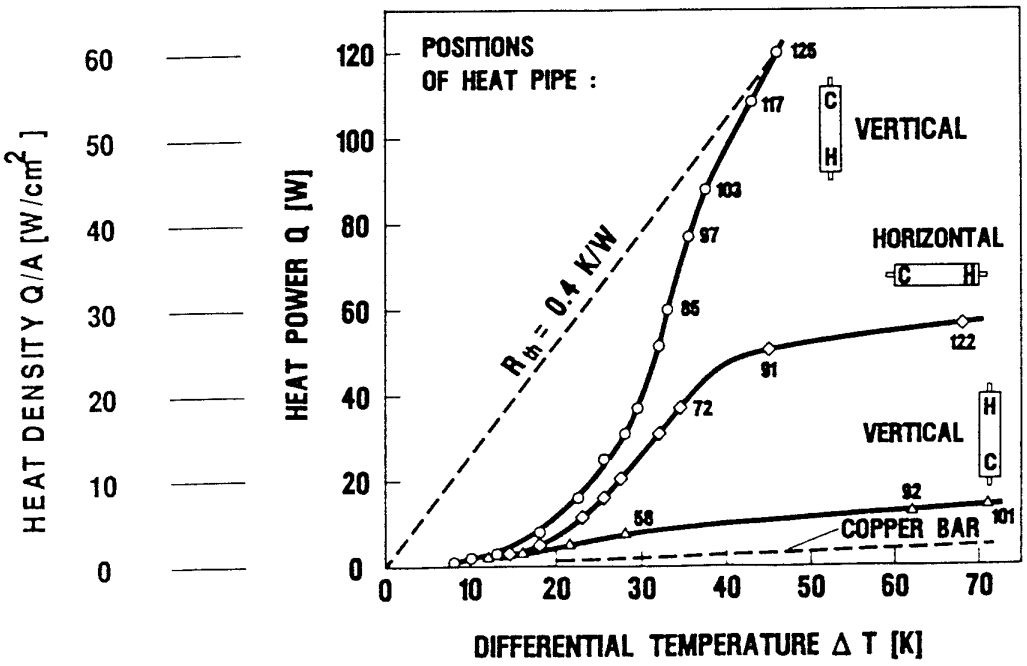
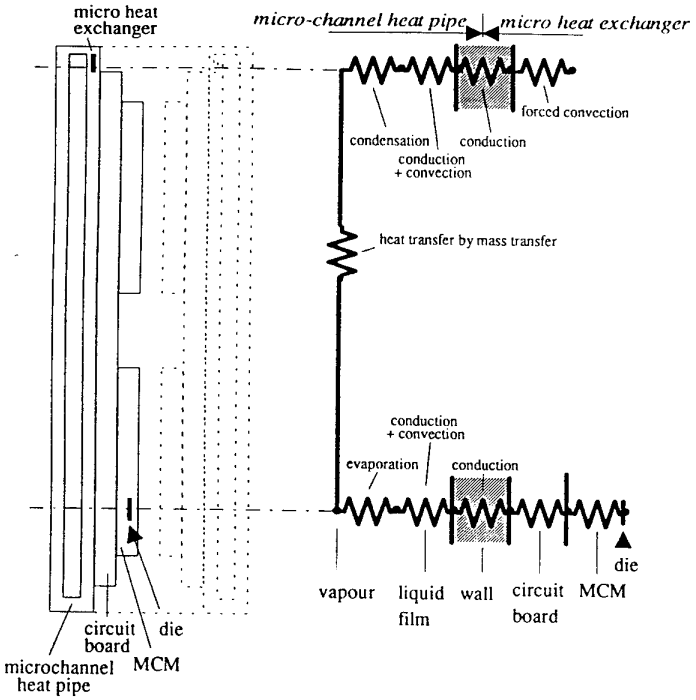
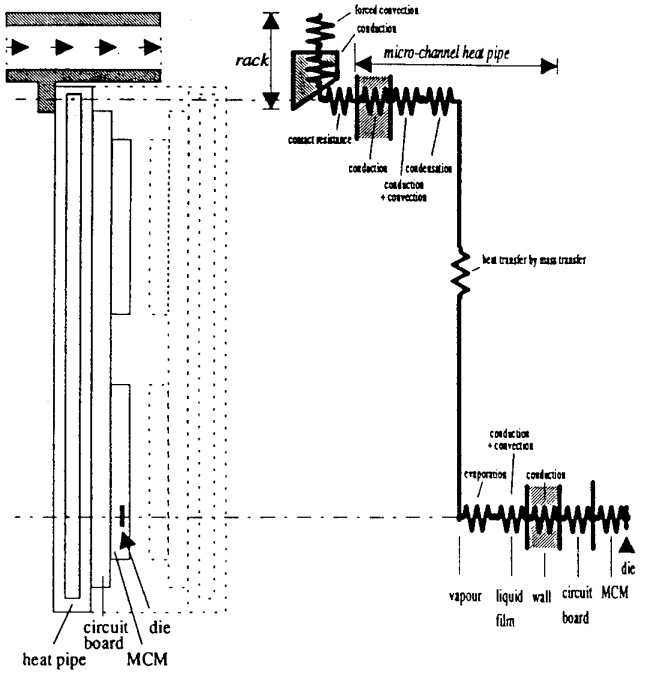


Figure 9: Heat Transfer of a Type II Heat Pipe for Different Orientations (from ref. 1). C= Cooling zone, H= Heating zone; cooling water temperature 28 deg C, numerical values entered at the measuring points: temperature of the heating surface



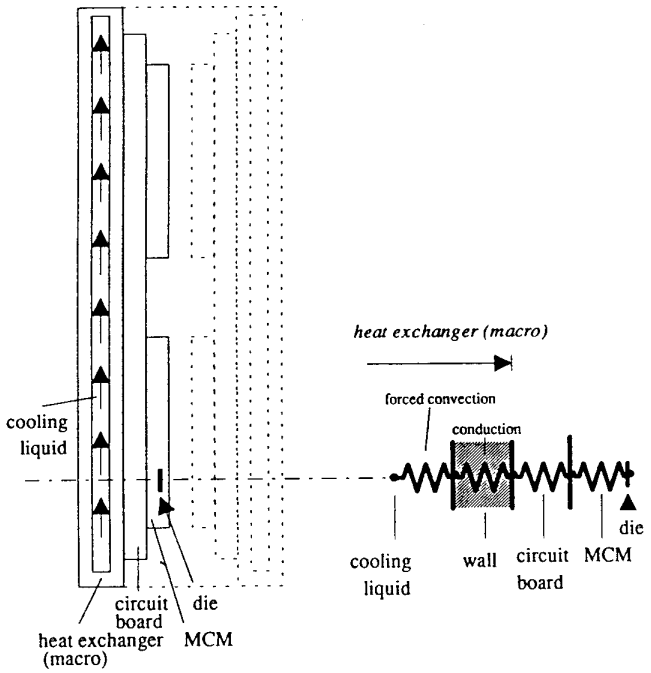
Microchannel Heat Pipe + Micro Heat Exchanger	R_{th} [K/W]
micro-channel heat pipe:	
- wall	0.022
- liquid film	0.615
- evaporation	0.667
- heat transfer by mass transfer	0.100
- condensation	0.089
- liquid film	0.082
- wall	0.003
micro heat exchanger:	
- forced convection (micro)	0.116
total	**1.694**

Fig. 10: Micro-channel Heat Pipe combined with Micro Heat Exchanger



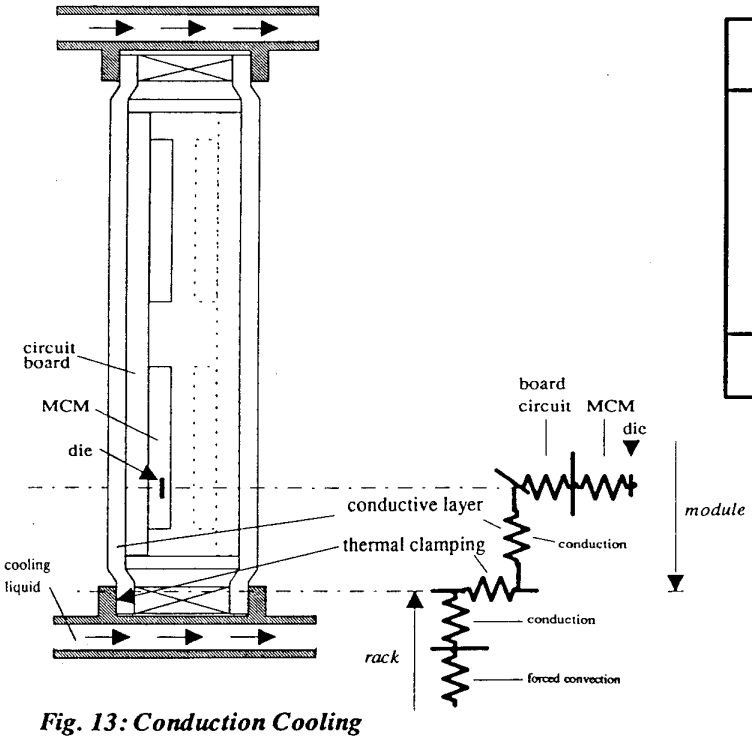
Microchannel Heat Pipe + Thermal Clamping + Rack Heat Exchanger	R_{th} [K/W]
micro-channel heat pipe:	
- wall	0.022
- liquid film	0.615
- evaporation	0.667
- heat transfer by mass transfer	0.100
- condensation	0.089
- liquid film	0.082
- wall	0.003
thermal clamping:	0.420
rack heat exchanger:	
- rib	0.410
- forced convection (macro)	0.667
total	**3.038**

Fig. 11: Micro-channel Heat Pipe combined with Thermal Clamping and Rack Heat Exchanger



Liquid-Flow-Through (LFT)	R_{th} [K/W]
macro heat exchanger:	
- wall	0.10
- forced convection (macro)	4.00
total	**4.10**

Fig. 12: Liquid Flow Through (= LFT)



Conduction Cooling	R_{th} [K/W]
conductive layer:	7.212
thermal clamping:	0.210
rack:	
- rib	0.205
- forced convection (macro)	0.333
total	**7.96**

Fig. 13: Conduction Cooling

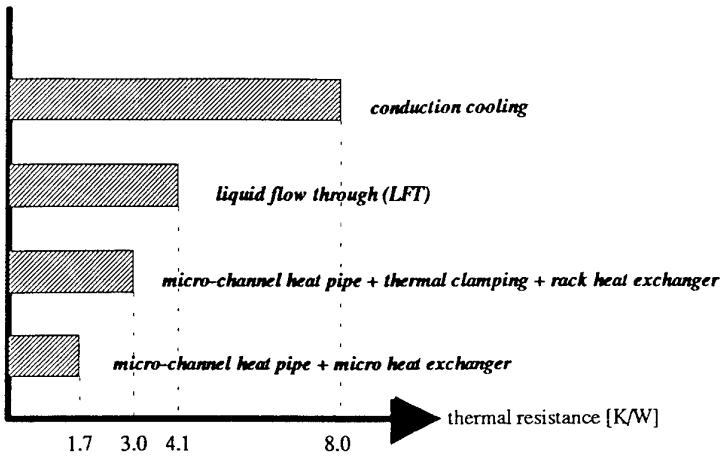


Fig. 14: Comparison of the Total Thermal Resistances between Circuit Board and Cooling Liquid

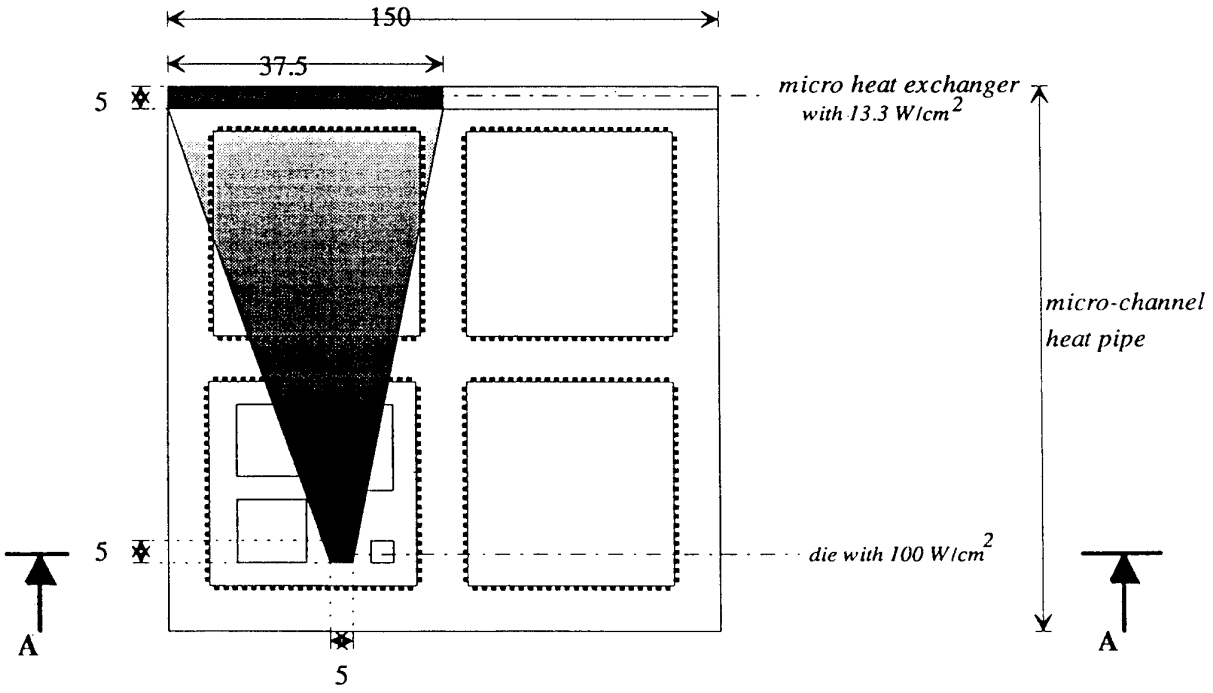


Fig. 15: Effect of Spreading of Heat Density by Mass Transport inside a Flat Heat Pipe

DISCUSSION

Question: How do costs compare between liquid flow through modules and modules using microchannel heat pipes?

Answer: This cannot be stated at the moment due to the early status of development.

Question: Have you thought about the expansion and contraction problems of heat pipes, since they are a sealed system?

Answer: This can be adjusted to the existing requirements by choice of working fluid. Nevertheless, for main working fluids, this question is less challenging due to the low evaporation pressures.

Comment: I believe you have understated the thermal performance of liquid flow throughs. In your paper, you state a thermal resistance [for LFT] of 4°C/EW. In fact, it is closer to 0.09°C/W. We also have customers who are achieving 0.05°C/W.

Author's Reply: The figure for the thermal resistance depends primarily on the assumptions one makes, e.g., for the mass flow and the pressure loss [as well as] which portion of the thermal path is looked upon and modelled.

Follow-up Comment: My models say that it is 4.1°C/W. Our results are based on empirical data.

Author's Reply: My model is also based on experimental data just recently gained which showed good compatibility with data available from [the] literature.

THE IEEE SCALABLE COHERENT INTERFACE -- AN APPROACH FOR A UNIFIED AVIONICS NETWORK

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1.0 Summary

The U. S. Navy Next Generation Computer Resources (NGCR) High Speed Data Transfer Network (HSDTN) program has chosen the IEEE Scalable Coherent Interface (SCI) as one of its baseline standards. This paper proposes to use SCI as a unified avionics network and describes SCI and extensions to it--particularly an extension known as SCI/ Real Time (SCI/RT). Because SCI can be used in a serial configuration, such a network provides an alternative to the need for ever denser and ever more reliable backplane connectors by reducing the number and size of interconnects and, hence, the need for large numbers of pins. In addition, SCI reduces packaging problems by using a small amount of board real estate and by using distance insensitive links which can extend board to board or box to box, thus facilitating a distributed backplane approach for retrofit aircraft applications. SCI is currently being applied to both ring and switch based networks, to both parallel and to serial implementations, to both message passing and shared memory computing paradigms, and to both electrical and optical physical layers.

SCI/RT is a set of proposed enhancements, developed initially by the Canadian Navy and now being evaluated by the NGCR HSDTN and IEEE working groups, to make SCI more fault tolerant and to provide the determinism and priorities necessary to support Rate Monotonic Scheduling. Addition of these features will allow SCI to perform, in a unified and seamless manner, the functions of command and control interconnect, data flow network, and sensor/ video network. Electrical and optical, and serial and parallel links can be intermixed for the most cost effective solution. As an added benefit, SCI has potential for use interconnecting multiple processing chips on the same board. Because SCI development has taken place in an open IEEE forum, it is cross national having implementation efforts by U. S. (Vitesse, LSI, Unisys, Convex, Apple), French (Thomson CSF, Bull), and Norwegian (Dolphin) companies.

2.0 Introduction

Current avionics architectures utilize a number of different digital interconnects for a number of different avionics applications. Figure 1 shows a typical design for a current system with the various interconnects conspicuously labeled. These interconnects were designed in the mid to late 1980s. With the rapid advances taking place in digital electronics most of these interconnects soon will become quite dated. Indeed new commercial interconnects are being developed with an order of magnitude higher speed than the current networks shown in Figure 1. The speed and flexibility of these new interconnects opens the opportunity for reducing avionics costs by allowing a single network to replace most or all of the current interconnects shown.

3.0 The Need For A Unified Avionics Network

As stated above, technology has progressed to the point that a single unified interconnect has become feasible. It is not only feasible, it is also desirable for the following reasons.

First, using multiple interconnects on a module takes excessive board real estate and may require more pins than would be necessary with a single interconnect. Special logic is needed to decide which interconnect to use for which purpose. In addition, reducing the number of pins and logic can increase system reliability. For example, if a system has 400 pins per connector and 200 modules, the total number of pins where a failure could occur is 80,000.

Second, passing data from one interconnect to another interconnect requires special interface modules called bridges or gateways. Because of dissimilarities of the interconnects, data passing through a bridge is often delayed. This results in increased latency and lower performance for the

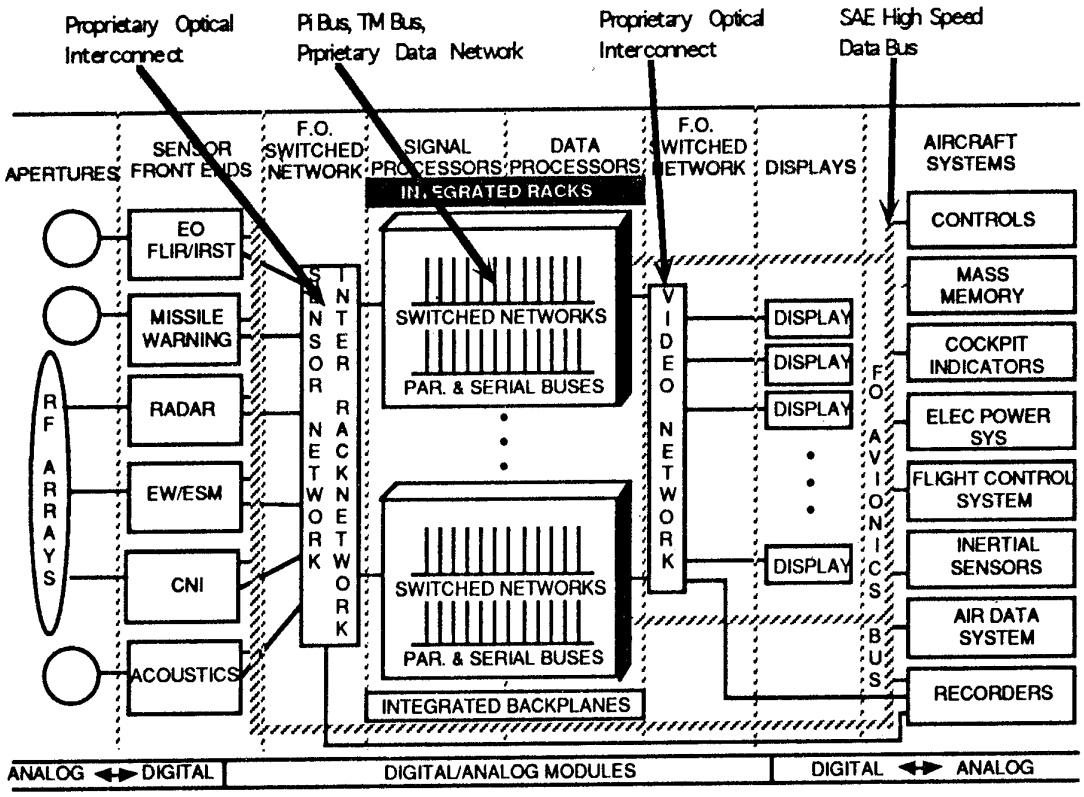


Figure 1. Example of a Current Modular Architecture

processors involved. Using a single interconnect system across the avionics system can eliminate bridges and support "wormhole routing", resulting in improved avionics system performance.

Third, buses require very elaborate backplanes with multiple power and ground layers to control high frequency ground bounce and noise which infects single-ended bused interconnects. Because of the high frequency at which new semiconductors switch, very high frequency noise is produced. Since most high frequency current is carried on the surface of conductors (the skin effect), a large number of grounding and power surfaces is necessary in a single ended tapped backplane. This requires many ground and power planes causing backplanes to become very thick (1/4 inch or more) and heavy (on the order of several pounds). Point to point links, either differential electrical or optical can result in much simpler and lighter backplanes.

Evolving technology places some additional requirements on the interconnect which cannot met by current interconnects. For example, the recent developments in parallel processing hold promise for making avionics systems much more capable and making software simpler and more scalable in very high performance applications. Studies, such as the Westinghouse "Parallel Processor Applications Study", (1989) done for Pave Pace, have shown that to maximally exploit future sensors, processing requirements will have to reach many hundreds of BOPS. Thus the interconnect must be capable of supporting hundreds of processors. Some high performance avionics applications which might benefit from parallel processing are fused sensor tracking applications, automatic target recognition, and sensor signal processing.

Currently, software in most parallel processing avionics applications is custom coded to make efficient use of the processors. This makes the software non-transportable and difficult to scale to larger or smaller processor configurations as computing needs change. By using a cache coherent computer paradigm, software can be made simpler and more scalable. Therefore, the interconnect must be able to support cache coherent shared memory architectures.

An interconnect which supports shared memory must also have the property of very low latency. Although a processor in a cached shared memory system waits for a new cache line only a small percentage of the time, a high latency

interconnect can cause this wait to be significant. With processors expected to reach 1000 MHz by year 2000 every nanosecond latency delay means a lost processor cycle. If a large number of parallel processors are waiting for memory access, the lost cycles can add up in a hurry. Presently it is not uncommon for large parallel systems to achieve processor utilization of less than 20%. This must be improved upon if parallel processors are to become feasible.

Networks used in military systems must meet the special military needs for harsh environment, fault tolerance, real time usage, maintainability, and testability. Current networks shown in Figure 1 meet most of these requirements. A unified network will also have to meet these requirements. However, one additional requirement which is necessary for a unified network is that it be able to mix command and control messages with streaming data and be able to ascertain that the command and control messages are not blocked by the streaming data. This requires a schedulable network using a technique such as Rate Monotonic Scheduling, or use of a very fast but lightly loaded network so that messages have little impact on one another.

A unified avionics network must be flexible enough to be used in different applications. Since some interconnects are less than an inch in distance and some are many yards long, the unified network must be relatively distance insensitive. Since some interconnects, such as shared memory interconnects, require multi-Gbits/sec bandwidth to keep up with emerging processor technology, and some interconnects, such as video networks are less than a Gbit/sec, the network should efficiently support a variety of bandwidths and be upwardly scalable. With present limitations on serial bandwidth to one or two Gbits/sec, parallel as well as serial versions of the interconnect are needed, at least for the present. Finally, the interconnect should be able to support both electrical and optical implementations, since optical is needed for long distance and for EMI control whereas electrical implementations are smaller, cheaper and sufficient for most "inside the rack" applications.

Another consideration is that new military systems want to leverage commercial technology. This is an important consideration in the U.S. Navy's Next Generation Computer Resources (NGCR) program. Leveraging commercial technology will provide lower costs and give an upward migration path, as long as popular standards are selected. However, the downside of commercial technology is that popular items are not necessarily based on the best underlying technology, but on other factors such as marketing. Thus commercial technology cannot be used blindly and enhancements are often needed in applying commercial technology to military systems.

4.0 Proposed Avionics Architecture Using a Unified Network

In a unified avionics network one interconnect will be used for a sensor network, video network, inter-rack network, command and control network (both backplane and inter-rack), data flow network and test and maintenance network. It must have the performance, flexibility, and scalability to be used in these different applications. A unified avionics network will lessen or eliminate the need for interface modules and logic to go between the different interconnects. A reduction in the number of unique interconnects will reduce cost and weight, improve performance and provide a path to parallel processing.

The IEEE Scalable Coherent Interface (SCI), IEEE Std. 1596-1992, is a good candidate to form the basis for such a unified network. SCI is a high performance, flexible and scalable network. It allows up to 8 Gbits/sec on each link, and since it is point-to-point it allows multiple simultaneous 8 Gbit/sec conversations. In addition, node latencies are relatively low (on the order of 25 to 100 nanoseconds). Point to point links can be configured as a centralized switched network, distributed switch, ring-based network, mesh, butterfly, hypercube and more, all of which can be intermixed in the system. The physical media can be electrical or optical, serial or parallel or intermixed. Its relative distance insensitivity allows its use as a peripheral interconnect to mass storage, sensors, and displays in addition to interconnecting parallel processors. SCI supports both message passing and cache coherent shared memory computing paradigms. It supports up to 64K nodes. And since simultaneous conversations are possible, the bandwidth scales with the number of processors.

Figure 2 shows SCI/RT used as a unified network replacement for the current interconnects shown in Figure 1.

5.0 Description of Baseline SCI

SCI is an interconnect system designed for both backplane and local area network usage. It was designed for high performance commercial computer systems and has been adopted by a

number of commercial computer manufacturers. Commercial interface chips are available with additional research taking place to improve performance and capability and establish long term viability.

In its basic format it is a system of rings and switches. It is intended for very high performance parallel processing--from small scale parallel to massively parallel. Rings and switches were selected as the basic communication medium, because they require only point to point links rather than multi-drop T tapped bus lines. Point to point links provide inherently cleaner signals and hence can run at higher speeds and lower voltages than multi-drop bused interconnects. In addition, switches provide for multiple simultaneous conversations among boards--a necessity for highly parallel systems. SCI rings, since they are insertion rings with bypass buffers, also allow multiple simultaneous conversations depending on the configuration of senders and receivers within the ring data flow. Because two party rings degrade into simple full duplex data links (one input and one output to/ from each node), SCI has been able to define interface protocols which are applicable to both rings and switches. With its support for both rings and switches, SCI is applicable for use in both centralized switch based parallel systems such as the BBN Butterfly machine, as well as in distributed switch systems such as the mesh based architecture in the Intel Touchstone. Obviously it can also support hybrids of the two architectures. Figures 3 through 7 illustrate some of the various topologies which SCI supports.

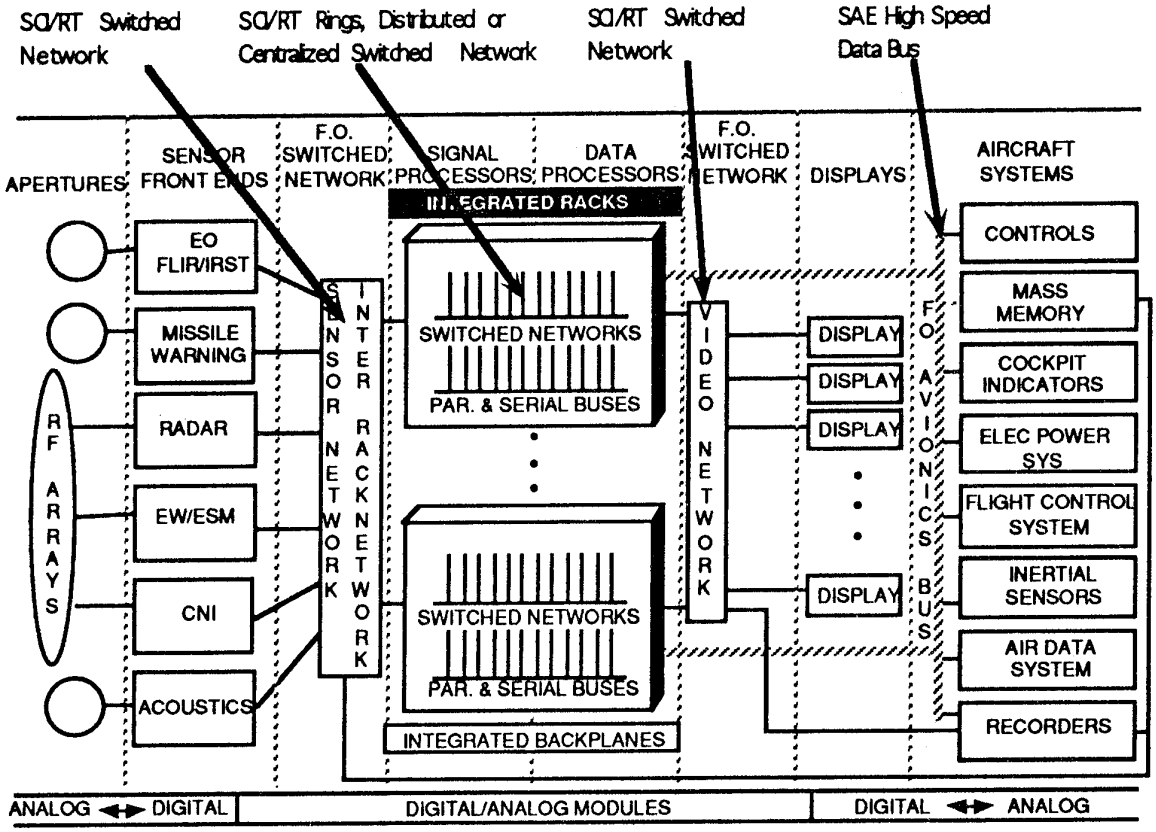


Figure 2. Proposed Avionics Architecture Using SCI/RT As A Unified Network

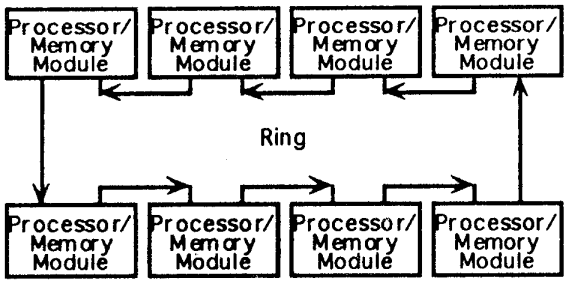


Figure 3.
Basic Ring

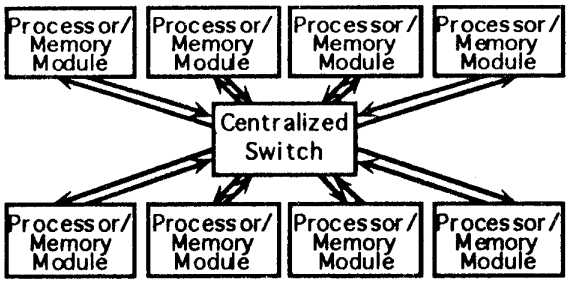


Figure 4
Central Switch--Two Party Rings

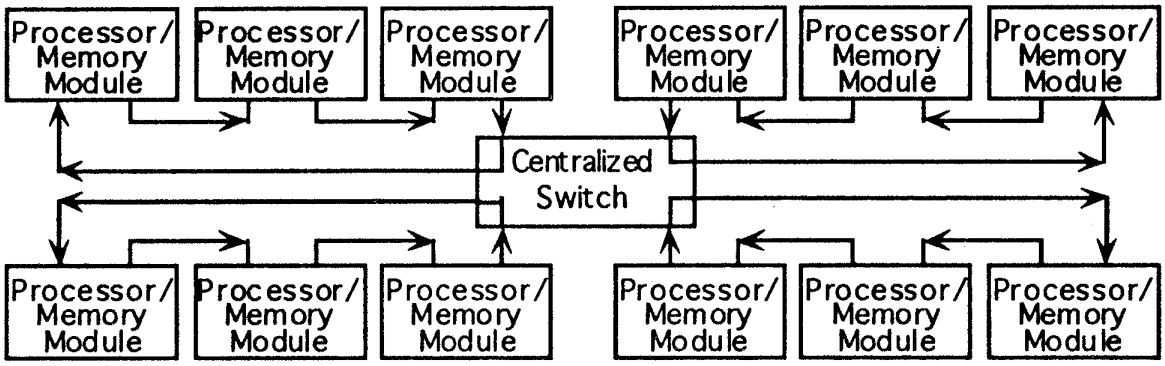


Figure 5
Rings Interconnected by a Switch

As its name implies SCI is designed for use in tightly coupled cache coherent shared memory systems, although it can also support message passing and block transfers. It uses a directory based cache coherency protocol, because of the inherent scalability of that scheme. It conforms to the IEEE 1212 Control and Status Register (CSR) standard and supports the shared memory locks specified therein.

Two physical variants of SCI are presently defined: (1) A 16 bit wide (plus a clock line and a flag line) parallel version running at 8 Gbps on each point to point link; and (2) A serial version, which may be either electrical or fiber optical, running at 1 Gbps. Because the SCI protocol requires no reverse direction handshakes between boards, links can extend for long distances. Electrical links can extend to about 30 meters and fiber optic links to several kilometers.

To improve signaling characteristics and control noise, the electrical versions of SCI use differential signaling. This has led to the development of the IEEE P1596.3 Low Voltage Differential Signaling standard, an additional option for SCI, which allows 0.4 volt signal swings, thereby reducing power. Current SCI parallel implementations are single chip solutions, including all driver chips. Serial implementations currently require the addition of serializer and deserializer chips which make that variant a three chip interface. However, it may be possible to combine the serializer chips and semi-conductor houses are investigating this option.

Data is transferred between nodes in SCI using transactions (usually) consisting of request and response subactions. Each subaction consists of sending two packets--send and echo. Transfer of data can occur during request-send, response-send or both. The SCI subactions are shown in Figure 8. SCI uses small packets to transfer data. Send packets are less than 300 bytes and echo packets are only 4 bytes long. This allows SCI to use small buffers and queues. It also allows higher priority packets to be quickly transmitted without waiting for a long packet to finish. The echo packet provides a ringlet local acknowledgment that a send packet was received at the agent or destination node allowing the ringlet local send queue entry to be cleared.

However, the echo does not indicate whether the data received was good or bad. This information is sent to the source node in the response-send packet. SCI also allows Move transactions, which consist only of a request subaction, and Event transactions, which have neither an echo nor a response.

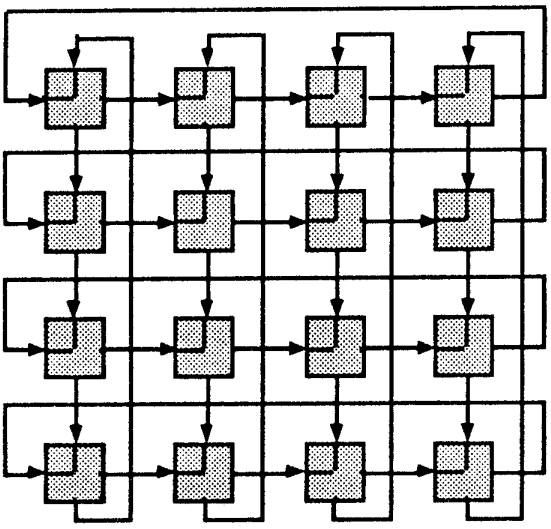


Figure 6
Distributed Switch, Toroidal Mesh Fault Tolerant

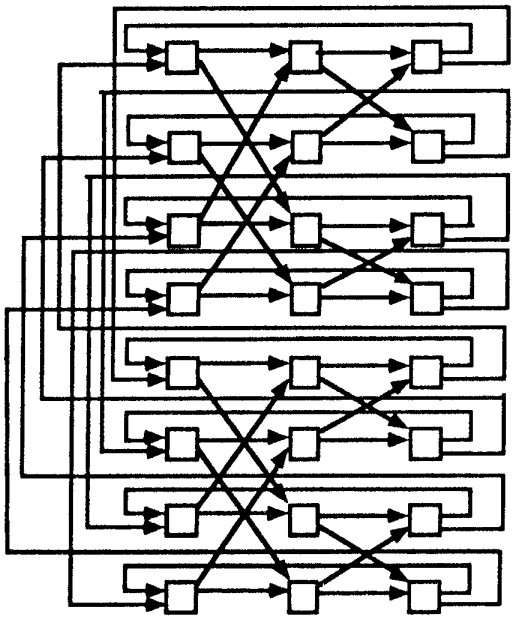


Figure 7
Distributed Switch, Wrapped Butterfly--Fault Tolerant

Priority enforcement in SCI is done through comparison of priority information for the node's next waiting packet and the node's estimate of the ring priority. The node's estimate of ring priority is gathered from the last send/echo transaction to traverse the ring and distributed to all ringlet nodes in idle symbols. In addition, a blocked node can temporarily shut down other nodes access to the ring in order that it can gain access. Unfortunately, SCI supports only four priority levels.

A small portion of the ringlet bandwidth is reserved for low priority packet "fairness" so that no node is indefinitely prevented from accessing the ring. This is done by use of "high-type" and "low-type" idle symbols. When idle symbols are created by stripping packets from the ring, a small percentage of "low type" idles are always created. Since packets must always be appended to an idle, and since only low priority packets can be appended to a low-type idles and a few low-type symbols are always present, some bandwidth is always reserved for low priority fairness.

One node on each ring is designated the scrubber node, which provides housekeeping tasks, such as deleting damaged packets, monitoring ringlet activity, returning nodeID addressing errors, and maintaining certain flow control parameters and timeout counters.

Baseline SCI has a number of features that make implementing a fault tolerant system easier including: (1) The use of differential signaling in the electrical variant provides for good noise immunity; (2) The subdivision of the network into multiple ringlets provides a compartmentalized fault containment region (FCR) which allows for good fault isolation and distributed fault recovery capabilities; (3) Good fault traceability and hardware support mechanisms for fault handling are inherently provided in the scrubber maintenance, trace bit, stomped packets, status codes, time-outs and the CSRs; (4) The echo and response time-outs are also useful fault detection mechanisms but the base standard needs to be augmented with an end to end "duplicate suppression" mechanism so that faulty packets can be resent without side effects; (5) The Command and Status Registers (CSR) are useful in isolating errors within the system; (6) The use of a distributed recovery list in the cache coherency protocol provides for resiliency to any single effect; and (7) SCI uses a 16 bit polynomial for a CRC level error check which provides for all single and double bit errors (regardless of data block length), all errors on an odd number of bits, all burst errors under 16 bits and if the burst error is over 17 bits the probability that an error will be undetected is $1/(16)^{16}$

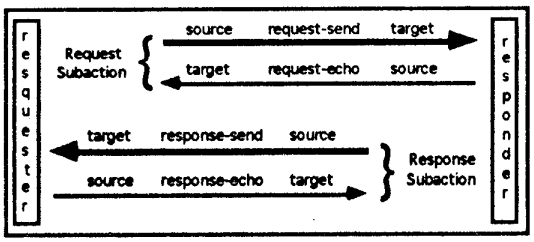


Figure 8. SCI Subaction

6.0 Description of SCI/RT and Other Proposed Enhancements

While the baseline SCI is an established IEEE standard, further development is still taking place on additions and variants. Additional parallel link widths are under consideration such as a narrower 8 bit wide version and a wider 32 bit wide version. Higher speed serial versions are being investigated with a target of 8 Gbps. Also, a tree structured directory based cache coherence protocol is being developed.

Additionally, an IEEE working group has been formed to enhance the SCI standard to make it more applicable to real time and fault tolerant applications such as are found in military and specialized commercial applications. The SCI/RT Working Group was started jointly by the Canadian Navy and the U. S. Navy Next Generation Computer Resources (NGCR) program. An initial draft of the SCI/RT standard was proposed by Edgewater Computer and the Canadian Navy and is available from the IEEE. The proposed enhancements are in the areas of improved determinism to better support real time scheduling, improved throughput and lower latency in real time applications, additional pinout and board specifications for military and other applications, and improved fault tolerance for use in mission critical applications. Security is also an area of concern for SCI/RT.

To improve determinism the SCI/RT proposal would increase the number of priority levels, replace input and output FIFOs with priority driven preemptive queues, and replace the single packet bypass FIFO with a multi-packet preemptive bypass queue. The increased number of priority levels allows use of Rate Monotonic Scheduling theory to schedule the interconnect. Priority driven preemptive input and output queues allows higher priority data to proceed through the interconnect ahead of lower priority data. And a priority driven, multi-packet preemptive bypass queue allows higher priority packets to begin transmission rather than be blocked by lower priority packets from upstream neighbors on a ring.

SCI/RT proposed enhancements to improve performance include better flow control, a method of immediately passing packets through a node without waiting for address checking, and a method of virtual circuit switching to support streaming data. The improved flow control will control ring access on a node group basis rather than for the ring as a whole. Immediately passing packets through a node without waiting for address checking will lower the latency from the current range of 25 to 100 nanoseconds to a one cycle delay (2 nsec. in a parallel implementation, and 1 bit or 1 nsec. in a serial implementation). Virtual circuit switching will support sensor and video networks.

Although baseline SCI provides many features for implementing fault tolerance, additional fault tolerance tools are needed to meet the requirement that no single failure can take down an entire box. A number of proposals are before the SCI/RT Working Group including: (1) a 32-bit CRC polynomial to provide additional error detection; (2) ringlet local fault retry; (3) end-to-end fault retry that provides for the duplicate suppression of transactions that if retried may have harmful effects; (4) skip-a-node and dual node topologies that will be specified as fault tolerant node configurations.

The basic ring configuration of SCI and SCI/RT allows for a number of flexible topologies and alternative approaches to fault tolerant architectures. The NGCR program is supporting three SCI topologies, the basic single node, the dual node, and the skip-a-node topologies. These node configurations are shown in Figures 9, 10, 11 respectively. It is expected that the dual node configuration, which supports mesh, butterfly, redundant centralized switch, and distributed switch topologies, all in a fault tolerant manner, would be used in tactical aircraft.

7.0 Other SCI-Related Work

Other SCI-related work includes the previously discussed Low Voltage Differential Signaling (LVDS), RamLink, and an SCI-like chip to chip interconnect. RamLink, IEEE P1596.4, is a simplification of the SCI protocol for a high bandwidth interface to exchange data between a single master (the memory controller) and one or more DRAMs. The chip-to-chip interconnect is an effort to provide a simple on-chip network for connecting multiple processors. Like RamLink, it is a simplification of the SCI protocol, but in

this case it connects multiple masters instead of a single master with one or more slaves.

8.0 How SCI and SCI/RT Satisfy the Needs of A Unified Network

SCI and/or SCI/RT can be used as described below to replace the unique interconnects that are now used in avionics systems.

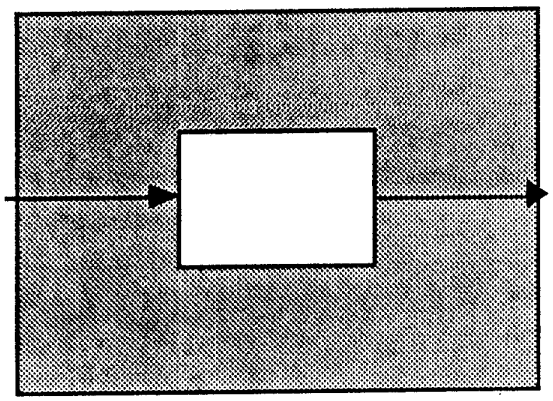


Figure 9
Basic Single Node Topology

The command and control bus in an avionics systems needs to guarantee arrival of real-time command and control messages. This can be

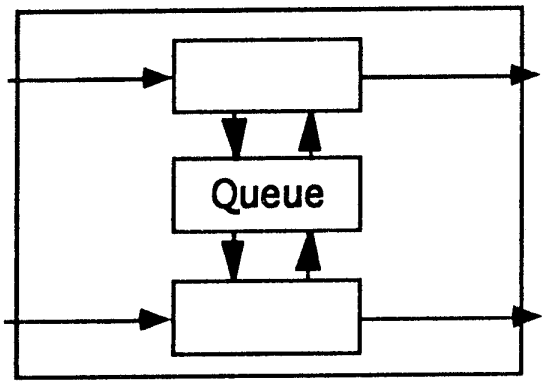


Figure 10
Dual Node Topology

accomplished using a lightly loaded SCI or a schedulable SCI/RT interconnect.

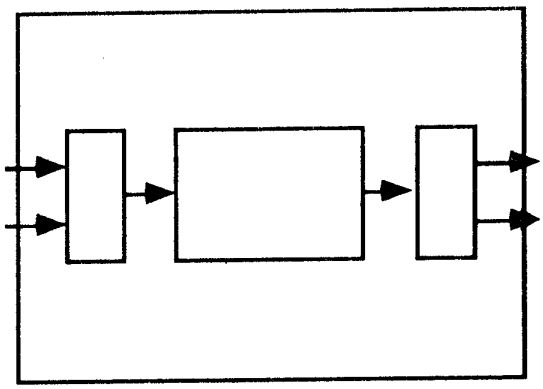


Figure 11
Skip-A-Node Board Configuration

The test and maintenance bus is used to test and troubleshoot modules throughout the system. It needs to provide an alternate access to the module to resolve the ambiguity of whether the module or the interconnect failed when a module does not respond to a query. The extra interconnect on a dual node system could function as a test and maintenance interface.

The data flow network connects processors in a high performance, cache coherent, shared memory or message passing parallel processor architecture. SCI or SCI/RT can be used in this application using moderate performance rings or high performance switches - either centralized or distributed switches.

The high speed data bus has lower performance requirements than the data flow network, and the cost of a single interconnect needs to be low enough to be cost effective in this application. In some cases, the HSDB functions could be mixed with other inter-box SCI interconnects.

The sensor/video network requires sending large amounts of data simultaneously between many pairs of nodes. An SCI-based centralized switch or virtual circuit router could accomplish this task.

Lastly, box-to-box interconnects requires a high performance, distance insensitive interconnect that can be accomplished using SCI or SCI/RT rings or switches.

The flexibility of SCI can provide a seamless interconnection from backplane to LAN, from electrical to optical and from serial to parallel.

9.0 Packaging Ramifications of the Unified Network

Ramifications of using a SCI-based unified network include impacts on pin counts, type of

cables, power/weight/volume cost of the backplane, and board real estate.

A comparison of pin count and performance between an unified avionics network and a current avionics network shows that the unified avionics network gives much greater performance per pin than is currently available. The pin count of a current avionics system using PI-bus, Data Flow Network and dual TM buses is about 145 pins. The throughput of this system is about 1 Gbps. Using a parallel implementation of dual SCI interconnects provides a total of 16 Gbps throughput with approximately the same amount of pins (taking into account the interconnects and power and ground pins). A serial implementation of a dual SCI network has 2 Gbps--twice the throughput as the current system while using only 44 pins (all but four are power and ground).

Fewer interconnect pins allow for more I/O pins, which allows for more flexibility in plugging in modules since fewer unique slots will be needed. It is expected that connectors will still require all the pins that they can hold, since there never seems to be enough pins for I/O. Since SCI is flexible enough to provide parallel or serial implementations, the best implementation can be selected for a particular application without affecting the logical layer of the protocol.

SCI can use either electrical cable or fiber optic cable to connect nodes. Again the choice can be tailored to the application without affecting the logical layer. SCI uses differential pairs in the electrical implementation to eliminate ground bounce noise. Coaxial cable seems to be necessary for Gbit/sec and higher links, although Autobahn has been able to tune differential stripline to run at 1.8 Gbps. In tests at the Naval Air Warfare Center/ Aircraft Division - Warminster, 5 Gbits/sec appears to be the limit for coaxial cable going two to three feet, as may be the worst case in a large integrated rack application. Beyond that speed and distance, fiber should be used. Therefore, it may make sense to go electrical within a row of cards, but use fibers between rows in the same box. Although coaxial contacts take more space, a single coax can replace the 18 contacts necessary for a parallel implementation. In the future, it may be practical to use parallel optics if small multiple fiber contacts can be developed and produced in a cost effective manner.

The power, weight and volume of the backplane will be affected by using SCI. The backplane will be simpler and lighter since the need for multiple power and ground planes is lessened. And the SCI Working Group has completed work on a low power version (LVDS) of SCI as previously described. In addition, if using the serial implementation of SCI, the number of unique backplane slots may decline since more of the backplane can be used for I/O. Also, by using a unified network there is no need for bridges between diverse interconnect systems.

10.0 Conclusion

The performance, flexibility, and scalability of SCI allows it to be used in a number of avionics applications, such as module-to-module interconnects, box-to-box interconnects, and sensor/video interconnects to form a unified avionics network. This would replace the current situation of having different interconnects for each network. A unified avionics network will allow commonality within an aircraft and among aircraft and will improve maintainability and reduce spare parts costs. A unified avionics network will reduce the number of unique interconnects which will save cost, lower weight, improve performance, and provide a path to parallel processing.

11.0 References

1. IEEE Std. 1596-1992 IEEE Standard Scalable Coherent Interface

2. IEEE P1596.2 IEEE Standard for Cache Optimization for Large Numbers of Processors using the Scalable Coherent Interface (SCI), Draft 0.35, March 22, 1994

3. IEEE P1596.3 IEEE Standard for Low Voltage Differential Signals for SCI, Draft 1.00, December 30, 1993

4. IEEE P1596.4 IEEE Standard for High-Bandwidth Memory Interface Based on SCI Signaling Technology, Draft 1.00, December 13, 1994

5. IEEE P1596.6 Scalable Coherent Interface for Real-Time Applications, Draft 0.12, October 2, 1992

6. IEEE Std. 1212-1991 IEEE Standard Control and Status Register (CSR) Architecture for Microcomputer Buses

DISCUSSION

Question: In which way is the SCI bus controlled - central or distributed?

Answer: SCI is 98% distributed control. However, there is one node on each ringlet that acts as a scrubber. While all nodes have scrubber capability, only one node is selected at intialization to perform the scrubber function. The scrubber maintins certain counters and "scrubs" the ring of broken and mis-addressed packets.

Question: What kind of failure recognition is applicable for this bus?

Answer: CRCs are used to detecgt errors in SCI packets. In addition, packets (which support error recovery) all have a response. If a response is not received, a timeout occurs, and the transaction originator takes corrective action. This corrective action may include retransmission of the original request packet. To protect against a failed node, redundant SCI interconnects can be used. In addition, some partially redundant solutions are possible. These include a "skip-a-node" design in which any node can be skipped over. Redundant lines are possible for the parallel version of SCI. Shunts around a failed SCI protocol chip have also been proposed.

Question: Existing and future modular avionics systems can be "missionized" by adding or removing cards to augment the avionics system for a particular need. This fact, plus the need for spare card slots, favors switched networks over rings. Please comment.

Answer: You are correct. One of the advantages of centralized switch systems is that any number of modules can be removed without affecting the remaining modules. This can be useful for reconfiguring the system. The downside of centralized switches is that they are expensive, consume more power, and [occupy] more board real estate than rings. Switches or rings should be used as the situation dictates.

Question: Interchangeability of modules over a long period of time (backwards compatibility of new technology modules) is important to keep life cycle costs down. The data communications method is a major driver for the module-to-backplane interface definition. How long will SCI interfaces (optical and electrical) remain stable (i.e., can SCI provide a technology transparent interface)?

Answer: It is impossible to predict what new technology may be developed. So a new interconnect design which is better could come about in the next 10 years or so. However, SCI is the product of an IEEE group with forward looking thinkers from a number of commercial and military computer vendors. These people feel that SCI is technologically far ahead of anything else. They see nothing better in the future. Therefore, SCI should have a long lifetime.

Question: How many ports (optical/electrical) could be accommodated in a SEM-E module using year 2000 technology?

Answer: The limiting factor on the number of SCI ports which can be put on a SEM-E module is the number of pins on the module. If a serial interconnect is used, 2 pins are needed for each link, assuming coax cable. It is probably reasonable to put 32 coax contacts on a SEM-E module, so that an 16 port module is possible.

A TECHNIQUE FOR INCREASING THE BANDWIDTH OF HIGH PERFORMANCE ELECTRICAL BACKPLANES

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1. SUMMARY

This paper presents an active matching technique for extending the data rates of electrical backplane interconnects into the gigabit per second (Gb/s) range. In the active matching technique an active bandpass amplifier is used to drive the backplane transmission lines. The gain characteristic of the amplifier is designed to be complementary to that of the transmission line and connectors using standard microwave matching techniques. This technique is suitable for use with conventional stripline and microstrip backplanes as well as newer microcoaxial cables. Using this technique, backplanes operating at serial data rates in excess of 4 Gb/s have been demonstrated and speeds of 10 Gb/s may be possible. These results suggest that electrical backplanes may be competitive with optical backplanes in speed and superior to them in cost, power consumption, and complexity.

2. INTRODUCTION

Currently available electrical backplanes represent a pinout bottleneck for high performance processors due to their bandwidth limiting transmission line and connector effects. Buses such as PI-Bus or Futurebus+ are limited by these effects to clock rates of 50 MHz or less, necessitating a large number of parallel lines to achieve the required data rates. In switched networks such as the F-22 Data Flow Network the large number of parallel lines requires large, cumbersome parallel switching elements to obtain full connectivity. Recently, standards such as the IEEE Standard for Scalable Coherent Interface (SCI) (IEEE 1596-1992[1]) have sought to overcome these limitations by using topologies based on point-to-point links and low-voltage differential signals. Backplanes based on SCI have been developed with data rates of 8 Gb/s using 18 parallel differential lines (16 data plus clock and flag) operating at a clock rate of 250 MHz clocked on both edges. While this is a significant achievement the problem remains of switching parallel lines in a switched network.

These considerations have driven network designers toward high speed serial interconnects and, in particular, toward optical backplane interconnects. In this paper we describe a low-power active matching technique which allows conventional electrical stripline, microstrip, and microcoaxial cable to be driven at data rates of several Gb/s.

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In section 3 we describe the active matching technique, in section 4 we present measurements of the performance of several types of conventional electrical backplanes and, in section 5, show the degree of improvement which can be obtained using active matching. Finally, in section 6 we discuss the ultimate limitations of electrical backplanes and compare them with those of comparable optical backplanes.

3. THE ACTIVE MATCHING TECHNIQUE

The active matching technique was originally developed as a means to extend the bandwidth of light emitting diodes into the GHz range[2], but it may be readily applied to any device having a low-pass characteristic, such as an ordinary transmission line.

In this technique, the S-parameters of the device to be driven, in this case a transmission line plus connectors, are measured and used to derive an equivalent circuit model. An active bandpass amplifier with a positive gain slope complementary to that of the transmission line roll-off is then designed. The combination of amplifier and transmission line is then modeled as a single microwave two-port and the amplifier component values adjusted to optimize the predicted bandwidth, gain flatness, and group delay. The active matching technique is shown conceptually in Figure 1.

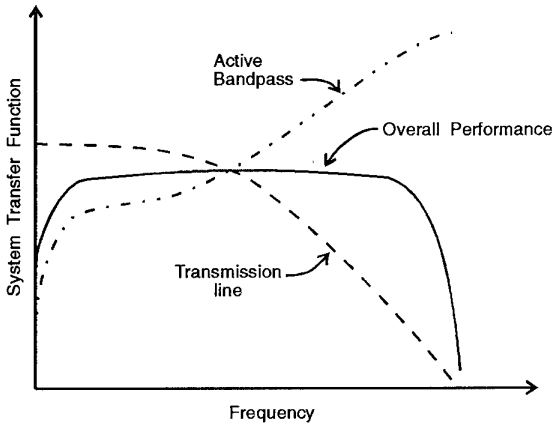


Figure 1. Conceptual diagram of the active matching technique.

4. ELECTRICAL BACKPLANE PERFORMANCE

The performance of two electrical backplane configurations was measured using a Hewlett-Packard 8720C network analyzer. Measurements were made of the magnitude, phase, and group delay for the S-parameters, S_{11} and S_{21}. In addition, for the case of striplines, crosstalk between nearby traces was measured using a Tektronix CSA 803 digitizing oscilloscope with SD-24 TDR/Sampling Head.

The first backplane measured was an AMP Stripline-100 Evaluation and Test Board/Interconnect with an SL100 edgecard connector, shown in Figure 2 (a). SMA connectors were mounted at the far ends of the motherboard and daughterboard in order to inject and extract test signals. The Stripline-100 is an SCI-compatible backplane with two signal planes separated by ground planes in the motherboard and four signal planes separated by ground planes in the daughterboard. The distribution of signal and ground planes in the motherboard and daughterboard are shown in Figure 2 (b).

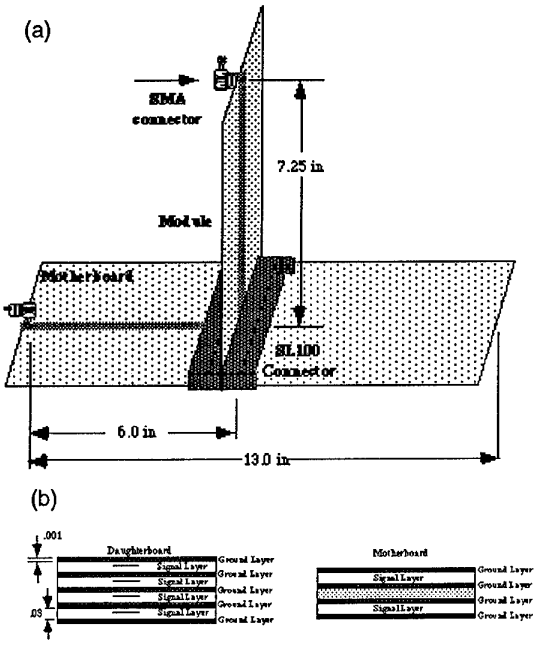


Figure 2. AMP Stripline-100 Test and Evaluation board configuration (a) and distribution of electrical planes (b).

The backplane's S-parameters and crosstalk were measured as described. Figure 3 shows S_{21} over the frequency range 50 MHz to 3 GHz. The marker at 1.26 GHz indicates the -3dB bandwidth. Group delay was about 2.7 ns with a variation of less than $\pm$ 500 ps over the -3dB bandwidth. Measured crosstalk between adjacent channels was less than -17 dB.

The second backplane measured used an AMP 533189-3 edgecard connector connected through the backplane by a one foot length of 8-mil (O.D.) microcoaxial cable available from Micro-Coax (division of UTI Corporation). This connector is a high frequency coaxial push-on connector specially designed for edgecard applications. The microcoax cable is designed for high frequency PCB interconnects and can be readily routed and attached using automated wire bonding techniques. It was selected because of its similarity to unjacketed fiber optic cable in size, weight, minimum bend radius, and susceptibility to EMI and RFI. Again, SMA connectors were attached to the mother and daughterboards in order to injects signals from the network analyzer. Figure 4 shows the magnitude and group delay (upper and lower curves respectively) for S_{21} for this backplane. The -3dB bandwidth of this backplane extends to about 1 GHz. Above this point a resonance appears which is again associated with connector capacitance. Below the resonance the group delay is about 1 ns $\pm$ 250 ps. Although not measured, we expect crosstalk between adjacent cables as well as susceptibility to EMI/RFI to be essentially nonexistent.

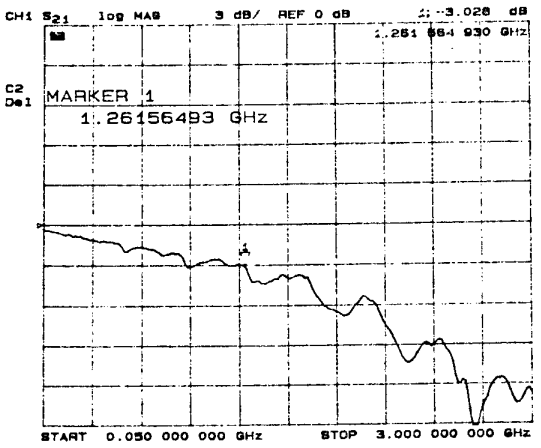


Figure 3. S_{21} for the AMP Stripline 100.

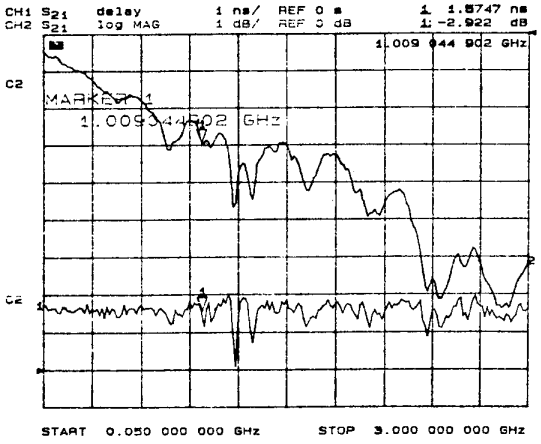


Figure 4. S_{21} magnitude and group delay for the microcoax backplane.

5. ACTIVE MATCHING BACKPLANE DRIVER

To evaluate the degree of improvement in performance which could be obtained by using the active matching technique, the 8-mil coaxial cable backplane was selected for a test design due to its similarity to fiber optic cable. In order to isolate the effects of the cable from those of connectors, a two-foot section

of cable was connected at either end to microwave SMA connectors mounted on 31-mil FR-4. The S-parameters of this transmission line were then measured and used to design the active bandpass amplifier.

A schematic diagram of the active bandpass amplifier is shown in Figure 5. The driver consists of a pre-emphasis network and a flat wide band response amplifier. A wide band MMIC amplifier (NEC UPG100) was chosen as the gain element. The MMIC is indicated by the dashed outline in Figure 5.

Figure 6 shows the measured bandwidth of the cable assembly itself (broken line) and with the actively matched driver (solid line). The measured response of the combined circuit was in good agreement with the predicted response. The -3dB bandwidth of the cable itself is about 500 MHz. Using the driver extends the bandwidth to about 2.1 GHz. Total power consumption of the amplifier is about 300 mW. It should be noted that the design was not optimized for low power consumption, so significant improvement may be expected with a refined design.

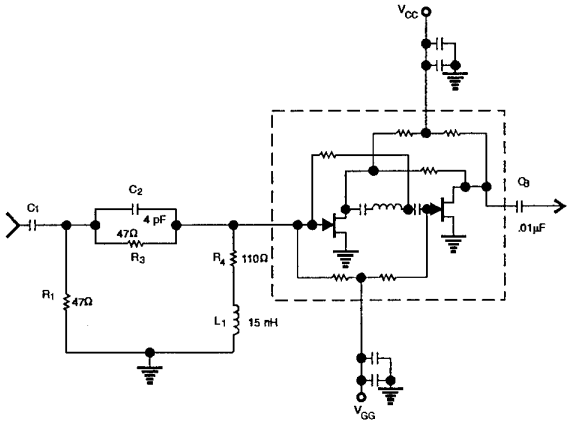


Figure 5. Schematic diagram of the active matching backplane driver.

6. CONCLUSIONS

In this paper we have presented measurements of the performance of two high performance electrical backplanes. Both backplanes exhibited bandwidths in excess of 1 GHz, corresponding to digital data rates in excess of 2 Gb/s. We also presented an active matching technique for extending the serial data rates of such backplanes into the range of 4 - 5 Gb/s. Currently the principal limitation to the performance of electrical backplanes is related to the connector. With improved high frequency electrical edgecard connectors, the results presented here suggest that electrical backplanes operating at serial data rates in the range of 5 to 10 Gb/s may be possible.

In view of these results the claimed speed advantage of optical backplanes may not be warranted. This is particularly true when the question of usable bandwidth is considered. In an avionics application the size and speed of the switch module is limited by the speed and power consumption of the electrical protocol and switching circuits. Currently available SCI protocol chips operate at 4 Gb/s and dissipate 20 W. To this must be added the power required by the serializer/deserializer circuits (2 W for the HP G-Link chipset at 1.25 Gbaud), and, for an optical backplane, the power consumption of the relatively inefficient optical transmitters and receivers (typically about 1 - 2 W at 1 Gbaud). Thus a 16 x 16 switch would dissipate about 368 W plus the power required for the switching element itself. Lower power protocol chips are currently under development which are intended for operation at 8 Gb/s, but increasing the speed of these chips as well as the serializer/deserializers to the point where they may take advantage of the speed of optics will result in a prohibitive increase in power consumption. Until low-power components can be developed which operate at speeds in excess of 8 Gb/s, the speed advantage of optical backplanes cannot be utilized, and their increased cost and complexity may not be justified.

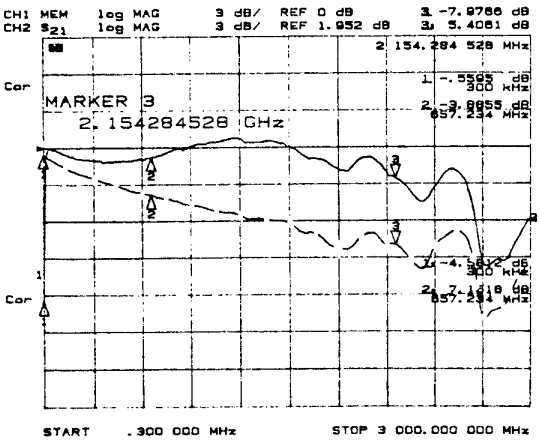


Figure 6. Measured bandwidth of the cable assembly (broken line) and combined driver/cable (solid line).

ACKNOWLEDGMENTS

The authors wish to express their thanks to Mr. Charles Caposell of the Naval Air Systems Command for his continued support throughout this effort, to Ms. Deborah Dolan of Micro-Coax for providing the coaxial cable and Mr. James Schroeder of AMP, Inc. for the Stripline-100 Test and Evaluation kit used in these measurements.

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2. Gershman, V., Daryoush, A.S., Lin, J.Y., and Rosen, W.A., "1.25 Gb/s Wideband LED Driver Design Using Active Matching Techniques", in *Proc. SPIE*, **1474**, 75, 1991.

DISCUSSION

Question: Have EMI/crosstalk effects been investigated?

Answer: Crosstalk was measured for both the stripline-100 and the 8 mil coax. For the stripline-100, it was about -17 dB for adjacent channels run single-ended. We expect it to be much lower when run in differential mode. Crosstalk was virtually nonexistent for the coaxial cable. EMI effects were not measured, but we anticipate it would be quite low for the coaxial cable. For the stripline-100, we expect it to be quite low when operated differentially. It could be further lowered by adding metallization in the ground plane without significant weight increase.

Optical Backplane for Modular Avionics

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1. SUMMARY

An experimental study was carried out by DASA and Daimler Benz Research, to demonstrate the feasibility of fiber optic technology for use in Modular Avionics. In the first step of the study an inter module communication up to 16 subscribers, with interconnection length of about 1m was demonstrated. Backplanes being composed of multimode and monomode fibers were tested in a configuration of 4 parallel data channels, each running with 1 GBit/s.

This paper will resume results of investigations as: Power budget, influence of modal noise with multimode fibers, effects of feedback as well as optical interference caused by reflections. The paper then goes on to describe the transparency for given protocols (e.g. PI-bus). A prospect of problems arising of optical interconnection of a relatively large number of subscribers and possible solutions by using in-line amplifiers (optically) are reviewed. The backplane implementation is prepared to be arranged as a serial/parallel bus or a part of a switched network. Finally this paper will give a synopsis of optical backplane solutions.

2. LIST OF SYMBOLS

a_w	waveguide attenuation
BER	bit error rate
D	network dimension
d	distance between modules
GRIN	gradient index
mcm	micro meter
N	number of modules
P	optical (output) power
PMMA	Polymethylmethacrylat
STANAG	Standardization Agreement (NATO)
z	number of coupler ports

3. INTRODUCTION

Data transmission via optical media in the area of telecommunication is rising steadily. One important factor of optical communication is the very high transmission bandwidth combined with a comparatively small transmission loss of optical fibers.
The use of fiber optic techniques in Modular Avionics opens up a new dimension of inter module communication caused by enhanced efficiency (e.g. data rate).
Reflecting on data processing in core avionics, for example, special focus is on reliability, redundancy and robustness against electromagnetic interference (EMI, EMP and lightning). Looking at the signal and sensor side of modular concepts an extremely high transmission rate is required. The well known principle of transmitting data via buses will be replaced more and more by the method of data/signal propagation in switched networks.

4. REQUIREMENT ANALYSIS OVERVIEW

An optical backplane can be defined as a general purpose communications network that provides interconnection of a variety of data communicating devices e.g. modules, within a small area or subscribers located outside the local rack.
The environment relevant to the optical backplane consists of stations (or terminals) connected to it and the environmental conditions (temperature, shock, vibration, etc.) under which it has to operate. The connected stations, modules, act as sources and sinks of messages. The main function of the optical backplane is to transfer messages between connected stations.
A Modular Avionic configuration is assumed. This avionic configuration should cover typical avionic architectures as presented in an AGARD conference (see Lit.1).
An optical backplane architecture is based on the choice for three items: A network topology, a medium access protocol and a set of components.
Data transmission systems can be characterized by data transfer capacity of network, dimension of network and the maximum number of subscribers, these factors are of importance in regard to data transfer reliability (in terms of signal to noise ratio and transmitter output power). A simple but powerful characterization of copper and fiber optic implementation is given by the performance triangle (see figure 1). If one of the three parameters is increased, the others have to be lowered. The diagram shows a copper backplane bus, for example the draft STANAG 3997 the NATO Standard of the PI-Bus (see Lit 3) and an estimated fiber optic network. The performance parameters of the fiber optic network (for example the network dimension) are more than 10 times, for the clock rate more than 100 times higher as the values of the electrical competitor.

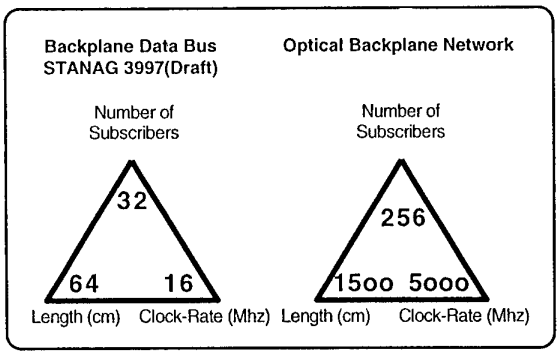


Fig. 1 Performance of Backplane Solutions

Active systems with repeater, as bus- and as star topology demonstrate good performance relating to a large number of subscribers, the switched network topology gives in addition high performance in speed and in multiple access capability.

Passive systems, star- or linear topologies display good performance in reliability and maintainability, problems arise from the attenuation in passive networks, resulting in a small (very small) number of subscribers. The passive optical switched network depicts extremely good performance in speed and real time access. Serious limitations arise from the attenuation which increases very rapidly with larger numbers of subscribers. At present time passive optical switched systems stay at 4 (max. 8) subscribers, fibre optic amplifiers may overcome this limitations.

5. BACKPLANE ARCHITECTURE

The investigation in network architectures will be selected for two technology steps. The two configurations are different with respect to the number of subscribers and the dimension of network. A brief description of these two configurations is given below.

System 1 is characterized by 16 to 32 subscribers, a comparatively small dimension of the network (expansion within one rack), and a passive manner of signal distribution.

System 2 may have capacity up to 256 subscribers, a larger network, distributing data not only within one rack but over a number of racks, optical signals may gained by fiber amplifiers and distributed by optical switches.

Design Parameter of Optical Backplanes

System 1

• Number of subscribers	16 to 32
• Max. link length	1 m
• Transmission rate (per line)	0.5 to 4(8) Gbit/s
• Word size	16/32 Bit
• Parallel Protocols	PI-Bus, Futurebus, ...
• Switched Network Protocol	TBD
• Multimaster/Master-Slave	yes
• Broadcast/Multicast	yes
• BER	10^{-9}

System 2

• Number of subscribers	32 to 256
• Max. link length	15 m
• Transmission rate (per line)	0.5 to 2 Gbit/s
• Word size	16 to 64 Bit
• Parallel Protocols	PI-Bus, Futurebus, ...
• Serial Protocols	Token Protocols e.g. HSDB
• Switched Network Protocol	TBD
• Multimaster/Master-Slave	yes
• Broadcast/Multicast	yes
• BER	10^{-9}

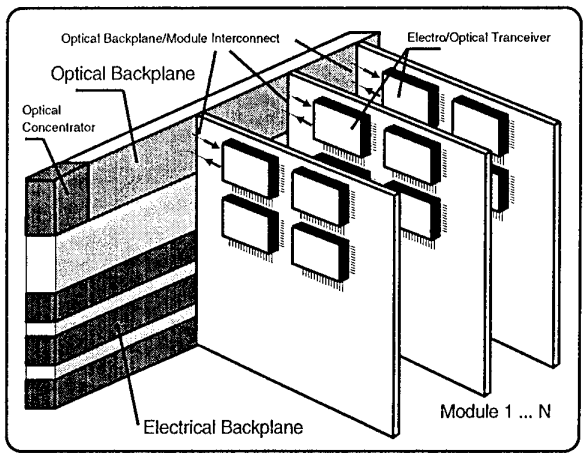


Fig. 2 Optical Backplane

The physical media of the network architecture is based on two main parts: The backplane structure itself with the modules including interconnect to the modules and transceivers and a distribution element e.g. an active or passive coupler or an optical switch matrix (see figure 2).

The media access protocol is not a subject to be investigated in this experimental study. Existing protocols for serial data transmission e.g. token protocol (see Lit. 4) as well as for parallel data transmission e.g. PI-Bus (see Lit. 3), should be supported by the backplane design. All possible protocols should be transmitted transparently. A "transparent" transmission means, that neither the sender nor the receiver have to generate/decode any auxiliary protocol informations.

To support serial protocols only one channel is required, parallel oriented transmission protocols requires two channels as a minimum, one channel for handshake the second channel for transferring commands/data. Optical backplanes may consist of several transmitting and receiving channels. In a first approach we implemented four lines in each direction, using a star topology as shown in figure 3 and figure 4.

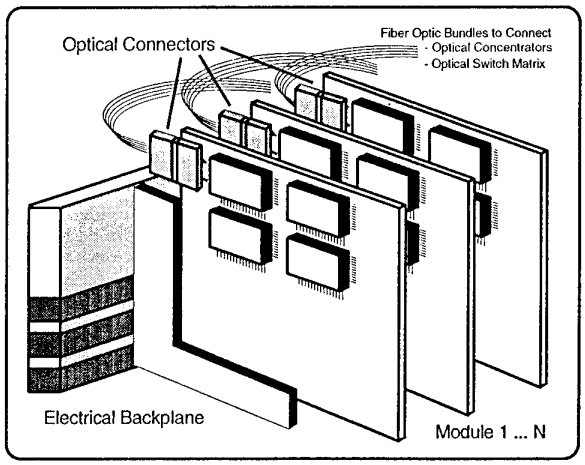


Fig. 3 Fiber Optic Interconnect of Modules

Star Topology

The physical nature of the star topology with respect to the utilization of various protocols is, fully identical to the linear topology, nevertheless it provides a better uniform (optical) power distribution, which results in a suitable starting basis for an optical waveguide implementation. Basically two different topologies are formed by using a reflective star (figure 4) on the one hand and a transmissive star on the other hand (figure 5). One suitable solution for optical backplane implementation is to build the backplane by using transmissive star couplers require two optic waveguides to connect each subscriber, one waveguide feeds the transmitter and the other the receiver. An important parameter in optical backplane design is derived from the loss budget. The lowest loss in the passive network appears, if a transmissive coupler is used, then the signal power at the receiver basically arrives at the output power of one transmitter divided by the number of subscribers plus some harness losses. A much higher loss is observed at the harness built using a reflective star coupler. In this case transmitter and receiver share the input/output ports of the coupler and additional coupling losses of > 6dB arise from the power splitting between the transmitter and the receiver. Figure 6 shows the network loss for reflective and transmissive star coupler topologies.

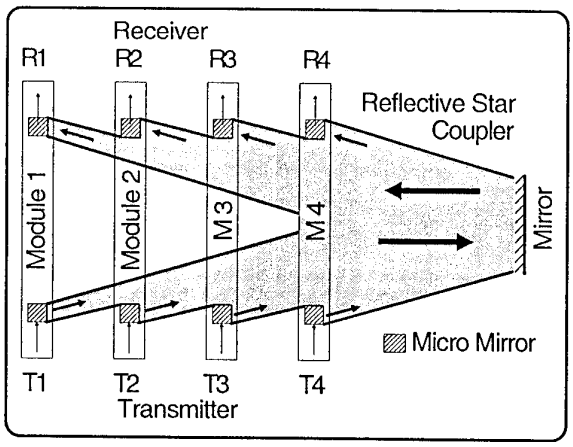


Fig. 4 Reflective Star, Planary Optic Backplane

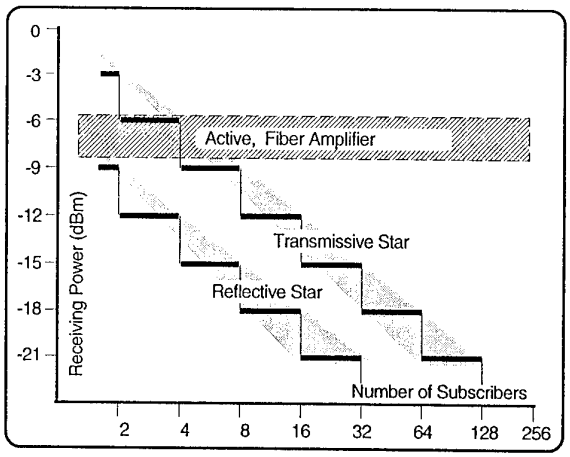


Fig. 6 Optical Power Budget of Various Topologies

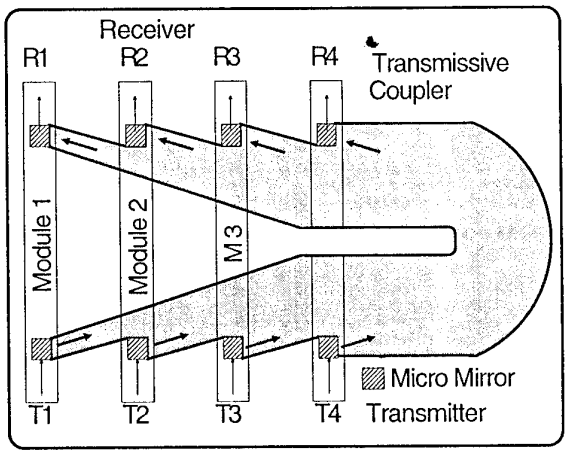


Fig. 5 Transmissive Star, Planary Optic Backplane

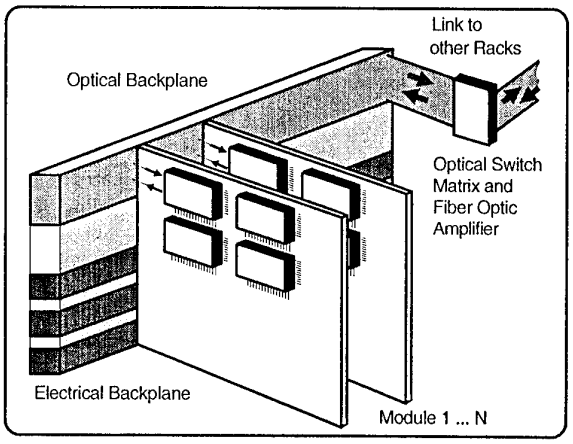


Fig. 7 Backplane with Optical Amplifier

Passive Star, Advantages/Disadvantages

Advantages:
- passive system
- a great variety of protocols
- low signal dynamic at the receiver
- agreeable power budget
- no limitation in wavelength

Disadvantages:
- centralized star coupler
- small number of subscribers
- reduced length of network
- high output power at the transmitter
- high receiver sensitivity
- reduced bandwidth

Star Topology Gained by Optical Amplification

In small local area networks, the power budget will be defined with respect to the loss of the harness and the power level requirements of receivers and transmitters (see table 1).
The power budget is one of the important factors in optical data transmission systems together with data rate and reliability. Active fibre optic systems which are very agreeable in terms of power budget (optical amplifier) and number of subscribers, are at a disadvantage owing to deficiency in safety and reliability required for air- and spacecraft. Optical amplifiers, both the semiconductor and the fibre optic type (see Lit.2), provide a good amplification of optical signals with comparatively low noise. Daimler Benz Research developed an erbium-doped fiber amplifier for a signal wavelength in the 1.5 mcm spectral region. The gain was measured as about 40 dB (small signal), the output power was 15 dBm and the noise figure was found, close to the fundamental quantum-limit, at 3.5 dB.

System Application:
From the safety and reliability point of view the erbium-doped fiber is a passive component such as waveguides, mirrors or couplers. The active part of the optical amplifier is the pump-diode witch provides reliability numbers similar to the laser diodes of the transmitter in the system. For higher reliability requirements a dual redundant diode-pump should be a sufficient solution. The ideas for the application of the fiber amplifier in the system can be as follows: Power amplifiers for boosting of transmitter output signals. Pre-amplifiers provide near quantum-limit detection at a comparatively high bandwidth. Inline-amplifier which pick off small signals and feed it into a distribution network like a central repeater (see figure 7).

Table: 1 Power Budget Calculation

Launched power (in fiber)	-3 dBm
Receiver sensitivity (1Gbit/s;BER 10^{-9})	-20 dBm
System power budget	17 dB
Safety margin	-3 dB
Network loss (allowance)	14 dB
Optical amplifier	>30 dBm
Network loss (allowance)	>44 dB
Coupling loss module/backplane	2 dB
Waveguide loss	$2*N*d*a_w$ dB
Power distribution	10*log z dB
Insertion loss	3 dB
Frenel loss	0.7 dB

Table 1 gives a calculation scheme for power budget calculation without (passive) and with optical amplifier. Based on this calculation scheme, star topology assumed and on laboratory measured parameters the required waveguide attenuation versus the number of subscribers is determined and displayed in the diagram of figure 10.

Optical Amplifiers, Advantages/Disadvantages

Advantages:
- excellent power budget
- large number of subscribers
- a great variety of protocols
- moderate sensitivity at the receiver
- moderate output power at the transmitter
- larger network

Disadvantages:
- amplifier adapted wave-length
- centralized active system
- additional amplifier/control circuits
- redundancy provisions

6. RESULT OF LABORATORY DEMONSTRATIONS

Multimode Approach.
Existing fiber optic components, developed for STANAG 3910 bus system (used in EF 2000) as multimode fibers, reflective star couplers (passive) and connectors has been assembled for investigating multi mode network looms with high speed optical signals. For moderate transmission bit-rate, we looked at the attenuation, the power budget is shown in table 2, and at the signal shape. Effects of modal noise and optical interference caused by reflections, seemed to be present together with the signal. At higher transmission bit-rate up to 1Gbit/s further investigations will look into details in particular into the influence of modal noise.

Table: 2 Power Budget, Reflective Star Multi Mode

Launched power (in fiber)		-3 dBm
Receiver: Tectronix optical head		>-30 dBm
Subscriber		N=3 +monitor
Number of ports		7
power distribution	8.45 dB	
coupler loss (port 4 to port 5)	2.88 dB	
connector loss	4x1.25 dB	
Insertion loss		16.33±.6 dB

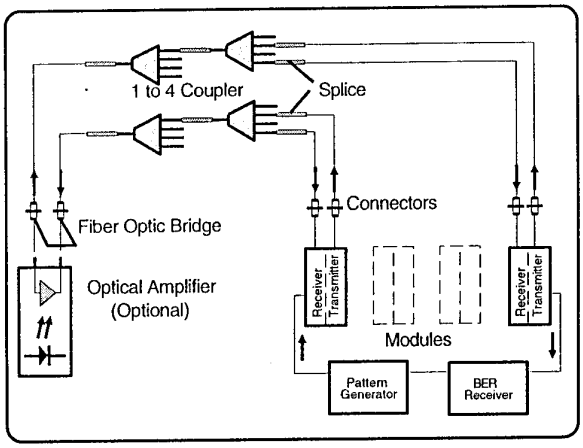


Fig. 8 Mono Mode Network Test

Monomode Approach.
The monomode network consists of cascaded 4-port coupler spliced to a 2x 16-port transmissiv star coupler (passive) with connectorized transmitter and receiver (see figure 8). In this configuration the bit error rate (BER) of a backplane receiver was tested with various bit patterns at 250Mbit/s. The results are depicted in figure 9. The loss budget of the mono mode implementation is given in table 3.

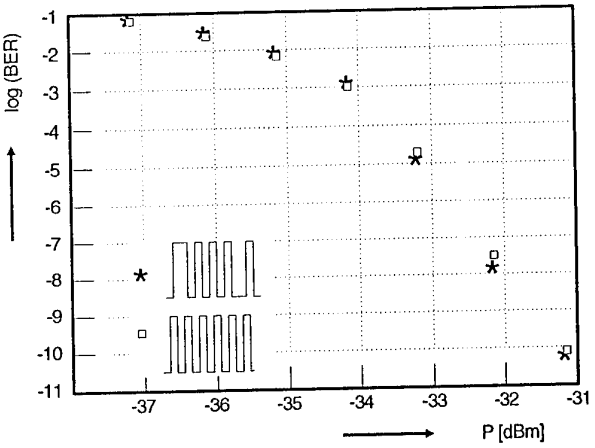


Fig. 9 BER v/s Receiver Power

Table: 3 Power Budget, Transmissive Star Mono Mode

Launched power (in fiber)		-6 dBm
Receiver sensitivity (250 Mbit/s; BER=10^{-9})		-31 dBm
Subscribers		N= 16
Number of ports		32
power distribution	2x 12.0 dB	
coupler loss	4x .3 dB	
splice loss	6x .15 dB	
connector loss	4x .5 dB	
Insertion loss		28.8± .6 dB

Optical Interconnection Technology.
Optical Waveguide
A lot of methods have been proposed to built waveguides for optical backplane. For this experimental study we considered two technologies: Etching of rib waveguides in polymer on glass and ion exchange in glass. As a result of edging induced roughness the loss increased to 1dB/cm in the polymer waveguide, to high for useful backplanes. To built a demonstrator we adopted the ion exchange technique and prepeared some sample of 1 to 4 couplers. The results of investigation are depicted in table 4 , the measured attenuation of about .1dB/cm should to be sufficient for interconnecting of about 10 subscribers (see figure 10).

Table: 4 Measured Power Distribution

Launched power (in fiber)		-2 dBm
Receiver Sensitivity (1Gbit/s;BER 10^{-9})		-20 dBm
	sample 1	sample 2
Port 1	11.7 dB	12.6 dB
Port 2	10.3 dB	11.7 dB
Port 3	11.6 dB	12.4 dB
Port 4	12.4 dB	12.3 dB
Mean value	11.5 dB	12.2 dB

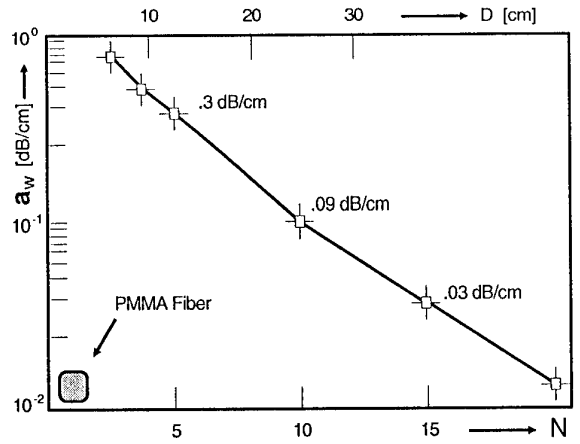


Fig. 10 Waveguide Attenuation v/s Number of Subscribers

Micro Optic Mirror

Micro mirrors offer good prospects for coupling light via waveguides or gradient index lens into backplane integrated waveguides/fibers. A principle arrangement is shown in figure 11. The Daimler Benz Research manufactured a mirror plane by photo ablation using eximer laser. After coating with CrAu layers a mirror loss of about .1dB have been demonstrated.

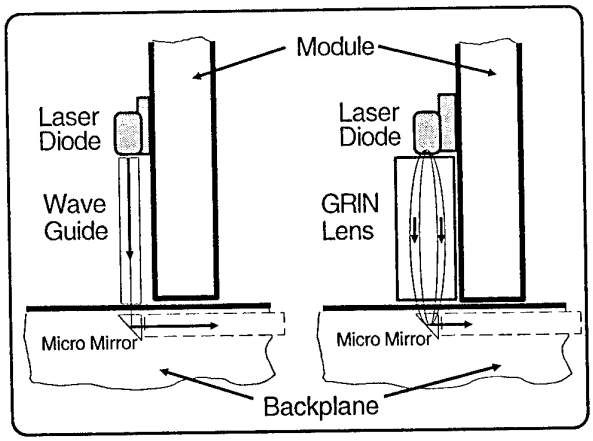


Fig. 11 Coupling Techniques Backplane/Module

Chip Solder Bonding

The interconnect of lasers, photo diodes, fibers and planar waveguides requires, particularly if monomode technology is applied, a precise position of the optical- and electro-optical components. Similar to the electronic chips, optical and electro-optical components are equipped with precise pads. During the soldering process self-alining of components can be observed. The process is represented in figure 12. These technique have been investigated with solder bumps of various diameters and chemical compound. At least good results were found using 80 mcm diameter and PbSn solder bumps. Alignment accuracy of 3 mcm has been measured, starting from a pre-alignment of about $\pm$ 100 mcm.

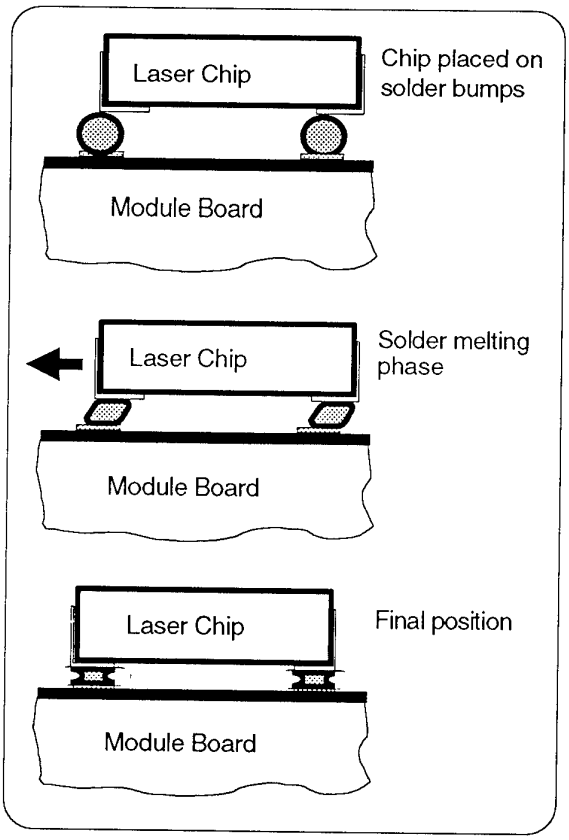


Fig. 12 Flip Chip Solder Bonding

7. CONCLUSION

An overview of optical backplane solution has been provided with reference to system requirements. Fiber optic and planary optic implementations have been discussed. The shown results of laboratory investigations on component as well as on system level may demonstrate that optical backplane technology is reaching the level of maturity that application in the modular avionics is becoming a reality. Further investigation in optical backplane technology will shed light on whether technology mono mode or multi mode, fibre or planary optic will have the best pre-condition for use in avionics.

8. REFERENCES

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[1] John C. Ostgaard, D. Reed Morgan, "The Evolution of Digital Avionics Architectures/Systems" AGARD Lecture Series No. 164, May 89

[2] David N. Payne, "Active Fibre and Optical Amplifiers" AGARD Lecture Series No. 184, May 92

Standardization Documents

[3] Standardization Document: 4710 SAE AS, PI-BUS STANDARD; Draft of: 28 September 1992

[4] Standardization Document: AS4074.1 SAE, Linear Token Passing Multiplex Data Bus; Issued 9-7-88

DISCUSSION

Question: Do you have any ideas how the connector could be [implemented] for monomode fibers (module connector)?

Answer: In this study, we do not look into connector problems in detail, but some solutions from Bell Labs, IBM, etc. have been monitored (commercial products); e.g., multiway connectors from NTT (Japan) are on our shopping list.

High Performance Backplane Components for Modular Avionics

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1 SUMMARY

The design and development of optoelectronic transceiver and optical pathway components for application in a modular avionics backplane demonstrator system are described and initial performance results are presented.

2 INTRODUCTION

The provision of interconnection networks of sufficient capacity within advanced processor computers is recognised as a critical issue in the design and construction of the high performance systems currently being planned and developed within the avionics community. The emergence of high performance processors, with increasing requirements for system bandwidth and interconnectivity, requires new interconnect technologies to exploit fully the potential of multiprocessor systems. Optical interconnections are increasingly recognised as the technology for providing these high performance interconnection networks. They offer:

- data capacity in excess of 10 $GBit.s^{-1}$, extendible further through multiplexing
- insensitivity to electro-magnetic interference
- absence of line capacitance
- negligible mutual coupling or crosstalk
- reduced weight and volume
- low power dissipation
- improved reliability.

The development of optical interconnect technologies and their incorporation into real avionics environments is the subject of considerable current research effort in both the USA and Europe, and is seen as critical for the next generation of high performance modular avionics systems.

This paper describes our investigation of the application of optoelectronic technologies to optical interconnections, with particular emphasis on the provision of avionics compatible optoelectronic interfaces. A major objective of our present programme is to explore and develop ways in which optical backplane architectures can be used to alleviate the dense, and intrinsically unreliable, electrical connections implicit in structures of this type, the ultimate implementation of this approach being seen as based on board-mounted optoelectronic drivers, with associated electronic circuitry, communicating directly over polymer waveguide backplanes via demountable connectors.

3 PROCESSOR SYSTEM ISSUES

Many contemporary electronic processor systems are configured as hierarchical structures, with several levels of interconnection, as shown schematically in Figure 1. A typical system comprises a "global network" as the highest hierarchical level, linking a family of lower-level processor racks. Each processor rack contains processor modules linked by a local interconnect network, the second level of the hierarchy, which may comprise either a conventional backplane or more local direct board-to-board links. A third level of the interconnect hierarchy provides the signal paths between the individual components on the processor module itself. The different levels of the interconnect hierarchy have their own requirements in terms of interconnect distance, degree of parallelism and data rate, requiring different applications of optical interconnect technologies.

For the longer distance requirements of the global link, the advantages of optics over electrical interconnections are clear, and several current high performance systems now employ optical fibre links in this role [1]. These links are frequently time-multiplexed to maximise the use of fibre bandwidth, and at present typically employ general purpose optoelectronic components, although there is a continuing demand for smaller, more efficient units. As data rate requirements become more demanding, extension to larger numbers of optical pathways through the use of ribbon fibre links is anticipated, thereby exploiting the parallelism offered by optics.

At the backplane and on-module levels within the processing system, the application of optical interconnections is expected to allow the realisation of new processor and switching network architectures and to help overcome existing limitations of interconnect within the processor rack, and for these reasons is now being considered seriously. In particular, existing electrical backplanes for high bandwidth applications suffer from length limitations, require high pin counts with small pitch lines, and consequent crosstalk.

The implementation of optical interconnects at this level requires the development of a broad range of enabling technologies:

- efficient optoelectronic interface component arrays, capable of providing serial or parallel optical input and output points from the processors, and consuming little power and space on the module,
- component and pathway alignment and packaging techniques capable of providing the required alignment tolerances
- practical "optical wiring" technology, providing low loss optical pathways of the required length and connectivity throughout the interconnect hierarchy.

These issues will be considered in detail here, using as technology examples a range of components and sub-systems being developed within the GEC Optical Interconnects Programme and the ESPRIT Collaborative Programme "Hierarchical Optical Interconnects for Computer Systems" (HOLICS).

4 OPTOELECTRONIC INTERFACE COMPONENTS

Opto-electronic interface elements provide the optical "bond pads", at which data is transferred between the electrical processor and the optical "wiring". Typical requirements for these interfaces include:

- High data rate, typically 0.5 - 2.5 GBit.s^{-1}
- Low power consumption
- Compatibility with VLSI logic signal levels
- Rugged construction for severe operating environments
- Extended temperature capability, (-25 C to +125 C)
- Low profile packaging, preferably surface mounting for compatibility with standard electronic build practices
- Low cost manufacture

4.1 Transmitter Issues

The choice of optical transmitter is strongly dependent on the particular interconnect required, the principal options being either a directly modulated source, or a local optical modulator illuminated by a remote CW source.

A directly modulated source (LED or laser, depending on the link length and data rate required) is almost certainly best for the longer distance serial data link, such as required for the global interconnect, and for backplane links. The low power modulator solution [2] is more attractive for dense, highly parallel interconnects, for example between a processor and its memory cache, and in situations where the (relatively) high levels of thermal dissipation associated with a large array of source elements cannot be tolerated. A major uncertainty relating to the use of modulator elements for the transmitting function relates to their relatively limited operating temperature range and uncertainties in their long term stability. Whilst adequate in applications for which a limited temperature range is acceptable or in which active temperature control is employed, the more demanding avionics applications require alternative solutions, such as directly modulated LEDs or laser diodes with emphasis on high operating temperature. Other factors to be considered include cost, compatibility with VLSI hybridisation, wavelength of operation, reliability and bandwidth, as summarised in Table 1.

Overall, laser diode sources are the preferred choice for backplane and global links, since they offer high launch power (essential for multi-node distribution in non-repeatered buses) and the required high data rate capability. In terms of cost, the laser based transceiver will be more expensive than LEDs, but through multiplexing, the higher bandwidth capability may permit a reduction in the number of optoelectronic transceivers deployed.

4.2 Receiver Issues

Receivers are generally based on *pin* photodiode detectors [3], with additional signal handling requirements determined largely by the protocol intended for use. For example, the use of a shared optical pathway fabric such as a ring or star requires the adoption of burst mode data transmission, with the consequent need for the receiver to acquire clock and signal rapidly during message preamble, and for high sensitivity and wide dynamic range. By contrast, the use of point to point links allows more conventional clock recovery techniques to be adopted, and lower levels of sensitivity and dynamic range.

4.3 Packaging Issues

Much current work on optoelectronic interface elements is focussing on the packaging of the transmit and receive components rather than on the actual active device technologies, which are now generally well established. Recent developments in micro-etched silicon packaging techniques have resulted in new opportunities for the production of very small, surface-mount compatible optoelectronic interface units with much smaller footprints than currently achievable with conventional optoelectronic packaging techniques. However, MCM packaging using ceramic and etched-silicon motherboards has reached a high level of maturity, making it desirable that the mechanical and optoelectronic interfacing techniques adopted are compatible with accepted standard packaging practices, so as to allow earliest adoption. Such etched silicon assemblies will incorporate structures for the hybrid mounting of laser and detector elements, interfacing to the appropriate optical pathway or connector, and the provision of associated control and interface ICs.

Table 1 Comparison of Transmitter Options

	Modulator	Laser	LED
Data Rate	multi-GHz	multi-GHz	few 100 MHz
Array Capability	Yes	Yes	Yes
Power Requirement	Low	Medium	High
Reliability	High	Medium	Medium
Temperature Range	Low	Medium	High

5 TRANSCEIVER REQUIREMENTS

In order to establish the design of an optoelectronic transceiver element, it is necessary to consider a number of relevant system-derived issues. In the present case, a requirement exists for inter-processor communications over a serial data bus operating at around 600 MBit.s^{-1}. The selected configuration uses a token-passing protocol to manage transmissions over a passive optical waveguide pathway, implemented as a polymer waveguide transmissive star, resulting in the development of a compact, low-dissipation transceiver compatible with a number of anticipated systems requirements.

The use of a star interconnection fabric puts specific demands on the optical transceiver. In particular, relatively high launch powers and receiver sensitivities are required to accommodate the inherent losses associated with splitting the optical signal between all module stations in the rack. Additionally, the variations in optical path lengths between different parts of the rack result in significant variations in optical path losses, and the receiver must be able to provide the necessary dynamic range. Finally, the use of a star topology with token passing requires that the optical transceivers operate in a burst mode, that is, only transmitting when the token is held. This influences the design of the transceiver, particularly with respect to laser control, receiver stability and signal clock recovery.

The optical transceiver must be compatible with use within a standard SEM-E avionics module. This requires the adoption of a small-footprint, surface-mount compatible package with very low headroom. The design target is a package measuring ~15 x 25 mm and 3 mm high. This is considerably smaller than conventional optoelectronic packages supporting this degree of functionality, and requires the adoption of novel micro-packaging techniques.

The optical transceiver is required to operate over the normal range of environments encountered in military avionics applications in terms of temperature, humidity, vibration, radiation and contamination, and the packaging technology needs to be appropriate for this.

5.1 Transceiver Design

The requirement for high power, low threshold, high reliability, wide temperature range, and compatibility with polymer waveguide material absorption windows led to the selection of the strained quantum-well active layer InGaAs/GaAs laser operating at a wavelength of 0.98 μm. These devices have demonstrated the capability for direct modulation at rates up to 2 GBit.s^{-1}, 10 mA threshold current, optical output of 30 mW (15 dBm) at 100 mA drive, capability of lasing at temperatures in excess of 160 C and relative insensitivity of both threshold current and efficiency with temperature without active temperature control [4]. The detector is a conventional planar *pin* diode with 75 μm diameter active area and top surface electrical contacts on a semi-insulating InP substrate [5].

5.2 Transceiver Packaging

The optoelectronic transceiver has been designed as a multi-chip module assembly, constructed on a silicon substrate housed in an all-silicon hermetic package, shown schematically in Figure 2. The design incorporates a number of novel features, which together aid in the practical realisation of a compact, low-profile surface-mounted package. This comprises three major silicon components, the baseplate, the spacer providing adequate headroom over certain relatively tall components, and the lid, together with an etched lead-frame for surface mounting. The silicon piece-parts incorporate etched V-groove solder channels, providing completely hermetic sealing on final assembly.

The integral silicon baseplate supports an electrical ground plane, together with a number of dc and signal interconnect metalisation layers, with etched V-grooves for the passive alignment of fibres to internal optoelectronic components. In order to minimise internal crosstalk, the transmitter function (laser diode chip and its associated drive circuit) and two stages of the receiver function (*pin* photodiode and preamplifier, followed by further amplification) are situated in separate compartments, effective electrical screening being provided by the full-height walls incorporated in the design. All optoelectronic and electronic components are solder mounted, top-surface connections being made where necessary via wire bonds; solder techniques are also applied to fibre alignment [6], with the entire optical assembly being intrinsically self-aligning.

The soldered-silicon assembly is compatible with low cost polymer encapsulation techniques, as well as conventional metal or ceramic packaging for higher performance applications. The dimensions of the assembled package are of the order of 15 mm x 25 mm x 3 mm, including the fibre bush, and the unit provides ECL-compatible burst-mode signalling at rates up to ~650 MBaud.

5.3 Prototype Transceiver Performance

Test structures for assessing laser-to-fibre and fibre-to-detector coupling were assembled using etched silicon baseplates from the transceiver assembly. Evaluation of these samples showed a laser-to-fibre excess coupling loss of ~4 dB, and a fibre-to-detector excess coupling loss of ~2 dB, both within the designed values and providing initial confirmation of the viability of the passive alignment technique employed. Figure 3 shows a (partially assembled) prototype transceiver. Completed transceivers have been evaluated in point-to-point link configurations and operated successfully at data rates up to 625 MBit.s^{-1}. Attempts to induce modal noise [7] in these links have indicated low sensitivity to this effect.

6 SYSTEM DEMONSTRATOR

6.1 System Architecture

The Demonstrator system, currently under construction, comprises a set of high-speed processors and associated circuits interconnected via a suitable backplane. Systems of this type are conventionally interconnected via parallel electrical bus structures, a typical contemporary high-performance configuration being the JIAWG Parallel Interface bus (PI-bus) [8], which in its most complete implementation operates over 58 electrical bus lines at a total rate (data and control) in excess of 500 MBit.s^{-1}.

Figure 4 shows schematically the modular avionics optical bus Demonstrator system, currently under construction. This is based on a waveguide star backplane, with optoelectronic transceivers at the terminals and a polymer waveguide communications medium serving each module. Each SEM-E module in the rack will be served by one optoelectronic transceiver; in a fully dual-redundant implementation, as required by the LTPB specification, the cabinet would contain two independent backplane stars and each SEM-E module would support two fully independent optical interfaces. Target performance and functionality of the Demonstrator System is outlined in Table 2.

Table 2 Target Performance for Modular Avionics Interconnect Demonstrator System

Processor	32-bit
Number of Boards	3 Processor Boards + 1 Global Interface Board (Fully populated system 16 Boards)
Backplane Medium	Polymer Optical Waveguide
Backplane Architecture	Serial Star Interconnection
Access Control	Token Passing
Channels/Board	2 (4 in Dual Redundant System)
Clock Rate	531 MHz
Data Rate	425 MBit.s^{-1} data + 106 MBit.s^{-1} protocol/coding (8B/10B) (531 MBaud)
Capacity	53.1 Mbyte.s^{-1}
Data Format	1 to 1000 word message
Latency	6 μs for 64 word message on unloaded bus 60 μs on loaded bus for priority message

6.2 System Protocol

The protocol selected for the Demonstrator system is a variant of the SAE Linear Token Passing Bus (LTPB)[9]. LTPB was developed specifically as a high speed bus for the avionics communications environment, and uses the principle of passing a token (i.e. a reserved digital symbol) between a network of identical terminals, giving the recipient station the right to transmit messages. The LTPB Standard, defined in such a way as to be independent of transmission medium technology, supports up to 128 terminals, with a maximum separation of 1000 m, connected to a common broadcast medium, either electrical conductor or optical fibre, allowing a transmitting terminal to be heard by all other terminals, including itself. Greater integrity is afforded by the use of dual redundancy, i.e. each station has two separate optical paths for transmission and reception. The LTPB Standard specifies that both transmitters be active at a transmitting station, that both channels be used in the signal path and that the first correct message be accepted. A convenient topological implementation is therefore the transmissive star based on the use of a single multi-port coupling element.

A new implementation of the LTPB standard has been devised, compatible with the requirements of the Demonstrator. The most significant difference, apart from the obvious consequences of increasing the data rate to 500 MBit.s^{-1}, is the substitution of ANSI 8b10b coding for the Manchester coding adopted in existing LTPB implementations. This modification, in addition to reflecting contemporary line coding practice for optical links, reduces the coding overhead from the 100% implicit in Manchester coding to 25% (625 MBaud signalling rate), although introducing additional demands in terms of clock recovery.

For the Demonstrator system, the interface between the processor and the optical backplane is controlled by a commercial chip set (AMCC Types S2030 and S2031), providing multiplexing/demultiplexing, coding/decoding and clock recovery functions. This provides 531 MBaud operation, (425 MBit.s^{-1} data with 8b10b coding, the Fibre Channel standard), and is compatible with burst mode operation. A custom protocol chip combining the LTPB protocol and interface chip functions, and capable of the full 625 MBaud signalling rate, is being developed for use in subsequent modular avionics system demonstrations.

6.3 Optical Pathway

The optical pathway fabric selected for this demonstrator system is a polymer waveguide , combining the capability for high functional interconnectivity with relatively low loss and low cost manufacture. Trials have been performed using the DuPont "Polyguide™" waveguide technology [10], which offers a low-loss, high temperature capability interconnect fabric, and prototype optical waveguide star couplers have been designed and fabricated. Using an optimised design, a low loss 8-way waveguide star has been demonstrated with less than 3 dB excess loss and better than 1 dB output uniformity. Figure 5 shows a graphical representation of excess loss measured along the 64 possible paths within this device, illustrating the excellent uniformity obtained with careful star design [11] [12] and the use of this material system.

6.4 Backplane Connector

A critical factor in module design is the selection of connector used at the backplane interface. In first prototypes, short lengths of multi-mode fibre will be employed to link the transceivers to fibre feed-through based connectors, held within conventional multi-way electrical board edge connector housings. This has the advantages of using established standard connector technology, as well as providing a convenient means of achieving stress relief between the transceiver and the connector, and greater freedom in transceiver location on the board. The backplane connector selected is a SEM-E modular connector (Teradyne types KS 1050 and M 1050), which has 372 pins on an 8 row grid, with up to eight 20 gauge feed through points capable of taking coaxial or fibre optic inserts.

7 CONCLUSIONS

Progress towards the realisation of an optical backplane compatible with use in a modular avionics system has been described. Critical components include robust, compact optoelectronic transceivers, optical backplane fabrics and demountable optical connectors. Prototype components have been demonstrated and the construction of a demonstrator system commenced.

8 ACKNOWLEDGEMENTS

This work has been carried out with the support of GEC businesses and of the Commission of the European Union in the ESPRIT III Project 6276 "Hierarchical Optical Interconnects for Computer Systems" (HOLICS).

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D. Israel, R. Baets, N. Shaw and M. J Goodwin
Tech. Digest MOC/GRIN '93, Kawasaki, Japan (1993)

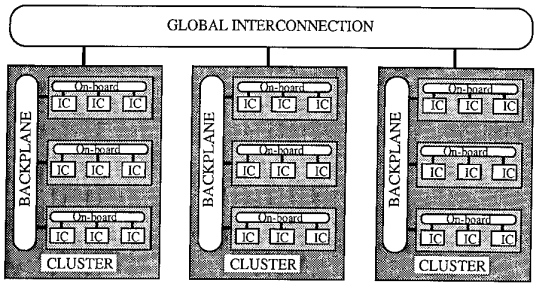
[12] Comparison of different polymeric multimode star couplers for backplane optical interconnect
D. Israel, R. Baets, N. Shaw, M. Salik and M.J. Goodwin
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DISCUSSION

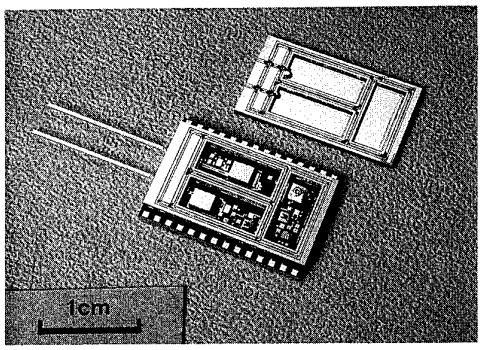
Question: Have you performed any environmental testing yet?

Answer: The laser chips have been characterized over at least the temperature range 20 - 90°C. Fully assembled transceiver modules have not been subjected to full environmental testing.

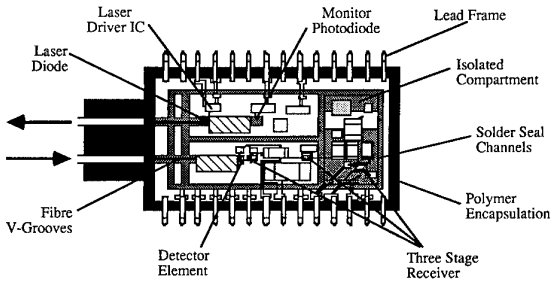
FIGURES



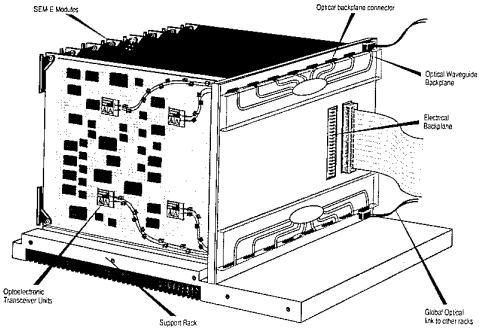
1 An hierarchically interconnected network



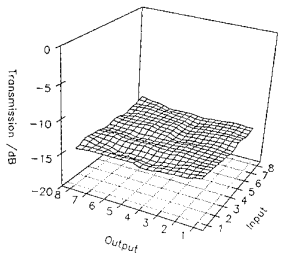
3 Partially assembled transceiver



2 Schematic of Transceiver layout



4 Schematic of avionics backplane demonstrator system



5 Response uniformity of polymer waveguide star coupler

The ROC Optical Connector

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1. SUMMARY

The new multimode connector has been developed that will function under harsh environmental conditions. It meets the military's need for a reliable optical insert that can be integrated into existing electrical, card-edge connectors. Expanded-beam optics and micro-machined silicon sub-assemblies are employed to achieve low optical loss (<1 dB) under blind-mate conditions. Low-mass, floating termini and kinematic design make the ROC connector insensitive to high levels of shock and vibration. Self sealing doors protect the optical assemblies from particulate contamination and abusive handling. The connector has performed flawlessly under extensive environmental and durability testing. This paper will describe the ROC design, features, and test results.

Note: This work was sponsored in part by the Air Force's Wright Laboratories (AAAS-1) under the AAAPT program, Contract No. F33615-89-C-1036.

2. INTRODUCTION

Optical transmission is rapidly becoming the physical transport medium of choice for high-bandwidth data communications. Emerging military systems are bring optical data links onto line-replaceable modules, driving the need for an integrated electro-optical card-edge connector. This is not a simple connector design, since optical and electrical connectors have different mating requirements. Electrical connectors conduct the flow of electrons between two conductors, whereas optical connectors focus light between two optical waveguides. Electrons will follow any convoluted path, as long as the two conductors are touching. Optical connections require the ends of the fiber waveguides to be parallel and precisely aligned to accuracy of a few tens of microns or less.

Almost all optical connectors in use today use a butt-joint (ferruled) connection. This connection is the optical analog of an electrical jack plug. Basically, the fiber ends are epoxied into separate ferrules and held in alignment by a sleeve and spring. In many cases, the sleeve is an integral part of one of the ferrules. Thus, it was not surprising that the first attempts to develop a card-edge optical connector used a butt-joint connection. Connector engineers modified existing in-line connectors to conform to the physical specifications of existing electrical connectors. This was not a straightforward task, since the critical alignment required for making a optical connection was magnified by the relatively large mis-alignment tolerances and blind-mate requirements of electrical card-edge connectors.

About five years ago, a joint Navy-Air Force task force conducted a series of durability and environmental tests using six of the leading card-edge optical connectors. Four of the six connectors failed catastrophically before the tests were completed and the remaining two connectors exhibited open connections and high losses (>20 dB). The results of these tests were particularly disturbing because a number of advanced military platforms were being predicated on line-replaceable modules with optical card-edge connections.

Several of the failures were attributed the relative gross alignment afforded by electrical connector shells. Butt-joint optical connections are quite sensitive to longitudinal separation. Their lowest optical loss occurs when the fiber ends touch and exceed 1 dB (a design maximum) at a separation of only 50 microns. Thus, the fiber faces must be maintained in near-touching alignment for a low-loss connection. This close proximity can introduce a problem called pistoning. Basically, the fiber end piston into one another under shock and vibration. Inadequate retention force and poor bonding of the fiber clad to the ferrule are two common causes of this problem.

The materials selection and manufacture of butt-joint ferrules poses a number of reliability issues A thermal coefficient of expansion mismatch between the ferrule and the fiber materials can lead to failure under thermal cycling. Ceramic ferrules solve this problem, but are themselves easily fractured under extreme shock and vibration. The ferrule holes require precise alignment and bore diameter. Any lateral misalignment, ellipticity, or eccentricity between the transmitting and receiving fiber core contributes to increased optical loss.

Butt-joint connectors are easily contaminated by sand and dust. The alignment sleeve is particularly prone to trapping contaminants and must be cleaned prior to mating. A small dust speck can easily block light transmission if it occludes the fiber core. Any trapped particulate matter larger than 50 microns (the diameter of fine sand is about 300 microns) will prevent the butt-joint fiber ends from achieving low-loss contact.

These problems have led to a radically different optical connector—the Reliable Optical Card-edge (ROC) connector.

3. OPTICAL DESIGN

The ROC connector use expanded beam optics and a silicon sub-assembly to circumvent many of these problems associated with butt-joint connections..

Expanded beam optics take advantage of the fact light can be focused by lenses placed in front of the fiber ends *(See Figure 1)*. Light diverging from the transmitting fiber end is collimated by the transmit fiber lens. The receiving lens focuses the collimated light beam into the receiving fiber core. This design provides two distinct advantages. First, the lowest optical loss is achieved when the lenses are slightly separated, eliminating the problems associated with pistoning. Secondly, the expanded beam optics form a larger collimated light cone; thereby relaxing lateral alignment requirements. Measurements have shown that the expanded beam optics can tolerate a order of magnitude greater longitudinal misalignment and a factor of two greater lateral misalignment than the butt-joint connection (for a 1 dB or less loss).

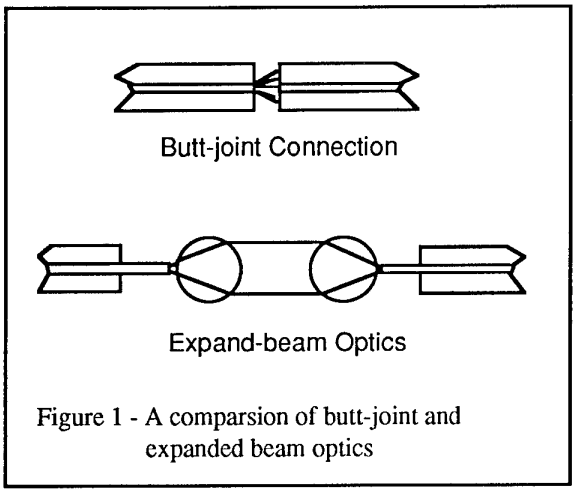


Figure 1 - A comparsion of butt-joint and expanded beam optics

The expanded beam optical assembly is implemented on a small silicon alignment chip. The fibers are accurately aligned to the lenses by a vee-grooves that are chemically etched in the chip. This etching process produces mirror-finished grooves that are accurate to less than one micron. The lenses are hard sapphire balls that have been coated to reduce reflections. The gap between ball lens and fiber end is filled with an index matching material to eliminate index mismatch losses and protect the fiber ends.

The ROC connector consists of a male and female optical assembly. These two assemblies form dual optical connections. The silicon chip used in the female assembly contains an additional groove in front of each ball lens *(see Figure 2)*. The male terminus' ball lens drops into this vee-groove in a movement similar to lowering a phonograph needle into a record groove. Since the two ball lenses are captured in vee-grooves, the termini are constrained from rotating laterally. The male termini contains a third sapphire ball, providing three points of contact. This kinematic alignment ensures that the male and female silicon blocks are perfectly parallel. The alignment is very positive and the silicon optical assemblies can be manually mated with low loss.

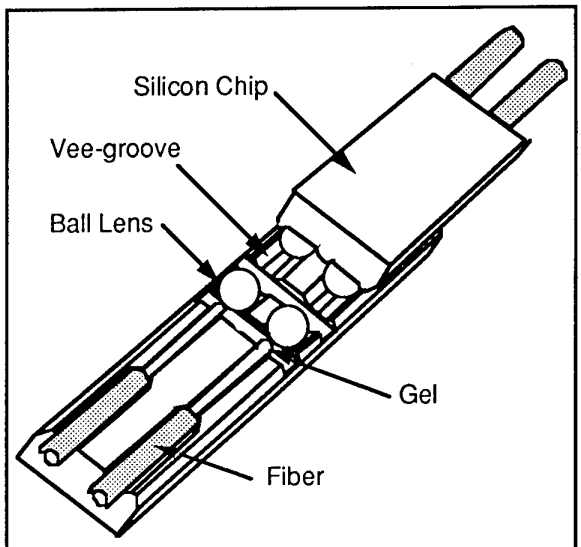


Figure 2 - Mated ROC Optical Assembly

4. THE CONNECTOR INSERT DESIGN

Expanded beam optics can accommodate greater longitudinal and lateral misalignments than a butt joint connector. However, they still requires a mating alignment that is five times more accurate than a typical high-density electrical connector. Electrical connectors use an alignment pin and sometimes the shell to provide electrical pin alignment. The ROC inserts are designed to float, bring the male and female inserts together with an accuracy of ± 0.1 millimeters in all three axes. The male optical termini float within the insert housing. They can move by ± 0.1 millimeters, compensating for any misalignment between the module and backplane inserts The silicon vee-groove technology provides the final lateral alignment to an accuracy of less than a two microns. A special spring holds the male termini flat against the female termini. Since module terminus can still float after mating, it will track any movement of the fixed female termini. A good analogy is that the module termini floats like a phonograph needle on a warped record. The module terminus is extremely low in mass and its floating ability make it highly immune to mechanical and thermal shock.

Figures 3 and 4 show the male and female ROC connector inserts. The external dimensions of the insert housings conform to the specifications of a given connector's insulator block. However, the interior cavities of the housings are common across all electrical connectors. Each housing incorporates a protective door that closes automatically upon disengagement. These doors prevent dust and other contaminants from reaching the optical assemblies. Since the volume swept by the door cannot contain any optics, minimizing door sweep was a critical design issue. The male housing employs a simple spring-loaded trap door, while the female

housing uses a visor-type door for minimum door sweep.

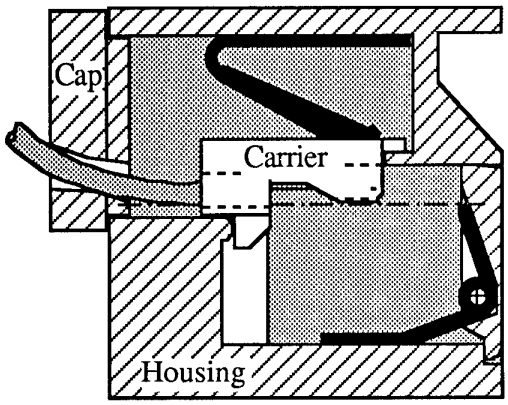


Figure 3 - The Male ROC Connector

The optical assemblies are bonded to special carriers forming a complete terminus. These carriers aid the final mating alignment and protect the optics from sand and dust. The male (module) termini are easily inserted and removed with a simple tool. The female (backplane) termini are designed to be field removable without tools. The termini are secured in their respective insert housing by retention caps. The module termini are secured by a snap-tab cap that holds the fiber at a precise bending angle. The female termini are held rigidly in place by screw-on retention cap. This cap employs a silicon cone to ensure a safe minimum bending radius for the fiber.

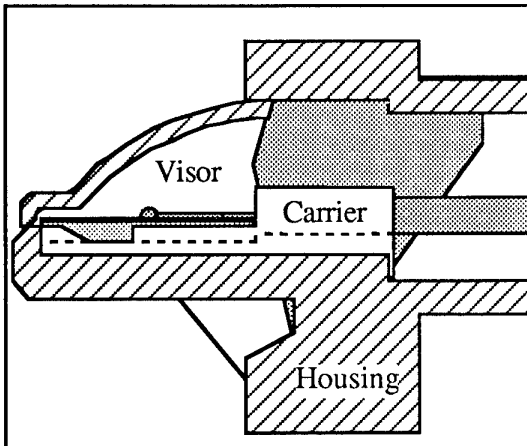


Figure 4 - The Female ROC Connector

5. TEST METROLOGY AND SETUP

Considerable care must be taken when making and comparing optical connector loss measurements. Connector loss is dependent on the fiber type and launch conditions. The measured loss for a given connector can vary by as much as 0.3 dB depending on how light is launched into the connector. Unfortunately, there is no single satisfactory way to measure loss. The EIA FOTP-34 standard alone defines four procedures. The most common measurement technique is to overfill the fiber core with light and remove unstable cladding modes through mode-stripping techniques. This procedure results in a uniform fill distribution across the fiber core (with no cladding modes) and yields in the greatest measured loss. This procedure provides reproducible launch conditions and a level ground for comparing connectors. Unfortunately, it does has several disadvantages. The launch conditions are not representative of most optical transmitters. Great care must be taken to ensure that the cladding modes have been stripped and not reintroduced by other effects such as microbends. This procedure requires a special broad beam transmitter. These transmitters are either CW or low clocking rate making them unsuitable for bit error rate (BER) measurements.

BER measurements are critical for detecting intermittent errors resulting from shock and vibration test. This measurements requires a transmitter that clocks at the high rate (100 to 400 MHz). These optical sources tend to underfill the fibers (i.e., equilibrium mode distribution conditions). The measured results are more representative of actual losses encounter in actual designs. However, it is difficult to compare data from different sources since the loss is dependent upon the shape of the launched beam.

AT&T engineers have solved this problem by deriving and verifying an accurate model that specifies a connector's loss over a wide range of launch condition. Once a single test parameter has been identified, this model yields the loss for most other launch conditions. The model is predicated on the fact that the steady state power distribution for most optical sources can be closely approximated by a truncated Gaussian shape. This model allowed the ROC using an underfill procedure and compared to the test results to other connector data.

Two basic test setups were used to measure and monitor optical loss in the ROC connector. Tests such as salt fog, thermal cycling, and sand/dust required measurements to be taken before and after the test conditions. This required an reproducible technique to break and remake connections with the measurement equipment. The optical source was an ODL 250 LED transmitter with a 62.5 μm fiber stub. This stub was fusion spliced to a 100/140 μm fiber and routed through a mode scrambler and stripper. The optical power output was highly stable (<0.01 dB) and reproducible. The test procedure consisted of taking the output fiber from the mode stripper and coupling it directly to the optical power meter. The power meter was then set to zero, so that the connector loss would be a direct readout. The connector termini were then fusion spliced between the mode stripper and the optical power meter, providing a direct reading of the connector loss.

Shock and vibration testing require in situ monitoring during testing to detect any intermittent faults. These intermittent faults can be brief and may not be detectable with an optical power meter (that displays a power average of a time interval). Two separate procedures were used to detect intermittent opens. The first procedure utilized an optical data link transmitter and receiver pair, an optical attenuator, and a bit error rate (BER) detector. The output from one channel of a ROC connector was attenuated to the point where a small variation in loss (~0.1 dB) would cause a significantly increase in the BER. Thus, any brief discontinuity would generate a cascade of bit errors. The optical transmitter was clocked at a bit rate of 200 Mb/s (NRZ , pseudo random 2^7-1 for BER detection). The second technique was to display the wave form of the output signal on an oscilloscope and record it on a video recorder. A second ROC channel was monitored using this procedure. The measurement sensitivity in both cases was less than 0.1 dB. Insertion loss measurements were also monitored in a third channel in accordance with paragraph 4.6 of MIL-C-83526.

6. TEST RESULTS

The ROC connector was designed to meet an initial mean insertion loss requirement of 0.75 dB, with a standard deviation of 0.2 dB. *Figure 5* shows the measured variations for the first ROC connectors. The solid bars show the loss measure for the silicon assemblies. This data was obtained by mounting the silicon assemblies on a micro-manipulator and aligning for minimal loss. The assemblies were then bonded to carriers and inserted into a ROC housing. These connectors were integrated into the Bendix T-7 connectors and mated. The measured losses for the mated connectors are plotted as solid white bars. As expected, there is some increase in loss (~0.15 dB) due to tolerance stackup and mechanical misalignment in the electrical connector.

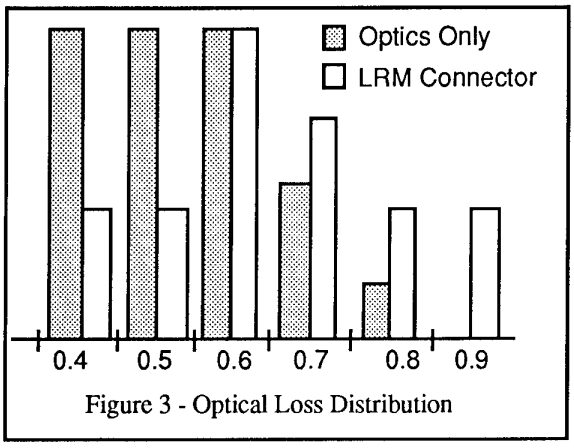


Figure 3 - Optical Loss Distribution

The first ROC connectors was subjected to over two hundred and fifty mating and unmating cycles The first 100 cycles were conducted on an connector insert pair mounted to the micro-positioner. This fixture provided mating loss measurements under ideal and controlled misalignment. Insertion conditions were highly reproducible under these test conditions. The insert was then integrated in a Bendix T-12 connector and attached to a SEM-E format frame. The frame was outfitted with Birtcher (torque-down) wedge locks and slotted in a rack/backplane test fixture. The optical loss measured after each of a 175 mating operations. The card guides in the enclosure segment was oversized to permit a unconstrained ±0.5 mm lateral (z-axis) movement between the backplane and module. The backplane block was not pre-aligned prior to testing and the tests were conducted closing the insertion/extraction levers in unison and individually. Different torque down forces were used and different people performed the tests to provide the variability found in a realistic maintenance environment.

Test results on the ROC connector demonstrated an unprecedented repeatability. Data taken from the micro-positioner test fixture showed a repeatability standard deviation of 0.025 dB, a value within the precision and stability of the experimental test equipment. Tests using the SEM-E module showed a variation in insertion loss of 0.09 dB, with the higher standard deviation being due to misalignment of the module with respect to the backplane connector. There was no visible damage to the inserts or termini after 200 mating cycles. Individual door assembles have undergone over 500 open/close cycles without failure.

The SEM-E module fixture was subjected to random vibration test according to MIL STD-202F, Method 214, Test Condition I, Letter E. The module was subjected to a 0.2 g^2/Hz power spectral density and a 16.9 rms g level in each of the three mutually perpendicular directions. Bit error rates and output wave forms were monitored during the testing to ensure no discontinuity escaped detection. No discernible discontinuity or increase in insertion loss was detected during vibration tests conducted along all three axes.

The module fixture was then subjected to sinusoidal vibrational tests in accordance with Mil-STD 202F, Method 204D, Test condition G. The test consists of a 0.060 inch sinusoidal displacement, ramping up in frequency for a peak acceleration of 30 g's. The tests was performed along all three axes. There was no increase in optical loss or change in the bit error rate.

Mechanical shock is often the Achilles' heal of optical connectors and few connectors are able to pass 30 g shock tests. The ROC shock tests was performed in accordance with the test procedures described by MIL-STD 202F, Method 213B, Condition C. Three half-sine shock pulses of 100 g peak value and 6 millisecond duration was applied in each direction along the three mutually perpendicular axes of the fixture (6 directions, 18 shocks). The connector performed flawlessly, and no discontinuity or change in insertion loss was detected.

The ROC connector was designed to withstand sand and dust conditions that were far more stringent than those

called out in the military specifications. Since particulate contamination is much more likely to occur when the connector is unmated, the ROC connector to designed withstand sand and dust in an unmated configuration. A male ROC connector (module) was exposed for several days to dust and dirt in a representative work environment (lab, outdoors, car trunk, environmental test facility). No additional loss was measured as a result of this test. Next, the unmated connector was exposed head on to sand and dust for six hours with flow conditions of 600 ± 80 meters/minute air velocity; at 23° C and 22% R.H. The optical power was measured before and after the test. No cleaning was conducted other than brushing of dust from the housing face. No definitive change in insertion loss was detected and no debris obstructed any of the optical elements. The standard MIL-STD 202, Method 110 test was conducted on a mated connector assembly and the optical insertion loss was measured in accordance with paragraph 4.6 of MIL-C-83526. No increase in insertion loss was detected on any of the three measured optical connections.

The salt fog test was performed as per MIL-STD 810, Method 509, Procedure I. The rear of the module shell was taped over to duplicate the protection afforded by LRM covers, but the rest of the mated connector was fully exposed to the salt fog environments. After 48 hours of exposure, the fixture was removed and inspected. The was considerable salt crustation on the shell assembly. The connector was unmated and some minor salt crusting was found on the connector face, but the overall appearance was fairly clean. One door assembly was stuck in the open position, but it closed when touched with a probe. The lack of salt crustation on the connector faces is attributed to the excellent seal between the EMI and backplane shell of the Bendix connector. After a 24 hour drying period, the losses for each optical connector was measured. No significant increase in loss was detected.

The ROC connectors was also tested for thermal shock durability using MIL-STD 212, Method 107. The test connector was subjected to twenty-five cycles (-55°C to +125°C) of thermal testing. The connectors were then mated and showed no increase in loss. Additional thermal shock tests have been conducted to test the reliability of the epoxy and gel bond. The optical assembly has been subjected to multiple cycles of -80°C to 155°C with a 60 second dwell. No damage to the epoxy or gel bond was detected.

7. SUMMARY AND CONCLUSIONS

The ROC connector has demonstrated that it can meet military durability requirements. Initial connectors exhibit a mean insertion loss of 0.75 dB with a standard deviation of 0.2 dB. The connector provides superb repeatability (standard deviation of 0.1 dB), and shows no evidence of degradation over many insertions and extractions. The connector has passed a battery of harsh environmental tests with no detectable discontinuity or measurable increase in insertion loss. The self sealing doors do indeed provide good protection, as evidenced by the fact that the connector optics never required cleaning throughout the testing. The connector is now in production and slated for use on several military platforms. Inserts are now being produced designed for several different card-edge connectors, including a single-mode version.

DISCUSSION

Question: Can you reach 100% protection against a sand grain during mating/demating of the connector?

Answer: Almost!

Question: Can we have an idea of the cost (absolute or relative compared to electrical pin) of an ROC optical point?

Answer: Optical connectors are more expensive - and so are the optical-electronic assmblies.

Question: Looking further in the future, what are the limitations of this approach (e.g., some SEM-E optical switch modules may have 128 optical inserts, possibly monomode)?

Answer: Limitations are most likely due to the board area required for the optical-electronic assembly, rather than connector density.

Question: What's the behavior of the ROC connector in extremely hot or cold environments and under sharp temperature differences? Can temperature affect the alignment?

Answer: Temperature extremes have no known effects on connector operation.

BOITIERS COMPOSITES POUR EQUIPEMENTS ELECTRONIQUES AEROPORTES : UNE ETUDE TECHNOLOGIQUE ET CEM

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RESUME
Le but de ce papier est de présenter les travaux de développement (étude, réalisation, qualification) d'un coffret et d'un capot de protection en matériaux composites destinés à des équipements électroniques aéroportés sur avion d'armes.

Les travaux ont été menés avec un double objectif : gagner de la masse par rapport à une solution métallique et obtenir des performances de blindage électromagnétique équivalentes.

La démarche technologique est présentée : choix des matériaux et des procédés de mise en oeuvre, dimensionnement mécanique et électromagnétique. Les procédés de fabrication sont décrits, ils ont permis d'obtenir les caractéristiques visées.

Les éléments en matériaux composites métallisés sont aujourd'hui en exploitation sur avion d'armes.

1. INTRODUCTION

Les systèmes électroniques embarqués sur avion d'armes se caractérisent par une très haute intégration technologique et par une recherche permanente de réduction de leur masse. S'agissant de cette dernière, une utilisation importante de matériaux composites a permis d'alléger la masse des structures et des fuselages des avions. L'étape suivante consiste alors à réaliser les coffrets des systèmes électroniques en matériaux composites. Néanmoins, le problème suivant se pose immédiatement : les circuits électroniques doivent être protégés contre l'environnement électromagnétique de plus en plus sévère et les matériaux composites organiques sont transparents face à ces agressions.

Face à cette situation, deux types d'action sont nécessaires. La première consiste à analyser précisément les agressions électromagnétiques auxquelles sont soumis les circuits électroniques. On distingue alors deux grands types: les phénomènes internes au coffret et les menaces extérieures à l'avion. La démarche consiste à déterminer le blindage nécessaire pour se protéger, ainsi que son meilleur emplacement en terme d'efficacité et de masse. Il est clair que si le résultat de cette analyse conduit a une épaisseur de blindage identique a celle des coffrets métalliques d'ancienne génération, l'utilisation de matériaux composites n'aura alors aucun sens.
Dès lors que les aspects de compatibilité électromagnétique sont pris en compte, la seconde action est de choisir la structure du matériau composite, ses constituants et la technologie de réalisation. Cette étape étant franchie, reste à traiter la métallisation du matériau selon les critères fournis par l'étude électromagnétique. Enfin, le coffret devra protéger les circuits électroniques contre les autres environnements, qu'ils soient mécanique, thermique ou climatique.

L'utilisation de matériaux composites ne peut donc se concevoir que dans le cadre d'une démarche simultanée entre les technologies (composites, métallisation) et la compatibilité électromagnétique.

L'objet du présent papier et de décrire le travail réalisé par la division Radars et Contre-Mesures (RCM) de THOMSON-CSF pour deux types d'application :

- un coffret en composites organiques concernant un ensemble de cartes électroniques,

- des capots de protection de cartes électroniques permettant de protéger ces dernières contre les émissions rayonnées par leurs voisines.

La démarche fait apparaître, dans une première partie, le travail sur les technologies et dans une seconde partie, l'analyse électromagnétique.

2. COFFRET

Les coffrets sont généralement réalisés à partir de tôles en aluminium assemblées par rivetage ou vissage sur une structure métallique interne.

L'allocation de masse accordée pour le coffret a rapidement mis en évidence que seul un changement de matériau pour certains éléments mécaniques permettait de rallier l'objectif de masse.

2.1.Choix de la technologie

Le coffret est composé d'éléments mécaniques de maintien et de positionnement assez peu sollicités mécaniquement et d'éléments structuraux qui confèrent au coffret ses

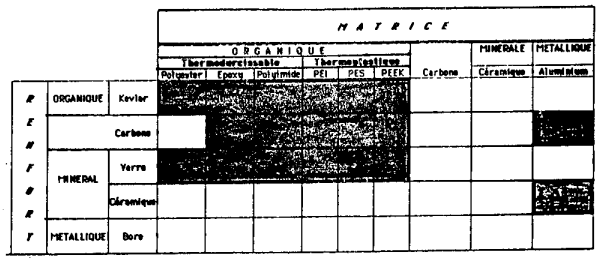
caractéristiques de raideur et de résistance. Un travail d'analyse de la valeur a montré que le meilleur compromis masse/coût serait obtenu en conservant en conception métallique les éléments de maintien et de positionnement et en remplaçant le métal des éléments structuraux par des matériaux composites.

Le coffret est un parallélépipède (600 x 300 x 200 mm) dont les 6 faces sont des panneaux structuraux.

2.2. Choix des matériaux

Le coffret est réalisé en matériaux composites c'est à dire, en matériaux de synthèse constitués d'un renfort filamentaire et d'une matrice. Le rôle du renfort filamentaire est de faire passer les efforts mécaniques, celui de la matrice est de conserver la disposition géométrique du renfort filamentaire et de répartir les contraintes dans celui-ci.

Pour ses applications à dominantes radioélectriques (antennes et radôme) et mécaniques THOMSON-CSF RCM utilise les composites suivants



Les caractéristiques d'un matériau dépendent évidemment des caractéristiques du renfort et la matrice qui le constituent. Le tableau ci-dessous compare les principales caractéristiques des matériaux composites avec les matériaux métalliques traditionnellement utilisés pour la fabrication des équipements aéroportés.

	densité	E(MPa)	R(MPa)	coef.de dilat. (°K).10⁻⁶
Carbone/Epoxy (Quasi-isotrope)	1.6	60 000	450	3
Carbone/Epoxy (unidirectionnel)	1.6	130 000 (sens fibres)	1 000 (sens fibres)	1 (sens fibres)
Kevlar/Epoxy (Quasi-isotrope)	1,37	32 000	550	1
Verre/Epoxy (Quasi-isotrope)	1,9	25 000	400	16
Carbone/PEEK (unidirectionnel)	1.6	134 000 (sens fibres)	2 100 (sens fibres)	1 (sens fibres)
Verre/PES (Quasi-isotrope)	1,9	28 000	250	14
Verre/PEI (Quasi-isotrope)	1,9	28 000	300	14
Céramique/Aluminium (Quasi-isotrope)	2,9	150 000	860	9
Verre/PES (30% fibres courtes)	1.6	10 000	110	30
Verre/PEEK (20% fibres courtes)	1,45	7 000	100	20
Aluminium	2,77	77 000	420	24
Acier	7,8	210 000	1 100	14
Titane	4,5	105 000	1 000	8

Ces valeurs sont indicatives. Il est impératif de connaître avec précision la distribution des contraintes dans les éléments structuraux afin d'améliorer les renforts dans le sens des efforts.

Les pièces travaillantes en composites doivent toujours être dimensionnées par le calcul.

Le matériau retenu pour la fabrication du coffret est le carbone / Epoxyde car il possède des caractéristiques mécaniques de raideur et de résistance à la rupture proche de l'aluminium mais avec une densité 40% plus faible.

Choix de la technologie :
Compte tenu du volume interne implanté et des dimensions extérieures, l'épaisseur allouée pour les faces du coffret est inférieure à 3 mm.

→ La technologie structure sandwich n'est pas adaptée. De plus les procédés de métallisation sous vide ou en milieu liquide nécessite souvent d'augmenter l'épaisseur donc la masse des peaux pour les rendre étanches.

Le coffret sera composé d'éléments monolithiques assemblés par rivetage. Cette technologie dite multiphases a été préférée à la technologie monophase (réalisation en une seule polymérisation) car elle nécessite des outillages beaucoup moins complexes et permet d'obtenir des tolérances beaucoup plus précises.

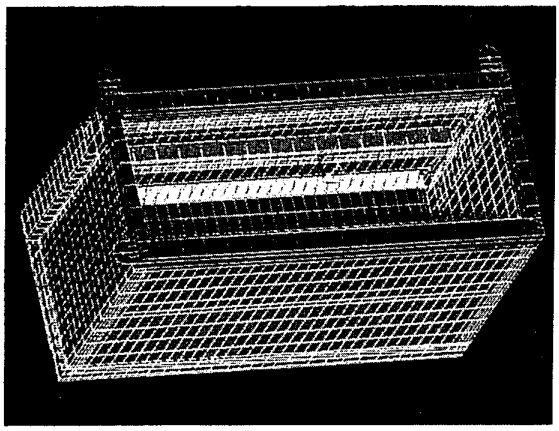
2.3. Dimensionnement du coffret

L'objectif étant le gain de masse, le dimensionnement par le calcul est indispensable pour ne pas sur dimensionner.

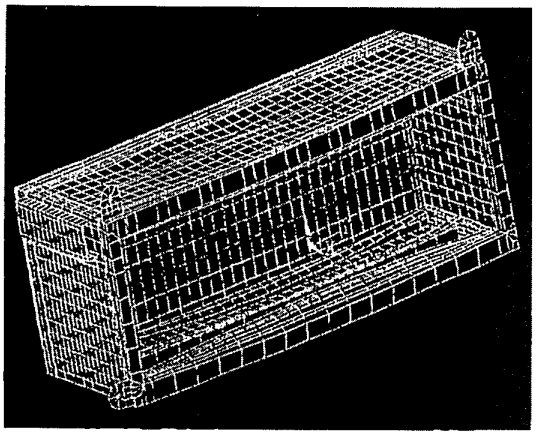
L'électronique embarquée sur avions d'armes est particulièrement sollicitée sur le plan mécanique car les niveaux vibratoires sont très élevés.

L'analyse mécanique globale a été effectuée avec le logiciel de calcul par éléments finis ANSYS.

Maillage :



Calcul des contraintes et des déformations :



Un travail d'analyse locale a été réalisé en utilisant les logiciels MIC-MAC de Stephen W. TSAI que nous avons modifiés afin de les rendre plus conviviaux.

Analyse du stratifié en traction :

Plaque hybride en traction

PLIS	Theta 1	Theta 2	Theta 3	Theta 4	Matériaux	Tissus Carbone 914/40%/G803		
Angle des plis	0	90	45	-45	Répétition	nb plis	Rotation 1	
Nombre de plis	1	1	0	0	2	8	0	
					Matériaux	Tissus Carbone 914/42%/G806		
Angle des plis	0	90	45	-45	Répétition	nb plis	Rotation 2	
Nombre de plis	1	1	0	0	2	8	0	

CHARGEMENT			CONTRAINTES			h (mm)	Rotation
N1	1000	N/mm	Sigma 1	23	N/mm²	3.48	0
N2	2000	N/mm	Sigma 2	46	N/mm²		
N6	3000	N/mm	Sigma 3	70	N/mm²		

MODULES D'ELASTICITE	E	E Quasi-isotrope	
E1	54719	37321	N/mm²
E2	54719	37321	N/mm²
E6	992	14139	N/mm²

MODIFICATION DU FICHIER MATERIAUX					Modifié !!!			
	T util	c. humid	vol/fibr	Em	Etx	Xm	Xtx	Em/Em°
Caract. de base	20	0.005	0.36	3.4	366.67	75	3347.22	0.2
Modifications	20	0.005	0.36	3.6	366.67	75	3347.22	0.3
Modifié ?	Non	Non	Non	Oui	Non	Non	Non	Non
Caract. de base	20	0.005	0.275	3.4	190.91	104	4381.82	0.2
Modifications	20	0.005	0.275	3.4	190.91	104	4381.82	0.2
Modifié ?	Non	Non	Non	Non	Non	Non	Non	Non

Analyse des contraintes moyennes dans le stratifié autour des trous des rivets :

Plaque trouée en traction

PLIS	Theta 1	Theta 2	Theta 3	Theta 4	Matériaux	Tissus Carbone 914/40%/G803		
Angle des plis	0	90	45	-45	Répétition	nb plis	h (mm)	Rotation
Nombre de plis	1	1	0	0	1	4	0.864	0

CHARGEMENT			Sécurité	1	R lim	0.67	ATTENTION !!!
N1	100	N/mm	CONTRAINTES			FACTEUR DE CONCENTRATION	
N2	0	N/mm	Sigma 1	78	N/mm²		traction / Compression
N6	0	N/mm	Sigma 2	0	N/mm²	Kc 1	4.96 / 0.00
q. pression	0	N/mm	Sigma 6	0	N/mm²	Kc 2	0.00 / 0.00
t. moment	0	N/mm	Sigma q	0	N/mm²	Kc 3	0.00 / 0.00
Angle de déper	0	degré	Sigma t	0	N/mm²		
Angle de fin	120	degré		en traction	en compression		
			Sigma max	574	-116	N/mm²	
			à l'angle	90.0	0.0	degré	

MODIFICATION DU FICHIER MATERIAUX					Modifié !!!			
	T util	c. humid	vol/fibr	Em	Etx	Xm	Xtx	Em/Em°
Caract. de base	20.0	0.005	0.36	3.40	367	75.0	3347	0.20
Modifications	20.0	0.0	0.5	3.4	366.7	75.0	3347.2	0.2
Modifié ?	Non	Non	Oui	Non	Non	Non	Non	Non

2.4 Métallisation du composite

La résine époxyde qui imprègne les fibres de carbone rend le composite intrinsèquement isolant. Les propriétés de blindage et de continuité doivent donc être conférées par un procédé externe au matériau. Cet aspect est traité au chapitre 4.

Mise au point de la métallisation :

THOMSON-CSF RCM dispose dans son unité à ELANCOURT d'un service de Plasturgie et d'un service de Traitement de surface. Par un travail en coopération entre les deux équipes les procédés de stratification et de métallisation ont été adaptés afin d'optimiser l'adhérence du dépôt métallique sur le matériau composite.

Qualification de la métallisation :

Des éprouvettes ont été réalisées et ont suivi un programme de vieillissement en environnement :

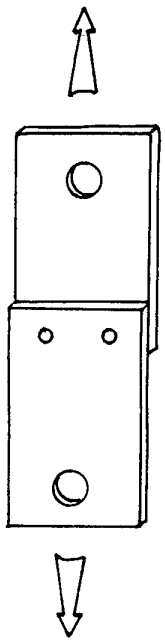
- Chaleur humide
- Variation rapide de température
- Brouillard salin

Les valeurs d'adhérence n'ont pas évolué après ces essais

2.5.Assemblage des panneaux en composite

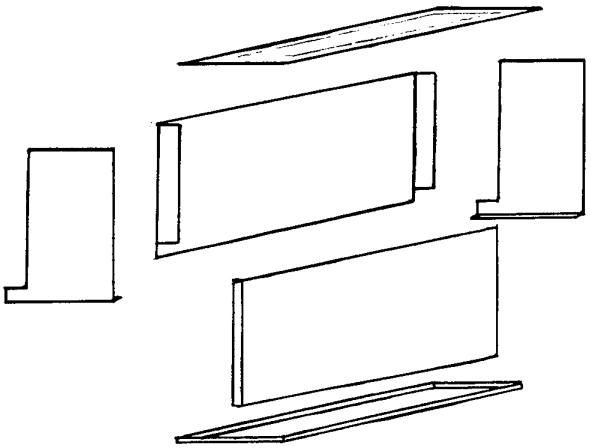
Les différents éléments en composite sont assemblés par rivetage.

Une campagne d'essais mécaniques sur éprouvettes a permis de déterminer la nature et le diamètre des rivets.

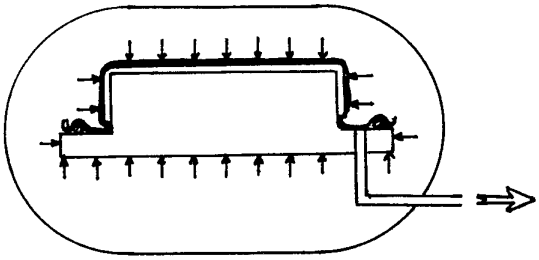


Les essais en brouillard salin ont mis en évidence les risques de corrosion entre le carbone et les rivets en aluminium qui sont à proscrire pour notre application.

2.6.Fabrication des éléments en composite
Le coffret est constitué de 6 éléments



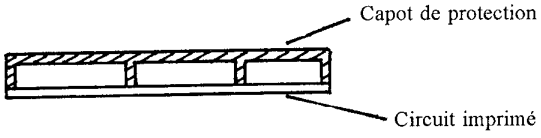
Les éléments sont réalisés à partir de tissus préimprégnés Carbone/Epoxyde stratifiés en autoclave.



Le service plasturgie de THOMSON-CSF RCM ELANCOURT dispose d'une salle de drapage en atmosphère contrôlée (température et hygrométrie) et d'un autoclave de polymérisation à 300°C et 30 bars
(voir ANNEXES A1 et A2).

2.7.Assemblage du coffret
Après stratification les éléments composites sont métallisés et assemblés par rivetage. L'annexe A3 montre le coffret avant peinture.

3.CAPOTS DE PROTECTION
Les circuits imprimés hautes fréquences qui assurent un découplage électronique entre les fonctions électroniques imputées sur la carte.



Les ensembles appelés "bandes" sont ensuite intégrés dans un coffret. Un coffret contient de 20 à 30 bandes. Les capots de protection réalisés par usinage d'un bloc d'aluminium présentent un bilan de poids élevé que nous avons réduit en changeant de technologie.

3.1. **Choix de la technologie**
Un capot métallique pèse 300 grammes et les quantités à produire peuvent être de plusieurs milliers.

Sur le plan structural cette pièce n'étant pas fortement travaillante, le choix s'est porté sur un matériau composite à matrice organique chargé de fibres courtes.

Le tableau ci-dessous indique les caractéristiques mécaniques des principales résines.

	densité	E(MPa)	R(MPa)	coef.de dilat. ($°K).10^{-6}$
Polyester	1.25	3 000	55	60
Epoxy	1.35	2 500	50	60
PEEK	1.32	3 600	92	50
PES	1.37	3 300	75	60
PEI	1.27	3 000	105	60

Les résines ont des valeurs mécaniques assez proches.

Compte tenu du nombre de pièces à fabriquer, la technologie de mise en oeuvre retenue est l'injection haute pression. Les résines thermodurcissables Polyester et Epoxy ont été éliminées à cause de leur temps de cycle de transformation beaucoup plus importants que celui des résines thermoplastiques.

Les critères de choix entre PEI, PES et PEEK ont été l'injectabilité et l'aptitude à la métallisation.

Injectabilité :
Une analyse par simulation numérique a été effectuée en utilisant les logiciels "Ideas for plastics" de SDRC. L'étude a porté sur le remplissage du moule et sur la déformation de la pièce après injection et a permis d'optimiser à 30% le taux de fibre de verre.

Métallisation :
Les propriétés de blindage électromagnétique sont assurées par un dépôt galvanique de métal sur le matériau composite.

L'adhérence de la métallisation a été étudiée sur 3 matériaux supports

- PEI chargé 30% de fibres de verre
- PES " " "
- PEEK " " "

Les éprouvettes d'essais ont subi une campagne de vieillissement accéléré.

- Chocs thermiques
- Chaleur humide
- Brouillard salin

La tenue de la métallisation a été mesurée par des essais d'arrachement après quadrillage. Le matériau qui a été retenu est le PES chargé de 30% de fibres de verre.

3.2. Réalisation des capots

THOMSON-CSF RCM possède une grande expérience dans l'injection des matériaux plastique hautes performances pour la réalisation des antennes et des radomes.

L'étude par simulation du remplissage a permis d'optimiser la position du point d'injection et les dimensions des canaux d'injection afin d'éviter les lignes de soudures et les retassures sur la pièce.

A partir de ces informations un moule en acier a été réalisé. Le PES s'injecte aux environs de 320° dans un moule stable à 200°. Le moule doit donc être équipé d'un dispositif de régulation thermique assuré par des résistances thermiques et par un système de circulation d'huile. L'analyse thermique par éléments finis a fourni les puissances et les positions de ces différents éléments. Les capots (ANNEXE B1) ont été injectés chez THOMSON-CSF RCM sur une presse ENGEL de 120 tonnes (ANNEXE B2), puis métallisé par dépôt galvanique (ANNEXE B3).

3.3 Conclusion

La masse du capot injecté métallisé est de 200 gr soit un gain de 25% par rapport à la solution métallique et des caractéristiques de blindage équivalentes.

L'analyse économique montre qu'au delà de 1000 pièces le prix série de la solution en plastique métallisé est moins élevé.

Cette technologie apporte donc un double intérêt de masse et de coût.

4. METHODE UTILISEE

Les matériaux composites ont une faible efficacité de blindage contre les champs électromagnétiques. Il est nécessaire de les recouvrir de matériaux conducteurs pour garantir la protection des circuits électroniques internes contre les perturbations électromagnétiques.
La masse de ces protections métalliques doit être aussi faible que possible de manière à ne pas s'opposer au gain de masse que l'on a réalisé en choisissant la filière composite.
Dans la pratique, deux types de blindages doivent être spécifiés : les blindages des cartes qui sont nécessaires à la protection des circuits contre les perturbations électromagnétiques inter-cartes et les blindages que l'on doit distribuer entre le coffret et les cartes pour assurer la protection contre les perturbations d'origine extérieure.
Les sources de perturbations extérieures qui ont été prises en compte dans le cadre de ce travail sont :

- les champs sinusoïdaux dont le champ électrique a un module de 200 V/mm, tels qu'ils sont définis par la norme MIL STD 461 C.

- l'onde IEMN (impulsion électromagnétique d'origine nucléaire).

La méthode de spécification définie ici peut être étendue à toute autre source.

4.1 Propriétés caractéristiques des blindages d'enceintes constituées de matériaux composites.

Les blindages que nous devons spécifier sont des films métalliques minces. Ils ne sont pas infiniment conducteurs et, par conséquent, ils laissent diffuser les champs électrique et magnétique.
Le champ électrique est fortement atténué à la traversée de la paroi. Le champ magnétique n'est pas atténué en basses fréquences. Ce champ magnétique diffusé est la cause des perturbations en basses fréquences.
Le calcul de ce champ a été effectué analytiquement dans le cas de la géométrie sphérique. Les résultats de ce calcul peuvent être extrapolés aisément au cas de la géométrie parallélépipédique du coffret et des cartes.
Dans le cas de l'illumination par une onde plane, le rapport entre les champs magnétiques interne et externe (atténuation) est donné par la relation suivante :

$$\frac{H_{int}}{H_{ext}} \simeq \left(1 + j\,\frac{2\pi\mu_0 a}{3Z_s}\right)^{-1}$$

où (a) est la dimension caractéristique de l'objet (coffret ou carte) définie par :

$$a = \sqrt[3]{\text{longueur x largeur x hauteur}}$$

z_s est l'impédance de surface de la protection métallique qui est donnée par la relation :

$$z_s = 1 / \sigma.d$$

où σ est la conductivité électrique du matériau de protection et d, son épaisseur.
Il apparaît que la protection métallique se comporte vis-à-vis du champ magnétique externe comme un filtre passe-bas du 1er ordre dont la fréquence de coupure est :

$$f_c = \frac{3 Z_s}{2\pi \mu_o a}$$

Cette fréquence de coupure dépend de la taille intrinsèque de l'objet. Cette propriété sera utilisée ultérieurement pour distribuer entre le coffret et les cartes les protections contre les perturbations d'origine externe.

Il apparaît enfin que, dans le domaine des hautes fréquences, la diffusion du champ magnétique à travers les parois conduit à des champs internes négligeables. Dans ce domaine de fréquence, les perturbations internes sont dues à la diffraction des champs à travers les imperfections de métallisation, connecteurs, joints ... Ainsi, dans ce domaine de fréquences, le problème se pose dans les mêmes termes que dans le cas des coffrets métalliques. Il est associé aux aspects technologiques des modes d'assemblage.

En conclusion, la définition de l'épaisseur des métallisations nécessaires à la protection électromagnétique des matériaux composites est uniquement liée à la diffusion du champ magnétique à travers la peau de structures non infiniment conductrices.

4.3 Règles régissant la répartition des blindages entre le coffret et les cartes.

Pour une efficacité de blindage donnée, nous devons déterminer la distribution des blindages entre le coffret et les cartes qui conduit à une masse maximum. Nous supposons que le même matériau (de conductivité électrique T) est utilisé pour blinder le coffret et les cartes.
Nous notons d_r, a_r et m_r, respectivement, l'épaisseur de la métallisation de protection, la dimension caractéristique de l'objet et la masse du matériau métallique de blindage nécessaire lorsque celui-ci est placé entièrement sur la surface du coffret.
Nous notons d_m, a_m et m_m les mêmes grandeurs dans le cas où la métallisation est déposée entièrement sur la surface des capots des cartes.

L'atténuation, constante, s'écrit dans les deux cas :

$$\frac{H_{int}}{H_{ext}} = cste = \left(1 + j \frac{f}{3} \left(2\pi \mu_o a_r \sigma d_r\right)\right)^{-1}$$

$$= 1 + j \frac{f}{3} \left(2\pi \mu_o a_m \sigma d_m\right)\Big)^{-1}$$

Nous en déduisons la condition : $a_r d_r = a_m d_m$

D'autre part, le volume du coffret est égal à la somme des volumes des cartes :

$$\frac{4}{3}\pi a_r^3 = n . \frac{4}{3}\pi a_m^3$$

Ainsi, la relation entre m_m et m_r pour une atténuation donnée, s'écrit :

$m_m = m_r \times \mu^{2/3}$

La solution la moins pénalisante, en terme de masse, pour protéger les circuits électroniques internes contre une agression électromagnétique externe est donc de disposer la masse de métal protecteur en totalité sur la paroi du rack.
Cette méthode présente l'inconvénient de n'apporter aucune protection en ce qui concerne les perturbations de cartes à cartes.
Les règles générales que nous avons suivies sont donc :

- les cartes ne sont protégées que par la masse minimale de métal nécessaire pour éviter les perturbations entre-elles,

- tout le complément nécessaire à la protection contre les agressions extérieures est implanté sur le coffret.

4.4 Définition de la protection nécessaire au niveau des capots des cartes

Cette définition nécessite la connaissance de la susceptibilité rayonnée des circuits électroniques à protéger de l'émission rayonnée des circuits qui les polluent.

4.4.1 Détermination de l'émission rayonnée

Nous avons mesuré l'émission rayonnée par des cartes génériques représentatives des produits de THOMSON-CSF. Ces mesures ont porté sur le niveau d'émission et sur la distribution spatiale des sources de rayonnement à la surface du circuit imprimé.
Pour déterminer cette cartographie des sources de rayonnement, nous avons mesuré le champ électromagnétique rayonné à la surface des cartes, à l'aide du dispositif EMSCAN (Electromagnetic Scanner). Ce système, développé par la Société AMPLIFIER RESEARCH, permet, dans la gamme de fréquences 10 MHz - 750 MHz, de dresser la carte des sources d'émission avec une résolution spatiale d'environ 7 mm.

Les mesures, sur les diverses cartes testées ont montré que les sources de rayonnement sont ponctuelles.

La mesure de l'amplitude du rayonnement est faite à 1 m de la carte, conformément à la procédure définie par la norme MIL STD 462.

4.4.2 Détermination de la susceptibilité rayonnée

Il a été difficile d'effectuer des testes systématiques concernant la susceptibilité des cartes électroniques san protection, en raison du risque de destruction. Nous avons choisi d'utiliser une approche théorique qui sera explicitée plus loin.

4.4.3 Valeurs d'émission et de susceptibilité rayonnées prises en compte pour calculer le blindage des LRM.

a) Emission rayonnées

Les mesures de champ proche décrites au paragraphe précédent ont montré que les sources de rayonnement sont ponctuelles et qu'elles ont une forte composante magnétique.
Nous admettrons que ces sources se comportent comme des moments dipolaires de ces dipôles à partir des mesures d'amplitudes effectuées à 1 m de la source.

Les modules des moments dipolaires s'écrivent :

$$|\vec{P}_m| = \frac{4\pi}{k}\sqrt{\frac{\varepsilon}{\mu}}\cdot|\vec{E}| \quad \text{pour } k=\frac{\omega}{c}<0{,}7$$

$$|\vec{P}_m| = \frac{4\pi}{k^2}\cdot\sqrt{\frac{\varepsilon}{\mu}}\cdot|\vec{E}| \quad \text{pour } k>0{,}7$$

où $|\vec{E}|$ est le module du champ magnétique mesuré à 1 m.
La valeur de $|\vec{E}|$ que nous retiendrons pour calculer l'épaisseur des blindages nécessaires est la plus grande des valeurs enregistrées lors des essais : $|\vec{E}|$ = 90 dB µ V/m.

b) Susceptibilité rayonnée (approche théorique)

Nous supposons que la tension induite entre deux points d'un composant ne doit jamais excéder 100 µV. Cette tension est définie comme la tension de circuit ouvert induite par le champ magnétique à travers une bande de surface S = 10 cm²

Cette tension est donnée par la relation :

$$V = -j\ S\ 2\pi f\ |H|\ \mu_o$$

$|\vec{H}|$ est le module du champ magnétique rayonné par le dipôle magnétique défini au paragraphe précédent et diffusé par la protection métallique des capots des cartes.

4.4.4 Calcul de l'épaisseur de blindage nécessaire à la protection des capots contre les perturbations carte à carte.

Le champ magnétique rayonné par le dipôle magnétique est atténué par diffusion à travers l'écran protecteur d'impédance de surface Z_s. Cette atténuation peut être calculée, sur l'axe du dipôle émetteur, par la relation :

$$\begin{cases} S(\ell_{13}) = \dfrac{H_z(\ell_{13})}{H_{zo}(\ell_{13})} = \left(1+\left(\dfrac{3}{\delta}\right)^2\right)^{3/2}\displaystyle\int_0^{\infty}\frac{\mu^2}{\mu+j\frac{\ell_{13}}{\ell_c}}\,J_1(\mu)\,e^{-\frac{\mu 3}{\delta}}\,d\mu \\ \ell_c = \dfrac{Z_s}{\pi\mu_o\delta} \end{cases}$$

où Hz (f.z) et Hzo (f.z) sont, respectivement, le champ magnétique rayonné en espace libre et le champ magnétique rayonné par le même dipôle et diffusé par l'écran d'impédance de surface Z_s. J_1 est la fonction de Bessel d'ordre 1. L'application numérique a été effectuée en prenant en compte un pas de cartes de 15,24 mm. Elle montre que l'impédance de surface Z_s = 100 µΩ permet de ne jamais dépasser la tension critique de 100 µV sur la boucle de test. Cette impédance de surface correspond à une couche d'aluminium dont l'épaisseur est de 280 µm.

4.5 Définition de la protection métallique du coffret

4.5.1 Cas de la protection contre une onde plane 200 V/m

Le calcul est toujours effectué dans l'hypothèse où la tension de court-circuit induite sur une boucle de surface 10 cm² ne doit pas excéder 100 µV. Dans le coffret, les cartes sont au format Double Europe et sont au nombre de 40. L'épaisseur de métallisation obtenue est de 5 µm.
On remarque, conformément à ce qui a été montré plus haut, qu'il est préférable, en terme de masse, de disposer le blindage sur la paroi du coffret que sur les capots de cartes. Il apparaît que la masse nécessaire à la protection contre l'agression extérieure est négligeable. Cette constatation valide l'hypothèse de l'intérêt du choix des matériaux composites. En effet, les coffrets métalliques dont les parois étaient définies sur des critères mécaniques étaient tout à fait surdimensionnés du point de vue de la protection contre l'agression électromagnétique externe 200 V/m.

4.5.2 Cas de la protection contre l'agression IEMN

Les calculs montrent que l'épaisseur totale du blindage doit être de : 140 µm.

Le fort contenu spectral basse fréquence de l'impulsion IEMN conduit à des épaisseurs plus importantes de blindage.

Dans ce cas, l'optimisation de la répartition des blindages entre coffret et cartes est nécessaire.

4.6 Conclusion sur les blindages

La combinaison d'approches théorique et expérimentale a permis, outre la définition des épaisseurs de métallisation nécessaires sur le coffret et sur les capots des cartes, de tirer les conclusions suivantes :

- l'utilisation de matériaux composites est possible d'un point de vue électromagnétique, mais l'épaisseur des blindages doit être optimisée en fonction des agressions et des géométries rencontrées.

- le meilleur blindage, en termes de masse et de performances, est obtenu en répartissant la métallisation entre le coffret et le capot des cartes qui y sont installées.

4.7 Mesure de la qualité électromagnétique des éléments métallisés avant assemblage

L'objectif est de déterminer le paramètre le plus pertinent pour évaluer l'atténuation apportée par un matériau donné avant fabrication d'un coffret : ce point est particulièrement vrai dans le cas des composites où plusieurs types de métallisation peuvent être utilisés. en d'autres termes, il est essentiel de connaître la meilleure métallisation pour une application donnée et ensuite de contrôler les lots de fabrication de composites métallisés avant assemblage.
Comme on a pu le voir dans le chapitre consacré au calcul des atténuations, le paramètre clé est l'impédance de surface Z_s, qui est le rapport entre le champ électrique E dans le matériau et la densité de courant surfacique J :

$$Z_s = \| E \| / \| J \|$$

ou encore, en fonction des caractéristiques du matériau :

$$Z_s = 1/ \delta.d$$

où δ est la conductivité du matériau et d, l'épaisseur. Le grand intérêt que présente ce paramètre est qu'il est facilement mesurable à l'aide d'une sonde développée à cet effet. Cette dernière est constituée d'une bobine de réception. La méthode consiste à émettre un champ magnétique perpendiculaire à la paroi du matériau à tester, la boucle de réception pouvant être placée, au choix, d'un côté ou de l'autre du matériau à tester. La mesure consiste à effectuer le rapport de la tension recueillie à la tension aux bornes de la bobine d'émission. Chacune des courbes obtenues se caractérise par une fréquence de coupure à - 3 dB, à partir de laquelle est déduite la valeur de l'impédance de surface.

L'ANNEXE C présente les courbes obtenues pour trois types de métallisation. Les valeurs mesurées sont les suivantes :

- matériau N° 1 : F_c à - 3 dB = 12,7 kHz ,
  Z_s = 1,15 mΩ ,

- matériau N° 2 : F_c à - 3 dB = 53,3 kHz ,
  Z_s = 4,85 mΩ ,

- matériau N° 3 : F_c à - 3 dB = 488 kHz ,
  Z_s = 44,4 mΩ ,

L'atténuation évoluant avec l'inverse de l'impédance de surface, le meilleur blindage est obtenu avec le matériau N° 1.
Comme on le voit, cette méthode est extrêmement simple de mise en oeuvre et permet rapidement de caractériser divers types de métallisation.
Il est clair que le choix final est un compromis entre les qualités électromagnétiques, la facilité de réalisation de la métallisation et la tenue de cette dernière aux environnements autres qu'électromagnétiques.

5. CONCLUSION

La phase ultime du développement du coffret en matériaux composites et des capots de protection en matériau thermoplastique a consisté en une qualification globale. En effet, chaque brique technologique de base a subi une qualification propre et la dernière étape consiste à tester le boîtier complet.

La première partie de la qualification a porté sur la confirmation des performances électromagnétiques. Pour cela, le coffret est illuminé successivement par une onde plane (14 KHz - 18 GHz) et par une onde IEMN et l'atténuation apportée par le blindage est mesurée. Pour l'illumination par l'onde IEMN, THOMSON-CSF/RCM est doté d'un équipement permettant d'illuminer un objet de dimension caractéristique de l'ordre de 1 m. Cet équipement comprend une cellule de Crawford (illuminateur) et un générateur 200 kV à faible temps de montée (source). Les atténuations obtenues sont tout à fait conformes aux résultats des calculs menés précédemment.

La seconde partie a porté sur la qualification dans les environnements autres qu'électromagnétiques : cette phase n'a posé aucun problème.

La principale conclusion de ce développement est que le coffret vole, depuis plusieurs mois, sur avion d'armes.

Cette étude a permis de montrer que l'étude d'un coffret en matériaux composites ne peut pas se dérouler suivant le même processus qu'un coffret métallique. Il est impératif de :

- prendre en compte les aspects de compatibilité électromagnétique très en amont afin d'étudier précisément les agressions externes et d'adapter les blindages nécessaires pour optimiser la masse.

- concevoir le coffret pour utiliser au mieux les propriétés mécaniques des composites et de minimiser les surcoûts.

- mettre en place des méthodes de contrôle simples des métallisations avant assemblage du coffret afin de prévoir, dans le cycle de fabrication, la qualité finale d'un point de vue électromagnétique.

- prévoir l'intégration du coffret sur le porteur en prenant en compte sa spécificité (à titre d'exemple, la mise à la masse du coffret doit se faire au plus près du connecteur afin d'éviter toute circulation de charge sur le coffret).

DISCUSSION

Question: What metallizations were used on the racks and covers? Metallization often peels up after aging; was this tested?

Answer: Several possbilities have been investigated in terms of their shielding effectiveness; electrical conductivity; resistance to contaminants, humidity [and] salt mist; and metallization/composite liaisons. The best solutions were obtained by mixing several layers of metal deposition. An effort has also been placed on the use of paint to avoid peeling effects. The best techniques were vacuum deposition and [a] galvanic one.

Question: The NATO goal is to have a small set of common modules used on many platforms in different nations. Since the choice of rack materials depends strongly on the platform environment, is it sensible to have a standard family of racks given the wide variation in platform environments?

Answer: It is more important to reach a common module family than a rack one. The latter could be adapted to the platform and the number of LRMs that must fit in.

Question: Environmental sujects become more important. So did you investigate getting rid of the composite material or will it last forever?

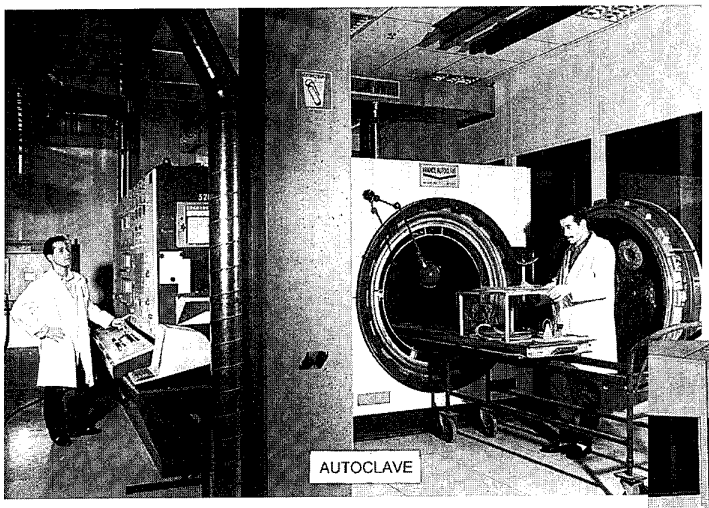
Answer: This question was not the main driver of the development. Nevertheless, the materialsw used are classical and non-toxic: resin and long carbon fiber.

Question: With the concerns of wear and damage, were any other types of shielding considered? (Examples: metallized fibers or metal layers in the composite material.)

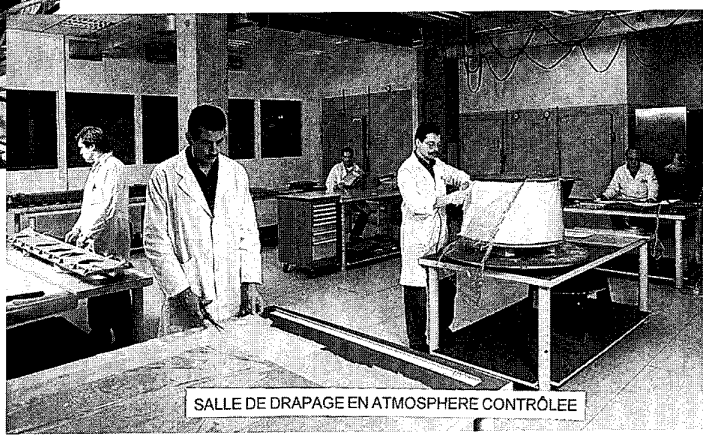
Answer: We have tested several types of possible metallizations including one-sided (internal) shielding, multilayer structures (composite-metal-composite), and double-sided. A trade-off analysis, taking into account criteria such as metal deposition capability, ease of manufacturing, and cost, has concluded that the best compromise is the double-sided shielding, with a specfic paint on the external parts.

Question: How long has your rack been flying on an aircraft?

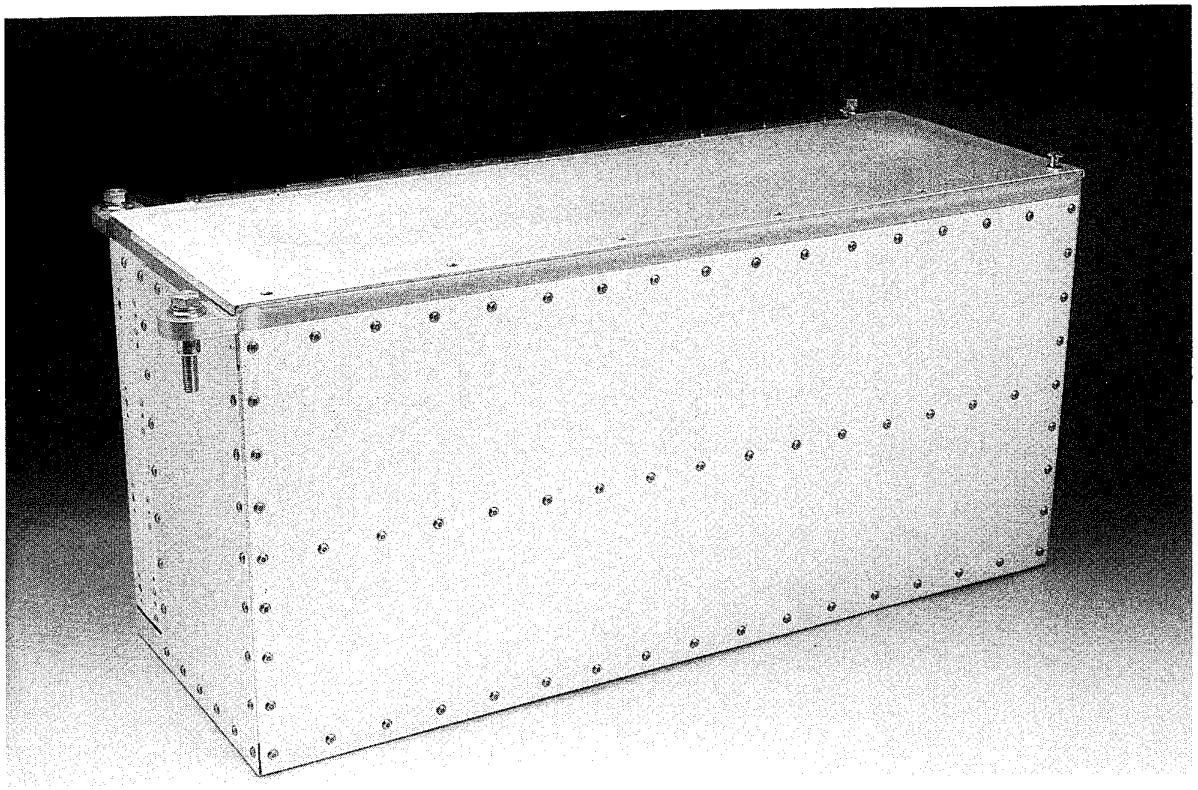
Answer: One year.



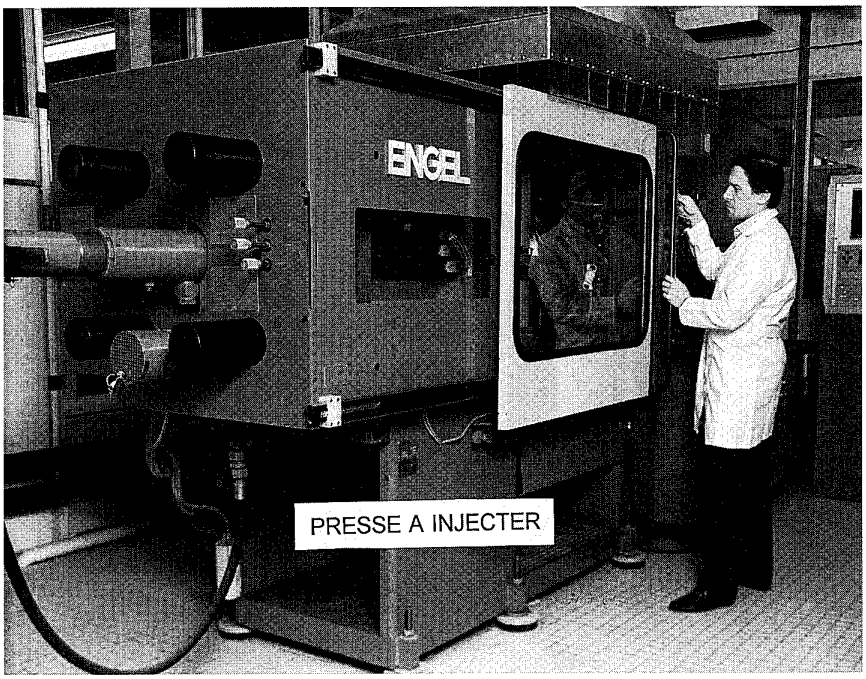
ANNEXE A1



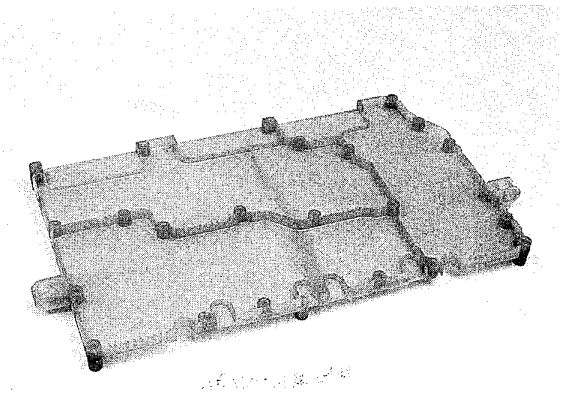
ANNEXE A2



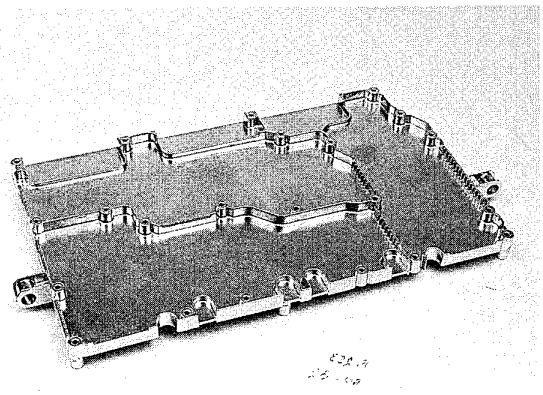
ANNEXE A3



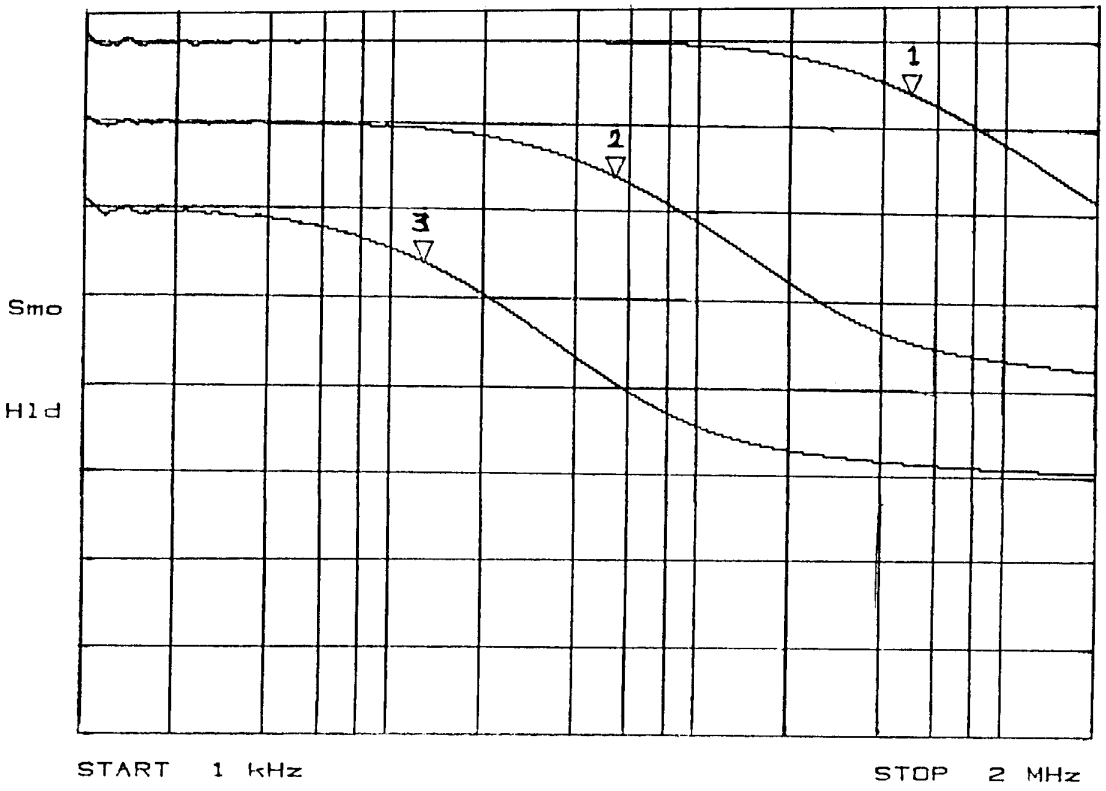
ANNEXE B1



ANNEXE B2



ANNEXE B3



ANNEXE C : Méthode de mesure de l'impédance de surface Z_s. Courbes obtenues pour 3 métallisations différentes.

LIGHTWEIGHT ELECTRONIC ENCLOSURES USING COMPOSITE MATERIALS

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SUMMARY

The ever increasing demand in technical and economical performances improvement of aircrafts has a direct incidence for avionics.

Except microelectronic integration, the enclosures have a high potential of evolution.

The main advantages of composite materials over metals in forming electronic enclosure are :

- reduction of weight (min 30%),
- better resistance to corrosion,
- improved fatigue and impact resistance,
- achievement of complex shapes,
- low coefficient of thermal expansion.

The main problems to be solved in extending the application of the use of composite materials to the field of airborne electronic equipments are to :

- provide adequate electromagnetic shielding,
- ensure survival in harsh thermal and mechanical environments,
- achieve global competitivity of the final products.

Different technologies have been considered :

- injection molding of short fibers reinforced thermoplastics for small sized equipments (V < 2 l),

- pressure molding of graphite and glass reinforced thermossets for ATR case families,

- metal matrix composites.

This paper will address the main investigations that have been undertaken in France since 1986 in the two first fields covering both manufacturing and evaluation results.

This studies have been undertaken through the French Industrial Aerospace Association (GIFAS) and have been supported by the Technical Department of Aeronautical Programs (STPA) of the French Ministery of Defense (MOD).

1 - INTRODUCTION

1.1 GENERAL ASPECTS

Airframer are insisting more and more on the factors that define the technical and economical performance of airplane and helicopters; this effort must particularly consider weight and cost reduction of avionics packaging.

In some cases the sum of unfolded enclosures walls might cover the whole aircraft structure with an aluminium layer.

The new generation of aircraft make extensive use of composite materials for the structural parts, the franco-german helicopter Tiger is said to be "all composite ", in such conditions the pressure in extending the use of composite materials to the avionics housings is very important.

The other constatation promoting for the use of composite materials as electronic housings is the place taken by these materials in the telecommunications, computer and houseware markets.

1.2 WHY TO USE COMPOSITE MATERIALS

The succes of composite materials in the aerospace field is justified due to their advantages :

- reduction of weight (≈ 30%)
- hight stiffness and strength
- high field strength
- improved fatigue and impact resistance
- insulating electrical properties
- tailorable coefficient of thermal expansion
- better resistance to corrosion, chemicals and fluids
- greater design freedom
- lower energetical content.

The drawbacks limiting a wider use of the materials in the field of avionics are :

- degradation of mechanical properties in case of geometrical abrupt change
- long term behaviour (humidity, UV)
- bad thermal and electrical conductivities
- possible galvanic corrosion with graphite

All these problems have to be taken into account when designing avionics enclosures in such a way as to :

- ensure survival in harsh thermal and mechanical environments
- provide adequate electromagnetic shielding
- achieve the global competitiveness of the end products compared to ones existing in metal.

1.3 DESCRIPTION OF THE STUDIES

A preliminary French MOD contract in 1986-1987 has permitted SEXTANT to :

- define the specific needs and material characteristics necessary for avionics applications
- analyze products available on the market
- establish the future and additional investigation work to be undertaken.

The main conclusions of this first study was to divide the applications of composite materials to avionics in two families :

- small sized equipment (V ≈ 2l depending on shape) made out of short-reinforcement injected thermoplastics.

- larger sizes, like standard ATR format cabinets using long fiber reinforced thermosets.

Following the Sextant recommendations, the two lines of thought axis have been investigated simultaneously.

The studies on thermoplastic small sized equipment followed up by Sextant will be presented first. For the second area (standard ATR case), a national committee was created through the French Industrial Aerospace Association (GIFAS) with the main airframers and equipment builders in order to establish a common specification, anticipate a larger scale production and limit the individual expenses among the different companies.

The specifications, selected technologies and evaluation result are developed in the second part of this paper.

The future developements in both areas and the new coming technologies are discussed at the end.

2 - AVIONICS ENCLOSURE REQUIREMENTS

Depending of the type of aircraft (fighter, transport or helicopter) and the location of the equipments inside the airframe, different levels of constraints are defined.

These requirements are defined by regulations and standards concerning the main following aspect :

- format and size definition
- maximum allowable weight
- structural dynamic behavior
- thermal requirements
- electromagnetic aspects
- fluid and chemical contamination
- fire resistance
- moisture resistance

The three reference regulations are :
MIL STD 810E, AIR 7306 and DO160.

The establisment of a single worst environmental requirement covering all the cases is not possible without making overspecification,

The objectives of the requirements document is first to list the maximum constraints envelope and then to establish the evaluation program based on a representative operational environment.

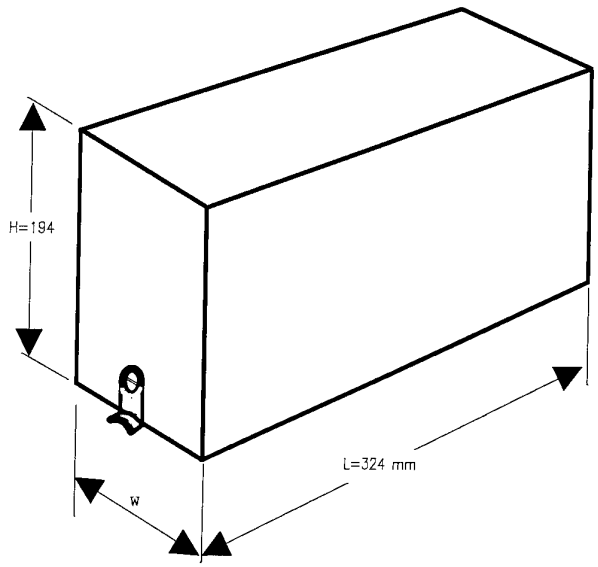
2.1 FORMAT, SIZES AND WEIGHTS

Three main families are identified :

- instrument panel
- standard equipment
- special equipment

Among the first type, eight sizes are defined, five of which have a volume lower than a liter (NFL 70.120).

The standard equipment is defined by the ARINC 600 regulation from 1 to 12 MCU (Modular Concept Unit) or equivalent ATR sizes. For this modular equipment, two dimensions are defined (L = 324 mm, H = 194 mm) and the front thickness varies from 25.4mm (1 MCU) to 388.3mm (12 MCU).



The special equipment not included in the two previous types is installed in areas where volume and shape must be adapted to the aircraft.

The ARINC 600 defines for each standard size a maximum allowable weight going from 2.5 kg (1 MCU) to 20 kg for a 12 MCU.

2.2 STRUCTURAL DYNAMIC BEHAVIOR

The selected values for the evaluation program are :

- constant acceleration	15 G
- harmonic vibrations	2.5 G
- random vibrations	0.02 g^2/Hz (90min /axis)
- shocks	30 G 9ms (3shocks /axis)
- crash	40 G 9ms

2.3 CLIMATIC CONSTRAINTS

2.3.1 Thermal constraints

In this case two types of requirement are necessary, depending on the heat generation source, which can be of :

External origin :

- low and high temperatures are defined by the geographical location of the aircraft
- or defined by the location inside the airframe (engine, skin, etc.)

Internal origin :

- In this case, the enclosure must provide a good thermal path with low thermal resistance between the components and the airframe structure.

The applicable temperatures for the evaluation program are :

- storage	-55°C	+95°C (72 hrs)
- thermal cycling	-55°C	+95°C (3 cycles)

For the dissipation of internal heat generation, three options are foreseen :

- forced convection : in this case the pressure drop must not exceed 25mm of water for an air flow of 18g/s in ground conditions.

- low local thermal resistance areas for the location of high power dissipating devices.

- in case of closed equipment where no convection is possible due to air tightness, the wall's intrinsic conduction must be improved and high thermal conductivity materials must be selected.

The evaluation program will only consider equipment with convection exchange, whether forced or natural, where material conductivity is of minor importance.

2.3.2 Salt spray

Specification 5% Nacl 35°C 96 hrs.

2.3.3 Contamination resistance

The selected aerospace "fluids" and operating condition are :

- fuel	50°C 24hrs	+65°C 165 hrs
- mineral hydraulic fluids	85°C 24 hrs	+65°C 165 hrs
- synthetic hydraulic fluids	120°C 24hrs	+65°C 165 hrs
- mineral lubricants	70°C 24 hrs	+65°C 165 hrs
- synthetic lubricants	150°C 24 hrs	+65°C 165 hrs
- solvents	23°C 15 hrs	+23°C 1 hrs
		+50°C 6 hrs

The test will be made on shielded samples (20x50mm).

2.3.4 Moisture resistance

Resistance to fungus development specified in AIR 7306, part 13 : duration 28 days.

2.4 FIRE RESISTANCE

Fire and flame resistance are evaluated on 115 x 320 x 2.5 mm samples following the FAR 25 Amdt 25.72, part I, and JAR 25 App., part I, regulations.

The material must be auto-extinguishable. Flame must not keep on burning 15 sec. after source flame stops.

2.5 ELECTRICAL AND ELECTROMAGNETIC REQUIREMENTS

To prevent poor electrical contacts between the different parts of the equipment and also to prevent electrostatic discharge, a minimum resistance value is specified :

- between connector ground reference and any other structure contact point,
- between any two points of the structure.

The measurement is made with a current of 10 A and the resistance must be between 0.5 and 10 mΩ depending on the required severity level. The typical value selected is 2.5 mΩ.

The second important aspect, since composite materials are low conductors, is the electromagnetic shielding.
Electromagnetic emission and susceptibility requirements for the control of electromagnetic interference are defined in MIL STD 461 and AIR 7306.
These specifications are applied to the final equipment, with the electronic functions inside. For the evaluation program, a shielding effectiveness of 65dB has been stated for the radiated electromagnetic fields (RFI).

3 - SMALL SIZE ENCLOSURES

Avionics enclosures are complex three dimensional structures containing bulkheads and precisely referenced mounting interface. They must fullfill all the defined requirements for a long period of time (over 20 years).
The new added requirements are weight and cost reduction.
Among the manufacturing processes able to produce near net shape 3D structures at low cost, the best suited is thermoplactic injection molding. One limitation of the technology is the use of materials with short fiber reinforcements that do not meet the stiffness requirements and dedicate the process to small and medium size housings. Although avionics enclosures are not elements for transmitting efforts, they must have high mechanical characteristics to prevent the occurrence of low frequency resonant modes.

During the preliminary phase, two types of housing have emerged :
- standards modular cases
- special ones.

All standard modular cabinets have a minimum lateral dimension of 324 x 194mm, which is a limit for short fibers, but among instrument panel and specific boxes small volumes can be identified. The anticipated reasonable limit is around 2 liters with regular shape.

3.1 PRELIMINARY THERMOPLASTICS SELECTION

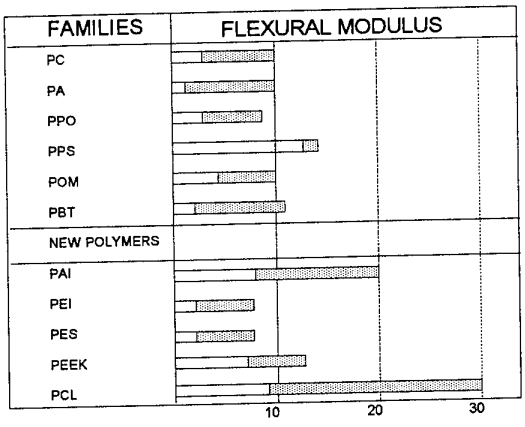
The products available on the market place have been analyzed for the following properties.

Thermal
- Heat deflection temperature at 1.82MPa
- Coefficients of linear thermal expansion

Mechanical
- Flexural modules
- Tensile strength
- Izod impact, notched

Physical
- Specific gravity
- Water absorption at 24 hours

Economical - Approximate price / kg



The higher performance thermoplastics have been compared using the above criteria. The resulting polymers selected were :

- PPS (Polyphenylene sulfide)
- LCP (Liquid crystal polymers).

PPS because apart from its excellent characteristics, it was already successfully used within the company (industrial component subsidiary), and LCP because it was new and had promising exceptional properties.

- Self-reinforcing polymers
- Exceptionnal strength, stiffness and toughness
- High thermal stability
- Inherently flame retardant
- Excellent chemical resistance
- Low tailorable CTE
- Dimensionally stable
- Low melt viscosity.

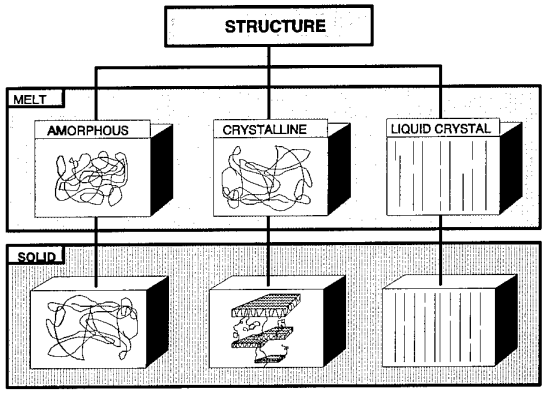
3.2 LIQUID CRYSTAL POLYMERS STUDIES

After the preliminary selection phase, the decision was made to launch a full evaluation program on the production of small size avionics enclosures using LCP based on :
- LCP grade selection
- electromagnetic shielding process selection
- assembly sub-techniques
- mold design and transformation process
- equipment evaluation (thermal, mechanical, shielding)

3.3 LCP GRADES SELECTION

3.3.1 What are LCPs ?

The origin of the name "liquid crystal" comes from their structure, which is intermediate between amorphous liquids, with a random molecular orientation, and crystalline solids, which are perfectly ordered.



The molecular chain is composed of a series of central rigid sections linked with flexible end groups. This rod-like structure gives a high degree of order in the melting state, producing a fibril structure which is frozen in solid state, giving the material the appearance of wood.

There are two kinds of liquid crystal polymers :

- lyotropic LCP produced from a solution (Kevlar aromatic polyamide fiber)
- thermotropic LCP that becomes liquid cristalline upon heating and can be processed by injection molding.

The moldable LCP are also called self-reinforcing polymer because when injection-molded " neat " or without reinforcing fibers, these aromatic polyester thermoplastics typically provide strengths equivalent to 30% fiber reinforced other technical polymers.

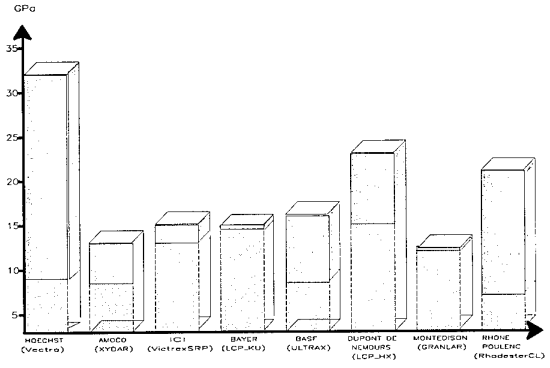
The resulting physical properties of the LCP are highly anisotropic and also strongly dependent on the thickness of molded parts.
This phenomenon is explained by the multilayered structure of the parts, composed of a skin with polymer chains oriented in the flow direction and a core with a perpendicular orientation.
The molecular structure is also responsible for the presence of weak weld lines when two melt fronts join.

3.3.2 LCP resin comparisons

During 1989-90 (LCP program) a number of resin producers were identified as potential sources for LCPs. They include Hoechst, Amoco, ICI, Dupont, Bayer, BASF, Montedison and Rhone Poulenc. Some other firms in Japan, the USA and Europe were also beginning developments on LCP. Today, only a few of them are still active in that area.
To select a grade or a family of products fulfilling the avionics requirements, the following list of properties was examined :

- specific gravity
- flexural modulus
- tensile strength
- heat deflection temperature at 1.82 MPa
- coefficients of thermal expansion in the flow and transverse direction.

The industrial aspects were also taken into account, through the annual production capacity.



The examination of all the data and the availability of the products on the market has resulted in the selection of a family of Vectra LCP from Hoescht for the subsequent analysis steps.

3.4 ELECTROMAGNETIC SHIELDING

After the LCP grade selection, the next important problem to solve was the selection of a compatible shielding treatment and the associated performance evaluation method.

3.4.1 Description of the shielding approach

The shielding effectiveness of the housing to the external electromagnetic aggression depends on the intrinsic characteristics of the materials (permeability, conductivity), the physical shape and size of the material, the characteristics of the field, and the distance between the source and the material.

The energy can penetrate inside the enclosure through different mechanisms :

- Diffusion of the fields through the openings (may or may not be protected by grid) for air circulation for example.

- The coupling through the walls which are not perfectly conductive (composite materials).

- The coupling through the imperfections of the mechanical junctions (covers, connectors).

- The direct coupling on the input/output cables (conducted interference).

Test methods used by manufacturers are not similar and the published results are difficult to compare.

The selected approach is to :

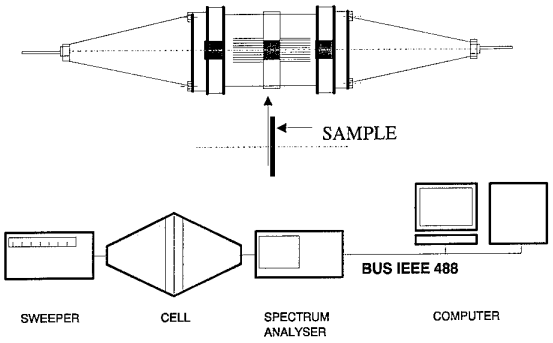
- make a relative shielding effectiveness measurement on samples,

- select the most efficient process,

- test the end product with the specified requirements.

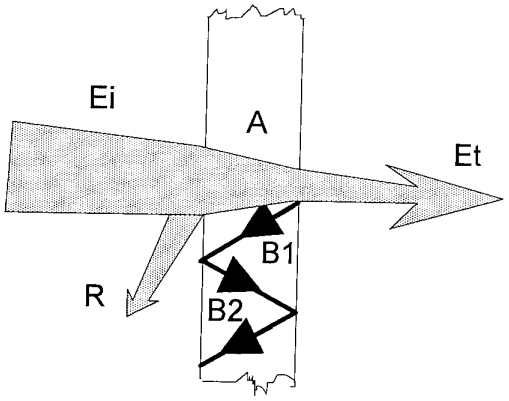
3.4.2 Shielding effectiveness measurement

Along the various existing methods, the coaxial transmission line will be used.



This method is not affected by external conditions. A 100mm circular plate is introduced in the sample holder and a scan is made from 10 MHz to 1Ghz.

The basic shielding equation SE = A + R + B shows that shielding effectiveness is equal to the sum of absorption (A), reflection (R) and re-reflection (B) losses, and is given in dB as the attenuation of the electromagnetic field strengh.



The measured SE = 20 log 10 $(\frac{Ei}{Et})$.

Where Ei is the incident field strength in µV/m and Et is the transmitted through the wall.

3.4.3 Shielding methods and materials

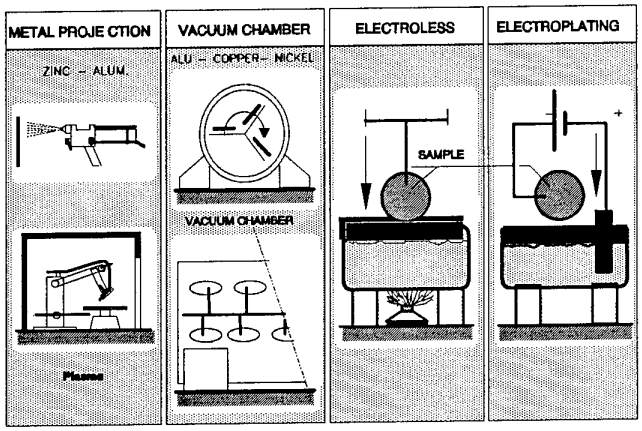
Numerous processes are available for plastic shielding and the selection of the most appropriate method for LCP must take into account :

- shielding effectiveness (minimum 70 dB)
- compatibility between coating and LCP
- adhesion on the substrate
- compatibility with environment specifications (climatic, thermal, mechanical)
- overal cost (material, equipment, labor)

The evaluated process are :

- melted metal projection by flame, arc or plasma
- vacuum deposit (evaporation and sputtering)
- electroless immersion plating
- electroplating
- conductive paints

LCP with conductive fillers (aluminum flakes, stainless steel) were not available.



Melted metal projections

This process uses flame or arc guns to project pure metallic coatings of zinc or aluminum.
Typical coating thicknesses are between 50 et 100µm.
The heat involved with flame is larger and is high enough to warp thin walled parts. The use of the automated plasma projection technique is dedicated to very high temperature melting materials.
This technique is cost effective, but the deposited surface is not very pretty and can lead to inconsistent shielding and flaking off of conductive particles on the electronic components.
The thickness is difficult to control and the process is also considered as dangerous to health and the environment.

Vacuum metallization

Thin layers of some microns are obtained by evaporation. In the sputtering technique adhesion is improved due to the higher energy levels involved.
The deposition being a "straight" line process, the parts must be moved during operations involving expensive equipment. The time to reach the vacuum level required in the chamber is also a limitation.

Electroless plating

Copper and nickel are deposited in immersion baths. The electroless nickel layer is corrosion and abrasion resistant.
The film thickness (a few microns) is uniform, but covers both internal and external surfaces, which may not be desirable (painting needed). For Vectra LCPs, grades having a good chemical resistance, a particular plating process is provided by Hoescht.

Electroplating

Before galvanic depositing the surfaces must be prepared so as to become conductives.
The location of the electrode must be selected to prevent visible coating damages.
The resulting thickness of copper or nickel deposit (10 to 100µm) is not uniform.
Electroless and electroplating processes can be combined.

Conductive paints

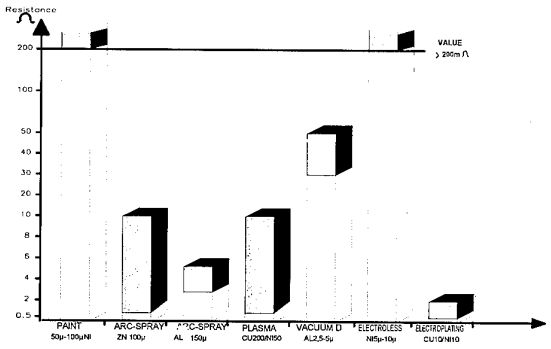
This process is by far the most important in volume.
The paints are composed of conductive materials - nickel, copper, silver and graphite - in acrylic or urethane binder systems.
This low cost and easy to use process gives typical coating thickness of 50 to 100 µm.

3.4.4 Shielding performances

The performances evoluation program was composed of the following steps :

- resistance measurements,
- shielding effectiveness measurement :
  - "adhesion test"
- thermal cycling
  - "adhesion test"
- salt spray
  - visual check.

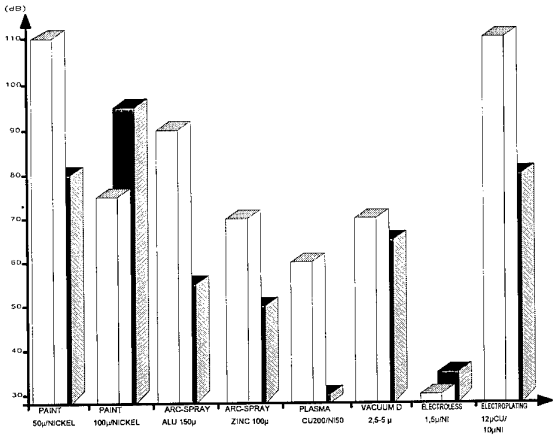
The surface resistance measurement results exhibited three processes fulfilling the 2.5 mΩ requirements :



- melted metal projection (arc and plasma)
- electro-plating (10 µCu + 10 µNi).

The other conclusion is that for the painting systems the resistance is > 200 mΩ, due to the non-metallic binder resistivity.

The shielding effectiveness results given by the transmission line method show that a lot of shielding processes can fullfill the requirement of 60-70dB.



Finally, after environment and adhesion testing, electroplating of copper and nickel was selected with a final thickness adjusted to the requirements and specificities of the integrated electronic functions.

3.5 TECHNOLOGICAL ASPECTS

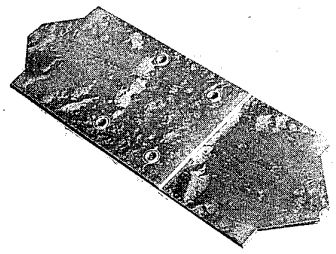
The change from metallic to composite technology will only be possible if all the requirements can be fulfilled at a satisfactory price.

For injection-molded parts, this means near net shape with minimum machining.

But at prototype stage or for a limited number of items of equipment, some modifications may be necessary.

To solve these problems the following assembly sub-technique has been evaluated with LCP :

- Adhesive bonding
- Ultrasonic welding
- Thermal and friction welding
- Inserts
- Machining.



In so far as concerns bond strength evaluation, 2 different Vectra grades were tested with different reinforcements (glass fibers and mineral) and four different adhesives. The tensile tests were conducted after thermal shocks (100 cycles, - 55°C, +125°C) and relative humidity (95%, 50°C, 240 hrs).

The selected adhesive systems are 1 part epoxy and 2 part acrylics.

All the other investigations on technological aspects (ultrasonic and thermal welding, insert mounting and machining) have provided good results after the necessary parameter adjustments phase.

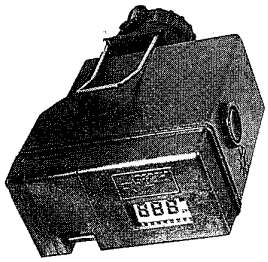
3.6 CONCLUSION FOR SMALL SIZE THERMOPLASTIC ENCLOSURES

Preliminary studies have established the general specifications for airborne electronic enclosures and some candidate thermoplastics have been selected.

LCP and particularly the Hoescht Vectra family, has proved to be an excellent candidate for the substitution of small metal boxes.

The study has brought solutions to the main problems, particularly the shielding aspects. Economic analysis shows that above some hundreds parts (depending on complexity) the thermoplastic solution is worthwhile.

Since this study, the Sextant has successfully produced thousands of small equipment items (DDIs) using LCPs.



4 - STANDARD EQUIPMENT

4.1 PROGRAM ORGANIZATION

As described in the introduction for larger size enclosures, defined by standards (ARINC 600), a committee was created in the GIFAS organization, with the objective of harmonizing the French national effort on composite materials applied to avionics.

The maximum size of such a standard housing is 12MCU (24liters), and can be compared to airframe structure, the natural tendancy has therefore so been to select the same manufacturing materials and processes, meaning thermosets reinforced with glass and long graphite fibers.

The committee is composed of the main airframers (Dassault Aviation, Eurocopter, Aerospatiale) and equipment manufacturers (Dassault Electronique, Elecma, Sextant, Sfim, Souriau, Thomson, Vibrachoc).

The responsibility for different phases of the study was distributed among the participant companies as follows :

1989	Harmonized technical requirement document (Sextant)
1989	Call for tender among the french composite manufacturers (Sfim).
1990	Development and manufacturing of the prototype (Sextant + Sfim).
1993	Evaluation phase (Dassault Aviation and Dassault Electronique)

4.2 REQUIREMENTS AND DEMONSTRATOR DEFINITION

The requirements are the same as for the small enclosures described in chapter 2. The added specifications are the characteristic of the selected technological demonstrator.

- Enclosure size	6 MCU (3/4 ATR)
- Rear panel	connector DOD C 83527, size 2
- Max weight (empty)	1.4kg (without connectors and locking devices)
- Max. weight equited	15 kg
- Max. power dissipation	300W
- Rack interfaces :	
. lower face	AER 310
. front panel	ARINC 600 (optional)
- Carrying handle	AER 310 or integrated

The objectives in terms of weight reduction are 30%.

4.3 SELECTED TECHNOLOGIES

Among the 13 proposals two were selected by the committee for the development phase.

4.3.1 Plastiremo concept

Molding method

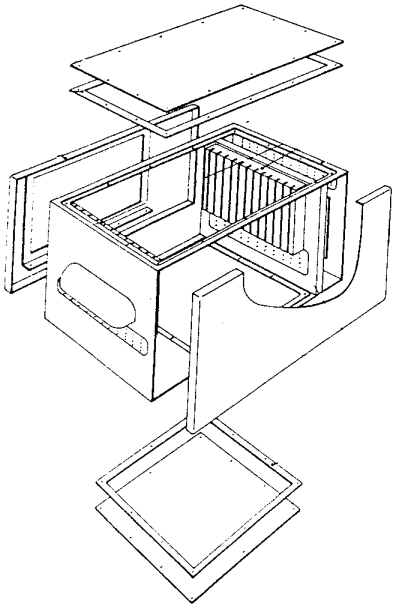
Plastiremo has been involved for 40 years in the molding of composite parts with high fiber ratios. The key element of the technology lies in the design of the tools composed of many movable components operated by a multidirectional press. Complex structures using glass and graphite fabrics or epoxy resin prepreg are possible with such a process.

The high fiber loading is obtained through a 25 bar pressure on the metal mold.

Modular design of the enclosure

The cabinet is composed of a central frame with four faces :

- front panel (handle)
- rear panel (connector)
- top face (open for card access)
- lower face (locking mechanism, access panel).



The two side walls are molded separately, then glued on to the central frame.
The advantage of this design is that it is modular. In case of a change in size only the central mold part is changed to get the right width.
The internal bulkhead holding the card-guides is a sandwich honeycomb screw-mounted to the walls.

Electromagnetic shielding

Technical and economical Plastiremo trade-offs on shielding processes have shown that copper and nickel coatings on both internal and external surfaces was a good compromise.

Seven microns of nickel are protecting the conductive copper layer against corrosion. The coating weight penalty is 175 grams and the electrical resistance between any two points of the structure is 1.5 mΩ.

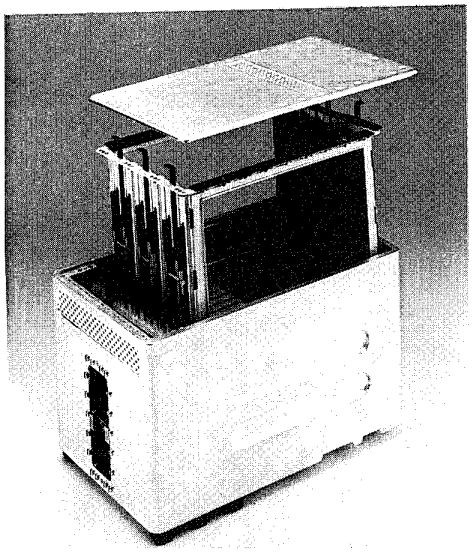
Conclusion

The advantage of the technology is to get a 30% weight reduction compared to aluminum coatings and to provide tight tolerances of the end product.

4.3.2 Alkan concept

Enclosure design

The structure is monolithic with integrated side panels.



The cards are located in a card frame linked to the structure by screws in the upper side and pins guides on the bottom.

The advantage of this design is :

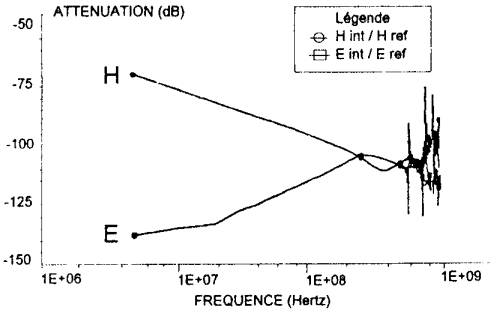
- aperture minimization for electromagnetic shielding,
- possibility of filtering the mechanical vibrations between the frame and the external structure.

The vacuum bag and autoclave molding processes are used with carbon epoxy prepregs. Composite card guides have also been proposed with an integrated locking mechanism. The operating principle of these card-guides is based on the flexibility or thin carbon layers.

Electromagnetic shielding

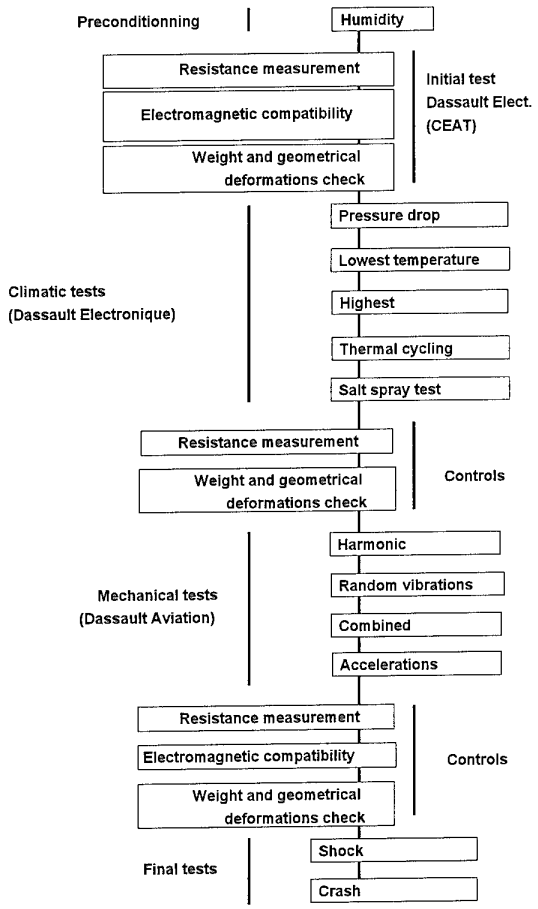
Various coating methods have been evaluated by Alkan and silver electroplating has been considered to be a good compromise between shielding effectiveness / resistance requirements and weight penalty.

The Alkan estimated resistance was around 0.6 mΩ and the measured electromagnetic attenuation in the electrical field was above 65 dB.



4.4 EVALUATION PROGRAM

Three demonstrators for each technology were submitted to the following test program :



Part of these tests were carried out by the MOD Laboratory, CEAT in Toulouse including the tests specimen representatives of the two technologies :

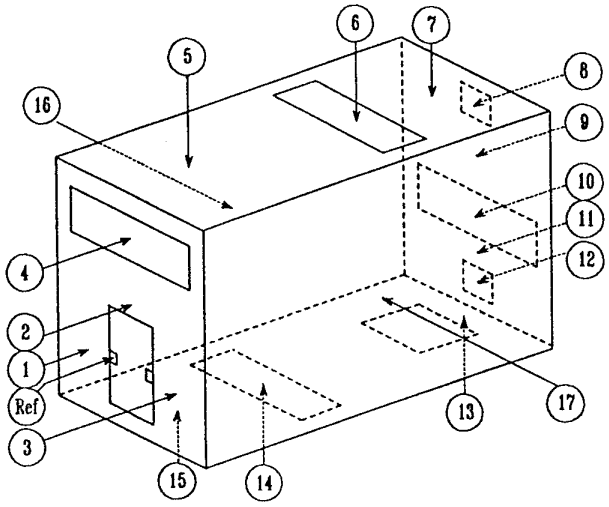
- Impact tests
- Contamination resistance
- Fire resistance
- Moisture absorption
- Painting adhesion.

4.5 RESULTS

Humidity : start of corrosion on screws and coatings.

Temperature storage and thermal cycling :
no change,
- a weight change of ≈ 10 grams was observed on both technologies .

Bonding path resistances :
- The measurements were made between the connector and 17 points distributed on the enclosures.



The following table shows that the resistance results are compatible with the requirements, with minor interface improvements to be made between the cover and the frame in the Plastiremo structures.

	Initial test	Humidity (750 hrs)	Climatic tests	Final tests
ALKAN	R<2.5mΩ R <1mΩ (except 2 points)	R<2.5mΩ R<1mΩ (except 3 points)	R<2.5mΩ	R< 2.5mΩ
PLASTIREMO	R<2.5mΩ	R<2.5mΩ	R<2.5mΩ (except 2 points)	R<2.5mΩ (except 2 points)

Salt spray test :

For a total duration of 240 hrs observations were made every 24 hours.

On both technologies, corrosion initiations were observed due to :
- a lack of thickness of the nickel layer
- galvanic corrosion between the cadmium connector and the metal coatings.

Presence of oxidation was also detected on screws.

Solutions can easily be found for these problems by a better selection of screws (high quality stainless steel), compatible connector materials and, overall, by painting the equipment.

Mechanical tests

The advantage of composite materials is to provide a higher intrinsic damping ratio resulting in lower transmissibility factors and better dynamic behavior. No major problems were detected during vibrations, and a structure transmissibility factor of around 5 was measured.

Electromagnetic compatibility

The final tests are still under evaluation but initial measurements showed electromagnetic attenuations > 65dB for the electrical field for the two technologies.

CONCLUSION

The two programs on thermoplastic injection-molded and larger-size ARINC enclosures, being carried out in France since 1987, have demonstrated that light-weight advanced composite was a viable alternative to aluminum for avionics housings.

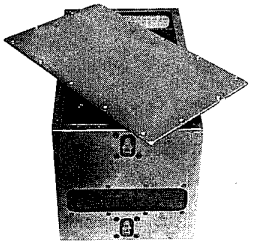
In both cases the weigh reduction objective of 30% was reached and the environment and EMC requirements were met.

Small thermoplastic equipment is already under production, and for standard enclosures, flying tests will be launched in the near future.

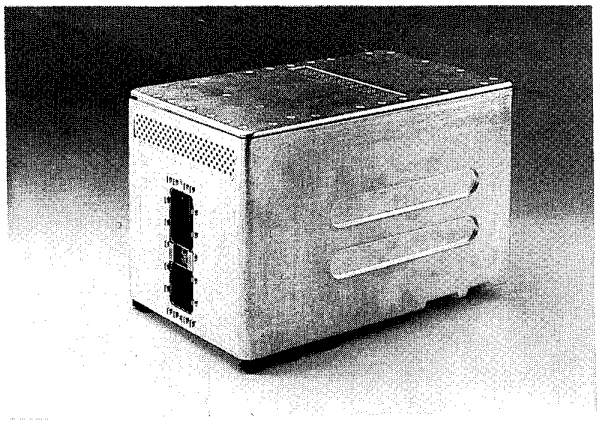
Future developments that Sextant has planned in the previous areas are :

- use of LCP blends to improve the characteristics of thermoplastic enclosures.
- investigation of metal matrix composite materials, which do not require shielding and thermal treatments
- improvement of polymeric composite processes via, cost effective new routes.

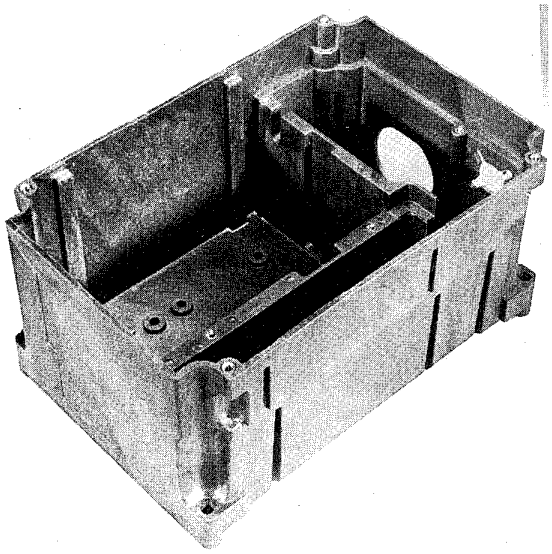
The last two areas should be included in a future European research program (EUCLID).



PLASTIREMO : 6 MCU



ALKAN : 6 MCU



SEXTANT : PRESSURE SENSOR UNIT LCP

DISCUSSION

Question: Given the lower thermal conduction of many composites and the trend to higher power dissipation per module (50 - 100 W or more), is it your feeling that liquid cooling or other methods would be needed with composite enclosures?

Answer: For low disspation enclosures, forced air cooling can be selected because this technology is material-independent. For higher power dissipation, liquid flow through and preferably heat pipes are necessary at the module level. The edge [heat] exchangers at the rack level shoul probably in this case use metal matrix composite.

Alimentations modulaires pour une architecture distribuée

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RESUME

Les futurs systèmes de l'avionique seront basés sur une architecture modulaire dans laquelle chaque fonction élémentaire correspondra à un module remplaçable en ligne (LRM : Line Replaceable Module). Des études paramétriques, telles que FASTPACK [1], ont montré que la solution optimale pour les réseaux d'alimentation était une architecture distribuée à un seul étage de conversion d'énergie, c'est-à-dire une alimentation modulaire sur chaque LRM capable de délivrer 50 W à 100 W directement à partir du réseau d'alimentation principal (270 V_{DC} ou réseau triphasé 200 V/400 Hz redressé).

Afin d'être cohérent du niveau d'intégration des circuits numériques, il a été nécessaire de développer de telles alimentations modulaires avec une densité de puissance fournie par unité de volume de l'ordre de 1500 W/dm^3. Par ailleurs, pour que ces alimentations puissent être implantées directement sur un LRM simple face, leur épaisseur a dû être limitée à 6,8 mm (boîtier compris).

Pour atteindre cet objectif d'intégration tout en garantissant les performances électriques des alimentations, des convertisseurs hybridés travaillant à haute fréquence de découpage (de l'ordre du MHz) ont été développés.

Après une présentation des avantages d'une architecture d'alimentation distribuée et un rappel des principaux objectifs techniques visés, cet article décrit les techniques et technologies mises en oeuvre pour atteindre ces objectifs. Une description approfondie des alimentations modulaires développées est donnée pour des puissances délivrées comprises entre 50 W et 100 W et pour différentes tensions de sortie.

Une dernière partie présente les développements futurs envisagés pour atteindre une densité de puissance fournie par unité de volume de 4000 W/dm^3.

1. INTRODUCTION

La fonction d'alimentation électrique dans un coffret de traitement numérique, que ce soit de données ou de signal, pour des équipements électroniques avancés, évolue d'une configuration centralisée vers une configuration complétement distribuée. La configuration centralisée correspond à celle rencontrée sur la majorité des équipements électroniques développés jusqu'alors : un coffret contenant un ensemble de cartes ou de modules électroniques comprend une alimentation délivrant à chaque carte sa puissance nécessaire, avec une tension correspondant à celle des composants. La configuration complétement distribuée est celle où chaque carte ou module d'un coffret comporte sa propre alimentation ayant pour tension d'entrée celle fournie par le porteur et en sortie, celle nécessaire aux composants. Entre ces deux configurations, se trouvent des cas comme ceux de programmes américains d'avionique modulaire tels Pave Pillar où la fonction d'alimentation se répartit dans quelques cartes dédiées fournissant chacune quelques cartes de traitement numérique. Néanmoins, ces choix ne sont qu'intermédiaires avant l'adoption d'un concept d'alimentation distribuée. Pourquoi l'alimentation distribuée est-elle une nécessité ?

Les composants électroniques des circuits numériques ont une consommation qui diminue à chaque nouvelle génération mais en parallèle, subissent une intégration technologique de plus en plus poussée. Ce dernier point amène au bilan constaté, d'une augmentation importante de la puissance nécessaire par carte de traitement numérique, utilisant des composants fonctionnant sous 5 V, voire à des tensions plus basses (3,3 V par exemple). Si dans un passé proche, des courants de 4 A étaient suffisants, il en est tout autrement avec des modules de 100 à 200 W, où les courants atteindront 20 à 40 A (sous 5 V), voire 60 A (sous 3,3 V).

Une autre raison est la nécessité d'une tolérance aux pannes et d'une fiabilité élevée pour la fonction d'alimentation électrique. Ces besoins entraînent le choix de la redondance, voire de la reconfiguration. Redonder une alimentation centralisée a pour conséquence le doublement du volume, de la masse et du coût de la fonction. Décomposer cette dernière en plusieurs briques individuelles permet d'optimiser la redondance : en effet, une brique supplémentaire permet une tolérance à la panne d'une brique de base. Néanmoins, le problème de maintenir des courants d'intensité élevée dans la carte mère subsiste. Il faut donc rapprocher les alimentations ou briques de base des circuits numériques. Outre le fait de faciliter la redondance, distribuer les alimentations permet, en les parallélisant, de reconfigurer la fonction d'alimentation. En effet, dans le cas d'une panne de l'alimentation d'une carte numérique, une gestion appropriée permet aux autres alimentations d'y suppléer.

Papers presented at the Avionics Panel Symposium held in San Diego, CA, USA, 6-9 June 1994.

Enfin, distribuer les alimentations apporte des avantages au niveau thermique par une meilleure répartition de la puissance dissipée : celle-ci n'est pas concentrée sur un bloc mais répartie sur chaque carte.

Une démonstration détaillée et chiffrée de la nécessité d'un concept d'alimentation distribuée est d'ailleurs présentée dans l'étude FASTPACK [1].

Néanmoins, ce choix de concept oblige à une intégration technologique plus importante des circuits d'alimentation. Il ne serait pas acceptable que l'alimentation soit l'élément le plus encombrant, tant en termes de surface occupée que de hauteur.

L'objet de la présente publication est de décrire le développement d'une première famille d'alimentation, dite modulaire, correspondant au nouveau concept retenu. Les principales caractéristiques de celle-ci sont :

- une très faible épaisseur (6,8 mm, boîtier compris) pour une intégration sur une carte simple face au pas de 12,7 mm et double face, au pas de 15,24 mm,

- un niveau d'intégration technologique de 1,5 kW/dm^3,
- une tension d'entrée de 270 V_{DC} ou 115 V_{AC},
- une qualification en environnement militaire.

2. RAPPEL DES PRINCIPAUX OBJECTIFS TECHNIQUES

L'objectif initial était de développer pour des applications militaires aéroportées une gamme d'alimentations modulaires à haut niveau d'intégration délivrant 50 W à 100 W à partir du réseau triphasé 200 V eff/400 Hz de manière à être cohérents des efforts d'intégration effectués au niveau des circuits utilisateurs (processeur de traitement du signal des radars, modules actifs, circuits hyperfréquences, etc ..).

2.1. Caractéristiques mécaniques visées

- Densité de puissance fournie ≈ environ 1500 W/dm^3 (soit un volume de 66 cm^3 pour une alimentation délivrant 100 W).

- Epaisseur compatible d'une implantation sur des LRM simple face au pas de 12,7 mm, soit une hauteur maximale de 6,8 mm.

- Masse inférieure à 150 grammes.

- Compatibilité avec les niveaux de vibrations et la gamme de température des matériels militaires aéroportés (soit température de fonctionnement de - 40°C à + 80°C, et température de stockage de - 55°C à + 125°C).

2.2. Caractéristiques électriques visées

- Compatibilité des alimentations avec le réseau de bord triphasé 200 V eff/400 Hz défini par la norme EN 2282. En particulier, ces alimentations doivent délivrer toutes leurs performances en présence de transitoires de tension à l'intérieur des limites 3 et 4 définies par cette norme (soit pour une tension entre phase et neutre comprise entre 60 Veff et 160 Veff. A l'extérieur de ces limites, les alimentations peuvent disjoncter et doivent recouvrer leurs performances à la fin du transitoire.

- Possibilité de mise en parallèle avec d'autres modules alimentations identiques. Cette possibilité permet :

  . de réaliser des alimentations capables de délivrer de fortes puissances avec des coûts de développement réduits.

  . d'accroître la fiabilité de la fonction "alimentation". Pour cela, il suffit de paralléliser n+1 alimentations modulaires lorsque le besoin réel est de n alimentations (ex : 6 alimentations 5 V/10 A pour alimenter un système ne consommant que 50 A). En cas de panne de l'une des alimentations, le système reste opérationnel.

- Rendement supérieur à 80 %

- Taux global de régulation (en fonction des variations de température, de la charge et de la tension réseau) meilleur que ± 2 %.

- Ondulation résiduelle superposée à la tension de sortie inférieure à 100 mV crête à crête (bande d'analyse de 20 MHz).

- Contrôle intégré du bon fonctionnement (protection contre les surcourants, test en surtension et sous-tension) et fourniture d'une information de bon fonctionnement.

- Réarmement automatique intégré suite à disjonction consécutive à un transitoire réseau au delà des limites 3 et 4.

- Possibilité de blocage de l'alimentation par signal logique externe.

- Consommation réduite lorsque l'alimentation est inhibée par le signal logique externe (inférieure à 3 W).

- Isolation galvanique entre la tension de sortie et le réseau triphasé d'entrée.

2.3. Gamme développée

Sept types d'alimentations modulaires ont été développés :

5 V / 10 A	7 V / 14 A
15 V / 3,3 A	3 V / 17 A
- 15 V / 3,3 A	24 V / 2 A
- 5,2 V / 10 A	

6 alimentations délivrent 50 W. Seule l'alimentation + 7 V délivre 100 W.

3. TECHNIQUES ET TECHNOLOGIES RETENUES

Pour atteindre le niveau d'intégration recherché tout en garantissant les performances électriques, il a été nécessaire de faire porter les efforts de développement sur 3 points :

- la structure du convertisseur continu-continu
- la technologie des transformateurs et inductances
- la technologie de réalisation de l'alimentation

3.1. Structure du convertisseur DC-DC

Le maintien des performances de l'alimentation en présence de transitoires de tension à l'intérieur des limites 3 et 4 définies par la norme EN 2282 (soit pour une tension phase/neutre comprise entre 60 Veff et 160 Veff) et le niveau d'intégration visé impose l'utilisation d'un convertisseur DC-DC fonctionnant à fréquence de découpage élevée. L'utilisation d'une fréquence de découpage élevée permet de diminuer le volume et la masse des composants réactifs (transformateurs, inductances, condensateurs) qui représentent une part importante du volume d'une alimentation.

En contre-partie, l'utilisation d'une haute fréquence de fonctionnement entraîne :

- pour des convertisseurs classiques à commutation dure (FORWARD, FLYBACK, etc ...) un accroissement des pertes en commutation dans les transistors de découpage, celles-ci étant proportionnelles à la fréquence de fonctionnement. Cet accroissement de la puissance dissipée dans les semi-conducteurs se caractérise par une diminution du rendement de l'alimentation.

- une augmentation des pertes fer dans les circuits magnétiques et des pertes joules dans le cuivre des bobinages (effet de peau). Ces pertes limitent au delà d'une certaine fréquence (environ 1 MHz) le gain escompté sur le volume des bobinages. En effet, au delà de cette fréquence, il devient nécessaire de prévoir un drain thermique pour évacuer la puissance dissipée dans les circuits magnétiques, ce qui annule le gain de volume résultant de l'augmentation de la fréquence de découpage.

La solution technique retenue découle naturellement de ces différentes considérations. Elle consiste :

1) A utiliser une architecture de convertisseur DC-DC à commutation douce de manière à réduire les pertes en commutation dans les transistors de découpage.

2) A limiter la fréquence de découpage à environ 1,3 MHz pour, d'une part, bénéficier pleinement de la réduction de volume des bobinages et d'autre part, atteindre l'objectif de rendement global de l'alimentation (limitation des pertes en commutation dans les interrupteurs et des pertes fer dans les circuits magnétiques).

La structure de convertisseur retenue est celle des convertisseurs à résonance série travaillant à une fréquence de découpage supérieure à la fréquence de résonance. Le convertisseur à résonance série présente un rendement meilleur sur celui du convertisseur à résonance série-parallèle. Ceci s'explique par le fait que le facteur de puissance du convertisseur série-parallèle est beaucoup plus faible que celui du convertisseur série, ce qui se traduit par un courant circulant dans le circuit oscillant (et donc dans les interrupteurs) plus élevé dans le cas du convertisseur série-parallèle. Ce courant élevé occasionne des pertes plus importantes dans les interrupteurs et dans les composants réactifs.

L'utilisation d'une fréquence de découpage supérieure à la fréquence de résonance du circuit oscillant permet de limiter les contraintes imposées à l'amorçage aux transistors de découpage.

3.1.1. Avantages du convertisseur résonnant-série

Outre les 2 principaux avantages évoqués précédemment, à savoir un rendement élevé du convertisseur grâce à l'utilisation de la commutation douce et une masse et un volume réduits des composants réactifs grâce à l'utilisation d'une haute fréquence de découpage, le convertisseur à résonance série permet également de réduire le niveau des perturbations électromagnétiques générées par rapport aux convertisseurs classiques à commutation dure et de limiter les contraintes en tension sur les interrupteurs.

En effet, la forme du courant circulant dans la cellule résonnante étant quasi-sinusoïdale, les phénomènes de di/dt qui donnent lieu à des perturbations électromagnétiques sont réduits.

Les niveaux de tensions appliqués sur les interrupteurs sont limités à la valeur de la tension continue d'entrée du convertisseur du fait de l'utilisation d'un onduleur résonnant demi-pont.

Cette tension continue étant obtenue par redressement du réseau triphasé 115 V efficace entre phase et neutre / 400 Hz, la tension maximale appliquée sur les interrupteurs sera atteinte lors des transitoires de surtension correspondant à la limite 1 de la norme EN 2282, soit pour une tension phase/neutre de 180 V efficace, ce qui correspond à une tension continue à l'entrée du convertisseur de 420 V.

Cette architecture permet donc d'utiliser pour les interrupteurs des transistors MOS de tension drain-source maximale égale à 500 V, composants très répandus sur le marché. Les transistors MOS présentent par ailleurs 2 autres avantages :

1) Ils ne possèdent pas de temps de stockage, ce qui les rend compatibles d'une utilisation à haute fréquence.

2) Ils possèdent une diode intrinsèque en anti-parallèle, ce qui les rend bidirectionnels en courant. Or, le fait de

travailler à une fréquence de découpage supérieure à la fréquence de résonance donne un caractère inductif au circuit RLC constitué de la cellule résonnante et de la charge en série avec cette cellule, ce qui impose l'utilisation d'interrupteurs bidirectionnels en courant et unidirectionnels en tension.

3.1.2. Contraintes d'utilisation du convertisseur résonnant-série

Bien que l'inductance et le condensateur constituant la cellule résonnante soient de faibles valeurs, ils doivent néanmoins véhiculer des courants élevés à haute fréquence. Ceci impose l'utilisation de technologies performantes pour minimiser les pertes. Par ailleurs, compte tenu de la contrainte d'épaisseur de l'alimentation (épaisseur maximale = 6,8 mm), la hauteur maximale admissible pour les composants est de 5 mm. Pour ces deux raisons, il a été nécessaire de développer une technologie de bobinages extra-plats et à faible perte (Cf § 3.2.).

Le condensateur de filtrage de la tension de sortie doit absorber un courant redressé double alternance haute fréquence conduisant à un courant efficace élevé ($\approx$ 8 A eff). Ce condensateur doit donc présenter une très faible résistance série équivalente et une fréquence de résonance propre élevée (supérieure à la fréquence de découpage) de manière à minimiser l'ondulation résiduelle en sortie d'alimentation et à réduire les pertes dans le condensateur. Un condensateur céramique à haute fréquence de résonance a été développé spécialement pour cette application. Quant au condensateur du circuit résonnant, il s'agit d'un condensateur céramique standard.

Enfin, la méthode de contrôle de la tension de sortie la plus simple à mettre en oeuvre et donc minimisant la surface de l'électronique de contrôle consiste à faire varier la fréquence de découpage. Toutefois, compte tenu de la grande dynamique de la tension d'entrée du convertisseur (140 V_{DC} à 375 V_{DC}) et de la charge (I = 0,1 Imax à Imax), la plage de variation de la fréquence de découpage est importante. Le rapport entre la fréquence minimale f_{min} obtenue à pleine charge et à tension d'entrée minimale et la fréquence maximale f_{max} obtenue à faible charge et à tension d'entrée maximale devrait être environ de 3. Ceci conduirait pour cette application à une fréquence de découpage f_{max} égale à 1,8 MHz incompatible des circuits de commande de gate des transistors MOS de découpage.

La solution a consisté à limiter cette fréquence de découpage à 1,3 MHz en employant une régulation de type on-off pour les faibles débits (suppression des impulsions de commande).

3.1.3. Description de l'alimentation

Le synoptique de l'alimentation modulaire complète est donné en Figure 1. Le réseau d'entrée triphasé 200 V eff / 400 Hz est préalablement redressé par un pont de GRAETZ puis filtré pour être transformé en une tension continue de 270 V nominale.

La cellule résonnante associée en série au primaire du transformateur de puissance est connectée entre les points milieu du diviseur capacitif de la tension continue 270 V et de l'onduleur de tension demi-pont constitué de 2 transistors MOS.

Le redressement double-alternance au secondaire du transformateur est réalisé par 2 diodes SHOTTKY afin de minimiser les pertes en conduction.

Un convertisseur DC-DC auxiliaire (Cf Figure 2) fournit les tensions (+ 5 V, $\pm$ 12 V) nécessaires aux circuits d'asservissement, de sécurité et de commande de gate des transistors MOS. Ce convertisseur est du type FLYBACK à restitution totale et travaille à une fréquence fixe de 200 kHz. Des régulateurs linéaires délivrent à partir d'une tension stabilisée + 15 V, les tensions régulées + 12 V et + 5 V. La tension - 12 V n'alimente que les amplificateurs opérationnels de la boucle d'asservissement et par conséquent la consommation est très faible (inférieure à 10 mA). Cette tension est élaborée simplement à l'aide d'un circuit à pompe de charges à partir de la tension + 12 V.

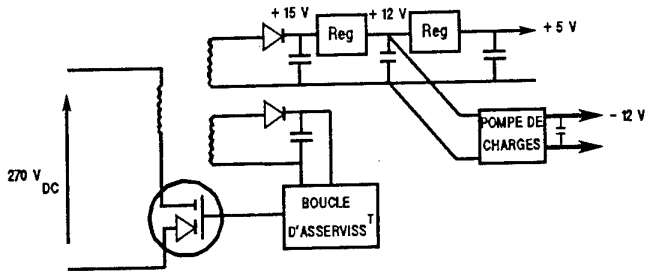


Figure 2 : Synoptique du convertisseur auxiliaire

L'ensemble des circuits d'asservissement, de sécurité et de commande sont référencés au zéro électrique de la tension de sortie. L'isolement galvanique entre la tension de sortie V_s et le réseau triphasé est obtenu d'une part, par le transformateur du convertisseur auxiliaire et d'autre part, par l'utilisation de transformateurs d'impulsion pour transmettre les commandes aux gates des transistors MOS de commutation.

L'un des principaux objectifs de ce développement était de pouvoir paralléliser plusieurs alimentations modulaires identiques. Or, les règles de l'électronique font qu'il n'est pas possible de mettre deux sources de tension en parallèle.

La solution a consisté à transformer chaque alimentation modulaire en générateur de courant.

Chaque alimentation modulaire dispose donc de sa propre boucle d'asservissement en courant qui reçoit une même référence de courant issue d'une unique boucle d'asservissement en tension. La lecture de courant est

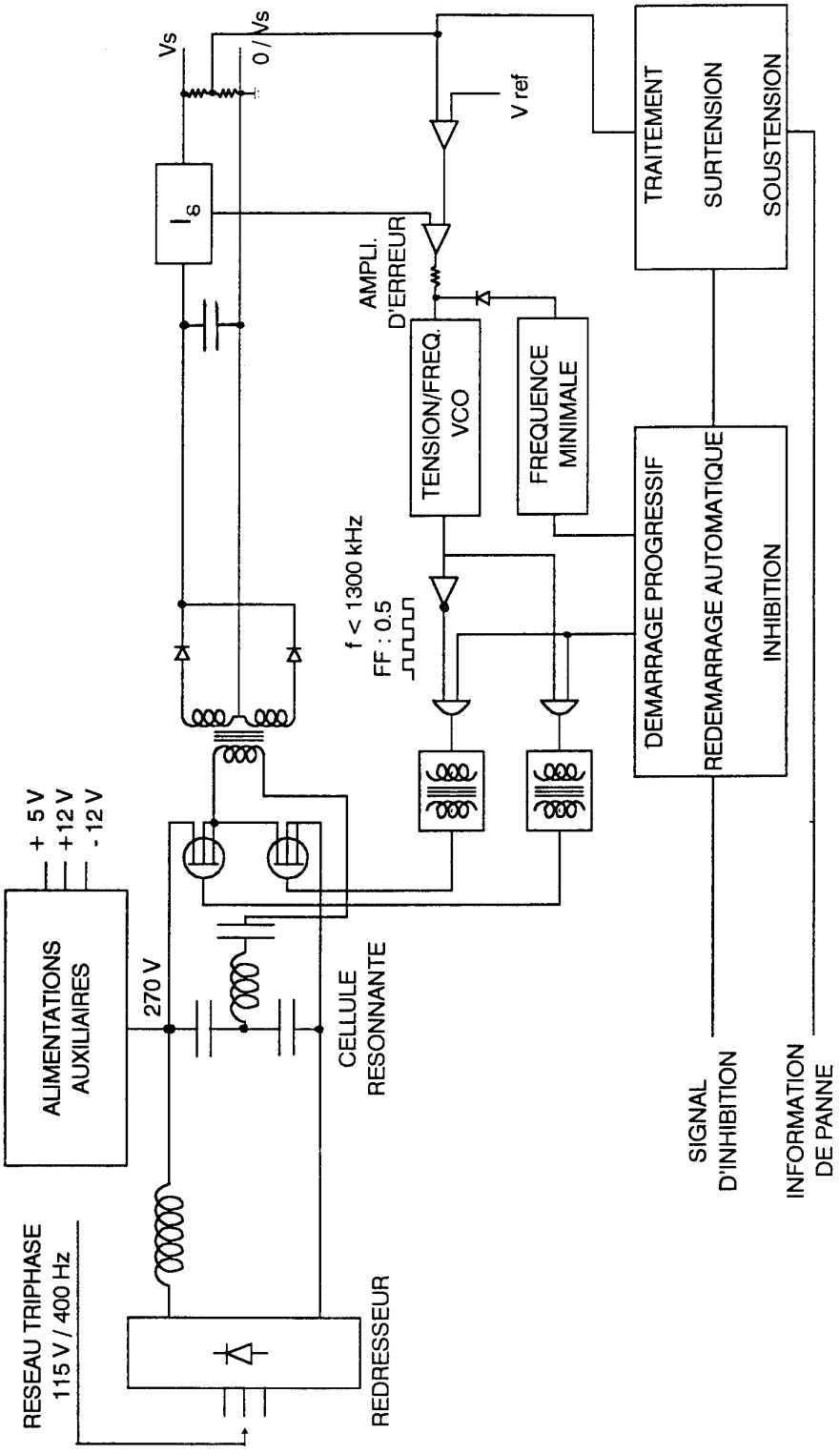


FIGURE 1 - SYNOPTIQUE DE L'ALIMENTATION MODULAIRE

effectuée à l'aide d'un shunt. Ce système présente par ailleurs l'avantage de garantir une répartition équilibrée du courant dans chaque alimentation modulaire quelle que soit la charge globale. Chaque alimentation modulaire est donc sollicitée de la même façon, ce qui est favorable à la fiabilité de l'ensemble.

La tension d'erreur issue de la double boucle d'asservissement courant-tension est appliquée à l'entrée d'un convertisseur tension-fréquence ("VCO"). Ce "VCO" délivre un signal carré de facteur de forme 1/2 et de fréquence proportionnelle au signal d'entrée (F = kVe + Fo, Fo = constante, Ve = tension d'entrée, F = fréquence du signal de sortie). Le signal de sortie du VCO commande en opposition de phase les 2 interrupteurs du convertisseur résonnant. La fréquence minimale Fo est obtenue en imposant une tension minimale à l'entrée du "VCO" afin d'avoir une fréquence de sortie du "VCO" toujours légèrement supérieure à la fréquence de résonance. En effet, le fonctionnement d'un convertisseur résonnant-série à une fréquence inférieure ou égale à la fréquence de résonance est formellement interdit.

L'alimentation dispose d'un dispositif de démarrage progressif permettant de limiter les contraintes en courant dans les transistors MOS pendant la phase transitoire de démarrage. Ce dispositif impose en sortie du "VCO" lors de chaque démarrage une fréquence très élevée qui diminue ensuite progressivement pour rallier la fréquence de fonctionnement nominale du convertisseur. L'alimentation dispose également d'une entrée permettant, à l'aide d'un signal logique externe, de bloquer son fonctionnement, c'est-à-dire d'imposer une tension de sortie nulle. Dans cette configuration, la puissance consommée sur le réseau triphasé est limitée à 3 W correspondant au courant de repos d'un nombre limité de circuits intégrés.

L'alimentation est équipée de circuits de sécurité permettant de la protéger contre des surcharges accidentelles des circuits utilisateurs et de protéger également ceux-ci contre d'éventuels défauts de l'alimentation (surtension ou sous-tension). Lors d'un surcourant sur la tension de sortie de l'alimentation, celle-ci disjoncte immédiatement et tente des redémarrages successifs jusqu'à disparition du défaut. En cas de surtension en sortie, l'alimentation disjoncte définitivement. Un signal logique de panne est transmis à l'extérieur dès que la tension de sortie sort de la plage autorisée.

3.2. Technologie des transformateurs et inductances

3.2.1. Le transformateur résonnant

Le transformateur de puissance dit "transformateur résonnant" est, de par sa fonction, son encombrement et les contraintes imposées, le composant magnétique le plus complexe.

Les principales caractéristiques exigées de ce transformateur sont :

- une gamme de fréquences de fonctionnement élevées qui impose une bonne maîtrise des éléments parasites,
- un rendement très élevé (> 95 %) qui oblige à minimiser les pertes à la fois dans les circuits magnétiques dites pertes "fer" et dans les conducteurs dites pertes "cuivre",
- une température maximale de fonctionnement de 110°C (soit une élévation de température de 30°C du circuit magnétique pour un environnement à 80°C),
- une puissance volumique élevée (typiquement de l'ordre de 18 kVA/dm^3),
- une tenue en tension et isolement supérieure à 1500 V efficace,
- une hauteur maximale de 5 mm.

Pour optimiser une telle puissance volumique avec une hauteur de 5mm, deux actions ont été menées :

- maîtriser les pertes dans les circuits magnétiques,
- optimiser la technologie de bobinage et d'encapsulation.

3.2.1.a Choix du circuit magnétique

La recherche d'une fréquence de résonance élevée et d'une inductance magnétisante importante a nécessité l'utilisation de matériaux ferrites de permeabilité μi comprise entre 700 et 2500.

Les matériaux sélectionnés appartiennent à la classe 3 optimisés en pertes dans la bande de fréquences de fonctionnement pour une gamme de température de fonctionnement comprise entre 80°C et 110°C ; les ferrites de la classe 4 sont encore au stade du laboratoire ou restent difficiles à approvisionner.

Les contraintes électromagnétiques et de hauteur ont nécessité d'optimiser la géométrie ; une modélisation a permis de déterminer la section magnétique minimale permettant de travailler à une induction telle que les pertes soient minimales dans la gamme de fréquences utilisée.

Cette optimisation de géométrie a nécessité l'utilisation de circuits magnétiques spécifiques obtenus par usinage et rectification et la mise au point d'un traitement thermique permettant d'éliminer toute contrainte magnétostrictive et de retrouver les propriétés intrinsèques du matériau.

3.2.1.b. Technologie de bobinage

La technologie de bobinage est classique : les bobinages sont réalisés sur deux jambes à l'aide de fils divisés de section circulaire définie pour minimiser les pertes "cuivre" (en particulier les pertes par effet de peau) et ensuite moulés.

Pour tenir les contraintes d'isolement, le primaire du transformateur est isolé du secondaire par un diélectrique dont le choix permet d'obtenir un bon compromis entre capacités parasites et inductances de fuite.

Le respect des tolérances mécaniques (hauteur $\leq$ 5 mm) et les conditions de report élevées (T > 125°C) ont nécessité :

- le développement de boîtiers injectés de toile de 0,3 mm,
- la formulation d'une nouvelle résine époxyde permettant à la fois de tenir les cotes mécaniques (pendant et après les différentes conditions de mise en oeuvre et d'environnement) et de minimiser les contraintes mécaniques au niveau du circuit magnétique,
- la mise en place d'un cycle de stabilisation en température.

Ce processus de réalisation a permis ainsi d'obtenir une bonne reproductibilité de l'inductance de fuite.

3.2.1.c. Performances obtenues

Les performances obtenues avec cette technologie sont données dans le tableau de la Figure 4 (bobinage classique).

3.2.2. L'inductance résonnante

L'architecture de l'alimentation impose des inductances résonnantes de faible valeur. Par ailleurs, l'utilisation directe de la tension réseau redressée (270 V_{DC}) comme source d'énergie conduit à faire travailler le matériau magnétique à une induction telle qu'à des fréquences de 1,3 MHz les pertes "fer" sont très élevées.

Une surface de base importante est donc nécessaire pour évacuer la puissance dissipée.

Les principales caractéristiques exigées pour l'inductance sont :

- une très forte puissance réactive transmise supérieure à 200 VA,
- de faibles pertes "fer" à un niveau d'induction élevée dans toute la gamme de fréquence de fonctionnement (inférieures à 1 %),
- des valeurs d'inductance comprises entre 20 μH et 50 μH,
- l'isolement vis-à-vis du réseau 200 Veff/400 Hz,
- une hauteur inférieure à 5 mm.

3.2.2.a. Choix du circuit magnétique

Les faibles valeurs d'inductance demandées nécessitent un faible nombre de spires ou une faible perméabilité apparente μa du circuit magnétique.

Un faible nombre de spires et une forte tension aux bornes de l'inductance imposent une induction B élevée dans le circuit magnétique.

Comme les pertes fer sont au moins proportionnelles à B^2, elles croissent alors très vite quand le nombre de spire décroît.

Ainsi, obtenir de faibles pertes fer nécessite un nombre de spires important, ce qui impose un circuit magnétique à faible perméabilité apparente.

Deux possibilités étaient offertes :

- la self à air ($\mu a = 1$) qui entraîne un encombrement important ; dans ce cas, il n'y a pas de pertes fer, par contre, les pertes "cuivre" sont très élevées et les perturbations électromagnétiques engendrées sont difficiles à éliminer dans le volume restreint,
- le circuit magnétique à entrefer :
  - soit à entrefer localisé mais à forte induction cet entrefer localisé devient une source de pertes par rayonnement qui va augmenter les pertes cuivre et perturber les circuits électroniques avoisinants,
  - soit à entrefer réparti, ce type de matériau est constitué de particules magnétiques espacées les unes des autres par un diélectrique. Ces minuscules interstices entre les grains de fer constituent des entrefers distribués au sein du matériau. Le flux de fuite de ces enterfers est donc réparti en petites fractions au lieu d'être concentré en un seul point comme avec l'enterfer localisé, ce qui a pour effet de réduire les pertes par rayonnement.

La solution retenue consiste à utiliser un circuit magnétique à enterfer réparti.

Pour être compatible des contraintes de hauteur, le circuit magnétique optimisé d'épaisseur 3 mm est obtenu par usinage et rectification de circuits standards, permettant d'assurer une reproductibilité des valeurs d'inductance avec une précision de 3 %.

Avec ce circuit magnétique optimisé, les pertes fer s'élèvent à 1,5 W/cm^3 pour une induction B = 30 mT à une fréquence de 1 MHz.

3.2.2.b. Technologie de bobinage

La technologie de bobinage des inductances est classique : le bobinage est réalisé sur un tore dont la section magnétique a été dimensionnée pour obtenir le niveau de pertes indiqué. Le processus de réalisation est identique à celui du transformateur.

3.2.2.c. Performances obtenues

Les performances obtenues avec cette technologie sont :

- une puissance réactive transmise typique de 282 VA à 0,7 MHz,
- des pertes de l'ordre de 2 W,
- une puissance réactive volumique de 60 kVA/l,
- des valeurs d'inductance (L) de 20 μH à 50 μH $\pm$ 3 %.

3.3. Technologie de réalisation de l'alimentation

La minimisation du volume de l'électronique par le choix adéquat de la structure du convertisseur DC-DC et de la technologie des bobinages n'est pas suffisante pour atteindre l'objectif de volume. Il faut également agir au niveau de la technologie de réalisation de l'alimentation. Celle-ci a été réalisée sous forme d'un circuit hybridé.

Les composants peu dissipatifs (circuits d'asservissement, de sécurité et de commande) sont hybridés sur un substrat en Alumine multicouche, le câblage interne entre puces étant effectué à l'aide de fil en Or d'un diamètre de 25 μm.

Les composants à forte dissipation (transistors MOS, diodes SHOTTKY) sont brasés sur des substrats en Oxyde de Beryllium (B_eO) afin de limiter la résistance thermique entre la jonction de ces semi-conducteurs et le fond du boîtier de l'alimentation (Résistance thermique < 2°C/W). L'Oxyde de Beryllium est en effet un très bon conducteur thermique (conductivité thermique $\approx$ 200 W/m.K). Les liaisons électriques véhiculant de forts courants sont réalisées avec du fil en Aluminium pouvant atteindre un diamètre de 150 μm ainsi que par des barres en alliage de Cuivre et Molybdène brasées sur les substrats. Ces barres sont principalement utilisées en sortie de l'alimentation là où les courants sont les plus élevés (17 A dans le cas de l'alimentation + 3 V).

Le boîtier est réalisé en Aluminium. Ce choix permet :

- de minimiser la masse de l'alimentation (par rapport à des boîtiers en Cuivre, Titane ou Ferro-Nickel),
- d'assurer une bonne évacuation de la puissance dissipée (conductivité thermique supérieure à 150 W/m.K).

Toutefois, le coefficient de dilatation de l'Aluminium étant très différent de celui de l'Alumine et de l'Oxyde de Beryllium, les substrats ont dû être reportés sur le fond de boîtier à l'aide d'une colle souple assurant la compensation des différences de dilatation. De même, les bobinages sont collés par préimprégnés sur le fond de boîtier.

Par ailleurs, les zones à forte tension (circuits connectés au réseau triphasé redressé principalement) sont localement enrobés dans une résine silicone afin de garantir la tenue en tension.

L'herméticité du boîtier nécessitée par l'utilisation de puces nues est obtenue par l'emploi de traversées électriques hermétiques (perle de verre) et par la fermeture du boîtier par un couvercle soudé par LASER.

4. RESULTATS OBTENUS

4.1. Caractéristiques mécaniques

L'alimentation 7 V/14 A a été réalisée dans un boîtier de 168 x 58 x 6,8 mm^3 (soit un volume de 66 cm^3) et de 145 grammes. Les autres alimentations délivrant une puissance de 50 W ont été réalisées dans un boîtier de 100 x 50 x 6,8 mm^3 (soit un volume de 34 cm^3) et de 105 grammes. Ces caractéristiques mécaniques correspondent à une densité de puissance fournie de l'ordre de 1500 W/dm^3.

Une photographie de l'alimentation 7 V/14 A est donnée en Annexe A1.

4.2. Performances électriques

Les performances électriques des différentes alimentations sont conformes aux objectifs initiaux. A titre indicatif, les principaux résultats obtenus sur l'alimentation 5 V/10 A sont donnés ci-dessous :

- Rendement
  La courbe de rendement en fonction du courant de sortie pour la tension nominale d'entrée (soit 270 V_{DC} après redressement) est donnée en Figure 3.
- Ondulation résiduelle
  L'ondulation résiduelle superposée à la tension de sortie est inférieure à 80 mV crête à crête (Bande d'analyse 20 MHz).

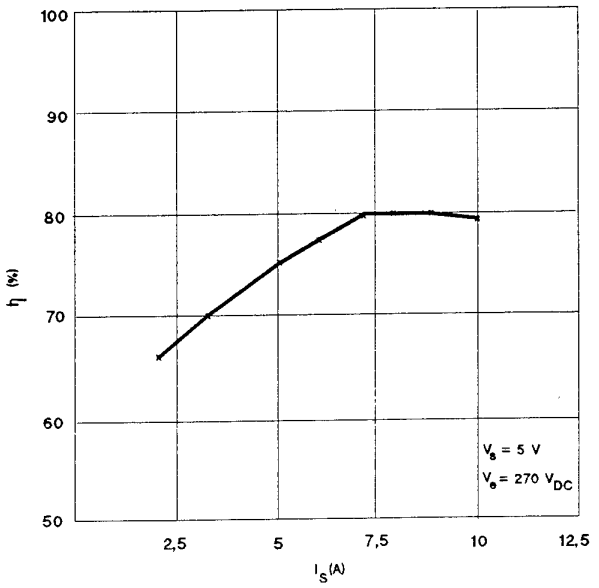


Figure 3 : Rendement mesuré pour l'alimentation 5V/10A

- Taux de régulation
  Les taux de régulation mesurés sur l'alimentation 5V/10A sont les suivants :

  . Variation de tension de sortie en fonction de la tension d'entrée
  ± 0,3 % (pour une tension d'entrée phase/neutre comprise entre 60 Veff et 160 Veff)

  . Variation de tension de sortie en fonction de la charge
  ± 0,2 % (pour un courant de sortie variant de 1 A à 10 A)

  . Variation de tension de sortie en fonction de la température
  ± 0,5 % (pour une température variant de -40°C à +80°C),

  soit un taux global de régulation de ± 1 %.

- Performances dynamiques
  L'alimentation 5V/10A délivre ses performances en présence de transitoires de tension à l'intérieur des limites 3 et 4 de la norme EN 2282 (soit entre 60 Veff et 160 Veff phase/neutre).

5. DEVELOPPEMENTS FUTURS

L'objectif des développements futurs est d'atteindre une densité de puissance fournie par unité de volume de 4000 W/dm^3 de manière à accompagner l'évolution du niveau d'intégration des futurs systèmes de l'avionique modulaire.

Il faudra ainsi développer une nouvelle famille d'alimentations modulaires délivrant une centaine de watts à partir du réseau triphasé redressé 200 Veff/400 Hz (270 V_{DC}) dans un volume d'environ 25 cm^3 et avec des performances électriques semblables à celles des alimentations actuelles. Leur épaisseur devra être inférieure à 7 mm pour être compatible d'une implantation sur un LRM double face.

Ce challenge pourra être relevé en travaillant selon les axes suivants :

- La recherche d'une nouvelle structure de convertisseur DC-DC permettant de minimiser le nombre de bobinages et le nombre de composants électroniques. Par exemple, une structure de convertisseur à un seul interrupteur référencé au zéro électrique de la tension d'entrée (0 V/270 V_{DC}) permet de supprimer les transformateurs d'impulsion de commande de gate des MOS, à condition de référencer également l'électronique de contrôle au 0 V/270 V_{DC}. Dans ce cas, l'isolement galvanique entre le réseau d'entrée et la tension de sortie impose de transmettre l'information de lecture de la tension de sortie vers les circuits de régulation à l'aide d'un optocoupleur.

- L'utilisation d'un ASIC mixte numérique/analogique permettant de réaliser les fonctions de régulation et de génération des signaux de commande de l'interrupteur ainsi que la fonction de contrôle et de test intégrés.

- Le remplacement de l'alimentation auxiliaire permanente utilisant un transformateur par une alimentation de démarrage sans transformateur. Cette alimentation fournira l'énergie nécessaire aux circuits de régulation, de contrôle et de test pendant la phase de démarrage de l'alimentation. Lorsque le convertisseur DC-DC aura atteint son régime permanent, l'énergie sera fournie à partir d'un enroulement secondaire du transformateur principal. Cette solution permet de faire l'économie d'une alimentation auxiliaire complexe.

- L'utilisation d'une nouvelle technologie pour réaliser les bobinages (transformateur et self). La technologie envisagée consiste à réaliser les spires des différents enroulements des bobinages par de la sérigraphie sur des céramiques multicouches au lieu d'utiliser le fil de cuivre habituel. Les premiers travaux effectués sur cette technologie ont montré qu'il était possible de réaliser les transformateurs des alimentations modulaires de la génération actuelle avec une densité de puissance transmise par unité de volume de 30 kW/dm^3 au lieu de 18 kW/dm^3 dans la technologie classique, soit un transformateur de 100 W dans le volume suivant : 26 x 26 x 5 mm^3.

  Par ailleurs cette technologie permet de mieux maîtriser les selfs de fuite et les capacités parasites et surtout de les réduire dans un rapport 3 à 4 ce qui, associé à l'utilisation des futurs circuits magnétiques à faible perte permet d'envisager une augmentation de la fréquence de fonctionnement, donc une nouvelle diminution de l'encombrement des bobinages. Le tableau de la Figure 4 permet de comparer les principales caractéristiques mesurées sur un transformateur de l'alimentation modulaire actuelle réalisé dans 2 technologies différentes (technologie classique et nouvelle technologie).

Technologie / Caractéristiques	Bobinage classique	Bobinage sur alumine sérigraphiée multicouches
Puissance volumique	18 kW/dm^3	30 kW/dm^3
Puissance transmissible	100 W	100 W
Tension d'isolement	1500 Veff	1500 Veff
Inductance de fuite	4 µH (± 10 %)	1,1 µH (± 5%)
Capacité primaire/second aire	80 pF	29 pF
Résistance primaire	200 mΩ	130 mΩ
Résistance secondaire	4,2 mΩ	4,8 mΩ
Gamme de fréquence	0,3 à 1,3 MHz	0,3 à 2 MHz
Gamme de température	-55°C à +125°C	-55°C à +125°C

Figure 4 : Caractéristiques des transformateurs extra-plats suivant différentes technologies

Une photographie des transformateurs réalisés dans cette nouvelle technologie est donnée en Annexe A2.

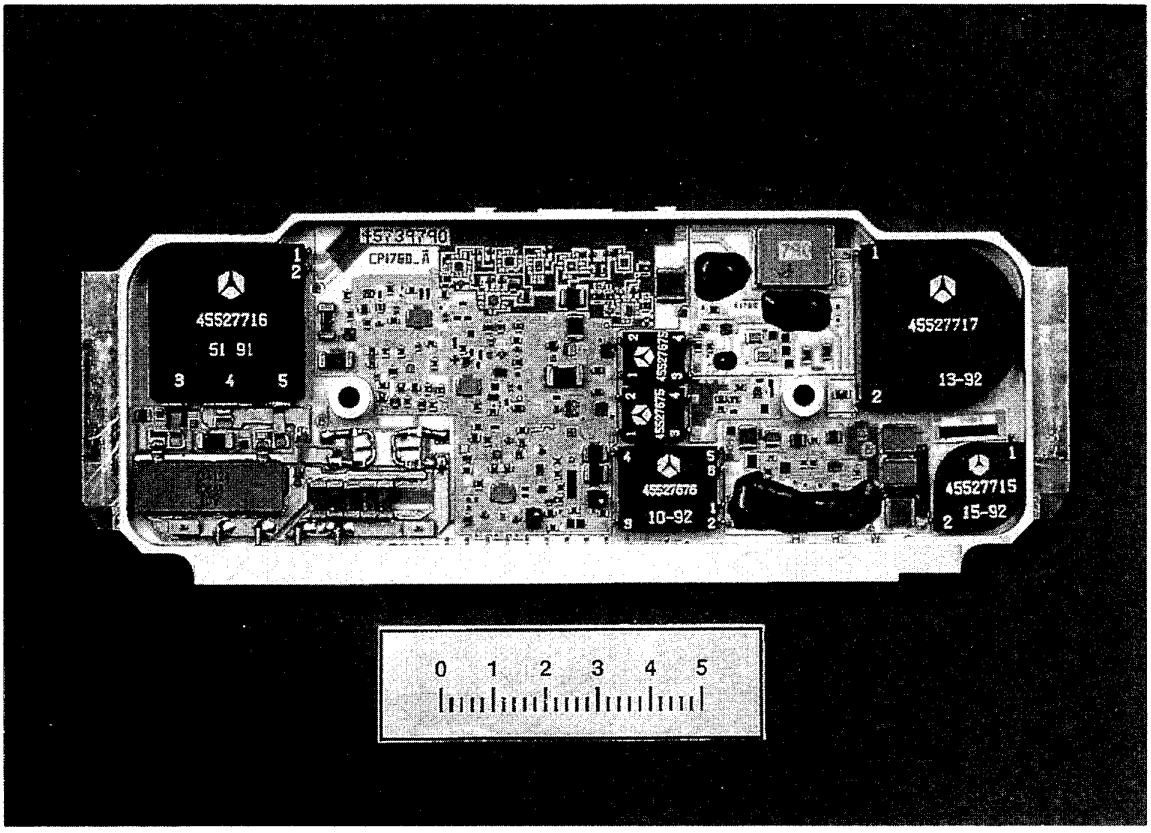
- La mise en oeuvre d'un nouveau packaging permettant d'augmenter le niveau d'intégration en exploitant mieux la totalité du volume disponible. On constate en effet que dans les alimentations modulaires actuelles, la hauteur disponible est pleinement utilisée uniquement dans les zones où il y a des bobinages. Par contre, au dessus des céramiques, un grand volume reste vide.

  Une solution consiste à utiliser les 2 faces externes du boîtier pour reporter des céramiques dans les zones où il n'y a pas de bobinages. Néanmoins, les aspects thermiques devront être étudiés finement car la face qui n'est pas en contact avec la plaque froide du LRM ne pourra pas évacuer beaucoup de puissance.

  Ces différents axes d'étude permettent d'envisager avec optimisme la réalisation d'une alimentation modulaire avec une densité de puissance fournie par unité de volume de 4000 W/dm^3.

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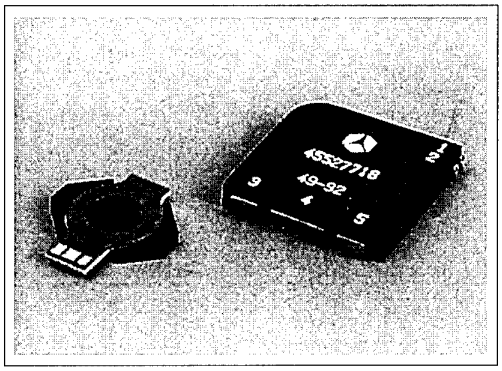


ANNEXE A1 - PHOTOGRAPHIE DE L'ALIMENTATION 7 V / 14 A

PUISSANCE VOLUMIQUE :
30 kW / l

PUISSANCE TRANSMISE :
100 W

GAMME DE FREQUENCES :
JUSQU'A 1,5 MHz

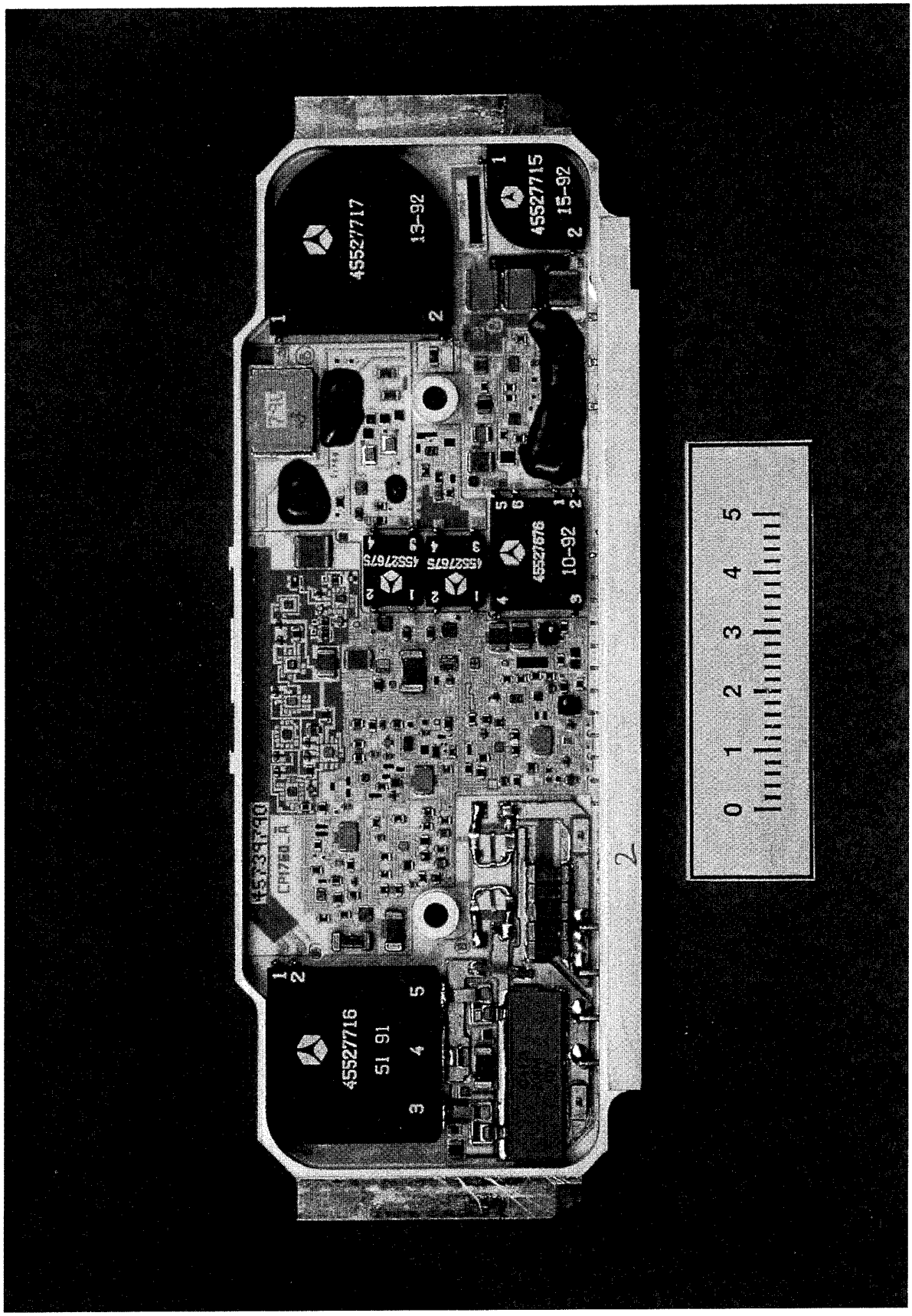


PUISSANCE VOLUMIQUE :
18 kW / l

PUISSANCE TRANSMISE :
85 W

GAMME DE FREQUENCES :
JUSQU'A 1,3 MHz

ANNEXE A2 - PHOTOGRAPHIE D'UN TRANSFORMATEUR DE NOUVELLE TECHNOLOGIE (à gauche) ET DE TECHNOLOGIE ACTUELLE (à droite)


4552717
13-92
4552715
15-92
4552716
51 91
4552676
10-92
0 1 2 3 4 5

ELECTROMAGNETIC COMPATIBILITY EFFECTS OF ADVANCED PACKAGING CONFIGURATIONS

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SUMMARY

The Electromagnetic Compatibility (EMC) of digital avionic equipments assumes ever larger dimensions especially in the light of the tendency of modern technology aimed at higher data trasmission rates and therefore higher clock frequencies and, at the same time, higher component density with reduced consumption.
The emission and susceptibility problems commonly encountered in digital circuits are examined indicating critical areas and praticable suggestions to improve design techniques.

1 INTRODUCTION

The present technology trend is addressed to develop smaller and faster ICs. In a recent digital technology conference [1] some developments have been presented which are really impressive especially if compared with the achievements of only some years ago. Improvements in CMOS processing have resulted in 256 Mbit dynamic RAMs, 64 Mbit flash memories. A CMOS superscalar microprocessor has been created capable of providing more computational throughput than a Cray 1 supercomputer. The processor which employs about 2.6 million transistors can execute up to four instructions per cycle. When running at the speed of 75 MHz it delivers the 300 MIPS peaks throughput. The speed crown is taken by a 32 bit RISC CPU that operates at 500 MHz developed by NEC in a 0.4 micron process.

The switching speed of digital components is increased because there is the need of using faster computing and information processing rates. Unfortunately there is a gap between the achievable highest rate of systems especially if they are intended for commercial applications. There are many reasons for this lack of performance matching between components and systems but surely one of the main causes is related to the difficulty of implementing electromagnetic theory principles to system design and packaging. When the component dimensions become comparable with $\lambda = \lambda o/\sqrt{\varepsilon}$ where λo as the free space wavelength of the highest intentionally generated frequency and ε is the permettivity of the dielectric material some concepts of circuit design theory shall be carefully revisited:

–the resistance R has a meaning different from the low frequency characterization because one has to take into account the skin effect which forces currents to propagate within the external perimeters of conductors.
Therefore it may happen that at high frequencies unwanted series resistances become comparable with the characteristic impedances of conducting paths which range from 50 to 150 Ohms

–parasitic inductances and capacitances shall also be taken into account because of their impact on impedance matching, propagation delay and coupling effects on nearby circuits. The inductance value of 1nH produces a reactive impedance of 1 Ohm at 160MHz and 10 Ohm at 1.6 GHz; this impedance starts to have importance in a 50 Ohm system. Similarly the coupling between two conductors due to a capacitance of 1nF is meaningless at 100 MHz but starts to become effective when the frequency approaches the GHz region.

The new digital technology frontiers impose to take into account Electromagnetic Compatibility (EMC) principles in the design of avionic systems where electromagnetic environment is particulary severe because space constraints require a large concentration of equipment. EMC problems will be examined considering the two axpects which characterize this discipline: emission and susceptibility. Emission is generally related to the nominal in band performances of ICs and mostly depends upon the geometrical lay out of PCBs and cables, while susceptibility is mainly related to out of band non linear performances of ICs.

2 EMISSION

The problem of emission from circuit boards with related problems of local susceptibility on the same board or nearby circuits assumes ever larger dimensions especially in the light of the tendency of modern technology aimed at higher data trasmission rates and therefore higher clock frequencies and, at the same time, higher component density with reduced consumption. The first problem to examine is to clarify whether the component itself generates radiated emission. To test this hypothesis a series of measurements [2] were conducted on the Motorola 68HC11 MCU with an EPROM and an application specific integrated circuit (ASIC). Software was written for the 68HC11 and the ASIC to find out how different functions affect the emissions of the circuit. Even if the emission level is low it is interesting to see that the radiated level changes according to the software routines because each routine activates a specific mode of operation of the circuit.

Most of radiated emission comes out of the PCB and strongly depends on its layout. Circuit board emission may occur either via differential or common mode radiation.

Differential mode radiation is caused by currents flowing in loops formed by the conductors of the circuit which act as small

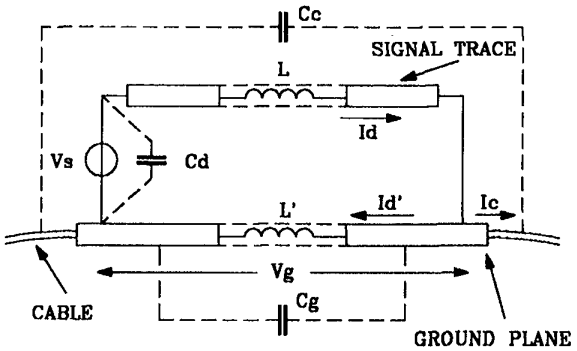
antennas.
The electric field emitted at the distance R by a small loop antenna of area A in which a current I flows is given by

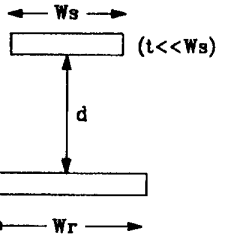
$$E = 1.316\ 10^{-16}\ f^2 A \frac{\text{sen}\,\theta}{R}$$

where f is the frequency of the emission and θ is the angle indicating the direction along which the electric field is produced. This equation is generally valid and it does not depend on the shape of the loop provided its perimeter is less than a quarter wavelength. As may be noted to minimize electric field emission one may reduce the current, its frequency or harmonic content or the area of the loop in which the emitting current flows. Multilayer circuit boards with internal ground planes eliminate these ground loops. The return path of the signal is in the ground plane which always lies below the hot side of the circuit.
Common mode radiation is caused by undesired voltage drops in the board. The cable connected to the board and/or the board itself because of their stray capacitances act as antennas. The antenna for common mode can be modelled as a short monopole of length l supplied with a common mode current I of frequency f. The electric field at distance R along a direction θ is given by

$$E = 4\pi 10^{-7}\ f\,Il \frac{\text{sen}\,\theta}{R}$$

The most obvious method for limiting common mode emission consists of limiting the current I.





L	inductance of the signal trace
L'	inductance of the ground plane
Cg	distributed stray capacitance of the ground plane
Cc	distributed stray capacitance of the cables
Cd	decoupling capacitor (CAC)
Vs	signal voltage
Vg	ground voltage

Figure 1 PCB with ground plane

In Figure 1 the lay out of a PCB with ground plane is shown. The common mode current Ic = Id – Id' is much lower than the differential currents Id and Id'. Nevertheless it generates higher radiated fields than differential mode currents because the latter ones tend to cancel. To reduce common mode emission the ground voltage Vg must be reduced. It is given by

$$Vg = L' \frac{dId'}{dt}$$

The inductance L'is given by

$$L' = \frac{1}{2\pi} \ln \left| \frac{d\pi}{Wr} + 1 \right| \quad (H)$$

where d is the distance between the signal trace and the ground plane, Wr and l are the width and the length of the ground plane. The signal trace inductance is given by the same equation wherein Wr is substituted by Ws. The inductance of a PCB track is therefore decreased by broadening the track to a plane and/or by reducing the distance between the signal track and the return one.

A multilayer PCB is better than a bilayer one. As a rule of thumb one can say that the net result is a factor of 10 in lower ground impedance per layer doubling. Using a 4 plane multilayer PCB instead of a bilayer PCB there is an improvement of 10(a factor of 5 due to the smaller distance between the signal and return track and a factor of 2 due to the plane doubling) [7].

Alternatively Vg can be reduced by providing additional return paths for the signal current.

From these considerations it appears that a highly emitting signal trace should be located on a layer adjacent to the ground plane with additional guard traces on its both sides; each guard trace shall be connected to the ground plane at both ends. Alternatively in case of a multilayer PCB the guard traces can be substituted by a shunt trace connected at both ends to the ground plane and located above the highly emitting signal trace [3] – [6].

To reduce the common mode emission due to the cables connected to the circuit board it is possible to use common mode chokes inserted in the cables. The efficiency of a choke is usually limited to less than 20dB owing to the by pass effect of stray capacitance.

A large source of interference on which to act to reduce both common mode and differential mode emmission is the control of transient current required by logical gates during switching. The area of the power current loop may be reduced by using suitable decoupling capacitors Cd as shown in Fig. 1. It is important to have capacitors located as close as possible to the logic elements that are sources of interference in order to reduce the emitting loop area A for the differential mode emission and the length l of the ground plane path for the common mode emission.

The close attached capacitor (CAC) [8] is a thin flat capacitor having the size comparable to an IC die that is placed on the active source of the die and connected to power and ground pads through very short wires with low equivalent series inductance (few hundred picoHenries) and series resistance.

However the use of capacitors for decoupling in power lines for printed circuit is not an entirely acceptable method above all as far as reliability is concerned. It is, therefore, advisable to attempt to reach high capacitance by exploiting the configuration of the board and the power supply track. Besides the avoidance of

adding concentrated capacitance, there is the additional advantage of having power lines with low characteristic impedance; this allows better matching conditions with the power supply circuit which has low impedance.

3 SUSCEPTIBILITY

Electromagnetic Interference has been known for a long time as a source of malfunctions and failures in digital circuits. In the past the main concern was related to the maximum amplitude of the interfering signal because the only possible malfunction was deemed to be an induced false switching.

Recently [11] it has been recognized that it is also possible to have induced delays due to low amplitude interference signals which in some cases may have more catastrophic effects than false switching. In the latter case malfunctions are dependent on the phase of the interference relative to a logic transition.

The mechanism which generates an induced delay is shown in Figure 2.

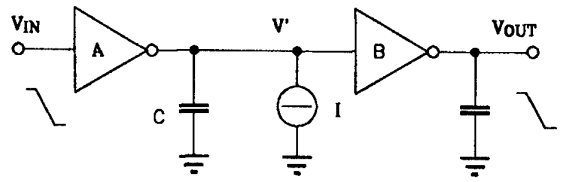


Figure 2 Two inverters with loading capacitors and an interference current I

The interference current I = Io sen(wt+ϕ) injected into the output capacitance C of inverter A determines the distortion of the waveform of V' as shown in Figure 3 causing the delay Δt in the crossing of the switching threshold of 2.5 V and consequently the delay of the start of the high to low transition of inverter B output. Obviously the output voltage Vout of inverter B is delayed of the same time interval Δt.

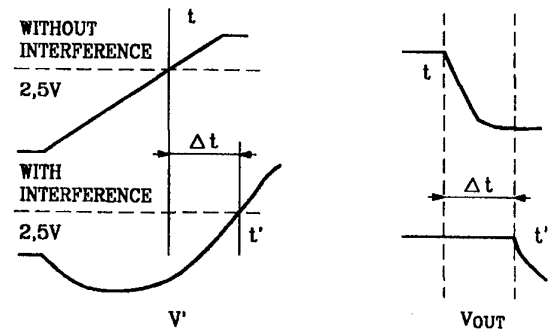


Figure 3 Voltage at the outputs of inverter A and B with and without interference.

Experimental measurements [11] have shown that the phase, amplitude and slew rates of the logic transitions affect the induced delay. It has been proposed to use the following equation to define the worst case interference induced delay

$$\Delta t = \left[\frac{a}{Sinput} + \frac{b}{Soutput} + c\right] V$$

where Sinput is the input slew rate of the logic gate
Soutput is the output slew rate of the logic gate
V is the amplitude of the induced interference at the logic gate input
a, b, c are constants depending on the interference frequency and logic transition polarity.

In order to quantitatively define the suceptibility margins of logic gates due to interference it is possible to define two noise margins.

–The static noise margin which takes into account false switching effects where interference is of sufficient amplitude to cause the change of a logic state.

–The dynamic noise margin which takes into account the propagation delay effects due to low amplitude interference signals.

The static noise [10] margin is defined on the basis of the input/output shown in Figure 4 where:

$V_{out} \geq V_{OH}$ when $V_{in} \leq V_{IL}$

$V_{out} \leq V_{OL}$ when $V_{in} \geq V_{IH}$

with $V_{IH} > V_{IL}$

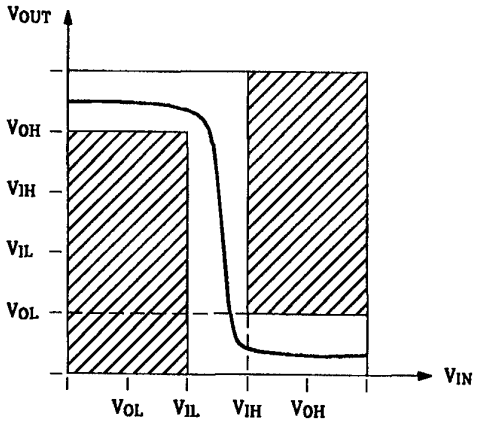


Figure 4 Logic levels at the input and output ports of a logic gate

The high and low static noise margins can be defined as

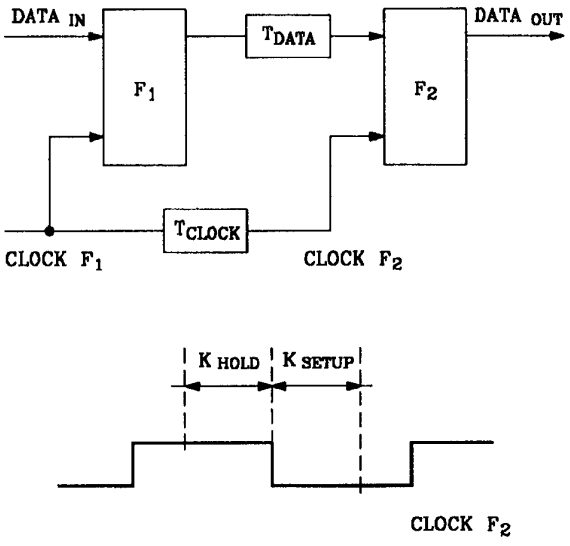
$SNM_H = V_{OH} - V_{IH}$

$SNM_L = V_{IL} - V_{OL}$

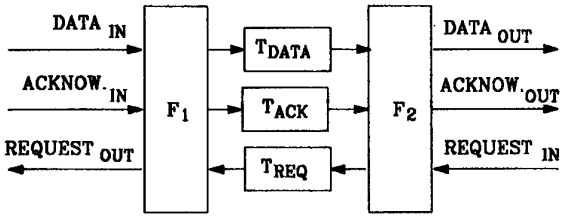
All transfer characteristics which fall within the unshaded area of Figure 4 give acceptable noise margins.

Dynamic noise margins are defined according to the type of circuits under examination. The timing constraints of a synchronous circuit are related to set up time (identified by Kset up)

which represents the minimum time that the data must be stable before the edge of the clock and to the hold time



a) Synchronous circuit



b) Asynchronous circuit

Figure 5 Synchronous and Asynchronous circuits

(identified by Khold) which represents the minimum time that the data must remain stable after the clock edge.

One can define a dynamic noise margin as the difference between the data and clock delays.

$$DNM_S = Tdata - Tclock$$

The dynamic noise margin limits for synchronous circuits are

$$-Khold < DNM_S < K\ set\ up$$

Asynchronous circuits do not have clock signals to coordinate the signal trasfer. The orderly execution of operations is controlled by completion and initation signals. The end of an operation defines the start of the next operation.

The dynamic noise margin is defined as the difference between the data and acknowledgment delays.

$$DNM_A = T_{data} - T_{ack}$$

The dynamic noise margin limit for asynchronous circuits is

$$DNM_A < K_{skew}$$

where Kskew is the positive delay margin of the data relative to the acknowledge signal. There is no negative limit which means that the circuit operates correctly in presence of any time interval by which the data signal preceds the acknowledgement signal.

On the basis of the previous discussion it appears that in order to maintenance adequate static and dynamic safety margins in the presence of interference it is important to control the PCB lay out in order to minimize spurious pick ups. The rules are the same as in the differential and common mode emissions.

A specific aspect of susceptibility effects regards those malfunction problems which derive from the internal structure of semiconductor components. In the past previous studies [15] demonstrated that the primary induced upset is interference signal rectification which is particularly severe in bipolar transistors.

Both analytical and empirical studies [16] showed that rectification efficiency decreases with increasing frequency by almost 40dB/decade and that there is higher likelihood of malfunction in high speed circuits.

The type of technology is also critical. CMOS and Schottky flip–flops have been compared [13]. Both devices show decreasing RF susceptibility with increasing frequencies from 1 to 200 MHz. The measurements on the clock and data ports seem to show that CMOS devices are RF harder than Schottky devices in the high frequency range (to 100 MHz) and that Scottky devices seem harder in the low frequency range.

CONCLUSION

Electromagnetic Compatibility in digital circuits represents an area where it is important to concentrate design efforts in order to avoid major problems of malfunction or even catastrophic failure at system level. This is particularly true for safety critical avionic systems which shall operate in dense and hazardous environmemts. Simple precautions in circuit lay out and/or in the selection of component may help solve difficult situations.

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DISCUSSION

Question: Voltages are, for the components, going from 5 V to 3.3 V or even 1.5 V. What is your opinion in terms of susceptibility effects?

Answer: A decrease in component voltages can affect mainly the probability of "false switching." From our experience, this should increase susceptibility effects only in very high field environments like EMP (electromagnetic pulse) and HPM (high power microwaves) but not in the standard electric field environments up to 200 V/m.

MODULAR CNI AVIONICS SYSTEM

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1. Introduction

Today's aircraft contain a multitude of different radio functions for communications, navigation and identification. The individual radio functions, like VHF/UHF, JTIDS/ MIDS, GPS or NIS, are each handled by an individual piece of equipment consisting of several LRU. In the absence of built-in redundancy, the failure of a single LRU can result in a failure of a radio function. In the future, individual radio functions need to be integrated in a modular system concept, the modular CNI system
(communication / navigation / identification).

List of Abbreviations

BIT	Built-in Test
CNI	Communication/Navigation/ Identification
COMSEC	Communication Security
DME	Distance Measuring Equipment
DME-P	Distance Measuring Equipment Precision
ECCM	Electronic Counter Counter-Measurements
GPS	Global Positioning System
JTIDS	Joint Tactical Information Distribution System
LRU	Line Replaceable Unit
MLS	Microwave Landing System
MIDS	Multifunctional Information Distribution System
MSN	Matrix Switch Network
MTBF	Mean Time Between Failure
NIS	NATO Identification System
RF	Radio Frequency
VHF	Very High Frequency
UHF	Ultra High Frequency

1
Essay acc. authors' own opinion

2. Tracking Reliability and Reconfigurability

A conventional system consisting of twelve radio units with an individual MTBF of 2500 h each, is expected to result in an operational system survival of about 2.1 h, assuming a required reliability of 99%. If, instead, a system is chosen which consists of twelve multifunction units (each also having an MTBF of 2500 h), of which no more than nine can be used simultaneously, then again for reliability of 99%, the system will continue operating for 120 h. In other words, the survival time for the operation of the total system has improved by a factor of 57.

To realize the benefits of such an avionics system three steps are useful. Step 1 is characterized by the minimization of development risk and cost, and realization of multifunctional equipment (like UHF) with different waveforms for upgrades of avionics systems. The advantages of dynamic reconfiguration are achievable with this (e.g. UHF) multifunctional equipments.

Step 2 realizes the multifunctional use over different operational RF waveforms in various frequency bands for all midterm avionics projects. The development risk is low with regard to the longer development time frame. This Step 2 is preparatory for long-term avionics development projects.

Step 3 is characterized by fully modular integrated RF subsystems including all waveforms and avionics performance capabilities like dynamic reallocation of resources and highly reliable BIT structure, etc. these goals are only possible with newest technology and additional forthcoming technology.

The way such a system is used in flight is divided into various phases in which the different CNI functions have different priorities. For example, in the run-in phase for a fighter-bomber the VHF and MLS / DME functions are not used at all, and HF has very low priority. However, if a high-priority CNI subsystem (like UHF) fails, the modular CNI system has a certain potential supply of modules which are either not currently in use or are in use for low-priority tasks, which can be used to take over the function that suffered the fault. This allows the main radio functions to be reconfigured if there is a fault.

This dynamic redundancy leads to a major improvement in system availability.

FIG 1 shows typical reliability functions for a single unit, state-of-the-art conventional system and modular CNI system as in the above example. While the reliability function of a conventional system decreases exponentially starting at t=0, the reliability for a system with redundancy is almost flat. For our example this means that the reliability function of a modular system does not fall below 99% until 120 h have elapsed, whereas this happens for a conventional system after 2.1 h.

3. System Architecture and Type of Modules

The basic modularization of the radio functions (FIG 3) was carried out using a functional top-down division of the transmit and receive circuitry, this being necessary to account for technical specifications and requirements.

When designing an obvious system, there are several CNI architectures (FIG 2) which are receivable, e.g. the architecture for Step 1 closely follows the FIG 2.A and the architecture for Step 2 and 3 is principally like FIG 2 B.
The reconfiguration of failed modules or groups of modules can be achieved using multiplexers of various complexity to switch the signal paths between the modules. The reliability of the multiplexers thus largely determines the reliability of the overall system. Complex multiplexers are more difficult to evaluate than simple ones which might have only two inputs and outputs.

Studies show that the avionics radios can be divided into 11 basic common modules. Each module fulfills a number of subfunctions. The 11 types of modules can realize all possible radio functions today, eight specific module types are needed for transmitting/receiving functions.

A receive system consists of the module family of antenna controller RF module (filter, amplifier, mixer, etc.), synthesizer, data demodulator (A/D converter, filter, correlator, etc.) and data processor.

A transmit system consists of

antenna controller, power amplifier, synthesizer and data processor.
The modules are controlled via a fast fiber-optic bus. Thus CNI radio functions can be built up from just eight module types, including the audio processor and the avionics bus interface. This architecture makes it possible to configure the following radio functions: HF, VHF/UHF, GPS, MLS and DME-P. More complex systems for VHF/UHF with ECCM; and COMSEC, MIDS/JTIDS or NIS require additional modules; however, the basic structure does not need to be changed.

From the above considerations, the CNI system architecture shown in FIG 4 resulted. This architecture is based on technology which is available today, or will be available in the immediate future. For example, multiplexers for analog RF signals are extremely difficult, whereas digital multiplexers are available even for very fast signals. The fiber-optic bus controlling the system as well as the connection to the avionics bus are designed with dual redundancy.

4. Present System Architecture

The system architecture described above permits a multitude of configurations for radio functions which are currently handled by specialized individual units. The various modules are supplied with setup data via the control bus and are thus set for a particular function. This allows a defined, preselected array of functions - for example from VHF to GPS - to be allocated in various ways to different branches of the CNI system or, in other words, configuration of a preselected array of functions under software control alone. So if a function that is currently needed is out of commission, the software can reconfigure this function in a simple way: it transfers one branch from a function which is not so important in the current phase of the mission to the particular function which is urgently needed and has failed (FIG 5). This quite obviously provides a considerable improvement in reliability and availability of the total system without forcing the aircraft to carry dead-weight redundancy.

The implementation of a modular CNI system appears more complex than previously discussed. To ensure the complete range of functions, we need different module types: in addition to the eight modules needed for receive and transmit paths, we need a data correlator, a transmit modulator and a control-bus interface. These eleven types also have a number of subtypes which are tailored to the technical and functional requirements of each CNI function Thus it seems neither sensible nor practical, for example, to provide a power amplifier which could handle the entire frequency range from HF to EHF. Another example is certain complex correlation functions needed for the NATO identification system (NIS).

Each of the modules must have a built-in test (BIT) feature as well as a nonvolatile memory for storing BIT results for later analysis. The BIT on module side must be enhanced with overall system functional testing. These overall tests help eliminating many false alarms and provide means to

achieve highly reliable systems for high reliable systems.

For simple and fast identification of a faulty module by maintenance crews, each module is provided with a go/nogo indicator. Integrated EMC features plus the fiber-optic inputs and outputs make the system a "green island" in the polluted avionics environment. With the number of different modules being limited, identifying of faulty modules is easy, as they are replaced in the flight-line area. All of this means benefits in terms of spares handling and maintenance planning, and thus reduces life cycle costs.

The data transfer between the modules (FIG 6) is carried out via the CNI control bus (clock, settings data, BIT) and special point-top-point data links (fast raw data). The total data transfer runs, as far as possible, via fiber-optic links to cut EMC problems, both internally between the CNI system units and externally (e.g. EMP). The control bus is distributed via star couplers in the rear of the rack. The CNI system is connected to the rest of the avionics system via the avionics bus, which only has to carry a small amount of data since all the internal CNI data transfers are handled separately.

Mechanically, the design is based on the line-replaceable-module (LRM) concept, which may include various widths of the hardware modules (FIG 7). Special cold plates conduct the dissipated heat to the ventilation channels in the top and bottom of the rack. The racks come in various widths for the space available and the function required. The modules are fully replaceable having plug-in connectors at the rear of the rack to make it easier to replace them.

5. CNI System Options Dependent on Technologies Performance

The above described technological basic idea comes from the US yet and is not limited to a special technology. Nevertheless the degree of integration of future CNI system is dependent on available technology.

Current CNI platforms require the integration of a large number of various communications, navigation and identification (CNI) units. Each function is performed by a specialized piece of avionic equipment, each dedicated to one particular function, such as HF, VHF, JTIDS/MIDS, GPS and/or NIS. In a modular CNI system these functions have to be integrated in an embedded modular system.

The forecast of CNI system options for future, military platforms is based on three technology levels: low, medium and high.

For each of the three technology levels, the following assumptions have been made:

a) Modular construction
b) Modular size in the order of 15x15x3 cm for all three technologies.
c) A module weight of 0.6 kg is assumed.
d) In the medium and high technologies the modules have a multifunctional use.

e) A maximum of 5 functions would be used simultaneously.

The three technology levels are further elaborated below.

Low Technology Level Solution

The low technology level solution incorporates stand alone modules; each module having a different function. Interoperability with different systems is achieved by dedicated hardware and redundancy achieved by the addition of dedicated modules. Antenna design is of dedicated conventional loop, whip and blade design.

Medium Technology Level

In the medium technology level solution the architecture is based on modules which have multifunctional use. This design incorporates a common modular design utilizing state of the art components. The modules are software controlled and because of their multifunctional design, no hardware redundancy is required (except for inertial sensors) due to dynamic reconfiguration. Multifunctional antennas are also embodied to reduce the mass and volume required. Interoperability is achieved by dedicated software.

High Technology Level

In the high technology level CNI suite, a modular design similar to that of the medium technology is used, However, the design utilizes expected future component developments. The number of required modules is further reduced due to increased commonalty. Phased array antennas, covering the entire CNI frequency spectrum, will be used. The system features built-in interoperability. Sensor technology will continue to provide higher accuracy and reliability with lower weight and cost.

The modular system design must provide maximum functionality with a minimum number of modules of different types. The system overhead shall be optimized by means of technology and system functional integration in order to realize all CNI functions within less weight, volume and power consumption, when compared to a LRU of a currently federated architecture.

The module design will be influenced by available technology related to a specific avionic program. The module interfaces and functions will need to be standardized in order to allow for improvements in technology and internal functionality without changing the modular CNI system architecture.

For design, development and test of CNI modules, a set of consistent tools shall be defined within a program.

Some of the basic requirements are of highest importance when establishing a concept for the physical integration of an advanced modular CNI system:
(a) Modularity
(b) Improved maintainability
(c) Better accessibility
(d) Low vulnerability
(e) High packaging density
(f) Growth potential
The CNI modules should be mounted normally in racks which interconnect, support and supply cooling to the modules. In addition, these racks and their mountings should attenuate environmental stresses to levels for which the modules are designed.

The modules should be allocated to physically separated racks to enhance survivability in the event of battle damage.

Summary

The better performance of modular CNI systems is due to higher system efficiency and reliability. A modular CNI system has growth potential: it allows the introduction of new technologies, or adaptation of the system to new functional requirements, in a simple and inexpensive manner. Thanks to the low maintenance and costs of spares handling, life cycle costs are reduced drastically. The modular design of the CNI system makes it possible to use it in a multitude of avionics systems. Resource sharing and dynamic redundancy, i.e. the ability to reconfigure faulty functions, provides a large improvement in reliability, availability and survivability of the system.

DISCUSSION

Question: Fault localization through BIT is very important for a modular reconfigurable system. What degree of localization can be achieved for the RF elements?

Answer: Fault localization is on two levels:

- Level One: the fault localization is on the module level.

- Level Two: the fault localization is on a functional row of modules, which fulfill a special RF function (waveform, etc.)

On both levels, different fault localization mechanisms are applied, i.e., initiated BIT and FTAG. The failure isolation is limited to one module; therefore, it's only necessary to have the localization of a failure to determine the defective module.

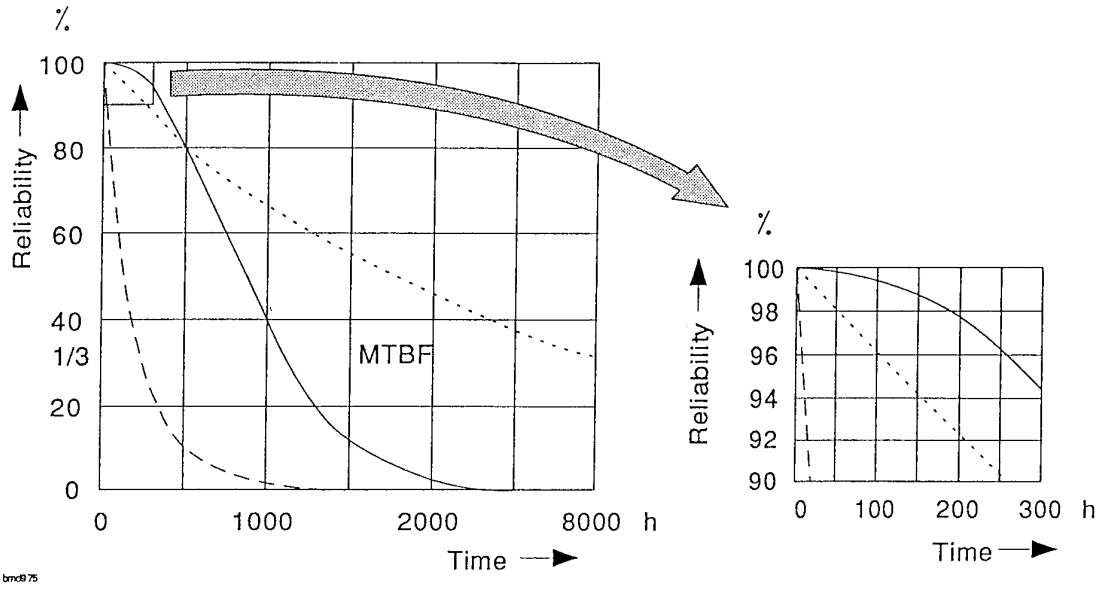


FIG. 1 Typical reliability curves for individual unit (pointed line), conventional system (broken line) and modular system (full line)

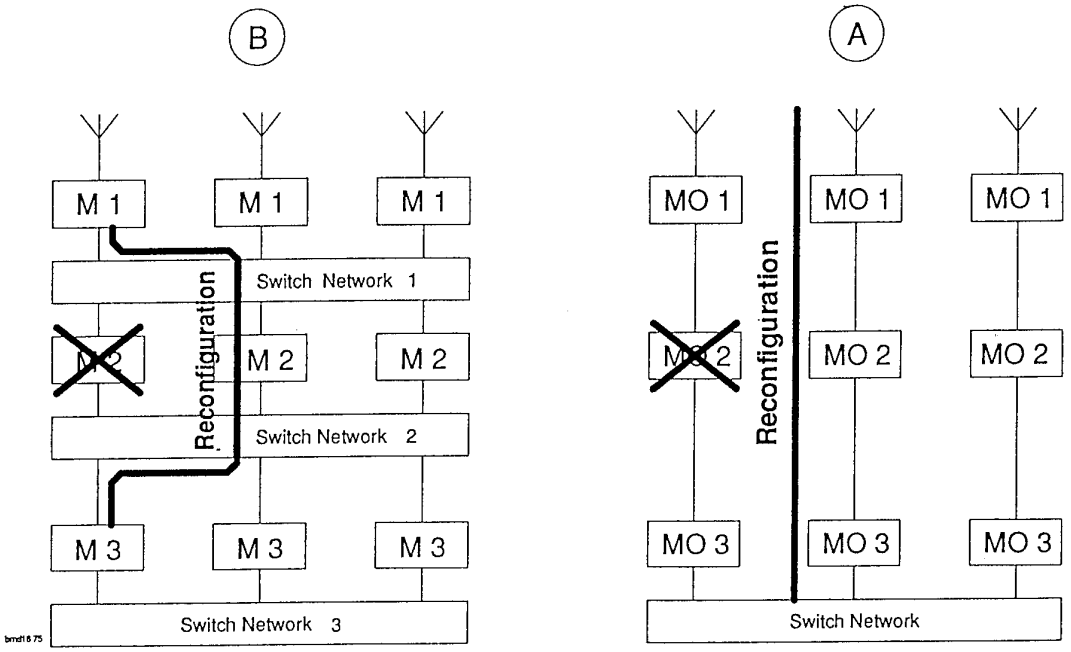


FIG. 2 Several systemarchitectures with different possibilities of reconfiguration

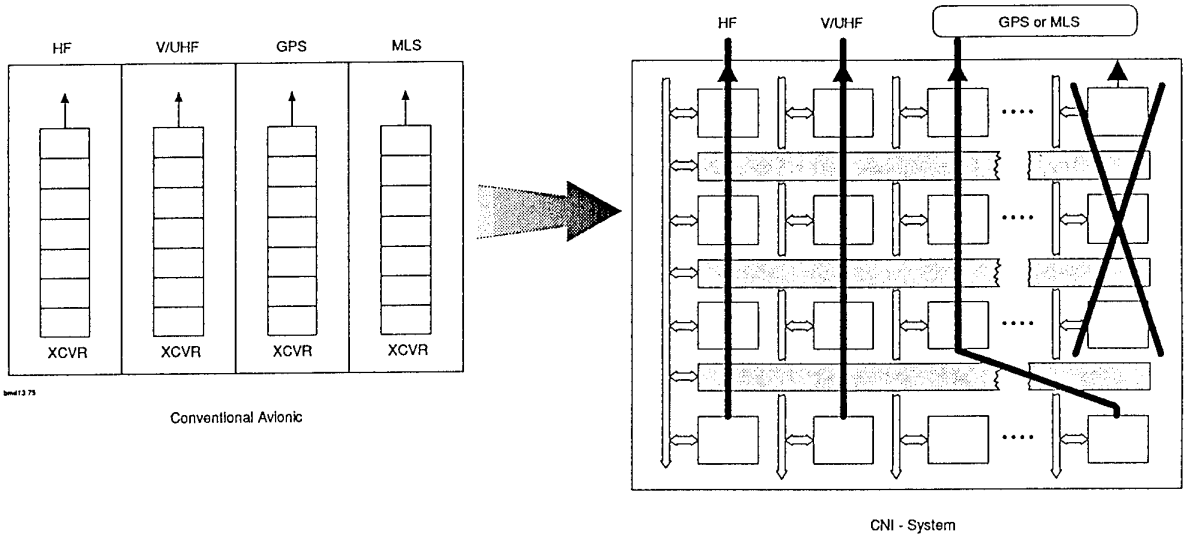


FIG. 5 In conventional system (left), fault in a function means loss of that function. Modular CNI system (right) maintains functionality by reconfiguring faulty function.

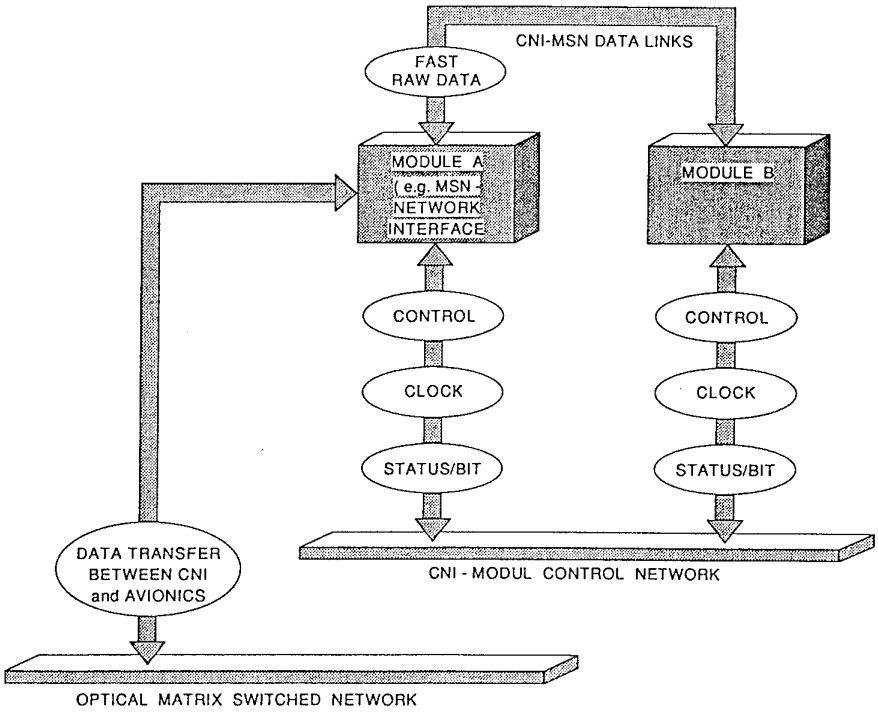


FIG. 6 Data transfer within CNI systems, and between CNI system and rest of avionics

bmd14 75

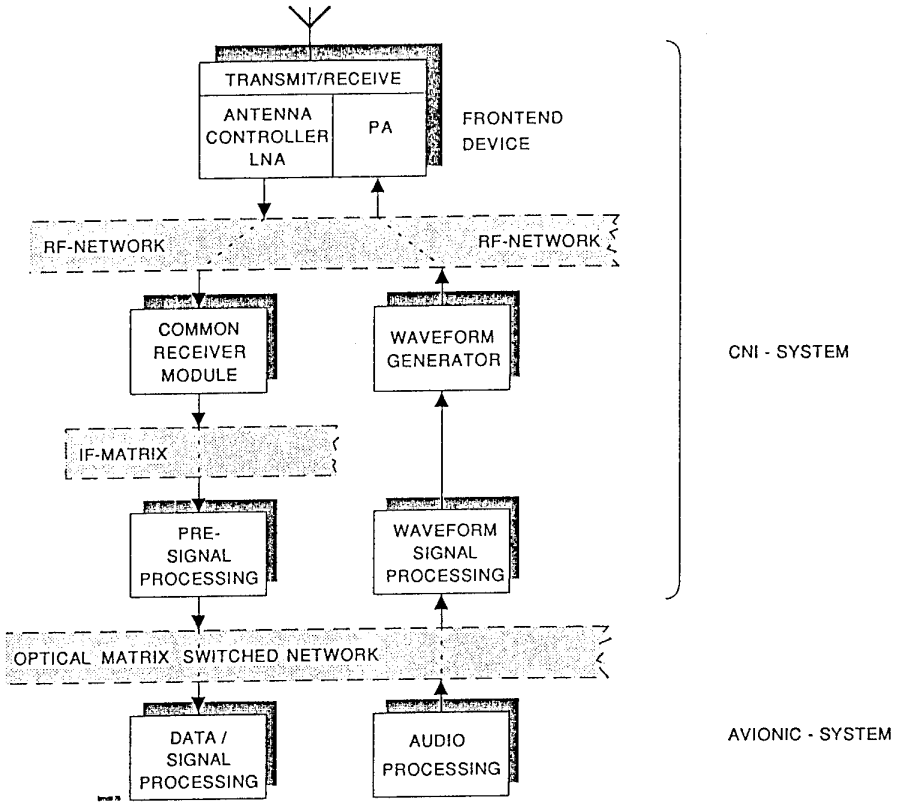


FIG. 3 Basic structure of radio functions in modular CNI system

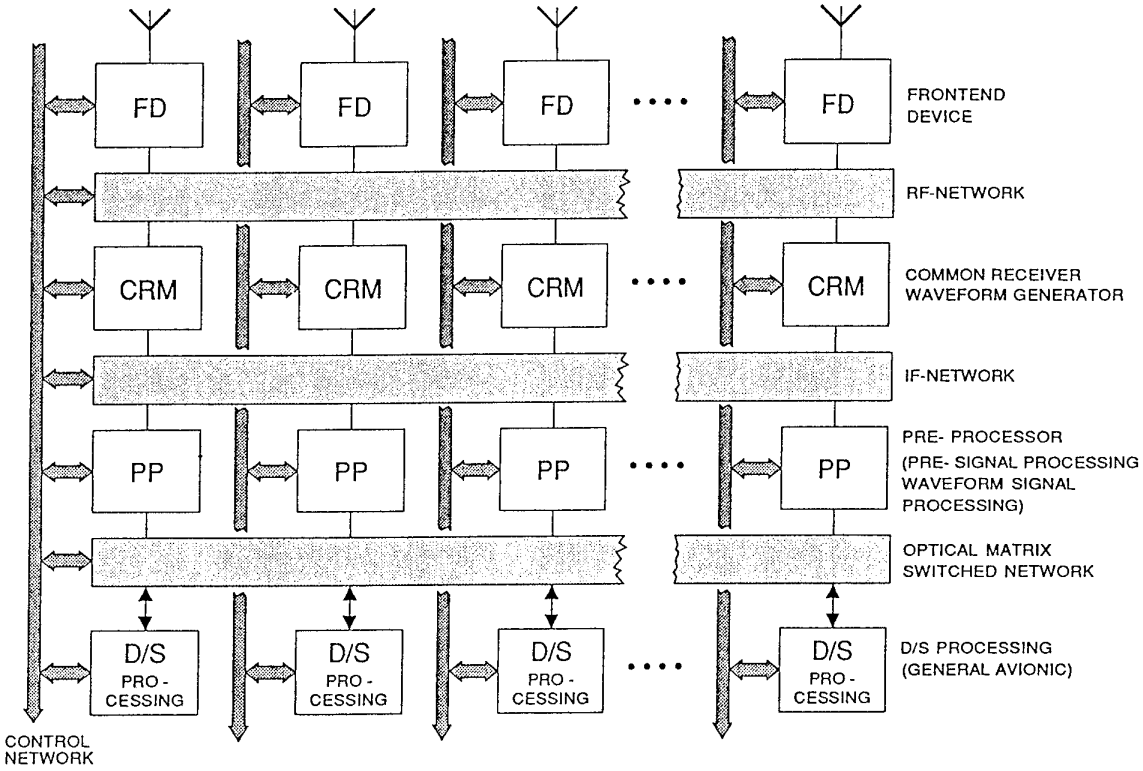
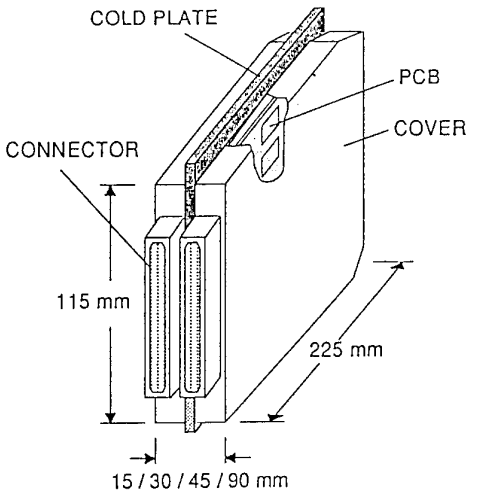


FIG. 4 CNI system architecture



List of connectors

Fiber optic connectors	up to	12	(9 data, 1 instructions, 2 control)
RF-connectors	up to	5	(4 RF, 1 IF)
Power pins	up to	6	
Discrete lines	up to	20	

bmd15 75

FIG. 7 Mechanical design of line replaceable module

LOW	MEDIUM	HIGH
. stand alone modules	. modular design based on state of art components	. modular design based on future component development
. different modules for different functions	. common multifunctional modules	. fewer multifunction modules due to increased common features
. limited SW	. SW control of module functions	. tailoring of mission depending waveforms
. state of art components	. HW redundancy reduced due to dynamic reconfiguration	
. multiband V/UHF antenna	. good resource management	
. HF loop antenna	. multifunctional antennas	. structural antennas with adaptive phased arrays
	. flexible selection of CNI waveforms	. phased array antennas covering the entire CNI frequency range
. interoperability by specific HW	. interoperability by dedicated SW	. built-in interoperability

FIG. 8 Key Parameters of three Technology Levels

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14. Abstract

A critical impediment to significantly improving the performance of digital airborne electronics or avionics is the limitation posed by current electronics packaging concepts. This symposium brought together experts from seemingly diverse, but interlocking disciplines ranging from logisticians to digital designers to mechanical engineers to establish the current baseline in digital packaging, failure modes of the electronics and support problems. Trends in both supportability and processing were described for early 21st century application. Along with the projections of asymptotic increase in signal, image and data processing, dramatic increases in thermal densities, chip interconnects, correctors and backplane traffic were described. Current packaging approaches were shown to be totally inadequate, both from performance and supportability perspectives. A system solution for packaging light weight, ultra-reliable and high performance real time digital processing was presented. Papers were presented on how diverse new technologies could be integrated to provide a system solution. Avionics currently comprise almost one-third of the flyaway costs and over one-third of the support costs of modern day fighters. These percentages are expected to steadily grow unless fundamental changes are made in the manner in which avionics are designed, manufactured, packaged, tested and supported. Advanced packaging technologies hold promise for achieving greater performance while holding down costs. Significantly reduced costs will result from the standardized digital electronic modules which are used in all of the avionics sub-systems. If these modules can also be used in multiple weapon systems, then the large numbers required will drive down costs.

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