MicroModule Systems™
Multichip Solutions

December 19, 1994

ARPA/ESTO
Dr. Nicholas J. Naclerio
3701 North Fairfax Drive
Arlington, VA 22203-1714

Subject: Contract MDA972-94-C-0001 - Phase I Program Completion and Final Reports (Contract Line Item Number 0002)

Reference: (a) Section C-2, Contract Line Items Number(CLIN) 0002AC, 0002AD, 0002AE, 0002AF, 0002AG and 0002AH

Enclosure: (1) Phase I Final Report (1 Copy)

Dear Dr. Naclerio:

In accordance with Reference (a), MicroModule Systems(MMS) is pleased to forward its report summarizing the results and findings for Phase I of the program. This information, which involved characterization of the electrical, mechanical, thermal and reliability features of using the interconnect for burn-in and test applications, was presented in our program briefing held at MMS' facilities on October 6, 1994.

The report itself addresses findings resulting from MMS' evaluation of several critical areas which impact design and use of the test membrane and carrier including, contact resistance and measurement, electrical characteristics, cavity size, backing material and approach, wafer material as well as bump uniformity. The report also includes a specification sheet for 1, 2 and 3 layer interconnect designs.

With this report, MMS has now completed Phase I of the program and based on the favorable findings, is poised to commence Phase II and III upon receipt of authorization to proceed from ARPA.

As required by Section F-3 of the above contract, copies of this report are being forwarded to the destinations listed below.

As always, should you have any questions, feel free to contact Mr. Fariborz Agahdel or the undersigned.

Sincerely,

Rick Strickland
Director, Government Programs

cc: F. Agahdel
S. Ulrey(ARPA/CMO)

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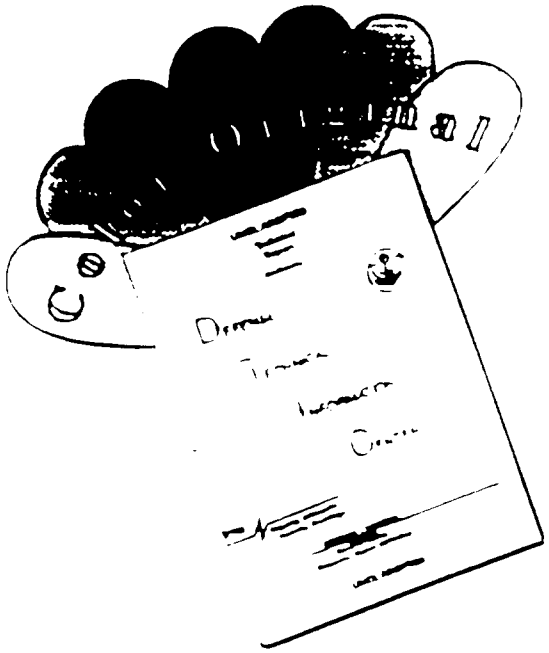

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Characterization of MMS' Interconnect for Bare Die Test & Burn In

Sponsored by:
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Interconnects for Bare Die Test

Program Summary
(Phase I)

The Interconnects for Bare Die Test Program sponsored by the Advanced Research Projects Administration (ARPA) under Contract MDA972-94-C-0001 is segmented into three complimentary phases which, when completed, will result in qualification and demonstration of a flexible cost effective solution for test and burn-in of bare die utilizing candidate IC parts supplied by selected vendors.

Research thus far has concentrated on identifying and quantifying those structural factors which are critical in determining test interconnect design. For the test membrane to achieve contact with all die pads of a given IC footprint, careful balance of these interdependent factors must first be achieved.

The first phase of the Program has focused on characterization of the interconnect to be used as the test membrane. The primary objective here was to understand the electrical, mechanical, thermal, and reliability characteristics of this membrane and to establish conclusions relative to the overall technical feasibility of this approach. Work accomplished under this phase allowed MMS to better understand the criteria and factors which affect overall design of the test interconnect structure.

Findings from Phase I have confirmed the feasibility of the approach with specified recommendations in carrier and membrane design to optimize die contact integrity.
This report summarizes the results and findings of MMS' evaluation into the following major sections:

Section	Title	CLIN
1	Mechanical Characterization	0002AC
2	Interconnect Electrical Characterization	0002AD
3	Product Size Characterization	0002AC
4	Membrane Support Characerization	0002AG
5	Low CTE Substrate Material	0002AF
6	Increased Contact Point Height	0002AG
7	Contact Point Height Uniformity	0002AG
8	Carrier Usabilty Tester	0002AH
9	Resistance Measurement System	0002AE

Each chapter contains a summary of conclusions resulting from the focused research and may, in some cases, include tables, specifications, and presentation material which was generated as the result of this research. Table 1 in this section summerizes the results of the technology characterizations.

MMS has also included a brief section highlighting Recommendations for Further Research based on Phase I findings and conclusions.

MMS appreciates the opportunity of working with ARPA on this important undertaking and we look forward to use of these Phase I findings in supporting Phase II and III qualification of several membrane designs for use in testing actual parts.

Technology Characteristic Summary Table

Parameter	1 Layer	2 Layers	2+ Layers	3 Layers
Min Pad Pitch	3 mils	3 mils	3 mils	3 mils
Min Pad Size	Dependant on Die size , Subs. material, bump height (See Sec. 1)			
Min Force Req.	Dependant on Die size , Subs. material, bump height (See Sec. 1)			
Max. Force Allowed	Dependant on Die size , Subs. material, bump height (See Sec. 1)			
Mechanical Shock	To be determined in Phase II (based on real application)			
Max. Die Size	None. Can accomodate varrying sizes by varrying the product size.			
Max. Die Thickness Tol.	Depends on force delivery mechanism tolerance. MMS/TI bare die carriers can tolerate upto 1 mils of variations.			
Min. Appl. Cycles	To be determined in Phase II (based on real application)			
Max. Cycles Between Cleanings	To be determined in Phase II (based on real application)			
Impedance Control	Coplanar	Mixed Coplanar & Microstrip	Mixed Coplanar & Microstrip	Microstrip
Signal Impedance (Ohms)	70 Ω	70 Ω, segmented in series with 50Ω	50 Ω	50 Ω
Crosstalk Backward (KB) Forward (KF)	< 7% (to be measured)	< 5% (to be measured)	<5% (to be measured)	<5% (to be measured)
Max. Signal Frequency (@ 5 signal per Pwr & Gnd pins, Rise time 10% of 1/f 0.5 V noise margin)	22 MHz	44 MHz	114 MHz	> 1 Ghz Limited by socket
Max. Pwr Inductance (10mm die size)	4.5 nH /Connect	2.25 nH /Connect	0.88 nH /Connect	0.05 nH /Connect
Power Connection Resistance/Connection	0.279 Ω (Avg.)	0.196 Ω (Avg.)	0.141 Ω (Avg.)	0.025 Ω (Avg.)
Ground Connection Resistance/Connection	0.048 Ω (Avg.)	0.030 Ω (Avg.)	0.011 Ω (Avg.)	0.028 Ω (Avg.)
Power Common Mode Resistance/Connection	NA	0.004 Ω (Avg.)	0.005 Ω (Avg.)	0.013 Ω (Avg.)
Ground Common Mode Resistance/Connection	0.025 Ω (Avg.)	0.017 Ω (Avg.)	0.006 Ω (Avg.)	0.013 Ω (Avg.)
Intrinsic Bypass Capacitance (Avg.)	4.0 pF /Connect	1.47 nF	1.54 nF	5.29 nf
Max. Power Die Contact Socket Contact	> 0.2 A /Contact 1 A / Contact	> 0.2 A /Contact 1 A / Contact	> 0.2 A /Contact 1 A / Contact	1A /Contact 1 A / Contact

Summary of Research and Findings

The overall objective of Phase I was to characterize the electrical, mechanical, thermal and reliability aspects of using a thin film interconnect for IC test and burn-in applications. The approach implemented was to modify several recently developed test vehicles representing variations in dimensional characteristics, pad pitch and number of layers to use as candidate structures for characterizing the critical mechanical dimensions of the target structure. A description of these test vehicles is provided in Section 1. these test vehicles were selected for use on this program to better match the structure type which is suited for existing burn-in and AC test applications of ICs.

A Summary Test Interconnect Specification is provided which delineates standard interconnect parameters for 1,2 and 3 layer membrane designs. These parameters were determined based on the initial Phase I characterization and may, therefore, continue to be adjusted, clarified and/or supplemented as additional test and evaluation data becomes available.

Following the Specification Table, MMS presents a summary of critical research areas by sections each delineating the objectives, approach and conclusions reached from this research.

The following summary of MMS' research is provided. As mentioned, quantitative results which support conclusions reached are provided in the respective report section:

1. Mechanical Characterization

The purpose of this research was to understand the structural characteristics of the interconnect by measuring contact resistance at the intersection of the die and test membrane. MMS concluded that the force necessary to make contact on each pad is dependent on such factors as pad pitch, number of contact points, die size, pad arrangement, membrane structure and contact point size. Contact resistance of the test vehicles was optimized at between 12 and 13 pounds with a corresponding contact resistance value of 45 miliohms. The research also indicates that there is no significant correlation between contact resistance value and pad pitch. Supporting information is provided in Section 1.

2. Electrical Characterization

The purpose of this work was to characterize the electrical integrity of the test frame device as well as understand the impact of different test frame design configurations on the electrical performance of the device itself. The approach was to measure and evaluate the AC/DC characteristics of different test frame designs including one layer (coplanar), two layer (part microstrip/part coplanar), modified 2 layer (all microstrip) and 3+ layer (full planes for power and ground). This includes signal lines, power distribution and contact to IC. In addition, we wanted to understand the impact of different test frame designs on the electrical performance of the device itself for the purpose of identifying test frame configurations which would be appropriate for a given application by establishing standard interconnect parameters. As the result of this effort,

MMS was able to identify critical electrical measurements and parameters based on given signal line dimensions for each of the coplanar and microstrip test vehicles selected including signal impedance, variations in signal impedance, crosstalk, power inductance, signal frequency, bypass capacitance and maximum power. These measurements, which are summarized in Section 2 can be used as design criteria for determining the optimum test frame configuration for a particular application.

3. Product Size Characterization

The purpose of this investigation was to identify the smallest test membrane size for a corresponding die size. Optimum size is a function of the membrane itself as well as the aluminum frame structure. The goal was to determine the optimum gap between the edge of the die and the edge of the aluminum frame. results indicate that with die size of 550 mils X 550 mils and bump size of 45um diameter with minimum of 4 mil pad pitch, a 45 mil gap is the optimized size. In evaluating the optimum aluminum frame design, MMS analyzed the state of the membrane/frame structure using a model which predicts bow and warpage based on the CTE of the membrane and aluminum frame at temperatures ranging from 25 degrees C to 100 degrees C. To use the results as an accurate prediction tool to optimize frame width, the initial pre-stressed condition of the structure must be better understood. The analytical tool was found to be useful for predicting the change in stress based on different frame dimensions and location on the wafer during processing.

4. Membrane Support Characterization

The purpose of this effort was to determine the maximum size cutout that may be deployed using material under the BDBITS' membrane without affecting the contact integrity of the bumps to the die under test. It was determined that if the layup, or support material is cut out (like a picture frame) so that it better supports the contact bump area, then the potential for damage to the die is minimized. On the other hand, if sufficient support is not provided under the contact bumps on the membrane, the electrical performance
of the BDBITS' by creating higher contact resistance or opens. Five support structures ranging from a cutout size of 526 mil to 551 mil square consisting of both silicone rubber and Kapton were evaluated. The centerlines of opposing rows of contact bumps on the TV20 test vehicle were 543 mils apart, therefore, the bumps were completely off the layup materials in the 551 mil case and well away from the edge of the layup materials in the 526 mil case. The relationship between improper support from the layup material and the increase in contact resistance, or even opens was evaluated for each of the cut out sizes. The results showed that as the cutout size increases from 531 mil, the number of contacts with resistance's greater than 0.2 microns as well as the number of opens increased significantly. conclusions indicate that
for any given device, the inner edge of the contact bump must be 6 mils or more outside the inner edge of the layup support material. Supporting information is provided in Section 4.

5. Low CTE Substrate Material

The objective here was to evaluate different substrate materials with Tce close to silicon in order to accommodate smaller pad openings and larger die sizes in some of the existing and future ICs. From the preliminary calculations of bump mark length vs. CTE on Al wafers, it was determined that the dominating factor effecting thermal mismatch was the Al frame itself rather than the PolyImide film. Several different candidate substrate materials were evaluated including Si, Kovar, Invar and Molybdenum. Moly appears to be the most promising material based on Phase I evaluations. However, although Moly can be used in its present form, the higher cost and lower yields will require further improvement of the incoming material. In particular, improvements are required relative to weight reduction, flatness and surface condition. It is recommended that incoming material specifications be developed with the Moly supplier. Supporting information is provided in Section 5 of this report.

6. Increased Contact Point Height

The purpose of this research was to evaluate different approaches for increasing the height of the contact points (bumps) on the membrane without increasing it's diameter. The bump height increase is deemed to be necessary to allow die with thicker passivation layer to be used. Two different options were considered for increasing bump height: increase the height of the bump and deepen the surface of the PolyImide. The process used was to increase photoresist thickness and then expose using both a proximity and projection aligner. MMS concluded that both photolithography processes will yield taller bumps. However, the projection aligner produced a more structural uniform bump. The proximity aligner produced more rounded or mushroom shape because of the optical diffraction. Thicker photoresist produces smaller final bump diameter with the same plated bump height. PI thickness of 12 microns appears to be durable enough for normal operation of the membrane.

7. Contact Point Height Uniformity

The purpose of this research was to evaluate means of increasing uniformity/planarity of the contact points on the substrate. The objective is to make the bump height variation between adjacent pads as small as possible for a given membrane compliance and pad pitch. MMS evaluated two approaches in improving the bump height uniformity: particle contact points and particleless bumps. To reduce the potential of bump height variations caused by non-uniform particle sizes, MMS evaluated methods for classifying and batching particles. It was concluded that both air classifiers and jet mills can be used to make uniform particles. Evaluation of particleless bumps indicates that the durability is comparable to that of bumps with particles while bump height uniformity is better. Although contact resistance's decrease more uniformly across the die using particleless bumps the total force needed to make contact is the same for either approach.

8. Carrier Usability Tester

The goal of this section was to identify a method, or tool for determining the functionality and condition of the test carrier between usage. This would allow the user to know when to replace the carrier due to damage and wear. Such a tool can be placed at the beginning or the end of the operation and would be independent of the process, product, or application. Two different approaches were evaluated both of which would be to integrate a measurement unit into an existing carrier pick and place system. The first approach was to test the carrier using a coupon which would be inserted into the carrier and then measuring the resistance of the traces and the contacts through the coupons. The cost of such a system appears to be prohibitive at this time. The second configuration verifies that the die pads are making the proper contact with the die carrier during or after the placement of the die carrier or after the placement of the die into the carrier. We believe this configuration can be made inexpensively enough to be adaptable into high volume manufacturing applications. However, further analysis of such a system with respect to existing carrier technologies and their applications in high and low volume manufacturing operations is recommended. More details of these findings are provided in Section 8 of this report.

9. Resistance Measurement System

The primary objective here was to design a die handling system that would accurately place a die on the test membrane and apply a controlled, user selected downward force on the die while electrical resistance is measured. This machine requires a force mechanism for testing and measuring contact resistance. A MRSI pick and place machine was selected as the baseline system. The system was then modified to incorporate some basic mechanical features including THETA stage lock-in as well as a more reliable force actuating and pressure measurement system. The modified system was tested and evaluated with successful results. Additional information on the results of this modified system are provided in Section 9.

SECTION 1

MECHANICAL CHARACTERIZATION

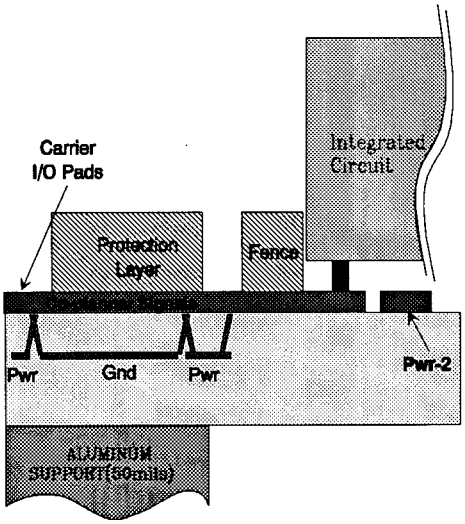
The objective of this research was to understand the mechanical characteristics of the interconnect. This information can be used in applying the technology to different applications, with different pad pitches and die sizes.

Process

Several different test vehicles were used in this project, which are discussed below:

- **TV20**. A two layer interconnect designed for 4 point Kelvin style measurement, using a blank die.

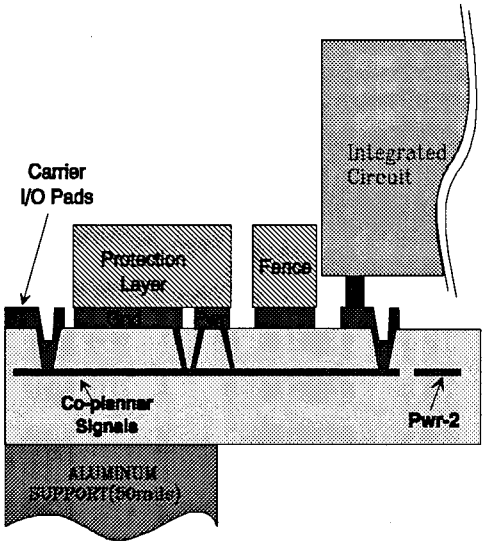
  Die Size : 0.550" X 0.550"
  Die Contact points : 372
  Pad pitches : 4 mils, 5 mils, 6 mils equally distributed on all four sides
  Die to substrate 4-point measurements : 72
  Substrate Size : 1.3" X 1.3"
  Substrate to socket Pins : 248
  Substrate to socket 4-point measurements : 36
  Substrate Membrane size : 0.750" X 0.750"



TV20 Cross-Section

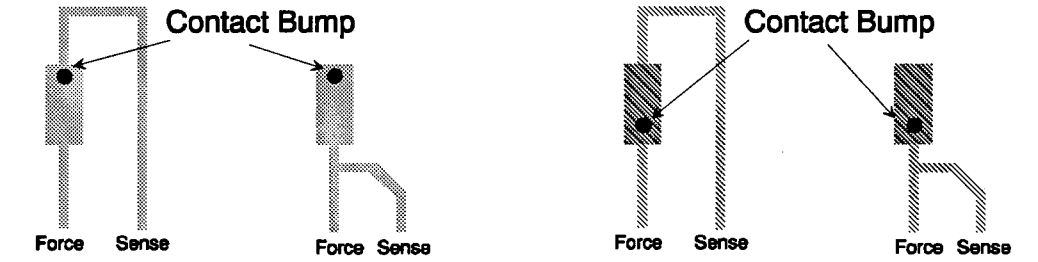
- **B0008**. A two layer interconnect designed for 4 point Kelvin style measurement, using a blank die.

  Die Size : 0.550" X 0.550"
  Die Contact points : 372
  Pad pitches : 3 mils, 4 mils, 5 mils equally distributed on all four sides
  Die to substrate 4-point measurements : 72
  Substrate Size : 1.3" X 1.3"
  Substrate to socket Pins : 248
  Substrate to socket 4-point measurements : 36
  Substrate Membrane size : 0.750" X 0.750"



B0008 Cross-Section

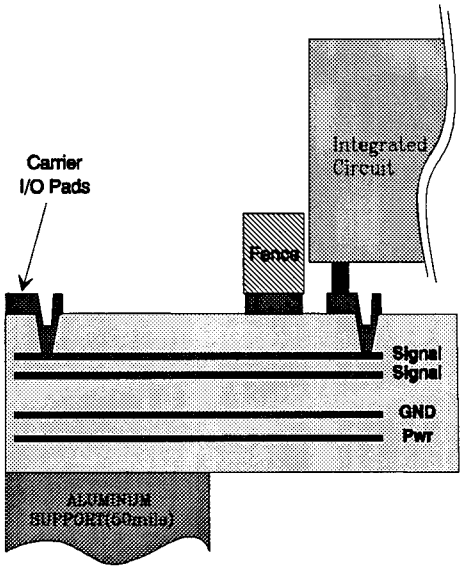
Both TV20 and B0008 contained two different connections at the contact points which are shown in the following figure as Type I and Type II. The purpose of these two configurations were to detect compliancy issues with the way a trace is connected to the contact pads.



TV20 & B0008 Substrate To Die Contact Points' Pad Types

- **B0011**. A three layer interconnect designed for 4 point Kelvin style measurement, using a specially HP designed die. The design and evaluation of this test vehicle was done in cooperation with HP Labs, in Palo Alto, CA.

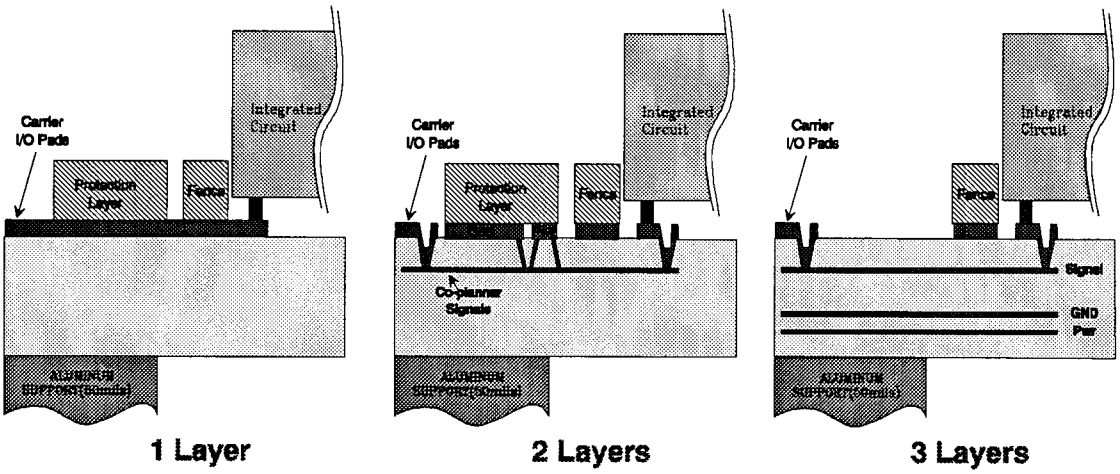
  Die Size : 0.590" X 0.690"
  Die Contact points : 2789
  Pad pitches : 0.250 mm
  Die to substrate 4-point measurements : 60 individual contacts, ~ 1800 contact chains.
  Substrate Size : 2.126" X 2.126"
  Substrate to socket Pins : 684
  Substrate Membrane size : 1.52" X 1.52"



B0011 Cross-Section

- **B0023, B0024, B0025, B0026**. One, 2, 2+ and 3 layers structures respectively. These test vehicles were designed for 4 point Kelvin style measurement as well as electrical characterization of the different structures, using a blank die.

  Die Size : 0.408" X 0.394"
  Die Contact points : 155
  Pad pitches : 4.9 mils
  Die to substrate 4-point measurements : 13
  Substrate Size : 1.25" X 1.25"
  Substrate to socket Pins : 280
  Substrate to socket 4-point measurements : 0
  Substrate Membrane size : 0.800" X 0.800"



B0023, B0024, B0026 Cross-Sections

Notes:

To reduce the cost of fabricating all different options, they were all put onto the same mask, along with B0011.

B0025 is the same as B0024 with the exception of the GND plane on the top layer extending to the edge of the die. This allows for better controlled impedance for the signals, as it is further explained in the Electrical Characterization section (Section 2) of this report.

Contact Resistance Measurements Tools

Die: Contact resistances were measured using blank Aluminum dice (Coupons).

4 Point Measurements : MMS used a Keithly 580 MicroOhm Meter with a 100 point switching matrix. Refer to "Resistance Measurement" Section (Section 10) in this report for more details on the configuration of the system.

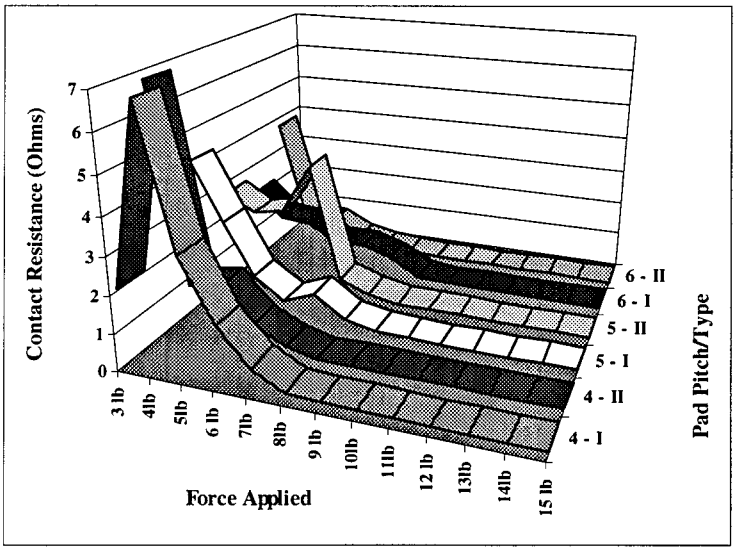
Force Applicator :

- A modifed MRSI - 503 system. Refer to "Resistance Measurement" Section (Section 10) in this report for more details on the configuration of the system.
- Standard carrier caps with different forces.

Results

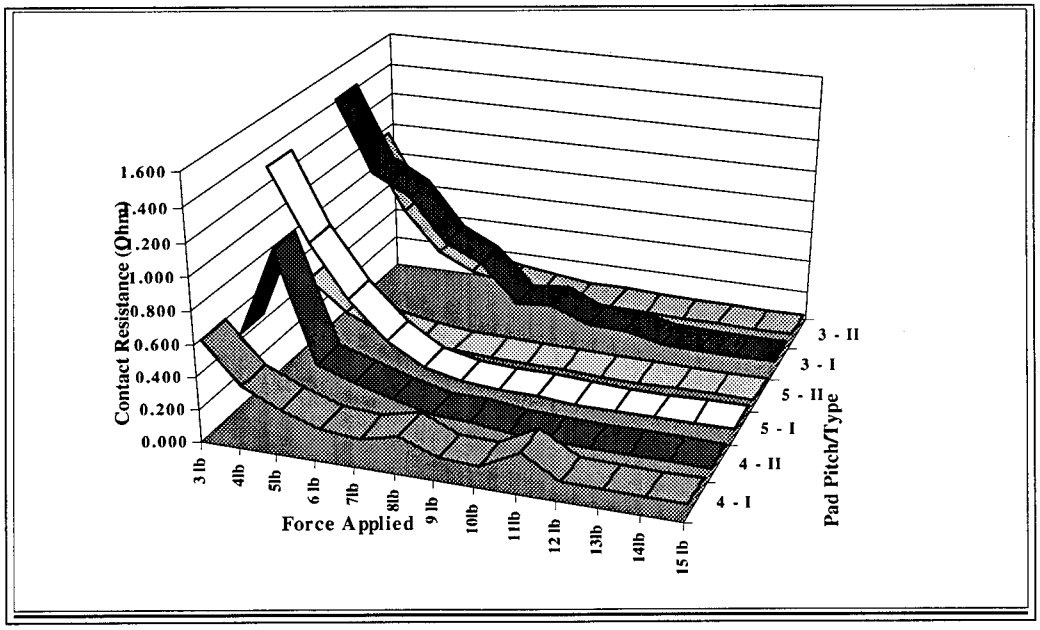
The following pages contain the contact resistance measurements for the above mentioned test vehicles, with respect to different forces.

Carrier #	Pad Pitch (mil)	Pad Type	Force Applied (lbs)												
			3 lb	4lb	5lb	6 lb	7lb	8lb	9 lb	10lb	11lb	12 lb	13lb	14lb	15 lb
862_10	4	I	1.476	1.091	1.158	0.454	0.130	0.093	0.078	0.071	0.067	0.059	0.058	0.057	0.057
862_09	4	I	2.380	1.471	0.847	4.568	2.160	0.266	0.165	0.119	0.097	0.085	0.061	0.086	0.079
862_07	4	I	1.440	0.525	0.256	0.149	0.109	0.103	0.094	0.094	0.081	0.070	0.065	0.066	0.065
862_05	4	I	1.277	0.942	3.006	1.786	0.474	0.318	0.237	0.190	0.110	0.074	0.073	0.068	0.065
862_03	4	I	3.780	30.022	10.687	0.804	0.206	0.103	0.080	0.066	0.058	0.056	0.053	0.051	0.050
Avg.	4	I	2.070	6.810	3.191	1.552	0.616	0.177	0.131	0.108	0.082	0.069	0.062	0.066	0.063
862_10	4	II	0.141	0.125	0.963	0.211	0.073	0.053	0.043	0.040	0.036	0.034	0.033	0.033	0.033
862_09	4	II	5.145	2.677	1.268	1.122	0.704	0.159	0.116	0.089	0.074	0.068	0.049	0.063	0.057
862_07	4	II	0.524	0.411	0.265	0.170	0.112	0.107	0.104	0.096	0.084	0.075	0.070	0.067	0.067
862_05	4	II	10.850	3.456	1.869	0.519	0.200	0.140	0.089	0.100	0.065	0.044	0.043	0.038	0.035
862_03	4	II	17.087	0.821	3.868	1.688	0.333	0.058	0.049	0.043	0.039	0.036	0.033	0.032	0.031
Avg.	4	II	6.749	1.498	1.647	0.742	0.284	0.103	0.080	0.074	0.060	0.052	0.046	0.047	0.045
862_10	5	I	0.270	0.177	0.133	0.231	0.092	0.073	0.060	0.057	0.054	0.052	0.051	0.051	0.051
862_09	5	I	4.339	5.075	1.129	0.646	0.324	0.144	0.114	0.094	0.086	0.078	0.070	0.074	0.069
862_07	5	I	2.335	1.196	0.561	0.282	0.129	0.121	0.105	0.094	0.087	0.083	0.074	0.073	0.072
862_05	5	I	3.516	5.130	3.426	1.429	3.802	1.050	0.358	0.181	0.091	0.068	0.065	0.060	0.058
862_03	5	I	10.440	1.325	0.359	0.179	0.100	0.089	0.068	0.063	0.056	0.052	0.049	0.047	0.046
Avg.	5	I	4.180	2.581	1.122	0.553	0.890	0.296	0.141	0.098	0.075	0.066	0.062	0.061	0.059
862_10	5	II	0.599	0.431	0.142	0.079	0.089	0.073	0.055	0.046	0.035	0.032	0.031	0.031	0.031
862_09	5	II	0.959	3.932	5.071	2.361	0.190	0.093	0.072	0.063	0.055	0.048	0.045	0.048	0.045
862_07	5	II	0.554	0.509	0.336	0.230	0.154	0.149	0.133	0.124	0.113	0.095	0.079	0.076	0.075
862_05	5	II	0.563	0.480	0.405	0.366	0.977	0.798	0.078	0.055	0.042	0.034	0.035	0.033	0.031
862_03	5	II	10.635	5.620	5.896	15.791	1.424	0.173	0.075	0.074	0.044	0.041	0.037	0.042	0.040
Avg.	5	II	2.662	2.194	2.370	3.765	0.567	0.257	0.083	0.072	0.058	0.050	0.045	0.046	0.044
862_10	6	I	0.281	0.229	0.150	0.105	0.076	0.451	0.093	0.073	0.064	0.059	0.059	0.056	0.055
862_09	6	I	3.828	1.428	0.640	0.924	0.285	0.101	0.078	0.065	0.061	0.059	0.094	0.056	0.057
862_07	6	I	0.805	0.543	0.290	0.199	0.133	0.169	0.104	0.091	0.081	0.073	0.069	0.069	0.066
862_05	6	I	0.845	0.710	2.730	1.216	3.555	1.548	0.230	0.097	0.067	0.054	0.053	0.050	0.050
862_03	6	I	4.848	4.220	2.764	2.008	0.281	0.813	0.161	0.097	0.073	0.076	0.071	0.068	0.069
Avg.	6	I	2.121	1.426	1.315	0.890	0.866	0.616	0.133	0.085	0.069	0.064	0.069	0.060	0.059
862_10	6	II	0.661	0.274	0.134	0.107	0.064	0.052	0.045	0.041	0.038	0.035	0.037	0.034	0.038
862_09	6	II	2.330	0.761	0.504	0.349	0.164	0.128	0.088	0.066	0.058	0.052	0.083	0.051	0.049
862_07	6	II	0.267	0.216	0.154	0.123	0.083	0.076	0.064	0.061	0.055	0.052	0.049	0.050	0.049
862_05	6	II	0.556	0.400	1.756	0.422	0.199	0.110	0.058	0.048	0.037	0.032	0.032	0.031	0.029
862_03	6	II	14.876	2.164	1.149	0.600	0.160	0.105	0.075	0.062	0.047	0.041	0.039	0.038	0.039
Avg.	3	II	3.738	0.763	0.740	0.320	0.134	0.094	0.066	0.055	0.047	0.042	0.048	0.041	0.041



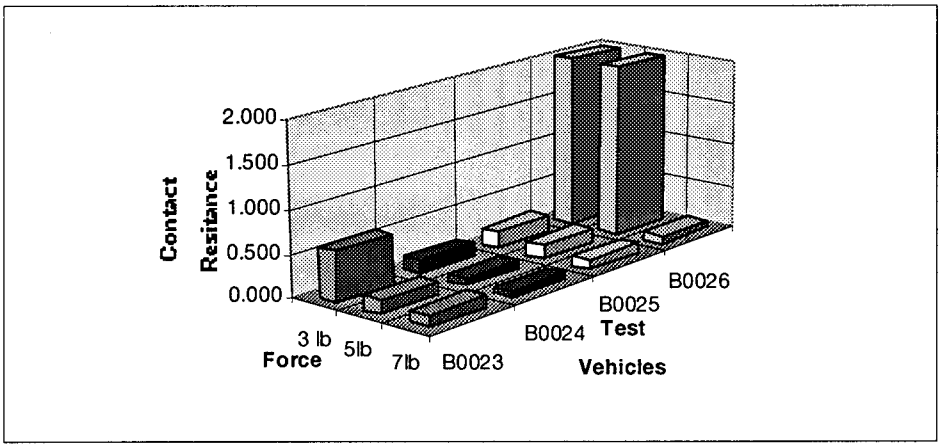
TV20 Contact Resistance Readings as a Function Of Force Applied

Carrier #	Pad Pitch (mil)	Pad Type	Force applied (lbs)												
			3 lb	4lb	5lb	6 lb	7lb	8lb	9 lb	10lb	11lb	12 lb	13lb	14lb	15 lb
801_04	4	I	0.584	0.317	0.196	0.132	0.099	0.089	0.082	0.077	0.076	0.075	0.075	0.075	0.075
801_02	4	I	1.165	0.479	0.410	0.167	0.144	0.108	0.091	0.085	0.082	0.080	0.079	0.066	0.078
801_12	4	I	0.487	0.476	0.312	0.279	0.264	0.636	0.185	0.133	0.799	0.098	0.076	0.070	0.068
801_10	4	I	0.482	0.245	0.134	0.106	0.095	0.081	0.074	0.070	0.067	0.066	0.066	0.066	0.066
801_01	4	I	0.265	0.231	0.141	0.109	0.088	0.076	0.072	0.067	0.066	0.065	0.064	0.064	0.064
Avg.	4	I	0.597	0.349	0.239	0.159	0.138	0.198	0.101	0.087	0.218	0.077	0.072	0.068	0.070
801_04	4	II	0.511	0.402	0.210	0.182	0.108	0.087	0.075	0.075	0.077	0.081	0.080	0.081	0.082
801_02	4	II	0.503	1.987	0.622	0.417	0.223	0.115	0.079	0.066	0.057	0.054	0.053	0.046	0.051
801_12	4	II	0.703	0.591	0.399	0.327	0.228	0.172	0.186	0.125	0.088	0.065	0.054	0.048	0.044
801_10	4	II	0.181	0.116	0.091	0.078	0.068	0.064	0.056	0.055	0.048	0.048	0.047	0.047	0.046
801_01	4	II	0.290	1.834	0.245	0.161	0.208	0.090	0.107	0.047	0.044	0.042	0.041	0.041	0.042
Avg.	4	II	0.437	0.986	0.313	0.233	0.167	0.106	0.101	0.073	0.063	0.058	0.055	0.053	0.053
801_04	5	I	0.837	0.323	0.183	0.146	0.107	0.089	0.080	0.076	0.075	0.075	0.074	0.074	0.074
801_02	5	I	2.211	1.211	0.479	0.209	0.139	0.102	0.086	0.080	0.072	0.073	0.068	0.073	0.071
801_12	5	I	1.346	1.658	1.425	0.351	0.182	0.138	0.125	0.109	0.092	0.072	0.068	0.067	0.066
801_10	5	I	1.321	0.670	0.324	0.653	0.284	0.137	0.115	0.104	0.074	0.073	0.073	0.073	0.073
801_01	5	I	0.771	0.414	0.238	0.147	0.097	0.082	0.071	0.065	0.063	0.062	0.062	0.062	0.062
Avg.	5	I	1.297	0.855	0.530	0.301	0.162	0.110	0.095	0.087	0.075	0.071	0.069	0.070	0.069
801_04	5	II	0.219	0.115	0.087	0.066	0.056	0.049	0.045	0.043	0.043	0.043	0.043	0.042	0.043
801_02	5	II	0.836	0.432	0.182	0.101	0.079	0.062	0.054	0.048	0.044	0.044	0.044	0.039	0.043
801_12	5	II	0.347	0.160	0.135	0.135	0.108	0.098	0.093	0.080	0.059	0.047	0.045	0.043	0.043
801_10	5	II	0.361	0.176	0.130	0.090	0.062	0.053	0.048	0.044	0.039	0.039	0.039	0.039	0.038
801_01	5	II	0.329	0.243	0.116	0.087	0.054	0.043	0.040	0.037	0.036	0.036	0.036	0.036	0.036
Avg.	5	II	0.418	0.225	0.130	0.096	0.072	0.061	0.056	0.050	0.044	0.042	0.041	0.040	0.041
801_04	3	I	0.673	1.037	0.692	0.235	0.323	0.206	0.148	0.109	0.100	0.102	0.101	0.101	0.105
801_02	3	I	3.182	1.949	2.627	0.388	1.087	0.350	0.257	0.132	0.113	0.109	0.111	0.080	0.106
801_12	3	I	1.610	0.710	0.364	1.859	0.593	0.349	0.687	0.334	0.384	0.092	0.085	0.082	0.079
801_10	3	I	0.843	0.568	0.321	0.213	0.193	0.123	0.098	0.088	0.082	0.082	0.081	0.081	0.080
801_01	3	I	0.801	0.600	0.221	0.144	0.108	0.095	0.081	0.072	0.069	0.068	0.067	0.067	0.067
Avg.	3	I	1.422	0.973	0.845	0.568	0.461	0.225	0.254	0.147	0.150	0.091	0.089	0.082	0.088
801_04	3	II	0.335	0.214	0.135	0.100	0.082	0.069	0.064	0.060	0.059	0.060	0.058	0.058	0.059
801_02	3	II	1.266	0.656	0.389	0.269	0.241	0.155	0.116	0.101	0.109	0.106	0.097	0.088	0.096
801_12	3	II	0.812	0.536	0.299	0.198	0.141	0.120	0.113	0.103	0.074	0.057	0.055	0.053	0.052
801_10	3	II	1.630	0.910	0.498	0.322	0.205	0.169	0.104	0.125	0.091	0.090	0.089	0.086	0.083
801_01	3	II	0.729	0.459	0.168	0.114	0.092	0.071	0.065	0.058	0.053	0.050	0.049	0.049	0.049
Avg.	3	II	0.955	0.555	0.298	0.201	0.152	0.117	0.093	0.090	0.077	0.073	0.070	0.067	0.068



B0008 Contact Resistance Readings as a Function Of Force Applied

Test Vehicles		3 lb	5lb	7lb
B0023 (1 Layer)	Average	0.578	0.155	0.131
	StdDev	0.928	0.106	0.125
B0024 (2 Layers)	Average	0.158	0.088	0.073
	StdDev	0.169	0.072	0.057
B0025 (2+ Layers)	Average	0.194	0.156	0.116
	StdDev	0.283	0.249	0.171
B0026 (3 Layers)	Average	11.607	2.331	0.090
	StdDev	32.519	7.554	0.101



B0023..B0026 Contact resistance readings as a Function of Force Applied

Conclusions

The force required to make contact for most technologies is to be measured during this evaluation phase. Using test vehicles as well as real applications of this technology for ICs, MMS has concluded that the force needed to make contact between a die and the MMS' membrane is dependant on the following factors:

- Pad pitch
- Number of contact points
- Die size
- Pad arrangement
- Membrane structure
- Contact point size

which make the specification of the force needed to make contact on a single pad very specific to an application, and not the technology. New methods, and test vehicles should be qualified to obtain such a value (force per pad) more achievable, if such a value is necessary for functional operation and usage of the final product.

The following summary of findings provide conclusions derived from specific test vehicle(s) evaluations:

TV20 & B0008

- Contact resistances decrease drastically as the applied force is increased from 3 to 13 lbs.
- Optimum force is determined to be between 12 to 13 pounds, where the resistance value does not decrease with increased force.
- Some contacts show very low contact resistance even at 3 lb force, while others showed no contact. This is due to non-uniformity of the contact points.
- Optimum contact resistance value was assumed to be less than 100 milliohms.
- Pad design type II exhibited about 15-20 milliohms higher reading due to additional resistance of the trace.
- 3 mil pitch pads showed higher contact resistance due to narrower pad width (50 microns pad vs. 60 microns pad.)
- Different 2 layer structures show no impact on compliancy of the membrane.
- The membrane compliance is very insensitive to different pad pitches (3-6 mils).

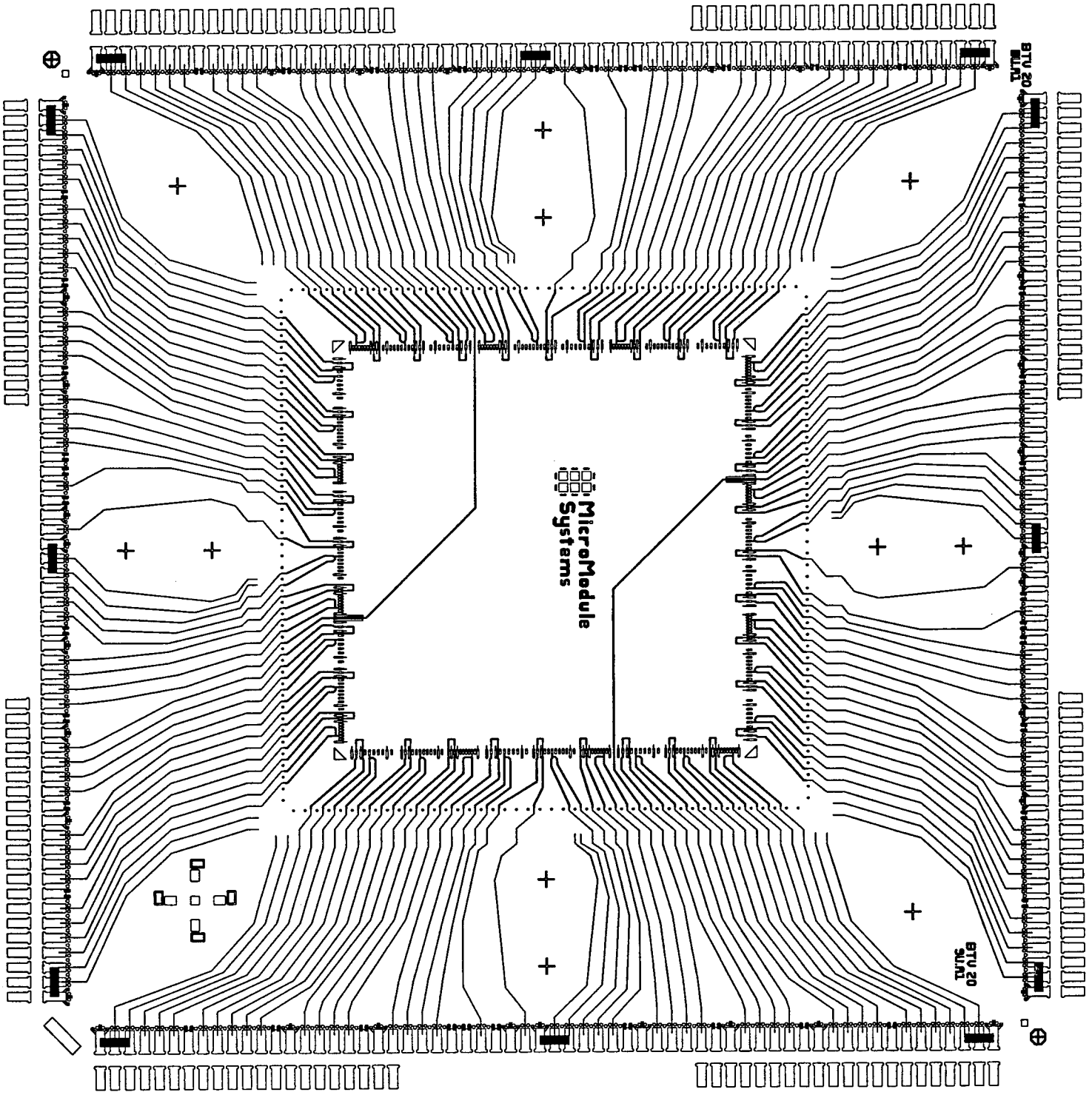
B0023, B0024, B0025, B0026

- The optimum force for all four different structures seems to be the same. This could result from the fact that the thickness of the Polyimide is the same for all four options, and the major difference among the first three options is signal and power routing which seems to have a minimum effect on the compliancy of the membrane.
- Contact resistances decrease drastically for the 3 layer design(B0026), but not as much for the other 3 designs. This could be attributed to the fact that the 3 layer

design has an extra metal layer under the contact points, thus reducing the compliancy of the membrane, requiring higher force to make good contact.

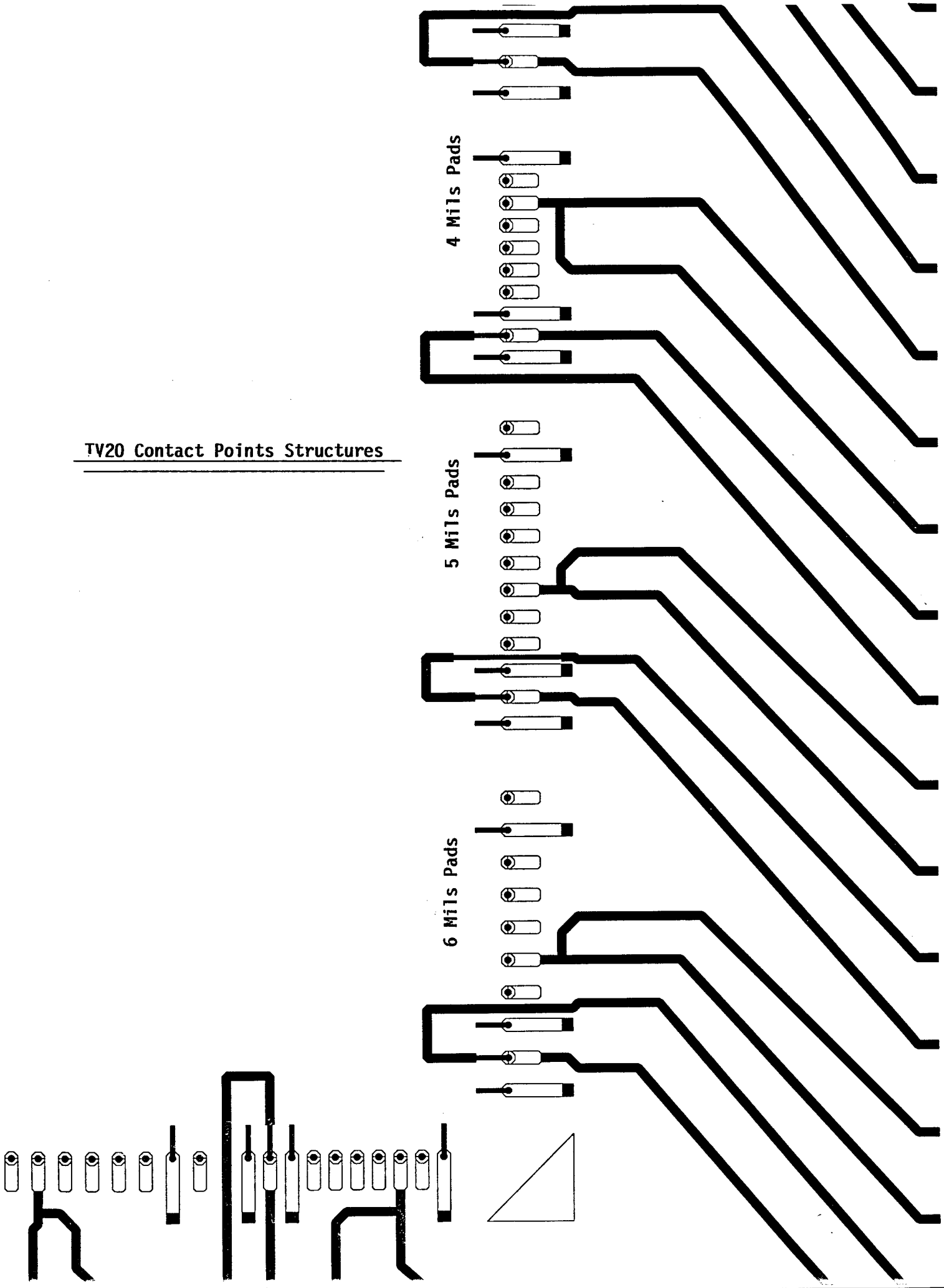
B0011

- Due to problems with the special fixturing required to make contact resistance measurement with this test vehicle, the results of this experiment are not available yet. This portion will be completed and reported in Phase II of the program.

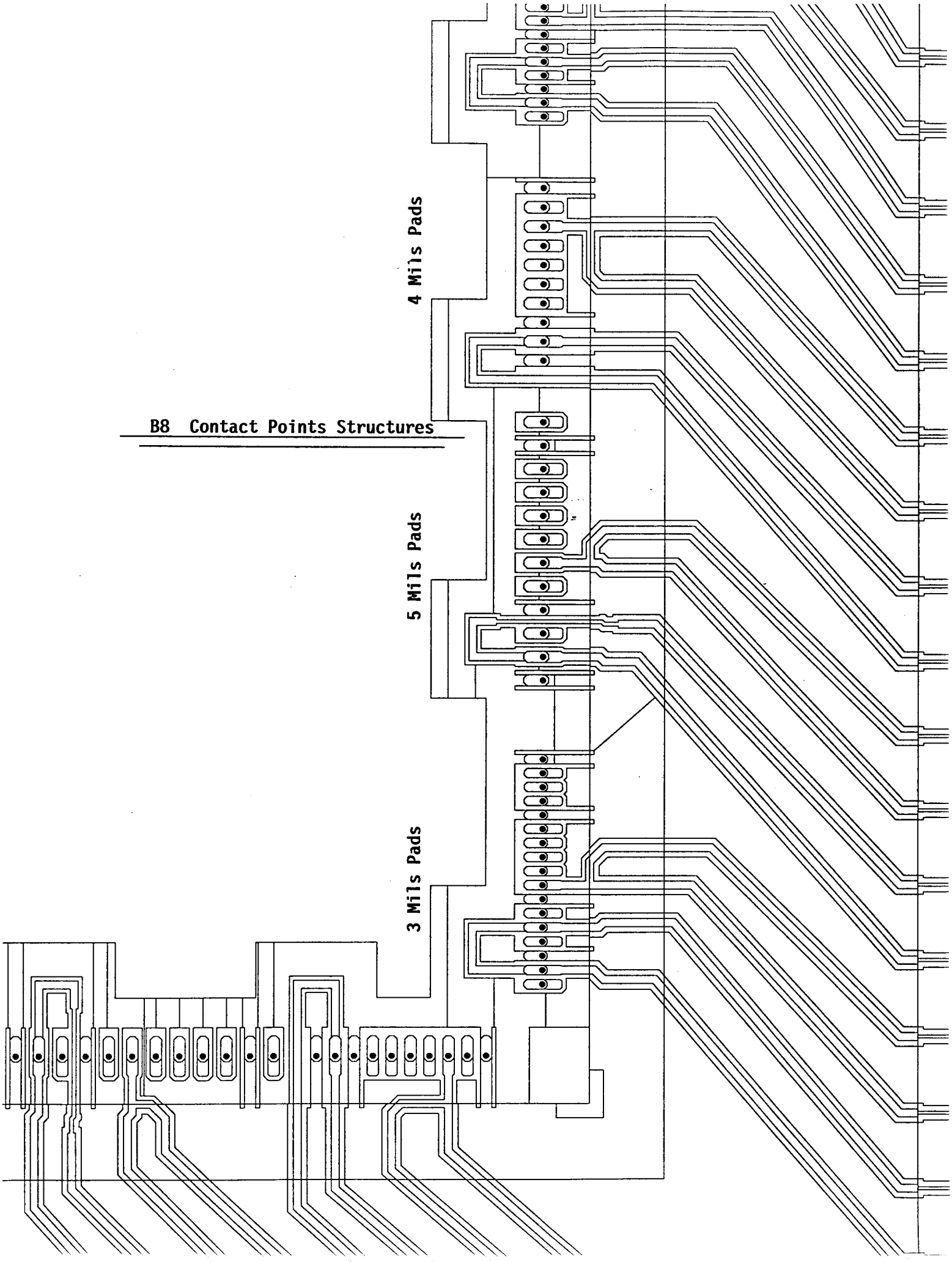


TV20 Interconnect Structure

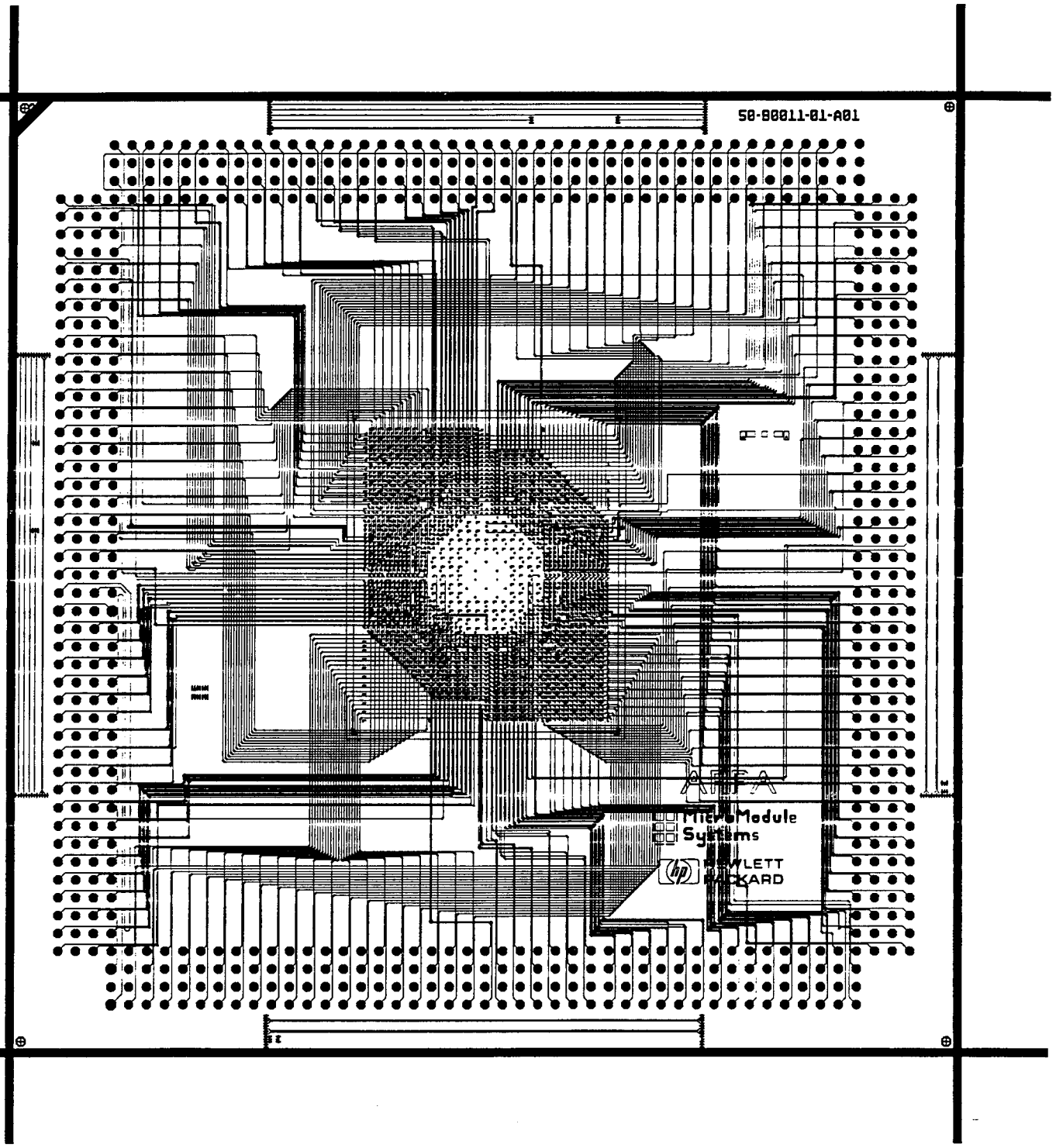
TV20 Contact Points Structures



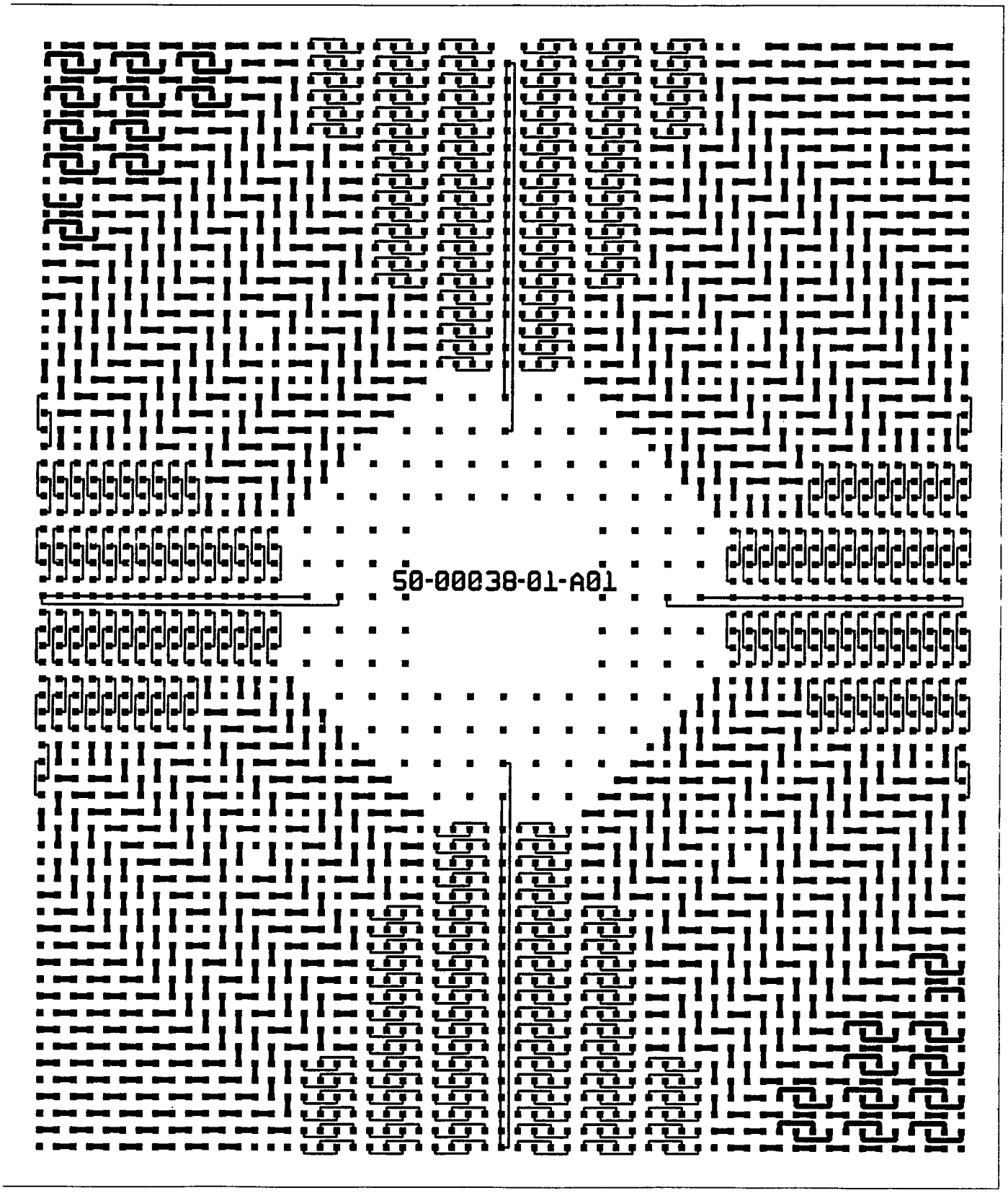
B8 Contact Points Structures



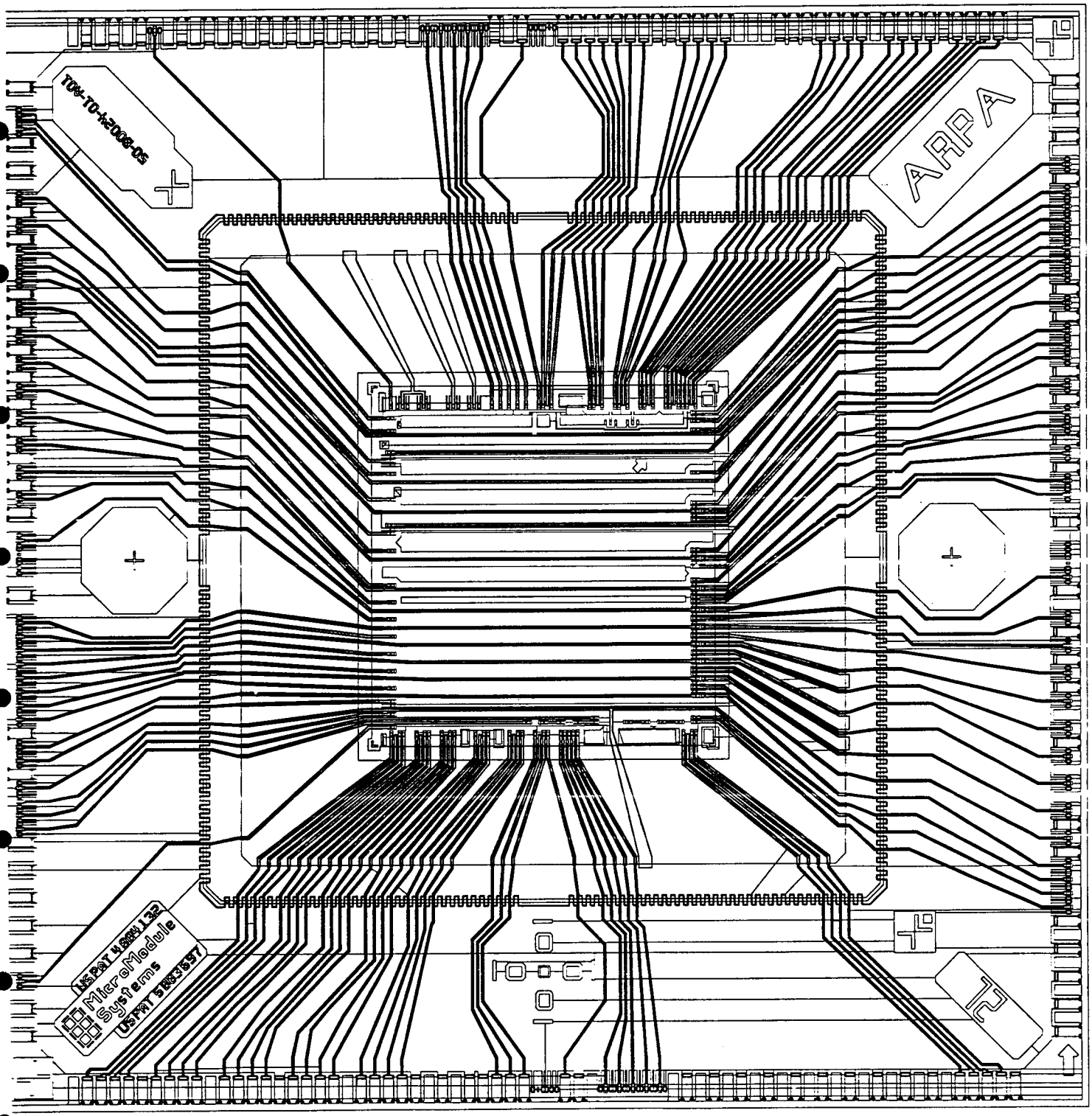
B0011 SUBSTRATE LAYOUT



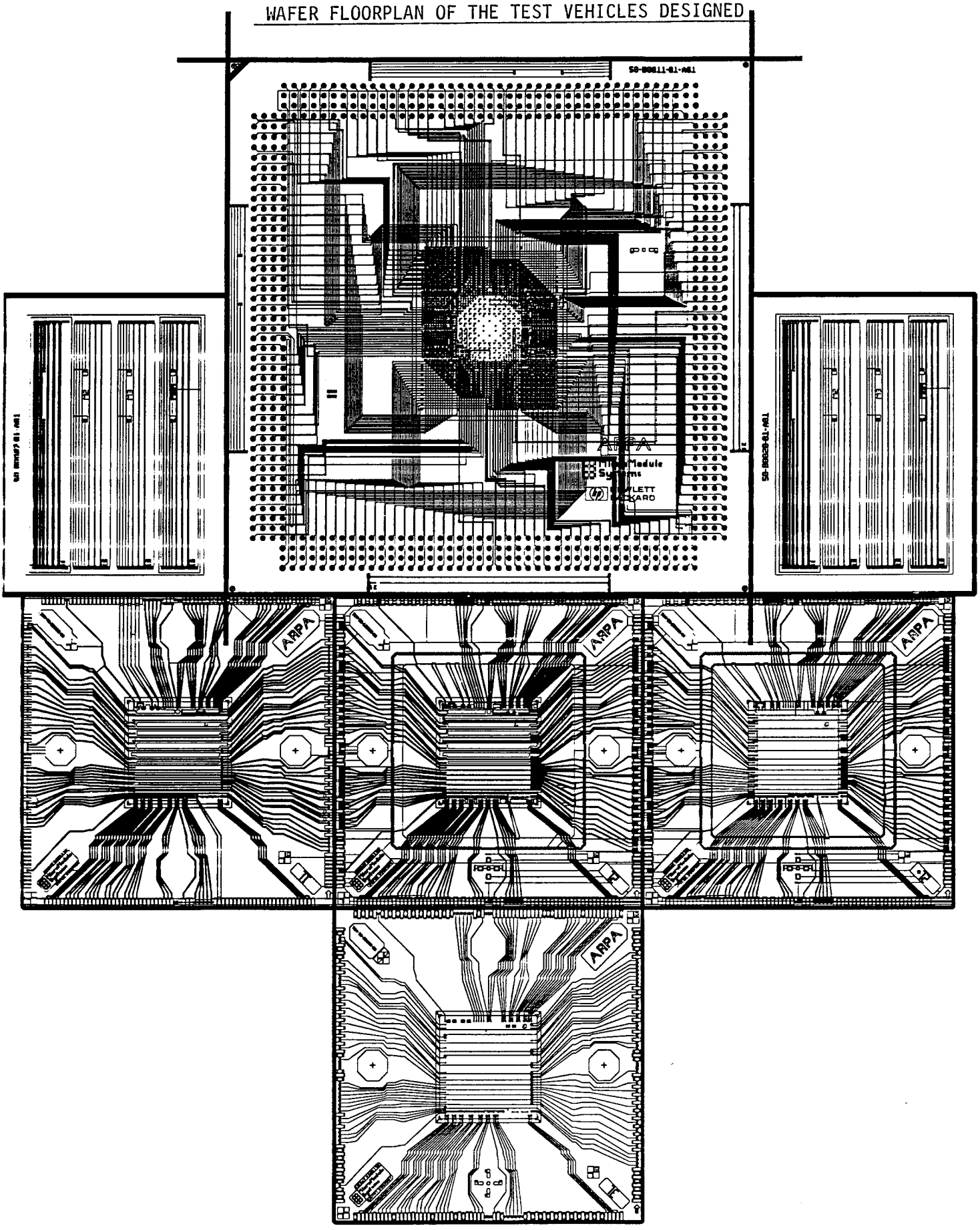
B0011 TEST DIE



B0024 SUBSTRATE LAYOUT



WAFER FLOORPLAN OF THE TEST VEHICLES DESIGNED



SECTION 2

ELECTRICAL CHARACTERIZATION

The intent of this work was to characterize the electrical integrity of the test frame device. Another goal was to understand the impact of different test frame design configurations on the electrical performance on the device. Finally, it was desired to establish standard interconnect parameters which can be used as design criteria for determining the optimum structure for a particular application.

Process

Test vehicles used in this experiment were as follows:

1. 1 layer coplanar interconnect with 280 pin socket footprint.
2. 2 layer coplanar interconnect with 280 pin socket footprint
3. 2+ layer coplanar interconnect with 280 pin socket footprint. The same as the 2 layer design, except the ground plane on the top surface is extended all the way to the edge of the die, to provide better impedance control for the tighter pitched IC pads.
4. 3 layer microstrip interconnect with 280 pin socket footprint.

The cross section of these test vehicles are shown in Figure 1, and the top view of the designs are included in the following pages.

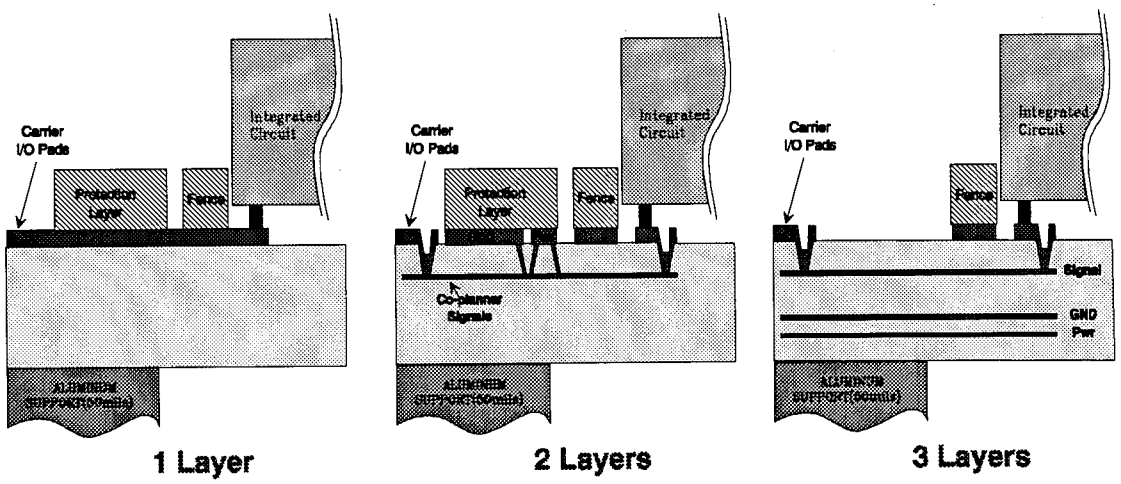


Figure 1.

Time Domain Reflectometry (TDR) was used to determine line impedance and propagation delays.

Using the configuration shown in Figure 2, the following power distribution resistance values were measured:

Common mode Resistance = Rc

Connection Resistance = Rs + Rc

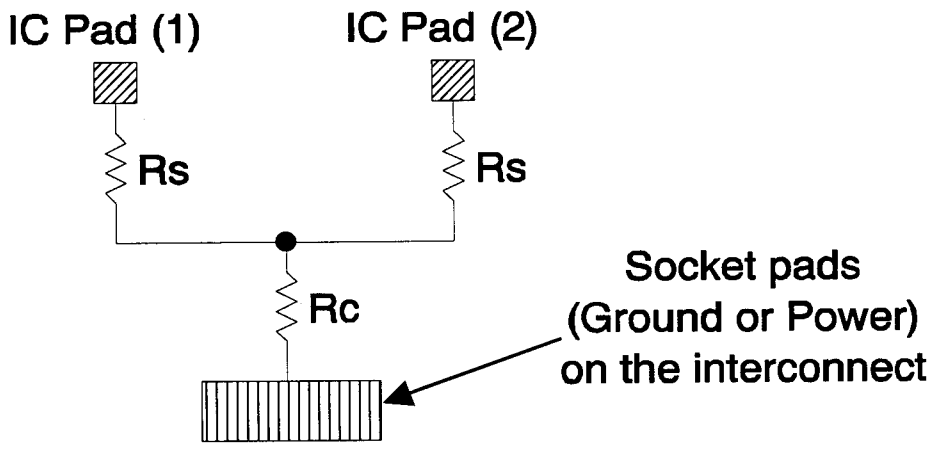


Figure 2.

Results

Signals With Coplanar Ground (1 layer and 2 layers, over the membrane portion)

Signal trace width	=	44 μm (nominal)
Signal trace to gnd spacing	=	28 μm (nominal)
Zo (sig. impedance)	=	69.9 Ohms (Average)
		2.39 Ohms (Std Dev)
Ro (sig. trace resistance)	=	0.92 Ohms/cm (Average)
Co (sig. trace capacitance)	=	0.94 pF/cm (Average)
Lo (sig. trace inductance)	=	3.22 nH/cm (calculated)
Cp (sig. to sig. capacitance)	=	0.07 pF/cm (Average)
		(22 um interstitial ground)
vp (propagation velocity)	=	55 ps/cm (Average)

⇒ Reducing space to 22 um, Zo changes to 60.4 Ohms; increasing signal width by 4 um , Zo changes to 69.2 Ohms

Signals With Coplanar ground (1 layer over Al substrate)

Signal trace width	=	44 μm (nominal)
Signal trace to gnd spacing	=	28 μm (nominal)
Signal trace to Al substrate	=	24 μm (nominal)
Zo (sig. impedance)	=	59.9 Ohms (Average)
		1.05 Ohms (Std Dev)
Ro (sig. trace resistance)	=	0.91 Ohms/cm (Average)
Co (sig. trace capacitance)	=	1.11 pF/cm (Average)
Lo (sig. trace inductance)	=	3.14 nH/cm (calculated)
Cp (sig. to sig. capacitance)	=	0.05 pF/cm (Average)
		(22 um interstitial ground)
vp (propagation velocity)	=	59 ps/cm (Average)

⇒ Reducing space to 22 um, Zo changes to 55.4 Ohms; increasing signal width by 4 um , Zo changes to 58.2 Ohms

Signals With Top Layer Ground Reference (2+ layers over the membrane portion)

Signal trace width	=	18 μm (nominal)
Signal trace to TOP gnd plane	=	12 μm (nominal)
Zo (sig. impedance)	=	49.8 Ohms (Average)
		1.39 Ohms (Std Dev)
Ro (sig. trace resistance)	=	1.97 Ohms/cm (Average)
Co (sig. trace capacitance)	=	1.68 pF/cm (Average)
Lo (sig. trace inductance)	=	2.92 nH/cm (calculated)
Cp (sig. to sig. capacitance)	=	0.10 pF/cm (Average)
		(42 μm space)
vp (propagation velocity)	=	70 ps/cm (Average)

Signals Over Power & Ground Reference Planes (3 layers and greater)

Signal trace width	=	18 μm (nominal)
Signal trace to BOT gnd plane	=	12 μm (nominal)
Zo (sig. impedance)	=	57.1 Ohms (Average)
		0.59 Ohms (Std Dev)
Ro (sig. trace resistance)	=	1.95 Ohms/cm (Average)
Co (sig. trace capacitance)	=	1.41 pF/cm (Average)
Lo (sig. trace inductance)	=	2.90 nH/cm (calculated)
Cp (sig. to sig. capacitance)	=	0.08 pF/cm (Average)
		(42 μm space)
vp (propagation velocity)	=	64 ps/cm (Average)

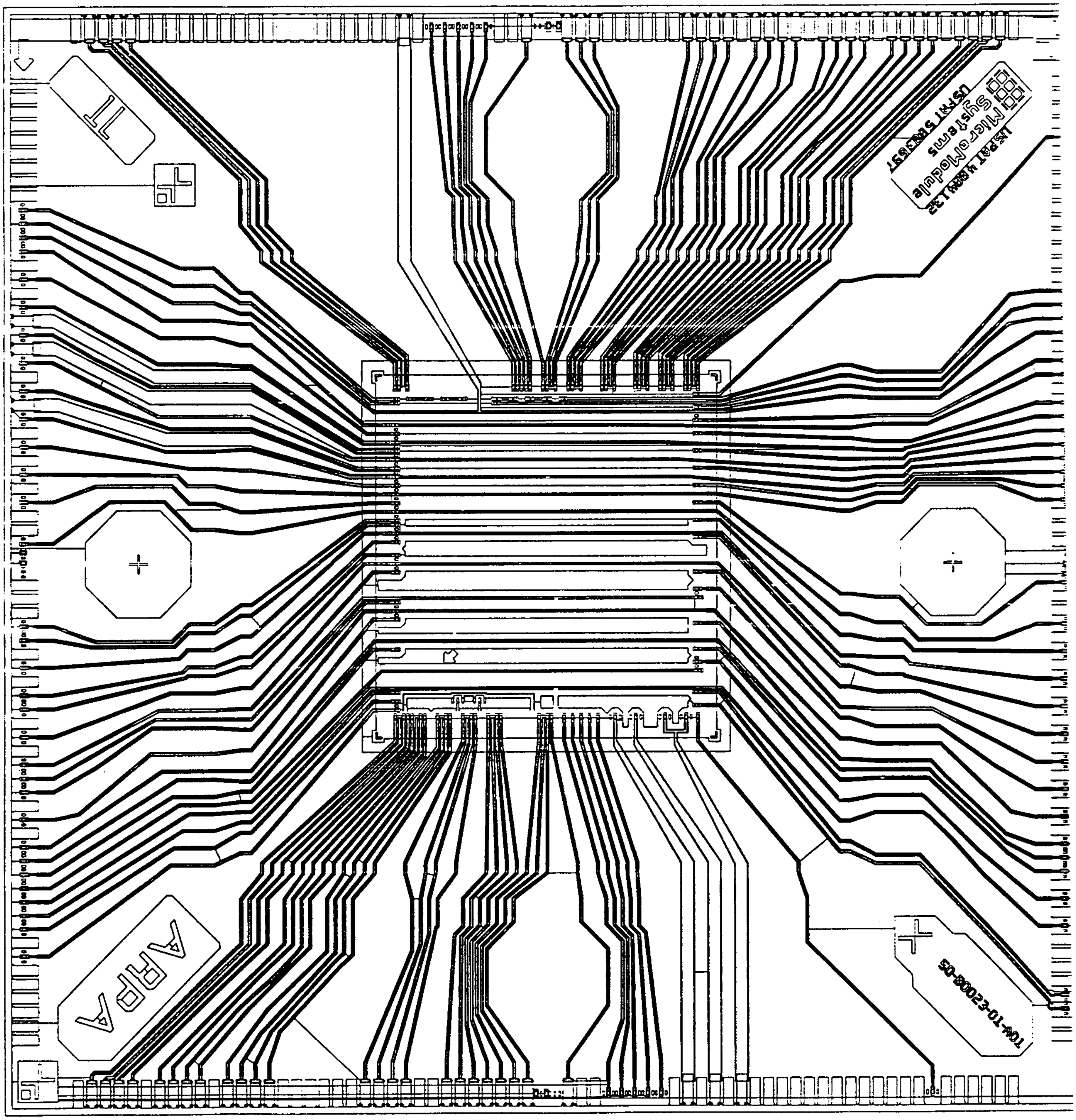
Signals With Coplanar Ground Reference (2 and 2+ layers over Al susbtrate)

Signal trace width	=	18 μm (nominal)
Signal trace to TOP gnd plane	=	12 μm (nominal)
Signal trace to gnd Spacing	=	28 μm (nominal)
Signal trace to Al substrate	=	24 μm (nominal)
Zo (sig. impedance)	=	50.1 Ohms (Average)
		1.13 Ohms (Std Dev)
Ro (sig. trace resistance)	=	1.97 Ohms/cm (Average)
Co (sig. trace capacitance)	=	1.70 pF/cm (Average)
Lo (sig. trace inductance)	=	2.88 nH/cm (calculated)
Cp (sig. to sig. capacitance)	=	0.06 pF/cm (Average)
		(42 μm space)
vp (propagation velocity)	=	70 ps/cm (Average)

Electrical Characteristic Summary Table				
Parameter	**1 Layer**	**2 Layers**	**2+ Layers**	**3 Layers**
Impedance Control	Coplanar	Mixed Coplanar & Microstrip	Mixed Coplanar & Microstrip	Microstrip
Signal Impedance (Ohms)	70 Ω	70 Ω, segmented in series with 50Ω	50 Ω	50 Ω
Crosstalk Backward (KB) Forward (KF)	< 7% (to be measured)	< 5% (to be measured)	<5% (to be measured)	<5% (to be measured)
Max. Signal Frequency (@ 5 signal per Pwr & Gnd pins, Rise time 10% of 1/f 0.5 V noise margin)	22 MHz	44 MHz	114 MHz	> 1 Ghz Limited by socket
Max. Pwr Inductance (10mm die size)	4.5 nH /Connect	2.25 nH /Connect	0.88 nH /Connect	0.05 nH /Connect
Power Connection Resistance/Connection	0.279 Ω (Avg.)	0.196 Ω (Avg.)	0.141 Ω (Avg.)	0.025 Ω (Avg.)
Ground Connection Resistance/Connection	0.048 Ω (Avg.)	0.030 Ω (Avg.)	0.011 Ω (Avg.)	0.028 Ω (Avg.)
Power Common Mode Resistance/Connection	NA	0.004 Ω (Avg.)	0.005 Ω (Avg.)	0.013 Ω (Avg.)
Ground Common Mode Resistance/Connection	0.025 Ω (Avg.)	0.017 Ω (Avg.)	0.006 Ω (Avg.)	0.013 Ω (Avg.)
Intrinsic Bypass Capacitance (Avg.)	4.0 pF /Connect	1.47 nF	1.54 nF	5.29 nf
Max. Power Die Contact Socket Contact	> 0.2 A /Contact 1 A / Contact	> 0.2 A /Contact 1 A / Contact	> 0.2 A /Contact 1 A / Contact	1A /Contact 1 A / Contact

REMAINING WORK:

Due to unforeseen delays in delivery of 50 Ohm terminator ICs to be used for this evaluation, AC Characterization of Power and Ground connections from IC through to carrier socket connection with S-parameter measurement equipment has not been completed yet. This portion of the project is currently scheduled to be completed during Phase II of the program.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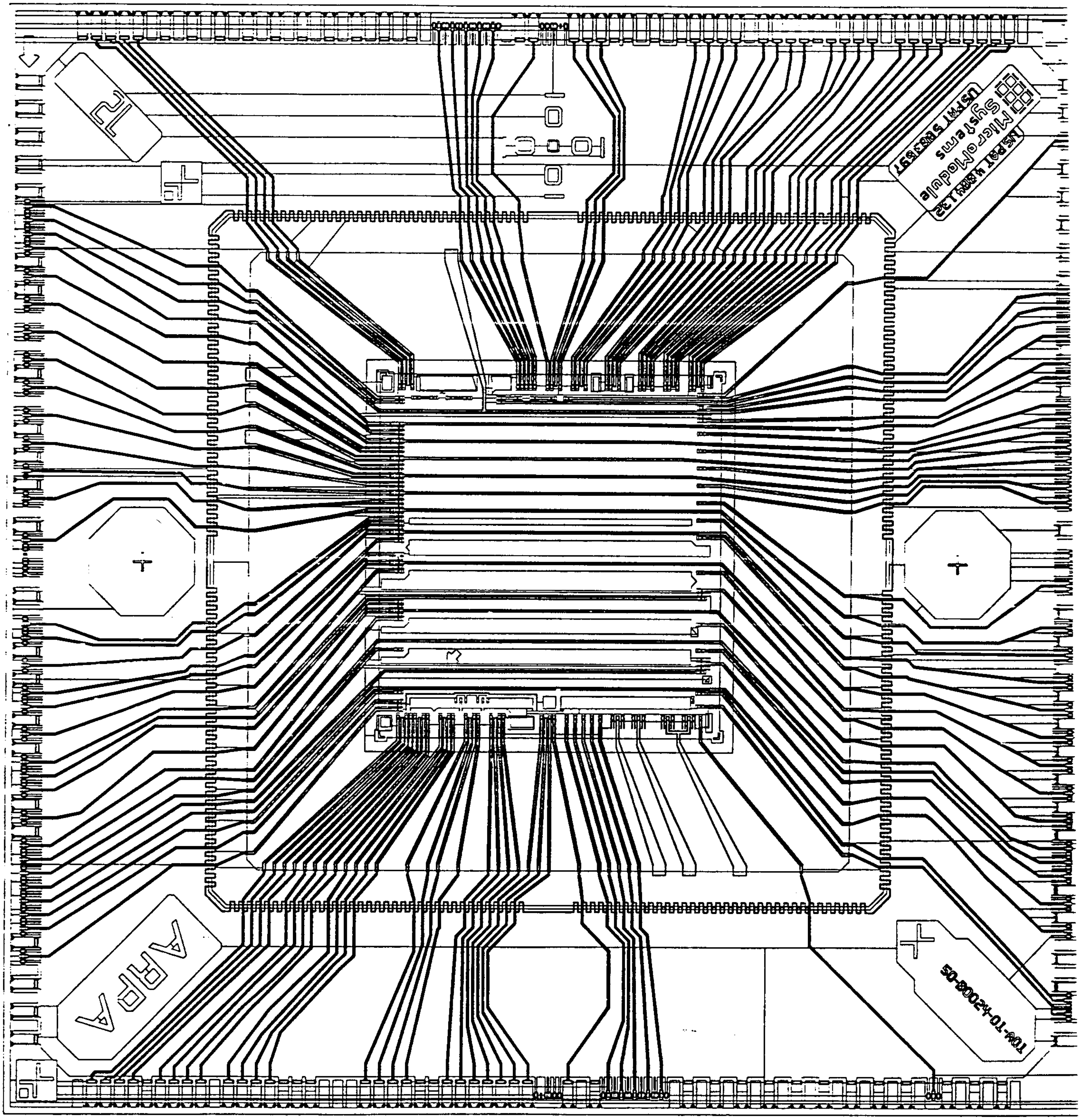
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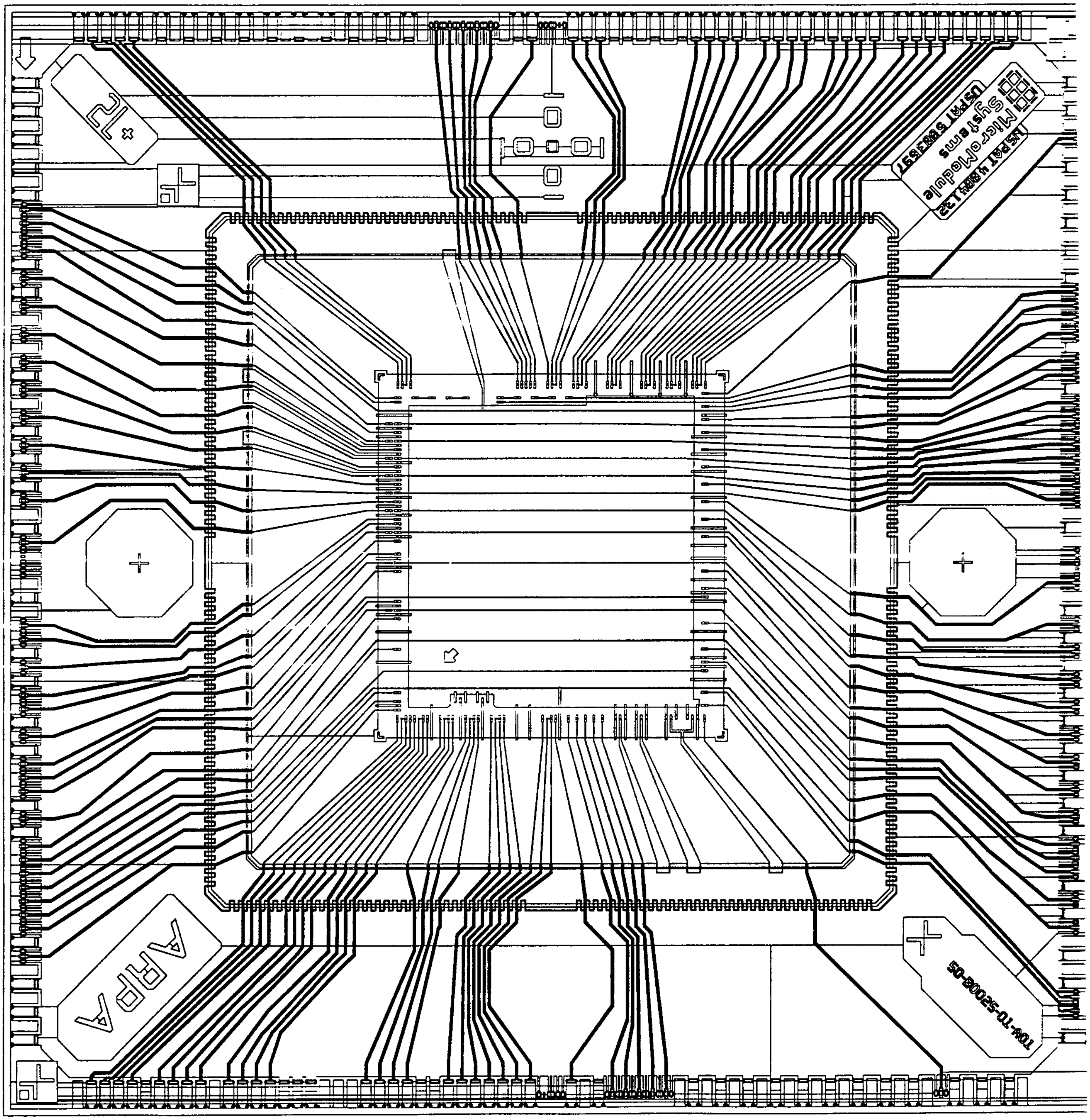
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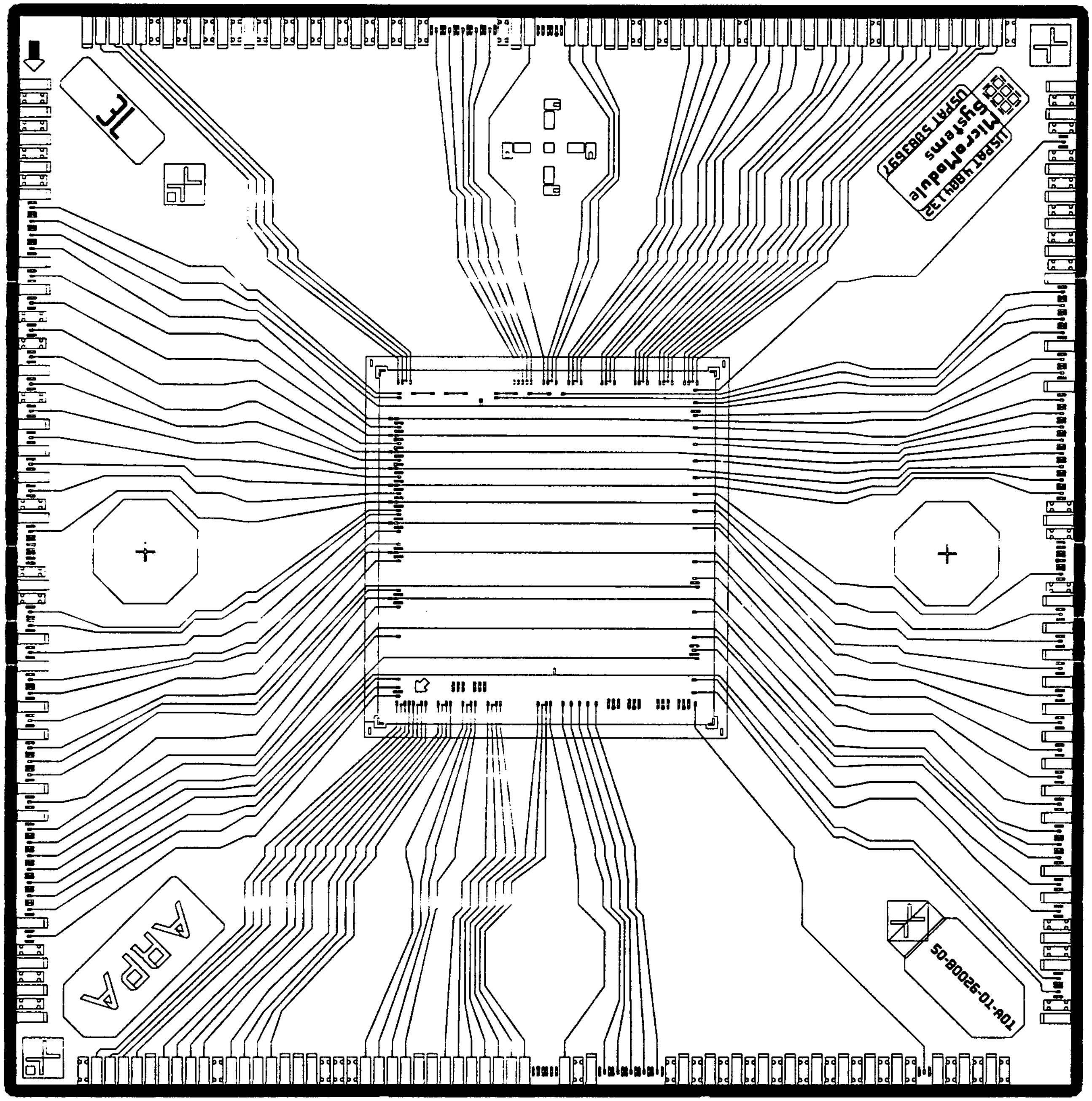
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SECTION 3

PRODUCT SIZE CHARACTERIZATION

The objective of this investigation was to identify the smallest product size for a given die size, since the size of the substrate greatly effects the product cost . The size of a substrate is governed by two factors, the membrane or the flexible area which itself is defined based on the die size, and the Al frame which holds the membrane in a taut condition.

In order to save time & money, this segment of the project was divided into two projects:

1. Membrane/Cavity size optimization
2. Al frame size optimization.

The optimized membrane size was determined through experimentation, and the optimized Al frame size is determined through modeling and Finite Element Analysis. This allows us to quickly change the parameters and find the optimized substrate size for a specific die size or a family of dice.

The membrane size optimization was defined through establishing the minimum gap between the edge of the die and the edge of the Al frame.

Membrane/Cavity Size Optimization

This evaluation was conducted by establishing an optimum gap between the edge of the die and the edge of the Aluminum frame holding the membrane portion (See Figure 1).

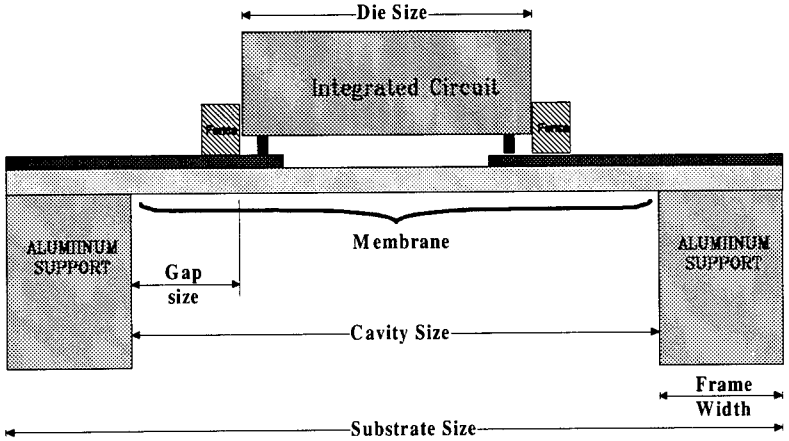


Figure 1. Membrane, Die, and Cavity Relationship

Process

TV20 test vehicles were used to establish a baseline for a 550 X 550 die data. The characteristics of TV20 is described in the Mechanical Characterization section (Section 1) of this report.

Standard TV20 gap size is 100 mils (cavity size of 750).

TV20 substrates with different gap sizes, from 35 mils to 100 mils, were fabricated to determine the optimum gap between the edge of the die and the Al frame.

The modifed MRSI pick & place machine was used to apply the force onto the backside of the die.

A Keithly microohm meter was used for all the resistance measurements.

The initial force used was 10 lbf (TV20 baseline is 12 lbf) and the resistance was measured and tabulated at all the 72 points. The force was then increased in one pound force increments up to 15 lbf.

Once the minimum cavity size was established, 3 additional substrates with the same cavity size were fabricated. Each substrate was then measured 5 times to validate the initial optimum cavity size findings.

Result

	Mean Contact Resistance (Ohms)		
FORCE	.620 CAVITY	.643 CAVITY	.645 CAVITY
10	4.720	0.093	0.074
11	3.260	0.090	0.078
12	2.260	0.085	0.071
13	0.520	0.095	0.068
14	1.770	0.110	0.071
15	0.310	0.120	0.077

Table 1. Cavity Size vs. Force Applied

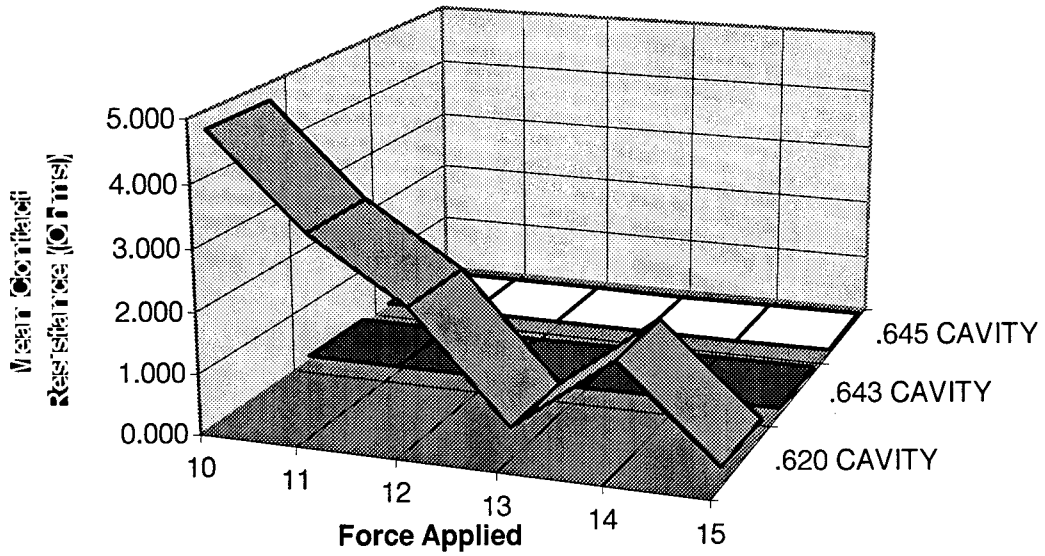


Figure 2. Cavity Size vs. Force Applied

Conclusions

With die size of 550 mils X 550 mils, and the bump size of 45 microns diameter with minimum of 4 mils pad pitch, 45 mils of gap between the edge of the die and the Al frame is the most optimized size.

Increasing the force to compensate for smaller gaps only causes deformation of the bumps and seems to have no effect on the making better contacts between the die and the substrate.

Al Frame Optimization

The smallest Al frame size (see Figure 1) can only be determined based on the substrate size and/or cavity size. Since the substrate size changes from application to application, it was then decided to use finite element analysis (FEA) to determine the minimum Al frame for a desired application. The analysis was performed for known applications and then verified using physical samples.

Process

Initial modeling suggested that the results for some cases may be nonlinear as the stresses predicted neared the yield of the Polyimide interconnect structure. It was therefore suggested that the experimental validation of the model be undertaken to gain confidence in the model predictions.

Initial experiments indicated that the sample structure behavior was elastic, but highly non-linear, especially in the cold bath region. Attempts to force the model predictions to fit the data were unsuccessful, using reasonable ranges of Polyimide material properties. The model prediction could only approximate the results in temperature range from about 25 °C to 100 °C.

The lack of correlation with the model predictions lead to questioning the validity of the experimental measurements. Indeed, it was found that the range of valid temperature compensation of the strain gages corresponded to the range in which reasonable comparison was obtained. A dummy sample was instrumented with the gages, and then tested. The dummy sample showed the same nonlinear behavior in cold temperatures. Therefore, the experiments were repeated with the dummy gages wired as a half bridge circuit (shown in the following pages),in an attempt to compensate for the behavior of the gages.

Figures 2 and 3 depict the physical dimensions and the structures of the two samples used in the experiments in this section. Details of the experiments and graphical presentation of the data are also included in the following pages.

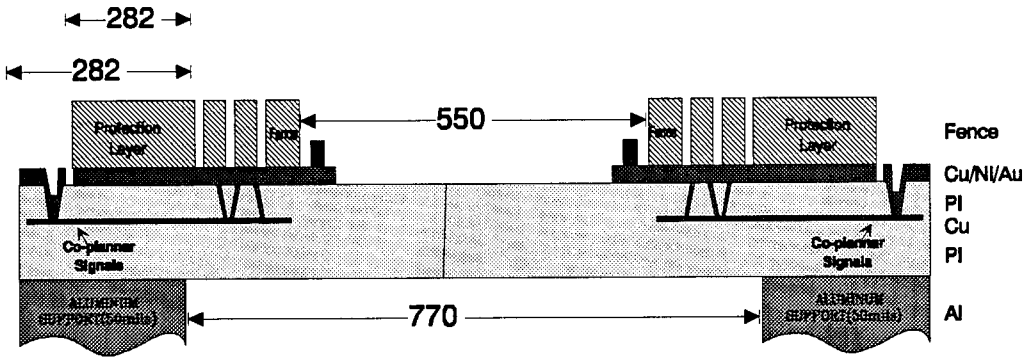


Figure 2. Sample # 4 Cross Section.

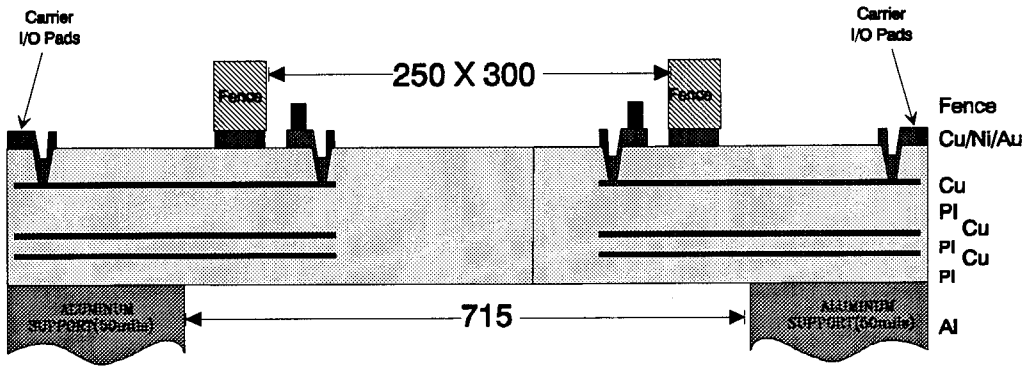


Figure 3. Sample #6 Cross Section.

Results

The data suggested that the CTE of the PI may drop to below that of the Al at about -25 °C. The data also showed that the behavior of the frame/interconnect structure is dominated by the prestressed state of the structure, and that this prestressed condition is likely asymmetric. This is probably due to the fact that the sample may be taken from a larger wafer, and the symmetry planes changes depending on the location of the substrate on the wafer. The analytical model, on the other hand, assumes complete symmetry and a zero initial stress state. Therefore, the behavior predicted does not match the one observed in the experiments.

The analysis predicts that the sample will bow over temperature ranges, but the experiments suggest that it more likely takes a saddle shape. Additionally, there

is likely more than one metastable state (i.e. two diagonally opposed corners bow up and the other two bow down or visa versa).

To use these results as an accurate prediction tool to optimize frame width, the initial prestressed condition must be known. This condition however, is dependent on the interconnect structure and fabrication process conditions and parameters. This model can then be used to predict a change in stress as a function of a given change in temperature.

The yield however, is a function of the absolute stress values. Therefore, the predicted change in stress must be added to the initial prestressed state to determine whether or not plastic deformation will occur.

Conclusions

While the analytical model does not exactly predict behavior, it is still useful for illustrating the effects of changing the frame geometry. The frame width, interconnect structure, fillet type or radius, can be quickly varied and the resulting change in stress can be estimated.

Recommendations

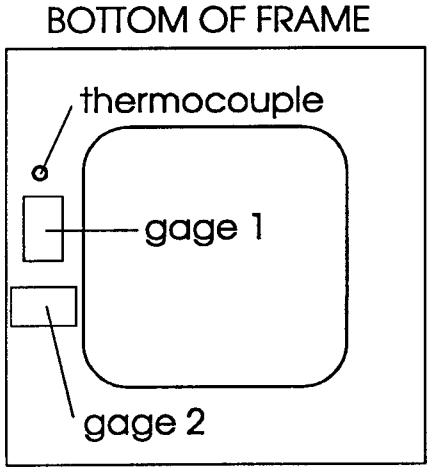
It is recommended that the interconnect fabrication process be analyzed to determine the initial prestressed state. This prestressed condition should then be input into the analytical model (expanded nonlinear analysis) to arrive at a more useful prediction tool. This model should then be tested with a wider range of samples that are instrumented with more accurate gages (temperature compensated over required range). The gages should also be as small as possible to give more of a "point" measurement.

MMS Frame Testing - Sample # 6
Engineering Lab EL 3, Washington State University
September 15, 1994 3:30 P.M.

PERSONELL:
Jeff Bakkom, ISR
Steve Antolovich, WSU
J. L. Ding, WSU
John Grimes, WSU

EQUIPMENT:
An Omega controller was used with a type K thermocouple to display temperatures and controll the oven.
Two aluminum temperture compensating strain gages were used in a 0/90 degree rosette to record the strain longitudinally and crosswise on one leg of the frame. The thermocouple was attached next to the rosette.
The strain gages were mounted to the frame bottom using a high temperature adhesive that was baked at 300 degrees F for about 2 hours. The gages were first wired to a terminal strip to prevent any added forces from the leads. Then the a 1/4 bridge circuit was set up to a strain indicator unit that displayed microstrain for each gage.

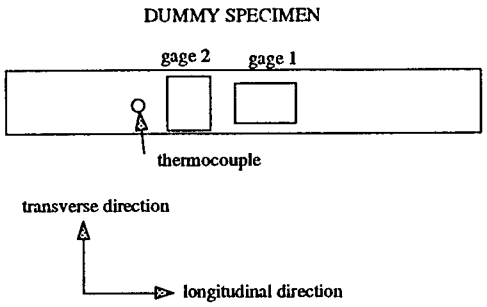
PROCEDURE:
-Part 1-
The specimen and terminal strip was placed in the furnace and the wire leads were routed to the strain indicator and Omega controller respectively. The strain indicator was zeroed and the current temperature was recorded.
The Omega controller was set to increase the temperature until it reached a value of 257 degrees F. Temperatures and corresponding strain values were recorded throughout the test. The temperature stabilized around 257 F for about 8 minutes at which point the furnace was turned off and the specimen allowed to cool until it reached room temperature..
-Part 2-
Two temperature baths were prepared for the cold testing. One bath consisted of ice water and the other of a mixture of dry ice and ethanol. The room temperature specimen was first place in the ice water until the temperature stabilized around 28 degrees F. Next, the specimen was placed in the dry ice mixture until its temperature stabilized around -66 degrees F. The specimen was finally removed and allowed to reach room temperature. Strain readings and temperatures were recorded throughout the test.

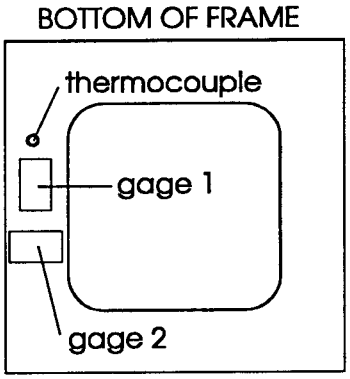


SAMPLE 6 TEST WITH TEMPERATURE COMPENSATION GAGE

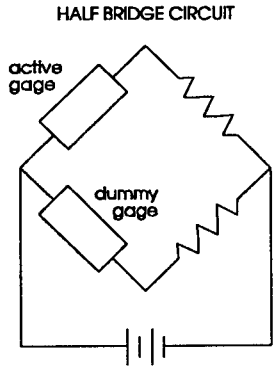
-Procedure-
The temperature compensation specimen was tested first by cooling in the ice bath. Next, the bag was immersed in the dry ice and ethanol mixture and cooled to nearly -80 degrees F. The bag was removed and subsequently the set up was removed from the bag while data was taken. After reaching room temperature, the set up was placed in the furnace and heated to 250 degrees F. A protective bag sealed the set up in the baths. Data was not taken as the specimen returned to room temperature.

-Set up-
The frame was tested with the temperature compensation "dummy gage". The temperatures were read from the thermocouple attached to the dummy gage.





The gages 1 from both the dummy specimen and the frame were wired in a half bridge. The gages 2 from each were also wired in a half bridge. This arrangement compensates for thermal expansion differences between the frame and the strain gages including the resistance property changes occuring in the gage at temperatures deviating largely from room temperature. Similar to previous tests, each set of gages (gage 1 or gage 2) are isolated from the other set and subsequent measurements represents the strain in just the gage direction. The half bridge circuit used for each set of gages is shown below.



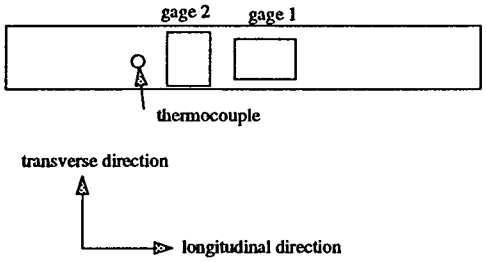
-Graphs-
The entire temperature range is shown in each graph. There are two graphs, one for each of the strain gages as follows:

gage	graph
1 - longitudinal	gage1
2 - transverse	gage2

TEMPERATURE COMPENSATION GAGE TEST

-Procedure-
The temperature compensation specimen was tested first by heating in the furnace. At 257 degrees F the furnace was turned off and data continued to be recorded until the sample reached room temperature. The specimen was then immersed in the ice bath followed by the dry ice and ethanol mixture. No protective bag was used over the specimen. However, I believe that protective coatings were used to seal the strair gage elements. Data was also taken as the specimen returned to room temperature.

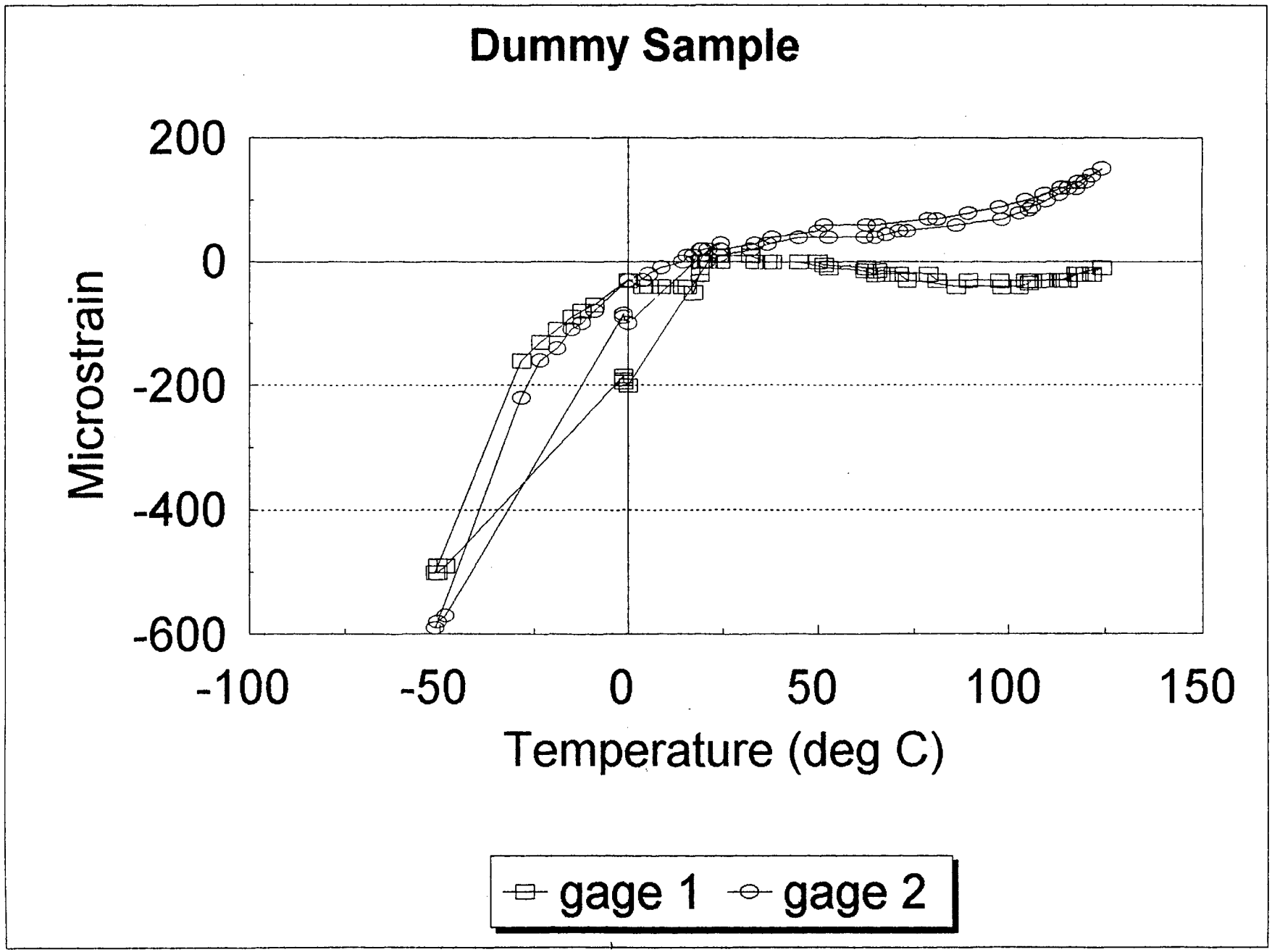
-Set up-
Aluminum temperature compensation dummy specimen with thickness and width similar to the sample 6 frame.



The gages were wired in a quarter bridge circuit, thus isolating each gage to give individual measurements.

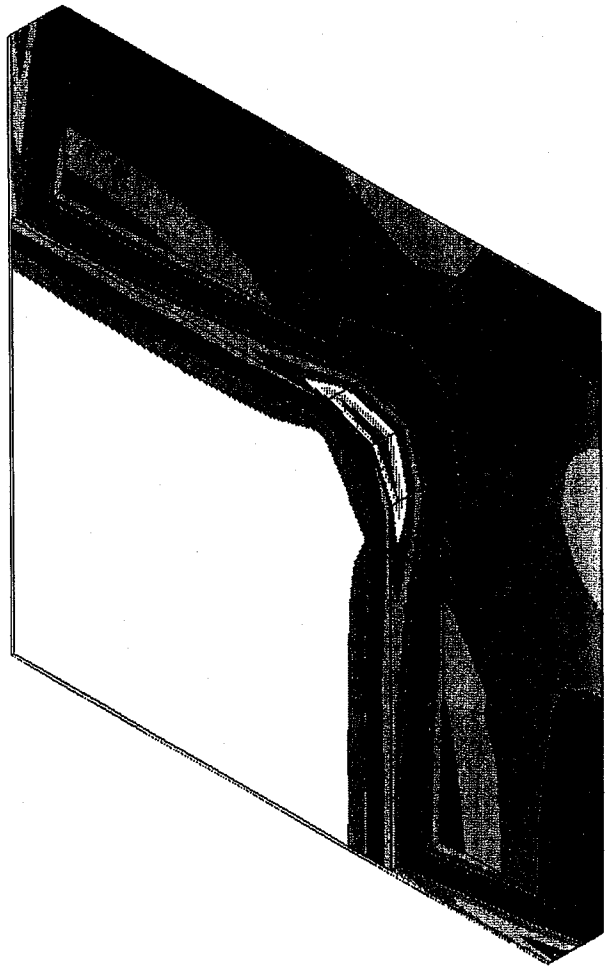
-Graphs-
The entire temperature range is shown in each graph. There are two graphs, one for each of the strain gages as follows:

gage	graph
1 - longitudinal	gage1
2 - transverse	gage2


Dummy Sample
200
0
-200
-400
-600
Microstrain
-100
-50
0
50
100
150
Temperature (deg C)
gage 1
gage 2

SAMPLE #6: 25 TO -55 DEG. C

frame full width



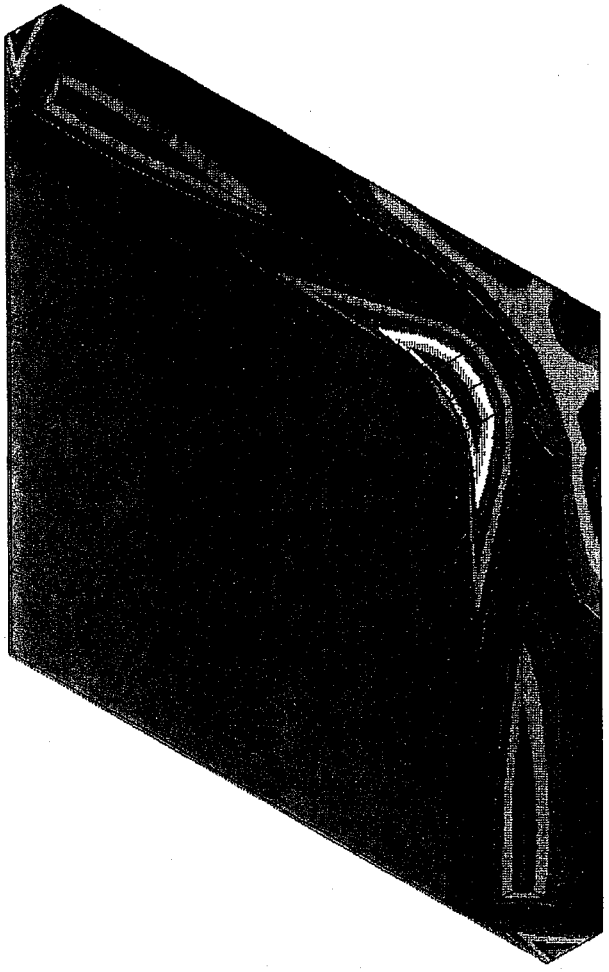
Von Mises

3.44E+08
3.10E+08
2.76E+08
2.42E+08
2.08E+08
1.74E+08
1.40E+08
1.06E+08
7.24E+07
3.84E+07
4.50E+06

dyne/cm/cm

SAMPLE#6 1/2 WIDTH 25 C TO -55 C

frame 1/2 width



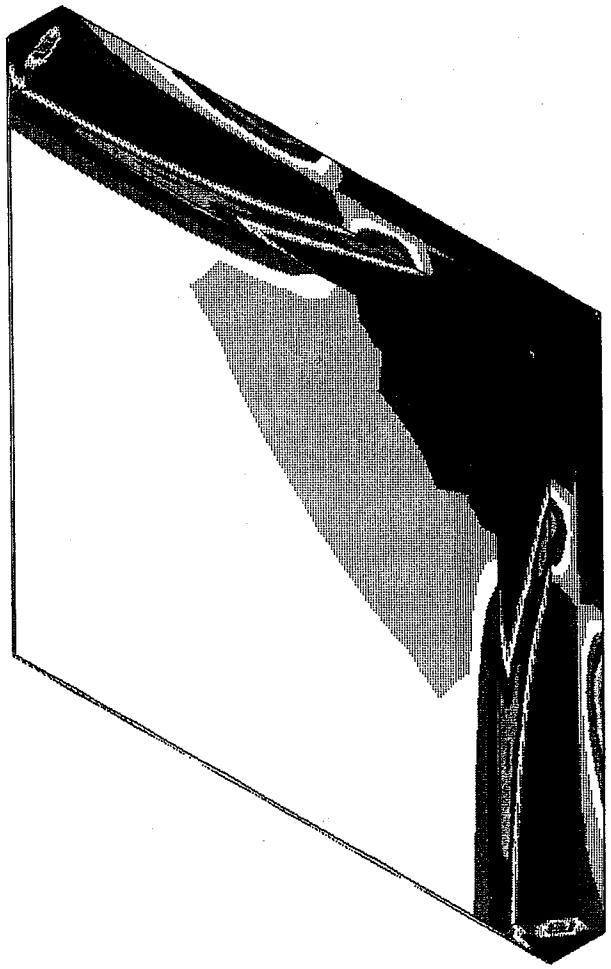
Von Mises

2.26E+08
2.04E+08
1.82E+08
1.59E+08
1.37E+08
1.15E+08
9.25E+07
7.02E+07
4.79E+07
2.56E+07
3.25E+06

dyne/cm/cm

SAMPLE #6: 25 TO -55 DEG. C

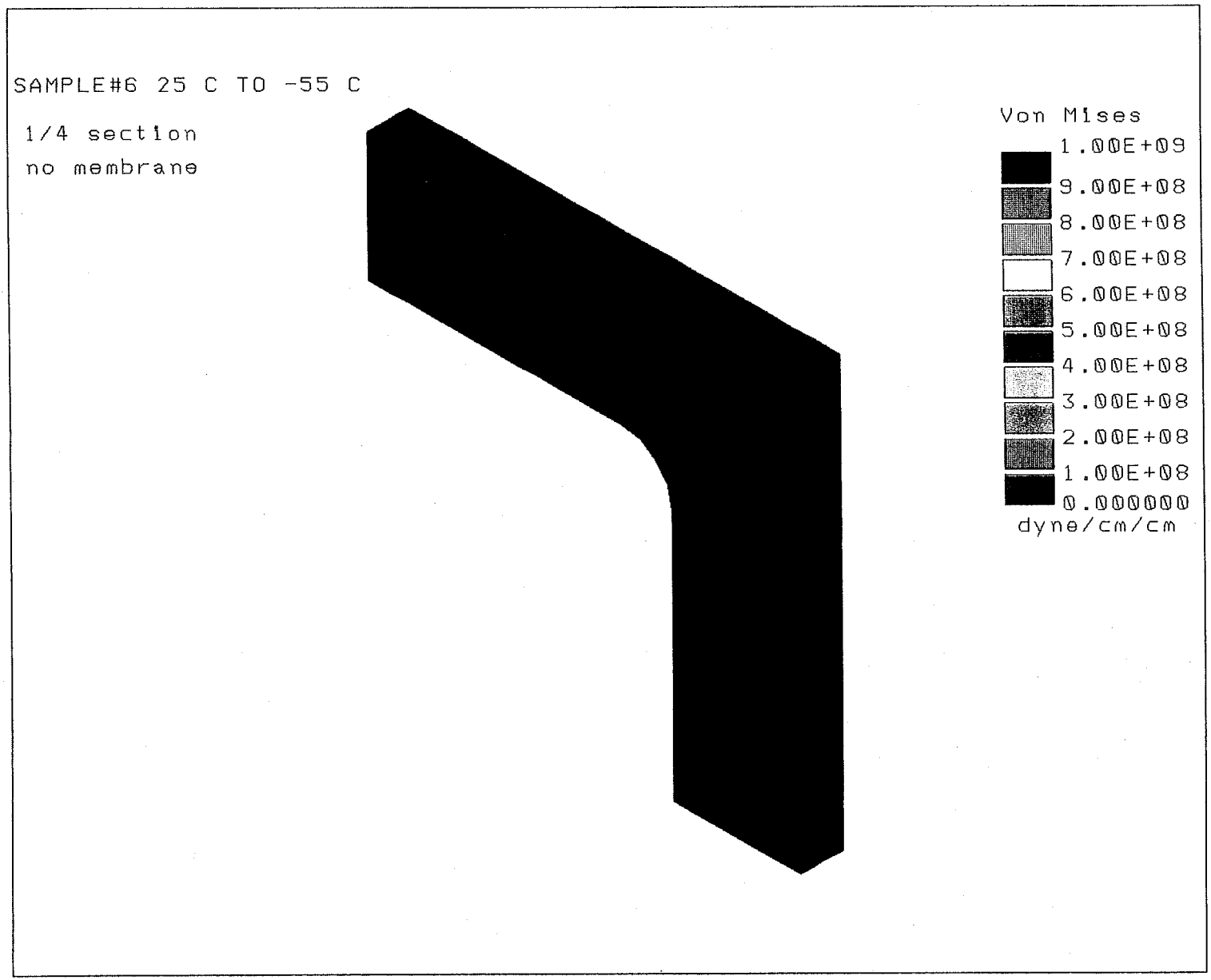
frame 1/3 width



Von Mises

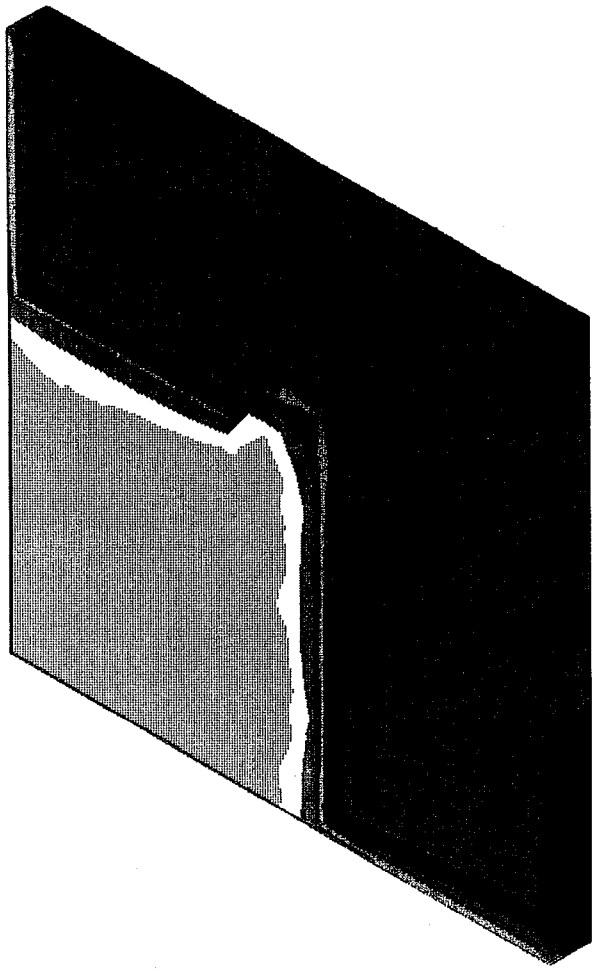
6.70E+07
6.07E+07
5.43E+07
4.80E+07
4.17E+07
3.53E+07
2.90E+07
2.27E+07
1.63E+07
1.00E+07
3.67E+06

dyne/cm/cm


SAMPLE#6 25 C TO -55 C
1/4 section
no membrane
Von Mises
1.00E+09
9.00E+08
8.00E+08
7.00E+08
6.00E+08
5.00E+08
4.00E+08
3.00E+08
2.00E+08
1.00E+08
0.000000
dyne/cm/cm

SAMPLE #4: 25 TO -55 DEG. C

frame full width



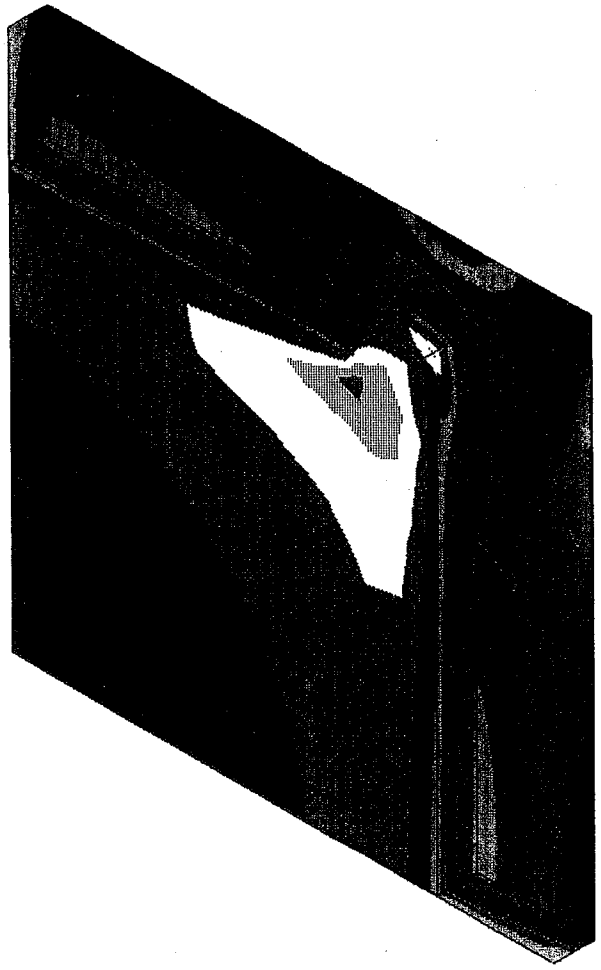
Von Mises

8.92E+08
8.03E+08
7.14E+08
6.26E+08
5.37E+08
4.48E+08
3.59E+08
2.70E+08
1.82E+08
9.29E+07
4.09E+06

dyne/cm/cm

SAMPLE #4: 25 TO -55 DEG. C

frame 1/2 width



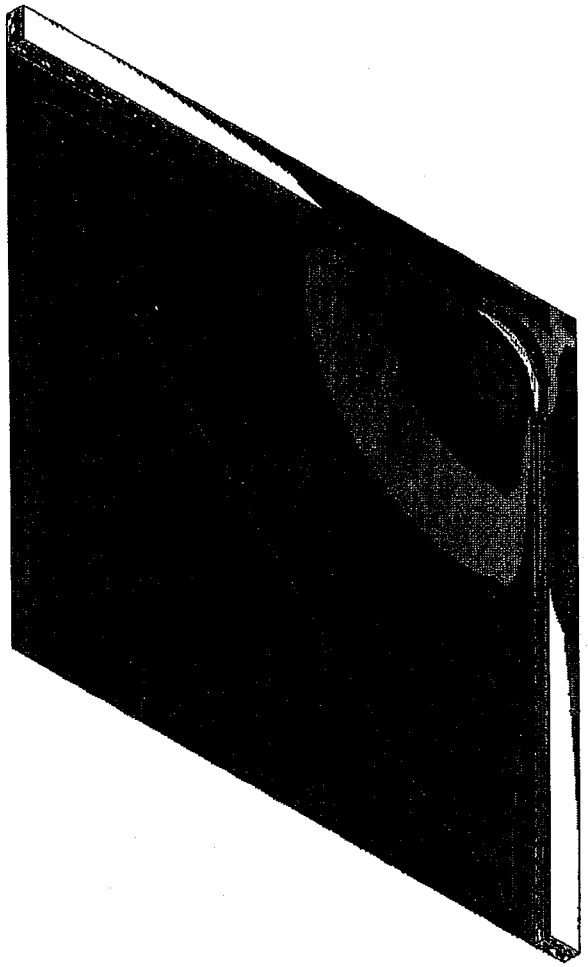
Von Mises

8.85E+08
7.97E+08
7.09E+08
6.21E+08
5.33E+08
4.45E+08
3.57E+08
2.69E+08
1.81E+08
9.28E+07
4.80E+06

dyne/cm/cm

SAMPLE #4: 25 TO -55 DEG. C

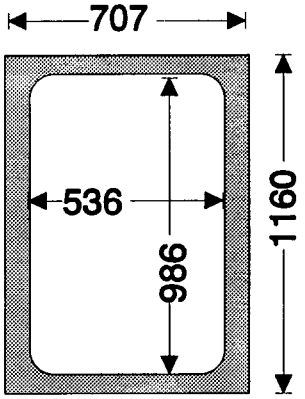
frame 1/8 width



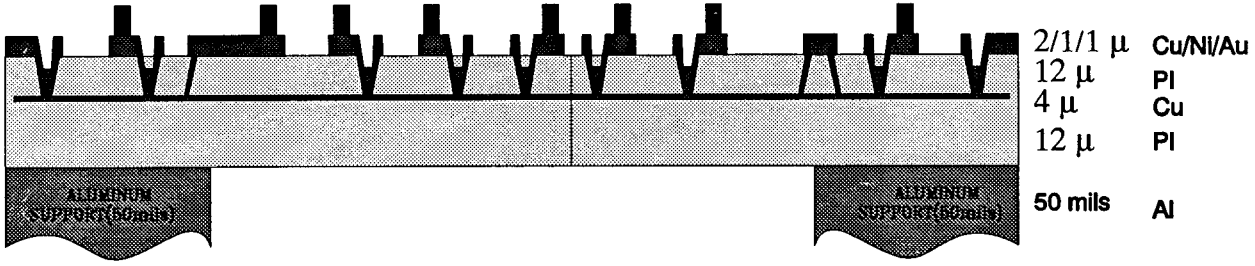
Von Mises

1.22E+09
1.10E+09
9.79E+08
8.61E+08
7.43E+08
6.25E+08
5.07E+08
3.89E+08
2.71E+08
1.53E+08
3.54E+07

dyne/cm/cm



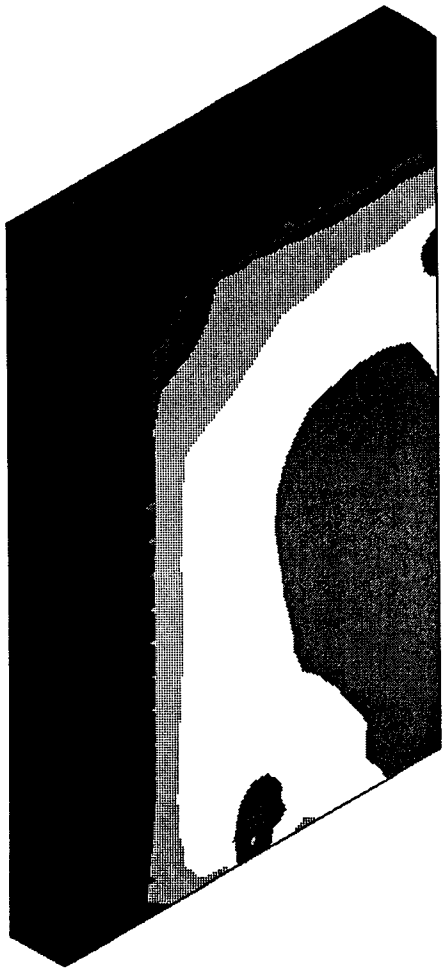
Sample #1



1.5 Layers

SAMPLE #1: 25 TO 125 DEG. C

frame full width



Von Mises

6.90E+09
6.21E+09
5.53E+09
4.84E+09
4.16E+09
3.47E+09
2.79E+09
2.10E+09
1.42E+09
7.35E+08
5.01E+07

dyne/cm/cm

SECTION 4

MEMBRANE SUPPORT CHARACTERIZATION

The purpose of this resaearch was to determine the maximum size cutout that may be deployed in the layup material under the BDBIT's membrane without affecting the contact integrity of the bumps to the silicon die under test. The purpose of the cutout is to minimize the area of contact between the membrane and the silicon die under test. In the standard BDBIT's device, the layup material are solid square pieces. This allows pressure to be applied over the entire area of the silicon die. If particulate contamination is present on the die surface, then the force applied by the BDBIT's carrier could damage the device under test. If the layup material could be cut out (like a picture frame, as shown in Figure 1) so that it only supports the contact bump area, then the potential for damage to the die is greatly reduced. It should be noted that the membrane itself may or may not also be cut out. However, if sufficient support is not provided under the contact bumps on the membrane, then the electrical performance of the BDBIT's device will be degraded, i.e., the contact resistance may be high or even open. Therefore, it is necessary to determine how close the edge of the cutout can be to the contact bumps.

Figure 1.

Process

The TV-20 test vehicle was used for this project, along with the latest version of the BDBIT's carrier. The only modification of the carrier was the use of a higher force spring to compensate for the large number of contact bumps in the TV-20 test vehicle. The appropriate spring force was determined using the standard layup. The size of the standard layup material for the TV-20 test vehicle is a solid piece 745 mils square. Cutouts in both layups, with five variations in size along with a control, which is not cutout, were evaluated. The cutouts ranged from 526 mils square to 551 mils square. In

all cases, the outside dimension of these were the same as the standard, 745 mils. Since the centerlines of opposing rows of contact bumps on the TV-20 test vehicle are 543 mils apart, the bump is completely off the layup material in 551 mils opening case and well away from the edge of the layup material in the 526 mils opening case. The simplified cross-section shown in Figure 2 illustrates the relationship between the silicon die under test, the contact bumps, the membrane, and the layup material. In this particular case, the bumps are shown lying within both edges of the layup material. It should be noted that membrane opening for the TV-20 is nominally 790 mils.

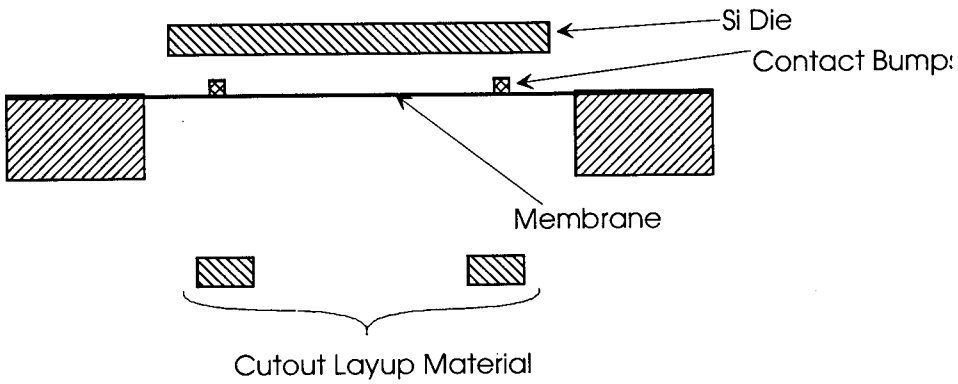


Figure 2.

Each of the five cutout size variations were mated to a silicon test die five times. The control using the standard solid layup was mated one time. The silicon test die used were coated with an unpatterned layer of aluminum and sized to fit the TV-20 test vehicle. The test die was replaced after each mating. One TV-20 test vehicle and carrier was dedicated to each size variation and the control, and was not changed during the matings. Each carrier was completely disassembled after each mating, then reassembled to insure randomization of the results.

The TV-20 test vehicle has 72 contact bumps which can be used for contact resistance measurements. The contact resistance was determined using the Kelvin (four wire) technique so that it is a true indication of the contact bump to die connection. A computer controlled micro-ohmmeter and switching matrix was used to make the Kelvin measurement. Each test run consisted of 72 contact resistance data points which were logged by the computer.

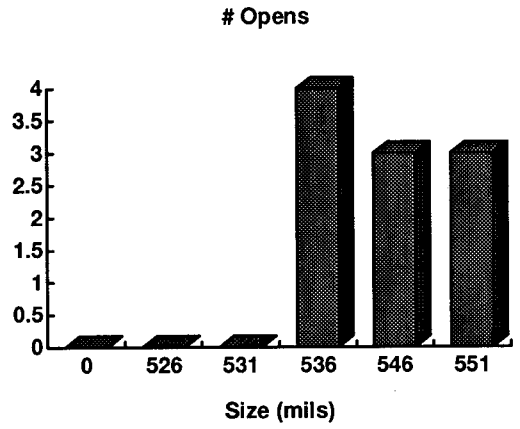
Results

It is suspected that improper support from the layup material would cause an increase in contact resistance, or even opens. This being the case, the data generated in the testing outlined above was first checked for the number of opens. In order to look for more subtle differences, the number of contacts with resistances greater that 0.2 Ω was also tabulated. The results are listed in Table 1.

Size (mils)	Control	526	531	536	546	551
# Opens	0	0	0	4	3	3
# >0.2 Ω	0	12	4	26	72	45

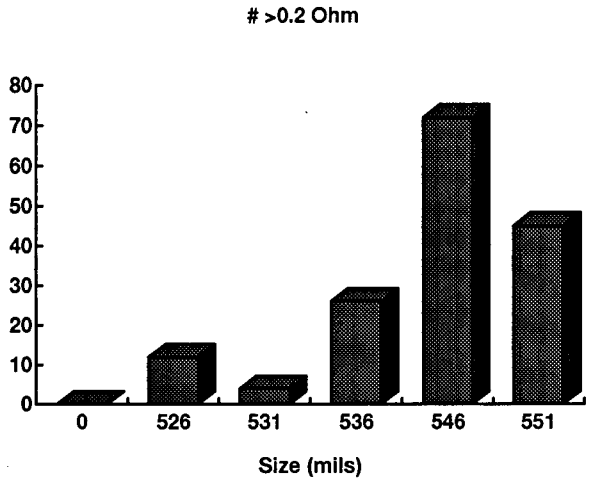
Table 1.

The data in Table 1 has been graphed to show the differences more clearly. The number of open contacts for each size cutout is shown in Graph 1.



Graph 1.

The number of contacts with resistances greater than 0.2 Ω for each size cutout is shown in Graph 2.



Graph 2.

The raw data collected in the testing outlined above is attached as an appendix to this report.

Conclusions

It is clear from the above data, that there is a increase in the number of open contacts and in the number of contacts with resistances above 200 milliohms when the size of the cutout is increased from 531 mils to 536 mils for the TV-20 test vehicle. These results can be generalized to other devices by considering the relationship of the edge of the contact bump to the inner edge of the cutout in the layup material. The centerline spacing of any two opposing bumps on the BDBIT's membrane is 543 mils and the bump diameter is about 2 mils. Therefore, the distance between the inner edges of the two contact bumps is 541 mils. In the case of the 531 mil cutout, the distance from the inner edge of the bump to the inner edge of the layup material is 6 mils (assuming that the layup material are centered in the membrane cavity). Since any cutout larger than 531 mils gives significantly poorer electrical results, it is clear that for any given device, the inner edge of the contact bump must be 6 mils or more away from the inner edge of the layup material.

SECTION 5

LOW CTE SUBSTRATE MATERIAL

To meet the demand of future products with larger sizes and smaller pad pitches and pad openings, it was apparent that a contacting material with thermal expansion properties close to Si should be used.
The mismatch between the IC and the contacting material can be calculated based on the length of the scratch marks on the IC pads, caused by temperature variations. Calculating the bump mark length vs. CTE on MMS' baseline products indicates that the CTE of the contact points is dominated by Al frame rather than Polyimide film. Thus, to lower the contact point's CTE mismatch between the die and the contact points, one has to use a base substrate material that has CTE closely matched with Si die (2.5 PPM/deg. C).

The objective of this research was to evaluate base substrate materials that are compatible to existing MMS technology, which would yield to the final product with a CTE close to Si.

PROCESS

Several different base substrate materials have been investigated. They include Si, Kovar, Invar and Molybdenum (Moly).

RESULTS:

Si The wafers could not be made into decals, since the etchant material would diffuse through Polyimide and attack the metal traces. Also, Silicon substrates are not easily machinable. They are very fragile, which may not be suitable for use in a manufacturing environment.

Kovar The wafers showed severe bow/warpage during process, the magnetic property of the Kovar wafers caused problems in sputtering and plasma etch systems, we also had difficulties decaling the wafers.

Invar The wafers showed severe bow/warpage during process.

Moly A(5.0 ppm/deg. C) has been identified to be the most promising material at the present.

Process Issues:

Polyimide Material: MMS' standard PI has ~50 ppm/oC CTE, which causes sever sagging of the membrane area, once the Moly substrate is removed from the designated area of the contacting surface. A lower CTE PI had to be used with Moly substrates.

Adhesion: Polyimide to Moly substrate adhesion seemed to be acceptable. No Polyimide delamination was observed after saw cut. No metal adhesion layer between Polyimide and Moly wafer is required as in our standard Al substrate process.

Plasma Etch: Moly reacted to MMS' standard plasma etching solution. A new plasma etch recipe had to be used to eliminate the formation of contamination in the plasma chamber.

Moly Etch: In order to make a decal, a portion of the Moly substrate has to be etched off while the copper interconnect circuitry is protected from contacting the etching solution. The initial protective materials used did not seem to be compatible to MMS process, since they either left residue behind, or remove the fence while being cleaned. MMS worked with an outside equipment vendor to evaluate the possibility of spraying the etching solution on only one side (the non-active side). The results of the evaluation seems very promising.

Projection Aligner: The Moly substrate thickness ranges from 15 to 20 mils (thickness of the wafers will be discussed later), which is significant thinner than our standard 50 mil Al substrates, projection aligner wafer disk/optics can not accommodate these thin substrates without modification. Currently we laminate tapes on the back of the wafers to increase the thickness of the substrates, and remove them after exposure. A projection aligner has to be dedicated for this material when the volume picks up.

Proximity Aligner: The Moly substrate has very low light contrast to plated Cu with Polyimide and photoresist overcoats, alignment targets could not be seen during the first via layer aligning, photoresist has to be manually removed on the alignment targets on each wafer to align.

Resist Cracking: Due to large CTE mismatch between Moly wafer and photoresist, thick resist tended to crack after hardbake. Mask design and bake process need to be optimized to reduce this problem.

Wafer Sawing and Drilling: Moly is a very hard material for machining, it takes a long time to saw each wafer. One option is to use chemical etching instead of sawing to separate each die, however, a wider scribeline is needed to accommodate the wet etch tolerance and reduces the usable real estate on each wafer. Drilling is still a problem, it significantly reduces the lifetime of the drill bits.

Material Issues:

Moly Substrate: The thickness and quality of the incoming substrates still remain to be the major obstacles of this project.

Moly has a density of 10.2 gram/cm3, which is significantly higher than our standard Al with a density of 2.7 gram/cm3. The heavy weight of the Moly wafers put a lot of strain on the fab equipment and wafer handling by operators, the absolute upper limit of the thickness is 20 mil, preferably to be less. With 15 mil Moly wafers, the wafers bowed/warped during fab process, which created vacuum breaks on equipment and process defects due to poor thermal conduction, such as closed vias and burnt resist. The bowed/warped wafers also created significant problems during testing.

The incoming wafers had heavy bow and lots of surface defects. The bow ranges from 1 to 10 mils across the wafers, which may account for the majority of the handling and yield problems. The incoming wafers also had scratches, pits, and protrusions which would have also caused the yield loss.

The wafers need to be chamfered on the edges to reduce particle generation during wafer handling.

A temporary specification has been devised as follows but no supplier has been identified:

Thickness: 18 mil (15 mils and 20 mils are standard thicknesses)
Flatness: 0.25 mil/inch (0.5 mil/inch is currently available if a better side is selected for fabrication)
Surface finish: average surface finish less than 10 microinches
Surface cleanliness: substrate surface should be free from dirt, stains, particulate and other foreign material.
Surface defect: any protrusions or ridges should be less than 40 microinches high, and any depressions or pin holes should be less than 80 microinches deep.

CONCLUSIONS:

MMS evaluated different substrate base materials to be used for the fabrication of the contacting technology. Moly seems to be the most promising material yet. Due to maturity of the Al substrate fabrication process, any deviation would cause an addition of expenses, as well as reduction of yield, thus increasing the cost of the final product, which may limit the usage and application of the contacting technology.

It is thus recommended that the use of the low CTE substrate materials be limited to applications that cannot be satisfied with MMS' Al substrates.

For volume applications, the incoming substrate has to be further improved.

SECTION 6

INCREASED CONTACT POINT HEIGHT

The objective of this research was to evaluate different schemes to increase the height of the contact points (bumps) on the membrane without increasing its diameter. The bump height increase is deemed to be necessary to allow die with thicker passivation layer to be used with this contacting technology. Due to the sensitivity of some passivation layers on ICs, it becomes necessary to reduce the possibility of either the surface of the membrane, or any potential contaminant on its surface, from becoming in contact with the die passivation surface. This is known to cause potential reliability issues with the die.

Process

Two different options were considered to effectively increase the bump surface from the membrane surface:

- Increase the height of the bump
- Deepen the surface of Polyimide.

1. Increased Bump Height

The structure currently used for the contact points on the membrane is depicted in Figure 1.

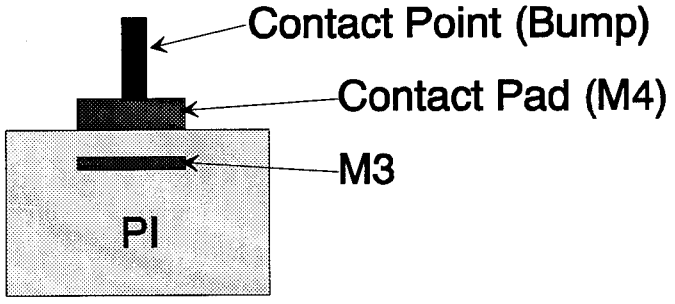


Figure 1. Contact Point Structure

To increase the height of the contact points, a thicker photoresist was used. Since this process usually results in a larger contact point surface, due to the slope of the resist walls after exposure, two different exposure process was evaluated, Proximity & Projection alignment processes.

To check for design to final size variations of the bump diameter surface area, a new bump mask was designed, which included bumps designed to 16, 20, 24, 30, and 44 microns bump diameters, distributed on different sites on the wafer. The following table includes the results of these experiments.

Resist Height (μm)	**Alignment Process**	**Bump Diameter (μm)**		**Bump Height (μm)**
		Designed	**Finished**	
45	Projection	20	38	35-47
45	Projection	30	50	35-47
45	Projection	44	68	35-47
45	Proximity	20	24	42
45	Proximity	30	46	42
45	Proximity	44	63	42
28	Projection	20	30	28
28	Projection	30	45	28
28	Projection	44	61	28
28	Proximity	20	39	25
28	Proximity	30	56	25
28	Proximity	44	74	25
38	Projection	20	25	28
38	Projection	30	34	28
38	Projection	44	61	28
38	Proximity	20	29	25
38	Proximity	30	44	25
38	Proximity	44	62	25

Resist Shape, using **Proximity** aligner:

Wafer #	**Bump Diameter (μm)**		
	Designed	**Resist Bottom**	**Resist Top**
1	16	15.5	21.1
	20	19.3	27.6
	30	30.1	36.7
	44	44.5	50.2
2	16	15.5	21.1
	20	19.4	25.4
	30	29.2	35.7
	44	42.0	48.5

Resist Shape, using **Projection** aligner:

Wafer #	Bump Diameter (μm)		
	Designed	**Resist Bottom**	**Resist Top**
1	16	15.5	17.2
	20	19.1	20.7
	24	23.6	26.0
	30	29.6	32.1
	44	41.1	44.5
2	16	17.1	19.6
	20	20.9	22.2
	24	24.9	26.5
	30	29.7	32.0
	44	45.1	47.1
3	16	17.3	18.4
	20	19.3	21.6
	24	26.0	26.9
	30	30.8	31.0
	44	45.0	47.0
4	16	15.4	17.2
	20	19.1	20.4
	24	23.5	25.7
	30	30.0	31.9
	44	43.5	46.5
5	16	13.0	16.3
	20	17.5	20.5
	24	20.9	23.5
	30	27.6	29.6
	44	39.7	43.0
6	16	14.8	15.7
	20	17.3	19.2
	24	20.7	23.7
	30	27.5	30.0
	44	40.5	42.8
7	16	15.9	17.2
	20	20.4	21.5
	24	24.1	24.7
	30	30.7	31.6
	44	44.3	44.9
8	16	14.4	15.5
	20	18.5	21.2
	24	23.8	24.9
	30	29.6	31.4
	44	44.7	46.2

2. Deepen The Surface Of PolyImide

To further increase the distance of the bump surface from the PI surface of the membrane, the PI is etched back as it is shown in Figure 2. Cavity sizes of 12 and 24 microns were fabricated. To insure membrane integrity and durability, starting PI thickness was also varied and evaluated.
Contact pad height was also varied in some of the experiments to enhance the bump surface to PI surface distance.

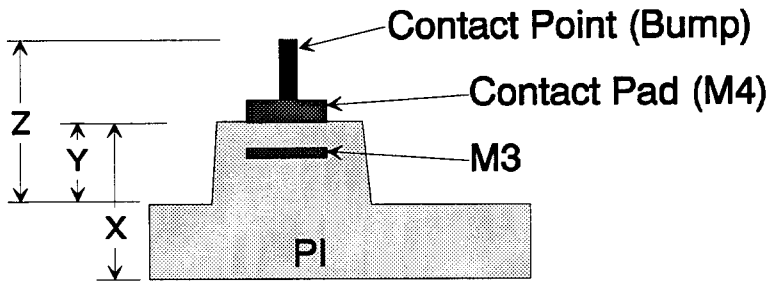


Figure 2. PI Cavity Created On The Membrane Surface

Design Value (μ)		Final Cavity Value (Y) (μ)		
PI Thickness (X)	Cavity Depth(Y)	Avg.	Range	Std. Dev.
36	12	12.40	3.10	1.10
48	12	12.73	6.5	1.69
48	24	24.48	19.4	3.61

CONCLUSIONS:

Through a series of experiments, different ways to increase the distance between the die surface and the membrane surface were evaluated. All the options considered deemed feasible, however, they all are achieve through extra processing, thus adding to the cost of the final product.

The projection exposure produced bump diameter (top) about 9 to 13 microns smaller than the proximity exposure bumps and the difference increases with increasing mask bump diameter. If the bump height is the same, the bump diameter variation between the projection and proximity alignment is slightly larger.

Thicker photoresist will produce smaller final bump diameter, with the same plated bump height. This is caused due to the resist wall profile, which is more vertical close to the bottom of photoresist.

12 Microns of remaining PI thickness seems to be durable enough for normal operation of the substrate.

The following table represents the possible die surface to membrane surface distances, achievable with MMS' existing technologies.

Option No.	Contact Pad Height (μ)	PI Thickness X (μ)	PI Cavity Y (μ)	Contact Point Height (μ)	Total Z (μ)
1	8	24	0	14	24
2	8	30	12	20	40
3	8	36	24	24	56
4	10	24	24	20	54
5	10	30	0	24	44
6	10	36	12	14	38
7	12	24	12	24	48
8	12	30	24	14	42
9	12	36	0	20	32

SECTION 7

CONTACT POINT HEIGHT UNIFORMITY

The objective of this research was to evaluate means to increase the uniformity/planarity of the contact points on the substrate. Contact points' non-uniformity on the substrate/membrane can cause die pad damage to the die and/or die pads, by applying focused forced on a few points where the contact points are higher than the others. The objective is to make the bump height variation between adjacent pads as small as possible. The acceptable bump to bump height variation depends on the membrane compliance, and the contact points' pitch.

Process

To create non-wiping oxide penetrating contact point on the membrane surface, MMS uses particulates embedded into the contact points. Although the particles will enable good contact between the die pads and substrates' bumps without the need for a wiping action, the same particles are the major cause of the height variation.

Two approaches were considered to improve the bump height uniformity:

- Small range of particle sizes, "Particle Size Control" project
- Eliminate the need of particles , "Particleless Bumps" project

1. Particle Size Control

The present source of particles suitable for MMS' applications range in size from submicrons to 60 μm.

Method: A number of methods are presently used to classify particles. These methods are classifiers, jet mills, impact milling, and ultrafine classifiers. MMS used Hosokawa Micron Power Systems in Summit, New Jersey, for all the particle separation operations.

A new batch of particles, specified to range in size from 2 μm to 4 μm, was purchased for this evaluation.

Results: The purchased particles were initially analyzed for sizes using a Cilas Model 920 Granulometre. The median was found to be 17.44 μm with 97% of the particles to be less than 65.48 μm. This result was verified using 325 mesh screen, which showed that a large percentage of the feed material was greater than 45 microns.

Passing these particulates through an air classifier, yielded 10.3% of the particles as fine fraction, with 97.0% of the fine products smaller than 3.84μm, and no particles larger than 5 microns.

Repeating the same test using a throughput rate of 977 g/hr, produced 6.9% fines fraction yield which was 100% finer than 4 μm and 97% finer than 3.51 μm.

Running the remaining materials through Alpine AFG Fluidized bed Jet Mill resulted in 97% of the material at 2.59 μm, with the median particle size to be 1.75 μm.

Conclusions: Both Air Classifiers and Jet Mills can be used to make uniform (narrower range of sizes) particles.
Higher fines fraction yields can be achieved utilizing lower throughput rates.
Although Jet Mills are more expensive they do not waste materials as do the air classifiers.

1. Particleless Bumps

A process that had already been developed by MMS engineers had shown the possibility of making the finished surface to be rough and sharp.

Method: Different samples were made with the particleless bumps. First samples were of the B0008 test vehicles. This was done to verify any force variation. Then new samples were made with an actual IC design to allow the technology to be evaluated in a real application/environment.

Results: Figure 1 depicts the force measurement results of B0008 test vehicle with particleless bumps.

5 samples of a carrier designed for an actual die were given to a MMS customer for evaluation of the technology in a real case application. The samples were temperature cycled from room to 125°C for 250 times, with the

die changed every 10 cycles. All 5 units functioned properly through the 250 temp. cycles.

	Force Applied												
	3 lb	4 lb	5 lb	6 lb	7 lb	8 lb	9 lb	10 lb	11 lb	12 lb	13 lb	14 lb	15 lb
Average	0.539	0.251	0.145	0.121	0.101	0.098	0.098	0.088	0.079	0.076	0.075	0.075	0.074
Max.	15.068	1.702	0.851	0.420	0.309	0.394	0.620	0.434	0.336	0.316	0.312	0.320	0.284
Std. Dev.	1.384	0.256	0.123	0.079	0.058	0.061	0.080	0.059	0.043	0.040	0.039	0.040	0.037

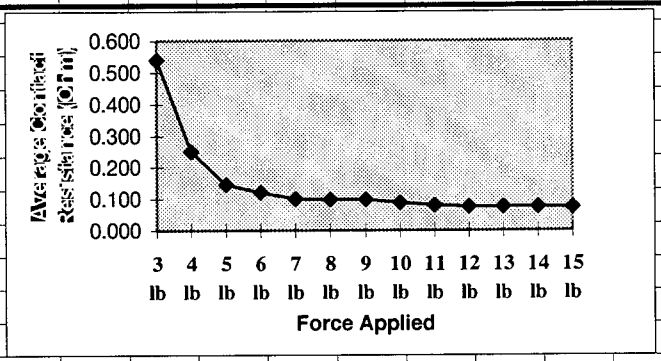


Figure 1. Contact Resistance Reading of Particleless Bumps on B0008 as a function of Force Applied

5 more samples of the same design were given to TI M&C (Mansfield) to evaluate them for any degradation in contact resistance after thermal and mechanical cycles. The following table tabulates the results of this evaluation.

	Die Insertion Cycles				
	100	200	300	400	500
Avg. Var.	-0.059	-0.084	-0.056	0.032	-0.070
Min. Var.	-0.819	-0.873	-0.864	-0.882	-0.878
Max. Var.	0.247	0.097	0.209	0.305	0.107

Table 1. Variation of Contact Resistance Readings vs. Die Insertion, Using a Particleless Bump and A Customer Designed Carrier.

	Temperature (Deg. C)		
	-15	**130**	**Room**
Avg. Var.	-0.261	0.919	-0.012
Min. Var.	-0.573	0.485	-0.214
Max. Var.	-0.165	1.324	0.164

Table 2. Variation of Contact Resistance Readings vs. Temperature, Using a Particleless Bump and A Customer Designed Carrier.

Conclusions: The particleless bumps seem to be as durable as the bumps with particles. Due to the absence of particles these bumps are more uniform than the bumps with particles. This had caused us to believe that units with particleless bumps would require less force to contact than others. As the data indicates, the contact resistances reduce more uniformly across the die, however, the total force needed to make optimum contact is the same with and without particles. This is believed to be caused by the fact the surface area of the contacts has been increased, and that more bumps have to be pushed down to make contact to all the bumps, however, the distance is much less, since the uniformity among the bumps are much higher.

SECTION 8

CARRIER USABILITY TESTER

The objective of this investigation was to evaluate different options which could determine if a carrier is still operational during its usage in a high volume manufacturing operation.

Background

During early evaluation phases of bare die carriers, it was determined that carriers within the same group will undergo a different number of die insertion and temperature cycles. To make sure that die carrier is not the cause for failure of the device (open failures), different options can be considered.

One is to monitor and keep track of the usage of the carriers during and through the operation. This would require elaborate tracking mechanisms at every stage of the operation, as well as a database and maintenance management to insure that a carrier is not used past its lifetime. This scheme also requires the manufacturers of the carriers to go through extensive evaluation processes to determine and guarantee the minimum life of their product, which in some cases would be very cost prohibitive. It is also determined that in some applications, the end life of the product would never be reached.

Another option is to provide a tool which would determine if a carrier is still usable. Such a tool/tester can then be placed at the beginning or the end of the operation and would be independent of the process, product, or application. This provides a more practical approach, by creating a universal solution that can be applied to different manufacturing approaches and different carrier technologies and products.

Systems Considered:

MMS had already conceptualized a system where a measurement unit is integrated into a die to carrier pick and place system. Two different configurations were considered.

The first configuration is to test the carrier using a coupon inserted onto the carrier, and then measuring the resistance of the traces and the contacts through the coupons. This configuration was abandoned since it adds an extra step to the die pick and place operation and it could also reduce the life of the carrier by increasing the number of insertions.

The second configuration verifies that the die pads are making the proper contact with the die carrier during or after the placement of the actual die into the carrier. Using this system insures the operation of the carrier while verifying that good contact is achieved

between the die and the carrier after the assembly operation. Two different measurement schemes of this configuration were considered.

Option 1 - Capacitance Measurement Unit

We looked into expanding one of MMS' existing capacitance measurement units which is designed to detect small variations in trace length. This system would first calibrate itself with each carrier and its trace lengths, and then look for variation in capacitance value once the die is placed onto the carrier.

Although feasible, the cost of such a system does not lend itself to be low enough for such an application.

Option 2 - Parametric Measurement Unit

In this scheme, a Parametric Measurement Unit (PMU) looks for an active device at the end of each trace by driving/sinking a small current through the traces. This configuration does not require a calibration process since it is independent of the individual carriers' trace lengths.

We believe that this configuration can be made inexpensive enough to be adaptable into high volume manufacturing applications.

Recommendations

There are still other questions that need to be answered:

- Is the carrier usage longer than the carrier/contacter life?
- Would it be less expensive to keep track of ICs' open failures and point to potential carrier problems if same open failure is observed with two different dice in a same carrier?
- When is it economical to add such a operation to the line?

Thus, further cost analysis of such a system with respect to existing carrier technologies and their applications in high and low volume manufacturing operations is recommended.

SECTION 9

RESISTANCE MEASUREMENT SYSTEM

In order to achieve accurate data with reduced potential to effect the results with manual inaccuracies, two systems were put together, modified and enhanced. This section describes the system configurations of these systems, and the enhancements necessary for their appropriate operation for this phase of this ARPA project.

4 Point Measurement System

Components:

- **1 x Keithly 580 MicroOhm Meter**

- **1 x Keithly 707 Switching Matrix.** An analog and digital switching matrix controller mainframe with six plug in card slots. The system provides three separate analog backplane for automatic switching card interconnect.

- **3 x Keithly 7075 Multiplexer Cards.** A general purpose multiples switching card that consists of eight banks of independent 1x12 multiplexer switching. Each bank has two switched circuits. The row is connected through jumpers on the card to the general purpose analog backplane in the model 707 switching mainframe. This provides the interconnect between the cards for multiplexer expansion (1x24, 1x36, etc.). A single card can be expanded to 1x96 by reconfiguring the supplied bank-to-bank jumpers. Eight 25 pin D connectors are provided for bank connections and one for row connection.

Force Applicator System

A standard MRSI-503 flip-chip pick & place system was chosen as the base system for die pick & place and force applicator/indicator system. The system was initially modified by MRSI to include

- Accurate die pick & place, from a Gel-Pak to a target substrate/carrier.
- Apply a controlled, user selected downward force on the die.

The main reason to select the 503 model as the base system was its capability to "look up and look down" with reasonable accuracy and cost.

MMS encountered numerous issues with the system as it was delivered. The major issues and their corresponding solutions are listed below.

- The equipment had no means of locking Theta stage.
  ⇒ A new bracket with locking jackscrew was designed and fabricated.
- The force actuating mechanism was designed with a different air pressure system. This system utilized an air cylinder moving a stage by introducing air at a higher pressure on one port and a lower pressure on the opposite port (Differential air system). The regulators used here was the non-relieving types and as such no "real time" force adjustment was possible. This system was also unstable.
  ⇒ A new cross roller slide mechanism with a spring backing and thumb screw adjustment was designed and installed. This allowed us to bypass the pneumatic system and all its unstable elements.
- The force gauge that was installed by the equipment vendor was an incorrect application of this type. This caused repeated failure of the force measurement system and the unit had to be sent back to manufacturer for installation of a new type of force gauge.
  ⇒ The whole force measurement system was replaced by the vendor
- The downward force acting independently on the die did not simulate the test carrier in such that there was no correlation between the test carrier and the MRSI-503 system. It was determined that somehow the downward force must be exerted to the die and the substrate assembly without pushing the whole substrate downward while sitting in the socket.
  ⇒ A new mechanism was designed and fabricated that allowed the operator to lock a ring on the two posts of the carrier before any downward force is applied on the die in the carrier.

SECTION 10

RECOMMENDATIONS FOR FURTHER RESEARCH

Moly Substrate Process & Product Specifications: Based on Phase I research, use of Moly wafers appears to be the best choice for specified applications which must accommodate large ICs with small pad pitches and pad openings. However, for Moly substrates to be cost effective and compatible with MMS' current fabrication processes, better product specifications must be developed.

Carrier Usability Tester: Further cost analysis of carrier usability test systems with respect to existing carrier technologies and their applications in high and low volume manufacturing operations must be conducted, before further developement of such a system is recommended.

Bump Height Enhancement: Existing proximity and projection alignment processes used to define bump height and bump diameter, pose disadvantages in terms of bump uniformty and cost. Use of laser direct write technology (maskless) would allow more uniform exposure of the surface material due in part to elimination of the slope that is associated with conventional photolithography process, thereby improving bump height accuracy. In addition, elimination of masks would greatly reduce recurring costs which is especially high in small volume runs.