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An investigation was undertaken to determine the feasibility of integrating low temperature growth GaAs:As and silicon for the development of opto-electronic devices. These devices attempt to exploit the opto-electronic properties of LT GaAs while integrating the structure on silicon substrates. Numerical models of LT GaAs are developed and implemented to aid in the design of such devices. An integrated MSM-LED structure was successfully fabricated on a silicon substrate. The results of the study show that it is feasible to integrate LT GaAs devices and silicon technology. Further development of the design software and a variety of structures, including a high voltage switch, a transceiver and a GHz tunable filter are proposed for a Phase II effort.

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I. Introduction

I.1 Background

Progress in modern communication systems is significantly enhanced by the availability of high-bandwidth, high-responsivity photo-detectors. Presently, most communications circuits are silicon based; however, GaAs photo-detectors offer bandwidth and responsivity improvements over comparable silicon devices. Recently, low temperature (LT) grown GaAs has generated considerable interest since the demonstration of subpicosecond lifetimes and high quantum efficiencies with comparatively good mobility.

The issue of whether GaAs photo-detectors can be usefully integrated directly onto silicon circuits was affirmatively addressed by Frankel, et al. [1],who studied the influence of growth temperature and post-growth anneal on the photo-generated lifetime and mobility in LT GaAs grown on silicon substrates. They demonstrated, using femtosecond time-resolved reflectivity measurements, a reduction in carrier lifetime to less than 0.5ps; and fabricated photo-conductive switches with approximately 1ps full-width-at-half-maximum (FWHM), with little sacrifice in carrier mobility.

The demonstration that GaAs photo-detectors can be integrated directly onto silicon circuits is the basis for this Phase I study, as well as a proposed Phase II SBIR program, for which the goal was to *design and market opto-electronic integrated circuits in which III-V photonics is combined with silicon electronics.* The Phase I study, as summarized below, provided the first steps towards realizing this opportunity in successfully achieving the following objectives:

1. Demonstrate that LT gallium arsenide can be successfully deposited on silicon and elucidating its resulting properties, particularly the interface properties.
2. Demonstrate that the material properties of the LT GaAs/Si structure can be used to provide guidance for parametric modeling studies.
3. Demonstrate that the various interface properties be modeled and combined with the LT GaAs models under development at SRA.
4. Demonstrate that the transient dynamic characteristics can provide a predictive model for assessing the operation of LT GaAs photo-detectors on silicon substrates.
5. Demonstrate that the modeling can be ported so that others interested in pursuing similar objects can access the code.
6. Determine alternatives to the LT GaAs/silicon system.

The Phase I study was successful: (i) opto-electronic devices were fabricated and are currently being tested; (ii) transient design models were established.

I.2 Brief Summary of the Phase I Study

A team of workers at Scientific Research Associates, Inc. (SRA) and at Purdue University/ Mellwood Laboratories proposed, under the Phase I SBIR effort, to establish a set of parameters for the development of GaAs/ Si optoelectronic devices. Under Phase I the SRA tasks were to identify key parameters associated with transient switching of the LTG materials under photo-excitation, and to develop physical models. The Purdue University/Mellwood Laboratories group was to establish the growth conditions for GaAs/Si integration.

The tasks were broken down as follows: The *Purdue University/Mellwood* group with Professors M. Melloch and J. Woodall as consultants used established procedures for nucleating GaAs on Si. This involved sequentially:

- a high temperature anneal (900°C) of a 4-degree off-axis (100) Si substrate;
- growth of a thin 100nm layer of GaAs at 400°C to generate a high density of GaAs nucleation sites;
- a 10 minute anneal under an As flux at 700°C to anneal defects and allow the misfit dislocations to equilibrate.

For "standard" MBE growth the substrate temperature is returned to 600°C. The substrate temperature is ramped down to 225-350° (the exact temperature used depends on the target excess As) for LT GaAs growth. The growth is terminated when the desired thickness is reached.

These goals were achieved, altering the growth procedure was initiated, and procedures for the development of three device applications based upon combined MSM/LED structures was generated.

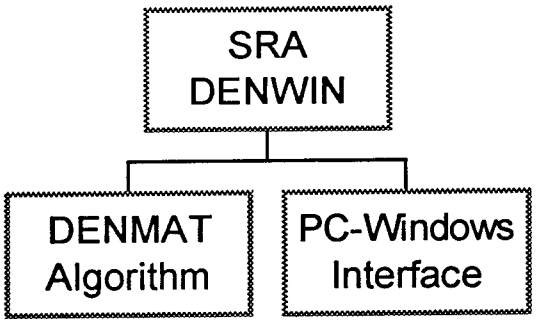
The *SRA Group* used numerical methods developed at SRA for:

- examining the response of LTG GaAs films to photo-excitation and relaxation back to equilibrium to observe differences in the time constants, and their dependence on material parameters;
- initiating design of the LED structures;
- determining the constraints in the design of the MSM/LTG structures, particularly with respect to the potential and charge distributions and their ability to respond to photo-excitation.

II. Simulation and Modeling Results

II.1 Background

There are two distinct parts to the numerical simulation of the MSM/LED structure. The LED structure is modeled using the density matrix algorithm developed at SRA, and/or the quantum hydrodynamic equations. The density matrix algorithm is presently configured for PC implementation under the name *DENWIN*. *DENWIN* is SRA's software package for studying quantum devices. As seen in the chart *DENWIN* includes *DENMAT*, which is SRA's FORTRAN algorithm for solving the quantum Liouville equation in the coordinate representation, and a *PC-Windows* interface.



There are two types of problems currently being solved using *DENMAT*, those in which the current through the structure is zero, and those for which the current is finite. All calculations performed with current flow include dissipation. Further, the physical structures for which the density matrix equations are solved are one-dimensional in coordinate space, but may be three-dimensional in the conjugate phase space.

The quantum Liouville equation in the coordinate representation for electrons is:

$$(1)\qquad \frac{\partial \rho}{\partial t}+\left(\frac{\hbar}{2mi}\right)\left(\nabla_x^2-\nabla_{x'}^2\right)\rho-\left(\frac{1}{i\hbar}\right)\left[V(\mathbf{x},t)-V(\mathbf{x}',t)\right]\rho+\left(\frac{\partial \rho}{\partial t}\right)_{scattering}=0$$

where $\rho(x,x',t))$ is the density matrix and $V(\mathbf{x},t)$ is the potential energy seen by the carriers, and includes contributions from any heterostructure interface and *Poisson's equation*. Dissipation is represented by the last term in equation (1). Density within the structure is obtained from the diagonal elements of the density matrix: $\rho(x,t)=\rho(x,x,t)$, and current is obtained from the diagonal element of the matrix: $j(x,x')=\left[\hbar/2m^*i\right](\nabla_x-\nabla_{x'})\rho$.

The details of the LED structure are shown in figure 1 and a *qualitative rendering* of the potential and density for a structure of this type is discussed in figures 2-5.

For the LED starting from the N^+ substrate, the 750 nm layer is a normal temperature buffer layer (i. e., start out with good quality MBE GaAs rather than the relatively poor quality GaAs substrate). The n-AlAs layer is a *lift-off* layer to be used to lift off the rest of the structure from the substrate. The 100 nm n-GaAs layer is a contact layer. *For the measurements underway at present we have not yet lifted the structure off the GaAs substrate, so contact to the n-region of the LED is made through the substrate. In the next stage when we lift off the structure, the AlAs region would be removed, and the $10^{18}/cm^3$ GaAs layer would then be in contact with the silicon. Likewise for the growth on silicon, contact will be made through the substrate (we can also make contact on top by etching down the $10^{18}/cm^3$ contact layer from the top).* Next the 200nm n-AlGaAs layer is the n side of the np heterojunction LED. The 50 nm i GaAs layer is in the depletion region of the LED to prevent the diffusion of Be into the AlGaAs layer. The 250 nm p-GaAs layer is the active region of the diode where most of the recombination will take place. The 50nm p-AlGaAs region is used as a barrier to electrons keeping electrons emitted from the n-AlGaAs inside the p-GaAs active region. The 50 nm p-GaAs layer is the contact layer for the p-side of the LED.

The 50 nm i-AlGaAs region is a barrier between the LED and the LTG-GaAs, and may also be useful as an etch stop for selective etches. The n-GaAs (500nm) is a transition between the LED and the LTG-GaAs MSM (doped slightly n-type to increase the carrier lifetime), and the 10nm i-AlGaAs layer on top is a surface passivation layer, as well as a cap for post growth anneals (helps prevent arsenic loss during anneal).

	i-Al(.2)Ga(.8)As,		10nm
Growth Temp 280C	n-GaAs,	1X10E17/cm3,	500nm
	i-Al(.6)Ga(.4)As,		50nm
	p-GaAs,	5X10E19/cm3,	50nm
Growth Temp 525C	p-Al(.2)Ga(.8)As,	5x10E19/cm3,	50nm
	p-GaAs,	5x10E19/cm3,	250nm
	i-GaAs,		50nm
	n-Al(.2)Ga(.8)As,	1x10E17/cm3,	200nm
	n-GaAs,	1x10E18/cm3,	100nm
Growth Temp 600C	n-AlAs,	1x10E18/cm3,	20nm
	n-GaAs,	1x10E18/cm3,	750nm
	N+GaAs Substrate: 083194A		

Figure 1. Details of the LED structure.

Calculations at SRA were performed using *DENWIN*, a *Windows*, based algorithm for solving the quantum Liouville equation in the coordinate representation, to obtain a rendering of the density profiles and to provide a basis in the later sections for the design principles to be addressed under the proposed Phase II study.

Figure 2 displays the equilibrium conduction band and valence band profile as well as the input band structure for a qualitative rendering of the equilibrium profile for the interior of the structure identified in figure 1. The structure is double hetero-pn diode, where the central 'i' layer has been ignored. Incorporating this layer would not materially alter the distribution of electron charge although it would elevate the potential energy within the p-GaAs region.

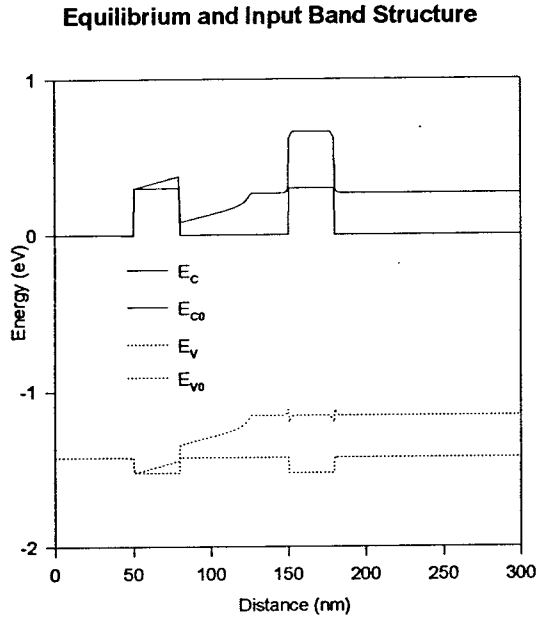


Figure 2. Equilibriun and input band structure for a rendering of an LED.

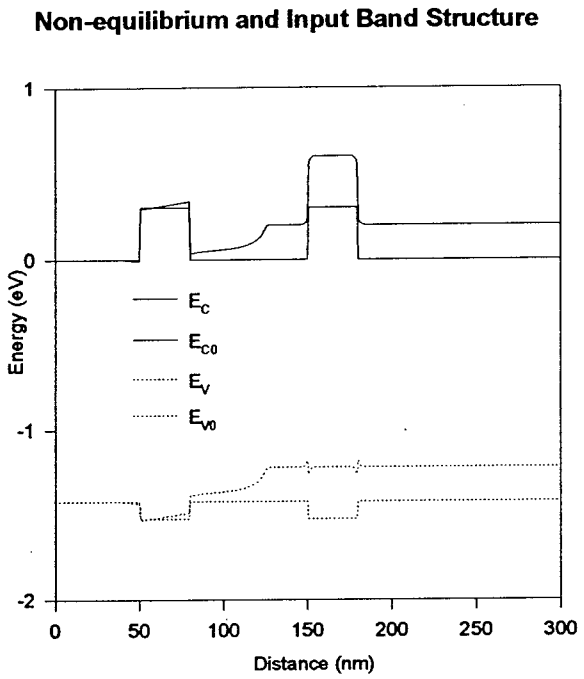


Figure 3. The nonequilibrium distribution of potential energy.

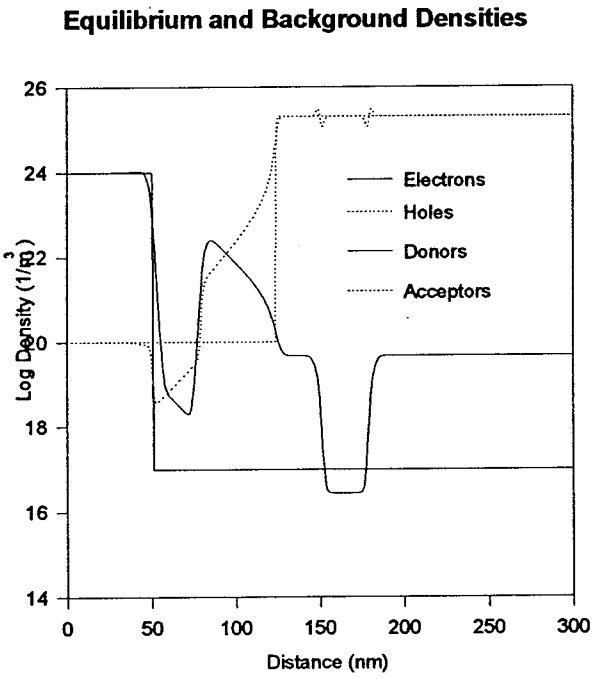


Figure 4. The equilibrium charge distribution associated with figure 3.

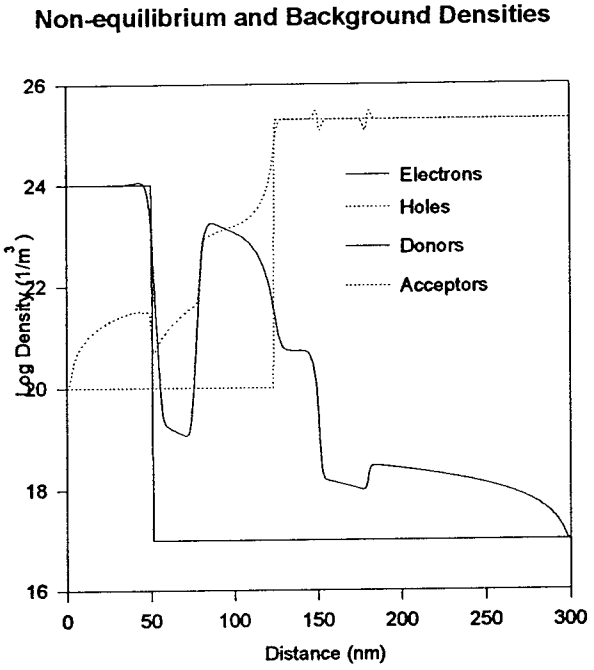


Figure 5. The non-equilibrium charge distribution associated with the potential distribution of figure 3.

The distribution of charge associated with figure 2 is shown in figure 4, where we see a significant population of charge within the p-GaAs region. The nonequilibriun potential energy, when the p region is negative with respect to its equilibrium value, is shown in figure 3. The corresponding charge distribution is shown in figure 5, where we see a substantial increase in the electron concentration in the p-GaAs region. It is within this region that electron-hole recombination takes place, with resultant optical excitation.

The transient behavior of the devices has been studied using **classical** equations.

The relevant equations are:

$$(2) \qquad \frac{\partial n}{\partial t} = \frac{1}{e}\nabla \cdot J_n + G_n - R_n, \qquad \frac{\partial p}{\partial t} = -\frac{1}{e}\nabla \cdot J_p + G_p - R_p$$

These equations identify local time dependent changes in electron n, and hole, p, carrier density arising from current flow and the generation, G, and recombination, R, of electrons and holes. In the above:

$$(3) \qquad J_n = -e\left(n\mu_n \nabla\psi + \phi_n - D_n \nabla_n\right) \qquad J_p = -e\left(p\mu_p \nabla\psi + \phi_p - D_p \nabla_p\right)$$

where ϕ_n and ϕ_p account for variations in the band structure arising from material interfaces. The material variations are used in the modeling of the clusters as work function differences and in the modeling of the gallium arsenide-silicon interface. The above equations are coupled to Poisson's equation

$$(4) \qquad \nabla \bullet \varepsilon \nabla \psi = e\left(n - p - \langle c \rangle\right)$$

where $\langle c \rangle$ is the net concentration of ionized donors and acceptors arising from both deep level traps, as well as shallow dopants.

The kinetics of capture and emission from multiple discrete levels of donor and acceptor traps (*as in the case of the the defect mode*) determine the recombination rates for electrons, R_n, and holes, R_p, introduced into equations (2) and (3).

$$(5) \qquad G_n - R_n = \sum_i C_{ni}^A \left(n_{1i}^A N_{Ai}^- - n N_{Ai}^0\right) + \sum_j C_{nj}^D \left(n_{1j}^D N_{Dj}^0 - n N_{Dji}^+\right) + \begin{bmatrix} generation\ due \\ to\ photoexitation \end{bmatrix}$$

where C_{ni}^A and C_{nj}^D denote capture rates of electrons from acceptors and donors, respectively. The superscripts on the trap levels denote '0' neutral traps, '+' positively ionized traps, '-' negatively ionized traps. For holes, the recombination rates are:

$$(6) \qquad G_p - R_p = \sum_i C_{pi}^A \left(p_{1i}^A N_{Ai}^o - p N_{Ai}^-\right) + \sum_j C_{pj}^D \left(p_{1j}^D N_{Dj}^+ - p N_{Dj}^o\right) + \begin{bmatrix} generation\ due \\ to\ photoexitation \end{bmatrix}$$

where C_{pi}^A and C_{pj}^D denote capture rates of holes from acceptors and donors, respectively. The n_1 and p_1 terms are obtained from equilibrium conditions, and under nondegenerate and single level trap conditions these are approximated by:

$$(7) \qquad n_1^A = N_C \exp -\left(\left(E_C - E_A\right)/k_B T\right), \quad n_1^D = N_C \exp -\left(\left(E_C - E_D\right)/k_B T\right)$$

$$(8) \qquad p_1^A = N_V \exp -\left(\left(E_A - E_V\right)/k_B T\right), \quad p_1^D = N_V \exp -\left(\left(E_D - E_V\right)/k_B T\right)$$

where the terms E_A and E_D denote the positions in energy of the trap levels.

Two distinct models were used to represent the properties of LTG materials. In one case a localized defect model was invoked to represent clusters. In earlier studies this was compared to the Schotkky model. As far as the dc characteristics were concerned

both models rendered the same information. While a major effort is underway under AFOSR Contract F49620-94-C-0024, to provide numerical simulations of the differences between these models particularly in the transient regime, distinctions between the two would have been impractical for the needs of the Phase I SBIR. We therefore, when dealing with clusters, dealt with the defect model.

The transient behavior of the structure is a consequence of two features: (i) the trap kinetics, and (ii) the clusters. In the defect model the clusters represent a high localized concentration of traps, with the traps governed by the trap kinetics. Thus two types of calculations were performed, one in which the trap kinetics was emphasized and the second in which we look for modifications in the trap kinetics due to the presence of clusters. Most of the results are for the former. The modifications due to the presence of clusters was also performed and is also discussed below.

II.2 Thin Film Trap Kinetics

We simulated the exposure of a film to 100mW band gap radiation. We note that the simulations are one-dimensional and uniform illumination is assumed. The LTG GaAs is modeled assuming deep acceptor 0.3 eV above the valance band at a density of $5x10^{17}/cm^3$. Deep donors, 0.69 eV below the conduction band at a density of $1x10^{18}/cm^3$ yield a mid gap Fermi level, 0.69 eV below the conduction band as well. Using accepted values for the capture coefficients in ordinary GaAs, the density of free electrons and holes, *in response to photo-excitation, and relaxation back to equilibrium,* after removing the source of excitation is shown in Fig. 6. The figure shows that in response to the excitation electrons and holes are rapidly generated. By 1.0 psec the electrons have reached a steady density level approximately three orders of magnitude greater than that without illumination. Holes closely follow the electrons. The densities of the electrons and holes for times less than 100 psec are governed by the generation/recombination time in the continuity equations. The trap rate equations have longer time scales and prior to 100 psec have not responded to the higher level of electrons and holes. Beyond 100 psec, the ionized donor population begins to decrease slightly in response to the excess electrons. Since the kinetics of the trap rate equations for the specified energy levels and capture coefficient dictate that the ionized acceptor trap concentration must be close to or equal to the ionized donors, the ionized acceptor concentration also declines. **As a result, the excess optically generated holes can no longer recombine at the same rate as the electrons and the hole density begins to rise again.** A new equilibrium is finally reached at about 1 msec. Here, the hole concentration reaches about $2.5\ 10^{13}/cm^3$ and is equal to the difference between the ionized acceptors and donors; i.e.,

$$0 = N_D^+ - N_A^- + h - e$$
$$\approx N_D^+ - N_A^- + h$$

where

$$e << h << N_D^+, N_A^-$$

When the optical stimulation is removed we observed a rapid reduction in electron concentration in less than 1 psec, but the holes remain at a high level until the traps respond to the reduced electron concentration on a 1 msec time scale.

If we examine the recombination terms in the continuity equations arising from the traps, we have

$$R_e = C_n n N_A^0 + C_n^+ n N_D^+$$

and

$$R_h = C_p^- p N_A^- + C_p p N_D^0$$

where $C_n = C_p^- = 1x10^{-5} cm^3/\sec$, $C_n^+ = 1.3x10^{-5} cm^3/\sec$, $C_p = 2.6x10^{-10} cm^3/\sec$. Now at equilibrium, with $N_D = 10^{18}$ and $N_A = 5x10^{17}$, $N_D^+ = N_D^0 = 5x10^{17}$, $N_A^- = 5x10^{17}$ and $N_A^0 = 0$. Thus, initial electron recombination takes place on a time scale of $\tau_e \approx 1/C_n^+ N_D^+ = .15$ psec. Holes also have an initial recombination time of $\tau_n = 1/N_A^- C_D^- = .2$ psec. The term involving N_A^0 in the electron recombination term is small because N_A^0 is always small compared to N_D^+. However, in the hole equation, N_A^- is approximately equal to N_D^0 and a second time constant $\tau_D' = 1/C_p N_D^0 = 7.7$ nsec is present. This same term appears in the trap rate equation and is responsible for upsetting the balance between ionized deep donors and acceptors on the long time scale which results in the long time increase in hole density.

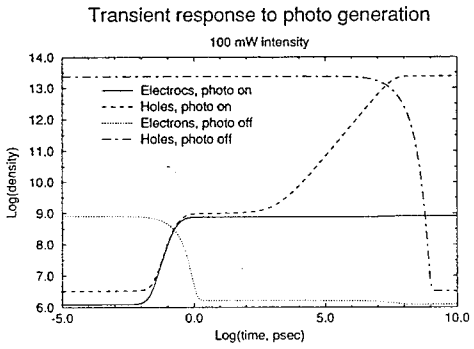


Figure 6. Transient response of LTG film to photo-excitation.

To verify this we repeated these simulations with C_p increased to $2.6x10^5 cm^3/sec$. The results, shown in Fig.7, show that the steady state value of the hole concentration is very close to that associated with the 1 psec time scale. Additionally, the initial hole decay from the illuminated state to dark is now on the 1 psec time scale. A long scale effect is still observed, however. The effect has been identified with the energy level of the acceptors compared to donors. In another simulation, we placed the acceptor traps 0.69

eV above the valence band and retained the increased value of C_p. The results reveal psec time scales for both electrons and holes with *no secondary time scales present.*

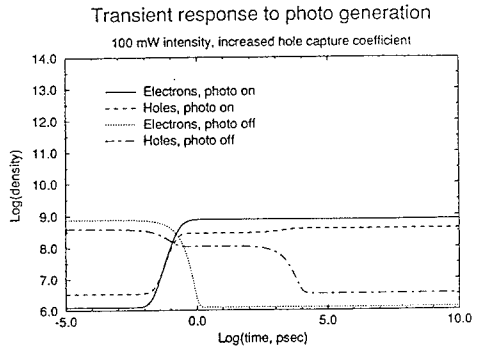


Figure 7. Transient response of LTG film to photo-excitation but with increased capture coefficients.

Further indications of the use of transients in determining the characteristics of LT GaAs are demonstrated with simulations in which the carrier lifetime was uniformly increased and decreased by a factor of 10. The structure used in these simulations is the *NIN* structure in which a 10 volt bias is placed across the device and 100 mW band gap radiation is applied to the "LT" region. Increasing (decreasing) the carrier lifetime results in an increase (decrease) in the steady state current, and a shorter (longer) turn on time.

II.3 Transient Limitations

A key ingredient in assessing the LTG structure is the response times and the role of the electron and hole transient contributions. The issue addressed was the minimum repetition rate that is possible with these materials. Figures 8 and 9 show the transient behavior of the current as well as electron and hole density over 10 cycles of 10 mW photo radiation. The electron response is symmetric over each cycle. However, the hole density does not relax to the initial state at the beginning of each cycle due to the longer relaxation time. As a result, over a large number of cycles, the excess holes will accumulate and the current transient may be altered. This is slightly observable in Fig. 9 as the "off" current increases slightly with time. When the hole lifetime is the same order as the electrons, both electrons and holes respond symmetrically to the light pulse and the off current level remains constant. *This result again shows the use of simulation in helping to reveal the precise physics of LT GaAs:As.*

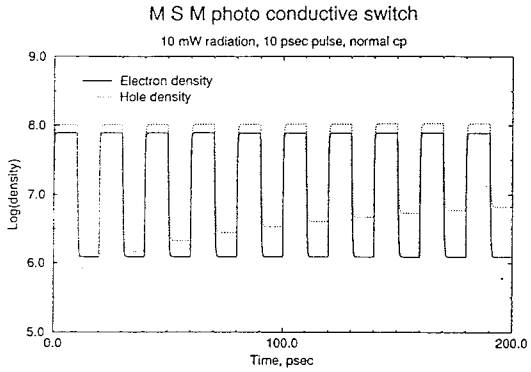


Figure 8. Response of electrons and holes to 10ps pulses, normal capture coefficients.

In the case of the MSM structure discussed in figure 1, one of the important features contributing to the transient behavior as elicited in the above figures is the potential distribution between, e.g., the interdigitated fingers. While a more realistic rendering requires a two dimensional simulation (which is discussed below) some information is gleaned from the one-dimensional studies discussed above. For example, in figure 10 we show the potential distribution across the device for 1 mW excitation at a time of approximately 1 nsec and for t greater than 10 msec. We observe no difference between the potential distributions before exposure and at 1 nsec. After 10 msec, we note a collapse in the field across the LT region. This is accompanied by a reduction in the photo current as well. The origin of this change is the different capture coefficients for electrons and holes which results in carrier depletion at the anode. *When the capture coefficients are equal there is no transient collapse in the potential at the anode.*

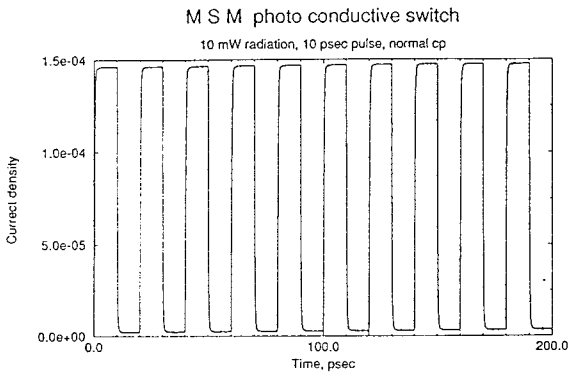


Figure 9. Response of current from figure 8 calculation.

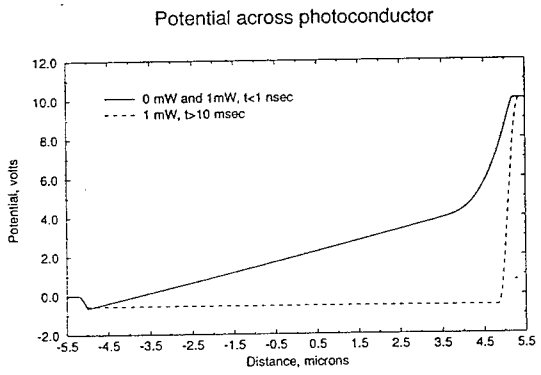


Figure 10. Transient potential distribution across the structure following optical excitaton.

II.4 Two-Dimensional Transients

The initial one-dimensional simulations were useful in establishing that the present approach to modeling of LT GaAs photoconductors is reasonable. However, two-dimensional effects are expected to play an important role in the design of photoconductive devices fabricated using LT materials. To begin to investigate two-dimensional

effects, we examined the same N-LT-N structure as used in the one-dimensional simulation. The device structure and the distribution of charge and potential under dark conditions were one-dimensional. However, whereas in the one-dimensional result, the photo-generation is assumed uniform; in the two-dimensional solution the generation decays with distance from the surface due to absorption of photons. The photon flux, and generation term are given as

$$\Gamma = \Gamma_o e^{-\alpha x}$$

and

$$G = \alpha\Gamma$$

where Γ_o is the photon flux transmitted through the surface, α is the optical absorption coefficient, and x is the distance of penetration measured along the optical path, in this case normal to the device surface. The initial photon flux, Γ_o is computed from the optical power

$$\Gamma_o = \frac{P_{opt}}{h\nu}$$

where

$$\nu = \frac{c}{\lambda}$$

Only photons with $h\nu \geq Eg$ can generate electron hole pairs. In our simulations we have assumed band gap radiation and take $\alpha = 1 \times 10^4$/cm.

The results for a transient switching of a square wave pulse of 5 psec duration is shown in figure 11 for an optical power of 100mW. The result is almost identical to the one-dimensional result (not shown). The peak current density is slightly lower, however. This is because the structure is assumed to be 1 μm deep and the photon flux has dropped to 0.3678 (1/e) of the surface value by the time the optical beam penetrates the device depth. The lower current density reflects the reduced flux, a two-dimensional effect.

An interesting detail which warrants discussion is the distribution of charge and potential within the device when illuminated. Due to the variation of the optical generation with device depth, the optically generated charge density shows a similar variation. However, at these power levels the charge density is not great enough to affect the potential distribution across the device. Thus, while there is an x direction dependence in optically generated charge, the resulting current is directed only in the z direction, the direction normal to the contacts. At higher optical power levels the density of the photo-generated charge would increase and at some point would affect the potential distribution, creating an x direction field. The current paths under such conditions will be more complex. Diffusion of carriers will also play a role; however, this is small due to the relatively low density of optically-generated carriers.

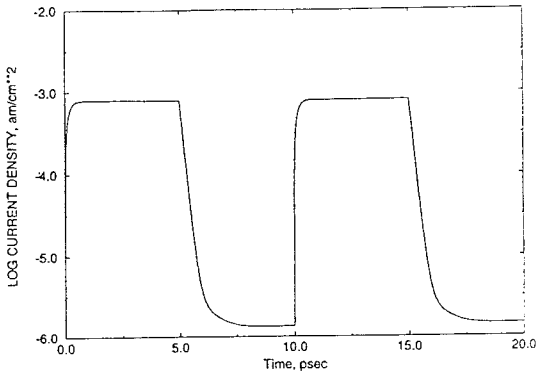


Figure 11. Transient current response for a two-dimensional simulation in which the generation rate is nonuniform.

After completion of these initial simulations we began to examine a structure representative of a section of a photo-conductive switch with interdigitated fingers. The structure is shown in figure 12 and is fabricated on a SI GaAs substrate. First a 2000 Å layer of high quality GaAs is grown, then 1 μm of LT GaAs:As is deposited. This material is annealed during the growth of a 200 Å GaAs cap layer. Ohmic contacts are located with 3 μm spacing. In our simulations the metallization is modeled as heavily doped N^+ regions which penetrate the GaAs cap layer and directly contact the LT GaAs:As. A 3 volt bias was placed across the structure.

The simulation proved very difficult from a computational viewpoint. To accurately obtain dark current levels requires super convergence of the numerical solution. While this is only time-consuming in one-dimension, it can be extremely difficult and extraordinarily time-consuming in two-dimensional simulations. The present results do not reflect accurate dark current levels.

After obtaining a moderately converged solution under dark conditions, we illuminated the devices from above at the 100 mw power level. The preliminary results for the current response are shown in figure 13. We see a rapid initial rise time but a failure of the current to saturate within 5 psec. The decay also shows a rapid initial response, followed by a secondary long time constant behavior. The longer time scales are being studied to determine their origin, i.e., computational rather than physical.

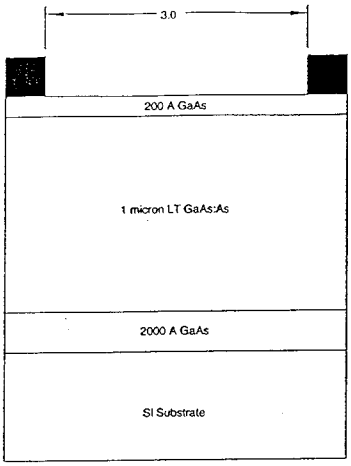


Figure 12. Two-dimensional representation of one section of an MSM structure,

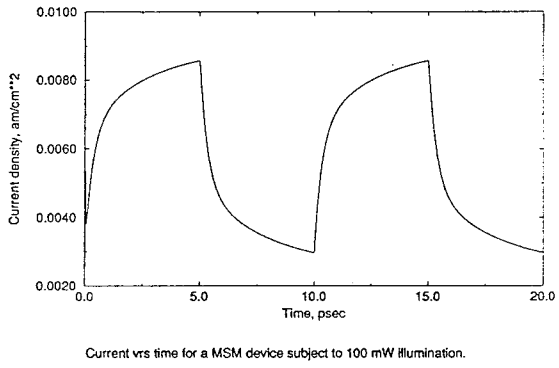


Figure 13. Transient current response for a two-dimensional simulation of the structure of figure 12.

II.5 Transients Cluster Calculations

Results were also obtained for a PIN structure in which clusters of high concentration of traps were used to model the LT material in the I region. A reverse bias of one volt was applied over a 5 μm structure. In the absence of illumination, the density of electrons and holes in the 'I' region is governed by the clusters and is shown in figure 14 to be on the order of the intrinsic concentration.

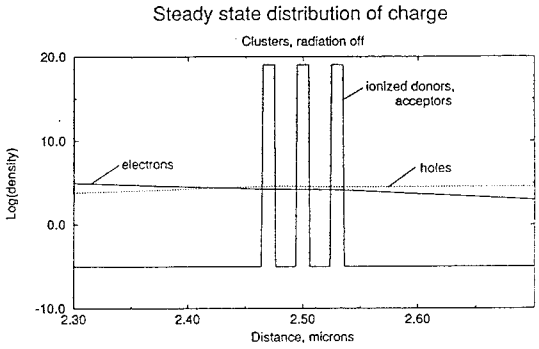


Figure 14. Steady state distribution of charge.

When illuminated at an optical power level sufficient to flood the I region with free electrons and holes, the resulting charge distribution is shown in figure 15. The electrons have neutralized some of the deep donors in the clusters and the holes neutralize some of the acceptors. However, the overall concentration of ionized traps remains high.

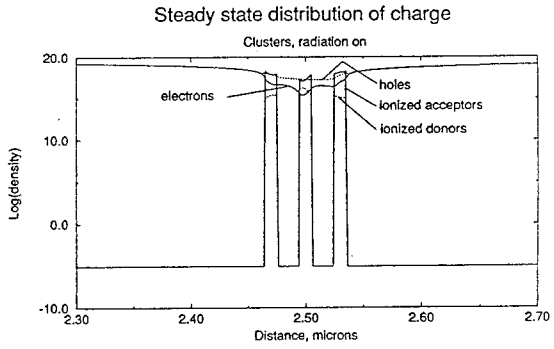


Figure 15. Steady state distribution of charge, radiation on.

One nanosecond after turning off the illumination, the distribution of charge appears as in figure 16. The electron concentration has begun to return to the pre-illumination state but the hole concentration remains high. There is a long time constant associated with the holes. The reason for this is presently unclear, based on results obtained for lower illumination. However, it may be due to the extremely high level of photo

generated carriers present, which significantly alters the trap states. This needs to be studied further under Phase II.

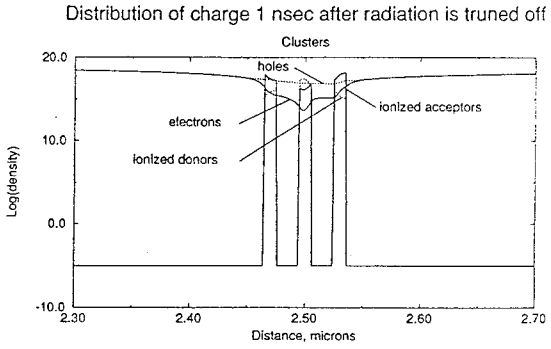


Figure 16. Distribution of charge after radiation has been turned off.

II.6 Interface Development

A key to success in this program is the ability to demonstrate the manufacturability of devices at low cost. It has being amply demonstrated that reduction in costs and improvement in devices can be obtained through design procedures. The revolutionary change in computational software has put design tools in the hands of many scientists and engineers.

Workers at SRA have, for the past several years, and recently very agressively, been configuring its numerical software for *PC Windows* and *UNIX Windows* enviroments. Interfaces have been develeped with user friendly menus. One of the objects of this study is to continue development of such interfaces particularly in the area of LTG based devices to enable the low cost design of these devices. To this end we have initiated the development of workstation software with graphical user interfaces (GUI). The user may select various options allowing him to setup and simulate a given device. After a solution is obtained, it is intended that results will be displayed graphically. Upon reviewing the results, the user will be able to alter various device parameters and repeat the simulation. Through the definition of an appropriate performance figure, the designer will be able to quickly identify improvements in device design.

III. Experimental Effort and Results

III.1 Introduction

The Phase I experimental work focused on determining applications for low temperature growth (LTG) GaAs suitable for product development. MellWood Laboratories completed the three tasks necessary for successful completion of the Phase I work. First, MellWood demonstrated that LT gallium arsenide could be successfully deposited on silicon for metal-semiconductor-metal (MSM) photodetector applications. Next, we designed an integrated LED-MSM structure which would allow MSM switches to be triggered via an integrated LED. Finally, we experimentally characterized this structure with growths on both silicon and gallium arsenide to assess the feasibility of the integrated LED-MSM device. The results of these initial experiments indicated that such a vertically integrated LED-MSM device is feasible and, indeed, is expected to fulfill our expectations as to ultimate device performance.

III.2 LTG-GaAs Growth on Silicon

MellWood's initial efforts focused on the growth of LTG GaAs on Si for possible integration of fast MSM detectors with silicon circuitry. Several recent publications have indicated that low temperature growth (LTG) of GaAs on silicon produces higher quality GaAs than "normal" temperature growths. In addition, low temperature growth of single crystal GaAs on GaAs has been realized down to substrate temperatures of 200°C. This LTG GaAs has exhibited a number of unusual properties that have been attributed to the excess arsenic incorporated during growth. Up to 2% excess arsenic may be incorporated in this layer and, when annealed to high (>600°C) temperatures, this excess arsenic precipitates into hexagonal arsenic clusters. The annealed material exhibits a very high resistivity and short carrier lifetimes, which makes this material nearly ideal for photoconductive switch and photconductive detector applications. As this material exhibits a large number of defects ($\sim 10^{17}$ cm^{-3} precipitates) which appear to contribute to the ideal photoconductive nature of this material, it might be expected that lattice mismatched growth may not substantially degrade photoconductive device performance. Indeed, recent publications of LTG-GaAs on silicon, as well as the work performed under Phase I of this SBIR, indicated that adequate photoconductive device performance with LTG-GaAs grown on silicon can be obtained [1-3].

There are several factors to consider for the growth of LTG-GaAs on silicon, the most important of which is the interface between the GaAs and the silicon. The two most important aspects of this interface are the silicon surface passivation and the initial monolayers of growth. As the Varian Gen II MBE system used for these growths does not have the capability to heat the substrate to temperatures greater than 900°C, it is impossible to desorb the native SiO_2 via thermal methods. Instead, we utilized a hydrogen passivation technique that prevents the oxide from growing on the silicon. The silicon wafers were prepared utilizing the RCA clean method ($H_2SO_4H_2O_2$, H_2O rinse, HF) with

the hydrofluoric acid as the final step. The silicon wafer was directly removed from the HF and placed in the entry chamber of the MBE system (note the HF solution does not "wet" a hydrogen passivated silicon surface, and hence the wafer is dry when removed from the solution). Reflection High Energy Electron Diffraction (RHEED) was utilized as the primary growth diagnostic. A 1x1 surface reconstruction was observed until the silicon substrate was heated to temperatures greater than 600°C, resulting in the desorption of the hydrogen passivation and the appearance of a 1x2 surface reconstruction. The temperature of the silicon substrate was further increased to 900°C (thermocouple reading) to insure that the hydrogen passivation was completely removed and that bi-layer steps were formed. Next, the substrate temperature was lowered to 250°C. The gallium (and aluminum, in some cases) shutters were then opened to initialize the growth with a monolayer of group III metal. Next, the arsenic shutter was opened and growth commenced. After the first 500 Å of material was grown, the growth was interrupted and a high temperature anneal (750°C, 10 min) was performed to attempt to anneal defects and allow the misfit dislocations to equilibriate. Finally, the LTG-GaAs active region was grown.

The recipe for growth of GaAs on silicon was determined after a number of unsuccessful runs. The earlier growth runs lost their surface reconstruction patterns (RHEED) early in the growth sequence. It was determined that there were two contributing factors to this loss of surface reconstruction. First, if arsenic is deposited on the silicon substrate before or simultaneously with the gallium, subsequent growth is severely degraded as the silicon-arsenic bonds appear to prevent the formation of good quality gallium arsenide. Thus, we deposit a monolayer of gallium (or aluminum gallium mixture) to initiate the growth and prevent the formation of the silicon-arsenic bonds. Next, the growth temperature for these initial growths was too low (~200°C), resulting in the incorporation to too much excess arsenic, which forced the film to become amorphous. With the corrections to the growth conditions (predeposition of gallium, higher temperature growth) the resulting films exhibited reasonable RHEED patterns with some evidence of three-dimensional growth, rather than the usual two-dimensional growth experienced when gallium arsenide is grown on a lattice-matched substrate.

III.3 Combination LED-MSM Development

While the growth efforts on silicon were successful, and good quality MSM detectors were produced, it became clear during the study of these devices that other routes should be examined. The growth of LTG-GaAs on silicon is successful because the LTG-GaAs is insulating due to the arsenic precipitates, and hence additional structural defects due to the large lattice mismatch with silicon do not cause severe problems. Also, the fact that low temperature growth is utilized reduces the effect of the differences in thermal expansion coefficients between GaAs and silicon. We determined that the integration of high quality "normal" temperature growth GaAs is much more difficult. Since the ideal device for integration on silicon would be a transceiver, the growth must be able to produce high quality LEDs (or laser diodes). As LED efficiency is very dependent on material quality, the lattice mismatched growth on silicon would not produce sufficient quality devices. An alternative to direct growth of these devices on silicon is to grow the

structure on GaAs so that perfect lattice matching can be achieved, and later transfer the structure to the silicon via epitaxial liftoff [4,5], or substrate removal. Because of the unique nature of annealed LTG-GaAs, such a device is very sensitive to illumination, has a very high 'off' resistance (and hence low dark current), and is capable of holding off large voltages because of the high breakdown field strength of this material. Further development studied the integration of fast MSM detectors with light-emitting diodes (LEDs) in order to combine the optical receiver (MSM) with an optical transmitter (LED). The resultant device is an optically-controlled electrical switch where the optical control is produced by a high-efficiency LED (See Fig. 17). Thus, various electrical-to-optical-to-electrical operations may be performed. The final result is a very versatile device that has a variety of applications, from high voltage (>10 kV) pulse generation to high frequency (< 1 GHz) transceivers for short haul optical communications to tunable narrow band filters for operation in the 1 to 50 GHz range.

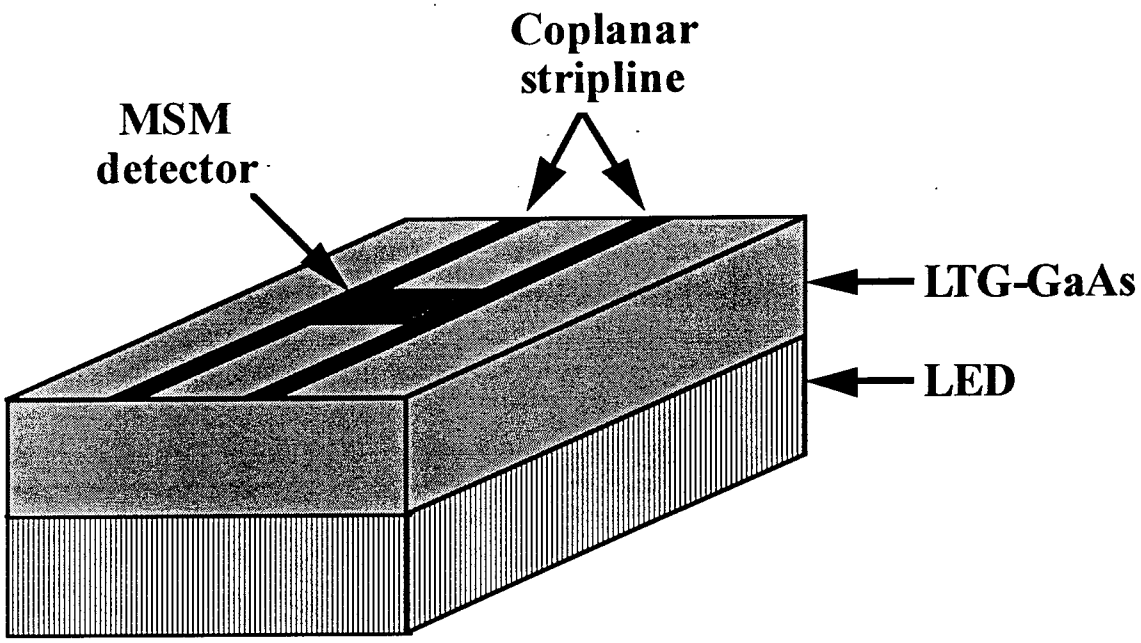


Figure 17. Schematic of the combination LED-MSM structure.

III.4 High Voltage Switch Development

The highly-resistive nature of annealed LTG-GaAs, combined with the high coupling efficiency between monolithic LEDs and the MSM photoconductor, should allow for very high switching efficiency (ratio of off resistance to on resistance). An ideal device would be capable of handling > 1kV applied bias with virtually no leakage currents. Once the LED is pulsed, the switch should instantaneously transition to an extremely low resistance operation, allowing at least 98% coupling efficiency between the high and low sides of the switch. If the bias is coupled into a 50 ohm high power transmission line, this requires the switch on resistance to be less than 1 ohm. This low on resistance can be

achieved by making the entire device large enough (many interdigitated fingers). Note also that since the LED structure is monolithically integrated underneath the MSM switch, the entire photoconductor would be illuminated, even the region under the fingers. Thus, the conductivity of the entire semiconductor region of the device will be considerably increased. Since high efficiency, large area LEDs are capable of emitting tens of milliwatts of optical power, the optical power should be sufficient to cause the illuminated LTG-GaAs to be very conductive. In addition, since we are considering time scales on the order of one nanosecond, it would be desirable to have the carrier lifetime be on the order of one nanosecond as photoconductivity is directly proportional to carrier lifetime. Thus, it appears that doped LTG-GaAs may be desirable for this application, as experimental evidence indicates that n-type LTG-GaAs has considerably longer lifetimes than that for undoped LTG-GaAs (< 10 psec lifetimes). In addition to high conductivity in the semiconductor, the contacts must not significantly contribute to the overall device resistance. Recently, Patkar, et al. [6] have developed a contact technology based upon LTG-GaAs that is very robust and results in very low specific contact resistances. The use of this LTG-GaAs contact technology should make the contact resistance for the MSMs negligible.

The key performance figure for a high voltage switch is the maximum voltage such a switch can hold off without breaking down. In many cases, if the device does break down, subsequent performance is considerably degraded. Currently, GaAs:As exhibits breakdown fields [7] in excess of 100 kV/cm (10 V/μm). If this breakdown field can be increased to greater than 10^6 V/cm (100 V/μm), then a switch capable of handling >1kV could be fabricated utilizing a MSM structure with 10 μm finger spacing. It has been determined that AlGaAs:As has a considerably higher breakdown field than GaAs:As, so AlGaAs:As will be uitilized for the high voltage switch. Note that this will necessitate the use of a similar mole fraction AlGaAs LED, in order to get significant absorption in the photoconductive AlGaAs:As. To produce switches capable of handling even higher voltages, it may be necessary to connect a number of 1 kV switches in series or to go to wider finger spacings. It will also be necessary to develop adequate isolation between the LED and the MSM photoconductive switch. If they are not adequately isolated, the high voltage on the MSM photoconductive switch will short out through the LED, resulting in breakdown at lower than anticipated voltages. It may be desirable to have the LED structure grown by MOCVD with a thick AlGaAs window on top to improve these isolation characteristics. The LTG-GaAs MSM could then be subsequently grown by MBE. This would result in the advantages of MOCVD for high efficiency LEDs and MBE for the LTG-GaAs (or LTG-AlGaAs) being combined for these structures. Note that once the growth of LTG-GaAs on production MOCVD LED films has been developed, we only need substitute a production MOCVD vertical cavity laser film, in order to monolithically integrate the LTG-GaAs with vertical cavity lasers.

Finally, we will qualitatively consider the design constraints of such a high voltage switch to insure that such a device is feasible. For these simple calculations, we will assume a switch voltage of 1 kV, 10μm by 10 μm fingers and spacings, and a 500 x 500 μm total device area. The breakdown field strength has been discussed above and should be

quite adequate for the devices under consideration. The other two important parameters are the off state leakage resistance and the on state conductance. To insure that thermal runaway is not a problem, we will require the device to dissipate less than 10 mW in the off state. A simple calculation indicates (Power=V^2/R) that the total device off resistance must be greater than 100 Mohm, or that the LTG-AlGaAs resistivity must be greater than 10^8 ohms cm, which is not difficult OT obtain in these LTG materials [7]. The on-state conductance is a little more difficult to achieve. A 2 kV pulse into a 50 ohm transmission line requires a source current of 20 amps. Assuming that the electrons in the device travel at a saturated velocity of $1x10^7$ cm/s and a device area of $1x10^{-4}cm^2$ (current conduction area for a 500 μm x 500 μm interdigitated device), this would necessitate 1.25×10^{17} cm^{-3} conducting electrons. To get this amount of electrons, an approximately 10 nJ optical input pulse would be required. Here it is important to note that the coupling efficiency between the LED and the LTG-GaAs will be very high because the dielectric constants will almost perfectly match and, since the *internal* quantum efficiency of GaAs LEDs approaches 100%, high efficiency LEDs should be able to produce the necessary pulses. Assuming a carrier lifetime in the LED of 10 nsec, the peak current density to the LED need only be 500 A/cm^2, well within the range of current device technology. This is a similar pulse energy to that required in the published reports of efficient high voltage switching in LTG-GaAs [8,9]. To directly compare our proposed device with published data, note that our proposed device utilizing interdigitated fingers has ~1/1000 the resistance of the simple gap structure used in ref. 9, and ~25 times larger area.

III.5 Transceiver Development

The only difference between the high power optical switch and a transceiver is that the transceiver is not required to hold off large voltages, thus 1 μm finger spacing and LTG-GaAs (no aluminum) can be readily used for this application. For this application, the speed of the LED is much more critical. A high luminescence LED with switching times near one nanosecond would be highly desirable. High efficiency LEDs with switching times less than 10 nanoseconds can be readily achieved [10] and switching times less than 1 nanosecond may be feasible. This would allow communication rates in excess of 100 Mbits/sec, 10 times faster than current ethernet rates. In addition, the omnidirectional nature of LED optical outputs would allow for wireless applications, as well as short haul optical fiber links. For this transceiver application, it may be desirable to integrate the transceiver directly on the silicon wafer to minimize interconnection noise. Since it appears that it is necessary to have the LED-MSM structure directly grown on GaAs because of the improved lattice matching, the devices would have to be transferred from the GaAs to the silicon substrate. Epitaxial liftoff techniques have been successful for high performance GaAs LEDs, so we expect the technique would be useful for LED-MSM devices. In addition, recent evidence indicates that substrate removal (utilizing an AlAs etch stop region), results in even higher performance for optical devices. Finally, it should be noted that replacing the LED with a vertical cavity surface emitting laser diode would allow for sub-nanosecond switching times and bandwidths in excess of 10 GHz.

III.6 GHz Tunable Filter Development

Finally, we explore the possibility of utilizing the combination LED-MSM in GHz tunable filter applications. Platte [11] has shown that periodic optical illumination of a coplanar waveguide on a photoconductive substrate can be utilized as a GHz filter element. The periodic optical illumination creates alternating regions of low (illuminated) and high (dark) impedance regions in the coplanar waveguide structure, which will selectively reflect certain frequencies when the Bragg condition is realized. By using many periods with alternating high and low impedance regions, a distributed Bragg reflector (DBR) , fig. 18, can be produced (in direct analogy of the distributed Bragg reflector used for semiconductor laser mirrors with alternating layers of high and low dielectric constants). Furthermore, Platte suggests that the frequency of operation of this DBR filter can be altered by changing the optical illumination so that length of the dark and illuminated regions is modified. In the LED-MSM structure, a large array of LEDs could be fabricated beneath the transmission line. By selectively applying current to these LEDs, certain regions of the transmission line could be illuminated, creating the low impedance regions. To re-configure the filter characteristics, all that is necessary is to choose which LEDs to turn on. This device could have far-ranging applications as a tunable filter for GHz applications.

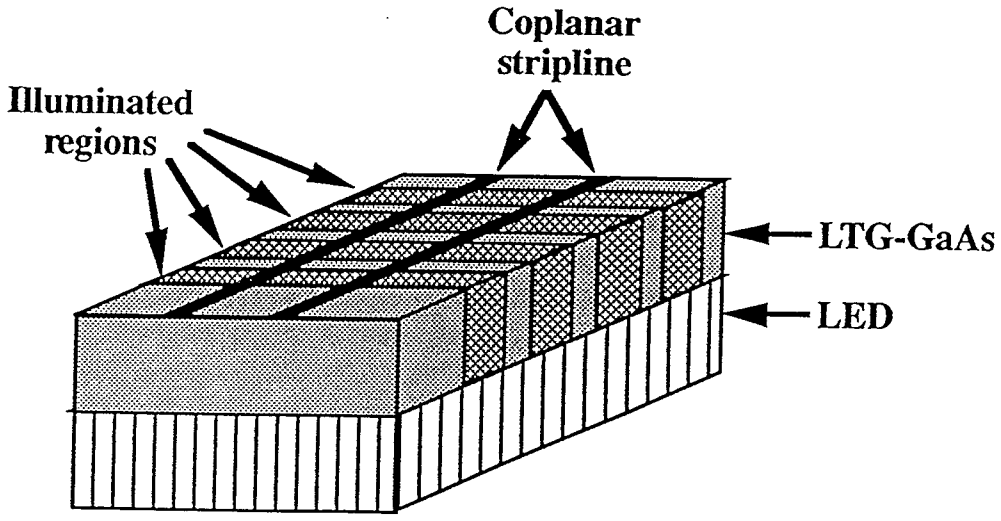


Fig. 18. Distributed Bragg reflector (DBR) achieved in a coplanar stripline by selectively illuminating regions of the LTG-GaAs, which would change the stripline impedance in these regions. The period and spacing of the array for reflection. Note that for this structure to be tunable, the illuminated sections would be generated by programming a large array of LEDs, with a number of adjacent LEDs being turned on for each illuminated region.

III.7 Initial Monolithically Integrated LED-MSM Results

The initial experiments on the integrated combination LED-MSM device were performed with three growth runs, two on a GaAs substrate and the other on a silicon substrate. The first growth runs (identical runs, one on a rate, one on a silicon substrate and the other on a GaAs substrate) utilized the film structure shown in Figure 19. In this structure, we see the active region of the LED is the $5x10^{19}$ cm^{-3} 0.25μm thick GaAs region, with $Al_{0.2}Ga_{0.8}As$ confinement regions. The MSM active region is the 0.5μm $1x10^{17}$ cm^{-3} LTG-n-GaAs region. The i-$Al_{0.6}Ga_{0.4}As$ region is included to provide isolation between the LED and the MSM, and also acts as an etch stop for a selective etch. The top i-$Al_{0.2}Ga_{0.8}As$ region is a protective layer on top of the MSM region. These two films were fabricated side by side, and the MSM and LED devices compared. We determined that the detectivity of the MSM structures was identical for both the growth on the GaAs substrate and the growth on the Si substrate. The LT-GaAs region grown on the silicon substrate appears to have about an order of magnitude smaller lifetime. While the MSM photodetectors produced were quite good for both growth runs, the LEDs were only suitable on the GaAs substrate. The light output of the LED on the silicon substrate was almost an order of magnitude smaller than that of the LED on the GaAs substrate, indicating that a significant amount of non-radiative recombination must be taking place on the silicon substrate.

While the LED and MSM devices could be made to work separately, we were not able to get the combination LED-MSM to work correctly. When the MSM was biased to a few volts and then a forward bias applied to the LED, we found that a large leakage current would appear in the MSM. This leakage current appeared to be directly proportional to the LED current, but did not appear to be due to the absorption of photons in the MSM region. On careful examination of the structure in Figure 3, it becomes apparent why this is the case. If we look closely, we can see a parasitic npn bipolar junction transistor (BJT) in this device where the n-type collector is the n-region of the LED, the base is the p-region of the LED, and the emitter is the LTG n-type GaAs. While this would not be a very efficient BJT, it could easily account for the leakage current observed, which was approximately three orders of magnitude smaller than the current through the LED. In addition to the parasitic BJT, we determined that bandgap shrinkage in the p++ region of the LED could be significant enough to result in almost negligible absorption in the MSM region. Since the bandgap shrinkage in $5x10^{19}$ cm^{-3} p-GaAs is expected to be greater than 200 meV, photons emitted from this region would not be strongly absorbed in "normal" GaAs.

In order to address these shortcomings, another structure was designed and tested. This design (see Fig. 20) is very similar to the first structure, with the addition of a 0.25μm low temperature growth $Al_{0.3}Ga_{0.7}As$ region to block the parasitic BJT current. This low temperature growth $Al_{0.3}Ga_{0.7}As$ region will be transparent to the light emitted from the LED, and is highly resistive. Additionally, the LED structure was changed so that the active region is now $Al_{0.15}Ga_{0.85}As$, in order to offset the bandgap shrinkage effects by increasing the bandgap of the semiconductor in the active region of the LED. The

aluminum content of the double heterostructure barriers surrounding the active region of the LED was also increased to insure adequate carrier confinement inside the active region of the LED.

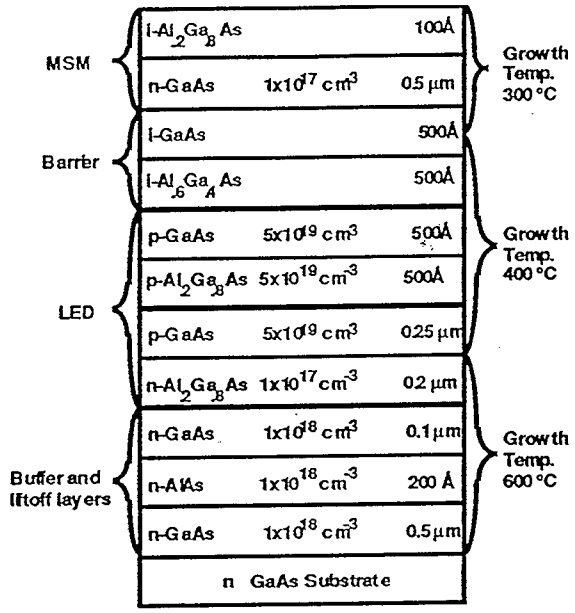


Figure 19.
Film structure for the combination LED-MSM initial growth. The LED region is a p-n double heterojunction diode to confine the injected electrons in the heavily doped p-GaAs region. The Barrier region is to prevent the flow of current between the MSM and the LED structures. The MSM structure is lightly n-doped in order to increase the carrier lifetime and hence increase the responsivity of the MSM detector. The AlGaAs region on top of the active region of the MSM detector is a diffusion barrier to prevent the out diffusion of arsenic from the LTG n-GaAs region.

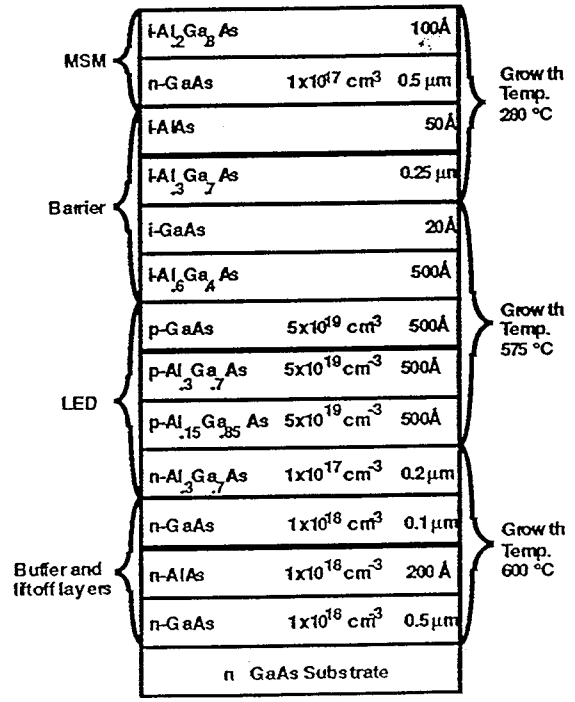


Figure 20.
Cross-sectional diagram of second iteration of combination LED-MSM device. This structure is similar to that presented in Fig. 19, with two important changes. First, the wavelength of the output of the LED has been significantly shortened to insure that the light generated in the LED is absorbed in the MSM. The output wavelength is shortened by increasing the Al mole fraction in the active region of the LED. Second, the Barrier region between the MSM and the LED has been enhanced by utilizing a highly-resistive LTG-AlGaAs region.

This second growth run successfully demonstrated that the combination LED-MSM concept works. The MSM detectors exhibited very good sensitivity to the light generated by the LED. The current-voltage response of the LED is shown in Fig. 21, where curve #1 (uppermost trace) shows the I-V response of the LED, curve #2 (middle trace) shows the corresponding current detected by the MSM versus the voltage applied to the LED, and curve #3 (bottom trace) shows the leakage current through the MSM versus the voltage applied to the LED. In general, we expect the light output of the LED to be proportional to the current through the LED, so the light incident on the MSM detector would be proportional to the LED current (note that the saturation at high current levels is due to resistance in the LED and to the current compliance level of 10mA). The leakage current was determined by applying zero bias across the MSM and measuring the current through the MSM. When two volts was applied across the MSM, a much higher current was observed, which must result from the absorption of photons emitted by the LED. Note that the test devices are very inefficient at collecting the light generated by the LED. Half of the generated light is lost through the substrate, and the device structure is such that only about 1/10 of the light that is not lost through the substrate illuminates the fingers of the MSM.

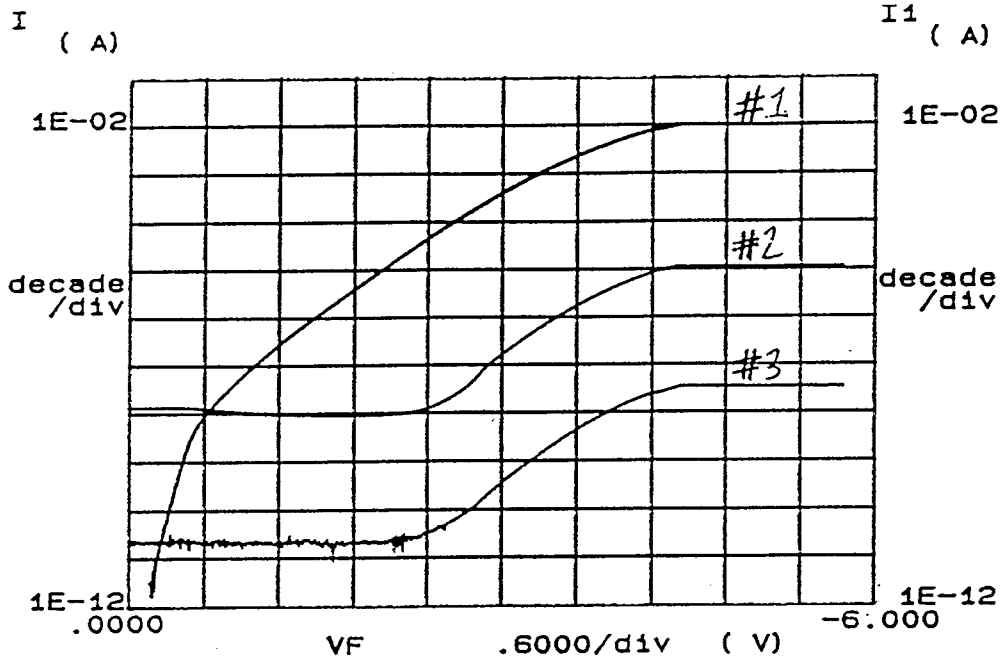


Figure 21. Current-voltage characteristics of the combination MSM-LED structure. Curve #1 shows the LED characteristics. Curve #2 shows the current detected in the MSM with two volts across the MSM. Curve #3 shows the leakage current detected in the MSM with zero volts across the MSM.

These results demonstrate that a MSM switch triggerable by a monolithically integrated LED is feasible. Future research and design efforts must be focused on reducing the leakage currents to negligible levels and increasing the breakdown fields of the MSM switch. The leakage currents may be reduced by increasing the thickness, aluminum mole fraction, and excess arsenic in the AlGaAs barrier layer between the LED and the detector. It may also be possible to improve the barrier layer by isolation junctions.

IV. Recommendations for Further Research

The work reported here has shown that it is feasible to develop and apply models of LT GaAs for the simulation and design of photo-optical devices and switches. However, to provide useful design tools will require continued development of the simulation models and the incorporation of the models in PC-based software. This software should include both one and two-dimensional, as well as transient capability. The development of such PC-based tools would be pursued under a Phase II effort.

In conjunction with continued software development, it is clear that the effort to integrate silicon and low temperature grown GaAs should be continued. We have demonstrated the possibility of integrating LED's and MSM structures on silicon and have indicated how this structure can be applied to high voltage switches, transceivers, and a GHz tunable filter. Optimization of these structures will require a combined analytical, experimental effort which would be the natural extension of the present work through a Phase II program.

We believe, based on the results of this Phase I study, that both software and hardware products are a potential outcome of this program.

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