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THESIS

ANALOG PREPROCESSING IN A SNS 2μ LOW-NOISE CMOS FOLDING ADC

by

Richard D. Carr

December 1994

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Significant research in high performance analog-to-digital converters (ADCs) has been directed at retaining part of the high-speed flash ADC architecture, while reducing the total number of comparators in the circuit. The symmetrical number system (SNS) can be used to preprocess the analog input signal, reducing the number of comparators and thus reducing the chip area and power consumption of the ADC. This thesis examines a Very Large Scale Integrated (VLSI) design for a folding circuit for a SNS analog preprocessing architecture in a 9-bit folding ADC with a total of 23 comparators. The analog folding circuit layout uses the Orbit 2μ CMOS N-well double-metal, double-poly low-noise analog process. The effects of Spice level 2 parameter tolerances during fabrication on the operation of the folding circuit are investigated numerically. The frequency response of the circuit is also quantified. An Application Specific Integrated Circuit (ASIC) is designed.

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ANALOG PREPROCESSING IN A SNS 2μ LOW-NOISE CMOS FOLDING ADC

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Submitted in partial fulfillment
of the requirements for the degree of

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from the

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December 1994

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ABSTRACT

Significant research in high performance analog-to-digital converters (ADCs) has been directed at retaining part of the high-speed flash ADC architecture, while reducing the total number of comparators in the circuit. The symmetrical number system (SNS) can be used to preprocess the analog input signal, reducing the number of comparators and thus reducing the chip area and power consumption of the ADC. This thesis examines a Very Large Scale Integrated (VLSI) design for a folding circuit for a SNS analog preprocessing architecture in a 9-bit folding ADC with a total of 23 comparators. The analog folding circuit layout uses the Orbit 2μ CMOS N-well double-metal, double-poly low-noise analog process. The effects of Spice level 2 parameter tolerances during fabrication on the operation of the folding circuit are investigated numerically. The frequency response of the circuit is also quantified. An Application Specific Integrated Circuit (ASIC) is designed.

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I. INTRODUCTION

Analog-to-digital converters (ADCs) form an integral part of an ever expanding base of hardware applications. From telecommunications to personal computers, ADCs which are faster, smaller, and dissipate less heat are in high demand. Significant research in high performance ADCs have been directed at retaining part of the high-speed flash ADC architecture, while reducing the total number of comparators. The symmetrical number system (SNS) can be used to preprocess the analog input signal, reducing the number of comparators, and thus reducing the chip area and power consumption of the ADC.

The SNS preprocessing is used to decompose the analog amplitude analyzer operation into a number of parallel sub-operations (moduli) which are of smaller computational complexity. Each sub-operation symmetrically folds the analog signal with a folding period equal to the modulus. A small comparator ladder mid-level quantizes each folded output. Each sub-operation, or channel, only requires a precision in accordance with that modulus. A much higher resolution is achieved after N different SNS moduli are used and the results of these low precision sub-operations are recombined. After the input signal has been preprocessed and quantized, the outputs of the comparators are applied to a channel programmable logic array (PLA). The output of this channel PLA represents the thermometer code in its SNS binary format. A second PLA is used to transform the SNS binary format into a standard binary number. [Refs. 1, 2]

A. RESEARCH GOALS

This thesis examines a folding circuit design for the SNS analog preprocessing architecture of a 9-bit folding ADC. Using an existing analog folding circuit design, a layout using the 2μ Complementary Metal-Oxide Semiconductor (CMOS) N-well process is implemented in a Very Large Scale Integrated (VLSI) circuit [Ref. 2]. The design and layout of the folding circuit is accomplished utilizing the VLSI Computer Aided Design (CAD) tool, Magic, developed by the University of California at Berkeley.

Simulation of the folding circuit layout is conducted using HSPICE, the industrial grade circuit analysis product from Meta-Software, in order to verify proper functional operation and to confirm the layout before fabrication. An Application Specific Integrated Circuit (ASIC) is designed using the Orbit 2μ CMOS N-well double-metal, double-poly, low-noise analog process. The effects of Spice level 2 parameter tolerances during fabrication and the frequency response is investigated and quantified. The chip has been fabricated and is currently undergoing testing.

B. THESIS OUTLINE

This thesis begins with a discussion of the symmetrical number system and its application to analog preprocessing. An overview of the design for a SNS 9-bit folding ADC architecture utilizing this analog preprocessing is presented. This overview includes both the analog and the digital portion of the ADC. The software tools used in the layout and simulation of the architecture are described.

Following this initial background information, the analog preprocessing architecture is presented in circuit form. A single folding stage is described which includes a differential amplifier pair and a current mirror. A summing amplifier used to connect the various folding stages and a voltage shifter are also discussed. The complete folding circuit for the SNS 9-bit folding ADC design is then discussed.

The main body of this thesis documents the implementation and simulation of an analog preprocessing architecture which uses a 2μ CMOS N-well VLSI process. The VLSI layout of each of the folding circuits is presented, along with the layout problems encountered. Simulation of the VLSI layout is conducted, including both a DC and transient analysis. The frequency response of the folding circuit is investigated and compared to the original Spice design. Spice level 2 parameters supplied by the Metal Oxide Semi-conductor Integrated Service (MOSIS) for two manufacturers are used in the simulation to show the effects of fabrication parameter tolerances on the folding circuit performance. It was discovered that these effects were quite significant and required modification of the individual folding stages in order to compensate for these tolerances.

Following the discussion and simulation of the folding circuit, this thesis investigates the design and layout of an application specific integrated circuit. Due to the size constraints on the substrate, only a portion of the folding circuits were included, reducing the dynamic range of the designed SNS 9-bit folding ADC. A summing amplifier and voltage shifter is included for each of the folding circuits in order to produce the proper folding waveforms that are used to drive several digital ASIC chips currently being

designed and fabricated. Finally, this thesis summarizes and offers recommendations for further research in the use of analog preprocessing in a VLSI design of a SNS 9-bit folding ADC.

II. BACKGROUND

A. SYMMETRICAL NUMBER SYSTEM

The symmetrical number system (SNS) is made up of a given number of pairwise relatively prime (PRP) moduli. Each SNS modulus m contains a unique set of integers which are derived from a symmetrically folded waveform. Values for this unique set of integers are produced by mid-level quantization of the symmetrically folded waveform. This unique set of integers forms a series in each SNS modulus which repeats itself with a period equal to the modulus.

The integer values within a modulus m can be generated with the following equations:

$$\bar{x}_m = [0, 1, ..., \lfloor m/2 \rfloor, \lfloor m/2 \rfloor, ..., 2, 1] \quad \text{for } m \text{ odd}, \tag{1}$$

and

$$\bar{x}_m = \left[0, 1, ..., \frac{m}{2}, \frac{m}{2} - 1, ..., 2, 1 \right] \quad \text{for } m \text{ even}. \tag{2}$$

Using this definition, a modulus 7 (mod 7) set would be the row vector [0,1,2,3,3,2,1,...], while a modulus 8 (mod 8) set would be the row vector [0,1,2,3,4,3,2,1,...]. Note that in each of the cases, the integer values repeat at a period equal to the modulus m. [Ref. 1]

A more efficient definition of a SNS modulus m involves the generation of a unique set of integers which repeats itself with a period equal to twice the modulus. This method has been described as the optimum SNS and is used for the design of the analog

preprocessing architecture in this thesis. The integer values within a modulus m can be generated with the following equation:

$$\bar{x}_m = [0, 1, ..., m-1,\ m-1, ..., 1, 0]. \tag{3}$$

Using this definition, a modulus 7 (mod 7) set would be [0,1,2,3,4,5,6,6,5,4,3,2,1,0,...], while a modulus 8 (mod 8) set would be [0,1,2,3,4,5,6,7,7,6,5,4,3,2,1,0,...]. Note that in this case, the integer values repeat at a period equal to twice the modulus, $2m$. [Ref. 3]

B. ANALOG PREPROCESSING

Due to the presence of ambiguities within a modulus, a single modulus does not form a complete residue system. However, a combination of N different moduli can detect and correct these ambiguities. This combination describes a number system that has a one-to-one correspondence with a residue system. By merging or recombining the integer values for each of the N different moduli, a numerical pattern is produced that does not repeat until the dynamic range M is reached. For the optimum SNS, the dynamic range is given by

$$M = \prod_{i=1}^{N} m_i . \tag{4}$$

An example of an optimum SNS with $m_1 = 3$ and $m_2 = 4$ is shown in Table 1. The dynamic range M for this system is 12, which also corresponds to the position of the first repetitive moduli row vector. [Ref. 4]

Dynamic Range	SNS Moduli	
	4	3
0	0	0
1	1	1
2	2	2
3	3	2
4	3	1
5	2	0
6	1	0
7	0	1
8	0	2
9	1	2
10	2	1
11	3	0
12	3	0
		$M = 12$

Table 1. Optimum SNS Preprocessing [From Ref. 3]

In optimum SNS analog preprocessing, a system is constructed based on N different moduli (channels) that will produce the desired dynamic range from Equation 4. An input signal is applied to the N different channels in parallel. Each channel is composed of a folding circuit that folds the input signal with a period based on twice the value of the corresponding modulus. The folded waveform that is produced at the output of each folding circuit is mid-level quantized with a small comparator ladder. The output of the comparator ladder represents the input signal in the SNS format.

C. OVERVIEW OF A SNS 9-BIT FOLDING ADC DESIGN

The architecture for this thesis incorporates the optimum SNS encoding into a 9-bit folding ADC using three parallel channels [Ref. 2]. In order to provide 9-bit resolution, a dynamic range M of 2^9 or 512 is necessary. Moduli chosen to provide this dynamic range M are $m_1 = 7$, $m_2 = 8$, and $m_3 = 11$. Using Equation 4 to calculate the dynamic range provided by the optimum SNS encoding yields a value of 616, which is well above the required 512.

The input signal is applied to each channel in parallel. Each channel is composed of a number of folding stages that produce a folded waveform with a period equal to twice the modulus. A small comparator ladder consisting of m_i - 1 comparators mid-level quantizes the folded output from each channel. The outputs of each comparator ladder are applied to a programmable logic array (PLA). The output of each channel PLA represents the thermometer code in its optimum SNS binary format. Another PLA is then used to transform the optimum SNS binary format into a more convenient digital output

(e.g., binary). Figure 1 shows a block diagram of a SNS 9-bit folding ADC along with the number of outputs from each major block.

The SNS 9-bit folding ADC design can be conveniently divided into an analog and a digital portion. The folding circuits for each channel form the analog portion of the ADC, while the comparators, channel PLAs and PLA comprise the digital portion of the ADC. Figure 2 is a functional block diagram of the SNS 9-bit folding ADC design. It is divided into its analog and digital portions and includes the number of individual components that make up the various sections of the modulus 11 channel. This thesis investigates the analog portion of the SNS 9-bit folding ADC design and its layout using a 2μ CMOS N-well low-noise process.

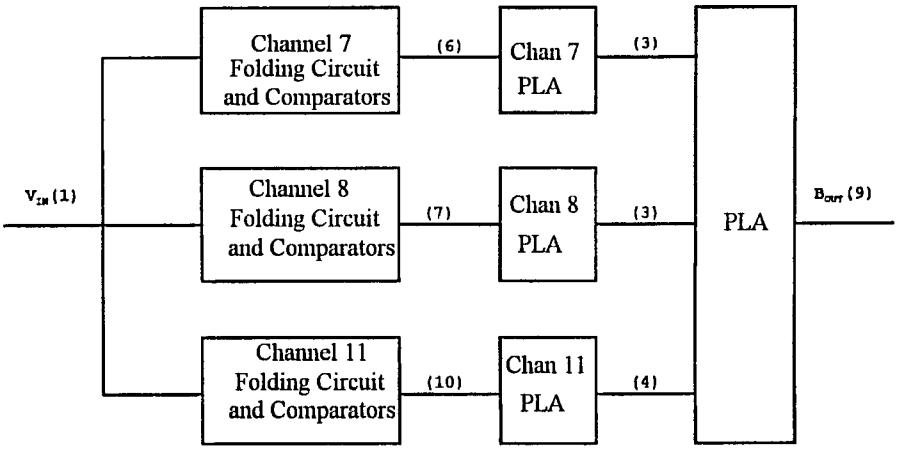


Figure 1. SNS 9-bit Folding ADC Block Diagram

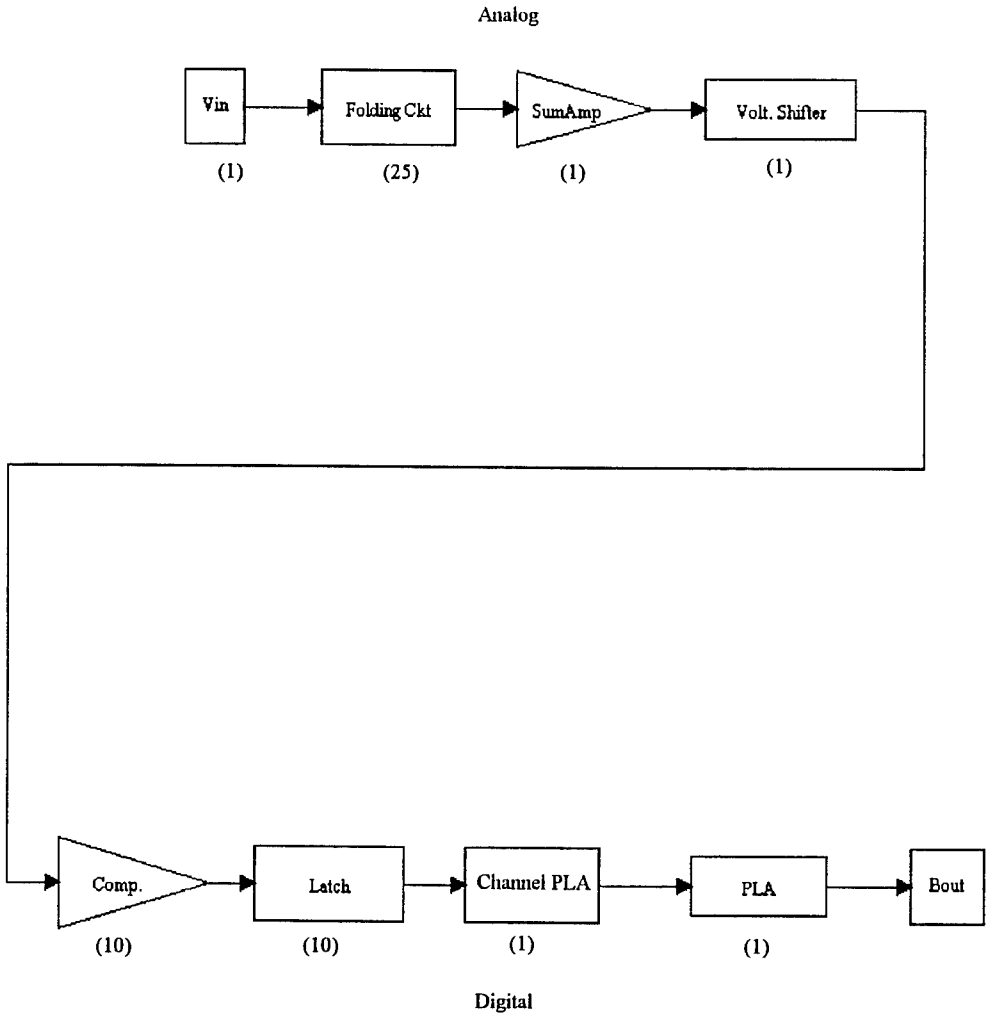


Figure 2. Channel 11 Functional Block Diagram

D. COMPUTER AIDED DESIGN AND SIMULATION TOOLS

1. Magic

All of the VLSI layouts completed for this thesis are accomplished using the CAD tool, Magic. Magic is an interactive editor used for the creation or modification of VLSI circuit layouts. It was developed by the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley. Using a color graphics display and a mouse, the designer can construct basic cell layouts and combine them hierarchically into larger integrated circuits. Magic contains a design rule checker that ensures compliance with layout rules for the particular technology being used. While editing, the design rule checker continuously monitors for design rule violations and creates a dotted pattern on areas that contain violations. Several commands are available to investigate these violations. Magic is based on the Mead-Conway style of design which advocates simple design rules and circuit layout. Only Manhattan designs are permitted, which contain vertical and horizontal edges. No diagonal or curved structures are allowed, which reduces the chip density by about 5-10%. As a means of interfacing with other design and simulation programs, Magic allows the designer to extract the developed layouts into the native language of other programs. This extraction tool has significant limitations for analog VLSI layout. Point-to-point resistance, gate capacitance, diffusion capacitance, and routing capacitance are extracted, but actual resistors or capacitors in the layout are not. Resistors and capacitors must be deleted from the layout before extraction and then manually added to the simulation file later. [Ref. 5]

2. Ext2spice

Ext2spice reads a file in the **.ext** format and creates a new file in the **.spice** format. The created file contains a list of transistors and capacitors. The designer must add the transistor model, in the form of Spice level 2 parameters, and other simulation information in order to produce an executable file in the spice format. Ext2spice assumes transistor model names of nfet and pfet. These names must agree with the Spice level 2 parameter names in the transistor model statement. Ext2spice assumes that ground is node 0, Vdd is node 1, and that node 2 is reserved as an error node. By labeling Vdd, Vdd!, and Ground, GND!, in the VLSI layout, the proper nodes will be assigned in the extraction. As noted above, all resistors, capacitors and any extraneous layout must be removed from the layout before extraction. If this is not accomplished, floating nodes are created which will cause the simulation to fail when run.

3. HSPICE

The industrial grade optimizing analog circuit analysis product HSPICE, from Meta-Software, is used for circuit simulations. It provides the ability to run simulations for electrical circuits in the steady-state, transient, and frequency domain. HSPICE incorporates superior convergence to similar SPICE variations. HSPICE is extremely versatile and provides high powered analysis of complex circuits. Several limitations had an impact on its use for this thesis. Due to the large number of transistors contained in the folding circuits, the processing times for the simulations were very long. Also, the site license for the use of HSPICE is limited to one Sun SPARCstation II. This created a

time-sharing problem when running multiple simulations. Waveform graphing of simulations is conducted using the Graphical Simulation Interface (GSI), packaged with HSPICE. GSI includes an interactive measurement facility and can manage analysis of results from one or many simulation runs. [Ref. 6]

III. ANALOG PREPROCESSING ARCHITECTURE

As shown in Figure 2, the analog preprocessing portion of the SNS 9-bit folding ADC is composed of a various number of folding stages, an operational amplifier connected in a summing configuration and a voltage shifter. Each channel (modulus m_i) used to produce the required dynamic range M contains these basic folding circuit components. The basic folding circuit design used in the original research for this architecture is used. This chapter will investigate each of the individual folding stages in the design and how they interconnect to form an entire folding circuit.

A. FOLDING STAGE

1. Differential Amplifier Pair

The primary component of the folding circuit is the individual folding stage. In order to produce the necessary folded waveform, a folding circuit is designed to take an analog input signal and fold it with the proper period to encode the signal in the optimum SNS format [Ref. 2]. In order to accomplish this, the folding stage shown in Figure 3 is used. The folding stage is composed of a pair of Metal-Oxide Semiconductor (MOS) differential amplifiers. An analog input signal V_{in} is applied to the base of M3, while a folding reference voltage V_{ref} is applied to the base of M4. Transistors M3 and M4 are biased by current source I2 and are in saturation. Transistors M5 and M6 are active loads. The drains of M3 and M4 are used to drive the bases of M1 and M2, respectively. Transistors M1 and M2 are biased by current source I1 and are also in saturation. The output V_{out} from the second differential amplifier pair is taken from the sources of M1 and

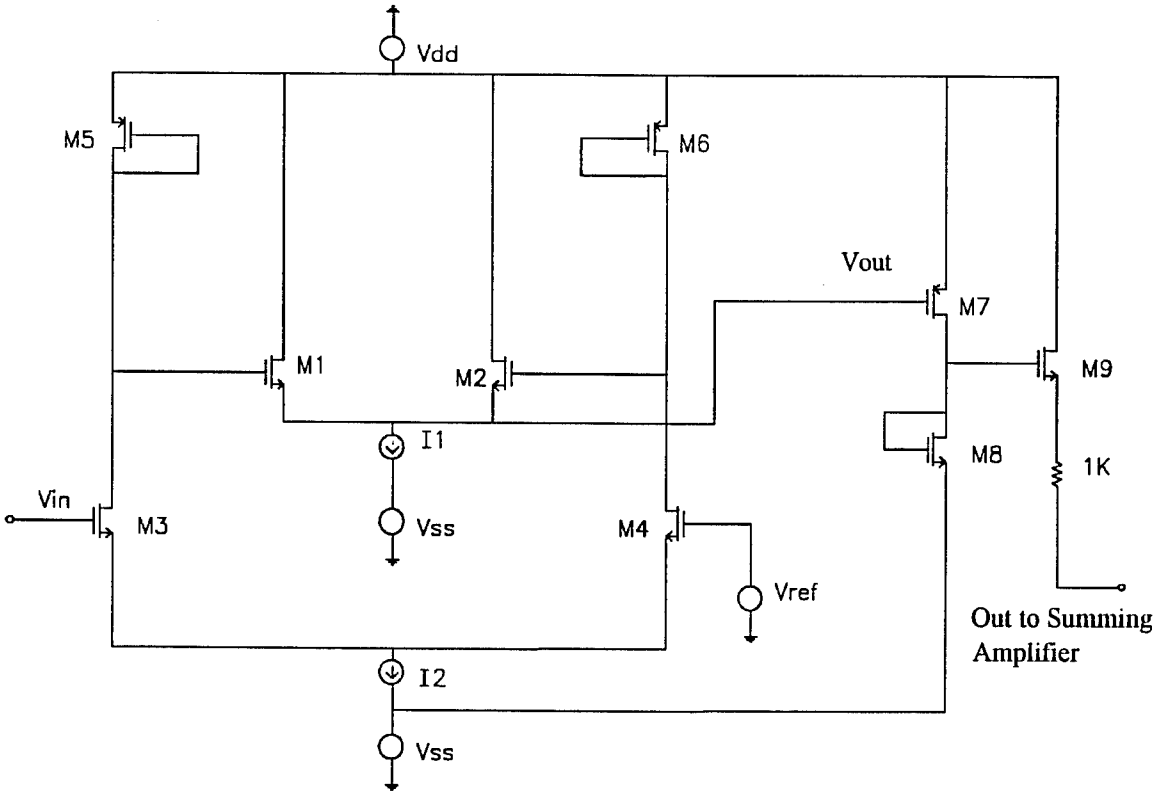


Figure 3. Folding Stage [After Ref. 2]

M2. This output is applied to the base of transistor M7 which provides some gain and dc voltage level shifting. Finally, an emitter follower M9 is used to ensure low output resistance of the folding stage. The 1 KΩ resistor is provided for the summing configuration of the operational amplifier for interconnecting the various folding stages together.

Transistors M3 and M4 provide a linear output symmetrical about V_{ref}. The higher of the base voltages to M1 and M2 is taken as the output V_{out}. Figure 4 provides a graphical representation of the circuit operation when V_{in} is ramped and a folding reference voltage V_{ref} of 0.64 volts is applied. Curve A represents the drain voltage from M3 that is applied to the base of M1. Curve B represents the drain voltage from M4 that is applied to the base of M2. The voltage waveform representing V_{out} measured at the sources of M1 and M2 is shown as curve C. Previous research and Spice simulation of the folding stage defines the power supplies at +18 and -18 volts respectively and the biasing currents I1 and I2 at 0.2 milliamps [Ref. 2].

2. Current Mirror

The original design of the folding stage used ideal current sources for I1 and I2 [Ref. 2]. In order to implement these current sources in a VLSI layout, a circuit is designed that allows layout using the 2μ CMOS N-well process. A cascode current mirror is chosen because of its excellent current accuracy and high output resistance [Ref. 7]. The cascode current mirror is so named because looking at the matched transistors that make up the circuit is much like looking into a mirror. The response of the circuit

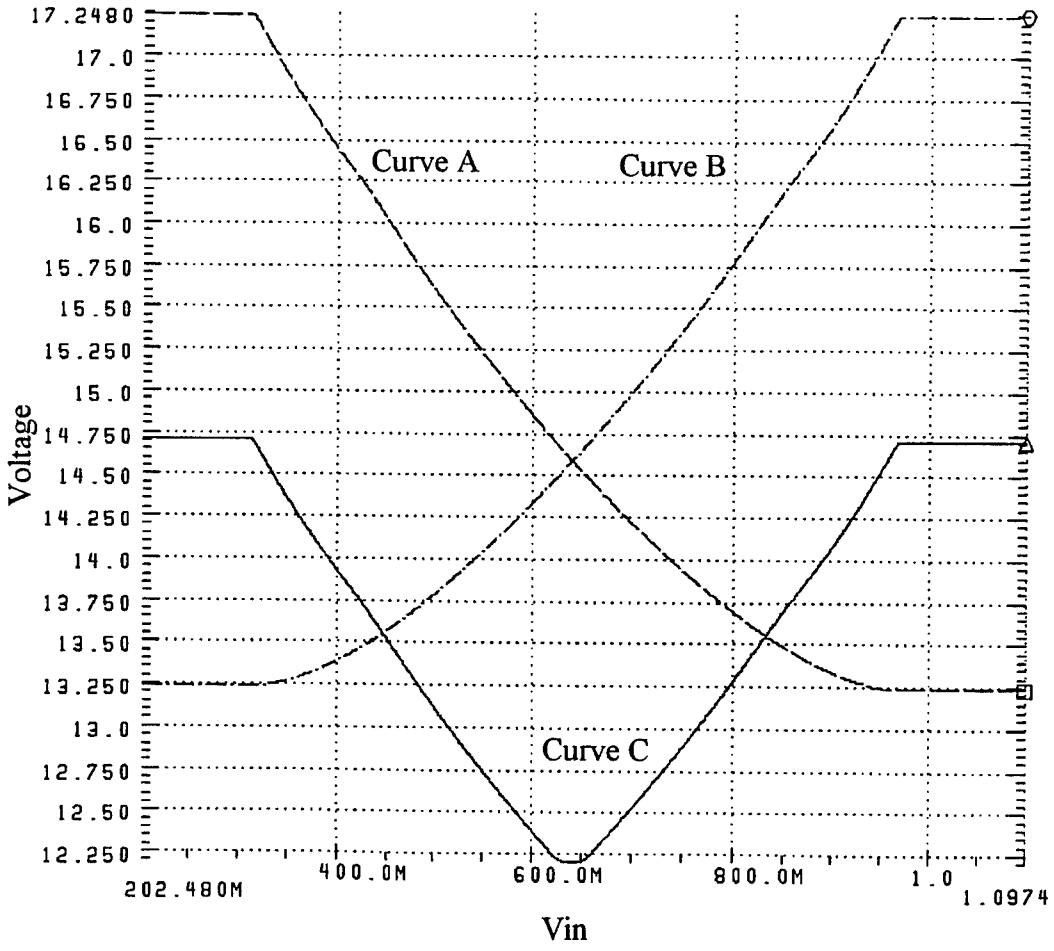


Figure 4. Folding Stage Transfer Curves

shown in Figure 5 can be expressed as

$$I_{out} = I_{ref} \frac{(W/L)_2}{(W/L)_1}, \tag{5}$$

where (W/L) is the gate width to length ratio for M1 and M2. During Spice simulations of the cascode current mirror, the current accuracy is increased over the range of operation of the folding stage by adding an extra pair of transistors to the basic design. The original VLSI layout uses individual cascode current mirrors for each current source, with power supplied by the individual folding stage. When it was determined that the current sources had to be capable of adjustment after fabrication of the VLSI chip, a *N*-output cascode current mirror was designed using power supplied from off-chip. In this case N corresponds to twice the number of folding stages in a particular channel. Figure 5 shows the final *N*-output cascode current mirror implemented in the folding stage design. Note that I_{ref} in Figure 5 is supplied from off-chip and that I_{ref} equals I_{out} for each of the *N*-outputs of the cascode current mirror.

B. SUMMING AMPLIFIER AND VOLTAGE SHIFTER

The folding stage previously defined describes a small portion of the dynamic range M of a SNS system. In order to describe the entire dynamic range M, a certain number of folding stages must be interconnected in parallel to form a folding circuit. In previous research, a significant loading problem was encountered when connecting the outputs of the folding stages together [Ref. 2]. It was concluded that since all of the

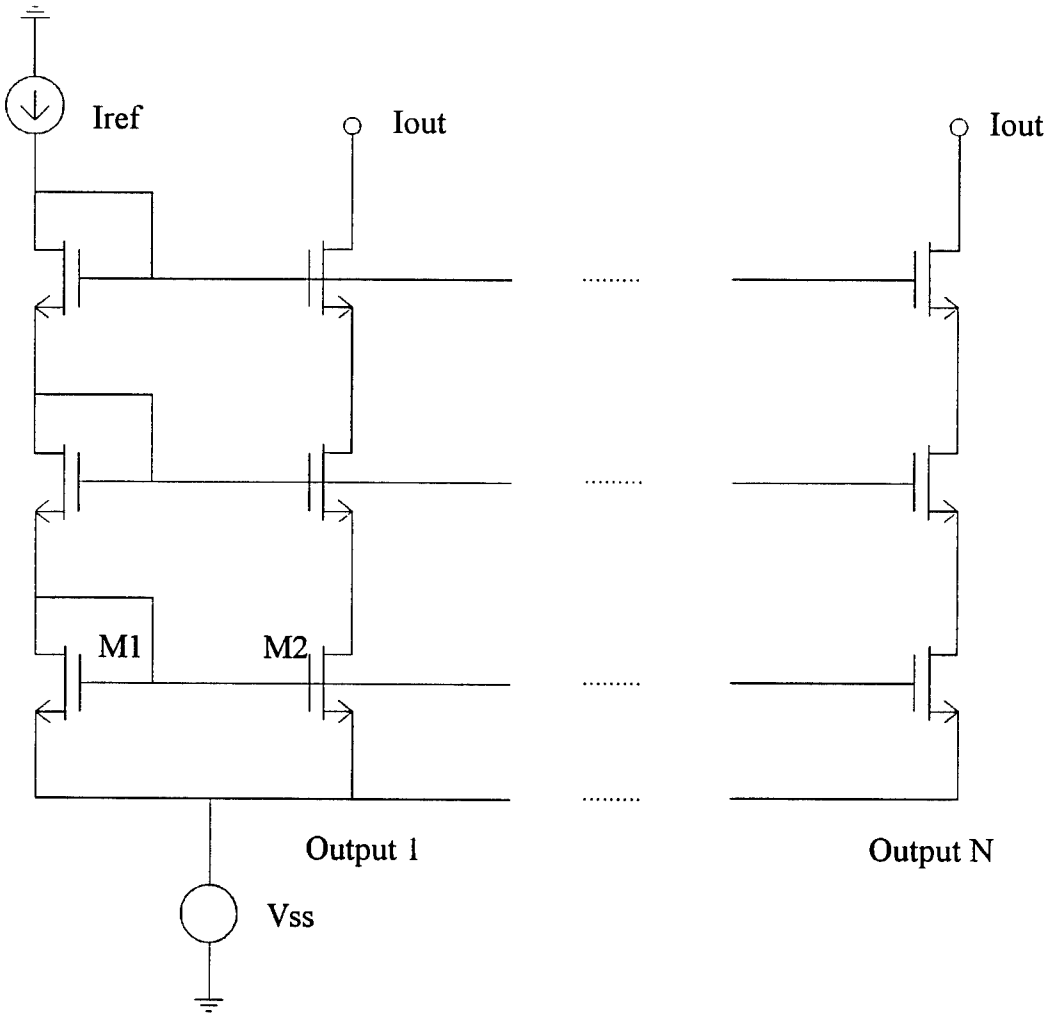


Figure 5. *N*-output Cascode Current Mirror

folding stages were connected at one node and that different voltage values were present at any instant at this node, no stable voltage value could be obtained. For this reason an operational amplifier connected in a summing configuration was added to the design. With the addition of the summing amplifier, each folding stage output is added uniformly to produce the entire waveform. Although subsequent testing revealed that some of the loading problem was still present, the summing amplifier was left in the design since it produced a better output. The operational amplifier chosen for the design is the CMOS two-stage operational amplifier connected in a summing configuration as shown in Figure 6 [Ref. 8]. Power supply, resistor and capacitor values used for the summing amplifier are listed in Table 2.

The value chosen for the feedback resistor R_f is based on providing a large enough gain to the folded waveform so that the matching voltages for the comparators at the output would be separated sufficiently to allow proper operation. This voltage gain can be calculated by

$$v_{out} = -\left(\frac{R_f}{1\ k\Omega} v_1 + \frac{R_f}{1\ k\Omega} v_2 + \ldots + \frac{R_f}{1\ k\Omega} v_N\right). \quad (6)$$

The values v_1 to v_N correspond to the voltages out of the N-different folding stages connected to the operational amplifier. The 1 kΩ resistors are located at the output of each of the folding stages as part of the summing configuration. A voltage shifter is added to the output of the operational amplifier in order to provide DC voltage level shifting

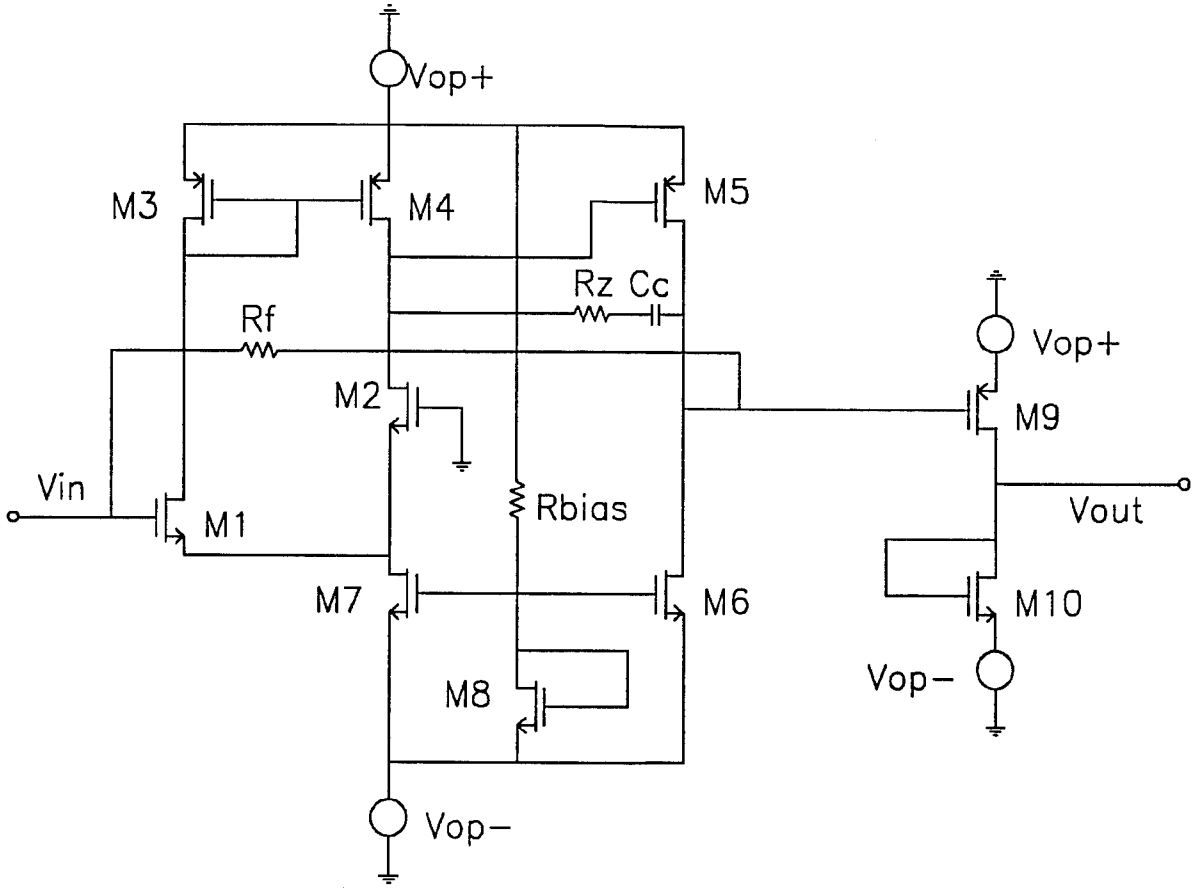


Figure 6. Summing Amplifier and Voltage Shifter

Vop+	+15 Volts
Vop-	-15 Volts
Rz	13 KΩ
Rbias	2 KΩ
Rf	20 KΩ
Cc	5 pF

Table 2. Summing Amplifier Parameter Values

capability. This maintains the voltage swing of the folded waveform from each channel so that the relative differences in the comparator matching voltages will be small across different channels. The voltage shifter follows the summing amplifier as shown in Figure 6. An example of the output of one folding stage connected to the summing amplifier and voltage shifter is shown in Figure 7.

C. FOLDING CIRCUIT

A single folding stage describes only a small portion of the dynamic range M of a SNS system. In order to describe the entire dynamic range M, a certain number of folding stages must be interconnected in parallel. Previous research defines the dynamic range of the SNS 9-bit folding ADC to be 15.0 volts [Ref. 2]. The fold width, or period of the folding waveform necessary to produce the proper SNS encoding for a channel (modulus

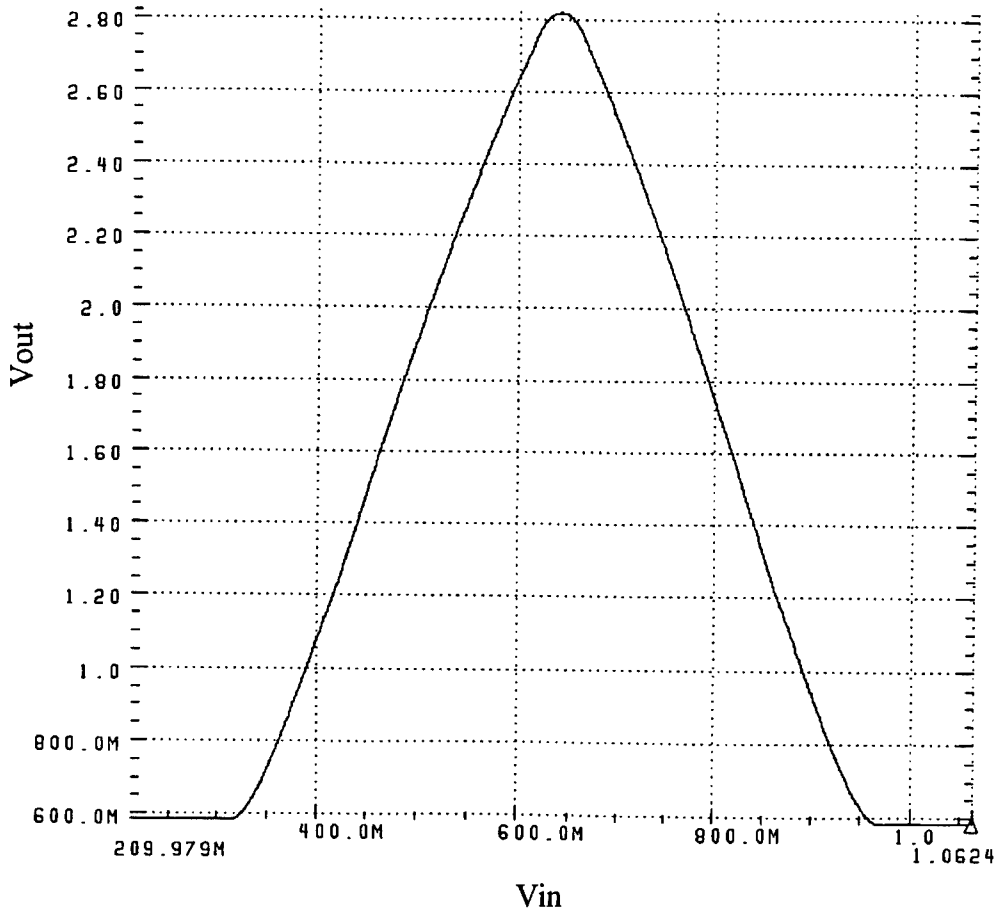


Figure 7. Example of a Folding Circuit Output

m_i) can be described by the equation

$$V_{width} = \frac{2m_i V}{M} \tag{7}$$

[Ref. 2]. Using Equation 7, the fold width for each of the SNS 9-bit folding ADC channels is

$$V_{width_7} = \frac{(2)(7)(15\,V)}{512} = 0.41\,V \tag{8}$$

$$V_{width_8} = \frac{(2)(8)(15\,V)}{512} = 0.47\,V \tag{9}$$

$$V_{width_{11}} = \frac{(2)(11)(15\,V)}{512} = 0.64\,V. \tag{10}$$

Based on these results, the number of folding stages necessary to cover the dynamic range is determined. Table 3 lists the required number of folding stages necessary for each channel.

Folding reference voltages V_{ref} for each of the folding stages are determined based on the calculated V_{width}. Tables 4 through 6 list the required folding reference voltages V_{ref} for each folding circuit. A voltage ladder is used to provide the proper folding reference voltage for each folding stage. Figure 8 shows a generic folding circuit with all folding stage outputs interconnected to the summing amplifier. A complete waveform for the

Channel	Folding Stages Required
7	38
8	33
11	25

Table 3. Number of Folding Stages Required for Each Channel

entire dynamic range of the channel 11 folding circuit is presented in Figure 9. This plot demonstrates the performance of the folding circuit design.

Folding Stage	Folding Reference Voltage V_{ref}
1	0
2	0.41
3	0.82
4	1.23
5	1.64
6	2.05
7	2.46
8	2.87
9	3.28
10	3.69
11	4.1
12	4.51
13	4.92
14	5.33
15	5.74
16	6.15
17	6.56
18	6.97
19	7.38

Folding Stage	Folding Reference Voltage V_{ref}
20	7.79
21	8.2
22	8.61
23	9.02
24	9.43
25	9.84
26	10.25
27	10.66
28	11.07
29	11.48
30	11.89
31	12.3
32	12.71
33	13.12
34	13.53
35	13.94
36	14.35
37	14.76
38	15.17

Table 4. Channel 7 Folding Reference Voltages

Folding Stage	Folding Reference Voltage V_{ref}
1	0
2	0.47
3	0.94
4	1.41
5	1.88
6	2.35
7	2.82
8	3.29
9	3.76
10	4.23
11	4.7
12	5.17
13	5.64
14	6.11
15	6.58
16	7.05
17	7.52

Folding Stage	Folding Reference Voltage V_{ref}
18	7.99
19	8.46
20	8.93
21	9.4
22	9.87
23	10.34
24	10.81
25	11.28
26	11.75
27	12.22
28	12.69
29	13.16
30	13.63
31	14.1
32	14.57
33	15.04

Table 5. Channel 8 Folding Reference Voltages

Folding Stage	Folding Reference Voltage V_{ref}
1	0
2	0.64
3	1.28
4	1.92
5	2.56
6	3.2
7	3.84
8	4.48
9	5.12
10	5.76
11	6.4
12	7.04
13	7.68

Folding Stage	Folding Reference Voltage V_{ref}
14	8.32
15	8.96
16	9.6
17	10.24
18	10.88
19	11.52
20	12.16
21	12.8
22	13.44
23	14.08
24	14.72
25	15.36

Table 6. Channel 11 Folding Reference Voltages

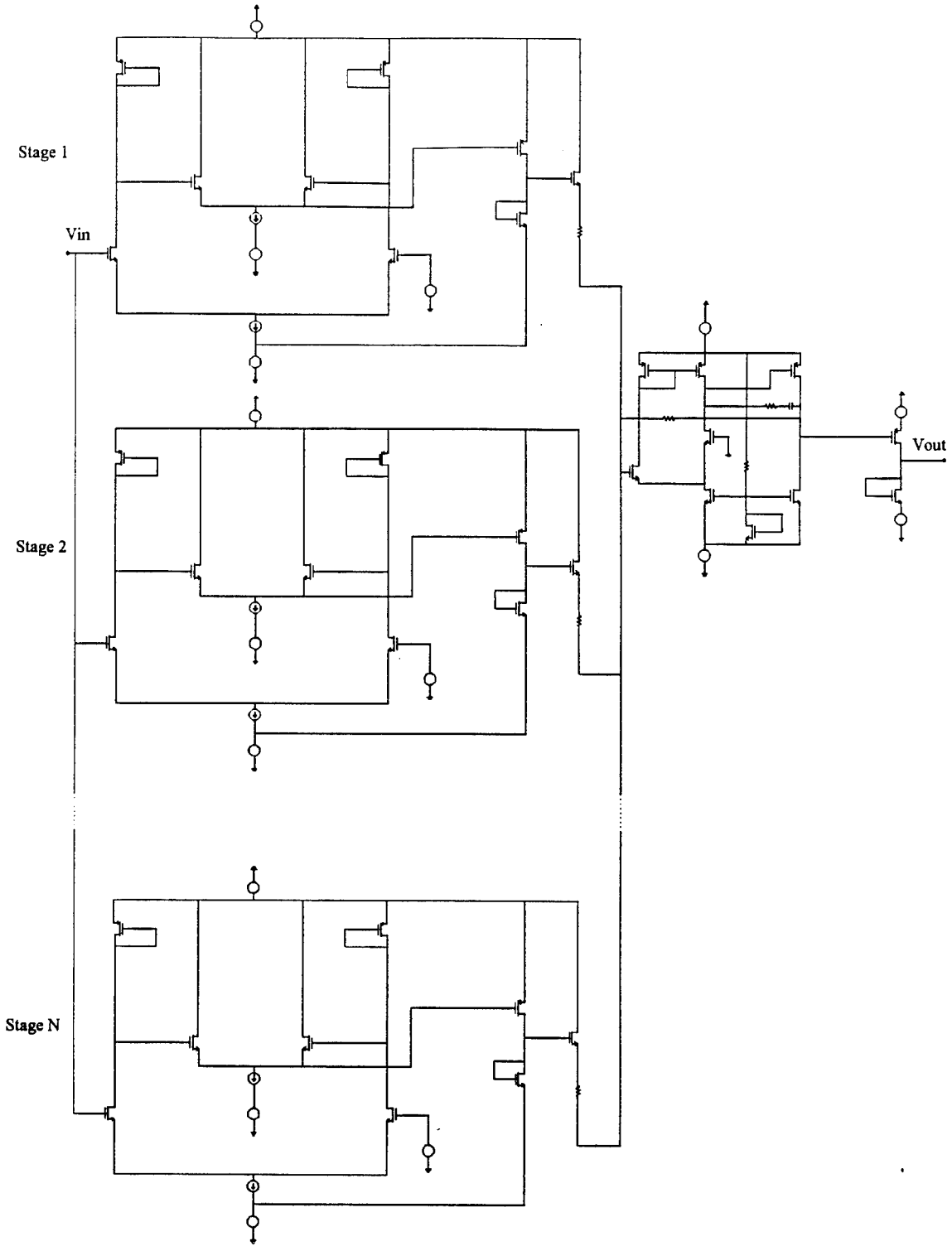


Figure 8. Generic Folding Circuit

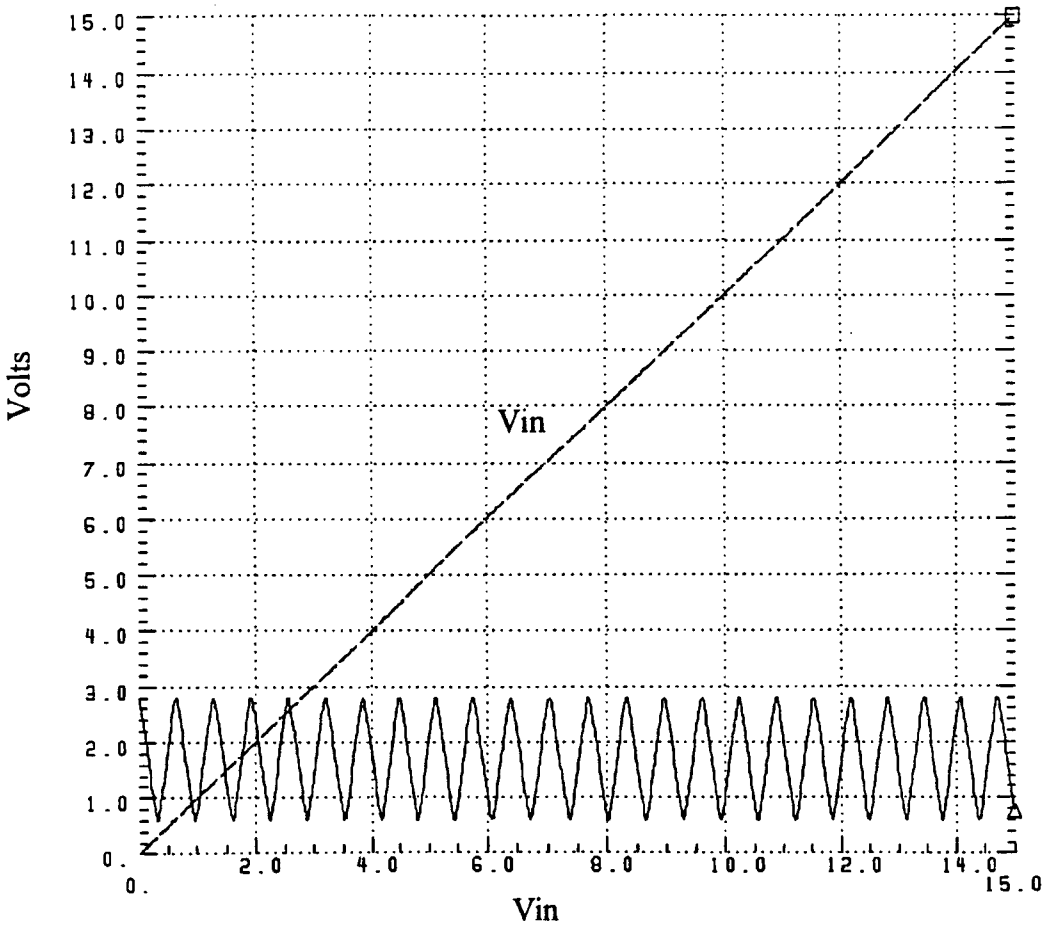


Figure 9. Channel 11 Folding Circuit Output

IV. IMPLEMENTATION

Once the folding circuits were defined for the three channels, the layout was accomplished using Magic. Design rules for the 2μ CMOS N-well technology were used to verify correct layout of the circuits. The discussion of the layout of the circuits follows the same outline as Chapter III. Each individual folding stage is examined and then a representative folding circuit is shown. An example nfet CMOS transistor layout is shown in Figure 10. Basic transistor features, gate length, gate width, dimensions and CMOS layer representations are labeled.

A. FOLDING STAGE

Close examination of the original simulation files for the folding stages for each channel reveal that all transistors but the lower differential pair are of the same gate width and length [Ref. 2]. Referring to Figure 3, the lower differential pair of transistors are M3 and M4. This allows the creation of a basic cell incorporating all of the transistors of the folding stage except for M3 and M4. This basic cell is then copied as necessary to obtain the proper number of folding stages in each of three folding circuits. Using the Magic command **:getcell**, individual M3 and M4 transistors, designed for each folding stage, are brought into each of the replicated basic cells. This method reduces the layout time significantly and ensures consistency in the layout.

As in most analog VLSI designs, many of the transistors in the folding stage are very large. Transistor gate widths up to 330 microns are used to obtain the proper folding characteristics. All transistors with gate widths in excess of 75 microns are constructed as

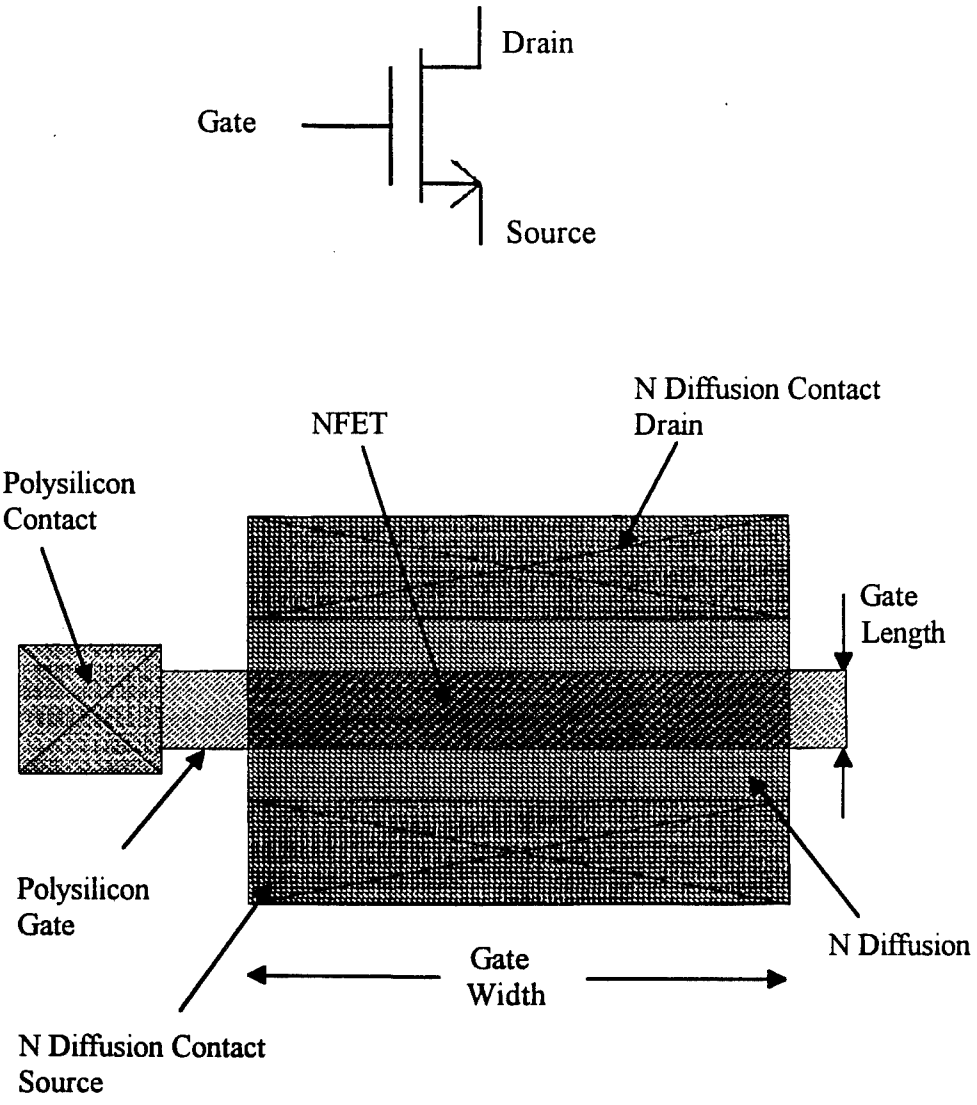


Figure 10. Example CMOS Transistor Layout

multi-fingered transistors using parallel gates with widths less than 75 microns. Two metal layers are used in the design with metal one used for vertical interconnects and metal two used for horizontal interconnects. The minimum size width for the power and ground conductors is chosen such that the current density of the particular conductor will not exceed the current limit for either metal one or metal two. Exceeding the current limit can cause electromigration, which is the migration of metal ions in the conductor away from the high current density. Electromigration can eventually cause an opening in the conductor rendering the circuit useless. Spice simulation results from the original design files are used for determining the minimum widths. A current limit of 0.6 milliamps per micron of width for metal one and 1.15 milliamps per micron of width for metal two is used. Another consideration in determining the minimum size width for the power and ground conductors is the voltage drop from the power and ground input pads to the circuit. In order for the circuit to operate properly, the correct voltages must be available at the circuit. Voltage drops for the power and ground conductors were calculated and determined to be insignificant. As stated earlier, the folding reference voltages V_{ref} supplied to each folding stage are developed in a resistor ladder network using the +18 volt power supply. Resistor values are chosen to produce the required folding reference voltage at each stage. These resistors are designed in the layout using p^+ diffusion with a sheet resistance of 40 ohms per square. By multiplying the sheet resistance times the length-to-width ratio of the p^+ diffusion area, a value for the resistance is obtained.

Substrate contacts are used extensively throughout the layout in order to ensure that the substrate-well junction remained reversed biased, thus preventing latchup.

Figure 11 shows the basic floor plan of a generic folding stage. It denotes the location of each of the transistors in the CMOS implementation of the circuit. The labeling of the transistors matches that of Figure 3. Figures 12 through 17 contain the individual transistor circuit level diagrams of the folding stage and their respective CMOS implementations. The final working layout of the entire folding stage is shown in Figure 18. Tables 8 through 11 in Appendix A contain a complete listing of gate dimensions of all transistors used in the folding stages.

As previously addressed in Chapter III, an *N*-output cascode current mirror is used to provide the biasing current to the folding stages. Figure 19 represents the CMOS implementation of one output stage of the current mirror. All transistors making up the current mirror have gate length equal to 2 microns and gate width equal to 3 microns.

B. SUMMING AMPLIFIER AND VOLTAGE SHIFTER

The floor plan used for the layout of the summing amplifier is shown in Figure 20. The CMOS implementations of the summing amplifier and voltage shifter described in Chapter III are shown in Figure 21 and Figure 22. Component labeling coincides with that presented in Figure 6. The summing amplifier and voltage shifter are the same for each of the three folding circuits in the design. Resistors are implemented in the layout using p^+ diffusion with a sheet resistance of 40 ohms per square in the same manner as with the folding stage. In order to reduce the area of resistors R_f and R_z, a zig zag pattern

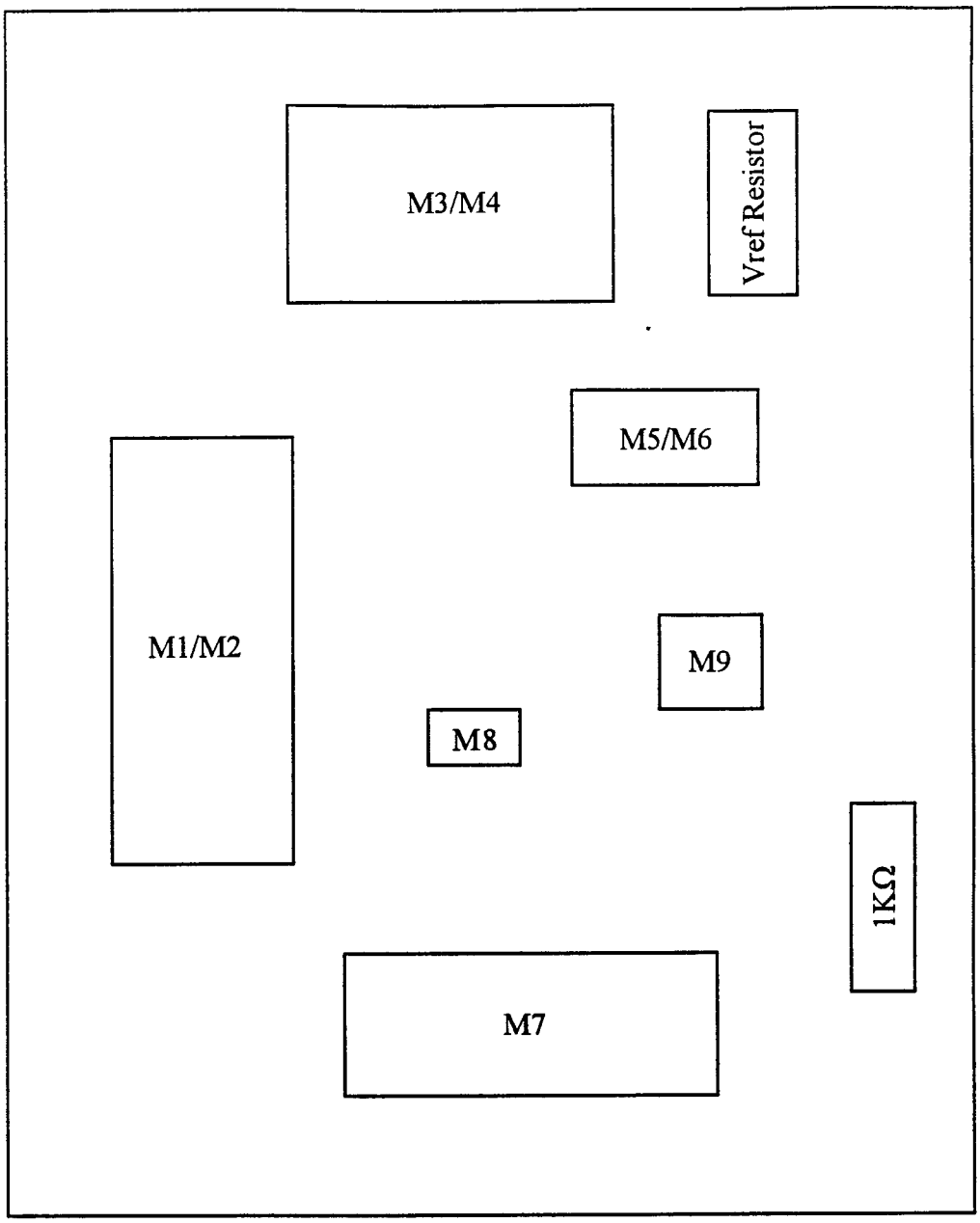
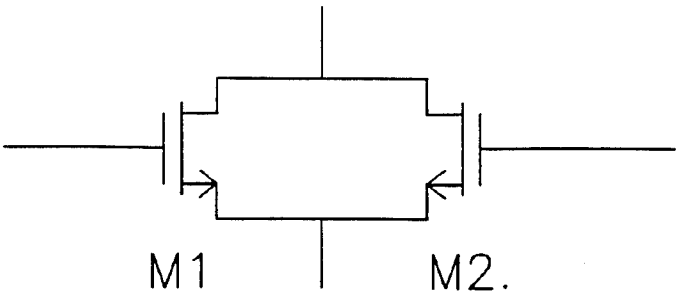


Figure 11. Folding Stage Floor Plan



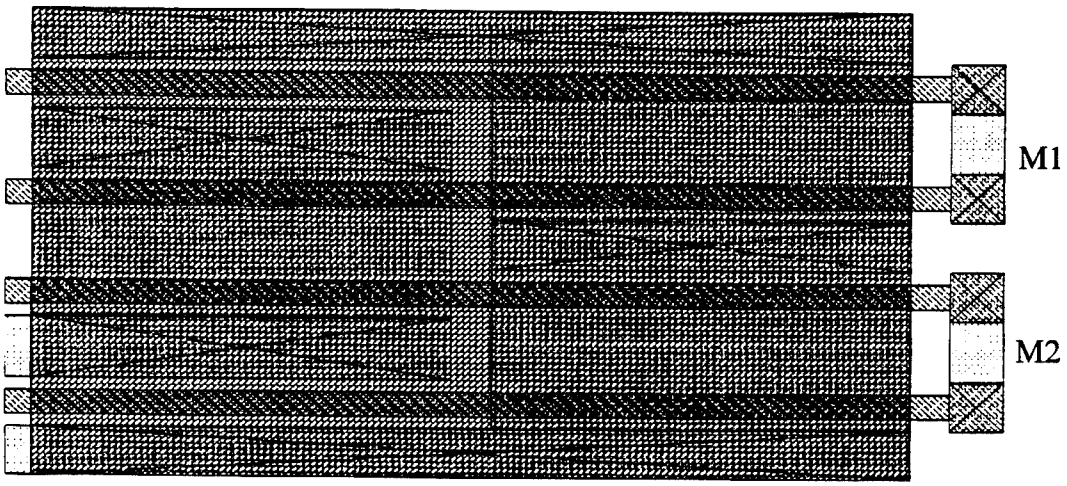
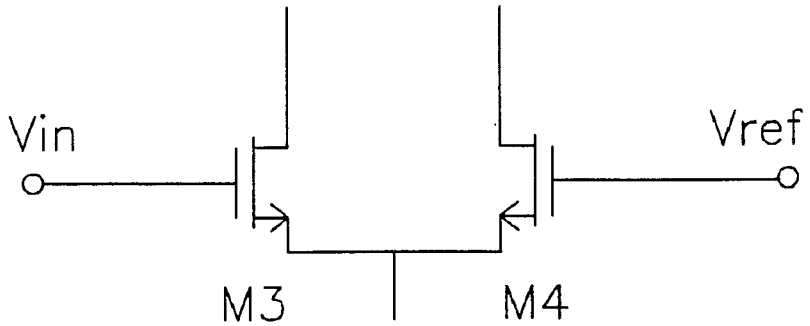


Figure 12. M1/M2 CMOS Layout



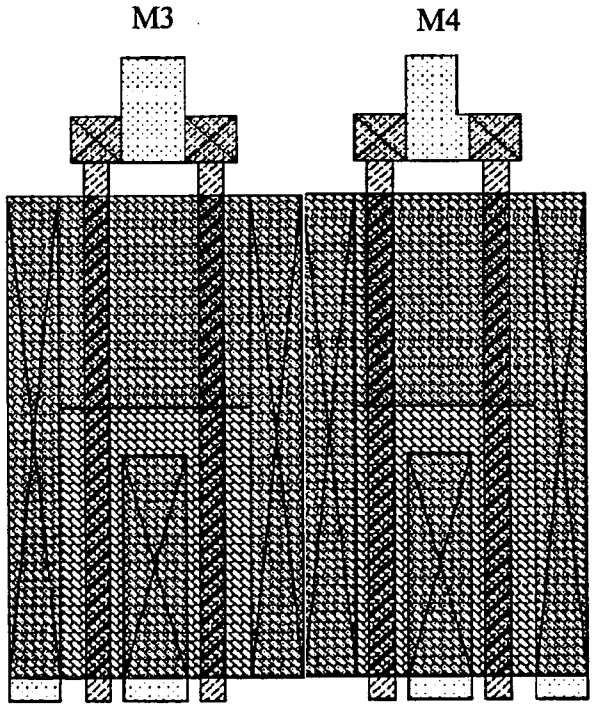


Figure 13. M3/M4 CMOS Layout

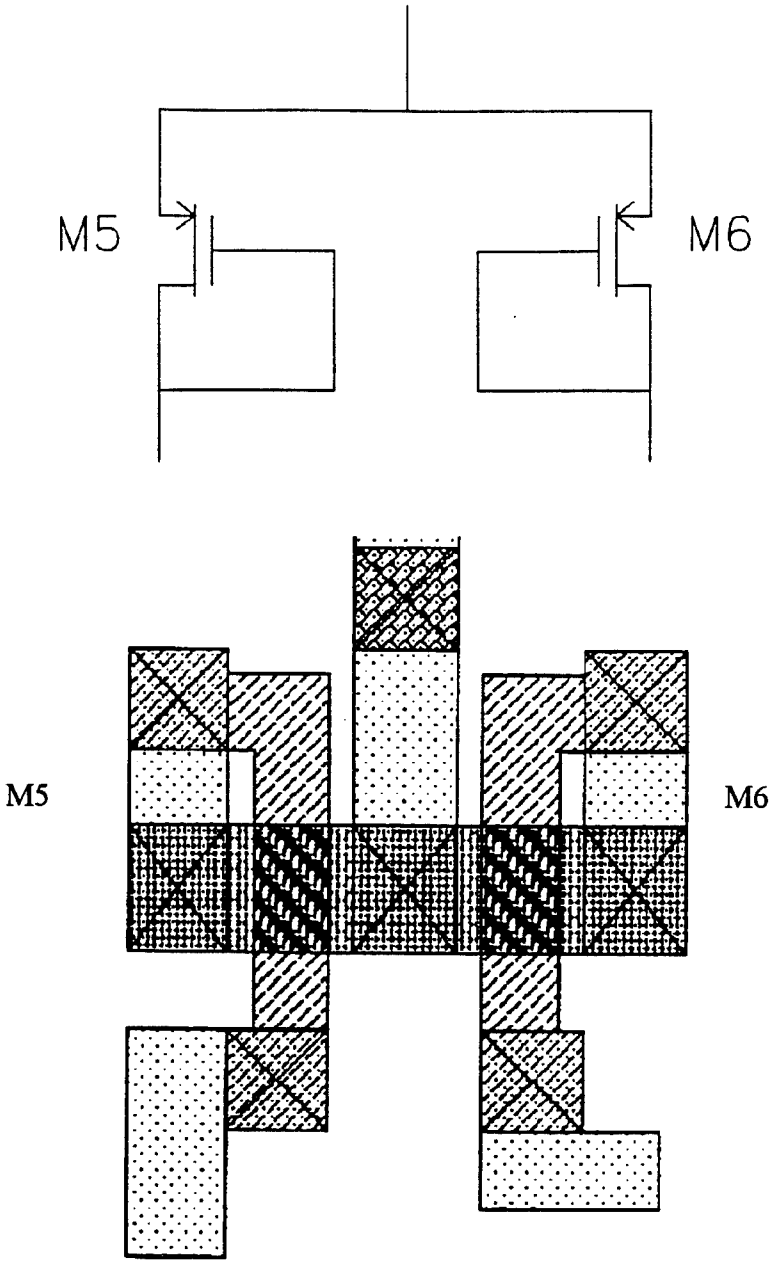
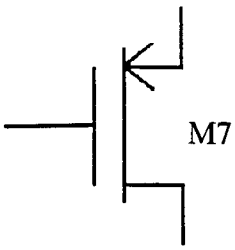


Figure 14. M5/M6 CMOS Layout



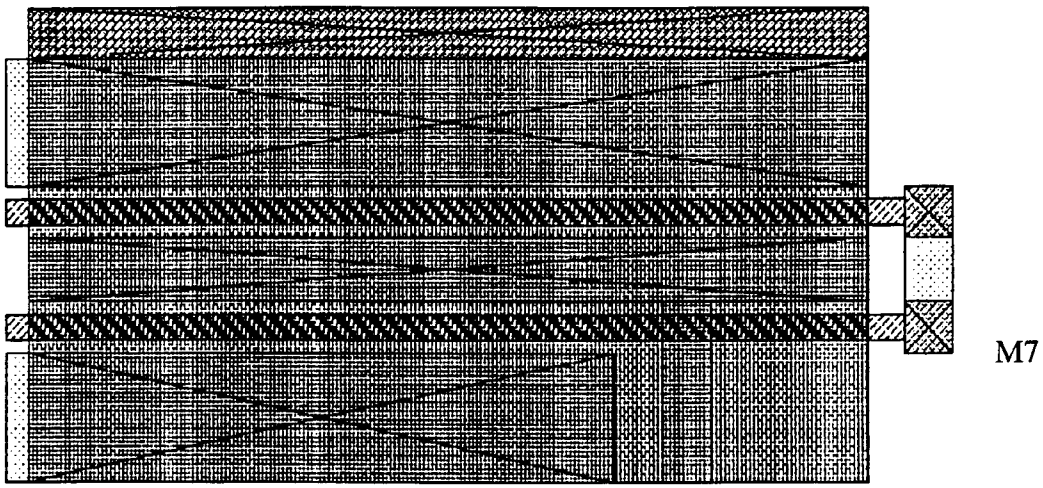
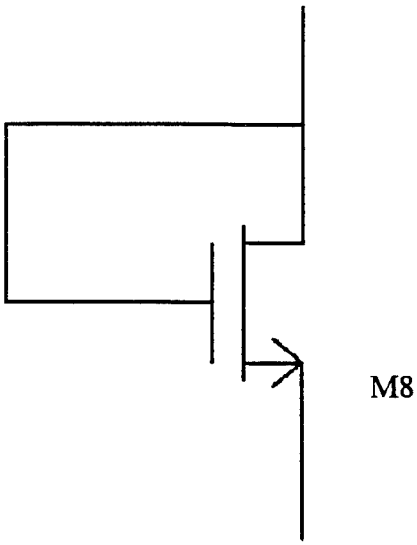


Figure 15. M7 CMOS Layout



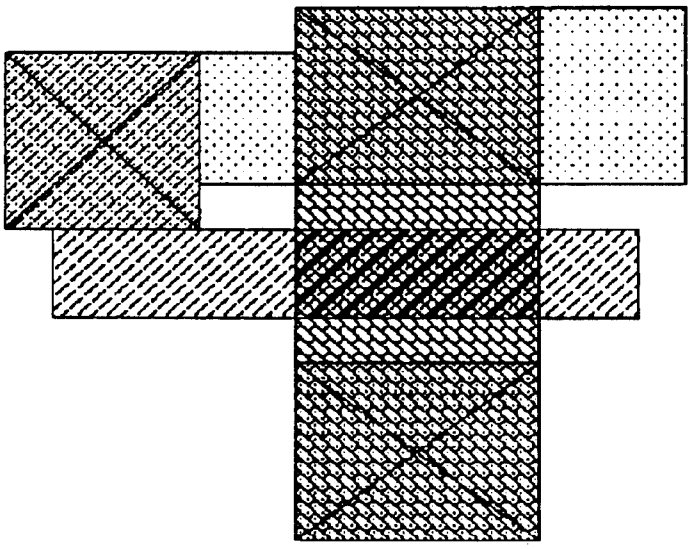
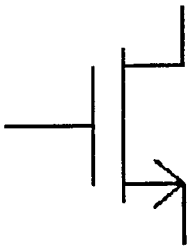
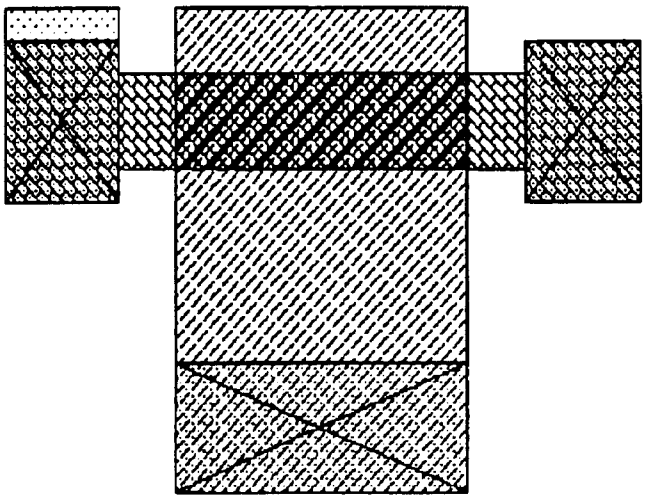


Figure 16. M8 CMOS Layout



M9



M9

Figure 17. M9 CMOS Layout

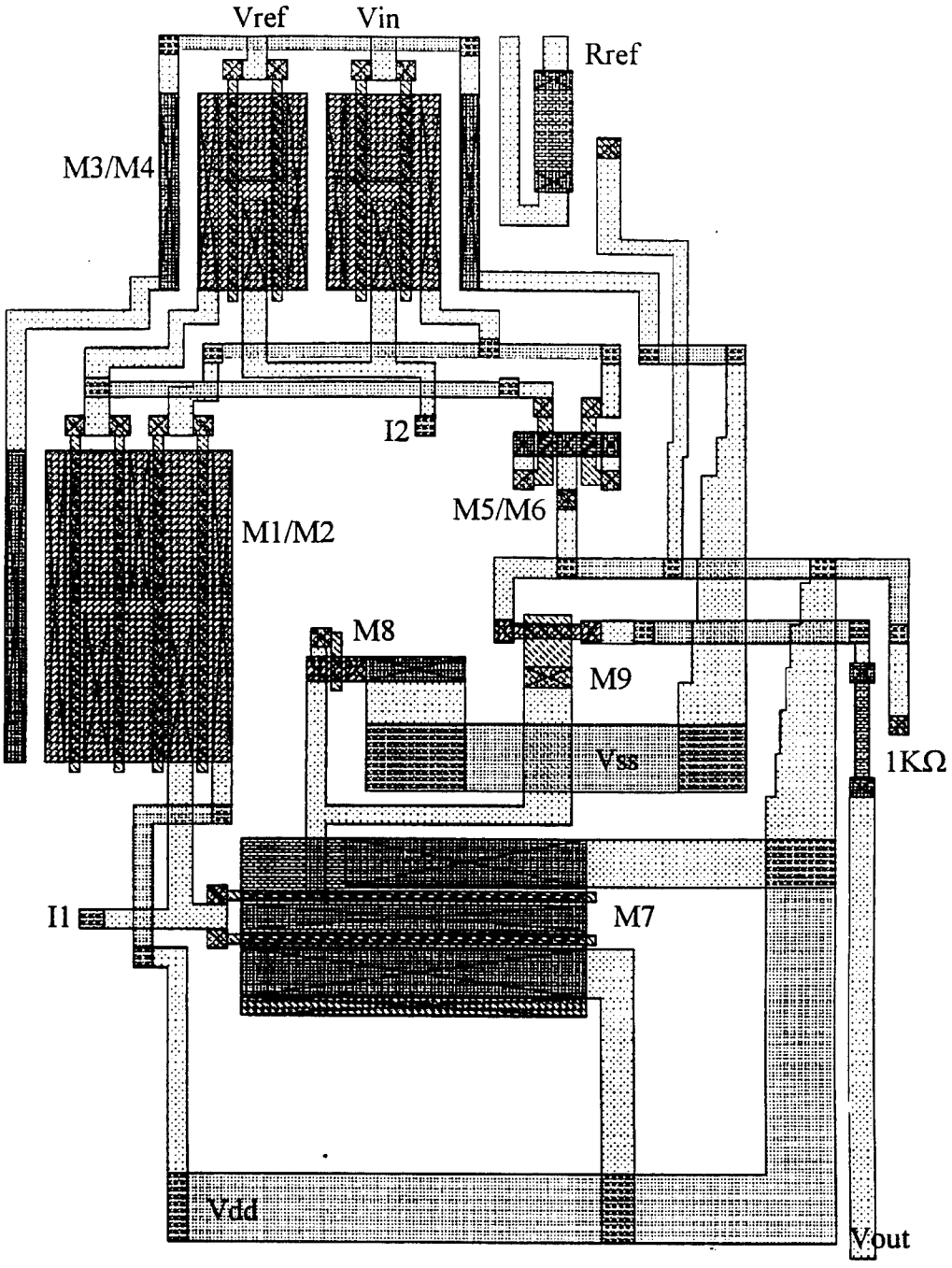


Figure 18. Folding Stage CMOS Layout

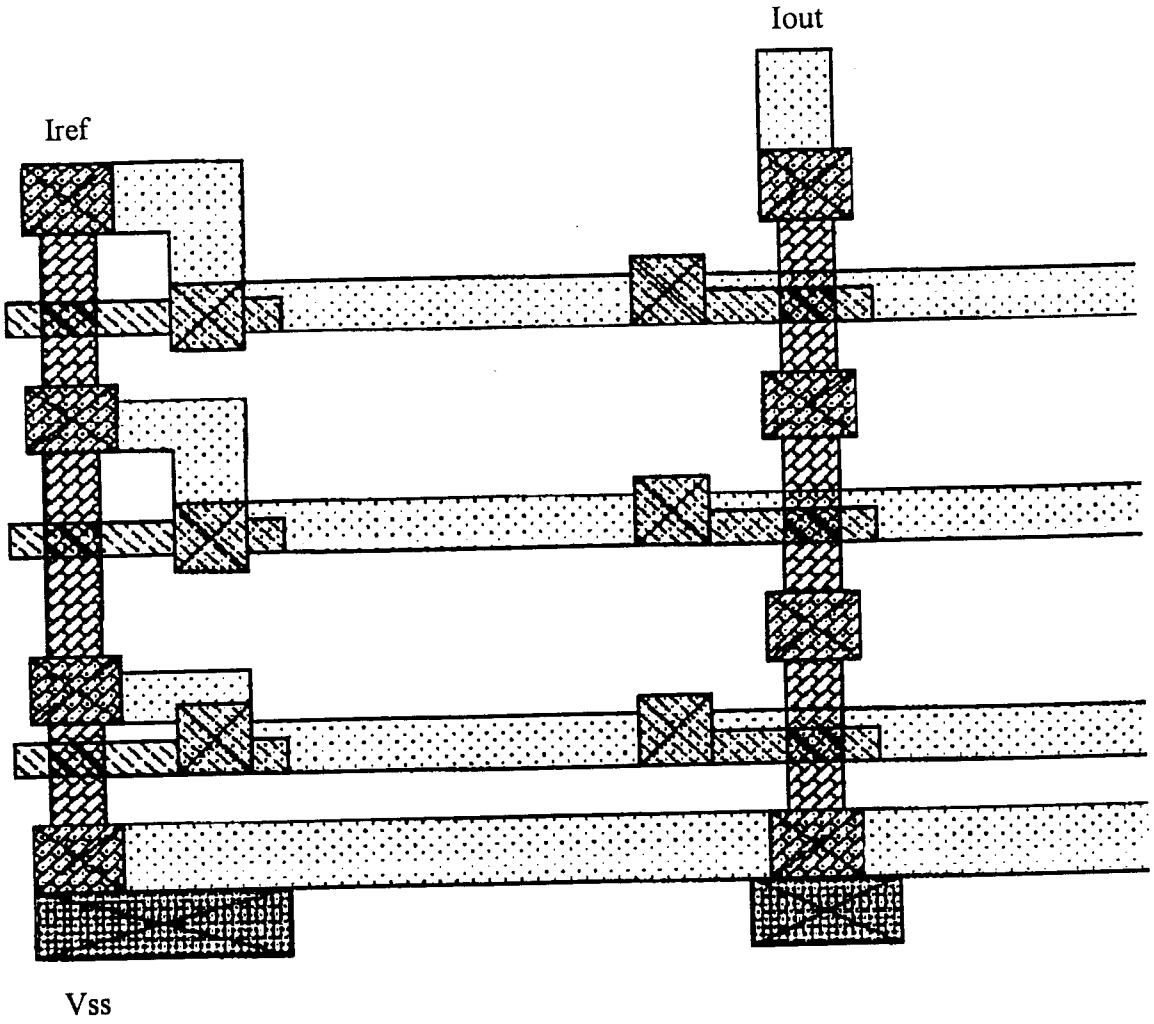


Figure 19. Current Mirror CMOS Layout

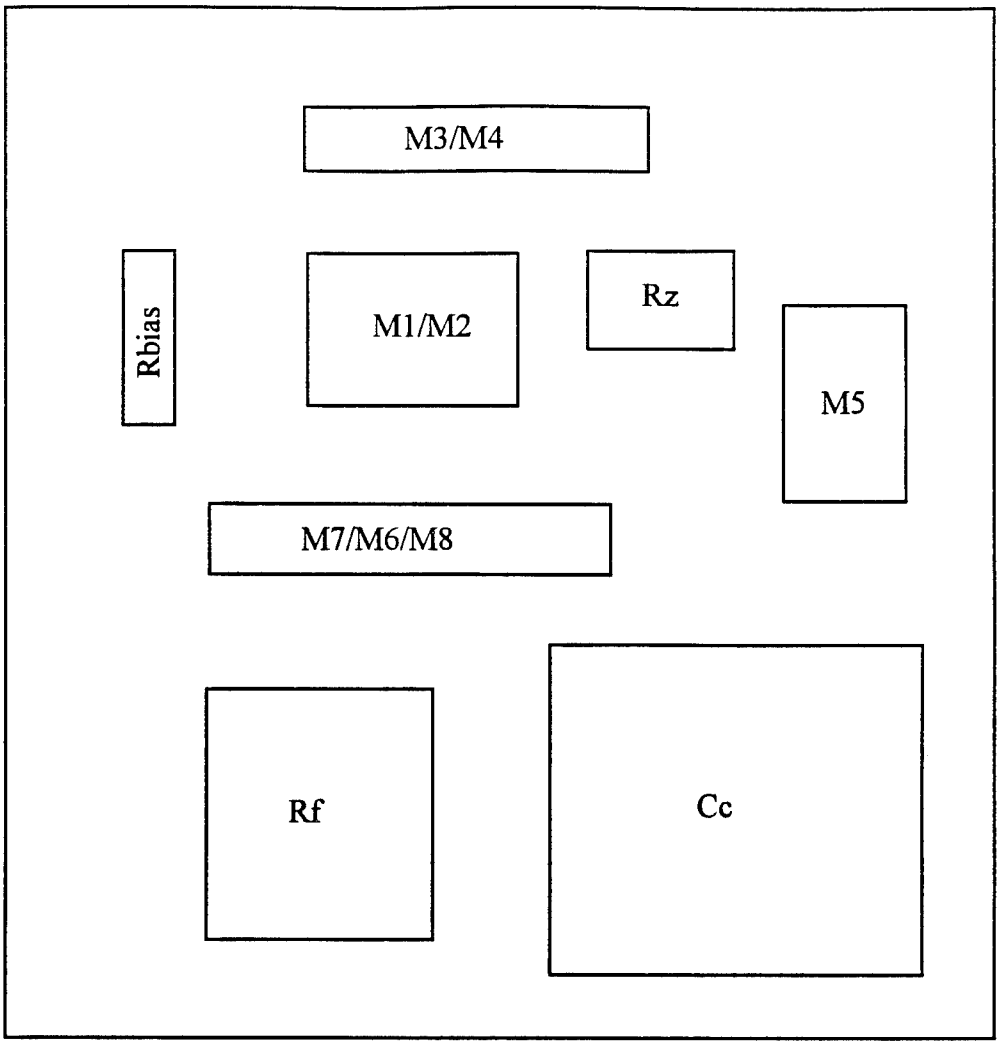


Figure 20. Summing Amplifier Floor Plan

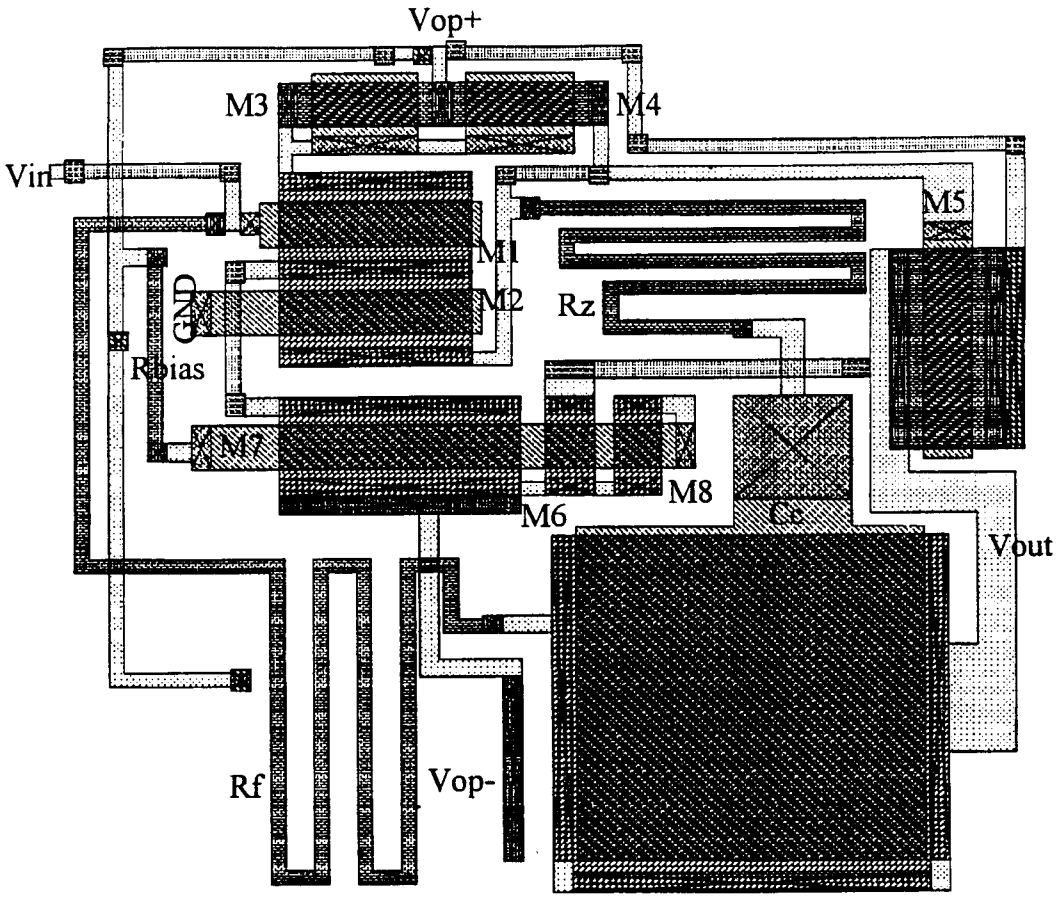


Figure 21. Summing Amplifier CMOS Layout

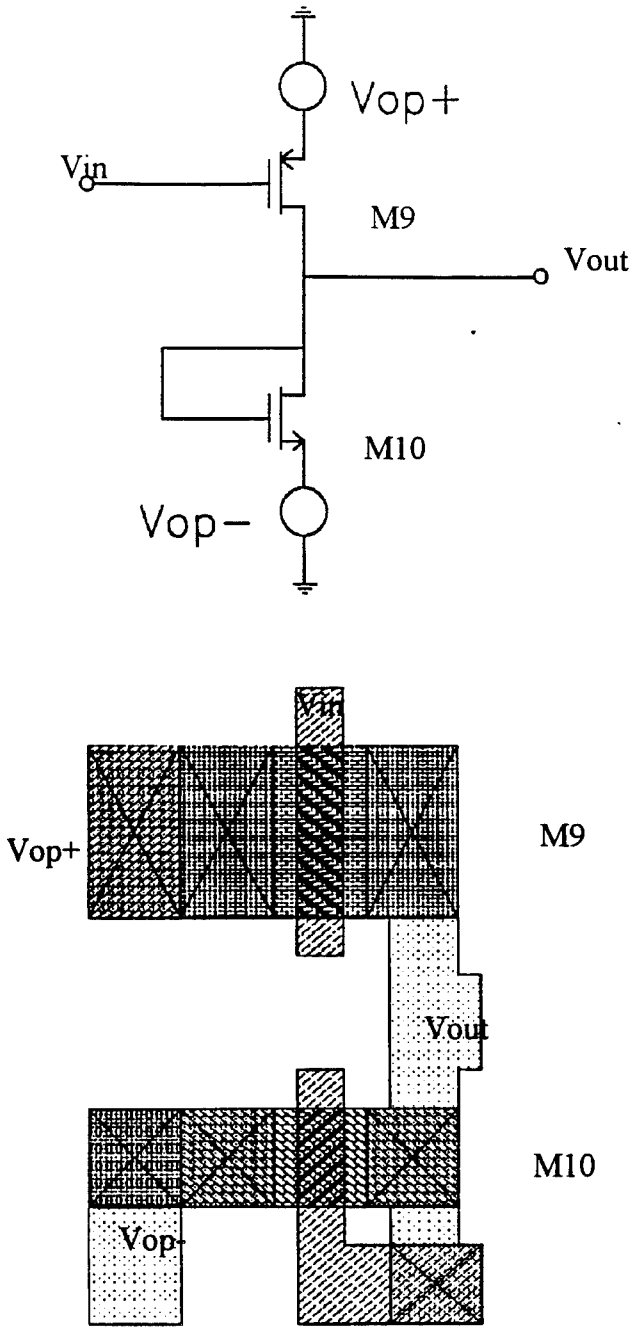


Figure 22. Voltage Shifter CMOS Layout

is used. When using this type of pattern, care must be taken when estimating the resistance. By breaking the pattern up into simple regions, resistance values of commonly encountered shapes are used. In the case of a zig zag pattern, this commonly encountered shape is a corner. A value of resistance for each corner is found to be equal to 2.5 times the sheet resistance using resistance values for nonrectangular shapes. By adding the resistance of the rectangular portions of the p^+ diffusion area to the resistance at the corners, the total resistance is obtained.

Of particular note is the amount of area that the capacitor Cc requires. The capacitor is constructed of polysilicon over n^+ diffusion. This arrangement produces a plate capacitance of 90×10^{-5} picofarads per micron^2. For the 5 picofarad capacitor required in the design, a chip area of approximately 5555 micron^2 (75x75 microns) is used. Table 12 in Appendix A contains a complete listing of gate dimensions of all transistors in the summing amplifier and voltage shifter.

C. FOLDING CIRCUIT

Implementing the entire folding circuit is accomplished in a hierarchical layered manner. A basic cell is created into which the individual folding stages for a particular channel are added by using the Magic command **:getcell**. The summing amplifier and voltage shifter are added in a similar manner. Figure 23 is the floor plan for the layout of the channel 11 folding circuit. The major goal in the layout is the minimization of the chip area used (compact design). Figure 24 is the CMOS implementation of this circuit.

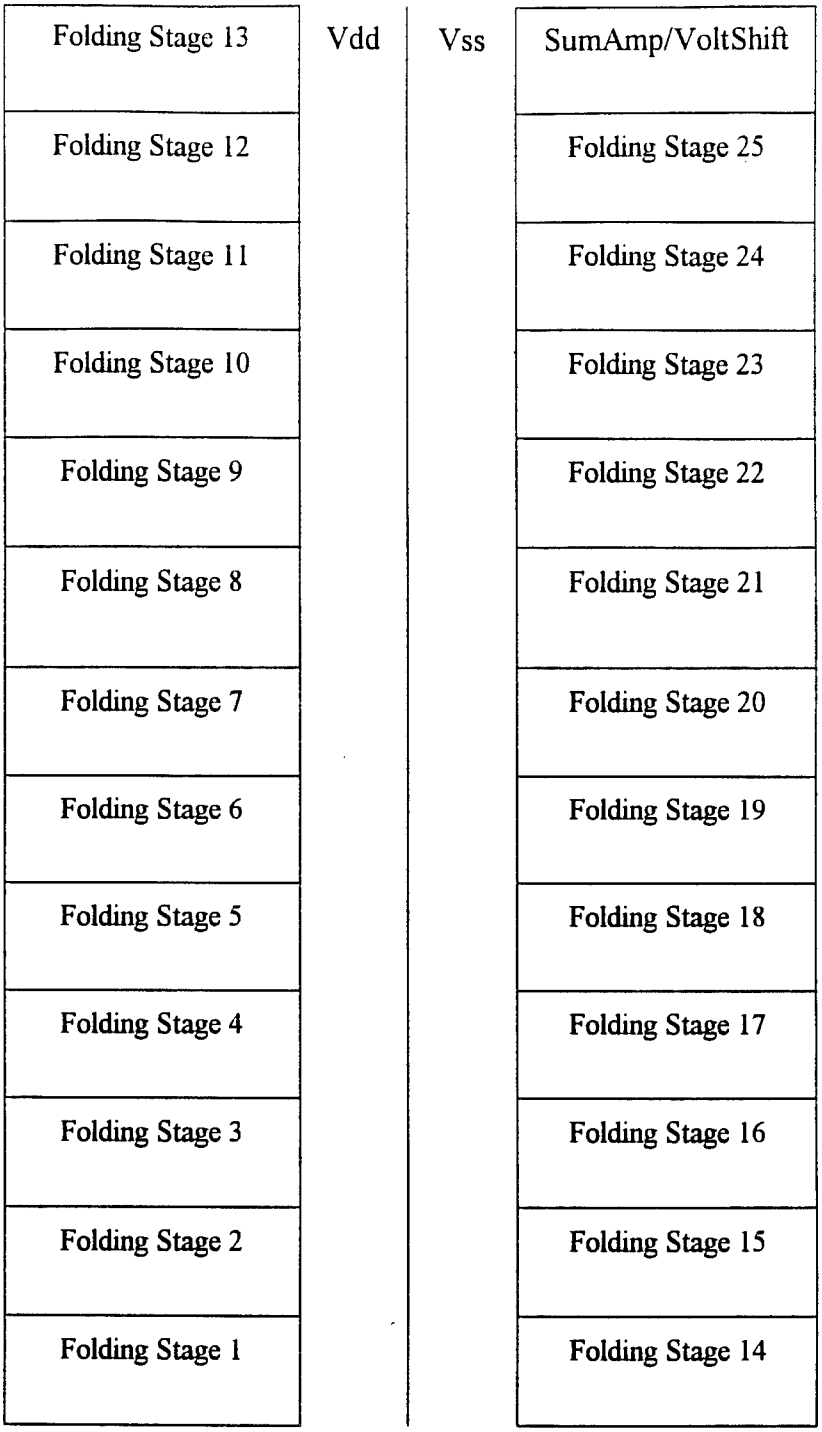


Figure 23. Channel 11 Folding Circuit Floor Plan

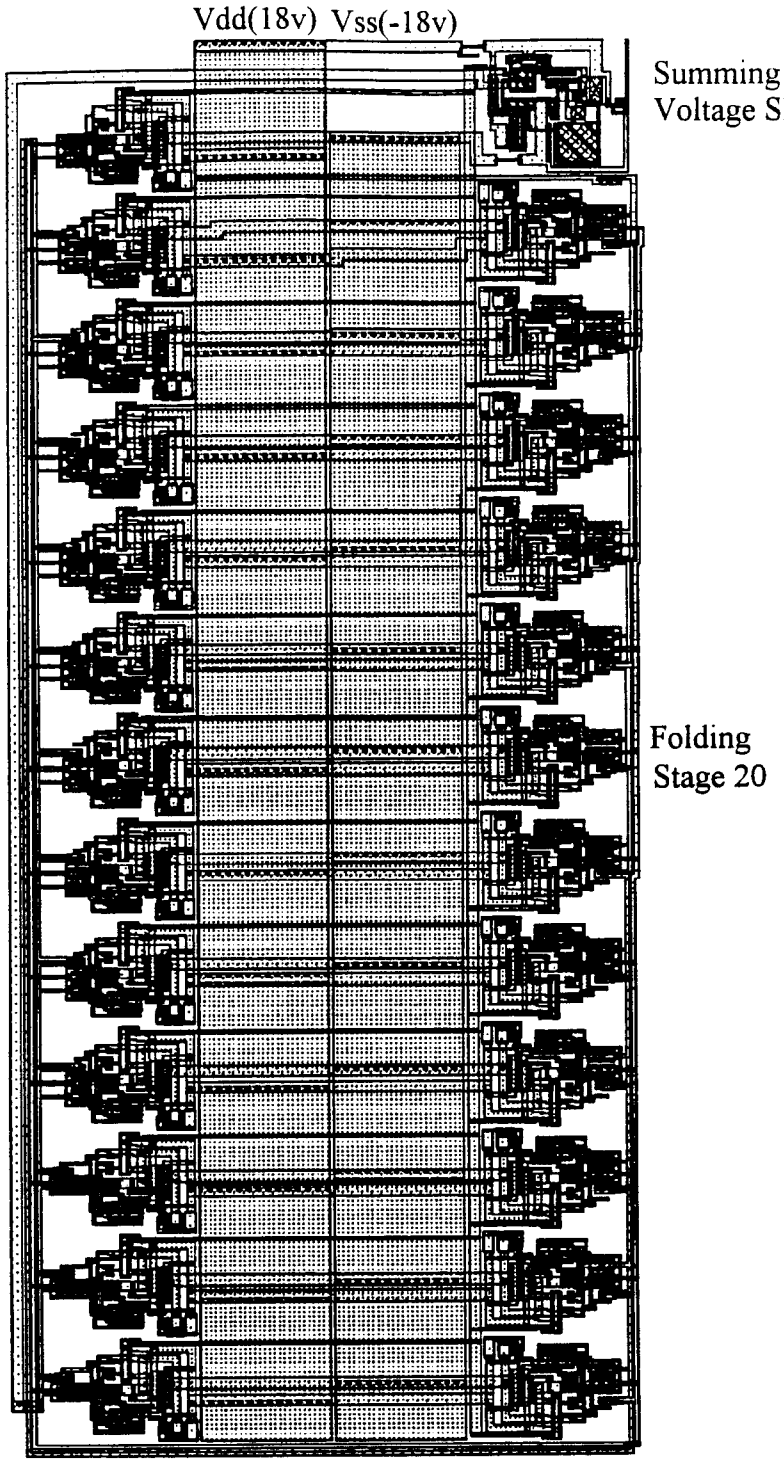


Figure 24. Channel 11 Folding Circuit CMOS Layout

As shown in Figure 24, the +18 volt and -18 volt power supply interconnects are located in the middle of the layout with folding stages located on either side. Widths for the interconnects are calculated based on the current limits of metal one and metal two as previously described in the layout of the folding stage. A common V_{in} interconnect is used with taps taken off to each of the folding stages. The designed folding reference voltage V_{ref} resistor ladder network is connected between the various stages and powered from the +18 volt power supply interconnect. The outputs for the folding stages are sent to a common interconnect and applied to the input of the summing amplifier. The +15 volt and -15 volt power supplies to the summing amplifier and voltage shifter are derived from the +18 volt and -18 volt power supplies by use of voltage dropping resistors. Dimensions of the channel 11 folding circuit is 1.2 mm by 2.78 mm resulting in a total chip area used of 3.34 mm^2. CMOS implementations of the channel 7 and channel 8 folding circuits use 4.87 mm^2 and 4.20 mm^2 respectively.

V. SIMULATIONS

Simulations are conducted at each step of the layout of the folding circuit in order to verify proper implementation of the circuit in CMOS, as well as to compare the layouts to the previous SNS analog preprocessing architecture research. A systematic methodology is followed during the layout and simulation phase of the project. Each designed and implemented circuit is simulated before proceeding to the next level of integration. Finally, simulations are completed on the entire folding circuit. Both DC and transient behavior of the circuits are investigated along with the effects of changing the Spice level 2 parameters describing the transistor models.

A. CIRCUIT SIMULATION METHODOLOGY

An iterative method is used for simulating the layout of each analog preprocessing channel. Figure 25 is a simulation flow chart developed for this analysis and contains seven steps. Once the layout of a portion of the circuit is complete, it must be modified to be simulated. This modification includes removing all resistors and capacitors in the layout and any extraneous layers that would be extracted as floating nodes. Before extraction, the extraction style active in Magic is verified. The extraction style specifies the scale factor between a Magic unit and a physical unit. The extraction style used in this thesis is 1.0, resulting in a unit in Magic corresponding to 1 micron. This is extremely important for the extraction process which bases transistor size on the layout area for a transistor in Magic.

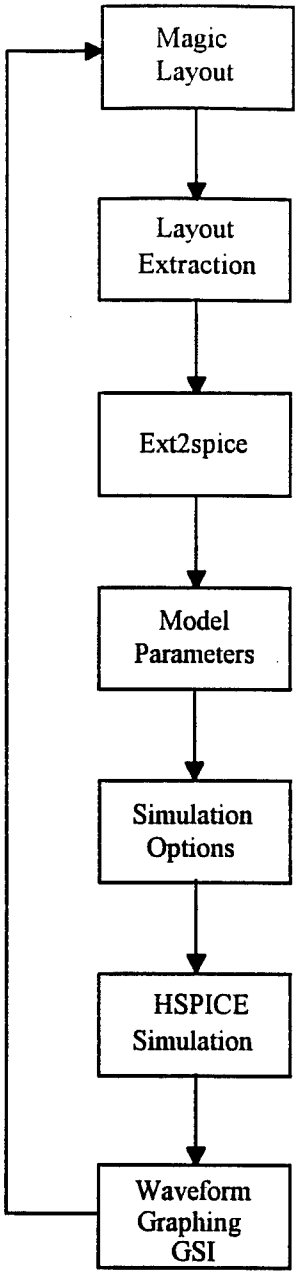


Figure 25. Layout Simulation Flow Chart

The layout is extracted using the Magic command **:extract** which, produces a **.ext** file. A **.ext** file for one folding stage is included in Appendix B part A. Following the extraction of the layout, the program ext2spice is used to convert the **.ext** file into a **.spice** file. The converted **.spice** file contains transistor instantiations in the spice format and any internodal coupling and substrate capacitance that is extracted. An example of the **.spice** file for the extracted folding stage is included in Appendix B part B.

In its converted format, the **.spice** file is not ready for simulation. Any capacitors or resistors in the original layout must be manually added to the file. It is important to note that these are ideal components and not the actual layout representations. Transistor model parameters and any simulation options must be added to the **.spice** file before successful simulation can take place. The transistor Spice level 2 model parameters used for all simulations in this thesis are provided by MOSIS and are included in Appendix C. These models are constructed from data accumulated from various recent fabrication runs by different vendors.

Appendix B part C is a modified **.spice** file, ready for simulation using HSPICE. The HSPICE run is based on the simulation options chosen with outputs of the simulation written to a file for later examination. Progress of the simulation can be tracked by using the simulation report file **.st0** or by monitoring the output file using the graphical interface GSI. After the simulation is complete, GSI can be used to obtain results of the run for verification and comparison to previous simulations. If the results of the simulation are

not satisfactory, the layout is modified and extracted, repeating the process above in an iterative fashion.

B. FOLDING CIRCUIT DC ANALYSIS

1. Folding Stage

Simulation of the folding stage is accomplished using the procedure described in the previous section. A representative channel 11 folding stage is extracted and an executable spice file created. The VLSI Technology Spice level 2 parameters used in the original research is used for the transistor models. This set of parameters can be found in Appendix C part A. The DC analysis of the circuit is performed by applying a linear ramp V_{in} of 0.0 volts to 2.0 volts to the input of the folding stage. A folding reference voltage V_{ref} of 1.28 volts is used to supply the proper folding period. Figure 26 shows the result of the simulation. The waveform obtained is measured at the output of the emitter follower and 1 kΩ resistor. The waveform has the correct shape required of the SNS analog preprocessing scheme and folds at the proper folding reference voltage V_{ref}.

Next, the current mirror is extracted and an executable spice file is produced. The VLSI Technology Spice level 2 parameters are used for the transistor models. The current mirror is tested over the voltage range measured during simulation of the folding stage. A reference current I_{ref} is produced using an 18 volt ideal voltage supply and a 85 kΩ resistor. Figure 27 contains the results of this simulation. A reference current I_{ref} of 0.2043 milliamps is produced with the output current I_{out} of the current mirror varying from 0.2050 to 0.2052 milliamps.

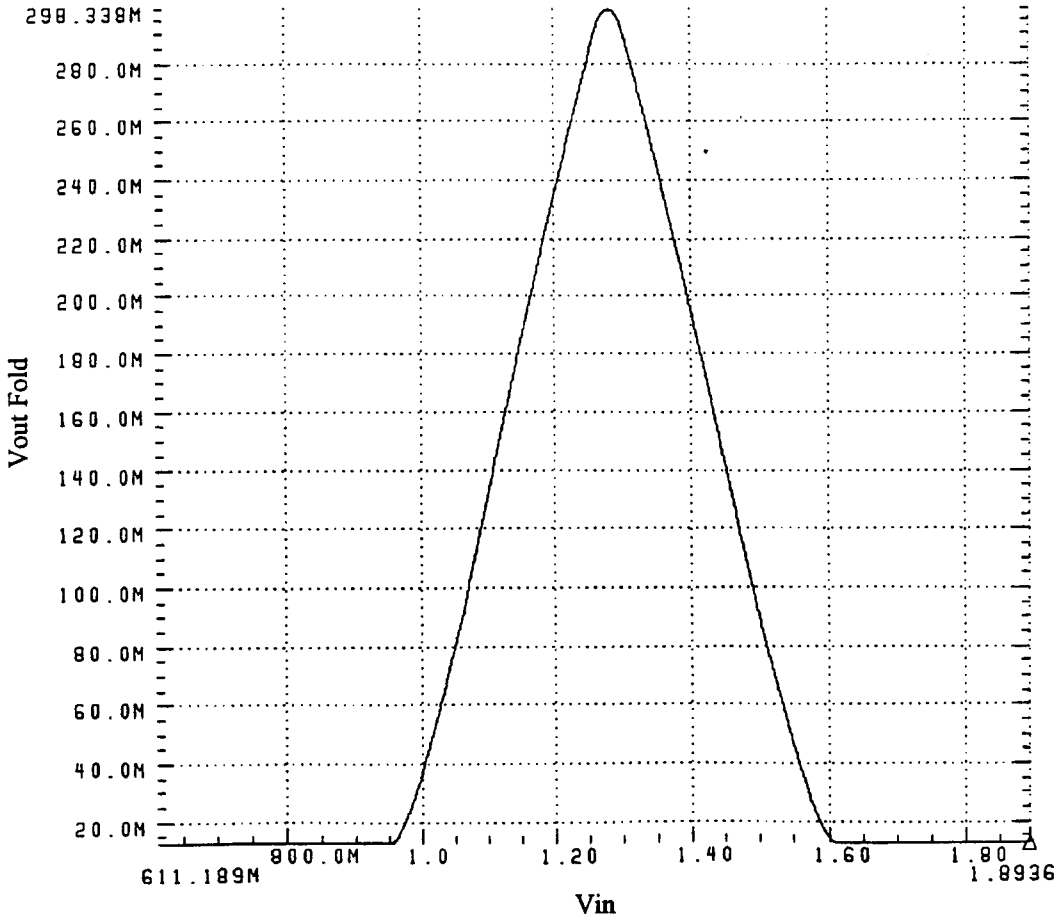


Figure 26. Folding Stage Simulation Output

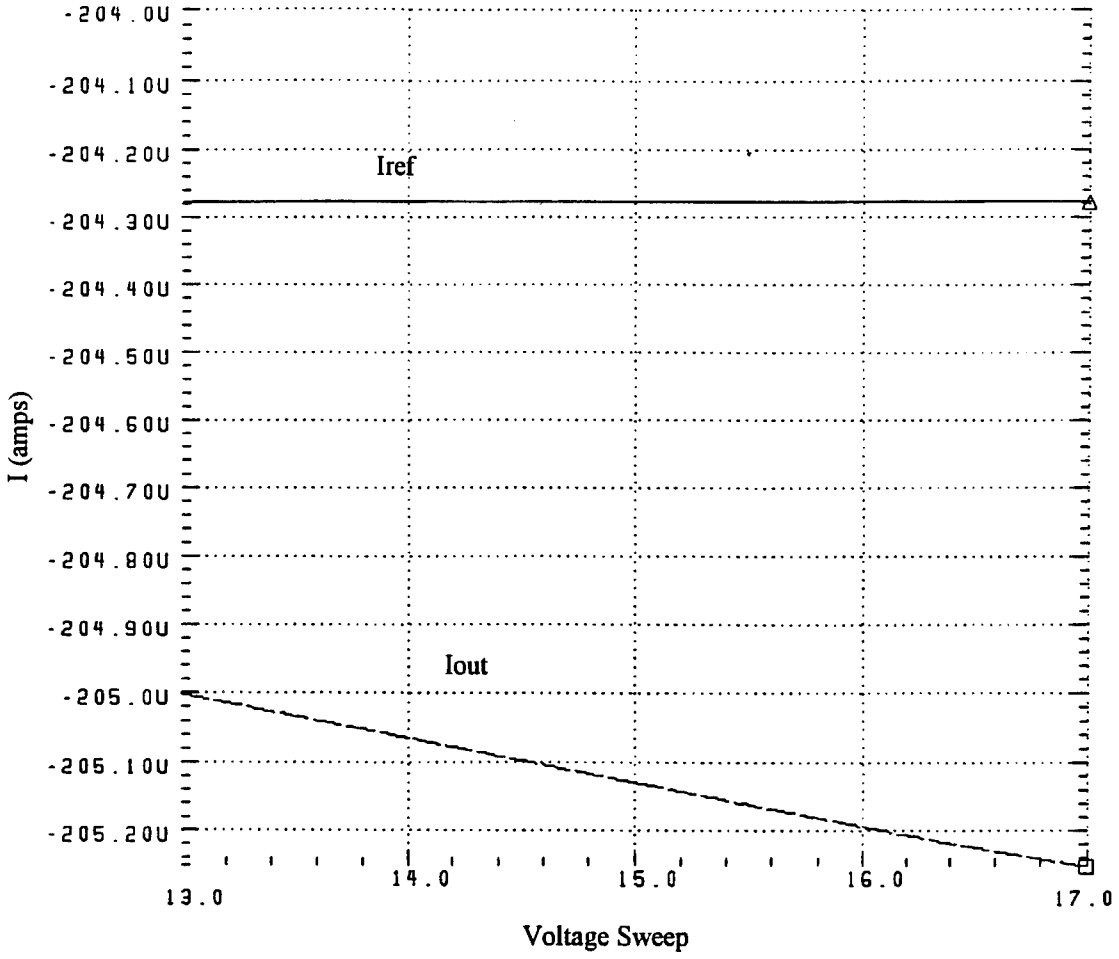


Figure 27. Current Mirror Simulation Output

2. Summing Amplifier and Voltage Shifter

Simulation of the summing amplifier and voltage shifter is accomplished by connecting the summing amplifier and voltage shifter layout to the generic folding stage layout. This combined layout is extracted and an executable spice file created. The DC analysis of the circuit is performed by applying a linear ramp V_{in} of 0.0 volts to 2.0 volts to the input of the folding stage. A folding reference voltage V_{ref} of 1.28 volts is used to supply the proper folding period. Figure 28 shows the result of the simulation. The waveform obtained is measured at the output of the voltage shifter. The waveform has the correct shape required of the SNS analog preprocessing scheme, folds at the proper folding reference voltage V_{ref} and has sufficient gain for input into the comparator ladder in the digital portion of the SNS 9-bit folding ADC.

3. Folding Circuit

After successful extraction and simulation of the individual folding stages, current mirror, summing amplifier and voltage shifter, simulations are conducted on the entire folding circuit. Channel folding circuits 7, 8 and 11 are extracted and executable spice files produced. The folding circuit spice simulation files are in the same format as Appendix B part C. Applicable folding reference voltages V_{ref} are added as ideal voltage sources to each folding circuit. VLSI Technology Spice level 2 parameters are used for the transistor models. The DC analysis of each folding circuit is performed by applying a linear ramp V_{in} of 0.0 volts to 15.0 volts to the input of the folding circuit. This yields simulation results for the entire dynamic range of the SNS 9-bit folding ADC design.

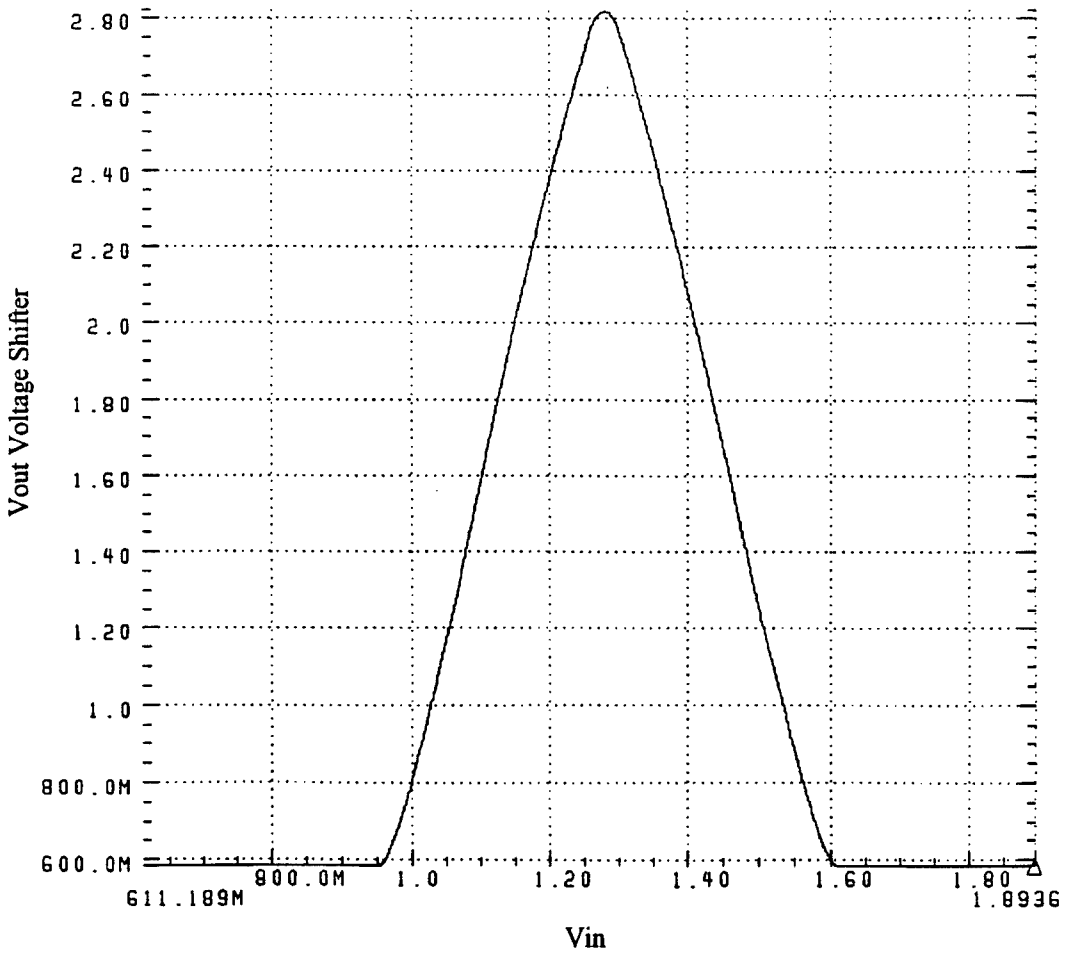


Figure 28. Summing Amplifier and Voltage Shifter Simulation Output

Simulation results are provided in Figure 29. The folding circuit for each channel generated the proper folded waveform with the correct folding period.

4. Power Estimation

As discussed in Chapter IV, the widths for power and ground conductors are chosen based on ensuring that the current density for the particular conductor is not exceeded. HSPICE is used to measure the current in the conductors and power consumption for each of the circuits. Table 7 provides the results of the analysis for the folding stage, summing amplifier and voltage shifter, and the three folding circuits.

Circuit	Current Load	Power
Folding Stage	15.77 mA	283.86 mW
Summing Amplifier Voltage Shifter	16.74 mA	251.10 mW
Folding Circuit for Channel 7	381.82 mA	6872 mW
Folding Circuit for Channel 8	332.17 mA	5979 mW
Folding Circuit for Channel 11	252.47 mA	4544 mW

Table 7. Current Loading and Power Consumption

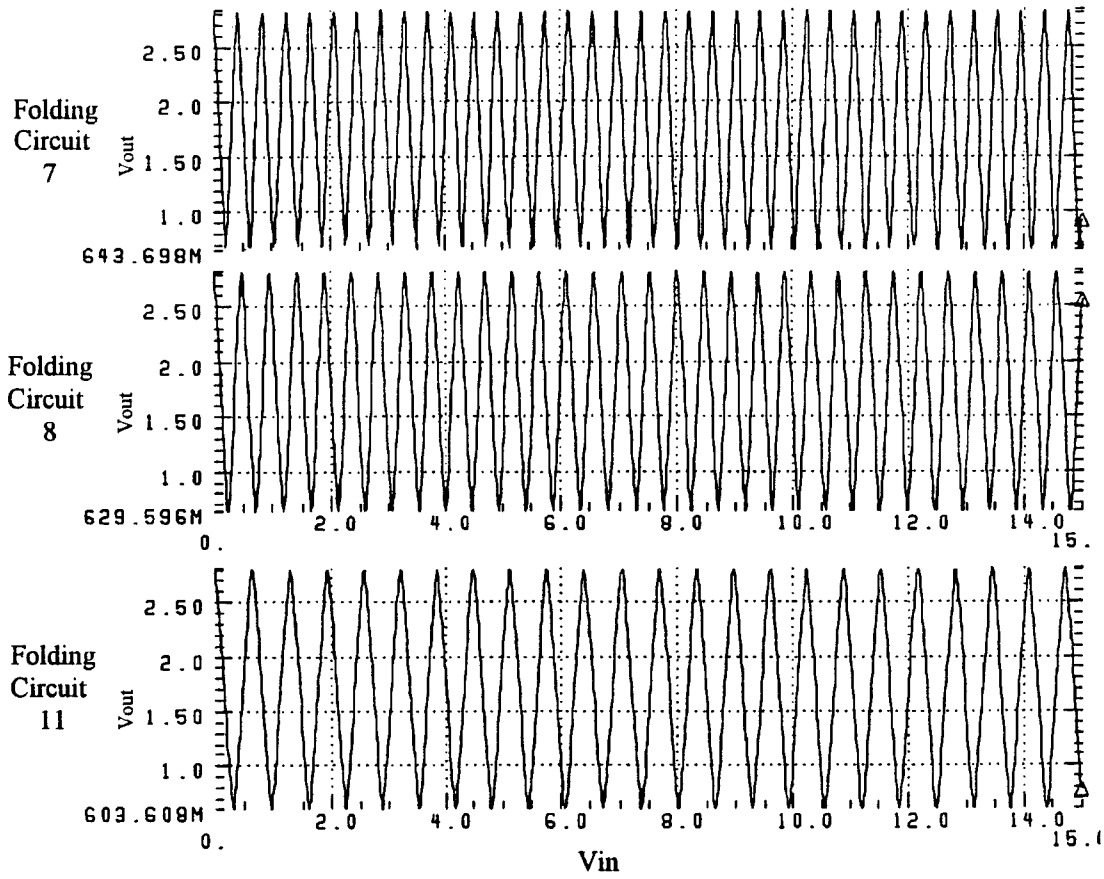


Figure 29. Folding Circuit 7, 8, and 11 Simulation Output

C. FOLDING CIRCUIT FREQUENCY RESPONSE

After satisfactory results are obtained from the DC analysis of the folding circuits, a transient analysis is conducted using HSPICE to determine the frequency response of each channel. A piece-wise linear PWL signal is generated in order to simulate a triangular wave input to the circuits. The input signal ranged from 0.0 volts to 15.0 volts to ensure that the entire dynamic range of the folding circuit is tested. The frequency of the input signal is increased over several trials ranging from 1 Hz to 1 MHz.

Figures 30 through 33 show the frequency response obtained for several input frequencies and the resulting effects on the folded waveform for the channel 11 folding circuit. Only a portion of each of the folding circuit waveform is shown in order to clearly see these effects. The frequency response is acceptable up to 100 KHz, but degrades rapidly after that as shown in Figures 32 and 33. The degradation is more apparent in Figure 34 which combines all of the various frequency responses of the previous figures. Even though the folded waveform shows some amplitude degradation at 100 KHz, it is still acceptable because the comparator thresholds do not occur at the top or bottom of the folded waveform. The frequency response exhibited by the extracted layout of the folding circuit agrees with previous research on the SNS analog preprocessing architecture [Ref. 2].

A possible explanation for the low frequency response of the folding circuit involves the size of the transistors used in the differential amplifier pairs of the folding stage. These transistors have very large widths, which increases the capacitance

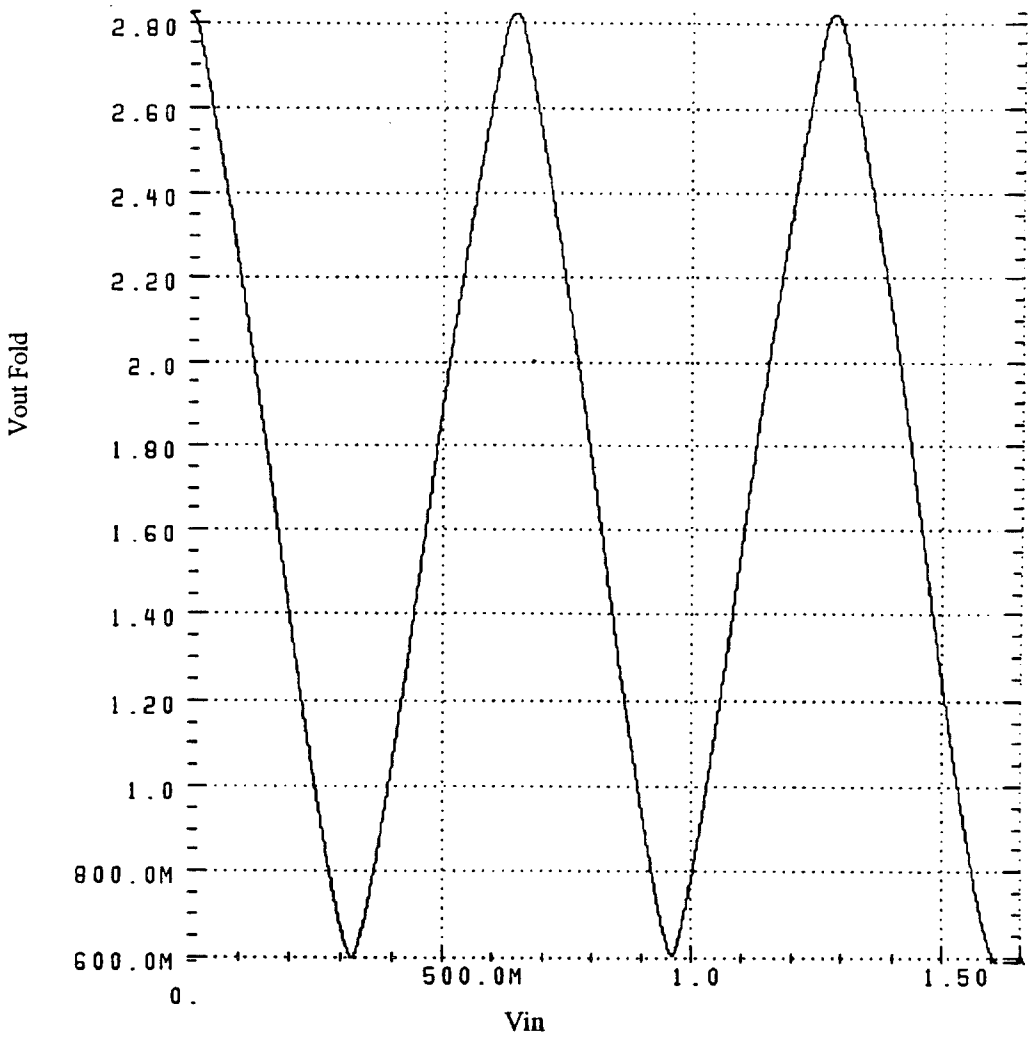


Figure 30. Folding Circuit Frequency Response for 10 KHz

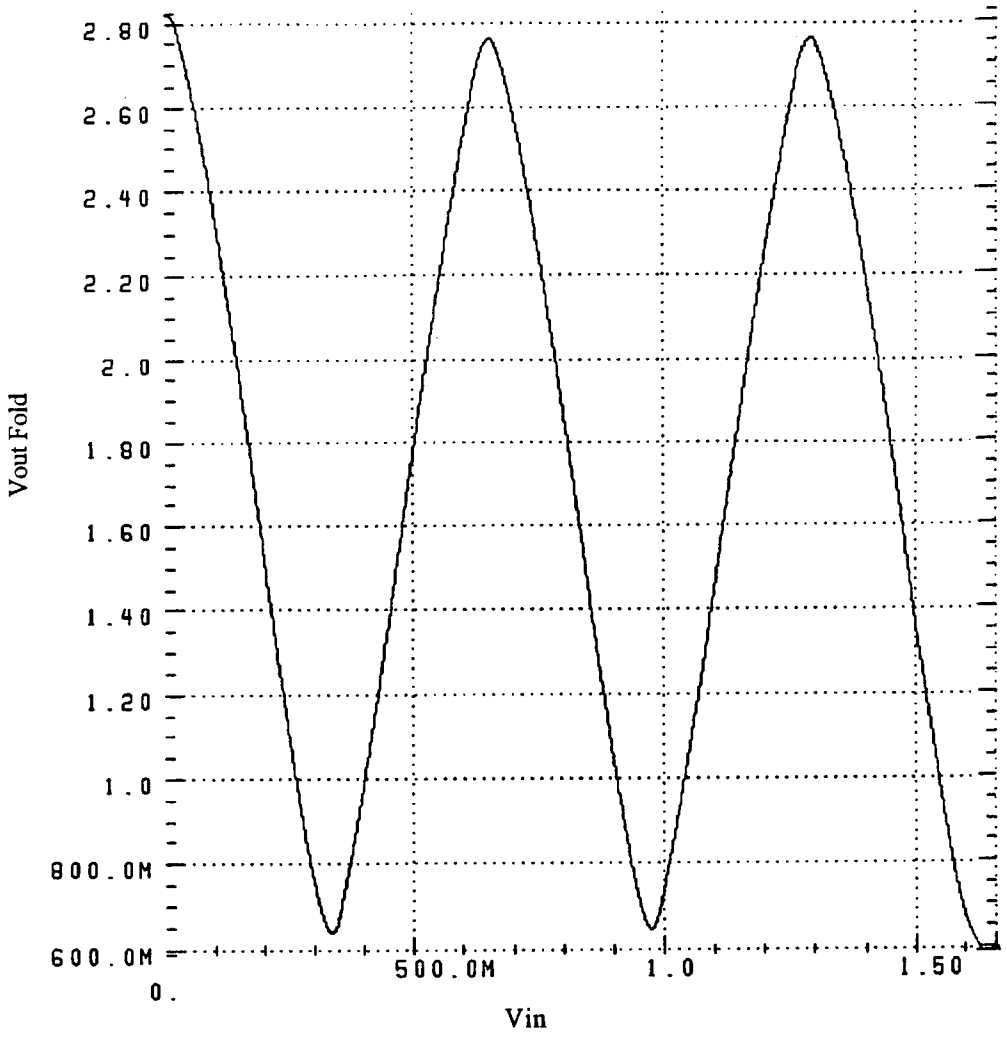


Figure 31. Folding Circuit Frequency Response for 100 KHz

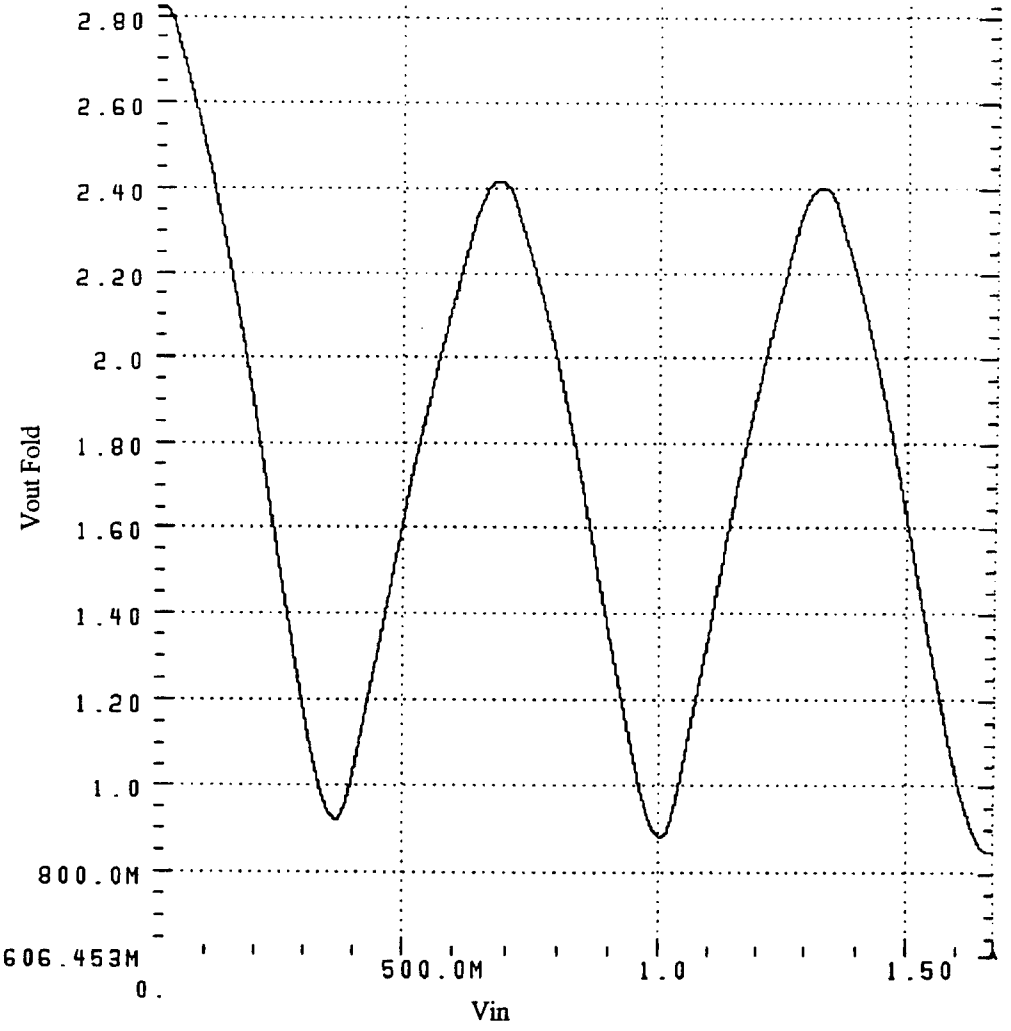


Figure 32. Folding Circuit Frequency Response for 500 KHz

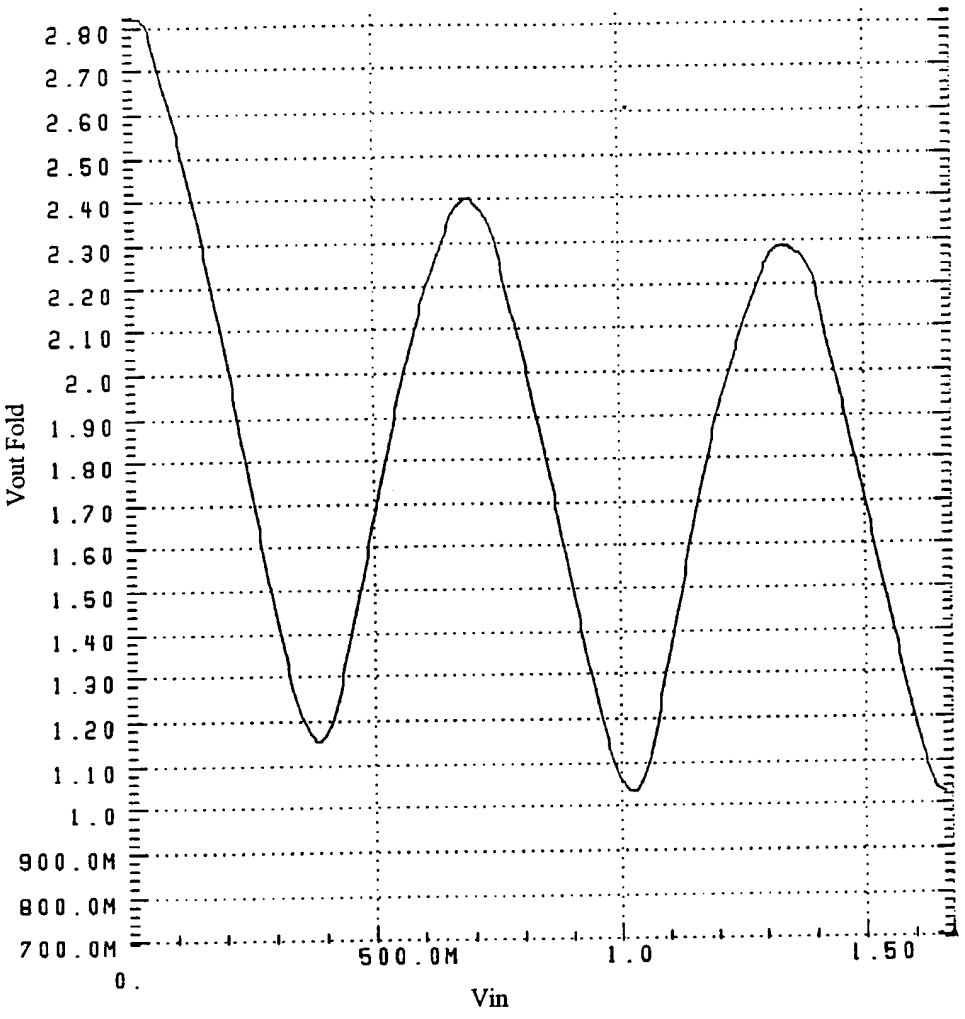


Figure 33. Folding Circuit Frequency Response for 1 MHz

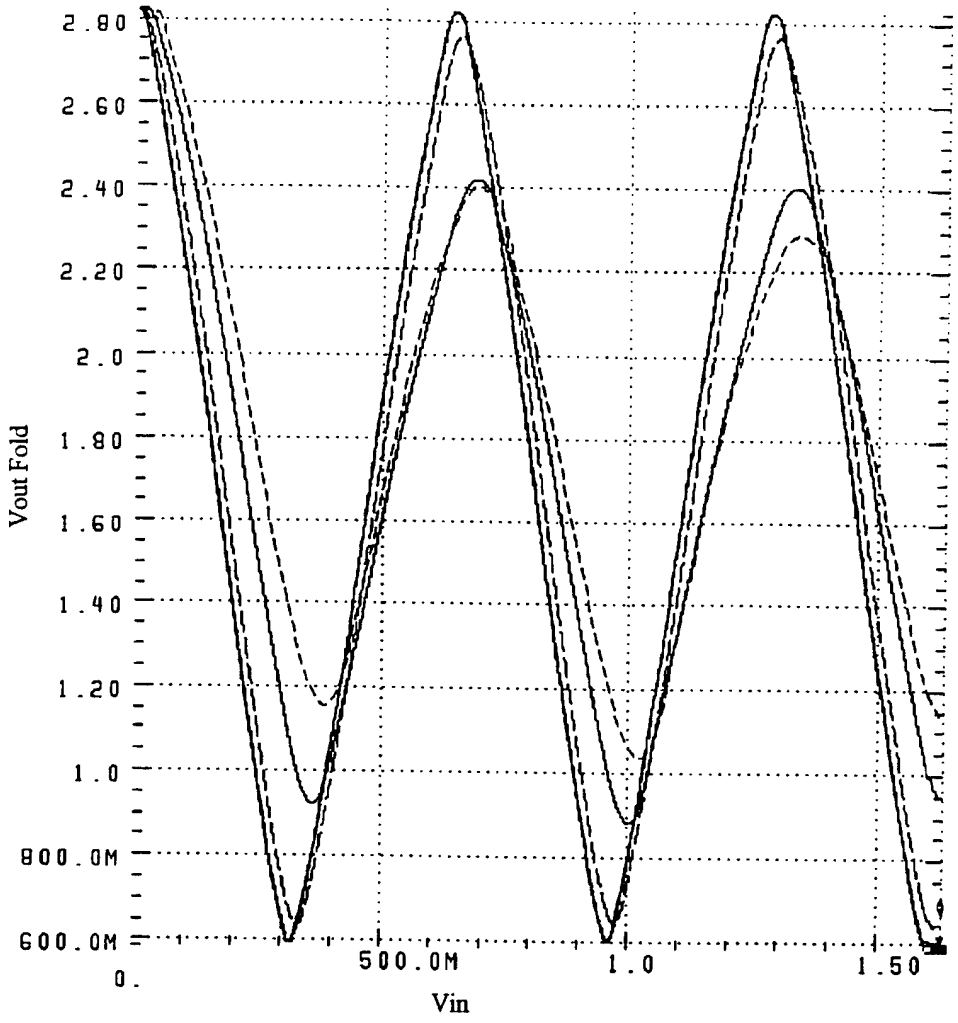


Figure 34. Folding Circuit Combined Frequency Response

associated with the transistors. The slew rate of the folding stage is inversely proportional to this capacitance by the equation

$$\text{Slew Rate} = \text{SR} = \frac{I}{C_c}, \tag{11}$$

where I is the biasing current, I1 or I2 in the folding stage and C_c is the capacitance associated with the transistors. A higher value of capacitance corresponds to a smaller slew rate which indicates a lower frequency response.

Another method of quantifying the degradation of the folded waveform as a function of frequency is by use of the extinction ratio defined as

$$\text{ER} = 20\log\left(\frac{V_{min}}{V_{max}}\right). \tag{12}$$

The voltages V_{min} and V_{max} are determined from the peak and trough of the folded waveform. Figure 35 summarizes these results for the transient analysis conducted on the folding circuit. [Ref. 9]

D. SPICE LEVEL 2 PARAMETER FABRICATION TOLERANCE

Several vendors are available that offer the 2μ CMOS N-well process for fabricating chips through MOSIS. The Orbit 2μ CMOS N-well double-metal, double-poly, low-noise analog process offers better noise characteristics that are critical to analog VLSI CMOS design and offers a more flexible fabrication schedule. Since all of

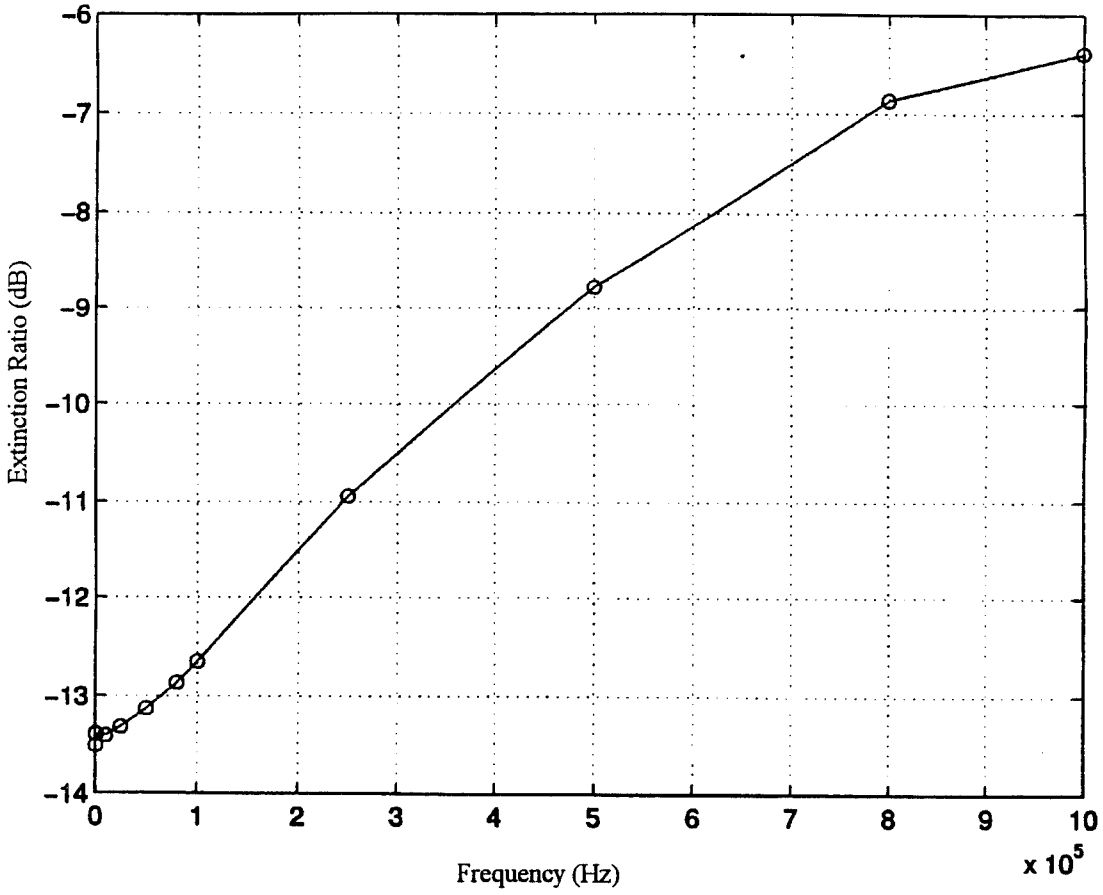


Figure 35. Extinction Ratio

the original design work and simulations on the circuit layouts were conducted using the VLSI Technology 2μ CMOS N-well Spice level 2 nominal parameters, simulations were repeated using the Orbit 2μ CMOS N-well Spice level 2 parameters.

Vendors supply Spice level 2 parameters as maximum and minimum values to account for fabrication tolerances in their manufacturing processes. Due to the sensitivity of analog circuits to noise, design and simulation of analog VLSI circuits must take these fabrication tolerances into account. The circuits must be designed so that they will function correctly within the boundaries of these tolerances. In order to verify that a circuit will behave correctly within the fabrication tolerances, simulations are run using a four corners approach. The four possible combinations of maximum and minimum values of the pfet and nfet transistor Spice level 2 model parameters are simulated with the circuit. These four combinations of Spice level 2 parameters for the Orbit 2μ CMOS N-well analog process are included in Appendix C part B.

A DC analysis is conducted on the folding circuits using the four corners approach. The results of these simulations are shown for the channel 11 folding circuit in Figure 36. Curve A represents results obtained for the maximum values of the Spice level 2 parameters for the pfet transistors and the minimum values of the Spice level 2 parameters for the nfet transistors. Curve B represents results obtained for the maximum parameter values for both pfet and nfet transistor types and curve C represents results obtained for the minimum parameter values for both pfet and nfet transistor types. Finally, curve D represents results obtained for the minimum parameter values for the pfet transistors and

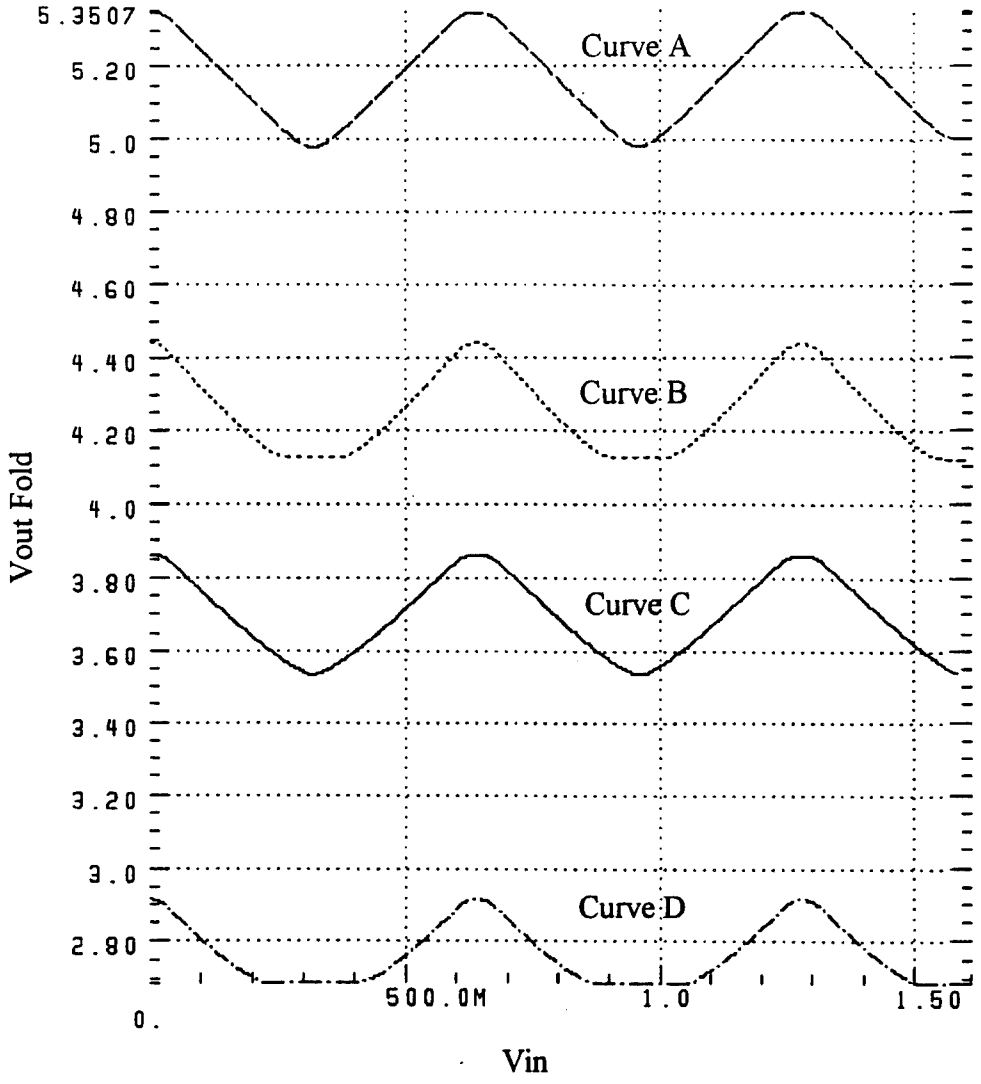


Figure 36. Folding Circuit Output for Orbit Parameters

for the maximum parameter values for the nfet transistors.

Results of the simulation were only relatively successful. Significant sensitivity to the change in parameter values is noted, including a decrease in the amplitude of the folding waveform, a DC voltage offset of the folding waveform, and cutoff of the lower portion of the folding waveform for two of the four simulations. However, the folding waveform still exhibits the proper folding period around the folding reference voltages V_{ref} and maintains the proper shape for use in SNS analog preprocessing.

The decrease in amplitude of the folding waveform is attributed to lower gain of the folding stage and summing amplifier at the transistor level. The transconductance g_m expresses the relationship between the output current and the input voltage and is a measure of the gain of the transistor. While a transistor is operating in the saturation region, the transconductance is given by

$$g_m = 2K(V_{GS} - V_t). \tag{13}$$

The intrinsic transconductance K and the threshold voltage V_t are device parameters and are affected by the fabrication process. The gate-source voltage V_{GS} is controlled by the designer. The intrinsic transconductance value for the VLSI Technology Spice level 2 parameters is higher than the Orbit Spice level 2 parameters and the threshold voltage is lower. These two factors combine to cause the transconductance and thus gain to be lower for simulations using the Orbit parameters. This is easily adjusted by changing the value of the feedback resistor R_f in the summing amplifier.

The DC voltage offset for the folding waveform is credited to the active load resistor in the voltage shifter. Referring to Figure 6, the diode connected transistor M10 controls the drain current I_D of transistor M9. The drain current can be determined by

$$I_D = 2K(V_{GS} - V_t)^2, \tag{14}$$

where V_{GS} is the gate-source voltage of the transistor. Again, the intrinsic transconductance K and the threshold voltage V_t are device parameters and are affected by the fabrication process. Changes in these parameters will change the drain current and thus the DC voltage drop across M10. The DC voltage offset of the folding waveform is accounted for by making the comparator threshold voltages adjustable in the digital portion of the SNS 9-bit folding ADC. Based on test results of the actual fabricated circuit and the measured output of the folding waveform, the correct threshold values are determined and applied to the comparator ladder of each folding circuit.

The cutoff of the lower portion of the folding waveform is attributed to the biasing of the differential amplifier pairs in the folding stage. From Equation 14, changes in the intrinsic transconductance K and the threshold voltage V_t change the drain current for a given gate-source voltage V_{GS}. This shifts the voltage-current characteristics of the transistor. The biasing currents I1 and I2 for the differential amplifier pairs in Figure 3 provide a DC bias or operating point for the transistor. Biasing currents are chosen to maintain the DC operating point in the middle of the saturation region of the transistor. This is important since a continuously changing input signal applied to the transistor

causes the instantaneous operating point to vary about this DC operating point. If the DC operating point is to close to the triode region of the transistor, the instantaneous operating point can enter the triode region causing distortion of the output signal. By changing the current-voltage characteristics of the transistor due to the fabrication process parameters, the DC operating point is effectively changed causing the cutoff in the lower portion of the folding waveform seen in Figure 36. This is corrected by applying different biasing currents I1 and I2 to the differential amplifier pairs in order to shift the DC operating point back to the middle of the saturation region of the transistor.

Figure 37 shows the results of changing the biasing current I1 and I2 values and the feedback resistor R_f value on the folding waveforms. A feedback resistor value of 200 kΩ and biasing current values ranging from 0.19 milliamps to 0.25 milliamps are chosen. The folding waveform curves are defined as in Figure 36. Note that the amplitude of the waveforms has increased from 0.4 volts to 1.25 volts and that no distortion is apparent in the waveforms.

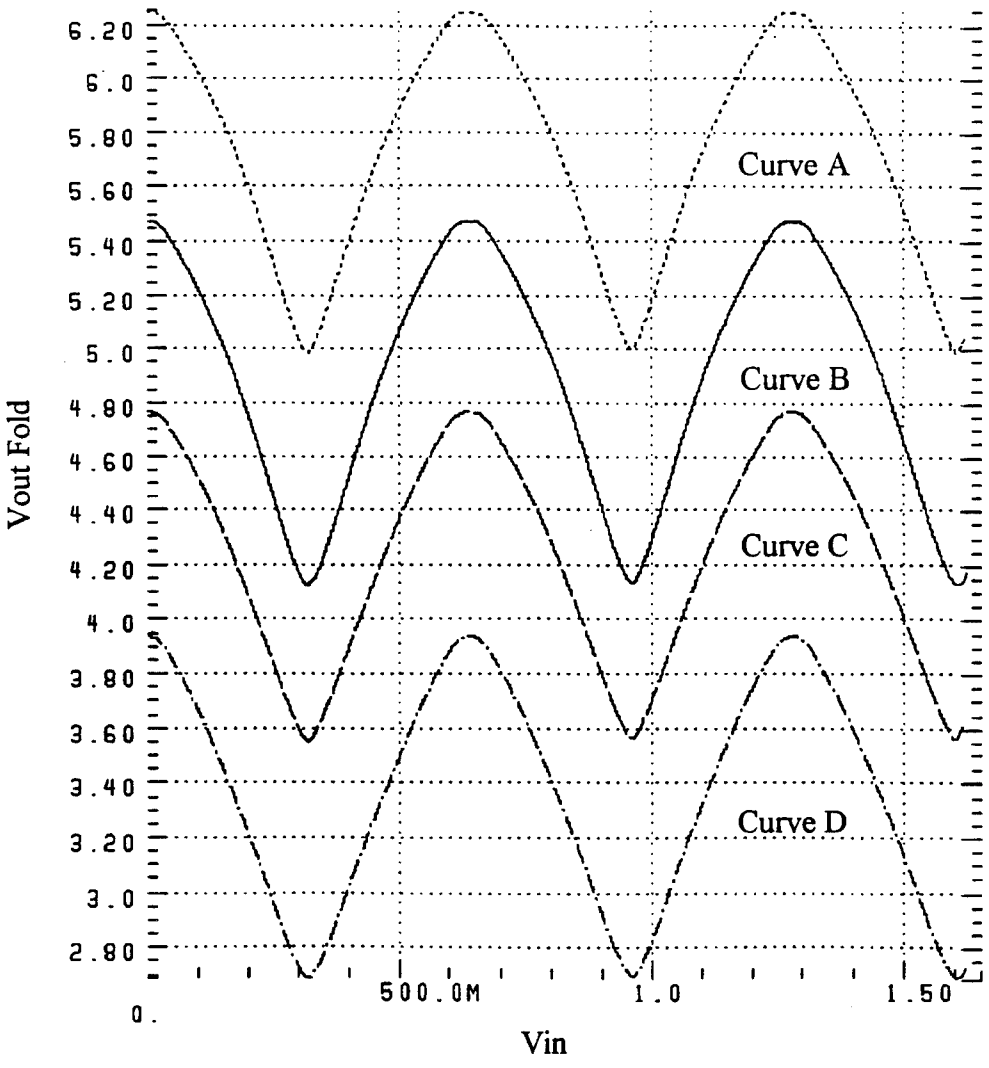


Figure 37. Modified Folding Circuit Output for Orbit Parameters

VI. FABRICATION

A. SNS 9-BIT FOLDING ADC VLSI ASIC

Originally, this thesis envisioned fabricating an entire SNS 9-bit folding ADC based on the original design shown in Figure 2. A CMOS VLSI layout is produced incorporating both the SNS analog preprocessing architecture in the form of channel 7, 8 and 11 and the necessary comparator, latch, channel PLA and PLA circuitry. Figure 38 is the floor plan used for this layout. The actual CMOS VLSI layout is shown in Figure 39. In order to fit the entire design on a single chip for fabrication by MOSIS, a small chip size is chosen with dimensions of 4.6 mm by 6.8 mm. The chip is to be fabricated using the VLSI Technology 2.0μ CMOS N-well process as originally designed and simulated [Ref. 2].

Before this layout was submitted for fabrication, simulation results for the folding circuits were obtained as discussed in Chapter V. Based on these results it is determined that fabricating the entire SNS 9-bit folding ADC will not be economically feasible without further testing of the folding circuits.

B. FOLDING CIRCUIT VLSI ASIC

After determining that the entire SNS 9-bit folding ADC will not be fabricated, a CMOS VLSI layout based solely on the SNS analog preprocessing architecture is proposed. In order to fabricate all three folding circuits, a small chip size of 4.6 mm by 6.8 mm is still necessary because of the dimensions of the individual folding circuits. This

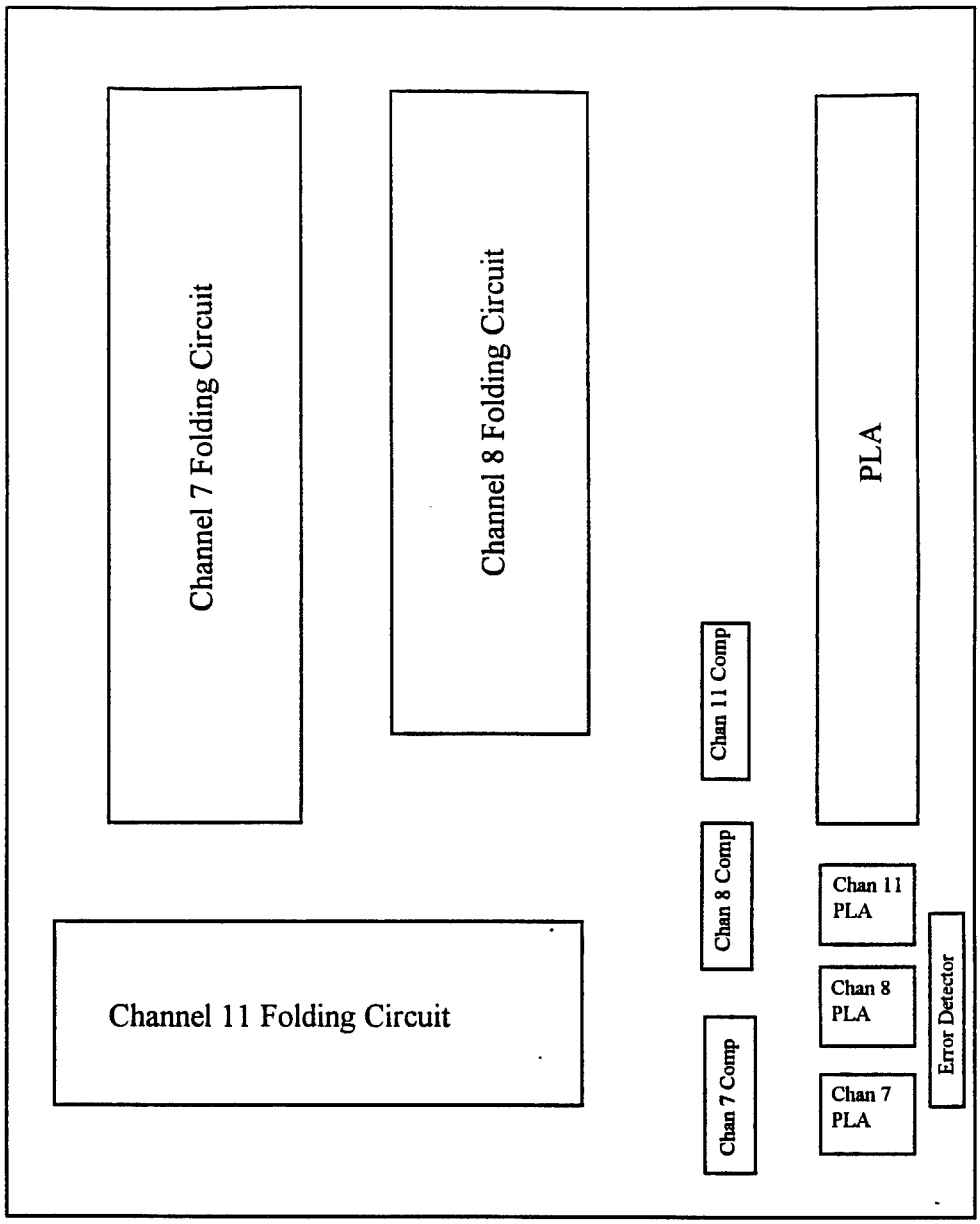


Figure 38. SNS 9-bit Folding ADC Floor Plan

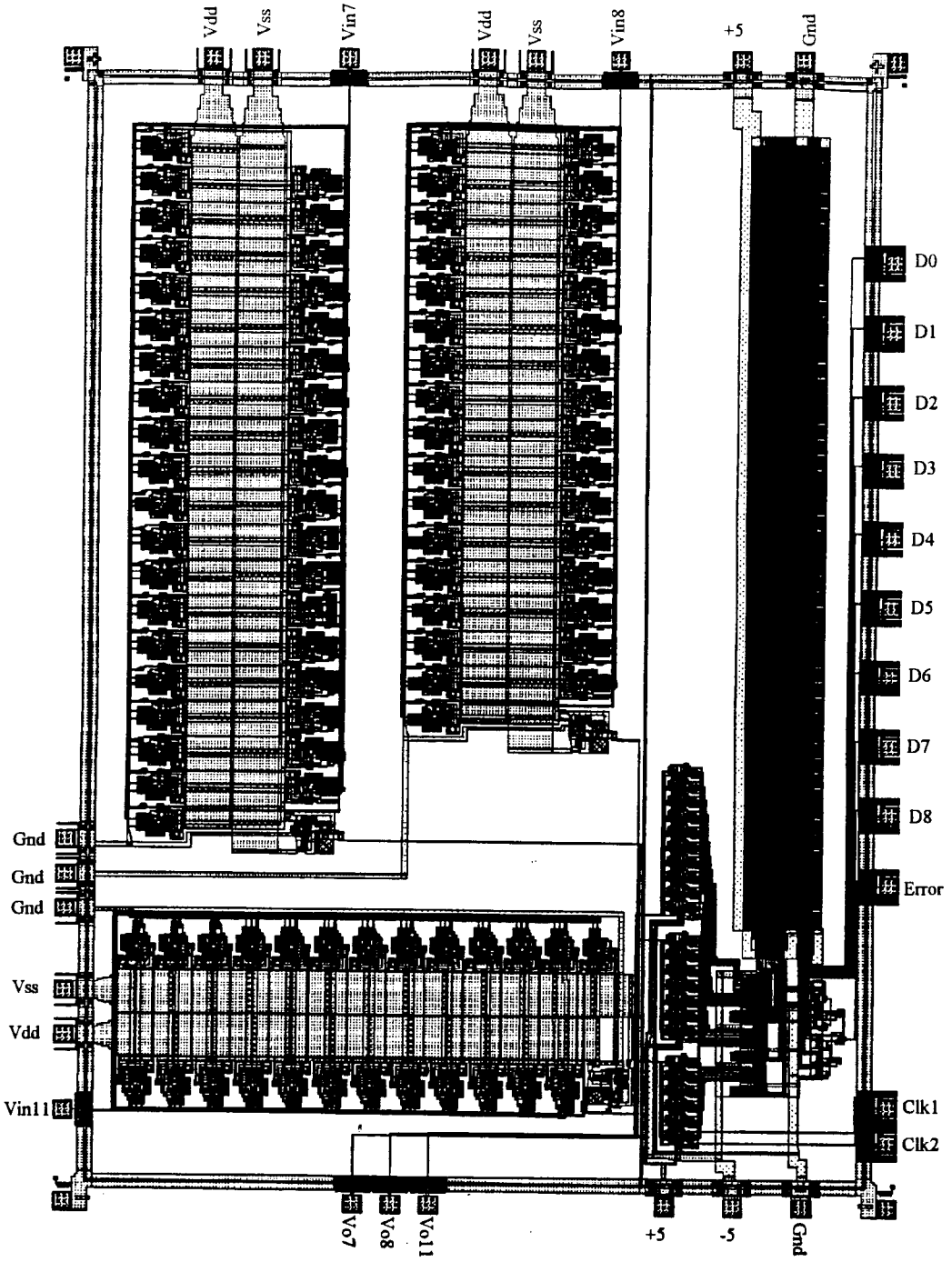


Figure 39. SNS 9-bit Folding ADC CMOS Layout

will result in a chip with a large amount of valuable die area wasted. A compromise is reached by using a tiny chip with dimensions of 2.22 mm by 2.25 mm. Using this chip size means that an entire folding circuit can not be reproduced. In order to provide valuable testing capability for the SNS analog preprocessing architecture and also produce a chip that can be used in future digital design work, a small portion of the dynamic range of each of the three folding circuits is fabricated. Seven folding stages for each of the three channels are constructed with outputs connected to a summing amplifier and voltage shifter for each channel. This arrangement provides a dynamic range of 2.5 volts for the layout. Figure 40 shows the CMOS layout for the seven folding stages comprising the channel 7 folding circuit portion of the chip. A common interconnect is provided between the individual folding stages for Vdd, Vss, Vin and Vout. Folding stage folding reference voltages V_{ref} are provided by a resistor ladder network. A cascode current mirror is used to provide the biasing currents I1 and I2 with individual taps for each folding stage.

A floor plan used for the layout of the folding circuit chip is shown in Figure 41. The actual folding circuit CMOS layout fabricated is shown in Figure 42. A common source of Vdd, Vss and Gnd is provided to the folding circuits. Input signal V_{in} and folding reference voltage sources V_{ref} are provided separately to each folding circuit to allow separate testing and adjustment of each circuit. Based on the simulation results of Chapter V, several extra pads are included in the layout to allow adjustment of the folding circuits to account for fabrication tolerances of the Spice level 2 parameters. In order to obtain the proper bias levels for the folding circuits, a separate I_{ref} input is included for

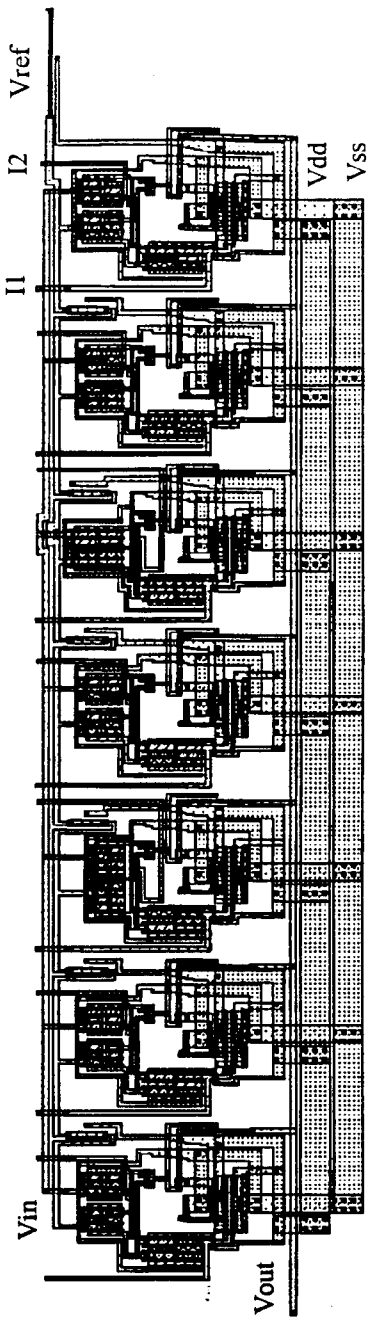


Figure 40. Folding Circuit CMOS Layout for Channel 7

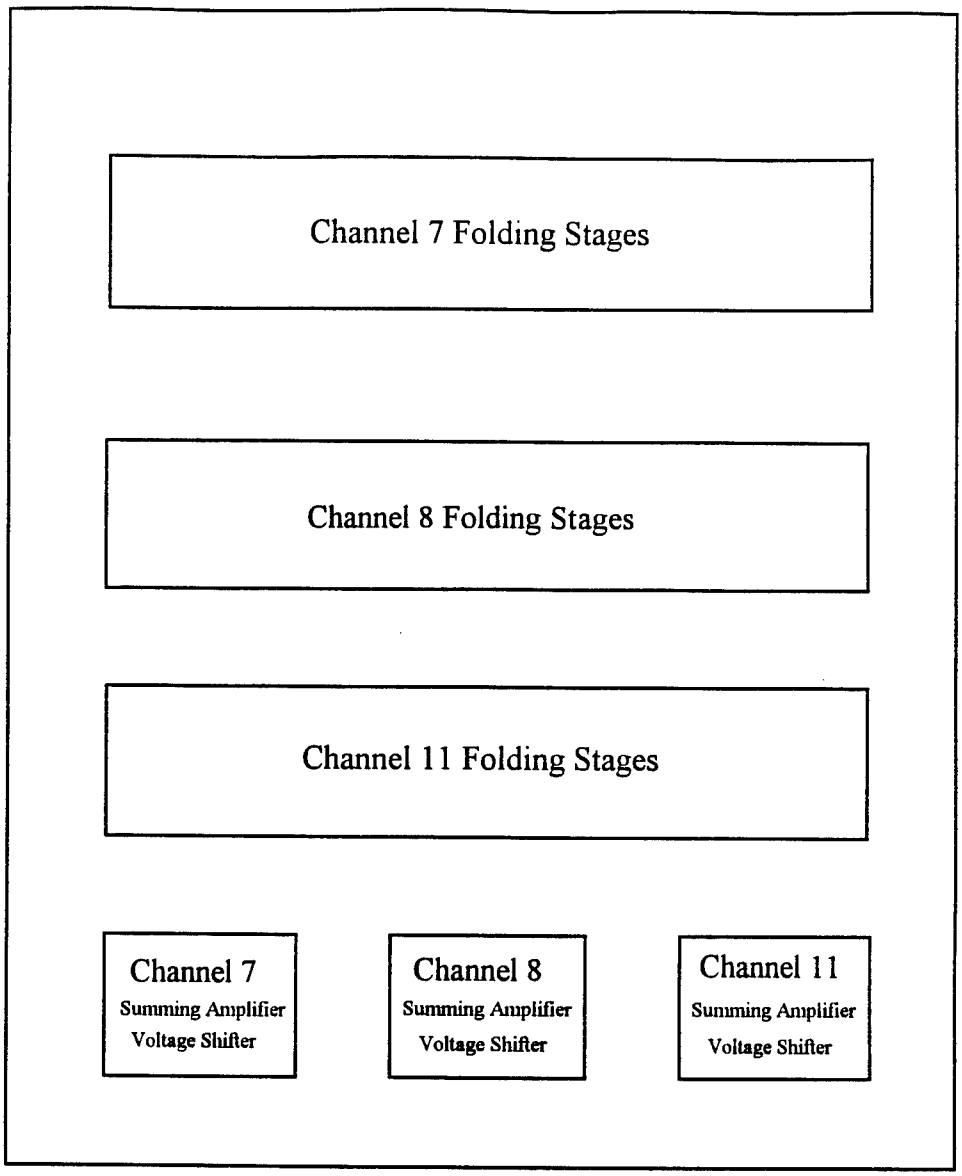


Figure 41. Folding Circuit Chip Floor Plan

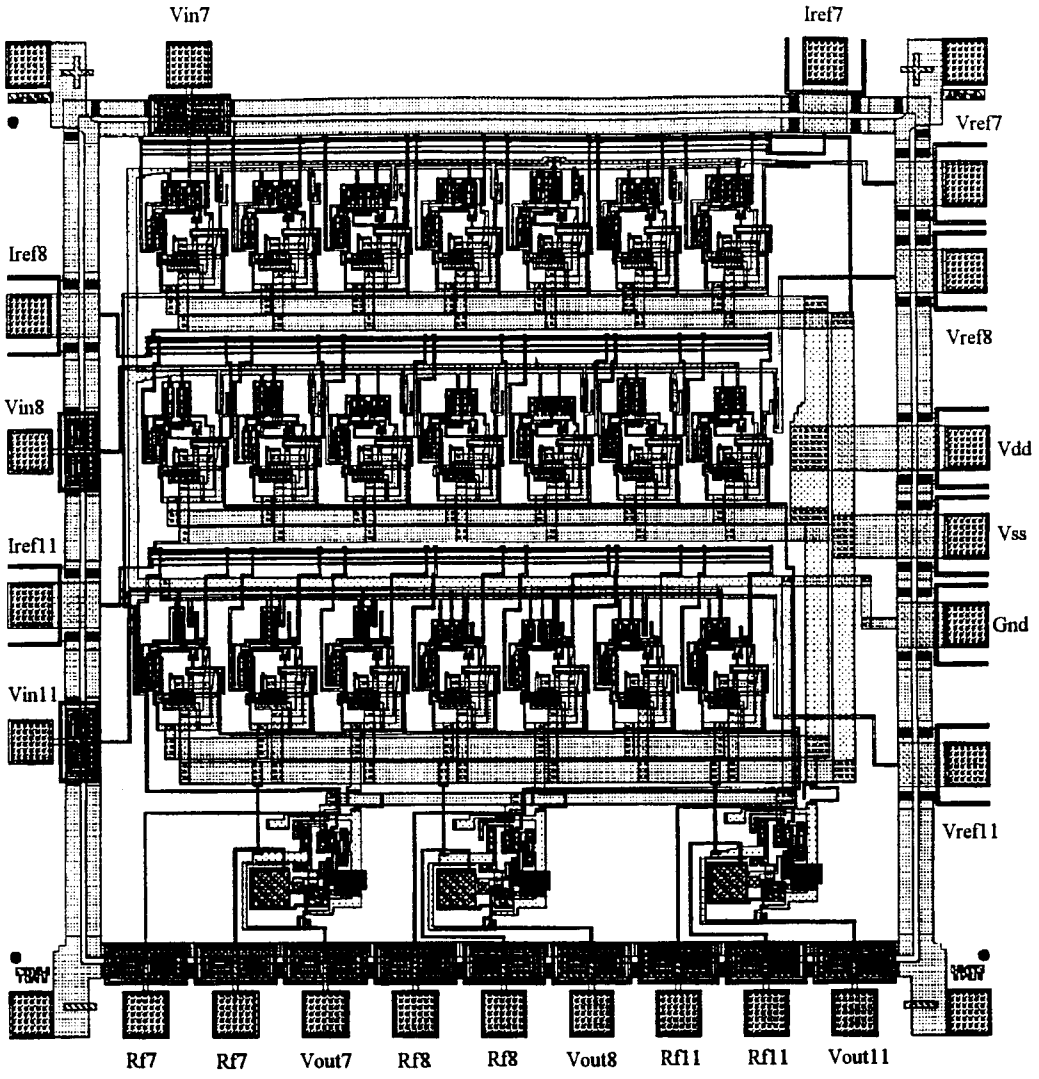


Figure 42. Folding Circuit Chip CMOS Layout

each folding circuit to allow adjustment of biasing currents I1 and I2. To allow adjustment of the gain of the folding waveforms at the outputs of the folding circuits, the feedback resistor R_f for the summing amplifier of each folding circuit is moved off chip.

The folding circuit chip is extracted and simulated to ensure proper functional operation and to confirm the correctness of the layout before submission to MOSIS for fabrication. The Orbit 2μ CMOS N-well double-metal, double-poly, low-noise analog process is used based on the analog only nature of the layout and the fabrication schedule in effect. Four chips were fabricated and received from MOSIS packaged in a 28 pin dual in-line package (DIP).

VII. CONCLUSIONS AND RECOMMENDATIONS

This thesis investigates the feasibility of implementing and fabricating a previously designed SNS analog preprocessing architecture using a 2μ CMOS N-well low-noise analog process. All circuits in the design are successfully implemented in VLSI using the CAD tool Magic. Simulations are conducted on the extracted layouts to verify functional operation and confirm proper layout before fabrication. An application specific integrated chip has been fabricated and awaits testing to confirm the results of simulations completed in this work [Ref. 10].

Several limitations of the designed architecture are noted during the course of this thesis. It is found that the modulus folding circuit is extremely sensitive to fabrication tolerances, producing distortions, reduced gain and DC voltage offsets in the folded waveform output. These anomalies are detrimental to the architecture's successful ability to be mid-level quantized by a comparator ladder in order to produce the proper SNS representation of the input signal. This limitation is corrected by including the ability to adjust the biasing currents to the folding stage and by including the ability to increase the gain of the output waveform through the summing amplifier.

Other limitations include the frequency response and power consumption of the architecture. The design only achieves a maximum frequency of 100 KHz before becoming unusable for SNS analog preprocessing. Although it confirms earlier research, it is well below that achieved in other designs. Power consumption for the folding circuits

is extremely high. The layouts are designed for this high power consumption, but it waits to be seen during testing of the fabricated chip if these results are accurate.

Finally, significant limitations to analog VLSI design are found in the available CAD tools. The inability to extract resistors and capacitors from a layout for simulation purposes reduces the confidence level of the simulation results and adds considerable time to the process of designing, extracting and simulating the architecture.

Future research in the area of SNS analog preprocessing should look toward designing a more compact folding stage that is insensitive to changes in fabrication parameter tolerances, that achieves a higher maximum frequency and that consumes less power. In its present state, the folding circuit described in this thesis requires an excessive amount of off chip functionality to allow adjustment for fabrication parameter variations. Investigation of other possible methods of producing the folded waveform with the required period for the SNS analog preprocessing architecture should be conducted. Other circuit designs that will produce the basic waveform that can be modified for use in this architecture should be evaluated. This research should include the use of the 0.8μ CMOS N-well technology, as well as the use of other types of semiconductor materials. Based on favorable results of this research, the SNS analog preprocessing architecture can be mated to the digital portion of the SNS 9-bit folding ADC to produce an analog-to-digital converter that truly presents a dramatic reduction in power consumption and chip size.

APPENDIX A. FOLDING CIRCUIT TRANSISTOR DIMENSIONS

A. FOLDING STAGE

1. Common Transistor Dimensions

Transistor	Length (microns)	Width (microns)
M1 (nfet)	2	130
M2 (nfet)	2	130
M5 (pfet)	3	5
M6 (pfet)	3	5
M7 (pfet)	2	140
M8 (nfet)	2	5
M9 (nfet)	10	3

Table 8. Folding Stage Common Transistor Dimensions

2. Channel 7 Transistor M3/M4 Dimensions

Folding Stage	Length (microns)	Width (microns)
1	2	164
2	2	168
3	2	170
4	2	172
5	2	174
6	2	176
7	2	178
8	2	180
9	2	180
10	2	186
11	2	188
12	2	192
13	2	196
14	2	200
15	2	204
16	2	208
17	2	212
18	2	216
19	2	220

Folding Stage	Length (microns)	Width (microns)
20	2	224
21	2	228
22	2	232
23	2	236
24	2	240
25	2	244
26	2	248
27	2	252
28	2	258
29	2	264
30	2	270
31	2	282
32	2	294
33	2	296
34	2	300
35	2	310
36	2	320
37	2	326
38	2	330

Table 9. Channel 7 Folding Circuit Transistor M3/M4 Dimensions

3. Channel 8 Transistor M3/M4 Dimensions

Folding Stage	Length (microns)	Width (microns)
1	2	132
2	2	134
3	2	136
4	2	138
5	2	140
6	2	142
7	2	144
8	2	144
9	2	150
10	2	152
11	2	154
12	2	156
13	2	158
14	2	160
15	2	162
16	2	164
17	2	166

Folding Stage	Length (microns)	Width (microns)
18	2	168
19	2	172
20	2	174
21	2	178
22	2	182
23	2	186
24	2	190
25	2	196
26	2	202
27	2	208
28	2	212
29	2	220
30	2	224
31	2	228
32	2	232
33	2	240

Table 10. Channel 8 Folding Circuit Transistor M3/M4 Dimensions

4. Channel 11 Transistor M3/M4 Dimensions

Folding Stage	Length (microns)	Width (microns)
1	2	68
2	2	68
3	2	69
4	2	70
5	2	72
6	2	74
7	2	76
8	2	78
9	2	80
10	2	82
11	2	84
12	2	86
13	2	88

Folding Stage	Length (microns)	Width (microns)
14	2	90
15.	2	92
16	2	94
17	2	98
18	2	100
19	2	102
20	2	104
21	2	106
22	2	110
23	2	116
24	2	122
25	2	128

Table 11. Channel 11 Folding Circuit Transistor M3/M4 Dimensions

B. SUMMING AMPLIFIER AND VOLTAGE SHIFTER

Transistor	Length (microns)	Width (microns)
M1 (nfet)	10	40
M2 (nfet)	10	40
M3 (pfet)	22	10
M4 (pfet)	22	10
M5 (pfet)	10	45
M6 (nfet)	10	10
M7 (nfet)	50	10
M8 (nfet)	10	10
M9 (pfet)	2	9
M10 (nfet)	2	5

Table 12. Summing Amplifier and Voltage Shifter Transistor Dimensions

APPENDIX B. FOLDING STAGE EXTRACTION

A. MAGIC EXTRACTION FILE FOR ONE FOLDING STAGE

```
timestamp 783362978
version 5.0
tech scmos
scale 1000 1000 100
resistclasses 38400 130400 25300 25300 49 33 2776000 3000000
node "Vout" 84 16 91 96 ndiff 26 22 0 0 0 0 0 0 0 0 0 0 0 0 0 0
node "8_48_68#" 1548 178 24 34 pdiff 25 20 490 154 190 88 0 0 644 262 0 0 0 0 0 0
node "C2" 2846 233 -9 70 ndiff 910 288 0 0 332 332 0 0 630 204 0 0 0 0 0 0
node "Vdd!" 4749 923 -16 70 ndc 1362 608 1570 346 0 0 0 0 2850 834 2936 620 0 0 0 0
node "8_10_276#" 2806 154 5 138 pc 340 146 25 20 389 368 0 0 259 170 219 158 0 0 0
0
node "C1" 436 100 52 168 ndiff 408 148 0 0 0 0 0 0 128 76 0 0 0 0 0 0
node "8_25_276#" 2806 155 -12 138 pc 340 146 25 20 389 368 0 0 254 160 333 234 0 0
0 0
node "Vss" 7949 71 -24 70 ppc 25 20 904 476 0 0 0 0 2008 670 756 214 0 0 0 0
node "Vin" 973 3 57 239 pc 0 0 0 0 162 162 0 0 0 0 0 0 0 0 0 0
node "GND!" 973 3 49 239 pc 0 0 0 0 162 162 0 0 0 0 0 0 0 0 0 0
cap "Vdd!" "C2" 31
cap "Vdd!" "8_48_68#" 2
cap "8_25_276#" "C1" 1
cap "Vss" "Vdd!" 2
cap "8_25_276#" "8_10_276#" 1
cap "C1" "8_10_276#" 1
cap "Vss" "8_48_68#" 6
fet pfet 24 32 25 33 140 144 "Vdd!" "C2" 4 0 "Vdd!" 70 0 "8_48_68#" 70 0
fet pfet 24 41 25 42 140 144 "Vdd!" "C2" 4 0 "8_48_68#" 70 0 "Vdd!" 70 0
fet nfet 42 87 43 88 10 14 "GND!" "8_48_68#" 4 0 "8_48_68#" 5 0 "Vss" 5 0
fet nfet 81 96 82 97 30 26 "GND!" "8_48_68#" 20 0 "Vdd!" 3 0 "Vout" 3 0
fet pfet 93 134 94 135 15 16 "Vdd!" "8_10_276#" 6 0 "Vdd!" 5 0 "8_10_276#" 5 0
fet pfet 84 134 85 135 15 16 "Vdd!" "8_25_276#" 6 0 "8_25_276#" 5 0 "Vdd!" 5 0
fet nfet 15 70 16 71 130 134 "GND!" "8_10_276#" 4 0 "C2" 65 0 "Vdd!" 65 0
fet nfet 6 70 7 71 130 134 "GND!" "8_10_276#" 4 0 "Vdd!" 65 0 "C2" 65 0
fet nfet -2 70 -1 71 130 134 "GND!" "8_25_276#" 4 0 "C2" 65 0 "Vdd!" 65 0
fet nfet -11 70 -10 71 130 134 "GND!" "8_25_276#" 4 0 "Vdd!" 65 0 "C2" 65 0
fet nfet 58 168 59 169 136 140 "GND!" "Vin" 4 0 "C1" 68 0 "8_10_276#" 68 0
fet nfet 50 168 51 169 136 140 "GND!" "GND!" 4 0 "8_25_276#" 68 0 "C1" 68 0
```

B. EXT2SPICE EXTRACTION FILE CONVERSION

```
** SPICE file created for circuit extf1
** Technology: scmos
**
** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M0 100 0 101 0 nfet L=2.0U W=68.0U
M1 102 103 100 0 nfet L=2.0U W=68.0U
M2 104 101 1 0 nfet L=2.0U W=65.0U
M3 1 101 104 0 nfet L=2.0U W=65.0U
M4 104 102 1 0 nfet L=2.0U W=65.0U
M5 1 102 104 0 nfet L=2.0U W=65.0U
M6 1 101 101 1 pfet L=3.0U W=5.0U
M7 102 102 1 1 pfet L=3.0U W=5.0U
M8 105 106 1 0 nfet L=10.0U W=3.0U
M9 107 106 106 0 nfet L=2.0U W=5.0U
M10 1 104 106 1 pfet L=2.0U W=70.0U
M11 106 104 1 1 pfet L=2.0U W=70.0U
C0 105 0 16F
** NODE: 105 = Vout
C1 106 0 178F
** NODE: 106 = 8_48_68#
C2 104 0 233F
** NODE: 104 = C2
C3 1 0 923F
** NODE: 1 = Vdd!
C4 102 0 154F
** NODE: 102 = 8_10_276#
C5 100 0 100F
** NODE: 100 = C1
C6 101 0 155F
** NODE: 101 = 8_25_276#
C7 107 0 71F
** NODE: 107 = Vss
** NODE: 103 = Vin
** NODE: 0 = GND!
```

C. SPICE FILE READY FOR SIMULATION

```
* SPICE3C PMOS and NMOS model level 2 corner parameters for
* the VLSI Technology 2.0U CMOS N-well process.  10/23/92
* SPICE3C PMOS and NMOS model level 2 nominal parameters,
* derived from corner parameters above.

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10 NSUB=6.0E+15
+ XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5 UEXP=0.29 VMAX=3.0E4
+ NEFF=2.65 DELTA=1.0 RSH=101 CGSO=1.9E-10 CGDO=1.9E-10
+ CJ=250U CJSW=350P MJ=0.535 MJSW=0.34 PB=0.8)

.MODEL nnf NMOS(LEVEL=2 VTO=+0.775 TOX=400E-10 NSUB=8.0E+15
+ XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5 UEXP=0.125 VMAX=5.1E4
+ NEFF=4.0 DELTA=1.4 RSH=36 CGSO=1.95E-10 CGDO=1.95E-10
+ CJ=195U CJSW=500P MJ=0.76 MJSW=0.30 PB=0.8)

*Sources
Vdd  1   0  18V
Vss  107 0 -18V

*Input signal
Vin  103 0 PWL 0 0.0V, 1 15.0V

** SPICE file created for circuit extf1
** Technology: scmos
**
** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M0 100 0 101 107 nnf L=2.0U W=68.0U
M1 102 103 100 107 nnf L=2.0U W=68.0U
M2 104 101 1 107 nnf L=2.0U W=65.0U
M3 1 101 104 107 nnf L=2.0U W=65.0U
M4 104 102 1 107 nnf L=2.0U W=65.0U
M5 1 102 104 107 nnf L=2.0U W=65.0U
M6 1 101 101 1 npf L=3.0U W=5.0U
M7 102 102 1 1 npf L=3.0U W=5.0U
M8 105 106 1 107 nnf L=10.0U W=3.0U
M9 107 106 106 107 nnf L=2.0U W=5.0U
M10 1 104 106 1 npf L=2.0U W=70.0U
M11 106 104 1 1 npf L=2.0U W=70.0U
```

```
C0 105 0 16F
** NODE: 105 = Vout
C1 106 0 178F
** NODE: 106 = 8_48_68#
C2 104 0 233F
** NODE: 104 = C2
C3 1 0 923F
** NODE: 1 = Vdd!
C4 102 0 154F
** NODE: 102 = 8_10_276#
C5 100 0 100F
** NODE: 100 = C1
C6 101 0 155F
** NODE: 101 = 8_25_276#
C7 107 0 71F
** NODE: 107 = Vss
** NODE: 103 = Vin
** NODE: 0 = GND!

****Simulation Parameters********

.option dcon=1 post probe

.probe tran V(103) V(105)

.tran .5ms 1s

.end
```

APPENDIX C. SPICE LEVEL 2 PARAMETERS

A. VLSI TECHNOLOGY SPICE LEVEL 2 PARAMETERS

```
* SPICE3C PMOS and NMOS model level 2 nominal parameters for
* the VLSI Technology 2.0U CMOS N-well process. 10/23/92

.MODEL nnf NMOS(LEVEL=2 VTO=+0.775 TOX=400E-10 NSUB=8.0E+15
+ XJ=0.15U LD=0.20U U0=650 UCRIT=0.62E5 UEXP=0.125 VMAX=5.1E4
+ NEFF=4.0 DELTA=1.4 RSH=36 CGSO=1.95E-10 CGDO=1.95E-10
+ CJ=195U CJSW=500P MJ=0.76 MJSW=0.30 PB=0.8)

.MODEL npf PMOS(LEVEL=2 VTO=-0.75 TOX=400E-10 NSUB=6.0E+15
+ XJ=0.05U LD=0.20U U0=255 UCRIT=0.86E5 UEXP=0.29 VMAX=3.0E4
+ NEFF=2.65 DELTA=1.0 RSH=101 CGSO=1.9E-10 CGDO=1.9E-10
+ CJ=250U CJSW=350P MJ=0.535 MJSW=0.34 PB=0.8)
```

B. ORBIT SPICE LEVEL 2 FOUR CORNER PARAMETERS

1. PMOS Maximum and NMOS Maximum Parameters

```
*SPICE3C PMOS and NMOS model level 2 corner parameters for
*the ORBIT 2.0U CMOS N-well process.

.MODEL nnf NMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
+TPG=1 VTO=1.0 DELTA=6.6420E+00 LD=2.4870E-07 KP=2.6E-05
+ UO=562.8 UEXP=1.5270E-01 UCRIT=7.7040E+04 RSH=2.4000E+01
+ GAMMA=0.35 NSUB=4.0880E+15 NFS=1.980E+11 NEFF=1.0000E+00
+VMAX=5.8030E+04 LAMBDA=3.1840E-02 CGDO=3.1306E-10 CGSO=3.1306E-10
+ CGBO=4.3449E-10 CJ=9.5711E-05 MJ=0.7817 CJSW=5.0429E-10
+ MJSW=0.346510 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -5.4940E-07

.MODEL npf PMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
+TPG=-1 VTO=-0.5 DELTA=5.75400E+00 LD=3.0910E-07 KP=8.5E-06
+ UO=203.1 UEXP=2.1320E-01 UCRIT=8.0280E+04 RSH=5.677E+01
+ GAMMA=0.65 NSUB=8.1610E+15 NFS=3.270E+11 NEFF=1.5000E+00
+VMAX=9.9990E+05 LAMBDA=4.5120E-02 CGDO=3.9050E-10 CGSO=3.9050E-10
+ CGBO=4.1280E-10 CJ=3.2437E-04 MJ=0.5637 CJSW=3.3912E-10
+ MJSW=0.275876 PB=0.800000
```

* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.1580E-07

2. PMOS Maximum and NMOS Minimum Parameters

*SPICE3C PMOS and NMOS model level 2 corner parameters for
*the ORBIT 2.0U CMOS N-well process.

.MODEL nnf NMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
+TPG=1 VTO=0.5 DELTA=6.6420E+00 LD=2.4870E-07 KP=2.0E-05
+ UO=562.8 UEXP=1.5270E-01 UCRIT=7.7040E+04 RSH=2.4000E+01
+ GAMMA=0.15 NSUB=4.0880E+15 NFS=1.980E+11 NEFF=1.0000E+00
+VMAX=5.8030E+04 LAMBDA=3.1840E-02 CGDO=3.1306E-10 CGSO=3.1306E-10
+ CGBO=4.3449E-10 CJ=9.5711E-05 MJ=0.7817 CJSW=5.0429E-10
+ MJSW=0.346510 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -5.4940E-07

.MODEL npf PMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
+TPG=-1 VTO=-0.5 DELTA=5.75400E+00 LD=3.0910E-07 KP=8.5E-06
+ UO=203.1 UEXP=2.1320E-01 UCRIT=8.0280E+04 RSH=5.677E+01
+ GAMMA=0.65 NSUB=8.1610E+15 NFS=3.270E+11 NEFF=1.5000E+00
+VMAX=9.9990E+05 LAMBDA=4.5120E-02 CGDO=3.9050E-10 CGSO=3.9050E-10
+ CGBO=4.1280E-10 CJ=3.2437E-04 MJ=0.5637 CJSW=3.3912E-10
+ MJSW=0.275876 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.1580E-07

3. PMOS Minimum and NMOS Maximum Parameters

*SPICE3C PMOS and NMOS model level 2 corner parameters for
*the ORBIT 2.0U CMOS N-well process.

.MODEL nnf NMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
+TPG=1 VTO=1.0 DELTA=6.6420E+00 LD=2.4870E-07 KP=2.6E-05
+ UO=562.8 UEXP=1.5270E-01 UCRIT=7.7040E+04 RSH=2.4000E+01
+ GAMMA=0.35 NSUB=4.0880E+15 NFS=1.980E+11 NEFF=1.0000E+00
+VMAX=5.8030E+04 LAMBDA=3.1840E-02 CGDO=3.1306E-10 CGSO=3.1306E-10
+ CGBO=4.3449E-10 CJ=9.5711E-05 MJ=0.7817 CJSW=5.0429E-10
+ MJSW=0.346510 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -5.4940E-07

.MODEL npf PMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
+TPG=-1 VTO=-1.0 DELTA=5.75400E+00 LD=3.0910E-07 KP=6.0E-06
+ UO=203.1 UEXP=2.1320E-01 UCRIT=8.0280E+04 RSH=5.677E+01
+ GAMMA=0.45 NSUB=8.1610E+15 NFS=3.270E+11 NEFF=1.5000E+00
+VMAX=9.9990E+05 LAMBDA=4.5120E-02 CGDO=3.9050E-10 CGSO=3.9050E-10
+ CGBO=4.1280E-10 CJ=3.2437E-04 MJ=0.5637 CJSW=3.3912E-10
+ MJSW=0.275876 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.1580E-07

4. PMOS Minimum and NMOS Minimum Parameters

*SPICE3C PMOS and NMOS model level 2 corner parameters for
*the ORBIT 2.0U CMOS N-well process.

MODEL nnf NMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
+TPG=1 VTO=0.5 DELTA=6.6420E+00 LD=2.4870E-07 KP=2.0E-05
+ UO=562.8 UEXP=1.5270E-01 UCRIT=7.7040E+04 RSH=2.4000E+01
+ GAMMA=0.15 NSUB=4.0880E+15 NFS=1.980E+11 NEFF=1.0000E+00
+VMAX=5.8030E+04 LAMBDA=3.1840E-02 CGDO=3.1306E-10 CGSO=3.1306E-10
+ CGBO=4.3449E-10 CJ=9.5711E-05 MJ=0.7817 CJSW=5.0429E-10
+ MJSW=0.346510 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -5.4940E-07

.MODEL npf PMOS LEVEL=2 PHI=0.600000 TOX=4.1000E-08 XJ=0.200000U
+TPG=-1 VTO=-1.0 DELTA=5.75400E+00 LD=3.0910E-07 KP=6.0E-06
+ UO=203.1 UEXP=2.1320E-01 UCRIT=8.0280E+04 RSH=5.677E+01
+ GAMMA=0.45 NSUB=8.1610E+15 NFS=3.270E+11 NEFF=1.5000E+00
+VMAX=9.9990E+05 LAMBDA=4.5120E-02 CGDO=3.9050E-10 CGSO=3.9050E-10
+ CGBO=4.1280E-10 CJ=3.2437E-04 MJ=0.5637 CJSW=3.3912E-10
+ MJSW=0.275876 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.1580E-07

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