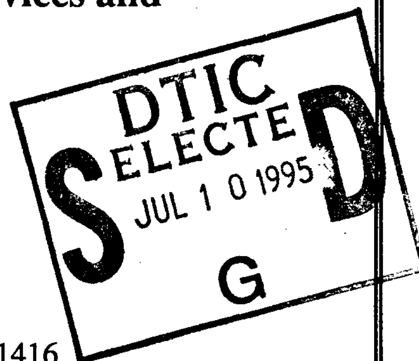
Semiannual Technical Report

Atomic Layer Epitaxy of Group IV Materials: Surface Processes, Thin Films, Devices and Their Characterization



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13. ABSTRACT *(Maximum 200 words)*

The ALE technique has been employed to deposit monocrystalline 3C-SiC thin films at 860±10°C. Wafers containing heterojunction bipolar transistor structures have been completely processed and characterized. No transistor activity was detected in any of the HBT structures. Electrical characterization of the emitter-base and collector-base junctions revealed rudimentary rectifying behavior, indicating that the base region of the completed HBT structures was too thick for transistor activity. $CoSi_2$ films have been electron beam evaporated onto Si <100> surfaces to study this material as a substrate for diamond deposition. The $CoSi_2$ film was characterized with LEED, AES depth profiling, quantitative XPS and TEM. Diamond films were subsequently grown upon the $CoSi_2$ surface using Microwave Plasma CVD. SEM was used to evaluate the resulting diamond films in terms of particle morphology and orientation. As-grown CeO_2 epitaxial films on Si(100) exhibited poor electrical and structural properties. Post growth oxidation anneals in argon followed or proceeded by oxygen environments improved both properties. However, the anneals in oxygen also resulted in the growth of an SiO_2 layer at the silicon interface which reduced the capacitance of the structure. An expression for the optimum oxidation time, τ, was developed as a function of the initial thicknesses of the deposited film.

14. SUBJECT TERMS
ALE, atomic layer epitaxy, SiC, silicon carbide, HBTs, transistor activity, $CoSi_2$ films, diamond films, particle morphology, orientation, CeO_2, oxidation, annealing

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Table of Contents

I. Introduction 1

II. Atomic Layer Epitaxy of Silicon Carbide Films and Their Application in the Development of Bipolar Transistors 4
J. Sumakeris and R. F. Davis

III. Oxidation Process and the Prediction of the Optimum Oxidation Time of $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si(111)$ 12
M. Tomita, A. H. Morshed, N. A. El-Masry and S. M. Bedair

IV. Electrical and Structural Properties of Annealed Epitaxial CeO_2 Films on Si(111) 22
A. H. Morshed and S. M. Bedair

V. Cobalt Disilicide as a Potential Diamond Substrate 28
P. Goeller, D. Tucker and J. T. Glass

VI. Distribution List 37

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I. Introduction

Atomic layer epitaxy (ALE) is the sequential chemisorption of one or more elemental species or complexes within a time period or chemical environment in which only one monolayer of each species is chemisorbed on the surface of the growing film in each period of the sequence. The excess of a given reactant which is in the gas phase or only physisorbed is purged from the substrate surface region before this surface is exposed to a subsequent reactant. This latter reactant chemisorbs and undergoes reaction with the first reactant on the substrate surface resulting in the formation of a solid film. There are essentially two types of ALE which, for convenience, shall be called Type I and Type II.

In its early development in Finland, the Type I growth scenario frequently involved the deposition of more than one monolayer of the given species. However, at that time, ALE was considered possible only in those materials wherein the bond energies between like metal species and like nonmetal species were each less than that of the metal-nonmetal combination. Thus, even if multiple monolayers of a given element were produced, the material in excess of one monolayer could be sublimed by increasing the temperature and/or waiting for a sufficient period of time under vacuum. Under these chemical constraints, materials such as GaAs were initially thought to be improbable since the Ga-Ga bond strength exceeds that of the GaAs bond strength. However, the self-limiting layer-by-layer deposition of this material proved to be an early example of Type II ALE wherein the trimethylgallium (TMG) chemisorbed to the growing surface and effectively prevented additional adsorption of the incoming metalorganic molecules. The introduction of As, however caused an exchange with the chemisorbed TMG such that a gaseous side product was removed from the growing surface. Two alternating molecular species are also frequently used such that chemisorption of each species occurs sequentially and is accompanied by extraction, abstraction and exchange reactions to produce self-limiting layer-by-layer growth of an element, solid solution or a compound.

The Type II approach has been used primarily for growth of II–VI compounds[1–13]; however, recent studies have shown that it is also applicable for oxides[14–17], nitrides [18], III–V GaAs-based semiconductors[19–32] and silicon[33–35]. The advantages of ALE include monolayer thickness control, growth of abrupt interfaces, growth of uniform and graded solid solutions with controlled composition, reduction in macroscopic defects and uniform coverage over large areas. A commercial application which makes use of the last attribute is large area electroluminescent displays produced from II–VI materials. Two comprehensive reviews[36,6], one limited overview[37] and a book[38] devoted entirely to the subject of ALE have recently been published.

In this reporting period, investigations concerned with (1) deposition via ALE of 3C-SiC films and the fabrication and characterization of bipolar transistors on these films, (2) nucleation, growth via microwave plasma CVD and SEM characterization of oriented

diamond particles on deposited $CoSi_2$ thin film substrates and (3) the deposition and oxidation of CeO_2 epitaxial films on Si(100) have been conducted.

The following sections introduce each topic, detail the experimental approaches, report the results to date and provide a discussion and a conclusion for each material. Each major section is self-contained with its own figures, tables and references.

References

1. T. Suntola and J. Antson, U.S. Patent 4,058,430, 1977.
2. M. Ahonen, M. Pessa and T. Suntola, Thin Solid Films **65**, 301, 1980.
3. M. Pessa, R. Makela, and T. Suntola, Appl. Phys. Lett. **38**, 131, 1981.
4. T. Yao and T. Takeda, Appl. Phys. Lett. **48**, 160, 1986.
5. T. Yao, T. Takeda, and T. Watanuki, Appl. Phys. Lett. **48**, 1615, 1986.
6. T. Yao, Jpn. J. Appl. Phys. **25**, L544, 1986.
7. T. Yao and T. Takeda, J. Cryst. Growth **81**, 43, 1987.
8. M. Pessa, P. Huttunen and M. A. Herman, J. Appl. Phys. **54**, 6047, 1983.
9. C. H. L. Goodman and M. V. Pessa, J. Appl. Phys. **60**, R65, 1986.
10. M. A. Herman, M. Valli and M. Pessa, J. Cryst. Growth **73**, 403, 1985.
11. V. P. Tanninen, M. Oikkonen and T. Tuomi, Phys. Status Solidi **A67**, 573, 1981.
12. V. P. Tanninen, M. Oikkonen and T. Tuomi, Thin Solid Films **90**, 283, 1983.
13. D. Theis, H. Oppolzer, G. Etchinghaus and S. Schild, J. Cryst. Growth **63**, 47, 1983.
14. S. Lin, J. Electrochm. Soc. **122**, 1405, 1975.
15. H. Antson, M. Leskela, L. Niinisto, E. Nykanen and M. Tammenmaa, Kem.-Kemi **12**, 11, 1985.
16. R. Tornqvist, Ref. 57 in the bibliography of Chapt. 1 of Ref. 38 of this report.
17. M. Ylilammi, M. Sc. Thesis, Helsinki Univ. of Technology, Espoo, 1979.
18. I. Suni, Ref. 66 in the bibliography of Chapt. 1 of Ref. 38 in this report.
19. S. M. Bedair, M. A. Tischler, T. Katsuyama and N. A. El-Masry, Appl. Phys. Lett. **47**, 51, 1985.
20. M. A. Tischler and S. M. Bedair **48**, 1681, 1986.
21. M. A. Tischler and S. M. Bedair, J. Cryst. Growth **77**, 89, 1986.
22. M. A. Tischler, N. G. Anderson and S. M. Bedair, Appl. Phys. Lett. **49**, 1199, 1986.
23. M. A. Tischler, N. G. Anderson, R. M. Kolbas and S. M. Bedair, Appl. Phys. Lett. **50**, 1266, 1987.
24. B. T. McDermott, N. A. El-Masry, M. A. Tischler and S. M. Bedair, Appl. Phys. Lett. **51**, 1830, 1987.
25. M. A. Tischler, N. G. Anderson, R. M. Kolbas and S. M. Bedair, SPIE Growth Comp. Semicond. **796**, 170, 1987.
26. S. M. Bedair in Compound Semiconductor Growth Processing and Devices for the 1990's, Gainesville, FL, 137, 1987.
27. J. Nishizawa, H. Abe and T. Kurabayashi, J. Electrochem. Soc. **132**, 1197, 1985.
28. M. Nishizawa, T. Kurabayashi, H. Abe, and N. Sakurai, J. Electrochm. Soc. **134**, 945, 1987.
29. P. D. Dapkus in Ref. 27, in the bibliography of Chapt. 1 of Ref. 38 in this report.
30. S. P. Denbaars, C. A. Beyler, A. Hariz and P. D. Dapkus, Appl. Phys. Lett. **51**, 1530, 1987.
31. M. Razeghi, Ph. Maurel, F. Omnes and J. Nagle, Appl. Phys. Lett. **51**, 2216, 1987.
32. M. Ozeki, K. Mochizuki, N. Ohtsuka and K. Kodama, J. Vac. Sci. Technol. **B5**, 1184, 1987.
33. Y. Suda, D. Lubben, T. Motooka and J. Greene, J. Vac. Sci. Technol. **B7**, 1171, 1989.
34. J. Nishizawa, K. Aoki, S. Suzuki and K. Kikuchi, J. Cryst. Growth **99**, 502, 1990.
35. T. Tanaka, T. Fukuda, Y. Nagasawa, S. Miyazaki and M. Hirose, Appl. Phys. Lett. **56**, 1445, 1990.

36. T. Suntola and J. Hyvarinen, Ann. Rev. Mater. Sci. **25**, 177, 1985.
37. M. Simpson and P. Smith, Chem. Brit. **23**, 37, 1987.
38. T. Suntola and M. Simpson, *Atomic Layer Epitaxy*, Chapman and Hall, New York, 1990.

II. Atomic Layer Epitaxy of Silicon Carbide Films and Their Application in the Development of Bipolar Transistors

A. Introduction

The utilization of active β-SiC components in semiconductor structures could dramatically enhance the performance of integrated circuits and discrete devices. Two convenient, standard criteria for comparing the relative merits and capabilities of semiconductor materials are the Johnson's and Keye's figures of merit. The Johnson's figure of merit estimates the maximum performance to be expected of a semiconductor material in discrete bipolar transistors[1] while the Keye's rating assesses a material's suitability for high density integrated circuit applications[2]. β-SiC ranks far above Si in both criteria, with ratings 33.9 and 5.82 times higher than Si by the Johnson's and Keye's figures of merit, respectively. Although these ratings for β-SiC demonstrate that both discrete devices and integrated circuitry employing β-SiC components should attain levels of performance unachievable with device technologies based solely on Si, relatively few devices containing β-SiC components have been produced[4,5].

A significant barrier to the widespread exploitation of the capabilities of β-SiC is the lack of an advanced β-SiC processing infrastructure. The most expeditious route to devices accessing the performance increases possible with β-SiC would be the development of a thin-film deposition technique to allow the integration of β-SiC into the existing Si device fabrication infrastructure. Conventional chemical vapor deposition (CVD) techniques for producing heteroepitaxial β-SiC films on Si wafers require a carbonizing pretreatment and high deposition temperatures[6]. These requirements make β-SiC CVD processes incompatible with existing Si sub-micron architecture process routes. However, as shown in a previous report (June, 1994), atomic layer epitaxy offers the ability to deposit monocrystalline β-SiC films on Si(100) substrates at low temperatures without the carbonizing pretreatment and may serve as a vehicle to facilitate the introduction of β-SiC into selected devices structures.

The objective of this research is to extend the state-of-the-art regarding SiC thin film deposition and application via the employment of atomic layer epitaxy to deposit β-SiC films on select substrates. During this reporting period, work has continued with the fabrication of trenched heterojunction bipolar transistors (HBTs) employing a wide bandgap β-SiC emitter. The second batch of transistors has been completely processed. The following sections describe the fabrication steps followed in this work and the results of characterization of the resultant devices via electrical measurements and scanning electron microscopy (SEM).

B. Experimental Procedure

ALE Reactor. The ALE reactor employed in this research has not been significantly modified since it was described in detail in a previous report (June, 1993). To prevent mixing

of process gases, flowing Ar "curtains" divide the reactor into four radial quadrants through which isolated fluxes of Si_2H_6, C_2H_4, NH_3 and triethylaluminum ($Al(C_2H_5)_3$) may flow. The quadrant containing NH_3 also contains a W filament that may be heated to produce atomic hydrogen or to crack NH_3 depending on gas flow conditions. During deposition, heated samples can be rotated alternately between quadrants and exposed to the species present to form films in a layer-by-layer process. Due to the construction of the reactor, SiC films can be deposited and doped n- and p-type with N and Al, respectively.

Fabrication of Trenched HBTs. The six level mask system designed to produce HBTs was described in detail in a previous report (June, 1994). Each die contained four transistors: a planar HBT, two HBTs in trench structures and one HBT with a corrugated or "waffle iron" structure. The geometry of the latter devices were engineered to exploit the high degree of conformality possible with layer-by-layer deposited SiC films. The procedures followed in producing the devices are explained in detail in the last report (December, 1994).

Deposition. SiC films were deposited on partially processed wafers. Three samples, HBT 6–HBT 8, were processed under the conditions listed in Table I. Prior to etching of the SiC to define the emitters, the thickness of each film was determined via cross-sectional SEM observation.

Table I. SiC Deposition Conditions for Second Batch of HBTs

Process parameter	HBT 6	HBT 7	HBT 8
Sample temperature	850° C	870° C	850° C
Si_2H_6 flow/ H_2 carrier	0.8 / 300 sccm	0.8 sccm/ 300 sccm	2
C_2H_4 flow/ H_2 carrier	2 / 200 sccm	2 sccm/ 200 sccm	2
Ar curtain flow	200 sccm	200 sccm	0 sccm
H_2 across filament	100 sccm	100 sccm	3 sccm
Filament temperature	1700°C	1700° C	unheated
Pressure	1.5 Torr	1.5 Torr	$\approx 10^{-3}$ Torr
Rotational scheme	rotate through Si_2H_6 and C_2H_4, wait under fil. 30 s. rpt. 1500 times.	rotate continuously to complete one Si-C-fil. cycle every 13 s. rpt. 3000 times	5 s. under Si_2H_6, 5 s. under H_2, 5 s. under C_2H_4, 5 s. under H_2 rpt. 1100 times.
Film thickness	0.18 μm	0.32 μm	0.2 μm

Ni Contacts (N-Type SiC). Ni contacts were sputtered onto the films using a photolithography lift-off technique. The specifics of the lift-off technique were discussed in detail in a previous report (June, 1994). Sputtering conditions were power = 100 watts 13.56 MHz R.F. and 20 mTorr Ar ambient. The Ni deposition rate was ≈ 2000 Å/Hr. Contacts were then annealed in a Heatpulse rapid thermal annealer (RTA) with an Ar ambient at 1000° C for 20 sec.

Al Contacts (P-type Si). Al contacts were vacuum evaporated from pure Al shot (99.9999% pure). The deposited Al film was subsequently processed using conventional microelectronic fabrication techniques.

Electrical Characterization. I-V and I_C vs. V_{CE} characterizations were performed with a Hewlett Packard 4145A Semiconductor Parameter Analyzer. Ambient light was found to have a significant effect on measured factors, therefore, all data was collected under dark conditions. Typical contact points are indicated in Fig. 1. Emitter and base connections for testing were made with W probes while the collector contact was made with a large area silver paint electrode on the wafer backside after grinding.

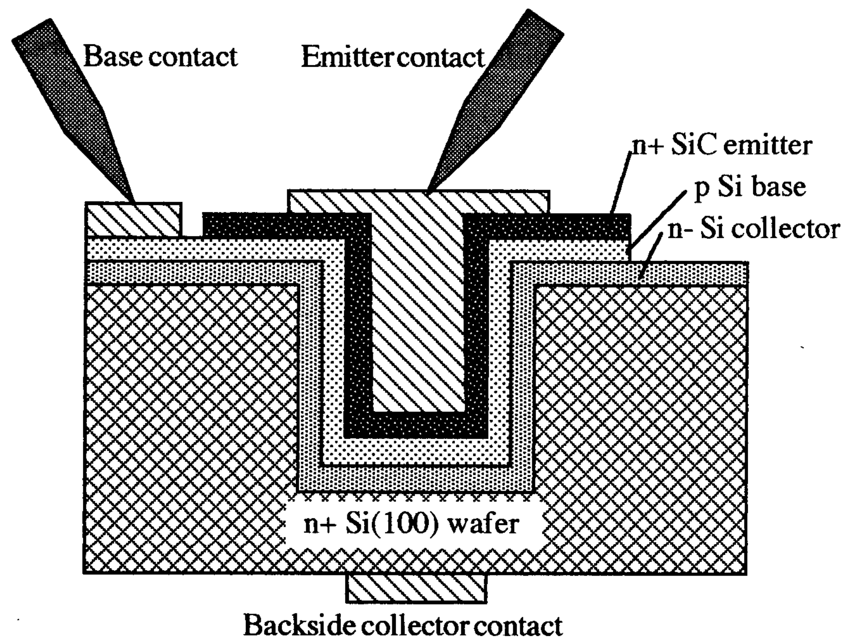
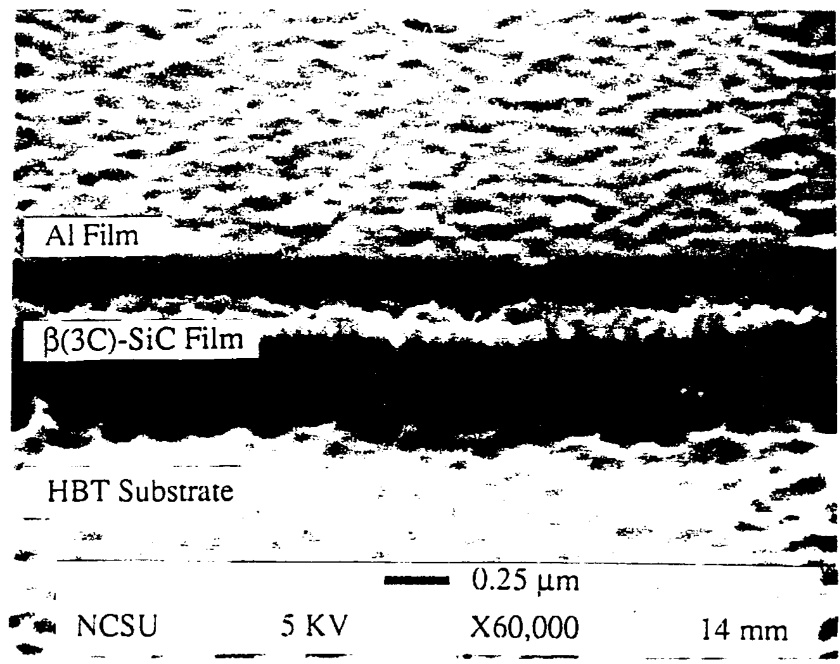


Figure 1. Testing contacts for electrical characterization of HBTs.

C. Results

The wafers in the second batch of HBT structures were denoted as: HBT 6, HBT 7 and HBT 8. The conditions under which the SiC films were deposited on these samples are tabulated in Table I. In general, these SiC films were thinner than those produced in the first batch of HBT structures in order to lessen the required accuracy of the SiC etch step.

Figure 2 is a SEM image of wafer HBT 6 taken after the SiC etch. The Al layer used to mask the SiC is visible in the image. There was some over-etching of the p-type Si base region on this wafer. The roughening of the Si surface is visible, although under-cutting of the emitter region is visible, it is not as excessive as reported previously (December, 1994). The excess etching in Fig. 2 is of the order of only 0.1 μm and did not result in the total removal of the base region which had an initial thickness of ≈ 1.5 μm.



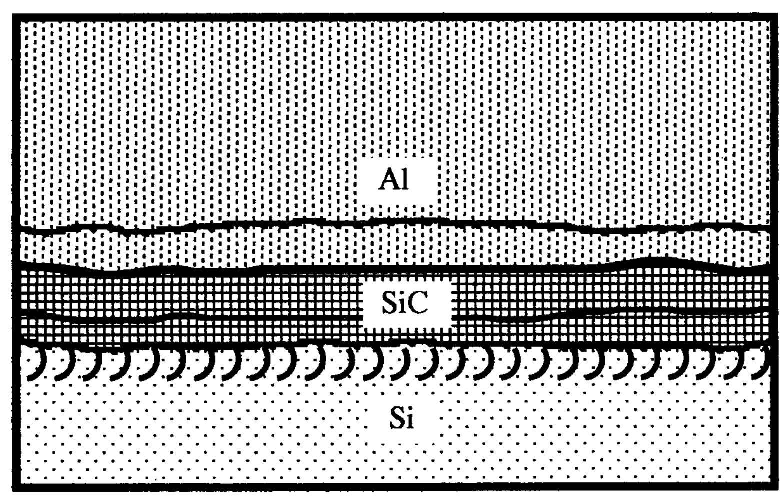


Figure 2. Wafer HBT 6 after etching of the SiC emitter layer.

Figures 3 and 4 are I-V curves generated across the emitter-base and the base-collector junctions, respectively, of a typical corrugated interface transistor on wafer HBT 6. Both junctions exhibited rectifying behavior. However, the emitter-base junction characterized in Fig. 3 was very leaky in reverse bias. This device had an active area of 28,700 μm^2, yielding a

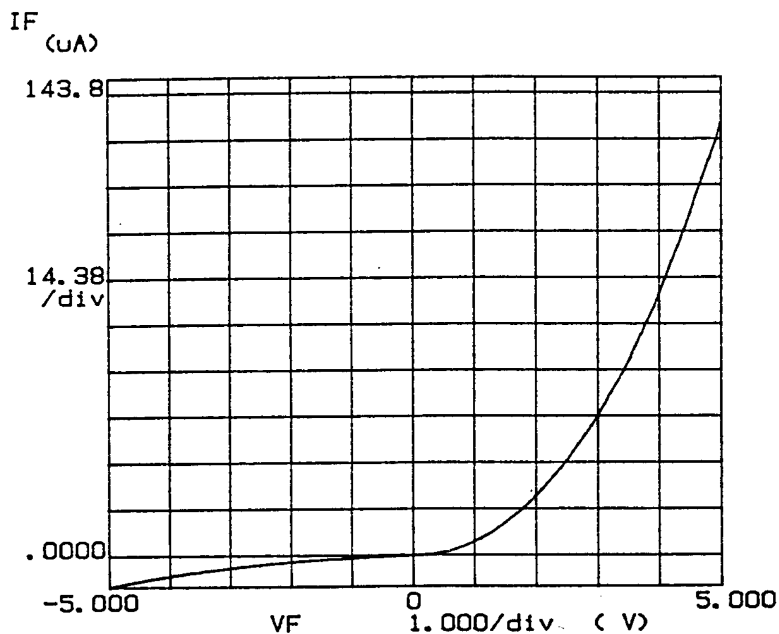


Figure 3. I-V characteristics of emitter-base junction of corrugated HBT on wafer HBT 6.

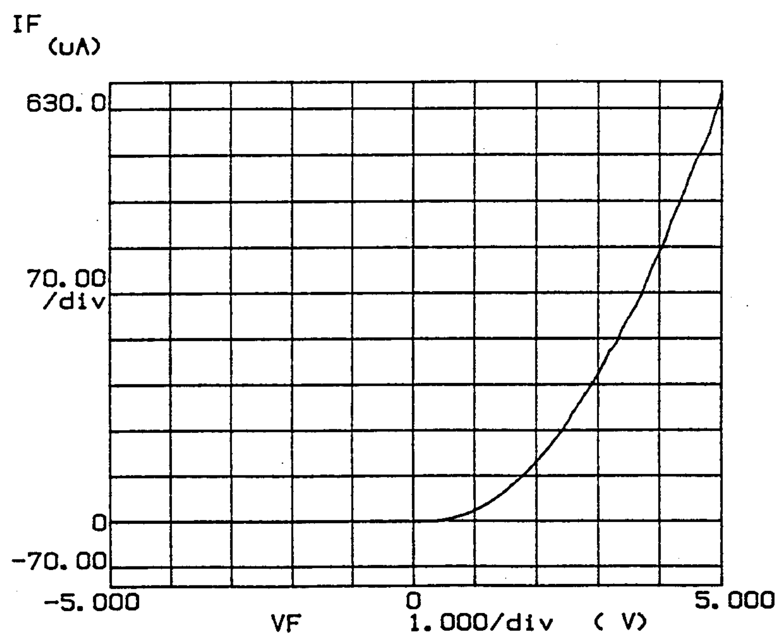


Figure 4. I-V characteristics of base-collector junction of corrugated HBT of wafer HBT 6.

reverse bias current density of 110 A cm^{-2} at -4.5 V. Good rectifying behavior across the base-collector junction and rectifying, but leaky behavior across the emitter-base junction were consistently observed on all three wafers of the second batch.

Figure 5 is a typical I_C vs. V_{CE} performance plot for a corrugated interface HBT on wafer HBT 6. In this plot I_C is determined as V_{CE} is varied from 0 to 5V while I_B is increased in 1 mA increments from 0 mA to 4 mA, yielding five separate curves. From this plot, there is no apparent gain in the transistors as I_C increases in each step by almost exactly the same value I_B increases. This behavior is similar to that observed for the transistors produces in the first batch of HBTs. Transistor activity was not observed in any of the devices produced in the second batch of HBTs.

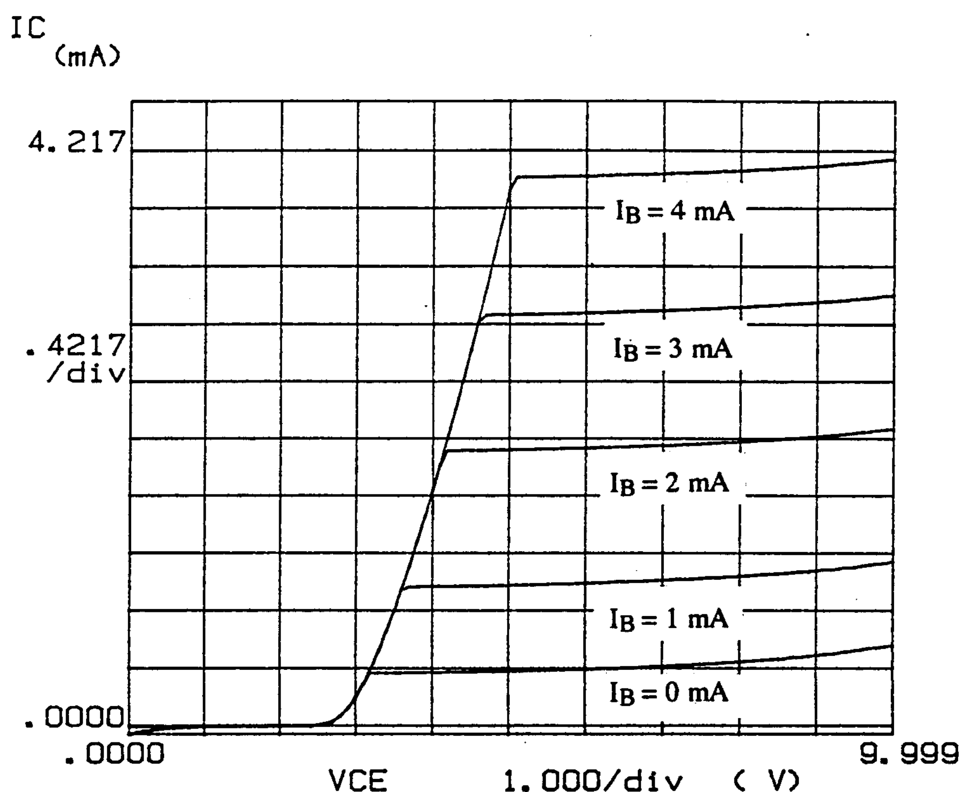


Figure 5. Typical I_C vs. V_{CE} behavior of a typical corrugated surface HBT in the second HBT batch at several I_B values.

D. Discussion

No transistor activity was observed in the second batch of HBTs. Two possible causes for the lack of performance were identified in the analysis of the first batch of HBTs: inaccurate etching of the SiC film deposited to form the emitters and too wide a base region. Examination of the wafers produced in the second batch after etching the SiC revealed that the etching was

performed accurately, removing all of the undesired SiC while only slightly etching the underlying p-type Si base region. The most probable cause of the absence of transistor activity was an excessive width of the base region.

Bipolar transistors usually operate by injecting minority carriers into the base region by forward biasing the emitter-base junction. If the minority carrier diffusion distance in the base is greater than the distance to the reverse biased base-collector junction, these carriers will eventually reach the collector region to contribute to I_C. However, if the base region is too wide for the carriers to transverse before recombining, the transistor becomes essentially two diodes sharing a common terminal. This was apparently the root flaw of the HBT structures developed in this work.

The collector and base regions of the HBT structures studied here were deposited by a commercial contractor. A spreading resistance profile of the deposited layers is presented in Fig. 6. Both the base region (p-type) and the collector region (lightly n-type) were much thicker than ordered. This is due to the complication of carrier migration during deposition. As these films were deposited at ≈1300°C, abrupt changes in carrier concentration are not possible

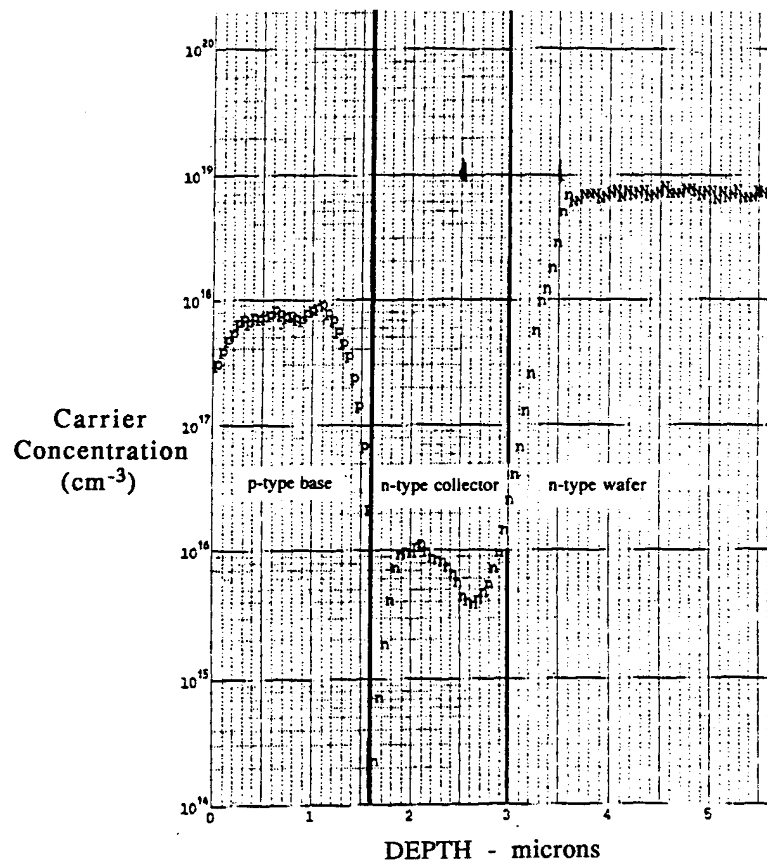


Figure 6. Spreading resistance profile of base and collector regions.

due to the diffusion of donors and acceptors. As a consequence, thicker films are necessary to achieve a relatively constant dopant level.

E. Conclusions

The second batch of devices was processed with thinner SiC films, reducing the required precision of the etching process. SEM examination of the second set of wafers indicated that the SiC was etched appropriately. However, none of the wafers in this second batch contained operational devices either. Electrical characterization of the latter devices revealed rectifying behavior at both the emitter-base and the base-collector junction. An excessive base width is hypothesized to be responsible for the lack of transistor behavior in the device structures. Due to the base region width, injected carriers recombined before reaching the base-collector junction. As a result, the transistors actually behaved as two independent p-n junctions that shared a p-terminal contact. Although a batch of devices with a thinner base region may have succeeded, this project was terminated.

F. Acknowledgements

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G. References

1. E. O. Johnson, RCA Rev. **26**, 163, 1965.
2. R. W. Keyes, Proc. IEEE **60**, 225, 1972.
3. *Handbook of Chemistry and Physics* , Editor-in-Chief D. R. Lide, CRC Press, 72nd ed., 1991-1992.
4. R. F. Davis, Physica B **185**, 1, 1993.
5. R. F. Davis, J. W. Palmour and J. A. Edmond, Mat. Res. Soc. Symp. Proc. **162**, 463, 1990.
6. H. P. Liaw and R. F. Davis, J. Electrochem. Soc. **131** 3014, 1984.

III. Oxidation Process and the Prediction of the Optimum Oxidation Time of $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si(111)$

A. Introduction

Cerium oxide (CeO_2) is a crystalline insulator. It is a promising material to realize the silicon-on-insulator (SOI) structure because it has a CaF_2-type cubic structure which is nearly lattice matched to Si with high dielectric constant (~26). The lattice misfit ($\Delta a/a$) is only 0.35%[1]. These values are considerably better than the respective values for other crystalline insulators such as CaF_2, sapphire, and spinel[2-4].

As previously reported, CeO_2 on Si has two distinct amorphous regions at the interface and the electrical properties of this structure can be improved by post-annealing in dry oxygen ambient[5,6]. In other words, altering the film structure from $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ to $CeO_2/SiO_2/Si$ greatly enhances the electrical properties. Unfortunately, this oxidation of the as-grown films increases the thickness of SiO_2. It is desirable to keep the SiO_2 thickness as thin as possible to maintain a large total capacitance.

In this report, oxidation models will be established for both $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ and $CeO_2/SiO_2/Si$. The investigation will examine how to meet the optimum oxidation time in order to arrive at maximum capacitance without an $\alpha\text{-}CeO_{2-x}$ layer.

B. Experimental Procedure

CeO_2 thin films have been grown on Si substrates using a UHV laser ablation system[5,6]. The base pressure was kept 10^{-8} Torr during the growth. The growth temperature was ~700°C, and post-annealing in dry oxygen ambient was applied. Both as-grown and annealed films were evaluated by high resolution transmission electron microscopy (HRTEM), Rutherford Back Scattering (RBS), and capacitance-voltage (C-V) measurements. The thickness of each film was determined from the TEM images.

The post oxidation in dry oxygen was exactly the same procedure as the standard oxidation of Si. The oxidation temperature was 900°C, and the oxidation times were 18 and 35 minutes[6]. Table I shows the thickness changes due to the oxidation as measured by TEM. From the experimental data in Table I, the following was deduced:

i) Initially, the oxidation and the O_2-diffusion processes were used mainly in converting $\alpha\text{-}CeO_{2-x}$ to CeO_2, thus reducing x_1 to zero and increasing x_o to its maximum steady value, i.e. $x_o(final) = x_o(initial)+x_1(initial)$. This initial stage was expected to be carried out in time $t \approx \tau$, where τ in Table I was less than 18 minutes, as concluded from the TEM microstructure observation.

Table I. Experimental Data of Each Layer Thickness Before and After Oxidation

Oxidation time [min]	CeO_2 thickness x_o [Å]	α-CeO_{2-x} thickness x_1 [Å]	SiO_2 thickness x_2 [Å]
as-grown	181	37	26
18	218	0	70
35	218	0	192

ii) For $t < \tau$ the thickness of $SiO_2(x_2)$ did not change much from its initial value x_2(initial). This assumption was based in the smaller relative increase in SiO_2 layer thickness during the first 18 minutes of oxidation time relative to the next 17 minutes of further oxidation.

C. Diffusion Model

The calculations used in this study were based on the Deal-Grove oxidation model of SiO_2/Si structure[7]. This model was modified to study the O_2 diffusion in the CeO_2/SiO_2/Si structure and determine an expression for x_2 for $t > \tau$. The model was also expanded to consider the more complicated CeO_2/α-CeO_{2-x}/SiO_2/Si structure.

Oxidation for $CeO_2/SiO_2/Si(111)$. Figure 1 shows the O_2 concentration profiles and the fluxes considered in studying the O_2 diffusion process in the CeO_2/SiO_2/Si structure.

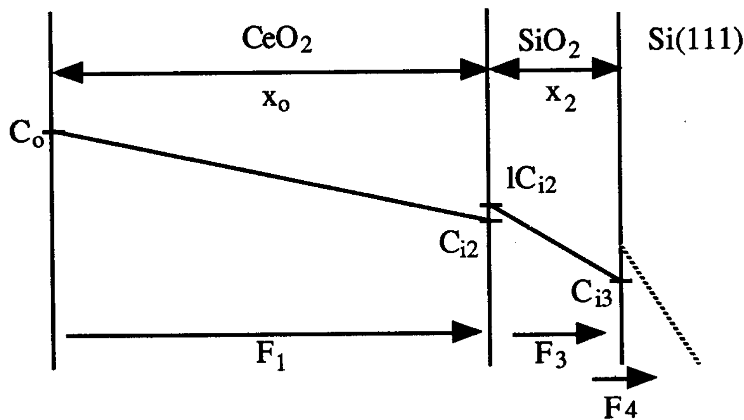


Figure 1. Schematic oxidation model for CeO_2/SiO_2/Si(111).

In this figure,

- x_o: thickness of CeO_2,
- x_2: thickness of SiO_2,
- F_1: oxygen flux in CeO_2,
- F_3: oxygen flux in SiO_2,
- F_4: oxygen flux through the SiO_2/Si interface,
- C_o: oxygen concentration at the CeO_2 surface,
- C_{i2}: oxygen concentration at the front surface of CeO_2/SiO_2 interface,
- C_{i3}: oxygen concentration at the SiO_2/Si interface, and
- l: segregation coefficient of oxygen at the CeO_2/SiO_2 interface.

The oxygen fluxes, $F_1 - F_4$, were as follows:

$$F_1 = D_o \frac{C_o - C_{i2}}{x_o},$$

$$F_3 = D_2 \frac{lC_{i2} - C_{i3}}{x_2},$$

$$F_4 = k_2 C_{i3},$$

where,

- D_o: diffusion constant of oxygen in CeO_2,
- D_2: diffusion constant of oxygen in SiO_2, and
- k_2: chemical reaction rate at SiO_2/Si interface.

Since the thickness of the Si substrate was too large compared with the other layers, the oxygen flux in Si substrate was almost zero. In the steady state of oxidation conditions, all the oxygen fluxes were equal, thus the oxygen concentration at SiO_2/Si, C_{i3}, was deduced from

$$C_{i3} = \frac{lC_o}{1 + \frac{lk_2 x_o}{D_o} + \frac{k_2 x_2}{D_2}}. \qquad (1)$$

The SiO_2 growth rate was generally given as:

$$\frac{dx_2}{dt} = \frac{F_3}{N_2} = \frac{k_2 C_{i3}}{N_2}, \qquad (2)$$

where,

N_2: the number of oxygen atoms incorporated into a unit volume of SiO_2.

Since x_o was assumed to be constant based on the experimental results, the integration of Eq. (2) with Eq. (1) led to the SiO_2 thickness as a function of time.

$$x_2 = \sqrt{\frac{2lD_2C_o}{N_2}(t-\tau) + \left(x_2^\tau + \frac{lD_2}{D_o} + \frac{D_2}{k_2}\right)^2} - \left(\frac{lD_2}{D_o} + \frac{D_2}{k_2}\right) \qquad (3)$$

The initial conditions used in Eq. (3) were as follows:

τ: oxidation time for the film structure to change from $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ to $CeO_2/SiO_2/Si$ (optimum oxidation time), and

x_2^τ: thickness of SiO_2 at $t = \tau$.

Equation (3) was valid for $t > \tau$. Using this solution and experimental data, the optimum oxidation time τ, i.e. the time required to recrystallize $\alpha\text{-}CeO_{2-x}$ without increasing the SiO_2 layer thickness, was deduced.

Oxidation for $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si(111)$. Figure 2 shows the schematic oxidation model for $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ with the same concept as the case above.

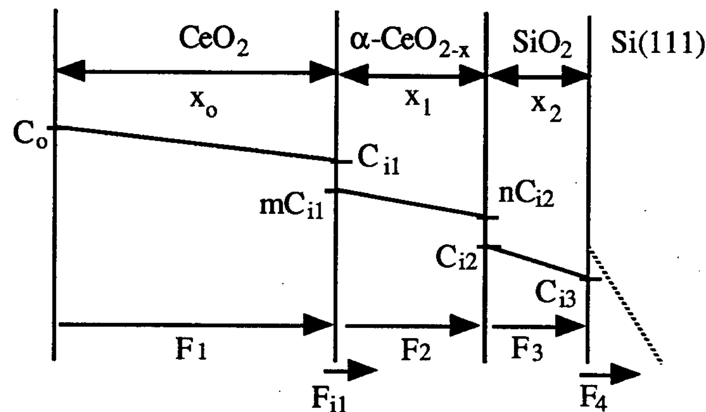


Figure 2. Schematic oxidation model for $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si(111)$.

The following extra parameters were used:

x_1: thickness of $\alpha\text{-}CeO_{2-x}$,

F_{i1}: oxygen flux at $CeO_2/\alpha\text{-}CeO_{2-x}$ interface,

F_2: oxygen flux in α-CeO_{2-x},

C_{i1}: oxygen concentration at the CeO_2/α-CeO_{2-x} interface,

m: segregation coefficient of oxygen at the CeO_2/α-CeO_{2-x} interface, and

n: segregation coefficient of oxygen at the α-CeO_{2-x}/SiO_2 interface.

The oxygen fluxes, $F_1 - F_4$, were as follows:

$$F_1 = D_o \frac{C_o - C_{i1}}{x_o}, \tag{4}$$

$$F_{i1} = k_1 C_{i1}, \tag{5}$$

$$F_2 = D_1 \frac{mC_{i1} - nC_{i2}}{x_1}, \tag{6}$$

$$F_3 = D_2 \frac{nC_{i2} - C_{i3}}{x_2}, \tag{7}$$

$$F_{i2} = k_2 C_{i3}, \tag{8}$$

where,

D_1: diffusion constant of oxygen in α-CeO_{2-x}, and

k_1: chemical reaction rate at CeO_2/α-CeO_{2-x} interface.

In the steady state oxidation conditions, the oxygen fluxes satisfied the following equations:

$$F_1 = F_{i1} + F_2, \tag{9}$$

and

$$F_2 = F_3 = F_4. \tag{10}$$

Substituting Eqs. (4)–(8) into Eqs. (9) and (10) gave

$$C_{i1} = \frac{C_o}{1 + \frac{k_1 x_o}{D_o} + \frac{mk_2 x_o / D_o}{k_2 x_1 / D_1 + n(1 + k_2 x_2 / D_2)}}, \tag{11}$$

and

$$C_{i3} = \frac{m}{\frac{k_2 x_1}{D_1} + n\left(1 + \frac{k_2 x_2}{D_2}\right)} \frac{C_o}{1 + \frac{k_1 x_o}{D_o} + \frac{mk_2 x_o / D_o}{k_2 x_1 / D_1 + n(1 + k_2 x_2 / D_2)}}. \tag{12}$$

The growth rates of CeO_2 and SiO_2 were as follows:

$$\frac{dx_o}{dt} = \frac{F_{i1}}{N_1} = \frac{k_1 C_{i1}}{N_1} \tag{13}$$

and

$$\frac{dx_2}{dt} = \frac{F_3}{N_2} = \frac{k_2 C_{i3}}{N_2}, \tag{2}$$

where,

N_1: the number of oxygen atoms incorporated into a unit volume of CeO_2.

Since the experimental data shown in Table I indicated that the sum of CeO_2 and α-CeO_{2-x} thicknesses did not change with oxidation, the thickness of α-CeO_{2-x} was given simply as

$$x_1 = x_0^{ini} + x_1^{ini} - x_0, \tag{14}$$

where,

x_0^{ini}: initial thickness of CeO_2, and

x_1^{ini}: initial thickness of α-CeO_{2-x}.

The differential Eqs. (13) and (2) had to be solved with Eqs. (11) and (12) in order to obtain CeO_2 and SiO_2 thicknesses as functions of time. However, the equations were too complex to solve mathematically. This research relied on an earlier assumption based on the data shown in Table I that most of the oxygen from the surface of CeO_2 was consumed at CeO_2/α-CeO_{2-x} interface. For $t<\tau$, this assumption seemed reasonable since the SiO_2 growth rate was much faster after the completion of α-CeO_{2-x} recrystallization ($t > \tau$) than before the completion ($t < \tau$). Using the oxidation models, this assumption was expressed as

$$F_{i1} \gg F_2 \tag{15}$$

and modified with Eqs. (7) and (8) as

$$k_1 \gg \frac{mk_2}{\frac{k_2 x_1}{D_1} + n\left(1 + \frac{k_2 x_2}{D_2}\right)}. \tag{15$'$}$$

Thus, Eqs. (11) and (12) were simplified as

$$C_{i1} \approx \frac{C_{\acute{o}}}{1 + k_1 x_o / D_o}, \tag{11$'$}$$

$$C_{i3} \ll \frac{k_1}{k_2} \frac{C_o}{1 + k_1 x_o / D_o},$$

and

$$k_2 C_{i3} \ll k_1 C_{i1}. \tag{12)'}$$

The CeO_2 thickness as a function of time was achieved by the integration of Eqs. (13) and (11)′:

$$x_o = \sqrt{\frac{2D_o C_o}{N_1} t + \left(x_o^{ini} + D_o / k_1\right)^2} - D_o / k_1. \tag{16}$$

Equation (12)′ implied that the SiO_2 growth was negligible while CeO_2 was growing by consuming the α-CeO_{2-x}. Thus,

$$x_2 = x_2^t = x_2^{ini} \quad \text{at } t < \tau, \tag{17}$$

where x_2^{ini} was the initial thickness of SiO_2 in the as-grown material.

Equations (14), (16), and (17) were valid for $t < \tau$. The optimum oxidation time τ was obtained from Eq. (16) with $x_0 = x_0^{ini} + x_1^{ini}$ as

$$\tau = \frac{N_1}{2D_o C_o} x_1^{ini}\left(2x_o^{ini} + x_1^{ini} + 2D_o / k_1\right). \tag{18}$$

By using this value τ, the optimum oxidation time for various initial thicknesses of CeO_2 and α-CeO_{2-x} was found. Since k_1 and C_o were unknown parameters, they were determined based on the experimental data as shown below.

D. Results and Considerations

The following physical constants were used in the above equations:

$D_o = 4.4 \times 10^{-9}$ cm^2/sec	Diffusion constant of oxygen in CeO_2[9],
$D_1 = 9.0 \times 10^{-8}$ cm^2/sec	Diffusion constant of oxygen in α-CeO_{2-x}[9],
$D_2 = 2.8 \times 10^{-9}$ cm^2/sec	Diffusion constant of oxygen in SiO_2[10],
$N_1 = 2.5 \times 10^{22}$ /cm^3	Quantity of Oxidant incorporated into CeO_2,
$N_2 = 2.2 \times 10^{22}$ /cm^3	Quantity of Oxidant incorporated into SiO_2, and
$k_2 = 2.2 \times 10^{-4}$ cm/sec	Chemical reaction rate of oxide formation at SiO_2/Si[7].

First, Eq. (3) was used with the data shown in Table I to obtain l, the segregation coefficient at the CeO_2/SiO_2 interface. Since Eq. (3) was valid for any $t > \tau$, data shown in Table I to obtain l was used and thus,

$$l = 2.7$$

was obtained.

In this report, $C_o = 6.0 \times 10^{16}\ /cm^3$ was used which is oxygen concentration at the SiO_2 surface[11]. Then, using Eqs. (3) and (17), τ was obtained as

$$\tau = 11.6 \text{ min.}$$

This was the average value of τ calculated with t = 18 minutes and t = 35 minutes. Finally, using Eq. (18) with this τ resulted in

$$k_1 = 2.5 \times 10^{-4} \text{ cm/sec.}$$

Since this value was so close to the one of SiO_2/Si, it suggested that the approximation which was applied was reasonable. Using these values, variation of thicknesses of each layer with oxidation time was calculated and is shown in Fig. 3.

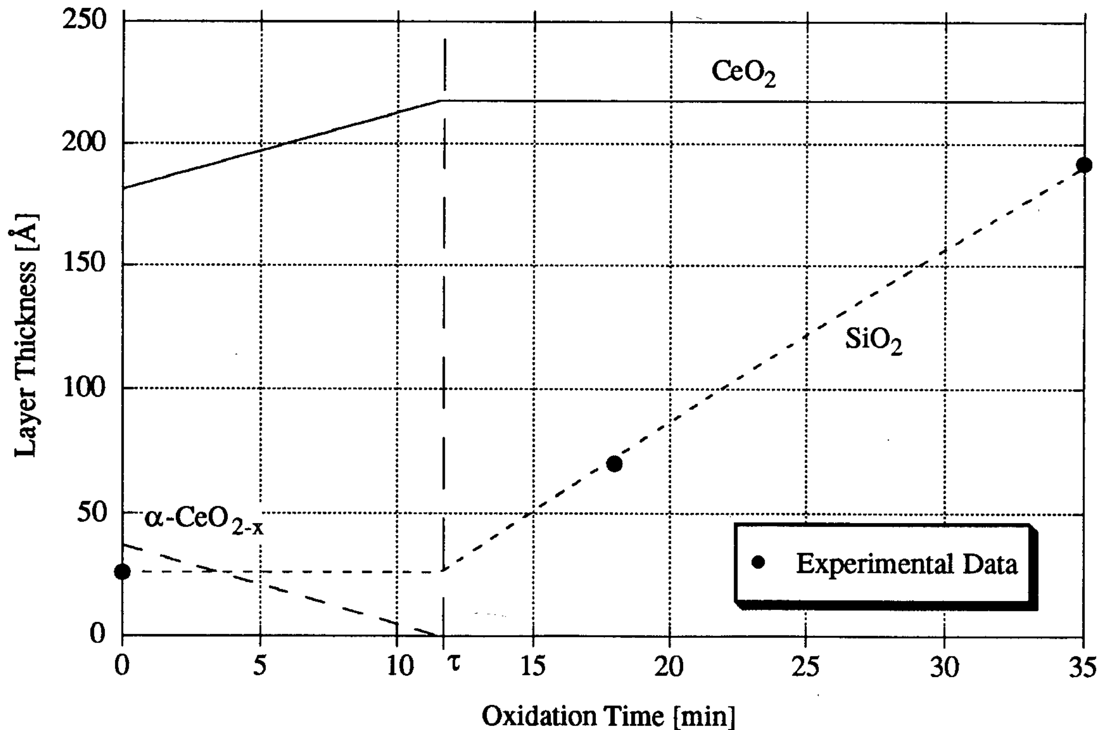


Figure 3. Time dependence of each layer thickness with oxidation as calculated by the approximation used in this report.

Data in Fig. 3 was obtained based on the approximation previously mentioned. However, the time dependence of thicknesses can also be obtained using fitting parameters by numerical calculation on Eqs. (11) and (12). The numerical approach can calculate SiO_2 growth during the recrystallization. Using the same parameters, the time dependence of thicknesses with fitting parameters m and n was obtained which was the segregation coefficients at the interfaces of $CeO_2/\alpha\text{-}CeO_{2-x}$ and $\alpha\text{-}CeO_{2-x}/SiO_2$, respectively. The results are shown in Fig. 4.

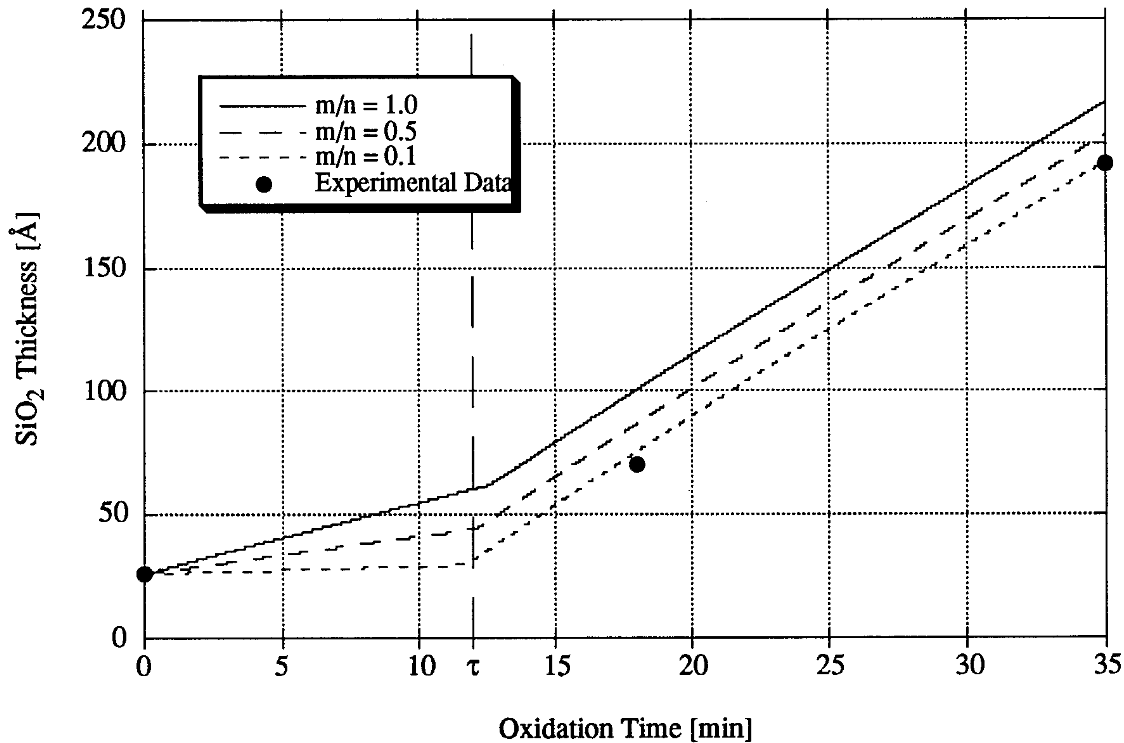


Figure 4. SiO_2 thickness changes with oxidation as calculated by the numerical calculation using m/n as fitting parameters.

From this figure, it was clear that if the ratio of m/n was close to zero, the calculation result closely reached that of the approximation based on experimental data. The large value of n was reasonable since $\alpha\text{-}CeO_{2-x}$ was eliminated much faster than SiO_2 growth. Other iteration can also be applied to the best fitting of data.

E. Conclusions

Oxidation models for $CeO_2/\alpha\text{-}CeO_{2-x}/SiO_2/Si$ and $CeO_2/SiO_2/Si$ are proposed in order to obtain optimum oxidation time τ which gives the $CeO_2/SiO_2/Si$ structure with the thinnest SiO_2 thickness. An expression for τ was developed as a function of the initial thickness of the deposited film. The numerical calculation results also indicated the validity of the assumption.

F. Future Plans and Goals

It is planned to use the above calculations to predict the optimum oxidation time for different initial CeO_2 deposited films and the use of TEM, RBS and C-V to confirm the validity of the above model.

G. References

1. T. Inoue, Y. Yamamoto, S. Koyama, S. Suzuki, and Y. Ueda, Appl. Phys. Lett. **56**, 1332, 1990.
2. T. Asano and H. Ishiwara, J. Appl. Phys. **55**, 3566, 1984.
3. M. Ishida, I. Katakabe, and T. Nakamura, Appl. Phys. Lett. **52**, 1326, 1988.
4. K. Egami, M. Mikami, and H. Tsuya, Appl. Phys. Lett. **43**, 757, 1983.
5. T. Chikyow, L. Tye, N. A. El-Masry, and S. M. Bedair, Appl. Phys. Lett. **65**, 1030, 1994.
6. L. Tye, T. Chikyow, N. A. El-Masry, and S. M. Bedair, Appl. Phys. Lett. **65**, 3081, 1994.
7. B. E. Deal and A. S. Grove, J. Appl. Phys. **36**, 3770, 1965.
8. Y. Takahashi, T. Ishiya, and M. Tabe, Appl. Phys. Lett. **65**, 2987, 1994.
9. B. C. Steele and J. M. Floyd, Proc. Brit. Ceram. Soc. **19**, 55, 1971.
10. S. M. Sze, *VLSI Technology*, McGraw Hill, 315, 1988.
11. F. J. Norton, Nature **171**, 701, 1961.

IV. Electrical and Structural Properties of Annealed Epitaxial CeO_2 Films on Si(111)

A. Introduction

CeO_2 films grown epitaxially on silicon are of interest for silicon on insulator (SOI) technology because of the closely lattice matched conditions (0.35%). CeO_2 also has a relatively high dielectric constant (~ 26), hence it is a candidate insulator for high density MOS memories[1-3]. The as-grown CeO_2 films have poor electrical and structural properties which were found to improve by oxygen annealing. This, however, results in the growth of a SiO_2 layer at the silicon interface which reduces the capacitance of the grown structure[2-5]. Annealing in argon and argon followed or proceeded by oxygen environments were investigated to improve the structural and electrical properties of the films while minimizing the intermediate SiO_2 layer thickness. The effect of annealing under different environments on the properties of the grown films is reported in the following.

B. Experimental Procedure

Epitaxial CeO_2 films were grown on Si(111) substrates by laser ablation of CeO_2 targets under ultra high vacuum conditions. They were post annealed in the following environments:

i) O_2 for 60 min. at 900°C,
ii) Ar for 60 min. at 900°C,
iii) Ar for 60 min. at 900°C followed by O_2 for 15 min. at 900°C,
iv) O_2 for 10 minutes at 900°C,
v) O_2 for 10 min at 900°C followed by Ar for 60 min. at 900°C, and
vi) O_2 for 10 min. at 900°C followed by Ar for 60 min. at 500°C.

Rutherford backscattering (RBS) measurements were made on samples with O_2 for 60 min. at 900°C, Ar for 60 min. at 900°C, and Ar for 60 min. at 900°C followed by O_2 for 15 min. at 900°C annealing. MOS capacitor structures were fabricated by evaporating aluminum dots onto the CeO_2 surface and the electrical properties of the films were investigated by C-V and I-V techniques.

C. Results and Discussion

Figure 1 shows RBS measurements done by Dr. N. P. Parikh at the Dept. of Physics and Astronomy, University of North Carolina at Chapel Hill. Figure 1(a) gives the RBS counts versus channel number of the sample annealed in O_2 for 60 min. at 900°C. The peaks in percentage counts indicated in the figure correspond to the CeO_2 surface (at channel # 400) and the CeO_2 / SiO_2 interface (at lower channel number). The lower percentage counts of ions

backscattered from the surface with alignment ($\chi = 27\%$) indicates better crystalline quality of the CeO_2 at the surface than the interface ($\chi = 44\%$). The same holds for the RBS data of the sample annealed in Ar for 60 min. at 900°C shown in Fig. 1(b) and Ar for 60 min. at 900°C

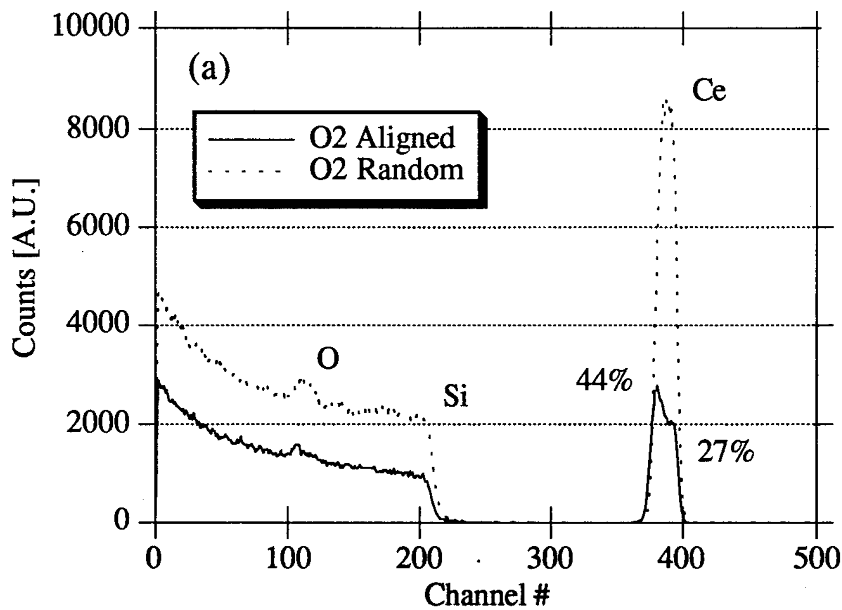


Fig. 1(a). RBS data of CeO_2 films annealed in O_2 for 60 min. at 900°C.

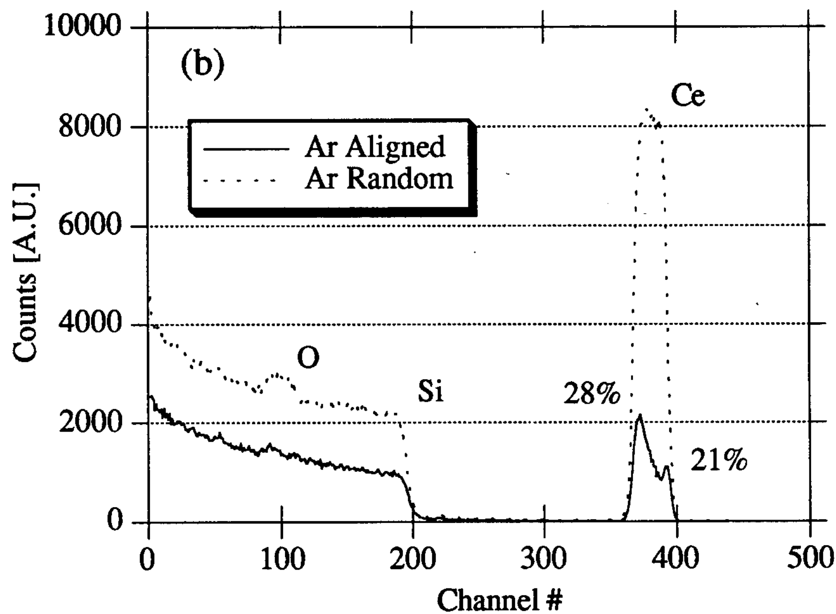


Fig. 1(b). RBS data of CeO_2 films annealed in Ar for 60 min at 900°C.

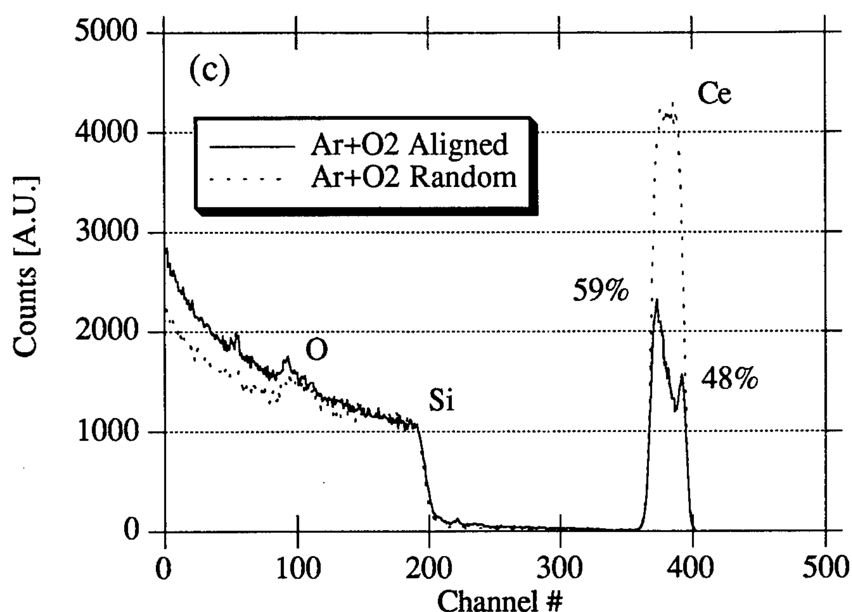
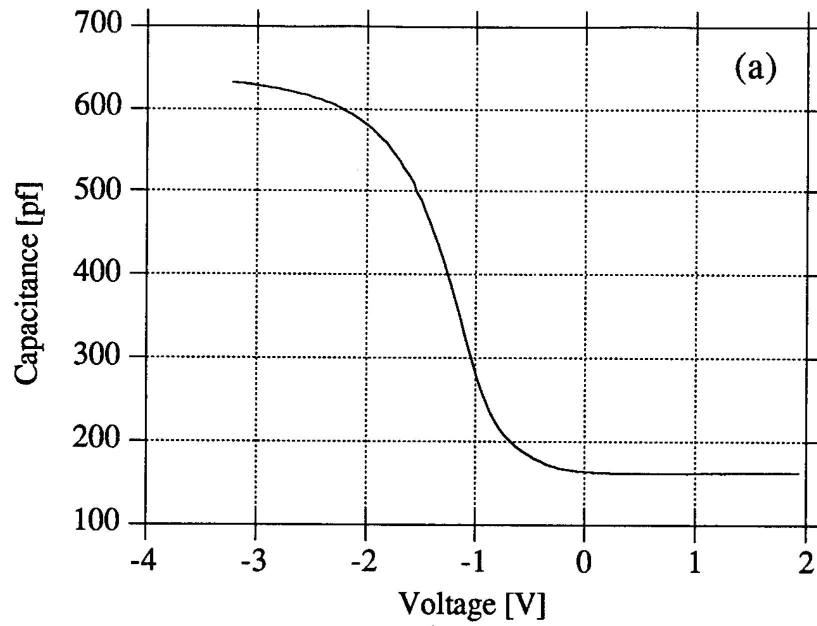


Fig. 1(c). RBS data of CeO_2 films annealed in Ar for 60 min. at 900°C followed by O_2 for 15 min. at 900°C

followed by O_2 for 15 min. at 900°C shown in Fig. 1(c). The figure indicates an improvement in the structural properties of the Ar annealed films (χmin= 21%) as compared to O_2 annealed (χmin= 27%) and Ar followed by O_2 annealed films (χmin= 48%). Argon annealed samples also exhibited generally larger breakdown voltages confirming the improvement of crystalline quality with the annealing.

Figure 2 shows typical high frequency C-V characteristics obtained with a Keithley 590 CV Analyser. A C-V curve obtained at 100KHz of films annealed in O_2 for 60 min. at 900°C is shown in Fig. 2(a) The curve is flat at positive voltages indicating inversion of the silicon surface. Fig. 2(b) shows a 1MHz C-V curve of films annealed in Ar for 60 min. at 900°C. While their accumulation capacitances were the largest indicating a minimal SiO_2 layer thickness, the C-V characteristics of these films did not exhibit inversion of the silicon surface. Instead, deep depletion was observed indicating a very large density of traps at the silicon interface.

All oxygen annealed samples showed inversion of the silicon surface as can be seen from Figs. 2(a), (c), and (d). Samples with short O_2 annealing (15 and 10 min., Figs. 2(c) and (d), respectively) had interface traps densities of the order 10^{-13} cm^{-2} whereas longer O_2 annealed sample (60 min., Fig. 2(a) had reduced interface traps densities of about 10^{-12} cm^{-2}. The accumulation capacitances of these were reduced due to more SiO_2 layer growth. Samples



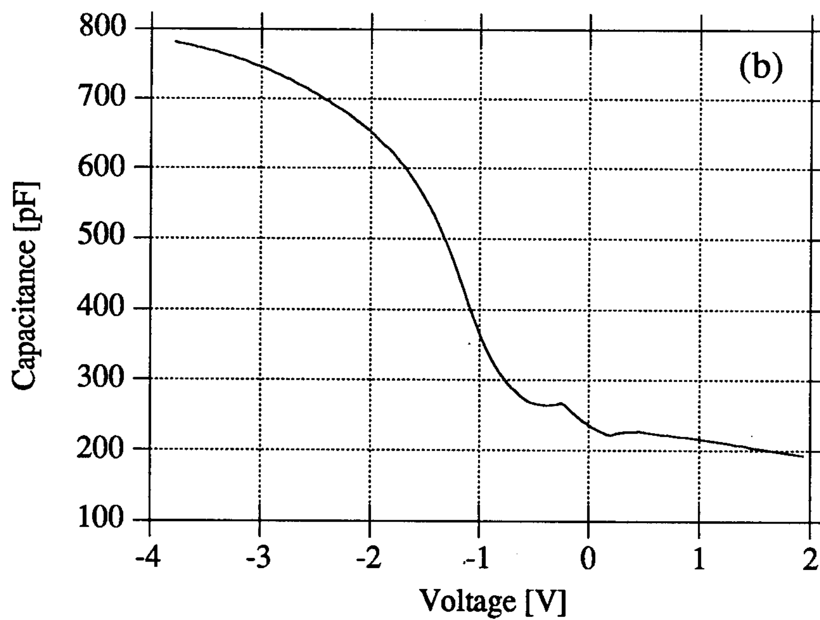
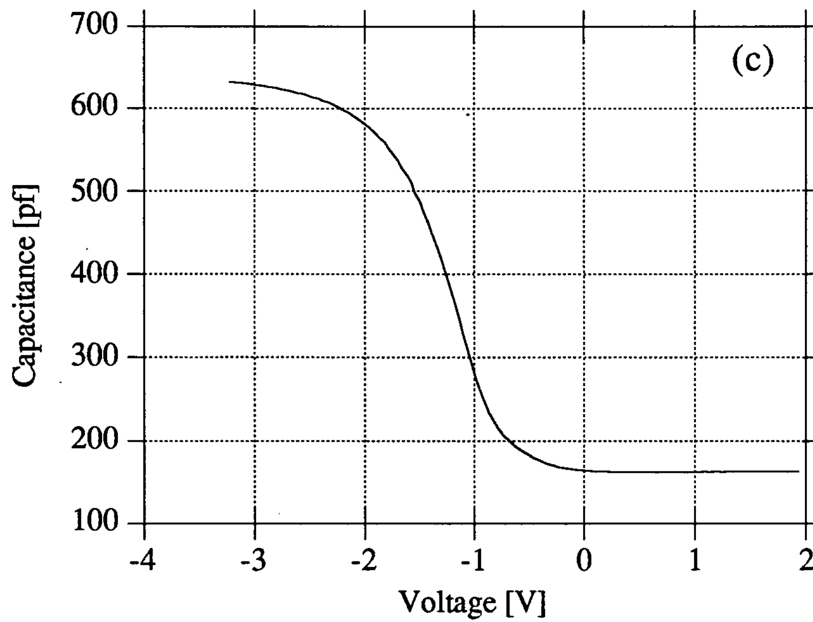


Figure 2. High frequency C-V curves of MOS capacitors with 35 mils diameter fabricated on CeO_2 films annealed in: (a) O_2 for 60 min. at 900°C, at a frequency of 100KHz; (b) Ar for 60 min at 900°C, at 1 MHz. Both with film thickness of about 900 Å.



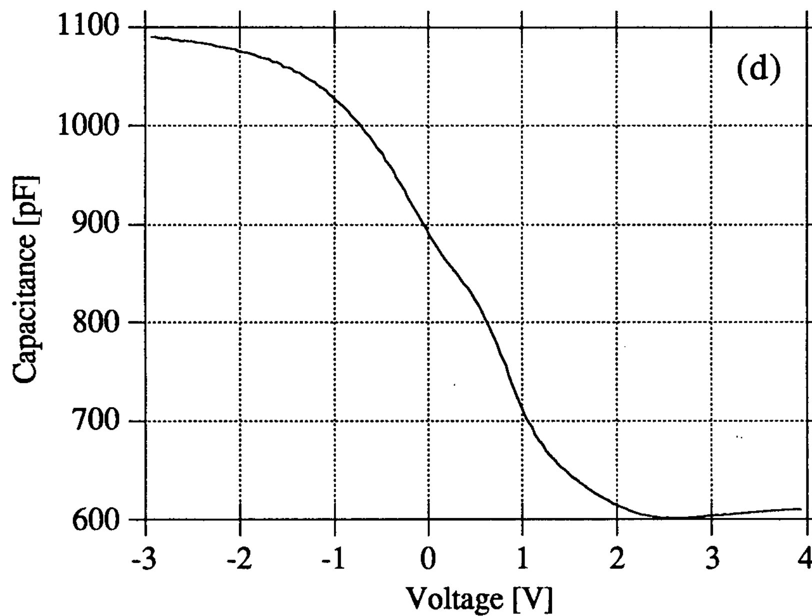


Figure 2. Con't. High frequency C-V curves of MOS capacitors with 35 mils diameter fabricated on CeO_2 films annealed in: (c) Ar for 60 min. at 900°C followed by O_2 for 15 min. at 900°C, at 1 MHz with film thickness of about 900 Å; and (d) O_2 for 10 min. at 900°C, at 100KHz with film thickness of about 400 Å.

annealed in oxygen followed by argon were excessively leaking and poor C-V curves were obtained. This was attributed to an initially very poor quality of their as grown films as these two were the only ones of the same deposition run.

The above data show that reduction of surface defects at the oxide / semiconductor interface for CeO_2 / SiO_2 / Si structure to achieve inversion of the silicon surface can be obtained with O_2 annealing for as short as 10 min. thus limiting the SiO_2 layer growth. A longer annealing time reduces the density of interface states at the cost of reducing the film capacitances for more SiO_2 growth.

D. Conclusions

A possibility of achieving device quality MOS structures of CeO_2 films on silicon exists. The optimal annealing conditions to cure the crystal and interface defects of grown films with minimal growth of SiO_2 at the silicon interface are still being investigated. Further studies of the properties of CeO_2 films require a nondestructive measurement of CeO_2 and SiO_2 layer thicknesses. Optical properties of CeO_2 films are, thus, being investigated.

E. Future Plans

Further optimization of the annealing conditions and growth of more CeO_2 material at different temperatures and growth rates to control SiO_2 layer thickness are to be carried out. Optical techniques can be used to measure the thickness of individual film layers and study the properties of the CeO_2 layers. Exploring the growth of silicon on top of CeO_2 and addressing growth on Si(100) substrates are planned.

F. References

1. T. Inoue, M. Osonoe, H. Tohda, M. Hiramatsu, Y. Yamamoto, A. Yamanaka and T. Nakayama, J. Appl. Phys. **69**, 8313, 1991.
2. T. Chikyow, L. Tye, N. El-Masry and S. Bedair, Appl. Phys. Lett. **65**, 1030, 1994.
3. L. Tye, T Chikyow, N. El-Masry and S. Bedair, Materials Research Society Spring Meeting, San Francisco, CA 1994.
4. L. Tye, N. El-Masry, T. Chikyow, P. McLarty and S. Bedair, Appl. Phys. Lett. **65**, 3081, 1994.
5. L. Tye, T. Chikyow, M. Tomita, N. El-Masry and S. Bedair, Electronic Materials Conference, Santa Barbara, CA, 1994.

* This report is a part of A. H. Morshed's Ph.D. Thesis.

V. Cobalt Disilicide as a Potential Diamond Substrate

A. Introduction

To realize the unique properties of diamond for many anticipated electronic and optical applications, two-dimensional single crystal films are essential. Nearly epitaxial diamond films have been grown on silicon, silicon carbide, nickel and most recently, cobalt[1-6]. One characteristic of nickel and cobalt which makes them highly advantageous for use as diamond substrates is that they are both closely lattice matched to diamond. A disadvantage to the use of cobalt and other transition metals as diamond substrates is that in their pure metallic state they have a high solubility for carbon and tend to catalyze the formation of graphite under diamond growth conditions. Even though this problem has been overcome on nickel and cobalt[5, 6], single crystalline diamond films are still not yet realized on these surfaces, possibly due to the fact that they are metallically bonded in contrast to diamond which is a covalently bonded material. Silicon is a well-known substrate material for obtaining oriented diamond nuclei, and silicon is a covalently bonded material sharing the same crystal structure as diamond. Cobalt disilicide has been investigated as a potential diamond substrate material in the present research since it contains the favorable bonding of silicon, but with a better lattice match to diamond than pure silicon. Cobalt disilicide is cubic with the fluorite structure. The silicon terminated (100) plane appears to have the most favorable lattice match with diamond; thus (100) single crystalline $CoSi_2$ was sought. Since bulk single crystal $CoSi_2$ is not generally available, methods for creating thin films of it on silicon were investigated.

Producing single crystal films of (100) oriented $CoSi_2$ on (100) Si substrates has proven to be difficult[7-11]. The resulting films have usually been polycrystalline with mixed (100) and (110) grains. A method of producing epitaxial (100) oriented $CoSi_2$ on Si (100) was recently described by Schowolter *et al*[8]. Co and Si were co-deposited onto Si (100) in a Co to Si ratio of 1 to 1.8. This slightly Co rich stoichiometry allowed some Co to diffuse into the Si substrate and form a Si/$CoSi_2$ interface below the substrate surface which inhibited the formation of the (110) oriented grains. The resulting epitaxial $CoSi_2$ film was entirely of the (100) orientation with a low density of pin holes.

B. Experimental Procedure

The method described above for preparing (100) $CoSi_2$ films was utilized in this work in an attempt to prepare an epitaxial (100) $CoSi_2$ film on Si (100) for use as a diamond substrate. As only a single electron gun evaporation system was available, a mixed Co-Si target was fabricated and the experiment attempted using this single source. Since the melting points and vapor pressures of Co and Si differ, activity data for the Co-Si system was consulted in order to determine the relative mole fractions of Co and Si required to make a mixed target that would

give a Co:Si vapor pressure ratio of 1:1.8. Fig. 1 shows the activity coefficients of Co and Si versus mole fraction at two different temperatures.

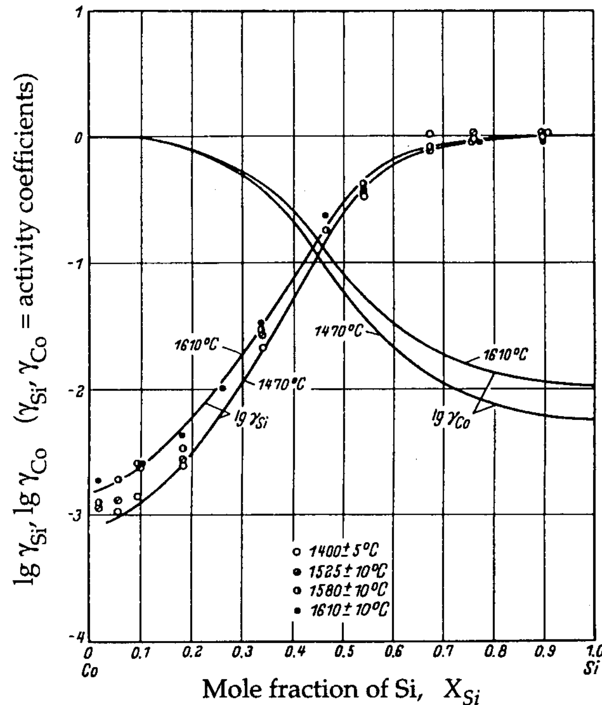


Figure 1. The logarithms of the activity coefficients of silicon and cobalt in the cobalt-silicon system[12].

Using the graph, the activities of Co and Si at any composition can be found from

$$\gamma_i = \frac{a_i}{X_i}$$

where γ_i is the activity coefficient, a_i is the activity and X_i is the mole fraction. The partial pressures of Co and Si can then be found using

$$a_i = \frac{p_i}{p_o}$$

where p_i is the partial pressure of component i in the mixture and p_o is the vapor pressure of the pure component i at the temperature of interest. The temperature was taken to be 1470 °C, which is close to the melting points of Co (1490 °C) and Si (1405 °C). The actual temperature of the target while it is molten during deposition is difficult to determine. Using values for the vapor pressures of pure Co and Si from the literature[13], the mole fractions of Co and Si necessary to give a p_{Si} to p_{Co} ratio of 1:1.8 could then be calculated. The results of the calculations are summarized in Table I.

Table I. Results of Calculations to Determine Co-Si Target Composition

	$\lg \gamma_i$	γ_i	a_i	p_o (Torr)	p_i (Torr)	X_i
Si	-0.420	0.380	0.202	7×10^{-4}	1.414×10^{-4}	0.53
Co	-1.35	0.045	0.021	3.65×10^{-3}	7.665×10^{-5}	0.47

The Si:Co partial pressure ratio is thus found to be $1.414 \times 10^{-4}/7.665 \times 10^{-5} = 1.84$ which is very close to 1.8. The mole fractions of Co and Si needed to give these partial pressures are 53% Si and 47% Co. A Co/Si target was then fabricated with this composition.

The target was then placed into the electron beam evaporation system. This system was a custom UHV assembly which consisted of a deposition chamber, load lock and LEED chamber. The deposition and LEED chambers were pumped with two Varian 60 l/s ion pumps and a Varian titanium sublimation pump. The base pressure of the system was 2×10^{-10} Torr while the maximum pressure during deposition was 2×10^{-8} Torr. The load lock was pumped with a Leybold 50 l/s turbomolecular pump. A Thermionics electron beam gun was employed for deposition. The e-gun and water cooled target holder are both mounted on a single $4\frac{5}{8}$" flange. An Inficon XTC vibrating crystal thickness monitor coupled to the e-gun power supply was used to control film thickness. Sample heating was accomplished with a pyrolytic boron nitride heater.

Characterization of the deposited $CoSi_2$ films was accomplished using LEED, quantitative XPS, AES depth profiling and TEM. LEED was performed *in situ*, while the other techniques required moving the sample to other systems. After characterization, the $CoSi_2$ films were exposed to diamond growth conditions using a microwave plasma CVD chamber. The resulting diamond films were characterized using SEM and compared to diamond films grown on bare Si <100> wafers in terms of particle morphology and orientation.

C. Results

Si <100> wafers were exposed to a 5 minute UV-ozone treatment prior to a spin etch[14] using alcohol and HF. The wafers were loaded within 20 minutes into a load lock and quickly brought down to the 10^{-6} Torr range and then transferred into the deposition chamber. The sample was heated to a temperature of 1000 °C for 10 minutes to thermally desorb the oxide. The sharp 2×1 LEED pattern obtained from the sample is shown in Fig. 2 (top). A shutter was placed between the sample and the $CoSi_{1.8}$ source while the source was brought to deposition

After 100 Å had been deposited, the source was turned off and the sample annealed at 800 °C for 30 minutes. A 2×2 LEED pattern resulted and is shown in Fig. 2 (bottom).

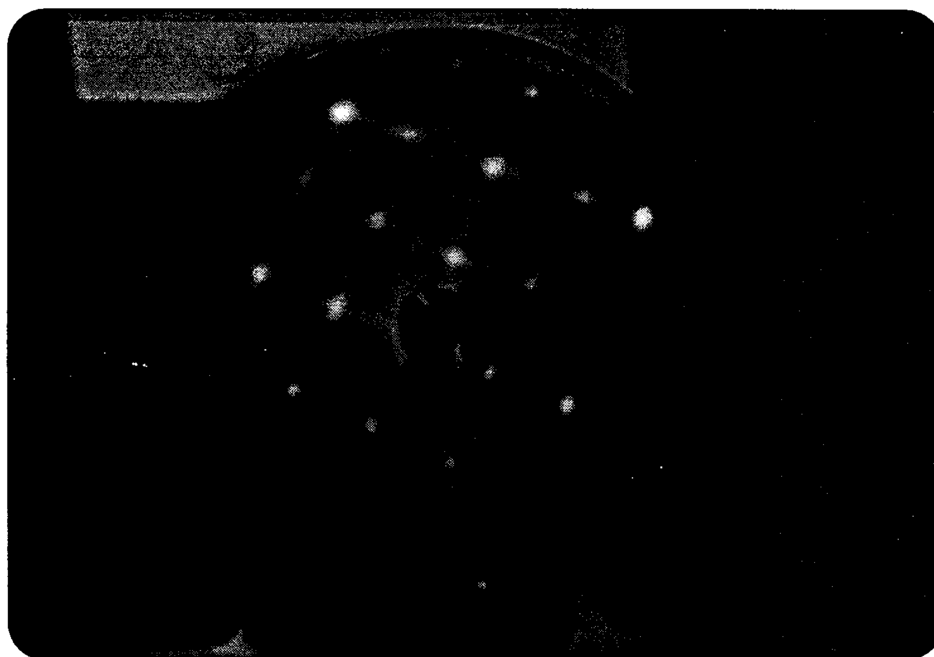


Figure 2. 2×1 LEED pattern of clean Si (top); 2×2 pattern after deposition of 100 Å $CoSi_2$ and annealing to 800 °C (bottom).

In order to assess the stoichiometry of the film, quantitative XPS was performed on the sample. After smoothing, the peak areas of the Si 2p and Co 3p peaks were determined and input into the following equation[15]:

$$\frac{X_{Si}}{X_{Co}} = \frac{I_{Si}}{I_{Co}} \bullet \frac{\sigma_{Co}}{\sigma_{Si}}$$

where X_{Si}, X_{Co} are the molar fractions of Si and Co; I_{Si} and I_{Co} are the peak areas of the Si 2p and Co 3p photoelectron peaks and σ_{Si}, σ_{Co} are the photoionization cross sections[16]. This method of determining concentrations assumes that the sample is flat and homogeneous, that the photoelectrons are emitted isotropically, and that the sample surface is clean without a layer of surface contamination. Using the above equation, the ratio of Si to Co at the surface of the film was determined to be 2.69, or 73% Si and 27% Co.

The scanning AES depth profile, shown in Fig. 3, indicated the relative concentrations of Si and Co at the surface to be approximately 72% Si and 28% Co.

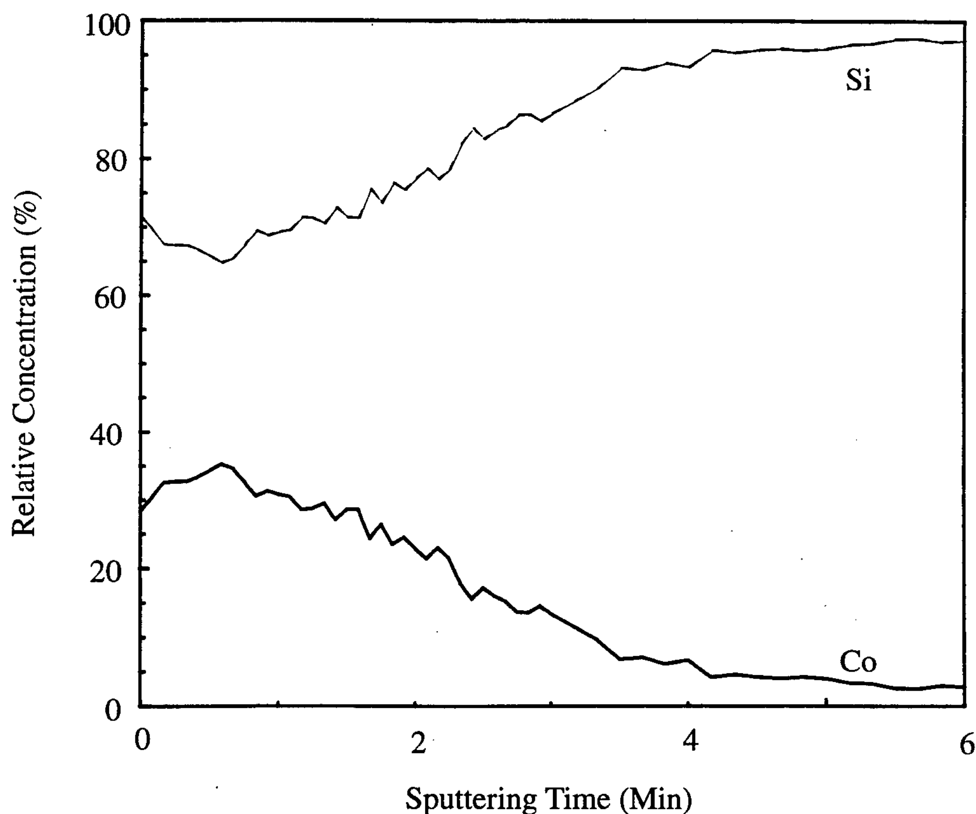


Figure 3. Scanning AES depth profile of $CoSi_2$ film.

Cross sectional TEM of the sample was performed. The bright field image, Fig. 4, shows the epitaxial orientation of the silicide layer. The micro diffraction pattern taken of the $CoSi_2$

layer (inset) indicates a single crystalline material with a [011] zone axis; consistent with a [001] oriented film.

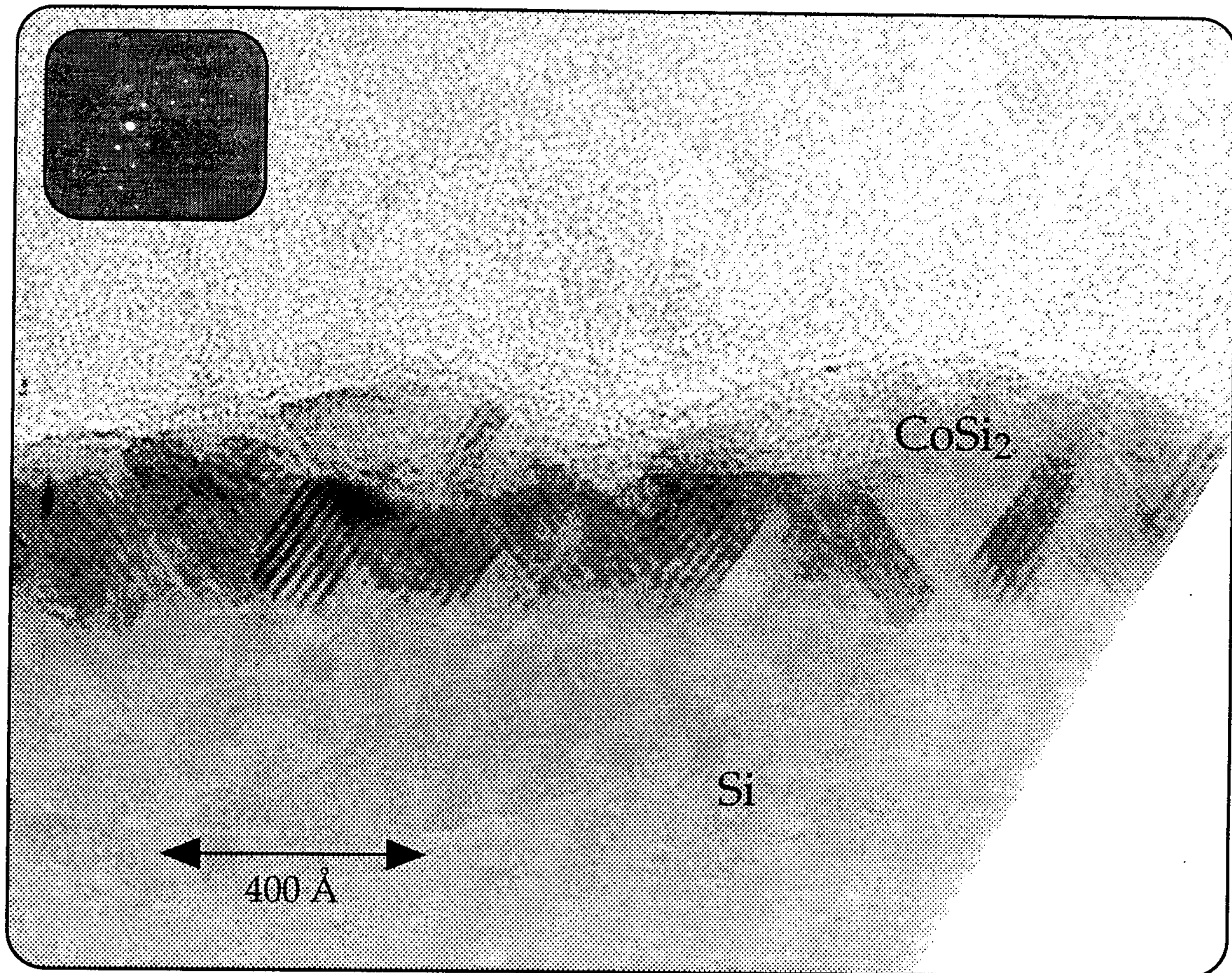


Figure 4. Cross sectional TEM of $CoSi_2$/Si interface.

The sample was then placed into a microwave CVD reactor for diamond growth. After a brief hydrogen plasma clean, the sample underwent a biased nucleation step[2, 3] and a growth step as follows:

	bias step	growth step
microwave power (W)	600	600
pressure (Torr)	20	25
H_2 flow (sccm)	500	500
CH_4 flow (sccm)	25	1
sample temp. (°C)	~800	~725
bias voltage (V)	-234	-
bias current (mA)	80	-
time	4 min.	21 hrs.

A bare Si <100> substrate was run under the same conditions to serve as a control sample. Both samples were examined using the SEM to ascertain the particle morphology and orientation. SEM micrographs showing (100) textured, oriented diamond particles on the Si control sample and the $CoSi_2$ sample appear in Fig. 5.

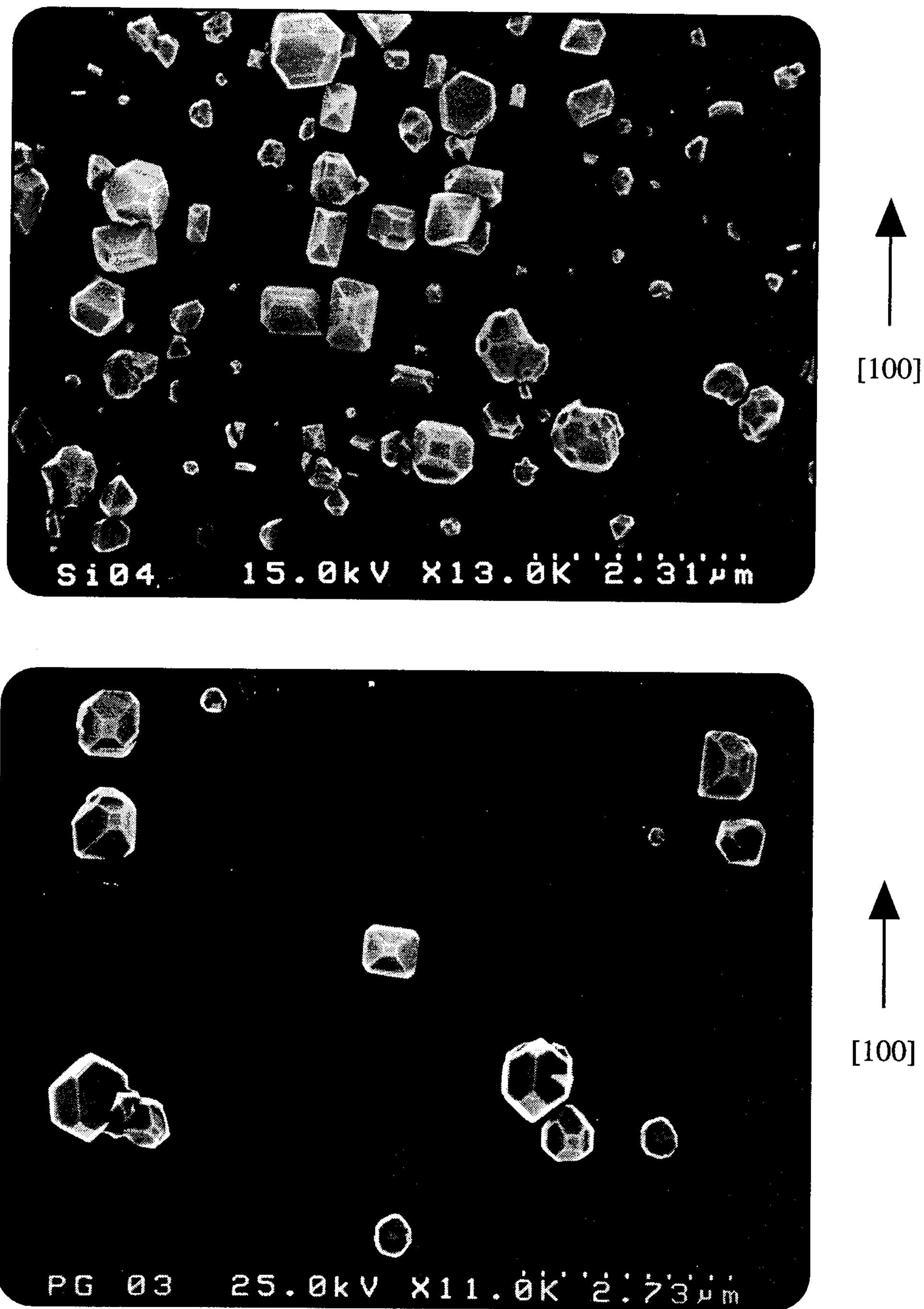


Figure 5. SEM micrograhs of some oriented (100) faceted diamond particles grown on bare Si (100) (top) and $CoSi_2$/Si (100) (bottom).

D. Discussion

The quantitative XPS and scanning AES depth profile both indicated that the sample surface was slightly Si rich. The excess Si may be due to the fact that the source material did not evaporate with the calculated vapor pressures of Si and Co or that Si diffused upward through the film during the annealing process. The 2×2 LEED pattern of the $CoSi_2$ film indicates that the surface is crystalline, but is not a pure Si surface. The TEM micro diffraction pattern and brightfield image of the sample cross section suggest a monocrystalline film or crystalline film with large domains.

A mixture of (100) and (110) textured particles was present on both the bare Si control sample and the silicide sample. In some areas on both samples, several neighboring (100) textured particles were aligned with the [100] direction of the Si substrate. More samples will need to be run in order to ascertain whether the silicide represents an improvement in promoting oriented diamond nucleation over bare Si.

E. Conclusions

A $CoSi_2$ film has been formed on a Si <100> surface in order to investigate the use of $CoSi_2$ as a diamond substrate. Quantitative XPS and Scanning AES Depth Profiling indicated that the surface of the e-beam deposited $CoSi_2$ film was slightly Si rich. LEED and Transmission Electron Microscopy indicated a monocrystalline silicide layer or a crystalline silicide layer with large domains. Diamond growth on the silicide layer resulted in a mixture of (100) and (110) textured diamond particles. In some areas of the sample, a number of the (100) textured particles were clearly aligned along the [100] direction of the Si substrate. More experiments are required in order to ascertain whether the degree of orientation on the silicide layer surpasses that achievable on bare Si.

F. Future Research Plans and Goals

A two source electron beam evaporation system, which will allow co-deposition of Si and Co, will be utilized to better control the stoichiometry of the $CoSi_2$ film. *In situ* RHEED capability will allow real time growth monitoring. Diamond films will be grown on a number of silicide samples in order to determine more quantitatively whether $CoSi_2$ represents an advantage over bare Si as a diamond substrate in terms of its ability to promote oriented diamond nuclei.

G. References

1. B. R. Stoner and J. T. Glass, Applied Physics Letters **60**(6), 698, 1992.
2. B. R. Stoner, S. R. Sahaida, and J. P. Bade, Journal of Materials Research **8**(6), 1334, 1993.
3. S. D. Wolter, *et al.*, Applied Physics Letters **62**(11), 1215, 1993.
4. W. Zhu, P. C. Yang, and J. T. Glass, Applied Physics Letters **63**(20), 1640, 1993.

5. P. C. Yang, W. Zhu, and J. T. Glass, Journal of Materials Research **8**(8), 1773, 1993.
6. W. Liu, et al., to be published in Journal of Applied Physics **78**(2), 1995.
7. J. R. Jimenez, *et al.*, Appl. Phys. Lett. **57**(26), 2811, 1990.
8. L. J. Schowalter, *et al.*, Journal of Crystal Growth **111**, 948, 1991.
9. R. T. Tung, F. Schrey, and S. M. Yalisove, Applied Physics Letters **55**(19), 2005, 1989.
10. S. M. Yalisove, R. T. Tung, and J. L. Batstone. in Materials Research Society Symposium. Materials Research Society, 1988.
11. S. M. Yalisove, R. T. Tung, and D. Loretto, J. Vac. Sci. Technol. **A7**(3), 1472, 1989.
12. K. Schwerdtfeger and H.-J. Engell, Archiv fuer das Eisenhuttenwesen **35**, 533, 1964.
13. C. B. Alcock, V. P. Itkin, and M. K. Horrigan, Canadian Metallurgical Quarterly **23**(3) 309, 1984.
14. D. B. Fenner, D. K. Biegelsen, and R. D. Bringans, Journal of Applied Physics **66**(1) 419, 1989.
15. L. C. Feldman and J. W. Mayer, *Fundamentals of Surface and Thin Film Analysis*, New York: North-Holland, 1986.
16. J. J. Yeh and I. Lindau, Atomic Data and Nuclear Data Tables **32**, 1, 1985.

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