# Complementary 2-D MESFET for Low Power Electronics

**Interim Report # 5**

**Air Force SBIR Phase I**
**Contract Number: F33615-95-C-1679**

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# (AirForce SBIR Contract F33615-95-C-1679)

## Phase I Interim Report #5

As detailed in the Phase I proposal, the project has four major tasks. These are 1) assessment of the p-channel 2-D MESFET device fabrication, 2) development of a p-channel 2-D MESFET model and implementation of the model into AIM-SPICE, 3) circuit simulations of complementary 2-D MESFET circuits using AIM-SPICE and comparison with conventional circuits, and, 4) analysis of manufacturability and technology insertion issues. This report summarizes progress in each task area through 29 AUG 95.

### Task 1: Assessment of p-Channel Device Fabrication

The assessment of the p-channel 2-D MESFET device fabrication is underway. A heterostructure wafer, which was to have been delivered in mid-August, is now scheduled to be delivered in the next couple weeks. A second wafer has been obtained from Vitesse Semiconductor Corporation and will be used for the first p-channel fabrication studies beginning in early September.

### Task 2: Development of p-Channel 2-D MESFET Model

The p-channel 2-D MESFET model has been implemented into AIM-Spice and is presently being used to simulate discrete p-channel 2-D MESFET *I-V* characteristics as well as complementary 2-D MESFET logic circuits (see below). The p-channel device model uses a lower Schottky barrier height (typically 0.6V) compared with that of the n-channel device (typically 0.8 V). Also, the hole mobility has been set to 1000 $cm^2/Vs$, consistent with the observed trend of enhanced electron mobility in the n-channel devices.

### Task 3: Complementary 2-D MESFET Circuit Simulations

Circuit simulations of complementary 2-D MESFET circuits are ongoing. In Fig. 1, we show the transient simulation of a 11-stage ring oscillator using complementary 2-D MESFET with a 0.8 V supply voltage. The gate switching delay was 12.3 ps and the power consumption was 2.2 μW. By varying the parameters of the individual FETs (e.g. threshold voltages, channel length, we observed small and offsetting changes in the delay and power, as expected. Further dc and transient simulations of different combinations of n- and p-channel devices will be performed to understand how to optimally match devices for low power-delay performance. Also, we will investigate possible circuit advantages of the multi-input gate operation of the 2-D MESFET.

### Task 4: Manufacturability and Technology Insertion Issues

This task will be summarized in the Final Report.

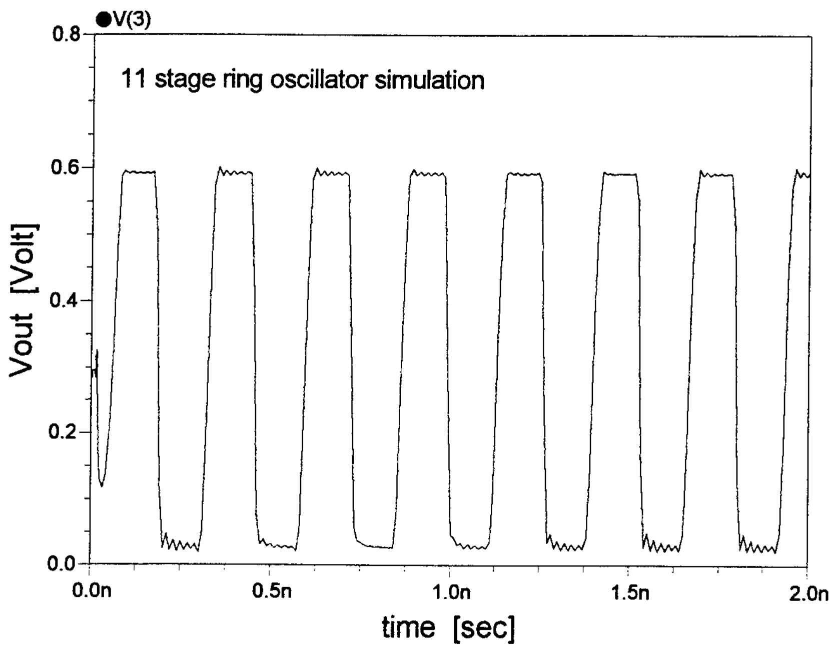


*Fig. 1. Complementary 2-D MESFET DC ring oscillator simulation (11-stage) showing a gate delay of 123 ps and power of 2.2 μW..*

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