Novel Field Effect Transistors for Low Power Electronics

Progress Report # 1

NAVY STTR Phase I
Contract Number: N00014-94-C-0260

October 28, 1994

Delivered To:

Dr. Alvin M. Goodman
Program Officer, Code 312
Office of Naval Research
Ballston Tower One
800 North Quincy Street
Arlington, VA 22217-5660

From:

Advanced Device Technologies, Inc.
1590 Ravens Place
Charlottesville, VA 22901
TEL: (804) 974-1416

W. C.B. Peatman 10/28/94
Dr. William C.B. Peatman, President

Novel Field Effect Transistors for Low Power Electronics
(ONR STTR Contract N00014-94-C-0260)

Table of Contents

I. Phase I Technical Objectives

The primary objective of this Phase I project is to determine the extent of the significant reduction in power consumption of integrated circuits which may be achieved by utilizing a novel sidegate FET technology. The new FET technology promises to eliminate the Narrow Channel Effect (NCE) which is one of the primary factors limiting the minimum power consumption of integrated circuits. By eliminating the NCE, we will be able to scale the device size dramatically and reduce the power consumption by an order of magnitude. The project will assess the power, speed, circuit design, processing, and manufacturability of the new FET technology for both digital and analog circuit applications. In particular, we will extract device parameters from the new ultra-low power FETs fabricated at UVa, develop device models, incorporate these models into a new SPICE package (AIM-Spice), simulate different logic families including DCFL and SCFL, and compare the predicted performance with the standard DCFL and SCFL logic. We will also analyze the gate current leakage and subthreshold slope as the primary factors limiting the noise margins at low power supplies, establish the minimum required bias voltage for reliable operation, and analyze the factors determining the threshold voltage changes from device to device as well as other factors which may limit the yield and integration scale.

II. Progress Report #1

As detailed in the Phase I proposal, the project has five major tasks. These are 1) 2-D MESFET (discrete) device fabrication, 2) detailed device evaluation and optimization for next iteration of device design and fabrication, 3) parameter extraction using AIM-SPICE to generate and refine AIM-SPICE 2-D MESFET models, 4) 2-D MESFET DCFL and SCFL logic circuit simulations using AIM-SPICE and comparison with conventional circuits, and 5) analysis of manufacturability and technology insertion issues. This report summarizes the background and progress to date in each of these task areas.

Task 1: Device Fabrication

The critical dimensions of the 2-D MESFET, shown in Fig. 1, include the channel width, W_0 and length, L_g and the drain-source spacing L_{DS}[1]. Two batches of prototype 2-D MESFETs having channel dimensions ranging from 0.5 - 1.0 micron (width) and 1.0 micron (length) were fabricated prior to the start of this STTR contract[2] on a double δ-doped InGaAs/AlGaAs heterostructure having sheet conductivity of 600 ohm/square at room temperature. A scanning electron micrograph of the 1.0 micron channel width device is shown in Fig. 2. Significant improvement in device yield was achieved over previous batches, primarily through modifications in the gate etch and electroplate processes. Further improvements to the gate metallization will be required to achieve higher yield and greater uniformity over the wafer.

New device batches using three different 2-DEG heterostructures are now in progress and will provide further data sets for the parameter extraction. The material for these batches include two AlGaAs/InGaAs heterostructures designed for high speed applications. The third structure is an AlGaAs/GaAs structure having very high (10^6 cm^2/V-s at 4K) mobility suitable for the investigation of the mesoscopic behavior of quantum wires.

Task 2: Evaluation, Optimization, Design

The dc I-V characteristics of 2-D MESFET devices will be measured and cataloged in library files according to device dimensions and material parameters. Such cataloging is useful in developing a new 2-D MESFET device model. To date, both enhancement and depletion mode devices have been obtained. Representative room temperature I_D-V_{DS} curves of each device type are shown in Fig. 3. These characteristics are notable for the high unit width current density and transconductance (D-mode) and excellent output characteristics (E-mode), as well as the a sharp pinch-off characteristic in each case. Table 1 summarizes the dimensional and electrical characteristics of these prototype devices.

The prototype devices have source and drain series resistances of order 2000 ohms. The high series resistance limits the transconductance (and therefore the speed) and it also causes a higher saturation voltage (which limits the reduction of the gate voltage swing) so a

---

1. W.C.B. Peatman, H. Park and M. Shur, "Two-Dimensional Metal-Semiconductor Field Effect Transistor for Ultra Low Power Circuit Applications," *IEEE Elect. Dev. Lett.*, Vol. 15, No. 7, pp. 245-247, July 1994.

2. Prior research on the 2-D MESFET was performed at the University of Virginia under ONR contract N00014-90-J-4006.

primary goal of the device fabrication (in Phase I and II) is to reduce series resistance. This will be achieved by reducing the drain-source spacing to 2-3 micron and by reducing the ohmic contact resistance to 0.1-0.2 ohm-mm. Further reduction will be achieved by utilizing higher sheet conductivity structures and possibly by cooling the devices for mobility enhancement. Such modifications should lead to R_s and R_d of order 100-200 ohms which, together with reduced channel lengths, should lead to significant increases in g_m and f_T. .

Task 3: 2-D MESFET AIM-SPICE Modeling

The measured transistor characteristics shown in Fig. 3 were fitted using the universal HFET model of AIM-SPICE[3], an advanced version of P-SPICE. So far, the HFET model yields a good agreement to the measured data. The parameters of the HFET simulations are summarized in Table 2. **The good fit obtained here to such narrow channel devices illustrates the fact that the 2-D MESFET does not suffer from the narrow channel effect which plagues conventional FETs at widths below about 5 micron**.

Currently, we are simulating the subthreshold region of the 2-D MESFET I-V characteristic since this region is of particular interest for low power applications. Measured data from previous devices indicated that the 2-D MESFET can have low gate leakage current of less than 1 nA, a subthreshold slope of 75 mV/decade and a ON/OFF current ratio in excess of 10^5, all at room temperature where most applications will be. Results of these simulations will be incorporated into the AIMSPICE model to be used in future simulations of 2-D MESFET circuits.

Task 4: 2-D MESFET DCFL and SCFL Circuit Simulation

Measurements and simulations of 2-D MESFET circuits will be underway shortly and will be reported in future progress reports.

Task 5: Manufacturability and Technology Insertion Issues

Several key questions concerning the manufacturability of 2-D MESFETs must be addressed during the course of this research. First, it will be necessary to determine the design and processing parameters which limit the yield (device-to-device and wafer-to-wafer). Results from the recent batches are encouraging, showing a significant increase in yield due to improving gate etch and plate processes. Threshold voltage variation as a function of channel width and sheet resistance must also be evaluated as the design for E/D devices becomes clearer. Gate leakage current and series resistance must also be improved in order to achieve significantly lower power-delay product compared with conventional circuits.

---

3. AIM-SPICE was developed by Ytterdal, Fjeldly, Shur, and Lee and is available on INTERNET through anonymous FTP.

III. Tables and Figures

Table 1: Parameters of Prototype D-Mode and E-Mode Devices

	W_0	L_g	L_{DS}	R_T (R_S+R_D)	V_{th}	J_p	g_m	f_T
	(μm)	(μm)	(μm)	(Ω)	(V)	(mA/ mm)	(mS/ mm)	(GHz)
D-mode	1.0	1.0	8.0	3800	-0.5	210	212	21.0
E-mode*	0.5	1.0	8.0	4110	0.0	60	60	(NA)

Table 2: Parameters of AIM-SPICE Modeling for Fig. 3 Fits

	Vth	V_T	δ	R_T (R_S+R_D)	m	λ	V_L
	(mV)	(V)		(Ω)		(1/V)	(V)
D-mode	25.9	-0.45	3.0	3900	1.9	.04	.314
E-mode	25.9	-0.01	3.0	4110	3.0	.002	.43

* preliminary data

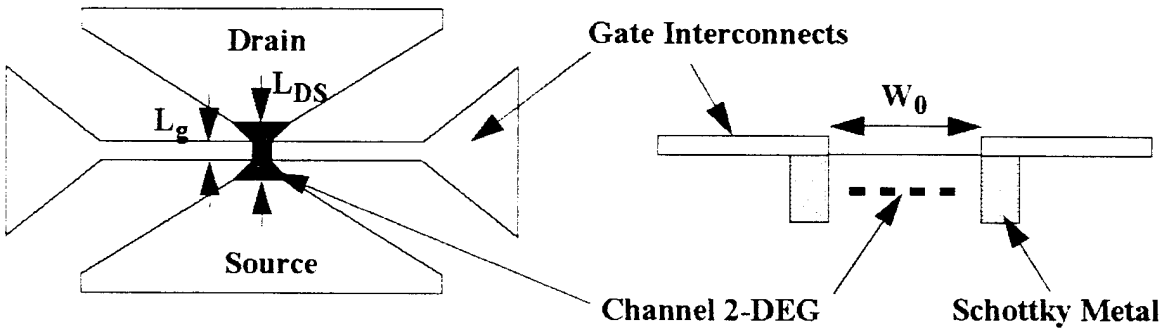

Fig. 1.Sketch of 2-D MESFET top view (left) and cross-section (right).

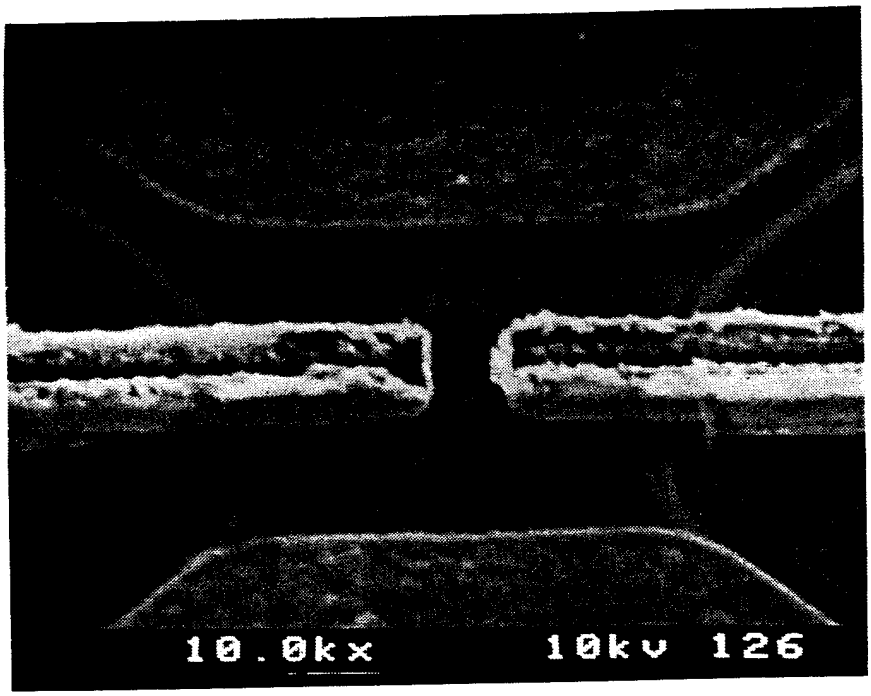

Fig. 2.SEM of prototype 2-D MESFET having channel dimensions of 1.0 micron wide by 1.0 micron long.

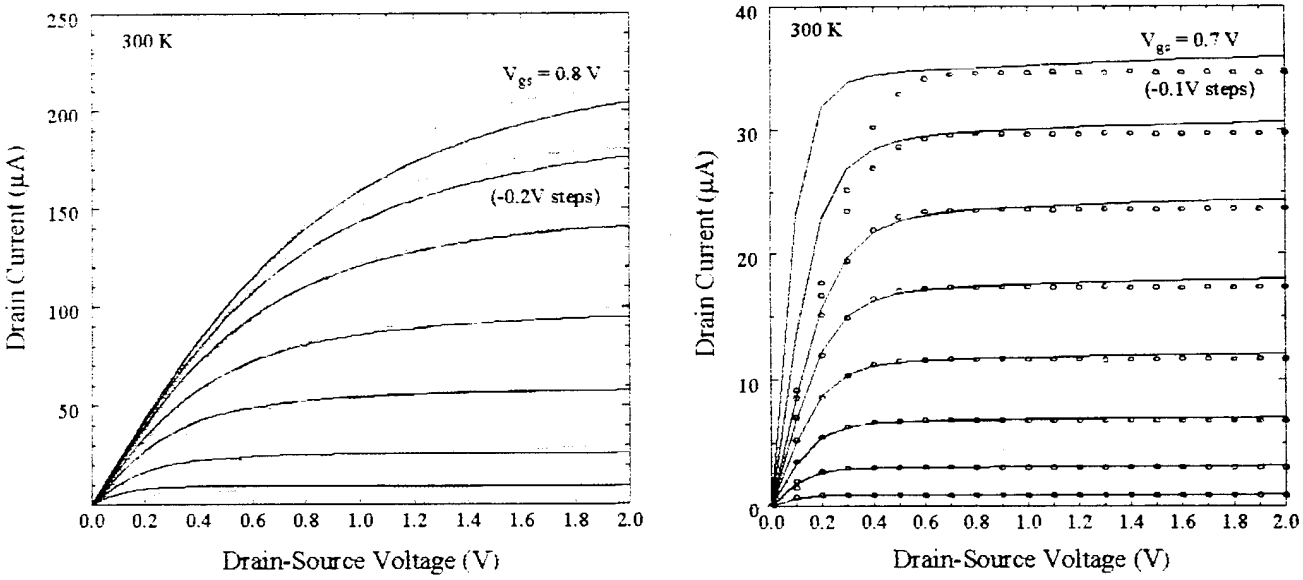

Fig. 3. Measured I-V characteristics (dots) of D-mode (left) and E-mode (right) 2-D MESFETs, fitted (solid lines) using AIMSPICE HFET model.

Distribution List

1-5 Office of Naval Research
Ballston Tower One
800 North Quincy Street
Arlington, VA 22217-5660

ATTN: Dr. Alvin M. Goodman
Code 312
(703) 696-4845

6 Administrative Contracting Officer
DCMAO Baltimore
ATTN: Chesapeake
200 Towsontown Blvd. West
Towson, MD 21204-5299

7 Naval Research Laboratory
Washington, DC 20375-5326
ATTN: Director, Code 2627

8-9 Defense Technical Information Center ✓
Building 5, Cameron Station
Alexandria, VA 22304-6145

10 University of Virginia
Office of Sponsored Programs
P.O. Box 9003
Charlottesville, VA 22906