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ABSTRACT *(Maximum 200 words)*

In Fault Modeling and Testing of Complex Systems such as the opto-electronic computing systems, a probablistic fault model for complex degradable system was proposed. This model has been validated by using an event-driven simulator and fault injector on the representative measures from both replicated and dilated multi-stage interconnection networks. Furthermore, an architecture which integrates the concept of concurrency and distributed test pattern generation for testing complex circuits on a planer layout has been proposed. This approach performs test pattern generation and response analysis concurrently, therefore minimizing testing time for the overall system testing. Circuits are partitioned into segments which can be tested in parallel in testing time bounded by 2^n clock cycles, where n is the maximum no. of inputs for the biggest cluster. The impact on the quality of the patterns generated has been found to be negligible. The software package is called Merced, which performs circuit test as well as performance analysis, with full compatibility with commercial tools.

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June 15, 1995

Re: Final report on ONR grant no: N00014-91-J-1017
Title: Fault Tolerance in Opto-electronic Computing
Principle Investigator: Professor Ting-Ting Y. Lin
Addressees:
Scientific Officer, Dr. Clifford G. Lau
Administrative Grants Officer
Director, Naval Research Laboratory
Defense Technical Information Center

Dear Sirs,

This final report serves to summarize all the research and development activities supported by the grant in three sections: research results, student support.

1. Research Results

Our work has matured greatly in the past couple of years. This is not evidence in the quality of the publications but also the number of invited presentations by industry and workshops. I will highlight some of the achievements followed by the list of the papers.

A. Fault Modeling and Testing of Complex Systems

This project has produced an architecture which integrates the concept of concurrency and distributed test pattern generation for testing complex circuits on a planer layout. This approach performs test pattern generation and response analysis concurrently, therefore minimizing testing time for the overall system testing. Circuits are partitioned into segments which can be tested in parallel in testing time bounded by 2^n clock cycles, where n is the maximum no. of inputs for the biggest cluster. The impact on the quality of the patterns generated has been found to be negligible. Our software is called Merced, which performs circuit test as well as performance analysis. A list of the papers in this area is in Appendix I.

B.. *Performance Evaluation of Fault Tolerant Optical Multi-stage Interconnection Network*

This project is to set up an evaluation scheme for complex degradable system. An event-driven simulator has been developed to study the corresponding measures as the replicated or

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dilated banyans degrade under component failure. A fault-injector is used to inject faults under some given distribution and to degrade the network accordingly. A detailed discussion on the choice for optical network based on these design parameters has been documented in volume I of 'Foundations of Dependable Computing' by Kluwer Academic Publishing. Results on a general N component system were very encouraging for evaluating degradable systems that have uniform components. And simulation results on both the replicated network and the dilated network verify that our modeling techniques were useful. A list of the papers is attached in Appendix II.

You probably will notice that the papers listed in the Appendices go beyond the period of the support. Some papers were extension of the work done after the supporting period. I included the ones that have been accepted here for completeness. Papers still been reviewed, will be augmented later, once accepted.

2. Student Support

Two graduate students have been supported in the past three years under this grant. They have either graduated or on his way to finishing up with the support of this funding. Amiya Bhattacharya is finishing up his thesis work in performability evaluation of complex systems. He has been contacting several research laboratories in possible continuing support of this work at their facilities. Huoy-Yu Liou, who developed the framework for the test architecture, has graduated and is currently working for Tandem Computers.. She will oversee that the design of all Tandem computers have the highest testability possible integrated using our framework. We thank the agency for their support over the past three years.

The above summarizes the agency's support on the project. We are looking at all possibilities to extend this research work to industrial use. If there are suggestions as to who may be interested in this topic, I'll be happy to accommodate. Thank you very much.

Best regards,

Ting-Ting Y. Lin
(619) 534-4738

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Appendix I (*Fault Modeling and Testing of Complex Systems*)

1. Dau-Tsuong Lu, Ting-Ting Y. Lin, Fouad E. Kiamilev, Sadik C. Esener, and Sing H. Lee: "Fault-Tolerant Computing on POEM," in Optical Computing, sponsored by Optical Society of America, March 4-6, 1991, Technical Digest, Series Volume 6, p. 104-107.

2. Ching-Wei Yeh, Chung-Kuan Cheng, and Ting-Ting Y. Lin: "A General Purpose Multiple Way Partitioning Algorithm," in Proceedings of the 28th ACM/IEEE Design Automation Confrerence (DAC91), June 1, 1991, pp. 421-426.

3. Ching-Wei Yeh, Chung-Kuan Cheng, and Ting-Ting Y. Lin: "An Experimental Evaluation of Partitioning Algorithms," The 4th IEEE Annual International ASIC Conference, September 23-27, 1991, pp. 1.1-1.4.

4. Ting-Ting Y. Lin and Charles Kaseff: "Performance Evaluation of Cascadable Built-In Tester for Large I/O Multichip Modules," The 4th IEEE Annual International ASIC Conference, September 23-27, 1991, pp. 3.1-3.4.

5. Ting-Ting Y. Lin, John Comito, and Charles Kaseff, "Evaluation of Test Strategies for Multichip Modules," in the proceedings of The 5th IEEE Annual International ASIC Conference and Exhibit, September 21-25, 1992, Rochester, N.Y., pp. 234-237.

6. C.W.Yeh, C.K.Cheng, T.T.Lin, "A probabilistic Multicommodity-Flow Solution to Circuit Clustering Problems," in the digest of technical papers of the IEEE/ACM Int. Conference on Computer-Aided Design, November 8-12, 1992, Santa Clara, CA, pp. 428-431.

7. T-T. Lin, "Improving Load Balancing Property During System Reconfiguration", in the proceedings of the 3rd International Conference on CAD & Computer Graphics, August 23-26, 1993, Beijing, China, pp. 582-588.

8. Huoy-Yu Liou and T-T. Lin, "Parallel Built-in Self Test and Pipelined Test Scheduling for Multi-chip Modules", in the proceedings of the 3rd International Conference on CAD & Computer Graphics, August 23-26, 1993, Beijing, China, pp. 622-628.

9.T-T. Lin and H-Y Liou: " A New Framework for Designing BIT MultiChip Modules with Pipelined Test Strategies," in IEEE Design & Test of Computers, December, 1993, pp. 38-51.

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10. Valentin O. Roda, and Ting-Ting Lin: "The Distributed Voting Strategy for Fault Diagnosis And Reconfiguration of Linear Processor Arrays," in the The Journal of Microelectronics and Reliability, Vol. 34, No. 6, pp. 955-967, 1994.

11. Ting-Ting Lin, and Valentin O. Roda: "Two Approaches for the Reconfiguration of Linear Processor Arrays," in Proceedings of the International Conference on Parallel and Distributed Systems (ICPADS'93), December 1993, pp. 274-278.

12. Dau-Tsuong Lu, Wang P.Poon, Ting-Ting Lin, Sing H. Lee: "Optoelectronic Component Modeling and System Simulation," in OSA Annual Meeting Technical Digest Vol. 16, pp. 37, 1993.

13. H.Y. Liou, and T-T. Lin, "Analysis on Link Failures in Free-Space Optical Interconnects", in Proceedings of the 1994 SPIE Optoelectronic Interconnects Conference, January, 1994.

14. H.Y. Liou, T-T.Y. Lin, L-T. Liu, and C-K. Cheng "Circuit Partitioning for Pipelined Pseudo-Exhaustive Testing Using Simulated Annealing", in Proceedings of 1994 Customed Integrated Circuts Conference (CICC), May, 1994, pp. 417-420.

15. H.Y. Liou, T-T.Y.Lin, L-T Liu, and C-K. Cheng " Partitioning for Pipelined Pseudo-Exhaustive Testing Using Simulated Annealing", in Proceedings of IEEE International ASIC Conference, September, 1994, pp. 421-425.

16. T-T.Y. Lin, R. Stave, and D.-Y. Kao "On Choosing the Right Error Model for Circuit Testing", in Proceedings of IEEE International ASIC Conference, September, 1994, pp. 400-402.

17. C. W. Yeh, C.K. Cheng, and T-T.Y. Lin: "A General PurposeMultiple Way Partitioning Algorithm," in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems, December, 1994, pp. 1480-1488.

18. C. W. Yeh, C.K. Cheng, and T-T.Y. Lin: "Optimization by Iterative Improvement: An Experimental Evaluation on Two-Way Partitioning", in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems, February, 1995, pp. 145-153.

19. C. W. Yeh, C.K. Cheng, and T-T.Y. Lin: "Circuit Clustering Using a Stochastic Flow Injection Method", in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems, February, 1995, pp. 154-162.

20. Valentin Obac Roda, and Ting-Ting. Y. Lin, "On the Effect of Spare Positioning on the Reconfigurability of Two-dimensional Processor Arrays", in the proceedings of the Aizu International Symposium on Parallel Algorithms/Architectuure Synthesis (pAs'95), March 13-18, 1995, pp. 153-159.

21. T.-T. Y. Lin, and L-C. Tai, "Iterative Improvement on Load Balancing Propertyof Array Configuration", in proceedings of the International Symposium on Parallel Architectures, Algorithms, and Networks (ISPAN), December 15-17, 1994.

22. Ting-Ting Y. Lin, and Huoy-Yu Liou, "Analyzing the Error of an Approximate Method for Computing Performance-Related Reliability", to be published in the proceedings of the fourth International Conference on CAD&CG, Oct. 22-26,1995.

Appendix II (*Performance Evaluation of Fault Tolerant Optical Multi-stage Interconnection Network*)

1. Dau-Tsuong Lu, Ting-Ting Y. Lin, Sing H. Lee: "Fault-Tolerant Switching Element for the Twin Butterfly," in OSA Annual Meeting Technical Digest, September 20-25, 1992 (Optical Society of America, Washington, D.C., 1992), Vol.23, pp.104.

2. H.E.Ascher, T-T. Lin, & D.P. Siewiorek, "Modification of: Error Log Analysis: Statistical Modeling and Heuristic Trend Analysis", IEEE Transactions on Reliability, December, 1992, pp. 599-602.

3. A. Bhattacharya, R. Rao, and T-T. Lin, "Delay Analysis of Synchronous Circuit-switched Delta Networks", in the proceedings of the 7th International Parallel Processing Symposium, April 13-16, 1993, Newport Beach, CA, pp. 666-670.

4. A. Bhattacharya, R. Rao, and T.-T. Y. Lin, "Performability Analysis of Non-Repairable Multicomponent Systems Using Order Statistics", in the proceedings of the Sixth IEEE Symposium on Parallel and Distributed Processing (SPDP), October, 1994, pp. 646-653.

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5. A. Bhattacharya, R. Rao, and T.-T. Y. Lin, "Evaluation of Performability Measures for Replicated Banyan Networks", in proceedings of the first IEEE Workshop on Parallel Processing (IWPP'95), December 26-30, 1994, pp. 234-239.

6. A. Bhattacharya, R. Rao, and T.-T. Y. Lin, "Evaluation of Performability Measures for Replicated Banyan Networks", in the proceedings of the IEEE International Computer Performance and Dependability Symposium(IPDS'95), April 26-29, 1995, pp. 265-276.

7. Zhiyu Tian, Peter C.K. Liu, Ting-Ting Y. Lin, and Shiyuan Yang, "Analyzing the Error of an Approximate Method for Computing Performance-Related Reliability", accepted to the Jounal of Microelectronics and Reliability.