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DIGITAL ROTATIONAL SPEED MEASUREMENT

CAPT RONALD J. FISCHER

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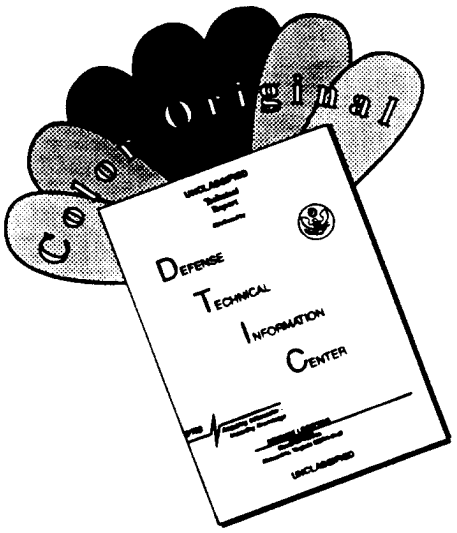

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13. ABSTRACT *(Maximum 200 words)*

THE COMPRESSOR RESEARCH FACILITY (CRF) LOCATED AT WRIGHT PATTERSON AFB, OHIO IS CONFIGURED TO PERMIT THE EVALUATION OF FULL-SCALE FANS OR COMPRESSORS IN SIMULATED FLIGHT CONDITIONS. ROTATIONAL SPEED MEASUREMENT IS USED BOTH FOR CONTROL AND PERFORMANCE DATA COLLECTION OF COMPRESSORS UNDER TEST. THIS REPORT DESCRIBES THE DESIGN OF AN INTEGRATED CIRCUIT AND SUPPORTING HARDWARE FOR REPLACING THE OLDER ROTATIONAL MEASUREMNT SYSTEM CURRENTLY IN USE IN THE CRF.

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FOREWORD

This design was completed in conjunction with the masters of Electrical Engineering Very Large Scale Integration (VLSI) course requirements at Wright State University. The design was performed at the Aero Propulsion and Power Directorate's Technology Branch, Compressor Research Facility, Wright Laboratory, WPAFB, Ohio. All Computer Aided Design (CAD) diagrams and simulation results were generated using the University of California, Berkeley CAD tools software packages. Integrated circuit fabrication was performed at MOSIS, USC Information Sciences Institute, 4676 Admiralty Way, marina Del Rey, CA 90292-6695. The production run number for the integrated circuit is N44NAE1. The disk containing the file is located at the Compressor Research Facility (513)255-6802. A copy of this file is required to fabricate the chip.

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SECTION 1

INTRODUCTION

The speed measurement board was designed to replace the current system used in the Compressor Research Facility (CRF). The circuit board currently used was designed using Transistor-Transistor Logic (TTL) technology and is made up of more than 30 different chips in addition to many individual circuit components. Troubleshooting the old system in the event of problems was very extensive and required many man hours of technician time. Because of this fact, it was desirable for the new speed measurement system to use the fewest amount of individual components possible. The reduction in components will provide for a more reliable system which is easier to trouble shoot.

Obtaining the goal of component reduction was accomplished with the use of a single Complimentary Metal Oxide Semiconductor (CMOS) system specific chip. The integrated circuit was designed specifically for use on this board, but by keeping functions like the clocking and input signal filtering and conditioning external to the chip, it will also be a useful package in any application requiring digital timing in between events. The use of a single CMOS integrated circuit to replace in excess of 30 TTL devices will reduce the complication of the system and add for ease in trouble shooting and repair since there are less components to check if there is a problem. The new board will consist of the CMOS speed measurement chip, a 150 kHz clock circuit, and a analog to digital input signal conditioner. This arrangement limits the number of components to 16.

The use of CMOS technology in the design of the board allows several advantages over the use of TTL circuits. CMOS circuits have less propagation delay when changing states and can therefore be driven at higher clock rates. This is not an important capability in the CRF application due to the relatively low clock speed required. In other applications however, this may be more important, giving the chip a wide range of potential applications. Another important factor in the use of CMOS over TTL is the lower power usage of a CMOS circuit. Digital circuits consume power during transitions in state. Since CMOS changes states more rapidly, circuits constructed from these components will use less power. Power usage in a digital circuit contributes to heat buildup in the components. Lower heat generation results in longer component life spans and greater system reliability.

SECTION 2

REQUIREMENTS

The environment of the CRF placed many design requirements on the speed measurement system. This environment includes the instrumentation used to generate the input signal for the system, the required range of the measurement, and the output data format representing the measurement.

2.1. INPUT SIGNAL

The input signal to the speed measurement system is generated by a Bently Nevada proximity probe. The pulse outputs a single pulse once every revolution of the drive shaft. This pulse has a magnitude of -15 volts and a duration of approximately 3.3 μsec. The signal magnitude is zero at all other times. The pulse needs to be digitized for use in a CMOS circuit. This means this analog signal must be digitized, converted to a 0 to 5 volt pulse, by the measurement system to be usable by a CMOS circuit as well as nondestructive to the components.

CMOS circuits will not work with negative signals or signals greater than 7.5 volts in magnitude. This condition depends slightly upon the operating conditions of the chip, such as temperature and supply voltage, but does not as a general rule vary far from the above limitations. Extended operation outside of this range will cause component failure. Therefore, it is essential in order for this design to be reliable source of speed data, that an input signal conditioning circuit be developed to protect the vulnerable CMOS components from direct input from the Bently Nevada probe.

The conditioned input signal from the proximity probe will need to also be digitized before being input into the speed measurement chip. This is because the signal, even after being limited to the correct voltage range, is still analog in nature and may have noise and slow rise and fall times associated with it. It is important to have a well behaved square pulse to a CMOS circuit since these components can be very susceptible to noise and variations in the input signal. Typical input parameters to a CMOS integrated circuit are a high voltage transition when the input goes above 2.7 volts and a low transition when the signal falls below 1.6 volts. This leaves a normal noise margin of approximately 1.1 volts. It can easily be seen from these input parameters that a slight variance of the input will cause errors in the processing of the probe data.

2.2. OPERATING FREQUENCY

The circuit needs to be capable of operating within the range of frequencies generated by the proximity probe. This is a once per revolution signal. The CRF's maximum rotation rate is 30,000 rpm which corresponds to a maximum frequency of 500 Hz from the proximity probe. This frequency is well within the operating speed of a CMOS circuit.

2.3. CIRCUIT OUTPUT

The circuit is required to output a digital word representing the speed or frequency of received proximity pulses. The digital output needs to be stable to allow enough time for it to be read accurately by the facility control computers. The control computers are on a different timing system from the speed measurement board. This will require the board to signal the control computer in fashion to indicate when reading the data is possible. This will eliminate the possibility of reading data when it is in a state of transition and introducing errors into the measurement.

SECTION 3

INTEGRATED CIRCUIT DESIGN DESCRIPTION

The circuit works by counting the time in between input pulses from the proximity probe. This is accomplished by using an external clock, operating at 150 kHz. The external clock was chosen for flexibility in the application of the chip. With different clock speeds the chip could be used elsewhere in the facility where digital speed measurement or event timing is required. The counter on the chip counts each pulse from the external clock. When a input pulse from the proximity probe is received, the counter is read into a memory location, and then reset. The counting process is then begun again. With this scheme the higher the count on the counter, the slower the shaft is rotating. To obtain some amount of input smoothing and rounding out of the noise effects, a moving average system is used. There are four memory locations the count is read into and stored. The average is obtained by adding all four locations together and ignoring the least two significant bits (LSB) of the sum. This is equivalent to dividing by four. The two LSB do give the decimal equivalent or remainder of the division and can be used to obtain more resolution from the chips output. Each time a clock read is performed, it is into a different memory location than the previous three reads. This gives an average of the current speed with the last three speeds. The functional block diagram of the complete circuit is shown in Figure 3.1.

The external clock speed determines the accuracy of the speed measured by the circuit. The 150 kHz clock was determined to be accurate enough to meet CRF requirements. The slowest speed readable in this arrangement is 550 rpm, or 9.16 Hz, giving a maximum count of 16,384. At this point the 14 bit clock will overflow and the data output of the chip will no longer be valid. This requires the speed chip to consist of a 14 bit clock and memory section. Using 150 kHz clock to represent 12,000 rpm, the normal CRF maximum operating speed while testing, gives a system accuracy of about + or - 1.5 rpm.

The above discussion reveals the chips input/output requirements. It will require two inputs, the 150 kHz clock and the proximity probe input. The output word from the adder is 16 bits. Since the Facility Control Computer (FCC) is on a different timing system than this chip, a data valid bit will also have to be incorporated. This gives a total input/output (I/O) requirement of 19 pads.

The following sections describe the subsystems of the overall chip design in detail. The subsections and their interconnections are displayed in the block diagram of Figure 3.1. They consist of the memory selection logic, a 14 bit counter, a 4X14 bit memory array, a 4X14 bit ripple carry adder, controller, output latch, and various other logic gates and buffers.

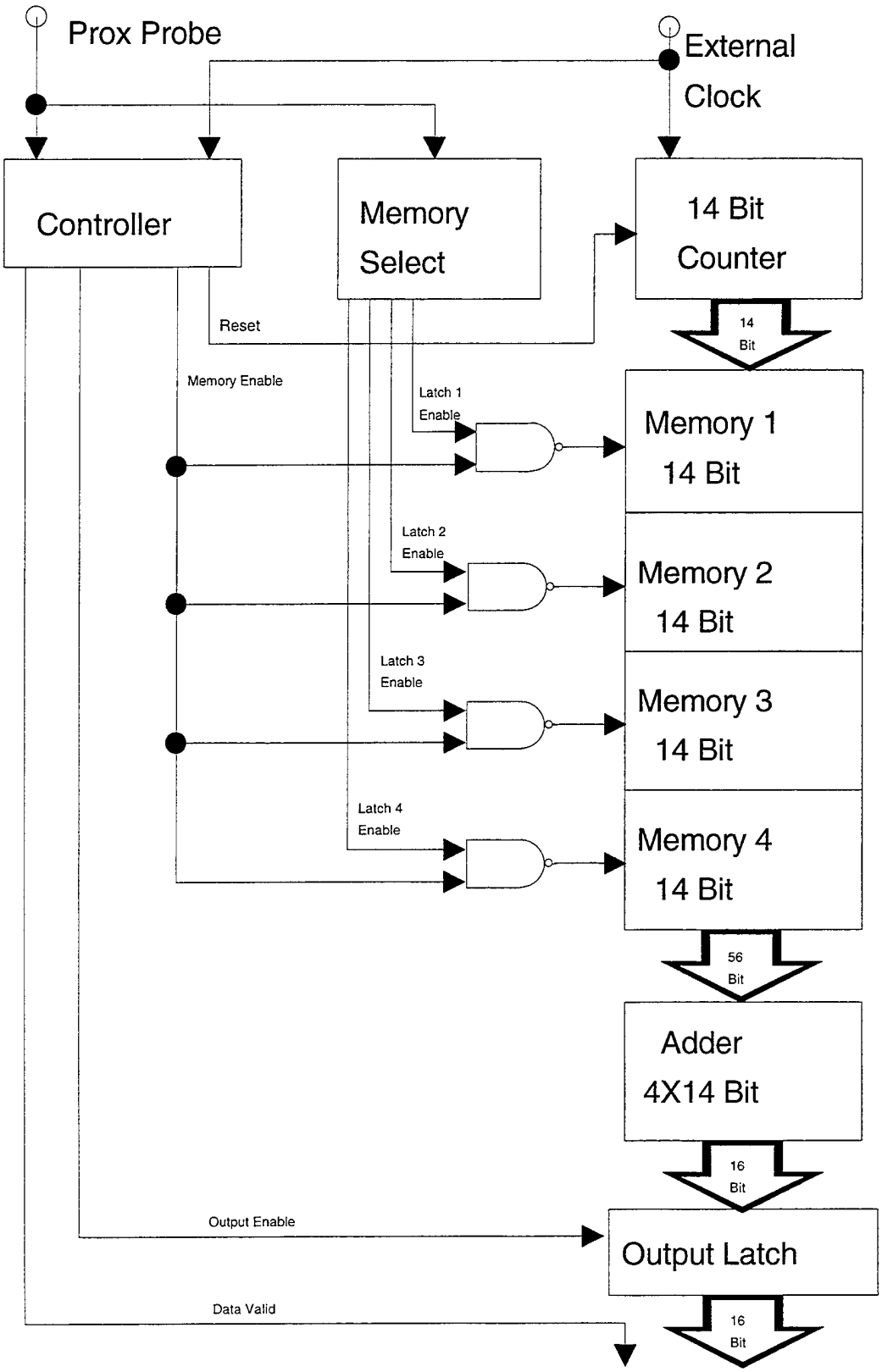

Figure 3.1. Integrated Circuit Functional Block Diagram

3.1. MEMORY SELECTION LOGIC

This system is made up of a two bit counter and a two to four bit encoder. It is used to select successively between the four different 14 bit memory arrays with each input pulse received from the proximity probe.

a. *Two Bit Counter:* The two bit counter is used to output a count from zero to three, binary, for each input pulse received. The logic diagram for this circuit is shown in Figure 3.2. The circuit is made up of two D flip-flops (dfnf311) standard cells[1] and a two input multiplexer (mux201). The clock input to the two flip-flops is from the proximity probe input, and the two bit output is from the flip-flops Q output and the Q inverse or Q' of these same two cells. The layout of the two bit counter is shown in Figure 3.3. This layout was generated by the Magic[2] CAD Tools software package. The cross hatched lines in this Figure, super imposed over the three squares representing the standard cells, are the interconnects between the individual units. The more detailed internal layout structure of the counter is shown in Figure 3.4. This drawing gives a look at the complexity of the internal layout. The different shades in this drawing represent the many different layers of the chip on the silicon wafer. The output of this layout given by the Spice[3] circuit simulation software is displayed in the Figure 3.5, for the clock pulse input as shown. The output shows the counter going from 1,1 to 0,0 to 0,1 and then to 1,0 as the clock pulses are received. The output represents Q_1, Q_0 or SA, SB, respectively. If the circuit is clocked one more time it transitions back to the beginning state or 1,1 again. There is in all cases a delay seen of about 5 ηsec from the time a pulse is received, until the outputs begin to change states. The delay is about 10 ηsec until they reach their final state. Also displayed in this output is the fact the counter is triggered by the negative edge of the received proximity pulse. This time delay of 10 ηsec is not a problem since the fastest the input pulses will be received will be 500 Hz or 2 msec.

b. *Two to four bit encoder:* The encoder is used to interpret the two bit word from the counter or "switch" section and turn one of the four enable signals to the memory arrays on, or to the read state. The logic diagram for the encoder is shown in Figure 3.6. The circuit consists of four standard cell NOR gates (norf201) interconnected as shown. The IRSIM[4] software package was used to give a logic level simulation of the encoder layout. The results for this simulation of the encoder are displayed in Figure 3.7. This proved the encoder to be working correctly. When both SA and SB are low the, L1 output is held high. The inputs to hold the other outputs high are also displayed in this diagram. The other point to be made from this drawing is only one output was allowed to go high at a time. The actual layout of this circuit is shown in Figure 3.6 along with the two bit counter section. The interconnects between units are again displayed by the cross hatched lines. The inputs SA and SB are the Q_1 and Q_0 outputs from the switch, respectively. The SA' and SB' are from the inverses of the flip flop Q outputs, or Q'. The outputs show little to no delay from the inputs to the latch enables, L1, L2, L3, and L4.

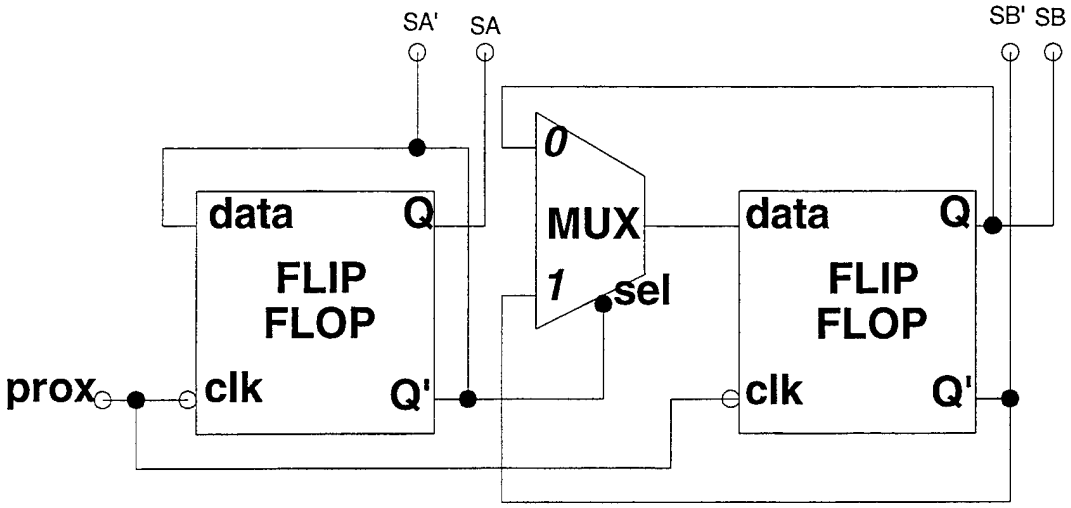

Figure 3.2. Memory Switching Circuit Logic Diagram

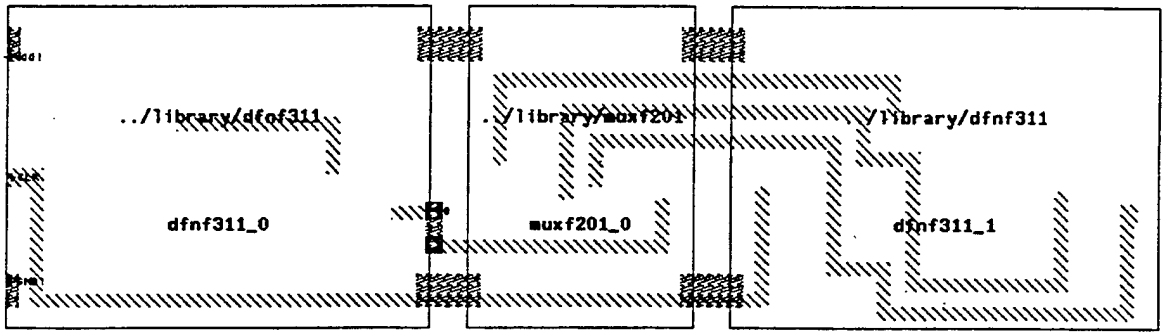

Figure 3.3. Two Bit Counter Standard Cell Layout

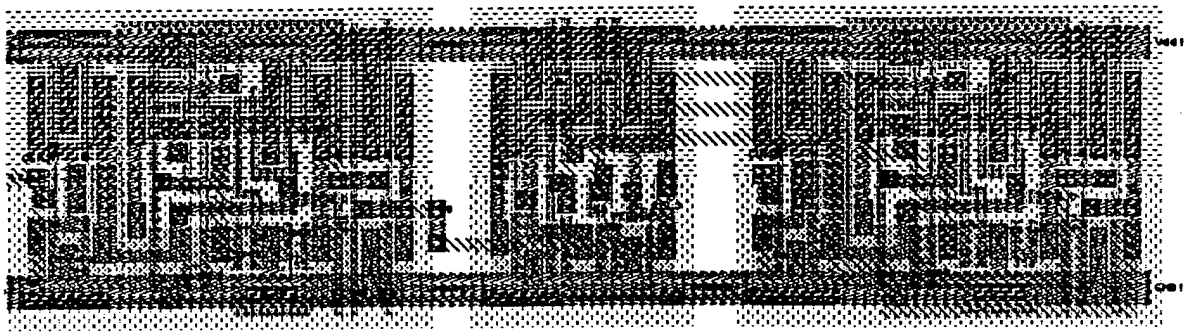

Figure 3.4. Two Bit Counter Internal Layout

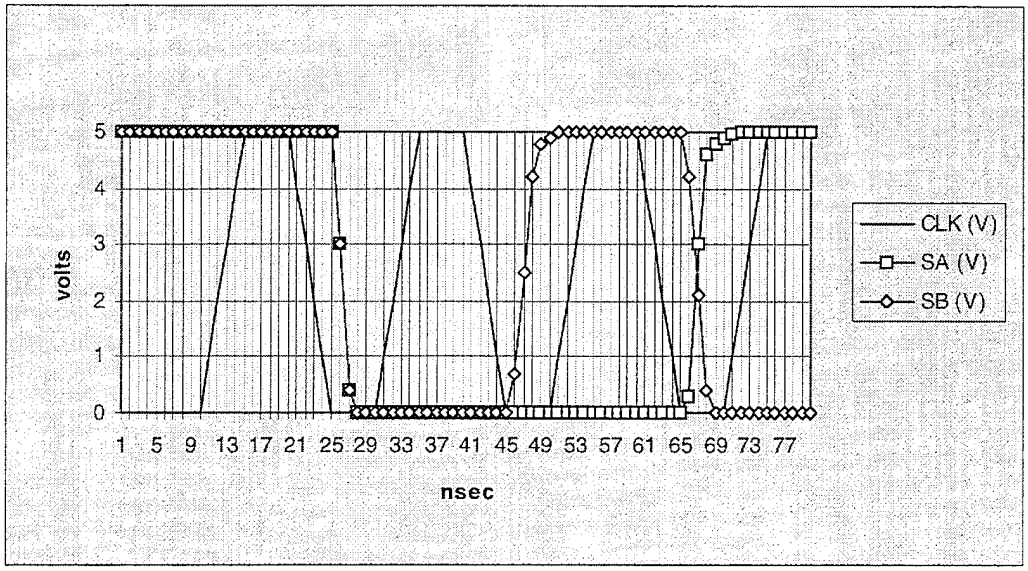

Figure 3.5. Two Bit Counter Circuit Simulation Results

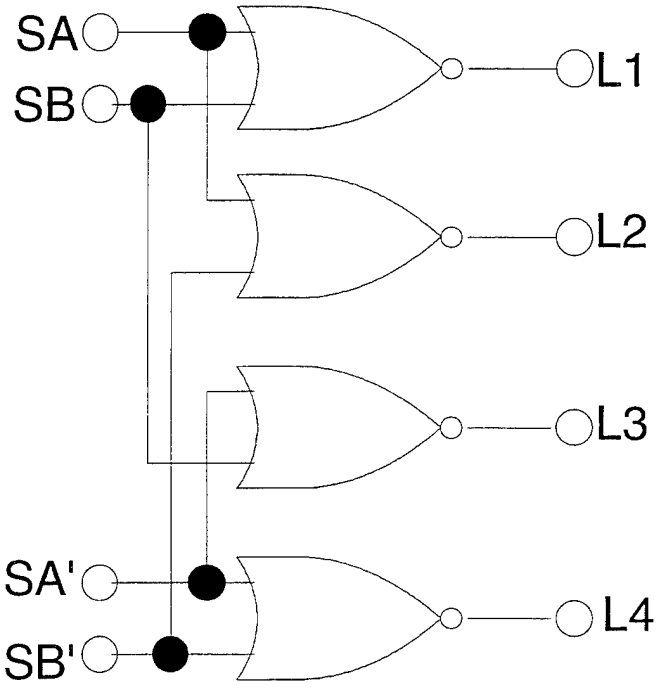

Figure 3.6. Encoder Logic Diagram

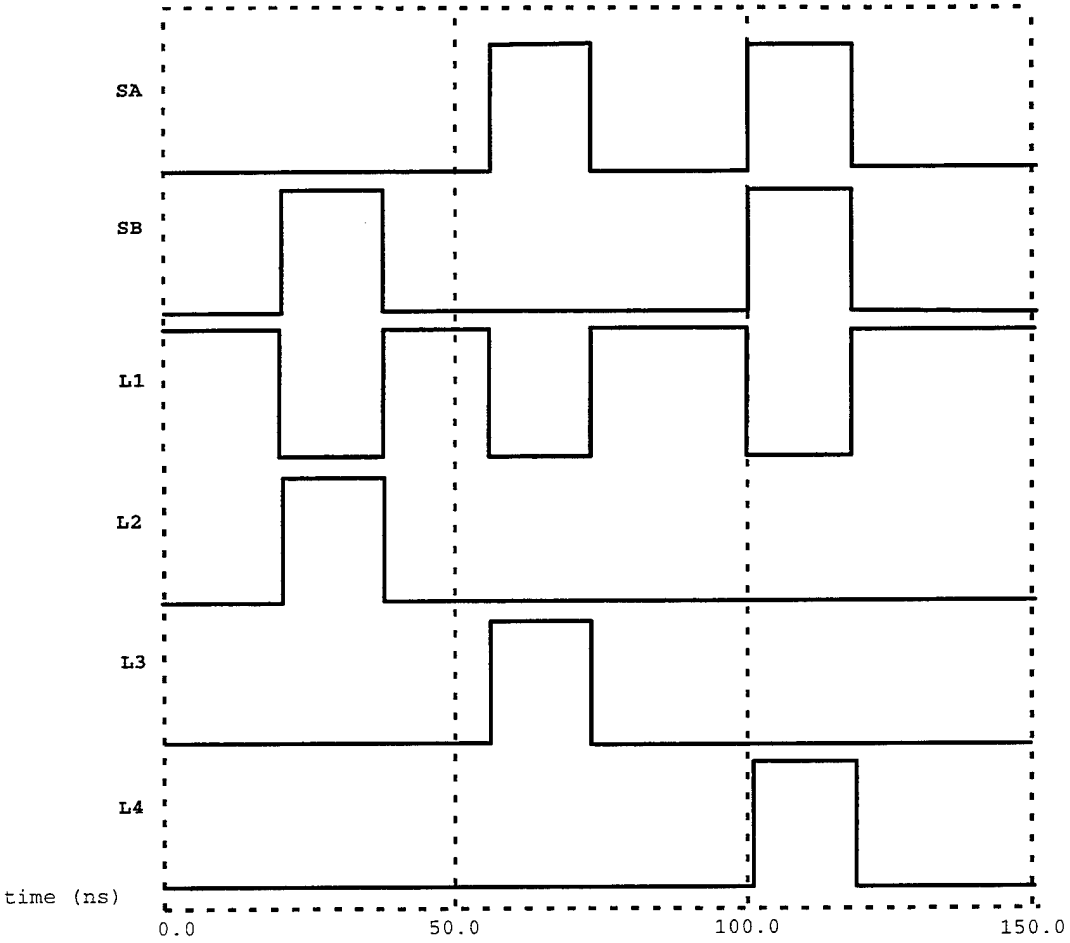

Figure 3.7. Encoder Logic Level Simulation Results

The entire memory selection logic was shown in Figure 3.6. This is made up of the encoder and the switch circuits. The combination is labeled as "select." The Spice software simulation output for the circuit is shown in Figures 3.8 through 3.12. Figure 3.8 displays the overall output signal from each of the four enables as clock input pulses are received. The remaining four drawings show the individual output line responses for clarity. For this example the proximity pulses were 2ms apart. The simulation results showed a different enable going high for each pulse while the other three remained low. The enables were not in the expected order of L1, L2, L3, and then L4. This was caused by not routing the Q and Q_b outputs to the NOR gate inputs as planned during the laying out of the design. Since the numbering scheme used in the layout is arbitrary and the circuit does perform correctly, this will not be a problem for circuit operation. The overall goal of this section of the chip was accomplished in that one memory enable was allowed to go high at a time while the other three were held low.

The geometry of the unit is also an important consideration given the number of chip functions required to fit into the 1.8 mm by 1.8 mm surface area of the silicon wafer. The overall area required by this particular unit is approximately 60 μm by 325 μm. The geometry for each unit will become important when trying to fit all the individual parts making up the functions of the whole chip into one surface area. The design of this chip requires many interconnections between the functional units. The large amount of surface area required for those interconnecting metal runs also has to be planned throughout the layout.

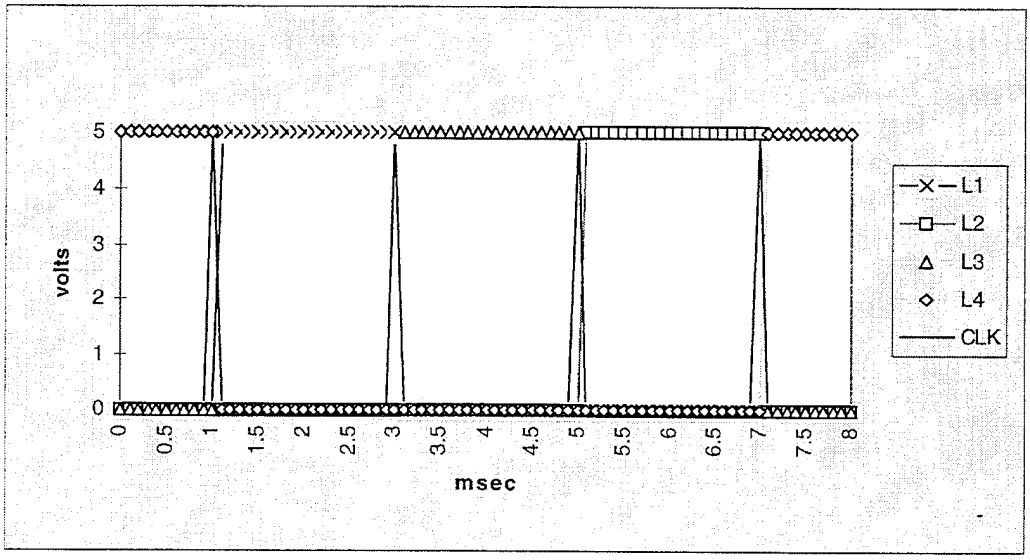

Figure 3.8. Selection Logic Simulation Output

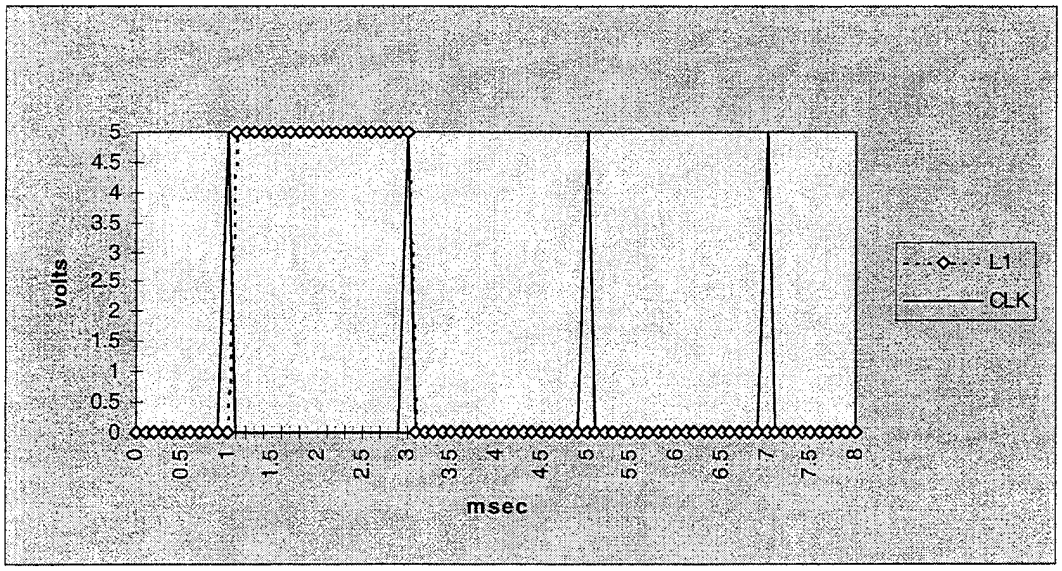

Figure 3.9. Selection Logic L1 Simulation Output

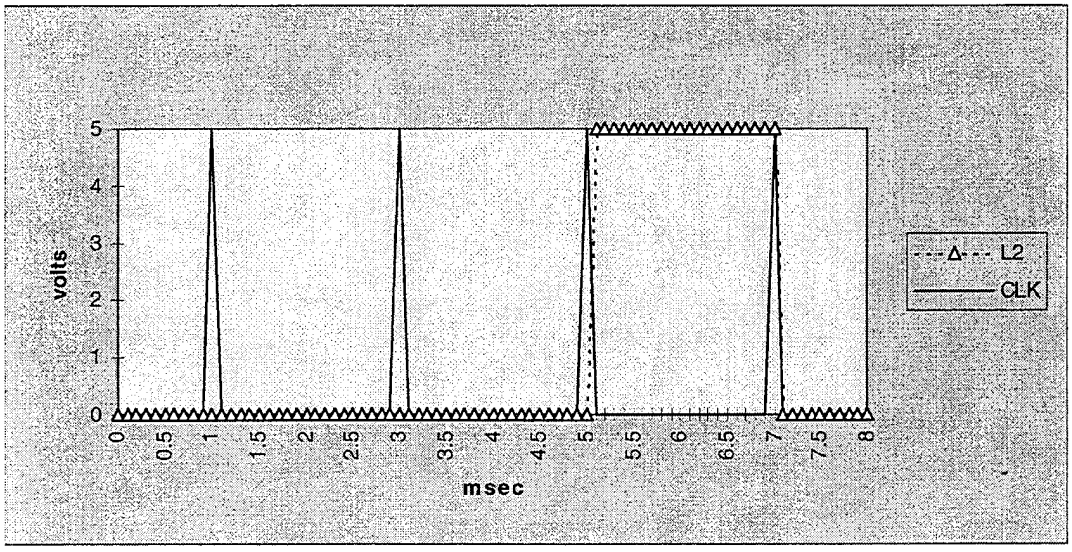

Figure 3.10. Selection Logic L2 Simulation Output

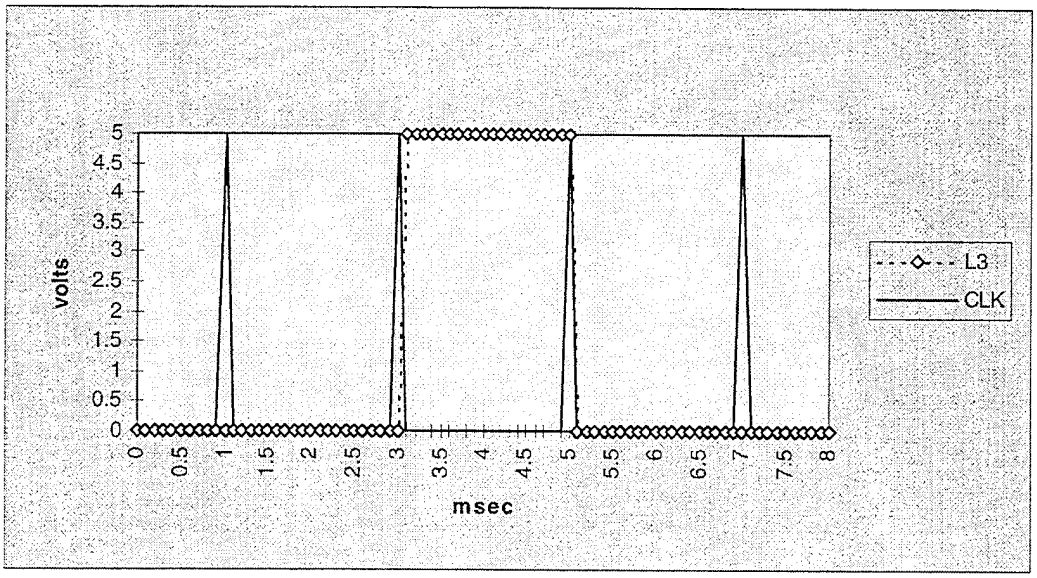

Figure 3.11. Selection Logic L3 Simulation Output

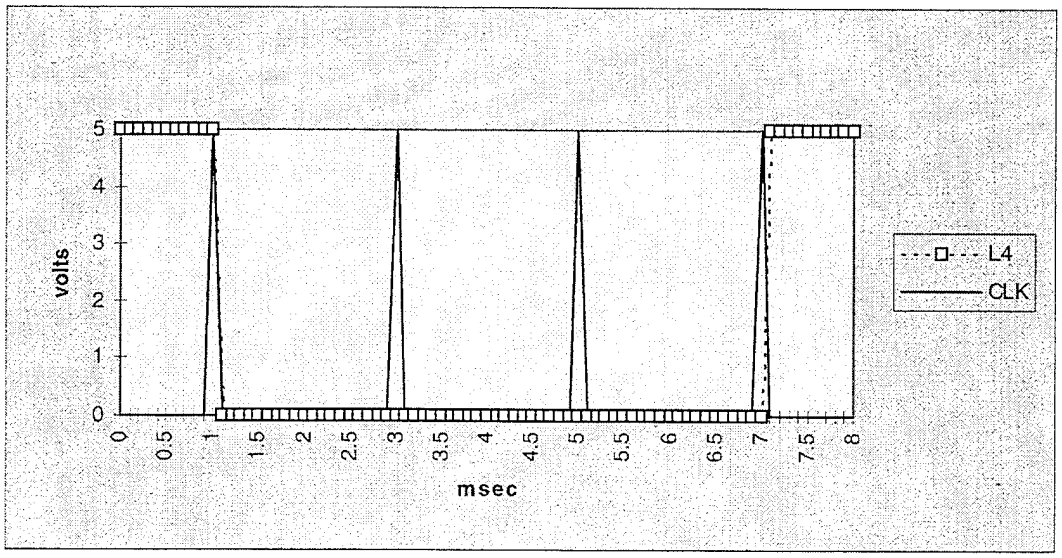

Figure 3.12. Selection Logic L4 Simulation Output

3.2. TIME INCREMENT COUNTER

This subsystem of the design measures the elapsed time between pulses from the proximity probe using a 150 kHz external clock. The basic standard cells used to make up this part of the system are 14 D flip flops with reset (dfrf311), 13 two input multiplexers (muxf201), and 12 two input AND gates (nanf211). The logic diagram, Figure 3.13, is equivalent to the two bit counter used in switch for the first two bits, but then adds the AND gate (invert NAND) for the remaining bits. The AND gate is used to inhibit the next stage or the following significant bit until both preceding bits are high. With the AND gate output forced low by the data out of the two preceding bits, the multiplexer is forced to select the data out of the current bit. Because of this the output of the multiplexer will be the same as the output of the flip flop. The output of the multiplexer is used to drive the input of the same flip flop. Therefore, the flip flop will not change state when clocked by the external source. When the two significant bits of the preceding section do go high, the multiplexer is allowed by the AND gate to select the flip flop inverted output. Then when clocked by the external source, the flip flop will change state. The arrangement is chained together to form the remaining 11 bits of output required by the design. The final addition to this subsystem is the reset line. It is normally held high during the counting process. When the reset is allowed to go low, the outputs of all 14 flip flops go low. The reset is used to zero out the counter between the proximity pulses in order to restart the counting for the next timing interval.

The layout for this circuit is shown in Figure 3.14 for the first three least significant bits, with the overall architecture for all 14 bits shown in Figure 3.15 on the next page. The first three significant bits were left in the expanded mode of the computer aided design (CAD) software in Figure 3.15 to give a reference point in viewing the layout. The counter is shaped in a single line of standard cells to make the outputs accessible to the memory arrays. It is bent as shown to fit around the outer edge of the tiny chip surface. This pattern gives an overall geometry of approximately 70 μm width. The outside dimensions are 1050 μm along the top, 1460 μm on the right edge, and 600 μm on the bottom edge.

IRSIM was used to display the performance of this part of the design and to validate its operation. The external clock pulses were input through the node labeled "IN". The first four bits were monitored, I0 through I3, because it would be impractical to count high enough to view all the bits changing. As can be seen in Figure 3.16, the system counted correctly up to binary four where the reset input, RST, was tested by allowing it to fall low. The RST line was also allowed to fall low at the beginning of the simulation run in order to reset all the bits to obtain a valid count. As can be seen in the simulation output, until RST is originally set low, there is no known value in the I1 through I4 outputs. This uncertain value is represented by the simulator as the gray shaded areas on the output plot. This is also true in the actual chip implementation. It cannot be guaranteed that all zeros are stored in the counter memory elements on power up until the initial reset command is issued from the controller. This is not a problem with the chip

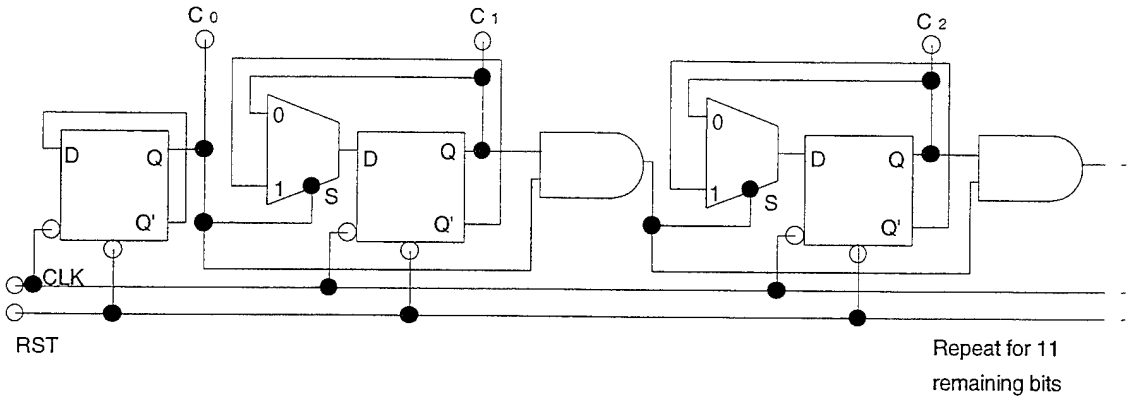

Figure 3.13. The 14 Bit Counter Logic Diagram

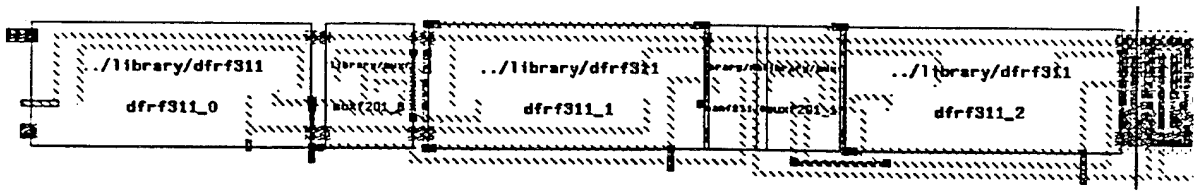

Figure 3.14. Counter Layout

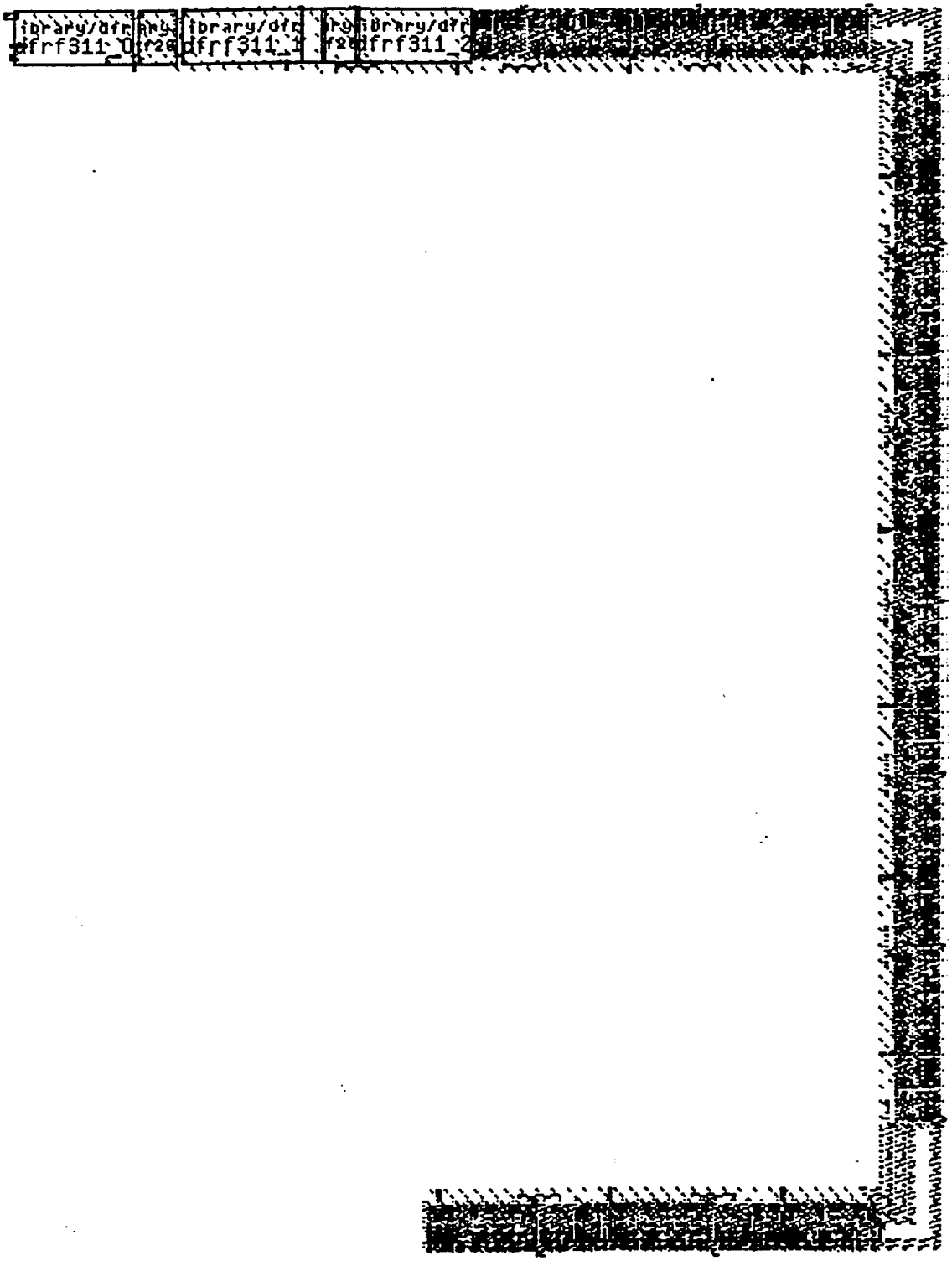

Figure 3.15. The 14 Bit Counter Architecture

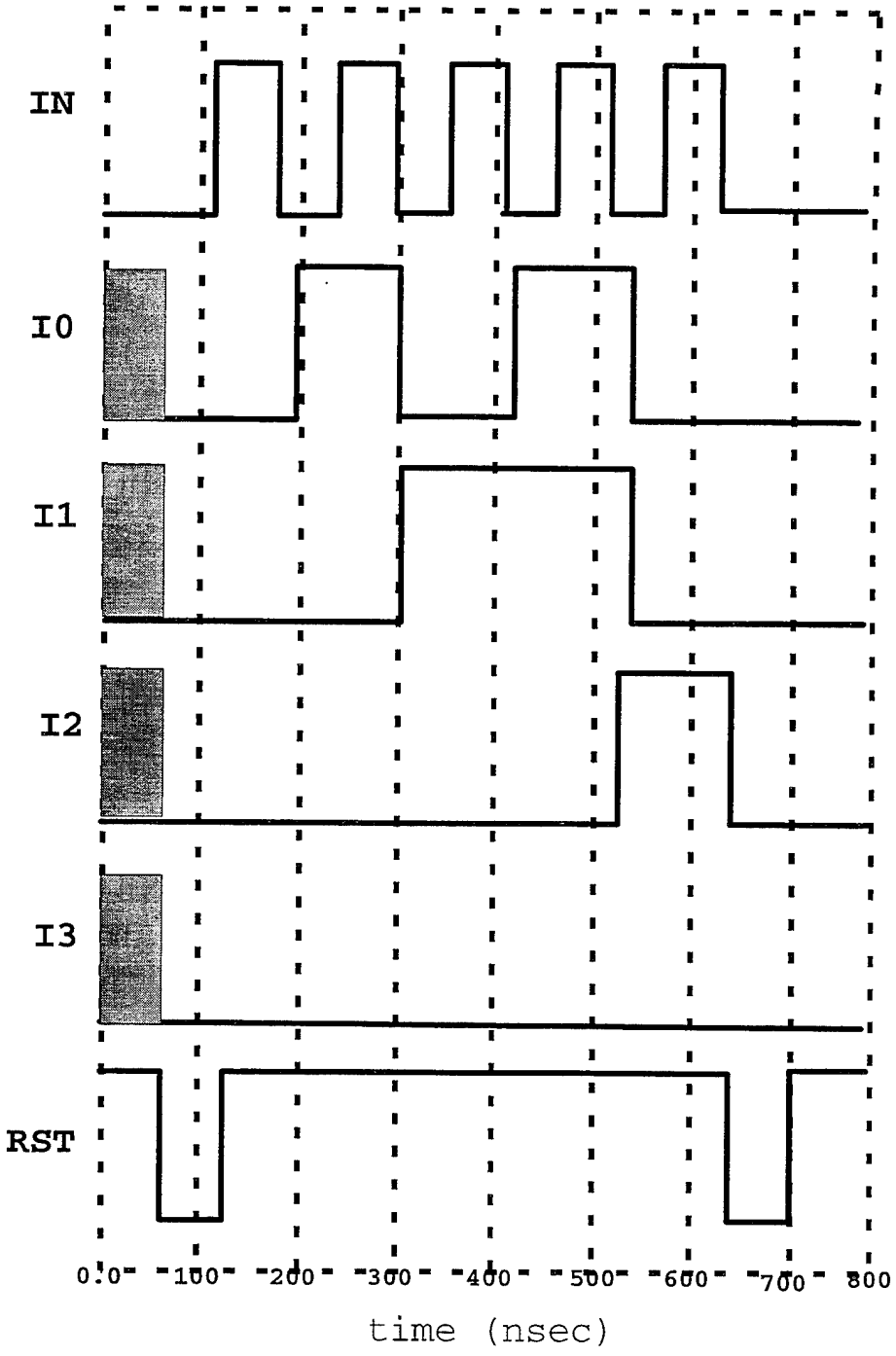

Figure 3.16. Counter Logic Level Simulation

operation, however, it just means that the data output from the chip will be incorrect for the first 26.4 μsec until the original invalid data are overwritten in the memory registers. The reset functioned correctly, resetting all the bits to zero in both cases. Also displayed in this Figure was the fact that this counter is negative edge triggered; as it can be seen the count output did not change until the clock pulse started low from high. The delay in the system from receiving a negative edge pulse to the logic level of the output bits changing was about 4.6 ηsec to 5 ηsec. Since data are available at all inputs at the time a negative edge pulse is received, and all flip-flops receive clock pulses at the same time, all bits will change with relatively the same delay, even out to the 14th bit.

3.3. 4X14 BIT MEMORY ARRAY

The 14 input data lines from the counter are input to the data ports of all four memory arrays. In this arrangement, one bit from the counter connects to all four of the arrays in the corresponding bit. Since only one memory array is allowed to be active or reading at one time, the data will only be read to the active array bit even though it is available to all four of the array's input ports. A read from the clock is stored by allowing the enable from the selection logic to go low and clock in the data on the input lines from the counter. In this manner, all 14 bits of the output number at the counter are stored at the same time into a single array. The logic diagram for this section is shown in Figure 3.17.

The 4X14 bit memory array was created entirely with D flip-flops (dfnf311). The 4X14 bit array is made up of two 2X14 bit sections placed together. The layout of two memory cells in the 2X14 bit array is shown in Figure 3.18 with an entire array shown in Figure 3.19. The entire 4X14 memory section is shown in Figure 3.20. The total geometry used by this section is 240 μm by 1040 μm. No simulation results have been generated on the memory section, since it is just implementing D flip-flop standard cells without any other logic gates.

The memory array activation logic resides next to the memory arrays. It consists of four two input NAND gates. The memory array is activated by the controller setting the memory enable line high, in conjunction with the memory selection logic setting one of the four memory select lines to high. The four memory select lines go to one specific NAND gate each, while the memory enable line goes to all four NAND gates. This allows only one gate to be actively reading at a time. The layout for the memory activation is shown in Figure 3.21.

The other purpose for placing the NAND gates in front of the memory arrays was to allow some input buffering. The relatively small geometry transistors in the standard cells of the controller and selection logic would have fanned out trying to activate the 14 flip flops. This is due to the fact only a small amount of current can be drawn through a small surface area transistor. The NAND gates provide the larger area transistors necessary to activate the parallel memory arrays.

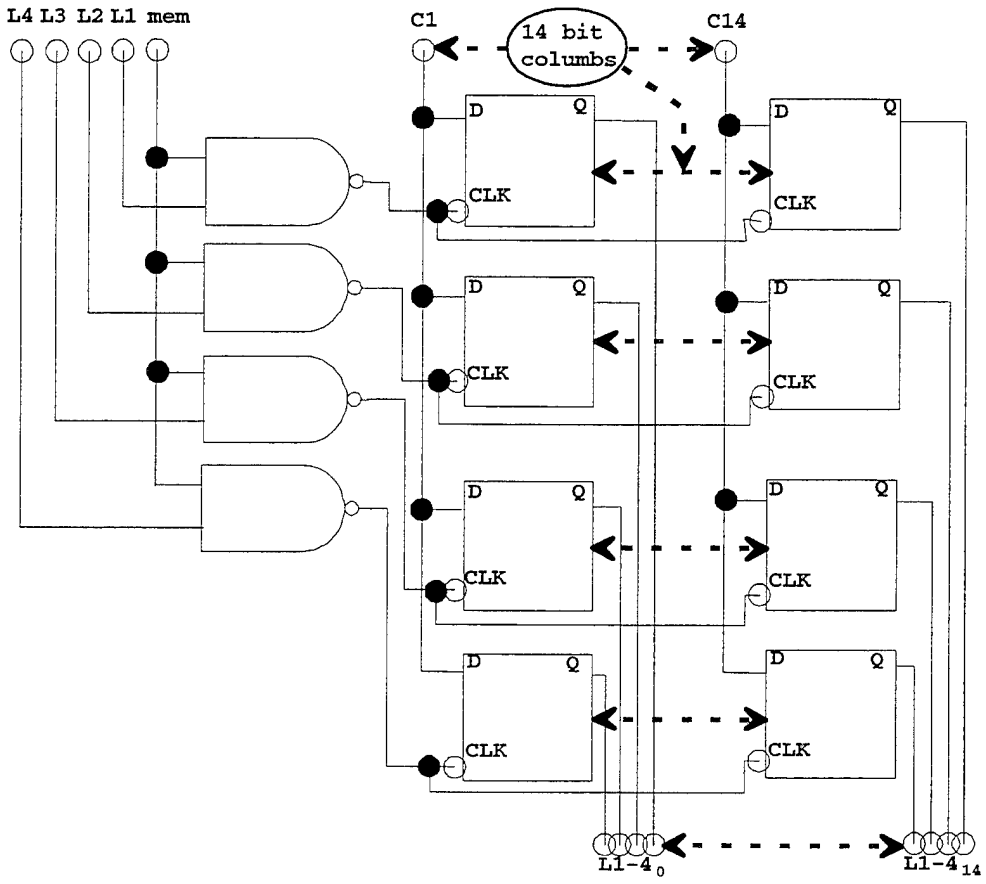

Figure 3.17. Memory Logic Diagram

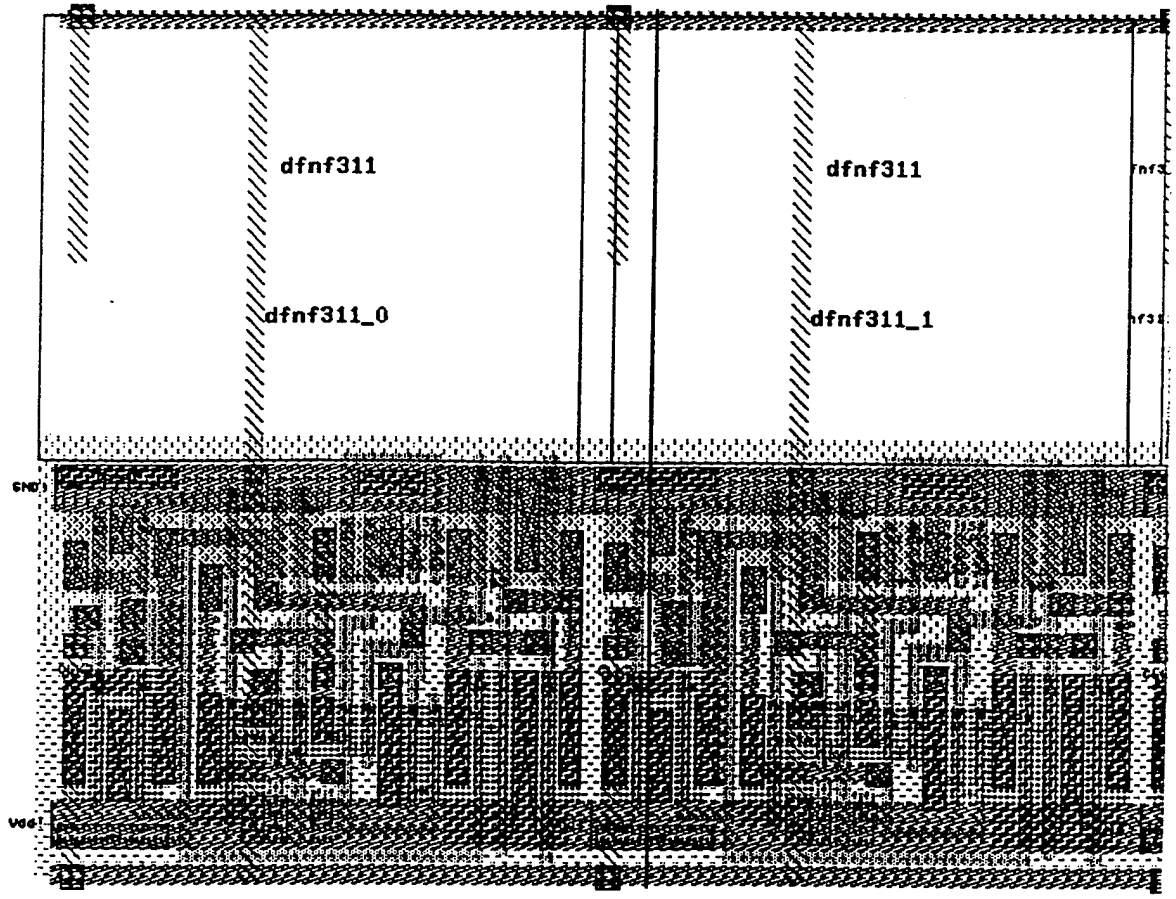

Figure 3.18. Two Bits of the Memory Array Architecture

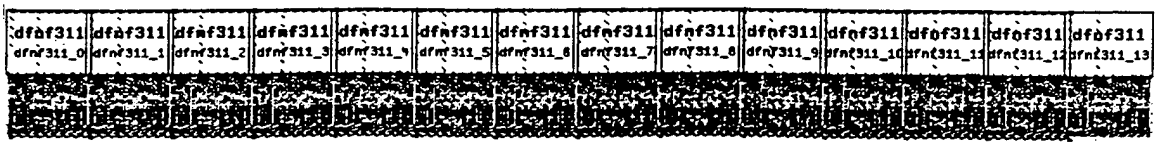

Figure 3.19. The 2X14 Bit Memory Array

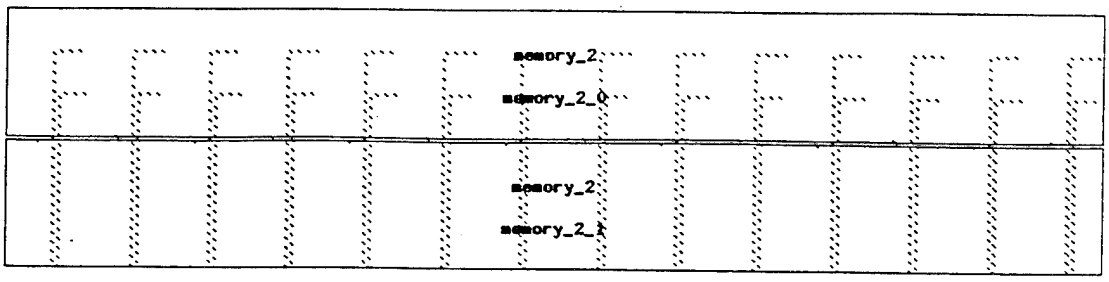

Figure 3.20. The 14X14 Memory Array Layout

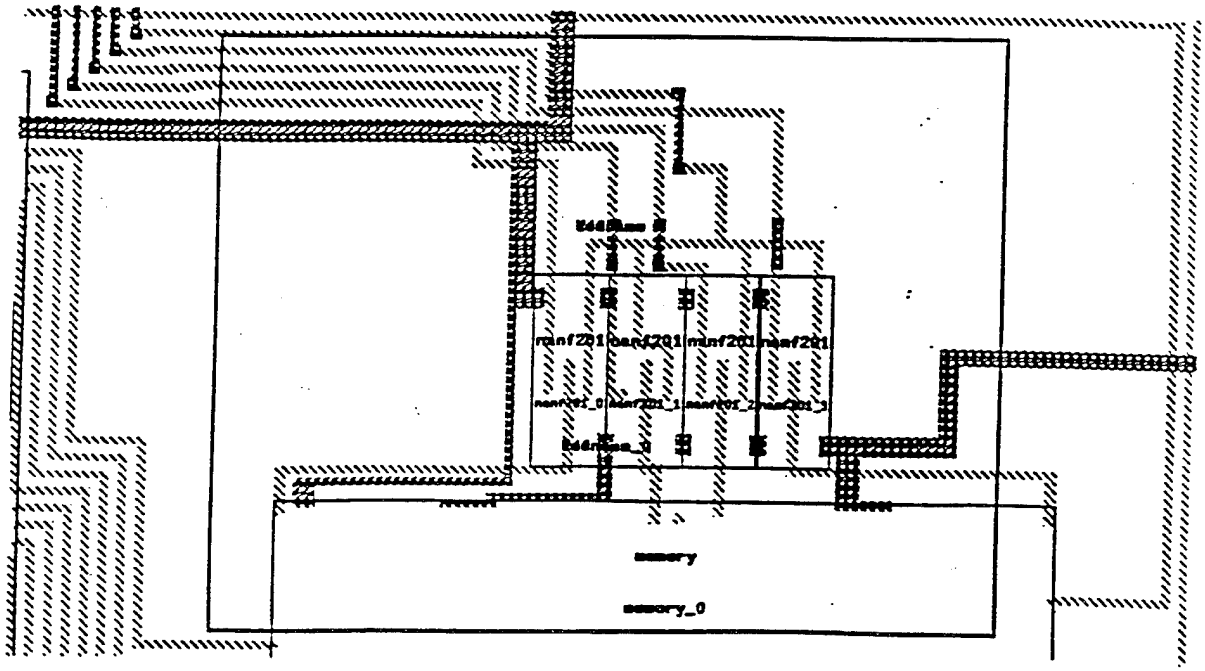

Figure 3.21. Memory Activation Layout

3.4. ADDER SECTION

The adder function is to continuously add the numbers stored in the four 14 bit memory arrays. This part of the circuit is not clocked, but is allowed to change status with the changes in the memory section in a ripple carry fashion. As the bits on the 56 inputs change, the adder will react to the change immediately. The logic diagram for the adder is shown in Figure 3.22. The adder is connected directly to the outputs of the four different memory arrays. There are 56 inputs to the adder and 16 outputs. The two least significant bits (S_0,S_1) of the adder's output are used for the decimal portion of the divide by four function while the remaining 14 bits are the whole number portion. The basic form of the adder is three rows of one bit adders. Two of the rows are used to add the corresponding bits of two memory arrays while the third row is used to add the results from the first two additions. All carry outs are added into the next most significant bit in the row. The adder architecture is displayed in Figure 3.23 with one bit or three one bit adders, displayed in Figure 3.24, and was constructed with 43 one bit full adders .

The adder was verified by logic level simulation with four known inputs. The output was then checked to insure it corresponded to the correct answer for the addition of the four numbers. The results of one of the simulations is shown in the table below:

INPUT ARRAY	BINARY INPUT	DECIMAL EQUIVALENT
L1	00111000100000	3616
L2	00101001101011	2667
L3	10100011001000	10440
L4	10000001101100	8300
RESULTANT OUTPUT	0110000110111111	25023

The actual simulation response for the verification test below to the inputs L1, L2, L3, and L4 is displayed in Figure 3.25. The Test Signal Input is a display of one of the adder inputs. All inputs were allowed to go to their simulation position at the same time. This line allows the output switching time to be correlated with the inputs on the same logic graph. Again, the shaded regions appeared in the simulation output. This time it was due to the fact, at the begin of the simulation run no inputs were specified until time was 0.0 seconds. Therefore, the simulation did not know what level to set the outputs too until 0.0 seconds when all inputs become zero. Even though this is at the beginning of the simulation run, the all zero inputs must propagate through the adder to the outputs. The shaded regions or unknown state remained until the output was given valid data. As can be seen in Figure 3.25 this occurred at about 13.3 ηsec. The output of the adder, S_0-S_{15}, was correct as can be seen above, after the data settled out. The output showed level switching as the inputs propagated across the adders, and settled to the final sum of 25023. The settling time for this simulation was about 17.5 ηsec after the test signals were set to their simulation positions. This propagation time was expected for a ripple-carry type adder

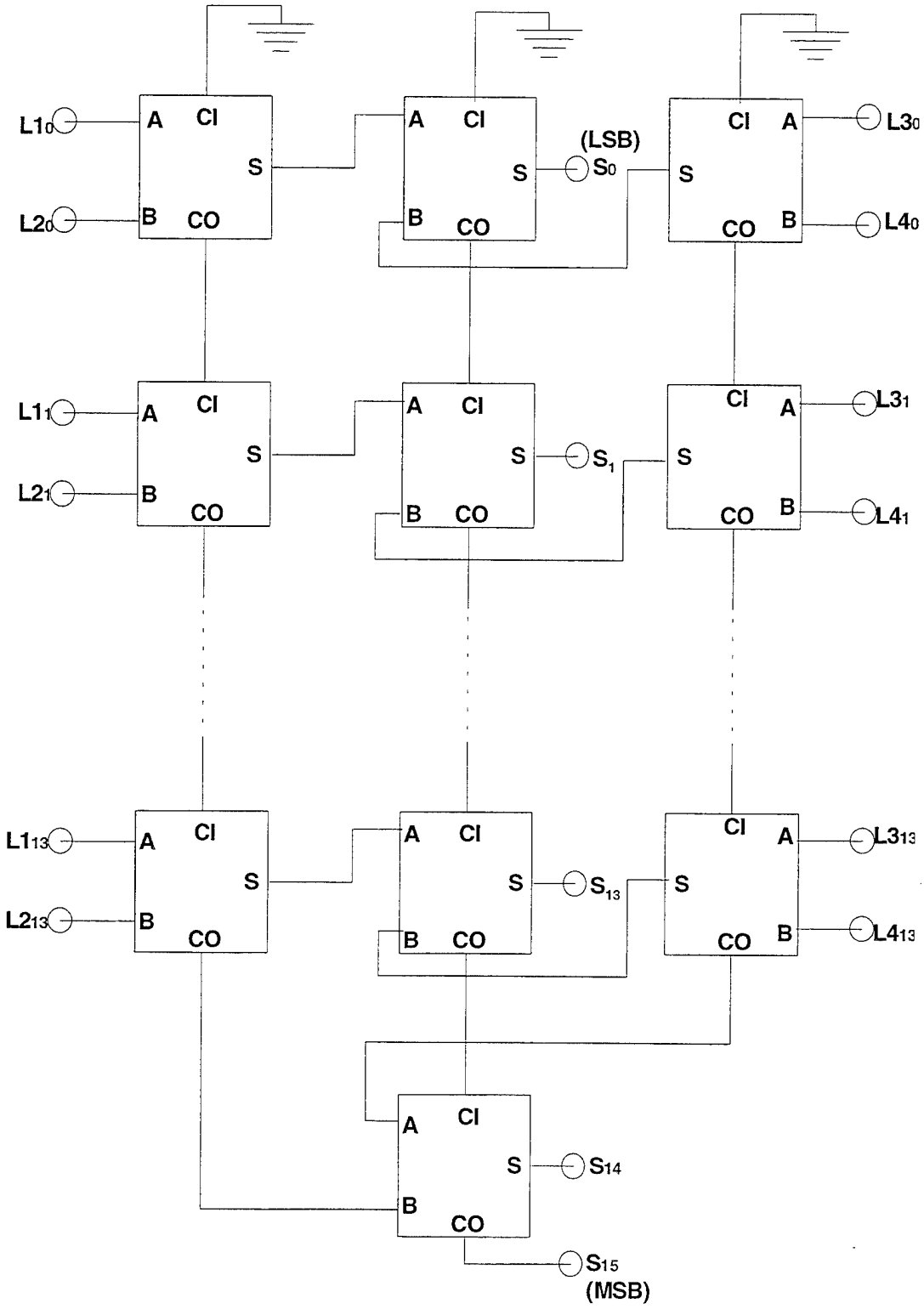

Figure 3.22. Adder Logic Diagram

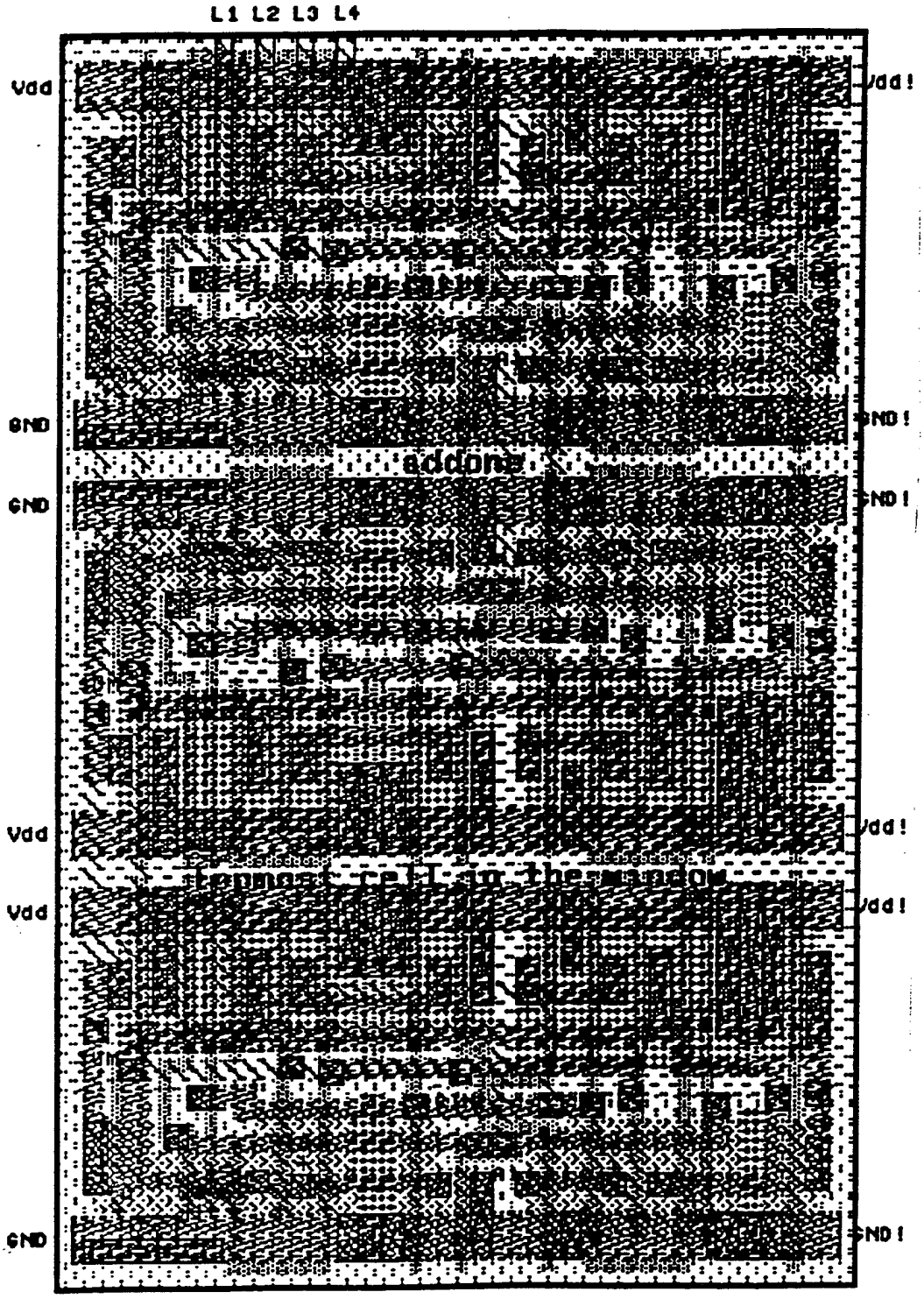

Figure 3.23. One Bit Adder Architecture

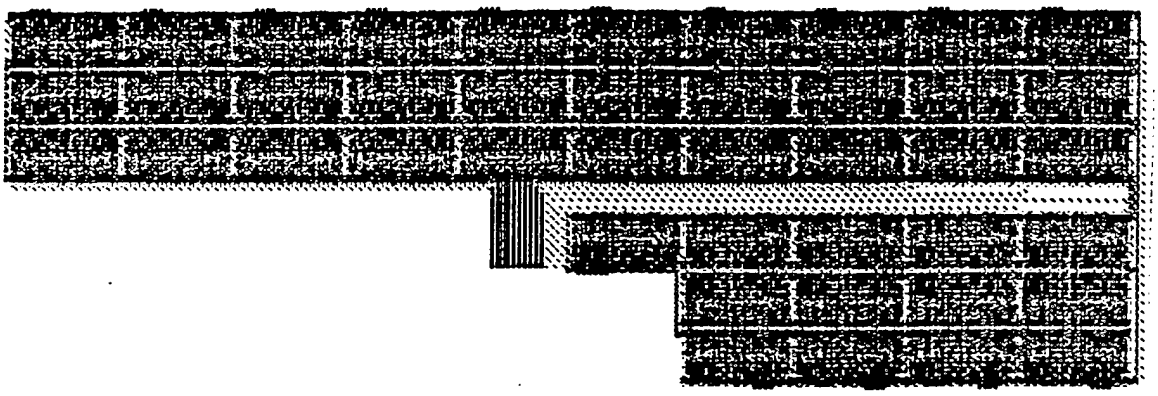

Figure 3.24. Adder Architecture

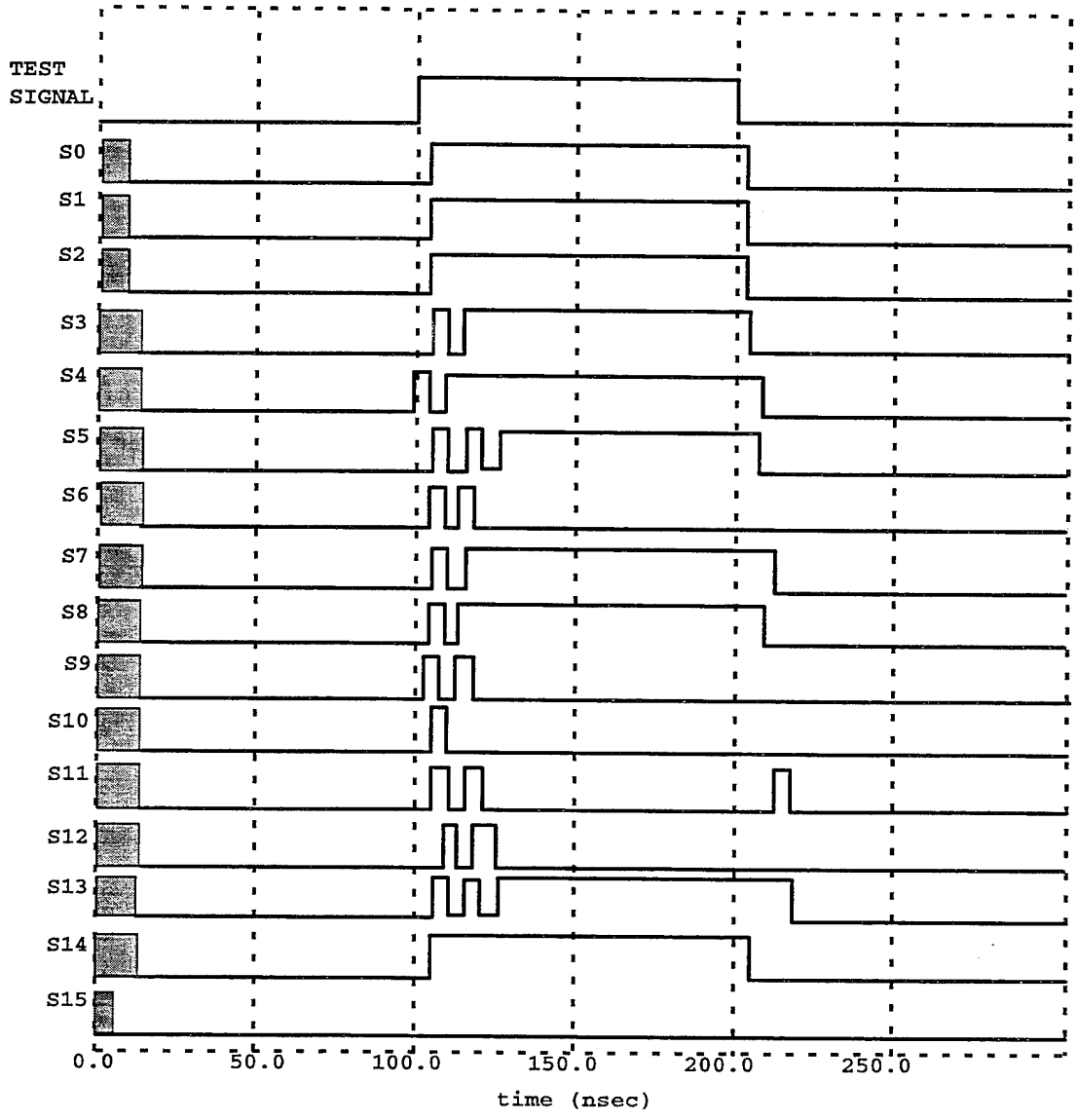

Figure 3.25. Adder Logic Level Simulation Output

3.5. OUTPUT LATCH

This section was incorporated into the final design to allow the output pins to be held at the last value read from the adder. This keeps the output pins from settling with the adder during a ripple carry function. The output latch is enabled by the controller to allow it to read the adder and then disabled so the value is held at the output side while the adder fluctuates while adding the next read from the counter into the a memory array. This buffers the output pins from this fluctuation. The output latch layout is identical to one of the arrays of the memory section, using D flip-flop (dfnf311) standard cells. Refer to the diagrams of the memory section for the layout and architecture. The only difference being the output latch is 16 bits long to carry the two least significant bits to the output pins. This gives the user of the chip the option of having the decimal remainder from the divide by four function.

3.6. CONTROLLER

This subsystem was incorporated into the design to synchronize the functions of the other subsystems on the chip to allow them to work together in the proper order. The controller is a state machine using the proximity probe input to begin its cycle of eight states. The 150 kHz external clock is used to switch the controller through its states after the initial proximity pulse is received. The states and actions executed at each state are determined by the logical order the chip was required to operate. This order is for the chip to count at 150 kHz until a proximity pulse is received. At this point a chain of events is to be initiated. This chain of events includes turning off the data valid bit, reading the count into the current memory location, resetting the counter for the next time period, enabling the output latch to send the new result of the counter to the output pins, and then finally turning back on the data valid bit. After all eight states have been traveled through, the controller goes back to the original state, counting clock pulses and waiting for another proximity probe pulse to begin the cycle again. The state diagram showing the controller flow path is in Figure 3.26 and the state table with the action performed at each state is shown in the table below. The abbreviations MEM, LAT, RST, and DVL stand for the memory enable, output latch enable, counter reset, and data valid, respectively.

Present State			Next State PRX=0			Next State PRX=1			Present Output				Action Taken
A	B	C	A	B	C	A	B	C	MEM	LAT	RST	DVL	
0	0	0	0	0	0	0	0	1	0	0	1	1	None
0	0	1	0	1	0	0	1	0	0	0	1	0	Turn off data valid
0	1	0	0	1	1	0	1	1	1	0	1	0	Enable memory
0	1	1	1	0	0	1	0	0	0	0	1	0	Disable memory
1	0	0	1	0	1	1	0	1	0	0	0	0	Reset counter
1	0	1	1	1	0	1	1	0	0	1	1	0	Enable output/count
1	1	0	1	1	1	1	1	1	0	0	1	0	Disable output
1	1	1	0	0	0	0	0	0	0	0	1	1	Turn on data valid

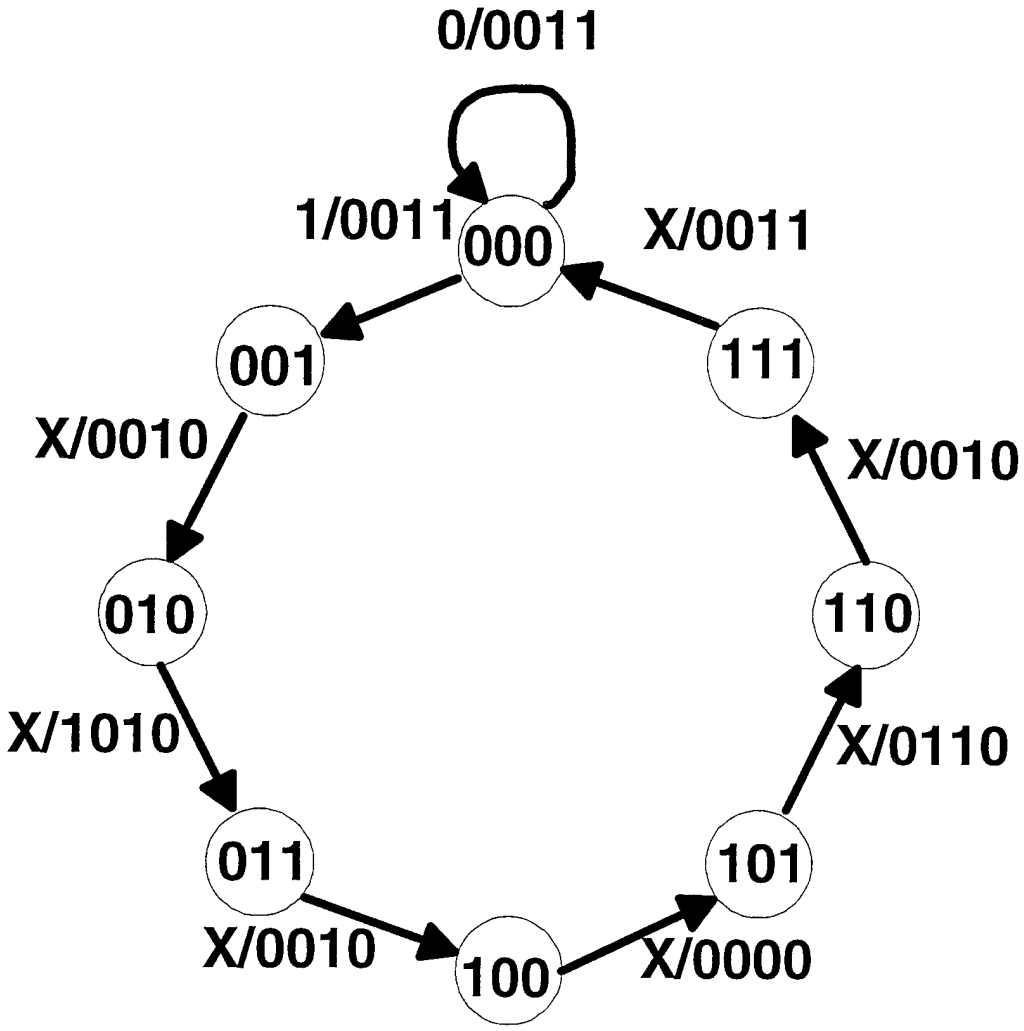

Figure 3.26. Controller State Machine Diagram

The state diagram shows the order the states defined in the table travel. The numbers next to the arrows in this diagram describe the controller output and next state conditions. The four digit number to the right of the back slash corresponds to the present output column of the previous table. The number to the left of the back slash is the proximity probe input required for the transition to the next state when a clocking pulse is received. In this case all the required signals after the first state or "000" is "X" or don't care. This means the state machine will traverse through all eight states after the original proximity pulse is received at each clock pulse regardless of the current proximity probe signal.

The controller programmable logic array (PLA) is a pseudo nmos device and was designed with the aid of the Berkeley CAD tools programs eqntott[5], espresso[6], and mpla[7]. Eqntott is a Boolean logic equation to truth table generator. The logic equations defining the state table operation above for this program to act upon were as follows:

A=(A AND NOT C) OR (A AND NOT B) OR (NOT A AND B AND C)
B=(B AND NOT C) OR (NOT B AND C)
C=(B AND NOT C) OR (A AND NOT C) OR (NOT C AND PRX)
MEM=NOT A AND B AND NOT C
LAT= A AND NOT B AND C
RST=NOT A OR B OR C
DVL=(NOT A AND NOT B AND NOT C) OR (A AND B AND C)

The output from this program was the following truth table:

PRESENT STATE				NEXT STATE			OUTPUTS			
A	B	C	PRX	A	B	C	MEM	LAT	RST	DVL
0	0	0	X	0	0	0	0	0	0	1
0	X	X	X	0	0	0	0	0	1	0
X	X	0	1	0	0	1	0	0	0	0
X	0	1	X	0	1	0	0	0	0	0
X	X	1	X	0	0	0	0	0	1	0
0	1	0	X	0	0	0	1	0	0	0
X	1	X	X	0	0	0	0	0	1	0
X	1	0	X	0	1	1	0	0	0	0
0	1	1	X	1	0	0	0	0	0	0
1	0	X	X	1	0	0	0	0	0	0
1	X	0	X	1	0	1	0	0	0	0
1	0	1	X	0	0	0	0	1	0	0
1	1	1	X	0	0	0	0	0	0	1

Espresso was used next to minimize and optimize the above truth table into the following truth table:

PRESENT STATE				NEXT STATE			OUTPUTS			
A	B	C	PRX	A	B	C	MEM	LAT	RST	DVL
1	0	1	X	1	0	0	0	1	0	0
0	1	0	X	0	0	1	1	0	0	0
X	X	0	1	0	0	1	0	0	0	0
0	0	0	X	0	0	0	0	0	1	1
1	1	1	X	0	0	0	0	0	1	1
0	1	1	X	1	0	0	0	0	1	0
1	X	0	X	1	0	1	0	0	0	0
X	0	1	X	0	1	0	0	0	1	0
X	1	0	X	0	1	0	0	0	1	0

This output was then used with mpla to generate the actual PLA circuit layout for the controller. The logic diagram for the controller is displayed in Figure 3.27. The actual layout generated is displayed in Figure 3.28. The three D flip-flops shown in this layout were added to the circuit generated by mpla in order to allow the PLA to be clocked through its eight states. The next state of the controller is held at the outputs and is allowed to transition through the latches to the new state inputs when a 150 kHz clock pulse is received. The corresponding output for the new state is then generated by the PLA array as well as the next state to transition too at the following clock pulse. This next state value is placed at the data inputs for the flip-flops.

The simulation for the controller is shown in Figure 3.29. Each step shown after the initial proximity probe input, occurs on the positive going clock cycle pulse. Also displayed in this diagram are the present state output, ABC. With the 150 kHz clock driving the circuit, the entire operation from receiving the proximity probe pulse, clocking through all eight states, and returning to the beginning wait state is 267μsec. The fastest rate the proximity pulses will be received for the CRF application is 500 Hz or one pulse every 2 msec. This will give the controller enough time to perform its function between proximity probe pulses.

It was noted from the state table, the controller reads the counter into memory in the third state and does not reset and enable the counter until the sixth state. This will

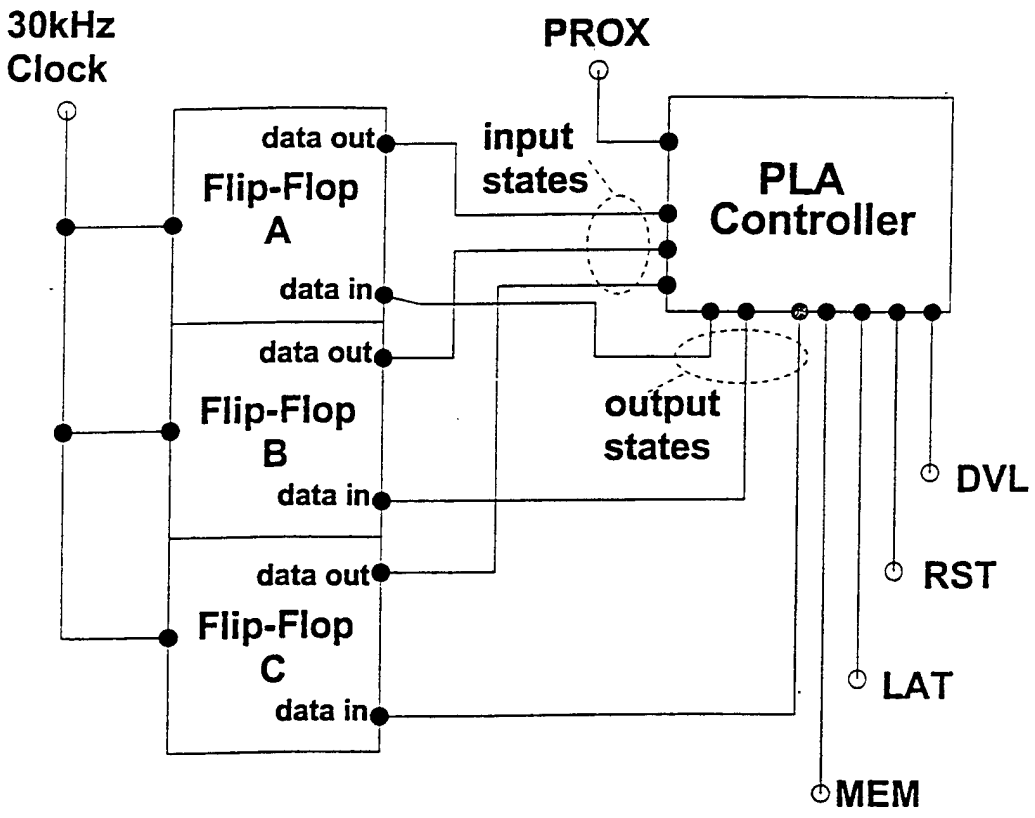

Figure 3.27. Controller Logic Diagram

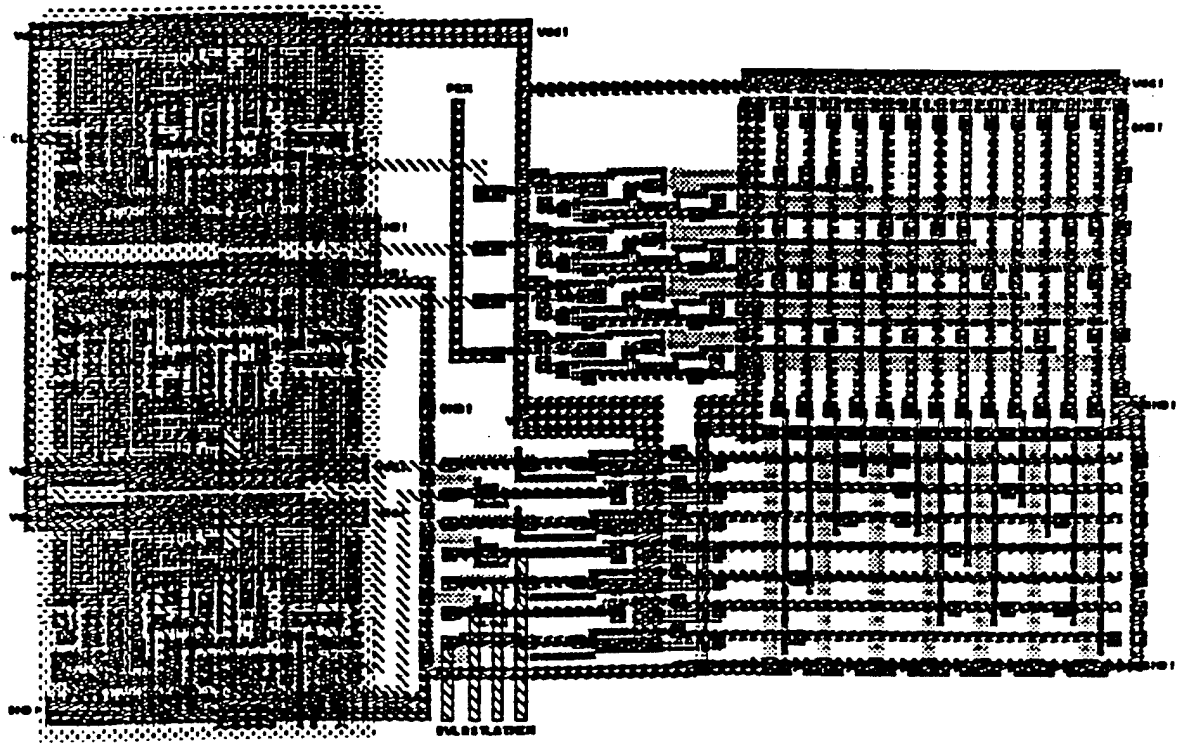

Figure 3.28. Controller Architecture

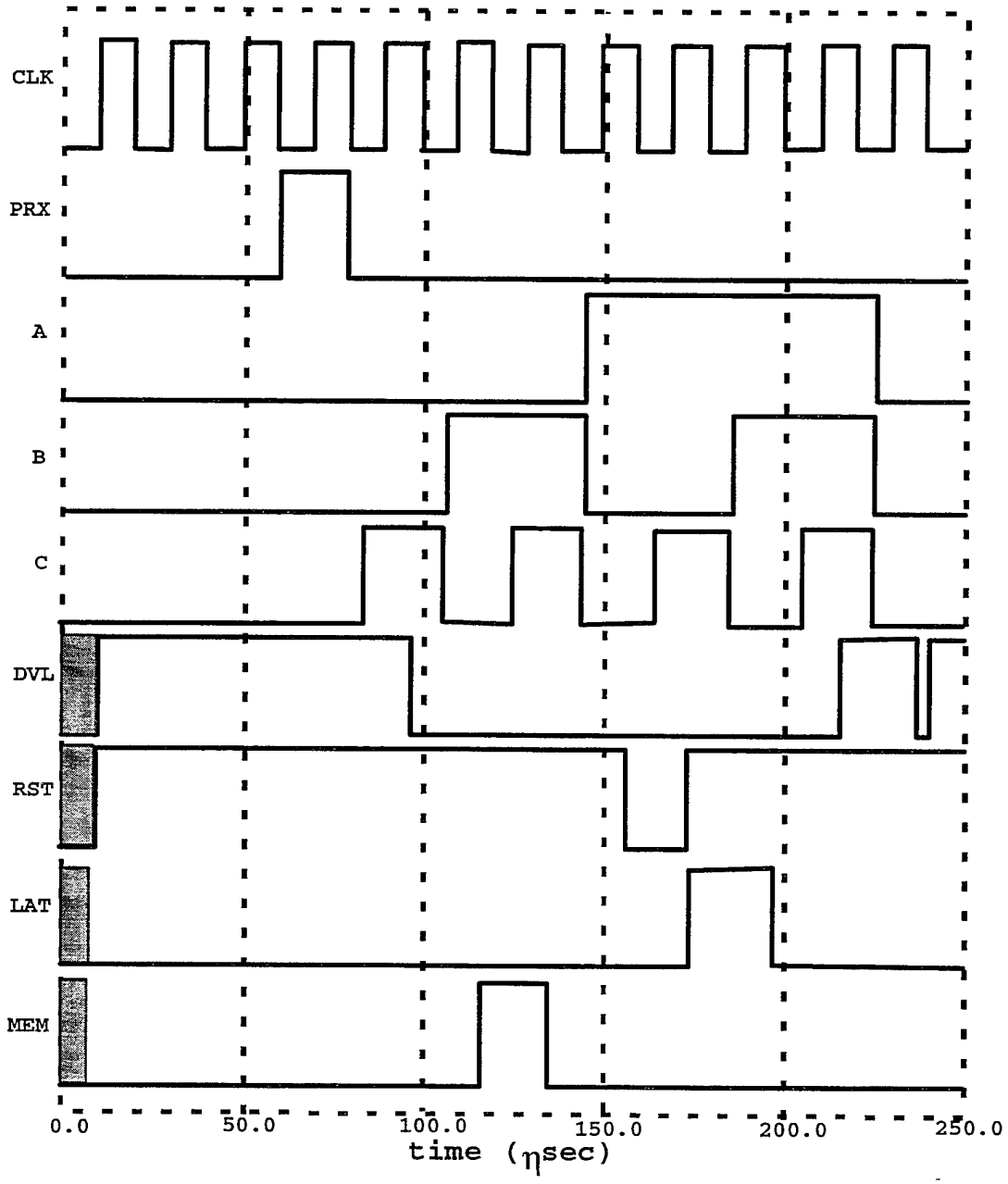

Figure 3.29. Controller Simulation Output

cause the chip output to be three clock pulses low at all times. These three lost counts will cause a negligible change in the output for CRF application purposes and can be adjusted for by adding them back in at the control computer software.

Outputs from the controller for the memory enable and latch enable were buffered by an inverter and NAND gates. The counter reset was also buffered. These buffers were required because the gates making up the PLA were minimum size and had a very limited drive capability. The large fan outs of the three previously mentioned parts of the circuits exceeded the PLA's ability during IRSIM simulations without the buffers in place. The memory enable and selection logic output are NAND together to choose the appropriate memory array. The single memory enable line from the controller routes to all four NAND gates. The output of the NAND gate runs to its respective memory row clock input to enable the row to read and store data on its input lines.

3.7. CHIP LEVEL DESIGN

The floor plan for the completed speed measurement chip is shown in Figure 3.30. The layout overall dimensions were 1750µm along the top and 1750µm along the right side. The controller is positioned in the upper left corner of the area. The selection logic is directly below the controller. The 14 bit counter runs along the top of the layout, bends all the way down the right side, and bends again along the bottom of the layout. This was done primarily to make the 14 outputs from the counter more accessible to the four memory arrays on the right side of the layout and also to save layout space with this large subsystem. The adder is located to the right of the memory arrays followed by the output latch. This formation of the three subsystems the data flows through from the counter to the latch made routing the enormous amount, approximately 102 data lines, of interconnections between these subsystems as simple as possible. Other single cells used in this design are the counter reset buffer immediately to the right of the selection logic and the four NAND gates buffering the memory arrays.

The interconnections between the input and output pads and the different subsystems show up in Figure 3.30 as cross hatched lines due to the limited detail available from this plot. Refer back to Figure 3.1 for a detail of the interconnections represented by the cross hatched lines.

The number of pins required for the speed measurement chip are as follows:

16 Output lines
1 Vdd (+5V)
1 GND
1 Data Valid (DVL)
1 Proximity probe input (PROX)
1 150 kHz clock (CLK)
21 Total pins used

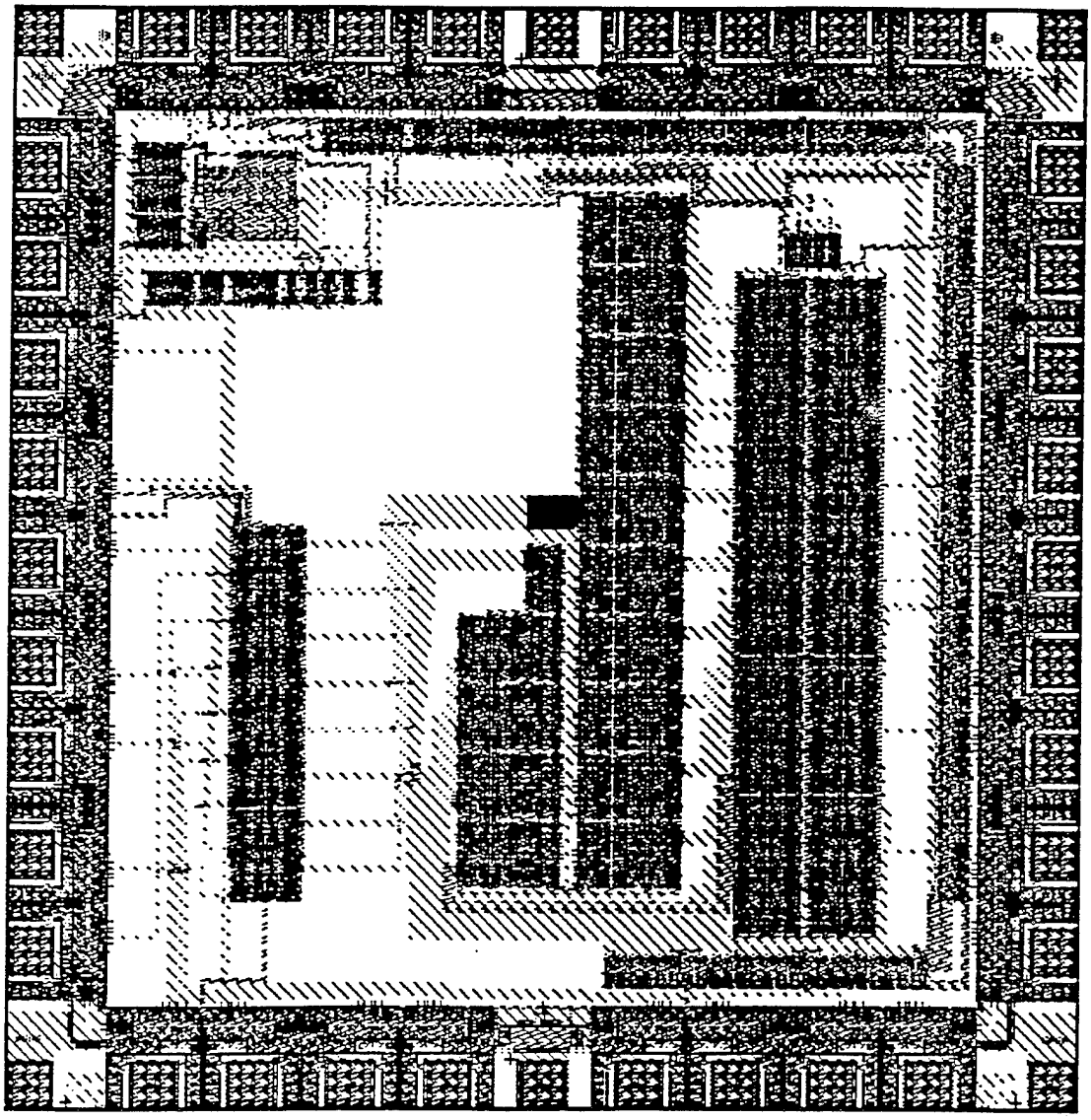

Figure 3.30. Overall Chip Layout Architecture

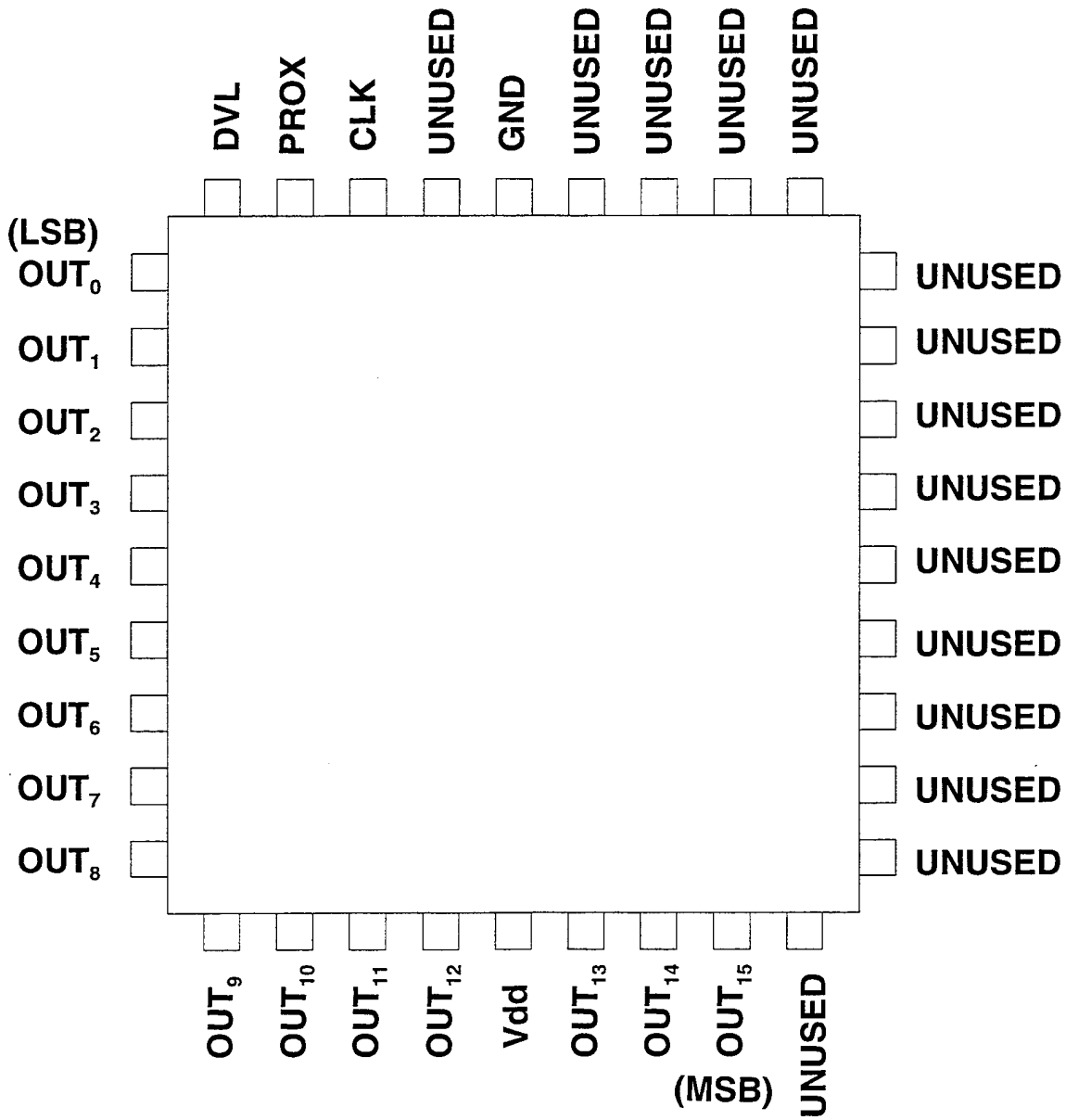

Figure 3.31. Chip Frame Pad Usage

The frame output pad usage diagram for this design is displayed in Figure 3.31. This diagram shows the output buffer pads used for this chip. The frame pictured in this diagram and the previous architecture picture is the standard frame supplied by the company fabricating the design. This part of the integrated circuit does not have to be designed. The design inside the frame does have to be connected to the frame output pads because they provide the buffering for the integrated circuit internal logic to the outside world. These pads give the small geometry internal components the ability to drive circuitry outside of the chip. The connections from the frame pads to the actual integrated circuit package pins is shown in Figure 3.32. The top down view of the IC package is also displayed in this figure. These two diagrams show the pinout of the chip as follows:

PIN NUMBER	FUNCTION
1 through 9	Unused
10	Ground
11	Unused
12	Clock Input
13	Trigger Signal Input
14	Data Valid Output
15	Unused
16	Output 0 (LSB)
17	Output 1
18	Output 2
19	Output 3
20	Output 4
21	Output 5
22	Output 6
23	Output 7
24	Unused
25	Output 8
26	Output 9
27	Output 10
28	Output 11
29	Output 12
30	Power Supply (+5V)
31	Output 13
32	Output 14
33	Output 15 (MSB)
34 through 40	Unused

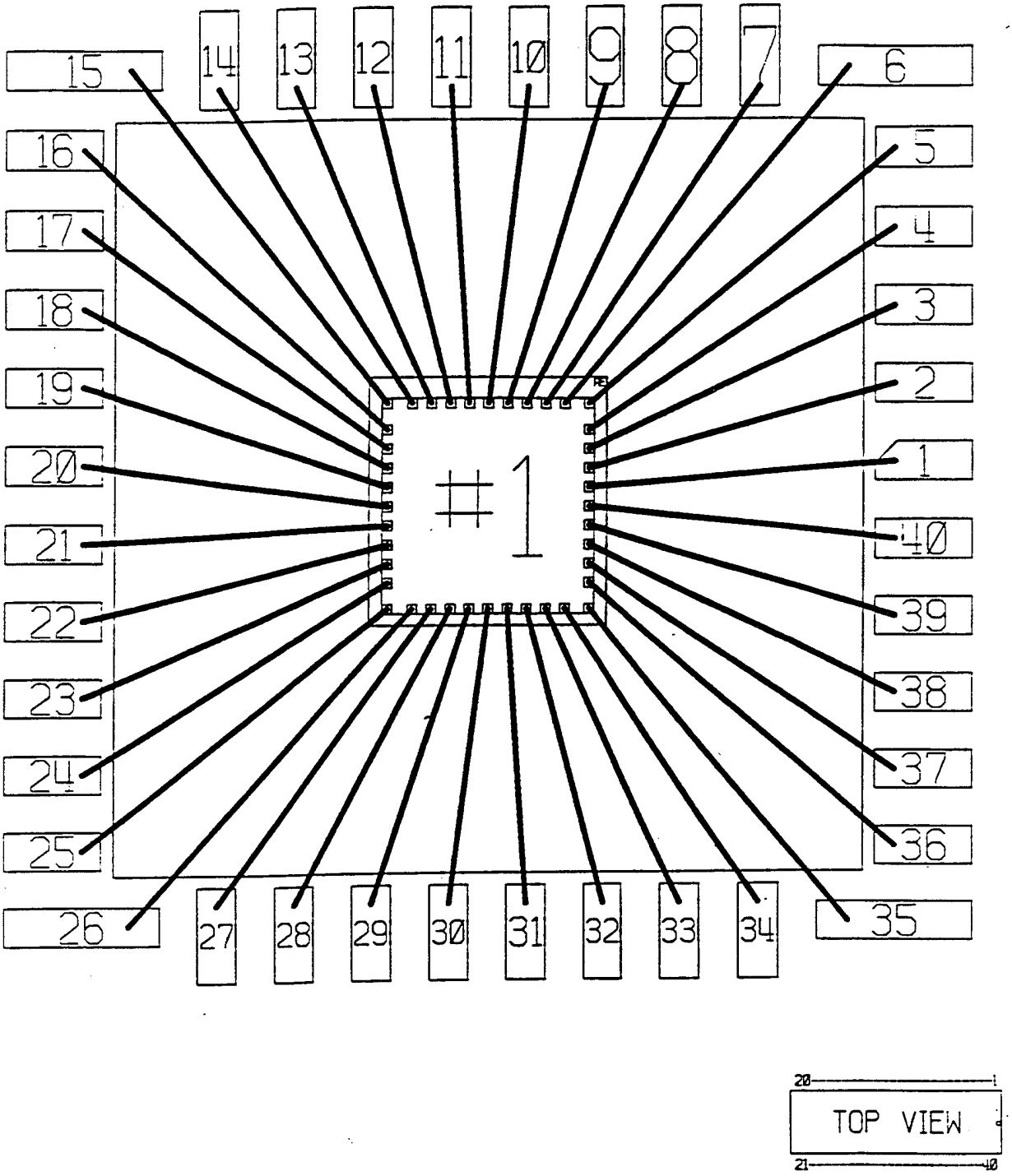

Figure 3.32. Integrated Circuit Pad Connection Diagram

SECTION 4

BOARD LEVEL DESIGN AND SUPPORTING HARDWARE

Two parts of the speed measurement circuit were not incorporated into the Integrated Circuit (IC) design. These two parts were the 150 kHz timing clock and the proximity probe signal detection, conditioning, and digitizing. These parts were intentionally left off the IC design so the chip would be more versatile in different applications other than the CRF speed measurement.

The ability to adjust the timing clock speed gives the IC many potential uses in applications with slower or faster event occurrences than the current application it was designed to meet. This is because the limit of how slow a frequency the chip can measure is based upon when the 14 bit counter overflows. The 14 bit counter gives the ability to count up to 16384 clock pulses between event occurrences. Therefore, if it is necessary to measure the time interval for a lower frequency event, the timing clock can be slowed to insure the counter does not overflow. In the same way the clock may be sped up to provide more accuracy to faster occurring events.

Leaving the signal conditioning off the chip allows for signals of all types to be detected and measured by this system. The proximity probe signal is a -2 to -15 volt analog pulse, but the signal conditioning can be designed to detect a variety of signals, analog or digital, giving the chip adaptability to any application requiring digital time measurement between events.

4.1. TIMING CLOCK

This part of the supporting hardware is used to drive the 14 bit counter of the speed measurement chip. It consists of a 10 MHz crystal with the resistor and capacitor values as given in Figure 4.1 and a 74HC4060 divider/oscillator CMOS integrated circuit.

The resistor and capacitors were chosen to give the 10 MHz crystal a stable and consistent oscillation. These values were determined on a trial and error basis until a stable clock oscillation was obtained. This circuit was then applied to the inputs of the divider/oscillator IC as shown in Figure 4.1.

The 74HC4060 divider/oscillator was chosen for its versatility in applications. Since it was desired to have a clock speed of approximately 150 kHz the 10 MHz crystal speed needed to be reduced. This is accomplished by choosing the output pin of the 74HC4060 corresponding to the sixth bit of its output word. This is equivalent to dividing 10 MHz by two to the sixth power or 64. This division results in a pulse with a frequency of 156,250 Hz or approximately the 150 kHz required by this circuit for input to the speed measurement chip. The versatility of this design using a divider/oscillator such as the 74HC4060 comes from the ability to choose any of the other output pins to obtain different division factors and thus different clock speeds from one 10 MHz crystal.

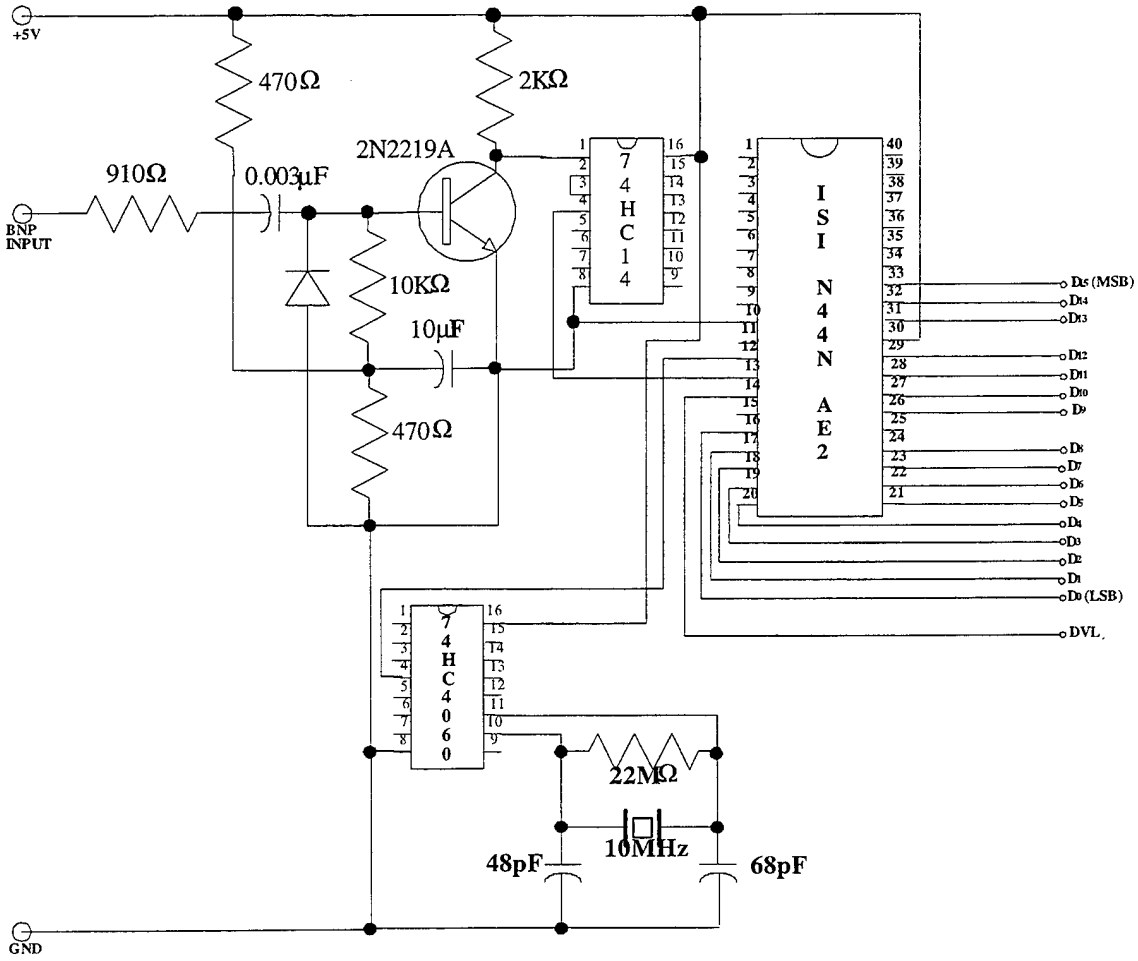

Figure 4.1. Speed Measurement Board Layout

4.2. SIGNAL DETECTION AND CONDITIONING

Signal conditioning is required because of the nature of the Bently Nevada Proximity (BNP) probe. The negative two to -15 volt pulse cannot be directly applied to the speed measurement chip. As stated earlier, CMOS requires a zero to 7.5 volt digitized pulse. The probe signal must therefore be converted from its original state into a CMOS compatible signal. This is the design goal of this part of the system.

Figure 4.1 shows the circuit used for signal detection and conditioning. It is made up of two 470 Ω, one 910 Ω, one 10 kΩ, and one 2 kΩ, resistors as well as a 0.003 μF and a 10 μF capacitor. Also, part of this circuit is the diode and bipolar junction (BJT) transistor. The 470 Ω resistors are used to set the input signal detection level. The 10 kΩ resistor is used to forward bias the BJT. The 910 Ω resistor and 0.003 μF capacitor work in conjunction to limit the time the input signal is applied to the BJT. This sets the width of the on/off signal used to drive the Schmitt trigger, IC 74HC14. The 2 kΩ resistor at the BJT output is used as a pull up resistor to set the input signal to the Schmitt trigger at 5 volts maximum.

The circuit works by forward biasing the BJT when no input signal is received. When the BJT is forward biased, current is conducted from the collector to the emitter causing a 5 volt drop across the pull up resistor. This sends a zero volt signal to the Schmitt trigger. When a input signal is received the transistor is reverse biased and current flow through it is cutoff. This causes the input to the Schmitt trigger to be pulled up to 5 volts until the 0.003 μF capacitor cuts off the BNP signal from the transistors base input. The Schmitt trigger digitizes this analog signal to a zero to 5 volt pulse. The final result of this part of the circuit is a digitized CMOS compatible signal representing the detection of one revolution of the compressor drive shaft.

SECTION 5

TEST RESULTS

The testing of the new system was accomplished in two parts. The first part of the testing involved only the chip. The second part of the testing involved the entire circuit including the chip, detection and signal conditioning circuits, and the 150 kHz clock.

5.1. INTEGRATED CIRCUIT VERIFICATION

This phase of the testing was accomplished in order to verify the design and fabrication of the CMOS integrated circuit. Because this was a chip only test, the two required input signals generated by the other parts of the complete system were simulated with various pieces of lab equipment. The list of lab equipment used is as follows:

Logic Analyzer
Pulse Generator
Signal Generator
Frequency Counter
Oscilloscope
Five Volt Power Supply

The actual setup and connections of this equipment for the test are shown in Figure 5.1.

Since the signal detection and conditioning portion of the system were not part of this test, the proximity signal was simulated with the designed output, or 0 to 5 volt signal, of this circuitry. This simulation was accomplished using a pulse generator with the high and low offsets set to obtain the 0 to 5 volt pulse. The rpm signal frequency being applied was then measured using a frequency counter. The pulse generator was selected to generate the signal for this simulation because it allowed for adjusting the input pulse shape. This allowed for verifying the chip's response to various pulse widths or duty cycles at different frequencies throughout the expected operating range of the CRF. Data observed through these adjustments served to help set up the final component values for the signal conditioning circuitry.

The clock signal was simulated using the signal generator in the square wave mode. Signal amplitude of the square wave was set to 5 volts producing a -2.5 to 2.5 volt pulse. To obtain the 0 to 5 volt pulse train desired, the signal was then offset by a positive 2.5 volts. The frequency of this signal was then adjusted at the signal generator and verified at the oscilloscope to obtain the different clock frequencies the chip was driven with during this initial testing phase.

The last two pieces of equipment used were the 5 volt power supply and the logic analyzer. The power supply was used to energize the chip. The logic analyzer was used to view the 16 output bits of the chip as well as the data valid bit. The logic analyzer

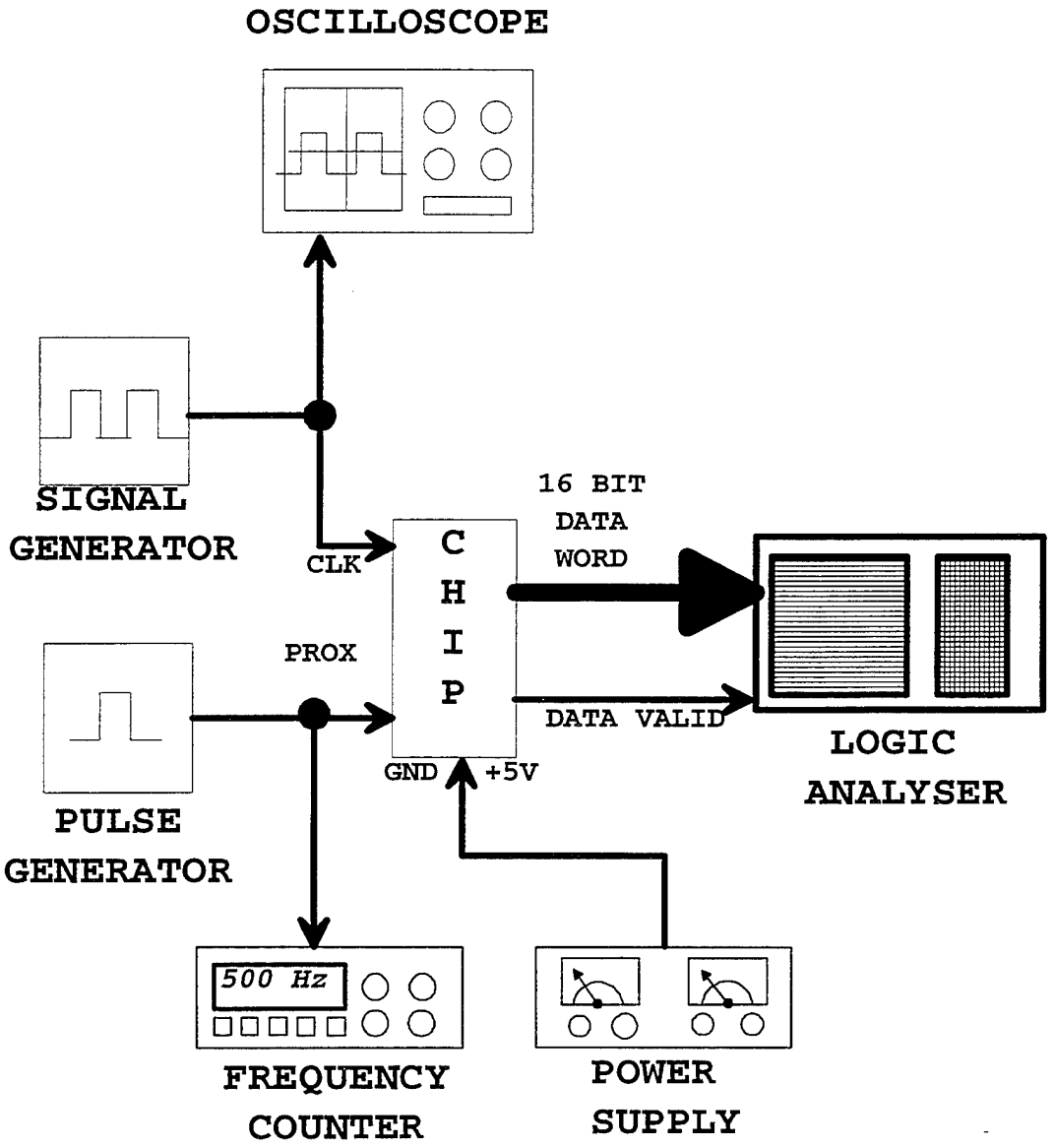

Figure 5.1. Chip Verification Test Setup

used allowed for binary to decimal conversion making the output data more readable during frequency adjustments.

The results of this testing verified the chip to be functioning as designed. Timing clock speeds were varied between 10 kHz and 150 kHz as well as varying the proximity input through the desired range of operation, 3600 to 30,000 rpm. This proximity probe range is equivalent to a frequency range of 60 to 500 Hz. All results from this testing were correct as determined by dividing the timing clock frequency by the proximity probe frequency. The main result derived from this testing was the required shape of the proximity pulse for accurate results from the IC. It was noted the input pulse simulated by the pulse generator had to be between 0.01 msec and 0.1 msec for the chip output to be accurate. This was an important result due to the fact it imposes design specifications upon the signal detection circuitry design.

5.2. BOARD LEVEL TESTING

This part of the design and testing involved three separate parts. The clocking circuit was fabricated on the proto board. The capacitance shown in Figure 4.1 was adjusted until a stable pulse stream was obtained and the frequency was verified using the frequency counter. The signal conditioning was set up as displayed in Figure 4.1. The input signal detection limiting was determined by adjusting the capacitor value at the proximity probe input until the desired signal duration length determined in the chip verification testing was obtained on the oscilloscope. With these two parts of the circuit completed and functional on the proto board, the IC was then added and the full system tested. All results showed the board to function correctly. Finally, the complete system was allowed to run for several days to check for consistent and reliable operation.

SECTION 6

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