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13. ABSTRACT

The Phase I program was primarily an experimental study to assess the feasibility of producing high-quality silicon carbide (SiC) heteroepitaxial films on silicon substrates using a sequential combination of chemical vapor deposition and metallic solution growth. These SiC-on-silicon structures are being developed for low-cost, large-area surrogate substrates to replace SiC wafers presently used in semiconductor device applications. An epitaxial lateral overgrowth process is designed to eliminate micropipe defects and stacking faults, and substantially reduce dislocations due to thermal stress and lattice mismatch. Selective heteroepitaxy of SiC on (111)Si was demonstrated using hexamethyldisilane (HMDS) as a precursor for Si and C. Metallic solution growth of SiC in the temperature range of 950 to 1270 °C from copper-silicon-carbon; zinc-aluminum-silicon-carbon; and nickel-silicon-carbon melts are described. Experiments showing extensive liquid-phase epitaxial lateral overgrowth of silicon on patterned, masked silicon substrates, and partial epitaxial lateral overgrowth of SiC on patterned, masked SiC are reported. These experiments indicate the feasibility of the proposed approach. In addition, an extensive literature survey and phase-equilibria modeling for solution growth of SiC was included in the Phase I work.

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Low-Defect SiC Material
by
Liquid-Phase Epitaxial Lateral Overgrowth

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1. INTRODUCTION AND OVERVIEW

The broad objective of the Phase I program is demonstrate the feasibility of new epitaxial growth technologies for the production of low-cost, high-quality silicon carbide (SiC) material for semiconductor device applications. Single-crystal layers of SiC are grown on silicon or SiC substrates by a sequential combination of two crystallization processes: selective vapor-phase epitaxy followed by metallic solution growth. The SiC-on-silicon heteroepitaxial structures serve as surrogate substrates for use in place of SiC wafers cut from SiC ingots. Our ultimate goal is to produce large-area SiC-on-silicon substrates which are superior in quality to that which is presently available in the form of bulk SiC, and at dramatically lower costs. This material is intended for SiC semiconductor device applications, such as bipolar and field-effect transistors in electronic circuits operating at high temperatures, radiation-hard devices, photodetectors, and light-emitting diodes. The approach is based on a unique near-equilibrium *epitaxial lateral overgrowth* process which is designed to reduce defect levels associated with thermal stress and lattice mismatch, and to prevent the formation and/or propagation of so-called "micropipe" defects. Presently, "micropipe" defects, stacking faults, and high dislocation densities plague SiC substrates and critically limit many applications and commercialization of SiC-based devices.

The technology developed here employs simple and inexpensive crystallization processes. We believe very significant cost reductions can be achieved due to the low cost epitaxy and the potential use of silicon substrates which obviates the need for any bulk SiC material. For SiC-on-silicon heteroepitaxy at relatively low (1000 to 1200 °C) temperatures, the cubic β-SiC polytype is thermodynamically favored. It may be possible for certain substrate crystallographic orientations and for growth conditions with larger deviations from thermodynamic equilibrium to achieve other SiC polytypes on silicon substrates. Otherwise, to produce hexagonal or rhombohedral polytypes of SiC that are free of micropipes, stacking faults, and dislocations, an α-SiC substrate can be used instead of a silicon substrate. In this case, the purpose of the epitaxial lateral overgrowth is to eliminate defects rather than to replace the bulk SiC substrate. Another important advantage of our approach is that the SiC-on-silicon heteroepitaxy should be scaleable for large-area (at least 100 mm in diameter) wafers.

An obvious constraint on the epitaxy process for SiC-on-silicon is that the highest growth temperature must be below the melting point of silicon (1420 °C). There are at least several chemical vapor deposition for SiC with growth temperatures sufficiently lower than the melting point of silicon processes (see sections 2.1 and 3.1). Most prior liquid-phase growth of SiC has employed either silicon-rich melts or transition metal solvents such as chromium, both at temperatures well above the melting point of silicon. The selection of a solvent suitable for solution growth of SiC is not trivial since SiC (or carbon) is only sparing soluble in most melts at temperatures in the range of 1000 to 1400 °C. A large part of the Phase I effort explored alternative solution compositions for low-temperature liquid-phase epitaxy of SiC.

FIGURE 1 shows epitaxial lateral overgrowth as applied to production of thin (< 5 microns) SiC films or thick (> 5 microns) SiC epitaxial layers. In various stages of development, and depending on the application, this process can be modified to utilize either silicon or SiC substrates. Also, the epitaxial lateral overgrowth can be effected using either vapor-phase epitaxy (VPE) or liquid-phase epitaxy (LPE), or, the epitaxial lateral overgrowth can be performed using a two- or multi-step combined process comprised of sequential VPE and LPE steps. In still another variation, the silicon or SiC substrate could be removed by selective etching to yield a free-standing SiC film, or a SiC film bonded to a foreign substrate such as quartz, graphite, or a ceramic.

In epitaxial lateral overgrowth, the substrate is prepared prior to epitaxy by first masking it with a thin film of dielectric material (e.g., silicon dioxide, silicon nitride, aluminum oxide) or with a refractory metal (e.g., tungsten, molybdenum) film. The mask is patterned with stripe openings, called *vias*, using photolithography and selective etching or by an epitaxial lift-off technique (FIGURE **1a**). The stripe openings are typically 5 to 10 microns wide and spaced 100 to 1000 microns apart, depending on the intended device application of the SiC structure. The alignment of the vias with respect to the crystallographic orientation of the substrate is often critical.

The openings in the mask at the stripe vias expose the underlying substrate through the mask. The exposed substrate areas selectively seed the crystallization of SiC. During the subsequent epitaxy step, oriented SiC crystals are preferentially nucleated at the vias (**1b**). The growth is selective in that there is virtually no nucleation or deposition of SiC on the mask. As the crystallization process proceeds, however, the SiC crystals laterally overgrowth the mask layer (**1c**). The growth can be terminated before SiC crystals nucleated at adjacent vias impinge (**1d**), or after a sufficiently long growth time so that the SiC crystals coalesce to form a continuous film (**1e**). A figure of merit of for epitaxial lateral overgrowth is the *aspect ratio*, defined as the ratio of lateral width over the mask to epitaxial layer thickness. It is normally an objective to maximize the aspect ratio. The aspect ratio depends on the orientation of the substrate, the alignment of the vias, the mask material and mask thickness, the melt composition (in solution growth), the growth temperature, the growth rate, and the deviation of the growth from thermodynamic equilibrium, i.e., the degree of supersaturation during various stages of the overgrowth process. These experimental parameters are generally controllable over a wide range, and the growth process can be systematically optimized to achieve consistent lateral overgrowth with reproducible aspect ratios.

The epitaxial lateral overgrowth process also permits new device structures. For instance, an insulating mask; such as a film of silicon nitride, alumina, or silicon dioxide; between the epitaxial SiC and the silicon substrate can be used to dielectrically isolate devices fabricated in the heteroepitaxial SiC layer. As another example, a reflective mask, such as a refractory metal or a composite multilayer structure of dielectric and semiconductor films, between the epitaxial SiC and the silicon substrate can be utilized as a "buried mirror" to improve the quantum efficiency of SiC LEDs and photodiodes.

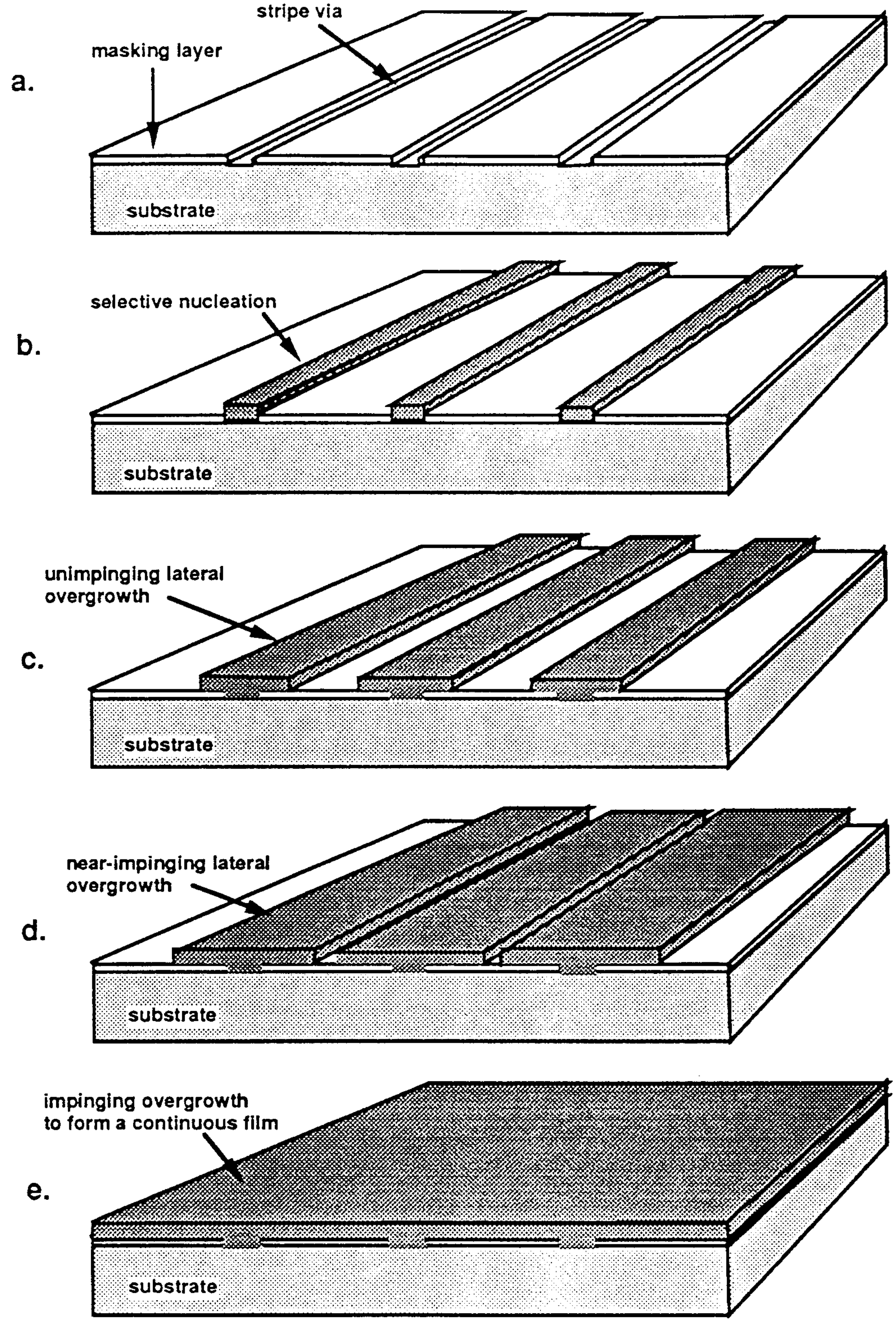

FIGURE 1: Epitaxial lateral overgrowth process for SiC on silicon or SiC substrates: **1a.** masked, stripe patterned substrate; **1b.** oriented SiC crystals preferentially nucleated at the vias. SiC crystals laterally overgrowth the mask layer (**1c**). The growth can be terminated before SiC crystals nucleated at adjacent vias impinge (**1d**), SiC crystals coalesce to form a continuous film (**1e**).

The "defect filtering" phenomena associated with epitaxial lateral overgrowth is indicated in FIGURE 2. Defects such as dislocations, stacking faults, and micropipes tend to propagate vertically from the growth interface. While areas of the epitaxial film directly over the seeding regions of the vias may exhibit such defects, areas of the epitaxial film over the mask will be free of defects. Thus, the epitaxial lateral overgrowth process produces large areas of material without defects and confines any defects to well-defined areas which are a small portion of the total substrate area. These defective areas, which correspond to the vias of the growth mask, can be avoided in the siting of monolithic devices fabricated in the epitaxial SiC film.

Stacking faults in heteroepitaxial films are often due to stress-induced glide of misfit dislocations away from the substrate-film interface [MAHAJAN, 1989]. They are also attributed to the discrete, *island* or *three-dimensional* type nucleation where the coalescence of discrete nuclei leads to stacking faults [POWELL and MATUS, 1987; YANG *et al.*, 1989]. In either case, we expect that laterally-overgrown films will have fewer stacking faults since growth must occur by a two-dimensional or step flow mechanism which will prevent the propagation of defects in epitaxial lateral overgrowth. UEDA *et al.* [1990] and NISHINO *et al.* [1995] have observed the step-flow mode of growth in SiC epitaxy. Finally, we note that previous work with silicon-on-silicon and GaAs-on-silicon liquid-phase epitaxial lateral overgrowth produced structurally perfect films with mirror like surfaces; areas of the epitaxial film grown over the mask were virtually free of dislocations and other defects [BAUSER, 1986; UIIJE and NISHINAGA, 1989; SUZUKI, 1989].

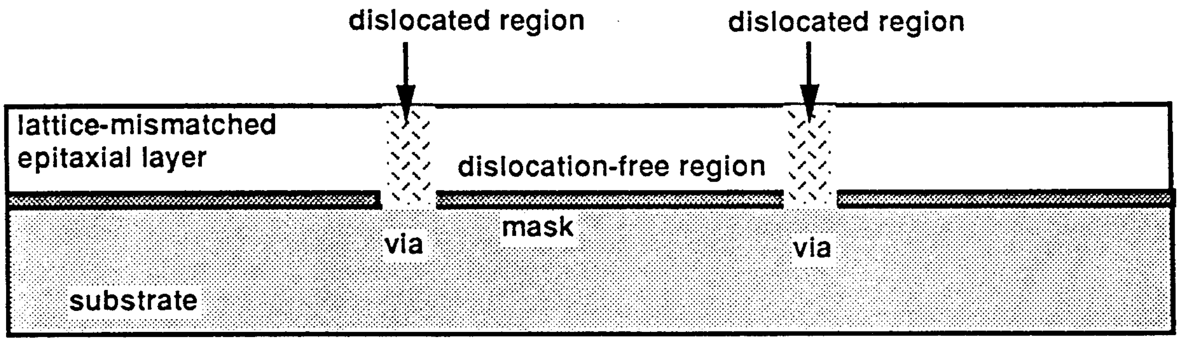

FIGURE 2: Defect Filtering in Epitaxial Lateral Overgrowth.

We believe that epitaxial lateral overgrowth can be effected with either vapor-phase epitaxy or liquid-phase epitaxy. Our experience, and the consensus of the literature, is that higher aspect ratios can be achieved with liquid-phase epitaxy since in LPE growth occurs very close to thermodynamic equilibrium. This results in a higher degree of growth rate anisotropy upon which significant lateral overgrowth is contingent. However, liquid-phase solution growth of SiC on silicon is problematic since: 1. Unlike vapor-phase epitaxy, the high lattice mismatch (20 %) between silicon and SiC impedes nucleation of the SiC epitaxial layer on the silicon substrate, and 2. Silicon is soluble in most, if not all, melts which dissolve appreciable SiC. Hence, there would unavoidably be some dissolution of a silicon substrate upon contact with growth solution. This is not necessarily an insurmountable problem—but does complicate the epitaxy process. We therefore propose a combined process wherein a heteroepitaxial film of SiC is first grown on silicon by a vapor-phase technique. This initial SiC-on-silicon film functions as a “buffer” layer to bridge the lattice mismatch between silicon and SiC. In a subsequent and separate step, a SiC layer is grown on the buffer layer by solution growth. The buffer layer can be grown selectively on a patterned, masked silicon wafer which is then used as the substrate for liquid-phase epitaxial lateral overgrowth. Alternatively, a film of SiC can be grown on an unmasked silicon wafer by VPE epitaxy. The SiC-on-silicon heteroepitaxial layer is then masked and patterned for use as a substrate in liquid-phase epitaxial lateral overgrowth.

The specific aim of the Phase I work is to demonstrate the feasibility of the several steps critical to the success of the proposed approach. Consequently, the experimental work of the Phase I program was focused on the following three tasks:

1. SiC epitaxial films are grown on SiC substrates using a relatively low-temperature liquid-phase epitaxy process. Liquid-metals (e.g., lead, tin, germanium, or other metals, or mixtures of these metals) are used as solvents for solution growth of SiC. The targeted growth temperatures are 1000 to 1400 °C. These growth temperatures will permit the use of silicon substrates. The SiC solution growth process is similar to conventional liquid-phase epitaxy as commonly applied in the production of III-V heterostucture optoelectronic devices such as LEDs and lasers.

2. Next, having established a reproducible, low-temperature solution-growth technique for SiC, a process is developed whereby the SiC substrate is first masked prior to growth with a dielectric or refractory metal coating. The masking layer is patterned with stripe openings. The exposed SiC surfaces at the stripe openings serve as sites for preferential nucleation of SiC during a subsequent LPE step.

3. An epitaxial film of cubic silicon carbide is grown on a silicon substrate using a simple vapor-phase epitaxy process. The SiC-on-Si heteroepitaxial layer can be used to seed the subsequent growth of a cubic SiC layer by liquid-phase epitaxy as described above.

In the interest of minimizing consumption of expensive SiC material, we also studied liquid-phase epitaxial lateral overgrowth of silicon on patterned, masked silicon substrates. These experiments were used to evaluate mask materials and to determine optimum alignments and geometries of the stripe vias with silicon substrates.

In addition to the experimental work, an extensive literature search was undertaken using Chemical Abstracts®, Current Contents®, Compendex®, various archival data bases of the University of Delaware Morris Library, and the InterLibrary Loan (ILL) service. The relevant work on solution growth of SiC is widely dispersed; much of the previous work on SiC LPE and metallic solution growth of SiC is from the Former Soviet Union and in Russian. Translations were made where necessary. Much of the relevant literature is given in the Phase I Report citations.

The main objective of a Phase II program will be to develop the approaches studied in the Phase I program for the production of high-quality SiC material. expand This entails continued optimization of vapor-phase SiC-on-silicon process. Further identification and evaluation of solvents for solution growth of SiC. Optimization of epitaxial lateral overgrowth for high aspect ratios. these steps and combine them in a process to produce high-quality SiC-on-silicon surrogate substrates.

2. BACKGROUND

The advantages and applications of SiC semiconductor devices are well known, see for example HARRIS and WANG [1987], RAHMAN *et al.* [1988], and HARRIS *et al.* [1990]. We will instead review the important materials issues and prior work relevant to the Phase I program including chemical vapor deposition of SiC on silicon (section 2.1), liquid-phase epitaxy of SiC (section 2.2), and epitaxial lateral overgrowth (section 2.3). Section 2.4 provides a discussion of some of potential advantages of SiC solution growth.

NEUDECK [1995] has provided a recent review of the status of SiC material for semiconductor device applications. The most critical issue in SiC wafer technology is related to so-called "mircopipe" defects. The micropipe defects are present typically in densities of several hundred per square centimeter with a minimum measured density of 55 per square centimeter [PALMOUR *et al.*, 1995]. Of next importance is the high dislocation density in SiC substrates and epitaxial layers, which may have effects on leakage currents, breakdown voltages, and minority carrier lifetimes. Dislocation densities in SiC substrates and epitaxial layers are on the order of 10,000 per square centimeter [WANG *et al.*, 1993; FAZI *et al.*, 1994].

2.1 Prior Work on CVD of SiC

Silicon carbide films can be formed on silicon substrates by chemical conversion processes, and by various chemical vapor or physical vapor deposition (sublimation) techniques. Thin-film SiC deposition processes include chemical vapor deposition by pyrolysis of volatile silicon and carbon precursors, molecular- and ion-beam epitaxy, reactive ion beam deposition, and electron-assisted chemical vapor deposition [HIRABAYASHI *et al.*, 1990], as well as sputtering and plasma-enhanced chemical vapor deposition. In this section, we review previous investigations and techniques which we deem potentially useful for forming a SiC buffer layer on silicon as would be required to as a seeding layer for SiC LPE.

Silicon carbide films can be grown on silicon substrates by so-called chemical conversion or *carbonization* processes is several ways. Heating a silicon wafer in high vacuum can result in the formation of a silicon carbide surface layer due to out-diffusion of carbon impurity in the bulk of the silicon [POSER, 1965; BIEDERMAN and BRACK, 1966]. Heating silicon in the presence of graphite and argon has also been reported to form a SiC surface layer [TOMBS *et al.*, 1965]. The most common method of chemical conversion, however, involves heating a silicon wafer in the presence of hydrocarbons. Silicon surfaces have been carbonized with methane [SPITZER *et al.*, 1959; NAKASHIMA *et al.*, 1966], and by reaction with unsaturated hydrocarbons (C_2H_4 and C_2H_2) in high and ultrahigh vacuum in the temperature range of 800 to 1000 °C [KHAN and SUMMERGRAD, 1967].

Chemical conversion steps are being incorporated in CVD growth techniques for β-SiC-on-silicon heteroepitaxy. One of the most successful approaches for the growth of -β-SiC films on silicon substrates uses a two-step process first developed by MATSUNAMI *et al.* [1981] and NISHINO *et al.* [1983a, 1983b], and later by ADDAMIANO and SPRAGUE [1984]. Many groups are now using this approach [POWELL and MATUS, 1987; DAVIS *et al.*, 1988]. In the first step, a thin buffer layer of β-SiC is formed on the surface of a silicon wafer by a chemical conversion process in which the silicon substrate is subjected at high temperatures to an ambient containing hydrocarbons. In the second step, a thicker layer of β-SiC is grown on the SiC buffer layer by a pyrolysis CVD reaction using gaseous silicon and carbon precursors. Much of the recent work on chemical conversion processes has been directed toward optimizing its utility in this two-step process.

RAI-CHOUDHURY and FORMIGONI [1969] formed β-SiC layers by reaction of silicon substrates of (100), (110), and (111) orientation with methane or acetylene at temperatures of 1100 to 1200 °C. Both hydrogen and argon ambients were used. The SiC films ranged from oriented single-crystalline to near-amorphous depending on the experimental conditions. KUROIWA and SUGANO [1973] used gas mixtures of CH_4 or Cl^4 in Ar or H_2 to grow β-SiC films on (111) silicon at temperatures of 1300 °C. SiC films up to 100 nm in thickness were grown. Near the surface, the SiC films were observed to have a single-crystal structure but were polycrystalline near the silicon-SiC interface. NISHINO *et al.* [1983a] developed a β-SiC-on-silicon buffer layer growth technique where the silicon substrate was first etched at 1200 °C in a gas mixture of 4% HCl in H_2 for ten minutes and cooled to room temperature. The buffer layer was grown by establishing a flow of 0.03 mole% C_3H_8 in H_2, heating the substrate to 1400 °C for one minute, terminating the flow of C_3H_8, and finally cooling to room temperature. The SiC buffer layer was 20 nm thick and mostly polycrystalline. ADDAMIANO and SPRAGUE [1984] reacted 1 mole% C_3H_8 in H_2 with (100) silicon by rapidly heating the silicon substrate to 1400 °C in 3 to 8 milliseconds. Reflection High Energy Electron Diffraction analyses showed these films to be monocrystalline. KIM *et al.* [1987] described β-SiC films formed on (100) silicon subjected to C_2H_4 at 1280 to 1330 °C. In the conversion step, the silicon substrate was heated at a rate of 500 °C/min. An optimum conversion time of 150 seconds was determined. The β-SiC films were about 10 nm in thickness and generally monocrystalline, but contained regions of disorder, pitting, stacking faults, and residual strain. LIAW and DAVIS [1985] found that under similar experimental conditions, longer conversion times resulted in SiC buffer layers with rougher surface morphology that were not conducive to SiC CVD. NISHINO and SARAIE [1989] reported a chemical conversion process using acetylene (C_2H_2, 1 cc/min) at 1360 °C for three minutes, resulting in monocrystalline SiC buffer layers. An HCl etch at 1240 °C was used prior to the chemical conversion. IWAMI *et al.* [1989] used medium energy ion scattering, soft X-ray spectroscopy, and transmission electron microscopy to study the SiC/silicon interface on (100) silicon substrates. They confirmed the monocrystallinity of the SiC buffer and a definite, strained epitaxial relation with the silicon substrate. HIRAI *et al.* [1992] lowered the chemical conversion temperature to 1230 °C by diluting the C_2H_4

with hydrogen. They found that the hydrogen flow rate plays an important role in the chemical conversion process.

SIRTL [1963] briefly reported the deposition of polycrystalline SiC using a close-spaced vapor transport technique with water vapor as a transport agent.
The growth of SiC is based on the reversible transport reaction

$$SiC(s) + 2\ H_2O(g) \rightleftarrows SiO(g) + 2\ H_2(g)$$

Few details were given.

GOLECKI *et al.* [1993, 1994] developed a low-pressure chemical vapor deposition process for the growth of monocrystalline epitaxial cubic SiC films on (100) silicon at 750 °C using methylsilane $SiCH_3H_3$ as a precursor for both Si and C. This is the lowest growth temperature for SiC-on-silicon heteroepitaxy ever reported. Hexagonal SiC-on-silicon films could also be achieved with the aid of a remote H_2 plasma.

TAKAHASHI *et al.* [1992] described the low-temperature growth of 3C-SiC on (100) and (111) silicon substrates by atmospheric-pressure chemical vapor deposition using hexamethyldisilane $Si_2(CH_3)_6$ (HMDS) and hydrogen. Epitaxy was achieved at substrate temperatures as low as 1100 °C. Single crystal layers of epitaxial cubic silicon carbide were grown on (111) Si with and without carbonized buffer layers at growth rates as high as 70 nm/min. With (100)Si substrates, a carbonized buffer layer was required for epitaxial growth of SiC on Si. NORDELL *et al.* [1994, 1995] reported a very similar technique for the growth of cubic SiC on (100) and (111) Si substrates and (0001) SiC substrates, with the main difference that the growth ambient was a mixture of argon and hydrogen. Polycrystalline layers were observed at low temperatures and with pure Ar as the carrier gas, with increased crystallinity and orientation at higher temperatures above 1300 °C and when H_2 was added to the ambient. Monocrystalline epitaxial SiC films on silicon substrates could be obtained under optimum conditions.

2.2 Prior Work on SiC LPE

Silicon carbide can be grown from silicon-carbon melts and from molten silicon-carbon-metal solutions. Liquid-phase crystallization has been used for the growth of both bulk SiC crystals and epitaxial growth of SiC layers. The phase diagram of the silicon-carbon binary system and the solubility of carbon in silicon-rich liquid solutions are shown in FIGURES 3 and 4. As an aside, O'CONNOR [1963] noted that the solubility of carbon in liquid silicon appears to be significantly increased by the presence of oxygen and that some precautions must be exercised in evaluating solubility data depending on experimental conditions. (This apparent increased carbon solubility is in actuality probably due to the loss of carbon from the melt through formation of carbon monoxide or carbon dioxide.) The data of FIGURES 3 and 4 underscore the chief problem of melt growth techniques in that the solubility of carbon is silicon is very low—less than 0.01 atomic percent near the melting point of silicon and increasing to only one atomic percent at 2150 °C [HALL, 1958; SCACE and SLACK, 1959].

SiC crystallization from molten silicon is hindered by several other problems. Growth from pure silicon requires a temperature of at least 1700 °C to achieve sufficient carbon solubility in the liquid phase. There is appreciable evaporation of silicon solvent at these temperatures. Also, molten silicon is very reactive and interaction between the melt and crucible leads to contamination of the solution. Despite these problems, crystallization of SiC from molten silicon-carbon solutions is a well-established technique for forming epitaxial layers and *p-n* junctions [GRIFFITHS and MLAVSKY, 1964; WRIGHT, 1965: KNIPPENBERG and VERSPUI, 1969; BRANDER and SUTTON, 1969; KUMAGAWA *et al.,* 1970; KAMATH, 1971; BRANDER, 1973; RYAN *et al.*, 1973]. Liquid-phase epitaxy of p-n junctions in 6H-SiC on 6-H SiC substrates using carbon-saturated silicon melts has been developed for blue LEDs [SUZUKI *et al.*, 1976; MATSUNAMI *et al.,* 1977; VISHNEVSKAYA *et al.*, 1988; MATSUSHITA *et al.*, 1990]. Violet and ultraviolet light-emitting diodes have been made by LPE of 4H-SiC layers on 4H-SiC substrates [DMITRIEV *et al.*, 1989; 1990]. Other devices made by SiC LPE include JFETs [DMIETRIEV *et al.*, 1991] and dynistors [VAINSHTEIN *et al.*, 1987; DMIETRIEV *et al.*, 1988].

Temperature gradient growth with a SiC source can be used to grow relatively thick SiC layers, even when the solubility of carbon in the melt is low. For instance, BRANDER and SUTTON [1969] described a temperature-gradient SiC growth technique using pure silicon as the solvent. At a substrate temperature of 1650 °C and an estimated temperature gradient in the melt of approximately 10 °C/cm, growth rates of several microns per minute were obtained. The SiC layers were the same polytype as the substrate and layers of thickness up to 100 microns were reproducibly grown. Temperature-gradient growth at temperatures as low as 1500 °C was achieved.

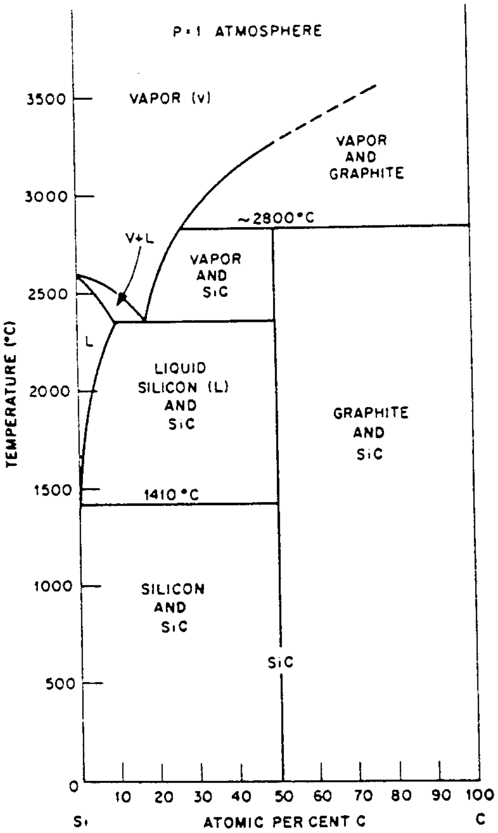

Figure 3: Si-C phase diagram. From Nowotny [1954].

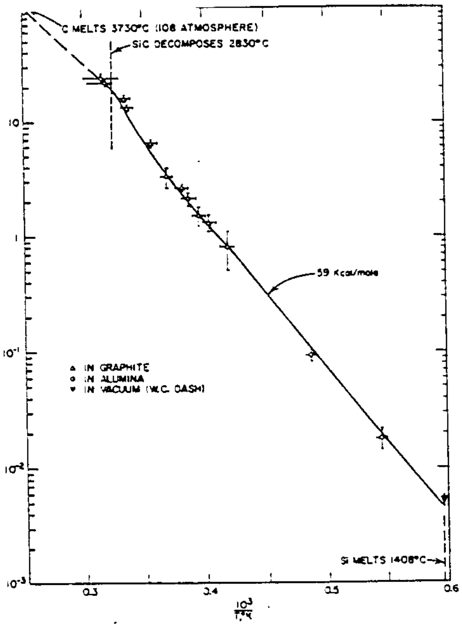

Figure 4: Solubility of carbon in molten silicon. From O'Connor [1963].

By alloying the silicon-carbon solution with certain metals in order to increase the carbon solubility, lower growth temperatures are possible. Ideally, the metal solvent should fully wet the substrate, readily dissolve SiC, and show a significant change in SiC solubility with temperature. The solvent must not attack the crucible material and should have a sufficiently low vapor pressure at the growth temperature. FIGURE 5 shows the solubility of carbon or SiC in several liquid metals and semiconductors: Pb, Sn, Ge, Ga, Al, and Si. Many of these solvents have previously been used successfully for LPE of Si, Ge, and various III-V compounds. Lead, tin, germanium, and gallium look especially promising. The previous work on the growth of SiC from silicon-metal solutions is reviewed below.

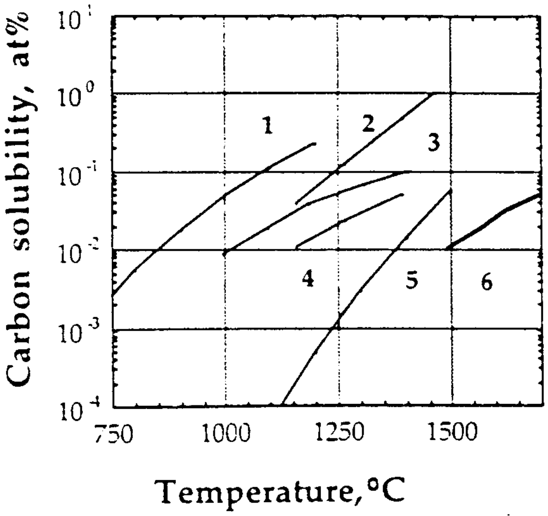

FIGURE 5: Carbon or SiC solubilities. **1**- C in Pb, **2**- SiC in Sn, **3**-SiC in Ge, **4**-SiC in Ga, **5**-C in Al, and **6**- C in Si. From DMITRIEV [1993].

BAUMANN [1952] grew small β-SiC crystals from a silicon-nickel eutectic at 1000 C and from a silicon-aluminum-zinc alloy at 525 °C. CHIPMAN [1954] described the formation of SiC from iron-silicon alloys in the temperature range of 1500 to 1800 °C. GRIFFITHS and MLAVSKY [1964] adapted a traveling solvent method for the growth of α-SiC from chromium-rich melts at 1750 °C. WOLFF *et al.* [1968] described the solution growth and traveling solvent growth with several liquid metal solvents. TAIROV and YAS'KOV [1970] investigated the growth of SiC from Fe-Si-C, Al-Si-C, Cu-Si-C, Ni-Si-C, Co-Si-C, Sn-Si-C, and Bi-Si-C solutions. PELLEGRINI and FELDMAN [1973] used various mixtures of transition metals and silicon as the solvent for SiC solution growth. BERMAN and COMER [1969] reported epitaxy of β-SiC using liquid metal solutions. GRIFFITHS and MLAVSKY [1964], WRIGHT [1965], and KUMAGAWA *et al.* [1970] used chromium as a solvent in a thin (100 to 200 micron) melt zone technique for the growth of SiC. Very fast growth rates, up to 10 microns/min can be achieved with this technique. PAVLICHENKO *et al.* [1969] employed rare earth solvents in a traveling zone technique for SiC.

More recent work on SiC solution growth has investigated new melt compositions with the objective of lower growth temperatures. IVANOV *et al.* [1981] and TAIROV *et al.* [1982] studied the solubility of SiC in Ge-Si, Ge-Sn, and Ge-Ga melts at temperatures between 1000 and 1400 °C. SiC solubilities in the range of 0.02 to 0.2 mole percent were determined. The growth of SiC layers and p-n junctions from, tin, gallium, and aluminum melts has been reported by TAIROV *et al.* [1981], RENDAKOVA [1986], VAINSHTEIN *et al.* [1987], and DMIETRIEV *et al.* [1986, 1992]. VAINSHTEIN *et al.*[1987] showed that the growth temperature of SiC p-n junctions can be reduced considerably by using melt compositions with tin, germanium, aluminum, or gallium. High-quality 6H-SiC *p-n* junctions have been grown by LPE at temperatures as low as 1150 °C. DMIETRIEV *et al.* [1986, 1992] used Sn-Al-Si, Ga-Al-Si, and Ge-Si solvents for temperature-gradient SiC LPE between 1100 to 1200 °C. Based on this analysis, lead and tin appear especially promising for the growth of SiC at temperatures below the melting point of silicon. DMIETRIEV *et al.* [1992] also demonstrated selective SiC LPE in openings patterned in a carbon mask coating a SiC substrate. Current-induced crystallization (electro-epitaxy) of SiC from gallium-ytterbium melts in the temperature range of 1200 to 1400 °C was developed by SAFARALIEV *et al.* [1984]. In work of some related interest, ELWELL [1982] has reported the electro-deposition of SiC from fused salts, however, the purity of this material for semiconductor applications is in doubt.

To assess the potential for solidification of SiC from metal based melts requires a careful phase equilibria analysis. For compositions and temperatures of certain melts, SiC may not be the only precipitate that forms upon cooling. For instance, PELLEGRINI *et al.* [1972] concluded that SiC could not be grown from Cr-rich melts at low temperatures due to the preferential formation of various chromium carbides (e.g., Cr_3C_2) or chromium silicides (e.g., Cr_3Si). They further reasoned that the formation of metal carbides or metal silicides in preference to SiC should be also expected in metal-rich ternaries of silicon, carbon, and the transition metals titanium, vanadium, cobalt, and nickel. RAGHAVAN [1986] determined the Fe-Si-C ternary phase diagram. At 1300 °C, a SiC solid phase with no solid iron, carbon, carbide or silicide, is shown for a silicon concentration in excess of 22 weight% and the liquid-phase carbon concentration in the range of about 0.2 to 0.3 weight%. The compositions for exclusive formation of SiC at this temperature was thus quite a fairly narrow range. AGEYEV *et al.* [1988] indicated that there is a minimum silicon concentration to produce SiC in the Fe-Cr-Mn-Si-C which they quantified as a function of melt composition and temperature. The SiC stability region increased with increasing silicon (5 to 15 weight percent). Similarly, KULINICH *et al.* [1988] showed analogous criteria apply for the formation of SiC in the Fe-Si-Cr-C system. With at least some metal solvents, particularly transition metals, it appears that the solidification of SiC requires that the concentration of Si significantly exceed that of carbon in the melt. For the formation of SiC from tin-rich melts saturated with carbon (graphite), KOZHITOV and BUROV [1988] observed that SiC formation occurs only at temperatures above 1200 °C. It is apparent that for many systems, an accurate knowledge of the phase equilibria will be required to grow SiC without accompanying solidification of other material.

If solvents with metal components are used, the impurity incorporation of metallic impurities in the SiC must be considered. Many metals are electrically active as ionized impurities, or else introduce minority carrier recombination or trapping centers. The extent to which this is a problem depends on: **1.** the nature and electrical activity of the impurity, **2.** its concentration in the SiC, **3.** its mobility and propensity to contaminate adjacent epitaxial SiC layers by solid-state diffusion during post-growth epitaxy and processing, **4.** the feasibility of post-growth impurity gettering as, for example, is increasingly successfully used in silicon technology, and **5.** the intended application of the solution-grown SiC material, i.e., whether majority carrier devices (e.g., FETs) or minority carrier devices (e.g., LEDs, bipolar transistors, photodiodes) will be fabricated in the solution-grown SiC material, or whether the SiC material will be used simply as a substrate for the subsequent epitaxy of higher purity SiC layers at lower growth temperatures.

The impurity concentration in solution-grown semiconductors is a function of melt composition and growth temperature. On the basis of simple chemical bonding considerations, O'CONNOR [1963] predicted that most metals will be strongly rejected from SiC solidifying from the liquid phase. There is not a great deal of data characterizing the distribution of metal impurities between SiC and liquid silicon or silicon-metal melts. However, if results from the solution growth of silicon from liquid metals are any indication, it seems reasonable that solution compositions can be tailored so that SiC of sufficient purity can be grown from metal-based solutions. For instance, high quality silicon epitaxial layers can be grown from tin or lead as these metals are electrically inactive in silicon [D'ASARO *et al.*, 1969; BALIGA, 1985]. Similarly, indium and bismuth, although electrically active in silicon as acceptor and donor impurities, respectively, are incorporated to a sufficiently small degree that low-doped (10^{15} to 10^{16} cm^{-3}) silicon can be solidified from solutions of silicon with these metals [BAUSER and STRUNK, 1985]. Recently, CISZEK *et al.* [1992] have demonstrated that silicon with a high minority carrier lifetime can be grown from copper-rich silicon-copper melts. These and other reports demonstrate that at least several metals are suitable solvents for the growth of semiconductor-grade silicon and suggest that solvent compositions which do not excessively dope SiC should also be possible. As some corroboration of this, BRANDER and SUTTON [1969] cited experiemntal evidence in the solution growth of SiC from melts which contained aluminum, boron, copper, titanium, beryllium, and oxygen indicating distribution coefficients much less than unity and confirming a general impurity gettering effect in solution growth of SiC.

The epitaxial relation between the SiC film and the SiC or silicon substrate is another consideration. In general, for solution growth the silicon carbide polytype of the epitaxial layer is the same as that of the substrate or seed crystal [KNIPPENBERG and VERSPUI, 1969; DMIETRIV, 1991], although occasionally some polytype conversion is observed [BRANDER, 1973]. Freely nucleating, i.e., unseeded or homogeneously nucleated, silicon carbide crystals are almost always the β-SiC polytype [KNIPPENBERG, 1963; HALDEN, 1960; BECKMAN, 1963; BARTLETT *et al.*, 1967]. The cubic polytype is favored at growth temperatures less than 2000 °C.

BRANDER [1973] noted that the liquid-phase epitaxy of β-SiC on β-SiC substrates could only be achieved with melts that contained excess silicon, i.e.,

$$[\mathrm{Si}] > [\mathrm{C}]$$

where $[\mathrm{Si}]$ is the concentration of silicon in the melt and $[\mathrm{C}]$ is the concentration of carbon in the melt. This implies the melt composition may influence which SiC polytype crystallizes. TAIROV and YAS'KOV [1970] described a temperature-gradient, traveling melt zone technique in which an evaporated film of metal is sandwiched between a SiC and a seeding substrate.

The low solubility of carbon or SiC in almost all metal-based solvents below 1400 °C will limit the thickness of a silicon carbide epitaxial layer and also results in slow growth rates. In temperature-gradient or traveling zone growth as described above, a SiC source in contact with the melt prevents depletion of carbon and silicon. There is also some precedence for replenishing the melt via the vapor-phase. In vapor-liquid-solid growth (VLS) of SiC whiskers [RYAN *et al.*, 1967; KNIPPENBERG and VERSPUI, 1969; BERMAN and RYAN, 1971; KRISHNA and MARSHALL, 1971; PORTNOI *et al.*, 1974; BOOTSMA *et al.* 1984; POSTNIKOV *et al.*, 1984; MILEWSKI *et al.*, 1985; MOTOJIMA *et al.*, 1988; and MCMAHON *et al.*, 1991], vapor-phase carbon or silicon precursor compounds react at the surface of the melt which thus remains saturated with silicon and carbon. These approaches provide recourse for growing thick SiC layers, or achieving high SiC growth rates, despite the low solubility of carbon and/or SiC in the growth solution at temperatures below the melting point of silicon.

2.3 Prior Work on Epitaxial Lateral Overgrowth

Epitaxial Lateral Overgrowth (ELO), also called *Lateral Epitaxy*, has been previously developed for the most common semiconductors. For silicon, lateral epitaxy by zone melting and recrystallization with lasers, focused lights, electron beams, or moving strip heaters is successfully used to produce silicon-on-insulator (SOI) structures. A melting and recrystallization technique, however, generally cannot be used for compound semiconductors since these materials either melt incongruently, or decompose at high temperatures due to the volatility of at least one of their components. Instead, vapor- or liquid-phase epitaxy is used for lateral overgrowth.

JASTRZEBSKI *et al.* [1983] optimized silicon CVD with chlorosilanes to achieve lateral overgrowth on patterned, oxide-masked silicon substrates. TSAUR *et al.* [1982] showed limited lateral overgrowth of GaAs on masked GaAs substrates using chemical vapor deposition. A common deficiency in vapor-phase epitaxy is that aspect ratios are not much greater than 5. Also, GIVARGIZOV [1991] noted the difficulty with vapor-phase lateral epitaxy in avoiding nucleation of polycrystalline material on the masking layer due to excessive supersaturation in the vapor phase.

Liquid-phase epitaxial lateral overgrowth with silicon, GaAs, and GaP has shown much higher aspect ratios. This is because liquid-phase epitaxy generally occurs very close to thermodynamic equilibrium. (Near-equilibrium growth results in the highly anisotropic growth rates needed for high-aspect ratio lateral epitaxy.) Similar near-equilibrium conditions are difficult to achieve in vapor-phase epitaxy, especially MOCVD, and not achievable at all with MBE or ALE. BAUSER *et al.*, [1985, 1986, 1990] and SUZUKI and NISHINAGA [1989, 1990] grew silicon from liquid metals on patterned, oxide-masked silicon substrates with aspect ratios as high as 40. They observed that areas of the silicon film over the oxide mask were virtually free of defects. Similar overgrowth results for GaAs [NISHINAGA and SUZUKI, 1988] and GaP [SUZUKI and NISHINAGA, 1989] liquid-phase epitaxial lateral overgrowth have also been reported. Especially relevant to the use of ELO as a defect filter is the work of UJIEE and NISHINAGA [1989] who developed a combined MBE/LPE technique for lateral overgrowth of GaAs on silicon. An MBE GaAs-on-silicon functioned as a buffer layer which was masked with SiO_2 and patterned with stripe openings. Liquid-phase epitaxial lateral overgrowth of GaAs produced overgrown films that were free of dislocations. This, despite the 4% lattice mismatch and thermal expansion mismatch which otherwise results in GaAs-on-silicon films with on the order of 10^8 dislocations cm^{-2}. These reports demonstrate the main premise of the Phase I program; namely that epitaxial lateral overgrowth based on near-equilibrium growth techniques, such as liquid-phase epitaxy, can produce low-defect epitaxial layers despite considerable thermal stress and lattice mismatch.

AstroPower has previously developed epitaxial lateral overgrowth for silicon and GaAs on patterned metal- and oxide-masked substrates using near-equilibrium chemical vapor transport and liquid-phase epitaxy (FIGURE 6). Our results with these semiconductor materials have demonstrated the successful epitaxial lateral overgrowth of semiconductor films over patterned, masked substrates and have shown the utility of epitaxial lateral overgrowth for reducing defect densities and thermal stress. We have achieved aspect ratios of close to 200 by systematically optimizing the substrate orientation, the alignment of the stripe openings, the melt composition, and the growth conditions. This defect reduction is due in large part to the function of the mask as a defect filter (FIGURE 2). For example, dislocations due to lattice mismatch tend to propagate vertically from the growth interface. Consequently, areas of the epitaxial layer formed directly over the mask are free of defects. This has been confirmed by us for silicon and GaAs epitaxial lateral overgrowth.

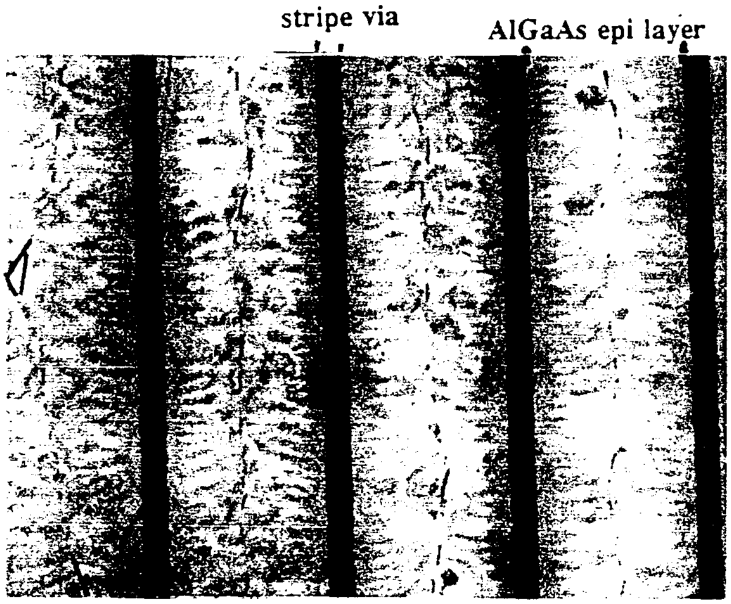

FIGURE 6: Top view photomicrograph of liquid-phase epitaxial lateral overgrowth of $Al_{0.5}Ga_{0.5}As$ on a tungsten-masked (111)GaAs wafer. The epitaxial layer is 2 microns thick. The stripe openings are 10 microns wide on 100 micron spacings.

2.4 Potential Advantages of SiC Solution Growth

Since lately solution growth for semiconductor epitaxy is often being superseded by molecular beam epitaxy, vapor-phase epitaxy, and atomic layer epitaxy, it is perhaps worthwhile to review some of the advantages of solution growth over these other epitaxy techniques. Further, it should be emphasized that our objective is to produce surrogate substrate structures to be used in place of bulk silicon carbide crystals. Therefore, many of the long standing drawbacks and objections to liquid-phase epitaxy (such as the inability to grow ultrathin layers or superlattices, or poor control of layer composition) are *not* relevant to the proposed work. An optional polishing step to achieve a mirror-smooth, highly-uniform finish on the surface of the SiC-on-silicon layer can also be considered. This will ameliorate any problems related to a less-than-perfect surface morphology that may be characteristic of the solution growth process. A brief discussion of the potential advantages inherent in solution growth of SiC is given below.

Lower Growth Temperatures. The use of silicon-metal alloy solvents for the growth of SiC will permit significantly lower growth temperatures. Furthermore, the replenishment of the solution from the vapor-phase allows thick layers to be grown at untypically low temperatures since solute (i.e., carbon) depletion of the solution is avoided. Growth temperatures in the range of 1000 to 1400°C may be feasible with a silicon-metal growth solution replenished by a gaseous carbon precursor. Lower growth temperatures will result in reduced thermal stress, reduced impurity levels and auto doping, improved compatibility (no melting of the substrate) with the silicon substrate, and fewer grown-in defects. Reduced growth temperature also simplify equipment design.

Near-Equilibrium Growth. In comparison to CVD, liquid-phase epitaxial growth occurs close to thermodynamic equilibrium. This results in fewer point defects such as vacancies, interstitials, and anti-site defects which act as carrier traps and non-radiative recombination centers [MAHAJAN, 1989]. Near-equilibrium solution growth produces very high-quality semiconductor material with respect to minority carrier lifetimes [MOON, 1980; HSIEH, 1980; LU *et al.*, 1992]. The near-equilibrium growth conditions are also necessary for achieving epitaxial lateral overgrowth with high aspect ratios. This is a unique advantage of liquid-phase epitaxy. As a comparison, normally the supersaturation in LPE corresponds to a 1 to 2 KCal/mole whereas typical supersaturations in MOCVD are as high as 25 KCal/mole and 15 Kcal/mole in MBE [WATANABE *et al.*, 1990]. Some near-equilibrium vapor-phase epitaxies develop supersaturations in the range of 1 to 5 Kcal/mole. Of all epitaxy techniques, LPE is closest to thermodynamic equilibrium.

Wide Range of Dopants. There is a wide selection of dopants which can be used in solution growth of SiC. For doping in CVD, gaseous impurity compounds are available as dopant precursors. On the other hand, controlled substitutional impurity doping can be achieved in solution growth by simply adding a predetermined amount of dopant to the melt. A relatively large number of dopants can be easily used in solution growth. This doping flexibility is important since the ionization energies of dopants vary considerably in SiC and full optimization of device performance may depend on a judicious choice of the dopant.

Faster Growth Rates. Relative to CVD, high growth rates can be achieved with solution growth at comparable temperatures. SiC growth rates as high as 0.5 to 2 microns per minute may be feasible. This is 10 to 60 times faster than what is typically reported for CVD growth of SiC ($\approx$ 3 microns/hour).

Growth Stabilization. Another potential advantage of the VLS technique over conventional solution growth is related to the possibility of inducing appreciable temperature gradients at the growth interface. Such temperature gradients can suppress growth instabilities, such as constitutional supercooling, and thereby further increase growth rates. The growth rates can be enhanced considerably since the liquid phase can be made thin, thereby increasing the solute diffusion rates. In this respect, the VLS technique is similar to the *traveling solvent* or *thin melt zone* crystallization technique mentioned previously. In the traveling solvent method as applied to SiC [GRIFFITHS and MLAVSKY, 1964; WRIGHT, 1965], a temperature gradient is imposed across a thin metal solvent zone sandwiched between two wafers of SiC. The temperature difference establishes a silicon carbide concentration gradient and silicon carbide diffuses through the liquid zone and precipitates on the cooler substrate. Using chromium solvents, growth rates up to 10 microns/min. have been achieved.

Selective Growth. Selective epitaxy and lateral epitaxial overgrowth are possible with solution growth. Reduced growth areas in selective epitaxy can be used to reduce the effects of residual stress. For example, YAMAGUCHI *et al.* [1990] have shown that for GaAs-on-silicon, a reduction in growth area by selective epitaxy can reduce thermal stress and stress-induced dislocations by more than an order of magnitude.

Reduction of Threading Dislocations. As observed in III-V compound In solution growth of semiconductors, there is also some observed tendency to "anneal-out" dislocations originating in the substrate or at the substrate-film interface [QUEISSER, 1972].

Reduced Concentration of Heavy Metals. In metallic solution growth almost all impurities, particularly heavy metals, preferentially segregate to the liquid phase. For example, in metallic solution growth of silicon the concentration of heavy metals in the silicon film can be reduced by several orders of magnitude from that observed with CVD [BALIGA, 1986].

Fewer Oxygen-Induced Defects. D'ASARO *et al.* [1969] cite evidence which suggests that many defects in melt-grown silicon are caused by the precipitation of impurities with low electrical activity, such as oxygen. Lower growth temperatures and the use of oxygen getterers (such as small amounts of aluminum or gallium) will reduce the concentration of oxygen in the epitaxial films.

Low Equipment and Operating Cost. The equipment and instrumentation are relatively inexpensive. There are no highly toxic precursors or byproducts associated with the proposed process.

3. PHASE I WORK AND RESULTS

Liquid-phase epitaxy of SiC directly on silicon substrates is probably not feasible due to the relatively large (20%) lattice mismatch between silicon and SiC, and 2, the relatively high solubility of silicon in many of the solvents used for SiC LPE. With regard to the first point, lattice mismatches greater than about 1% impede nucleation in LPE because of the near-equilibrium growth conditions. This does not seem to be a limitation in vapor-phase growth where a high thermodynamic driving force (i.e., a high supersaturation) for nucleation can be achieved. Therefore, in the Phase I program, we developed heteroepitaxy of SiC on silicon substrates using only vapor-phase epitaxy techniques and limited solution growth experiments to epitaxy on SiC substrates. Experimental work in the related area of liquid-phase epitaxial lateral overgrowth of silicon films on patterned, masked silicon substrates was also deemed useful in order to study issues related to mask materials, mask patterning, and alignment and spacing of stripe via patterns. This latter work on lateral overgrowth of silicon on silicon substrates permitted us to conserve SiC substrates which are very expensive. The Phase I research logically divided into three areas: 1. experiments for selective vapor-phase epitaxy on patterned, oxide-masked (111) silicon substrates (section 3.2), 2. experiments for solution growth epitaxy on patterned, masked (1000) 6-H SiC substrates (section 3.3), and 3. experiments on liquid-phase epitaxial lateral overgrowth of silicon on patterned, oxide-masked (111) silicon substrates (section 3.4). Prior to the solution growth work, it was necessary to obtain single-crystal SiC substrates as described in section 3.1.

3.1 Procurement of SiC Substrates and SiC Source Material

An inventory of high purity SiC material was needed to commence the experimental work. This is not trivial since single crystal silicon carbide substrates are quite expensive and many (25 to 50) epitaxy experiments were needed. While in some cases substrates can be re-used, there is still a significant fraction of experiments where this is neither feasible nor desirable. At any rate, we estimate 20 to 40 1-cm^2 single crystal substrates will be required for the Phase I program. The sole domestic supplier is Cree Research, Inc. Their latest prices for single-crystal SiC wafers are approximately $800 per square cm. Commercial heteroepitaxial SiC on silicon substrates are even more expensive. In view of the constraints of the Phase I budget and the requirements of the experimental work, these prices are deemed prohibitive. Instead, we ordered single-crystal 6H-SiC substrates from FTIKKKS Ltd. (St. Petersburg, Russia), which sell for $100 per square centimeter. The FTIKKKS substrates have the following specifications:

FTIKKS Silicon Carbide Substrates

polytype: 6H
orientation: (0001)
off-axis orientations: 0, 1.0, 2.0., or 3.0° toward $\langle 1100 \rangle$ or $\langle 1120 \rangle$
etch pit density: 10^{2} cm^{-2}
n-type doping: 1 to 5 10^{18} cm^{-3}
thickness: 0.3 to 0.45 mm
polishing: silicon face

A few nominally (0001) 6H-SiC substrates were also obtained from Cree Research, Inc. The exact specifications of this material were not provided. Some preliminary X-ray diffraction analysis on these substrates was provided by Dr. Ilan Golecki of Allied-Signal (Morristown, NJ), and indicated the presence of several polytypes in these substrates.

High purity polycrystralline SiC material was purchased from Dallas Ceramics (Rowlett, TX). This material is obtained in rectangular plates and will be used as source material for LPE and CVD.

3.2 Chemical Vapor Transport for SiC-on-Silicon Heteroepitaxy

We developed a selective SiC-on-silicon vapor-phase heteroepitaxy process with hexamethydisilane (HMDS) as the silicon and carbon precursor according to a technique first reported by TAKAHASHI *et al.* [1992], and further developed by NORDELL *et al.* [1994, 1995]. This work was reviewed in section 2.1. Our objective was to experimentally optimize this technique for *selective* growth of SiC on patterned, oxide-masked silicon substrates.

FIGURES 7 and 8 are top-view photomicrographs of selectively grown SiC on a (111) patterned, oxide-masked Si substrate using HMDS as a precursor. The mask is 100-nm thick thermally grown silicon dioxide patterned with 10-micron wide stripe openings with 100-micron spacings. The ambient was Pd-purified hydrogen at 1 atm pressure and a flow rate of 30 ml/min bubbled through HMDS liquid at room-temperature. The SiC crystals are approximately 2 microns thick and are transparent with a slight greenish tinge. The sample of FIGURE 7 was grown at a substrate temperature of 1100 °C and shows much spurious nucleation and growth on the oxide mask. By lowering the growth temperature to 1050 °C, the SiC is much more selective and there is relatively little deposit on the mask (FIGURE 8). This demonstrates that by controlling growth conditions, selective epitaxy of SiC on silicon can be achieved with this process.

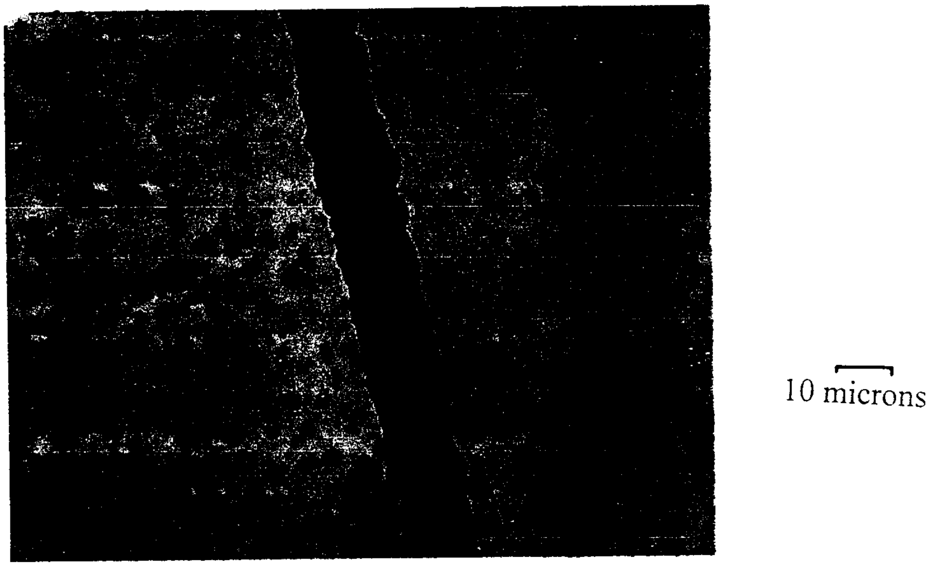

FIGURE 7: Top-view photomicrograph showing selectively grown SiC on a (111) patterned, oxide-masked Si substrate with a substrate temperature of 1100 °C. There is considerable deposition of SiC on the oxide mask.

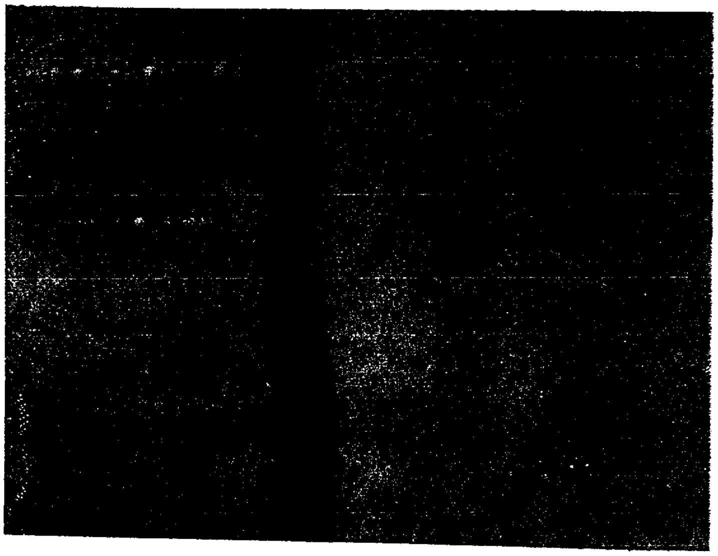

FIGURE 8: Top-view photomicrograph showing selectively grown SiC on a (111) patterned, oxide-masked Si substrate with a substrate temperature of 1050 °C. There is relatively little deposition of SiC on the oxide mask.

3.3. Liquid-Phase Epitaxy of SiC

Liquid-phase epitaxy (LPE) of silicon carbide is well established. Conventional SiC LPE employs molten silicon as a solvent. The low solubility of carbon in silicon necessitates high growth temperatures. We investigated metal solvents for SiC starting with some of the more promising metal solvents suggested by previous workers (see section 2.3).

We investigated metallic solution growth of SiC from a number of solutions including:

- Pb saturated with SiC at 1070 and 1140 °C
- Sn saturated with SiC at 1250 °C
- Cu saturated with SiC at 1040 and 1150 °C
- Ge saturated with SiC at 1160 °C [TAIROV *et al.*, 1981]
- Sb saturated with SiC at 1160 °C
- Au saturated with SiC at 1040 °C
- Pb:Sn (1:1) saturated with SiC at 1250 °C
- Cu:Pb (1:1) saturated with SiC at 1145 °C
- Ni:Si (8:5) saturated with SiC at 1250 °C [BAUMANN, 1952]
- Pb:Sn:Al (1:1:0.001) saturated with SiC at 1160 °C
- Zn:Al:Si:C (3:1.5:0.8:0.4) at 940 °C [BAUMANN, 1952]

The weight ratios are indicated in parentheses. Some of these melt compositions and temperatures were suggested by the prior work reported in the literature as cited. Approximately twenty-five SiC LPE experiments were performed during the Phase I program.

For liquid-phase epitaxy of SiC, we used a standard horizontal slideboat technique as is commonly employed for the epitaxy of III-V compound optoelectronic devices [CASEY and PANISH, 1978]. The graphite (Poco Graphite grade DF-3) slideboat is situated in a 50-mm diameter fused quartz tube placed in a microprocessor-controlled horizontal furnace. The ambient is palladium-purified hydrogen at atmospheric pressure and a flow rate of 50 cc/min.

The substrates are 0.8 cm x 1 cm (0001) nominally 6H-SiC wafers as described in section 3.1. The metals are of at least 5-9s purity, obtained in 3-mm shot form from Alfa Aesar. The melts were saturated with carbon by equilibrating them in contact with a SiC wafer for at least two hours at the growth temperature. In some cases carbon was added to the melt in the form of high-purity graphite powder. Additional silicon, when desired, was added to the melt in the form of silicon wafer fragments.

Both unmasked and masked SiC substrates were used. The masked substrates were coated with a 100- to 200-nm thick film of silicon nitride or tungsten. The silicon nitride mask was deposited by plasma-enhanced chemical vapor deposition. The tungsten mask was deposited by sputtering. The mask was then patterned by photolithography and selective etching to form circular are stripe openings to expose the underlying SiC substrate. The array of circular openings were 5 microns in diameter, spaced 100 microns apart. The stripe openings were 10 microns wide, spaced 100 microns apart.

To initiate growth, the equilibrated melts were supercooled 5 to 10 °C. The SiC seed substrate was then contacted with the melt and the a programmed ramp-cooling of 0.25 °C/min. After a growth time of 1 to 6 hours, the melt was separated from the substrate. Excess melt was removed by etching in aqua regia ($HCl:HNO_3$) solutions or other acid etchants as appropriate for the melt composition. The substrates were then examined by optical and scanning electron microscopy for the presence of any crystallization.

We now present some of the more significant results of our SiC LPE experiments. SiC crystallization from the melt was indicated by the presence of selectively nucleated, faceted crystals in the mask openings. The crystals were thicker than the mask and consequently protruded above the masked substrate surface. The crystals had a characteristic hexagonal morphology of 6H-SiC and exhibited a definite oriented (i.e., epitaxial) relationship with the single-crystal SiC substrate. These observations were made with an optical and a scanning electron microscope. The heights of the crystals (which range from a few tenths of a micron to several microns or more) were measured with a surface profiler. Energy Dispersive X-ray analysis determined that the crystals were silicon with some carbon content. This analysis is not particularly sensitive to carbon so the stoichiometry or Si:C ratio of the crystals could not be quantified. No other metal component of the melt was detected in the crystal by Energy Dispersive X-ray Analysis, the sensitivity of which for these metals is at about atomic% concentration level. The crystals did not show any dissolution in the known etchants for silicon such as $HF:HNO_3$, implying that the crystals were not silicon. The discrete crystals were generally too small for X-ray diffraction analysis. Some of the thicker SiC epitaxial films will be evaluated by X-ray diffraction analysis. (Dr. Ilan Golecki of Allied-Signal, Morristown, NJ has offered to perform X-ray analysis on our SiC samples.)

FIGURE 9 is a top-view photomicrograph of (0001)SiC crystals grown from copper saturated with SiC at 1160 °C on an unmasked SiC substrate. FIGURE 10 is a scanning electron micrograph of a SiC crystal selectively grown in a 5-micron diameter opening of a Si_3N_4 mask coating a SiC substrate. The selectively-nucleated SiC crystals were grown from molten copper saturated with SiC. Growth was effected by cooling the Cu-Si-C solution in contact with substrate from 1045 to 920 °C over 4 hours. While the circular opening in the mask was 5 microns in diameter, the SiC crystal is almost 10 microns wide, indicating some overgrowth of the nitride mask.

FIGURE 11 is a photomicrograph of a cleaved sample showing the cross-section of a SiC epitaxial layer on a SiC substrate. This layer was grown from an Ni:Si (0.8 g : 0.5 g) melt saturated with SiC at 1250 °C. During growth the melt was cooled from 1250 to 1090 °C over 3 hours. FIGURE 12 is the same sample cross-section under higher magnification.

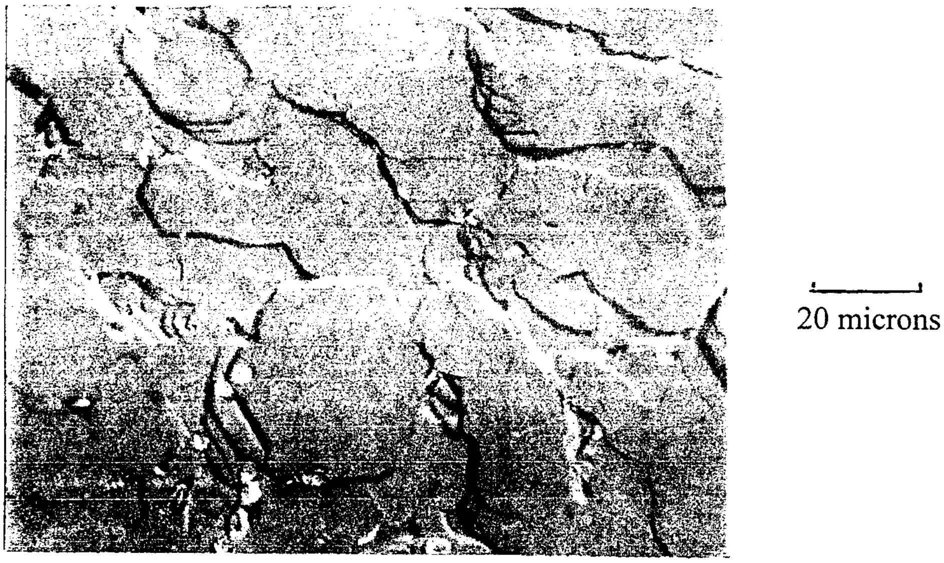

FIGURE 9: Top-view photomicrograph of (0001)SiC crystals grown from copper saturated with SiC at 1160 °C on an unmased SiC substrate.

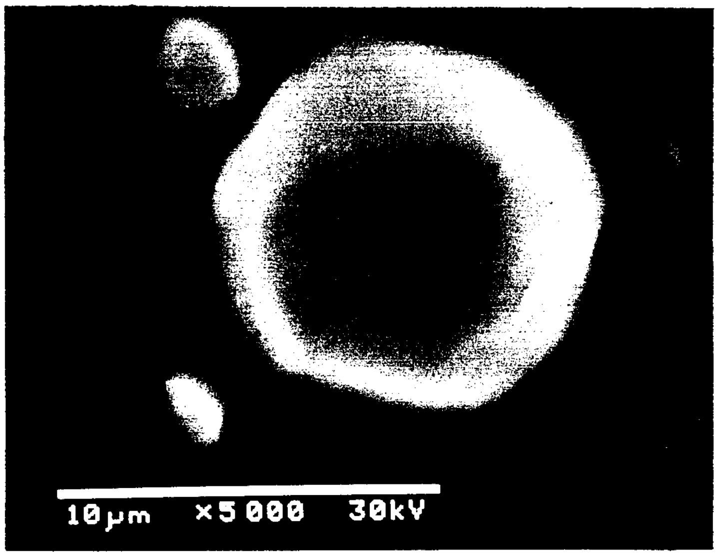

FIGURE 10: Scanning electron micrograph of a SiC crystal selectively grown in a 5-micron diameter opening of a Si_3N_4 mask coating a SiC substrate.

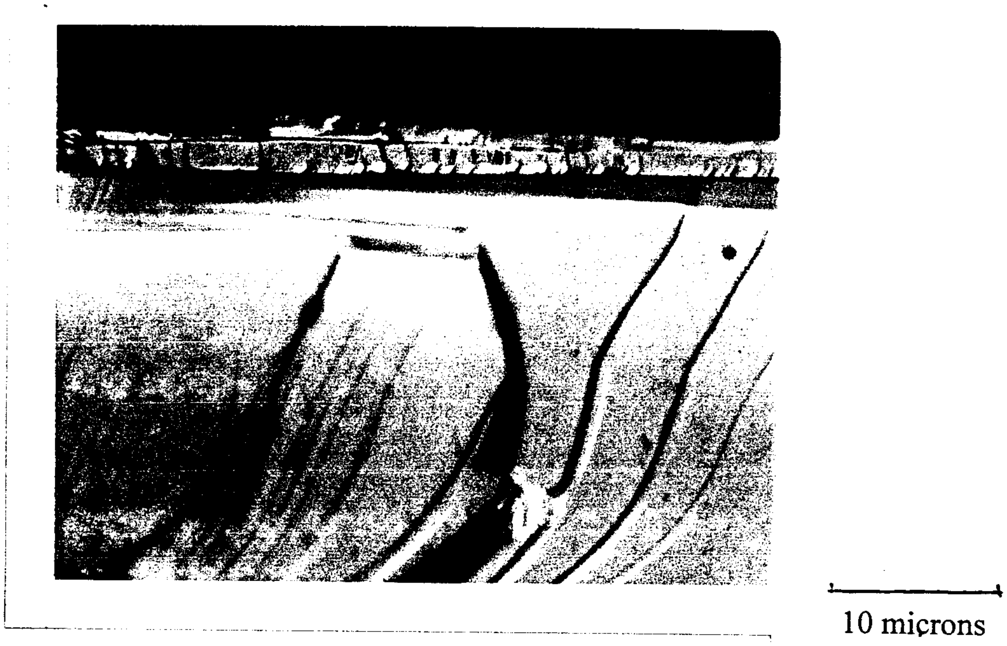

FIGURE 11: Photomicrograph of a cleaved sample showing the cross-section of a SiC epitaxial layer on a SiC substrate.

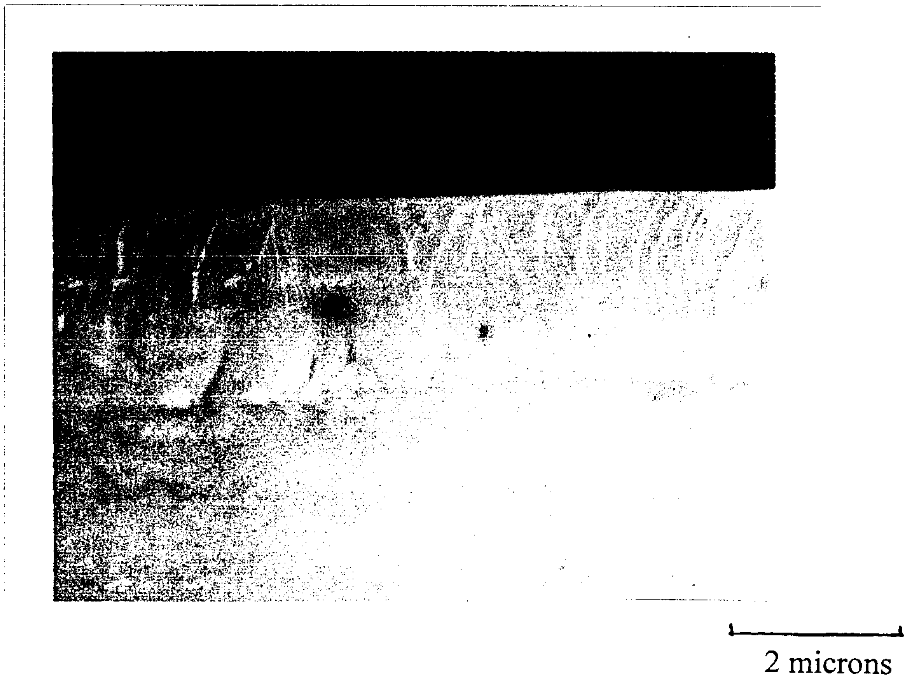

FIGURE 12: Same sample as FIGURE 11, cross-section under higher magnification.

3.4 Epitaxial Lateral Overgrowth of Silicon

While developing a solution-growth process for SiC, we simultaneously investigated epitaxial lateral overgrowth of Si on patterned, masked substrates using liquid-phase epitaxy. In epitaxial lateral overgrowth, the substrate is masked with a dielectric or refractory metal film. The film is patterned with stripe openings which expose areas of the underlying substrate. The exposed substrate areas serve as sites for preferential nucleation of a silicon carbide film. As growth proceeds, the selectively nucleated SiC films overgrow the mask. This lateral overgrowth yields a structure which simulates an epitaxial film formed on a foreign substrate, and as such, can be used to dielectrically isolate the film from the substrate. Of more interest to the present application is the use of the mask layer as a defect filter. Since defects tend to propagate vertically from the growth interface (normal to the plane of the substrate), areas of the film overgrown atop the mask should exhibit a substantial reduction in defects compared to films grown on unmasked substrates. As discussed, this phenomenon may be useful for reducing or eliminating so-called *micropipe defects* that have plagued SiC material.

We first applied this technique to Si solution growth from Pb, Sn, and Pb-Sn solvents. Our purpose was to first investigate liquid metals as solvents for high-temperature solution growth without sacrificing silicon carbide substrates. The main differences between SiC LPE and Si LPE are:

1. Silicon is somewhat more soluble in these metals than is carbon or SiC.
2. The silicon substrate is more susceptible to oxidation than is SiC. Surface oxides on the substrate tend to impede epitaxial growth.
3. SiC exhibits polytypism whereas crystalline silicon exists in only the diamond structure.

Silicon was grown on (111) Si substrates at 1050 to 1100 °C using a standard slideboat technique [CASEY and PANISH, 1978]. FIGURES 13 and 14 are micrographs of epitaxial growth on silicon substrates from Sn and Pb-Sn solvents. The substrates a masked with a patterned, tungsten coating. It is clear that it feasible to grow silicon selectively on silicon.

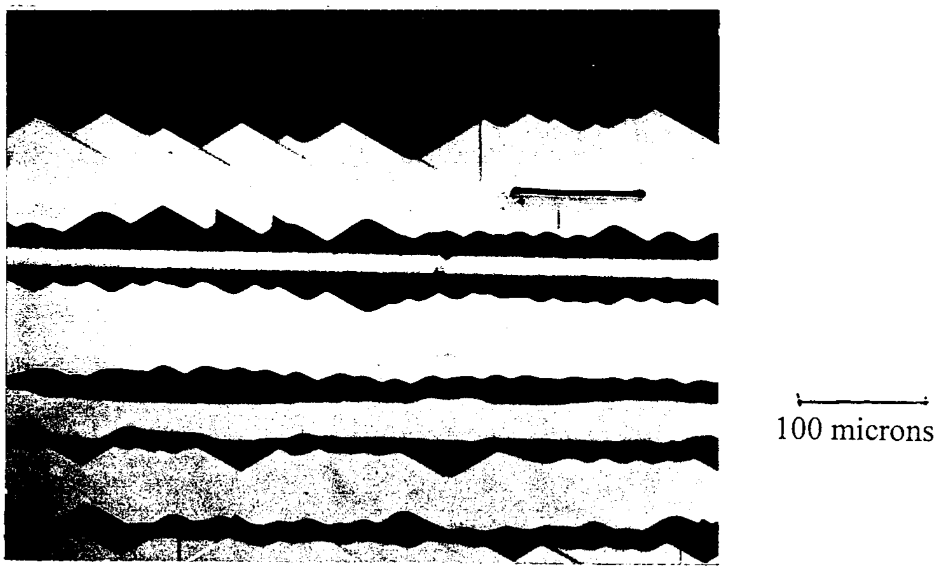

Figure 13: Photomicrograph of silicon selectively grown on a tungsten-masked (111) silicon substrate. The mask is patterned with 10-micron wide stripe openings on 100-micron spacings. The crystals nucleated at each stripe show significant lateral overgrowth of the tungsten mask.

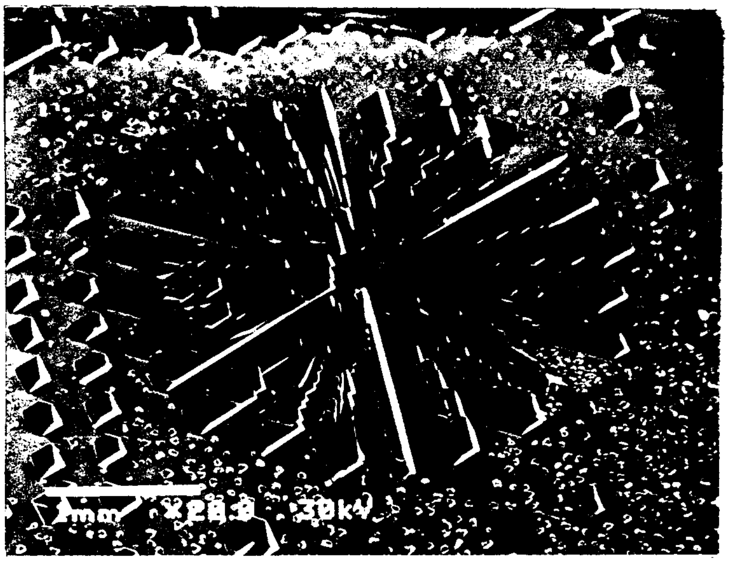

Figure 14: Scanning electron micrograph of silicon selectively grown on a tungsten-masked (111) silicon substrate. The mask is patterned with 10-micron wide stripe openings on 100-micron spacings arranged in a radial pattern. The extend of lateral overgrowth depends on the stripe opening, indicating that the crystallographic alignment of the stripe opening can be optimized to increase the extent of lateral overgrowth.

4. SUMMARY, DISCUSSION, AND CONCLUSION

We believe the Phase I work has experimentally demonstrated all the critical components needed to develop low-cost, low-defect SiC surrogate substrates. The significant results of the Phase I program are:

- SiC was selectively grown on patterned, oxide-masked silicon substrates using a simple vapor-phase epitaxy process.
- Metal solvents for SiC LPE were identified. In certain cases, some epitaxial lateral overgrowth was observed for SiC LPE on patterned, nitride masked 6-H SiC.
- Epitaxial lateral overgrowth of silicon on patterned, metal-masked silicon substrates was demonstrated.

In the Phase II program, we propose to combine these steps as follows. A silicon substrate will be masked with an oxide, nitride, or refractory metal. The mask will be patterned with stripe openings. SiC will be selectively-grown in the stripe openings using a vapor-phase epitaxy process with HMDS as the Si and C precursor. The selectively-grown SiC-on-silicon structures will then be used as substrates for liquid-phase epitaxial lateral overgrowth of SiC. Such lateral epitaxy will utilize the defect filtering effect of the mask to eliminate micropipe defects, stacking faults, and dislocations in the SiC epitaxial layer. This material will serve as a low-cost, low-defect SiC surrogate substrate. A large part of the Phase II program will concentrate on identifying better metal-based solvents for SiC LPE and optimizing the epitaxial lateral overgrowth process for SiC. Several variations of this process, depending on intended device applications, are also evident to us.

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Appendix:
PHASE-EQUILIBRIA MODELING FOR SOLUTION GROWTH OF SIC

To evaluate other metal solvents or mixtures of metal solvents for solution growth of SiC, it is useful to develop phase equilibria models. The utility of such a model is based on extending the limited experimental data available. SiC solubilities can be extrapolated to wider temperature ranges. The thermodynamic consistentcy of solubility data can be assessed. More importantly, the models can be generalized to estimated the solubility of silicon carbide in solvent mixtures which might have more optimal characteristics than elemental solvents. Finally, the models are useful for estimating segregation coefficients which are needed to controlably dope the epitaxial films and which also provide an indication of the sensitity to impurities and potential of impurity gettering effects.

The phase equilibria for silicon carbide crystallization from a metal solvent is established based on the following criteria.

The solidfication of SiC from a liquid solution containing silicon and carbon as solutes is described by the reaction

$$\mathrm{Si(L)} + \mathrm{C(L)} \rightarrow \mathrm{SiC(S)}$$

which implies the following relation between the chemical potentials of silicon and carbon in the liquid phase and SiC in the solid phase

$$\mu_{\mathrm{Si}}^{\mathrm{L}} + \mu_{\mathrm{C}}^{\mathrm{L}} = \mu_{\mathrm{SiC}}^{\mathrm{S}}$$

This can be formulated in terms of the silicon and carbon liquid-phase activities as

$$\mu_{\mathrm{Si}}^{L,\ominus}(T) + RT\ln a_{\mathrm{Si}} + \mu_{\mathrm{C}}^{\mathrm{L},\ominus}(T) + RT\ln a_{\mathrm{C}} = \mu_{\mathrm{SiC}}^{\mathrm{S},\ominus}(T)$$

where $\mu_{\mathrm{Si}}^{L,\ominus}$ is the chemical potential of pure liquid silicon, $\mu_{\mathrm{C}}^{L,\ominus}$ is the chemical potential of pure liquid carbon, and $\mu_{\mathrm{SiC}}^{S,\ominus}$ is the chemical potential of pure solid silicon carbide. We mention that carbon does not exist in liquid form at one atmopshere pressure at any temperature and therefore $\mu_{\mathrm{C}}^{L,\ominus}$ refers to a hypothetical state of carbon that must be ultimately related to some measureable thermodynamic state of carbon, such as graphite. We have neglected the distribution of metals, silicon, or elemetal carbon in the solid phase which we assume is pure SiC.

The activities are related to the liquid-phase concentrations as

$$a_{\mathrm{Si}} = \gamma_{\mathrm{Si}} \cdot X_{\mathrm{Si}}$$
$$a_{\mathrm{C}} = \gamma_{\mathrm{C}} \cdot X_{\mathrm{C}}$$

where X_{Si} and X_{C} are the atomic fractions of Si and C in the molten solution and γ_{Si} and γ_{C} are the activity coefficients of Si and C. The liquidus curve in terms of activity coefficients is

$$\mu_{\mathrm{Si}}^{L,\ominus} + RT \cdot \ln\{\gamma_{\mathrm{Si}}^{L} \cdot X_{\mathrm{Si}}\} + \mu_{\mathrm{C}}^{L,\ominus} + RT \ln\{\gamma_{\mathrm{C}}^{L} \cdot X_{\mathrm{C}}\} = \mu_{\mathrm{SiC}}^{S,\ominus}$$

$$(\mu_{\mathrm{Si}}^{L,\ominus} - \mu_{\mathrm{Si}}^{S,\ominus}) + RT \cdot \ln\{\gamma_{\mathrm{Si}}^{L} \cdot X_{\mathrm{Si}}\} + (\mu_{\mathrm{C}}^{L,\ominus} - \mu_{\mathrm{C}}^{S,\ominus}) + RT \ln\{\gamma_{\mathrm{C}}^{L} \cdot X_{\mathrm{C}}\} = \mu_{\mathrm{SiC}}^{S,\ominus} - \mu_{\mathrm{Si}}^{S,\ominus} - \mu_{\mathrm{C}}^{S,\ominus}$$

The right side of the above equation is the Gibbs Free-Energy of Formation of SiC from crystalline Si(c) and graphite C(graph)

$$\mathrm{Si(c)} + \mathrm{C(graph)} \rightarrow \mathrm{SiC(s)}$$

$$\mu_{\mathrm{SiC}}^{S,\ominus} - \mu_{\mathrm{Si}}^{S,\ominus} - \mu_{\mathrm{C}}^{S,\ominus} = -\Delta G_{\mathrm{SiC}}^{F}(T)$$

The term $(\mu_{\mathrm{Si}}^{L,\ominus} - \mu_{\mathrm{Si}}^{S,\ominus}$ is the Gibbs Free Energy of Fusion of pure silicon denoted as $-\Delta G_{Si}^{FUS}(T)$. The equation for the solubility of Si and C in the liquid phase is then

$$-\Delta G_{\mathrm{Si}}^{FUS}(T) + RT \cdot \ln\{\gamma_{\mathrm{Si}}^{L} \cdot X_{\mathrm{Si}}\} + (\mu_{\mathrm{C}}^{L,\ominus} - \mu_{\mathrm{C}}^{S,\ominus}) + RT \ln\{\gamma_{\mathrm{C}}^{L} \cdot X_{\mathrm{C}}\} = \Delta G_{\mathrm{SiC}}^{F}(T)$$

We assume *simple* solution behavior, in which case the activity coefficients are expressed in terms of binary interaction parameters Ω_{ij} which in general are a function of temperature of a form such as, for example,

$$\Omega_{ij} = a_{ij} - b_{ij} \cdot T + c_{ij} \cdot T^2$$

or as in the quasi-regular solution model, by a simple linear function of temperature

$$\Omega_{ij} = a_{ij} - b_{ij} \cdot T$$

JORDAN [1974] has derived a relation between the acitivity coefficients γ_i, the liquid compositions X_i, the binary interaction parameters Ω_{ij}, and the temperature T for an *m*-component simple solution as

$$RT\ln\gamma_i = \sum_{\substack{j=1\\ i\neq i}}^{m} \Omega_{ij}\cdot X_j^2 + \sum_{\substack{k=1,\\ k<j}}^{m}\sum_{j=1}^{m} X_k\cdot X_j\cdot(\Omega_{ij}+\Omega_{ik}-\Omega_{kj}$$

For a four-component system, Si-C-M1-M2, the activity coefficients of silicon and carbon can be expressed explicitly in terms of interaction parameters and solution composition as

$$\begin{aligned} RT\ln\gamma_{\mathrm{Si}} &= \Omega_{\mathrm{Si-C}}\cdot X_{\mathrm{C}}^2 + \Omega_{\mathrm{Si-M1}}\cdot X_{\mathrm{M1}}^2 + \Omega_{\mathrm{Si-M2}}\cdot X_{\mathrm{M2}}^2 + X_{\mathrm{C}}\cdot X_{\mathrm{M1}}\cdot(\Omega_{\mathrm{Si-C}}+\Omega_{\mathrm{Si-M1}}-\Omega_{\mathrm{C-M1}}) \\ &\quad + X_{\mathrm{C}}\cdot X_{\mathrm{M2}}\cdot(\Omega_{\mathrm{Si-C}}+\Omega_{\mathrm{Si-M2}}-\Omega_{\mathrm{C-M2}}) + X_{\mathrm{M1}}\cdot X_{\mathrm{M2}}\cdot(\Omega_{\mathrm{Si-M1}}+\Omega_{\mathrm{Si-M2}}-\Omega_{\mathrm{M1-M2}}) \end{aligned}$$

$$\begin{aligned} RT\ln\gamma_{\mathrm{C}} &= \Omega_{\mathrm{Si-C}}\cdot X_{\mathrm{Si}}^2 + \Omega_{\mathrm{C-M1}}\cdot X_{\mathrm{M1}}^2 + \Omega_{\mathrm{C-M2}}\cdot X_{\mathrm{M2}}^2 + X_{\mathrm{Si}}\cdot X_{\mathrm{M1}}\cdot(\Omega_{\mathrm{Si-C}}+\Omega_{\mathrm{C-M1}}-\Omega_{\mathrm{Si-M1}} \\ &\quad + X_{\mathrm{M1}}\cdot X_{\mathrm{M2}}\cdot(\Omega_{\mathrm{C-M1}}+\Omega_{\mathrm{C-M2}}-\Omega_{\mathrm{M1-M2}}) + X_{\mathrm{Si}}\cdot X_{\mathrm{M2}}\cdot(\Omega_{\mathrm{Si-M1}}+\Omega_{\mathrm{C-M2}}-\Omega_{\mathrm{Si-M2}}) \end{aligned}$$

$$RT\ln X_{Si} + RT\ln X_C + RT\ln\gamma_{Si}^{L} + RT\ln\gamma_C + (\mu_C^{L,\Theta}-\mu_C^{S,\Theta}) = \Delta G_{\mathrm{SiC}}^{F}(T) + \Delta G_{Si}^{FUS}(T)$$

or in terms of interaction parameters, the liquidus surface of the Si-C-M1-M2 quaternary is given by

$$\begin{aligned} & RT\ln X_{Si} + RT\ln X_C - (\mu_C^{L,\Theta}-\mu_C^{S,\Theta}) - \Delta G_{\mathrm{SiC}}^{F}(T) + \Delta G_{Si}^{FUS}(T) \\ & + \Omega_{\mathrm{Si-C}}\cdot X_{\mathrm{C}}^2 + \Omega_{\mathrm{Si-M1}}\cdot X_{\mathrm{M1}}^2 + \Omega_{\mathrm{Si-M2}}\cdot X_{\mathrm{M2}}^2 + X_{\mathrm{C}}\cdot X_{\mathrm{M1}}\cdot(\Omega_{\mathrm{Si-C}}+\Omega_{\mathrm{Si-M1}}-\Omega_{\mathrm{C-M1}}) \\ & + X_{\mathrm{C}}\cdot X_{\mathrm{M2}}\cdot(\Omega_{\mathrm{Si-C}}+\Omega_{\mathrm{Si-M2}}-\Omega_{\mathrm{C-M2}}) + X_{\mathrm{M1}}\cdot X_{\mathrm{M2}}\cdot(\Omega_{\mathrm{Si-M1}}+\Omega_{\mathrm{Si-M2}}-\Omega_{\mathrm{M1-M2}}) \\ & + \Omega_{\mathrm{Si-C}}\cdot X_{\mathrm{Si}}^2 + \Omega_{\mathrm{C-M1}}\cdot X_{\mathrm{M1}}^2 + \Omega_{\mathrm{C-M2}}\cdot X_{\mathrm{M2}}^2 + X_{\mathrm{Si}}\cdot X_{\mathrm{M1}}\cdot(\Omega_{\mathrm{Si-C}}+\Omega_{\mathrm{C-M1}}-\Omega_{\mathrm{Si-M1}}) \\ & + X_{\mathrm{M1}}\cdot X_{\mathrm{M2}}\cdot(\Omega_{\mathrm{C-M1}}+\Omega_{\mathrm{C-M2}}-\Omega_{\mathrm{M1-M2}}) + X_{\mathrm{Si}}\cdot X_{\mathrm{M2}}\cdot(\Omega_{\mathrm{Si-M1}}+\Omega_{\mathrm{C-M2}}-\Omega_{\mathrm{Si-M2}}) \\ & = 0 \end{aligned}$$

2.2.1 Evaluation of Si and C Liquid-Phase Activities from Related Binaries

The interaction parameters are derived from related binaries or pseudobinaries

- **a.** Si-C Binary $(\Omega_{\text{Si-C}})$
- **b.** Si-Metal Binaries $(\Omega_{\text{Si-M}})$
- **c.** C-Metal Binaries $(\Omega_{\text{C-M}})$
- **d.** SiC solubility in liquid metals $(\Omega_{\text{Si-C}})$
- **e.** Metal-Metal Binaries $(\Omega_{\text{M1-M2}})$

There are also theoretical and semi-empirical equations to predict interaction parameters. In addition, some measurement or estimate of

a. The Si-C Binary

The liquidus curve for Si-rich SiC binary, which is essentially the temperature-dependent solubility of carbon in molten silicon, is given by

$$RT\ln X_{\text{C}} + RT\ln\gamma_{\text{C}} = (\mu_{\text{C}}^{L,\ominus} - \mu_{\text{C}}^{S,\ominus}$$

Assuming simple solution behavior

$$RT\cdot\ln\gamma_{\text{C}}^{L} = \Omega_{\text{Si-C}}\cdot X_{\text{S}i}^{2} = \Omega_{\text{Si-C}}\cdot(1 - X_{\text{C}})^{2}$$

so that the carbon liquidus is

$$RT\ln X_{\text{C}} + \Omega_{\text{Si-C}}\cdot(1 - X_{\text{C}})^{2} = (\mu_{\text{C}}^{L,\ominus} - \mu_{\text{C}}^{S,\ominus}$$

Since the carbon solubility in liquid silicon is relatively low for the temperature range of interest, we can assume Henry's Law behavior, or in effect, that the activity coefficient is independent of compostion, i.e.,

$$RT\ln\gamma_{\text{C}} = \Omega_{\text{Si-C}}\cdot(1 - X_{\text{C}})^{2} \cong \Omega_{\text{Si-C}}$$

So that

$$\ln X_{\text{C}} \cong \frac{(\mu_{\text{C}}^{L,\ominus} - \mu_{\text{C}}^{S,\ominus}) - \Omega_{\text{Si-C}}}{RT} = \alpha_{\text{Si-C}} - \frac{\beta_{\text{Si-C}}}{T}$$

Since there is no data for the