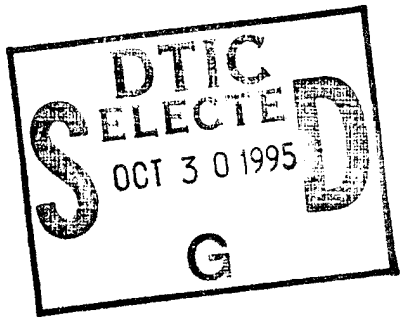
PROJECT PROGRESS REPORT V
The 2nd Year

For The Project Of

LOCALLY CONNECTED ADAPTIVE GABOR FILTER FOR REAL-TIME MOTION COMPENSATION

For the Period from January 20th of 1995
to April 20th of 1995



This Report Is Submitted to ONR

April 19th, 1995

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1. The Report

2. The Design Documentation of the High-Gain, High-Bandwidth OpAmp

The Progress Report

This report is the 5th quartly report for the project of "*locally connected adaptive Gabor filter for real-time motion compensation,*" with grant number N00014-94-1-0077, which has been in the process since October 20th of 1993 and has been conducted under the supervision of the principal investigator, Professor Hua Harry Li of Texas Tech University. As at the end of the 1st quarter of the 2nd year of this three-year project, we have been making progress towards the goals of this research as planned in the project proposal, 2(a) and (b) on page 21. At the current phase, our work is focused on the design and simulation of electronic analog circuits as basic building blocks for the VLSI implementation, as well as the testing of the first-run fabricated chips. This phase of the work is a little bit ahead of the schedule than we originally planned in the proposal. This hardware design phase concurrent with the algorithm analysis and verification provided coherent work and ensured the quality of the analog VLSI design. The work in VLSI implementation at this stage includes

1. Refine the design of the most essential building blocks, video frequency opAmp. We have developed a new high-gain and high-frequency bandwidth opAmp based on the state-of-the-art technique, super MOST technique. The new refined design provides DC gain of 110 db and GBW of 162 Mhz (for a load of 1 pf) and phase margin of 35 degree. With extensive SPICE simulations using the device model provided from MOSIS actual fabrication run, we have completed the design. The characteristics of the OpAmp to be used to build two-dimensional convolution unit is given in a research memo and was included in this report as an Appendix.
2. Benchmark testing of the fabricated 5-by-5 Gabor convolution unit. The testing consists of electrical characterization of the chips, data collection and comparison to the SPICE simulation result. In our first fabrication run (October 1994), 4 chips were manufactured. Additional 8 chips are now under fabrication through MOSIS service. Figure 1 shows one of the fabricated chip.
3. In order to fully test the chip, we also start building a test board which will digitized the image, then feed the image data to our designed chip for processing. The board is PCI bus based board and can be programed to work with 486 machine to form an integrated testing environment.

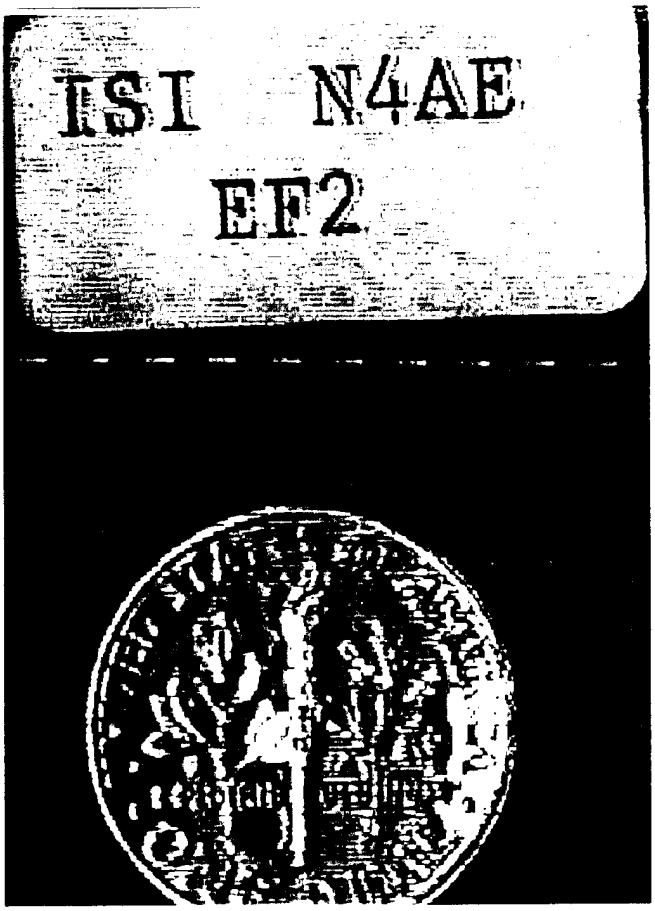

Figure 1. Top of the figure is the fabricated VLSI chip (major part), which is the implementation of 5-by-5 Gabor convolution unit, and the bottom of the figure is a U.S. dime for a reference purpose.

DESIGN OF A HIGH GAIN, HIGH FREQUENCY OPAMP

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Abstract— **The design of a higyh performance opmp with high unity gain-bandwidth (GBW), high DC gain and rail-to-rail output voltage swing is presented in this paper. The goal is to achieve a GBW of at least 100MHz, a DC gain of at least 90dB and a -5V to +5V output voltage swing corresponding to the voltage supplies VSS and VDD. In order to increase the DC gain without affecting GBW, the regulated cascode structure, super MOS, is used in the design of an opamp for video applications. PSPICE simulations confirm the design and show the gain enhancement.**

1. INTRODUCTION

Today's analog CMOS VLSI design is still a difficult process, which usually doesn't provide basic building blocks with a consistent behaviour over the whole spectrum of requirements: gain, frequency response, stability, delay and output linearity. Each time the designer had to compromise and trade in some good features in order to improve other characteristics for which the circuit was designed for. So far, analog signal processing systems have been integrated for applications not exceeding the low megahertz range, mainly due to the lack of high frequency opamps.

The task of designing an opamp with high GBW and high DC gain is not a trivial one, because these two design constraints lead to contradictory requirements. High GBW requires a single-stage topology, with short-channel devices biased at high bias currents, while high DC gain needs multi-stage configuration with long channel devices biased at low bias currents. Therefore, the designer needs to use a method which allows the decoupling of AC and DC requirements.

In the last ten years, the research done in the field of opamp design has produced two general configurations: the mirrored cascode (MC) [1] and the folded cascode (FC) [2]. A comparison [3], using the settling time as a selection criteria, leads to the conclusion that the MC structure is better for large capacitive loads, (greater than 1pF)-due to its large slew rate capabilities-, while the FC structure yields better results for small capacitive loads (smaller than 1pF). Taking all the above mentioned constraints in consideration, a hybrid complementary folded cascode (CFC) structure was proposed [3].

2. SIMPLE AMPLIFIER STAGE

High frequency behaviour, DC gain and decoupling the AC and DC constraints seriously limit the design of a simple inverting amplifier stage.

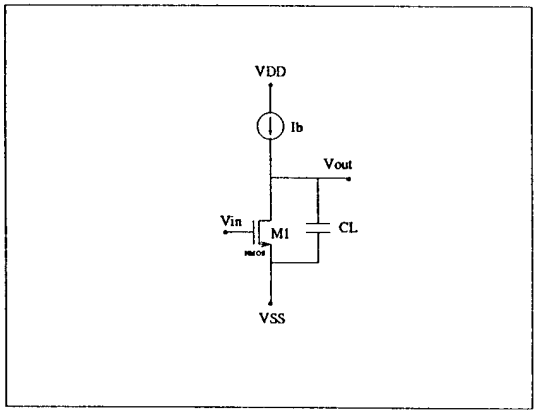

Fig. 1 Simple inverting amplifier.

First, we need to define the following small signal model parameters for a MOS transistor:

$$g_m = \sqrt{\frac{2K'W}{L}}\sqrt{\mid I_{DSQ} \mid} \tag{1}$$

$$g_{mb} = \eta g_m \tag{2}$$

$$g_{ds} \simeq \lambda \mid I_{Dsat} \mid = \frac{1}{r_{ds}} \tag{3}$$

where

$$\eta = \frac{\gamma}{2\sqrt{\phi - V_{BSQ}}} \tag{4}$$

g_m is the transconductance, g_{mb} is the bulk transconductance and g_{ds} the output conductance. K' is the saturation parameter, W and L are the width and the length of the MOS device, I_{DSQ} is the quiescent biasing drain-source current, γ is the bulk threshold, ϕ is the surface potential, λ is the channel-length modulation parameter, η is the static feedback effect parameter and V_{BSQ} is the quiescent bulk-source potential.

For the simple inverter amplifier (Figure 1), the DC gain, the output resistance and the dominant pole are given by:

$$A_v = -g_m r_{out} \tag{5}$$

$$r_{out} = r_{ds} \| r_{I_{load}} \simeq r_{ds} \tag{6}$$

and

$$\omega_{-3dB} = \frac{1}{r_{I_{load}}(C_2 + C_3)} \simeq \frac{1}{r_{out} C_{load}} \tag{7}$$

where $r_{I_{load}}$ is the output resistance of the current source used as a load, ω_{-3dB} is the dominant pole of the amplifier which causes the first roll-off of the frequency characteristic, C_2 and C_3 represent all the parasitic capacitors associated with the input and output nodes.

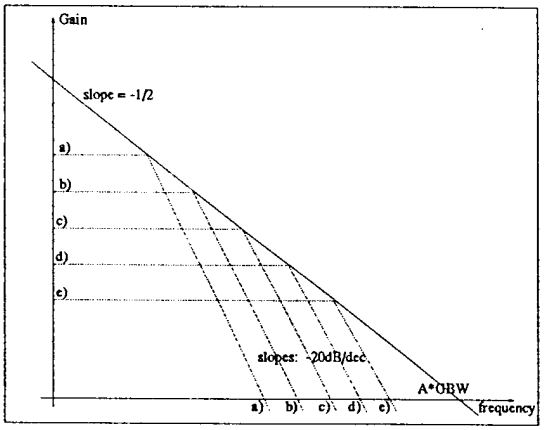

Fig. 2 Gain-bandwidth limitation.

Figure 2 shows the basic gain-bandwidth limitation [4]. These figure represents a family of transfer characteristics of a simple gain stage obtained by varying the L/V_{gs} ratio. Suppose curve c) is the transfer characteristic of a simple gain stage. Increasing the ratio L/V_{gs} increases the gain and decreases GBW, resulting in curves b) and a). Decreasing this ratio gives curves d) and e). The -3dB points of these characteristics lie on a straight line with slope -1/2. This line shows the maximum possible unity-gain bandwidth frequency. Transfer characteristics of the given stage are possible only below this line. Unless we use other techniques (cascoding), it is not possible to obtain a characteristic above this line.

The DC gain expression shows that, in order to increase its value, we need to increase the value of the output impedance. We could increase r_{out} by making the length of the input MOST larger, but this will make the transconductance smaller and therefore the DC gain will also become smaller. As stated above, this shows that these two design constraints (GBW and DC gain) lead to a contradiction. This problem can be partially solved , by using the so called cascode structure.

3. CASCODE AMPLIFIER STAGE

Increasing the output impedance of an amplifier stage without degrading its frequency behaviour can be done using the cascode structure (Figure 3).

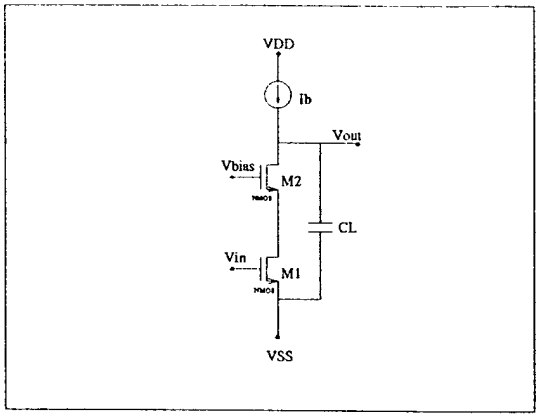

Fig. 3 Cascode amplifier.

The cascoded amplifier has a DC gain equal to the product of an effective transconductance g_{meff} and the output impedance r_{out} [4]. Transistor M2 is the cascoding device. For low frequencies, it increases the output impedance with a negligible effect on the transconductance and, for high frequencies its effect is almost nil. The effective transconductance is given by:

$$g_{meff} = \frac{\Delta I_{out}}{\Delta V_{in}} = g_{m1} \frac{g_{m2} r_{ds1} + r_{ds1}/r_{ds2}}{g_{m2} r_{ds1} + r_{ds1}/r_{ds2} + 1} \tag{8}$$

which is almost equal to g_{m1}. Therefore, the voltage gain will be:

$$A_v = g_{meff} r_{out} \tag{9}$$

The output impedance is given by:

$$r_{out} = (g_{m2} r_{ds2} + 1) r_{ds1} + r_{ds2} \approx g_{m2} r_{ds2} r_{ds1} \tag{10}$$

This roughly equals to the output resistance of the input transistor, r_{ds1}, multiplied by the gain of the cascode device, $g_{m2} r_{ds2}$. The role of the cascode transistor is to keep M1 biased at a constant voltage V_{DS1}, by shielding the drain of M1 from the variations of the output voltage by a factor equal to the gain of M2. This leads to the following DC gain:

$$A_v = g_{m1} r_{ds1} (g_{m2} r_{ds2} + 1) \tag{11}$$

We can conclude from here that the gain of the cascoded amplifier stage equals almost the square of the gain of the simple amplifier stage:

$$A_{vcascode} \approx g_{m1} r_{ds1} g_{m2} r_{ds2} \approx A_{vsimple} \tag{12}$$

Also, the GBW of the cascoded stage, given by:

$$GBW_{cascode} = \frac{g_{eff}}{C_{load}} \tag{13}$$

is approximately equal to GBW_{simple}. Anyway, we cannot increase the gain freely; there is also a constant

product between the square root of the gain and the GBW:

$$\sqrt{A_{vcascode}}GBW_{cascode} = constant \qquad (14)$$

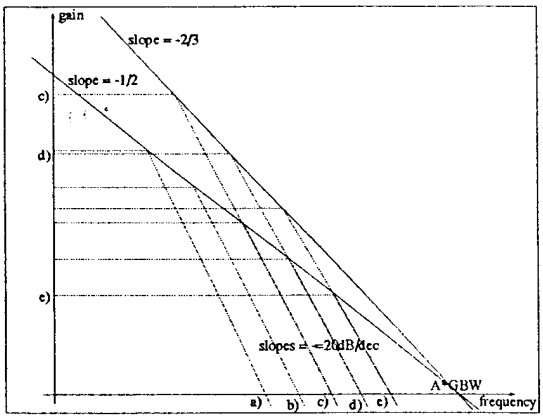

Fig. 4 Improvement of gain bandwith limitation.

The improvement of the cascoding amplifier stage can be illustrated with Figure 4. This figure represents a family of transfer characteristics of a cascode amplifier stage compared to a family of transfer characteristics of a simple amplifier stage, for different L/V_{gs} ratios. It shows that for the same unity gain frequency, we are capable of achieving a much higher gain. The -3dB line has, in this situation a steeper slope (-2/3).

As Eq. 14 shows, the gain cannot be infinitely increased and that the AC and DC requirements are still not decoupled. A technique which really achieves the desired results will be presented in the next section.

4. CASCODE AMPLIFIER STAGE WITH GAIN ENHANCEMENT

The technique which allows a single-stage amplifier to exhibit almost the same gain as a multi-stage amplifier without any speed penalties is illustrated in Figure 5.

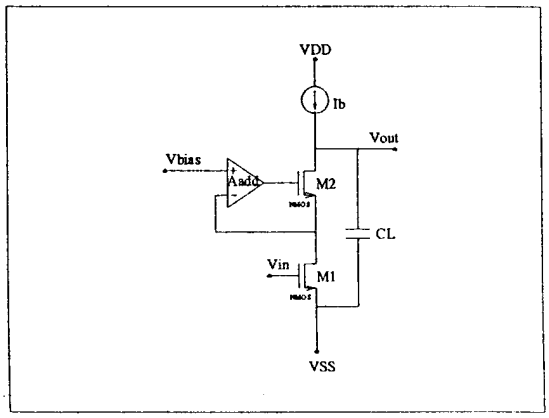

Fig. 5 Cascode amplifier with gain enhancement.

The gain boosting effect is achieved by increasing the cascoding effect of M2 with an additional gain stage, thus increasing the output impedance. Equation 9 shows that the only way to increase the DC gain without loosing the frequency characteristics is to increase the output impedance. M2 has already done that and besides, it shielded the drain of the input transistor from the output voltage swing. The additional opamp, acting as an error amplifier, reduces the feedback from the output to the drain of M1 by a factor of A_{add}, where A_{add} is the gain of the additional stage. With this new configuration, the output impedance has the expression:

$$r_{out} = [(g_{m2}r_{ds2}(A_{add}+1)+1]r_{ds1} + r_{ds2} \qquad (15)$$

and the effective transconductance:

$$g_{meff} = \frac{\Delta I_{out}}{\Delta V_{in}} = g_{m1}\frac{g_{m2}r_{ds1}(A_{add}+1)+r_{ds1}/r_{ds2}}{g_{m2}r_{ds1}(A_{add}+1)+r_{ds1}/r_{ds2}+1} \qquad (16)$$

Therefore, the gain of this circuit becomes:

$$A_{tot} = g_{m1}r_{ds1}[g_{m2}r_{ds2}(A_{add}+1)+1] \qquad (17)$$

5. THE REGULATED CASCODE CIRCUIT

A great inconvenience associated with the previously described circuit is the complexity of the design and layout. Also, a disadvantage of cascoded amplifiers is the big number of biasing voltages, which requires long wires across the chip. These long wires consume a considerable amount of space and the cross-talk between them results in instability. That is why the regulated cascode circuit comes as a very good alternative to these gain enhancement methods. This circuit has the same behaviour as a regular MOS transistor, but has a much higher output impedance, a lower feedback capacitance and an intrinsic gain of more than 90dB. The configuration is depicted in Figure 6.

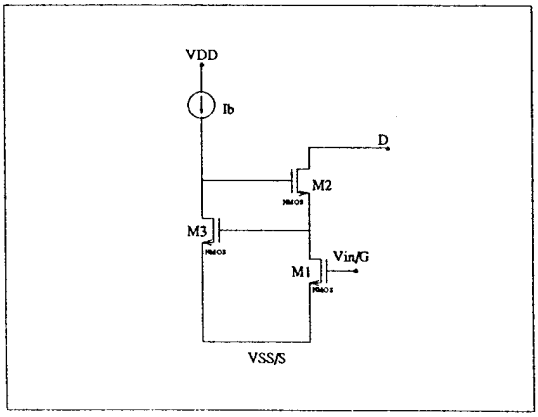

Fig. 6 Regulated cascode circuit.

Transistor M1 converts the input voltage into a drain current which flows into transistor M2. In order to eliminate the effect of channel-length modulation of M1, the drain-source voltage across this device must be kept

very stable. This is done by a feedback loop consisting of an amplifier (M3 and Ib) and M2 as a source follower. This feedback loop keeps the drain-source voltage across M1 regulated to a constant value even when M2 becomes biased into its ohmic region, which extends the minimum saturation voltage of the regulated cascode circuit. The output impedance of this circuit is given by:

$$r_{out} = \frac{g_{m2} g_{m3} r_{ds1} r_{ds2}}{g_{o3} + g_{oi}} \qquad (18)$$

where g_{o3} is the output conductance of transistor M3 and g_{oi} is the output conductance of the current source I_b. This output impedance is greater by a factor of $\frac{g_{m3}}{g_{o3}+g_{oi}}$ (which is around 100) than the output impedance of an optimally biased cascode amplifier. This value represents the loop gain of the regulating amplifier (M3 and I_b). The figures from Appendix A offers a comparison between the output characteristics of a simple N-type and P-type transistors and the output characteristics of a regulated N-type and P-type cascode circuits (called super MOS [5]) with the same W/L ratio for different gate voltages.

These figures demonstrate that the super MOST has a much higher output impedance (given by the inverse of the slope of the saturated region) than a simple device with the same W/L ratio. Therefore it can be succesfully used in more complicated circuits, like current mirrors, amplifier stages and opamps, where a device with high gain, high output impedance and small feedback capacitance is needed. In the next section the improvement of the DC gain of an opamp is illustrated, when its output stage transistors are replaced with super MOSTs.

6. OPAMP DC GAIN IMPROVEMENT

First, a complementary folded cascode (CFC) [3] is designed and simulated. This circuit employs regular N-type and P-type transistors. The circuit is shown in Figure 7.

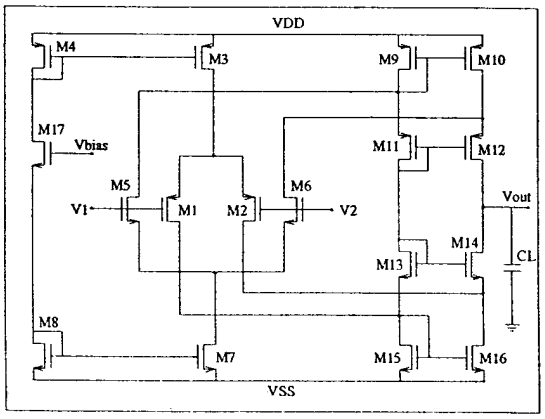

Fig. 7 Complementary folded cascode opamp.

A complementary input stage was chosen because it offers a rail-to-rail output voltage swing. The transfer characteristic and the frequency/phase plots of this circuit are included in the Appendix B. Replacing the transistors in the folded cascode stage by super MOS devices improves the DC gain with 50 dB with very little influence on GBW. The transfer characteristic and the frequency/phase plots of this circuit are also included in Appendix B. All simulations were performed for a 20 pF load. This clearly demonstrates that the super MOS device succesfully replaced the regular MOS transistor.The source files for the PSPICE simulations are included in Appendix C. The characteristics of the two opamps-with and without gain enhancement-are summarized in the following table:

	Opamp without gain enhancement	Opamp with gain enhancement
Technology	2μ m n-well	2μ m n-well
Supply voltage	$\pm$5V	$\pm$5V
Load capacitor	20.0 pF	20.0 pF
Bias current	322μA	322μA
Rout	413.2 kΩ	137.5 MΩ
DC gain	60 dB	110.4 dB
GBW	19.4 MHz	17.2 MHz
Phase margin	87°	75.5°
Power dissip.	21 mW	19.4 mW
Slew rate -	37.8 V/μs	51.3 V/μs
Slew rate +	38.2 V/μs	47.8 V/μs

7. CONCLUSIONS

These simulations show that applying the gain enhancement principle using super MOS devices to replace the ordinary CMOS devices in the circuit points where high impedance is required, considerably enhances the DC gain of the opamp.

So far, this technique was only applied to the complementary folded cascode opamp, resulting in a DC gain of 110 dB, a GBW of 162 MHz (for a load of 1 pF) and a phase margin of 35° (see Appendix D). Next stage in our reserch will be to implement this idea in the complementary mirrored cascode circuit shown in Figure 8.

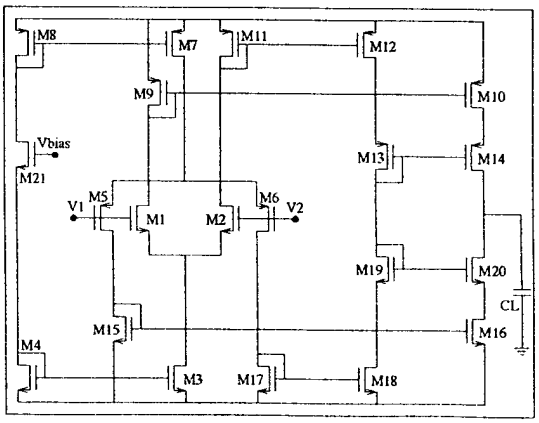

Fig. 8 Complementary mirrored cascode opamp.

This circuit is capable of higher slew rate than the complementary folded cascode opamp and, therefore able to drive bigger capacitive loads. The DC gain of this circuit is given by:

$$A_v = \frac{v_o}{v_i} = g_{m1} a_i r_{out} \tag{19}$$

where g_{m1} is the transconductance of the first stage (M1, M2, M5, M6), a_i is the current gain in the current gain stage (M9-M12 and M15-M18), and r_{out} is the total output impedance. The dominant pole is located at:

$$\omega_1 = \frac{1}{r_{out} C_L} \tag{20}$$

and the GBW is placed at:

$$\omega_{GBW} = \frac{g_{m1} a_i}{C_L} \tag{21}$$

where C_L is the load capacitor.

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N-TYPE AND P-TYPE SUPER MOSTs

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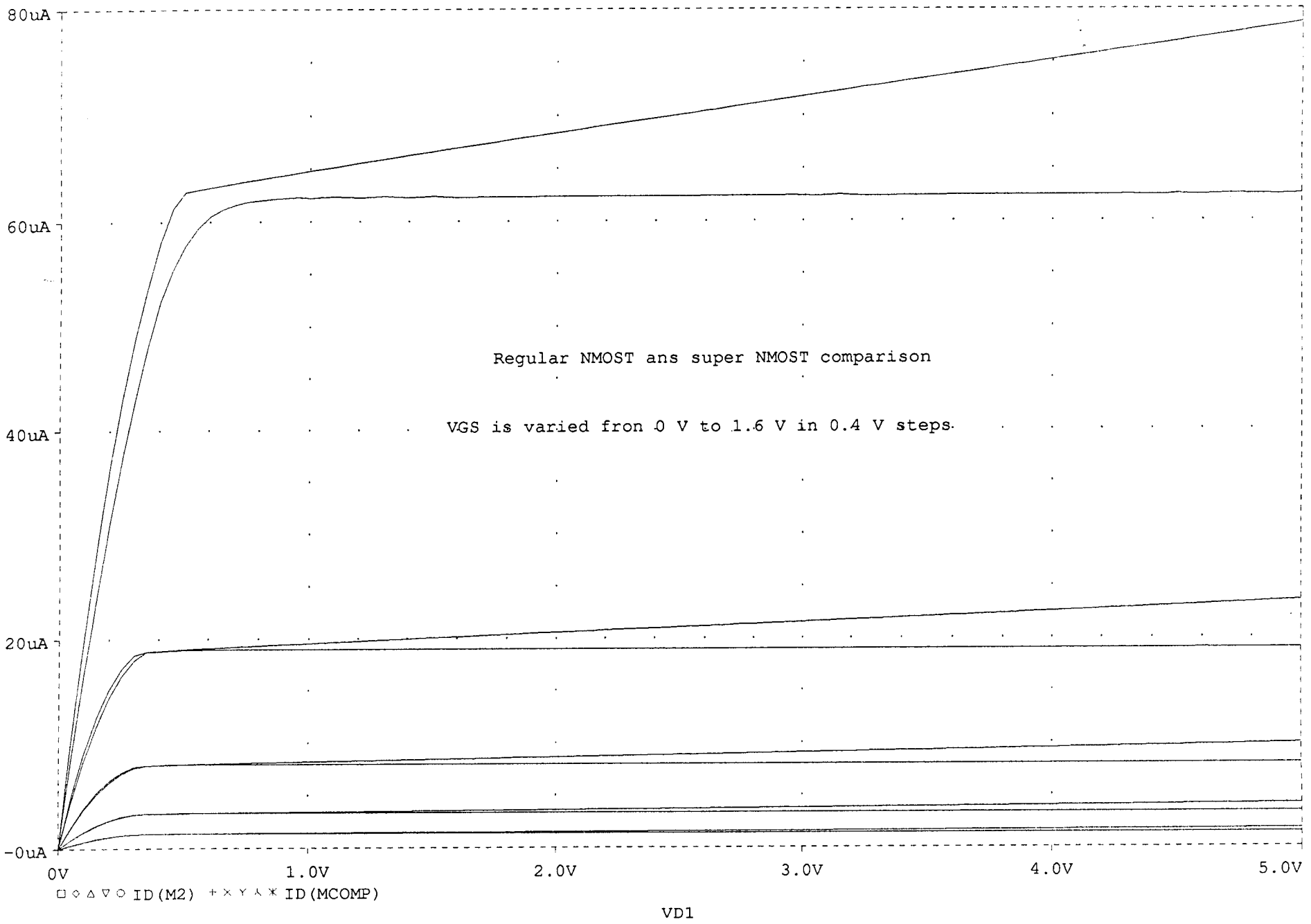

N-TYPE AND P-TYPE SUPER MOSTs

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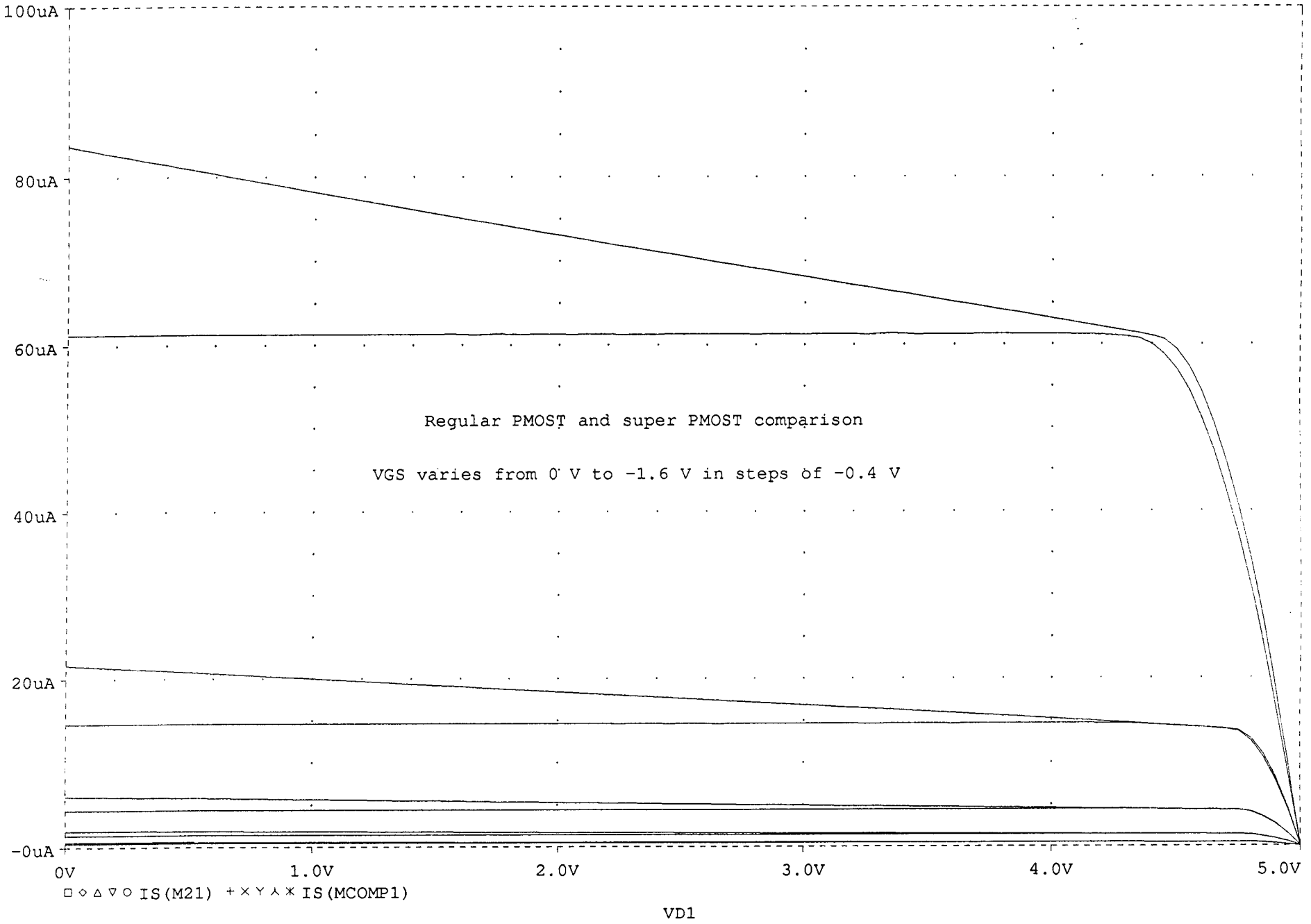

APPENDIX B

*COMPLEMENTARY FOLDED CASCODE AMPLIFIER

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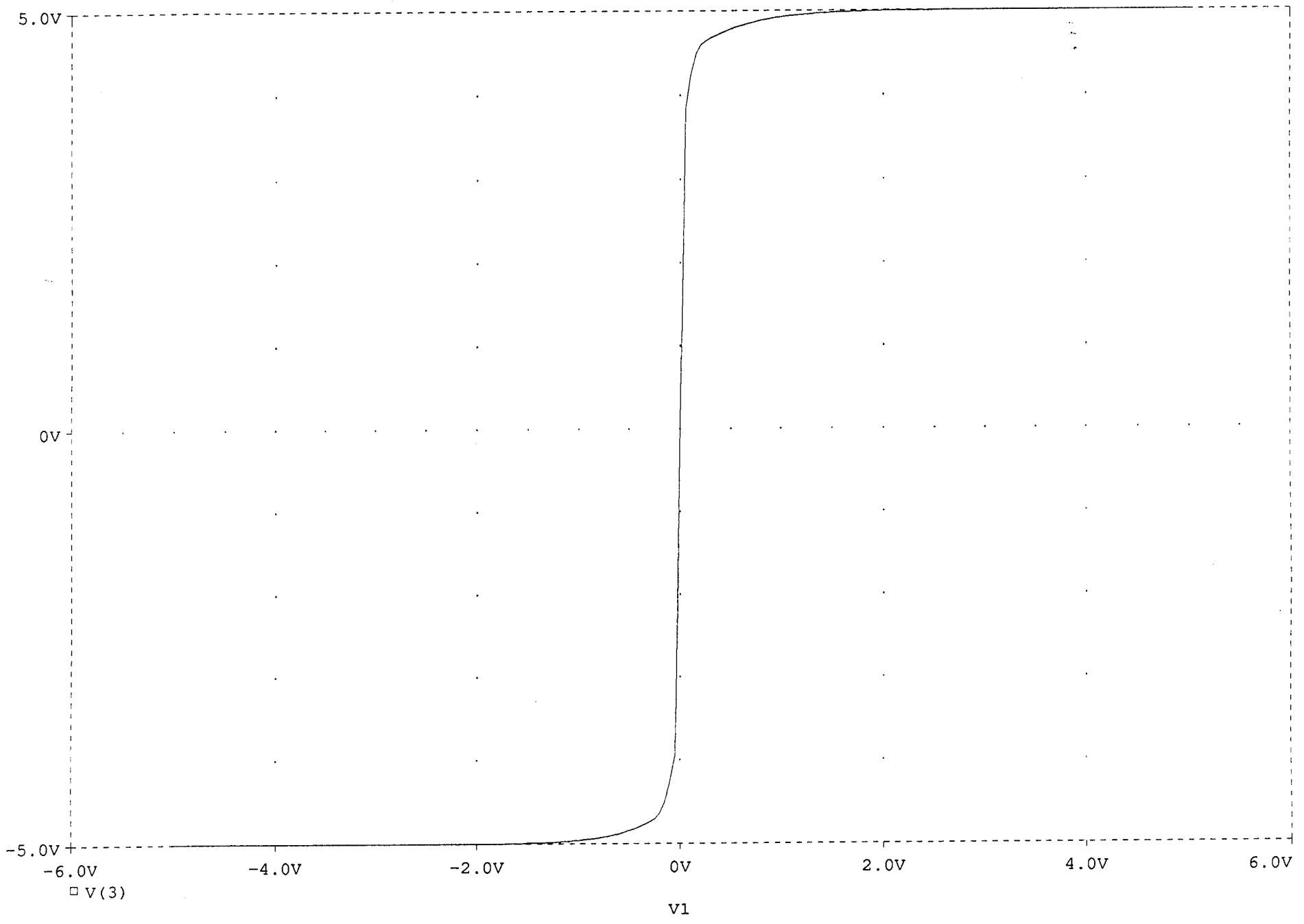

*COMPLEMENTARY FOLDED CASCODE AMPLIFIER

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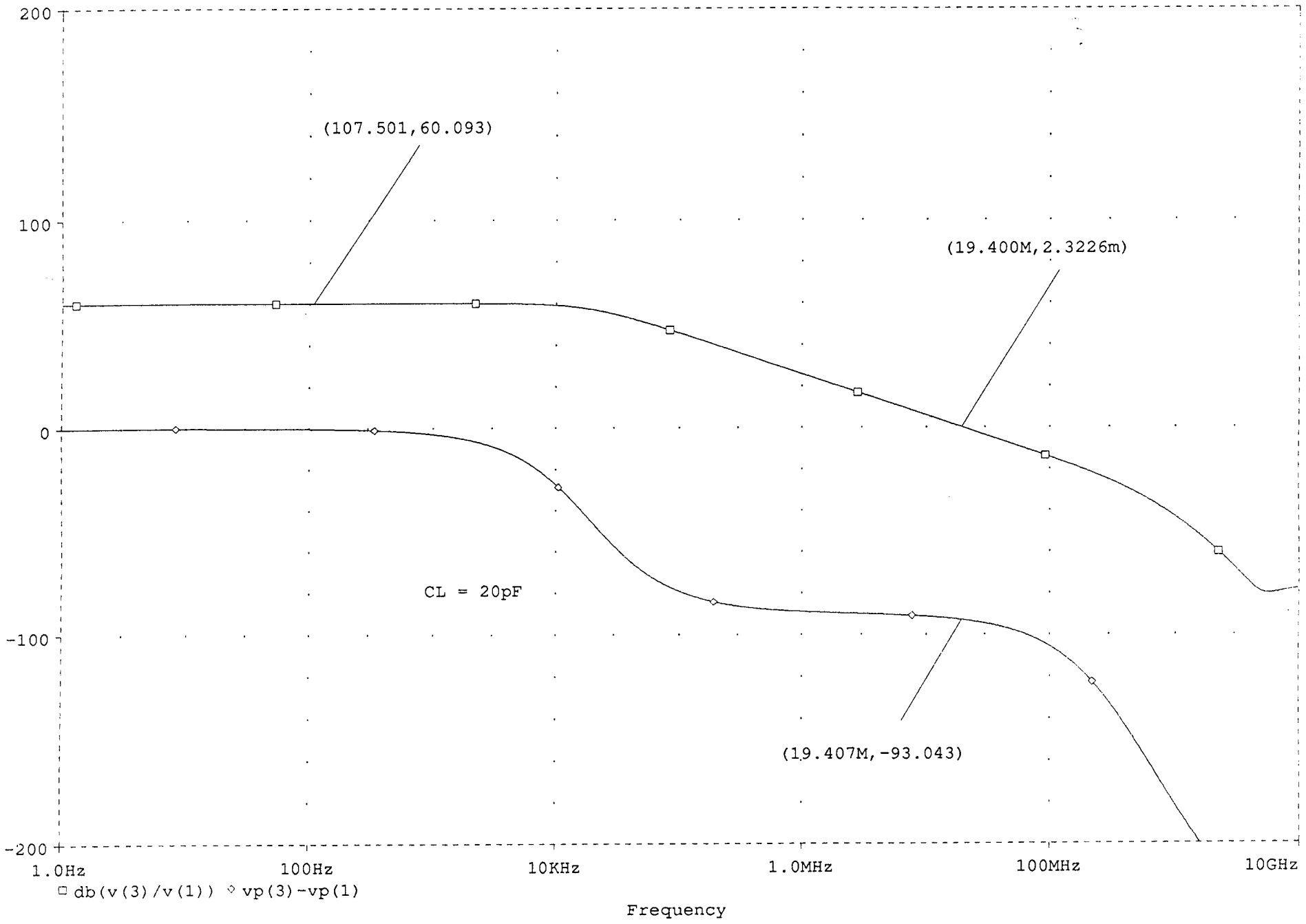

*COMPLEMENTARY FOLDED CASCODE AMPLIFIER WITH GAIN ENHANCEMENT

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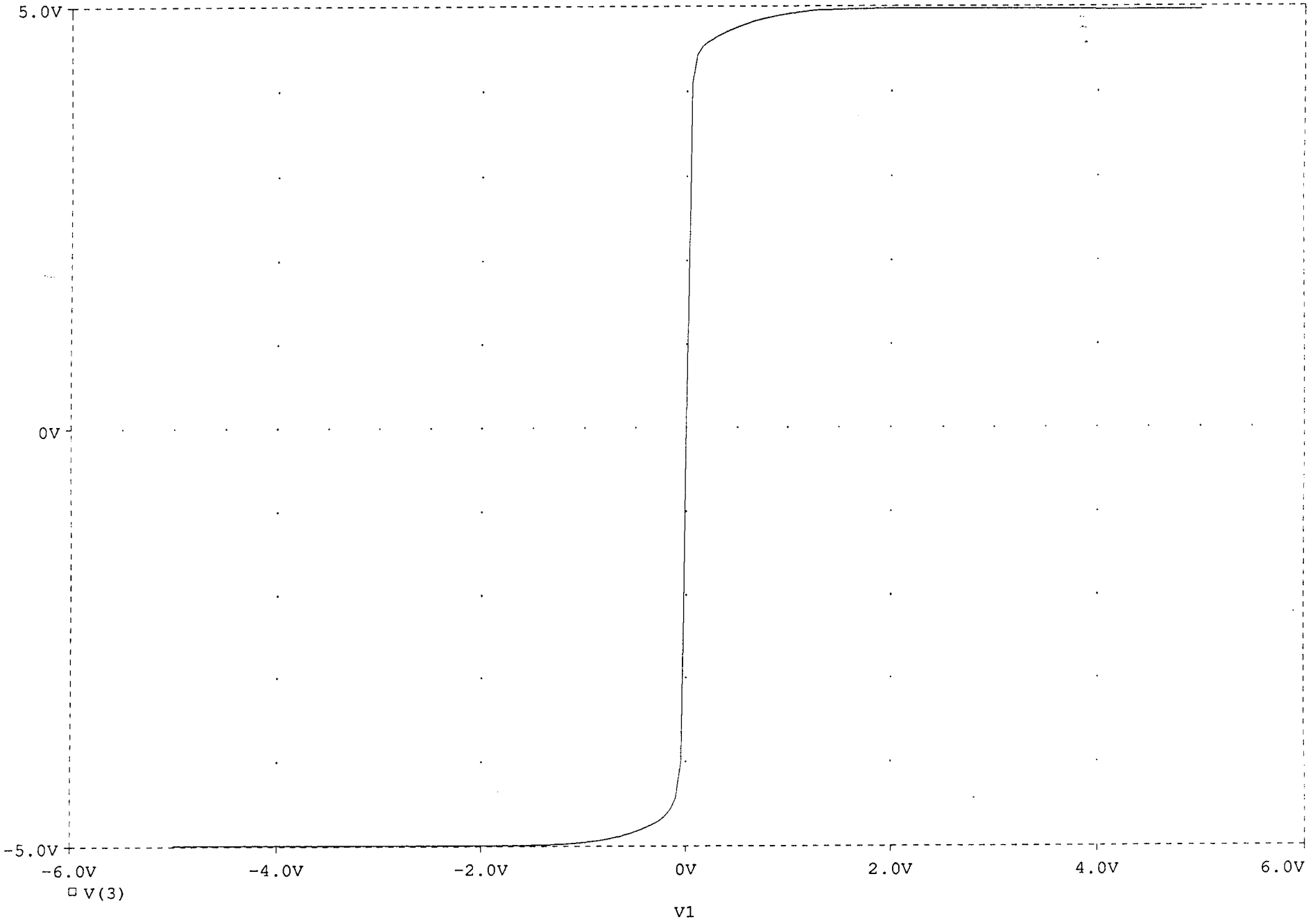

*COMPLEMENTARY FOLDED CASCODE AMPLIFIER WITH GAIN ENHANCEMENT

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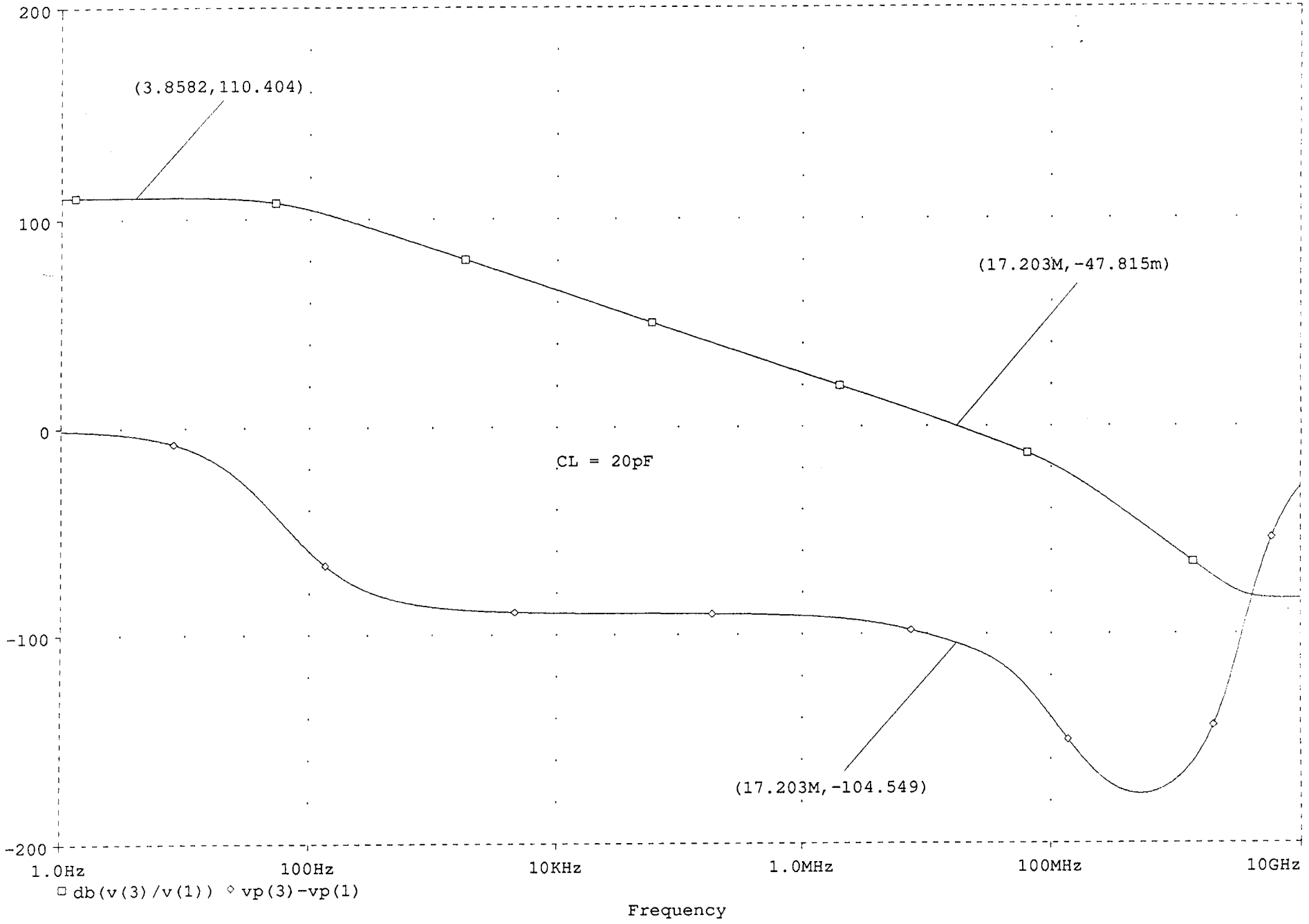


APPENDIX C

```
*COMPLEMENTARY FOLDED CASCODE AMPLIFIER

.OPTION NOECHO NOMOD

.include model.h

*P differential stage and bias

M1 14 1 6 4 P W=300U L=2U
M2 13 2 6 4 P W=300U L=2U
M3 6 8 4 4 P W=49U L=2U
M4 8 8 4 4 P W=24U L=2U

*N differential stage and bias

M5 10 1 7 5 N W=80U L=2U
M6 11 2 7 5 N W=80U L=2U
M7 7 9 5 5 N W=16U L=2U
M8 9 9 5 5 N W=8U L=2U

*P-type stacked current mirror

M9 10 10 4 4 P W=39U L=2U
M10 11 10 4 4 P W=39U L=2U
M11 12 12 10 4 P W=39U L=2U
M12 3 12 11 4 P W=39U L=2U

*N-type stacked current mirror

M13 12 12 14 5 N W=14U L=2U
M14 3 12 13 5 N W=14U L=2U
M15 14 14 5 5 N W=14U L=2U
M16 13 14 5 5 N W=14U L=2U

*transistor used as current source

M17 8 15 9 5 N W=4U L=2U
*RF 2 3 1P

*load

*RL 3 0 {RL}
CL 3 0 {CL}

**** supplies ****
```

```
VDD 4 0 DC 5V
VSS 5 0 DC -5V
Vbias 15 0 {VB}

**** voltages ****

*V1 1 0 AC 1MV PWL(0NS .1V 0.00001NS -.1V 100NS -.1V 100.00001NS .1V
*+200NS .1V 200.00001NS -.1V 300NS -.1V)
V1 1 0 AC 1V SIN(0V 1MV 500K)
V2 2 0 dc 0v ac 0v

.PARAM CL=1P
.PARAM RL=5MEG
.PARAM VB=2.75V

*ANALYSIS

.STEP PARAM CL 1P 16P 15P
.DC V1 -5V 5V .05V
.WATCH DC V(3)
.WATCH TRAN V(3)
.TRAN .1PS 300NS
.WATCH AC V(3)
.AC DEC 100 1 1e10
.TF V(3) V1
.PROBE V(3) V(1) V(2)
.OP
.END
```

```
*COMPLEMENTARY FOLDED CASCODE AMPLIFIER WITH GAIN
ENHANCEMENT*

.OPTION NOECHO NOMOD

*DEFINITION OF MODELS

*N4AE  SPICE LEVEL 2 PARAMETERS

.MODEL N NMOS LEVEL=2 PHI=0.600000 TOX=4.3500E-08 XJ=0.200000U TPG=1
+ VTO=0.8756 DELTA=8.5650E+00 LD=2.3950E-07 KP=4.5494E-05
+ UO=573.1 UEXP=1.5920E-01 UCRIT=5.9160E+04 RSH=1.0310E+01
+ GAMMA=0.4179 NSUB=3.3160E+15 NFS=8.1800E+12 VMAX=6.0280E+04
+ LAMBDA=2.9330E-02 CGDO=2.8518E-10 CGSO=2.8518E-10
+ CGBO=4.0921E-10 CJ=1.0375E-04 MJ=0.6604 CJSW=2.1694E-10
+ MJSW=0.178543 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.0460E-07
.MODEL P PMOS LEVEL=2 PHI=0.600000 TOX=4.3500E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8889 DELTA=4.8720E+00 LD=2.9230E-07 KP=1.5035E-05
+ UO=189.4 UEXP=2.7910E-01 UCRIT=9.5670E+04 RSH=1.8180E+01
+ GAMMA=0.7327 NSUB=1.0190E+16 NFS=6.1500E+12 VMAX=9.9990E+05
+ LAMBDA=4.2290E-02 CGDO=3.4805E-10 CGSO=3.4805E-10
+ CGBO=4.0305E-10 CJ=3.2456E-04 MJ=0.6044 CJSW=2.5430E-10
+ MJSW=0.244194 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -3.6560E-07
**********************************************************************

*P differential stage and bias

M1 14 1 6 4 P W=300U L=2U
M2 13 2 6 4 P W=300U L=2U
M3 6 8 4 4 P W=49U L=2U
M4 8 8 4 4 P W=24U L=2U

*N differential stage and bias

M5 10 1 7 5 N W=80U L=2U
M6 11 2 7 5 N W=80U L=2U
M7 7 9 5 5 N W=16U L=2U
M8 9 9 5 5 N W=8U L=2U

*P-type superMOS current mirror
```

```
X9 10 10 4 PsuperMOS
X10 11 10 4 PsuperMOS
X11 12 12 10 PsuperMOS
X12 3 12 11 PsuperMOS

*N-type stacked current mirror

X13 12 12 14 NsuperMOS
X14 3 12 13 NsuperMOS
X15 14 14 5 NsuperMOS
X16 13 14 5 NsuperMOS

**********************************************************
* N superMOS

.subckt NsuperMOS 1 2 3
*              D G S

M1 4 2 3 3 N W={WN} L=2U
M2 1 5 4 4 N W={WN} L=2U
M3 5 4 3 3 N W=6U L=2U
M4 5 6 7 7 P W=7U L=2U

V7 7 0 5V
V8 8 0 -5V
Vbias 6 0 4V

.ends
**************************************************************

* P superMOS

.subckt PsuperMOS 8 9 10
*              D G  S

M11 11 9 10 10 P W={WP} L=2U
M21 8 12 11 11 P W={WP} L=2U
M31 12 11 10 10 P W=26U L=2U
M41 12 14 13 13 N W=3U L=2U

V13 13 0 -5V
V15 15 0 5V
Vbias 14 0 -4V

.ends
```

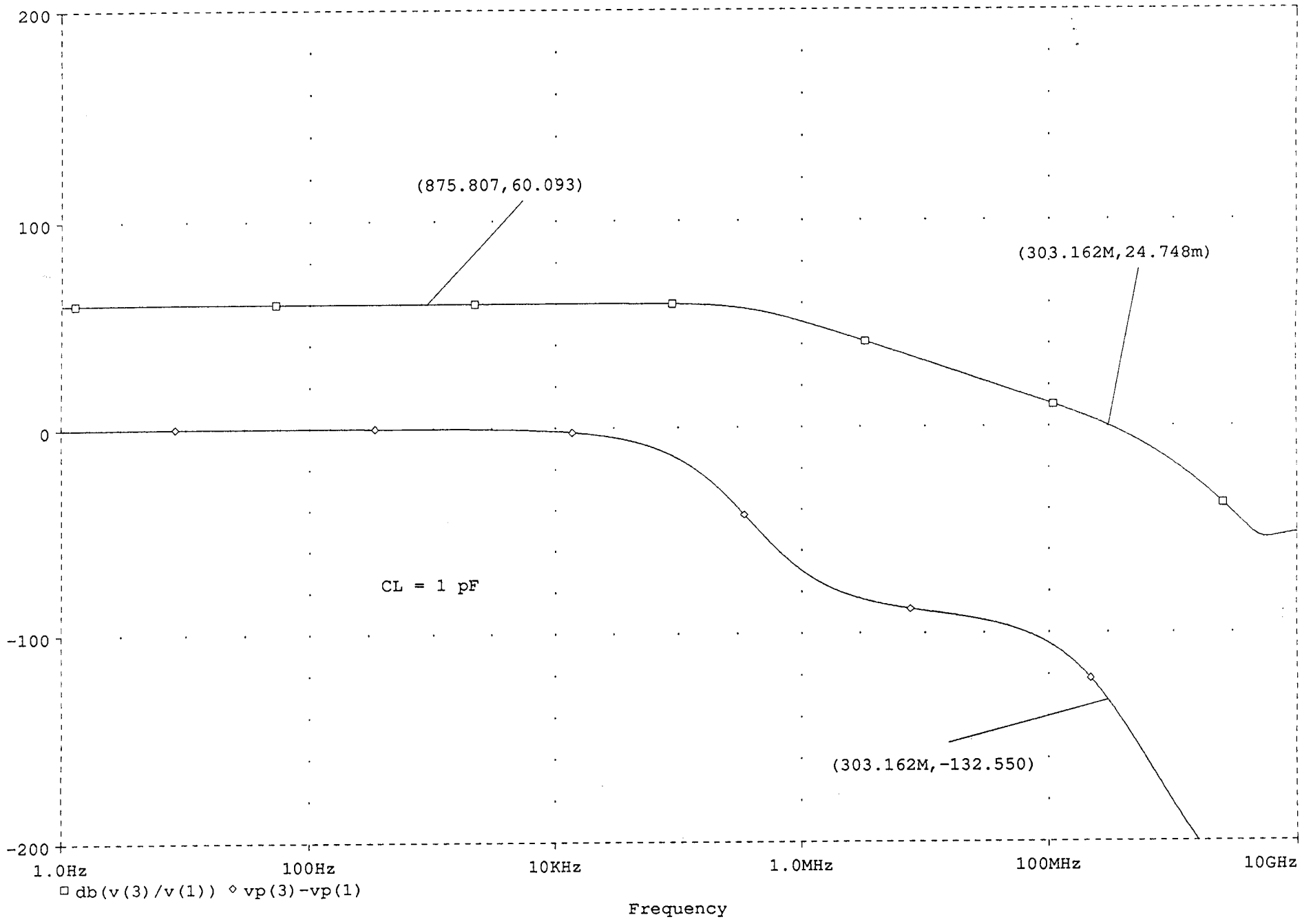
```
**************************************************************


M17 8 15 9 5 N W=4U L=2U
*RF 2 3 1P

*load

*RL 3 0 {RL}
CL 3 0 {CL}

**** supplies ****

VDD 4 0 DC 5V
VSS 5 0 DC -5V
Vbias 15 0 {VB}


**** voltages ****

*V- 1 0 ac 1v PWL(0NS 0V 1US 0V 1.00001US 1mV 10.1US 1mV 10.10001US 0V
30US 0V)
V- 1 0 AC .1V SIN(0V 1V 10K)
*V- 1 0 AC 1V PWL(0NS {VP} 0.00001NS {-VP} 200NS {-VP} 200.00001NS {VP}
*+400NS {VP} 400.00001NS {-VP} 600NS {-VP})
*V- 1 0 AC 1MV PULSE(0V -1MV 0US 1FS 1FS 10US 20US)
*V+ 1 0 dc 0v ac 0v
V+ 2 0 dc 0V ac 0v


.PARAM CL=1P
.PARAM RL=100MEG
.PARAM VB=2.75V
.PARAM VP=1V
.PARAM WN=14U
.PARAM WP=39U

*ANALYSIS

*.STEP PARAM VP .5 1 .25
*.DC V+ -5V 5V .01V
.WATCH DC V(3)
.TRAN .1PS 600NS
.WATCH TRAN V(3)
.AC DEC 100 1 1e10
```

APPENDIX D

*COMPLEMENTARY FOLDED CASCODE AMPLIFIER

Date/Time run: 04/21/95 01:01:06

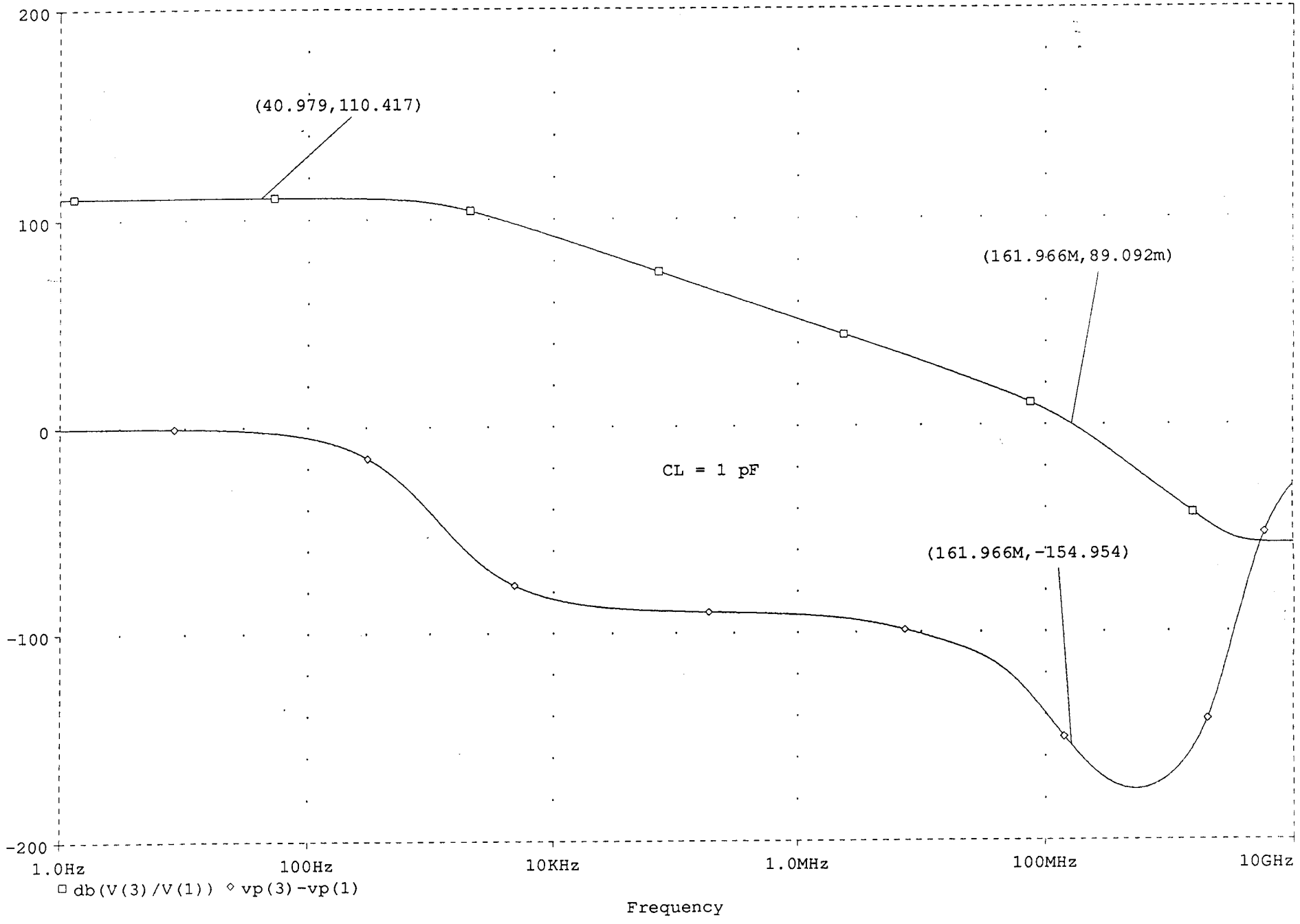
Temperature: 27.0



*COMPLEMENTARY FOLDED CASCODE AMPLIFIER WITH GAIN ENHANCEMENT

Date/Time run: 04/21/95 00:57:06

Temperature: 27.0



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CORPORATE PROGRAMS DIVISION
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800 NORTH QUINCY STREET
ARLINGTON, VA 22217-5660

1995 1027 050

1. Reference: DoD Directive 5230.24, Distribution Statements on Technical Documents, 18 Mar 87.

2. The Defense Technical Information Center received the enclosed report (referenced below) which is not marked in accordance with the above reference.

PROGRESS REPORT/ 20 JAN-20 APR 95
N00014-94-1-0077
TITLE: LOCALLY CONNECTED
ADAPTIVE GABOR FILTER FOR REAL-
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3. We request the appropriate distribution statement be assigned and the report returned to DTIC within 5 working days.

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A

(Statement)

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DEPUTY DIRECTOR
CORPORATE PROGRAMS OFFICE

(Signature & Typed Name) (Assigning Office)

15 SEP 1995

(Date Statement Assigned)