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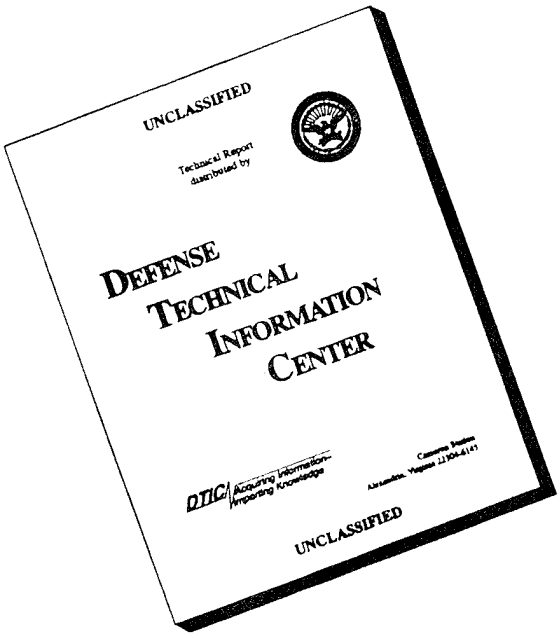

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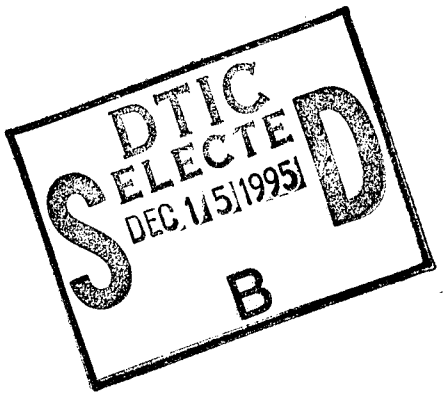

ADVANCES IN ELECTRONIC CIRCUIT PACKAGING

Volume 4

Proceedings of the Fourth International Electronic Circuit Packaging Symposium sponsored by the University of Colorado, EDN (Electrical Design News), and Design News, held at Boulder, Colorado, August 14-16, 1963

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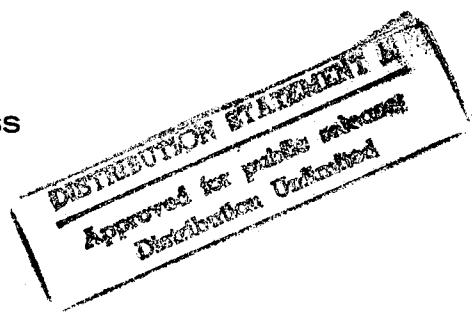

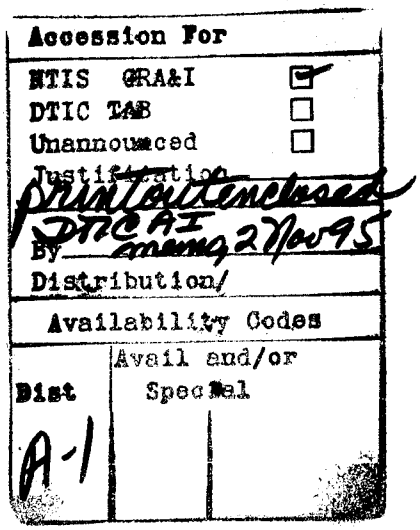

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Foreword

Volume 4 of *Advances in Electronic Circuit Packaging* is more than just a report of what occurred at the Fourth International Electronic Circuit Packaging Symposium. It is also a history of a key industry in which definite trends are already evident.

The twenty-eight technical papers contained in this volume are the logical continuation of all the papers that have gone before them in previous sessions of the Symposium. This is so for a number of reasons – first, the nature of the Symposium's call for papers; second, the methods used in the selection of papers; and third, the techniques employed in sampling Symposium participants' opinions on the value of papers presented.

In its call for papers, the Symposium has made the most general possible appeal to all circuit packaging designers and engineers to submit paper outlines for consideration. In its selection of papers, the Symposium since its 1961 sessions has relied on the services of a Program Selection Committee elected by attendees from every segment of the circuit packaging field.

Finally, following each year's session, all participants are asked to evaluate the papers they have heard. The Program Selection Committee utilizes these evaluations in establishing ground rules for the selection of the following year's presentations. Thus the papers submitted in outline, and those selected for presentation, represent not only the "state of the packaging art" at that particular time, but also the "state of the mind" of circuit packaging design leaders.

Thus, with the completion of the Fourth Symposium, it has become possible to evaluate some of the "trends" in research and development which have established themselves in electronic circuit packaging in the years from 1960 through 1963. For this purpose, it is helpful to tabulate the papers presented in each of the four years. It is then a simple matter to indicate certain pertinent trends.

In the table below, the papers presented at all four Symposium sessions are classified and enumerated under twelve separate headings. There is bound to be some overlap of areas covered by even a single paper, but classification by the Program Selection Committee has been made as closely as possible within a category which reflects the major area of coverage in each case. Though four Symposia do not constitute a large body of historical data, some inferences regarding present trends can be made.

Category	1960	1961	1962	1963
Automation	–	2	1	–
Case Histories	7	3	3	5
Display/Control	–	1	3	–
Environment	1	2	1	3
Evaluation	3	1	–	–
Interconnections	–	1	2	3
Materials/Components	3	5	2	1
Methods	4	3	5	7
Microelectronics	3	2	6	5
Standards	1	–	–	2
Systems	–	2	1	–
Thermal Problems	2	2	3	2
Totals	24	24	27	28

Note first the numbers of categories represented at successive sessions. There were eight categories in 1960, eleven in 1961, ten in 1962, and eight again in 1963. Next, review the dominant categories at each session: In 1960, Case Histories with seven papers, followed by Methods with four; in 1961, Materials/Components with five papers, followed by Case Histories and Methods with three each; in 1962, Microelectronics with six papers, followed by Methods with five; and in 1963, Methods with seven papers, followed by Case Histories and Microelectronics with five each.

Materials/Components has declined during the four-year period while Methods has increased. Microelectronics has grown in interest along with Microcircuits. Interconnections has had a slight but steady increase. Thermal Problems has remained essentially stable.

Balancing the declining interest in Materials/Components against the growing interest in Methods indicates that circuit packaging has found its "bricks and mortar" and is now concentrating on learning how to put them together for the best results. The growing interest in Interconnections seems to bear out this inference.

The revival of interest in Standards, which showed up with two papers in 1963, after a total absence for two years, may permit the inference that circuit packaging has reached a stage of development where fewer and fewer special or exotic materials and components are required. This is closely related to the declining interest in Materials/Components and the growing interest in Methods. If the Materials/Components area really has become stabilized for a time, surely the development of Standards goes hand in hand with the development of Methods.

The sustained interest in Case Histories emphasizes the generally felt need for the exchange of information in circuit packaging. Solutions to other problems may apply directly to our own. Certainly this thought has been expressed many times at each Symposium.

The comparisons made and inferences drawn here indicate a more organized progress in the still very exciting field of electronic circuit packaging. The Proceedings of the Symposium will continue to plot the magnitudes and directions of its advance.

Michael A. Marrese, Director
Idea Exchange Programs
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Contents

DONALD H. MCHUGH
The B-Module 1

TAICHIRO ATARASHI
Interim Packaging Concept for Frequency Division Multiplex Carrier Telephone Equipment 12

C. F. MIDDLETON
The Application of Welded Micrologic Modules and Wire Wrap Techniques to Ground Support Equipment 25

J. MOORE, M. BERBERIAN, AND F. FEIGIN
Mechanical Design and Integration of a Microelectronic Tape Control Unit . . 31

R. C. FRANK AND R. E. KALFAYAN
Interconnecting Complex Miniature Electronic Systems 48

KENNETH E. HARRIS
Electronic Packaging Design for the OAO Primary Processor and Data Storage Equipment 58

MAX CALLEN AND PAUL MAYO
Honeywell Electronic Packaging for Apollo 100

J. J. OKADA
System Packaging Design of a Digital Flight Control Computer 107

JOHN R. WOODS
Design and Construction of a Polaris Timer to Space-Available Configuration . . 135

GORDON G. MESSICK
Advanced Spacecraft Command Receiver Design 142

KENNETH W. PLUNKETT
Electronic Module Connectors 154

W. MCMORRAN, D. GRASSI, AND B. EDGERTON
Packaging Flyable Welded Miniaturized Computer Electronics 183

M. E. ECKER, H. R. KAUPP, AND D. P. SCHNORR
Separable Multicontact Connectors for High-Speed Computer Circuits . . . 198

GEORGE MESSNER
Multilayer Printed Circuits 210

ROBERT J. GERLACH
The Role of Standards in Electronic Packaging 225

R. W. BERRY, E. H. MAYER, E. E. MULLER, H. J. SCAGNELLI, AND K. E. STIEFEL
Thin-Film Logic Units 231

D. J. GARIBOTTI AND W. V. LANE
The Enhanced Micromodule: A Disciplined Approach to Microcircuit Integration 250

H. G. STECH
Packaging a Thin-Film High-Speed Counter 276

GLEN R. MADLAND
A New Flat Package for Monolithic Integrated Circuits 288

MILTON I. ROSS
Encapsulation of Electrical Components by Transfer Molding vs. Precision Formed Encapsulation Shells 294

E. B. SMITH
Design for Space Applications 302

BOB G. BENDER AND ROY W. DREYER
Recent Developments in Swiss Cheese Microcircuitry 318

H. F. SAWYER
3-D Welded Module Design and Manufacturing Control Parameters 325

Handbook of 3-D Welded Mobile Module Design and Manufacturing Control Parameters 347

F. R. SCHOLLHAMMER
The Encapsulation of Electronic Components by Electron Beam Welding . . 381

M. M. FULK AND K. S. HORR
Sublimation of Materials Problem in Electronic Packaging for Spacecraft . . 396

C. S. LANKTON
Thermal Characteristics of Electronic Module Design 410

PAUL F. ANDRUS
Some Practical Approaches to Thermal Problems in Airborn and Missileborne Electronics 422

DON E. LONGMIRE
Packaging and Magnetic Field Interference 438

DISCUSSIONS 445

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The B-Module

DONALD H. MCHUGH
Burroughs Corporation, Military Electronic Computer Division, Detroit, Michigan

This paper illustrates a new concept in welded circuit module construction. The B-Module has been specifically designed to provide for manual fabrication in small quantities at moderate cost, or for continuous, automated, mass production in large quantities at low cost. The concept is adaptable to all sizes and types of components, including integrated circuit subassemblies. Packing densities of the order of 80 components per cubic inch are practicable, depending on component sizes, using "off the shelf" components. The design results in a module which has high reliability, meets military specifications, provides high component density, and permits automated fabrication.

INTRODUCTION

MOST OF THE welded cordwood-type modules presently in use require several intricate hand-assembly operations. These designs are adequate when the production quantities involved are small, but the solution to large-quantity, continuous high-rate production requirements has long been a problem. The normal procedure has been to institute brute-force techniques requiring added manpower, welding equipment, facilities, and space, to say nothing of costly training programs. It is therefore desirable that a module design lend itself to continuous automated processes and still be practical to fabricate on a manual basis. This paper illustrates an approach, herein referred to as the B-Module, which meets these goals and also achieves a number of additional advantages. The design concept is adaptable to any circuit configuration and all sizes and types of components, including integrated circuit subassemblies. Packing densities in the order of 80 components per cubic inch are practical, dependent on component sizes, using standard "off the shelf" components.

B-MODULE DESCRIPTION

The B-Module utilizes stamped or etched parts to replace individual round or ribbon wires for circuit interconnections. Basically, it consists of a two-sided metal "basket" running longitudinally through the center of the module in which the components are inserted and the leads welded. The basket is designed to provide the required interconnections within the module. The following paragraphs contain a detailed description.

Horizontal Wiring Grid

The horizontal wiring grid is a thin, flat metal strip, which is stamped or etched into six equally spaced, parallel webs of material as indicated in Fig. 1. This grid is a detail part of the basket subassembly and forms a portion of the component interconnecting wiring. The fixture holes, located at each end, provide an accurate means of alignment during subsequent assembly operations.

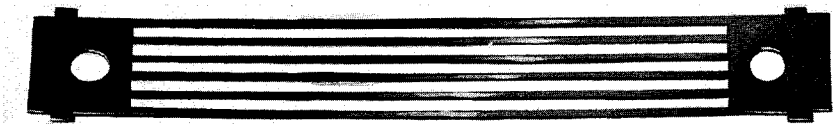


Fig. 1. Horizontal wiring grid.

Vertical Wiring Grid

The vertical wiring grid, like the horizontal grid, is a thin, flat metal strip, which is stamped or etched to form the grid pattern indicated by Fig. 2. The alternating length tabs projecting beyond the body of the grid are later formed to provide for component mounting. This grid is also a detail part of the basket subassembly and provides an additional portion of the component interconnecting wiring. Fixture holes are utilized as in the horizontal grid.

Insulator

A thin sheet of dielectric material is utilized as an insulator in the B-Module assembly. This insulator has small punched holes located to coincide with the intersection points of webs of the horizontal and vertical grids, where required by the circuit design. Fixture holes for locations are again used as illustrated in Fig. 3.

Basket Subassembly

The insulator is sandwiched between the vertical and horizontal grids, using the fixture holes for accurate alignment. The ribbons of the horizontal and vertical grids which intersect coincidental to the holes in the insulator are resistance welded at the intersection to form the subassembly. The welds, which pass through the holes in the insulator, are used to both mechanically and electrically interconnect the vertical and horizontal grids, where required by the circuit design.

After the welding has been completed, the next step is to program the subassembly into a circuit pattern. To accomplish this, the grids are punched to break the continuous metal webs and form the circuit design pattern required for that particular module.

The tabs, which project from the vertical grid, are formed to two levels to provide seats for the component leads. The formed basket subassembly provides approximately half the circuitry required for a given module. The other half of the circuitry is obtained by another basket subassembly identical to the first one, except for the programming of the weld and punch locations, which vary as dictated by the circuit design.

Basket Assembly

The horizontal wiring grid is a thin, flat metal strip, which is stamped or etched into six horizontal grids, and two additional insulators are used. The horizontal grid is sandwiched between the two insulators and next the two basket subassemblies. The middle horizontal grid is offset by one ribbon space from the horizontal grids in the basket subassemblies. In other words, the middle grid ribbons fall in line with the spaces between the ribbons of the

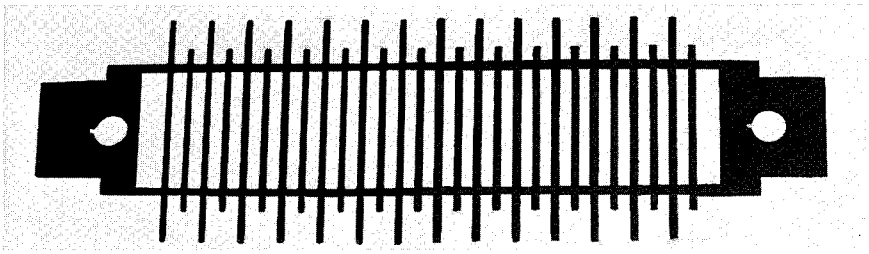


Fig. 2. Vertical wiring grid.

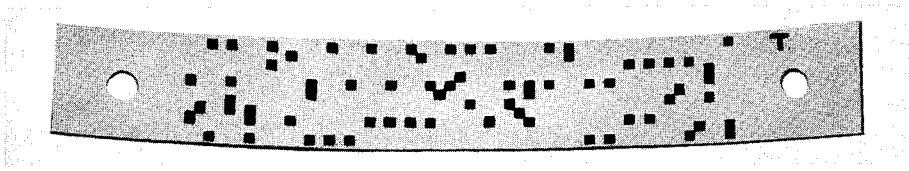


Fig. 3. Dielectric insulator.

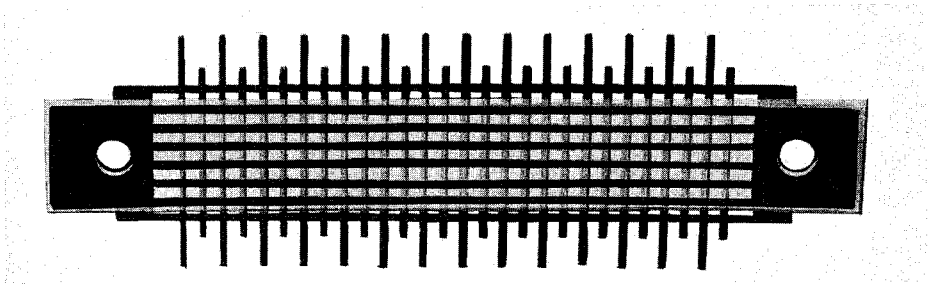


Fig. 4. Welded basket subassembly.

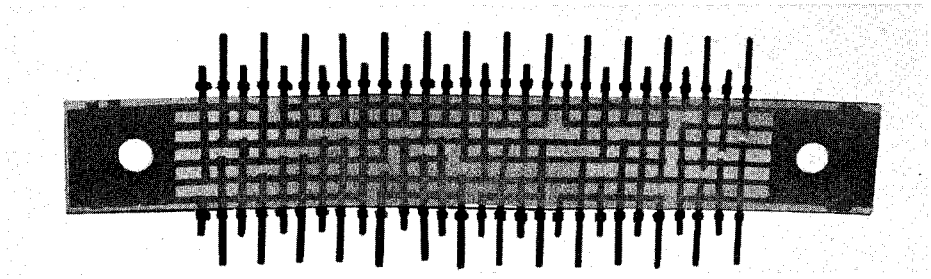


Fig. 5. Punched basket subassembly.

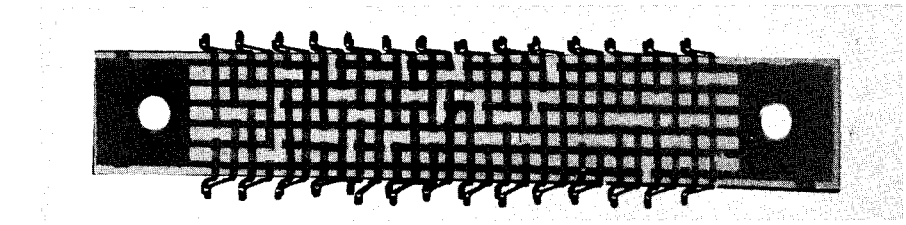


Fig. 6. Formed basket subassembly.

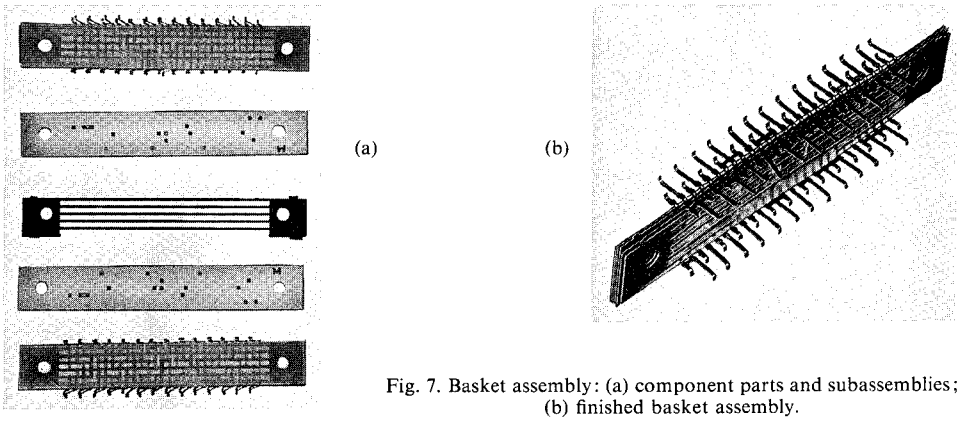


Fig. 7. Basket assembly: (a) component parts and subassemblies; (b) finished basket assembly.

horizontal grids in the basket subassemblies. By the same token, the vertical grids in the two basket subassemblies are offset from each other by one ribbon space. The result is that except for the two extreme outer horizontal grids, no ribbon in the five-layer matrix falls in line with another. This allows, with proper placement of weld clearance holes in the insulators, any vertical ribbon in either basket subassembly to be welded to any ribbon in the middle horizontal grid. In this manner, the two basket subassemblies are mechanically and electrically interconnected to form the final "basket" assembly. The finished basket assembly contains all wiring and interconnections to complete a given circuit.

Component Assembly

The components are now nested on and resistance welded to the projecting formed tabs of the vertical wiring grids. The excess component leads are trimmed off flush with the ends of the tabs. Leads are left long on the components which require inputs or outputs to the mother board to which the module will be assembled. The ends of the basket assembly, which contain the fixture holes, are cut off flush with the last component at either end. At this time, the module is checked electrically and may be repaired or reworked if needed. The last operation is to transfer mold or encapsulate the component assembly for environmental protection. A final electrical test of the completed module is made at this time. Note that modules may be marked or coded in any desired manner during the molding process by the use of colored encapsulants or mold inserts.

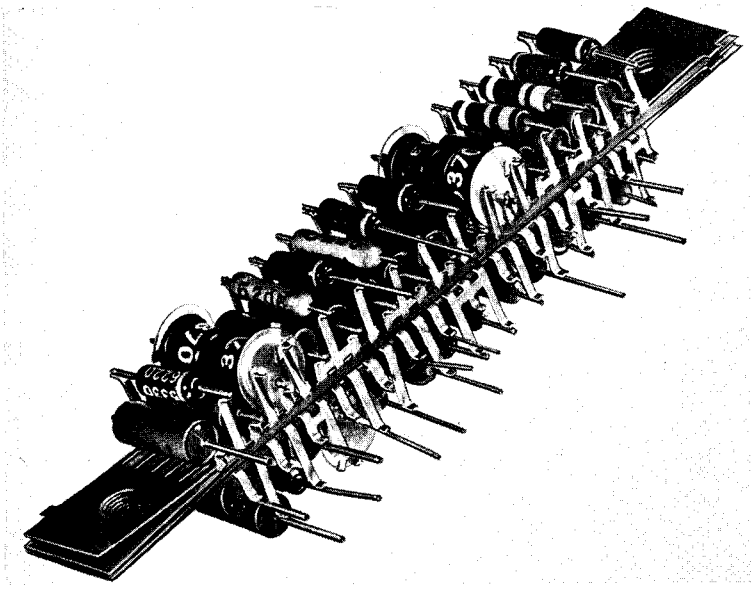
Physical Dimensions

All B-Modules, regardless of circuit configuration, are 0.63 in. wide and 0.58 in. high. Table I lists the length and volume of six typical modules that meet a specific design requirement.

TABLE I

Typical Module Sizes

No. of Circuits	Type of circuit	Number of components	Length, in.	Volume, in.^{3}
5	Two-input diode "AND" diode "OR" gate	21	0.98	0.358
2	High current driver	18	0.98	0.358
4	Emitter follower amplifier	20	0.98	0.358
1	Trailing edge flip-flop	43	1.87	0.650
2	Inverter amplifier	17	0.98	0.358
1	Single-shot multivibrator	30	1.87	0.650



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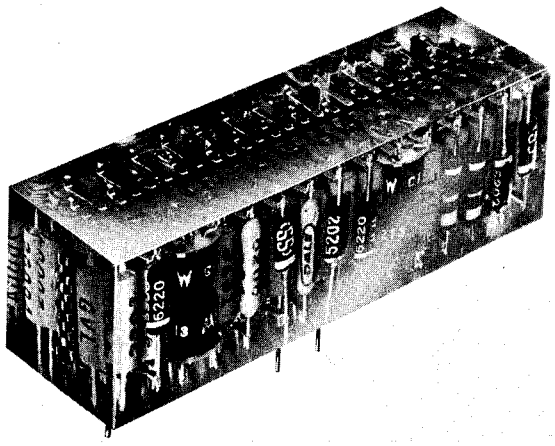

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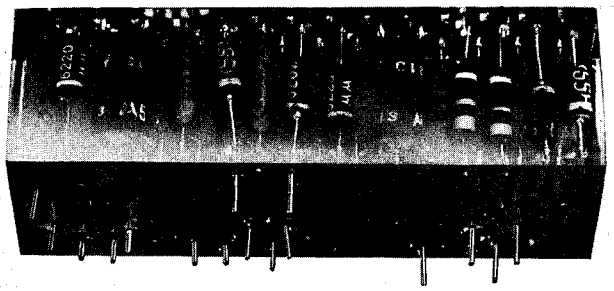

(c)

Fig. 8. Component assembly: (a) prior to encapsulation; (b) after encapsulation; (c) completed assembly.

RELIABILITY

Although the actual numerical reliability advantage of the B-Module design is not known at this time, its features are such that overall decrease of built-in defects or human errors in assembly can be anticipated as compared to most existing cordwood module designs.

The following features are advantageous to high module reliability:

1. The large surface area of the ribbonlike interconnecting material provides large contact area for the weld and for electrode contact resulting in consistent welds.
2. Automated machines will provide excellent control of electrode positioning prior to the weld pulse and prevent element slippage during the weld. The result is a high degree of weld uniformity.
3. The parallel electrode position for welding the component leads to the tabs eliminates many difficult electrode positioning and maintenance problems.
4. The elimination of plaques and the reduction in length of the path which the encapsulating material must travel between components decreases the possibility of voids in the encapsulant.
5. A low component operating temperature results from the short heat path to the module's surface, the large dissipating surface, and the heat transfer through the component leads to a mounting board.
6. Few operator assembly decisions are required, thus human error is held to a minimum.
7. The use of only one weld schedule for all interconnections and the parallel electrode position simplifies electrode dressing.
8. Since a header is not required in the B-Module design, the problem of adhesion between the encapsulant and the header is removed as a potential defect.
9. The module is easily repairable prior to encapsulation.
10. All circuit interconnections are made prior to mounting the components, thus decreasing the chance of component damage during fabrication.

The B-Module requires more welded joints than most other cordwood modules. For comparison purposes, a flip-flop circuit was analyzed using an in-house cordwood technique (see Fig. 9) and the B-Module.

The effect of the additional welds on module reliability is shown below.

Known:

1. Cordwood module has 139 welds.
2. B-Module has 207 welds (68 additional welds).

Assume:

1. Cordwood failure rate = 16.7×10^{-6} failures/hr (predicted).
2. Weld failure rate for both cordwood and B-Module = 0.1×10^{-8} failures/hr. (Equivalent to Atlas Missile Program solder joint failure rate.)

Computation shows that the additional welds decrease the total MTBF by 0.41 %.

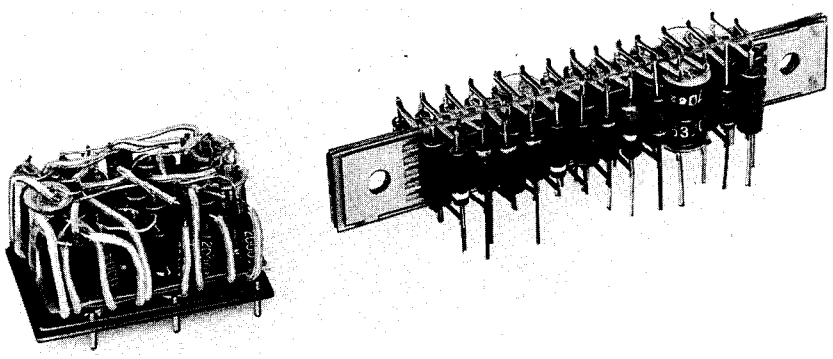

Fig. 9. Module used for weld comparison.

AUTOMATED PRODUCTION

A definite need for the automation of modules has become apparent. A flow diagram (Fig. 10) shows a planned automated production line for B-Modules. This diagram shows, by area, the direction of part flow, transfer machines required, punch presses, welding stations, component insertion stations, transistor stations, and encapsulation area.

Transfer Machine No. 1 and No. 2. Raw strip stock is fed from three spools into separate punch presses, where they are stamped into the horizontal grid, vertical grid, and insulator hole patterns. As the strips emerge from their respective presses, they are automatically merged and fixturized in proper alignment. As the fixturized subassembly indexes through the weld station, programmed welders make the necessary interconnections. The welded subassembly then progresses through a blanking station where programmed punches operate to perforate the grids. Upon completion of the punching, the vertical grid tabs are formed and the subassembly is trimmed to length. The completed upper and lower basket subassemblies are then advanced to bench station No. 1.

Transfer Machine No. 3. Transfer Machine No. 3 is simply a double station, progressive die setup. The center horizontal grid and its two insulators are perforated and blanked, and then conveyors advance the parts to bench station No. 1.

Bench Station No. 1. This area is used to fixturize the upper and lower basket subassemblies with the middle horizontal grid and insulators. The fixturized parts are then sent on their way to transfer machine No. 4.

Transfer Machine No. 4. The fixturized basket assembly is resistance welded by programmed welders. The part then indexes through the component insertion stations. The components are automatically dropped onto the upper basket tabs and held in place by the nest-type fixture. Welding of the components is done automatically by programmed welders. The part is advanced to bench station No. 2.

Bench Station No. 2. This station is used to simply invert the module in the fixture to allow component insertion and welding to the lower half of the module. The fixturized module is fed into transfer machine No. 5.

Transfer Machine No. 5. This transfer machine is identical to transfer machine No. 4, with the elimination of the basket assembly matrix weld station. The components are inserted and welded and passed on to area No. 6.

Area No. 6. The excess component leads are trimmed flush with the basket tabs, except for the mother card interconnection leads. Transistors may be automatically or manually inserted. If manual insertion is used, they are inserted and welded at bench stations. Welding the transistors in place completes the assembly and the module is given a "go–no-go" type of electrical test. Any faulty modules are sent to a repair station while the rest are routed to the encapsulation area. The modules can be either cast or transfer molded into their final form factor. The last operation is a final electrical test to ensure a finished working module.

CAPACITANCE STUDY

In the B-Module, the capacity formed by the "basket" assembly will depend primarily on the cross-sectional area between planes, distance between planes, the dielectric, and the number and location of welds. In the cordwood-type construction, it will depend on the wire routing, the interconnection configuration, and wire length to the input and output pins.

From a preliminary analysis, it appeared that under worst-case conditions the output capacities could add appreciably to the total input and output pin capacities. However, further investigation showed clearly that the input and output pin capacities of the B-Module and the cordwood-type are comparable. Table II shows the measured results of a trailing edge flip-flop circuit utilizing the two packaging techniques.

THERMAL ANALYSIS

The use of the thermal electrical analogy method of solution for heat transfer problems was chosen because of the information of this type available on the cordwood module. This

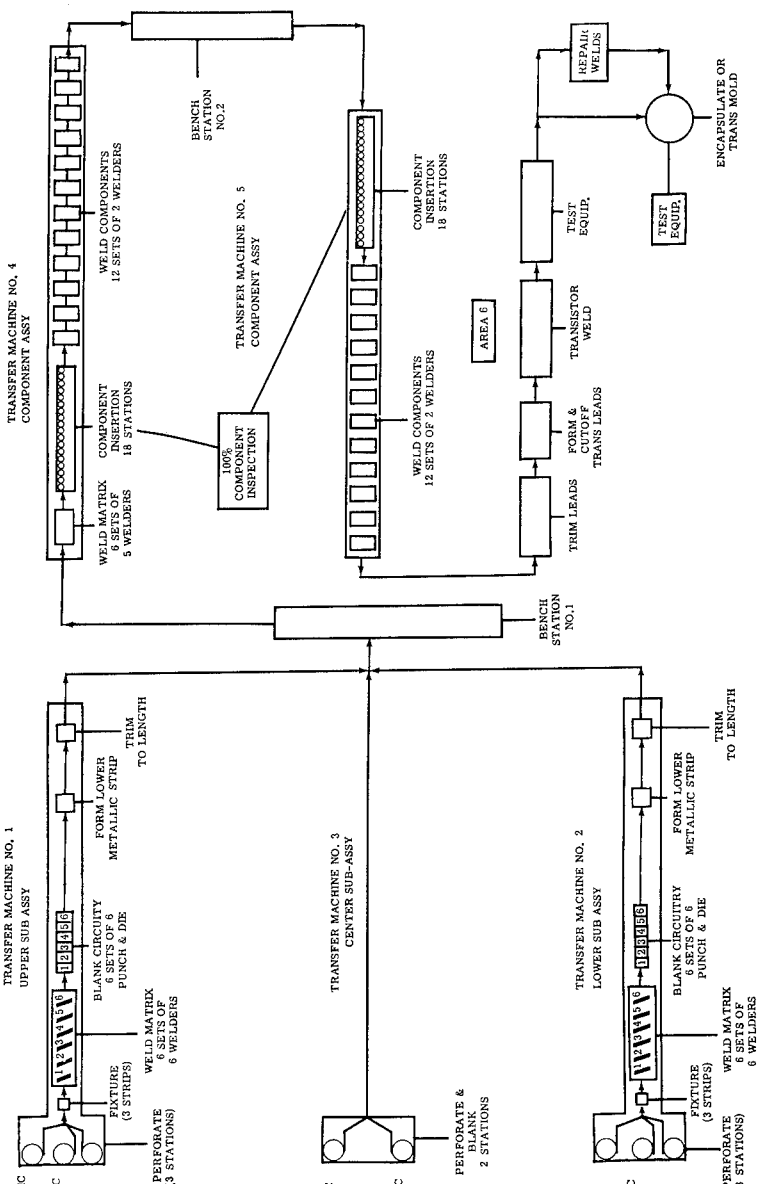

Fig. 10. Automation flow diagram.

TABLE II

Input/Output Capacitance

Circuit	Capacity, pF	
	B-Module	Cordwood-type
Clock input	29	32
"I" input	15	17
"O" input	16	18
"I" output	36	24
"O" output	27	23.5

method of analysis is based on the similarity of the equations describing heat transfer and electrical circuits. The analogous parameters are shown in Table III.

In general, a given package configuration may be presented by a network of resistors, each of which presents an element of thermal resistance to heat flow. The network may then be solved for the primary paths of heat transfer from the source to the surface cooling area. This method of solution offers increased facility to compare alternate designs of component and/or circuit packaging.

Figures 11 and 12 depict the cross section of the modules on which this study is based, and the following heat paths may be established:

Side of Module R_A: This path is through the epoxy coating, R1.

End of Module R_B: This path is through the epoxy encapsulant, R2.

Top of Module R_C: Two paths are used here—one directly from the component assembly through the epoxy, R3; the other is via the component tabs of the basket, R4, and the remaining epoxy, R5.

Bottom of Module R_D: Here two paths are again established. One path, R_E, is directly via the component leads, R6. The other path, R_F, is similar to the top of the module with the addition of the projections and air gap between the encapsulation and the mother card to which it mounts.

Each section of material was treated as having a "lumped" resistance R_T. Based on a circuit dissipating 850 mW, the B-Module has a thermal differential between components and surface measurements of 1.22°F, in comparison to 3.07°F for a cordwood module. This lower differential is due to the greater heat transfer to the surface. The calculated improvement for the circuit is summarized in Table IV where the improved heat transfer is reflected in the reduced thermal resistance R_T of the B-Module. Due to the method of component placement in the B-Module, these figures will vary with component count.

TABLE III

Electrical and Thermal Analogous Parameters

Item	Electrical		Thermal	
	Description	Symbol	Description	Symbol
Source	Voltage	V	Temperature	°F
Flow	Current	I	Heat	Btu/hr
Resistance	Electrical R	R_E	Thermal R	R_T
Law	$V/I = R_E$		°F/Btu-hr $= R_T$	
Conductance	$A/\rho L$	$1/R_E$	$k(A/L)$	$1/R_T$

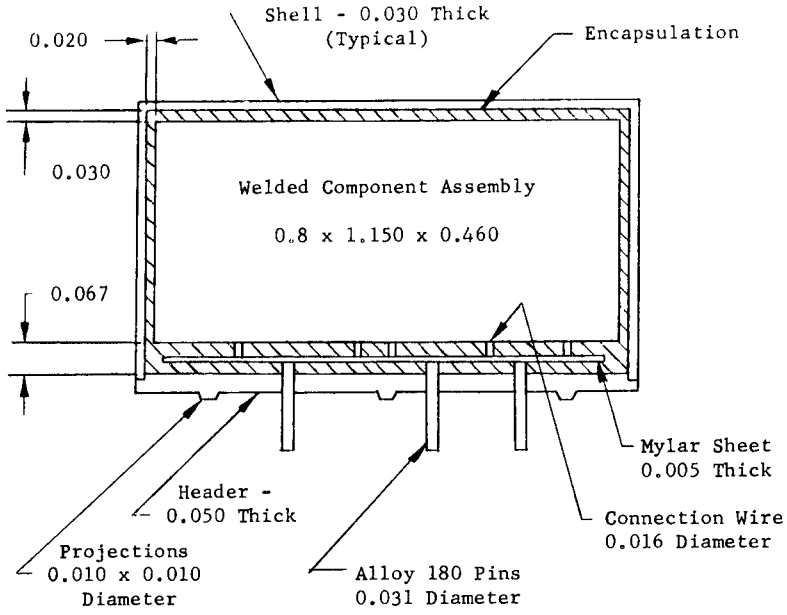

Fig. 11. Section of typical cordwood module.

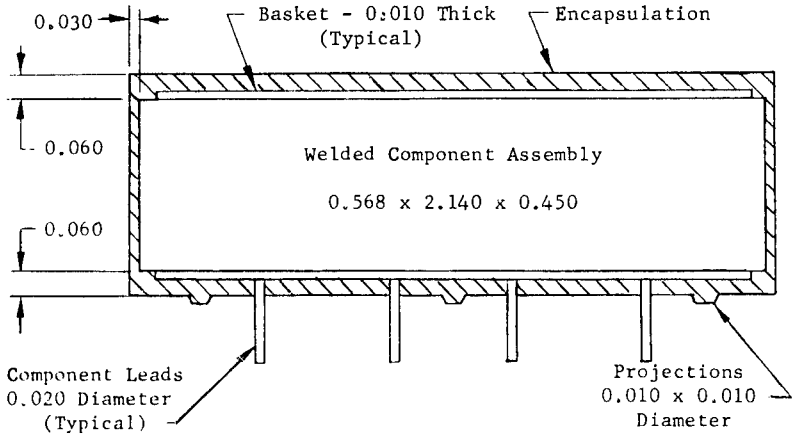

Fig. 12. Section of typical B-Module.

TABLE IV

Thermal Comparison of Cordwood Module and B-Module

Heat flow path	Heat transfer, °F/Btu-hr		
	Cordwood module	B-Module	% Improvement
R_A side	5.71	1.487	74.0
R_B end	6.11	5.203	14.8
R_C top	7.83	2.655	66.1
R_D bottom	17.75	10.053	43.4

RESULTS AND CONCLUSIONS

The B-Module has eliminated the most time-consuming operations of module fabrication—shaping the interconnection wires to intersect the appropriate component leads, applying insulating sleeving where required, and finally positioning and welding these interconnections. The design considers size, cost, weight, fabrication, reliability, maintenance, and cooling. The B-Module results in a module which will meet military specifications, provide high component densities, and permit automated fabrication.

ACKNOWLEDGMENTS

The author acknowledges the assistance from the following engineers, who helped in the preparation of this paper: Mr. R. Kroll for his contribution to the thermal analysis studies and Mr. G. Christ for his contribution to the capacitance studies.

8063

Interim Packaging Concept for Frequency Division Multiplex Carrier Telephone Equipment

TAICHIRO ATARASHI
Fujitsu Limited, Kawasaki, Japan

This paper provides an explanation of the packaging of an advanced design for trial channel modulator equipment adapted to CCITT recommendations. The entire packaging concept is covered in general, and it is emphasized that the equipment is designed for rationalization of assembling and testing, and for simplification of maintenance. Each voice channel circuit, including signaling circuits is installed in one plug-in unit, and all plug-in units needed for a system of twelve voice channels are installed in a shelf. Furthermore, as a result of new packaging techniques, the equipment can be mounted in a bay with up to 240 voice channels.

INTRODUCTION

SINCE 1936, when we started to produce them, we have been manufacturing various kinds of carrier equipments. In 1958, we began to produce all-transistorized equipments to take the place of conventional ones using vacuum-tube systems. At present, transistorization has been achieved in every field of carrier equipment. Use of transistors in carrier equipments has led to reductions in size, power consumption, and cost, as well as to simplification of maintenance, and, as a result, carrier equipments are now employed in many new areas.

In order to broaden the field of possible application of carrier equipments, further reductions in cost and size and simplifications of maintenance are required. To this end, we have been accelerating the development of smaller equipments than the present transistorized ones, and have now produced a prototype of a miniaturized equipment to be used for modulating voice or voice-frequency signals in the frequency band from 60 to 108 kc (group B of the CCITT recommendations).

As a result of miniaturization, this equipment can mount four times as many channel units as the transistorized channel modulator equipment that we have been making up to now. That is to say, the present transistorized equipment can mount 60 channel units and the trial equipment 240.

The channel modulator equipments developed in 1958 were supplied to Japanese National Railways, National Defense Agency, electric power companies, etc., as well as Nippon Telegraph and Telephone Public Corporation, and produced satisfactory results. The design of the experimental miniaturized channel modulator equipment has been based on the actual results in these broad fields of application.

BASIC DESIGN CONSIDERATION

As stated above, in order to broaden the field of application of carrier equipments we must achieve reductions in cost and in size and simplification of maintenance, and still furnish the high reliability and good electrical performance that are required to maintain long communication circuits stable and of good quality.

Furthermore, activity in data transmission has recently increased and, as discussed in CCITT, it is now felt that the range of communication should be enlarged from intra- to intercontinental communication. Consequently, even higher reliability and better electrical performance are required, and miniaturization and greater economy in the design of equipment are a must.

Fortunately, techniques today are greatly improved over those of five years ago, and present conditions are favorable for the realization of miniaturized and economical transistorized carrier equipment. Especially remarkable progress has been made in the development of various kinds of electrical materials and electrical components.

Our company has projected the miniaturization of capacitors, resistors, filters, and polar relays, and has begun to investigate the packaging of miniaturized equipment using these components with the aim of rationalizing the manufacturing process and testing procedures and simplifying maintenance. This investigation has been conducted on the assumption that the equipment will be constructed using one plug-in unit per channel (it now uses three) and that each group of twelve channels (which corresponds to group B of the CCITT recommendations) will be installed on one shelf (it now occupies three).

Filters are used at various stages in frequency division multiplex carrier equipment and play a very important role. These filters require many inductors and, moreover, inductance must be adjusted precisely.

Since the miniaturization of inductors is far more difficult than that of such other components as capacitor and resistor, the only practical approach to system miniaturization is to miniaturize the other components and to introduce effective packaging.

In the present transistorized equipment, axial lead components such as capacitors and resistors are attached to the printed circuit board, together with the inductors, individually and parallel to the board, so that the component density is not very high. To improve the component density, it was decided to adopt cordwood module packaging for such mounted components as resistors, capacitors, and diodes. To rationalize production, a uniform module size has been adopted. The components used in the modules have recently been standardized. The average component density (per unit effective mounting space) is about twice as high for the miniaturized equipment than it is for the present standard equipment.

In order to make the plug-in unit adaptable to carrier equipments using higher frequencies without any structural changes, an electrical shield cover is provided. Nonsoldered wiring connections (wire-wrapped connections) have been adopted to decrease work in fabrication and improve reliability.

The centralized jack panel mounted on the present equipment for purposes of maintenance and testing has been replaced by panels on each plug-in unit of the trial equipment, with a view to simplifying maintenance work. This not only makes the mounting space of the centralized jack available for mounting the system shelves, but also simplifies the wiring of the equipment since the rack wiring from each system shelf can be connected directly to the terminal block at the top of the bay rather than via the centralized jack panel. In this way it becomes possible to mount four times as many systems, and the assembly of the equipment becomes simpler.

It goes without saying that the above considerations are, in part, the result of data obtained during widespread use of transistorized carrier equipments manufactured over the past five years.

SPECIFICATIONS

Generally speaking, the electrical characteristics and construction of the equipment are designed to meet the CCITT recommendations. Mechanical construction, in particular, meets the following specifications:

1. Equipment to be mounted on a standard free-standing iron frame, 2750 mm high × 520 mm wide × 225 mm deep.
2. Equipment to have front access for ease of installation and maintenance and to allow back-to-back installation.

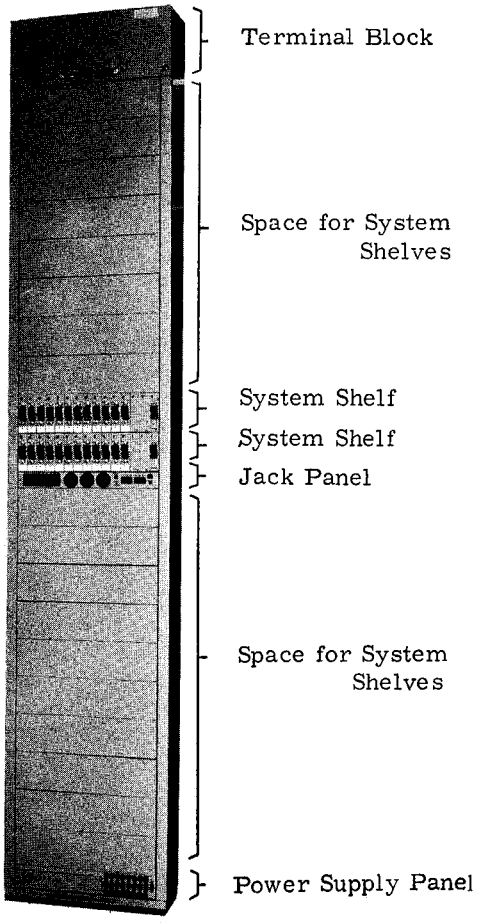

Fig. 1. Trial miniaturized channel modulator bay.

3. Test points and adjustments to be accessible from the front of the equipment for ease of maintenance and testing.

DESCRIPTION OF THE EQUIPMENT

The equipment is mounted on the above-described free-standing frame, which is made of thin steel and is designed to have maximum interior space by the elimination of the conventional door.

At the top of the frame there is the terminal block through which the wiring in the frame is connected to the office cables that carry voice, signaling, carrier current, and power supply.

The jack panel for maintenance work is located near the middle of the frame, and the power-supply panel for distributing and supplying power and carrier current is at the bottom of the frame.

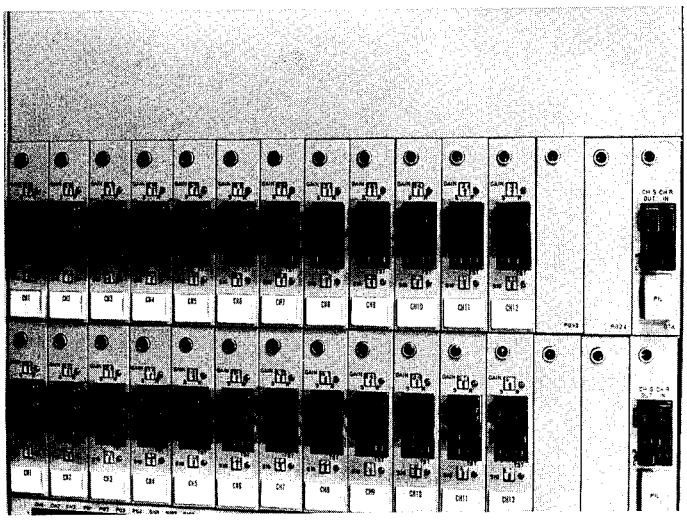

Fig. 2. System shelf assembly.

For channel modulation, 15 units plugged into each shelf are grouped to serve as one system (12 channels). Ten systems can be located above the jack panel and ten systems below it. Thus a fully equipped frame can accommodate twenty systems. A frame with two systems is shown in Fig. 1.

Shelf

The shelf is 119 mm high (nominal value), and is fastened to the frame at four points (the upper and lower sides of the front and back flank) with screws and nuts. Thirty grooves of 15 mm pitch are hollowed out on the upper and lower sides of the shelf for inserting the plug-in units. The standard width of the unit is 33 mm. One shelf is equipped with up to 15 units. The arrangement of the plug-in units shown in Fig. 2 is as follows: from the left, CH1, 2, 3, . . . , 12, channel modulator-demodulator, PG 1–3, PG 2–4, pregroup modulator-demodulator (two PGs are mounted on one unit), and the group transmitting amplifier. These 15 units comprise one system (12 channels), which is as recommended by CCITT.

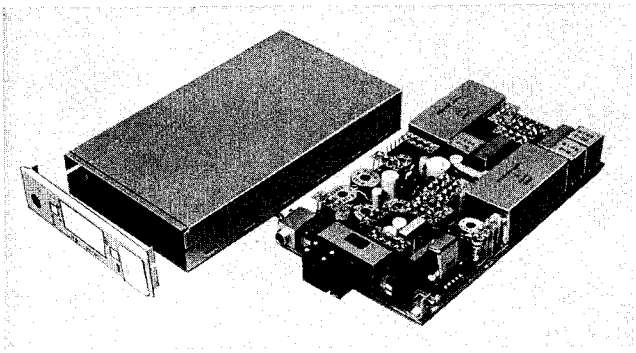

Fig. 3. Plug-in unit assembly.

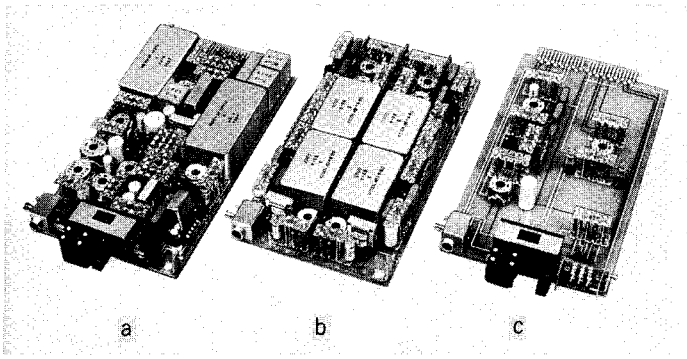

Fig. 4. Plug-in unit: (a) channel unit, (b) pregroup unit, (c) transmitting amplifier unit.

Plug-in Unit

The plug-in unit (approx. 107 mm × 198 mm × 30 mm) consists of an aluminum case, a printed circuit board which slides into the case, and a cover plate (see Fig. 3). The aluminum case serves as a shield between units. This design has the advantage that the unit can be used not only in channel translating equipment but also in high-frequency applications.

The printed circuit uses a double-sided board with through-hole plating, with individual components (filters, coils, etc.) and circuit components in small cordwood modules mounted on one side of the board.

The plug-in terminal is of the card-in type and is provided with 27 terminals (with the key notch).

The channel composition is 1 CH per unit, including a ringer circuit, and the pregroup composition is 2 PG per unit, including modulator and demodulator. One system (12 CHs) is mounted on each shelf. This affords easy maintenance. Three kinds of units (CH, PG, GTA) are shown in Fig. 4.

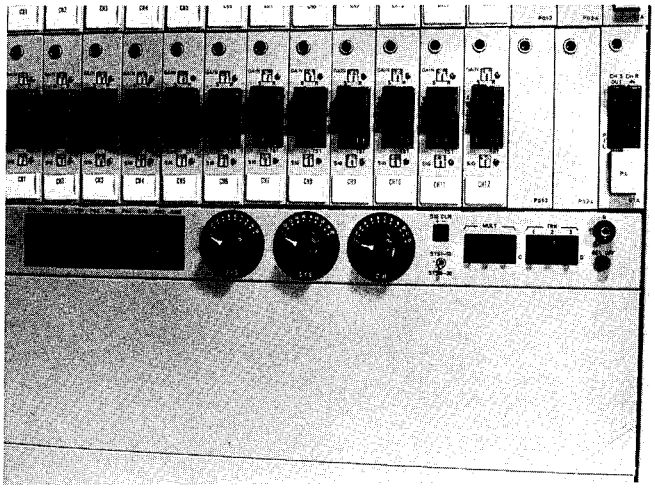

Fig. 5. Jack panel.

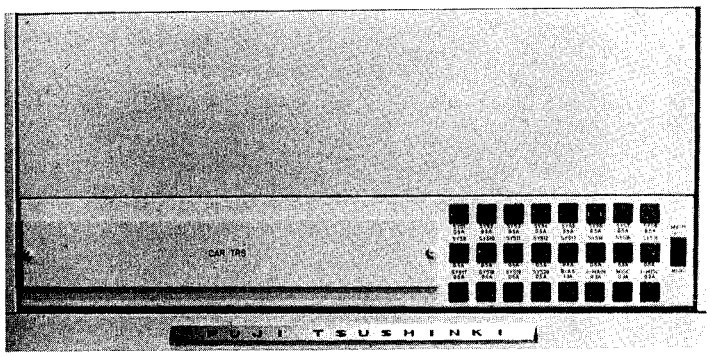

Fig. 6. Power supply panel.

Jack Panel

Level measurement, maintenance, and check of the equipment can be performed at the front of each unit. The jack panel is provided with jacks for measuring carrier current level and signal current, switches for channel selection, bell-off push button and ground terminal (see Fig. 5). These facilities are common to the whole equipment and are used for maintenance.

As signal current is measured most frequently and as this operation is simple, the equipment has been so designed that all jacks needed for it are concentrated on the jack panel and channel selection can be performed by means of three rotary switches and one snap switch.

Power Supply Panel

This panel, mounted at the bottom of the equipment, has the twofold function of distributing power and carrier current. Power is supplied at -21 V DC from the station battery and is distributed to each system (12 CHs) through a miniature fuse which has an alarm contact point when fused. The relay group for central alarm indication, which consists of two fuse alarm relays and one bell-off, is also mounted in this panel.

The different carrier currents supplied from other equipment, e.g., the No. 1–3 CH carriers, No. 1–4 PG carriers, No. 1–3 signal carriers, and pilot carrier, are impedance-matched, level-adjusted for the load, and distributed to each five systems (60 CHs) through the carrier transformers (CAR TRS). One unit functions as carrier distribution unit for each carrier frequency, and level adjustment for the load can be performed at the front of it by changing terminal connections. A front view of this panel is shown in Fig. 6.

Wiring and Terminal Block

Nonsoldered connections have been adopted for the equipment in order to provide higher reliability, that is, wire wrapped connections for the terminal blocks (see Fig. 7), card receptacles and terminals for miscellaneous units, and compression connections for the terminals of large current capacity, such as the power supply.

The band cable shown in Fig. 8 is used for voice wires and signaling wires (between the on-frame terminal and the system) in order to save wiring space and working time. It is formed by the required number of insulated wires joined with adhesive in parallel to make a band. For voice, 12 pairs of wires, and for signaling, 28 single wires are joined with adhesive in this manner. The band cable for one system (12 CHs) is made up of two pairs of these voice and signaling bands.

Metallized paper is inserted between the voice wires and the signaling wires to avoid noise caused by cross-talk of the signal pulse between the signaling wire and the voice wire.

Terminals of the terminal block and card receptacles for back-panel connections are of the wire wrapped type, and each terminal block is provided with the terminals for one system

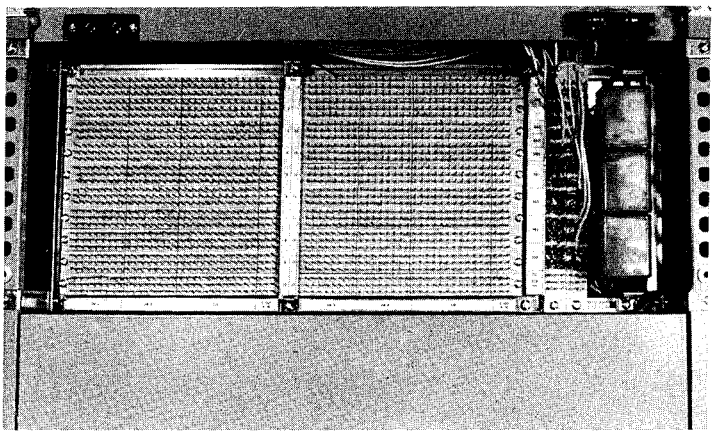

Fig. 7. Terminal blocks.

(12 CHs). The wiring of the terminal block and back panel is shown in Fig. 9. The arrangement of the terminals and the wiring scheme are shown in Fig. 10.

Components Used

Modules. To obtain high component density, circuit components such as resistors, capacitors, and diodes are mounted on the printed circuit board, not simply but in the form of small cordwood modules (see Fig. 11). The printed board for modules of uniform size (9 mm × 24 mm × 0.5 mm thick) has ten component-mounting slots along its perimeter.

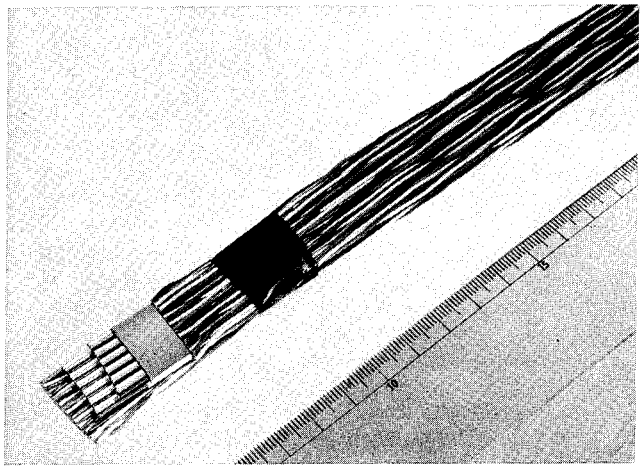

Fig. 8. Band cable. (Note that in this and succeeding figures, the scale is in centimeters.)

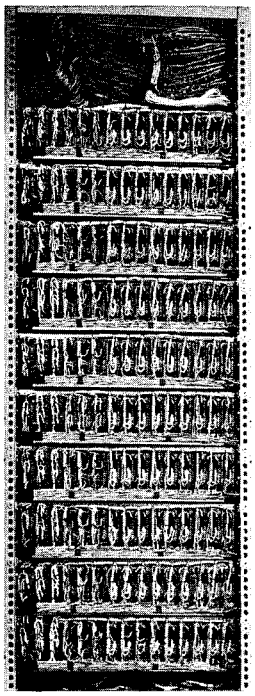

Fig. 9. Wiring of terminal blocks and shelves (shows upper half of bay).

Each module has two printed boards with the necessary printed circuits at the top and the bottom, with the components arranged and connected between them. The leads of the components are used as terminals of the module when it is mounted to the main printed-circuit board. Component density is approximately 1 piece/cm^3.

The component length for the module is kept less than standard (max. 13.5 mm) to limit the height of the module. Different kinds of components are shown in Fig. 12. Typical sizes of miniature components are compared with those of conventional ones in Table I.

Filters and Polar Relays

(1) *Channel and Pregroup Filters.* The volume of the hermetically sealed filters is reduced as shown in Table II due to the use of small coils, miniature capacitors, and a unique miniature packaging method. The channel filter compared with the conventional one is shown in Fig. 13.

TABLE I

A Comparison of Typical Sizes for Miniaturized and Conventional Components

Component	Volume, cm^3		Ratio, %
	Conventional	Type MT	
Resistor (carbon)	0.16	0.06	35.5
Capacitor (Mylar)	0.42	0.38	90.0
Capacitor (MT)	7.0	1.3	18.5
Capacitor (tantalum)	0.7	0.17	24.5
Capacitor (polystyrene—for filter use)	0.65	0.18	27.8

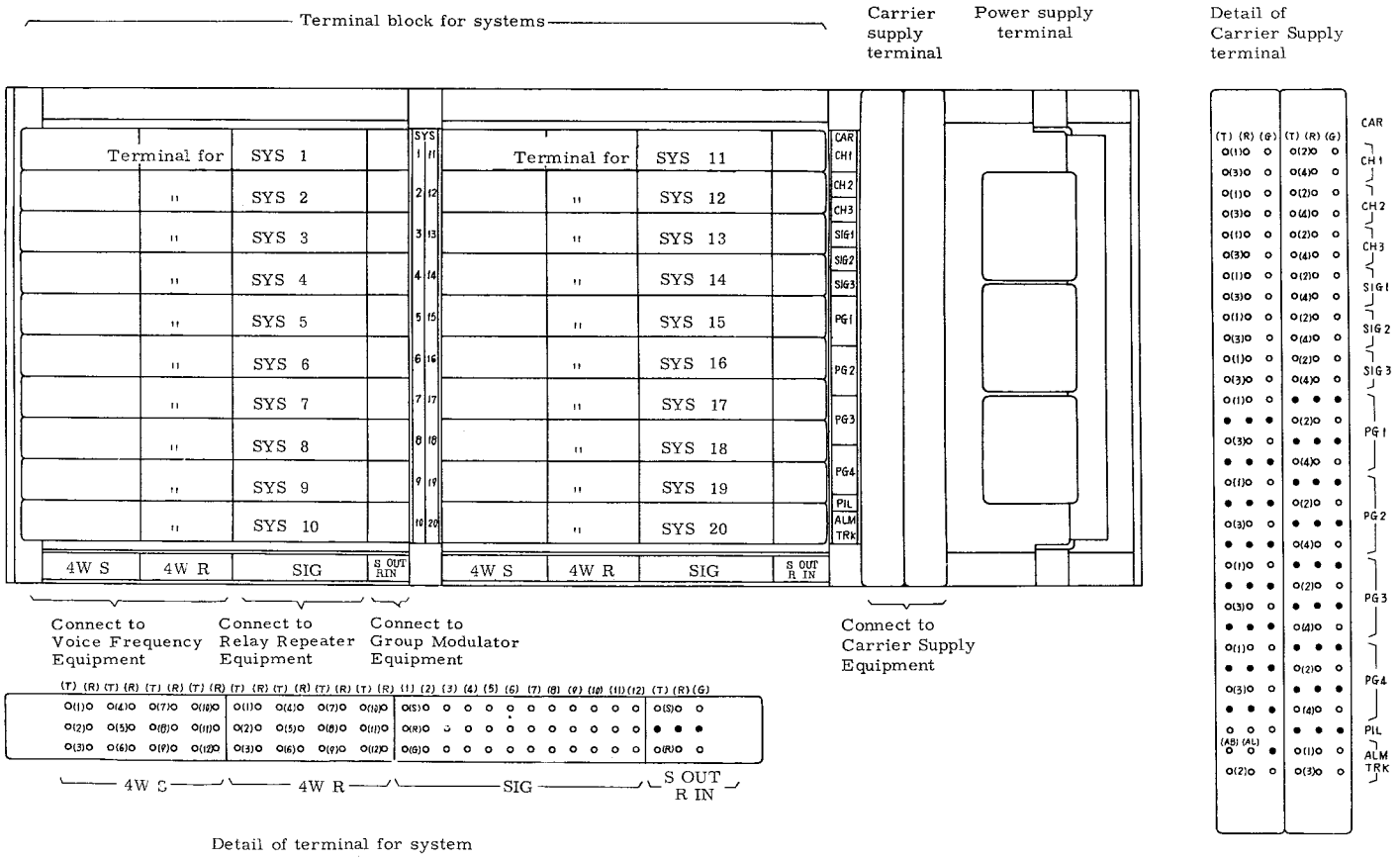

Fig. 10. Arrangement of terminal blocks. Each system band cable is connected to the system terminal blocks horizontally, while office cables are connected to system terminal blocks vertically.

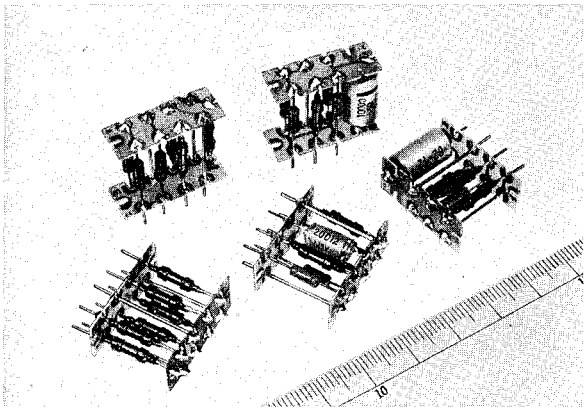

Fig. 11. Modules.

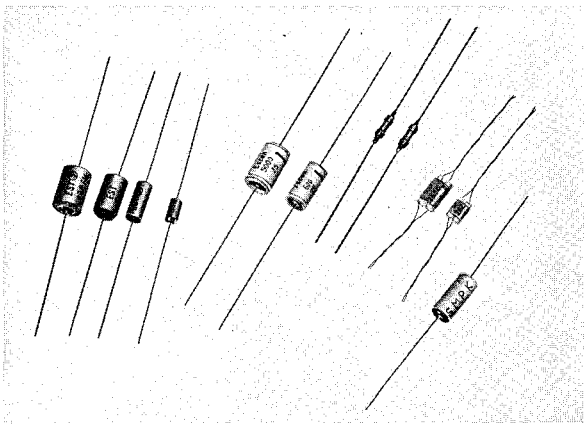

Fig. 12. Capacitors and resistors for use in modules.

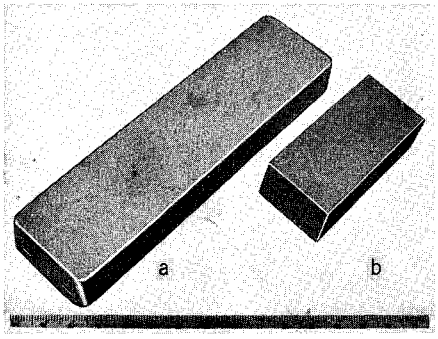

Fig. 13. Filters: (a) conventional filter, (b) miniaturized filter.

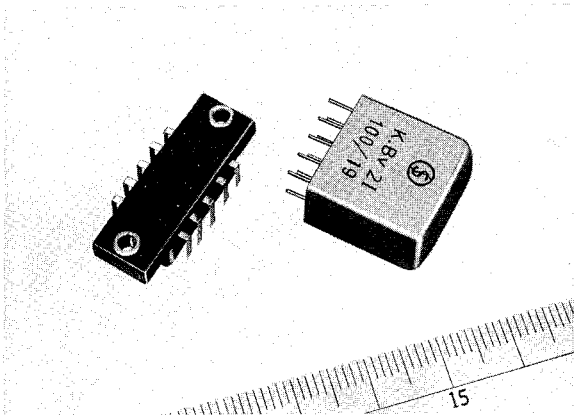

Fig. 14. Type 22 polar relay.

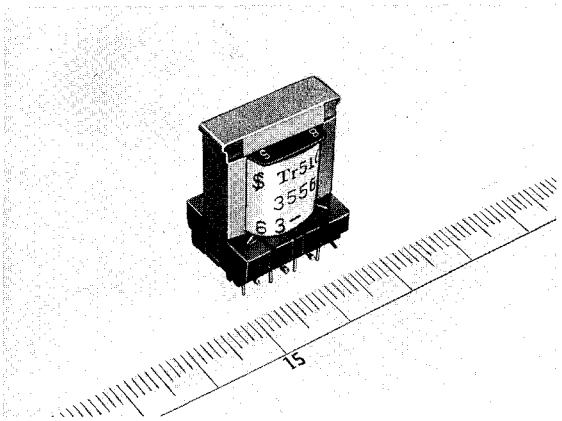

Fig. 15. Transformer assembly.

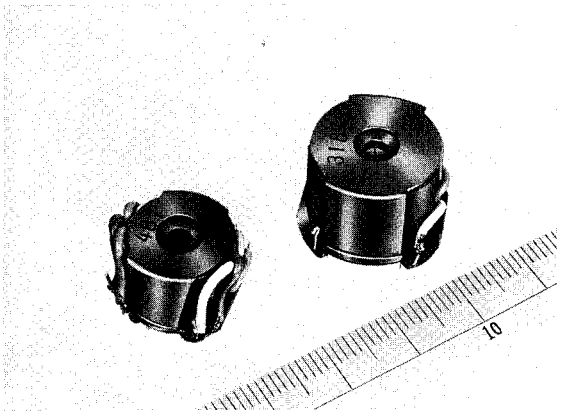

Fig. 16. Coil assembly.

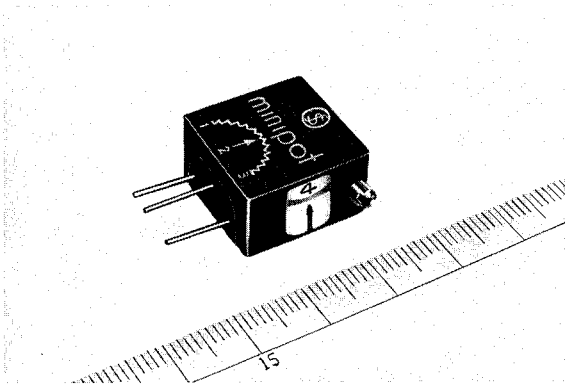

Fig. 17. Miniaturized potentiometer.

(2) *Signal Filter.* Adoption of the mechanical filter replacing the conventional crystal filter contributed much to the reduction in size. A comparison with the conventional filter is shown in Table III.

(3) *Polar Relay.* The epoch-making miniaturization owes much to the newly developed Type 21 polar relay, shown in Fig. 14, which is used instead of the conventional Type 55. The figures are given in Table IV.

Coils and Transformers. Construction is simplified by the adoption of open-type coils, replacing the pot type with plastic seals (see Figs. 15 and 16). Moreover, due to the improvements in the material, the diameter of the cup core is reduced from 18 mm to 14 mm, which also reduces the cost. A comparison is given in Table V.

Potentiometer. A miniaturized potentiometer using evaporated thin-film metal resistors on a wafer has been developed. It has an indicator to facilitate maintenance (see Fig. 17).

TABLE II

A Comparison of Sizes for Miniaturized and Conventional Filters

Filter	Volume, cm^3		Ratio, %
	Conventional	Type MT	
Channel filter	120.0	49.0	40.7
Pregroup filter	96.0	38.0	39.5

TABLE III

A Comparison of Sizes for Miniaturized and Conventional Signal Filters

Filter	Volume, cm^3		Ratio, %
	Conventional	Type MT	
Transmitting	40.0	12.0	30.0
Receiving	64.0	18.0	28.0

TABLE IV

A Comparison of Sizes for Miniaturized and Conventional Polar Relays

Component	Volume, cm^3		Ratio, %
	Conventional	Type MT	
Polar relay	3.50	4.5	13

TABLE V

A Comparison of Sizes for Miniaturized and Conventional Coils and Transformers

Kinds	Volume, cm^3		Ratio, %
	Conventional	Type MT	
Cup core	7.45	2.92	39.5
Laminate core	7.8	5.95	76.0

CONCLUSION

The equipment discussed above is an experimental design, and various investigations are being conducted into its characteristics and capabilities. Based on our results, we should be able to refine the design even further in the near future.

8064

The Application of Welded Micrologic Modules and Wire Wrap Techniques to Ground Support Equipment

C. F. MIDDLETON
Product Design Engineer, Raytheon, Sudbury, Massachusetts

The objective of the design described in this paper is to solve the ever-present problem of low production quantities, through reduction of functional entities to the point where the greatest number of repetitive items can be realized. This is accomplished without losing sight of the essential factors of reliability, maintenance, producibility, handling, documentation, quality, and cost. The unique method by which the welded terminations are treated within the micrologic modules contributes greatly to the reliability and producibility of the system. The use of wire wrapped interconnections also enhances reliability and producibility, while giving inherent quality to the completed assemblies.

INTRODUCTION

THIS REPORT DEALS with the application of two modern-day by-products of the electronics industry which ultimately increase reliability, automate costly production operations, and enhance maintenance features, namely, welded modules and wire wrapped interconnections. At the outset, the requirements were that the package be capable of housing digital electronics that theoretically would be packaged in modular building blocks. However, every system eventually must give way (for one reason or another) to one or more situations that require additional volume over and above that of the standard building block. Therefore, one of the ground rules was to provide inherent flexibility in the design of the circuit building blocks without hindering standardization. As in any conceptual problem, the originator must establish parameters that satisfy all of the associated customers and support functions. In this design activity these parameters were as follows:

a. The design to be compatible with both breadboard and production problems through the reduction of dissimilar techniques and layout configurations.
b. Breakdown of subassemblies to be consistent with quantity production techniques; items peculiar broken off at the lowest possible design entity.
c. Modular subassemblies to be constructed and designed for quick interchangeability and replacement, with emphasis on maximum in-rack test capability.
d. Subassemblies that house circuit functions to be limited in weight to 30 lb for ease of handling.
e. The interconnection media of logic circuits to be the wire wrap process, in the interest of reliability and automation.
f. The design configuration to be compatible with incorporating as much interconnection "thinking" as possible within the wire wrap program.
g. Interconnections between wire wrapped assemblies to be through the use of "non-thinking" jumper cables, in the interest of standardization and reduction of inevitable production changes.

h. Where "thinking" cables are utilized, their size and complexity should be minimized.
i. Logic circuits to be packaged in modular plug-in building blocks that do not exceed practical cost for storage of spares, etc.
j. Logic modules to have all internal electrical connections welded, with emphasis on overall reduction of the number of welds, in the interest of reliability and ease of assembly.
k. Logic modules to be encapsulated in their final form to enhance reliability.
l. Due to the space restrictions imposed by complex ground-based systems, higher packaging density is desired.
m. Reliability, producibility, and maintenance features to be of foremost interest.

THE LOGIC DRAWER

The *logic drawer* described herein is basically a standardized modular concept for the purpose of housing logic circuits for either computers or computer check-out equipment as applied to military specifications. Because many computer functions are available as commercial items (tape punches, tape readers, etc.), and are most commonly sized to fit 19-in. panel-width enclosures, one ground rule was to design the logic drawer to be compatible with standard enclosures and equipment. The size requirements of this drawer are as follows: front panel dimensions should not exceed 19 in. wide × $12\frac{1}{4}$ in. high, and drawer depth (including cable followers), should be compatible with 30-in.-deep enclosures.

The packaging capacity of the drawer is divided into smaller subassemblies consistent with handling requirements and contributing to the overall flexibility of the drawer. A drawer that is fully loaded with logic modules would normally have five logic plate assemblies and one interconnection plate assembly. The drawer in Fig. 1 shows the inherent flexibility that this unit possesses. In this particular application, fewer logic modules were required along with the added requirement for a power-supply assembly. The incorporation of the power supply was achieved by deleting two logic plates and utilizing the same mounting holes for attaching the power supply. The logic plate assemblies utilize wire wrapped plates that are supported by an extruded aluminum frame. The wire wrapped pins (1400 per plate) are protected by a phenolic cover with 1400 corresponding holes. The holes in the phenolic cover provide test point capabilities when the logic plates are in the extended position. The circuit side of this assembly has a load capacity of 64 standard-width modules (0.37 wide) and two 60-pin connectors, which attach via flexible jumper cables to the interconnection media.

The wire wrap plate, which is also a structural member of aluminum, is filled with 1330 nylon insulated contacts (Fig. 2). In addition to this, there are 70 contacts in direct electrical contact with the aluminum plate. This is accomplished by substituting an aluminum bushing for the standard nylon pin insulator. This feature enables utilization of the aluminum plate as a ground plane and, consequently, each circuit module has its number 20 pin in continuity with this ground plane. The ground plane is insulated from its chassis by a hard anodized finish on the logic plate assembly frames. Flexible jumper cables (120 wires each) connect the logic plate assemblies to the main interconnection plate. The power supply is connected to the interconnection plate with a cable of 60 wires.

The interconnection plate assembly utilizes the same basic hardware as the logic plate assemblies with slight modifications to facilitate mounting hardware. The purpose of an interconnection assembly is threefold.

a. This assembly provides a termination area for all internal jumper cables.
b. By utilizing the programmed process of wire wrap to do the interconnecting, which would normally be accomplished with a complex wiring harness, cables can be of the simple jumper cable variety.
c. The physical location of this assembly within the drawer allows accessibility through the test point cover to all interconnection terminations within the drawer from the front of the unit. Accessibility to the connector side of the interconnection assembly is achieved by pivoting it forward. In addition to the termination of logic and

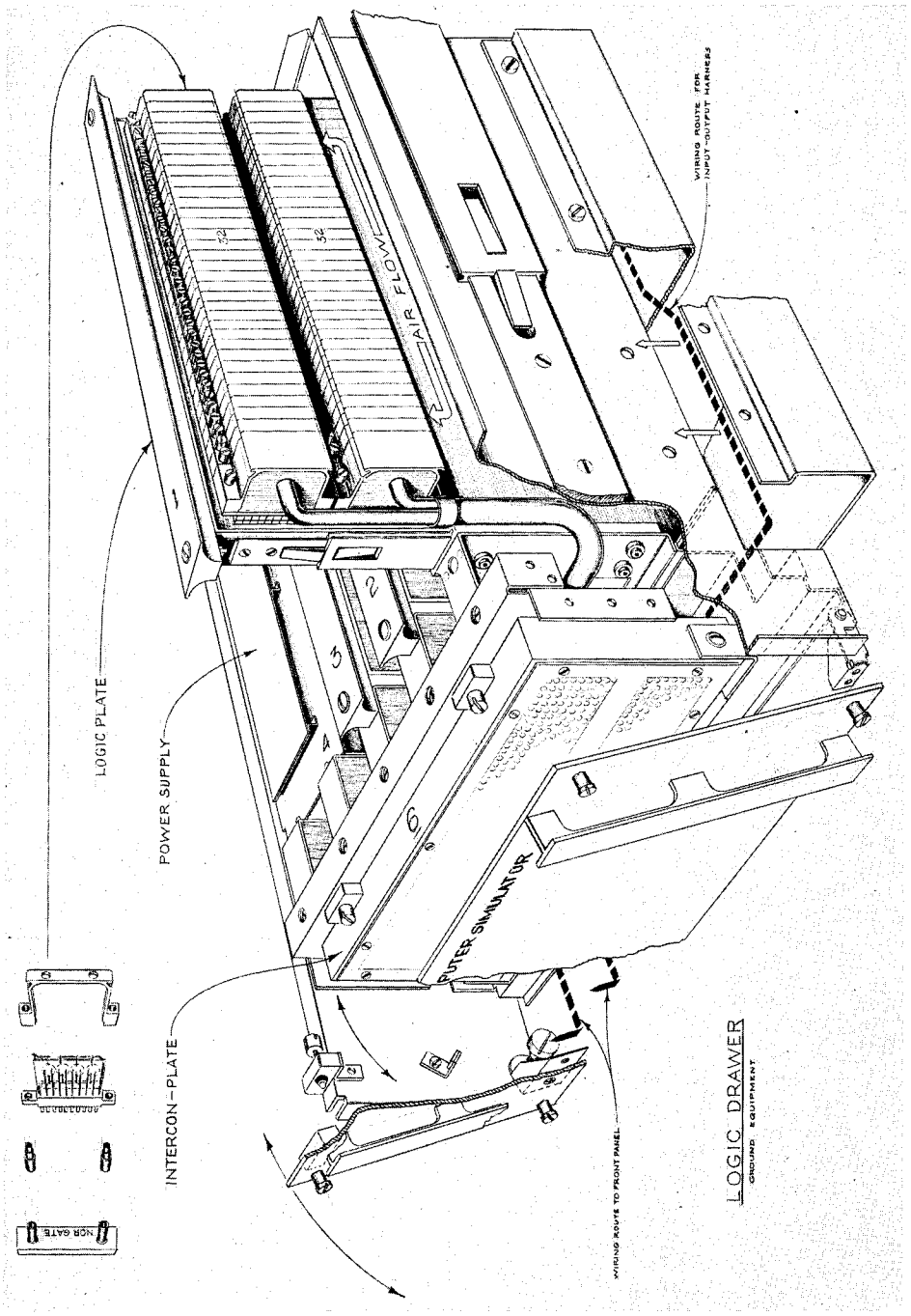

Fig. 1. Fully assembled logic drawer.

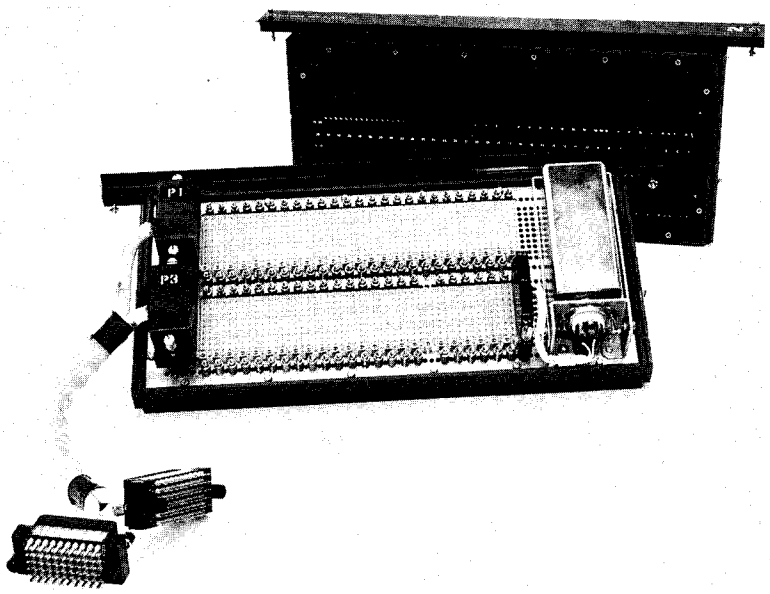

Fig. 2. Wire wrapped plate and frame assembly.

power-supply assembly cables at the interconnection plate, front panel and input–output cables terminate here as well.

The front panel assemblies are peculiar to each type of drawer and therefore, the entire front panel has been designed as a functional entity. Its wiring harness is terminated with connectors to facilitate plugging into the interconnection assembly. The front panel has also been designed to pivot for access to the interconnection plate test point panel as well as for ease of maintaining front-panel components.

THE WELDED MODULES

Vacuum tube manufacturers have applied the reliable techniques of resistance spot welding for many years, but its more recent application to electronic circuitry has met with conservative

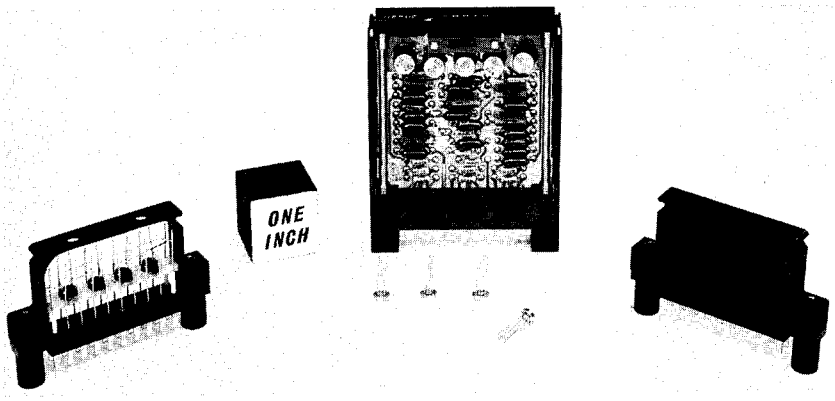

Fig. 3. Logic drawer module.

acceptance. Its progress as a competitive method of packaging, as compared to printed circuits has been lagging due to the economics. Resistance spot welding, as opposed to soldered terminations, has been proven capable of meeting the most stringent requirements. To a large degree this can be attributed to the type of controls that permit the location of welds in close proximity to the component bodies with no resultant heat damage to the components.

In any electronics system, reliability is increased by cutting down the number of interconnection terminations. In the modules utilizing welding, the number of terminations required for a component to reach its outermost point on the connector pin has been reduced to one. The use of micrologic reduces the number of terminations even further when compared to building circuits utilizing conventional components and techniques. The micrologic circuit utilized in this system is the NOR circuit. The NOR element, or building block, is equivalent to three conventional transistors and two resistors. The diffused-mesa transistor principles have been applied to the development of micrologic elements. This process is a natural extension of current techniques and has proven reliability in the semiconductor industry. Each element, or TO-47 can, has an eight-lead header but only six of these leads are active in the NOR element. The diffusion process eliminates many terminations that would normally be made by soldering or welding. These features combined with the previously mentioned reduction in terminations that the module design offers contribute greatly to the anticipated overall system reliability. Reasons such as these encourage us to develop welded modules toward a comparable economic status with printed circuits, while keeping in mind the obvious advantages achieved. The following types of modules are currently in production:

NOR Module	Micrologic } Represents approximately
Gated Flip-Flop Module	Micrologic } 85% of circuitry in system
Driver Module	Conventional components
Transformer Driver Module	Conventional components
Resistor Module	Conventional components
Diode Module	Conventional components
Interface Receiver Module	Conventional components
Interface Coupling Module	Conventional components
D to A Converter Module	Conventional components
Clock Module	Conventional components

FEATURES OF MODULE (Fig. 3)

The interconnections within these logic modules is accomplished through the highly reliable process of resistance spot welding. Approximately 85% of these modules contain micrologic, and all are encapsulated in their final form.

Connector

The connector is molded of diallyl phthalate and contains twenty feed-through pins that rise the entire height of the module on the circuit side of the connector. This feature reduces the number of welds, which subsequently enhances reliability and contributes to the structural integrity of the circuit matrix prior to encapsulation.

Index Receptacles

The receptacles integrate module keying, captivation of hold-down hardware, and the means of fastening the module structure together.

Module Frame

This extruded aluminum frame incorporates features for receiving an extraction tool and serves as a protective wrap-around for circuits, thus eliminating the requirement for expensive molding dies. This wrap-around can provide heatsink capability for circuits with the requirement. The extrusion also allows for modules to have a flexible third dimension. All of these

modules are encapsulated in their final form with Stycast 2850 which is a metal-filled epoxy having a thermal conductivity of 4.0 Btu-ft^2/hr-°F-in.

The Wire Wrapped Interconnections

Wire wrap, as the name implies, accomplishes the industry-old problem of terminating jumper wires by wrapping the conductor around the terminal, as opposed to soldering, welding, or crimping. Although interconnection volume is not reduced to any startling degree, the advantages are many. Certainly welded matrix and flex print can be designed into less volume if this is an absolute must. But, let us look at these many advantages. By simply orienting one's thinking of modules and interface connectors so that they plug into the same plane, the designing of interconnections can be thought of as a two-dimensional problem. The wire wrap plate becomes a structural member of the overall package, with the capacity for as many terminals as required, spaced 0.20 in. apart on X and Y coordinates. The failure rate of termination is considered to be $\frac{1}{10}$ that of soldering, and the mechanical strength increases with age. The clean metal-to-metal contact and closely controlled wrapping forces produce reliable gastight terminations consistently. Although the equipment required to convert from conventional practices may impose a large initial expenditure, the rewards soon justify this investment. The time required to design and produce cable harnesses and point-to-point wiring, with due consideration for incorporation of changes, are very real problems to anyone in the electronics business. However, with short-term effort on the part of programmers, computers solve the wire routing with regard to third-dimensional build-up of lead density, etc. With computer logic routes now punched on cards, the wire wrap machine takes this information and interconnects the plate. As the requirement for production quantities increases, the machine repeats the operations dictated by the cards in less than two hours per plate, depending on its complexity. This automated method of interconnecting many terminations on a single surface also facilitates changes with hand tools while maintaining its consistently high-quality appearance.

Producibility

One of our greatest problems in the design of packaging systems for military applications is flexibility. Designs must not only have the capability of taking on increased design scope, but this must be accomplished without hindering production schedules. In any event, schedule slippage must be kept to a minimum.

The most significant feature of this design in terms of reducing schedule slippage lies in the attempt to restrict all of the logic interconnections to the assemblies that incorporate wire wrap. In the logic drawer that is discussed herein, there have been two exceptions to this basic ground rule. The first being the power supply cable and the second the front panel cable. However, in both cases, the complexity of the items has been reduced to its lowest practical level. Because of the inherent speed in which wire wrap programming and actual machine wrapping can be accomplished, changes in the logic flow diagrams can occur until the last stages of the drawer assembly process. Logic module assignments can be juggled until the final stages of assembly with only slight modifications to key codes and indexing post orientation. Last-minute changes to the wire wrap plates can be incorporated on the unused third level that is provided for this activity. The important factor is that changes do not affect the fabrication of modules, jumper cables, and hardware. Last-minute changes to the front panels, that are not readily incorporated, do not effect a hold on unit assembly. The front panel can be quickly detached at its pivot points and unplugged from its interconnection plate assembly without affecting other assemblies. A new panel can be fabricated, parts salvaged from the old assembly, and with minimum time loss a new front panel can be installed.

8065

Mechanical Design and Integration of a Microelectronic Tape Control Unit

J. MOORE, M. BERBERIAN, AND F. FEIGIN

Sylvania Electronic Systems; A Division of Sylvania Electric Products, Inc., Needham, Massachusetts

A prototype equipment has been developed which demonstrates a total concept in the application of a family of microelectronic circuits. Logic circuits have been designed for microelectronic application and specifically for the package configuration described in this paper. Unique tooling and construction techniques have been developed for the manufacture of the plug-in circuit module. Interconnecting wiring techniques, modular package nests and housing subassemblies, chassis, special tools, assembly and maintenance techniques, and environmental protection complete the total microelectronic packaging system concept.

INTRODUCTION

A FAMILY OF microminiature logic circuit devices has been developed by Sylvania to meet the requirements for the Navy Tape Control Unit (TCU). This unit interconnects Sylvania-built, militarized, high-speed, digital magnetic tape transports with current Navy shipboard computer systems. It supplies data buffering, device control, and timing for four tape handlers, and also provides for extensive tape handler evaluation tests under computer program control.

The Tape Control Unit will serve as a prototype equipment to demonstrate a basic hardware design featuring microelectronics. This total concept encompasses logic circuits designed for use in microelectronic wafers, a new type of plug-in wafer, and physical hardware, designed to function with any digital system, large or small, in the low-megacycle speed range.

The following text describes the construction of microelectronic circuit wafers and of the physical hardware which houses them.

THE MICROELECTRONIC PLUG-IN WAFER

General Description

The basic replaceable electronic element is the plug-in microelectronic wafer shown in Fig. 1. The external dimensions, in inches, of the package are 1.165 wide by 0.20 thick by 1.658 long including the connector pins, with a volume of 0.343 in.^{3} and weight of 0.25 oz. A 22-pin, double-row connector is attached as an integral part of the package.

These wafers are made by joining conventional but microsized active components (such as TO–51 case, transistors, and microdiodes) to thin-film passive components on an alumina base. This base gives rigidity, low and fixed capacitance, and excellent thermal conductivity to the circuit. Detailed fabrication techniques were presented at the Third Annual Packaging Symposium.*

* "Microcircuitry: An Approach to the Fabrication of Microelectronic Circuitry" by Franklin L. Feigin, Sylvania Electric Products, Inc., presented at: Third International Electronic Circuit Packaging Symposium, August 15–17, 1962, University of Colorado, Boulder, Colorado.

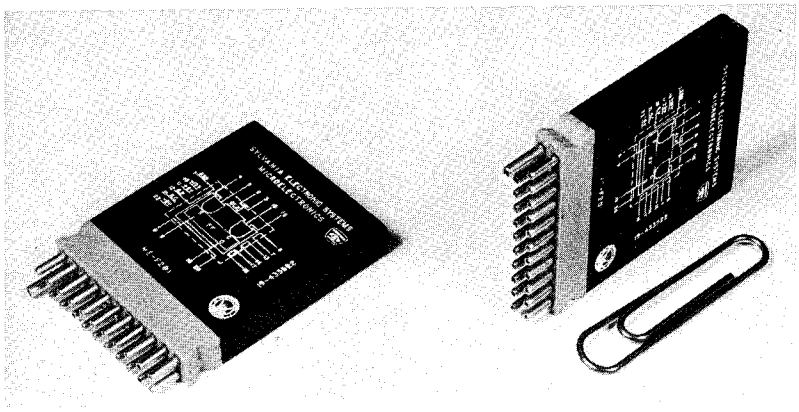

Fig. 1. Sylvania's microelectronic plug-in wafer.

The backbone of the wafer is a 0.020-in.-thick, high-alumina ceramic substrate measuring 1.125 in. square. The excellent mechanical, thermal, and electrical properties of this material provide a rugged, reliable product capable of withstanding extreme shock, vibration, humidity, and temperature. Thin-film conductive patterns on the active face are formed of a silver-glass frit, which is silk-screened onto the wafer and fired in place at a high temperature. High conductivity and bond strength obtained by this process result in reliable, low-loss conductors, suitable for applications up to the UHF spectrum.

Thin-film resistors are applied to the active face by vacuum deposition of nichrome through appropriate masks, and are preaged at an elevated temperature to ensure stability. Routine $\pm 5\%$ tolerances can be tightened to $\pm 2\%$ in special cases. The temperature coefficient of these resistors is nominally $+50$ ppm/°C, and their 1000-hr load life stability is better than 1%. Each wafer contains two to four transistors and other associated components and elements, to form the equivalent of a 40–50 component circuit. These components, either purchased or

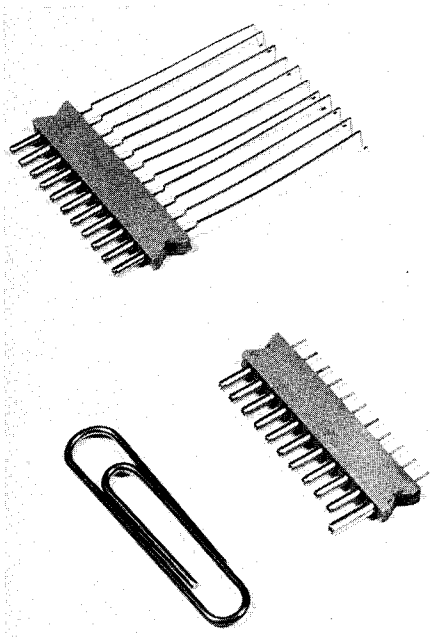

Fig. 2. Miniature connector used in microelectronic circuits.

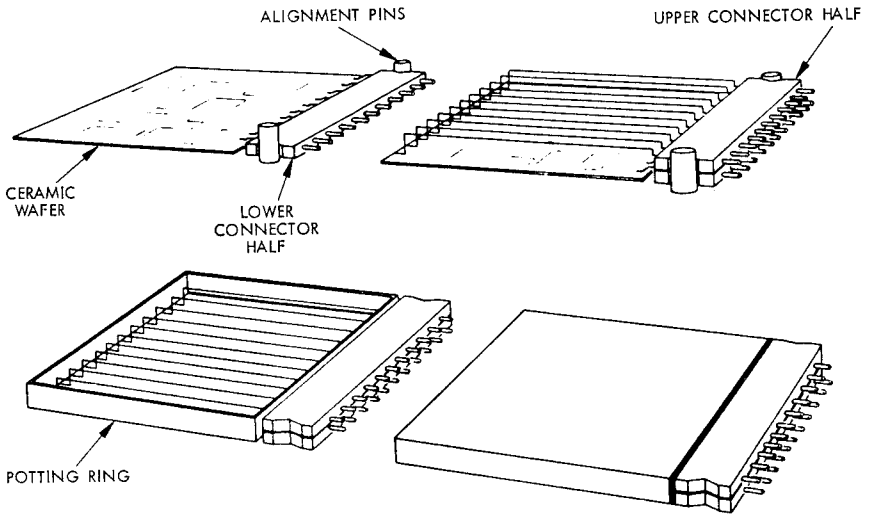

Fig. 3. Wafer assembly.

fabricated in microsizes, are attached to the active face by capacitor-discharge welding of their leads to suitable points in the silver conductor pattern. A wide range of component types is available, including ceramic and tantalum capacitors, flat spiral or ferrite toroidal inductors, thermistors, silicon transistors, and silicon diodes.

The terminal leads to the microcircuits are crimped to the pins of a conventional, but miniature, connector as shown in Fig. 2. The alumina base with the welded components is assembled with the predressed connector leads. Where desirable, soldering may be applied over the welded joints as shown in the illustrations. Figure 3 shows the following steps pictorially.

The electrically-complete ceramic wafer is precision-welded to the leads of the lower half of the connector. The upper connector half, with long leads, is solvent-bonded to the lower connector half, and its leads are welded to the ceramic wafer. The potting ring or shell is mounted on the wafer and epoxy-sealed in position. The upper and lower connector leads, which pass through precut slots in the potting ring, are epoxy-sealed; the connector is bonded in place during the same operation. The microcircuit is then given its final encapsulation, which consists of an initial flexible silicone layer followed by a final rigid epoxy layer.

The package now constitutes the basic physical as well as logical building block of the entire equipment.

Details of Fabrication

The previous discussion briefly explained the TCU microelectronic wafer in terms of its gross construction. It remains to examine in more detail the fabrication steps and fixtures required to manufacture the package. The fabrication methods and machinery described in last year's paper at this symposium will not be restated, except to give a brief description of the process steps leading to the automatic welding of components and the final protection of the circuit.

Thin-Film Process and Preparations for Welding. All of the TCU circuits are hybrid circuits using thin-film technology and welded components. Ceramic wafers of 96 % alumina are cleaned and inspected prior to use. Silver-frit conductor patterns are then silk-screened and fused to the ceramic substrate. Where connector insulation is required for subsequently welded-on components, an insulation layer of glass is screened and fired in position. The conductor-insulation patterns are then inspected and the wafer sent to the vacuum evaporator where resistors are vacuum-deposited. The resistors are inspected electrically and brought to value where necessary.

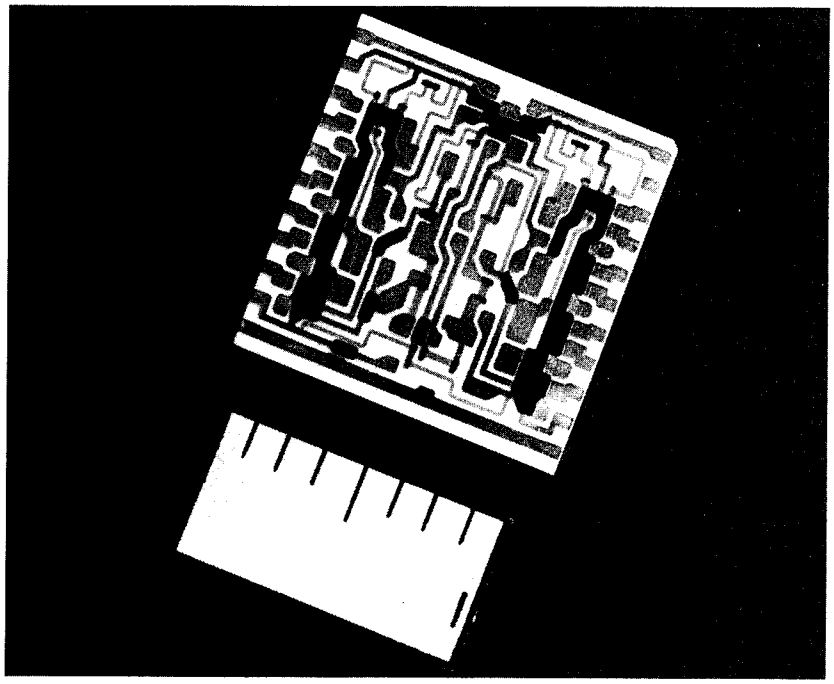

Fig. 4. Wafer with conductors and resistors only.

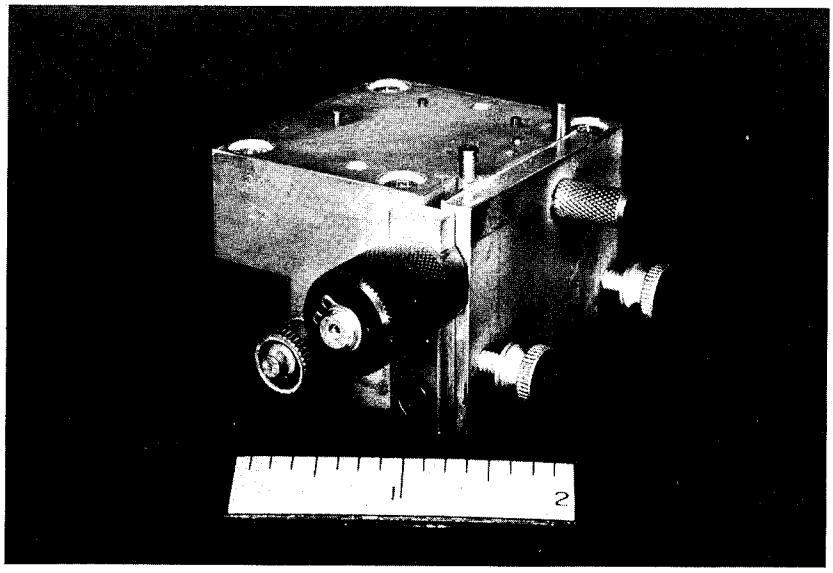

Fig. 5. Alignment block.

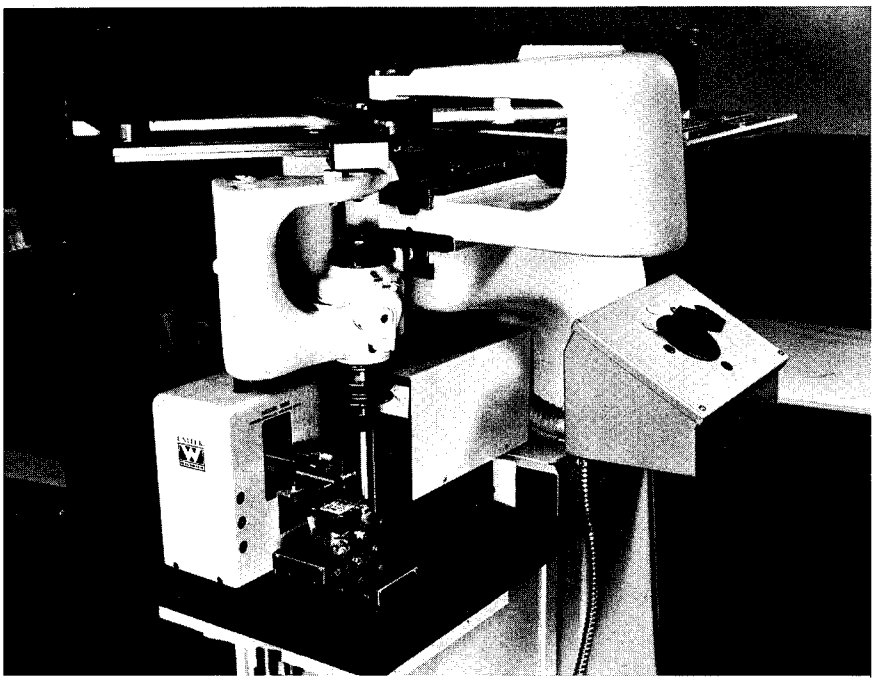

Fig. 6. Pantograph welder setup with alignment block.

Figure 4 shows a wafer with conductor and resistor paths in place. The gray areas are resistor patterns, and the black areas are glass conductor insulators. During this initial construction time, capacitors, diodes, and transistors to be welded into the package undergo a thorough electrical and physical check, and their leads are prepared for automatic welding by forming and shearing with precision dies.

The Alignment Block. A fixture was designed to facilitate handling of the ceramic substrate, after resistor deposition, through the rest of the fabrication cycle. This fixture, shown in Fig. 5, is designed to position the ceramic substrate accurately during component welding, connector and potting ring assembly, and final encapsulation of the finished package. The fixture or alignment block places the wafer precisely against two edges at 90° to each other, and holds it securely in place by vacuum. Two mechanical clamps shown in Fig. 8 retain the wafer when vacuum is removed or lost; the third holds connector halves in place. Figure 9 shows other clamps used in the potting and sealing processes.

The Block and Pantograph Welder. The alignment block is first used in conjunction with the pantograph welder shown in Fig. 6. A component locator of 10-mil beryllium copper is set in place above the wafer, and components such as diodes and transistors are loaded into precision-etched locating slots in the component locator. The pantograph welder is ready for operation with the mounting of the block in the welder. The welding electrode of the pantograph welder is connected through the pantograph linkage to a stylus. This linkage is preset at a reduction ratio of 10 to 1. The stylus tip fits in the holes of a predrilled metal template which is exactly ten times the size of the wafer. For accurate weld-point positioning, both wafer and template are constructed on the same X-Y coordinate pattern. Locating the stylus in one drilled template hole, or single weld point, fixes the welding electrode exactly on the

corresponding component lead. The weld is made by closing a switch mounted in the handle of the stylus. The stylus and linked welding electrode are moved to their next successive position and the process repeated. Since each component type can vary in lead thickness or material, provision is made for more than one weld cycle or setting. The welder is designed to handle five fixed weld settings and one variable setting. Each setting is color-coded, on the pantograph weld template and on the control knob of the machine, to conform to each predetermined heat cycle.

The Block and Welding of Leads. A special welding electrode was designed which will weld flat component leads as narrow as 0.018 in., with a 0.015-in. weld-spot diameter. Components are welded in place by color-coded weld groups, at a production rate of up to 3500 welds per hour. The lower connector is mounted on the alignment block and the connector leads are welded in position with the same technique. Upon weld completion, the alignment block is removed from the welder and the leads of certain components such as toroid coils, not adaptable to machine welding, are individually welded. The upper half of the connector is solvent-bonded directly to the lower connector, and held in exact position and registration by the alignment block. The long leads of the upper connectors are attached by means of an in-line welder shown in Fig. 7. A cam generates the step-by-step motion of the fixture-mounted wafer to bring each lead precisely under the welding electrode. The cam has twelve positions, one for each of the eleven welded leads, and a twelfth position for loading and unloading the alignment block. Provisions have also been made, by using a step block on the in-line welder, to weld both upper and lower connector leads for microcircuits not suited to automatic welding by the pantograph welder.

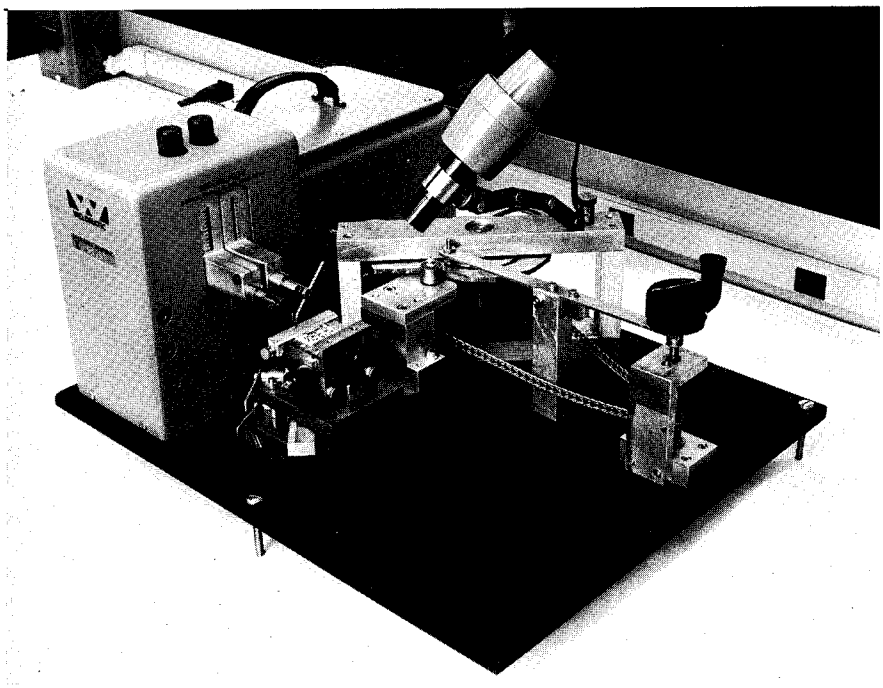

Fig. 7. In-line welder setup with alignment block.

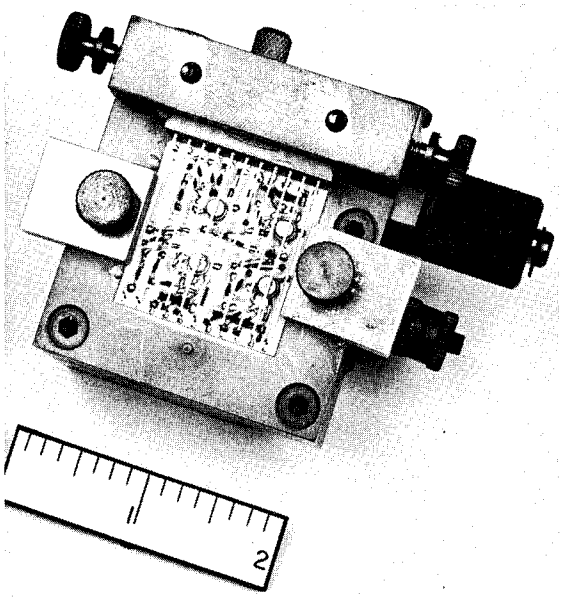

Fig. 8. Welded wafer mounted in alignment block.

The Block and Potting, Sealing. Figure 8 shows the welded assembly mounted in the alignment block. Figure 9 shows the same assembly with the potting ring epoxy-bonded in place and the block in position for sealing the connector to the potting ring. This bonding and sealing operation has been designed to take up any dimensional tolerance accumulations

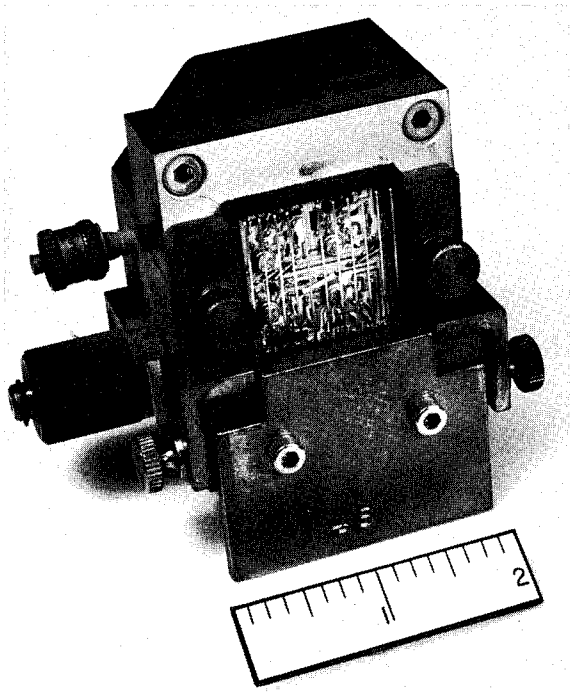

Fig. 9. Welded wafer with potting ring ready for sealing and potting.

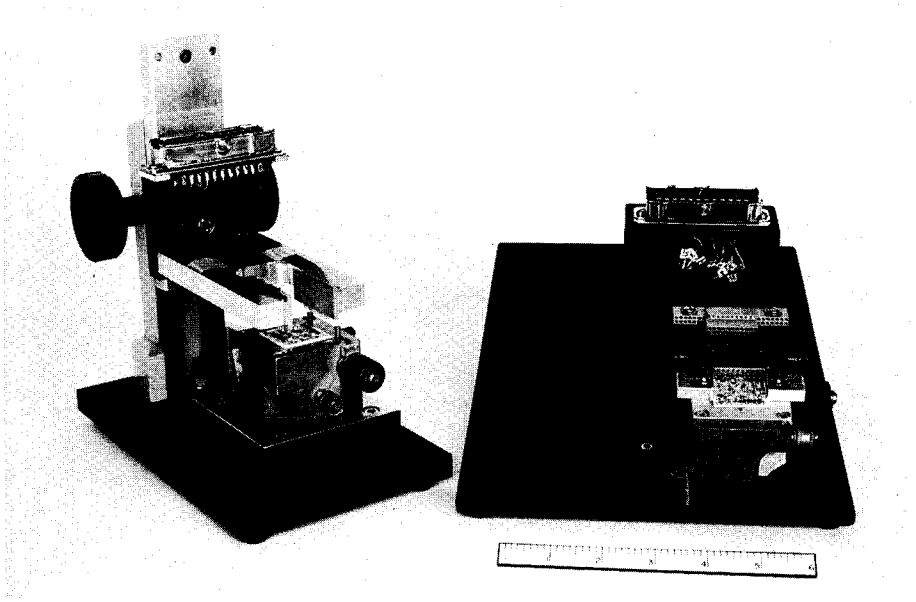

Fig. 10. Electrical test fixtures.

between the ceramic wafer, potting ring, and connector body, so that the final flat package dimensions are under reasonable control. The microcircuit is then removed from the alignment block prior to final encapsulation.

Encapsulation. Plastic encapsulation protection is obtained by embedding the electrical components inside the potting ring in a soft elastomeric silicone resin and by sealing the finished unit under an epoxy resin layer. This final epoxy seal is made to the sides and top of the potting ring; it provides a height-controlled, void-free, moisture-proof package.

The completed package is electrically checked, color-coded, and properly labeled as shown previously in Fig. 1.

Tests During Fabrication

The electrical test fixtures shown in Fig. 10 permit testing of the wafer on the alignment block at any stage of fabrication. Prior to attachment of the welded connector halves, electrical contact is made by spring contacts bearing directly on the metallic conductor pattern lands to which the connector leads are subsequently welded. At the assembly stage, where only the lower connector-half is welded in place, the lower connector engages a mating connector-half and spring contacts are used as before on the rear or unwelded metallic land areas. When both halves of the connector are welded in place, a standard mating connector is employed.

Qualities of the Microelectronic Wafer

The TCU microelectronic package readily lends itself to economical volume production. The basic package concept has been expanded into a family of various wafer sizes. Thin-film and hybrid microcircuit wafers can be packaged with this method, which is designed to employ effectively the advanced microelectronic circuit elements and construction techniques now under development by Sylvania.

PHYSICAL DESIGN OF THE TAPE CONTROL UNIT

General Configuration

Figure 11 shows the overall layout of the Sylvania Tape Control Unit which is designed as a slide mounted drawer. The left-hand section contains three hinged pages, and each page has a capacity of 360 plug-in wafers. The right-hand section contains the 60-cycle power supply and a small electronic package and waveform generator which is constructed of conventional printed-circuit boards because the components and power dissipation do not lend themselves to circuit wafer techniques.

The front panel is used for manual diagnostic purposes. It indicates and provides manual control over data which is transferred between the computer and the tape transport, instructions to the tape transport, displays tape status, displays errors in computer instructions and tape performance, permits manual control of block size, etc.

A cooling system is provided by a 60-cycle axial flow fan mounted at the rear of the unit so that air is drawn in through slots in the front panel, directed through the power supply and wafers by means of suitable baffles and gaskets, and exhausted at the rear of the unit. A single page containing six wiring modules, each of which will accept 60-circuit wafers, is shown in Figs. 12 and 13. Figure 14 shows a typical module with wafers in place.

Basic Wiring Module

The basic wiring module is shown in Fig. 15. Each row of circuit wafers is separated by a 0.100-in. spacer, which may be used for voltage or ground bussing, electrical test points, or interconnecting wiring terminal strips. As shown in Fig. 15, the five center spacers provide four voltage busses and one ground buss while the remaining spacers are used as test-point strips or terminal strips. All three types of spacers, the circuit wafer header, and the female connector body, which accepts the plug-in circuit wafer, are assembled from a standard family of molded receptacles and male and female contacts.

Figure 16 shows the three molded strips which differ only in height, and the location of an internal molded ridge or ring which secures the contact when it is inserted into the strip. Figure 17 shows the standard contacts. From Fig. 16, the type A strip houses the standard male contact and two type A strips comprise the receptacle for the plug-in circuit wafer. The type B and C strips are combined to create either buss bars or terminal strips in the following fashion: female contacts are soldered to strips of copper buss bar and then inserted into type C strips which captivate the contacts. This strip and contact assembly is then permanently mated with an empty type B strip, and when male contacts are inserted into the type B strip they make electrical contact with the bussed captive female contact and are captivated by the type B strip. Thus the main difference between a buss bar and a terminal strip lies in the number of common female contacts; i.e., in a buss bar all contacts are common and in a terminal strip any arrangement of common contacts may be used. The present equipment terminal strips utilize sets of two common contacts in the terminal strips.

With reference to Fig. 17, both the male and female contacts are captivated by means of molded-in rings or ridges in the Lexan strips or bodies. The contacts are forced through the rings, and the Lexan, having both resilience and memory, deforms to allow the contact entrance, and then contracts into the recessed collar in the contact exterior to captivate the contact. The female contact is a simple hollow tube and the male contact is formed of two beryllium copper wires shaped into four bowed segments at 90° to each other, spot welded at the tip where all four segments meet, and then crimped into a copper barrel. Two number 28 AWG wires can be accepted by the copper barrel for crimped backwiring. Both types of contacts are gold-over-nickel plated.

Wiring Sequence

From Fig. 15 again, the first level of backwiring commences at the basic 60-wafer module level with the insertion of the voltage and ground runs. These runs go to preassigned pin positions which are standard throughout the unit (see Fig. 18). Approximately 60% of the backwiring is accomplished at this level.

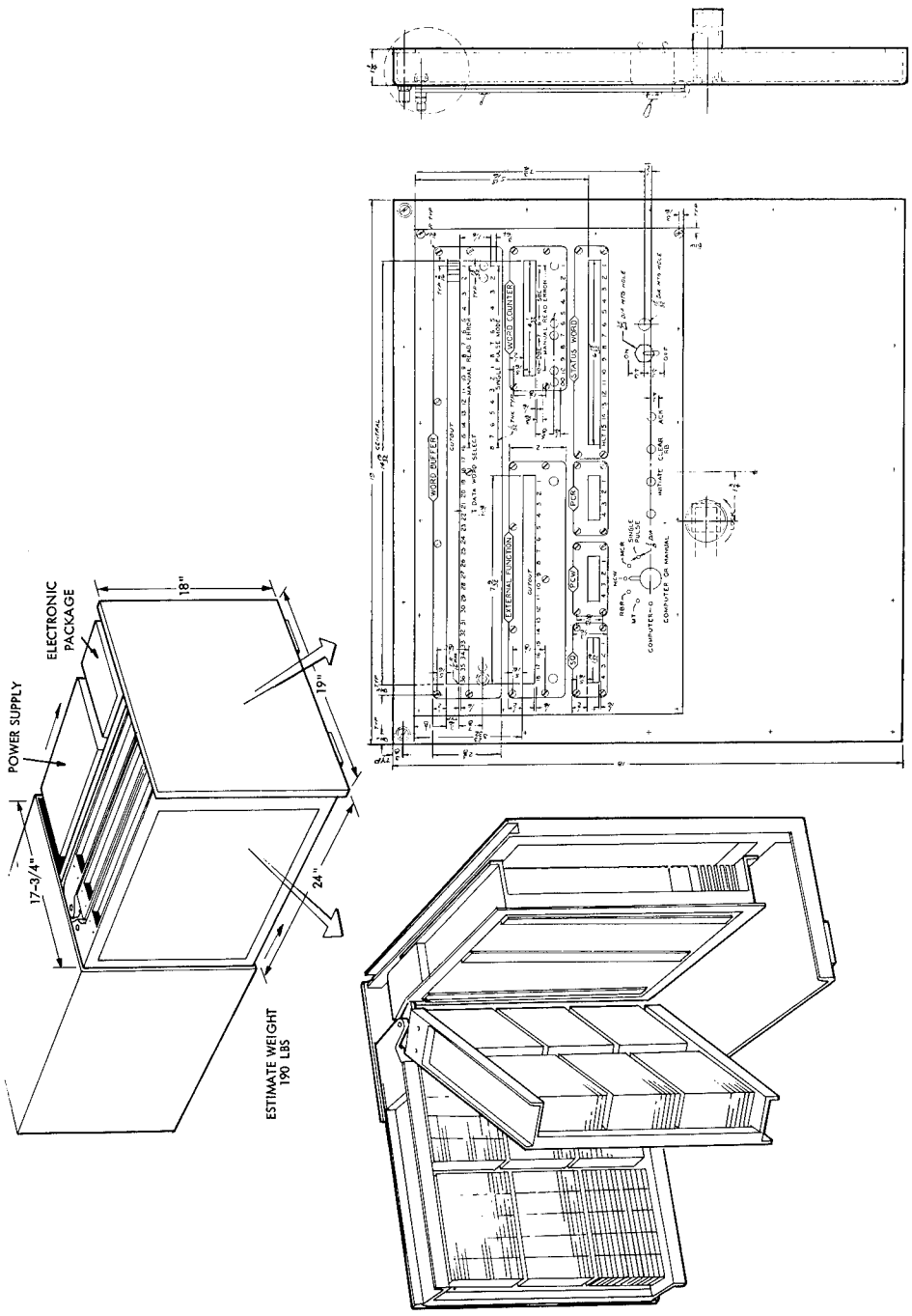

Fig. 11. Overall view of Tape Control Unit.

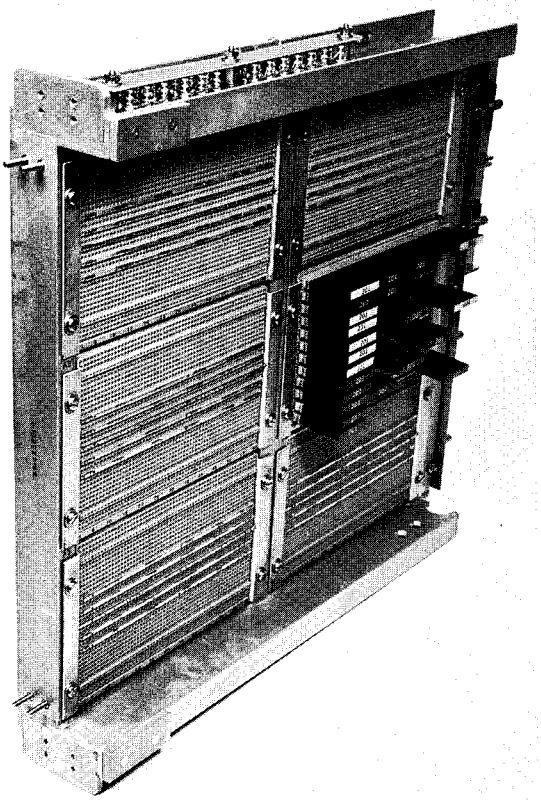

Fig. 12. Page—wafer side.

The long polarizing guide shown in Fig. 18 is also a ground pin. It is the last pin to lose contact on wafer extraction and the first pin to make contact on wafer insertion. This is a precaution against the possible reverse biasing of transistor emitter junctions and polarized capacitors which could occur with the improper sequencing of voltage application to the wafer.

All wiring runs are preassembled as a string of wire and contacts as shown in Fig. 19. One of the primary reasons for using crimp-type "poke-home" contacts is to permit the fabrication of such preassembled wire runs prior to insertion of contacts in the wiring module. These preassembled runs provide a practical means of hand-assembling point-to-point wiring on 0.100-in. centers. All backwiring utilizes the male connector because it is more fragile than the female, and in the backwiring application is always accessible and replaceable in the event of damage. The female pins are more rugged and are therefore used in the circuit wafers and buss bars for greater permanency. Test points are actually standard female contacts while the test-point probe is a slender insulated probe with a 0.050-diameter solid tip.

The second level of wiring is performed when the prewired modules are assembled to the page and interwired. Because all leads leaving a module are terminated at a terminal strip within the module during first-level wiring, there is no occurrence of uncrimped, dangling leads which must be joined and terminated at the intermodule wiring level. Therefore, this wiring is also accomplished using preassembled, precrimped strings.

Interpage wiring is the third wiring level and is accomplished through connector strips mounted to each page. All wiring leaving the page and going to or coming from any other page is brought to these connectors. The mating half or hinge side of the interpage wiring is

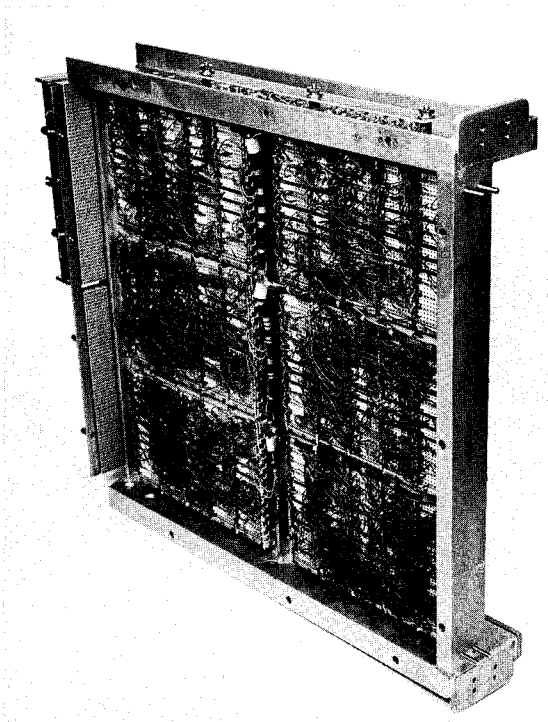

Fig. 13. Page—wiring side.

preassembled in the form of short, flat, flex-loops, each of which contains two loops and carries three of the mating connectors shown in Fig. 20. When the pages are connected to the hinges the flex-loops are installed, and all interpage wiring is accomplished through these simple, removable harnesses.

At the final wiring level, DC power, and all signal communications with the front panel and chassis level connectors are brought directly to the pages by small harness flex-loops. This wiring level is separated from the interpage wiring in order to preserve the simplicity of the interpage flex-loops.

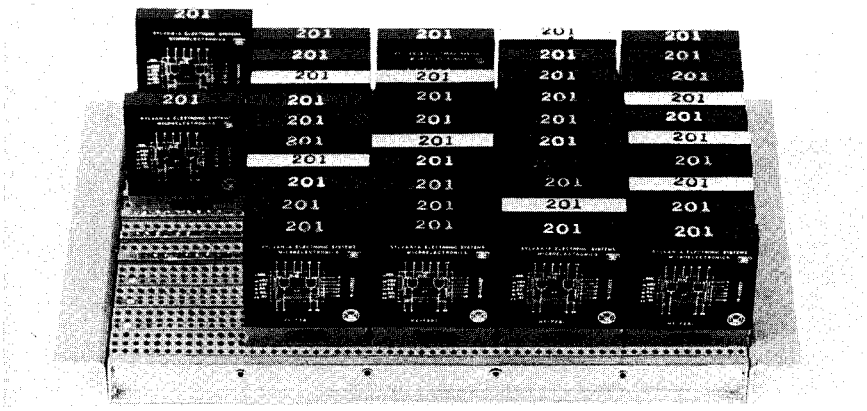

Fig. 14. Typical Sylvania module.

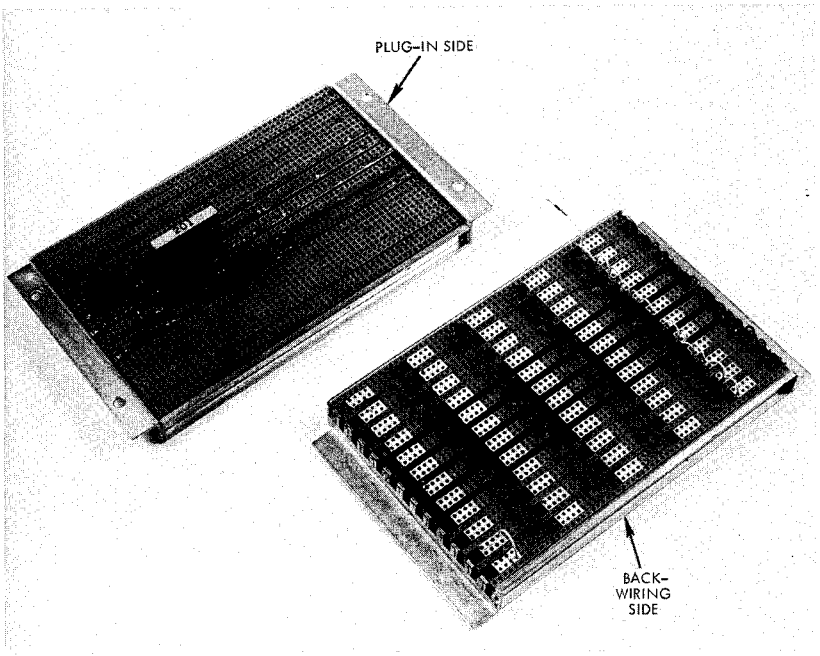

Fig. 15. Basic module.

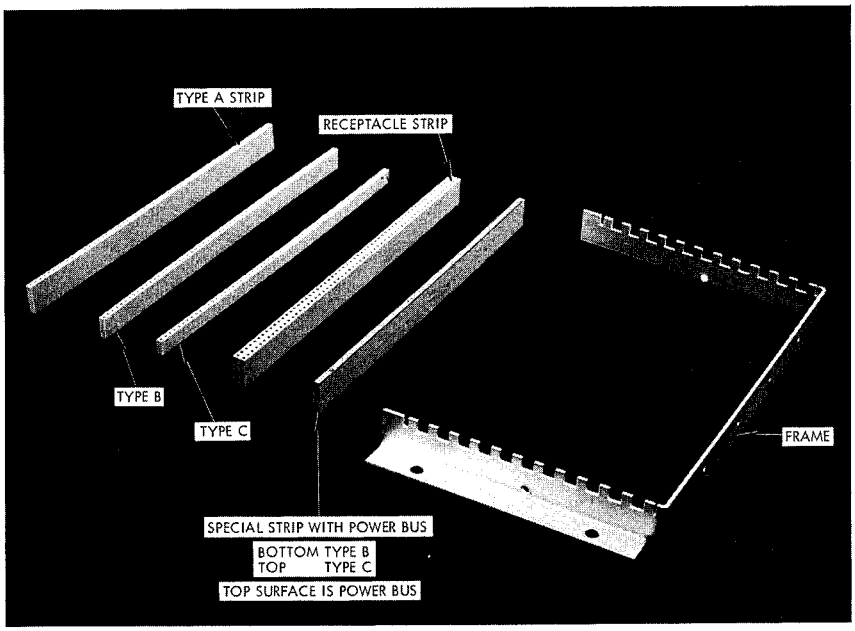

Fig. 16. Module elements.

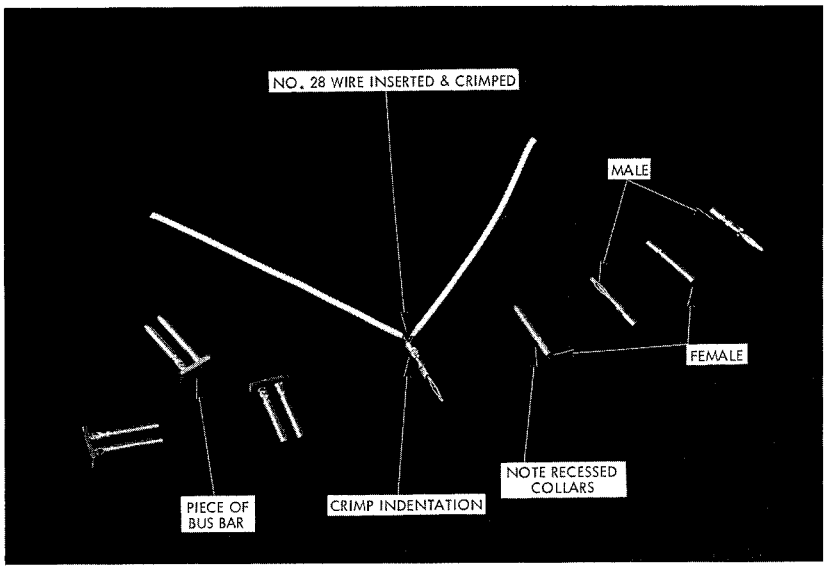

Fig. 17. Contact details.

Maintainability

Access to circuit wafers for removal and replacement, and to electrical test points and backwiring for check-out, is achieved by sliding the chassis from its rack mounting and opening the hinged pages. In this fashion all circuit wafers, wiring, and test points are exposed and accessible while the equipment is operating. Circuit wafers may be removed and reinserted

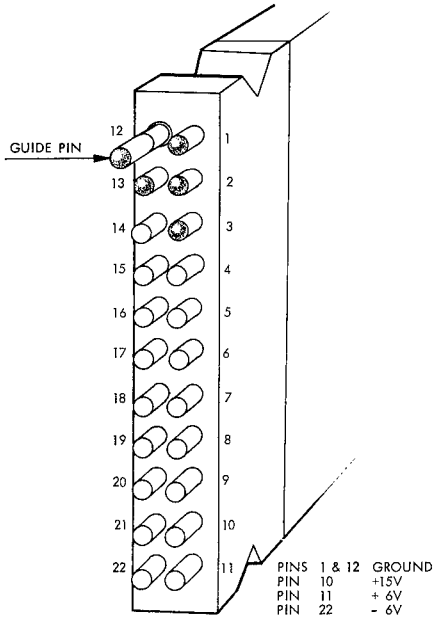

Fig. 18. Standard wafer pin arrangement.

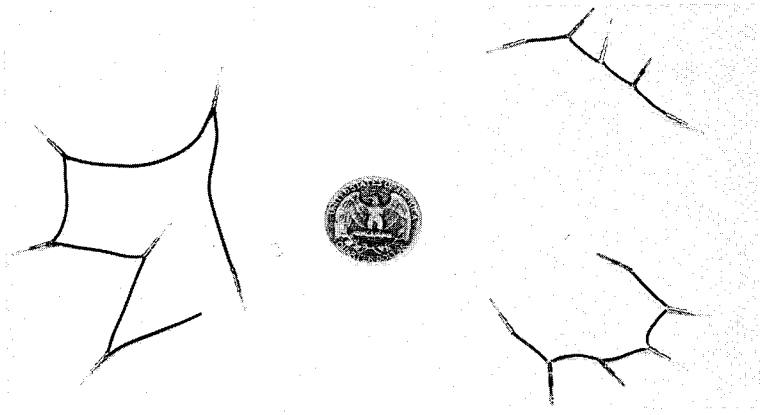

Fig. 19. Preassembled wire-contact string.

while the equipment is operating. The ease of circuit wafer replacement has a beneficial effect upon mean time between failure calculations in that it represents a high availability factor and minimizes downtime in the determination of fault location and its repair.

A wafer extraction tool (Fig. 21) has been designed to simplify insertion and withdrawal of a wafer from the module. This tool is constructed of two, 0.025-in.-thick corrosion-resistant

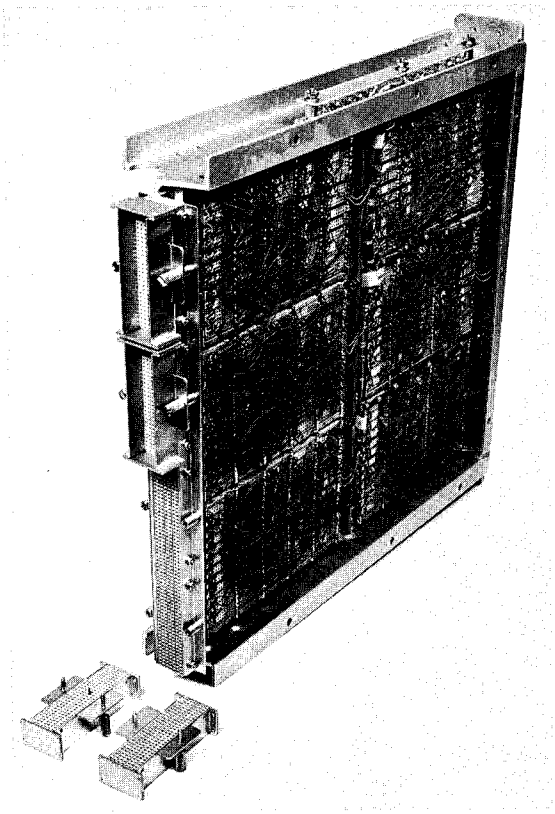

Fig. 20. Connectors for interpage wiring flex-loops.

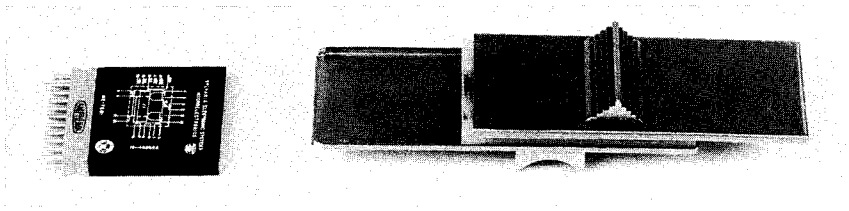

Fig. 21. Wafer extraction tool.

steel plates separated by a nylon block. One plate is fixed to the block and provides the gripping action on the wafer connector header. The second plate is a sliding member which encloses the wafer in the tool. For ease in manipulating the tool with one hand, finger and thumb rests are attached to the side plates. In the process of insertion or withdrawal, the wafer is completely enclosed by the plates and is gripped at the two notches on the wafer header. This technique ensures that no stresses will be placed on the wafer proper. The tool can be used to insert and withdraw a wafer from anywhere within the 60-wafer module without interfering with other wafers or the wiring. Its overall dimensions are $3\frac{3}{8}$ in. long by $1\frac{1}{4}$ in. wide by $\frac{1}{4}$ in. thick.

The unit is readily disassembled to the page level to ease manufacture and repair or change, and all backwiring is installed sufficiently slack to accommodate at least two additional stripping and crimping operations in the event of change or damage repair. After all wiring is in place contacts are reasonably accessible for probing or repair. This access is the result of judicious location of circuit wafers to effect a compromise between functional circuit considerations and minimizing wiring build-up.

Design Flexibility

Due to the building block design features, expansion or contraction of the system size is readily accomplished through varying page size and number, or utilizing any desired frame while employing the same wiring modules and interconnection techniques. The wafer fabrication techniques previously described lend themselves to a variety of circuits and choice of actual components, thus facilitating their application to the special circuit requirements needed to complete a system. In the case of the TCU, examples of these special requirements are given by the interface or matching circuits.

Since the present unit is a developmental model, the facility to make wiring changes and modify circuit wafer arrangement is very important. This is the primary reason for using hand-assembled point-to-point wiring, which provides easy access to all wiring, test points, and circuit wafers. It might be observed that overall packaging density has been allowed to suffer in order to maintain a high degree of accessibility. The logic behind this decision is that ease of access for any desired modifications, including the addition of more circuits, is more important at this stage than achievement of a maximum package density. In effect, the purpose of the present unit is to provide a usable end product with wide applicability while utilizing the developing techniques of microelectronic circuit wafers.

Environmental Protection

Two parallel cooling airflow paths are used, one for cooling the circuit wafers, and the other for cooling the power supply and electronic package. The total dissipation of the wafers is 235 W and the anticipated temperature rise of the air from inlet to exhaust is approximately 21°F. The cooling blower has a capacity of 400 cfm at $\frac{1}{4}$ in. H_2O pressure; and final air distribution in the unit will be accomplished through experimental balancing. When the pages are closed, a sponge rubber pad presses on the top of the wafers securing them for shock and vibration protection. This creates a baffle to channel the airflow between wafers. While the pages are closed the wafers and power supply receive proper cooling whether or not the drawer is withdrawn from its enclosure. The environmental conditions which the unit is designed to meet are:

Temperature	
Nonoperating	−62°C to +75°C
Operating	+25°C to +50°C
Humidity	95% R.H.
Vibration per MIL-STD-167 Type I	5 to 33 cps 0.010 in. amplitude
Shock per MIL-S-901B	Three blows each of 3 planes—total of 9 blows Hammer height—1 ft, 3 ft, 5 ft.

Preliminary Tests

To date preliminary tests have yielded the following facts:

1. Individual wafers have been operated continuously for several hours in the temperature chambers without forced air circulation at ambient temperatures of 90°C with no circuit deterioration. Wafer tests also have been run under the same conditions for shorter periods at 175°C. It has been determined that the circuits are capable of continuous operation at 125°C.
2. Individual page assemblies, loaded with a combination of dummy and active wafers, have been subjected to vibration and shock tests, with no harmful resonances or resultant damage to either the structure or wafers. Active wafers suffered no deterioration in performance characteristics as a result of test.
3. Individual wafers have successfully withstood the environmental conditions listed, but of even more importance, they successfully withstood such handling tests as a 3-ft drop to a concrete floor. Such a test condition is considered to be most realistic.

A study is now scheduled to determine whether or not adequate cooling may be achieved by natural convection with the cooling paths oriented either vertically or horizontally. It should be noted that the present configuration is adaptable to cold-plate cooling or radiation cooling. With either of these cooling techniques, spring-loaded metallic fins would protrude into the void between circuit wafers making intimate contact with the wafer faces. A coolant would then flow through the fins, or in the case of radiation cooling the fins would terminate in a radiator or heat sink.

SUMMARY

The total packaging system described in this paper represents an initial step only in the practical application of microelectronic circuit techniques. An outgrowth of the work described is the current development by Sylvania of microelectronic circuits of a higher order of sophistication than the logic circuits used in the TCU. Construction technology will soon be available for producing not only hybrid circuits but complete thin-film circuitry on glazed ceramic wafers utilizing deposited thin-film conductors, resistors, capacitors, diodes, and transistors. The basic TCU package described will accommodate both the hybrid and thin-film circuit construction techniques.

8066

Interconnecting Complex Miniature Electronic Systems

R. C. FRANK AND R. E. KALFAYAN
Advance Missile Technology, Douglas Aircraft Company, Santa Monica, California

The advantages of what have come to be known as matrices in interconnecting complex electronic units or systems are well known. As systems have decreased in physical size, while increasing in electrical complexity, matrix fabricating techniques have required refinement. Design and construction details utilized in building a variety of closely spaced matrices will be discussed and evaluated in this paper, leading to the conclusion that these devices can be manufactured economically in a number of ways, depending on the facilities and capabilities available in the particular organization involved.

INTRODUCTION

AS ELECTRONIC SYSTEMS increase in complexity and decrease in physical size, the problems of interconnecting modules or circuit assemblies within the unit or system become more difficult. In digital systems, where entire circuits now occupy less volume than a single miniature component required two years ago, this situation becomes critical. Fortunately, the assembly of significant numbers of functional circuits in a single large module, or circuit assembly, is gaining wide acceptance. This change helps to keep the interconnection problem within reasonable bounds, even though a ten-to-one reduction in interconnection area is frequently required.

In the past, the standard method of interconnecting modules or circuit assemblies was through the use of connectors. The connectors were interconnected with point-to-point wiring, and the circuit assemblies were inserted into friction contacts which completed the system. Figure 1 shows the wired side of a typical point-to-point connector system. The interconnecting wires in this case are secured to the connector terminals by wire wrapping on 0.2 in. centers, a technique which is widely accepted. Our problem evolves when it becomes necessary to make these same interconnections on $\frac{1}{16}$ in. centers, and to build the system to withstand airborne, missile, or space environments.

It might be well to consider at this time the advantages of the connector, point-to-point wired combination. The system is very flexible in that wiring changes are easily made. Circuit assembly replacement is convenient, requiring only the withdrawal of the defective unit and the insertion of a replacement. The system has wide acceptance, making hardware, tooling, and production relatively inexpensive. It should be mentioned, however, that connectors are frequently the major causes of system unreliability, a condition which tends to be emphasized as the devices are miniaturized and subjected to adverse environments. In systems where reliability is of paramount importance and repair is difficult or impossible, a more reliable (if less flexible and maintainable) interconnection system is worthy of consideration.

The interconnecting systems which have gained favor in recent years are prewired systems. That is, electronic circuit assemblies when properly connected into the prewired interconnecting

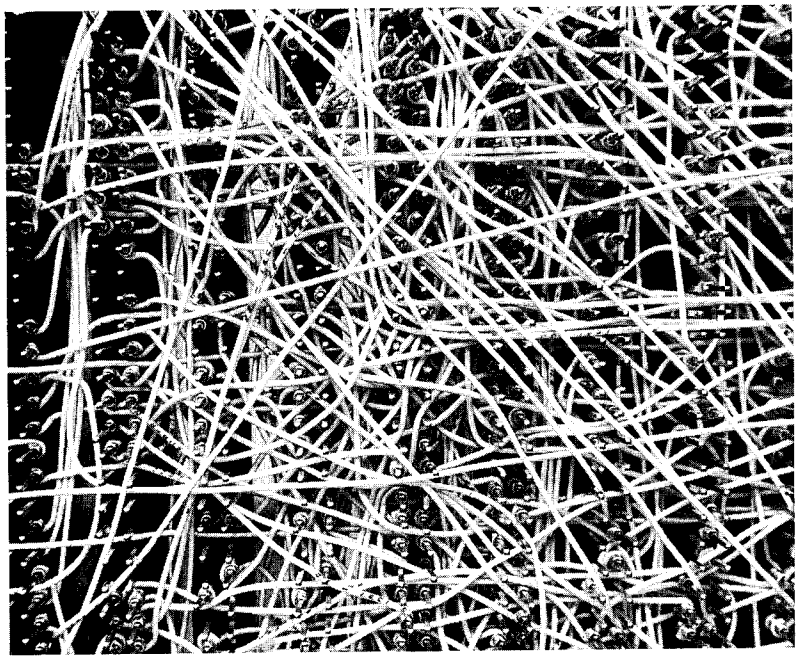

Fig. 1. Typical wire wrapped connector system.

system are, by virtue of the prewiring, interconnected as a system. The interconnecting system incorporates the function of the connectors and the connector point-to-point interwiring within a single block. These interconnecting systems, which are referred to as matrices, have taken a wide variety of forms.

Although this paper will not discuss interconnecting systems which include connectors, it will be evident that connectors can be used in place of the solid connections, thus gaining back the ease of maintenance at a sacrifice of reliability.

Generally, matrices are flat sheetlike devices. The circuit assemblies, which the matrix interconnects, are mounted on, or adjacent to, one flat side of the matrix. The circuit assembly leads extend through holes in the matrix and are available on the side opposite the circuit assemblies for attachment to the appropriate leads of the matrix as shown in Fig. 2. In some cases the matrix has also been considered a structural member.

In order to indicate the degree of complexity under discussion it should be pointed out that the systems which will be discussed have been used in making interconnections on a grid 0.065×0.090 in. It will be evident in the discussion that this grid is by no means a limiting parameter and that, in fact, these same techniques are applicable through further refinement to much smaller grid spacings, should these be required. No effort will be made here to enumerate or discuss all the possible prewiring systems which can be applied to interconnect complex systems. Instead, a number of systems will be discussed in some detail, in an effort to indicate that there are numerous available solutions to the problem, and that it remains only to select one which is particularly applicable to a situation, and practice it.

Choices can be made in several areas in regard to prewired, or matrix, interconnecting systems:

1. Connection between the circuit assembly and the matrix can be made in several ways, e.g., welding, soldering, or wire wrapping. Even in a system where maintainability has

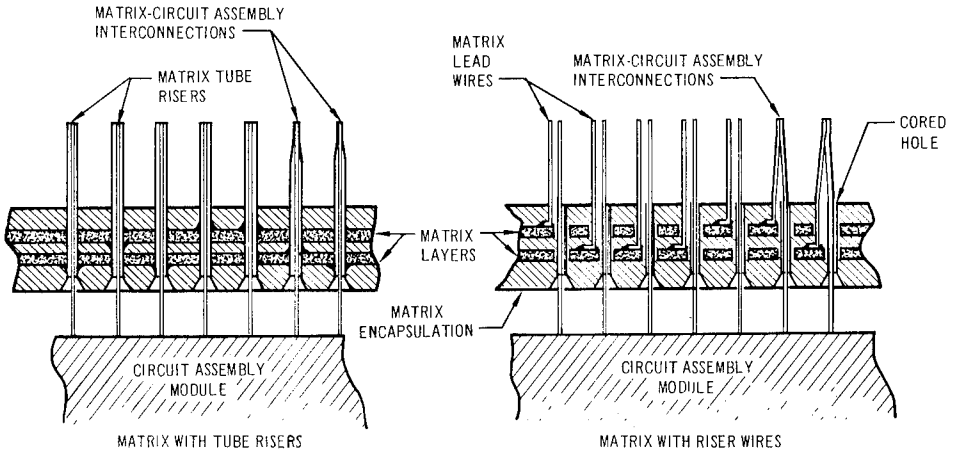

Fig. 2. Cross section through assembly of a circuit assembly and matrix.

been sacrificed for reliability, maintenance is required. Provision must therefore be made in each of the above cases for disconnecting the circuit assembly without destroying the usefulness of the matrix.

2. Leads can be brought from the matrix for connection to the circuit assembly in a number of ways, including pads, flush with the matrix surface, tubes, through which the circuit assembly leads extend, pins or wires, immediately adjacent to cord holes through which the circuit assembly leads protrude, or pins or wires placed at some distance from the circuit assembly leads. In the latter case, bridging devices are required to effect the circuit to matrix connection.
3. The prewiring within the matrix can utilize various techniques, such as standard printed circuits, multilayer printed circuits, welded wires, and weldable printed circuits.

The preceding list is not complete and is offered only to indicate the wide variety of options available. Each of the choices listed offers advantages and disadvantages. It is apparent that, unless a mutually acceptable method of weighting these factors is arrived at, agreement is unlikely on a "best" system.

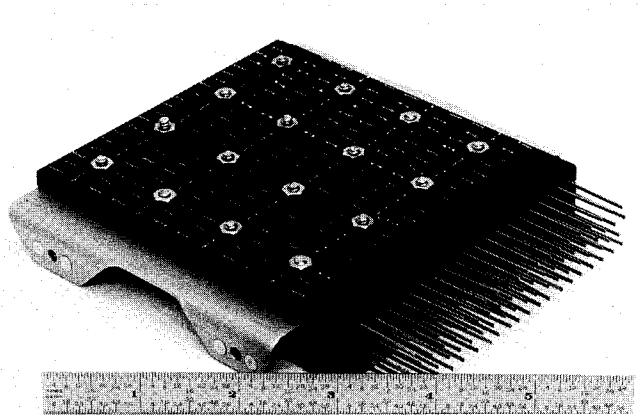

Fig. 3. Matrix-circuit assemblies bridge connected.

In the past, where matrix connection density was not high, circuit assembly leads were brought through the matrix at some distance from the matrix leads. Connection between the two leads was made in a bridging operation, as shown in Fig. 3. This system makes replacement of circuit assemblies relatively easy. As the grid becomes tighter, however, it is necessary to abandon the bridge because of the space it consumes and to place the circuit assembly leads immediately adjacent to the matrix leads or to bring the assembly leads through the matrix leads, where tubes or pads are used.

Four kinds of interconnecting systems have been designed and fabricated in this program. A fifth system, which is commercially available and is widely used, will also be discussed.

SOLDERED PRINTED CIRCUIT MATRIX

The first system utilizes double-sided printed circuit boards to which 0.025-in.-O.D., 0.020-in.-I.D. "A" nickel tubes are soldered. The tubes which have been found best suited for this work are soft-annealed. Although the soft tubes present a handling problem in that they are easily crushed, they are more durable than hard tubes since they can withstand a degree of bending.

Design ground rules for use with this system include use of 0.015-in.-wide lines, spaced midway between tube risers. The nominal clearance between line and tube is therefore 0.012 in. It has been found desirable from the point of view of space utilization to use offset solder pads which do not provide a solder joint around the entire periphery of the tube. This departure from accepted procedure has not caused difficulty. The solder pads are oriented with respect to the tubes in such a manner that all the connections are made from the same direction. In this manner, the tubes are inserted a line at a time and soldered into position using a standard small soldering iron.

The circuit lines of any one circuit in the matrix (e.g., the ground circuit) are placed on one side of a board only. This practice eliminates the necessity of communicating between opposite sides of the board, although it might also require the use of additional boards in particular cases. It is never necessary to connect any tube to both sides of a board or to more than one board.

Since the tubes from each layer of the matrix pass through the entire matrix, clearance holes are provided in all the boards. In soldering the tubes into the boards it is necessary to exercise care to maintain tube position accurately so that the mating of the matrix layers can be readily accomplished. A thick block with accurately spaced clearance holes holds the tubes in proper position during the soldering operation. When this operation is performed with care the several layers of the matrix can be mated without other special tools, in spite of the fact that several hundred tubes are involved.

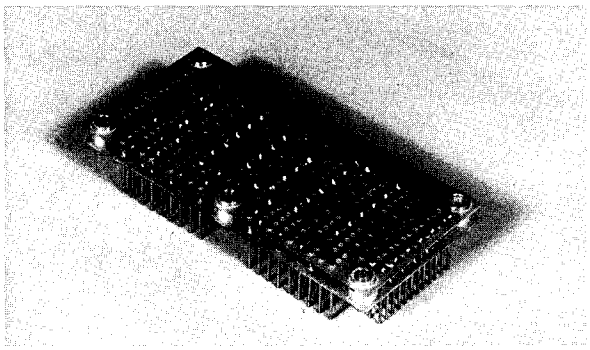

Fig. 4. Soldered printed circuit matrix.

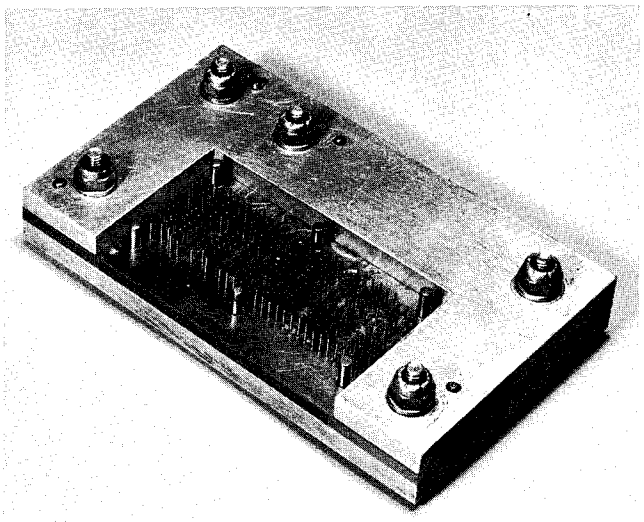

Fig. 5. Matrix assembled in encapsulating mold.

The finished layers of the matrix are mated, spaced apart, and encapsulated. Figure 4 shows a matrix prior to encapsulating. The spacers which are placed around the periphery of the encapsulation also provide holes for mounting the matrix at final assembly.

Encapsulation in epoxy resin requires a four-piece mold, as illustrated in Fig. 5. The back plate of the mold is a flat plate. The front plate is appropriately holed to accommodate the many tubes. The holes are loose enough to provide ease of assembly and are countersunk on the inside of the plate. A seal is effected around the individual tubes using latex. The rear side

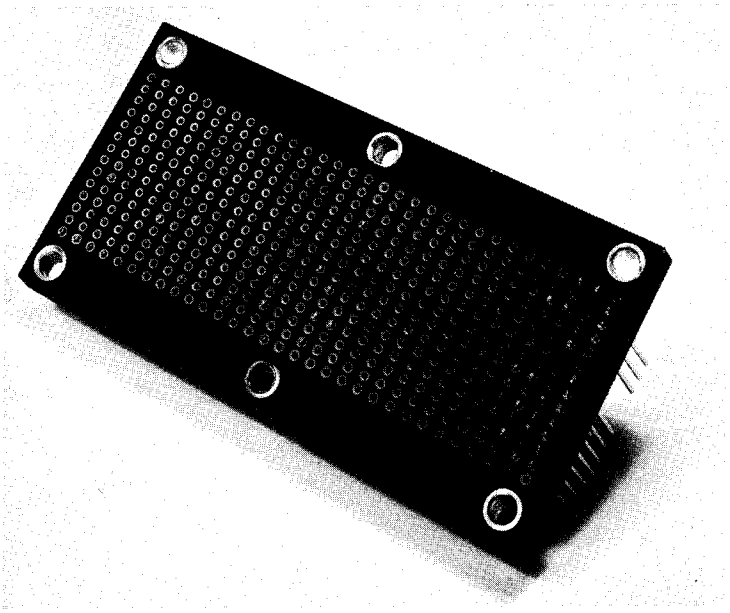

Fig. 6. Finished matrix—rear view.

of each tube is also sealed with latex before the assembly is placed in the mold. A poor seal in either place, particularly at the rear of the tube is a disaster. Fortunately, the seals are not difficult to make, but care must be exercised. Preheating of the mold and the resin is very helpful in making void-free encapsulations. It is sometimes required that holes be cored in the matrix in order to bring a circuit assembly wire through for connection beyond the matrix. In this case a solid core, coated with a suitable mold release, is cast in place, like a tube. The cores are removed before the encapsulation is removed from the mold.

After encapsulation the seals at the rear surface of the matrix are removed and each hole is countersunk, as shown in Fig. 6, to simplify the mating of the circuit assemblies to the matrix. An advantage of this kind of matrix assembly is the fact that it can be made from simple printed circuit boards with standard tools and very simple fixtures.

PARALLEL-GAP WELDED MATRIX

A second interconnection assembly can be made using very similar techniques, but substituting welding for the soldering process. Recent improvements have been made in what is now called parallel-gap welding. This type of welding makes possible the welding of flat ribbon leads (or any other shape) to printed circuits. It is desirable, but not necessary, that the printed circuit be made of a high-resistance material, such as nickel or a nickel alloy, and that the wire welded to it be of similar material. Nickel laminates are becoming available and can be processed using standard etching techniques.

Printed circuits can be designed using the same criteria mentioned in the first system discussed, except that there is no reason to provide a pad of any kind. It is advantageous to have the etched conductors of a standard width in order to eliminate a welding variable. Variations in the sequence of welding this assembly are possible; a system which has been found very workable consists of first welding a nickel wire lead, either flat or round, to the soft nickel tube. The axial position of this weld is controlled, which in turn controls the position of the tube with respect to the printed circuit later on.

Welding to soft, thin-walled, nickel tubes is accomplished by filling the tube with a snug fitting solid mandrel. Tungsten has been found to make a satisfactory mandrel which does not weld to the inside of the tube nor crush because of the heat and pressure of welding. A standard capacitor-discharge welder which is now found in most electronic manufacturing facilities is used. The tubes are then placed in the holes of the printed circuit board and the same predrilled block that was used in soldering the first matrix. The junction is welded using the parallel-gap method.* An assembled unit is shown in Fig. 7. From this point onward, assembly proceeds as it did with the first matrix.

Had the decision been made to use a wire riser out of the matrix, a hooked wire could have been welded to the board and the second weld eliminated. The tube riser is used because it simplifies the encapsulating process. To use straight wire matrix leads requires that the matrix be cored adjacent to each riser.

If straight wires had been used, individual cores would have been used with the printed circuit board holes providing alignment. Drilling would be impractical because of the small hole size and close tolerances. Likewise, it is felt that to use a plate to which all the cores are attached would be difficult since in this case keying, due to misalignment, would be inevitable.

Again, this second kind of matrix requires a combination of printed circuit and welding knowhow. Most companies in the electronic industry possess capability in both these areas.

WELDED PRINTED CIRCUIT MATRIX

A third type of matrix, similar to the second, can be made by using printed circuits, which are made usually by a transfer process of some kind. The printed circuit portion of the matrix

* Parallel-Gap Welding, (SP22-A62), by Richard P. Bywaters, Integrated Circuits Engineer, Space Systems Department, Texas Instruments, Inc., Apparatus Division, 6000 Lemon Avenue, Dallas 22, Texas.

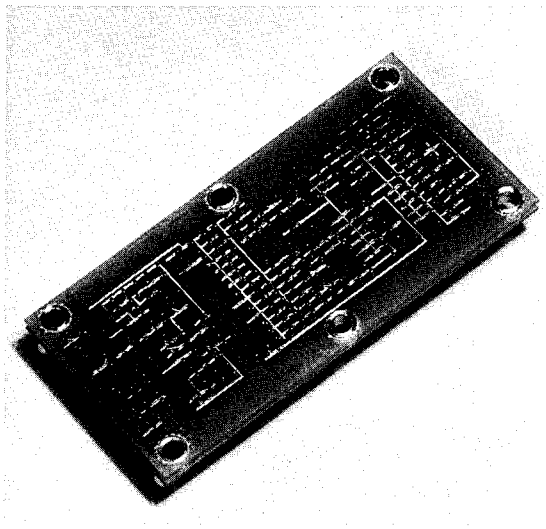

Fig. 7. Parallel-gap welded printed circuit matrix.

is made to incorporate the hook to which the riser tube is welded. Since these circuit boards and the circuits themselves are rigid, it is convenient to nest the series of boards with their short risers extended from the nest in one direction. The tubes are then inserted in lines, and welded using an assembly block for alignment. A tungsten mandrel is used in the tubes. For convenience, the welding is done on the short end of the tubes. Figure 8 shows the assembly ready for welding and welded ready for encapsulation.

The kinds of printed circuits required to build the third kind of matrix are beyond the immediate capability of many electronics companies, but they are available commercially and additional organizations are becoming interested in their production. The circuit boards used in this program were purchased.

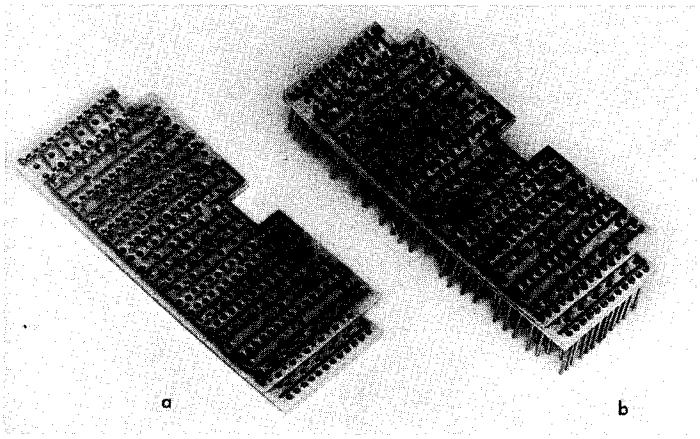

Fig. 8. Special printed circuit welded matrix: (a) nested for welding, (b) with tubes welded in position.

MULTILAYERED PRINTED CIRCUIT MATRIX

The fourth kind of interconnection assembly is the multilayer printed circuit board which has become readily available during the past year. This device is gaining wide acceptance both for interconnecting circuit assemblies and for making the circuit assemblies themselves.

Details of manufacture of the multilayer printed circuit boards vary from company to company. One or more companies can furnish boards with risers which extend above the board's surface in the form of tubes to which circuit assemblies can be welded. If longer risers are desirable they can, of course, be soldered in place. Additional rigidity can also be supplied by encapsulating.

The multilayer printed circuit boards that are used as interconnecting matrices generally have flush pads similar to those provided on standard printed circuit boards. Connection is made to the assembly by soldering, although parallel-gap techniques make welding possible. When a circuit assembly which has thirty leads must be removed from a board it is necessary to unsolder all thirty leads at one time or to remove the solder from the joints as they are unsoldered one at a time. Special tools are required in either case, but this is certainly a condition which can be tolerated. Several companies have made assemblies with grids considerably finer than the 0.065 × 0.090 in. grid used in the matrices discussed.

It is felt that this fourth, like the third, kind of matrix requires more specialized process and fabrication knowledge than many companies possess.

WELDED WIRE MATRIX

The fifth matrix design is the strictly welded wire configuration. Several kinds of welded wire matrices have been made including point-to-point, without regard to grid pattern and the strictly gridded matrix. For matrices which are not particularly closely spaced, the point-to-point configuration offers advantages. It is simpler to build and requires less organization and tooling. Since crossover of wires is not flexible, the number of matrix layers tends to grow. A minimum number of welds are required in making a point-to-point matrix. Where close lead spacing is required, however, a gridded arrangement seems more usable in spite of the fact that it requires more welds and necessitates considerably more organization and tooling.

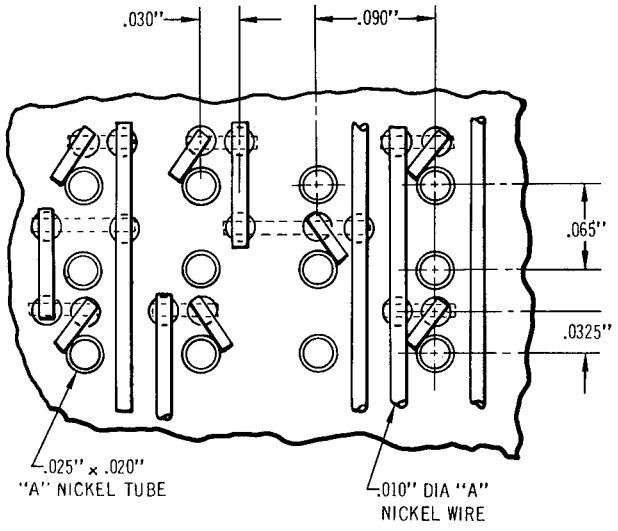

Fig. 9. Welded matrix design dimensions.

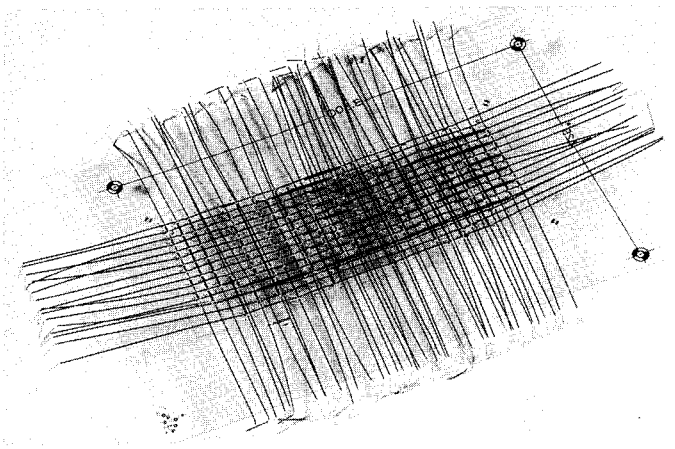

Fig. 10. Welded matrix grid.

The gridded matrix is made by arranging sets of wires, separated by an insulator, at right angles. Point-to-point connections are then made utilizing these grid wires, which are interconnected by welding through holes in the insulation. This basic technique has been described and is well known throughout the electronics industry.

The particular design utilized in this program is illustrated in Fig. 9. The tubes are again placed on 0.065 × 0.090 in. centers. Provision is made to pass one horizontal wire and two vertical wires between tubes. Ten-thousandths-diameter wire is used. The matrix is made using 0.004-in.-thick Mylar on which the matrix wires are outlined as in normal welded module practice. Holes are punched in the Mylar to make provision for the through-welding and the tubes. The matrix wires are placed in a welding fixture separated by the Mylar. Since in the welding process the wires tend to elongate, it has been found desirable to provide for this event in the fixture. This can be done in a number of ways. Welding is then done from the center of the wires out, or from one end to another, never on the ends first.

After the welding operation is complete, the welded grid is removed from the fixture and trimmed in accordance with the wiring pattern. Figure 10 shows an untrimmed welded grid.

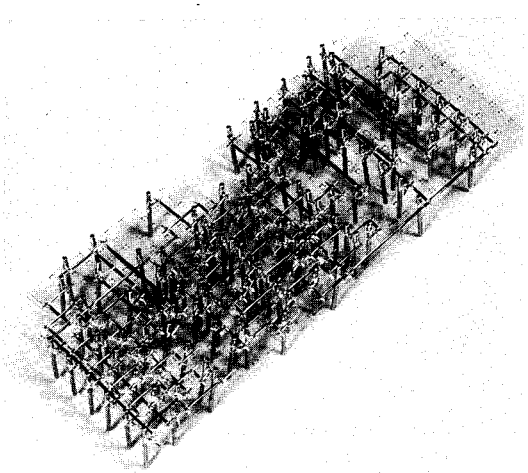

Fig. 11. Welded matrix with tubes in welded position.

Wires are attached to the nickel tubes as in the third matrix, and with similar tube positioning arrangements the tube wire is welded to the matrix as shown in Fig. 11. The matrix layers are assembled and interleaved with a Mylar sheet and the assembly is encapsulated.

The gridded matrix design has a number of advantages over the point-to-point arrangement. It is possible, because of the Mylar separator, to have more crossovers than in the point-to-point system. This tends to minimize the number of layers of matrix required. The use of a grid also tends to give positive spacing to the lead wires minimizing the possibility of shorts.

Where long runs of wire are loose on the matrix they can be attached by providing welded crosses between vertical and horizontal layers. Placing the tube offset, essentially in the center of a 0.060-in. square, instead of attached directly to the horizontal or vertical wires, also minimizes the possibility of shorts. It is of course possible to use a single vertical wire centered between the tubes with a resulting increase in the number of layers required for a given matrix.

Building of closely spaced matrices using welded wire techniques is essentially a tooling problem. The equipment required to make the assemblies is the standard capacitor-discharge welder.

Several other problems aside from matrices themselves should be mentioned regarding their use. The mating of the matrix to the circuit assemblies requires the accurate positioning of circuit assembly lead wires and matrix holes into which they fit. It is desirable to use an assembly fixture to accomplish this mating operation when the circuit assemblies have appreciable numbers of leads. Since it is required that the connection between the circuit assembly leads and the matrix be solid, the end of the matrix tube can be soldered to the circuit assembly lead, or the tube can be crushed around the circuit assembly lead and welded.

It is also necessary to maintain the assembled unit by removing and replacing circuit assemblies. This is done by unsoldering or cutting off the welded junction. The matrices depending on cutting off of the end of the leads for disconnecting obviously must be replaced themselves after only a few circuit assembly replacements.

Use of wire wrapping techniques increases the number of replacements possible, but standard wire wrap tools require more space than is available on a 0.065×0.090 in. grid. A development program is underway to develop tools to accomplish wire wrapping on closer centers.

Most companies in the electronics industry are capable of building some of the matrix systems which have been described here. The designer faced with a complex interconnection problem can exercise his own ingenuity in designing a system to solve his problem and fit in with his company's capabilities.

8067

Electronic Packaging Design for the OAO Primary Processor and Data Storage Equipment

KENNETH E. HARRIS

International Business Machines Corporation, Space Guidance Center; Owego, New York

This paper describes the packaging design of the Orbiting Astronomical Observatory (OAO) Primary Processor and Data Storage (PPDS) equipment, including considerations made in the equipment design and development program for the environmental extremes to be encountered by the OAO satellite. Also included is a description of the evaluation program to assure vacuum stability of organic materials for use in the PPDS equipment, a description of the equipment design and development test program for vibration environment, and a description of the design, analysis and development test program for thermal environment.

INTRODUCTION

THE ORBITING ASTRONOMICAL OBSERVATION (OAO) satellite being designed and fabricated by Grumman Aircraft Engineering Corporation (GAEC) for the National Aeronautics and Space Administration (NASA) will permit astronomical experiments to be performed, unobstructed by the earth's atmospheric distortion. The life of the satellite in orbit is to be one year. Presently two such satellites are under contract with the first satellite date scheduled for 1965.

GAEC awarded a contract to the International Business Machines Corporation (IBM) in December 1960 to design and fabricate the Primary Processor and Data Storage (PPDS) equipment for OAO. The function of the PPDS will be to handle all command and control data transmitted to the satellite, and to store all data obtained by the satellite experimenters. Basically, the OAO is linked to a ground control station by means of a radio receiver and transmitter. All commands transmitted to the satellite will be handled by the PPDS which will check the commands for transmission errors, interpret the commands, and distribute the commands to the proper section of the spacecraft in real time or store the commands for distribution at a later time. In addition, experimentation data obtained by the satellite are stored by the PPDS for transmission to the ground when the satellite is in contact with the ground control station.

The necessary logic and memory devices to perform the PPDS function are installed in two units (Fig. 1). The size, weight, and component count for each of these units is as follows:

Unit No.	*Weight (lb)*	*Volume (in.^{3})*	*Component Count*
140	122.12	4140	38,541
230	112.17	3845	33,396
Totals	234.29	7985	71,937

PACKAGE DESIGN

Package Components

Two units comprise the PPDS, the command processor and data storage (unit No. 140) and the Control Processor and Command Storage (No. 230) (Fig. 1). The basic packaging

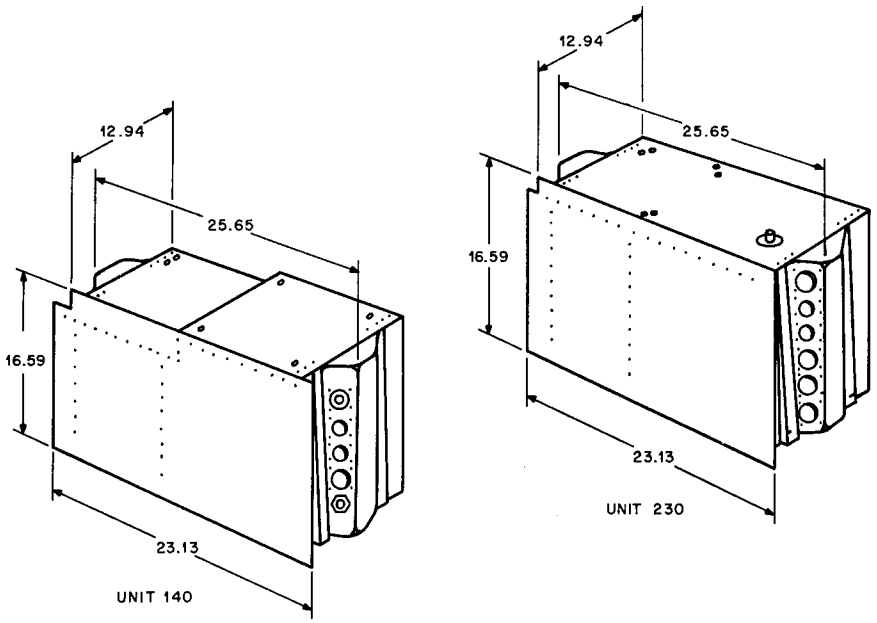

Fig. 1. PPDS units.

components which make up these units are the circuit modules which are packaged in cells of AMP/MECA design, the printed circuit cell panels which mount and interconnect the circuit modules, the memories which are nondestructive core devices contained in 64 × 64 and 32 × 32 matrix planes, and the PPDS power converter.

Circuit Modules

The AMP cell circuit module packages consist of a 1.090 × 1.275 × 0.800 glass filled diallyl phthalate case with a Lexan cover as shown in Fig. 2. Installed in the package are two epoxy glass wafers with the circuit electrical components mounted between them. The components are positioned in the cell for maximum packaging density, with the component bodies staggered where necessary. A minimum electrical clearance of 0.015 is maintained between all electrical conductors in the cells. The component leads protrude through clearance holes in the wafers and are interconnected by 0.010 × 0.020 nickel tape, which is attached to the leads by resistance welding. The input–output tapes are routed to the top edge of the wafers as shown in Fig. 2. The assembly is inserted into the cell case and the input–output tapes are welded to the cell contacts which are phosphor bronze bifurcated springs mounted in slots on two sides of the cell case.

Assembled cells are conformally coated or completely encapsulated, with an epoxy material to (1) provide an insulating barrier between components and electrical conductors in the cell; (2) to add mechanical strength to the cell for protection in vibration environment; and (3) to provide a thermal conduction path from the heat dissipating components to the base of the cell.

The cells are divided into three general categories for the purpose of defining the coating or encapsulation process, depending principally on their heat dissipation. Cells categorized as low dissipators (0–100 mW) are given a light conformal coating of Shell Epon 828 and 871 epoxy material. The average weight of the coating material in low-heat-dissipating cells is 1 g.

Cells categorized as medium dissipators (101–300 mW) are given a heavy conformal coat of Furane Plastics No. 1448 epoxy material. This material has the property of being thixotropic (resisting flow). Therefore, it is possible to add the material to the cell and by swinging or

centrifuging the cell at a controlled speed and time leave a specified amount of epoxy material in the cell. The medium dissipating cells are centrifuged with the cell base away from the center of rotation. Holes in the base permit the epoxy material to be removed during rotation and also cause the material remaining in the cell to bridge from the components to the cell base, thus providing heat conduction paths to the base of the cell. The average coating material weight in the medium heat dissipating cells is 3.8 g.

High-heat-dissipating cells (excess of 300 mW) are completely encapsulated with a lithefrax-filled Epon 828 and 871 epoxy material. Although the lithefrax does improve the thermal conductivity of the encapsulant, its primary purpose is to reduce the shrinkage of the encapsulant material. The average weight of encapsulant in high-dissipating cells is 12 g.

Cell Panel Design

The AMP cells are mounted on panel assemblies designed in four different cell matrix arrangements, 4 × 4, 4 × 8, 5 × 8, and 6 × 9, with different circuitry on each panel, depending on the panel function. The panel assembly (Fig. 3) is made up of a base board, side rails, cell spacers, edge connectors, and cells. The base board is epoxy glass material per MIL-P-13949 with tin lead coated copper printed circuitry on both sides of the board. The side rails are an AMP/MECA design and are also made of epoxy glass material with six machined conductors on one side of each rail. The male electrical contacts for the circuit cells are mounted on the side rails, opposite the conductor lines, by two clinch tabs which fit through slots at the top and bottom of the side rail and clinch over to retain the contact in position. Additional tabs located along the side and at the base of the contact fit through holes in the side rail and panel, respectively, to pick up the electrical conductors. These contact tabs are soldered to the printed circuitry on the side rail and to the panel base board to hold the side rail in place. Contacts may also be installed in positions where they are not connected to cells to provide connection between the side rail and base board.

Each row of cells on the panel is separated by two side rails with the cell positions in each row separated by phosphor bronze spacers. These spacers have four tabs which fit through slots at the top and bottom of the side rails and clinch over to retain the spacer. Two additional tabs at the bottom of the spacer fit through holes in the panel base board and are soldered in place. The space between the side rails, separating the cell rows, is filled with Epon 828 epoxy encapsulant with fillers added to stiffen the side rails and provide an insulating barrier between side rail conductors. Edge connectors, incorporating 28 contacts mounted on the edges of the

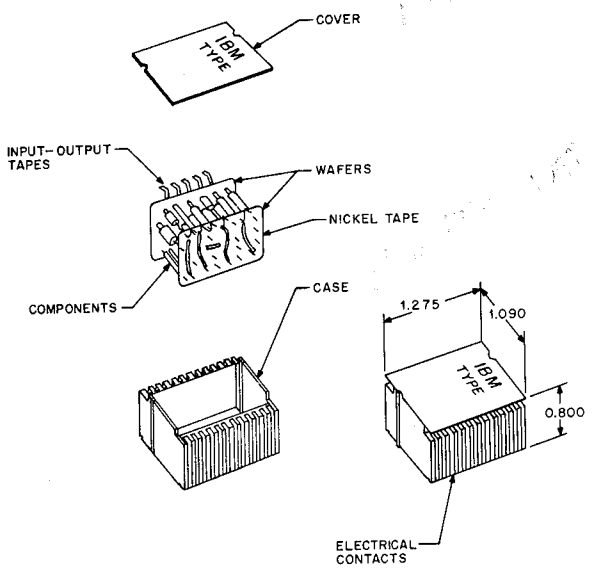

Fig. 2. AMP cell circuit module.

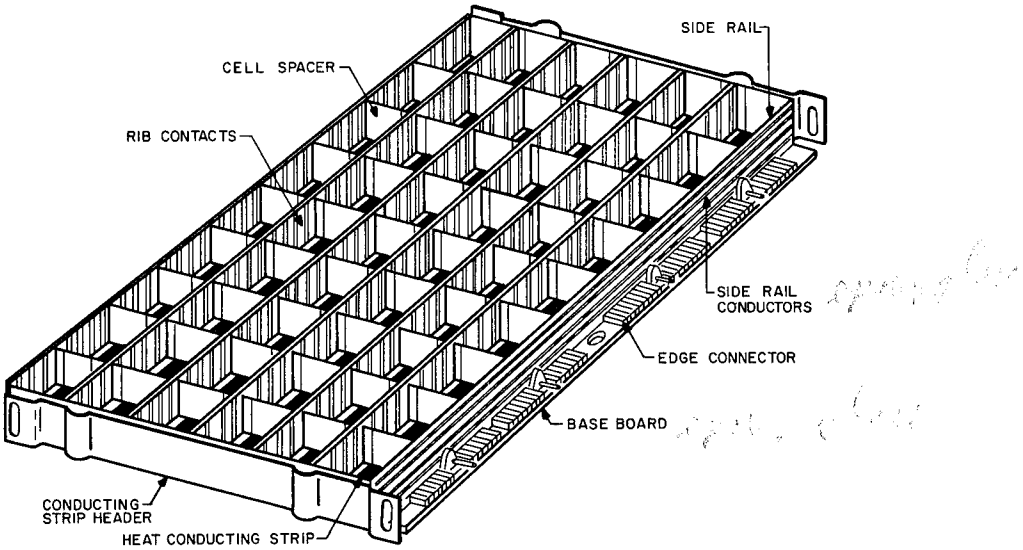

Fig. 3. Panel assembly.

panels, provide electrical interconnection of panels within the units. The electrical connectors are attached to the panel by soldering the connector contacts to circuitry on the base board and cementing the connector body to the panel base board with adhesive backed Mylar film.

The 6 × 9 panels with higher-heat-dissipating circuitry incorporate copper heat conducting strips which are located between side rails and are joined at each end of the panel by headers. The ends of the headers form tabs which are connected to the panel support hardware during assembly. Lower-heat-dissipating panels incorporate brackets at four corners. These brackets bear against the bottom corner of the panel and flange to form a connecting tab, similar to the conducting strip header, for panel attachment at assembly. Both the conducting strips and corner brackets are attached to the panels by adhesive impregnated glass cloth Stan-preg 28 V-E, which is applied under heat and pressure.

Memory Array Design

The magnetic memory cores are packaged in planes (Fig. 4), each of which consists of a frame with two rows of contacts along the four edges, the magnetic cores, and the wiring for sense, inhibit, and address instruction. After the cores are wired in position in the frame the core area is encapsulated with Dow Corning Sylgard 182. The Sylgard encapsulant is molded in a waffle pattern to allow for material displacement during assembly and for thermal expansion, and extends 0.003 in. beyond the frame on each side of the plane.

The completed planes are then stacked and end caps are placed at each end of the stack to form an array as shown in Fig. 5. Four stainless steel bolts, which pass through the mounting tabs at each corner of the planes and the end caps, are taken up so that the plane frames bear against one another, thereby compressing the Sylgard encapsulant material. The command storage array incorporates 30 planes and the two data storage arrays incorporate 25 planes plus one dummy plane each.

The array planes are interconnected by epoxy glass jumper strips which incorporate printed circuitry. These jumper strips are soldered to the contacts on the four sides of the array planes as shown in Fig. 5. After installation of the jumper strips, T rails are installed along the four corners of the array and bolted to the sides of the end caps to act as corner braces for the array planes. The gap between the planes and T rail is filled with silicone sponge rubber. Connectors

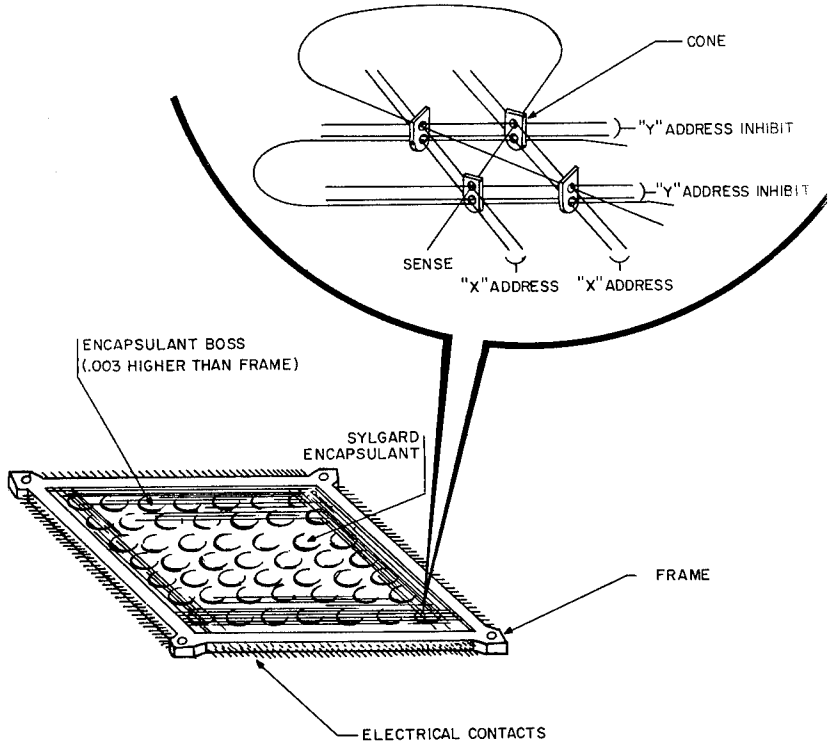

Fig. 4. Memory array plane.

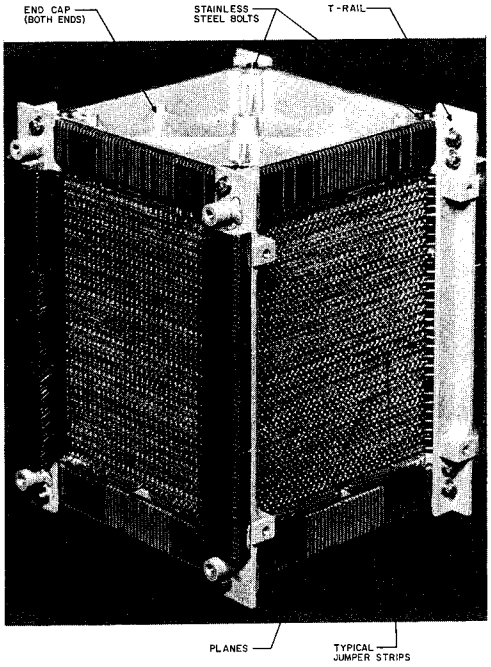

Fig. 5. Memory array.

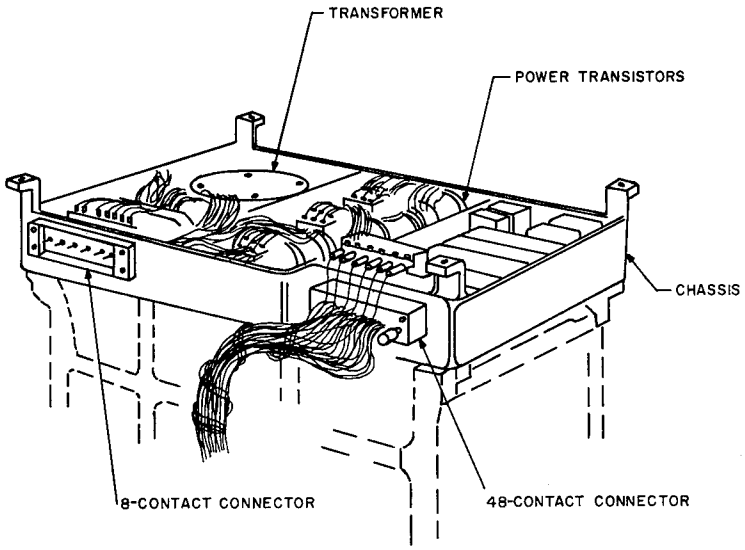

Fig. 6. Power converter.

for the array interconnection with the memory circuitry are mounted on the T rails and end caps as shown.

Power Converter Packaging

The PPDS power converter (Fig. 6) is basically a ribbed-pan-type chassis. The ribs provide a mounting surface for components and/or subassemblies and act as mechanical stiffeners for the chassis. The power transformer mounts in one corner on the chassis and the power transistors mount on the ribbed sections. Other circuitry, including smaller components, is potted in Hysol to form modules which attach to the base of the chassis. Interconnection of the power supply is provided by one 8-contact and one 48-contact connector attached to the chassis as shown in Fig. 6.

Unit Assembly

The assembly of the PPDS packaging components described above in the 140 and 230 units is shown in Figs. 7 and 8. The command processor and control processor logic subassemblies each consist of twelve 9 × 6 panels stacked as shown. The stacks are clamped together by titanium tie rods that connect to aluminum tie rod brackets which bear against the top and bottom panel of the stacks at their four corners. The two tie rods at each corner of the stacks are under tension to provide the desired preload on the stacks. Struts are then installed at each corner of the stacks, connecting to the tie and brackets and the panel conducting strip headers or corner brackets to serve as corner braces for the stacks and to provide heat conduction paths from the panels to the unit cases.

The data storage and command storage memory subassemblies are mounted in frames with the memory arrays located in the center of the packages and the panels nested around the arrays as shown. The panels are held in place by pressure plates which attach to the outer members of the frames and bear against the outer panels in the memory packages. The power converter mounts on the top of the command storage subassembly and serves as the pressure plate for the top panels in this package. Memory interconnection subassemblies (MIA) are installed between the memory arrays and the inner panels of the memory packages as shown in Fig. 9. This provides the necessary interconnections to control the memory array address, sense, and inhibit functions.

The logic and memory subassemblies are installed in their unit cases by first attaching the subassemblies to the unit covers. The unit cases are then placed over the subassemblies and attached to the covers and subassemblies. Connection between the logic subassemblies and the unit cases is made through bushings as shown in Fig. 10, which are adjusted to bear against

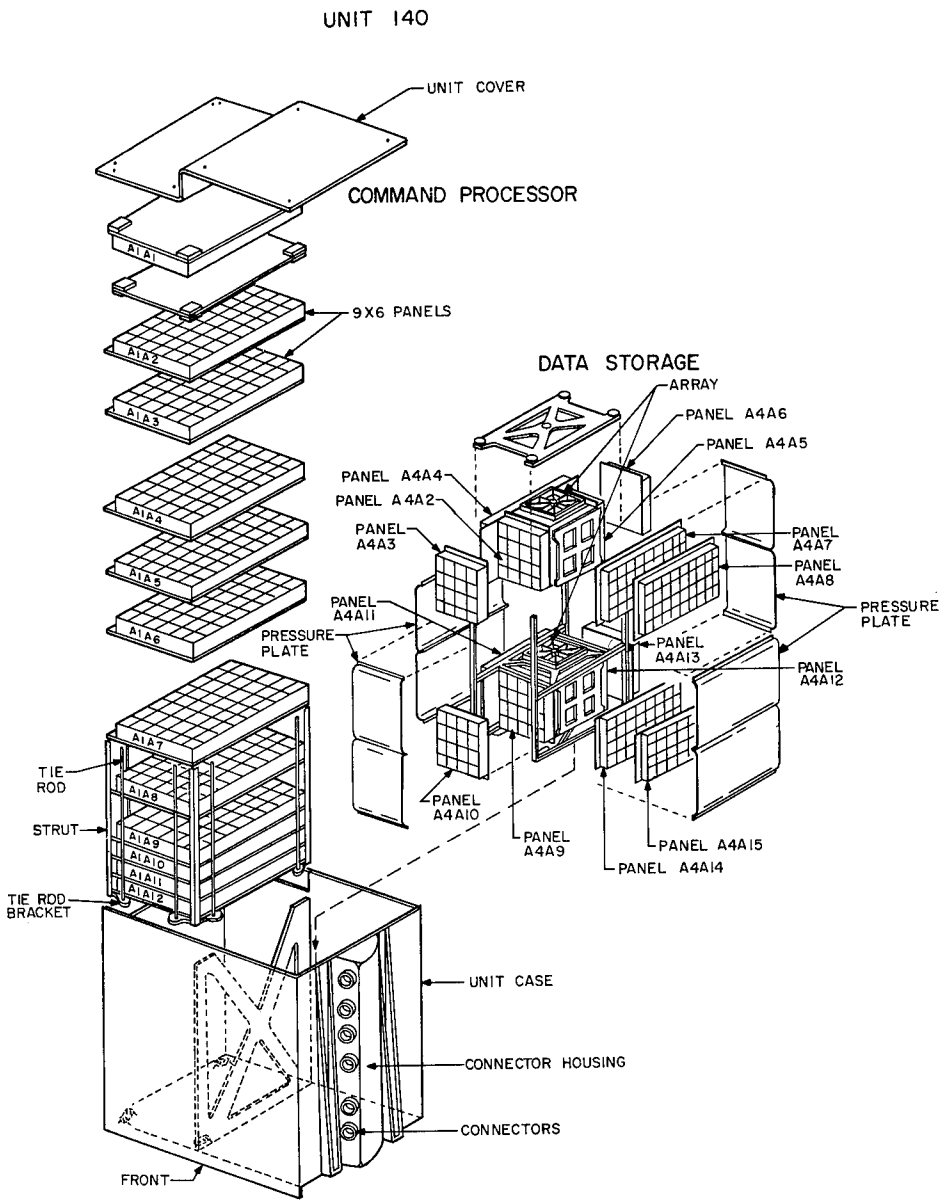

Fig. 7. PPDS Unit 140.

the tie rod brackets of the bottom of the logic stacks without altering the preloading of the stacks. The unit connectors on the subassembly's wiring harnesses are finally attached to the connector housings of the unit cases and the connector housings are attached to the unit cases. This completes the unit assembly operations.

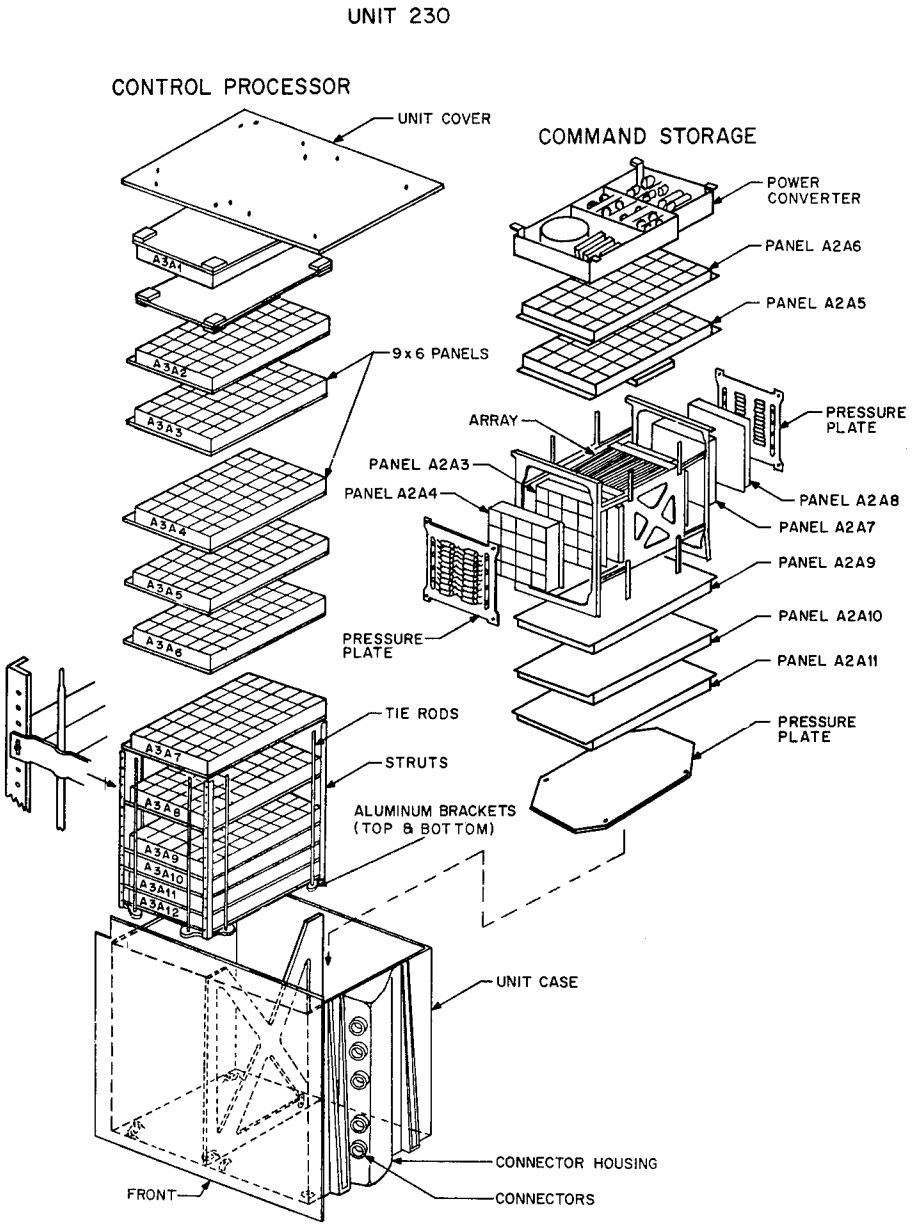

Fig. 8. PPDS Unit 230.

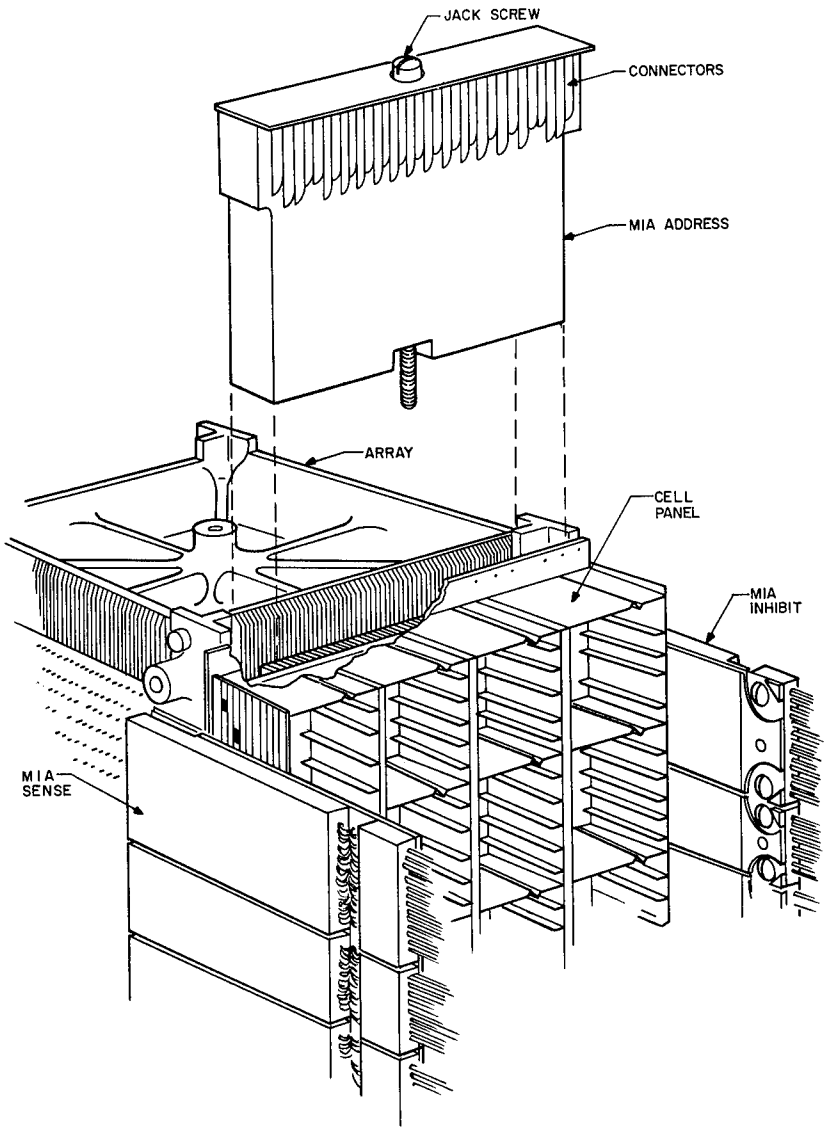

Fig. 9. Memory interconnect assemblies.

MATERIAL SELECTION

The OAO satellite is to perform astronomical experiments, requiring the use of optical equipment. As a result contaminants resulting from outgassing of materials which could collect on the optical equipments must be kept to an absolute minimum. Therefore, at the outset of the PPDS design program it was recognized that one of the major problems to be faced was the selection of nonmetallic materials suitable for use in the OAO environment. Since the selection of these materials involved manufacturing processes and, in many cases, necessitated study of process techniques and tooling preparation, definition of these materials early in the program

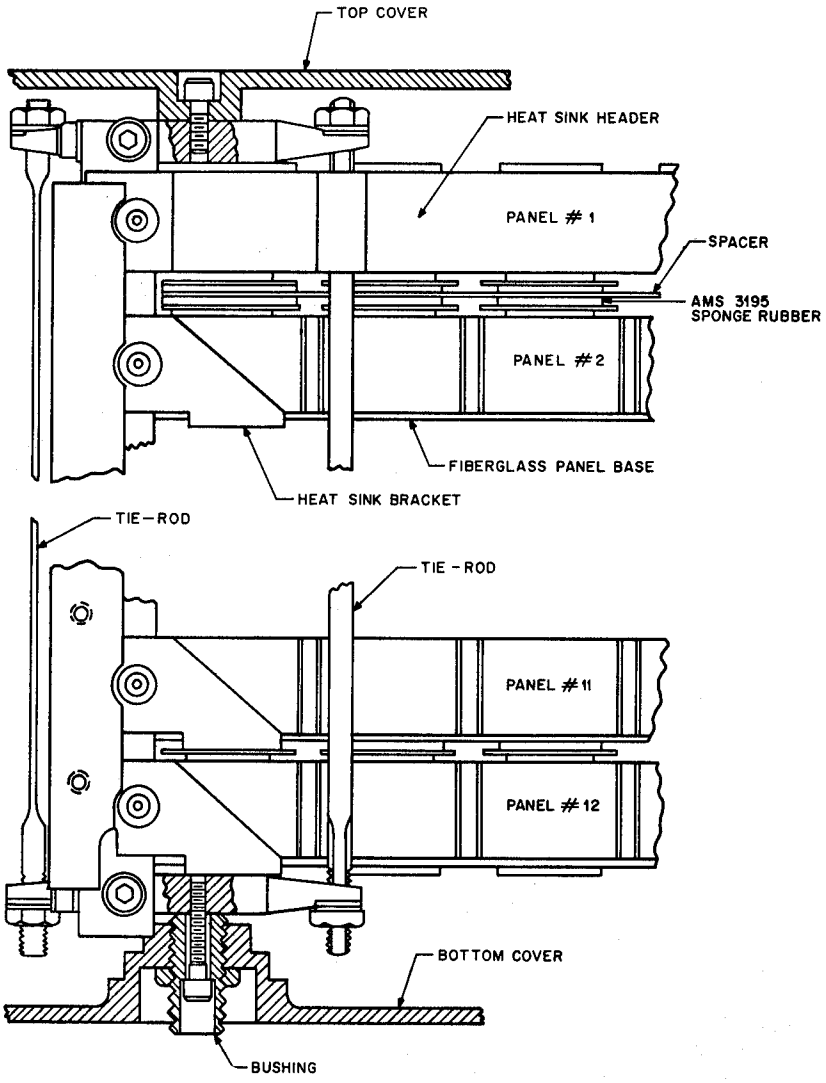

Fig. 10. Logic panel stack case attachment.

was necessary. For these reasons the IBM Owego Materials Group worked closely with the PPDS Design Group from design inception in an effort to select suitable nonmetallic materials for each specific design requirement.

The OAO mission and material environment is defined by either a 500-mile circular orbit or an elliptical orbit with a 400-mile perigee and a 600-mile apogee. According to WADDTR60-785, Part I, the gas composition at this altitude expressed in number density is as follows:

Hydrogen (H^+)	*Hydrogen* (H)	*Oxygen* (O)	*Positive Ions*
5×10^3 n/cm^3	5×10^4 n/cm^3	7×10^5 n/cm^3	1×10^5 n/cm^3

The ozone content at mission altitude is not considered significant. The estimated pressure at

orbital altitudes varies somewhat with source, but a figure of 5×10^{-9} mm Hg is most prevalent. Although the lower Van Allen radiation belt comes as low as 620 miles above the earth's surface, it is quite difficult to predict exact energy levels due to solar activity. The aforementioned WADD report states the level is low enough that organics that reach 25% damage in a few hours in a reactor will last 10^5 hr in a lower level belt. They conclude that radiation is not a problem. The temperature levels within the PPDS equipment during normal operation will vary from a maximum of 185°F to a minimum of 27°F.

Early searches of available data on behavior of nonmetallic materials in vacuum environment were not encouraging. Little if any information could be found on the vacuum stability of many commonly used nonmetallics. The conclusion reached was that it would be necessary to develop an acceptance criterion for nonmetallic materials which could be verified by testing in a reasonable time period with available vacuum equipment. The acceptance criterion selected is as follows:

Sample Preparation

a. Materials which are used in thickness of 0.5 mm or greater shall be prepared as follows:
   1. All samples shall be cast or molded in a thickness of 0.5 mm minimum to 5 mm maximum as pore-free as possible and as free from volatiles such as mold releases and solvents as possible.
   2. The area of the sample shall be 50 to 100 cm^2 with the first figure preferable.
   3. A flat square disk with no holes or fins is preferable due to its ease of handling and area measurement.

b. Materials that are used in thicknesses of 0.5 mm or less and which cannot be cast or molded shall be prepared as follows:
   1. These materials shall be applied to one or both sides of a piece of aluminum or stainless steel 0.07 mm minimum to 0.15 mm maximum thickness with an area of 50 to 100 cm^2 with the first figure preferred.
   2. The sample shall be a flat square or disk with no fins but may have a maximum of two holes for handling. The holes shall be $\frac{1}{16}$ in. in diameter or less.
   3. The metal substrate shall be free of all contaminants, (good electroplating practice), and shall be dried in a forced convection oven for 1 hr at 100 to 120°C.
   4. The metal shall be cooled in a desiccator and immediately weighed and measured in thickness prior to application of organic.
   5. Nonmetallic shall be applied to the substrate and cured if necessary. If required, the substrate may be preheated prior to application. The cure should be representative of actual fabrication procedure to be used in the PPDS/PSSC equipment.

Testing Procedure

a. Degrease sample if necessary and remove any apparent dust, lint, or the like.
b. Condition the sample for a minimum of 6 hr at laboratory ambient conditions (shielded from dust).
c. The sample is then weighed on an analytical balance.
d. The sample is then immediately placed in a high vacuum chamber and pumping started.
e. The sample is then subjected to 100 ± 5°C for a minimum of 24 hr up to 96 hr at an ultimate low of 1×10^{-7} mm Hg and a high 5×10^{-6} mm Hg. The ultimate low pressure is usually maintained for 8 hr during a day when liquid nitrogen trapping is available. Pressure and temperature are logged daily.
f. After the test run, the chamber is brought to atmospheric pressure. The sample is removed using acceptable techniques and immediately reweighed.
g. The following data are recorded:
   1. Percent weight loss after vacuum exposure based on initial weight of sample obtained in (c) above.
   2. Weight loss per unit area expressed in 100 × gram loss per square centimeter.
   3. Thickness of sample.

h. *Acceptance Criteria*—The material loss shall not exceed 2% of the original material weight or, in the case of marking ink, the weight loss per unit area shall not exceed 0.003 g/cm^2. If the weight loss is over 2%, the sample weight regain after exposure to laboratory ambient conditions may be monitored. If the weight regained reduces the permanent weight loss to less than 2%, the material is acceptable.

The foregoing test criterion was established based on experimentation with organic materials in vacuum environment and examining their time *vs.* outgassing characteristics. A plot of time *vs.* pressure was first established for the materials evaluation vacuum equipment as shown in Fig. 16. Using the same control point settings on the vacuum equipment, the pump-down characteristics were then monitored with various samples of materials to be evaluated. It was found that materials which meet the acceptance criterion shown above have the volatiles removed, and the vacuum equipment reaches the pressure indicated by the control point settings within the 96-hr test period. This is illustrated in Fig. 17 which shows the vacuum equipment pump-down characteristics for a typical material tested together with the vacuum equipment pump-down characteristics without the material as shown in Fig. 16. A pressure value of 10^{-7} mm Hg was used for evaluation because of vacuum equipment limitations. The vacuum characteristics of materials evaluated by the foregoing test criterion is shown in Table I.

TABLE I

OAO Vacuum-Resistant Materials—General List

Material	Vendor and identification	Weight loss % g/g	Weight loss g/cm^2 %
	Encapsulant and Potting Compounds		
Elastomer, silicone	Dow Corning, RTV 731	1.5	0.173
Elastomer, silicone	Dow Corning, Sylgard 182	1.2	0.198
Epoxy compound	Hysol Corp. No. 4799 and 3596	0.03	0.0024
Epoxy molding compound	American-Marrietta Tybon XN-1341	0.2	0.059
Elastomer, silicone mineral filled	G.E. RTV 11 and Lithefrax	1.15	0.097
	Adhesives		
Epoxy	Minn. Mining and Mfg. EC-1469	0.05	0.01
Epoxy patch kit	Hysol Corp., No. 1-C	0.38	0.03
Epoxy	Shell Chem., Epon VI	0.54	0.05
Epoxy	IBM Owego AR1T 6009653	0.25	0.037
	Coatings		
Epoxy, conformal	Furane, 1448 and 9816	0.15	0.016
	Miscellaneous		
Laminate glass epoxy	MIL-P-18177 Type GEE	0.2	0.005
Diallyl phthalate	Rogers RX-1360 (MIL-M-14 type SDG)	0.51	0.056
Diallyl phthalate	Acme Resins Corp, Compound No. 1-520	0.51	0.075
Lexan	Gen. Elect. 100-07 Blue	0.27	0.047
Silicone rubber	Used in Deutsch Co. connector	0.14	0.006
Teflon tape	Minn. Mining and Mfg. No. 549	0.124 to 0.213	
Teflon lacing tape, rubberized	Gudebrod style 256-H	0.43	
Mylar tape	Permacel 94 1 in. wide	0.025	
Ink, marking, ivory	Marken Mach. Co. HM-7133		0.02
Glass cloth, preimpregnated	Standard Insul., Stanpreg 28V-E	0.25	

VIBRATION DESIGN AND TESTING

Environment

The sinusoidal qualification vibration environment specified for the PPDS equipment is shown in Figs. 11 and 12 for all three equipment axes. Note that the lateral vibration envelopes are specified along axes at 45° to the orthogonal axes of the units. In addition, the equipment is required to endure the following random vibration environment during qualification in all three axes:

5–40 cps—09 g^2/cps
40–2000 cps—0.015 g^2/cps

As installed in the spacecraft the PPDS units are mounted on vibration isolators provided by GAEC. The above-described vibration levels represent responses to the equipment on the isolation system and are, therefore, hard-mount test levels. The resonant frequency of the isolation system as provided by GAEC is 20–30 cps. Since the PPDS does not operate during launch of the spacecraft, all vibration testing is conducted on the PPDS units with the power turned off.

Vibration Design

AMP Cells. To provide for PPDS package resonances and accompanying vibration transmissibilities with a safety factor, the PPDS components, with a few exceptions where required, were qualified for a 70-*g* peak vibration environment from 5–3000 cps. The 70-*g* vibration level was applied to the components with the component bodies clamped to the exciter table. At the cell level, component mounting was examined with the objective of either: (1) maintaining the natural frequency of the components above the qualification vibration envelope, or (2) maintaining the natural frequency of the components above the expected resonances of the PPDS unit panels. Analysis indicated that this could be accomplished on resistors, diodes (Fairchild F200), and smaller transistors (Fairchild type S4317) by fixing the component leads at the wafers, i.e., clamping the component leads where they pass through

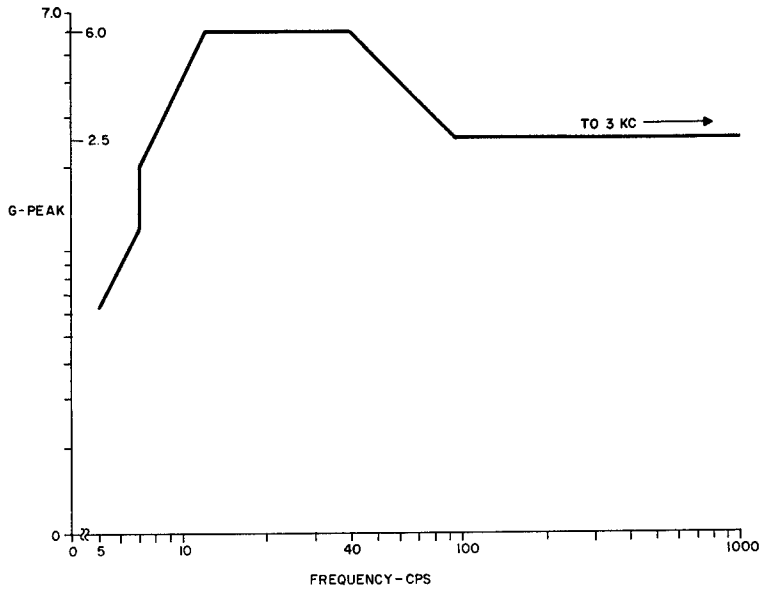

Fig. 11. Sinusoidal vibration envelope—*X*-*X* axis.

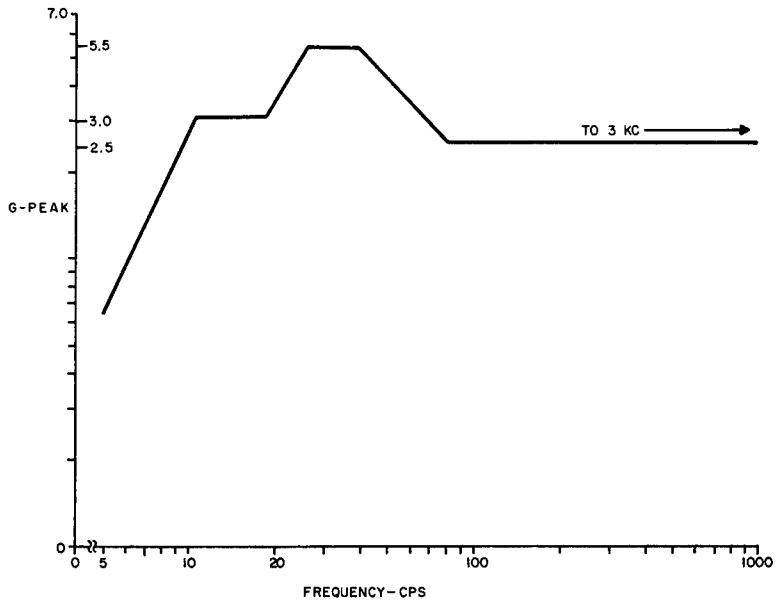

Fig. 12. Sinusoidal vibration envelope— *Yc*-*Yc* and *Zc*-*Zc* axes.

the wafer holes. To accomplish this a requirement was imposed that the cell conformal coating epoxies bridge all component leads to the cell wafers.

Larger transistors with heavier bodies could not be mounted from the cell wafers by their leads and meet the above requirements. It was, therefore, required that the conformal coating epoxy bridge between the large transistor body and wafer. To ensure that no relative motion occurred between the cell cases and wafers in conformal coated cells, it was also required that the epoxy coating material bridge between the cell case and wafer around the outer edges of the wafer. To support still heavier components such as the Bulova Type ST-70-AX crystals, the cells containing these components were filled with encapsulant.

Memory Arrays. As mentioned earlier, the memory cores are encapsulated in Sylgard 182, a silicone elastomer material, to support these devices in a vibration environment. The Sylgard encapsulant is molded in a waffled pattern as shown in Fig. 4, such that the high spots of the waffle boss exceeds the frame thickness by 0.000 to 0.003 in. During assembly the array planes are stacked between end caps (Fig. 5) and pulled together until the plane frames bear against one another thereby compressing the Sylgard encapsulant. Compression of the encapsulant is sufficient to ensure plane-to-plane contact in the core area over the operating temperature range of the system of 44 to 119°F.

The plane-to-plane contact in the core area ensures preload in the array which varies with temperature as shown in Fig. 13. Calculations and strain gage tests indicated that this results in a natural frequency of approximately 500 cps within the array at room temperature. This was well above the expected natural frequency of the array structure and, as a result, was felt to be sufficiently stiff.

Logic Stack. The 6 × 9 logic panels, as described earlier, are assembled in stack fashion and clamped at their corners by tie rods. Aluminum brackets bear on the four corners of the top and bottom panels with two tie rods connecting each bracket. The natural frequency of the logic panel stack is controlled by adjusting the tension on the tie rods. Stacks were assembled early in the program and the tie rod tension was adjusted to obtain the desired natural frequency, as determined by vibration tests.

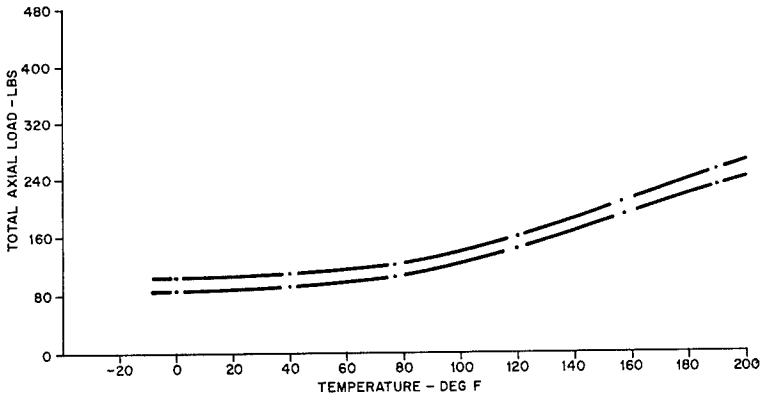

Fig. 13. Memory array preloading.

It was found that a tension of 200 lb on each tie rod resulted in a natural frequency of approximately 150 cps on the panel stack. This value of natural frequency was felt to be sufficiently above the PPDS isolation system resonance so as not to result in a problem with overlap of resonances in this area. Further, it was not practical to raise the frequency higher due to load limitations of the panel corner cells.

Vibration Development Testing

Unit Tests. A development test mock-up of each PPDS unit was fabricated for vibration testing. The unit cases and internal structures were duplicated in every detail using final design drawings for fabrication, and panels were duplicated except for details of printed-wiring layout. A functional power converter was installed in the 230 unit and connected so that its operation could be monitored before and after vibration exposure.

The lower data storage memory array in the 140 unit was simulated by dummy frames potted together to simulate the array mass and the upper data storage array was simulated using dummy planes in the 7 end positions at the top of the array and the 6 end positions at the bottom of the array. The 13 center planes in the upper data storage array were actual array planes containing cores. Read and write operation and continuity of windings of the center (13th) plane was monitored during test. The command storage array was dummied in the development test unit.

Functional cells were not installed in the vibration test mock-up units. Cell cases were partially filled with RTV-731 material and installed on the panels as necessary to simulate final panel weights and Cg's. Partial unit harnesses were installed in each unit connecting panels, power converter, and external connectors as required to give a sufficient representation of panel-to-panel and panel-to-unit connector wiring.

Each unit was instrumented as shown in Figs. 14 and 15. The accelerometer numbers are indicated in the balloons on these figures and the direction of accelerometer sensitivity is indicated by the arrows pointing to the balloons. The logic stack tie rods in each unit contained strain gages, which were used to monitor initial loading of the tie rods and loading after vibration exposure. The units were individually exposed to the sinusoidal vibration levels as shown in Figs. 11 and 12 using an MB Electronics C50 exciter. The units were then individually exposed to the random vibration levels shown above using an MB Electronics C210 exciter. Reduced data resulting from these tests are shown in Table II.

The unit development tests resulted in the following conclusions:

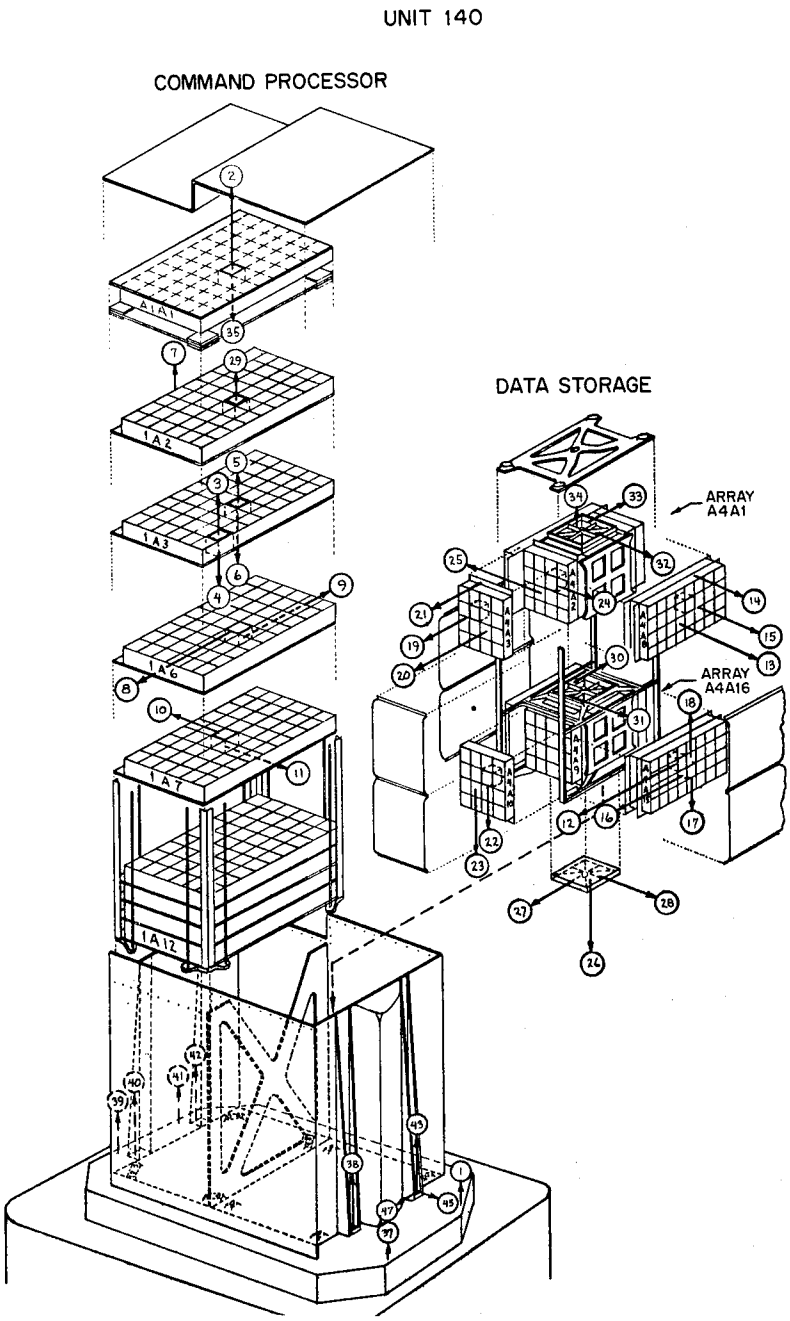

Fig. 14a. Unit 140—accelerometer locations: X-X axis.

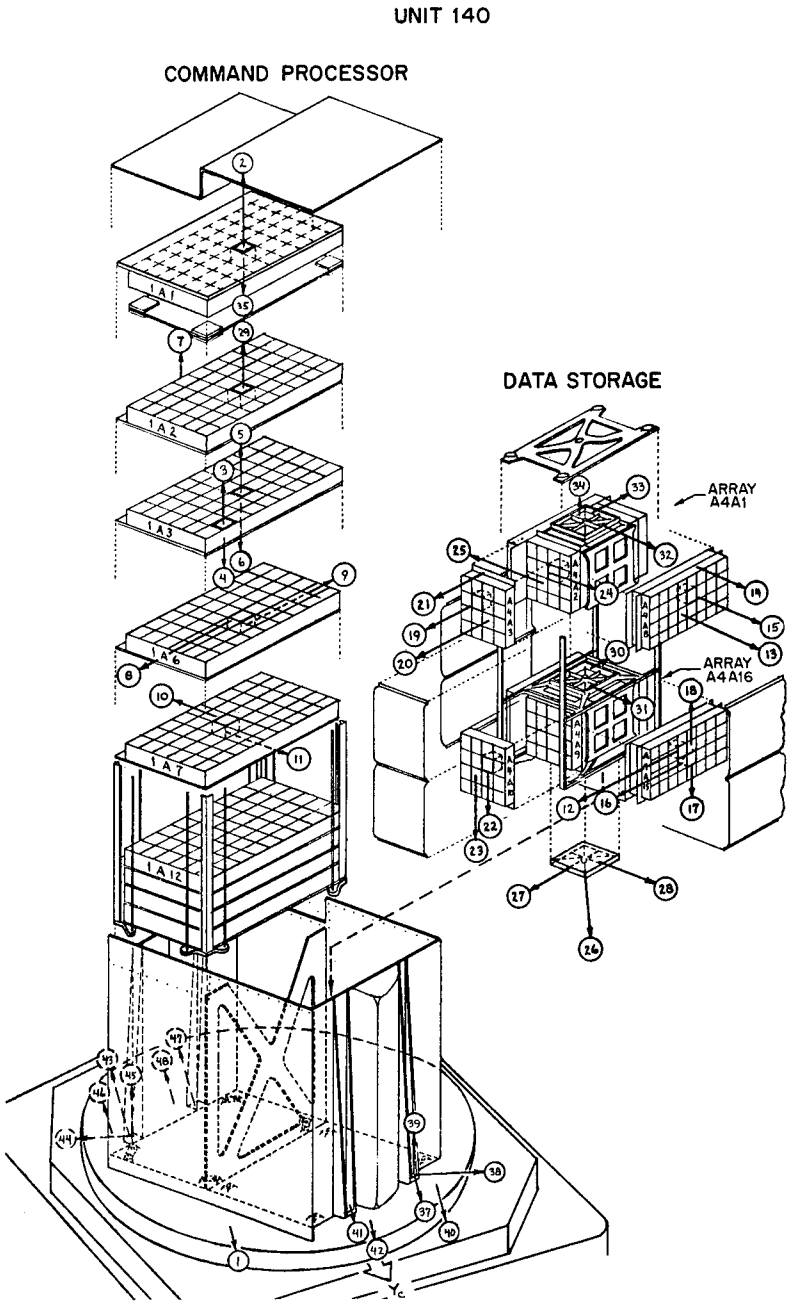

Fig. 14b. Unit 140—accelerometer locations: *Yc*-*Yc* axis.

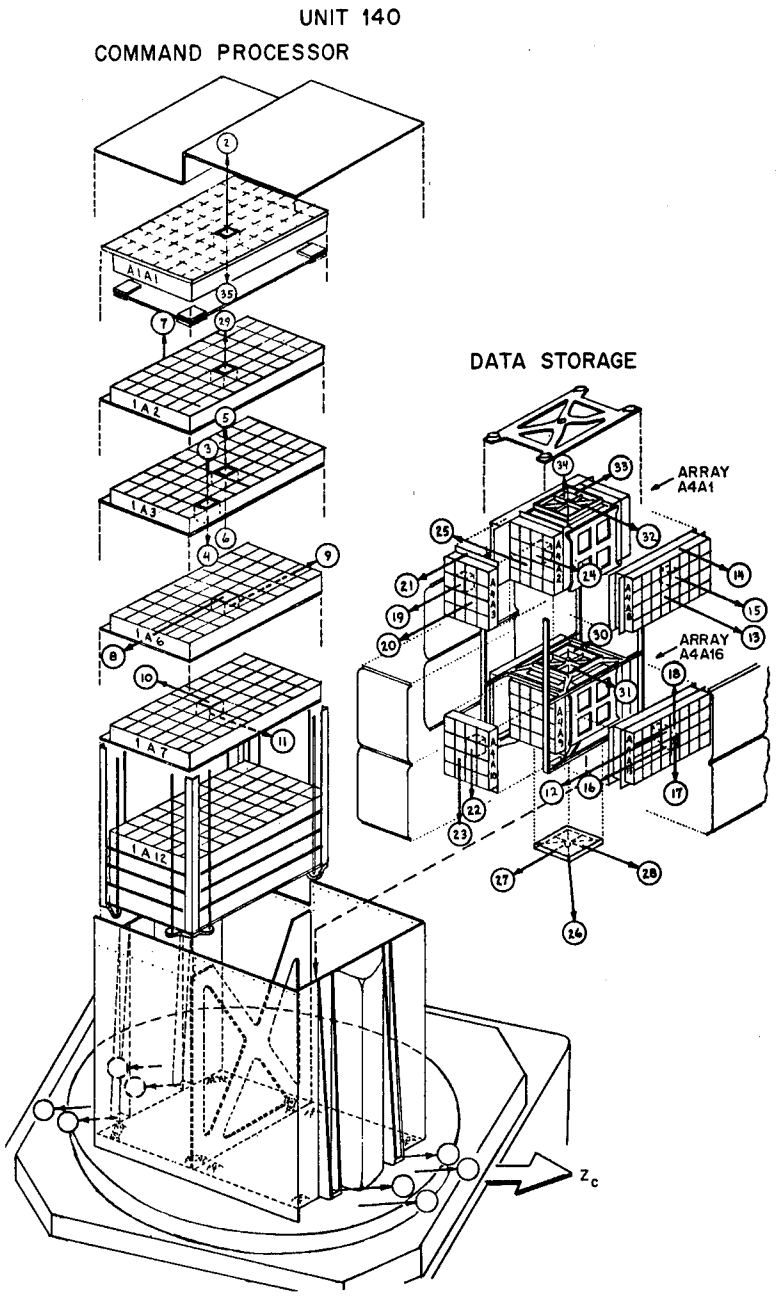

Fig. 14c. Unit 140—accelerometer locations: *Zc-Zc* axis.

(*a*) *Cells:* As shown in Table II, no responses at cell locations exceeded 70-*g* peak. Therefore, in those instances where analysis indicated that a one-to-one transmissibility between the cell case and cell components could be obtained up to 3000 cps, the cell components should not be exposed to vibration levels above their qualification limit. From analysis it was determined that the lowest natural frequency of any component would be 1500 cps. Responses at cell locations at this frequency and up to 3000 cps are all below 5 *g*. With an input of this magnitude to the cell, the vibration level on a component in resonance would not be expected to exceed 70-*g* peak. It was, therefore, concluded that no cell components with resonance below 3000 cps would exceed their qualification vibration limits in the system qualifications.

(*b*) *Power Converter:* The power converter was functionally tested following vibration exposure and was found to meet all specification requirements on the voltage output levels. The converter was visually examined and found to be structurally sound with no evidence of cracks, broken wires, etc. It was, therefore, concluded that the power converter would meet qualification environmental requirements.

(*c*) *Memory Arrays:* Monitoring of read and write operations of one data storage array plane during vibration exposure indicated proper memory function. Check of continuity in windings of the same plane during and after vibration exposure indicated no broken wiring. Visual examination of upper data storage array and command storage array showed no evidence of structural damage or broken wire. The conclusion reached was that the memory arrays could withstand PPDS qualification vibration environment.

(*d*) *Logic Stacks:* The natural frequencies of the logic stacks from Table II were found to be $\sim$160 cps in the 140 unit and $\sim$180 cps in the 230 unit. Since this is above PPDS vibration isolator resonance, the tie rod tension previously determined was felt to be satisfactory. Visual examination of the logic stacks, however, indicated cracked cell cases in the corner locations of several panels. This revealed a dynamic loading problem in this area, which was resolved by encapsulating the corner cells.

(*e*) *Memory Structure:* Visual examination of the data storage and command storage memory structures indicated no failures in these areas and resulted in the conclusion that the memory packaging was satisfactory for vibration environment.

(*f*) *Harnesses:* No evidence of broken wiring or connectors was found as a result of visual examination of the unit harnesses following unit vibration testing.

(*g*) *Unit Cases:* Visual examination of the unit cases following vibration exposure indicated no evidence of damage.

Subassembly Tests. Subsequent to unit development tests, the following additional vibration development testing was conducted on a subassembly level to verify design analysis and support previous conclusions as additional hardware became available.

(*a*) *AMP Cells:* Using data obtained from the unit development tests, composite sinusoidal vibration envelopes were constructed showing worst-case response of all panel cell locations monitored. Representative samples of cells were selected which included all components used in cell assemblies and included the three cell-coating and/or encapsulation materials. These cells were exposed to the composite vibration envelope levels and functionally tested following vibration exposure. No cell failures were noted following the cell vibration tests.

(*b*) *Panel Connectors:* As in the case of the AMP cells, composite vibration envelopes were constructed using responses obtained at panel connector locations during unit tests. A mated panel connector with wiring attached was subjected to vibration levels described by these envelopes. During vibration exposure all wiring through the connector was monitored for continuity. The connector maintained electrical continuity during vibration exposure and showed no evidence of mechanical damage on examination following vibration test.

(*c*) *Memory Array:* With data obtained from the unit test, composite vibration envelopes were prepared for the memory arrays. A data storage memory array was constructed, and subjected to the vibration levels described by these envelopes. Fourteen of the array planes located throughout the array had their sense, inhibit, and address lines connected externally to form a series circuit. Continuity was monitored in this circuit during vibration exposure of

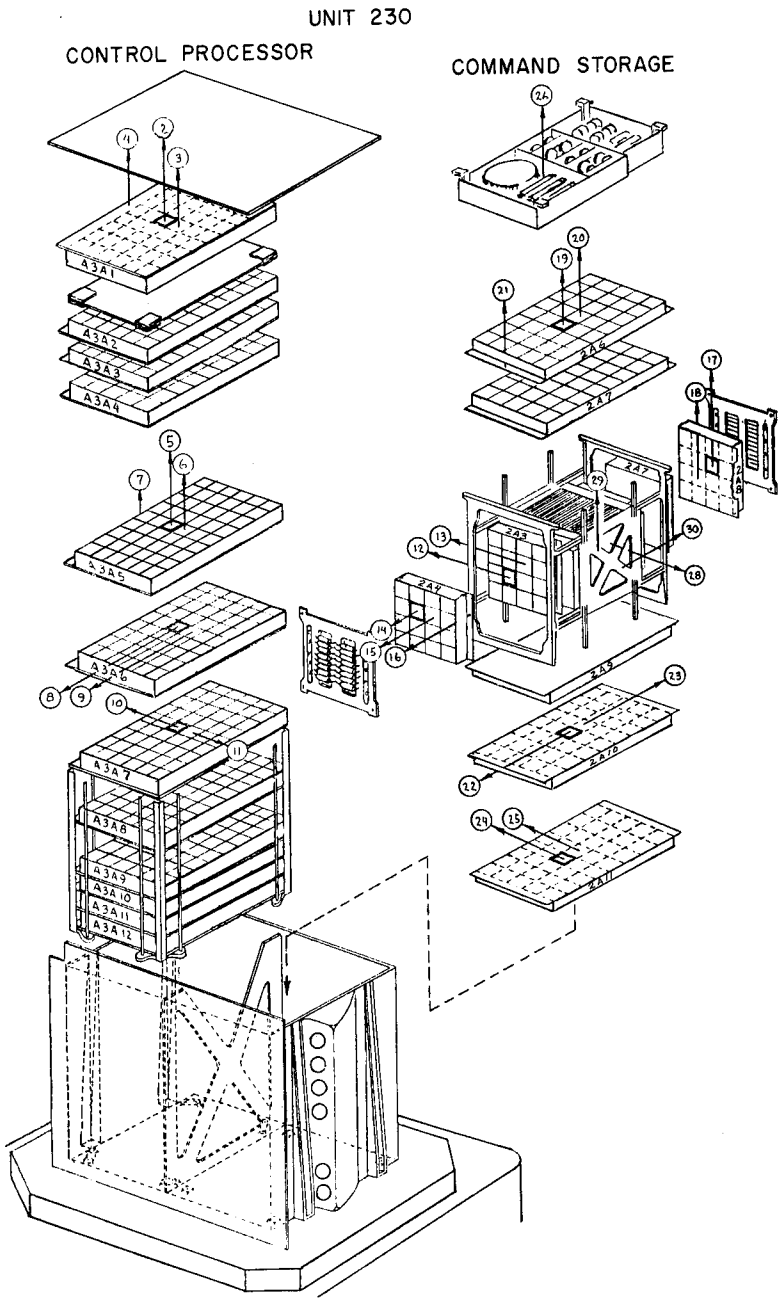

Fig. 15a. Unit 230—accelerometer locations: X-X axis.

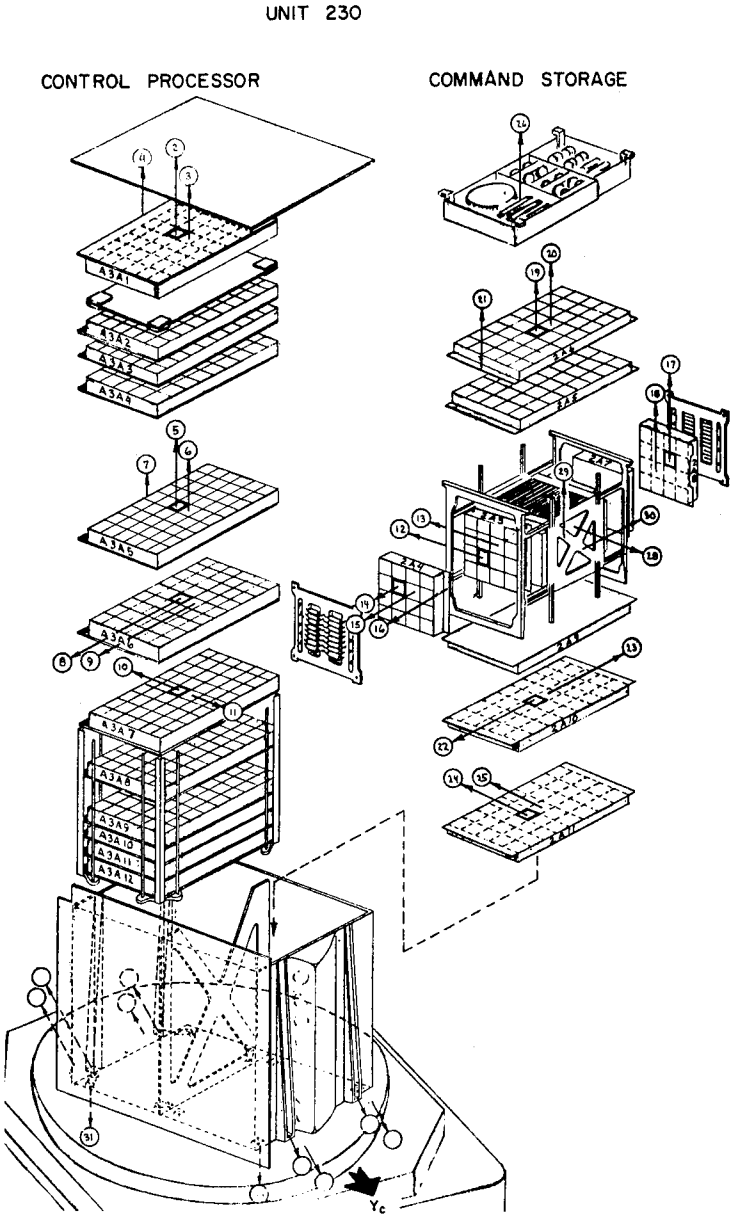

Fig. 15b. Unit 230—accelerometer locations: *Yc*-*Yc* axis.

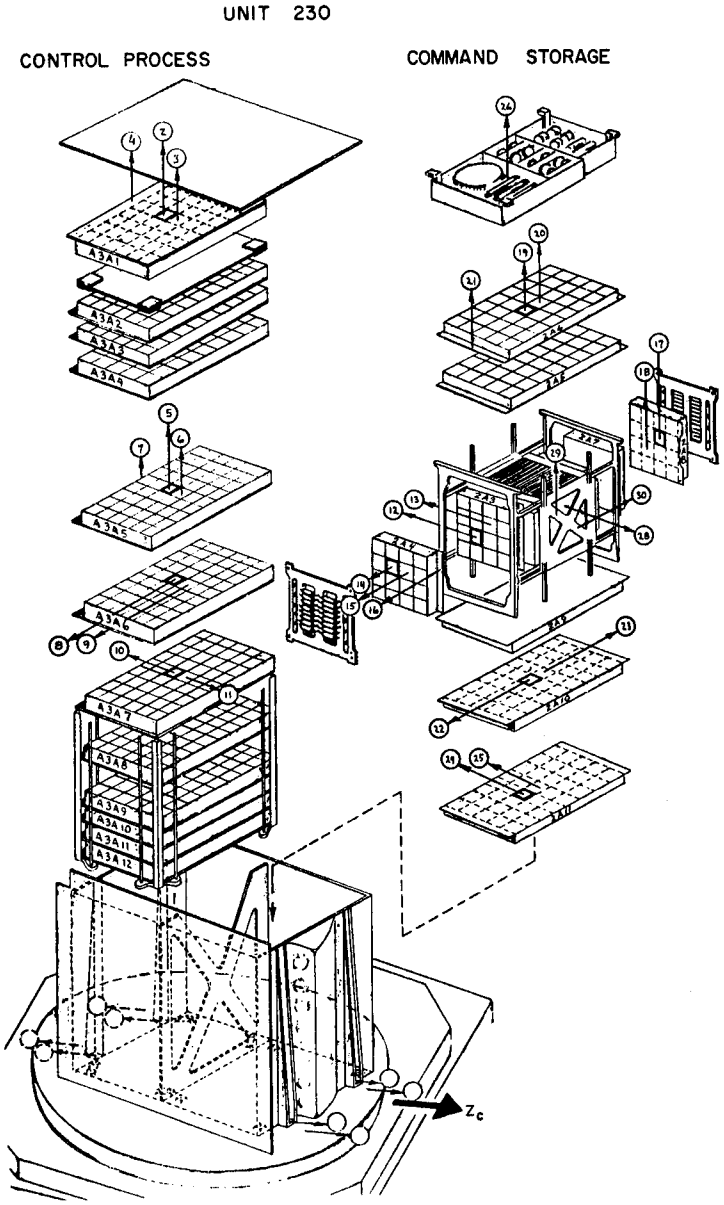

Fig. 15c. Unit 230—accelerometer locations: *Zc-Zc* axis.

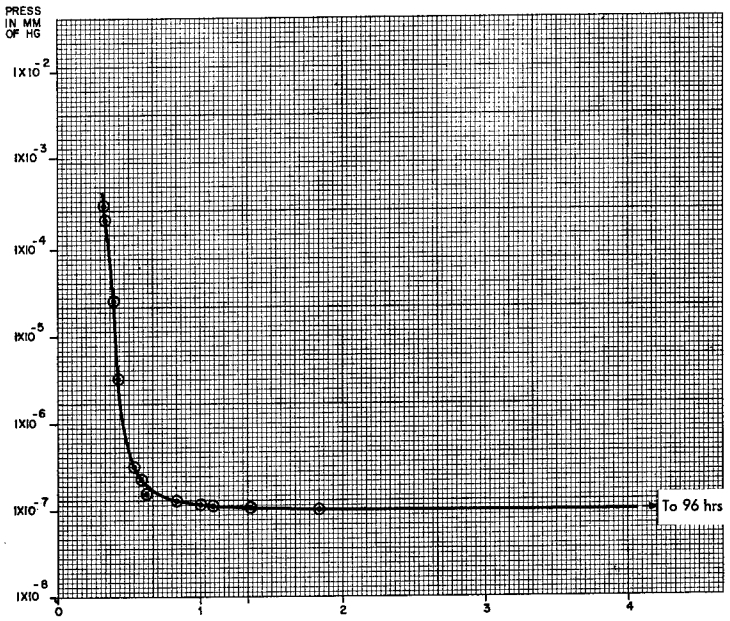

Fig. 16. Pump-down characteristics of materials evaluation vacuum equipment.

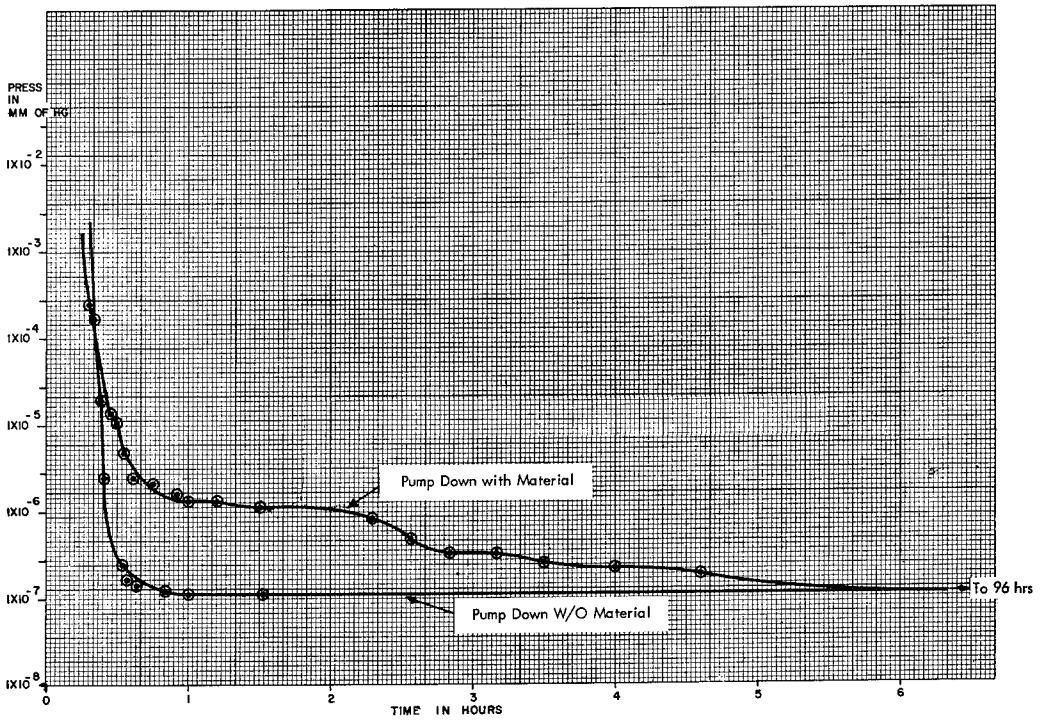

Fig. 17. Pump-down characteristics of material evaluation vacuum equipment with material sample.

the array. No loss of electrical continuity was encountered which could be attributed to a failure of the array wiring during test. Following vibration the array was given a thorough visual inspection and no mechanical discrepancies were evident.

THERMAL DESIGN AND TESTING

Environment

The thermal design of the OAO electronic equipment is dependent on a passive system. All electrical heat is conducted to a specified surface of the equipment from which it is radiated to the spacecraft skin and thence to outer space. Heat transfer between the other internal spacecraft structures and the electronic equipment is kept to an absolute minimum by: (1) installing thermal insulation between the equipment mounting surfaces and the spacecraft structure to minimize conduction of electrical heat to the spacecraft, and (2) by installing Mylar-backed aluminum foil over the internal spacecraft structure (except the skin) to minimize radiation heat transfer to the spacecraft structure from the electronic equipment. This is necessary to minimize temperature gradients on the internal spacecraft structure and the effects the accompanying structural distortions would have on the alignment of OAO experimenters' optical equipment (Fig. 18).

The temperature of the PPDS units' surfaces facing the spacecraft skin, i.e., unit heat sink surfaces, are therefore dependent on the environmental heat load on the spacecraft skin, the absorptivity of the external spacecraft skin, the emissivity of the inside spacecraft skin and the units' heat sink surfaces, the area of the spacecraft skin and the units' heat sink surfaces, and the units' electrical heat load. These parameters are related as follows:

(1) Considering first the spacecraft skin, the following heat balance is obtained:

$$A_e/A_{sk} + Q_{env} = \sigma E_{sko} T_{sk}^4$$

(2) A similar heat balance on the units' heat sink surfaces is obtained by

$$Q_e + \sigma F_{21} E_{ski} T_{sk}^4 = \sigma F_{12} E_e T_e^4$$

(3) Solving (1) for T_{sk}^4 and substituting in (2), we obtain

$$T_e^4 = \frac{Q_e}{\sigma F_{12}}\left[\frac{1}{A_e} + \frac{F_{21}}{E_{sko} A_{sk}}\right] + \frac{F_{21} Q_{env}}{F_{12} \sigma E_{sko}}$$

where

$$F_{12} = \frac{1}{1/E_e + [(A_e/A_{sk})(1/E_{ski})] - 1}$$

and

$$F_{21} = \frac{1}{1/E_{ski} + [(A_{sk}/A_e)(1/E_e)] - 1}$$

and the nomenclature is defined as follows: A_e is the area of units' heat sink surface, ft^2; A_{sk} is the area of spacecraft skin adjacent to units, ft^2; Q_e is the units' electrical heat load, Btu/hr; Q_{env} is the environmental heat load to spacecraft skin, Btu/hr-ft^2; σ is Boltzmann's constant;

E_{ski} is the emissivity of inside of spacecraft skin; E_{sko} is the emissivity of outside of spacecraft skin; E_e is the emissivity of units' heat sink surfaces; T_e is the unit's heat sink surface temperature (absolute); T_{sk} is the spacecraft skin temperature (absolute); F_{12} is a form factor—unit to skin; and F_{21} is a form factor—skin to unit.

With (3) above, the average steady state heat sink surface temperature for the PPDS units may be obtained, assuming the time-averaged heat loads for a specific orbit and satellite orientation. These temperatures for maximum and minimum environmental heat loads are shown in Figs. 19 and 20 in the form of curves for varying PPDS unit electrical heat loads.

Thermal Design

Thermal Design Limits. The temperature limits initially placed on the PPDS components for orbital operation of the PPDS were as follows:

Subassembly	*Limiting component*	*Temperature limits*	
		max	*min*
Cells	Carbon composition resistor	185°F	53°F
Power converter	2N1100 germanium transistor	160°F	53°F
Memory array	Magnetic core	153°F	17°F

The carbon composition resistor was limited to a 185°F maximum surface temperature, and minimum surface temperature of 53°F to provide a +7% and −8% tolerance on this component at the end of 12,000 hr life. This was the tolerance required in critical circuit application, using tolerance data available on other components in the circuits to provide series-parallel circuit redundancy and allow for component failures which may occur during the one-year operating life of equipment in orbit. The 160°F upper case temperature limit on the 2N1100 transistor is typical for germanium devices. The 53°F lower temperature limit was used to maintain the transistor beta within limits required. The memory array cores were tested and found to provide reliable outputs within the temperature range shown above.

Thermal Packaging Design. The PPDS unit heat dissipation is radiated to the spacecraft skin from the unit front panels or heat sink surfaces; therefore, all heat generated in the units must be conducted to the unit front panel.

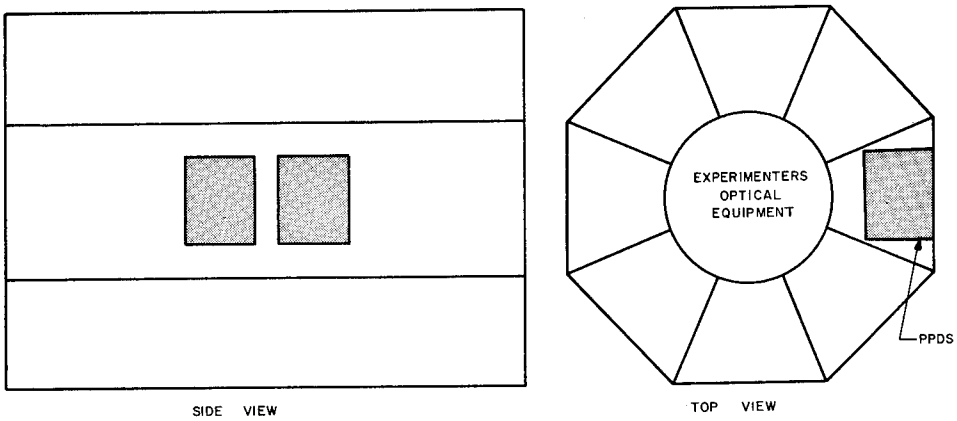

Fig. 18. PPDS location in satellite.

Table II

DATA SHEET: SINUSOIDAL VIBRATIONS — INPUT: ALONG THE VERTICAL (X - X) AXIS OF THE UNIT — CURVE # 3 — UNIT NO. 140

DATE TEST STARTED: — DATE COMPLETED: — RUN NO.

CHANNEL	G PEAK OUT @ 110 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 130 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 134 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @140 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 160 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 165 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 170 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 190 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 200 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 400 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 500 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 650 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 700 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 750 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @850 CPS WITH 2.5 G PEAK INPUT	CHANNEL
1	2.3	2.3	2.3	2.6	2.2	2.5	2.5	2.5	2.5	2.3	2.3	2.3	2.5	2.5	2.3	1
2	3.8	5.0	5.0	4.0	7.5	14.0	11.5	6.0	8.0	2.0	5.5	1.0	3.0	3.5	2.0	2
3	4.0	5.0	5.5	4.0	5.0	8.0	7.0	3.5	3.5	2.0	3.5	3.0	5.0	8.0	4.0	3
4	3.8	5.0	5.0	3.5	5.0	8.0	7.5	3.5	3.0	2.0	3.0	3.0	5.0	8.0	4.0	4
5	5.7	7.5	7.5	6.0	10.0	20.0	18.0	9.0	10.5	2.0	8.0	4.0	4.0	2.0	1.5	5
6	5.7	7.5	8.0	6.0	11.0	20.0	18.0	9.0	11.0	2.0	8.0	4.0	3.5	2.0	1.0	6
7	Not Recording	-	-	-	-	-	-	-	-	-	-	-	-	-	-	7
8	1.5	2.5	3.0	2.0	2.0	2.0	2.0	1.5	1.5	1.0	1.5	1.5	1.5	2.0	1.5	8
9	1.0	2.0	2.5	1.5	2.0	2.0	2.0	2.0	1.5	1.0	1.0	1.0	1.5	1.0	1.5	9
10	1.5	2.0	3.0	1.5	2.5	5.0	3.5	2.0	2.0	1.5	1.5	3.0	5.5	13.0	3.0	10
11	2.0	3.0	3.5	4.0	4.0	10.0	8.0	4.0	4.0	1.5	5.0	1.5	1.5	2.0	1.0	11
12	1.0	5.0	9.0	5.0	2.2	3.0	3.0	2.0	1.5	1.5	3.0	1.0	1.0	1.5	1.0	12
13	2.0	2.3	7.0	5.5	6.0	6.0	4.0	1.5	1.5	3.0	2.0	1.0	1.0	1.5	1.5	13
14	Not Recording	-	-	-	-	-	-	-	-	-	-	-	-	-	-	14
15	2.0	3.5	3.5	3.0	1.5	1.0	1.0	1.5	1.5	2.0	1.0	1.0	1.0	1.0	1.5	15
16	1.0	3.0	5.0	3.5	2.0	2.0	1.5	1.5	1.5	1.0	1.0	1.0	1.0	3.0	1.0	16
17	6.0	20.0	32.0	24.0	9.0	8.0	6.0	3.5	3.0	3.5	3.0	3.5	4.0	2.5	1.5	17
18	6.5	20.0	28.0	21.0	7.5	7.0	5.5	3.0	2.5	3.5	2.5	2.0	2.0	2.0	1.0	18
19	1.0	2.0	2.0	2.0	1.5	1.5	1.5	1.5	1.5	1.5	1.7	1.5	1.5	1.5	1.5	19
20	1.0	2.0	3.0	3.0	2.0	1.5	1.5	1.5	1.5	1.5	1.7	1.7	1.7	1.5	1.5	20
21	3.0	6.0	9.0	7.0	3.0	2.5	2.5	2.0	2.0	1.5	1.5	1.5	1.7	1.7	1.7	21
22	7.0	24.0	32.0	30.0	12.0	9.0	7.0	5.0	4.5	2.3	2.5	1.5	1.5	1.5	1.5	22
23	6.0	14.0	22.0	20.0	8.0	6.0	5.5	4.0	4.0	3.0	3.0	2.0	2.0	2.0	2.0	23
24	1.5	4.0	7.0	6.0	4.0	3.0	2.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	24
25	2.0	8.0	13.0	12.0	8.0	7.0	4.0	2.0	2.0	1.5	2.0	2.5	8.0	2.0	1.7	25
26	6.0	16.0	23.0	18.0	8.0	7.0	6.0	3.5	3.0	1.5	1.0	1.5	1.5	1.5	1.5	26
27	1.0	2.5	4.0	3.0	2.0	2.0	2.0	1.5	1.0	1.0	1.0	1.0	1.0	1.0	1.0	27
28	1.0	2.5	4.0	4.0	3.0	3.0	2.5	1.5	1.0	1.5	1.5	1.5	1.5	1.5	1.5	28
29	6.0	9.0	10.0	8.0	14.0	24.0	20.0	10.0	12.0	2.3	9.0	5.8	2.0	3.0	2.0	29
30	1.0	3.0	5.0	4.0	2.0	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	30
31	1.5	4.0	6.0	6.0	4.0	5.0	4.0	2.5	2.0	1.5	1.7	1.5	1.5	1.5	1.7	31
32	1.5	1.5	1.5	1.5	1.0	1.0	1.0	1.0	1.0	1.5	1.0	1.0	1.0	1.0	1.0	32
33	1.5	2.0	3.0	2.0	1.5	1.5	1.5	1.0	1.0	1.5	1.0	1.0	1.0	1.0	1.0	33
34	5.0	14.0	21.0	16.0	7.0	6.0	5.0	4.0	3.5	1.5	1.5	1.5	1.5	1.5	1.5	34
35	Not Recording	-	-	-	-	-	-	-	-	-	-	-	-	-	-	35
36	2.3	2.3	2.4	2.5	2.5	2.5	2.5	2.5	2.5	2.3	2.3	2.3	2.3	2.3	2.3	36
37																37
38																38
39																39
40																40

Table II (cont)

DATA SHEET: SINUSOIDAL VIBRATIONS — INPUT: ALONG THE VERTICAL (X - X) AXIS — CURVE # 3 — UNIT NO. 230

DATE TEST STARTED: — DATE COMPLETED: — RUN NO.

CHANN	G PEAK OUT @ 20 CPS WITH 6.0 G PEAK INPUT	G PEAK OUT @ 110 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 130 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 140 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 150 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 170 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 180 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 220 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 280 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 300 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 400 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 425 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 500 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 575 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 600 CPS WITH 2.5 G PEAK INPUT	CHANN
1	Not Used															1
2	6.5	4.0	6.0	8.0	10.0	14.0	38.0	12.0	5.0	5.0	2.5	3.0	5.5	5.5	4.0	2
3	7.0	4.0	6.5	8.0	10.0	14.0	38.0	11.0	6.0	6.0	3.0	3.8	6.5	8.0	4.2	3
4	8.0	4.0	6.0	9.0	11.0	18.0	46.0	14.0	5.0	2.0	4.2	4.0	4.0	3.0	2.0	4
5	7.0	4.2	6.5	8.2	10.0	14.5	37.0	11.0	5:0	4.0	3.5	4.0	7.0	10.0	7.5	5
6	7.0	4.5	6.5	8.0	10.0	14.0	37.0	10.5	5.5	4.0	2.5	3.5	7.0	11.0	8.0	6
7	8.5	4.2	6.0	4.5	9.0	13.0	34.0	9.0	3.5	2.0	2.5	5.0	3.5	12.0	5.0	7
8	Not Used															8
9	1.0	1.0	1.5	2.0	6.5	2.0	2.0	2.0	1.5	1.5	1.5	1.5	1.5	1.5	1.5	9
10	Not Used															10
11	1.0	1.0	1.0	1.0	1.5	3.8	4.2	1.2	1.0	1.0	1.0	1.0	1.5	1.8	1.8	11
12	Not Used															12
13	Not Recording	—	—	—	—	—	—	—	—	—	—	—	—	—	—	13
14	Not Used															14
15	Not Used															15
16	Not Used															16
17	4.5	3.5	4.0	7.0	13.0	10.0	6.0	1.8	1.0	1.0	1.5	3.5	2.0	1.5	1.5	17
18	6.0	3.5	4.5	6.5	13.0	9.0	6.2	1.8	.8	.8	1.5	3.5	2.5	1.5	1.0	18
19	Not Recording	—	—	—	—	—	—	—	—	—	—	—	—	—	—	19
20	7.0	5.5	9.0	13.0	28.0	22.0	15.0	5.0	3.0	2.5	3.8	4.0	6.5	3.0	2.0	20
21	8.5	5.0	11.0	27.0	37.0	44.0	32.0	4.0	15.0	3.5	8.0	22.0	13.0	11.5	5.0	21
22	Not Used															22
23	.5	.5	1.0	2.0	6.5	3.5	2.2	2.0	1.0	1.0	.8	1.5	1.8	1.0	.5	23
24	Not Used															24
25	.8	.5	.5	1.0	8.0	3.0	2.0	.5	1.0	1.0	1.2	1.5	1.0	.8	.5	25
26	6.5	6.0	8.0	12.0	27.0	23.0	17.0	5.0	3.0	2.5	4.0	4.0	3.5	3.0	2.0	26
27	Not Used															27
28	Not Used															28
29	7.0	5.0	7.0	12.0	28.0	20.0	12.5	4.0	2.0	1.0	.3	1.5	1.5	1.8	1.5	29
30																30
31																31
32																32
33																33
34																34
35																35
36																36
37																37
38																38
39																39
40																40

Table II (cont)

DATA SHEET: SINUSOIDAL VIBRATIONS — INPUT: ALONG THE LATERAL Y_c - Y_c AXIS OF THE UNIT — CURVE # 3 — UNIT NO. 140

DATE TEST STARTED: — DATE COMPLETED: — RUN NO.

CHANN	G PEAK OUT @ 10 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 25 CPS WITH 5.1 G PEAK INPUT	G PEAK OUT @ 80 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 87 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 90 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 145 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 152 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 160 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 220 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 270 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 380 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 450 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 500 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 700 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 750 CPS WITH 2.5 G PEAK INPUT	CHANN
1	3.0	6.0	3.0	3.2	3.2	3.0	3.2	3.2	3.0	3.0	3.0	3.0	3.0	3.0	3.0	1
2	.7	1.0	1.0	4.0	2.0	1.0	2.2	2.0	1.0	1.0	2.0	1.5	1.5	1.5	1.5	2
3	.7	1.0	2.0	7.0	4.2	2.0	2.0	1.5	2.0	2.5	3.0	4.0	1.5	1.0	1.5	3
4	.7	1.0	2.0	7.0	4.0	1.8	1.8	1.5	2.0	2.0	2.0	3.5	1.5	1.0	1.5	4
5	.7	1.5	2.0	6.0	3.8	1.5	4.0	3.0	1.5	1.5	2.0	1.5	3.0	1.5	1.0	5
6	1.0	1.0	2.0	6.0	3.0	1.0	3.0	3.0	1.0	1.5	1.5	1.5	2.5	1.5	1.0	6
7	.7	1.0	8.0	14.0	10.0	6.0	8.0	5.0	2.0	5.0	11.0	5.0	11.0	6.0	3.0	7
8	2.0	6.0	7.5	17.0	11.0	4.0	5.0	4.0	3.0	3.5	6.0	2.5	1.0	2.0	1.5	8
9	2.0	5.0	7.0	16.0	10.0	3.0	5.0	4.0	2.0	3.5	4.5	2.0	1.5	1.0	1.0	9
10	2.0	4.5	4.5	7.0	4.0	6.0	14.0	10.0	2.0	1.5	5.0	5.0	5.0	3.0	11.0	10
11	Not Recording	-	-	-	-	-	-	-	-	-	-	-	-	-	-	11
12	2.0	4.0	4.0	8.0	6.0	3.5	6.0	4.0	2.0	10.0	2.0	2.0	2.5	1.5	1.5	12
13	2.0	4.5	4.5	7.0	3.5	10.0	22.0	15.0	4.0	2.0	8.0	8.0	4.0	1.0	1.0	13
14	1.0	1.0	1.5	6.0	4.0	3.5	5.0	3.0	1.0	1.0	2.5	1.0	1.0	1.5	1.5	14
15	2.0	4.5	4.0	5.0	2.0	8.0	19.0	12.0	2.0	2.0	2.0	1.5	2.0	1.5	1.0	15
16	2.0	4.0	4.0	7.0	4.0	4.0	6.0	3.5	2.0	7.0	2.0	1.5	1.5	4.0	2.0	16
17	1.0	2.0	2.5	6.0	3.5	4.5	2.8	5.5	1.5	4.0	6.0	9.0	8.0	3.0	2.0	17
18	1.0	1.0	1.5	3.0	2.0	4.0	4.0	4.0	2.0	2.0	7.0	5.0	4.0	1.5	1.5	18
19	2.0	4.5	7.0	18.0	12.0	3.0	7.0	5.5	2.0	2.0	2.0	6.0	1.5	1.5	1.5	19
20	2.0	4.0	6.0	14.0	10.0	3.0	9.0	6.0	2.0	3.0	2.5	5.0	1.5	2.0	1.5	20
21	2.5	5.0	8.0	21.0	15.0	3.5	6.0	5.5	2.5	6.0	2.5	3.0	1.5	2.0	2.5	21
22	2.0	3.5	2.0	9.0	7.0	10.0	23.0	15.0	3.8	10.0	6.0	3.5	3.5	4.5	4.0	22
23	1.0	1.0	2.0	7.2	5.0	6.0	12.0	7.0	2.0	5.0	5.0	2.0	2.0	1.5	1.5	23
24	2.5	6.0	7.0	15.5	11.5	1.0	4.5	3.5	.7	3.5	4.5	3.0	2.0	1.5	1.0	24
25	3.0	8.0	6.0	12.0	6.0	12.0	30.0	20.0	5.0	3.0	2.0	6.0	3.0	16.0	3.0	25
26	1.0	1.0	1.5	3.0	2.0	3.0	3.0	2.5	1.0	2.0	2.5	1.8	1.5	1.0	1.0	26
27	2.0	4.0	2.5	3.5	2.5	3.5	3.8	2.0	2.5	5.0	2.0	2.2	1.5	1.5	1.5	27
28	2.0	4.0	3.5	4.0	2.0	4.0	9.0	5.5	1.0	1.5	3.0	3.0	2.0	1.5	1.5	28
29	1.0	2.0	4.0	9.0	4.5	2.0	4.0	3.5	1.8	3.0	2.5	2.2	3.5	3.8	2.0	29
30	2.5	4.0	5.0	13.0	7.5	2.0	4.0	3.0	3.5	7.5	3.0	2.0	1.5	1.5	1.5	30
31	1.5	2.0	1.5	7.0	5.5	7.0	14.0	10.0	4.0	6.0	2.5	1.0	1.0	1.0	1.0	31
32	1.5	2.0	1.8	1.8	1.5	2.0	3.5	2.5	1.0	1.5	1.0	1.5	1.0	1.0	1.0	32
33	2.0	4.5	6.5	19.0	13.0	3.0	4.0	3.8	1.8	4.0	2.0	1.0	1.0	1.0	1.0	33
34	Not Recording	-	-	-	-	-	-	-	-	-	-	-	-	-	-	34
35	1.5	1.5	2.0	6.0	3.0	1.5	3.0	3.0	1.0	1.5	1.5	2.0	2.0	2.0	2.5	35
36	3.0	6.0	3.0	3.0	2.5	2.8	3.0	3.0	3.0	3.0	3.0	3.2	3.2	3.2	3.2	36
37																37
38																38
39																39
40																40

Table II (cont)

DATA SHEET: SINUSOIDAL VIBRATIONS — INPUT: ALONG THE LATERAL Y_c - Y_c AXIS — CURVE # 3 — UNIT NO. 230

DATE TEST STARTED: — DATE COMPLETED: — RUN NO.

CHANN	G PEAK OUT @ 20 CPS WITH G PEAK INPUT	G PEAK OUT @ 75 CPS WITH G PEAK INPUT	G PEAK OUT @ 78 CPS WITH G PEAK INPUT	G PEAK OUT @ 85 CPS WITH G PEAK INPUT	G PEAK OUT @ 130 CPS WITH G PEAK INPUT	G PEAK OUT @ 150 CPS WITH G PEAK INPUT	G PEAK OUT @ 170 CPS WITH G PEAK INPUT	G PEAK OUT @ 210 CPS WITH G PEAK INPUT	G PEAK OUT @ 260 CPS WITH G PEAK INPUT	G PEAK OUT @ 275 CPS WITH G PEAK INPUT	G PEAK OUT @ 300 CPS WITH G PEAK INPUT	G PEAK OUT @ 340 CPS WITH G PEAK INPUT	G PEAK OUT @ 360 CPS WITH G PEAK INPUT	G PEAK OUT @ 460 CPS WITH G PEAK INPUT	G PEAK OUT @ 575 CPS WITH G PEAK INPUT	CHANN
1	Not Used															1
2	1.0	2.0	5.5	4.0	1.5	1.5	1.5	1.8	1.5	1.0	1.0	8.0	3.2	2.5	1.5	2
3	1.0	2.0	6.5	4.0	1.8	1.8	1.8	1.8	1.5	1.5	1.5	8.5	3.8	2.5	2.5	3
4	2.0	2.0	6.0	4.2	2.0	1.0	1.0	1.0	3.0	6.0	6.0	16.0	7.0	4.0	2.0	4
5	1.0	2.0	5.5	3.0	1.0	1.0	1.5	1.8	1.0	1.0	1.0	3.5	3.0	2.5	1.0	5
6	.8	2.0	5.5	3.5	1.0	2.0	1.5	1.5	1.5	2.0	1.5	4.5	4.0	2.0	2.5	6
7	1.2	2.0	5.0	4.0	3.0	1.8	2.0	1.8	2.5	3.5	2.0	9.0	7.0	1.8	11.0	7
8	3.0	8.0	12.5	9.0	3.5	3.0	3.0	3.8	3.0	2.5	3.0	2.5	3.5	3.8	2.5	8
9	3.8	8.0	11.0	8.5	3.0	2.5	3.0	3.0	2.0	2.0	2.0	2.0	3.0	3.0	2.5	9
10	3.0	4.0	8.0	4.0	3.8	5.0	13.0	3.5	1.8	1.5	1.5	3.0	9.0	4.5	1.0	10
11	3.8	4.5	6.5	4.5	3.8	6.5	14.0	3.8	1.8	1.8	1.5	3.5	8.5	5.0	1.5	11
12	Not Used															12
13	3.0	4.0	6.0	5.0	4.5	17.0	12.0	4.0	4.5	2.0	2.0	4.0	4.0	2.0	1.0	13
14	Not Used															14
15	Not Used															15
16	3.7	9.0	18.0	10.0	2.0	3.0	3.0	2.0	4.0	3.0	2.0	2.0	4.0	2.0	1.0	16
17	Not Used															17
18	Not Used															18
19	Not Used															19
20	.8	2.0	12.5	7.5	1.0	2.5	3.0	1.2	1.5	3.0	1.0	1.0	3.5	2.0	1.0	20
21	1.0	6.0	36.0	11.0	3.0	5.0	4.0	5.0	9.0	38.0	4.0	2.0	2.5	8.0	9.0	21
22	Not Used															22
23	3.0	6.5	10.0	6.0	2.0	2.5	4.0	6.5	1.0	2.0	2.0	3.5	1.0	2.0	2.0	23
24	3.0	2.5	4.0	2.0	2.0	8.0	2.5	2.0	2.0	2.5	2.2	2.5	2.0	2.0	2.0	24
25	2.5	2.0	3.0	2.5	2.5	11.0	4.0	1.5	1.5	2.5	4.0	4.5	4.0	1.5	2.5	25
26	Not Used															26
27	Not Used															27
28	Not Used															28
29	Not Used															29
30	.8	1.2	1.5	1.2	.8	.8	.8	.8	.8	.8	.8	.8	.8	.8	.8	30
31																31
32																32
33																33
34																34
35																35
36																36
37																37
38																38
39																39
40																40

Table II (cont)

DATA SHEET: SINUSOIDAL VIBRATIONS — INPUT: INPUT ALONG THE LATERAL $Z_c - Z_c$ AXIS OF THE UNIT — CURVE # 3 — UNIT NO. 140

DATE TEST STARTED: — DATE COMPLETED: — RUN NO.

CHANN	G PEAK OUT @ 15 CPS WITH 3.0G PEAK INPUT	G PEAK OUT @ 30 CPS WITH 5.5G PEAK INPUT	G PEAK OUT @ 80 CPS WITH 2.5G PEAK INPUT	G PEAK OUT @ 85 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 90 CPS WITH 2.5G PEAK INPUT	G PEAK OUT @ 120 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 140 CPS WITH 2.5 G PEAK INPUT	G PEAK CUT @ 145 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 155 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 170 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 240 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 340 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 380 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 450 CPS WITH 2.5 G PEAK INPUT	G PEAK OUT @ 600 CPS WITH 2.5 G PEAK INPUT	CHANN
1	3.0	5.5	2.8	2.8	3.0	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	1
2	.7	1.0	1.0	2.5	2.0	.8	1.0	3.0	2.5	2.0	1.0	1.0	1.5	2.0	1.0	2
3	.7	1.0	2.5	5.8	4.2	2.0	2.0	2.5	2.0	2.0	1.5	2.0	2.0	1.5	1.5	3
4	.7	1.0	2.5	5.0	4.0	2.0	2.0	2.5	2.0	2.0	1.5	2.0	2.0	1.5	1.0	4
5	.7	1.0	2.0	5.0	3.5	1.2	2.0	4.0	3.5	3.0	1.0	1.0	2.0	2.0	1.5	5
6	.7	1.0	1.5	4.0	3.0	1.0	2.0	3.8	3.5	3.0	1.0	1.0	2.0	1.5	1.0	6
7	.7	5.8	16.0	13.0	12.0	2.0	4.0	7.0	6.0	3.0	2.0	5.0	12.0	9.0	3.0	7
8	3.5	5.5	9.0	13.0	10.0	3.5	2.0	6.0	6.0	4.0	2.0	1.5	2.0	4.0	2.5	8
9	3.5	5.0	7.0	12.0	9.0	2.5	2.0	5.0	5.0	4.0	2.0	1.5	2.0	3.0	1.5	9
10	3.0	4.0	5.0	5.0	3.0	3.0	4.0	11.0	6.5	6.0	2.0	1.5	5.0	5.0	1.5	10
11	Not Recording	-	-	-	-	-	-	-	-	-	-	-	-	-	-	11
12	3.0	4.5	6.5	10.0	7.5	1.0	2.0	6.0	3.0	3.0	3.0	3.0	6.5	10.0	1.5	12
13	3.0	4.0	4.0	5.0	4.0	3.5	10.0	19.0	11.5	8.0	4.0	10.0	2.0	8.0	2.0	13
14	.7	1.5	2.5	4.0	3.0	1.8	3.0	4.0	3.0	2.0	1.5	1.5	2.0	1.5	1.0	14
15	3.0	4.5	5.0	5.0	3.0	1.8	6.0	9.0	6.0	7.0	2.0	6.0	2.0	1.5	2.0	15
16	3.0	4.0	5.5	7.0	5.0	1.0	2.0	4.0	4.0	2.5	2.5	2.0	5.0	6.0	5.0	16
17	2.0	3.0	3.5	4.5	3.5	1.5	3.0	5.0	4.0	3.0	3.0	6.0	10.0	7.0	1.0	17
18	1.0	1.0	1.5	2.0	1.5	1.2	2.0	5.0	3.0	2.5	2.0	4.0	4.0	4.5	1.5	18
19	2.0	5.0	10.0	16.0	12.0	4.0	4.0	4.0	8.0	3.0	1.0	2.0	3.5	7.0	2.0	19
20	2.0	5.0	10.0	15.0	10.0	3.0	2.0	2.0	7.0	3.0	1.5	3.0	4.0	7.0	2.0	20
21	1.8	3.0	9.0	18.0	13.0	5.0	5.0	5.5	10.0	4.0	1.5	1.5	2.0	3.5	3.0	21
22	2.0	4.0	7.0	14.0	10.0	2.0	3.0	3.8	16.0	6.0	4.0	4.0	14.0	4.0	3.5	22
23	.5	1.0	3.0	6.0	6.0	3.0	2.0	2.0	10.0	4.0	3.0	4.0	8.0	4.0	2.0	23
24	3.0	5.5	9.5	16.0	11.5	3.0	2.5	2.8	4.2	2.2	1.2	3.0	4.0	2.0	.8	24
25	5.0	8.0	10.0	12.0	7.5	4.0	8.0	9.0	26.0	14.0	6.0	6.0	3.0	8.0	2.0	25
26	.7	1.0	1.5	2.5	2.0	1.5	1.5	2.2	3.0	1.5	1.0	1.0	1.5	1.0	1.2	26
27	3.0	4.5	4.0	3.5	3.5	2.0	2.0	2.0	2.5	2.5	3.5	2.5	3.5	3.5	2.0	27
28	2.5	4.5	3.5	3.8	3.0	2.0	3.0	3.5	8.0	4.0	1.0	3.5	3.5	2.0	2.5	28
29	.7	1.8	3.8	5.0	4.0	1.8	1.5	1.7	4.0	3.8	1.8	2.0	2.2	1.0	2.0	29
30	3.0	6.0	8.0	13.5	9.0	2.0	2.0	2.0	2.1	2.5	2.0	3.0	2.5	2.5	2.0	30
31	4.0	7.0	8.0	11.0	7.0	2.5	4.0	4.5	11.5	7.0	3.0	5.0	3.5	2.5	1.5	31
32	1.5	2.0	1.5	1.8	1.5	1.5	1.5	2.0	4.0	2.0	1.0	1.0	1.5	1.2	1.2	32
33	3.5	5.0	9.0	16.0	12.0	5.0	4.0	4.0	4.0	2.0	2.0	2.0	2.0	1.5	1.0	33
34	Not Recording	-	-	-	-	-	-	-	-	-	-	-	-	-	-	34
35	.8	1.0	1.5	4.0	3.0	1.5	1.0	1.5	3.0	3.5	1.5	1.0	2.0	2.2	1.5	35
36	3.0	5.5	2.8	2.8	3.0	2.8	3.0	3.0	3.1	2.5	3.0	3.0	3.0	3.0	3.0	36
37																37
38																38
39																39
40																40

Table II (cont)

DATA SHEET: SINUSOIDAL VIBRATIONS — INPUT: ALONG THE LATERAL $Z_c - Z_c$ AXIS — CURVE # 3 — UNIT NO. 230

DATE TEST STARTED: — DATE COMPLETED: — RUN NO.

CHAN	G PEAK OUT @ 10 CPS WITH G PEAK INPUT	G PEAK OUT @ 70 CPS WITH G PEAK INPUT	G PEAK OUT @ 85 CPS WITH G PEAK INPUT	G PEAK OUT @ 110 CPS WITH G PEAK INPUT	G PEAK OUT @ 137 CPS WITH G PEAK INPUT	G PEAK OUT @ 140 CPS WITH G PEAK INPUT	G PEAK OUT @ 160 CPS WITH G PEAK INPUT	G PEAK OUT @ 180 CPS WITH G PEAK INPUT	G PEAK OUT @ 210 CPS WITH G PEAK INPUT	G PEAK OUT @ 240 CPS WITH G PEAK INPUT	G PEAK OUT @ 320 CPS WITH G PEAK INPUT	G PEAK OUT @ 350 CPS WITH G PEAK INPUT	G PEAK OUT @ 425 CPS WITH G PEAK INPUT	G PEAK OUT @ 475 CPS WITH G PEAK INPUT	G PEAK OUT @ 550 CPS WITH G PEAK INPUT	CHAN
1	Not Used															1
2	Not Used															2
3	Not Used															3
4	Not Used															4
5	Not Used															5
6	Not Used															6
7	Not Used															7
8	Not Used															8
9	2.5	4.0	14.0	4.0	4.0	4.0	2.0	2.0	4.0	3.5	4.0	6.0	2.0	2.0	2.0	9
10	Not Used															10
11	2.0	3.0	5.0	3.8	7.0	8.0	13.0	6.0	2.5	2.0	3.5	12.0	4.5	6.0	2.0	11
12	Not Used															12
13	2.0	3.5	6.0	3.8	12.0	18.0	10.0	4.5	3.0	2.0	3.0	5.0	2.0	2.0	2.0	13
14	Not Used															14
15	2.0	4.0	15.0	3.0	1.8	1.5	2.5	1.0	2.5	2.0	1.8	2.0	1.0	1.0	1.0	15
16	2.0	5.0	15.0	3.8	2.0	2.5	2.0	1.2	1.5	1.5	1.8	2.0	1.0	1.0	1.0	16
17	Not Used															17
18	Not Used															18
19	Not Used															19
20	Not Used															20
21	Not Used															21
22	2.0	4.0	4.0	3.8	12.0	17.0	10.0	5.0	3.0	2.5	4.0	5.0	2.0	2.0	2.0	22
23	2.0	4.0	9.0	1.8	3.0	6.0	1.5	1.5	8.0	2.0	3.5	2.0	2.0	2.0	1.8	23
24	Not Used															24
25	2.0	3.0	4.0	2.0	5.0	9.0	3.0	1.2	1.5	1.5	3.8	4.5	2.0	1.2	2.2	25
26	Not Used															26
27	Not Used															27
28	Not Used															28
29	Not Used															29
30	2.0	4.0	11.0	2.0	1.5	2.5	2.0	1.5	3.0	2.0	1.5	2.0	1.0	1.2	1.0	30
31																31
32																32
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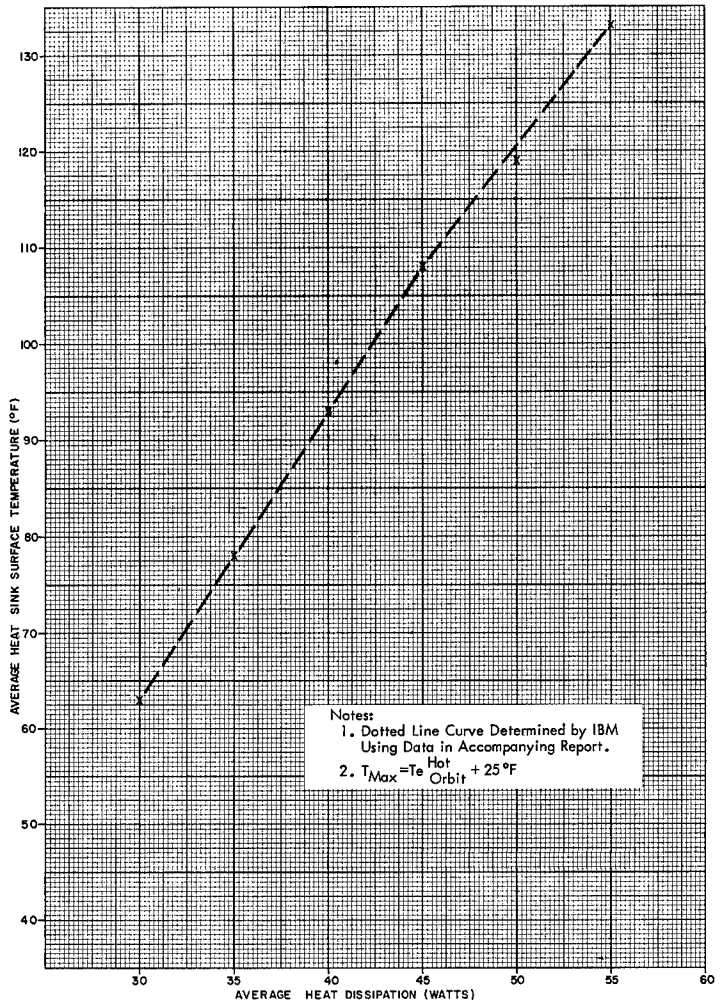


Fig. 19. Hot orbit—PPDS heat sink surface temperature.

The primary heat flow path from the circuit cells is from the components to the base of the cells, with some heat also being dissipated through the electrical connections. The coating or encapsulating material provided in the cells offers a conduction path from the components to the cell base. In the case of the logic panels the heat is transferred from the cell base to the panel and removed from the panel at the four corners which connect to the panel mounting structure, as shown in Figs. 7 and 8. Higher-heat-dissipating logic panels incorporate copper conducting strips which connect to front and rear headers on the panel, which in turn include mounting tabs for attachment to the panel mounting structure. The lower-heat-dissipating logic panels include corner brackets which attach to the panel mounting structure in the same manner as the conducting strip headers. The logic panel mounting structure or struts at the front of the unit provide a thermal path directly to the unit heat sink surface, i.e., are bolted to the unit front panel, while the struts at the rear of the unit tie to and provide a heat flow path to the top and bottom of the unit can.

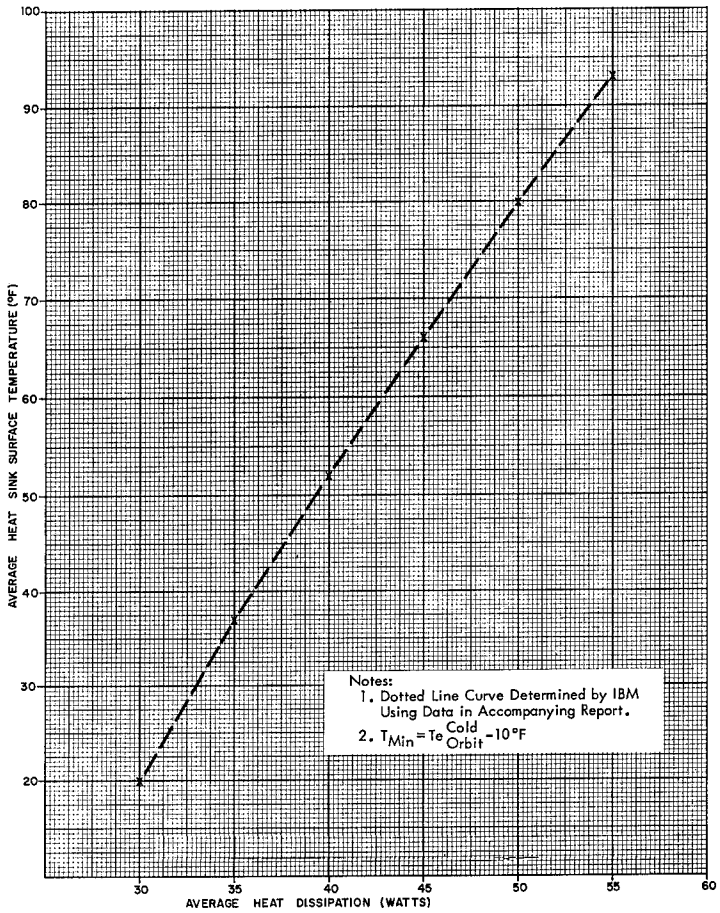


Fig. 20. Cold orbit—PPDS heat sink surface temperature.

The memory cell heat dissipation is transferred from the cell base to the memory panels, to the memory structure, and to the top and bottom of the unit case. The higher-heat-dissipating memory cells are encapsulated in a similar fashion as the logic panel corner cells, i.e., they have encapsulant built up to the cell cover. These cells are mounted in panels opposite the memory pressure plates, which are provided with copper conducting strips which contact the cell covers. In this manner two-dimensional heat flow is provided from these cells to the memory structure.

The PPDS power converter (Fig. 8) mounts directly to the top of the unit 230 case, providing an excellent heat transfer path from this unit to the unit heat sink surface. (The heat dissipation of the memory arrays is negligible.) These devices essentially will assume the temperature of surrounding structure in steady-state operation.

Provision for conduction paths from heat dissipating components to the unit heat sink surfaces required that all mechanical joints be made with the utmost care. Thermal conducting compound consisting of RTV11 filled with 33% lithefrax was applied to all joints to maximize contact area. This compound was also used between higher dissipating circuit cells and the

cell panels to increase the heat transfer effectiveness of this interface. The effect of conducting compound in this area is shown in Fig. 21.

Thermal Analysis

To permit analysis of the PPDS thermal design effectiveness an IBM 7090 three-dimensional heat transfer computer program was developed. Use of this program involves dividing all portions of the unit to be analyzed into rectangular parallelepipeds or nodes. Each node represents a segment of the total heat transfer path from the heat generating elements to the ultimate sink. The program is capable of handling up to 1000 nodes, and, in addition, six separate boundary condition forms can be handled simultaneously on each node face in the Cartesian framework. With reference to Fig. 22 the general program equation may be illustrated by considering all possible heat transfer paths for one node denoted by subscript j.

T_j'	Temperature of node j after some time interval
T_j	Original temperature of node j
$T_e, T_i, T_k, T_m, T_n, T_o$	Temperatures of surrounding nodes
ρ	Density of node j
C_p	Specific heat of node j
$(\Delta x \times \Delta y \times \Delta z)$	Volume of node j
$\Delta\theta$	Computing time interval
q	Heat generation of node j
h	Convection heat transfer coefficient
A, B, C	Constants dependent upon the cross-sectional area of thermal path considered or face area considered for radiation and convection

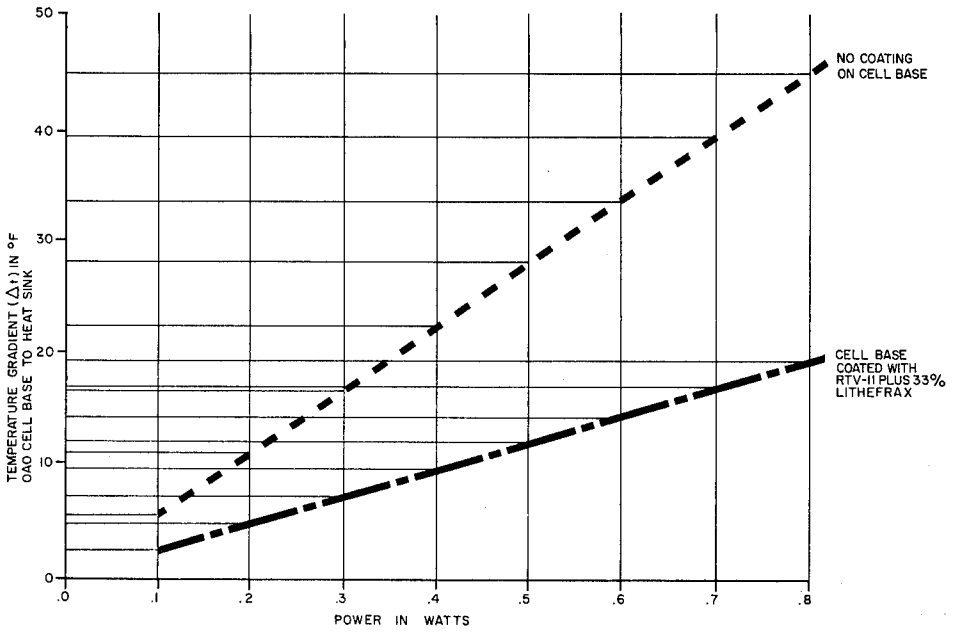
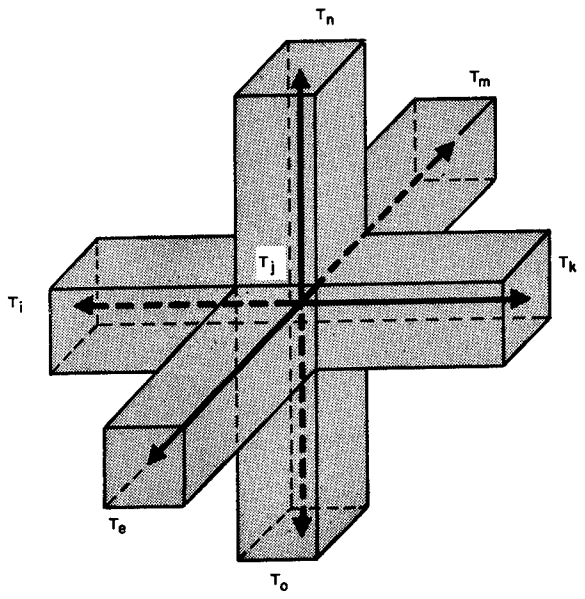


Fig. 21. Cell base to panel temperature gradients with and without RTV-11 at interface.



GENERAL EQUATION:

$$T_j' = T_j + \frac{A\Delta\theta}{(\rho c_p \Delta x \Delta y \Delta z)_j}(T_i - T_j) - \frac{A\Delta\theta}{(\rho c_p \Delta x \Delta y \Delta z)_j}(T_j - T_k)$$

$$+ \frac{B\Delta\theta}{(\rho c_p \Delta x \Delta y \Delta z)_j}(T_e - T_j) - \frac{B\Delta\theta}{(\rho c_p \Delta x \Delta y \Delta z)_j}(T_j - T_m)$$

$$+ \frac{C\Delta\theta}{(\rho c_p \Delta x \Delta y \Delta z)_j}(T_n - T_j) \quad \frac{C\Delta\theta}{(\rho c_p \Delta x \Delta y \Delta z)_j}(T_j - T_o)$$

$$+ \frac{q'''\Delta\theta}{(\rho c_p \Delta x \Delta y \Delta z)_j} \pm \frac{\sigma F\epsilon (T_j^4 - T_s^4)\Delta x \Delta y \Delta\theta}{(\rho c_p \Delta x \Delta y \Delta z)_j}$$

$$\pm \frac{h\Delta x \Delta y (T_j - T_s)\Delta\theta}{(\rho c_p \Delta x \Delta y \Delta z)_j}$$

Fig. 22. General equation for heat transfer program.

σ .. .. Stefan–Boltzmann constant for radiation

$F\varepsilon$ .. .. Combined geometric and surface property form factor for radiation

T_s .. .. Convenient sink or source temperature specified for radiation and convection. (Note: this temperature may or may not vary with time.)

Each node was geometrically placed in the computer network to simulate its position in relation to surrounding nodes. Care was exercised in providing contact areas from node to node commensurate with the actual unit design. Proper physical and thermal properties, along with nodal dimensions and heat generations were also assigned. For the PPDS solution, special end conditions in the form of radiation constants are relevant for the following:

1. Each of the unit's front panel nodes radiating to the internal vehicle skin.
2. The inside skin accepting radiation from the unit front panel.
3. The outside skin radiating to outer space (absolute zero).

In accordance with the above, each radiating unit node has the entire vehicle skin surface adjacent to the unit. Therefore, radiation form factors are calculated as such.

To minimize the computer time in obtaining steady-state solutions, lumped constants are placed in a matrix IBM 7090 computer format. Through an iterative process, temperature values are altered until all nodes are thermally balanced in all three coordinates.

Use of the program for the PPDS thermal analysis involved dividing each panel into nodes representing each cell position. The power converter was divided into nodes representing the various heat dissipating components. The units' structure and cases were divided into nodes to simulate the heat conduction paths from the cell panels and power converter.

To obtain a maximum of analytical data for each unit, computer solutions were performed on each unit half with approximately 900 nodal joints used for each section. Typical nodal breakdowns are shown in Figs. 23 through 25. In each case, the solution provided complete temperature profiles of the units as a function of interior conduction paths, unit heat dissipation, and spacecraft environment. To meet the component reliability temperatures mentioned earlier, an allowance was made for the temperature differential between operating component temperature and cell base temperature. This differential can only be evaluated empirically and is covered more thoroughly in the thermal test section.

However, with the allowance mentioned above, the computer solution did indicate cell panels heat sink sizing requirements. Furthermore, this sizing is accomplished taking full advantage of all possible modes of heat transfer, providing an optimum overall thermal design.

Thermal Vacuum Development Testing

Subassembly Testing. To establish circuit cell components to cell panel temperature gradients, a panel containing a representative sample of cells with varying heat dissipations was fabricated. The panel selected was a 9 × 6 matrix panel containing copper conducting strips and contained high-, low-, and medium-heat-dissipating cells. A representative sample of each cell type was thermocoupled by placing 36-gage copper constantan sensors on the highest-dissipating components and/or high-dissipating components close to the top of the cell. The inside of the cell base and the panel below each cell to be monitored were also thermocoupled.

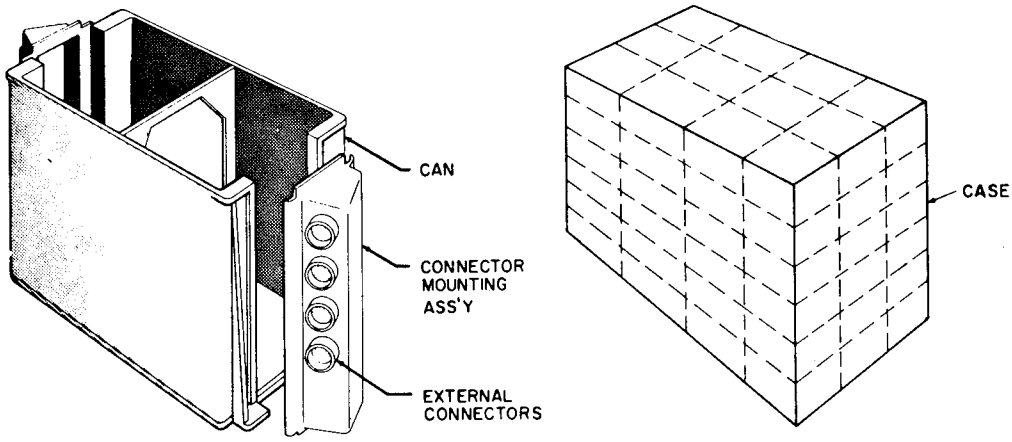


Fig. 23. Unit case.

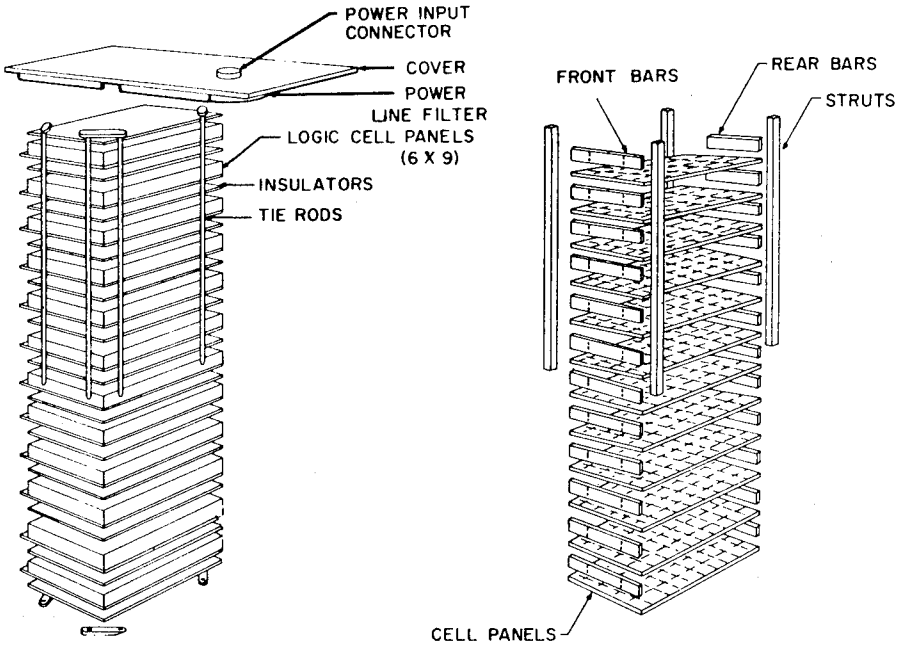


Fig. 24. Logic panel stack.

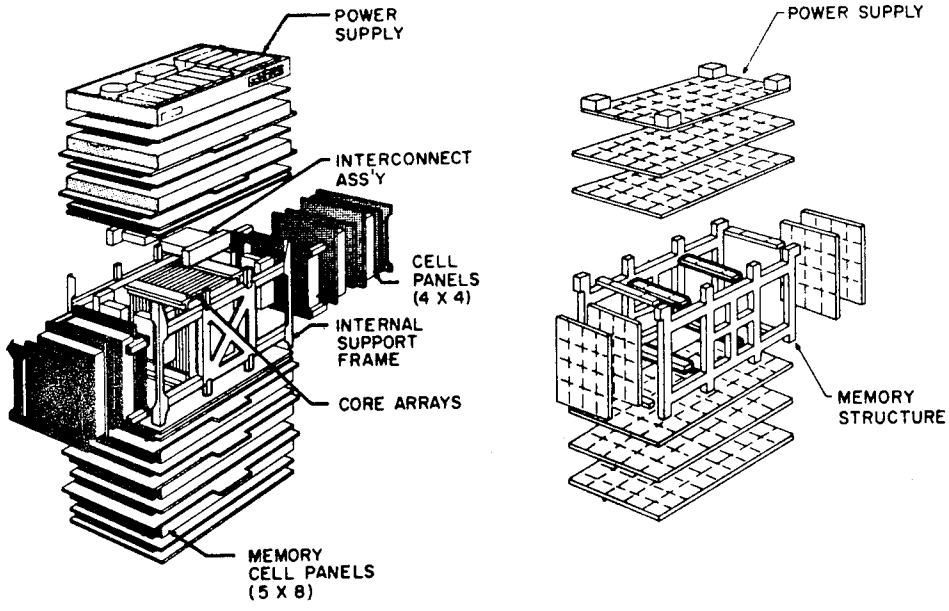


Fig. 25. Memory subassembly.

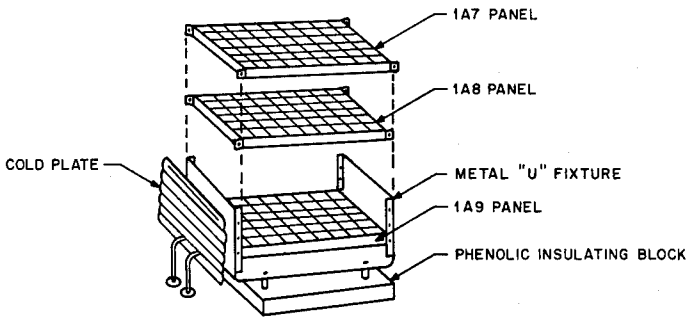


Fig. 26. Panel thermal test fixture.

The panel was installed in the test fixture (Fig. 26) between two thermal dummy panels to simulate actual installation conditions. The thermal dummy panels contained load resistors potted in cell cases to simulate the actual heat distribution on the system panels which were mounted above and below the test panel.

The test fixture with the panels was installed in a Model CR24 High Vacuum Equipment Corporation vacuum chamber with the test panel connected to test fixture so as to simulate its normal function in the system. The load resistors in the dummy panels were connected to a power supply and the voltage controlled to simulate their normal heat dissipation. A liquid-nitrogen-cooled cold plate was located approximately 1 in. from the front of the fixture to provide radiation heat transfer from the fixture to the cold plate. The cold-plate temperature was controlled during the test to stabilize the panel at a representative temperature as obtained from the thermal analysis. The test fixture and panels were wrapped with Mylar-backed aluminum foil insulation to minimize radiation from the panels to the vacuum chamber walls, and thermal insulators were installed between the test fixture base and the chamber. The vacuum chamber pressure was held at 10^{-6} mm Hg during the test. The maximum cell component to panel temperature gradients determined from this test for the cells monitored were as follows:

High-heat-dissipating cell	25°F
Medium-heat-dissipating cell	25°F
Low-heat-dissipating cell	15°F

In addition to the test described above, various other high-heat-dissipating cells, not used in the test panel, were evaluated to be certain that the component to panel temperature gradient of 25°F was not exceeded in other cell types. This evaluation was conducted on a small test panel containing three cell positions (Fig. 27). The cells to be tested were thermocoupled in a fashion similar to the technique described for the above test as was the test panel below the cells. The test was conducted in a vacuum chamber under 10^{-6} mm Hg pressure and the cells normal operation was achieved with test equipment. The 25°F temperature gradient was found valid for all cells tested except for one cell type which dissipated 800 mW. The component-to-panel gradient for this cell type was found to be 35°F.

Unit Testing

(*a*) *Description of Test.* The mock-up units used for vibration development testing were also used for thermal testing. As already described, the mock-up unit cases and structure simulated the final unit construction in every detail. The cell panels contained thermal conducting strips where required, but the printed wiring did not simulate final unit design. Instead the circuitry on the thermal test unit cell panels was arranged to supply power to load resistors encapsulated in cell cases. Each cell contained a load resistor, in lieu of operational circuitry,

which was rated and powered so as to simulate the heat dissipation of the actual circuit cell in the panel location. A system power converter was installed in the thermal mock-up of the 230 unit and connected to dummy loads to simulate the system loads. The same mock-up memory arrays used for vibration testing were used for thermal testing.

The thermal mock-up units were tested individually in a High Vacuum Equipment Corporation vacuum chamber 4 ft in diameter × 8 ft long. The units were generously instrumented with 36 gage copper constantan thermocouples, employing 294 thermocouples in the 140 unit and 248 thermocouples in the 230 unit. The instrumentation was installed so as to obtain representative maximum and minimum cell panel temperatures, panel conducting strip headers on corner bracket temperatures, power converter component temperatures, memory array temperatures, and representative packaging structure temperatures. For high-temperature tests power was applied to the units to simulate their maximum average heat dissipation per orbital time period of 110 min. For low-temperature tests the units were powered to simulate their minimum orbital average heat dissipation. The present calculated heat dissipation of each unit is as follows:

Unit	*Test condition*	*Orbital average heat (max)*	*Dissipation (min)*
140	Hi Temp	38.1 W	
140	Lo Temp		29.7 W
230	Hi Temp	42.0 W	
230	Lo Temp		41.6 W

During the tests the units' heat sink surface was stabilized at the average temperature determined for hot orbit and cold orbit qualification environment. The method used for determining these temperatures has been described. The average unit heat sink surface temperature was controlled using a cold plate, which was located approximately 1 in. from the units' front

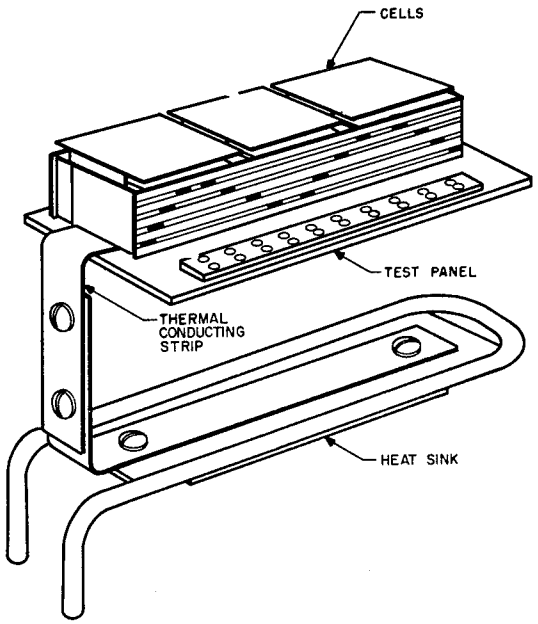


Fig. 27. Cell thermal test fixture.

panel in the vacuum chamber (Fig. 28). The cold-plate surface was painted with the same high-emissivity black epoxy paint used on units and contained tubes through which liquid nitrogen was circulated. The cold-plate temperature necessary to obtain the desired unit heat sink surface temperature, using radiation heat transfer from the units to the cold plate, was determined. Thermocouples on the cold plate were then tied into a Minneapolis–Honeywell controller, which operated a proportional valve in the liquid-nitrogen supply lines to obtain this temperature on the cold plate.

To simulate the thermal conditions of the OAO satellite installation, the units were set in the vacuum chamber on thermal insulators to minimize conduction heat transfer between the unit cases and the vacuum chamber. The units were installed in a shroud faced on five sides with 25 layers of Mylar-backed aluminum foil (Fig. 28) to minimize radiation heat transfer between the units and the vacuum chamber walls.

Test and Analysis Results

The temperature values predicted for the PPDS cell panels, power converter components, and memory arrays from the high- and low-temperature tests and from analysis for orbital operation are shown in Table III. Package structure temperatures except for the unit heat sink surfaces are not included in Table III.

Using the panel temperatures in Table III and the component-to-panel temperature gradients obtained from the subassembly tests indicates that the initial design requirement that all cell components operate at or below their maximum allowable surface temperature of 185°F. The maximum expected component temperatures for each unit is as follows:

2A11 .. .. CT 41 = Panel T(160) + Cell T(25) = 185°F
4A10 .. .. CT 30 = Panel T(145) + Cell T(35) = 180°F

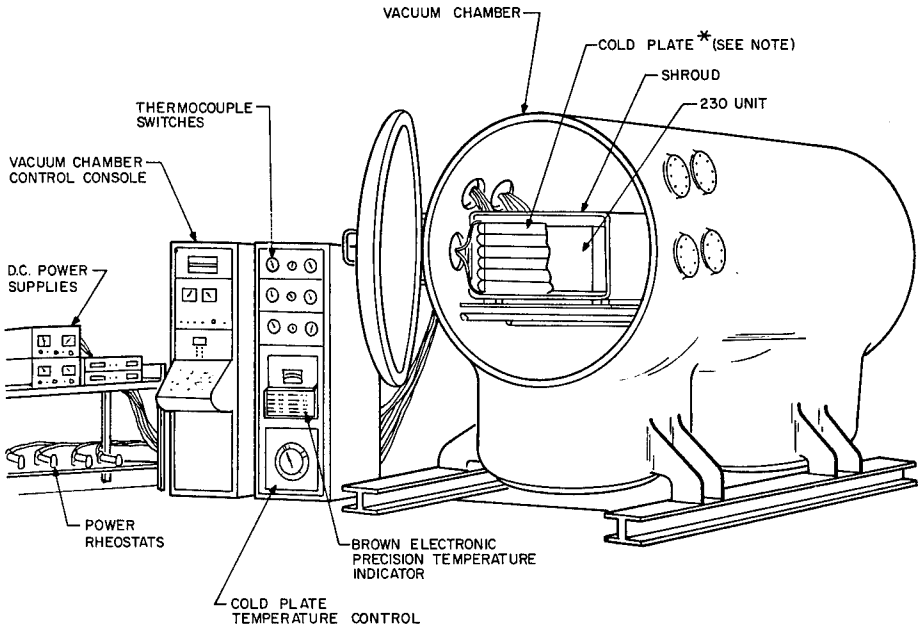


Fig. 28. Unit thermal test setup.

Examination of the panel temperatures obtained during low-temperature tests indicated that the cell components would not be exposed to temperatures below their minimum temperature value of 53°F. The minimum expected component temperature is

$$\text{CT 220} = \text{Panel 1A7 T(39)} + \text{Cell T(15°F)} = 54°\text{F}$$

The maximum operating component temperature in the power converter on the 2N1100 germanium power transistors was 143°F, or below the maximum allowable temperature of 160°F. The minimum temperature on this component was found to be 72°F, which is above its minimum allowable temperature of 53°F.

The maximum and minimum memory array temperature obtained during thermal vacuum testing were 134 and 44°F, respectively. This is within the allowable temperature range of the arrays which is from 153 to 17°F.

Examination of the package structure temperatures obtained during thermal vacuum testing indicated that expected temperature gradients of 0.5°F/W across mechanical interfaces were not exceeded except at the power converter–230 unit case interface. A temperature gradient of 8°F was obtained at the connection in this interface. The excessive ΔT in this area was found to be due to a below-tolerance dimension on the overall height of the command storage–power converter assembly, which resulted in a poor interface or a slight gap between power converter and unit 230 case.

The results of the thermal vacuum test when compared with the results of the IBM 7090 computer analysis showed the following correlation:

Logic Stacks (9 × 6 panels)	2–10°F, or 6°F avg. T
Power Converter	1–3°F, or 2°F avg. T
Memory Arrays	1–2°F, or 1°F avg. T
Memory Panels	1–14°F, or 8°F avg. T

As shown relatively good correlation was obtained in all areas.

CONCLUSIONS

The objective of this paper has been to present the packaging design approach which was used for a relatively complex electronics system for long-duration space application, together

TABLE III

Unit 140			Unit 230		
	Temp., °F			Temp., °F	
Thermocouple location	max	min	Thermocouple location	max	min
Heat sink surface-avg.	92	27	Heat sink surface-avg.	104	62
Panel 1A3 under CT 2	133		Panel 3A1 under CT 48	140	
Panel 1A3 under CT 20		51	Panel 3A1 under CT 19		78
Panel 1A5 under CT 250	140		Panel 3A5 under CT 18	150	
Panel 1A5 under CT 13		45	Panel 3A5 under CT 18		73
Panel 1A7 under CT	133		Panel 3A11 under CT 18	134	
Panel 1A7 under CT 220		39	Panel 3A11 under CT 13		67
Panel 4A9 under CT 340	150		Panel 2A3 under CT 87	134	
Panel 4A9 under CT 33		49	Panel 2A3 under CT 22		78
Panel 4A10 under CT 30	145		Panel 2A7 under CT 87	140	
Panel 4A10 under CT 220		49	Panel 2A7 under CT 45		82
Panel 4A14 under CT 420	128		Panel 2A11 under CT 41	160	
Panel 4A14 under CT 220		44	Panel 2A11 under CT 30		82
Memory arrays	119	44	Memory arrays	134	92
			Power converter-2N1100 transistor	143	102

with some detail on the development testing necessary to check the design for expected environmental extremes.

In the process of the PPDS design a respect for the complexity of the thermal design problem for space application was gained. It is believed that the proper application of a program such as outlined above can be of tremendous assistance in this area. It would be urged that the entire industry cooperate to make available information on vacuum stability of nonmetallic materials. This could be a real asset in expediting design and fabrication of space electronics equipment.

8068

Honeywell Electronic Packaging for Apollo

MAX CALLEN AND PAUL MAYO
Minneapolis–Honeywell Regulator Company, Minneapolis, Minnesota

The Apollo program, being our nation's most extensive manned space venture, presents a special challenge in the field of electronic packaging. This paper describes the techniques which Honeywell is utilizing to meet this challenge in the packaging of electronics required for the Apollo Stabilization and Control System. The design provides for in-flight replacement of electronic subassemblies which are capable of withstanding high vibration and continuous operation in a vacuum. It incorporates a unique method of transferring heat from the electronic parts to the spacecraft cooling system.

INTRODUCTION

THE APOLLO PROGRAM, presently our nation's most ambitious manned space venture, offers a special challenge in the field of electronic packaging. This paper describes the techniques Honeywell, as a subcontractor to North American Aviation, is using to meet packaging requirements of the stabilization and control system for the Apollo Command Capsule.

CONSTRAINTS

At the start of the program a number of constraints were established for the design of the control and display electronics packaging. The most significant are:

1. Severe vibration
2. Operation in a vacuum
3. In-flight maintenance in a zero g environment
4. High reliability

Vibration

It is anticipated that the Apollo vehicle will undergo severe vibration during blast-off and re-entry. Therefore, initial vibration qualification requirements were established of the order of 8 g's peak sinusoidal superimposed on 6.2 g's rms random. Honeywell saw two alternatives to achieve satisfactory operation under these conditions:

1. Make the packaging stiff enough to raise the natural frequency above the highest frequency required. For the package chassis this would mean considerable "beefing up" of the structure resulting in a serious weight penalty.
2. Accept a relatively flexible structure and provide damping by adding resilient material to it. This would serve to attenuate the resonant peaks.

Because of the weight saving and because the natural response for a damped structure is much lower than for a stiff one, the second approach was selected.

Vacuum Operation

A second important constraint was the requirement that the electronics operate in a vacuum. Vacuum operation in the Apollo vehicle dictates that all heat be removed from

electronic components by conduction only. Radiation provides little assistance because the design temperature is relatively low. Thus thermal paths were required from the heat-producing components to the vehicle cooling system.

In-Flight Maintenance

Because the astronauts must be able to maintain all electronic assemblies during flight (zero *g* environment) while wearing a pressure suit, easily accessible packages with completely replaceable card construction were required.

High Reliability

The reliability requirements for the stabilization and control system are of the order of 0.995 for mission accomplishment and 0.999 for crew safety. Solutions to this constraint revolved around stringent observance of qualification and testing techniques such as those used on the Minuteman program. Another aid to solving the problem was to minimize the temperature and vibration to which the components would be exposed.

SOLUTIONS

Introduction

When designing the packaging, Honeywell attempted to solve all constraints concurrently. The resulting design, therefore, is a compromise to meet all the problems.

Chassis Structure

The basic electronic package is called an Electronic Control Assembly (ECA). Five are used in the Apollo Command Capsule to provide all necessary electronic circuitry for the stabilization and control system and associated displays. The ECA is packaged in a drawer shape which slides into a corresponding space in the equipment bay. The equipment bay structure in turn provides physical support, electrical interface, and conductive cooling.

The ECA chassis (Fig. 1) contains replaceable electronic assemblies or cards. The chassis consists of vertical struts, superstructure, and fixed portions of the card-mounting clamps, all dip brazed to a base plate. The base plate then serves as the primary structural member of the chassis assembly.

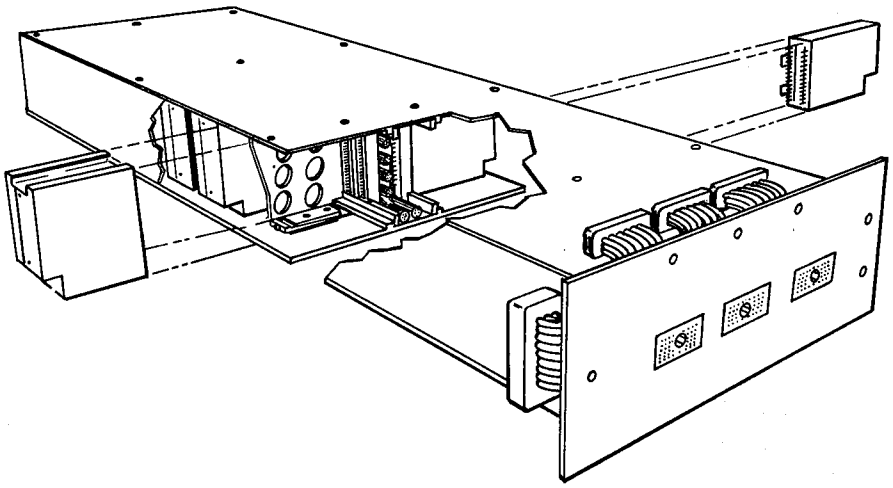


Fig. 1. Electronic control assembly ECA; exploded view.

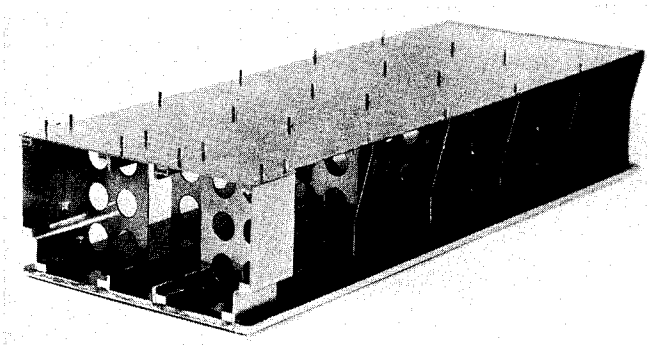


Fig. 2. Chassis assembled for dip brazing.

The dip-brazing technique used by Honeywell is as follows. The parts are assembled as shown in Fig. 2. Prior to brazing, the assembly is held together by tabs protruding through slots in the base. The tabs are twisted slightly to hold the assembly secure. After brazing the tabs are ground off flush with the surface.

Wherever two surfaces are to be joined, a thin (approximately 0.001 in.) layer of aluminum brazing alloy is placed between the mating surfaces. The complete assembly is then dipped into molten alkaline brazing flux heated to a temperature about 25°F below the melting point of the structural surfaces.

Because of the high, uniform temperature, the structure comes out of the bath completely stress relieved. Heat treating restores about 98% of the aluminum's original properties.

Advantages of dip brazing include:

1. Light weight
2. Thin sections can be handled easily
3. Retention of almost all of the strength of the prebrazed material
4. Process is quick and economical compared to casting and machining

For the most part, ECA design was dictated by two of the constraints: vibration requirements and conductive cooling for vacuum operation. Honeywell's design was based on a compromise between these two requirements. In other words, the design had to utilize the advantages of damping to overcome the weight and response problems by incorporating special structural techniques in the replaceable electronic assemblies. These same assemblies provide thermal paths to the chassis base, which is clamped to the vehicle's liquid-cooled cold plate.

Module Structure

The electronic parts are arranged in welded, cordwood-stacked, potted modules with component leads machined flush with the surface of the module. These are constructed with components arranged vertically between two parallel jig-wafers. Imprinted jig-wafers indicate the schematic designation, component location, and component polarity where necessary. Connecting bus routing and flags for top and bottom views of the module assembly are also shown on the jig-wafers. The components may be laid out on a coordinate system or randomly located. Due to irregularly-sized components, random location affords maximum component packaging density.

Card Structure

The individual modules are assembled into replaceable electronic cards. The same vibration problem noted in the design of the chassis affected the design of the replaceable card assembly. The card had to be made strong enough to support the potted, welded electronic part modules but still flexible enough to avoid the weight penalty associated with the brute-force method of overcoming vibration.

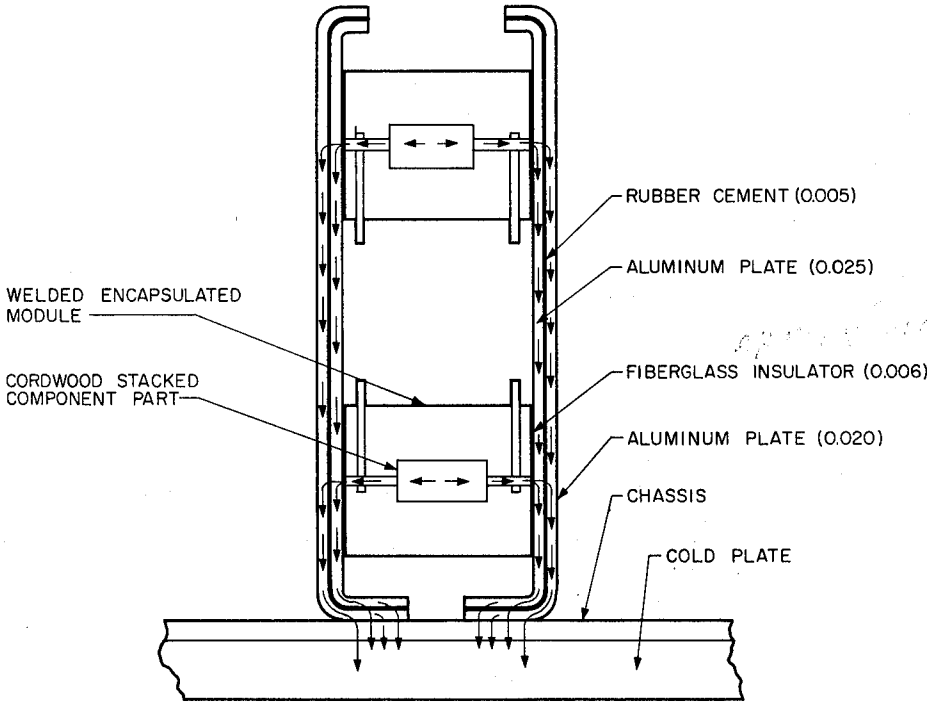


Fig. 3. Electronic card thermal paths.

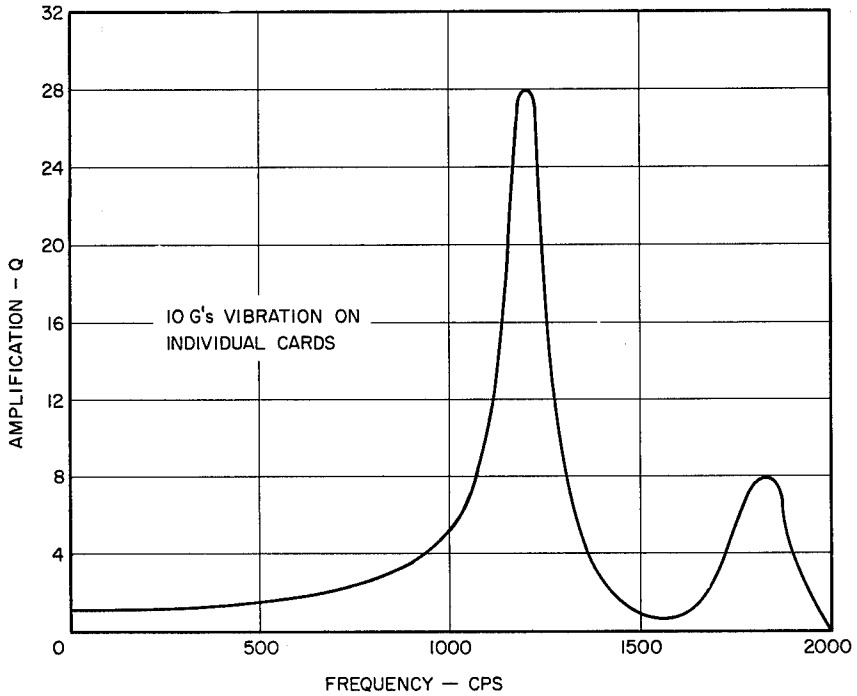


Fig. 4. Vibration of nonlaminated cards.

These cards are approximately $3\frac{1}{2}$ by 4 in. with thickness varied between 1.0 and 3.0 in., depending upon the type of components being used. The sides of each card are laminated of a sheet of elastomer between two sheets of aluminum. These sides provide structural support of the electronic components, vibration damping, and heat conduction from the components to the chassis. Thin epoxy fiberglass insulators are placed between the module and the aluminum sides of the card. As shown in Fig. 3, the heat generated in each component is transmitted along its leads, across the thin insulator, into the aluminum side plates, and then down to the chassis base which is in direct contact with the cold plate. This allows the units to meet the conductive cooling requirements necessary for vacuum operation. Electrical connections between the welded modules and the connector are made with conventional point-to-point wiring.

It was shown that point-to-point wiring within the card assembly represented reliability improvement over printed wiring cards.

RESULTS

Figure 4 illustrates the vibration amplification of a card assembly similar to that described except that the sides are made up of solid aluminum sheets rather than laminated ones. It shows a peak amplification of 28, which would be unacceptable.

Figure 5 shows the same type of data for the laminated design. Here the amplification has been reduced to a maximum of 6.

Figure 6 shows the maximum response of the chassis itself. Note that the natural frequency is different from the natural frequency of the cards. Thus, the natural frequencies of the two structures cannot reinforce one another. In fact, as is shown in Figure 7, each structure tends to attenuate the response of the other.

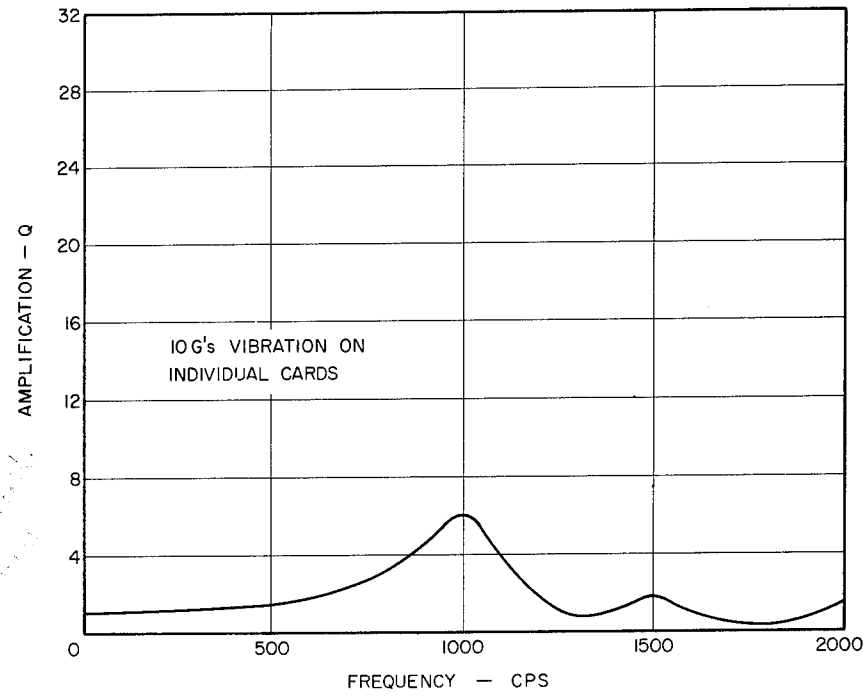


Fig. 5. Vibration of laminated cards.

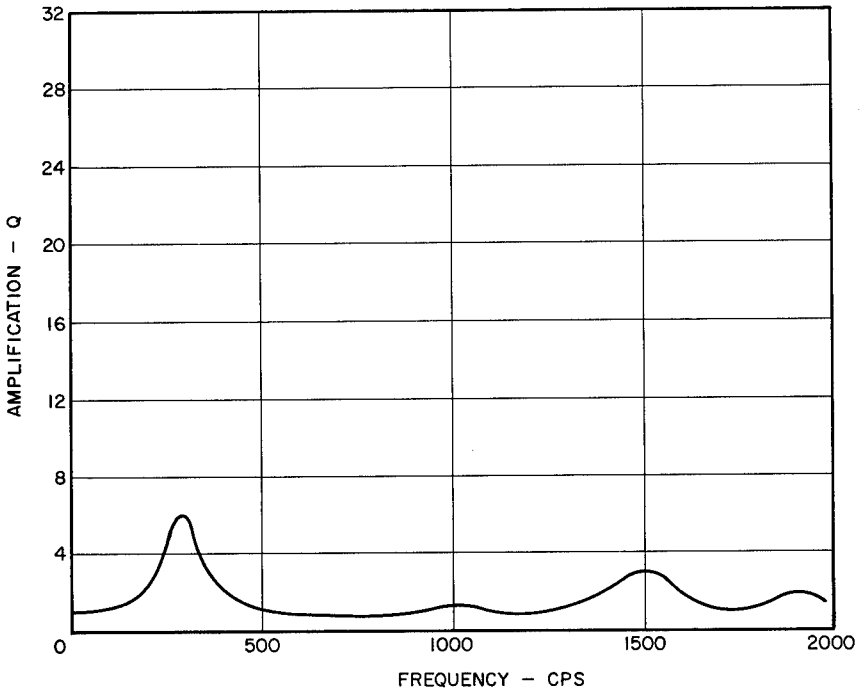


Fig. 6. Ten g's vibration of chassis—longitudinal (response at top rear of chassis).

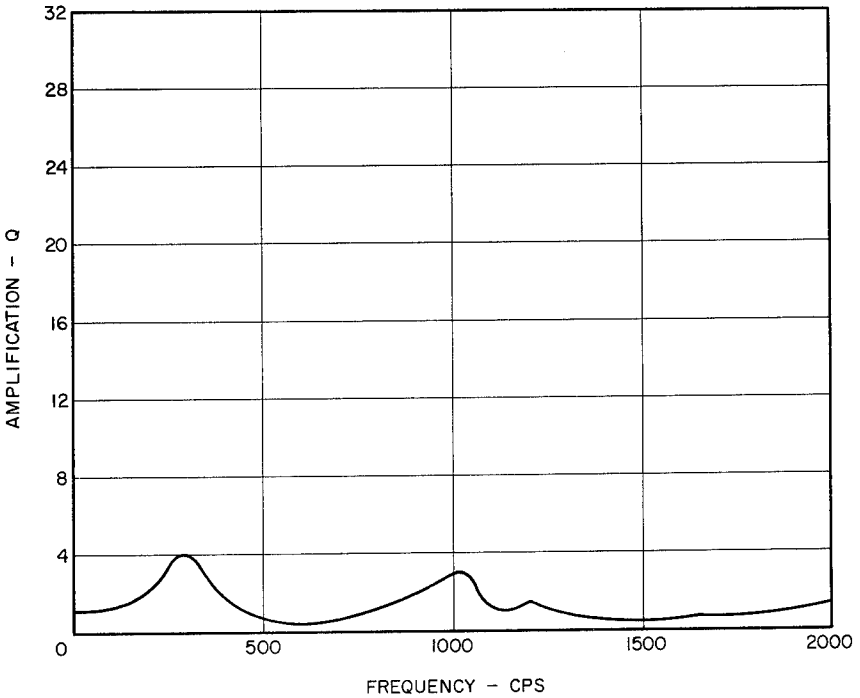


Fig. 7. Ten g's vibration of card mounted in chassis (response at center of card).

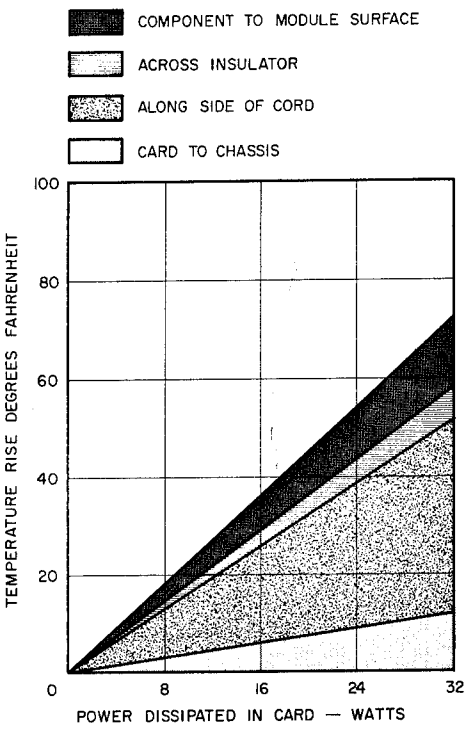


Fig. 8. Temperature rise of hot spot in welded module potted in Stycast and bolted to both sides of card.

Figure 8 illustrates the temperature drops encountered in the various portions of the structure from the component to the base of the unit which is in direct contact with the cold plate. The greatest temperature drop is along the side of the card. Thus the thickness of the card side was determined as a compromise of weight *vs.* temperature rise and card stiffness. The majority of cards operate under 5 W per card. The worst case is 32 W maximum instantaneous but at a low duty cycle (5% or less).

Many tests and analyses have been run on the various parts which make up the ECA and on the assembled ECA's themselves. Test results demonstrate that the design is performing up to qualification requirements. Specifically, the tests pointed up the following characteristics:

1. Maximum vibration amplification is under 4.0. This substantially solves the vibration constraint.
2. In a hard vacuum, the thermal rise from the cold plate to the component is approximately 2.4°F/W. This adequately solved the heat-removal problem.
3. Each plug-in card is easily removable for in-flight replacement even under zero-*g* conditions.

8069

System Packaging Design of a Digital Flight Control Computer

J. J. OKADA
Advance Missile Technology, Douglas Aircraft Company, Santa Monica, California

The Douglas Advanced Electronic Program has developed a packaging system for a general-purpose airborne computer to meet missile and space-borne flight environments. The Digital Flight Control Computer is composed of seven major sections: arithmetic unit, control unit, memory, memory circuitry, clock, power supply, and input-output unit, and contains approximately ten thousand components. The computer system logic diagram was analyzed to determine how much design standardization was possible. It was found by actual function count that gates and flip-flops accounted for 90% of the computer circuitry. An examination of these logic functions showed ten different gates and three different flip-flops. To simplify the 13 function types, high- and low-power gates were combined through circuit changes; and to reduce the variety of functions, extra diodes were placed in some of the circuits. These changes resulted in an acceptable level of standardization where only four-function types satisfied the needs of 90% of the computer circuitry. Layout packaging of the four functions further decreased the differences in the four basic logic building blocks. Components were carefully arranged so that the same intraconnection scheme could be used for several functions, which made possible fabrication of some 700 gates and flip-flops from only four intraconnection patterns and resulted in savings in manufacturing costs owing to use of prefabricated intraconnections. The design discussed not only provides adequate protection for environmental conditions and heat rejection, but indicates how economies in cordwood module fabrication can be realized with careful planning.

INTRODUCTION

AT DOUGLAS, the Advanced Electronic Development Program is aimed at selecting systems for future applications and resolving the problems associated with these systems. A significant part of the Program has been the development of a general-purpose airborne computer, called the Digital Flight Control (DFC) Computer. This computer, built with printed circuit cards, has undergone extensive evaluation tests. The system design has been and will continue to be upgraded to accept new components and to meet more demanding system requirements.

During the packaging study, it was decided that a computer model would be built as well as a partially functional thermally simulated prototype. An 1100-component portion of the arithmetic and control unit was selected as the functional part of the prototype. The package design and the computer model have been completed, and fabrication of the prototype computer is well underway.

This paper describes the packaging design for this computer to meet missile and space-borne flight environments. The design includes system organization from the packaging viewpoint, analysis of cost *vs.* minimum number of subassemblies, use of cordwood module and matrix techniques, module design for interconnection simplicity and manufacturing economy, mechanical strength, and heat dissipation.

SYSTEM DESCRIPTION

The DFC system specifications are summarized as follows:

a. Random access memory cycle time: 1 μsec
b. Clock pulse repetition frequency: 1 Mc
c. Operation temperature: -55 to 100°C

The computer is composed of seven sections: arithmetic unit, control unit, clock, memory, memory circuitry, power supply, and input–output unit.

The *arithmetic unit* adds, subtracts, multiplies, and temporarily stores solutions to computations. It is composed of 197 gates and 37 flip-flops representing 2250 components.

The *control unit* routes information and instructions between units, keeps track of where the information is located, and generates signals to control and sequence the computer operations. It is composed of 434 gates and 29 flip-flops representing 3740 components.

The *clock unit* generates timing pulses to synchronize the computer operations. It is composed of a clock oscillator, an amplifier, a delay line, a flip-flop, several gates, and 16 driver circuits. These circuits represent 440 components.

The *memory* stores information and instructions and can have this stored data altered electronically. The size, power requirements, and number of connections of the memory for the flight package were based on a Burroughs thin-film memory.

The *memory circuitry* is an interface between the memory and the rest of the computer. It selects the cells within the memory to write in and read out data. It also amplifies signals coming from the memory. The memory circuitry is composed of 44 driver circuits, 12 amplifiers, 20 flip-flops, 7 gates, and a 16 × 16-diode selection matrix. These circuits represent 2670 components.

The *input–output* unit is the interface between the computer and the missile or space vehicle system. It would contain analog-to-digital converters. This unit is in the process of being developed for the operating computer and is not included in this design.

The *power supply* converts 28-V missile power to ± 6 V and $+12$ V. It contains 125 components and dissipates 17 W of power.

It was apparent from the composition of six of the seven major sections of the computer that simplifications and economies through standardization could best be achieved in the arithmetic and control units. By actual function count, the flip-flops and gates account for 90% of the computer circuitry, excluding the input–output unit. Therefore, these logic functions were selected as the primary level of standardization.

ARITHMETIC AND CONTROL UNITS BREAKDOWN BY FUNCTIONS

Original Breakdown

Although the arithmetic and control units are composed of only gates and flip-flops, there are variations within these functions. (See Figs. 1 and 2.) First, there are low-power gates that can drive three functions and high-power gates that can drive six functions. Next, the number of inputs to both high- and low-power gates varies from one to five. Finally, the number of set inputs to flip-flops differs to yield three types of flip-flops. Table I shows the breakdown of these function variations. It also shows the penalty, in the increased number of diodes, incurred in decreasing the types of variations. Figure 3 is a graph of the penalty in diode quantity *vs.* the number of function variations.

Simplified Breakdown

Fortunately, the circuitry for the gates was simplified at this point, and the penalties were reduced for decreasing the number of function types. Figure 4 shows the circuit schematic for a combined high- and low-power gate. The benefits of a *combined high- and low-power* gate are not easily appreciated. For that reason, the previous section was put into this paper as a comparison in function trade-offs.

TABLE I

Arithmetic and Control Unit Function Breakdown and Trade-offs

Function	Quantity	After 1st trade-off	After 2nd trade-off	After 3rd trade-off	After 4th trade-off
One-input low power gate	166	166	166	0	0
Two-input low power gate	170	170	170	336	0
Three-input low power gate	67	67	0	0	0
Four-input low power gate	32	0	0	0	0
Five-input low power gate	28	60	127	127	463
One-input high power gate	120	120	120	120	0
Two-input high power gate	28	0	0	0	0
Three-input high power gate	11	39	0	0	0
Four-input high power gate	6	0	45	0	0
Five-input high power gate	3	9	3	48	168
One set, two reset flip-flop	44	44	44	44	0
Two set, two reset flip-flop	17	0	0	0	0
Three set, two reset flip-flop	5	22	22	22	66

13-function types	9-function types	8-function types	6-function types	3-function types
Penalty				
Number of diodes	93	250	461	2137
% of total components*	1.4%	3.8%	7.9%	32.5%
Cost of diodes	$298.00	$800.00	$1475.00	$6411.00
% of component cost†	1.7%	4.6%	8.6%	39.5%

* In arith.-control units
† Prices based on quantities for one computer.

Table II shows the simplified trade-offs now possible by the elimination of the difference in fabricating high- and low-power gates. Penalties for the simplified functions are plotted in Fig. 3 as a comparison with the initial design. The third trade-off in Table II was selected as the function variation breakdown to be used for the design. Although a less expensive penalty is incurred with the second trade-off (Table II), it was discarded because the requirements for three-input gates were expected to grow and the relative penalty difference between trade-offs No. 2 and No. 3 is small.

LOGIC FUNCTION PACKAGING

Functional Packaging

Upon close examination it is clear that the four-function types selected are really only two types to the package designer. The one-input, three-input, and five-input gates differ only by input diodes. Thus, it is possible to design one configuration for all gates. The components to be used in these function modules are described in Fig. 5. Layouts of these functions are shown in Figs. 6 and 7. The logic function modules were sized to $\frac{1}{3}$-in. increments for convenience in the next level combination.

Locations of the ground, -6-V, $+6$-V, and $+12$-V input leads were chosen for a specific purpose. Each is placed in sequence on the diagonal of a module. When the modules are oriented in prescribed arrangements, the power connections form concentric rectangular patterns (see Fig. 8). All signal connections are made on a second level of interconnection because of the interconnection density and for manufacturing simplicity.

Function Interconnection

Several approaches were available for interconnecting these function modules. The first method evaluated was to interconnect approximately 116 logic functions on one interconnection block. These modules, which would be freeze-coated, offered a lightweight and low-cost replacement approach. This method has the following undesirable features: (1) Ruggedness is sacrificed for high vibration due to lack of a mechanical attachment. (2) Some handling problems are caused by the lack of a solid rectangular block construction. (3) A complex interconnection is required where an average of approximately 65 connections would be required per square inch. For 16 in.^{2} (4 × 4 in. assembly), 1040 connections and their interconnections would be required. (4) If conduction is considered as the only method of transferring heat, a large temperature difference would exist from the components to any heat sink because only the component leads could conduct away the heat. This point is discussed in more detail in the thermal analysis portion of this paper.

The second approach considered and chosen for this analysis was to build modules containing functions as submodules. Figure 9 shows the possible combinations available for a standard 1 × 1 in. module. Examination of the arithmetic and control logic diagram indicates that ninety 1 × 1 in. module types would be required out of a total of 144 modules. This would indicate that only a minimal effort should be expended to obtain similarities in the

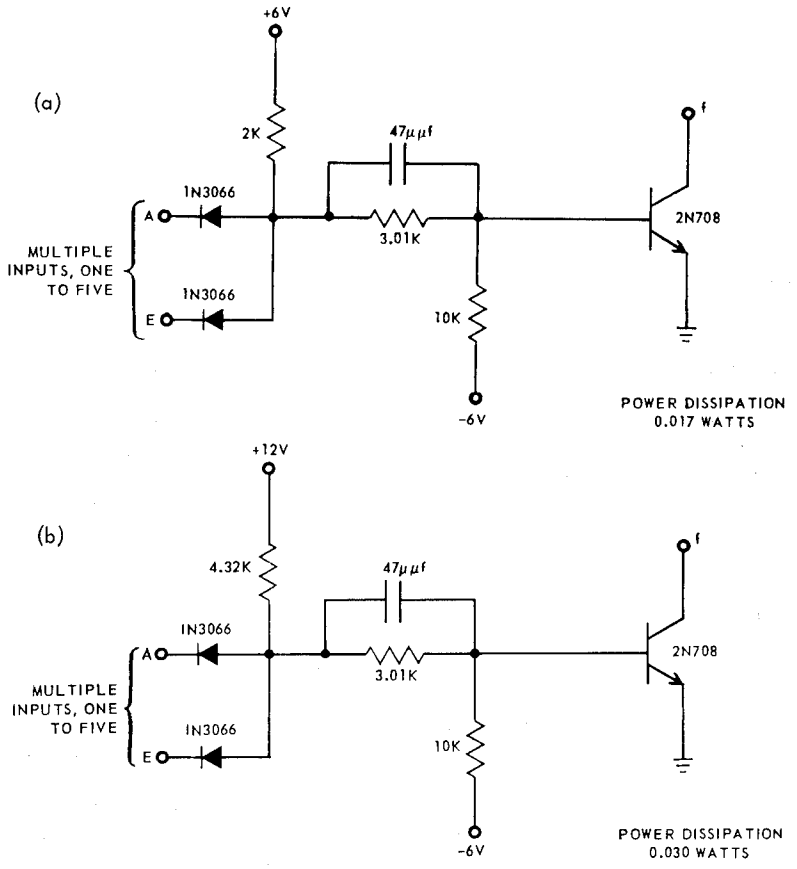


Fig. 1. Sheffer stroke gate circuit configurations: (a) low-power stroke gate; (b) high-power stroke gate.

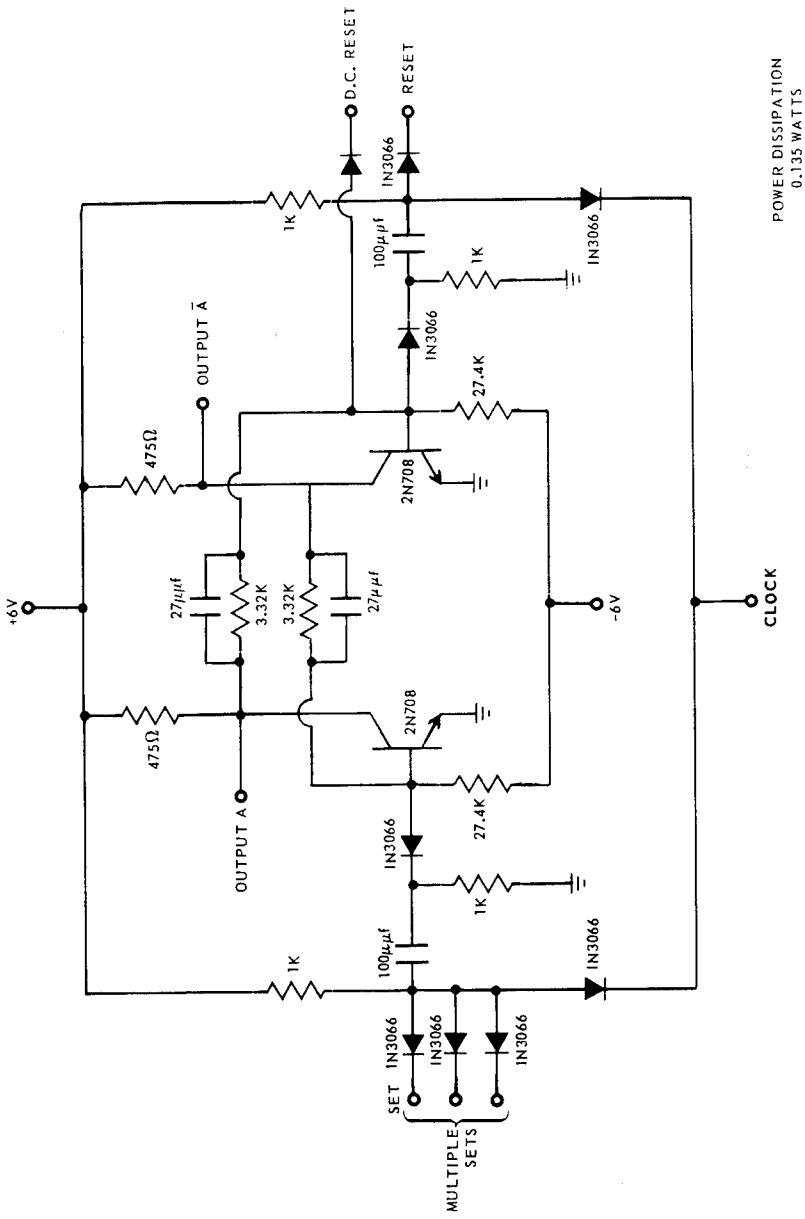


Fig. 2. R-S flip-flop.

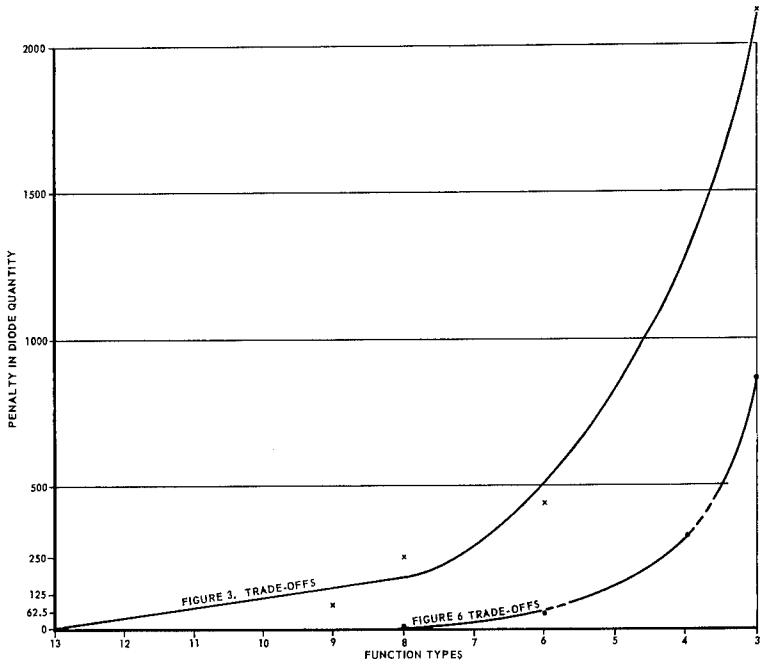


Fig. 3. Diode penalty.

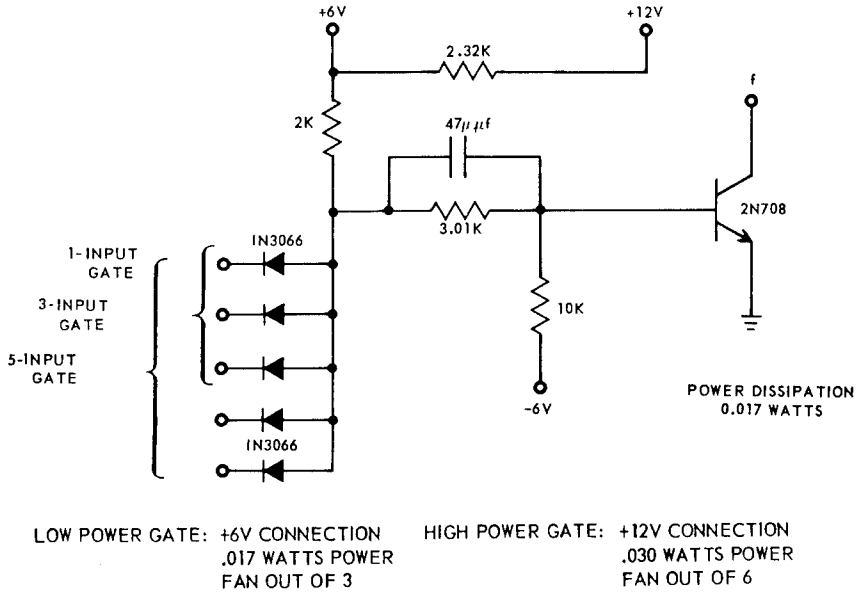


Fig. 4. Combined high- and low-power stroke gate.

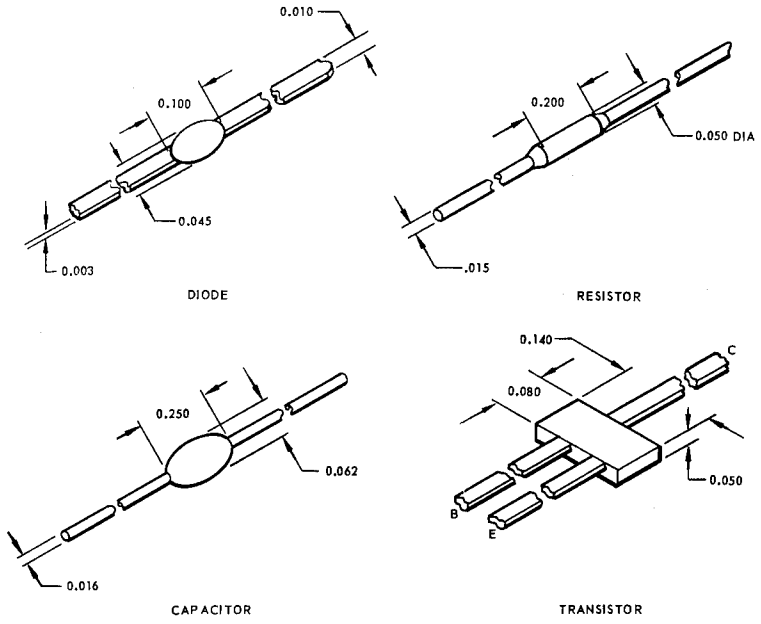
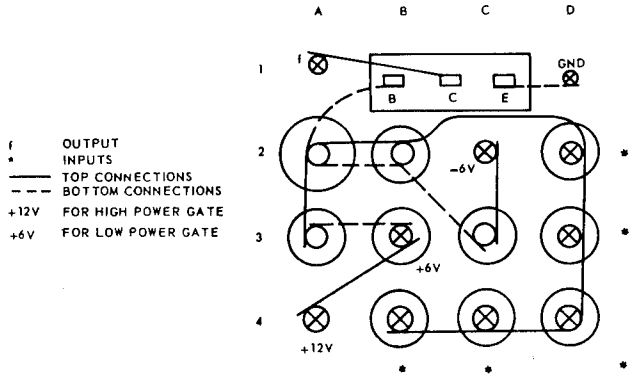
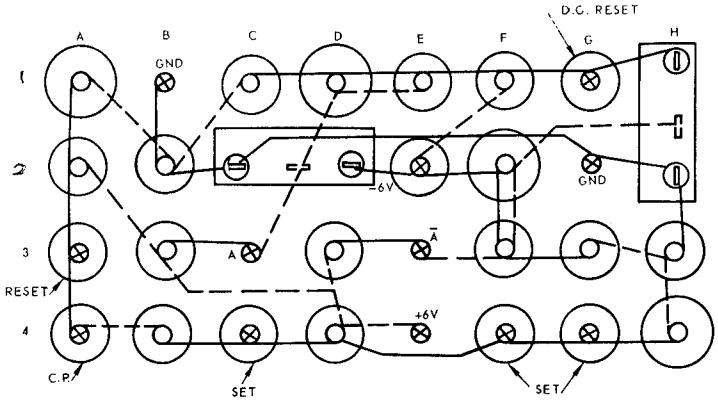


Fig. 5. Component description.



GRID COORDINATE	1 INPUT GATE	3 INPUT GATE	5 INPUT GATE
A1	FEED THRU	FEED THRU	FEED THRU
A2	47μμf	47μμf	47μμf
A3	2K	2K	2 K
A4	FEED THRU	FEED THRU	FEED THRU
B1	(2N708) (PMT 121)	(2N708) (PMT 121)	(2N708) (PMT 121)
B2	3.01 K	3.01 K	3.01 K
B3	2.3 K	2.3 K	2.3 K
B4	–	1N3066 (PD 311)	1N3066 (PD 311)
C1	(2N708) (PMT 121)	(2N708) (PMT 121)	(2N708) (PMT 121)
C2	FEED THRU	FEED THRU	FEED THRU
C3	10 K	10 K	10 K
C4	–	–	1N3066 (PD 311)
D1	FEED THRU	FEED THRU	FEED THRU
D2	–	1N3066 (PD 311)	1N3066 (PD 311)
D3	–	–	1N3066 (PD 311)
D4	1N3066 (PD 311)	1N3006 (PD 311)	1N3066 (PD 311)

Fig. 6. Connection diagram for high and low power: 1-input gate, 3-input gate, and 5-input gate.



GRID COORDINATE	COMPONENT	GRID COORDINATE	COMPONENT
A1	100 μμf	E1	3.32K
A2	1K	E2	27.4K
A3	1N3066 (PD 311)	E3	FEED THRU
A4	1N3066 (PD 311)	E4	FEED THRU
B1	FEED THRU	F1	27.4K
B2	1K	F2	27 μμf
B3	475 Ω	F3	3.32K
B4	1N3066 (PD 311)	F4	1N3066 (PD 311)
C1	1N3066 (PD 311)	G1	1N3066 (PD 311)
C2	(2N708) (PMT 121)	G2	FEED THRU
C3	FEED THRU	G3	1N3066 (PD 311)
C4	1N3066 (PD 311)	G4	1N3066 (PD 311)
D1	27 μμf	H1	(2N708) (PMT 121)
D2	(2N708) (PMT 121)	H2	(2N708) (PMT 121)
D3	475 Ω	H3	1K
D4	1K	H4	100 μμf

Fig. 7. Connection diagram for R-S flip-flop.

1 × 1 in. module. Emphasis should be placed on keeping the module simple and economical to design and produce. However, identical module designs will be created as a matter of course.

Function Components Costs

Component cost comparison for logic function modules and the 1 × 1 in. modules are shown in Table III.

MODULE DESIGN

*Module intraconnections** were evaluated in four randomly selected areas of the arithmetic and control units (see Fig. 10). With ground rules established for submodule arrangements, connection schemes were arrived at in several minutes. It is evident from Fig. 10 that the module intraconnections are relatively simple and producible.

The *module interconnection* density was noted to have decreased to 20 connections/in.^{2} from the 65 connections/in.^{2} observed in connecting function submodules. Forty-five connections/in.^{2} on the average have been absorbed in the module intraconnections.

* From this point on in the paper, a module will be understood to be the 1 × 1 in. unit; *intra*connections will be connections internal to the subject unit, and *inter*connections will be connections between units.

The *mechanical design* of the module utilizes an attachment screw. The center $\frac{1}{3}$ in. $\times$ $\frac{1}{3}$ in. area of the module has been left unused for a mounting spacer. The approximate weight of a module is 0.035 lb. The maximum combined acceleration–shock–vibration load taken from existing missile systems is 225 g's. Calculations for the module attachment are contained in Appendix 1 and indicate more than adequate strength.

The *thermal analysis* of the module requires a brief description of the mounting arrangement. Sixteen modules, in a square array, are mounted on an aluminum structure (see Figs. 11, 12, and 13). The structure provides the mechanical support for the modules and the module interconnections. It also provides a thermal path directly from the module surface to the package structure.

To analyze the thermal aspects of the module, the following approach was taken:

a. The largest heat-generating module was selected from the logic diagram.
b. Three conduction heat paths were evaluated in the module.
c. An equivalent heat path was approximated to obtain the difference in temperature between the hot spot in the module and the module mounting channel.
d. A module was fabricated and tested to verify the difference in temperature calculated in part c.

An appraisal of the distribution of submodules in modules, taken from the logic diagram, shows that 0.390 W for a two-flip-flop and four-gate combination is the worst thermal condition. For comparison, the average heat dissipation per module is 0.218 W. Figure 14 shows the two-flip-flop, four-gate arrangement indicating the locations of the heat-generating resistors.

The three thermal conduction paths in the module are shown in Fig. 14. For path 1,

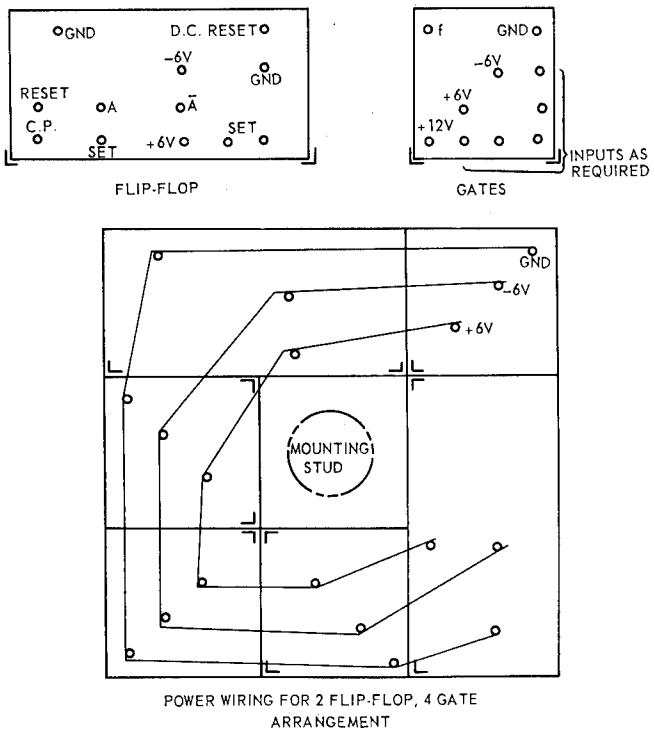


Fig. 8. Function lead orientation and power wiring.

TABLE II

Simplified Arithmetic and Control Unit Function Breakdown and Trade-offs

Function	Quantity	After 1st trade-off	After 2nd trade-off	After 3rd trade-off	After 4th trade-off
One-input high-low gate	286	286	286	286	286
Two-input high-low gate	198	198	198		
Three-input high-low gate	78	78		276	
Four-input high-low gate	38				
Five-input high-low gate	31	69	147	69	345
One set, two reset flip-flop	44	44			
Two set, two reset flip-flop	17				
Three set, two reset flip-flop	5	22	66	66	66
8-function types		6-function types	4-function types	4-function types	3-function types
Penalty					
Additional resistors 631*		$612*	$612*	$612*	$612*
Number of diodes		55	297	341	893
% of total components		0.8%	4.5%	5.2%	13.5%
Cost of diodes		$176.00	$950.00	$1091.00	$2858.00
% of component cost		1.0%	5.3%	6%	16%
Resistor and diode cost %		4.4%	8.8%	9.6%	19.4%

* 631 extra resistors for high–low gate costing $612.

the resistor locations were approximated to be at a radius b from the center of the module. This approximation allows calculations to be made for heat flow from the walls to the center of a cylinder. For path 2, the effective cross-sectional area for the heat flow toward the channel was approximated to be three times the resistor body diameter. For path 3, 20 wires were assumed present to carry away heat. Wire diameter, material, and path length are given in

TABLE III

Component Costs for Arithmetic and Control Units

	One DFC	Two DFC's	Five DFC's	Fifty DFC's
1-input gate	$14.44	$12.28	$11.97	$ 8.93
3-input gate	$21.04	$18.28	$17.57	$12.53
5-input gate	$27.44	$24.28	$23.17	$16.13
Flip-flop	$62.08	$55.70	$48.12	$33.72
8-gate module	$160.00	$144.00	$132.00	$ 96.00
1ff, 6-gate module	$181.00	$159.00	$148.00	$106.00
2ff, 4-gate module	$204.00	$175.00	$163.00	$115.00
3ff, 2-gate module	$226.00	$191.00	$178.00	$125.00
4ff module	$248.00	$206.00	$193.00	$135.00

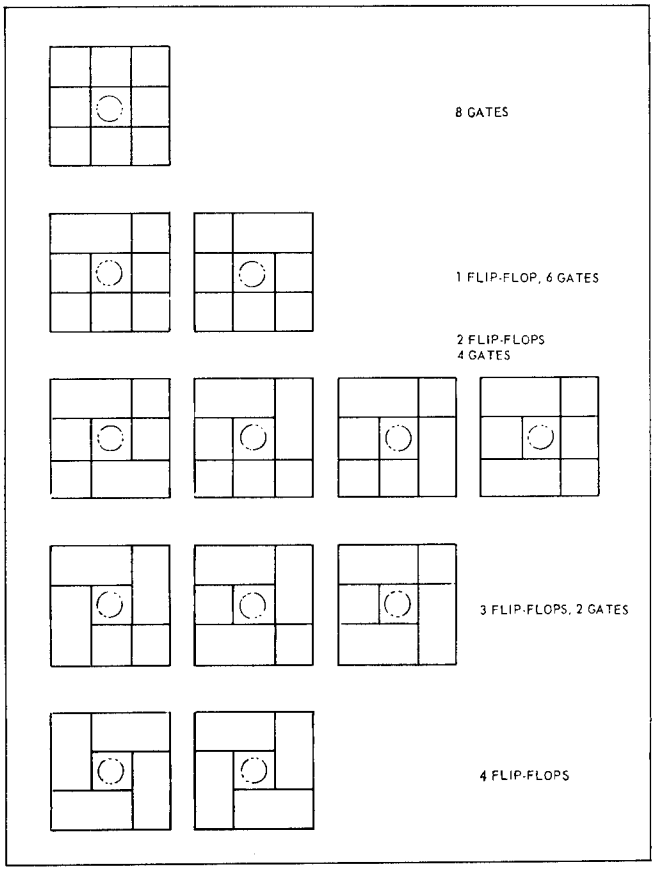


Fig. 9. Function submodule combinations.

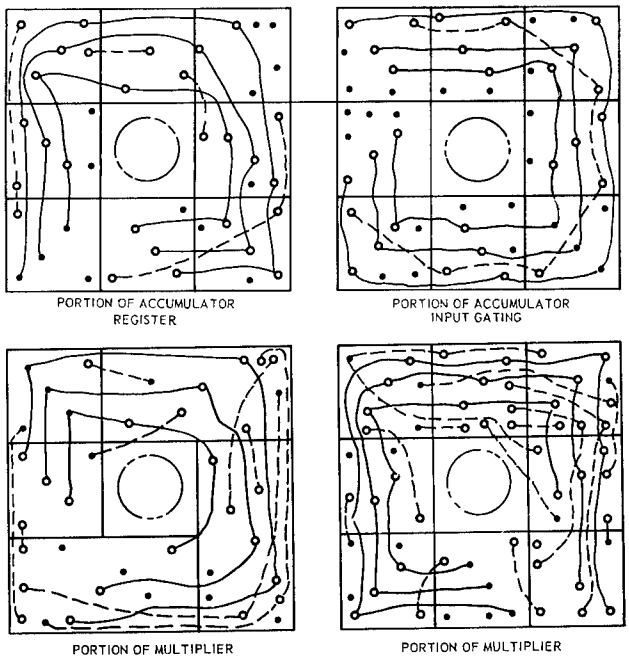


Fig. 10. Module intraconnection samples.

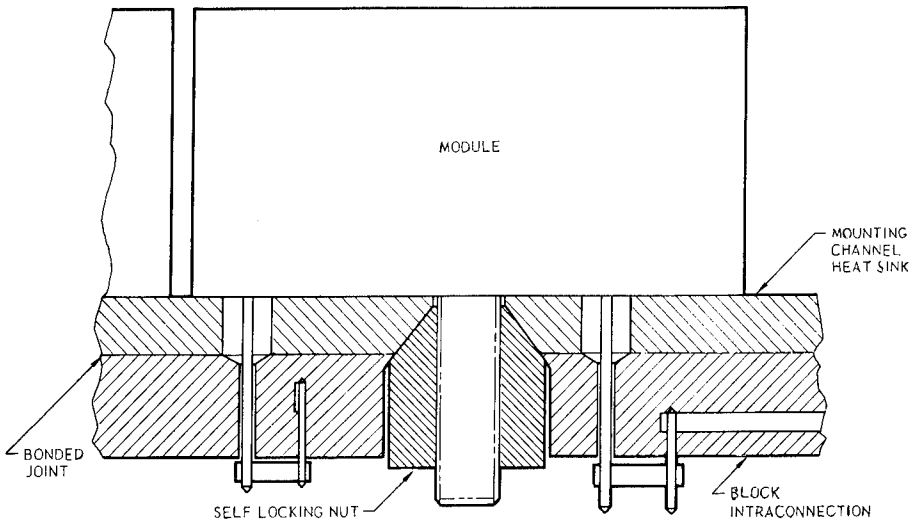


Fig. 11. Module mounting and interconnection.

Appendix 2. The calculated temperature difference between the module hot spot and the C channel for parallel heat paths is 35.8°F, or 19.9°C (see Appendix 2).

Figure 15 shows the test unit fabricated for temperature-difference measurement. Twelve resistors were connected and embedded to simulate thermally the module shown in Fig. 14. Thermistors were used to monitor temperatures. The test unit was placed in a cardboard box filled with insulation. This was done to minimize thermal conduction and convection. The near steady-state temperature difference observed was 11°F or 6.1°C. Figure 16 shows the time–temperature history of the module dissipating 0.390 W.

BLOCK DESIGN

The term "block" is assigned to the unit containing 16 modules. The block represents approximately one-ninth of the computer and contains an average of 1100 components.

Simplification for *block intraconnections* appears extremely difficult except to provide alternative module orientations which will allow the designer to select the cleanest arrangement. It was anticipated that four interconnection layers would be the maximum required for the block intraconnection. The power connections could occupy two of these four layers. Figure 17 illustrates the power wiring grid configuration which allows each module to orient itself in any one of four ways. This complicated-looking grid is only required as an underlay guide in planning power wire routing. The following method is proposed in laying out the block intraconnection:

a. Orient modules for signal connection simplicity.
b. Overlay module orientation on the power wiring grid.
c. Select the power connections using the grid as a guide.

Figure 18 shows part of a completed block power intraconnection.

The *block interconnections* are made by rectangular wire wrap terminals. Figure 19 shows how these terminals are connected to the block intraconnections and the package matrix. It

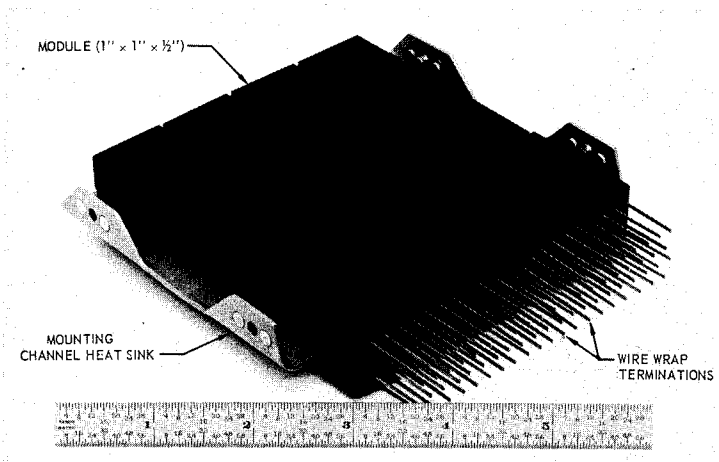


Fig. 12 TOP VIEW OF BLOCK

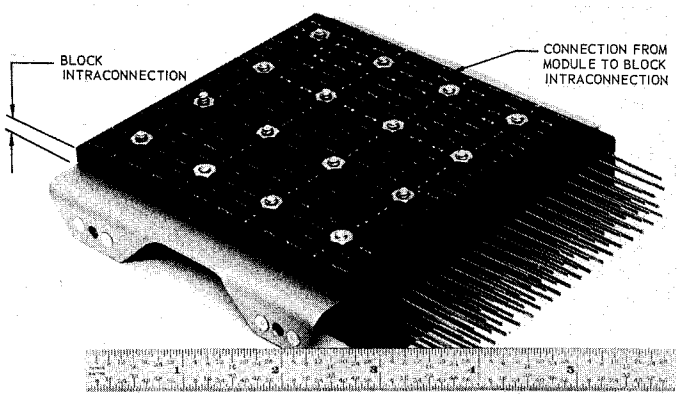


Fig. 13 BOTTOM VIEW OF BLOCK

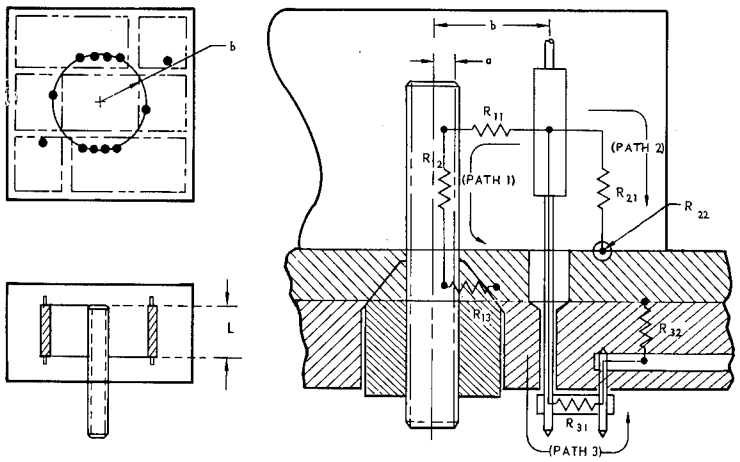


Fig. 14. Module thermal paths.

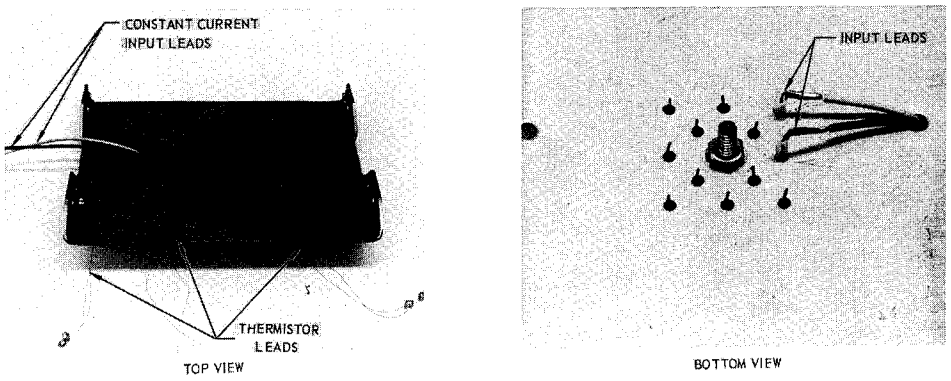


Fig. 15

should be noted that the wire wrap header, block intraconnection, and support channel are all permanently bonded together. Figure 20 shows the front view of the package matrix and the wire wrap connections between the blocks and the package matrix.

The *mechanical strength* of the block has been analyzed by the following approach:

a. Approximating the allowable static deflection to keep the natural vibration resonant frequency above 100 cps.
b. Determining the module, channel, and interconnection weight load for 25 *g*'s vibration.
c. Determining the section properties of the block structure with derating assumptions for the holes.
d. Calculating the static deflection under vibration loads for various channel configurations.
e. Analyzing areas of critical stresses.

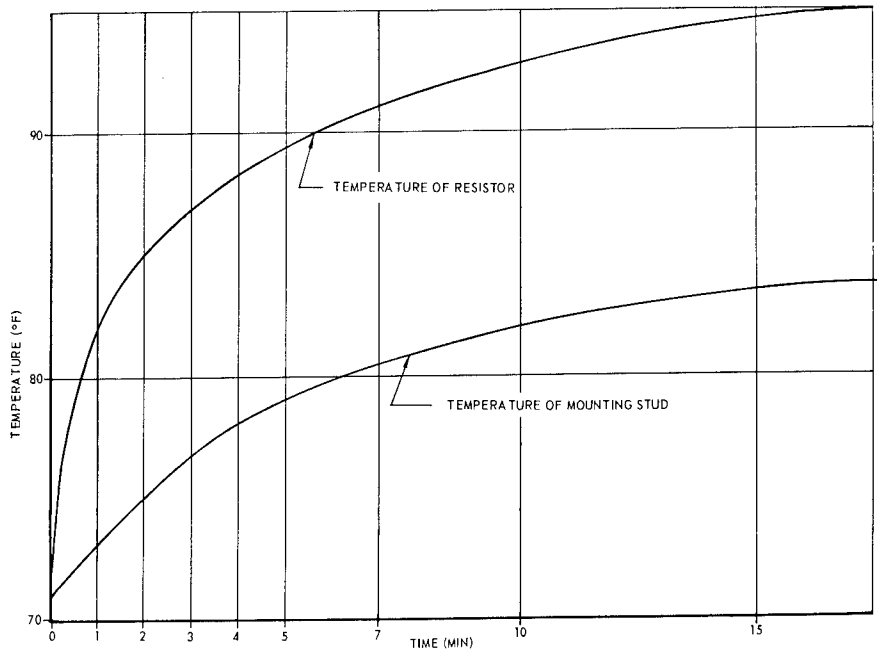


Fig. 16. Time–temperature curve for 0.390-watt module.

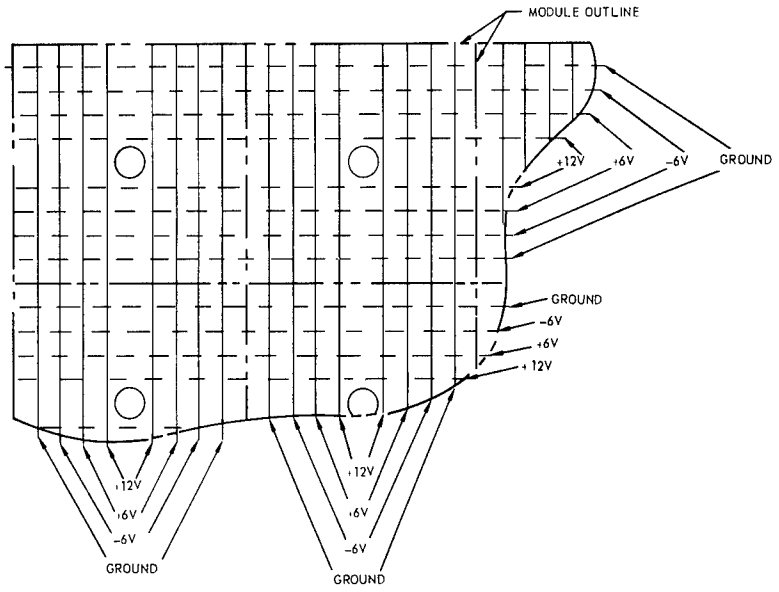


Fig. 17. Power wiring grid underlay.

Calculations for the block mechanical analysis are contained in Appendix 1. The results of the calculations show that a plain channel must be approximately $\frac{1}{4}$ in. thick to keep the natural resonant frequency above 100 cps. This was unsatisfactory for weight and volume considerations. A compartmented channel, shown in Appendix 1, was selected as a better

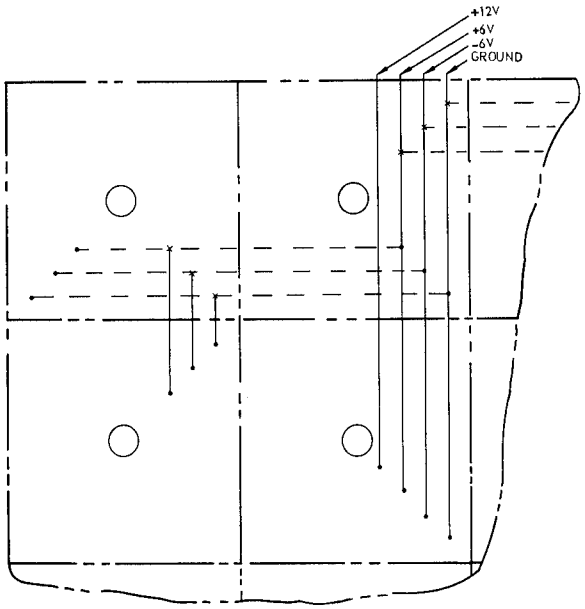


Fig. 18. Block power intraconnection.

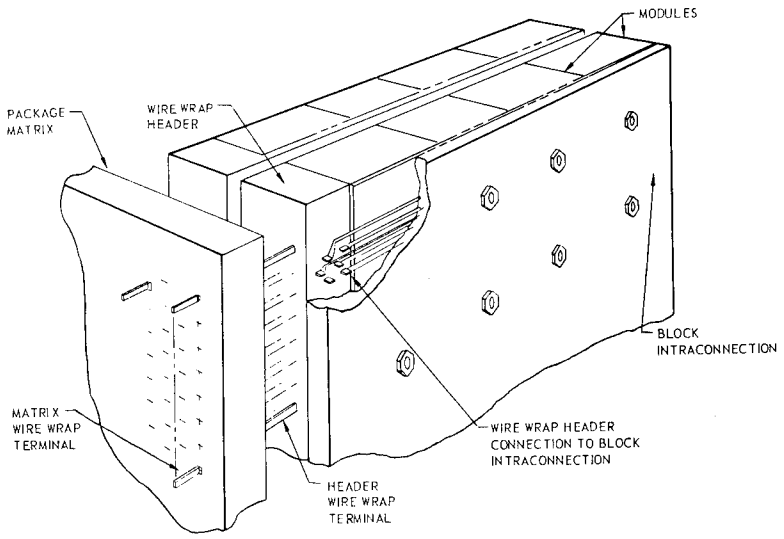


Fig. 19. Block interconnection.

design. Although it is not as simple as the plain channel, the 0.040-in. version is 20 times more rigid and $\frac{1}{2}$ lb lighter than the $\frac{1}{4}$-in.-thick channel. A compression rod was included perpendicular to and passing through the center of the block for additional rigidity.

The *thermal analysis* of the block indicates that a temperature difference of approximately 6.4°C will exist between the hottest portion of the channel and the top and bottom sides of the package. This temperature difference was obtained based on certain assumptions and makes the result valuable only as an approximation.

MEMORY AND MEMORY CIRCUITRY

The memory and the memory circuitry are packaged together as a single section of the computer. This is done because the lead lengths between the memory and its circuitry must be kept short. Also, the number of interconnections (60) to the memory and memory circuitry section is relatively small. The size of this section is 5.4 × 5.3 × 3 in. and its power dissipation is approximately 19 W. Wire wrap connections are brought directly from the memory and power supply to the package matrix.

PACKAGE MATRIX

The package matrix contains:

a. Electrical connectors (42-4574S, Winchester Electronics).
b. Interconnection layers that route conductors from block to block, power supply to blocks, memory to blocks, and input–output connectors to blocks, memory, and power supply.
c. Wire wrap terminals from the interconnection layers.
d. Holes adjacent to the matrix terminals for the wire wrap terminals from the memory, power supply, and blocks.

Evaluation of the *matrix terminations* for the nine blocks shows a total requirement of 135 connections to the input–output connectors and 800 connections internal to the package. This indicates a need for 935 terminations on the face of the matrix.

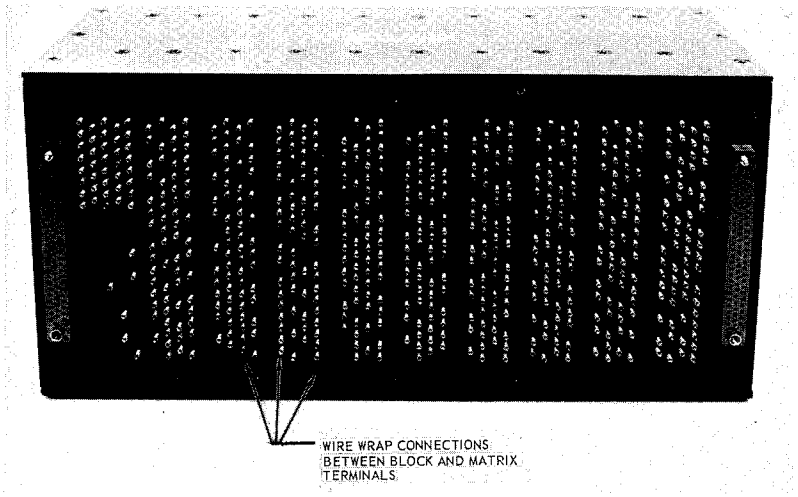


Fig. 20. Block interconnection to matrix.

The wire wrap terminals selected for this design have a cross section of 0.020 × 0.045 in. When two of these terminals, (one from the matrix and one from the block), are placed together, they form a rectangle 0.040 × 0.045 in. Twenty-six gage wire is wrapped around both terminals with a Keller bit No. A-24255.

The terminal center-to-center minimum spacing for the wire wrap bit and sleeve is $\frac{1}{8}$ in. An offset 0.150-in. spacing was used for the layout of the terminations. This gives a potential of 120 connections for a rectangular block header 0.750 × 5.0 in. Evaluation of the blocks

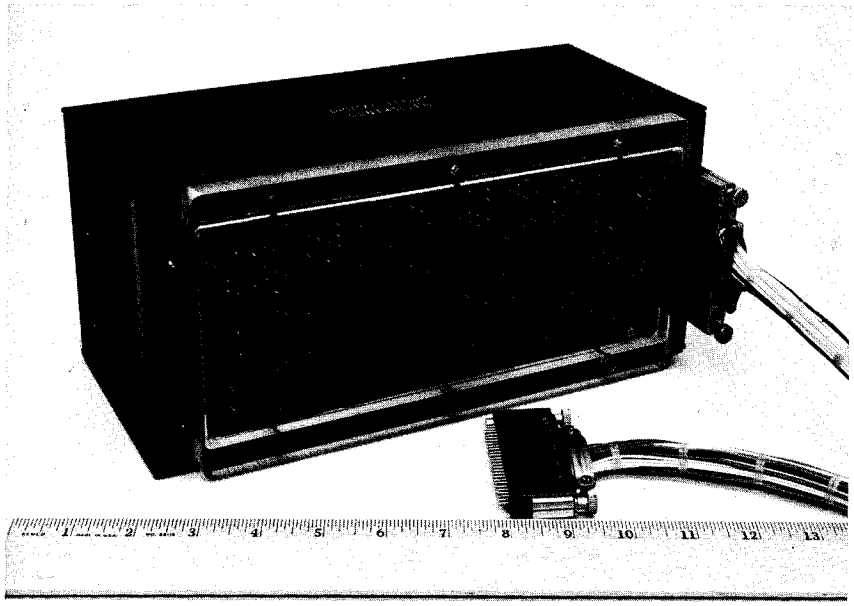


Fig. 21. Digital flight controller model.

shows that an average of 96 connections per block are required. There is thus a 20% growth possible in termination requirements.

The *interconnection layers* are fabricated by either etched circuit boards or welded planes. Matrix layers in both forms have successfully been made for a Douglas Programmer using the Rebound circuitry. The interconnection layers for the DFC matrix would not require the close spacing and narrow conductors of the Programmer design. The completed matrix is a solid structure 5.6 in. wide, 11.5 in. long, and 0.5 in. thick. It weighs approximately 2.2 lb (see Fig. 20).

PACKAGE ENCLOSURE

The package enclosure consists of six separate parts. The two end pieces are milled sections $\frac{5}{8}$ in. thick. These provide end attachments for the package matrix plus the top, bottom, and back panels. The matrix cover protects the wire wrap terminations and is bolted to the matrix. Installation attachments are provided on the bottom of the end pieces. Figure 21 shows an assembled model of the DFC. The outside dimensions of the package are 11.5 × 6.5 × 5.6 in.

The *package mechanical analysis* is contained in Appendix I. Calculations were made for the package section properties and deflections under load. The results show that the boxlike construction is very rigid. The approximate natural resonant frequency for the 13.2-lb package is 180 cps. The frequency is for a vibration acceleration of 25 *g*'s.

The *thermal analysis* for the package shows the total heat generated is 57 W or 194.6 Btu/hr. Evaluation of the temperature differences expected in the package structure shows they must be considered (see Appendix II).

MAINTENANCE PHILOSOPHY

It has been attempted in this design to provide a simple replacement level for maintenance. This level is the wire wrap connected block. It is proposed that spare blocks be stocked at repair depots and field stations. In case of malfunction, a block may be simply and quickly replaced by unwrapping and rewrapping the block terminations. The malfunctioning block is returned to the manufacturer for repair.

To repair a block, the inoperative module would first be isolated and removed. An identical module would be fabricated from pretested submodules and assembled in the block. The completed block may now be tested before shipment to the depot or field station.

CONCLUSIONS

The design analysis of the Douglas Digital Flight Control Computer shows that this device can be adequately packaged to meet missile and spaceborne applications. Mounting the modules on an aluminum channel in the manner described provides a strong mechanical structure, a thermal conduction path, and a method for removing modules.

The analysis also shows that much of the detailed design and fabrication of the unit may be simplified by careful selection of basic standards. Examples of these standards are the four configurations of logic functions and the two physical configurations of the submodules.

ACKNOWLEDGMENTS

The author wishes to acknowledge the contributions of M. N. Winters, H. R. Fields, R. R. Erkeneff, T. J. Nelson, R. G. Saez, and R. C. Frank. Valuable assistance was also rendered by I. A. Robins and R. E. Kalfayan.

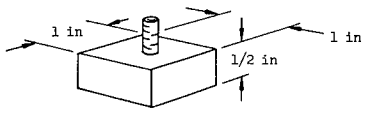
REFERENCES

1. "Development of Digital Flight Controller," Douglas Report SM-38775, June 1961.
2. "Development of Digital Flight Controller," Douglas Report SM-41907, May 1962.

APPENDIX I: MECHANICAL ANALYSIS

Module

(Module leads omitted for clarity)



Stud Strength

Module Weight	0.035 lb
Acceleration	225 g's
Root Diameter Area	0.0075 in.^{2} (Nos. 6–32 stud)
Maximum Load	(0.035 lb) (225 g's) = 79 lb
Tensile and Shear Stress	79 lb/0.0075 in.^{2} = 10,500 psi

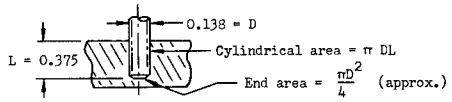
NAS 1454-06 Stud Rated 90,000 psi yield

Stud to Module Bond Strength

Epoxy Mechanical Properties

Adhesion	4000 psi	
Shear	6000 psi	(Average values taken from
Tensile	8800 psi	manufacturers' data sheets)

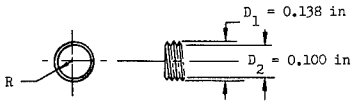
Axial Load Strength



$$\pi DL = (3.14)(0.138)(0.375) = 0.118 \text{ in.}^2 \text{ in shear}$$
$$\pi D^2/4 = (3.14)(0.138)^2/4 = 0.015 \text{ in.}^2 \text{ in adhesion}$$

Axial Load Strength = (0.118 in.^{2})(6000 lb)/in.^{2} + (0.015 in.^{2})(4000 lb)/in.^{2}
Axial Load Strength = 770 lb
Maximum Load = 79 lb

Torque Strength



$$\text{Number of Threads} = (0.375 \text{ in.})\frac{(32 \text{ threads})}{\text{in.}} = 12 \text{ threads}$$

$$\frac{\text{Thread Area}}{\text{Thread}} = 2\left[\frac{\pi D_1^2}{4} - \frac{\pi D_2^2}{4}\right] \quad \text{(approx.)}$$

$$= \frac{\pi}{2}\left[D_1^2 - D_2^2\right] = \frac{\pi}{2}[(0.138)^2 - (0.100)^2]$$

$$= 0.0142 \text{ in.}^2$$

Total Thread Area = (12)(0.0142) = 0.17 in.^{2}

$$\text{Adhesion Strength to Thread} = \frac{(0.17 \text{ in.}^2)(4000 \text{ lb})}{\text{in.}^2} = 680 \text{ lb}$$

Mean Radius R = 0.07 in.
Torque Strength = (680 lb)(0.07 in.) = 47 in.-lb

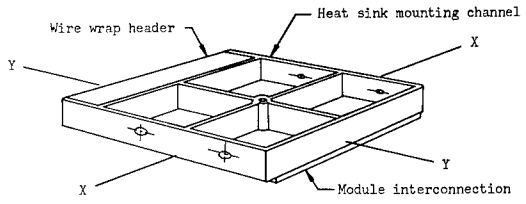
Block

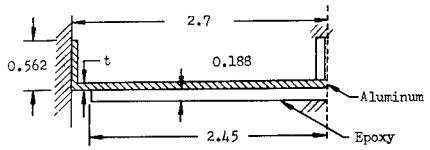
The natural vibration resonant frequency has been arbitrarily set at 100 cps minimum. An approximation for the relationship between static deflection and resonant frequency is:

$$\sqrt{\delta_t} = \frac{3.55}{f_r} = \frac{3.55}{100}$$

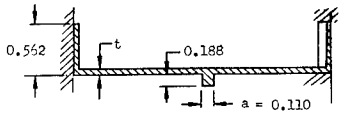
$$\delta_t = (0.0355)^2 = 0.00126 \text{ in.}$$

Section Properties and Static Deflection





One-Half of X–X Section



One-half of X–X section with epoxy transformed to aluminum

$E_{al} = 10^7$ psi

$E_{epoxy} = 4.5 \times 10^5$ psi

$$a = \frac{2.45(E_e)}{(E_{al})}$$

$$a = \frac{2.45(4.5 \times 10^5)}{10^7}$$

$$a = 0.110 \text{ in.}$$

Module Weight	4×0.035 lb $= 0.14$ lb
Interconnection Weight	0.04 lb
Channel Weight	7.3 in.$^2 \times t \times 0.1$ lb/in.^{3}

$$\delta \cong \frac{5WL^4}{384EI} \quad \text{(approximate)}$$

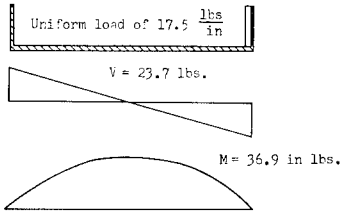
t	Total weight, lb	Load at 25 g's, lb	Moment of inertia (I_{an}) in.^{4}	δ, in.
0.060	0.224	5.60	0.002438	6.30×10^{-5}
0.040	0.210	5.2	0.00175	7.67×10^{-5}

Calculations for the section properties and the deflections in the y-y direction are omitted. Loads are identical and the y-y section is estimated to be more rigid than the x-x section.

Stress Evaluation

Total weight in one-quarter block section = 0.21 lb

Load at 225 g's P = 225 × 0.21 lb = 47.3 lb



$$\tau = \frac{V}{\text{Area}} \qquad \sigma_B = \frac{MC}{I}$$

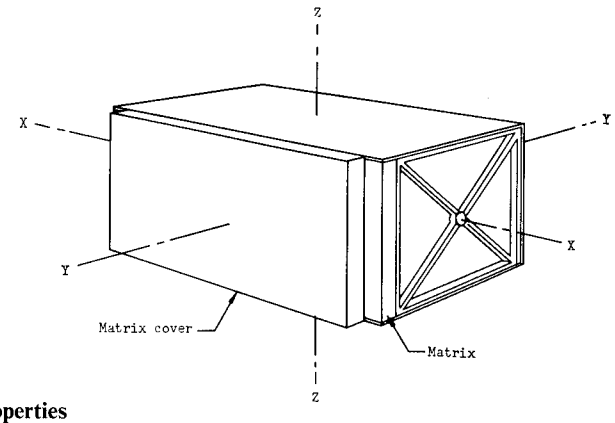
$$\tau = \frac{(23.7)}{(0.040)(2.62)} = 260.5 \text{ psi} \qquad \sigma_B = \frac{(36.9)(0.028)}{(0.00175)} = 590 \text{ psi}$$

Attachment

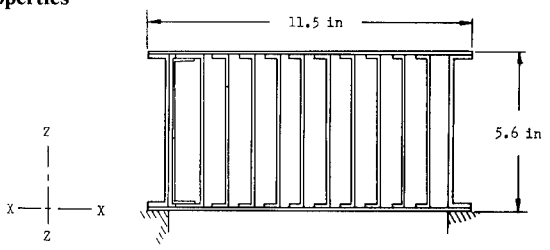
Load per Screw = 47.3 lb

$$\text{Bolt Shear} = \frac{47.3 \text{ lb}}{0.0075 \text{ in.}^2} = 6306 \text{ psi}$$

Package



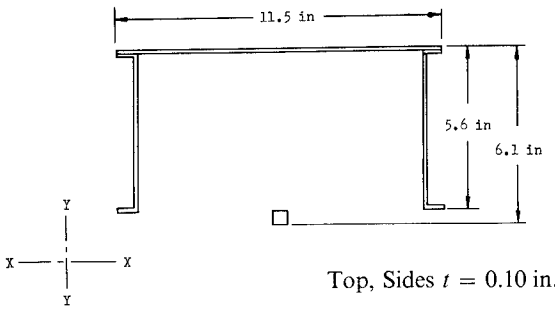
Section Properties



Section A

Top, Bottom, Sides $t = 0.10$ in. Webs $t = 0.040$ in.

$I_{na} = 20.7 \text{ in.}^4$

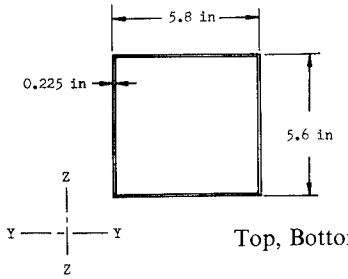


Top, Sides $t = 0.10$ in.

Section B

Epoxy matrix transformed to aluminum

$I_{na} = 14.6$ in.^{4}



Top, Bottom, Side $t = 0.10$ in.

Section C

Epoxy matrix transformed to aluminum

$I_{na} = 13.8$ in.^{4}

Package Weight

9 Blocks at 0.84 lb	7.56 lb
Memory and Power Supply	1.19 lb
Matrix	2.20 lb
Package Structure	2.29 lb
Total Weight	13.24 lb

Static Deflection for Resonance Approximation

$$\delta = \frac{5WL^4}{384EI} \quad \text{(approximate)}$$

$W = 13.24 \times 25\ g$'s $= 331$ lb along z–z axis (worst case)

$\delta = 3.6 \times 10^{-4}$ in.

$$f_r = \frac{3.55}{\sqrt{\delta_T}} = \frac{3.55}{\sqrt{3.6 \times 10^{-4}}} = 180 \text{ cps} \quad \text{(approximate)}$$

APPENDIX II: THERMAL ANALYSIS

Module to Channel

Equations and Symbols. The following steady-state heat transfer equations are used in the analysis:

Linear Flow of Heat

$$q = kA(\Delta T/\Delta X)$$
$$q = kA(\Delta T/l)$$

Radial Flow of Heat

$$q = k2\pi RL(\Delta T/\Delta r)$$
$$q = \frac{k2\pi L\Delta T}{\ln(r_2/r_1)}$$

Heat Flow Across Contact Interface

$$q = h_c A\Delta T$$

Two additional equations are used:

Composite Heat Transfer Equation

$$q = \Delta T/R_{eq}$$

Parallel Combination of Thermal Resistance

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \cdots$$

List of Symbols

q = Heat flow rate (Btu/hr)
k = Thermal conductivity of material (Btu-in./hr-ft^2-°F)
A = Area (ft^2)
ΔT = Temperature difference (°F)
l = Length of conduction path (in.)
L = Length of cylinder in radial heat flow (in.)
r_1, r_2 = Radii of cylinder in radial heat flow (in.)
h_c = Interface conductance coefficient (Btu/hr-ft^2-°F)
R_{eq} = Equivalent thermal resistance (ft^2-hr-°F/Btu-in.^{2})
R_1 = Thermal resistance for path 1
R_{11} = Thermal resistance for part 1 of path 1
R_{12} = Thermal resistance for part 2 of path 1

Calculations (See Fig. 15)

For Path 1

$$q = \frac{k_e 2\pi L\Delta T_{11}}{\ln(b/a)}$$

$$R_{11} = \frac{\ln(b/a)}{k_e 2\pi L}$$

where k_e = 1.74 Btu-in./ft^2-hr-°F, L = 0.200 in., a = 0.060 in., and b = 0.280 in.:*

$$R_{11} = \frac{1.54}{(1.74)(2\pi)(0.200)} = 0.057 \frac{\text{ft}^2\text{-hr-°F}}{\text{in.}^2\text{-Btu}}$$

* DACo Lab Report No. MP30,001, dated September 29, 1961, "Thermal Conductivity of Filled Epoxy Resins."

$$q_{12} = \frac{k_{al}A_s\Delta T_{12}}{l_{12}}$$

$$R_{12} = \frac{l_{12}}{k_{al}A_s}$$

where $k_{al} = 1422$ Btu-in./ft^2-hr-°F, $l_{12} = 0.300$ in., and $A_s = 0.0075$ in.^{2} (stud area):

$$R_{12} = \frac{0.300}{(1422)(0.0075)} = 0.028\frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$Q_{13} = h_cA_{cs}\Delta T_{13}$$

$$R_{13} = \frac{1}{h_cA_{cs}}$$

where $h_c = 60$ Btu/hr-ft^2-°F and $A_{cs} = 0.076$ in.^{2} (counter sink area):*

$$R_{13} = \frac{1}{(60)(0.076)} = 0.219\frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$R_1 = R_{11} + R_{12} + R_{13} = 0.507 + 0.028 + 0.219 = 0.754\frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

For Path 2

$$q_{21} = \frac{k_eA_{3R}\Delta T_{21}}{l_{21}}$$

$$R_{21} = \frac{l_{21}}{k_eA_{3R}}$$

where $l_{21} = 0.250$ in., $k_e = 1.74$ Btu-in./ft^2-hr-°F, and $A_{3R} = 0.27$ in.^{2}†

$$R_{21} = \frac{0.250}{(1.74)(0.27)} = 0.532\frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$q_{22} = h_cA_{3R}\Delta T_{22}$$

$$R_{22} = \frac{1}{h_cA_{3R}}$$

where $h_c = 60$ Btu/hr-ft^2-°F and $A_{3R} = 0.27$ in.^{2}

$$R_{22} = \frac{1}{(60)(0.27)} = 0.062\frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$R_2 = R_{21} + R_{22} = 0.532 + 0.062 = \frac{0.594\ \text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

For Path 3

$$q_{31} = \frac{k_cA_w\Delta T_{31}}{l_{31}}$$

* Contact pressure 35 psi at 10^{-4} mm Hg vacuum. (R. L. Vaughan, Thermodynamics Section).
† Approximation of three times resistor body diameter times the number of resistors.

$$R_{31} = \frac{l_{31}}{k_c A_w}$$

where $l_{31} = 0.900$ in.,* $k_c = 2670$ Btu-in./ft^2-hr-°F (copper), and $A_w = 0.003$ in.^{2}:†

$$R_{31} = \frac{0.900}{(2760)(0.003)} = 0.112 \frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$q_{32} = \frac{k_e A_{NR} \Delta T_{32}}{l_{32}}$$

$$R_{32} = \frac{l_{32}}{k_e A_{NR}}$$

where $l_{32} = 0.05$ in.,‡ $k_e = 1.74$ Btu-in./ft^2-hr-°F, and $A_{NR} = 0.090$ in.^{2}:§

$$R_{32} = \frac{0.05}{(1.74)(0.090)} = 0.319 \frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$R_3 = R_{31} + R_{32} = 0.112 + 0.319 = 0.431 \frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

Equivalent Path Temperature Difference

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

$$R_{eq} = \frac{R_1 R_2 R_3}{R_2 R_3 + R_1 R_3 + R_1 R_2} = \frac{(0.193)}{0.256 + 0.325 + 0.448} = \frac{0.187 \text{ ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$q_{total} = \frac{\Delta T_{total}}{R_{eq}}$$

$$= 0.390 \text{ W (maximum)} = 1.331 \text{ Btu/hr}$$

$$\Delta T_{total} = (q_{total})(R_{eq})$$

$$= \frac{(1.331 \text{ Btu})}{\text{hr}} \frac{(0.187 \text{ ft}^2\text{-hr-°F})}{\text{Btu-in.}^2} \frac{144 \text{ in.}^2}{\text{ft}^2}$$

$$= 35.8°\text{F} = 19.9°\text{C}$$

Channel to Package Structure

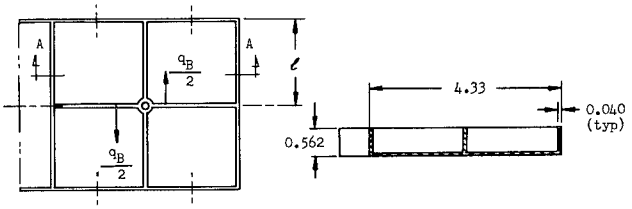
Average heat generated per block = (16)(0.218 W)

$$q_B = 3.49 \text{ W} = 11.9 \text{ Btu/hr}$$

Temperature Difference in Channel. Assumptions:

1. All of the heat is generated at the centerline of the block.
2. No heat flows through the compression rod.

* Average path length of wires from component body to embedded interconnections.
† Twenty wires of 0.015 in. diameter.
‡ Distance between nickel ribbon in interconnection and channel.
§ Approximation of twenty ribbon segments areas.



Section A-A

Area = 0.235 in.^{2}

$$\frac{q_B}{2} = \frac{k_{al} A \Delta T_1}{l}$$

$$\Delta T_1 = \frac{q_B l}{k_{al} A \cdot 2}$$

where k_{al} = 1422 Btu-in./ft^2-hr-°F and l = 2.7 in.

$$\Delta T_1 = \frac{11.9 \text{ Btu} \cdot 2.7 \text{ in.-hr-°F-ft}^2 \cdot 144 \text{ in.}^2}{2 \cdot \text{hr} \cdot 1422 \text{ Btu-in. } 0.235 \text{ in.}^2\text{-ft}^2} = 6.9°\text{F} = 3.8°\text{C}$$

Temperature Difference Across Interface

$$q_B/2 = h_c A \Delta T$$

$$\Delta T_2 = \frac{q_B}{2h_c A}$$

where $A = 0.562 \times 5.4 = 3.03$ in.^{2} and h_c = 60 Btu/hr-ft^2-°F

$$\Delta T_2 = \frac{11.9 \text{ Btu-hr-ft}^2\text{-°F } 144 \text{ in.}^2}{\text{hr} \cdot 2 \cdot 60 \text{ Btu} \cdot 3.03 \text{ in.}^2\text{-ft}^2}$$

$$\Delta T_2 = 4.7°\text{F} = 2.6°\text{C}$$

Total Temperature Difference

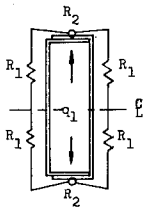
$$\Delta T_t = \Delta T_1 + \Delta T_2 = 3.8°\text{C} + 2.6°\text{C} = 6.4°\text{C}$$

Power Supply–Memory to Package Structure

Heat generated by memory	19 W
Heat generated by power supply	17 W
Total	36 W = 122.9 Btu/hr = q_1

Temperature Difference—Assumptions:

1. All heat generated on centerline.
2. Equal amounts of heat flow in two directions.



l = 2.7 in.

K_{al} = 1422 Btu-in./ft^2-hr-°F

$A = 5 \times 0.1 = 0.5$ in.^{2}

h_c = 60 Btu/hr-ft^2-°F

$$R_1 \frac{l}{KA} = \frac{2.7}{(1422)(0.5)} = \frac{0.004 \text{ ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$R_2 = \frac{1}{h_c A} = \frac{1}{(60)(5)} = \frac{0.003\ \text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

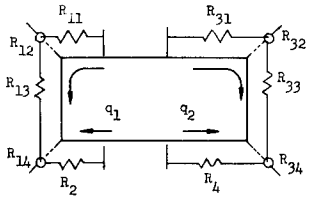
$$R_{eq} = \frac{R_1 R_1}{2R_1} + R_2 = \frac{(0.004)(0.004)}{0.008} + 0.003 = 0.005 \frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$\Delta T = \frac{q_1}{2} R_{eq} = \frac{(122.9\ \text{Btu})}{2\ \text{hr}} \frac{(0.005\ \text{ft}^2\text{-hr-°F})}{\text{Btu-in.}^2} \frac{144\ \text{in.}^2}{\text{ft}^2} = 44°\text{F} = 24°\text{C}$$

Package

Total heat generated by blocks	21 W
Total heat generated by power supply and memory	36 W
Total heat generated	57 W
Total heat generated	194.6 Btu/hr

Temperature Difference in Package:



$$q_1 = 36\ \text{W} = 122.9\ \text{Btu/hr}$$

$$q_2 = 21\ \text{W} = 71.7\ \text{Btu/hr}$$

Power Supply and Memory Area:

$$R = \frac{l}{K_{al} A} \text{ (for } R_{11}, R_{13}, \text{ and } R_2\text{)}$$

$$R = \frac{l}{h_c A} \text{ (for } R_{12} \text{ and } R_{14}\text{)}$$

where $K_{al} = 1422$ Btu-in./ft^2-hr-°F and $h_c = 60$ Btu/hr-ft^2-°F

	R	l (in.)	A (in.^{2})
$R_{11} = 0.0015$	11	1.3	6.1 × 0.1 = 0.61
$R_{12} = 0.0049$	12	—	6.1 × 0.562 = 0.342
$R_{13} = 0.0070$	13	5.6	5.6 × 0.1 = 0.56
$R_{14} = 0.0049$	14	—	6.1 × 0.562 = 0.342
$R_1 = 0.0183$	2	1.3	6.1 × 0.1 = 0.61
$R_2 = 0.0015$			

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = \frac{(0.0183)(0.0015)}{0.0198} = 0.0014 \frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$\Delta T = \frac{(122.9\ \text{Btu})}{\text{hr}} \frac{(0.0014)\ \text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2} \frac{144\ \text{in.}^2}{\text{ft}^2} = 24.8°\text{F} = 13.8°\text{C}$$

Block Area:

$$R = \frac{l}{K_{al}A} \text{ (for } R_{31}, R_{33}, \text{ and } R_4\text{)}$$

$$R = \frac{1}{h_c A} \text{ (for } R_{32} \text{ and } R_{34}\text{)}$$

	R	l (in.)	A (in.^{2})
$R_{31} = 0.0069$	31	6	$6.1 \times 0.1 = 0.61$
$R_{32} = 0.0049$	32	—	$6.1 \times 0.562 = 0.342$
$R_{33} = 0.0070$	33	5.6	$5.6 \times 0.1 = 0.56$
$R_{34} = 0.0049$	34	—	$6.1 \times 0.562 = 0.342$
$R_3 = 0.0237$	4	6	$6.1 \times 0.1 = 0.61$
$R_4 = 0.0069$			

$$R_{eq} = \frac{R_3 R_4}{R_3 + R_4} = \frac{(0.0237)(0.0069)}{(0.0306)} = \frac{\text{ft}^2\text{-hr-°F}}{\text{Btu-in.}^2}$$

$$\Delta T = \frac{(71.7 \text{ Btu})}{\text{hr}} \frac{(0.005 \text{ ft}^2\text{-hr-°F})}{\text{Btu-in.}^2} \frac{144 \text{ in.}^2}{\text{ft}^2} = 51.6\text{°F} = 28.7\text{°C}$$

8070

Design and Construction of a Polaris Timer to Space-Available Configuration

JOHN R. WOODS
University of Colorado, Boulder, Colorado

The adaptability of welded electronic circuitry to odd-shaped configurations is discussed, using as a format, a case history of a project completed under so called "crash conditions." The work used as a basis for this paper was performed at the Lockheed Electronics Company, Avionics, and Industrial Products facility in the City of Commerce, California, by the Special Products Department of the Telemetry and Data Systems Division.

INTRODUCTION

THE PRESENT state-of-the-art in electronic circuit packaging allows the imaginative designer great latitude in the selection of components and packaging methods. The various papers presented at this Symposium describe many of these techniques ranging from thin-film to conventional printed circuit construction.

The requirements of the project upon which this paper is based were such that the only logical choice was welded cordwood construction. The prime factor to be considered was component lead time. With only twelve weeks to design, build, and qualify four units, it became immediately apparent that breadboarded circuits would have to be assembled and tested almost in parallel with circuit design. Thus, standard "off-the-shelf" components, readily available, whose reliability numbers were known, were all that could be considered for inclusion in the system.

The inherent flexibility of cordwood packaging, its adaptability to various geometric patterns, coupled with the obvious density that would be required, eliminated the printed circuit approach to standard component use. The choice of welded circuitry also minimized the problem of achieving a package which would meet the weight and environmental requirements of the design specification.

PROJECT REQUIREMENTS

The design specification for the multievent timer under discussion contained several basic and unalterable limitations. The available space in the vehicle dictated the size and shape (Fig. 1). As indicated in the outline drawing, the position and type of connectors were also specified, and because of cable routing, these had to remain unchanged. The fixed position of these connectors further narrowed the latitude normally allowed the design engineer.

It became very apparent when the functional requirements were considered that a high order of density would have to be achieved to house the approximately 350 components which initial estimates indicated would be required.

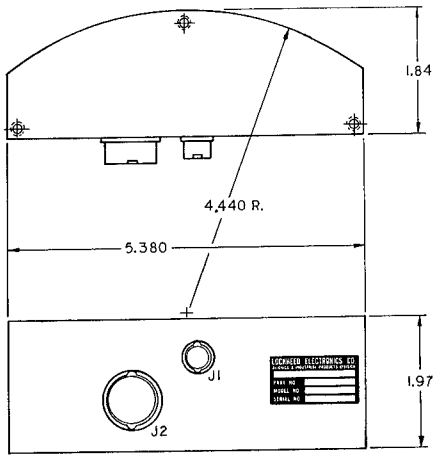


Fig. 1. Block diagram thin film high speed counter.

Immediate consideration had to be given also to the weight requirement. Limited to a maximum of 16 oz, investigations were begun at once into lightweight encapsulation systems capable of meeting the stringent environmental requirements (Tables I and II) required of all Polaris flight articles.

Since the project was essentially prototype in nature, the ability to repair or replace any component at any stage of the manufacturing cycle was a virtual necessity. The encapsulation systems finally chosen allowed for this eventuality.

DESIGN CONCEPT

The complex electrical design was finalized using 300 components, two of these required lab setting after final assembly. Subdivision of the total circuit resulted in eleven component modules. The breakdown was determined on the basis of repetitive circuitry and electrical function.

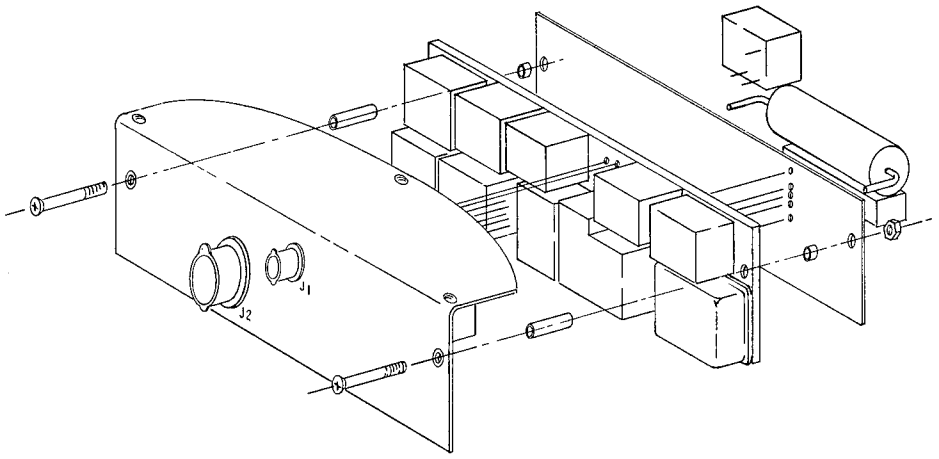


Fig. 2

TABLE I

Preoperation Environmental Conditions

	Condition	Duration
Temperature:	−65 to +160°F	30 days
	−40 to +135°F	5 years
Humidity:	95% relative maximum	12 hr
	50% relative maximum	5 years
	MIL-E-5272, Procedure I	120 hr
Pressure:	4 to 21.1 psia	5 years
	Ambient to 52.5 psia at 1.75 psi per second maximum rate of change, stabilized, and returned to ambient at a rate of 7 psi/sec maximum	75 min at 52.5 psia
Vibration, sinusoidal:	Conditions specified in Standard MIL-STD-167. 8 in. peak-to-peak, 1–2 cps	20 cycles

The twelve flip-flops required were combined into dual units; this resulted in improved density and reduced the number of interconnections in the base matrix. In order to achieve the required configuration, two interconnect matrices were used. The base, or No. 1 Matrix, interconnected nine of the eleven modules and served as a main supporting structure. The

TABLE II

Operating Environmental Conditions

	Condition		Duration
Temperature:	+135°F		4 hr
	+200°F		120 sec
Pressure:	Ambient to 52.5 psia with 1.25 psi/sec maximum rate of change, stabilized and returned to ambient at a maximum rate of 7.0 psi/sec		75 min at 52.5 psia
	Rapid decompression from 14.0 psia to an altitude pressure of 0.0033 psia within 85 msec		
Acceleration:	100 g normal to the true X axis		400 msec
	+10 g along the true X axis		1 min
	±4 g along the true Y and Z axes		1 min
Vibration, gaussian random:	Frequency (cps)	Envelope of peaks of g^2/cps	
	20	0.04	60 sec each axis
	2000	0.04	
Shock:	+18 g peak along each axis		40 msec
	±30 g peak along the true X axis		7 msec
	+100 g peak along the true X axis		2.5 msec

top, or No. 2 Matrix, was in fact a glass epoxy sheet. Placed adjacent to the base matrix with the remaining two modules attached, the resultant stack, high in the center, allowed the final unit to meet the shape requirement (Fig. 2).

Interconnection between matrices and connector terminals was accomplished by drilling holes in the matrices and the utilization of pass-through wires. The lone fabricated item was an L-shaped contoured plate, which formed the front panel and system base plate. The front panel was cut to accept the connectors and the base plate fitted with helicoil recepticals for the mounting screws.

MODULE DESIGN

The various component modules were designed along conventional cordwood lines. The height of each module was determined by T018 transistors placed back to back. In all possible cases glass capacitors were used. This choice was made on the basis of reliability and the adaptability of the rectangular case to dense packaging.

All layouts were made with the straightest possible runs with a minimum of pass-throughs and lap welds. Typical of the density achieved was the aforementioned dual flip-flop unit. The 34 components required of this portion of the circuit when encapsulated yielded a $\frac{3}{4}$-in. cube.

Simultaneously with the module design, weld schedules were developed as required, and existing schedules verified if they were to be used. At this point, perhaps a review of some weld do's and don'ts in module design would be in order.

1. Don't use runs with bends in excess of 90°.
2. Do allow sufficient clearance between conductors for the welding electrodes.
3. Don't allow unsupported parallel runs to be any closer than 0.075 in. and avoid them completely when possible.
4. Do insulate any pass-throughs adjacent to "hot" components.
5. Don't allow any bends at the weld; continue the run at least 0.050 in. before bending.
6. Do remember that your designs have to be assembled by someone, and if possible, discuss your design with your manufacturing people before you make it final.

THE MATRIX

The base matrix was designed as a two layer *x-y* type. This method simplifies the interconnect problem as crossovers can be made by simply changing levels. Vertical conductors are used to jump over the blocking wire and to conduct from level to level. The construction method employed uses the holding fixture as a potting mold and the layout pattern as between layer insulators. The two drawings required for the design are photo reduced and printed on clear Mylar. These drawings in addition to the trace patterns indicate riser position, pass-through holes and matrix to module connections. A frame outline and registration marks were included to assure alignment and indicate the overall tool size.

A sheet of the $\frac{1}{4}$-in. Teflon cut to the size of the frame outline and containing a hole pattern corresponding to the risers required is used as the holding tool. The first Mylar is positioned over the Teflon and the first riser is inserted, a nickel ribbon conductor perpendicular to the riser, and is welded in place. Another riser is inserted and the conductor welded, this continuing until the first layer is completed (Fig. 3). The second Mylar is now positioned and the process continued until the matrix is completed.

An aluminum frame is now fastened to the Teflon plate forming the encapsulation mold. The matrix is encapsulated using a DER332-DTA system and when cured the frame is removed and the matrix separated from the Teflon plate. The riser pins which were inserted into the Teflon are now protruding from the casting and these are then used as the inputs to the matrix. The matrix is drilled as indicated by the pass-through markings. The module leads inserted through these holes appear adjacent to their matrix input pins and a short length of ribbon is crosswelded between module leads and matrix pins completing the interconnect. Should module replacement be necessary clipping the cross-weld, inserting a new module and rewelding

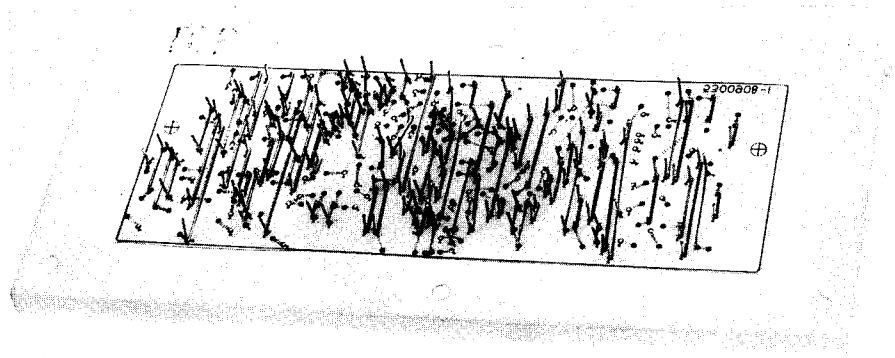


Fig. 3. Teflon base plate with Mylar and first layer welded in place.

is all that is required. The second matrix because of the minimum number of connections necessary was simply a glass epoxy board with silk screened guide lines for the point-to-point conductors.

ENCAPSULATION

The individual component modules were functionally tested and a freeze coating applied by the dipping method. A satisfactory coating has been found to be Uralane 241 mixed 10 to 1 with No. 973 Hardner.

Experience indicates that a repetition of the functional test is advisable at this point since weak connections and marginal components will often reveal themselves during the freeze-coating operation. The subject of so-called "slush molding" can usually generate a divergence of opinion in any gathering of packaging engineers. This type of tooling has been used at Lockheed Electronics Company for several years with generally satisfactory results.

Cerrotru with a melting point of 281°F and an expansion on cooling of 0.005 in./in. has proven to be a very satisfactory medium. Held at a constant temperature of 295°F, this alloy is capable of producing good molds. When used with a foam system, care should be taken to assure adequate wall thickness, as thin walls tend to bend outward under pressure.

The problem of centering the module in the mold sometimes encountered when encapsulation wall thickness is held to less than 0.05 in. was solved by designing a mold with a $\frac{1}{8}$-in. lip on the clamping shoulder.

A selection of glass epoxy board cut to fit inside the positioning lip was predrilled with a hole pattern corresponding to the module output leads. When the leads were inserted through the glass header and the module positioned in the mold, the unit was ready to be foamed.

The system selected, Eccofoam FP, is relatively easy to handle and produces a satisfactory module. Recent investigations indicate an improved product can be obtained by the use of FPH in similar applications.

In this application the mixed system was injected into the prepared module with a disposable syringe through one of the holes drilled in the mold and the excess allowed to escape through the relief hole. A little finger pressure over both holes when the system begins to turn will minimize the possibility of voids appearing when the mold is removed.

The modules requiring lab set were foamed in the same manner except that a Teflon block was used to make a recessed trough into which the lab set component could be placed (Fig. 4). The Teflon was drilled to accept the leads to which the lab set would be attached and treated as part of the module during the potting cycle.

When the Teflon block was removed, a slot with exposed leads resulted (Fig. 5). Once the correct value of lab set component had been determined, connection to the exposed leads was accomplished. Since the total system was to be encapsulated the component was left exposed.

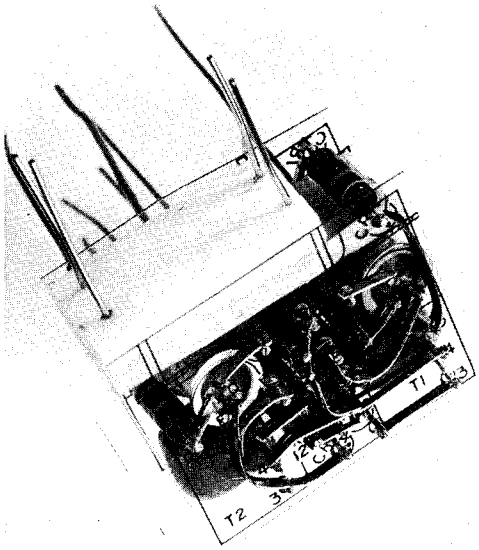


Fig. 4. Unencapsulated lab set with Teflon block in place.

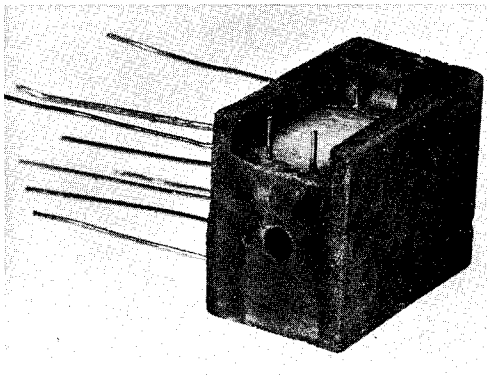


Fig. 5. Foamed lab set module with Teflon block removed.

In the prototype units, circuit changes and component replacement was found to be necessary after the modules had been foamed. The utilization of a precision air abrasive unit made this operation relatively simple. Using sodium bicarbonate as an abrasive medium, the foam and freeze coating was "sandblasted" away with no detrimental effect to either the lead material or adjoining components.

Where components had to be replaced, the foam was removed by abrasion exposing the interconnect ribbons and Mylar film. The ribbons were cut away from the component leads and a hole cut in the Mylar with an exacto knife. Further abrasion released the component from the surrounding foam. A new component was inserted and lap welded in place.

FINAL ASSEMBLY

The initial step in the final assembly consisted of welding 3-in. lengths of 0.020-in. nickel wire to the connector pins. The connectors were then mounted on the previously discussed fabricated plate.

The base matrix with modules attached was positioned behind the connector plate in such a manner that the connector leads could be inserted through the matrix. Alignment and final positioning was accomplished by the use of spacers over two machine screws; the connectors were then welded into the assembly by the same crossweld technique used to connect the modules.

The second matrix was installed in a similar manner; a second set of spacers was slipped over the machine screws and tightened. At this time, the unit was subjected to functional test, including temperature cycling. Even at this advanced stage of construction, repairs could be made in a relatively economical manner should they prove necessary.

The unit was now ready for final encapsulation. Since only four units were required, the economics of the situation, coupled with the short time factor remaining, ruled out the use of a "breakaway" machined mold.

The "one-time" capability of silastic molds was deemed adequate for this situation. To minimize the possibility of distortion, the silastic wall thickness was held to not more than 1 in. and then reinforced by an aluminum frame.

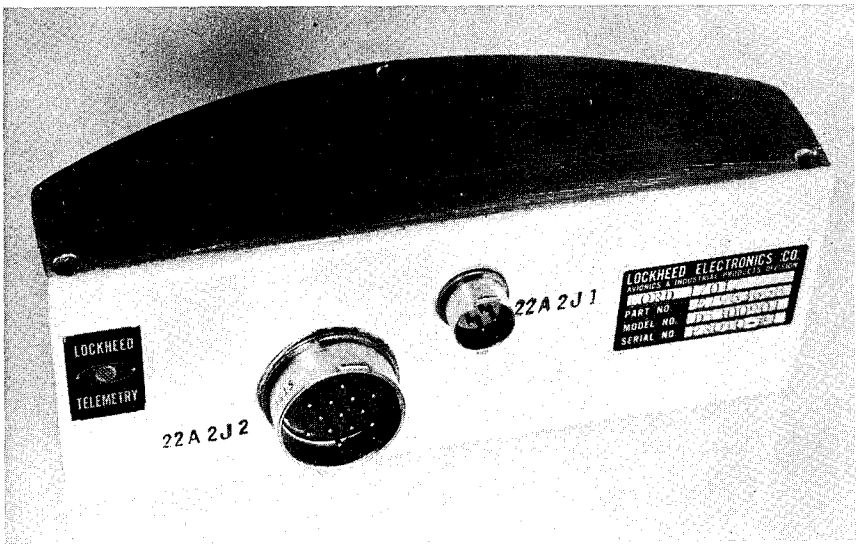


Fig. 6. Completed timer ready for shipment.

The total weight was still of concern, so the encapsulant used was a Scotchcast 8 system mixed 1 : 1 and loaded with eccospheres. The 1 oz by volume to 35 g of Scotchcast formulation resulted in a light, but rugged, outer casing.

The mold was so designed that the two surfaces formed by the fabricated plate remained exposed, their edges flush with the encapsulated sides. With the exception of the base plate, the unit was sprayed with two coats of white epoxy paint held to a maximum build-up of ten mils per coat (Fig. 6). All that remained of the task at this point was marking and testing to the customer's Acceptance Test Procedure.

The results of this effort can be summarized briefly, as follows: The 300 components, and the 1188 welds required to assemble them into a system, were housed within the required dimensions, the system performed the function required and instead of the 16 oz allowed, the four units weighed between 14 and 15 oz with an average of 14.5 oz.

CONCLUSIONS

An attempt has been made to show the freedom of form available to the designer using welded circuit techniques. Modules can be designed to many configurations and matrices can be made to assume many geometric patterns.

While the design described in this paper utilized modules mounted on only one side of the matrix, systems are presently in production at Lockheed Electronics Company which contain modules mounted on both sides of a matrix. Subsystems are being built with several modules being interconnected by use of point-to-point wiring, additional evidence of the versatility of the welded technique.

It is hoped that continuing research will result in better encapsulation systems, capable of being used in the hostile environments to which much of today's welded circuitry is eventually subjected. In the past few months, an increase has been noted in the number of component manufacturers who offer as an option, highly weldable leads; however, much more remains to be done in this field.

Sometimes referred to as an interim technique, it appears that welding, due to its flexibility, low cost, and short lead time, will remain an important segment of packaging technology for many years to come.

8071

Advanced Spacecraft Command Receiver Design

GORDON G. MESSICK
Space Technology Laboratories, Inc., Redondo Beach, California

Reliable performance of a command receiver under radiation, space vacuum, and other environmental requirements has become more critical as missions increase in complexity and cost. Today's designs show more sophistication than those used a few short years ago. Receiver stages are shielded from each other by compartmentalization of functional circuit blocks. Machined metal construction, rather than sheet metal, is used for structural parts to provide radio-frequency sealing and simplicity of design. Radiation and vacuum-resistant parts and insulation materials are fully tested and selected. Difficulties formerly encountered in soldered RF circuits are overcome with welded circuitry. With increased knowledge of requirements for space equipment, solutions to design problems have shown considerable progress.

EVOLUTION OF DESIGN

THE FIRST COMMAND receiver built by Space Technology Laboratories was for the Thor–Able series of re-entry nose cones in 1957 and 1958. Because the space environment was not known, the design followed what was considered the safest approach at that time. Layer upon layer of electronic parts was inserted into a housing and then potted in place with casting resins. A high weight penalty resulted from overdesign. Maintenance was nearly impossible. This first-generation unit was difficult to build and difficult to align. Nevertheless, this early re-entry nose cone command receiver operated satisfactorily and was a reasonably successful design.

In the latter part of 1958, a second generation command receiver was designed (Fig. 1) for a series of earth-orbiting space vehicles and deep-space probes, commonly known as the paddle-wheel satellites. This was a phase-locked command receiver operating in the 400-Mc range. The basic receiver consisted of a number of functional modular blocks. By adding or subtracting functions, many variations of the receiver could be achieved. Actually two receiver types were developed. One was a payload command receiver whose output operated a digital demodulator. The second type was a guidance receiver whose output was in the form of tones.

Originally, only seven units were to be constructed by laboratory technicians rather than production personnel. The receiver, however, proved to be very versatile and has been widely used. The design was used in such vehicles as Explorer VI and Pioneer V, and is still being used in such spacecraft as Transit, Courier, and the present Air Force 823 program. The unit has never failed to operate in any space mission. In Pioneer V (Fig. 2), the receiver functioned successfully as a communications link to a range of 22,500,000 miles into space, which has remained a record until this past year. In all, more than 120 receivers of this type have been built.

The four years in which these receivers were in production and use have made it obvious that even small-quantity spacecraft equipment should be designed for production. Also, while spacecraft equipment requires no access in actual use, all parts of the equipment are required to be accessible for testing, alignment, and prelaunch check-out. Both of these requirements have been incorporated into the design of new spacecraft command receivers now in production and in the development stage.

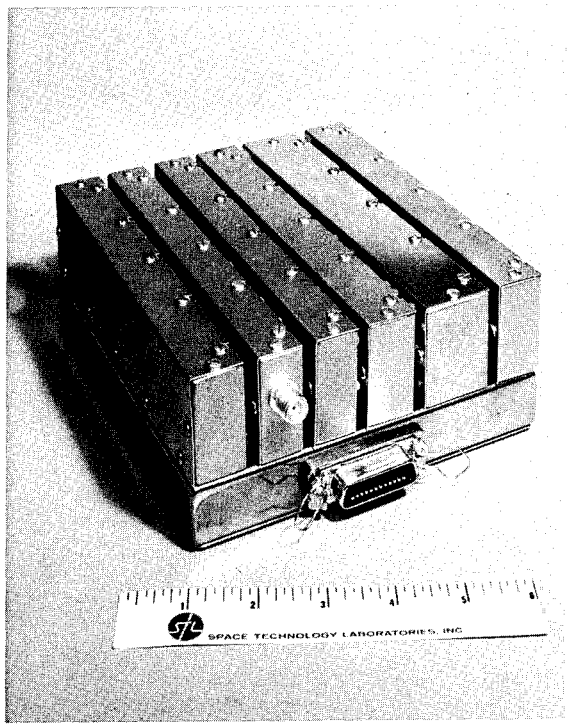


Fig. 1. Command receiver built for Able series space vehicles.

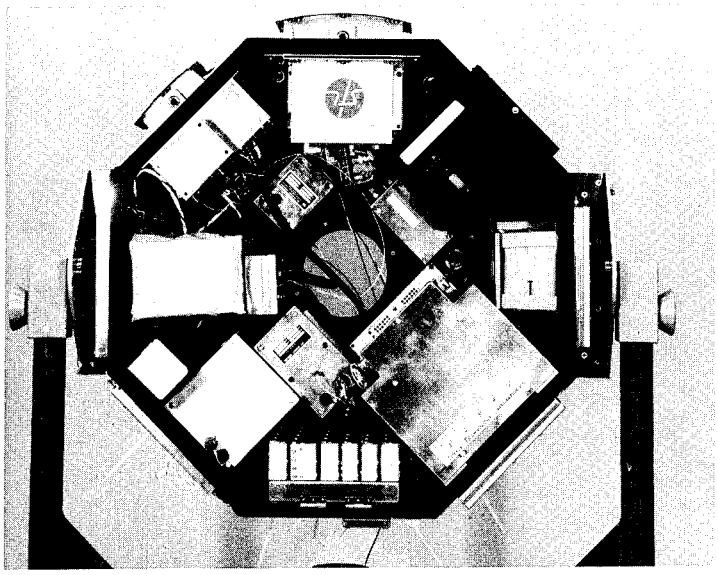


Fig. 2. Pioneer V payload, showing mounting of receiver (bottom of photo).

In 1962, complete redesign of the command receiver was undertaken. The third-generation receiver integrates the best features of the earlier units with additional requirements placed on the design by the advancing state-of-the-art. This design experience of the last year is now being utilized for the Space–Ground Link System, which is in the process of development for 1964 and 1965 Air Force space programs.

DESIGN REQUIREMENTS

The recently completed unit is a radiation-hardened 400-Mc phase-locked command receiver. This unit provides demodulated tones to a command decoder and a transmitter drive signal for Doppler tracking which is a multiple of and coherent with the received signal. Receiver sensitivity is specified as a minimum of -115 db below 1 mW.

Environmental test requirements (Table I) are typical of most spacecraft equipment, with the exception of radiation.

DESIGN FEATURES

The manner in which requirements are met is illustrated by examining some features of the third-generation radiation-hardened command receiver (Fig. 3). These features incorporate what is considered today's useful state-of-the-art. In general, emphasis is placed on simple well-integrated design. Novelty is avoided and only tested and proved techniques are used for equipment reliability and confidence.

Structure. The receiver structure basically consists of a one-piece compartmentalized housing with bolted-on covers. Both housing and covers are machined out of solid blocks of 6061 aluminum alloy. This machined construction provides the required dimensional precision, and necessary rigidity, and reduces vibration transmissibility in the critical frequency range.

Thermal. The flat surfaces of three of the receiver covers furnish a large surface (Fig. 4) for transmission of internally generated heat to the spacecraft structure. Since there is no

TABLE I

Command Receiver Environmental Test Requirements

Vibration, sinusoidal
(45 min per axis)

5 to 14 cps	0.5 in. peak to peak
14 to 40 cps	5.0 *g*, zero to peak
40 to 400 cps	7.5 *g*, zero to peak
400 to 3000 cps	15.0 *g*, zero to peak

Vibration, random (Gaussian)
(5 min per axis)
15 to 2000 cps .. 0.5 g^2/cps

Acceleration
(10 min per axis)

Longitudinal	10 *g*
Lateral	2 *g*
Normal	2 *g*

Shock

18 impact shocks
One-half sine wave acceleration of
6 ± 0.5 msec duration with
acceleration peak of 40 *g*

Thermal vacuum (5×10^{-5} mm Hg)

High temperature	165 + 5°F, 24 hr
Low temperature	−30 ± 5°F, 24 hr

Radiation (total dose for one year)

Neutrons (All energies)	1×10^{13}/cm² (90% above 0.1 MeV)
Gamma photons (All energies)	1×10^{8} carbon rads

Electrointerference: MIL-I-26600

Probability of survival for 90 days as specified: 0.925

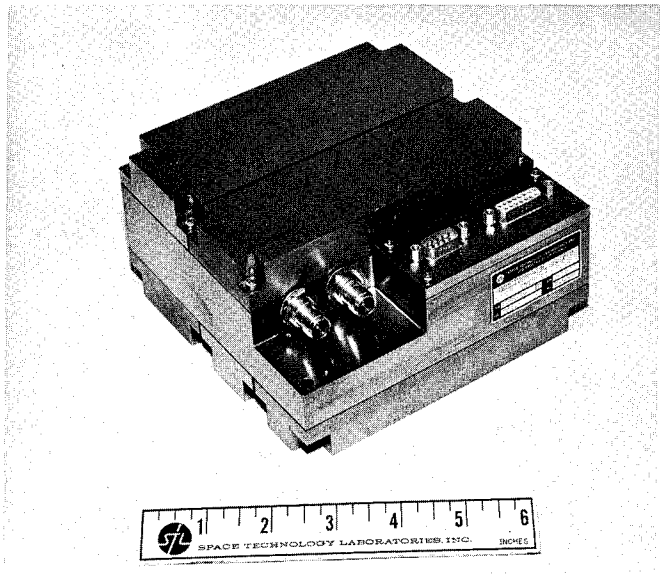


Fig. 3. Radiation-hardened command receiver (top view).

convection cooling in the space environment, the package has been carefully designed for transmission of excess heat to the spacecraft structure. If required to enhance the heat exchange, a thermally conducting silicone compound can be applied between the mounting surfaces. Physical mounting is accomplished by use of four mounting bolts through the corners of the package.

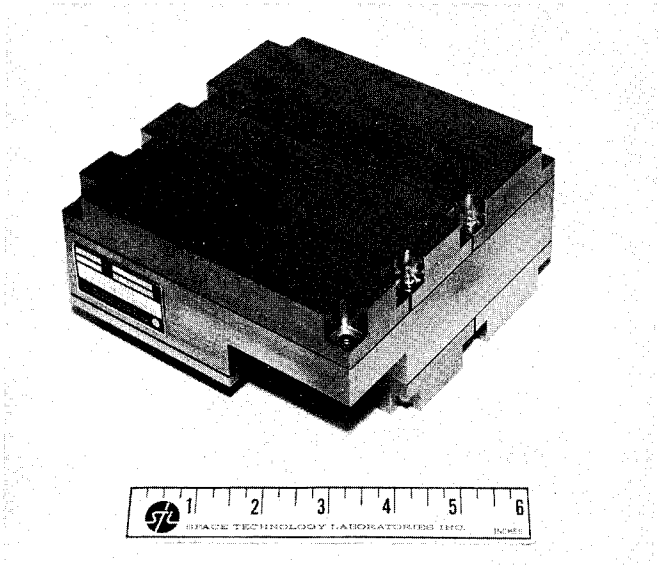


Fig. 4. Radiation-hardened command receiver (mounting surface).

External RF Shielding. Each of the covers is precision machined to provide a lip which fits closely within 0.0005 to 0.005 in. over the edge of a mating lip in the housing. This provides effective integral RF shielding against either the reception or transmission of stray electro-interference signals. Due to the nature of the sensitive phase lock receiver, the electrointer-ference requirement is particularly severe. RF shielding is accomplished in this design without use of spring fingers, woven wire gasketing, or other special shielding materials or hardware. Since the seal is provided by metal-to-metal contact on the inside surfaces, a 0.010-in. gap is allowed on the outside lip of the covers.

Functional Circuit Blocks. The receiver circuitry is subdivided functionally into six major circuit blocks, contained in a separate compartment accessible by removal of one of the five covers. Three factors were used in deciding how the circuit (Fig. 5) was to be divided into modules, thus determining the basic package of the unit. These factors were:

a. *Interconnections.* Interconnections were kept to a minimum since the usefulness of a modularized design is based on limiting the number of interconnections. The design goal for all modules, except the power supply, was one RF signal in, one RF signal out, two DC voltage lines, and one ground wire.
b. *Function.* Each module was required to be a functional entity which could be tested and aligned as a subunit.
c. *Growth Possibility.* The modules were required to be versatile so that the receiver could be easily modified for additional functions.

Circuit Boards. The circuit boards, containing all electronic parts (Fig. 6) fit inside each of the major circuit block compartments. All RF circuitry is mounted on one side of the flat gold-plated aluminum boards, with the circuitry extending into the cover, and all DC parts are mounted on the opposite side, extending into the housing. The circuit boards are mounted to the covers by screws.

Interstage RF Shielding. In addition to the shielding requirements for internally-generated and external electrointerference, it is necessary to provide RF shielding between the stages of the command receiver to prevent self-interference. This interstage RF shielding is provided in three ways:

a. Use of aluminum circuit boards to separate DC circuitry from RF circuitry.
b. Compartment walls within module covers, where required, to shield RF stages from each other. These compartment walls (Fig. 7) fit tightly against the circuit boards to provide a positive RF seal.
c. For complete isolation between modules (Fig. 8), bypass filters are used on the DC lines and coaxial connectors are used on RF signal lines where they enter or leave a module. Use of coax connectors was decided upon as a result of leakage experienced in other units in which the cable was merely passed through an elastomer grommet.

Parts Mounting. Electronic parts are arranged on the circuit boards to provide clearance for the compartment walls of the covers. Resistance welding is used to attach the parts to specially designed terminal pins. A survey of small terminals indicated a problem area in the selection of feed-throughs and standoffs. All commercial press-in type terminals used Teflon, which is prohibited by the radiation environment. Solder-in terminals with glass insulators have posts of Kovar or related alloys. Although Kovar is weldable, its conductivity, 3% of copper, results in unfavorable mass ratios when welding the wide range of lead materials used on today's electronic parts. To overcome these problems (Fig. 9), a press-in type terminal using a nickel post and a nylon base was designed. Diameter of the nickel post was selected after weld test evaluation to determine optimum diameter for compatibility with the maximum number of part lead materials. The average pull-out force for the posts is 10.4 lb. Terminals serve mainly as electrical tie points to support electronic parts prior to conformal coating with epoxy resin after electrical check-out. The coating material is a semiresilient adhesive which provides good bonding, bridges up to $\frac{1}{8}$ in., does not detune RF circuits, and permits removal and replacement of parts.

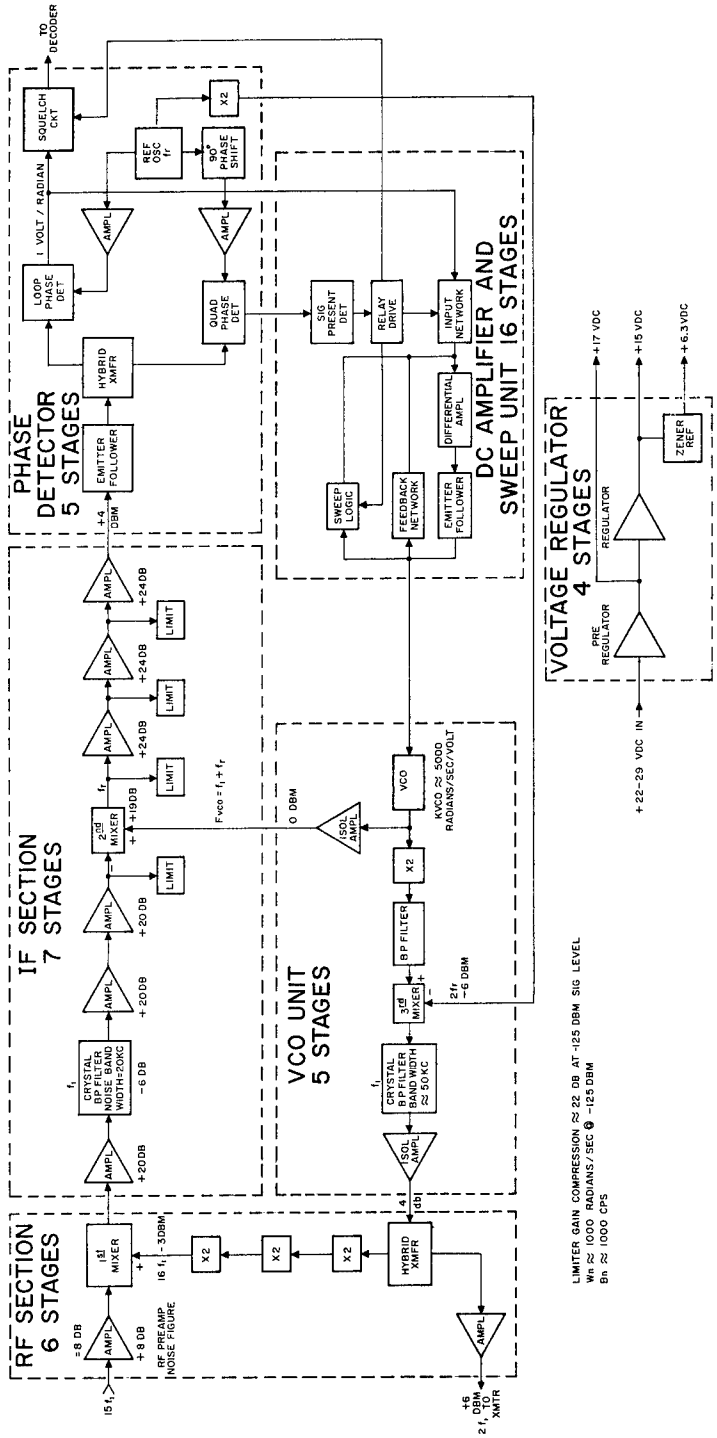


Fig. 5. Block diagram, 400-Mc phase-locked command receiver.

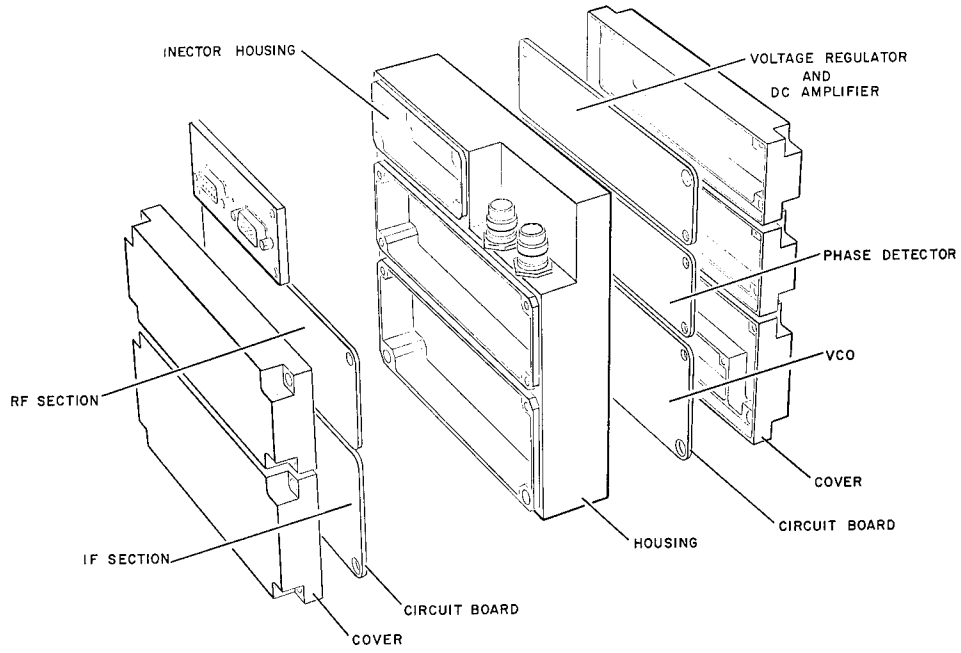


Fig. 6. Exploded view, structure of radiation-hardened command receiver.

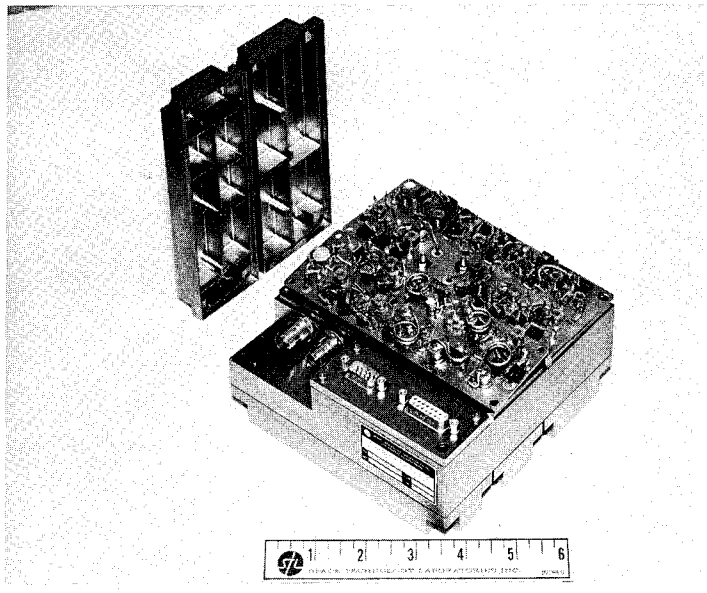


Fig. 7. Radiation-hardened command receiver, covers removed, showing compartmentalization for interstage RF shielding.

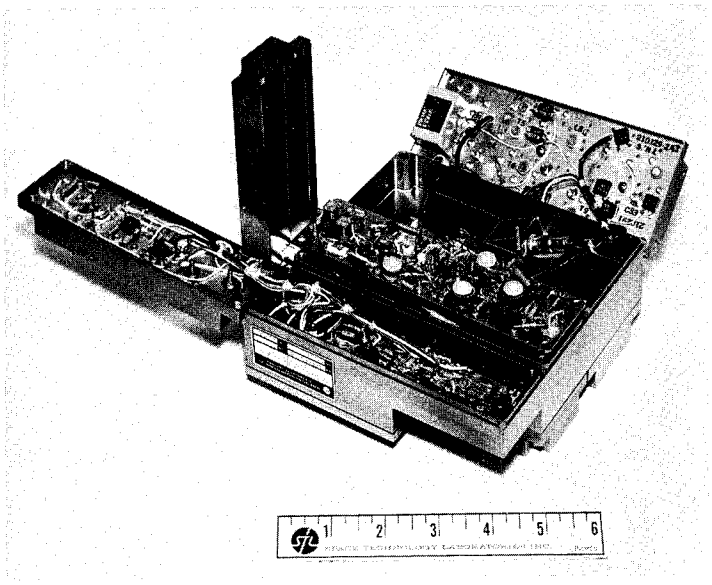


Fig. 8. Radiation-hardened command receiver, open to show DC line filters and coaxial connectors for interstage RF shielding between modules.

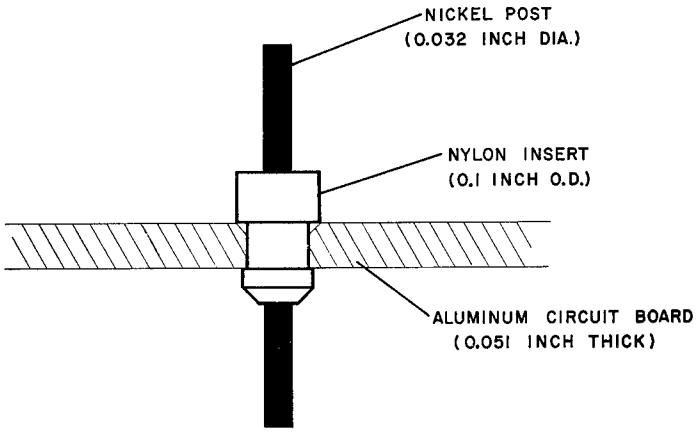


Fig. 9. Specially designed press-in type terminal.

Resistance Welding. Resistance welding is used for electrical connections, except for solid copper wires smaller than No. 28 gage (0.0126 in.) and stranded interconnecting wire, both DC and RF, which require soldering. Resistance welding offers the following advantages:

a. Heat damage to sensitive electronic parts is avoided by use of resistance welding.
b. Mechanical stress of parts is avoided since it is not necessary to wrap part leads around terminals.
c. Parts density is increased, resulting in compact circuits and maximum utilization of mounting area.
d. Welded connections produce a more reliable unit, eliminating fluxes, loose solder particles, and poor solder joints.
e. Use of a patented process for welding directly through insulated wire eliminates sleeving of jumper wires and the hazard of wire damage in stripping insulated wire.

Accessibility. Careful attention has been given to providing easy access to all electronic circuits and parts (Fig. 8). This accessibility saves many hours of time in assembly, inspection, testing, alignment, and maintenance without sacrifice of either size or weight. Test covers have been fabricated with holes to allow tuning and alignment. These adjustments may be made on the modules before or after interconnection. Following check-out, the test covers are replaced with flight covers.

Size and Weight. The receiver resulting from this design weighs 2.9 lb. It is 6 by 6 by 3 in. and contains just over 500 electronic parts. The earlier receiver it replaced was 6 by 7 by 3 in., weighed 4 lb, and contained 550 electronic parts. If the old receiver were to be used for this application, it would be necessary to add a sheet metal cover to meet the electrointerference requirement (Military Specification MIL-I-26600) which would bring the unit weight to 5.2 lb.

Growth Potential. The design approach, as briefly described here, is versatile and is now being applied to several new units, including the Air Force Space–Ground Link System, a 2.2 kMc receiver, and an X-band transponder.

Vacuum Resistant Materials. A feature of the receiver design which places restraints upon the packaging engineer, requiring considerable design and testing, is the selection of materials for resistance to the effects of space vacuum. Although the unit is completely sealed against RF leakage, hermetic sealing against the space vacuum environment is undesirable. All insulating, coating, bonding, and other plastic materials have been subjected to vacuum testing, conditioning, or evaluation to assure minimum evaporation, sublimation, or outgassing characteristics.

Other Design Features. Two additional features of the receiver design are worthy of special mention. These are (a) the use of machined rather than conventional sheet metal construction and (b) the program required to assure selection of materials resistant to nuclear radiation.

MACHINED METAL CONSTRUCTION

A special feature of this design is the use of housing and covers milled from solid aluminum stock. At first glance, this construction appears to involve high cost and excessive amounts of machine fabrication time. This, however, is not true. Costs compare favorably with conventional sheet metal construction for similar equipment. Machined construction cost is aproximately 20% less than sheet metal when fabricating a few units and drops to as much as 50% less than sheet metal for quantities of around 20 units.

Among the factors influencing the decision to use machined fabrication are the following:

Precision Requirements. Although it is possible to fabricate sheet metal to precision requirements, skilled craftsmen who can hold the necessary tolerances are difficult to find. On the other hand, many precision machinists are accustomed to working to tolerances of a few ten-thousandths of an inch.

Compartmentalization Requirements. The compartmentalized covers and coaxial connectors between modules used in this design (Fig. 10) are exceedingly difficult to fabricate with sheet metal, requiring welding or brazing of walls and brackets. The alternative method, using

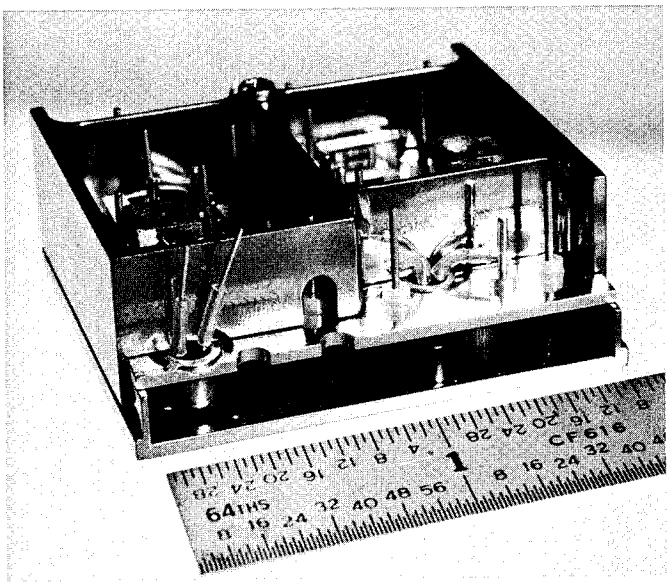


Fig. 10. Section of command receiver module showing RF sealing and compartmentalization detail.

separate sheet metal cans or covers similar to the previous receiver, would result in complications in manufacturing, assembly, and servicing.

Integrated Design. Machining makes possible simple well-integrated design with the fewest number of mechanical parts. Mechanical parts in this design perform multiple functions, serving at the same time as parts mounting boards, structural members, electrointerference shielding, and thermal transmission paths. Excess hardware is eliminated with no brackets, no troublesome sheet metal inserts, no stiffening straps, no RF sealing hardware, and only a minimum number of such parts as screws and washers.

Structural Considerations. Machined construction provides better structural characteristics than sheet metal. Integral stiffening members reduce vibration transmissibility in the specification frequency range. Weight of the structural parts, with wall thicknesses from 0.030 to 0.040 in., is comparable for both types of fabrication. The overall unit weight, however, is lower for the machined construction because the number of hardware items is reduced and integrated design makes improved arrangement of elements possible.

Growth Possibility. Changes and modifications of circuit and performance requirements may be required for each separate space mission. Milled construction makes it possible to accommodate these changes with little difficulty. If quantity production is desired for the needs of a particular program, it is possible to consider a changeover from a machined housing to a casting. With sheet metal construction, costs remain approximately the same regardless of quantity.

Dollar costs of this type of design, versus other approaches, have been carefully analyzed. In quantities less than 20, units would be milled either singly or on programmed multiple-head equipment. To evaluate costs, the housing and cover drawings were submitted to possible fabricators for bids. Use of castings was found to be practical only for quantities of more than 20 units since it is necessary to amortize the costs of initial tooling and since considerable machine finishing of the raw casting is required.

Machined construction for few-of-a-kind items of this type has been found to be so versatile and generally satisfactory that the technique is now being used in a number of other applications.

RADIATION HARDENING

The necessity for survival and operation of the command receiver in a radiation environment required an investigative program into the performance of both materials and electronic parts. A testing program was conducted at a radiation facility to determine the effects of the radiation dosage specified for this equipment.

Semiconductors. Particular stress was placed on testing of semiconductors since these are most severely affected by radiation. Results may be summarized as follows:

a. Germanium transistors with a very high alpha cutoff frequency were generally found most satisfactory.
b. Silicon transistors were not quite as good as germanium, but the differences were small for high-frequency units.
c. DC beta reductions of two and three to one from the value prior to irradiation were common for the best transistors.
d. Transistors with a high cutoff frequency prior to irradiation tended to degrade uniformly during exposure.

Transistors for use in the receiver were therefore selected for high initial DC beta and high initial cutoff frequency. Among the transistors which suffered least from radiation were the 2N707A, 2N834, 2N915, 2N918, 2N995, and 2N1493.

Some general-purpose silicon diodes were shown by test results to have radiation tolerances in excess of 10^{15} neutrons/cm^3. Zener diodes were affected by neutron irradiations in the decade of 10^{14} to 10^{15} neutrons/cm^3 with changes of approximately 1% in the reference voltage. Diodes selected for use included 1N3064, FD200, and FD600.

Passive Electronic Parts. For components other than semiconductors, radiation tests indicated that carbon composition resistors and paper capacitors were severely degraded and should be avoided. Tantalum capacitors suffered leakage currents two to four times normal under dosage rates of 1×10^{11} neutrons/cm^3 or 1×10^6 carbon rads/hr.

Materials Testing. A list of 30 metals, ceramics, and plastics contemplated for use in receiver construction was submitted for evaluation in order to establish an acceptable materials list. The two objectives of this evaluation were:

a. To avoid producing secondary sources of radiation within the receiver which would contribute to the degradation of semiconductor devices.
b. To ensure the maintenance of the physical integrity of the insulators and heat sink materials used.

Wherever test results were not available in the literature, samples were irradiated at the nuclear facility in bag tests. It was recommended that substitutes be used for the following materials: nickel, copper, gold, stainless steel, iron, Teflon, Vinyl, chromium, brass, cadmium, cobalt, mercury, rhodium, and silver.

Plating Finish. The selection of a suitable corrosion-resistant finish for the receiver structure required a compromise. In the past all receivers were finished with gold-plating over electroless nickel. Although nickel and gold are undesirable in a radiation environment since both are activated, gold has an additional disadvantage since upon activation it produces a high-energy emitting isotope which decays to mercury. Thus gold not only supplies an additional source of radiation, but may suffer a loss of physical integrity. Gold was therefore removed from the housing and covers of the receiver which were plated with electroless nickel to meet corrosion requirements. Electrical requirements for low-resistance ground returns, however, required that gold be used on circuit boards.

Radiation Design Approach. It is likely that radiation resistance will increasingly become a design requirement for spacecraft electronic equipment, both to meet space radiation environment and to withstand the effects of on-board nuclear power sources. The radiation design approach for this program has proved to be satisfactory, resulting in a command receiver which successfully met acceptance test requirements. This approach has involved a test program under radiation conditions which simulate the actual anticipated environment in order to

establish lists of both acceptable and unacceptable materials and electronic parts. In actual practice, these requirements placed considerably greater restraints upon the designer than may be obvious and required a number of design trade-off compromises.

CONCLUSION

The spacecraft command receiver design, as described, represents the third generation in a family of spacecraft receivers which have performed satisfactorily in numerous missions. The new design has met all qualification and acceptance test requirements. Ease of manufacturability, one of the major design objectives, is now being demonstrated in the fabrication of the unit.

ACKNOWLEDGMENT

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8072

Electronic Module Connectors

KENNETH W. PLUNKETT

Guidance and Control Laboratory, U.S. Army Missile Command, Redstone Arsenal, Alabama

Present military maintenance concepts require replaceable, throw-away modules. A task was initiated to develop a small connector to interconnect electronic modules with a "mother board" in a minimum of space and to permit fast and reliable module replacement. Since pin and socket type connectors require long insertion depths which dictate their minimum size, a basic connector concept was developed in which the contact insertion depth was equal to its contact spring deflection. The connector size could then be reduced to about the size of a normal header used on the output side of a module. Three prototype connectors using the basic concept were developed. All of the prototype modules were tested for contact resistance, spring force and deflection, insulation resistance, dielectric strength, humidity, altitude, thermal shock, contact life, and vibration. Evaluation of the results of the first phase of the module connector development revealed that the first connector design, a 21-contact connector, was impractical; and the second design, a ten contact connector, could be refined with major design changes. It was concluded that the third connector, which contained ten contacts, was a sound basic design that could fill the requirements for a module connector with only minor design changes.

INTRODUCTION

PRESENT MAINTENANCE CONCEPTS for military electronic equipment are based upon replaceable, throw-away subunits. The electronic subunits are now being made in the form of three-dimensional modules by a large majority of military electronic producers in preference to the familiar two-dimensional printed circuit boards. This change to 3-D modules as the basic electronic subunit has evolved because the equipment engineers needed higher packaging densities, better environmental protection, and higher component connection reliabilities obtainable in the cross-wire welding technique.

The introduction of the modules into electronic equipment has generated a common packaging problem: "How are the modules to be interconnected?" The most prevalent technique used today is to mount all the modules on printed circuit boards and solder all the connections; usually by automatic soldering techniques, where high reliability is desired. In the case where welded modules are used, interconnecting modules by soldering is inconsistent with the basic philosophy of using a connection technique that does not permit heat flow into the electronic components. More important, however, are the maintenance problems involved in replacing modules soldered onto printed circuit boards.

The repair procedure requires removal of the protective conformal coating on the printed circuit board over the solder joints, and usually from around the base of the module. If all the module output leads are on a standard grid dimension, a special heating tool may be used for melting all the solder joints simultaneously, while withdrawing the module. Otherwise, a "solder-sucker" or similar instrument must be used to remove the solder from one joint at a time before the module can be removed.

The soldering procedure to install the new module is done manually, instead of closely controlled automatic soldering. The level of quality control exercised at fourth echelon maintenance areas is generally well below that of the original manufacturing facility. The newly

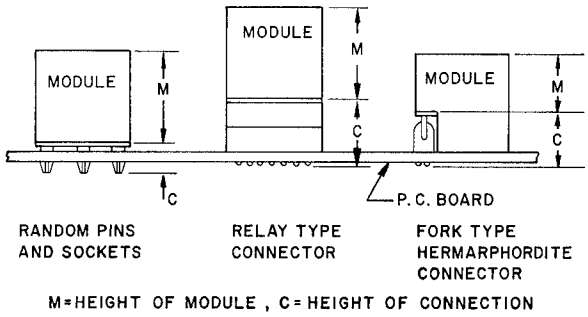


Fig. 1. Size of existing connectors reduce packaging efficiency.

replaced module, therefore, may be subjected to heat stresses if the hand-soldering is not carefully performed. The printed circuitry is likewise subjected to possible heat damage during soldering and unsoldering in repair.

The interconnection of modules by welding techniques is being used by one company, and is in various stages of development in other companies. Although the welded interconnections are much less objectional than soldering, maintenance problems still exist. In most of the techniques proposed, usually modified printed circuit boards with tabs for welding, the number of replacements from a given module location is very limited because some of the welding tab must be cut off for each replacement. If a good module is inadvertently removed, its replacement is very difficult since its leads were clipped off in removal.

The welded interconnection technique being developed by General Dynamics/Pomona overcomes the above objections by permitting repeated replacements with reweldable ribbon. Simple, foolproof welding equipment, however, is still required for field maintenance use.

Although the use of module connectors for easy replacement is obviously desirable, most engineers hesitate to use them for several reasons. First of all, only a very few connectors have been designed for use with 3-D modules. The existing module connectors and those that have been adapted for module use are so large in comparison with the module size, that the overall packaging efficiency is very low (Fig. 1). Since most of the connectors used were not designed specifically for welded modules, the connectors are difficult to integrate with the module and additional space is wasted inside the module.

Many engineers have not used pressure connections because they lack faith in the connection reliability. We at the U.S. Army Missile Command have used and specified various types of printed circuit board connectors in many of our missile systems with excellent results. Our success with the pressure connection has been dependent, of course, upon proper design and extensive testing of connector devices proposed for use.

In order to overcome the module interconnection problem previously discussed, an in-house module connector design program was started. The program objectives are to design and develop a reliable electronic module connector to interconnect modules in a minimum of space and still retain the easy module disconnect desired. The following sections of this report will describe the prototype module connectors designed and built to date, report the results of performance and environmental tests, and summarize the advantages and disadvantages of each design.

CONNECTOR DEVELOPMENT

Basic Concept

An analysis of existing connectors revealed that their large size was generally attributed to the use of pin and socket type construction. The depth of insertion of these connections was at least twenty times the actual contact spring deflection (Fig. 2). It was decided to base our connector designs on the use of a contact in which the spring contact deflection was equal to the depth of insertion (Fig. 3).

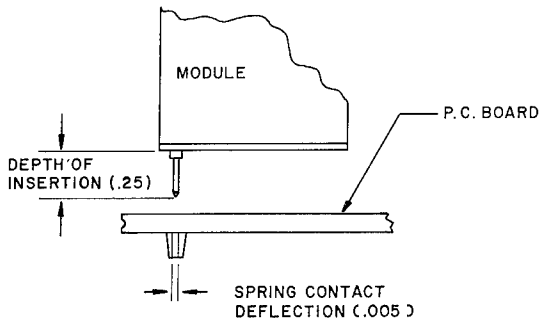


Fig. 2. Typical pin and socket-type connector insertion *vs.* deflection characteristics.

The basic spring contact used is a semielliptical spring with one free end. Wire was used as the spring material form for ease of welding inside the module, ease of tooling, and because it is readily available. Beryllium copper was chosen for the spring wire material for its well-known spring properties when heat treated. All contacts are gold-plated to prevent surface corrosion problems which may cause high resistance connections and poor welds. After considering a number of module connector concepts, it was decided to initially develop three particular connectors, build engineering prototypes, and evaluate the concepts.

Design No. 1

Design No. 1 is a 21-contact module connector consisting of two mating halves (Fig. 4). The connector was designed to have the male half (with contact springs) mounted on the module, and recessed into the module header (Fig. 5). The mating female half of the connector is made to be recessed into a printed wiring board or a welded interconnection matrix (Fig. 6). The connector would mate as shown in Fig. 7.

The physical dimensions of Design No. 1 are 0.810 × 0.350 in. The male half is 0.030 in. thick and the female half 0.050 in. thick. There are 21 contacts on 0.030-in. centers. The electrical contact, as shown in Fig. 7, is from wire spring to wire contact. All wire contacts are 0.010-in. gold-plated beryllium copper wire, and are bonded into the connector bodies with Armstrong C-1 adhesive. The connection leads of the female connector are brought out in a staggered array to facilitate connections in one plane, such as on a printed wiring board. The male half connection leads are not staggered to conserve space inside the module and because connections to the leads will probably be made at different levels within the module.

Connector No. 1 was designed to be molded of glass-filled diallyl phthalate. All development models made and tested, however, were machined from solid stock in a model shop to conserve funds before proving the design.

Contact resistance tests made on the initial Design No. 1 connector averaged 29 mΩ. While not excessive, the resistance was higher than anticipated, and was the result of very poor gold-plating, small contact area, and medium contact force.

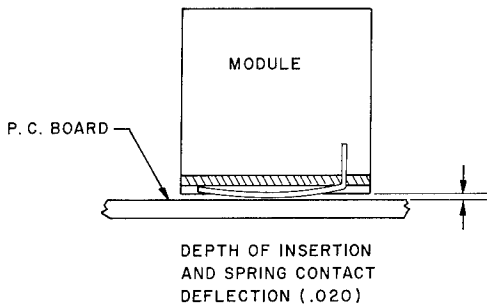


Fig. 3. The basic module connector concept.

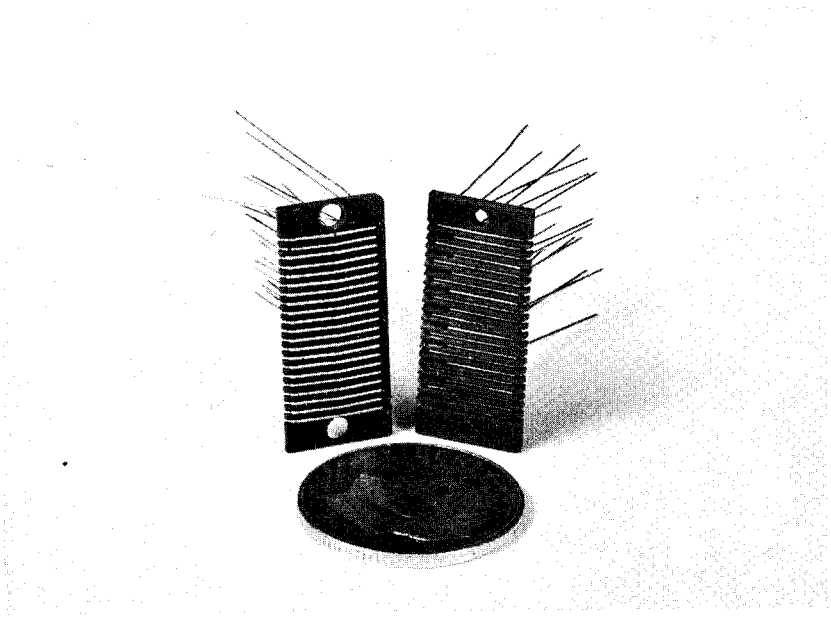


Fig. 4. Design No. 1 connectors.

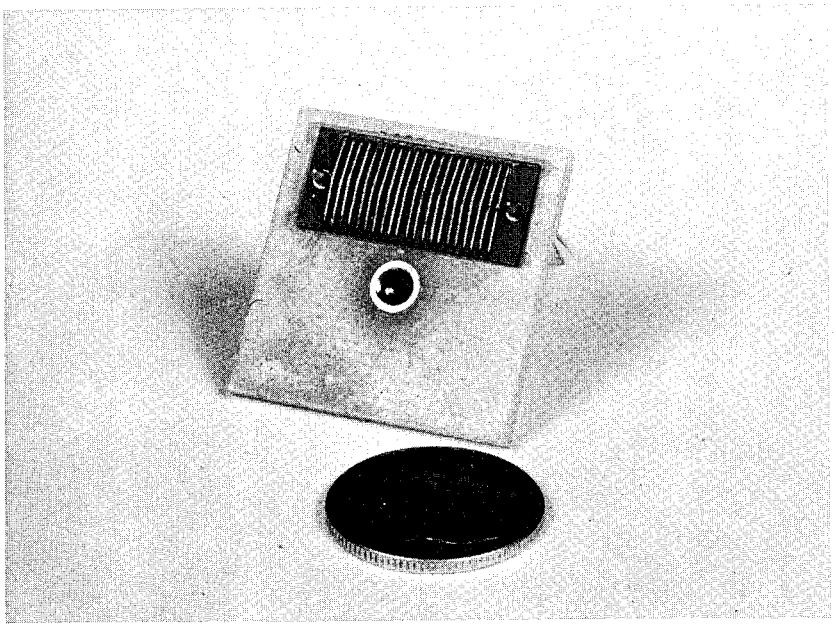


Fig. 5. Male half of Design No. 1 mounted in a module header.

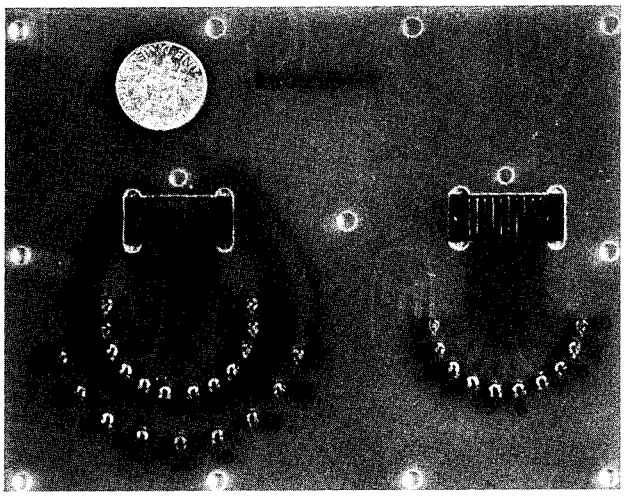


Fig. 6. Female halves of Design No. 1, on the right, and Design No. 2, on the left, mounted in the test printed wiring board.

Design No. 2

Connector Design No. 2 was initiated to improve the contact resistance obtained in Design No. 1. Design No. 2 is a ten-contact module connector consisting of two mating halves, very similar to Design No. 1 connector (Fig. 8). The mating halves are recessed into their respective assemblies as shown in Figs. 6 and 9. The female half of Design No. 2 was made with a pair of wire contacts in each slot (Figs. 8 and 10). The contacting area was doubled to reduce the contact resistance. Other differences in Design No. 2 are the 0.060-in. center-to-center contact spacing, a 0.030-in.-longer connector body, and connection leads brought out on alternate sides of the female half (Fig. 11). The materials, wire size, plating, and spring design are identical to Design No. 1. The connector body of Design No. 2 was also machined out of solid stock glass-filled diallyl phthalate for the engineering models discussed herein.

Design No. 3

Connector Design No. 3 represents a slightly different approach from our first connector design efforts. The changes evident in Design No. 3 were made after reviewing the advantages and disadvantages of the first two designs. Design No. 3 is a ten-contact module connector and case assembly consisting of a module header containing ten 0.020-in. wire spring contacts

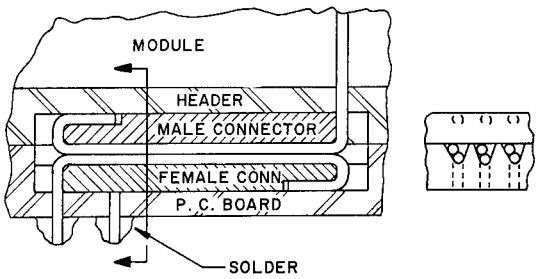


Fig. 7. Detail of Design No. 1 when mated. Note wire-to-wire contact in right section.

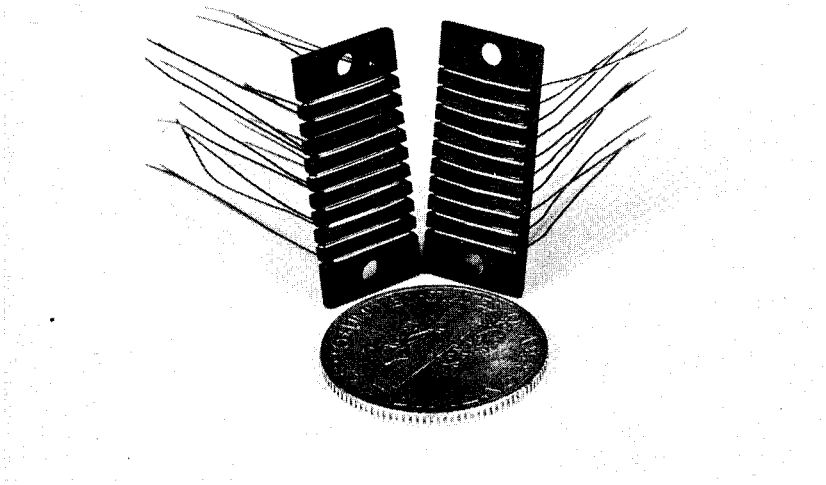


Fig. 8. Design No. 2 connectors.

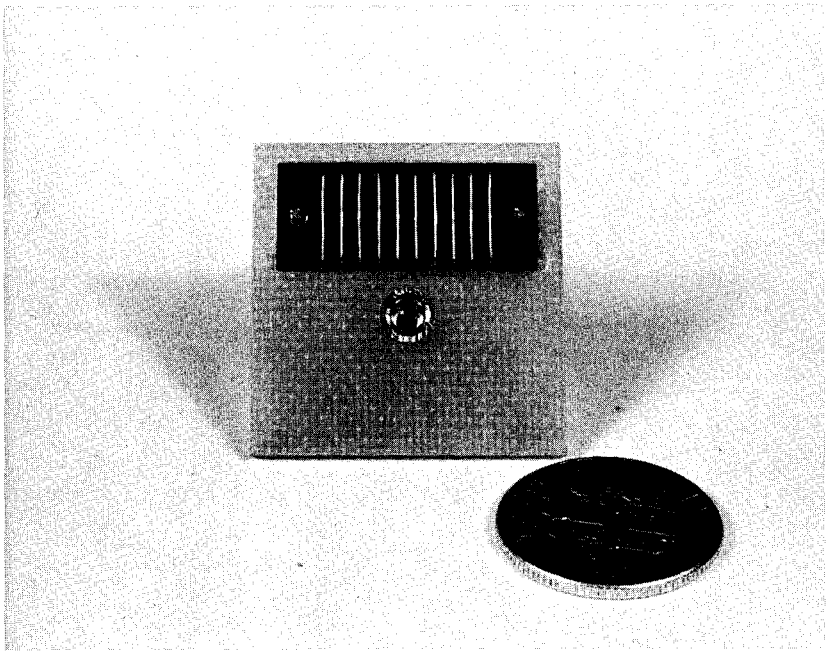


Fig. 9. Male half of Design No. 2 mounted in a module header.

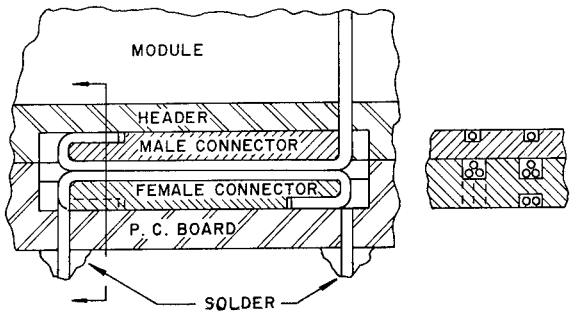


Fig. 10. Detail of Design No. 2 when mated. Note single to double wire contact in right section.

on 0.062 in. centers and a module case containing captive mounting screws (Figs. 12 and 13). The connector is designed to mate directly with the printed wiring board conductor pattern (Figs. 14 and 15). The elimination of the mating female half of the connector and the separate header results in less parts in the module assembly and thus a simpler, less expensive, and more reliable end product.

The connector body (module header) (Fig. 16) is a sturdy compression molding of glass-filled diallyl phthalate, 0.100 in. thick and 1.00 × 1.00 in. in area. The mating face is slotted to separate the wire contact springs. The slots are deep enough to allow the header mating surface to mate flush with the printed circuit board and still permit the contact spring force to maintain the electrical contact.

The contact springs which are mounted in the header are 0.020-in. gold-plated beryllium copper wires which have been heat-treated to obtain the spring properties. The free end of

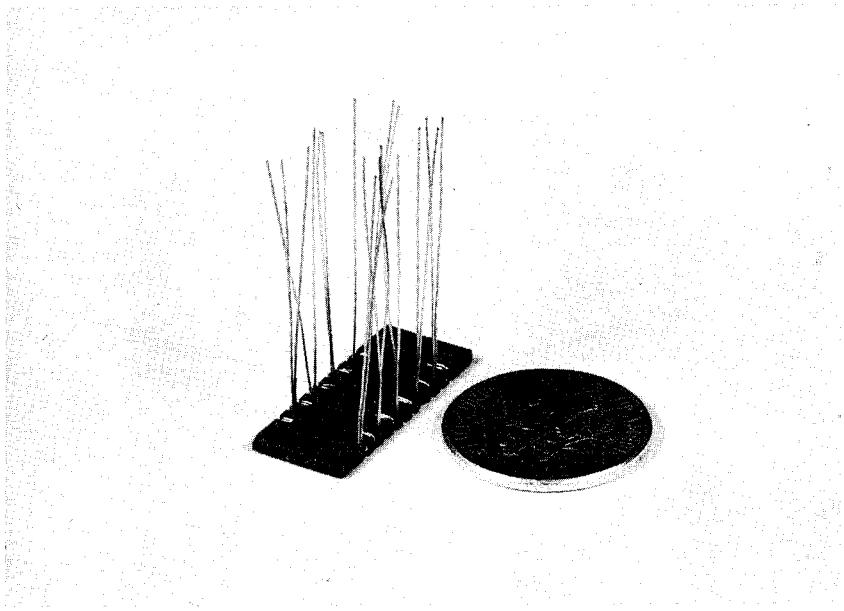


Fig. 11. Bottom side of Design No. 2 female half. Connection leads are on alternate sides.

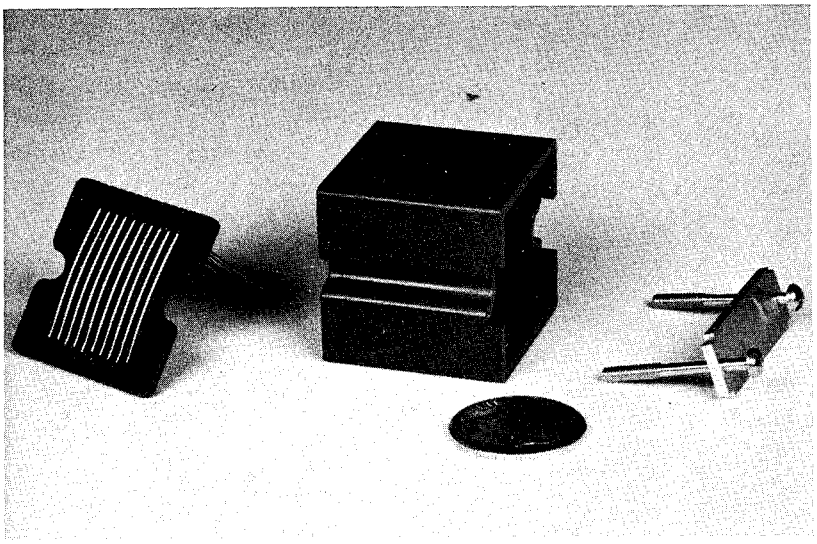


Fig. 12. Design No. 3 connector and associated parts.

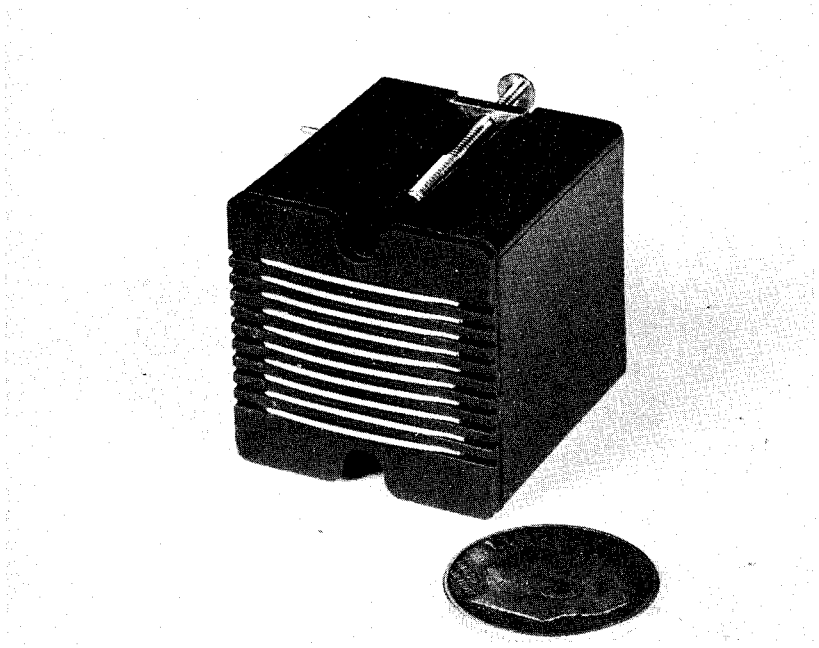


Fig. 13. Test module with Design No. 3 connector.

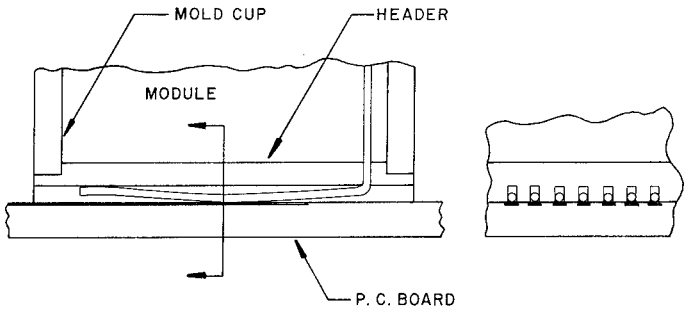


Fig. 14. Detail of Design No. 3 when mated. Note wire to printed wiring contact in right section.

this design does not bend around to the opposite side of the connector body, but remains on the mating side of the connector (Fig. 17). The initial prototype connectors of Design No. 3 used contact wire springs of 0.015-in. and 0.020-in. wire stock. The contact resistance of the 0.015-in. contacts averaged 9 mΩ and the 0.020-in. contacts averaged 3 mΩ contact resistance. Thereafter, all the Design No. 3 connectors were made with the larger springs.

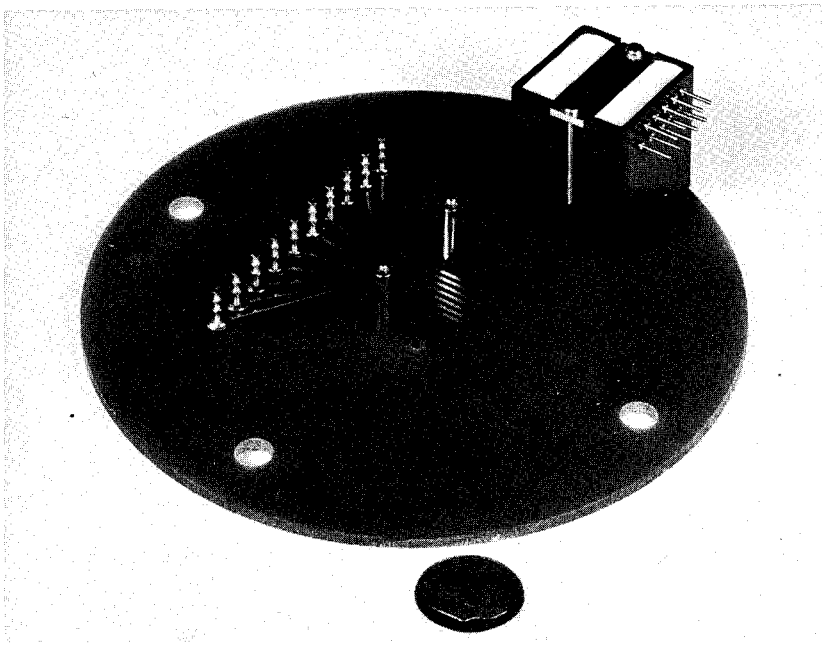


Fig. 15. Printed wiring test board and module for Design No. 3.

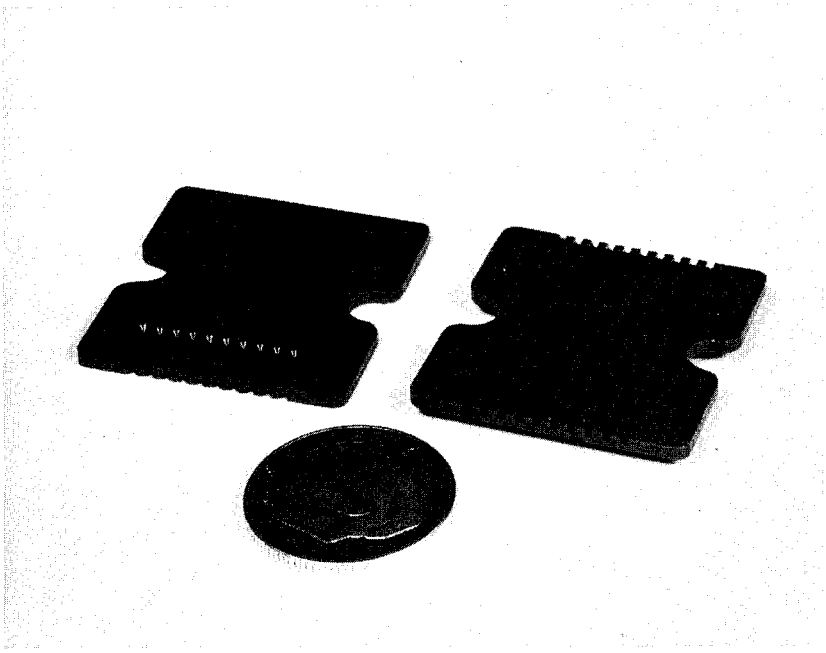


Fig. 16. Design No. 3 connector header, top and bottom views.

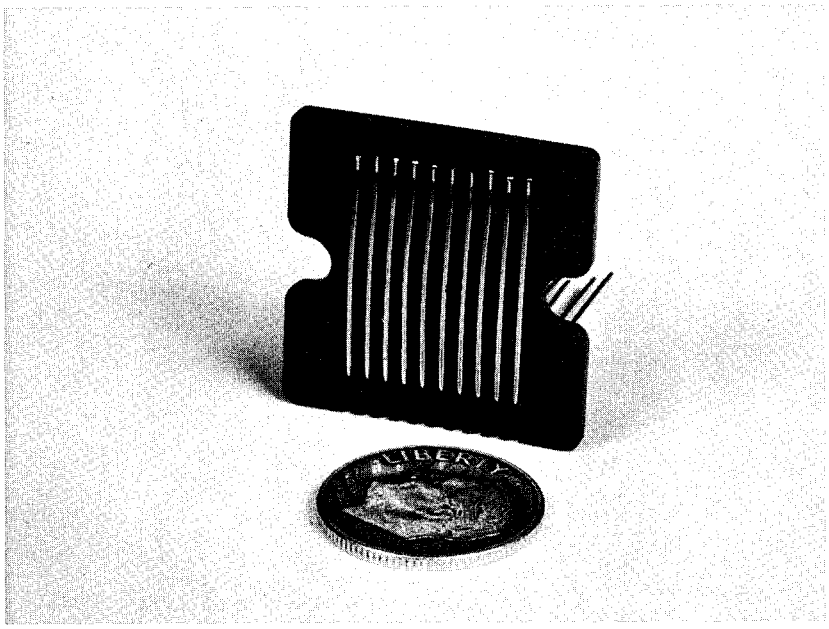


Fig. 17. Design No. 3 connector assembly.

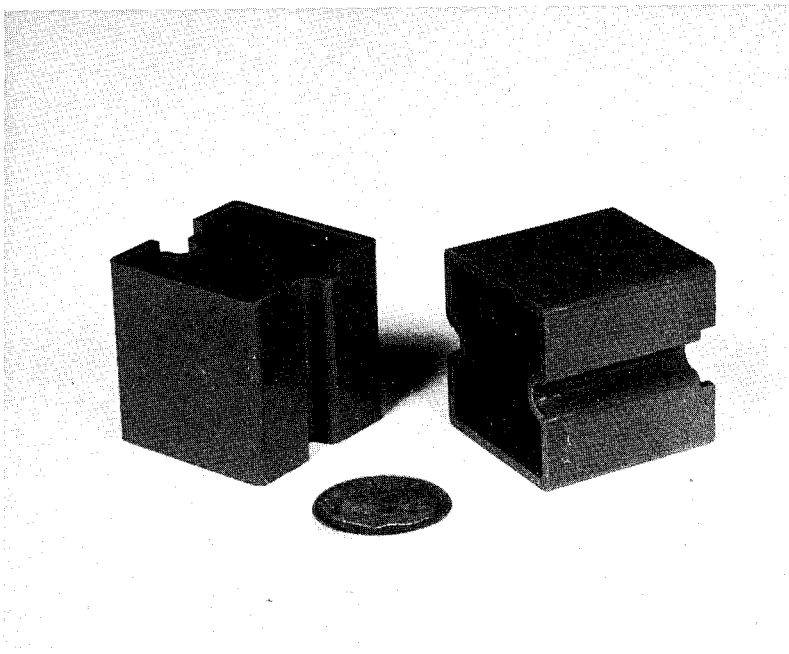


Fig. 18. Design No. 3 module case.

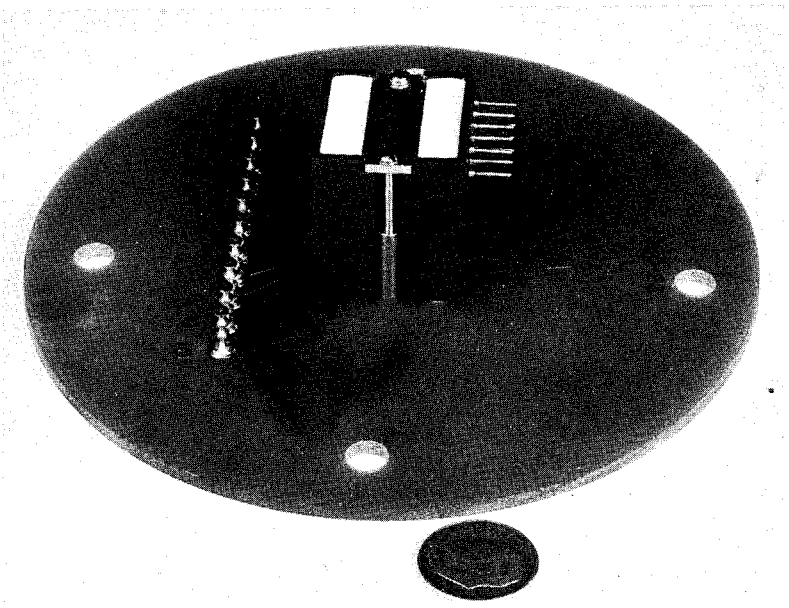


Fig. 19. Design No. 3 test module mounted on the test board between threaded mounting posts.

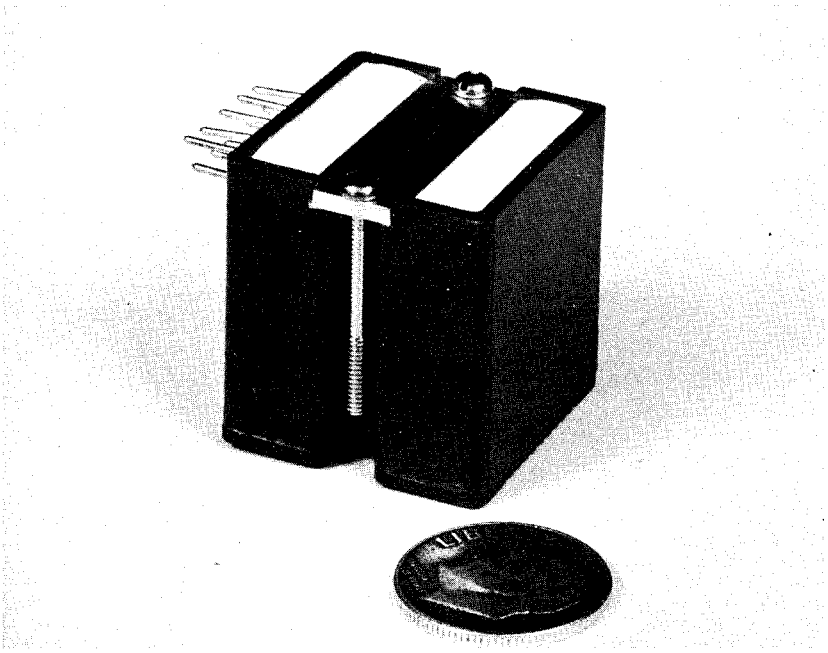


Fig. 20. Design No. 3 test module.

The module case (Fig. 18) is made to fit on the outer rim of the connector header and serve as a mold for module embedment. The module case and connector header have indented radii in both sides which act as locating surfaces when mounting the module between threaded mounting posts on the printed wiring board (Fig. 19). The threaded posts are pressed and swaged onto the printed wiring boards. The module mounting screws are captive in an aluminum bar which is placed over the module and held in place by the embedment compound (Fig. 20). All mounting parts are captive and the modules may be removed from the printed wiring board without requiring access to the bottom side of the board.

The module case is compression molded glass-filled diallyl phthalate of 0.062 in. thickness and is a 1-in. cube. The case thickness could be reduced if enough pieces were made to justify extruding the case shape.

PERFORMANCE EVALUATION

Dummy Test Modules

Nine dummy modules were made for evaluation of the connector designs; two each for Designs No. 1 and 2, and five for Design No. 3. The dummy modules were solid epoxy resin with electrical connections from each connector spring brought out of the top or side of the module for monitoring during tests. The test module for Design No. 1 is shown in Fig. 21; Design No. 2 in Fig. 22; and Design No. 3 in Fig. 20.

Difficulties were encountered while making the modules for the Design No. 1 connector. Improper sealing around the connector recessed in the header and around the header in the potting mold resulted in the epoxy resin seeping onto the connector springs and ruining two prototype Design No. 1 connectors. Fortunately, one backup connector was available for test.

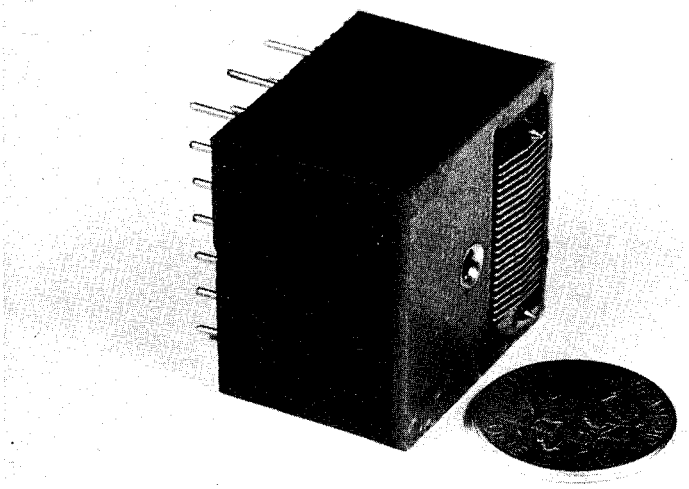


Fig. 21. Design No. 1 test module.

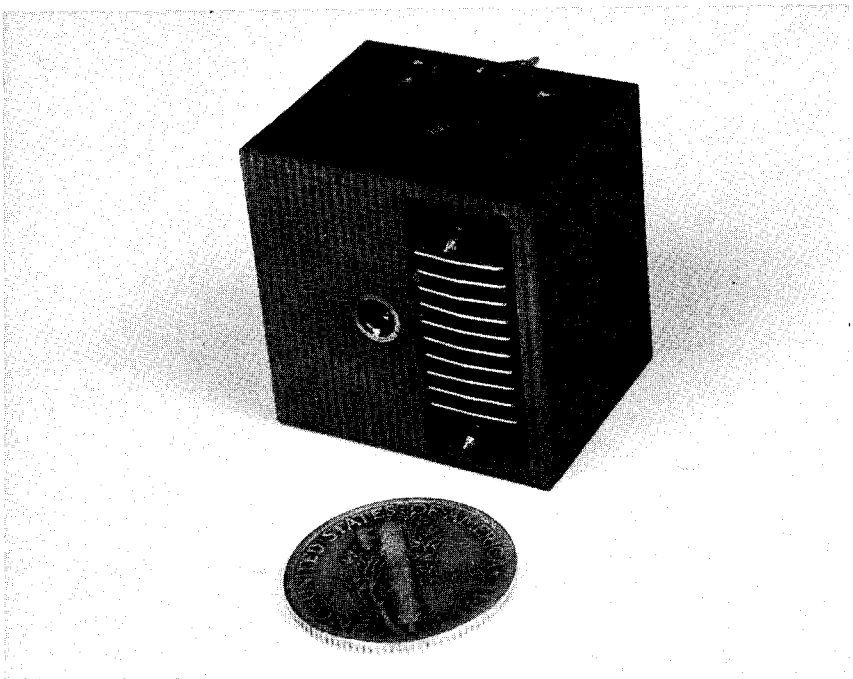


Fig. 22. Design No. 2 test module.

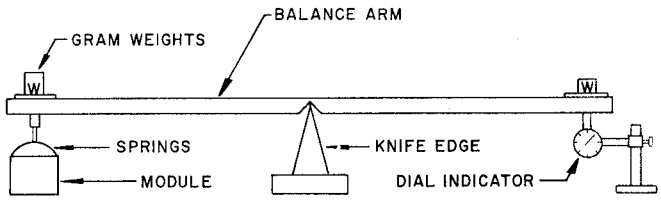


Fig. 23. Force-deflection measurement device.

Two different printed wiring boards were designed and made to simulate actual mounting and interconnection during the tests. One board, Fig. 6, contains the female halves of both Designs No. 1 and 2. The modules for Designs No. 1 and 2 connectors have a threaded insert for mounting to the printed wiring board. The other test board contains the printed wiring pattern which mates with the Design No. 3 connector (Fig. 15).

Test Criteria and Special Equipment

The test criteria for the connector design evaluation is outlined in Appendix A. The sequence of tests for each connector is shown in Table I.

The device made to measure the force-deflection characteristics of the contact springs is illustrated in Fig. 23. The unbalance in the main arm and the force exerted by the dial indicator is balanced out before measurements are taken. Since the fulcrum point is midway between the point of contact and the dial indicator, the readings taken are actual spring deflections. Weights were applied directly above the point of contact on the spring.

The equipment used to perform the life test on the Design No. 3 connector is illustrated in Fig. 24. The module was mounted on the test printed wiring board loosely so each spring could be fully deflected on each cycle. The connectors were mated at a rate of 50 cpm, using a force of 25 lb.

Discussion of Results

Design No. 1. The performance test results are summarized in Table II, and given in detail in the Appendices. Gold plating was missing during initial visual inspection in spots on all

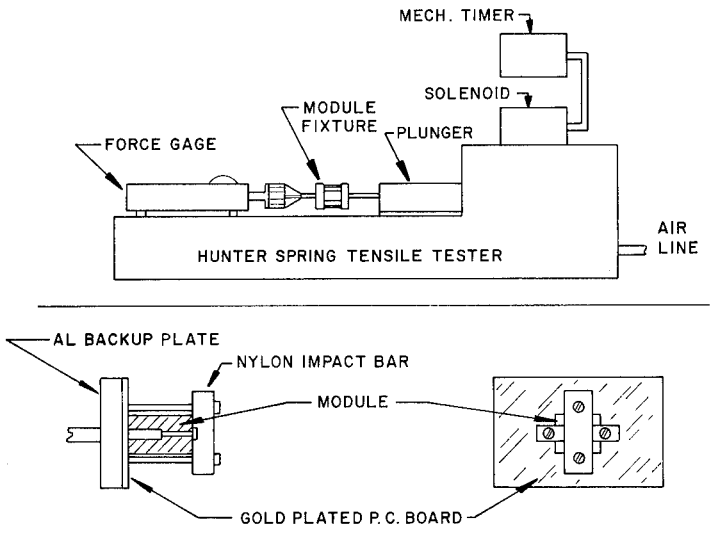


Fig. 24. Connector life test equipment and fixture.

the contacts in both mating halves. The surfaces of the connector bodies were slightly rough since the parts were machined from diallyl phthalate solid stock. The test results are better than anticipated, in view of the connectors initial condition.

Contact deflection was not as large as the design requires, especially after contact life tests. The low contact deflection probably contributed to the three contact openings which occurred during vibration tests. The mating halves of the connector were not fully recessed into their respective assemblies and prevented the module from mounting flush with the printed wiring board. This probably caused some of the rocking action of the module which was observed during vibration when the contact openings occurred.

TABLE I

Connector Test Sequence
(Paragraph Numbers Refer to Test Criteria in Appendix A)

Test module number							
1	2A	2B	3A	3B	3C	3D	3E
1.1	1.1	1.1	1.1	1.1	1.1	1.1	1.1
1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4
1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
2.3	2.3	2.3	2.3	2.3	2.3	2.5	2.5
2.4	2.2	2.2	2.4	2.4	2.4		
2.2	2.1	2.5	2.5	2.2	2.2	2.4	
2.1	2.5		2.2	2.1	2.1	2.3	
2.5	(1)	(1)	(2)	2.5	2.5	2.2	(3)

(1) Contact life not performed on these connectors.
(2) Extensive vibration and life tests were performed instead of moisture tests.
(3) After 2.5, extensive vibration tests broke several contacts. Further tests not run.

TABLE II

Summary of Performance Test Results

		Average values for all connector contacts		
		Design No. 1	Design No. 2	Design No. 3
Spring deflection (in.)	Initial	0.015	0.016	0.027
	After life test	0.012	(1)	0.024
Maximum force (oz)	Initial	16	10.2	17.8
	After life test	14	(1)	16.2
Contact resistance (Ω)	Initial	0.011	0.015	0.0010
	After life test	0.013	(1)	0.0015
Insulation resistance (M)	Initial	325,000	870,000	250,000
	After humidity	45,000	210,000	100,000
Dielectric withstanding voltage (V AC)	Initial	750	1000	1200 (3)
	At altitude	200	300	200 (3)
Continuity	During vibration	3 opens	O.K.	Broken contact
	During thermal shock	O.K.	4 opens (2)	1 open (4)

(1) Life tests were not run on these connectors.
(2) Internal module wiring opened, no contact.
(3) Printed wiring board limited maximum breakdown voltage.
(4) Misalignment to test board.

Design No. 2. The performance test results are summarized in Table II, and given in detail in the Appendices. Contact life tests were not conducted on Design No. 2, since a mating fixture was not available at the time. However, contact degradation similar to that experienced by Design No. 1 can be assumed since the contact springs are identical. The contact resistance was higher than expected. Initial visual inspection revealed some adhesive on the female contacts of module connector No. 2A, which would explain why its average contact resistance was higher than module connector No. 2B. The average contact resistance of connector No. 2B was still higher than the average for Design No. 1.

Four contacts were found open at −55°C during the last cycle of thermal shock tests and one of the four was open at 85°C on connector No. 2A. No openings occurred on connector No. 2B. Subsequent tests revealed that loss of continuity occurred because of faulty internal module wiring, and it was probably a defective weld.

Design No. 3. The performance test results are summarized in Table II and given in detail in the Appendices. A value of contact resistance can be obtained by subtracting the printed wiring resistance and internal module resistance for individual contacts listed in Appendix H from the total mated resistance given in Appendix G. This value of contact resistance varies widely from 0.0001 to 0.0003 Ω and is dependent on the shape of the contact spring. If the spring contacts the printed wiring pattern at its exit point from the module, the contact resistance value is lower than the case of the spring contacting the printed wiring at a distance further from the exit point of the module.

Initial visual inspection revealed small cracks from $\frac{1}{64}$ to $\frac{9}{64}$ in. long in the module cases immediately under some of the edges of the aluminum bar across the top of the module. These cracks occurred while curing the epoxy resin which filled the module case. Inspection after thermal shock tests indicated that these cracks were slightly elongated and several more cracks created in the same location. During the last cycle of the thermal shock test, contact No. 10 on module connector No. 3D was found to be open at −55°C, 85°C, and at room temperature. The module was removed, placed on another test board, and recycled through thermal shocks of −85°F and 225°F without any contact openings. It was determined that contact could be lost when using the original test board by moving the module to one side because of incorrect locating of the mounting posts.

Breakdown across the printed wiring connection pattern occurred while attempting to measure insulation resistance at high humidity after the ten cycles of humidity testing. This breakdown was caused by a film of water which had formed on the printed wiring board. The module was removed from the test board and the unmated connector insulation resistance measured greater than 450 M while under high humidity. All measurements were satisfactory after the drying cycle called for in the specified procedures.

When the specified vibration tests failed to open the contacts on module connector No. 3E, more severe vibration tests were made (Appendix S). The module was vibrated at resonance for five minutes with 70 *g*'s input to the vibration fixture with no failures. The contacts finally opened after the mounting screws were deliberately loosened several turns. Without removing the module, the screws were tightened again and the connector vibrated at resonance for 30 min with 30 *g*'s input to the fixture without openings. When the connector was removed, however, five connector springs were found broken at their point of entry into the header.

Since it was believed that the springs broke when the connector was vibrated with the mounting screws loose, further extensive vibration tests were made on module connector No. 3A. One mounting post on the test printed wiring board was found loose when initially mounting connector No. 3A. This post was replaced before further testing. No contact openings occurred on connector No. 3A when vibrated to the extreme levels noted in Appendix S, and connector springs were not damaged. One mounting post broke at the printed wiring board during the last 5 min of the 30-min resonant test, but the other mounting post and screw prevented the connector from losing contact.

Another broken contact was experienced on the last module connector vibrated, No. 3C. As in the case of connector No. 3E, the continuity indicator did not indicate a contact open until the module was being removed after the test. Examination of the connector, broken contact, and printed wiring board revealed that the broken contact protruded above the other

contacts at its point of exit from the module. Force was therefore exerted on the rigid portion of the contact spring rather than on the movable spring arm.

Extensive contact life tests were performed on module connector No. 3A after the extra vibration tests in an attempt to break the connector springs. The connector springs were still effective, however, after a total of 45,000 mating cycles. The connector performance after these extra tests is outlined in Appendix T.

DESIGN EVALUATION AND CONCLUSIONS

Design No. 1

Only limited conclusions can be made on test results of one connector. Satisfactory module connector performance could be achieved by design improvement, but a designer has several disadvantages to consider if he needs to use this small 21-contact connector.

Special care must be taken in cementing the contacts into the connector, and the connectors into the header and printed wiring board to avoid getting cement onto the contacts. The connector must be properly cemented into the module header to prevent the module embedment compound from seeping through onto the connector. The machining of the recesses into the printed wiring board and the module header would increase the cost of fabricating an assembly using the Design No. 1 connectors. The close spacing of the 21 contacts would also require careful layout and welding techniques inside the module to avoid any possible short circuits.

In an assembly requiring high-density connections, very compact packaging, and ease of replacement, the connector design does offer a solution. The 21 connections are made in a volume only slightly larger than that required for soldering a module directly to a printed wiring board. The connector is versatile in that it may be used in modules of various sizes and shapes, with printed wiring boards or welded-wire matrices, or utilized to connect module to module directly as shown in Fig. 25.

Design refinement of Design No. 1 will not be attempted. Only isolated interconnection problems would justify the extra cost involved to attain the connection density offered by the connector. Any further use of the connector would require that adequate process controls be established for heat treating, plating, cementing, and assembling the connector parts to obtain a reliable connector.

Design No. 2

A review of the performance of the Design No. 2 connector indicates that the double-wire contact in the female half did not reduce its contact resistance value below that of Design No. 1 as intended. Evidently, the resistance of the wire contact itself is the major contributor to the contact resistance value measured, rather than the resistance of the contact interface.

The use of only ten contacts on 0.060 in. centers did increase the voltage breakdown safety factor and resulted in simplified layout and welding of the internal module connections. However, the double-wire contacts in the female half made assembly to the printed wiring board a tedious process. Design No. 2 also had the same problems of cementing and mounting the

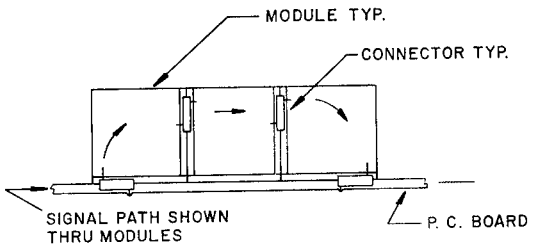


Fig. 25. Use of Design No. 1 connector for module to module interconnection.

connector into recesses in the module header and printed wiring board previously discussed for Design No. 1.

Design No. 2 would be improved by eliminating the female half of the connector, which is recessed into the printed wiring board. Fewer parts would be required and the connector simplified by mating the module connector directly to the conductor pattern on a printed wiring board. This can be accomplished easily since the contact spacing is on 0.060 in. centers. Further development would also require establishment of process controls for contact forming, heat treating, plating, and assembly.

Design No. 3

Connector Design No. 3 is small, simple, and rugged. It will maintain a low contact resistance and operate reliably under high vibration levels and after numerous contact matings. The small number of parts involved, the simple assembly operation, the use of the module case for embedment, and the extension of the round wire contacts up into the module for interconnection will make the module connector economical to use. Module replacement is fast and simple, and the connection is just as reliable as the initial assembly. Access is required to only one side of the "mother board" for installing or removing the modules, the mounting hardware is captive, and the connector alignment to the printed wiring board is determined by the mounting posts.

The test and evaluation of the prototype connector indicated that several design improvements were required for further development of the connector. Some method of indexing the connector to the printed wiring board must be incorporated in the next design to prevent mounting the module connector 180° out of alignment, thus reversing the contacts.

One weak point in the module connector assembly under high vibration was the mounting posts which were swaged into the printed wiring board. The mounting posts used in the prototype evaluation tests were drilled and tapped down to the point where the post entered the printed wiring board. The post was thus weakened at its highest stress point by unnecessarily reducing its wall thickness. The mounting post will be redesigned to give it maximum strength at its high stress point and another material will be chosen for more strength.

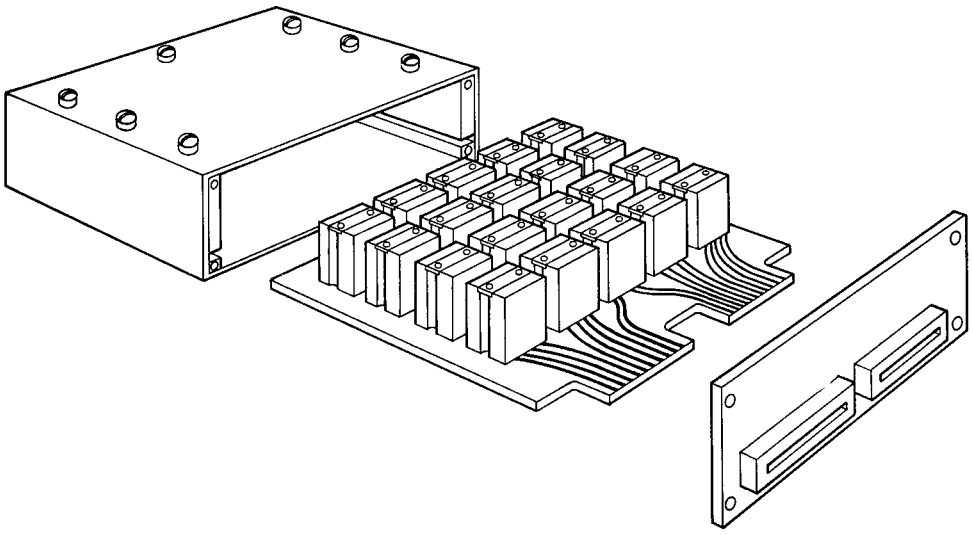


Fig. 26. Example of Design No. 3 connectors used in an electronic assembly.

Improved reliability under high vibration will also be assured by changing the connector header, the contact heat treatment, and the shape of the contact spring. Future contact springs will have to be formed with tooling that will permit good repeatability of the contact curvature. A larger chamfer will be used on the contact spring holes in the connector header to match the radius of the 90° bend in the contact spring. These two changes should permit the spring to make contact only at its point of good flexibility. Improved methods of heat-treating beryllium copper will also be used to increase the spring's ductility while retaining good spring properties.

With the present configuration of the module case and mounting strap, it is not possible to fill the module case with embedment compound flush with the top of the module. The gaps on the top edges of the module case allows the embedment compound to spill out. The design of the module case and mounting strap must be altered to permit complete embedment of the module and to strengthen the stress points which cracked during curing of the embedment compound.

If the connector is to be used in conditions of high humidity, the printed wiring conductor pattern must be sealed from moisture. An alternative solution may be to use two rows of contact springs of shorter length with increased spacing on the connector. This would permit the printed wiring conductor spacing to be doubled. While a design of this nature may pass a humidity test under controlled conditions and with very clean test boards, reliable operation under actual use could not be predicted. A redesign of the connector will include a seal to prevent moisture from bridging the printed conductor pattern.

After redesign of the module connector to correct all deficiencies found in the prototype models, complete qualification tests must be completed and evaluated before the connector is used in military equipment. It is felt that the final design of the connector will be a reliable product to assist the engineer with the problems of packaging electronic equipment, such as shown in Fig. 26, for fast and reliable maintenance.

APPENDIX A: TEST CRITERIA FOR CONNECTOR DESIGN-EVALUATION

1.0 Initial Measurements

1.1 *Visual Inspection:* Inspect all connectors, modules, and test boards, and record description and location for any physical defects such as burrs, cracks, pits, and uniformity of gold plating. Use microscope as required for close inspection.

1.2 *Force-Deflection:* Measure the initial height and the force-deflection characteristics of each connector spring.

1.3 *Contact Resistance:* Measure the contact resistance of each connector contact while properly mated, using a Keighley Model 502 milliohmmeter and the four-terminal procedure per MIL-STD-202B, Method 307. The resistance will be measured from the printed circuit wiring immediately adjacent to the module to the base of the test pins on the module. (The internal module connection resistance will be previously determined for evaluation of the actual contact resistance portion of the overall resistance readings.)

1.4 *Insulation Resistance:* Measure the insulation resistance between all connector contacts as per MIL-STD-202B, Method 302, Test Condition B. Use electrification time of 2 min and consistent polarity on all tests. (Designs No. 1 and 2 will be mated to the printed circuit board for tests; Design No. 3 will be tested on and off the printed circuit board.)

1.5 *Dielectric Strength:* The dielectric withstanding voltage will be measured between all connector contacts as per MIL-STD-202B, Method 301, for a duration of 60 sec. Determine the breakdown voltage for each connector and test printed wiring board. Conduct subsequent test at voltage levels just below the breakdown levels determined. (Designs No. 1 and 2 will be tested while mounted on the test printed wiring board; Design No. 3 will be tested on and off the test board.)

2.0 Environmental Tests

2.1 *Moisture Resistance:* The connectors shall be tested as per MIL-STD-202B, Method 106A, except steps 7A and 7B shall be omitted. Perform insulation resistance test per paragraph 1.4 before and after the humidity cycles.

2.2 *Thermal Shock:* Subject the connectors to thermal shock as per MIL-STD-202B, Method 107A, Test Condition A. On the last cycle measure the contact resistance of each contact at each temperature extreme (i.e., at −55°C and at 85°C). Inspect visually for physical damage.

2.3 *Altitude:* The dielectric withstanding voltage will be measured as per paragraph 1.5 while the connectors are under the conditions specified in MIL-STD-202B, Method 105, Test Condition D. The corona starting voltage will be determined for each connector and printed wiring board at the specified altitude. Subsequent test will be conducted at voltage levels just below the corona starting voltage.

2.4 *Contact Life:* (Design No. 3 only) Subject each connector to 3000 mating cycles to a gold-plated two-ounce copper-clad printed circuit board. Visually inspect the connector contacts for wear before and after the test. At conclusion of the life test perform contact resistance tests per paragraph 1.3 and force-deflection tests per paragraph 1.2.

2.5 *Vibration:* All connectors shall be subjected to vibration as per MIL-STD-810, Method 514, Test Nomenclature 4A3C. Monitor the connectors for discontinuities exceeding 10 microseconds while being vibrated in each of the three mutually perpendicular axes. Visually inspect the connectors and mounting hardware for physical damage after test.

APPENDIX B: INITIAL FORCE-DEFLECTION DESIGN NO. 1

Contact	Module No. 1		Contact	Module No. 1	
	Spring deflection, in.	Maximum force, oz		Spring deflection, in.	Maximum force, oz
1	0.013	16	13	0.016	18
2	0.014	18	14	0.016	16
3	0.018	16	15	0.015	16
4	0.017	16	16	0.015	16
5	0.016	16	17	0.015	18
6	0.016	14	18	0.015	18
7	0.014	16	19	0.016	16
8	0.017	14	20	0.017	14
9	0.015	16	21	0.014	14
10	0.016	16	High	0.018	18
11	0.015	16	Low	0.013	14
12	0.015	16	Avg.	0.015	16

APPENDIX C: INITIAL FORCE-DEFLECTION DESIGN NO. 2

Contact	Module 2A		Module 2B	
	Spring deflection, in.	Maximum force, oz	Spring deflection, in.	Maximum force, oz
1	0.018	14	0.017	10
2	0.016	18	0.015	8
3	0.016	12	0.017	8
4	0.016	12	0.019	10
5	0.013	8	0.014	8
6	0.015	8	0.016	8
7	0.015	14	0.015	8
8	0.015	12	0.018	10
9	0.015	10	0.014	8
10	0.015	10	0.014	8
High	0.018	18	0.019	10
Low	0.013	8	0.014	8
Avg.	0.015	12	0.016	8.6

Spring deflection—(20 readings) High .. 0.019, Low .. 0.013, Avg. .. 0.016

Maximum force—(20 readings) High .. 18, Low .. 8, Avg. .. 10.2

APPENDIX D: INITIAL FORCE-DEFLECTION DESIGN NO. 3

Contact	Module 3A		Module 3B		Module 3C		Module 3D		Module 3E	
	Spring flexure, in.	Maximum force, oz	Spring flexure, in.	Maximum force, oz	Spring flexure, in.	Maximum force, oz	Spring flexure, in.	Maximum force, oz	Spring flexure, in.	Maximum force, oz
1	0.023	16	0.022	16	0.027	18	0.025	14	0.027	18
2	0.027	20	0.026	18	0.020	14	0.030	20	0.027	16
3	0.026	16	0.026	18	0.027	20	0.031	20	0.027	18
4	0.032	22	0.028	20	0.023	16	0.030	18	0.031	18
5	0.031	22	0.027	18	0.028	18	0.029	18	0.026	16
6	0.028	20	0.025	18	0.028	18	0.031	20	0.028	18
7	0.027	20	0.031	22	0.025	16	0.031	20	0.029	18
8	0.029	20	0.025	18	0.021	14	0.029	18	0.027	16
9	0.024	16	0.028	20	0.028	18	0.030	20	0.025	16
10	0.024	16	0.024	16	0.017	12	0.022	16	0.025	16
High	0.032	22	0.031	22	0.028	20	0.031	20	0.031	18
Low	0.023	16	0.022	16	0.017	12	0.022	14	0.025	16
Avg.	0.027	18.8	0.026	18.4	0.024	16.4	0.029	18.4	0.027	17.0

Spring deflection—(50 readings) High .. 0.032, Low .. 0.017, Avg. .. 0.027

Maximum force—(50 readings) High .. 22.0, Low .. 12.0, Avg. .. 17.8

APPENDIX E: INITIAL CONTACT RESISTANCE

DESIGN NO. 1

Contact	Printed wiring resistance, Ω	Internal module resistance, Ω	Total mated resistance, Ω	Contact resistance, Ω*
1	0.0118	0.039	0.060	0.009
2	0.0114	0.029	0.0595	0.009
3	0.0139	0.034	0.054	0.006
4	0.0249	0.037	0.074	0.012
5	0.0138	0.029	0.060	0.017
6	0.0238	0.034	0.068	0.010
7	0.0145	0.036	0.065	0.015
8	0.0228	0.029	0.063	0.011
9	0.0148	0.034	0.055	0.006
10	0.0212	0.037	0.067	0.009
11	0.0150	0.028	0.058	0.015
12	0.0271	0.032	0.069	0.010
13	0.0157	0.035	0.066	0.015
14	0.0217	0.027	0.058	0.009
15	0.0137	0.033	0.060	0.013
16	0.0252	0.035	0.072	0.012
17	0.0131	0.027	0.054	0.014
18	0.0263	0.031	0.069	0.012
19	0.0129	0.036	0.064	0.015
20	0.0260	0.030	0.066	0.010
21	0.0106	0.033	0.055	0.011
High				0.017
Low				0.006
Avg.				0.011

* Contact resistance is the total mated resistance less the printed wiring and internal module resistance.

APPENDIX F: INITIAL CONTACT RESISTANCE

DESIGN NO. 2

		Module 2A			Module 2B		
Contact	Printed wiring resistance, Ω	Internal module resistance, Ω	Total mated resistance, Ω	Contact* resistance, Ω	Internal module resistance, Ω	Total mated resistance, Ω	Contact* resistance, Ω
1	0.0118	0.0520	0.085	0.021	0.040	0.062	0.010
2	0.0111	0.0430	0.069	0.015	0.044	0.071	0.016
3	0.0158	0.0470	0.078	0.015	0.040	0.071	0.015
4	0.0112	0.0410	0.067	0.015	0.043	0.067	0.013
5	0.0140	0.0480	0.082	0.020	0.037	0.064	0.013
6	0.0120	0.0430	0.077	0.022	0.042	0.061	0.007
7	0.0142	0.0460	0.076	0.016	0.037	0.064	0.013
8	0.0117	0.0420	0.072	0.018	0.042	0.066	0.012
9	0.0137	0.0490	0.078	0.015	0.039	0.064	0.011
10	0.0100	0.0460	0.073	0.017	0.044	0.067	0.013
High			0.022				0.016
Low			0.015				0.007
Avg.			0.017				0.012

* Contact resistance is the total mated resistance less the printed wiring and internal module resistance.

APPENDIX G: INITIAL TOTAL MATED RESISTANCE

DESIGN NO. 3

	Resistance in Ohms				
	Module connector number				
Contact*	3A	3B	3C	3D	3E
1	0.0124	0.0119	0.0146	0.0128	0.0124
3	0.0113	0.0122	0.0122	0.0126	0.0122
5	0.0116	0.0118	0.0136	0.0124	0.0113
7	0.0125	0.0121	0.0132	0.0130	0.0128
9	0.0121	0.0116	0.0128	0.0120	0.0130
High	0.0125	0.0122	0.0146	0.0130	0.0130
Low	0.0113	0.0116	0.0122	0.0120	0.0113
Avg.	0.012	0.012	0.013	0.013	0.012
2	0.0128	0.0136	0.0123	0.0131	0.0146
4	0.0133	0.0132	0.0120	0.0137	0.0132
6	0.0138	0.0130	0.0136	0.0130	0.0129
8	0.0126	0.0130	0.0128	0.0140	0.0142
10	0.0126	0.0124	0.0127	0.0123	0.0131
High	0.0138	0.0136	0.0136	0.0140	0.0146
Low	0.0126	0.0124	0.0120	0.0123	0.0129
Avg.	0.013	0.013	0.013	0.013	0.014

Odd-numbered contacts (25 readings)—Avg. .. 0.012.

Even-numbered contacts (25 readings)—Avg. .. 0.013.

* Internal module wiring is slightly shorter for odd number contacts.

APPENDIX H: PRINTED WIRING AND INTERNAL MODULE RESISTANCE

DESIGN NO. 3

	Resistance in ohms					
		Internal module wiring				
Contact	Printed wiring	3A	3B	3C	3D	3E
1	0.0013	0.0094	0.0094	0.0118	0.0098	0.0102
3	0.0016	0.0095	0.0096	0.0096	0.0096	0.0095
5	0.0017	0.0096	0.0097	0.0096	0.0097	0.0095
7	0.0016	0.0095	0.0097	0.0095	0.0097	0.0097
9	0.0014	0.0096	0.0096	0.0098	0.0097	0.0102
Avg.	0.0015	0.0095	0.0096	0.0100	0.0097	0.0098
2	0.0015	0.0106	0.0106	0.0105	0.0104	0.0105
4	0.0015	0.0106	0.0104	0.0101	0.0106	0.0107
6	0.0015	0.0104	0.0108	0.0106	0.0106	0.0107
8	0.0014	0.0106	0.0106	0.0103	0.0106	0.0106
10	0.0014	0.0104	0.0106	0.0106	0.0106	0.0104
Avg.	0.0015	0.0105	0.0106	0.0104	0.0106	0.0106

Internal module wiring: Odd-numbered contacts (25 readings)—Avg. .. 0.0097
Even-numbered contacts (25 readings)—Avg. .. 0.0105

Average total wiring resistance: Odd-numbered contacts—0.011. Even-numbered contacts—0.012.

APPENDIX I

Initial Insulation Resistance

1. *Design No. 1—Mated—20 Readings*
   High .. 400,000 M
   Low .. 250,000 M
2. *Design No. 2—Mated—18 Readings*
   High .. 2,000,000 M
   Low .. 300,000 M
3. *Design No. 3—Unmated—45 Readings*
   High .. 280,000 M
   Low .. 190,000 M
4. *Design No. 3—Mated—45 Readings*
   High .. 300,000 M
   Low .. 110,000 M

Initial Dielectric Withstanding Voltage

1. *Design No. 1—Mated—20 Readings*
   Test Voltage .. 750 V AC—All Passed
   Approx. Breakdown Voltage .. 1000 V AC
2. *Design No. 2—Mated—18 Readings*
   Test Voltage.. 1000 V AC—All Passed
   Approx. Breakdown Voltage .. 1500 V AC
3. *Design No. 3—Unmated—45 Readings*
   Test Voltage .. 1500 V AC—All Passed
   Approx. Breakdown Voltage .. 1950 V AC
4. *Design No. 3—Mated—45 Readings*
   Test Voltage .. 1200 V AC—Intermittent breakdown on printed wiring board at two points.
   Approx. Breakdown Voltage .. 1300 V AC

APPENDIX J

Humidity Tests

1. *Design No. 1—Mated—20 Readings*
   Before Test
   High .. 410,000 M
   Low .. 340,000 M
   After Test
   High .. 78,000 M
   Low .. 14,000 M
2. *Design No. 2—Mated—9 Readings*
   Before Test
   High .. 420,000 M
   Low .. 360,000 M
   After Test
   High .. 320,000 M
   Low .. 69,000 M
3. *Design No. 3—Unmated—27 Readings*
   Before Test
   High .. 400,000 M
   Low .. 220,000 M
   After Test
   High .. 450,000 M
   Low .. 8,200 M
4. *Design No. 3—Mated—27 Readings*
   Before Test
   High .. 420,000 M
   Low .. 220,000 M
   After Test
   High .. 280,000 M
   Low .. 8,000 M

APPENDIX K: THERMAL SHOCK

DESIGN NO. 1

	Total mated resistance in ohms during last cycle		
Contact	−55°C	Initial measurements	+85°C
1	0.058	0.060	0.067
2	0.050	0.0595	0.055
3	0.050	0.054	0.0545
4	0.065	0.074	0.0755
5	0.053	0.060	0.0585
6	0.062	0.068	0.0705
7	0.059	0.065	0.0670
8	0.059	0.063	0.0645
9	0.053	0.055	0.0585
10	0.064	0.067	0.0715
11	0.0545	0.058	0.0595
12	0.065	0.069	0.0710
13	0.0605	0.066	0.068
14	0.051	0.058	0.060
15	0.057	0.060	0.0615
16	0.0655	0.072	0.0715
17	0.051	0.054	0.0550
18	0.065	0.069	0.0705
19	0.062	0.064	0.0660
20	0.063	0.066	0.0675
21	0.0525	0.055	0.0560

APPENDIX L: THERMAL SHOCK

DESIGN NO. 2

	Total mated resistance in ohms after test					
	Module 2A			Module 2B		
Contact	−55°C	Initial measurements	+85°C	−55°C	Initial measurements	+85°C
1	Open*	0.085	Open*	0.064	0.062	0.069
2	0.0685	0.069	0.073	0.065	0.071	0.071
3	Open*	0.078	0.081	0.069	0.071	0.074
4	0.0685	0.067	0.0695	0.064	0.067	0.070
5	Open*	0.082	0.0840	0.061	0.064	0.068
6	Open*	0.077	0.0830	0.058	0.061	0.065
7	0.082	0.076	0.0820	0.062	0.064	0.068
8	0.190	0.072	0.0845	0.065	0.066	0.071
9	0.075	0.078	0.083	0.062	0.064	0.068
10	0.077	0.073	0.0725	0.064	0.067	0.069

* Subsequent tests found the opening to be caused by an internal wiring fault; probably a weld.

APPENDIX M: THERMAL SHOCK

DESIGN NO. 3

	Total mated resistance in ohms on last thermal cycle					
	Module 3B		Module 3C		Module 3D	
Contact	−55°C	+85°C	−55°C	+85°C	−55°C	+85°C
1	0.0129	0.0121	0.0153	0.0162	0.0235	0.0206
3	0.0122	0.0128	0.0126	0.0135	0.0111	0.0128
5	0.0119	0.0122	0.0135	0.0145	0.0110	0.0124
7	0.0123	0.0130	0.0145	0.0140	0.0119	0.0126
9	0.0123	0.0128	0.0160	0.0135	0.0120	0.0124
Avg.	0.012	0.013	0.014	0.014	0.014	0.014
2	0.0134	0.0140	0.0126	0.0135	0.0119	0.0136
4	0.0130	0.0138	0.0119	0.0125	0.0121	0.0140
6	0.0130	0.0135	0.0145	0.0146	0.0135	0.0131
8	0.0135	0.0140	0.0127	0.0135	0.0138	0.0140
10	0.0125	0.0132	0.0127	0.0135	Open*	Open*
Avg.	0.013	0.014	0.013	0.014	0.013	0.014

NOTE: Measurements are not given for Module 3A because resistance was measured across a different length of circuit and readings are not comparable.

* Improper alignment of module to the test board caused open.

APPENDIX N: ALTITUDE DIELECTRIC WITHSTANDING VOLTAGE

1. *Design No. 1—Mated—20 Readings*
   Test Voltage .. 200 V AC—All Passed
   Approx. Breakdown Voltage .. 250 V AC
2. *Design No. 2—Mated—18 Readings*
   Test Voltage .. 300 V AC—All Passed
   Approx. Breakdown Voltage .. 350 V AC
3. *Design No. 3—Mated—36 Readings*
   Test Voltage .. 200 V AC—All Passed
   Approx. Breakdown Voltage 280 V AC (printed circuit wiring)

APPENDIX O: CONTACT LIFE

DESIGN NO. 1

	Force-deflection and resistance after test				
Contact	Spring deflection, in.	Max. force, oz	Printed and internal wiring resistance, Ω	Total mated resistance, Ω	Contact* resistance, Ω
1	0.011	12	0.0508	0.0670	0.016
2	0.009	14	0.0404	0.0555	0.015
3	0.013	12	0.0479	0.0550	0.007
4	0.012	14	0.0619	0.0735	0.012
5	0.011	12	0.0428	0.0580	0.015
6	0.012	14	0.0578	0.0685	0.011
7	0.011	16	0.0505	0.0655	0.015
8	0.012	10	0.0518	0.0630	0.011
9	0.011	14	0.0488	0.0575	0.008
10	0.011	12	0.0582	0.0700	0.012
11	0.010	12	0.0430	0.0590	0.016
12	0.011	14	0.0591	0.0695	0.010
13	0.012	16	0.0507	0.0660	0.015
14	0.012	16	0.0487	0.0590	0.010
15	0.011	14	0.0467	0.0615	0.015
16	0.011	14	0.0602	0.0720	0.012
17	0.011	18	0.0401	0.0540	0.014
18	0.013	20	0.0573	0.0690	0.012
19	0.011	14	0.0489	0.0660	0.017
20	0.014	14	0.0560	0.0665	0.011
21	0.013	14	0.0436	0.0565	0.013
High	0.014	20			0.017
Low	0.009	10			0.007
Avg.	0.012	14			0.013

* Contact resistance is the total mated resistance less the printed wiring and internal module resistance.

APPENDIX P: CONTACT LIFE, RESISTANCE MEASUREMENTS

DESIGN NO. 3

	Total mated resistance in ohms after tests			
	Test module number			
Contact	3A	3B	3C	3D
1	0.0126	0.0115	0.0148	0.0129
3	0.0116	0.0120	0.0124	0.0131
5	0.0116	0.0116	0.0134	0.0132
7	0.0123	0.0120	0.0143	0.0136
9	0.0123	0.0116	0.0129	0.0128
High	0.0126	0.0120	0.0148	0.0136
Low	0.0116	0.0115	0.0124	0.0128
Avg.	0.012	0.012	0.014	0.013
2	0.0128	0.0135	0.0126	0.0137
4	0.0133	0.0129	0.0119	0.0145
6	0.0138	0.0127	0.0136	0.0138
8	0.0127	0.0127	0.0127	0.0146
10	0.0128	0.0123	0.0124	0.0138
High	0.0138	0.0135	0.0136	0.0146
Low	0.0127	0.0123	0.0119	0.0137
Avg.	0.013	0.013	0.013	0.014

Odd-numbered contacts (20 readings)—Avg. .. 0.013
Even-numbered contacts (20 readings)—Avg. .. 0.013

APPENDIX Q: CONTACT LIFE, FORCE-DEFLECTION

DESIGN NO. 3

Contact	Module 3A		Module 3B		Module 3C		Module 3D	
	Spring deflection, in.	Max. force, oz	Spring deflection, in.	Max. force, oz	Spring deflection, in.	Max. force, oz	Spring deflection, in.	Max. force, oz
1	0.023	14	0.022	16	0.025	18	0.021	12
2	0.025	16	0.027	18	0.016	12	0.026	16
3	0.020	14	0.026	18	0.026	18	0.026	16
4	0.027	18	0.027	20	0.019	14	0.026	16
5	0.026	18	0.026	18	0.026	18	0.025	16
6	0.027	18	0.025	18	0.026	18	0.026	16
7	0.026	18	0.027	20	0.024	18	0.028	18
8	0.026	16	0.024	16	0.020	14	0.026	16
9	0.024	16	0.025	16	0.026	16	0.025	16
10	0.023	16	0.021	14	0.013	8	0.019	14
High	0.027	18	0.027	20	0.026	18	0.028	18
Low	0.020	14	0.021	14	0.013	8	0.019	12
Avg.	0.025	16.4	0.025	17.4	0.022	15.4	0.025	15.6

Spring deflection (40 readings)—High .. 0.028
Low .. 0.013
Avg. .. 0.024

Maximum force (40 readings)—High .. 20
Low .. 8
Avg. .. 16.2

APPENDIX R: VIBRATION TESTS

The vibration input to the vibration test fixture in each axis for every module tested was 0.06-in. double-amplitude displacement, 5 to 56 cps and 10 *g*'s, 50 to 2000 cps. Total cycling time was 30 min for 5 cps to 2000 cps to 5 cps. There was an additional 10-min dwell at each major resonance point for each axis. No contact openings or failures occurred in the initial cycling. The only openings or failures at resonance are noted for Module 1A and Module 3C.

Resonant Vibration Levels on Module 1A

Direction of vibration	1st		2nd		3rd		4th	
	g's	cps	*g*'s	cps	*g*'s	cps	*g*'s	cps
Across contacts	38	498	49.5	576	45	809	40	844
Along contacts	93 (1)	559	41	631	60	852	35.5	1452
Normal to contacts	198 (2)	468	103	622	123	640	117	664

(1) Contact No. 1 opened after 4 min.
(2) Contact No. 1, 2, and 13 opened after 2 min.

Resonant Vibration Levels on Module 2A

Direction of vibration	1st		2nd		3rd		4th	
	g's	cps	*g*'s	cps	*g*'s	cps	*g*'s	cps
Across contacts	49.5	498	43	517	71	533	120	576
Along contacts	131	520	63	562				
Normal to contacts	104	436	52	616	62	634	93	664

Resonant Vibration Levels on Module 2B

Direction of vibration	1st		2nd		3rd	
	g's	cps	*g*'s	cps	*g*'s	cps
Across contacts	82	376	18.7	479		
Along contacts	52	409	16.8	480		
Normal to contacts	181	610	69	638	59	767

Resonant Vibration Levels on Module 3A

Direction of vibration	1st		2nd		3rd	
	g's	cps	g's	cps	g's	cps
Across contacts	22.5	550	53	750		
Along contacts	59	590	23.5	725		
Normal to contacts	79	498	385	533	296	566

Resonant Vibration Levels on Module 3B

Direction of vibration	1st		2nd		3rd	
	g's	cps	g's	cps	g's	cps
Across contacts	57.5	534	122	578	504	605
Along contacts	290	517	280	566		
Normal to contacts	595	545	14	1242	43.5	1557

Resonant Vibration Levels on Module 3C(1)

Direction of vibration	1st		2nd		3rd	
	g's	cps	g's	cps	g's	cps
Across contacts	39	755	215	844	24	1275
Along contacts	54.5	482	128	746		
Normal to contacts	590	602	49.5	749	45.5	1591

(1) When module was removed at end of test, contact No. 4 was found broken.

Resonant Vibration Levels on Module 3D

Direction of vibration	1st		2nd		3rd	
	g's	cps	g's	cps	g's	cps
Across contacts	45	794	16	1275		
Along contacts	60	723				
Normal to contacts	217	509	287	545	35.5	1247

Resonant Vibration Levels on Module 3E

Direction of vibration	1st		2nd		3rd	
	g's	cps	g's	cps	g's	cps
Across contacts	50	740				
Along contacts	60	708				
Normal to contacts	435	615	43.5	723	36.5	1577

APPENDIX S: SPECIAL VIBRATION TESTS

Module No. 3E: (Direction of vibration normal to the test board)

1. Vibrated at resonant frequency of 615 cps for 5 min with no contact openings.

Input Level	*Module Level*
10 *g*	435 *g*
70 *g*	2825 *g* (Estimated)*

* Based on a Q of 43.5 at 10 *g* level.

2. Vibrated at resonant frequency with module mounting screws loosened (5 min). Opening occurred at the 70 *g* level.
3. Vibrated at resonant frequency of 962 cps for 30 min with printed wiring board mounted on rubber pad flat against the vibration test fixture.

Input Level	*Module Level*
70 *g*	415 *g*

No openings occurred.

When connector was removed, five contact springs were found broken. The mounting post had become loose in the printed wiring board and was replaced.

Module No. 3A: (Direction of vibration normal to test board)

1. Vibrated at resonant frequency of 574 cps for 5 min with no contact openings.

Input Level	*Module Level*
30 *g*	515 *g*
40 *g*	572 *g*
50 *g*	700 *g* (Estimated)*

* Based on a Q of 14 at 40 *g* level.

2. Printed wiring board mounted on a rubber pad flat against the vibration fixture. Vibrated at the highest resonant frequency for 30 min with no contact openings.

Frequency	*Input Level*	*Module Level*
934 cps	30 *g*	217 *g*
921 cps	30 *g*	237 *g*
917 cps	30 *g*	247 *g*
895 cps	30 *g*	287 *g**

* One mounting post fractured at the point of entry into the printed wiring board in the last few minutes of the tests, but the contacts did not open.

APPENDIX T: SPECIAL CONTACT LIFE TESTS

MODULE CONNECTOR NO. 3A

	13,500 cycles			34,500 cycles			45,000 cycles		
Contact	Spring flexure, in.	Max. force, oz	Total mated resistance, Ω	Spring flexure, in.	Max. force, oz	Total mated resistance, Ω	Spring flexure, in.	Max. force, oz	Total mated resistance, Ω
1	0.024	16	0.0134	0.023	16	0.0131	0.023	14	0.0130
2	0.025	18	0.0133	0.024	16	0.0138	0.024	14	0.0136
3	0.018	12	0.0125	0.019	12	0.0138	0.018	12	0.0120
4	0.024	16	0.0141	0.024	16	0.0138	0.024	16	0.0137
5	0.023	16	0.0120	0.024	14	0.0128	0.023	14	0.0123
6	0.024	16	0.0140	0.025	16	0.0140	0.024	14	0.0138
7	0.024	16	0.0132	0.025	16	0.0132	0.022	12	0.0129
8	0.023	14	0.0134	0.025	14	0.0136	0.023	14	0.0130
9	0.020	14	0.0128	0.022	14	0.0129	0.023	14	0.0128
10	0.021	14	0.0130	0.023	14	0.0133	0.024	14	0.0130
Avg.	0.023	15		0.023	15		0.023	14	
	Avg. resistance: Odd-numbered contacts—0.013 Even-numbered contacts—0.014			*Avg. resistance:* Odd-numbered contacts—0.013 Even-numbered contacts—0.014			*Avg. resistance:* Odd-numbered contacts—0.013 Even-numbered contacts—0.013		

8073

Packaging Flyable Welded Miniaturized Computer Electronics

W. McMorran, D. Grassi, and B. Edgerton
Missile and Space Division, Raytheon Company, Sudbury, Massachusetts

Starting with the present welded missile logic and analog equipment now in production, this paper traces the problems encountered in attempting to miniaturize these packages, while still maintaining the high reliability necessary for military and space-probe systems. Specific examples are cited to show how initial design decisions were implemented into firm configurations, using varied welding and plastics techniques with both integrated and discrete components, in the light of the end use of the product as well as the production skills and tools available.

INTRODUCTION

The continual demand by military and space-probe planners for smaller and lighter guidance and navigation equipment forces both electrical and mechanical engineers to constantly upgrade their capabilities as new techniques and components become available. This pressure toward miniaturization is often in direct conflict with the parallel goals of high reliability, low cost, and ease of fabrication and maintenance. This article briefly describes some of the progress and problems encountered in miniaturizing welded aerospace-computer circuits that are functionally similar to those now in production.

Initially, the decision was made to remain primarily with welded fabrication techniques. This was based both upon the preferences of our customers as well as our operation's reputation and capability for highly controlled welding processes. The services of key production, industrial engineering, and various consultant groups throughout the operation were employed from the beginning during the evolution of new design prototypes. This was done so that these groups would be familiar with the resultant designs, techniques, and engineering knowledge. This familiarity greatly simplifies the transition into full production. The basic aim is to explore a variety of packaging techniques that may be applicable to our specialized products so that the knowledge is on hand to select the most favorable one for producing any particular equipment in light of such requirements as scheduling, cost, density, and reliability.

INTEGRATED DIGITAL EQUIPMENT

The primary means of successfully miniaturizing digital logic has been through the use of integrated circuitry. A size reduction of approximately 70%, including both fixed and removable interconnections, is readily possible using Micrologic in TO-47 cans instead of conventional welded packaging using discrete components of $\frac{1}{4}$-W resistor size. This is illustrated by comparing discrete-component logic sticks to integrated-circuit logic sticks (see Fig. 1). The discrete-component logic stick provides for 66 three-input NOR gates. The integrated-circuit logic stick accommodates 120 Fairchild Micrologic three-input NOR gates (see Fig. 2). Both of the computer designs were evolved by the MIT Instrumentation Laboratory in conjunction with Raytheon Company at Sudbury, Massachusetts.

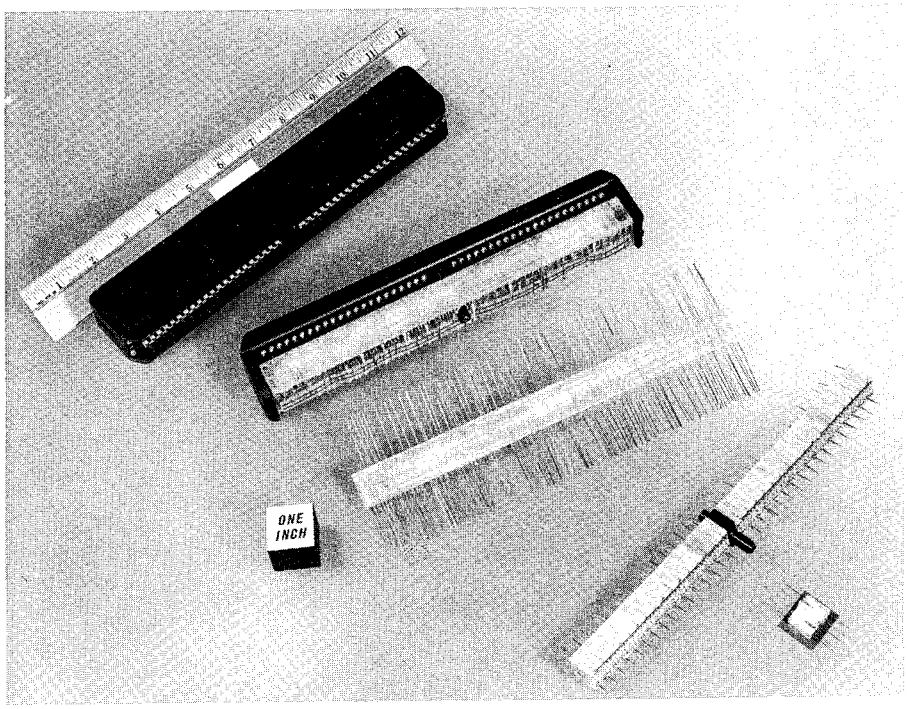


Fig. 1. Welded logic stick using discrete components.

Recent work on digital circuitry has been concentrated around the use of smaller flat rectangular integrated logic such as that shown in Fig. 3. This is now becoming available from several component manufacturers. Unfortunately, there is yet no standardization of case sizes. This is illustrated in Fig. 4. However, most manufacturers have standardized five 0.003-in.-diameter gold-plated Kovar leads per side on 0.050-in. centers so that packaging schemes can be evolved that permit intermixing different manufacturers' logic elements. Intermixing is important on programs requiring second source procurement and also because of the seemingly perverse nature of electrical engineers to submit drastic component changes just prior to final fabrication of prototype equipment.

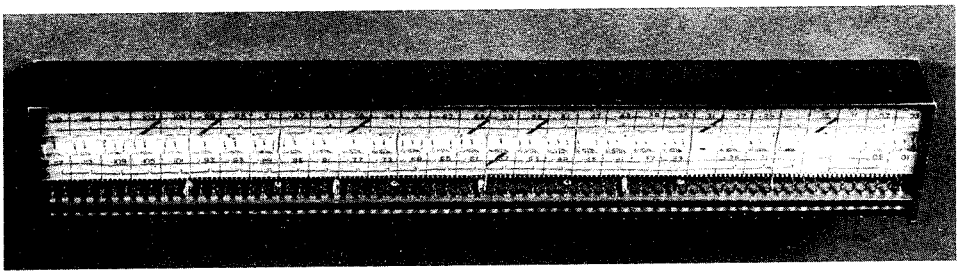


Fig. 2. Unpotted guidance computer stick with 120 TO-47 NOR gates.

The Texas Instruments integrated logic element illustrated in Fig. 3 is a dual three-input NOR gate. Integrated logic elements are also available as single six-input NOR gates or triggered flip-flops with some options for emitter follower outputs for higher fan-out capability. Other manufacturers, such as Westinghouse, Signetics, and Fairchild, now make a similar variety of solid circuits for NAND, OR, and AND logic.

SOLID CIRCUIT* **TYPE SN 514**

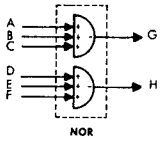
DIFFUSED SILICON "NOR" OR "NAND" LOGIC NETWORK

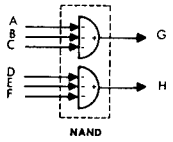
A SERIES 51 MICROELECTRONIC DUAL "NOR" OR "NAND" GATE

for application in

• Digital Computer Systems • Data Handling Systems • Control Systems

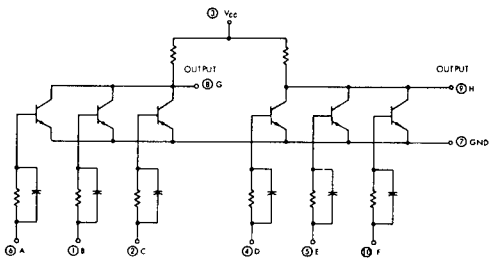
logic diagram





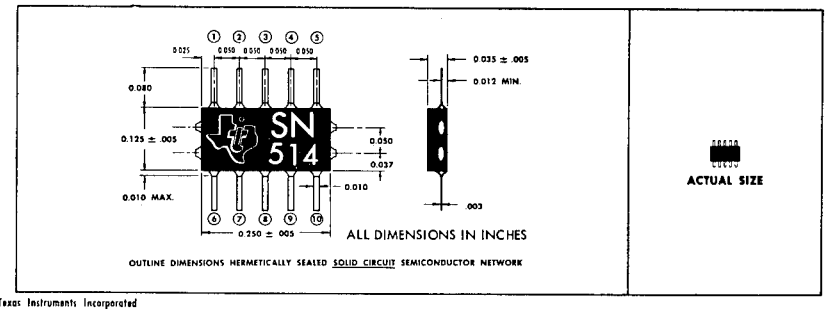
Logic		
	NAND	NOR
G	$\overline{ABC}$	$\overline{A+B+C}$
H	$\overline{DEF}$	$\overline{D+E+F}$

circuit diagram



mechanical data

Solid Circuit semiconductor networks are mounted in a glass-to-metal hermetically sealed package. Leads are gold-plated Kovar. Weight: 0.1 gram.



*Trademark of Texas Instruments Incorporated

COMPONENTS DIVISION
CAPACITORS DIODES
RECTIFIERS RESISTORS
SEMICONDUCTOR NETWORKS
SILICON CONTROLLED RECTIFIERS

TEXAS INSTRUMENTS
INCORPORATED
13500 N. CENTRAL EXPRESSWAY
P. O. BOX 5012 • DALLAS 22, TEXAS

Fig. 3. Texas Instruments Bulletin No. DL-S 622844.

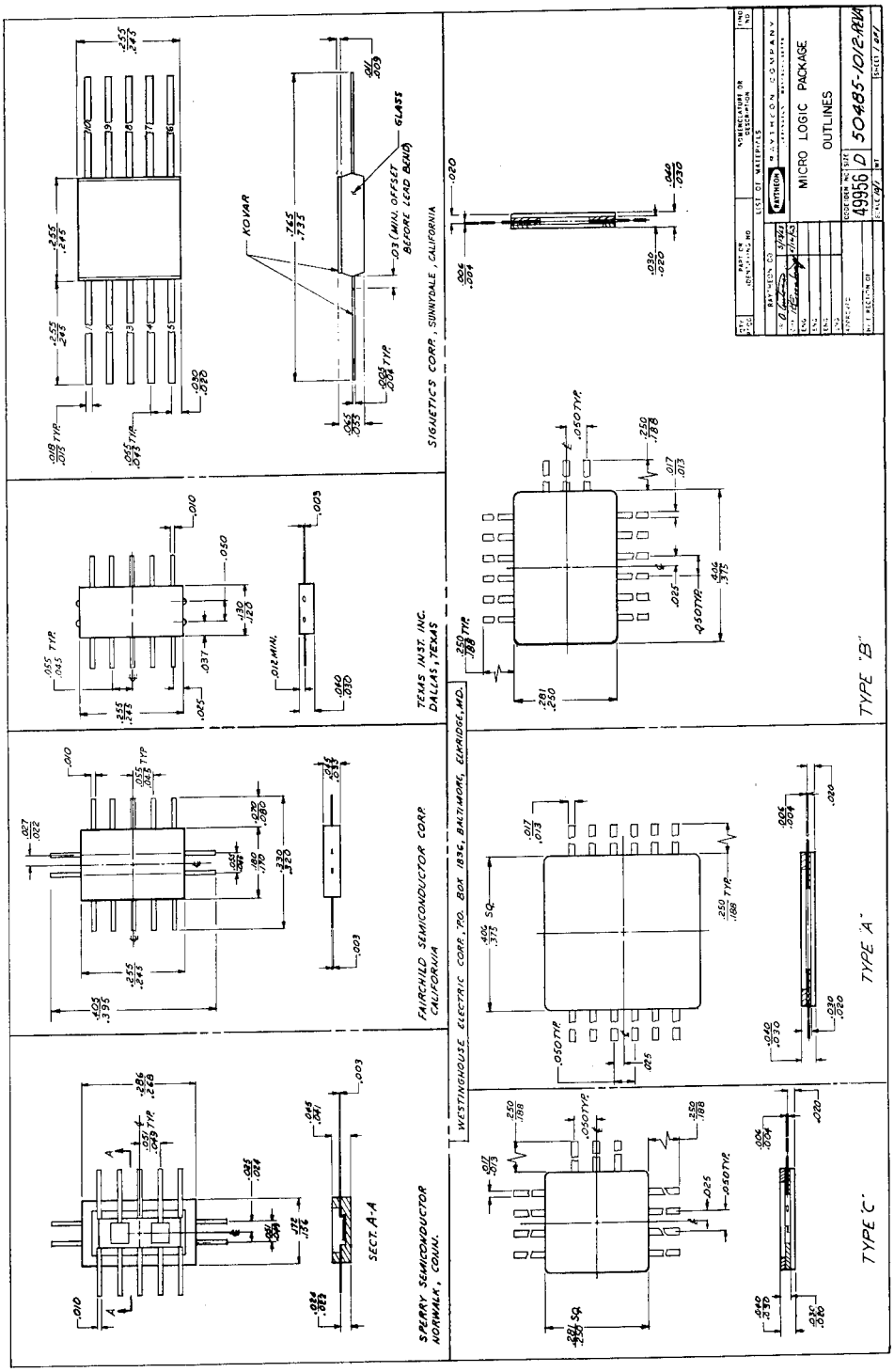


Fig. 4. Integrated logic package outlines.

TABLE I

Texas Instruments Environmental Data

Integrated semiconductor networks environmental data		
Sinusoidal vibration	100–2000 cps 50 *g*	All tests as per MIT-S-19500B
Vibration fatigue	60 cps 50 *g*	
Shock	3500 *g* 0.5 msec	
Acceleration	30,000 *g*	
Thermal shock	0 to 100°C	Data as per Texas Instruments Reliability Report (1962)
Salt atmosphere	24 hr	
Temperature	55°C to +125°C	

Integrated semiconductor networks heat transfer survey	
Maximum ambient temperature for Series 51 network combined with worst cond. input voltage applied (T_A = 125°C, C_{cc} = 6 V, V_{on} = 0.30 V max)	125°C
Heat dissipation assume 16 mW per network (based on 2 gates per SN514 network)	0.016 W (approx. 3 : 1 safety factor)
Module Stick use figure of maximum 42 networks	0.67 W

The Texas Instruments NOR-logic gate and R-S flip-flops are fabricated by interconnecting two NOR gates. Some 90% of logic circuits in some of our applications consist of these elements. Table I presents some indication of the environmental and heat transfer data of these modules.

One of the early packaging problems is to determine how many elements should be packaged together as an assembly. This is based on many factors such as logic functional breakdown, component cost per repairable or throw-away package, customer's requirements, or interconnection complexity.

With the logic for one computer which comprises 528 gates as an example, a study was made to determine the optimum number of integrated logic elements to be packaged together. A resultant graph shown on Fig. 5 plots the number of Texas Instruments units *vs.* the number of external leads per assembly that would be required. Using integrated logic, it appears reasonable to use packages which provide room for up to 42 Texas Instruments elements and 84 external leads. This allows a minimum of eight spare pins for each package. Naturally, a unique graph will evolve for any particular logic flow being considered.

Two major types of packaging are presently being evaluated. In the first example, conventional resistance welding with wire matrices is being used. In the second example, either parallel-gap welding with wire matrices or parallel-gap welding onto plated, etched, or solid circuitry is used.

Examples of the first type are shown in Figs. 6 and 7. The main advantage of this construction is that it requires only a single-layer matrix on each horizontal deck constructed on Lexan or Mylar insulator and 0.010-in.-diameter nickel wire. All spacing is on 0.050-in. centers so that all horizontal welding is easily adapted to semiautomatic or fully automatic welding.

No problems are encountered in welding the 0.003 in. by 0.010 in. gold-plated Kovar module leads to the nickel wire other than keeping the leads from being bent in handling. All matrices pass simple nondestructive continuity and pull tests. All of the vertical welding between decks can be completed by a production floor worker in less than two hours.

External connections can be made with hand wire wrapping on 0.100 in. centers or by wire wrapping to modified Amphenol Intercon tabs on printed circuit boards without the

wire between tabs as shown in Fig. 6. The latter method would provide the advantage that the logic stick would be removable by cutting the wrapped wire only. This method would be a more suitable system for low production R & D space-probe equipment than for a high-volume military field-employed system where rapid stick replacement is a necessity. A third solution would be to again build an all-welded computer. This too is perhaps most applicable for low-volume, flyable, space-probe equipment where entire backup computers would be readily available for quick substitution.

The Malco wire-wrap connector on 0.010 in. centers is presently being used for all of our miniaturized modules (see Figs. 8 and 9). This connector was chosen primarily because of basic simplicity and reliability. However, a comparison of the volume of active electrical

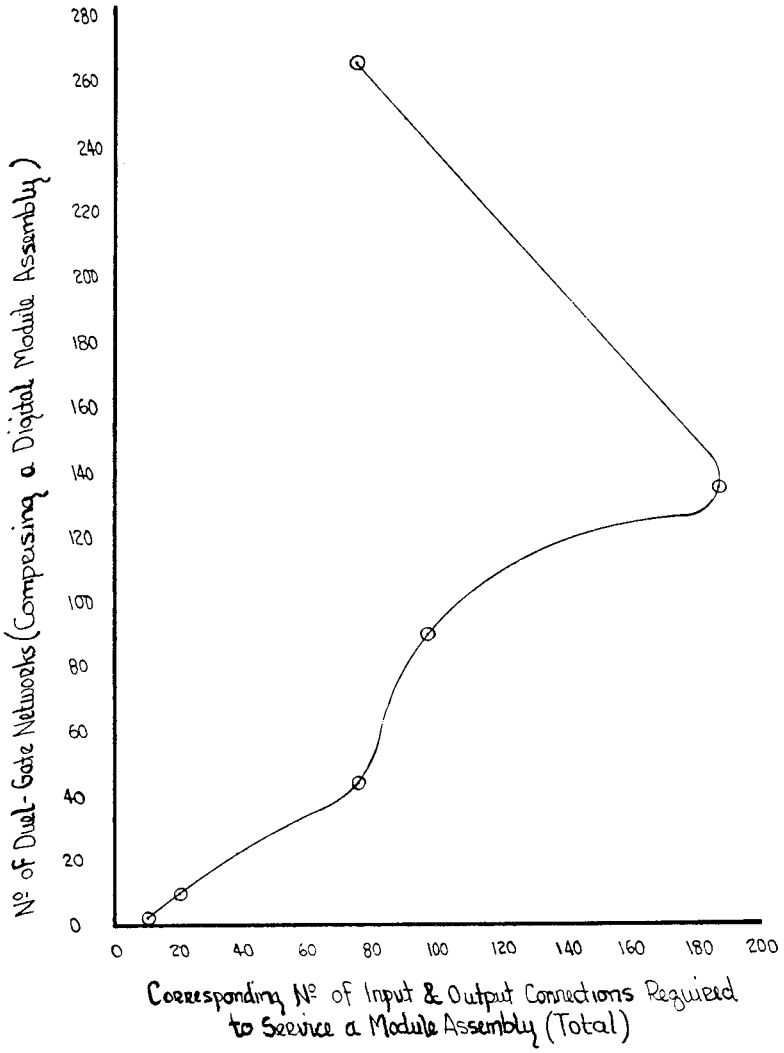


Fig. 5. Graph of required number of external loads *vs.* number of integrated logic elements packaged.

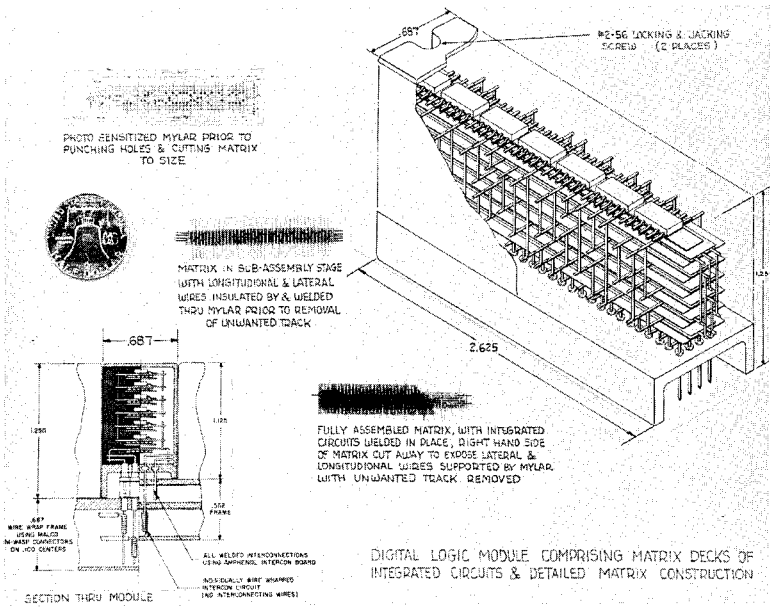


Fig. 6. Digital fabrication procedures using horizontally decked wire matrices.

components packaged *vs.* the total volume required for interconnections shows that a tremendous volume savings could be further obtained if a reliable rugged connector on 0.050 in. centers were available.

On the negative side, it would be necessary to completely cut all of the vertical wiring around at one level to expose and replace an element for repairs on the stacked-horizontal

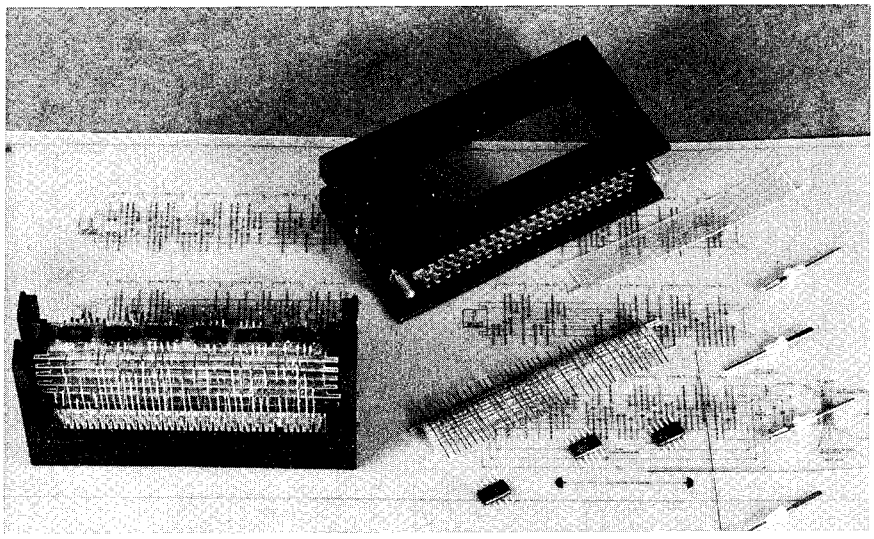


Fig. 7. Digital logic assembly with horizontal wire-matrix subassemblies.

MALCO MINI-WASP MICROMINIATURE COMPONENTS

A Development Program

THE PRESENT TREND TOWARD DENSER AND LESS SPACE CONSUMING PACKAGING CONCEPTS HAS BROUGHT ABOUT OUR DEVELOPMENT OF "**MINI-WASP**." THIS SYSTEM IS APPROXIMATELY A ONE-HALF SIZE VERSION OF THE HIGHLY SUCCESSFUL "**WASP**" SYSTEM.

USING WRAPOSTS WITH .025" SQUARE BY ½" LONG EFFECTIVE WRAP AREA THESE PLATES AND COMPONENTS UTILIZE THE ALUMINUM MATRIX METHOD OF REGISTERING CONTACTS FOR THE HIGHEST ELECTRICAL RELIABILITY AND EASE OF MACHINE WIRING.

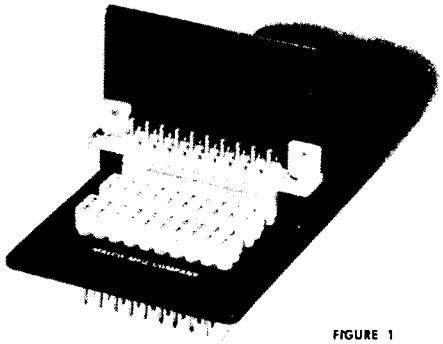
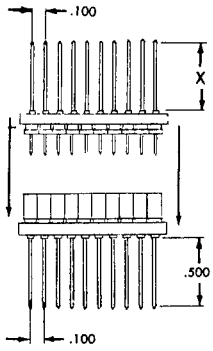


FIGURE 1

THE LENGTH "X" IN FIGURE 2 CAN BE INCREASED TO ALLOW THREE LEVELS OF RIGHT ANGLE BENDS FOR **P. C. BOARD** CONNECTIONS OR DECREASED FOR WELDING OR SOLDERING OF COMPONENTS.

WRAPOST PLATES CAN HAVE GROUPS OF CONTACTS LOCATED ON A CONSTANT GRID TO SUIT CIRCUITRY REQUIREMENTS. RECEPTACLE CONTACTS ARE PRODUCED IN HEAT-TREATED BERYLLIUM COPPER.

MATING BLADES WILL BE AVAILABLE IN ONE-HALF HARD BRASS.



MALE

FIGURE 2

FEMALE

FIGURE 3

Miniature Grid Systems Proposed

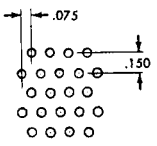


FIGURE 4

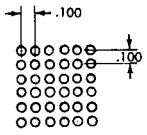


FIGURE 5

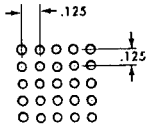


FIGURE 6

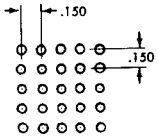


FIGURE 7

THE ABOVE GRID SYSTEMS HAVE BEEN PROPOSED FOR CONSIDERATION. THE .075" X .150" PATTERN WILL ALLOW DIAGONAL WIRING IN AUTOMATIC PRODUCTION. THIS IS A REQUIREMENT OF HIGH SPEED COMPUTERS WHERE WIRE ROUTING MUST BE THE SHORTEST POSSIBLE POINT-TO-POINT. THE OTHER SYSTEMS SHOWN INCREASE WIRE DENSITY AND MINIMIZE PANEL AREA.

Fig. 8. Malco Manufacturing Company Bulletin 621.

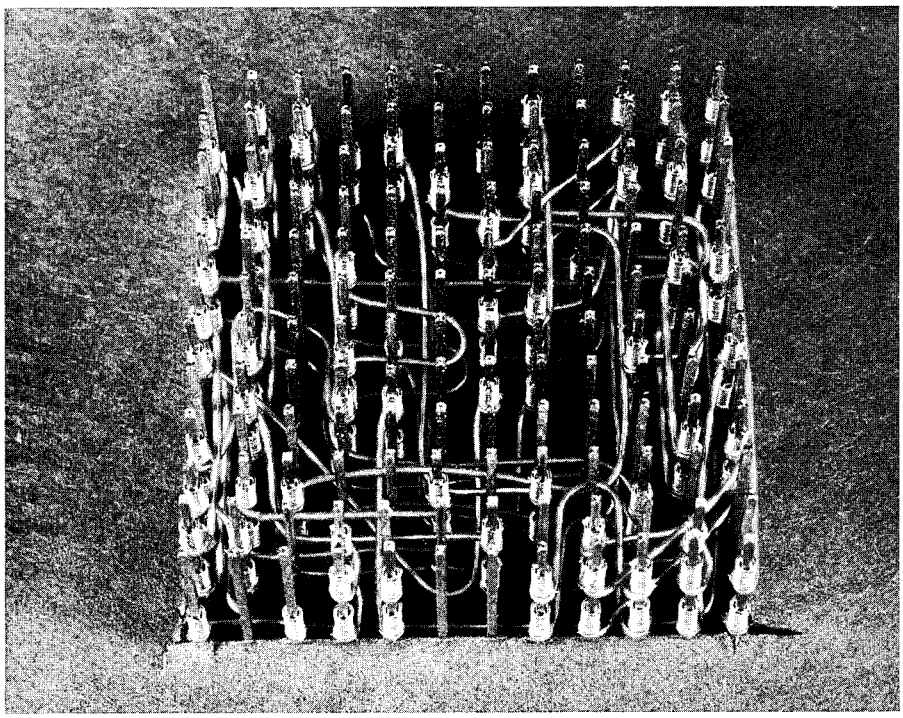


Fig. 9. Wire wrap interconnections between Malco Miniwrap connectors.

deck-type modules. However, it is assumed that each deck would be fully tested electrically prior to vertical assembly. The extended horizontal wires provide room for at least three repair welds on each wire. Our experience shows that there are very few electrical failures caused by the subsequent potting operations.

Figure 10 shows an alternative vertical configuration aimed at further volume reduction. This configuration leaves all elements exposed for ease of repairs or logic module replacement.

While the first models of this configuration have wire matrices, present plans call for it to also serve as the study model for further investigation of solid-plated multilayer matrices. An example of a plated matrix is shown on Fig. 12. The primary advantage of a plated matrix is that it is theoretically a multilayered circuit in which each electrical path becomes a solid homogeneous column of metal. This advantage is opposed to a conventional multilayered printed circuit which obtains final electrical continuity by plating-through holes after completing the individual etched circuits. To date, the results from reliability tests on matrices constructed by plating have been somewhat disappointing in that intermittents between plated layers have developed during environmental tests (see Fig. 12). However, plating vendors are continuing to make improvements so that hopefully a reliable product will become obtainable in the near future.

Parallel-gap welding (sometimes referred to as single or double point welding) would be the ideal welding process for use with plated matrices. Instead of welding from both sides as in conventional resistance welding, both electrodes approach from the same side on a movable arm. This technique was investigated by Raytheon's Industrial Component Division some ten years ago, but it has only recently come into widespread industrial use. Present production welders are easily modified for parallel gap welding.

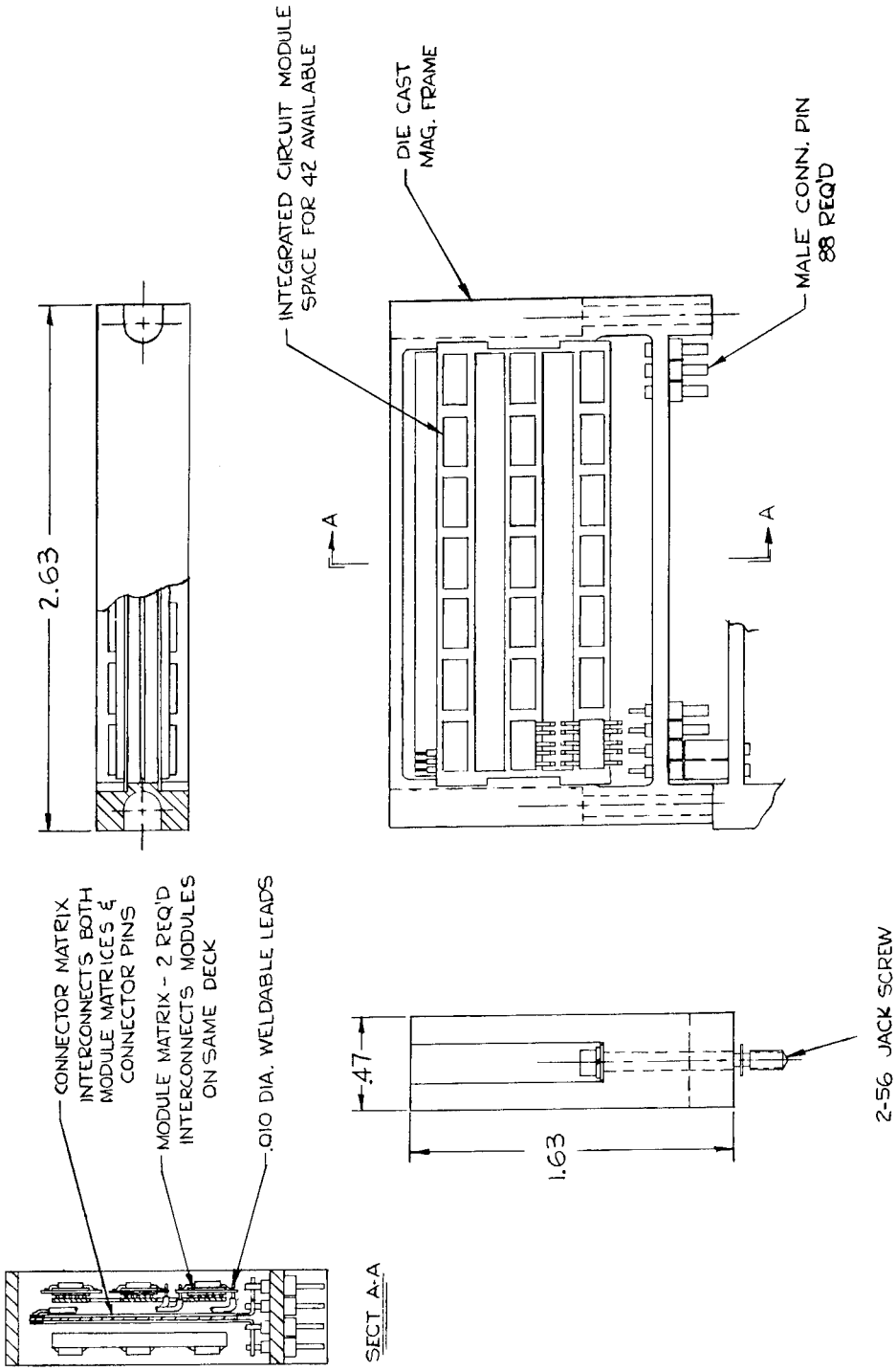


Fig. 10. Digital logic assembly with vertical matrix construction.

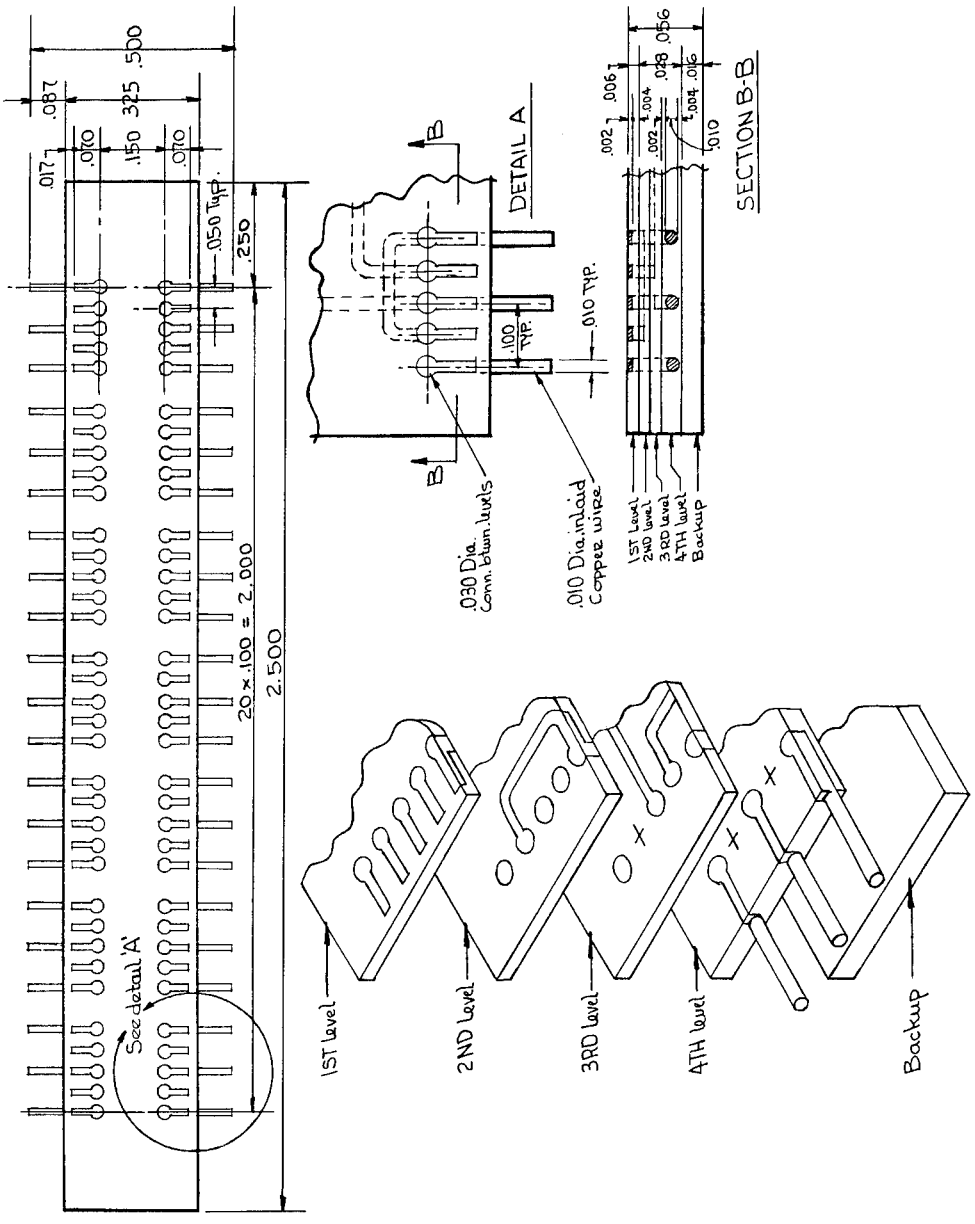


Fig. 11. Multilayer plated matrix.

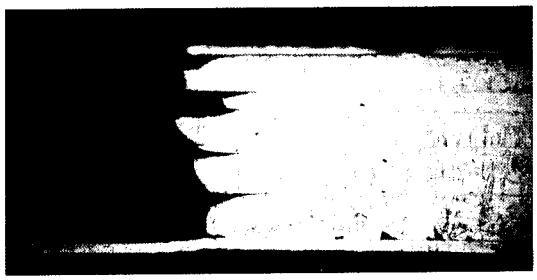


Fig. 12. Microscopic cross section of a plated multiple-layer matrix board (enlarged 35 times).

An example of parallel gap welding with modified conventional welding equipment is shown on Fig. 14. Note that both electrodes are on the top movable arm and are separated by a thin insulator.

A comparison of the advantages of welding wire matrices with other alternatives such as plated construction, etched circuitry, or weldable heavy vapor depositing shows wire's primary advantages. Wire is made by being pulled through an extruding die to very close tolerances. If there is any question as to its outside diameter, it can be measured simply. All of the alternatives require destructive testing to actually measure the thickness of the deposited or etched

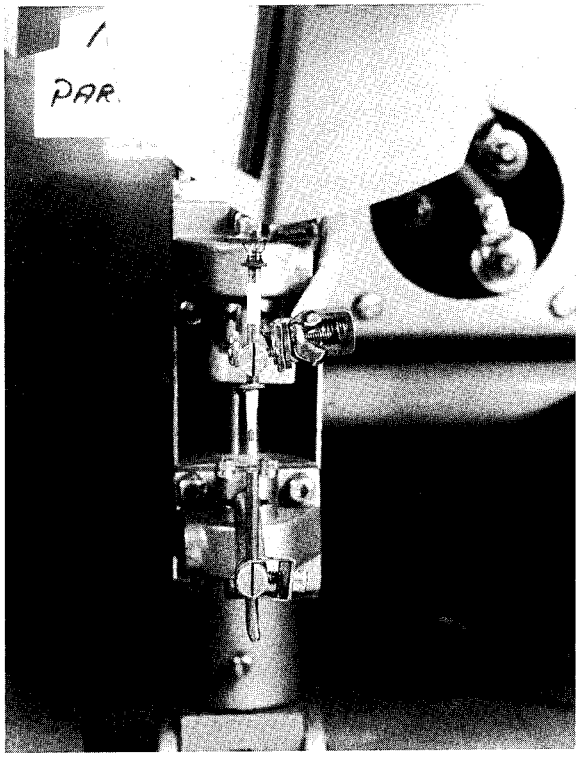


Fig. 13. Conventional welding equipment modified for parallel-gap welding.

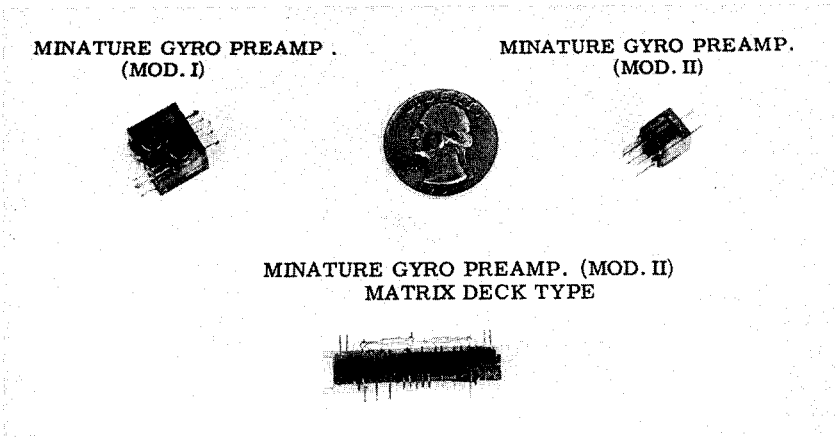


Fig. 14. Three successive versions of 4800-CPS gimbal output amplifier.

leads. The cross section of a parallel-gap weld becomes critical because it depends upon the same heat dissipation or I^2R simultaneously being developed in both the element lead and the plated or etched matrix lead during the welding cycle.

On the other hand, wire matrices require more welding than any of the alternatives. Also, successful solid matrices exposed along any desired vertical or horizontal surface will permit much more freedom in choosing packaging configurations and should result in greater packaging densities.

Table II shows the total relative volumetric saving in the use of both round transistor can Micrologic and flat package integrated logic including male and female connectors. Micrologic packaging in round cans (TO-47 size) reduces sizes approximately 70% over welded discrete components. With flat rectangular integrated logic, a volumetric reduction of 90% is readily possible.

TABLE II

Digital Packaging Size-Weight Comparison

Unit	Volumetric comparison to Polaris	Logic stick size, in.	Volume, in.^{3}	Equivalent number of discrete components	Component density, components per ft^3	Volume required per gate, in.^{3}/gate
Type Polaris Mark II single digital logic module (contains 66 gates)	100% base	10.0 × 1.0 × 1.5	15.00	484	56,000	0.55
Apollo Type 120 TO-47 NOR gate digital logic module	30%	9.1 × 0.8 × 1.3	9.49	1,000	182,000	0.17
Typ. Adv. Pkg. Polaris Equi. single digital logic module (contains 42 dual-gates)	9%	2.6 × 0.6 × 1.4	2.18	718	570,000	0.06

At present, Micrologic elements in cans are less expensive than flat integrated logic, even considering they may contain only one half as much logic. Since the leads are easier to handle (0.017 in. diameter *vs.* 0.003 × 0.010 in. flat), there is no question that module fabrication can be packaged so that it is easier to assemble by less sophisticated techniques when the absolute minimum package size is not important.

However, all present predictions by military planners and the vendors themselves is that the use of integrated logic in flat rectangular packages will shortly surpass that of both TO-5 and TO-47 with competitive pricing.

DISCRETE AND HYBRID CIRCUITS

Since there will always be circuits that do not lend themselves to thin-film integrated techniques, means must be found for packaging small discrete component stages and mixing discrete components into hybrid stages with integrated modules. This must be done without losing a significant portion of the volume savings gained through the use of the integrated logic. In digital equipment, this consideration becomes necessary for the power supply and clock oscillator and interface circuits to the associated analog and exterior equipment.

For low-level power stages, the packaging can sometimes be handled the same as the wire matrices system used in the digital equipment. Figure 14 shows three successive versions of miniaturizing a gimbal output amplifier.

The last version uses two dual transistors, available in integrated logic cases, and twelve fixed-value discrete components prepackaged in groups of four. These are welded directly onto the wire matrix. The two longitudinal resistors are nominal values soldered on after their required value has been determined. The fixed-value component groups can also be obtained on thin-film deposited chips in hermetically sealed integrated logic cases when production

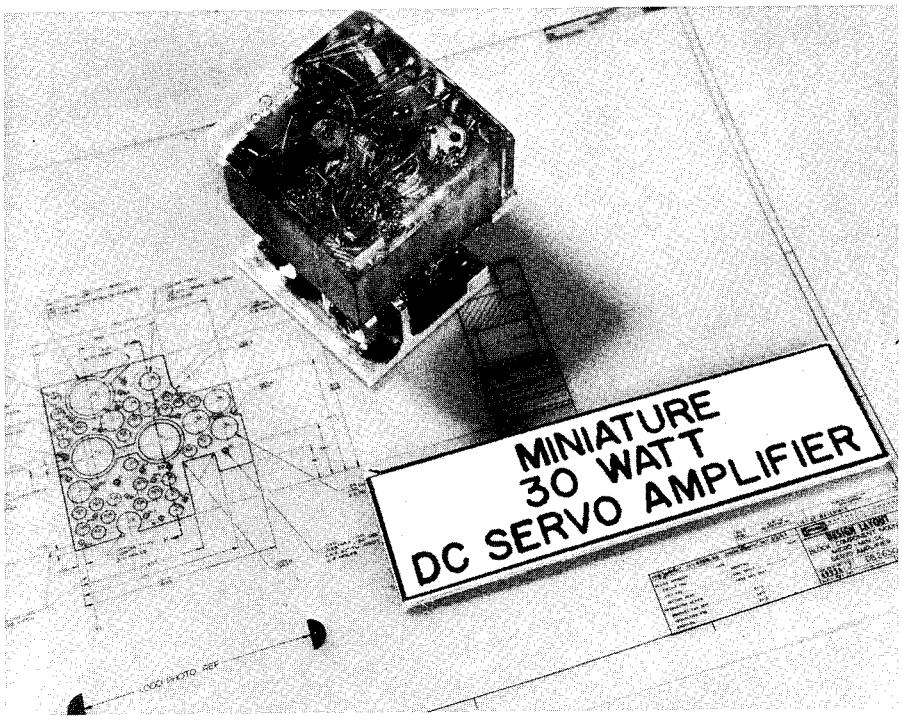


Fig. 15. 30-W DC servo amplifier.

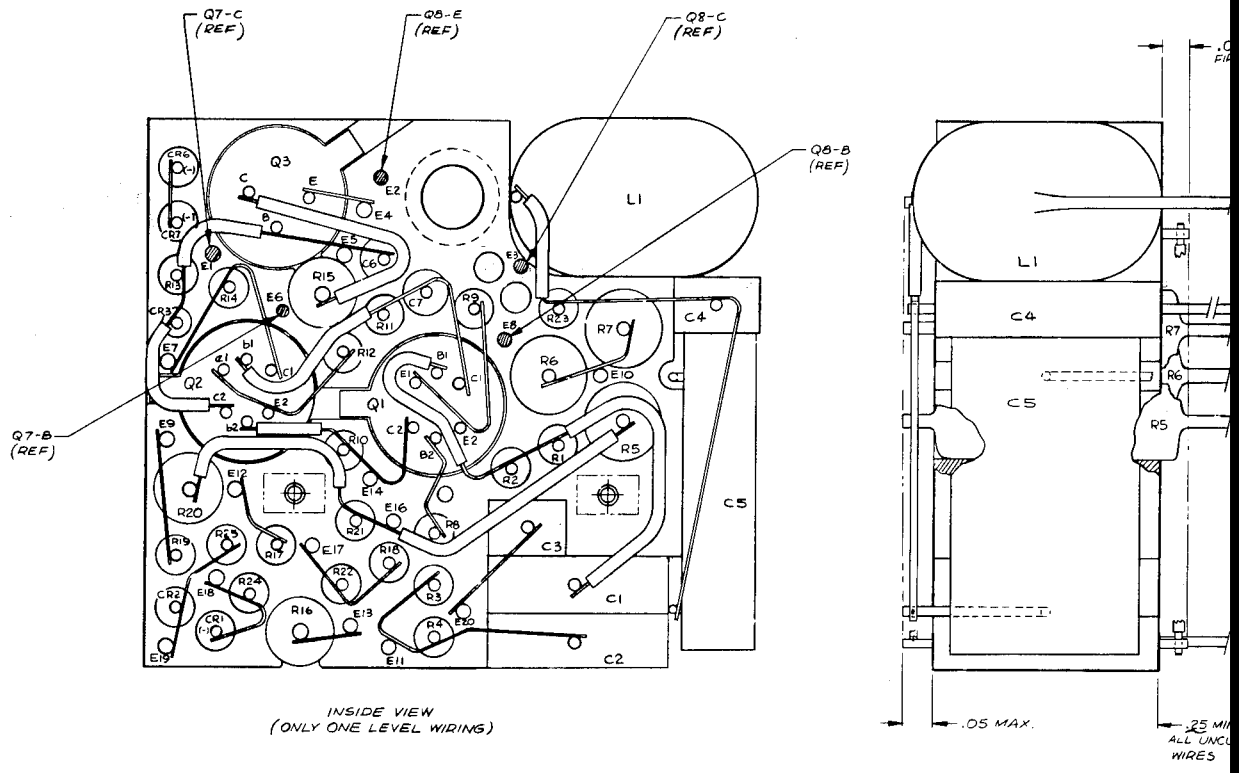
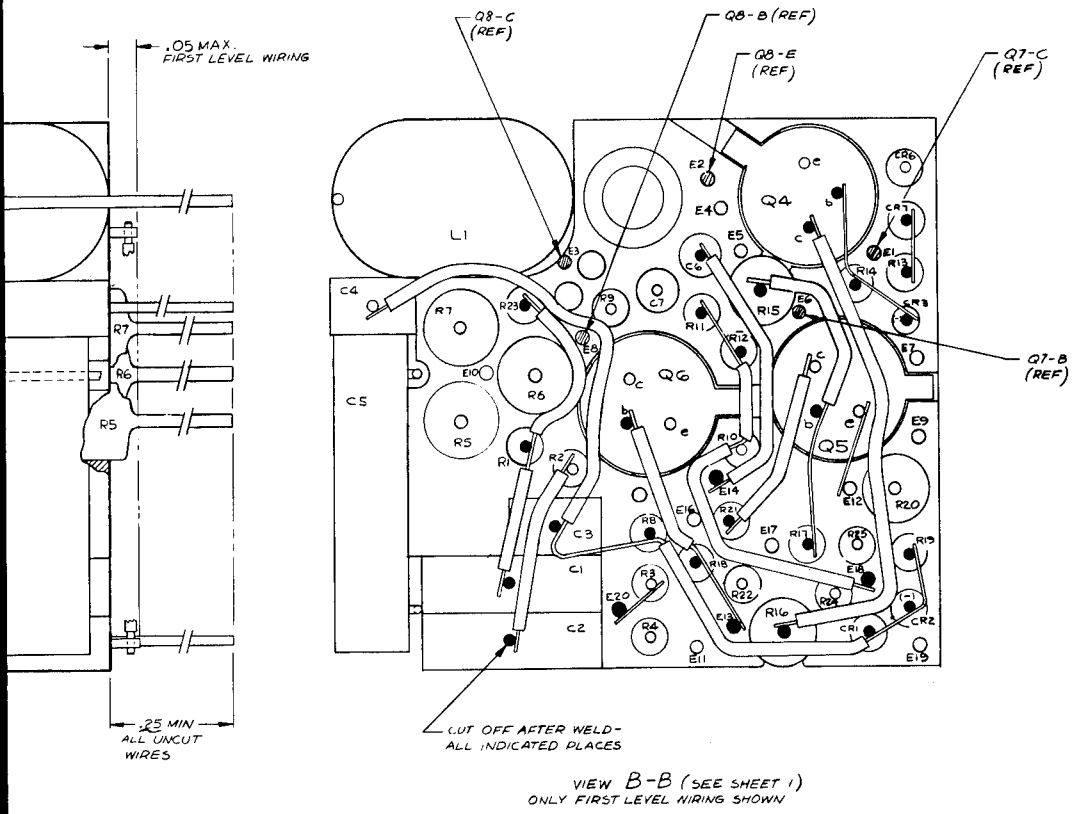


Fig. 17. Servo amplifier assembly, She



VIEW B-B (SEE SHEET 1)
ONLY FIRST LEVEL WIRING SHOWN

plifier assembly, Sheet 2.

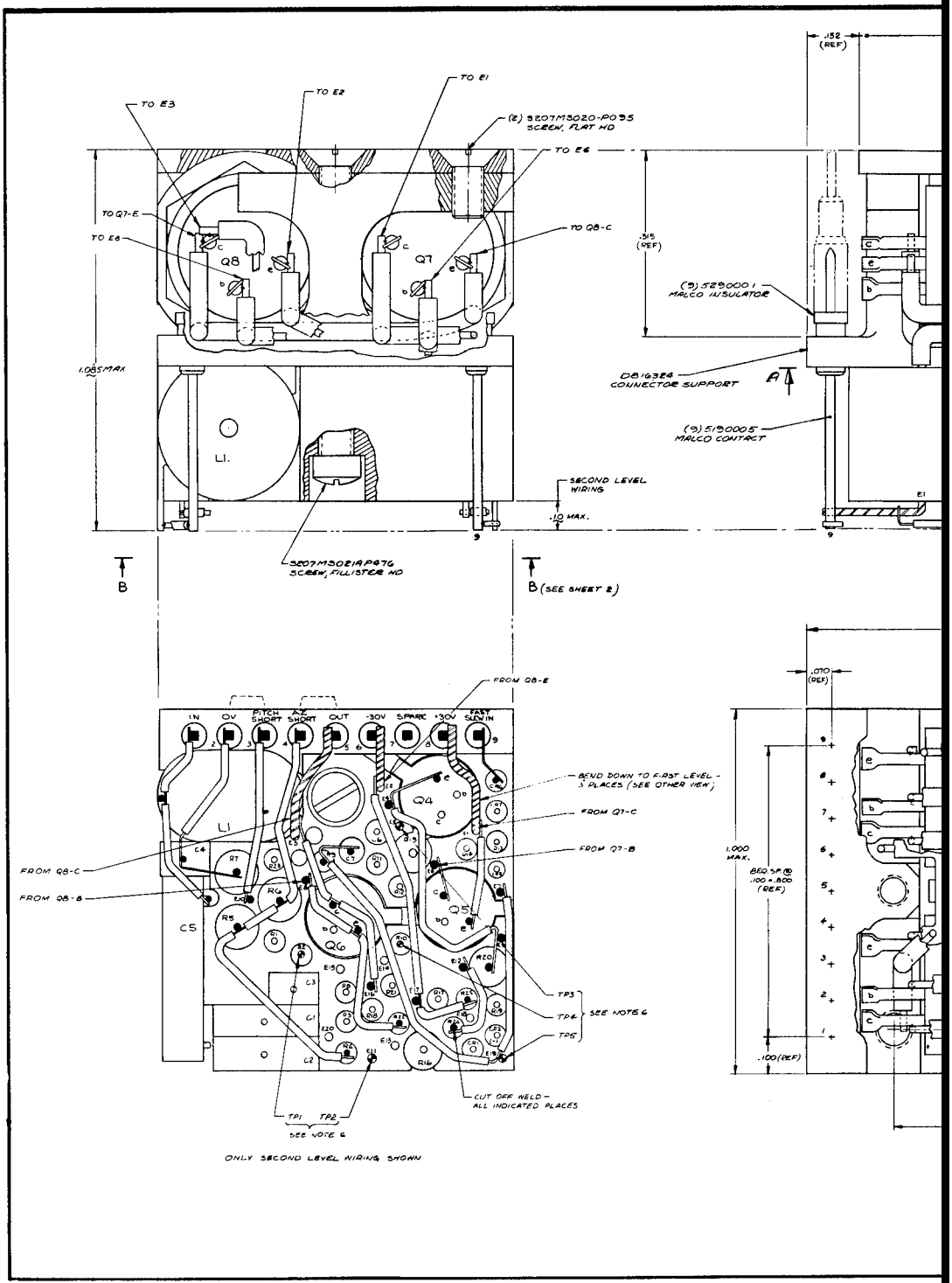
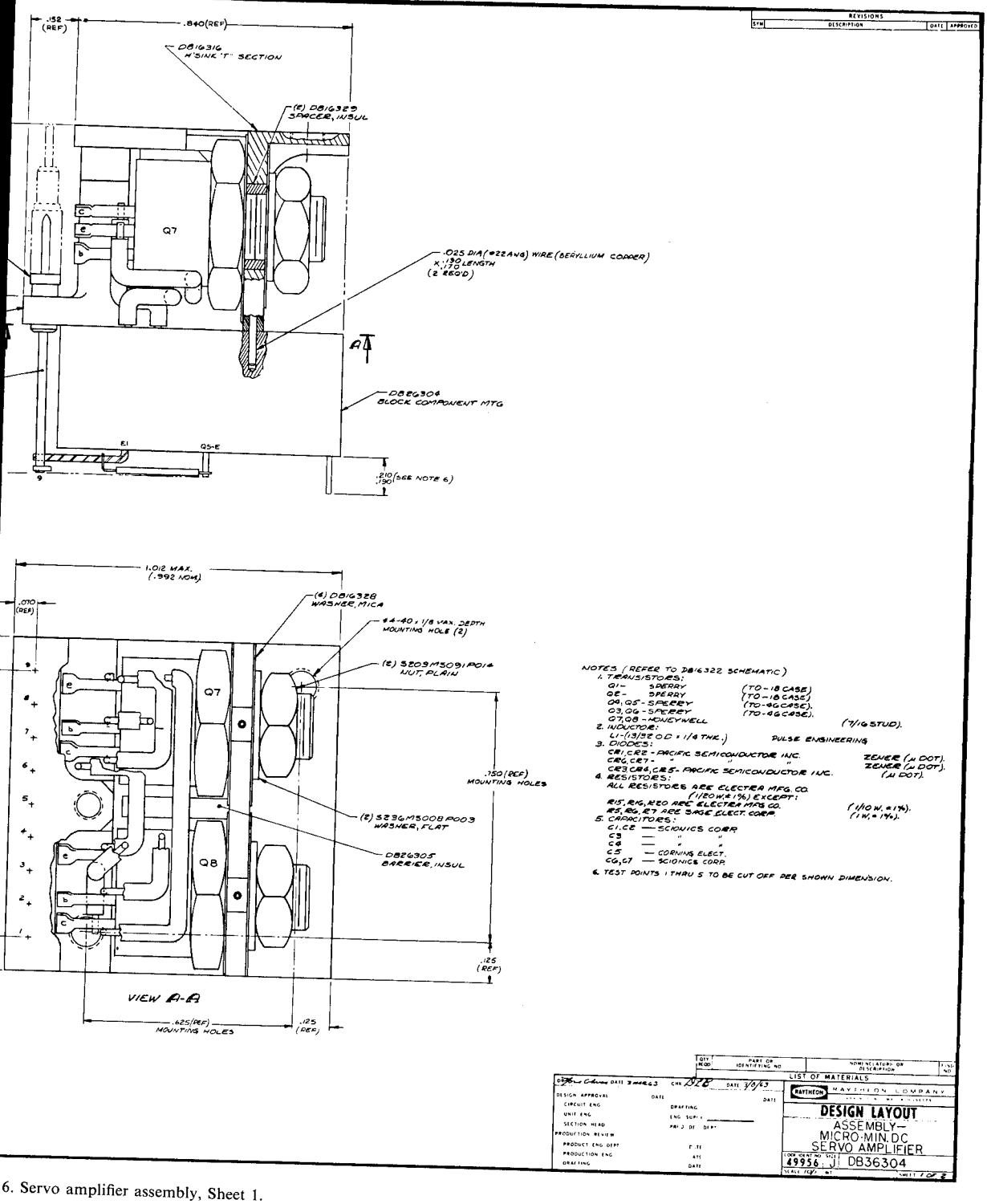


Fig. 16. Servo amplifie



REVISIONS

SYM	DESCRIPTION	DATE	APPROVED

NOTES (REFER TO DB16322 SCHEMATIC)

1. TRANSISTORS:
   Q1— SPERRY (TO-18 CASE)
   Q2— SPERRY (TO-18 CASE)
   Q4, Q5 - SPERRY (TO-46 CASE).
   Q3, Q6 - SPERRY (TO-46 CASE).
   Q7, Q8 - HONEYWELL (7/16 STUD).
2. INDUCTOR:
   L1 - (13/32 O.D. x 1/4 THK.) PULSE ENGINEERING
3. DIODES:
   CR1, CR2 - PACIFIC SEMICONDUCTOR INC. ZENER (1 DOT).
   CR5, CR7 - " " ZENER (2 DOT).
   CR3, CR4, CR6 - PACIFIC SEMICONDUCTOR INC. (1 DOT).
4. RESISTORS:
   ALL RESISTORS ARE ELECTRA MFG. CO. (1/20 W, ±1%) EXCEPT:
   R15, R16, R20 ARE ELECTRA MFG CO. (1/10 W, ±1%).
   R5, R6, R7 ARE SAGE ELECT. CORP. (1 W, ±1%).
5. CAPACITORS:
   C1, C2 — SCIONICS CORP.
   C3 — " "
   C4 — " "
   C5 — CORNING ELECT.
   C6, C7 — SCIONICS CORP.
6. TEST POINTS 1 THRU 5 TO BE CUT OFF PER SHOWN DIMENSION.

QTY (REQD)	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	F.S.C. NO.

LIST OF MATERIALS

DESIGN APPROVAL	DATE		DATE
CIRCUIT ENG		DRAFTING	
UNIT ENG		ENG. SUPV.	
SECTION HEAD		PROJ. DE. DEPT	
PRODUCTION REVIEW			
PRODUCT ENG. DEPT		E. TE	
PRODUCTION ENG.		ATE	
DRAFTING		DATE	

CHK DZB DATE 3/6/63

RAYTHEON MAYTHEON COMPANY

DESIGN LAYOUT
ASSEMBLY—
MICRO-MIN. DC
SERVO AMPLIFIER

LOCATION NO. SIZE	DRAWING NO.	REV.
49936 J	DB36304	

SCALE FULL WT. SHEET 1 OF 2

g. 16. Servo amplifier assembly, Sheet 1.

volume warrants. If component values are changed during production, as often happens, discrete components in open "egg crate" holders can be used temporarily in production until the deposited modules again become available.

Naturally, heat dissipation problems limit the packaging density on higher-powered analog and power supply circuitry instead of interconnection limitations as is the case in digital equipment. However, significant miniaturization can often still be achieved by separating the low-dissipation components into conventional welded cordwood packaging. They are then mounted in preformed holding forms with the high-heat dissipating components mounted directly onto heat sinks. The heat sinks transfer the heat directly out of the module. The prototype DC servo amplifier, shown on Figs. 15 and 16 contains 48 discrete components and is capable of delivering up to 30 W on demand. It is an example where this technique has been used.

One further problem, which is a continuing and present headache in production, is the great variety of component lead sizes and materials (i.e., Kovar, Dumet, nickel-based alloys) that each manufacturer prefers for his own discrete components. Hopefully, there will shortly be some semblance of standardization. Otherwise we will all be forced to try to coerce each manufacturer to make "specials" for us, merely to reduce the number of different weld schedules.

From a welded packaging consideration, discrete components with radial or circular pattern leads are more difficult to package. The discrete transistors with parallel leads protruding from rectangular packages in a manner similar to rectangular integrated logic are easiest to handle. Generally speaking, the availability of miniaturized rugged connectors and larger-valued capacitors lags behind the availability of a variety of miniaturized transistors, diodes, and resistors.

CONCLUSION

It is possible to significantly reduce the size of present aerospace computer equipment now in production without drastically increasing production skills and fabrication methods. This is made possible primarily by the advances of component manufacturers to manufacture smaller reliable components as well as volume production of integrated circuits. Solid multilayer matrices potentially offer a means in the right direction toward significantly reducing the complexity of interconnections. However, a considerable amount of progress is still necessary in the areas of reliability control and nondestructive testing.

From a systems viewpoint, there is much to be gained by leaving the component problems to the component manufacturer. However, they perhaps do themselves a disservice when they limit themselves to their own fabrication problems and offer components in peculiar shapes and with varied lead materials and sizes. This merely pushes the problems onto the system packaging engineers. An analogous argument can be made from the systems circuit engineering standpoint. In short, more attempts at standardized requirements would benefit all concerned.

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Separable Multicontact Connectors for High-Speed Computer Circuits

M. E. ECKER, H. R. KAUPP, AND D. P. SCHNORR
Computer Advance Development, Radio Corporation of America, Camden, New Jersey

Recent trends in the growth of nanosecond computer systems have indicated the need for transmission lines as the means for interconnecting large numbers of logic circuits. This paper describes the development and fabrication of a pluggable edge-board connector designed for such use, and employing coaxial cable down to 0.008 in. diameter. Electrical parameters such as cross-talk, reflection ratios, and image impedance of the connectors are considered, as are the means devised for distribution of precisely regulated bias voltages to the logic wafers.

INTRODUCTION

PERIODICALLY, in the normal improvement of any technology, particular problems arise which require solutions utilizing novel, and at times, not completely orthodox techniques. Such a problem instigated the development described by this paper; a development which ultimately produced a separable multicontact connector suitable for use with miniature coaxial cable.

Recognizing the need for an extension of the computer state-of-the-art to include high-speed digital equipment, the Government began a program several years ago to develop nanosecond computer techniques and circuitry. RCA was one of the companies selected to participate in this activity. The project goal was three to four logic levels per nanosecond, ten nanoseconds per memory read-regenerate cycle, and a shift rate of about six to eight bits per memory cycle. At these speeds problems occur in packaging density, cross-talk, and wiring delays. At the expected rate of propagation, an interconnecting transmission line, $1\frac{1}{2}$ in. in length corresponds to a delay of one logic level. The cross-talk tendency in high-speed computers necessitates the use of a well-shielded transmission medium. The problem, therefore, resolves itself into one of techniques aimed toward dense packaging and the use of coaxial cable as well as associated connectors.

DISCUSSION

Signal transmission, at kilomegacycle computing rates, introduces a number of new problems in packaging; in addition, the extremely low voltages and delay minimization demanded for proper operation of the tunnel-diode computer circuits [1] led to careful consideration of the following design criteria:

1. Use of transmission line is necessary; line lengths must be kept as short as possible because of propagation delay.
2. Since point-to-point cabling is desirable to minimize delays, it is imperative that coaxial cable be used for this application. This is the best connection method permitting wiring crossover without the danger of cross-talk at high frequencies.

3. Serious discontinuities in the transmission system will cause reflections which can have an undesirable effect on the operation of the circuits.
4. In a feasibility study machine, the basic logic gate circuit should be a plug-in, since circuit components must be readily available for testing and/or replacement.
5. Due to noise sensitivity of the high-speed circuits, filtered low-impedance power supply distribution lines are required.
6. Any connection method used should be open enough to provide ample room for air passage between the circuits; dissipation of heat is essential to proper operation of this equipment.

After examination of many alternatives, a test unit was constructed. This structure, as illustrated in Fig. 1, contains 34 logic gates disposed in three columns, with the logic gate wafers spaced 0.350 in. apart. The basic wafer is 0.7 in. by 1.5 in., and is composed of a 0.040-in.-thick brass ground plane, with a 0.030-in.-thick glass-filled Teflon circuit board. The circuit board is notched along both sides to accept power supply filtering elements, consisting of silvered segments of barium titanate. The signal input connection tabs are located along the bottom edge of the wafer. The wafer and wafer holder assembly fits between two I-beams which, in addition to providing structural support, also serve as guides for the low-impedance power supply lines feeding the individual wafers. The low-impedance power supply lines were silvered strips of barium titanate 0.010 in. thick by 0.300 in. wide by 5.5 in. long. Miniature solid-jacketed coaxial cable was used extensively in making interwafer connections and a wide range of this type of transmission line was developed for the project; i.e., cables having an O.D. of 0.008 to 0.039 in. and characteristic impedance of 4.5 to 100 Ω. The cables are connected to the wafers by soldering—the outer jacket was soldered to the wafer ground plane and the center conductor was soldered to appropriate pads on the wafer.

CONNECTOR DEVELOPMENT

Initial designs of the connector considered primarily a means of connecting to the signal tabs of the wafer, with the power connection as a secondary issue. The connector was originally visualized as a combination of individual contact pins, shielded from each other by a metal partition which would be part of the corresponding ground contacts. These ground contacts were to be connected together to make a common interconnected grounding shield. Due to

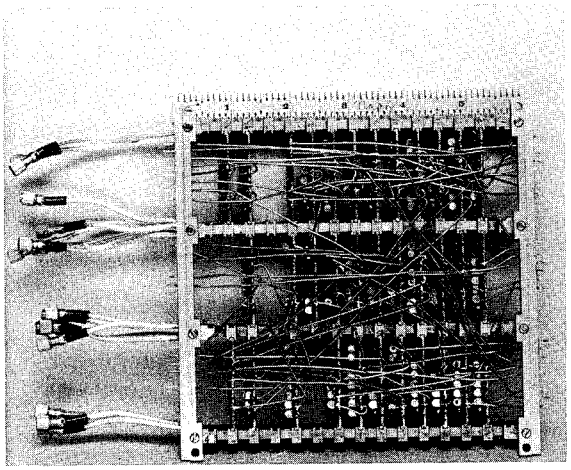

Fig. 1. Logic test unit.

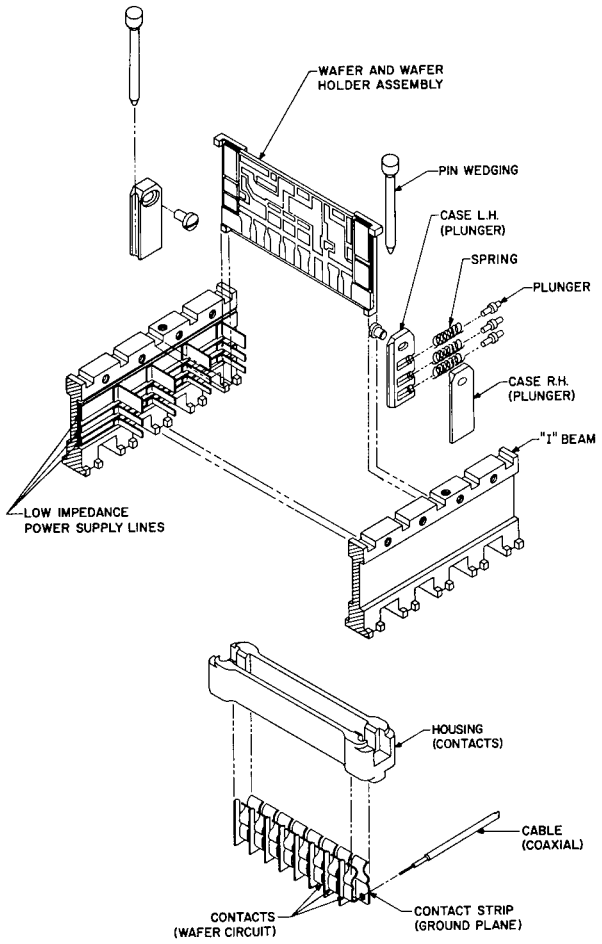

Fig. 2. Exploded view of wafer connector.

the expedient nature of the project, it was decided to use the basic edge-board connector idea, with modifications to adapt such a device for use with coaxial cable together with a ground plane wafer.

The method of power distribution down the I-beams presented some problems to the connector designer. The lines were constructed of silvered barium titanate strips, which are very fragile and, therefore, any connection scheme forcing connecting tabs onto wafer power tabs must use limited pressure. This pressure should be such that it will not crack the barium titanate, yet be sufficient to establish good electrical contact. The presence of hairline cracks in the 0.010-in.-thick barium titanate power lines could present the possibility of silver migration from both silvered surfaces and could result in a shorted line.

In order to prove out the design, the connector concept had to be modified to accept a wafer which was being used in a systems feasibility study machine. Since the I-beam and wafer design was already finalized and oriented toward soldered connections, the connector philosophy had to be changed considerably. Figure 2 shows an exploded view of the connection system for this type of wafer. With the slight modifications made, the base portion of the connector assembly was adapted to the subsystem frame structure. Power distribution was accomplished by means of a beam containing a number of small spring-loaded plungers, as shown on the

figure. The beam is mounted to the I-beams so as to permit its displacement toward the circuit face of the wafer. A wedging pin is inserted between the grooved edge of the beam and the rear face of an adjacent wafer. The spring-loaded plungers are oriented in the beams so that they press the tabs of the low-impedance power supply against the pads on the wafer with sufficient force to ensure good electrical contact.

MISMATCH—SIGNAL REFLECTIONS

Independent of mechanical design considerations and reliability, it is important to know how a connector behaves as a circuit element. An impedance mismatch in a transmission line system will cause part of a signal incident to the electrical discontinuity (which, in this case, is the connector) to be reflected back toward the source.

The test arrangement used to measure the connector reflections is shown in Fig. 3. Since the connector is used in conjunction with circuits having rise times of the order of 0.2 nsec, it is desirable that the rise time of the pulse used to test the connector response be at least as fast. Two problems limit the accuracy of these measurements. First, the fastest pulses presently available are generated by tunnel diodes; but, since tunnel diodes are used in the logic system itself, the test system cannot use much faster pulses. Secondly, it is necessary to use miniature coaxial cables to separate and make distinguishable reflections in the system under test. Because the loss of these cables is of the order of 1 db/ft at 1 kMc, long cables will significantly distort the fast rise time pulses.

The heart of the test system is a very fast tunnel-diode pulser. The tunnel diode has no leads, and is held against the unbroken center conductor of an RG-188 coaxial T-connector. The tunnel diode, which has a peak current of 50 mA and a capacity of 5.7 pF, is used in a bistable mode and is biased close to the peak. The diode is triggered by an external pulse generator. Resetting of the diode is aided by the negative reflection caused by the termination of the 75-Ω coax in 3 Ω, as shown in Fig. 3. Thus, by locally generating the fast pulse, it is feasible to use a relatively slow pulse generator and the long lengths of coax delay cables associated with the timing of sampling oscilloscopes. The rise time of the pulse generator, as seen on the oscilloscope using vertical amplifiers of 0.35 and 0.1 nsec, is 0.4 and 0.17 nsec, respectively.

Coaxial cable is used to terminate the wafer side of the connector, since it virtually eliminates stray parameters from the setup. To make this connection, a hole is drilled through the wafer at a signal tab. The coaxial cable center conductor is then passed through the hole and soldered onto the tab. The cable's outer conductor is soldered to the ground plane of the

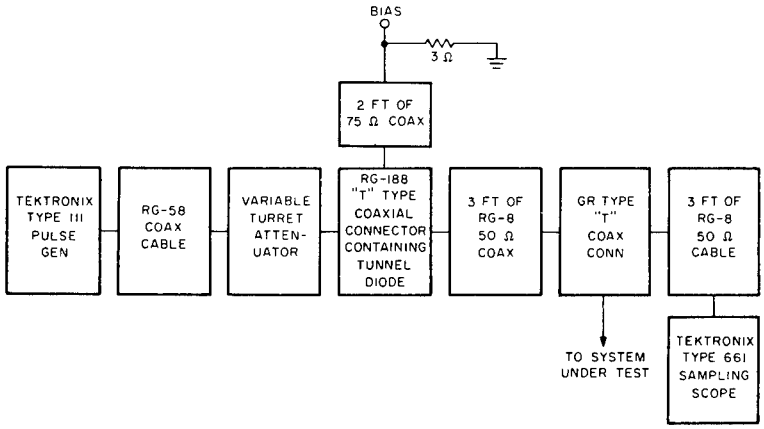

Fig. 3. Test setup for observing pulse response of coaxial connectors.

wafer. To observe the connector reflections, a 1-ft length of coaxial cable was used as a termination and another identical length was used on the conventional end of the connector. Thus, the discontinuity in the coaxial line is in the connector and its associated wafer tab. The wafer tab must be considered as part of the connector characteristic.

The extent of the discontinuity presented to the pulse by the connector is implicit in the reflection ratio. The reflection ratio here is defined as the ratio of the maximum voltage amplitude of the pulse reflected from the connector to the steady-state voltage level of the pulse incident to the connector. A negative sign in the reflection ratio indicates that the reflected and the incident pulses are of opposite polarity.

The incident voltage signal is observed on the scope as the voltage reflected from an open-circuited connector. Table I indicates some experimental voltage reflection ratios of the connector as used with coaxial cables having different characteristic impedances. For comparison purposes, the reflection ratio of an RG-188, 50-Ω coaxial cable-to-cable connector was observed to be 2.8%.

EQUIVALENT CIRCUIT

From a qualitative standpoint, it is convenient to think of the connector as a short piece of lossless transmission line. Consequently, since it is short, the connector can be adequately represented by a constant K filter section [2] as illustrated in Fig. 4a. Under matched conditions, the characteristic or image impedance and delay of this equivalent circuit are approximately,

$$R_I = \sqrt{L/C} \qquad T = \sqrt{LC}$$

where R_I is the image impedance of the connector.

$$e_R = e_I - R_0 i_1$$

$$e_T = i_2 R_0$$

where e_I, e_T, and e_R are, respectively, the incident, transmitted, and reflected voltages of the connector and R_0 is the characteristic impedance of the cable. The incident, as well as reflected waveforms for a cable characteristic impedance of 25 Ω, were observed on the oscilloscope and are shown in Fig. 4b. The reflected waveform was then computed, with the aid of an RCA 301 computer, using the observed incident voltage in numerical form. Values for R_I

TABLE I

Reflection Ratio of Miniature Plug-in Wafer Connector for Various Characteristic Impedance Cables

Type of cable	Characteristic impedance, Ω	Voltage reflection ratio, %
Solid copper jacket (20-mil O.D.)	6.5	23.2
Solid copper jacket (35-mil O.D.)	25	9.1
Solid copper jacket (20-mil O.D.)	54	1.8
Microdot	75	−2.7

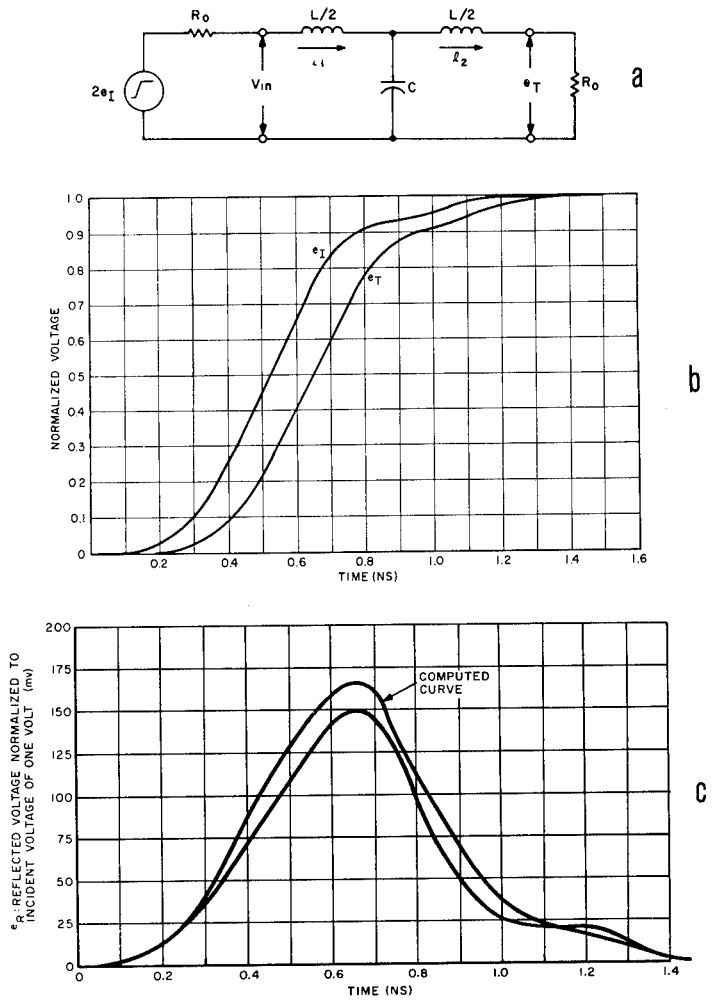

Fig. 4. Plug-in connector circuit model and computed waveforms: (a) equivalent circuit; (b) incident and transmitted voltage waveforms for $R_0 = 25\ \Omega$, $L = 5.5$ nH, $C = 1.8$ pF; (c) comparison of computed and experimental reflected waveforms for $R_0 = 25\ \Omega$, $L = 5.5$ nH, $C = 1.8$ pF.

and T as indicated by experimental results were used. Computation runs were made, adjusting R_I and T, until the computed and experimental waveforms coincided, as shown in Fig. 4c.

The parameters used to compute the waveforms in Fig. 4 yielded a matched image impedance of 55 Ω, and a delay of 0.1 nsec. This checks closely with the measured delay of 0.11 nsec observed with the 54-Ω terminated connector. Also, the computed and measured connector delay both equal 0.13 nsec for the connector terminated in 25 Ω.

A plot of reflection ratio versus incident voltage rise time for the connector terminated in 25 Ω is shown in Fig. 5. This curve was obtained using the 0.1-nsec oscilloscope unit. For rise times greater than 20 times the connector delay, the reflection ratio is less than 5%. However, for signals with rise times of the order of 0.2 nsec, the reflection ratio is close to 25%. When the connector is used in conjunction with a circuit wafer, the connector reflection might be

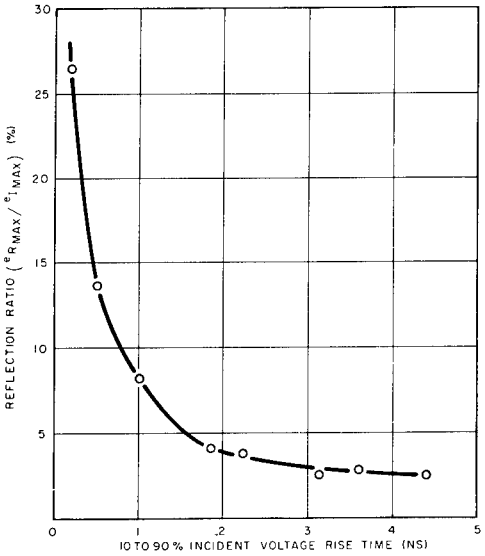

Fig. 5. Reflection ratio of plug-in connector as a function of incident voltage rise time with 25-Ω cable terminations.

insignificant in comparison to the reflection caused by the nonlinear impedance of the switching circuit. However, if the connector is used to interconnect cables, a reflection of 25% could be significant.

It should be noted that the reflections shown in Fig. 5 were caused by a discontinuity less than 0.25 in. long. Making the ground path 1 in. longer than the signal path—even when using a 1.5-in.-wide copper bus—caused the reflections to more than double in amplitude.

CROSS-TALK

Perhaps more important than signal reflections caused by the connector is the connector cross-talk problem, i.e., the signal induced in a cable, through its connector, by the signal passing through an adjacent connector. The setup used to observe the cross-talk between two adjacent connectors is shown schematically in Fig. 6a. This setup replaces the GR-type T-connector in the test system of Fig. 3. The voltage incident to point 1 of Fig. 6a, observed using the 0.35-nsec oscilloscope plug-in unit, is shown in Fig. 6b. The corresponding transmitted and cross-pulse waveforms, as defined in Fig. 6a, are shown in Fig. 7.

By referring to Fig. 7, it can be seen that the backward cross-pulse has the same polarity as the incident pulse while the forward cross-pulse is of opposite polarity. The difference between the incident and transmitted waveforms is primarily due to skin-effect losses in the 2 ft of coaxial cable. It is not caused by the connector, as verified by the computation of the transmitted waveform illustrated in Fig. 4b. The cross-pulse ratio here is defined as the ratio of the steady-state incident voltage level to the maximum value of the cross-pulse signals. Figure 8 shows plots of this ratio *vs.* the rise time for solid-jacketed coaxial cables having characteristic impedance of 25, 54, and 75 Ω. The data used to plot these curves were obtained using the 0.1-nsec oscilloscope plug-in unit, hence the curves are accurate down to 0.4 nsec input rise time. Below 0.4 nsec, the curves are optimistic because the narrow pulses are attenuated by the scope and the incident voltage level is not. When the cables were soldered directly to the wafers, the cross-pulses were approximately 15 db further down. Cross-pulses induced into one connector further removed are about 12 db further down than the adjacent cross-pulse.

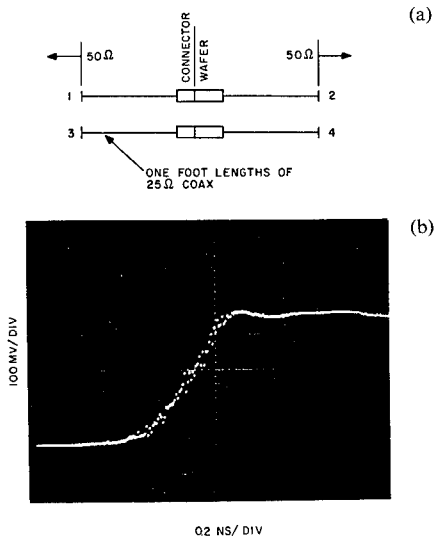

Fig. 6. Cross-talk test setup and results: (a) method of observing cross-pulses. 1–incident pulse. 2–transmitted pulse, 3–back cross-pulse, 4–forward cross–pulse; (b) output of tunnel diode pulser.

CONTACT RESISTANCE

The pulse evaluation previously discussed indicates the response of the connector as a dynamic circuit element. However, it is also important to understand how the connectors will behave in typical circuit use, as well as what variations exist between individual connectors. The DC contact resistance, therefore, was used to index the dependability of the connector.

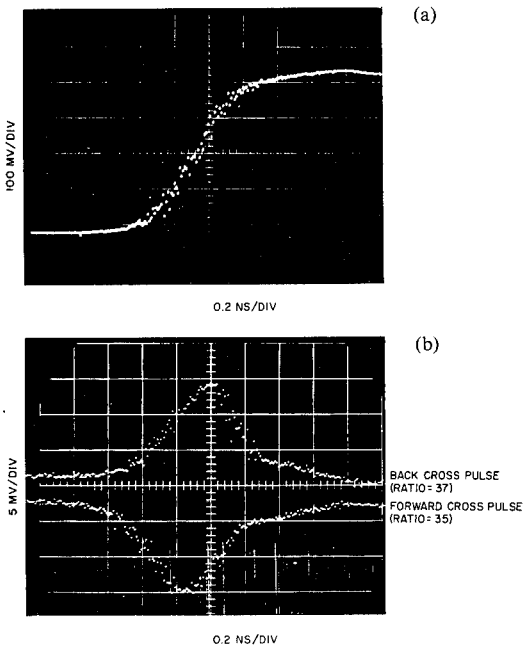

Fig. 7. Response of coaxial connector measuring setup to incident pulse (Z_0 25 Ω): (a) transmitted pulse; (b) cross-pulses at adjacent connector.

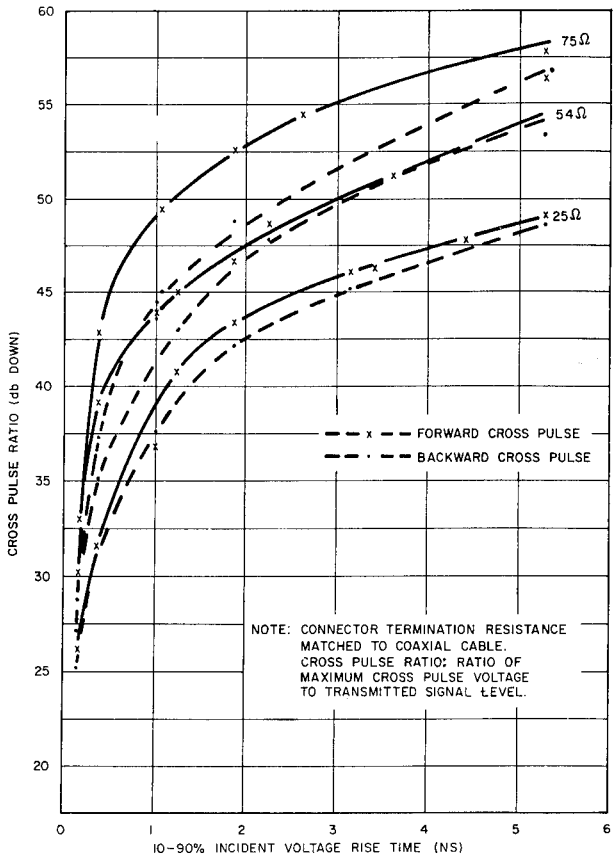

Fig. 8. Cross-pulse ratios of plug-in coax-wafer connector *vs.* incident voltage rise time for 25-, 54-, and 75-Ω coax.

In the test setup used, the contact resistance of two connectors at a time was measured. The resistance measured is the contact point at the junction of the signal spring and the wafer pad. Contact resistance was measured as a function of current and was found to be quite uniform. It averaged about 4 mΩ for current over 5 mA. The contact resistance was also observed as a function of the number of times a wafer is inserted into the connector bank. As expected, the contact resistance decreased with the number of insertions.

CONTINUOUS PERFORMANCE TESTS

Other tests were run to check contact resistance as a function of time. This was done to determine the effect of dirt or oxide film on the contact resistance. As in the insertion test, the current was maintained at 5 mA, and the wafer tabs were milled flat. Wafers 0.080 in. thick were used. Of the connectors tested, half were continuously supplied with current, while the other half were supplied with current only during the resistance measurement.

Measurements continued on 32 connections for a period of 19 days. Each day the contact resistance had substantially increased, but, after applying pressure to the wafer, the resistance was decreased to about 10 mΩ. It is believed that the increase in resistance was caused by some imperceptible movement of the wafer in its connector due to handling of the connector supporting frame, or by slight vibrations caused by moving the frame on the lab bench. This motion or vibration could have permitted dust particles to work down between the contact

surfaces or a shifting of the wafer might have resulted in the displacement of the contact onto an oxide film surface.

Next, test data were taken for wafers rigidly held in their connectors so that no movement of the signal spring on the wafer tab could occur. The procedure was identical to that of the previous test except that 64 connections, instead of 32, were used. This test was run over a period of one month. The contact resistance values stayed between 3 and 5 mΩ during this period.

Finally, a test was run that simulated actual subsystem conditions. A fan, forcing air in the direction of the connector, was used to cool the wafers. A total of 64 connections was tested. The other test conditions were as noted above.

At the end of the two-month test, all 64 connectors exhibited a contact resistance of 3 to 5 mΩ, despite the fact that the connector bases were completely fouled with dirt from the cooling system.

Therefore, among the conclusions of the above tests are:

1. In this low-voltage application, it makes no difference whether the connectors are continuously supplied with current.
2. Circuit wafers should be tightly secured in the connector so that mechanical disturbances cannot cause the signal spring to move onto an oxide film that opens the circuit. If this is not practical, a contact protectant, such as "Cramolin," should be used.
3. In order to maintain flat wafer tabs of uniform thickness and eliminate oxide deposits, it was decided to put gold plating on future printed copper wafer tabs.

MODIFICATIONS OF ORIGINAL DESIGN

The development of improved logic circuits and a new power distribution concept necessitated further refinements in the original connection scheme. The new connectors were developed for a 40-gate subsystem, having logic circuits with reduced delays and power dissipation, increased repetition rate, increased fan-in and fan-out, and considerably smaller electrical components. These new logic circuits made it possible to utilize the 0.7 by 1.5 in. wafer size previously used but required additional signal connections on the base connector; i.e., 12 instead of 8. Thus, closer spacing of connectors was required using contact centers of 0.100 in. instead of 0.150 in.

The new connector design incorporated:

1. A shorter electrical path.
2. A spring contact configuration designed to permit heat treatment.
3. Higher contact forces.
4. A 12-contact-pair connector per logic wafer unit.
5. A 20-db reduction in cross-talk due to better shielding.
6. Effective characteristic impedance of 40 Ω.
7. Overall reduction in physical size, thereby improving packaging density capability.

Figures 9a and 9b illustrate the front and rear surfaces of the basic circuit wafer. The circuit wafer is comprised of three basic parts properly registered and bonded together. The first part carries the actual circuit; this is a 0.005-in.-thick cementable Teflon substrate clad with 1 oz of copper for printed wiring. This circuit element is bonded to the second part, which is a 0.015-in.-thick gold-plated brass ground plane, which also serves as a rigid support plate. The third part is composed of barium titanate, 0.010 in. thick, which is soldered onto the brass ground plane. This barium titanate element is completely silvered on one side and on the other side is silvered by a screened pattern as indicated in Fig. 9b. These silvered areas serve as filtering capacitors that absorb transient switching signals, thereby reducing power supply noise. The circuit element is smaller than the ground plane to allow lands on both edges of the circuit side to be exposed for ground plane connection.

Because of the increased high-frequency filtering capability on the rear of the wafer, it was possible to relax several of the I-beam power distribution requirements; i.e., the power

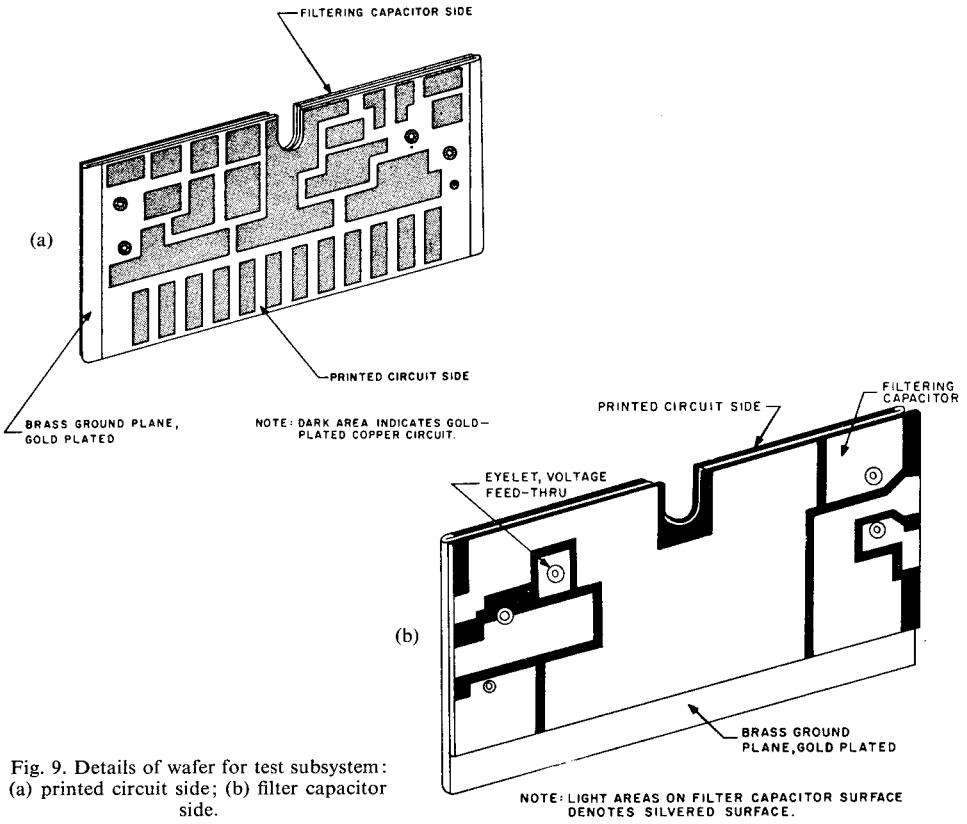

Fig. 9. Details of wafer for test subsystem: (a) printed circuit side; (b) filter capacitor side.

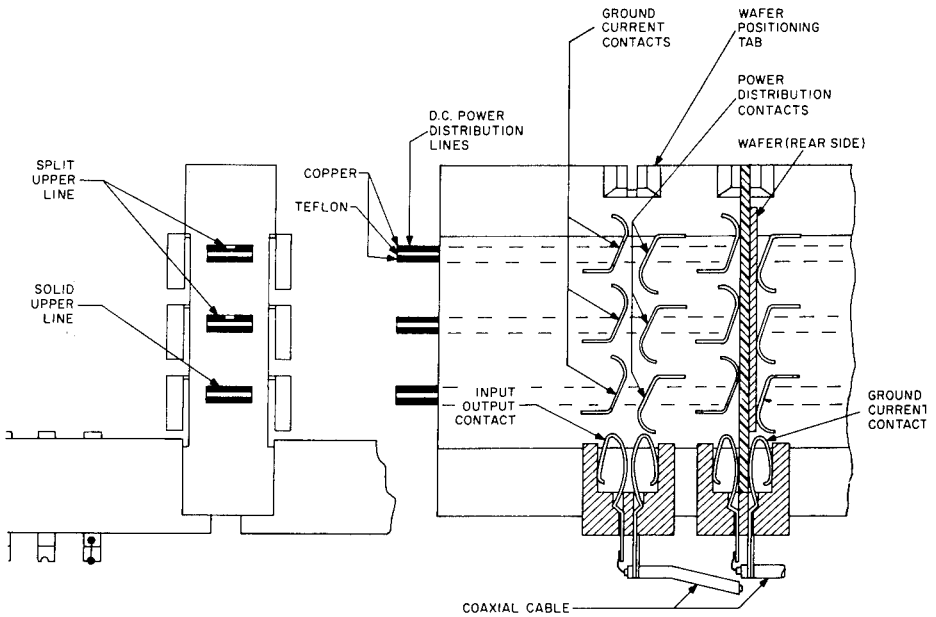

Fig. 10. Sectional view of subsystem frame assembly.

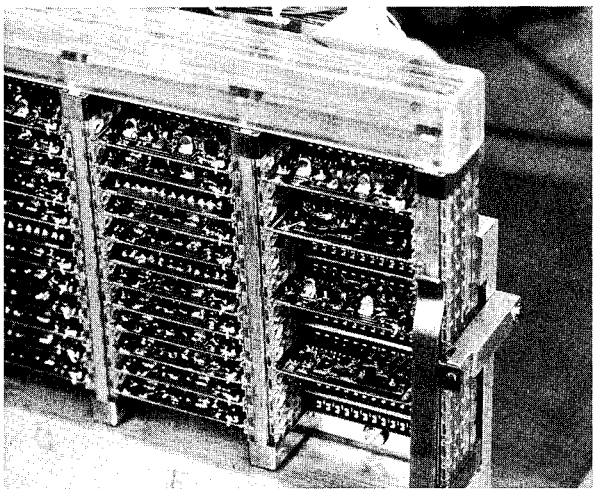

Fig. 11. Feasibility subsystem (front view).

distribution lines need only be comprised of double copper-clad Teflon. These new considerations are illustrated in Fig. 10. The power-carrying I-beam was fabricated from four sections of an acrylic thermoplastic material designed to have suitable apertures and channels to contain horizontal power distribution lines with attached contact springs when stacked together. The lower segment had a steel reinforcing member running its full length for structural support.

The lower section also contained removable inserts to permit the removal of individual base connector members after assembly and wiring operations had been performed. Repairability of the I-beam was made possible by holding the entire assembly together with clips at each end and a leaf-spring across the top of the beam which was locked by the clips. Figure 11 is a closeup view of a portion of the 40-gate subsystem showing the connector-wafer relationship. This subsystem was designed to accommodate 48 logic gates and measures 7.25 × 3.25 × 0.9 in. It has been operated for over 1000 hr without a contact failure. An oxide film problem occurred with the silvered surfaces of the filter capacitors on the back of the logic wafers. This problem will be solved in future wafer construction by glazing the contact surface with gold.

CONCLUSION

The feasibility of interconnecting high-speed circuits by means of a flat-spring connector with "coaxlike" behavior was proven. The development and subsequent testing of at least two different types gave encouraging results, and at the present time, these connectors are in actual operation in the 40-gate subsystem mentioned.

ACKNOWLEDGMENT

The authors wish to express their appreciation to D. R. Crosby and S. T. Jolly for their guidance during this development.

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Multilayer Printed Circuits

GEORGE MESSNER
Photocircuits Corporation, Glen Cove, New York

This paper describes the design criteria and methods for preparing pattern layouts and artwork for multilayer printed circuits. Performance capabilities of multilayer printed circuits, their reliability problems, and the results of environmental and electrical tests are discussed, and descriptions of current multilayer applications are given. The paper also deals with anticipated future usage of multilayer circuits and describes various interconnection techniques, such as wire wrap, welding, and plug-in contacts, and discusses the economic aspects of packaging with multilayer circuits.

THE MULTILAYER CIRCUIT CONCEPT

THE QUESTION of interconnections between components or modules has become one of the foremost topics whenever the problems of electronic packaging are discussed. The complexity of present-day electronic systems requires a tremendous number of such interconnections. Space environments require them to be highly reliable and not subject to environmental damage or changes. Miniaturization requires the interconnections to be fitted into very small areas and throw-away concepts require that the majority be separable for easy replacement.

One interconnecting approach which attempts to meet those requirements is multilayer printed wiring. Multilayer printed boards consist of a number of circuit planes separated by dielectric (plastic) materials. The conductors located on various levels can be interconnected between themselves and brought out to the surfaces at any desired location. At these surfaces points, components or modules are connected to the internal circuitry. There are a number of methods available for achieving the interconnections between circuit layers and the surfaces but the most frequently and widely used so far is the plated-through hole method.

The multilayer printed boards preserve all the characteristics of regular printed wiring: large volume production capability, exact reproducibility of circuitry from board to board, significant reduction of wiring time, elimination of miswiring, and support for components with components easily mounted or replaced. But multilayer printed wiring also has its own unique characteristics which are important in the era of miniaturized and complex electronic systems: high density of circuitry and terminal points, increased freedom of conductor routing, shorter conductor paths, integral shielding and heat sink planes and improved environmental performance achieved by locating all conductors within a homogeneous dielectric material. Certain disadvantages of this technique are apparent: changes in the circuitry of a completed board are difficult to achieve, the interconnections are not visible and the boards are costly.

In the past three years, multilayer printed wiring has been used for a wide range of interconnection applications: interconnecting standard components mounted in regular fashion or in cordwood configuration, interconnecting various welded or encapsulated modules, and functional circuit cards and interconnecting integrated circuitry, either in TO cans or flat packages. Just to make the picture complete, multilayer printed wiring boards with internally located ground planes have been used to achieve a "strip line" effect in high-speed computers.

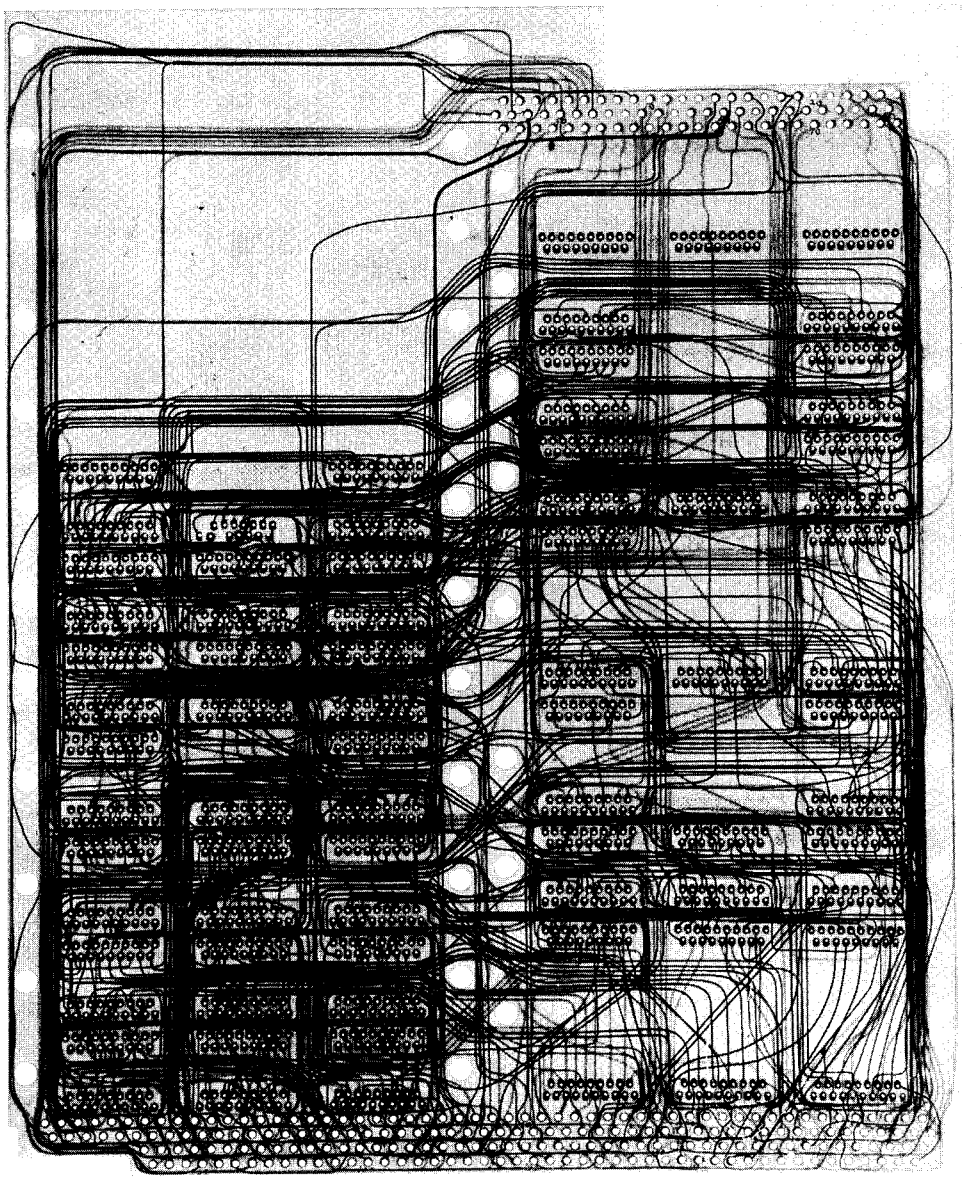

Fig. 1. Seven-layer Encapsulayer board showing the high conductor density possible with multilayers. All circuit layers are encapsulated within the board.

The use of multilayer printed wiring so far has been limited primarily to various military equipment, usually mobile or airborne computers, where demands for miniaturization and weight reduction play a predominant role.

EFFICIENT DESIGN FOR MULTILAYER CIRCUITS

When developing the packaging design for an electronic system one fact has to be borne in mind. There is an optimal limit to the size and cost of a single discrete unit or a functional block, card, etc., after which it is uneconomical or inefficient to further increase its complexity

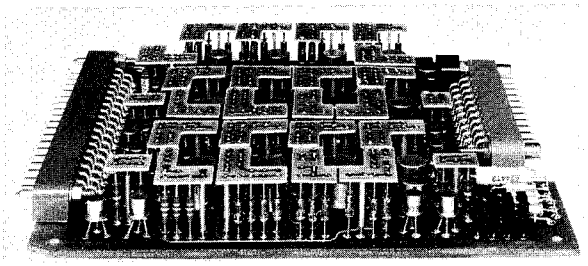

Fig. 2. Cordwood assembly which utilizes a four-layer Encapsulayer as the "mother" board.

or dimensions, since it will then become either too specialized and therefore not easily interchangeable, or too costly to be thrown away. After this limit for individual module size has been established, further interconnections between such units must be made separable for easy maintenance of the equipment. Since there are usually a very large number of such discrete modules in a given system, a simple, compact, and efficient medium must be provided for their interconnection.

It is for exactly such application, that multilayer printed wiring has found its widest use, i.e., to serve as "mother boards" for interconnections of either a large number of multipin modules or connector banks (into which printed circuit cards are plugged) or, most recently, for the interconnection of integrated circuit packages. In these applications the inherent characteristics of multilayer printed wiring have been utilized to the fullest extent. For instance, multilayer boards interconnecting 130 to 300 multipin encapsulated modules have been manufactured in fairly large quantities. Also, a number of multilayer boards have been made, each interconnecting approximately 600 integrated circuit packages in TO-5 cans or 400 flat packages. These examples indicate that a single multilayer board can interconnect large segments of an electronic system thus saving a considerable amount of space and weight while efficiently reducing the number of input–output terminations with associated hardware which would be required if conventional wiring approaches had been used.

To illustrate this point: seven large two-sided cards with a total of approximately 600 input–output terminals have been integrated into a single multilayer board of approximately the same size as one of the double-sided boards with only 100 inputs–outputs needed for interconnection to the rest of the system. As a general rule, multilayer boards are most efficiently used when the majority of interconnections are located within the board and only a small percentage of them are needed for communication with the outside. Terminations to the outside world from multilayer boards can be achieved by any existing printed circuit terminals or connectors.

There are also numerous systems in use which consist of a number of smaller multilayer boards which interconnect various modular packages. Such cards are then interconnected

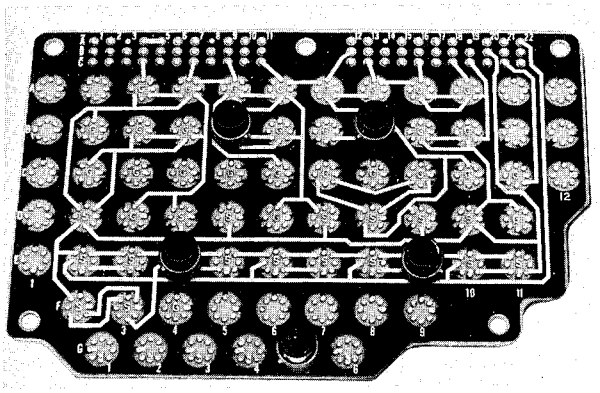

Fig. 3. Five-layer Encapsulayer used for interconnection of Fairchild "Micrologic" elements. One internal layer is a ground plane.

between themselves by larger multilayer mother boards which in turn are connected by a "grandmother" multilayer board. Such packaging techniques enable the achievement of a very compact package with a strong mechanical structure, an efficient heat sinking and ventilation system, and a minimum of cabling and harnessing. When designing such a multiple card system, substantial savings in artwork and tooling, as well as manufacturing costs can be achieved if all multilayer cards are of the same general configuration and the modules are located on identical positions on all boards—changing only the internal circuitry from board to board as the design requires. In this case multilayers provide the unique possibility of accommodating interconnections of varying degrees of complexity on different boards with exactly the same dimensions. This can be achieved by the fact that the thickness of individual layers can vary from 0.004 to 0.016 in. in steps of 0.002 in. and can be selected in a manner to provide the same overall board thickness through a wide range in the number of layers. This possibility of adding or eliminating layers and still keeping the required overall board thickness gives the design engineer greater freedom and permits him to exercise better control of circuit layout than is possible with conventional packaging methods. With multilayers, circuit paths can be made shorter, conductors in critical areas can be separated and dispersed on various layers, tight designs can be opened up and circuitry modification is achieved with a minimum of difficulties.

Another unique feature of multilayer wiring which can eliminate many cross-talk and interference problems is the possibility of incorporating shielding planes into the board. This possibility was not the prime reason for developing the multilayer concept, but it has proved to be quite a significant factor in present designs and approximately 90% of the boards now manufactured have one or more such planes incorporated into them. The shield or ground planes separate critical circuitry from interference from other signals going through the boards. Multilayers have been manufactured carrying AC and DC circuitry within the same board with no signal intermixes whatsoever. Since the ground layers are solid copper planes, they can also act as efficient heat sinks. Heat sink planes of any desired thickness can also be placed on the surface since they will not interfere with the circuitry which is encapsulated inside of the board. Therefore, depending on the requirements, the number of layers, the layer sequence,

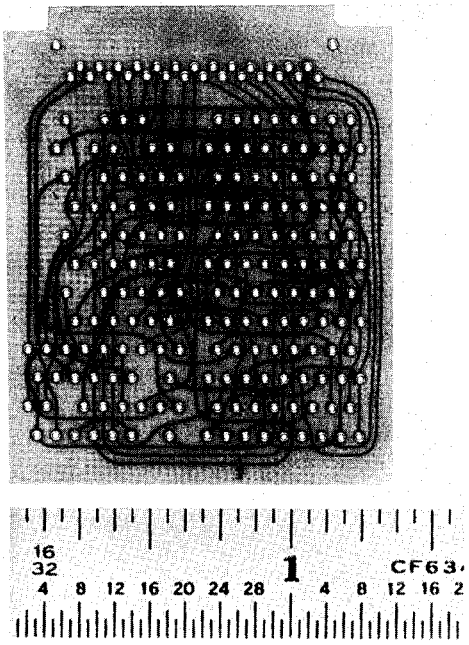

Fig. 4. Miniaturized three-layer Encapsulayer with holes located on 0.050 in. centers.

and the location of shields or heat sinks can be varied as required in the multilayer board. This provides a great deal of design flexibility and eliminates the need for complicated packaging techniques to achieve a desired component density. As pointed out previously, the size of the multilayer board, the number of modules or components to be interconnected, and the complexity of the circuitry are not critical design parameters of multilayer printed circuits. This means that the multilayer concept lends itself to a great many packaging requirements.

There are also certain limitations which must be borne in mind when working on a multilayer board design. The base material universally used for such boards is fiberglass-reinforced epoxy, which may present some problems in computers with clockrates over the 50-Mc range. Also, there is a limit on overall board thickness which is imposed by the plated-through hole process. As a general rule, the board should not be thicker than three diameters of the smallest plated-through hole. This does not appear to be a severe limitation since, to date, it has been possible to accommodate all the required circuit layers within the maximum permissible board thickness for a given design. Although the encapsulation of all conductors within the epoxy board has made possible line widths and spacings down to 0.010 in., there is still a limit to the terminal point density which can be achieved on multilayer boards.

If the holes are spaced on 0.100-in. and wider intervals, at least one conductor can be routed between two adjacent holes with the proper size pads around them. There are no serious design problems with multilayer boards since the required number of conductors can be placed one below another on subsequent layers and any desired interconnection density can be achieved.

If holes are spaced 0.075 in. apart, only one conductor can be routed between two adjacent holes. However this is a fairly tight spacing situation and should be avoided. No conductors can be routed between holes spaced on 0.050 in. centers. It is fortunate that presently available integrated circuitry packages, which have pins spaced from 0.075 to 0.050 in. apart, leave sufficient room underneath or outside of the module configuration for the routing of conductors.

In summary, a continued grid of holes on 0.100 in., and larger, center distances can be efficiently interconnected with multilayer boards. Clusters of holes on 0.075 or 0.050 in. centers can be interconnected with multilayers but not a continuous grid of holes with such spacing. Despite this limitation imposed by the present state of the art, packaging densities achieved by the use of multilayer printed boards are high and suffice for the majority of present day requirements.

To illustrate the possibilities of packaging density which can be achieved by multilayer boards with presently used integrated circuitry packages such as TO-5 cans with 8, 10, or 12 leads, TO-18 cans, and the TI type package with 10 leads on 0.050-in. centers, the following hypothetical limits were calculated:

1. *TO-5 Cans:* Leads are on the perimeter of a 0.200-in. circle. The minimum center-to-center spacing at which these modules can be spaced and still permit two 0.010-in. conductors to be placed between them is 0.300 in. However, since the actual size of TO-5 cans varies between 0.300 and 0.360 in., a realistic number for center-to-center location is 0.360 in. With this distribution, a density of 7.5 TO-5 cans per square inch can be achieved.

2. *TO-18 Cans:* These have a maximum diameter of 0.225 in. and therefore can be located on 0.300 in. center distances giving a density of 11 cans per square inch.

3. *TI Type Flat Package:* The minimum possible center-to-center distances at which these "bugs" can be located is 0.275 in. along the short dimension and 0.350 in. along the long dimension. With this density of packaging, 10 modules/in.^{2} can be placed on a multilayer board. Realistically, it is strongly advised to work with 0.300-in. spacing along the short dimension which allows one conductor between adjacent modules and yields a density of 9 modules/in.^{2} Multilayer boards interconnecting these modules can be stacked on a mother board at 0.100-in. intervals, which makes possible a packaging density of 90 TI type modules/in.^{3}

All the values given above are necessarily approximate and will depend upon board geometry. Also, these values are given for only the active area (i.e., the area where only modules and interconnecting circuitry are located) of the multilayer board. Approximately 10% should be added to the active area for framing and mounting purposes and another 10% for the input—output terminal areas. However, even with these reservations, it is apparent that

multilayers provide a very efficient method of interconnecting integrated circuit modules. In many instances the packaging density achieved by multilayer printed circuits is limited by the module geometry rather than the interconnecting circuitry. It should also be noted that weight per square inch of a six-layer multilayer board made of 0.006-in.-thick layers is approximately 2 g/in.

ARTWORK PREPARATION

Since multilayers usually interconnect standard size modules with repetitive pin locations, the layout of interconnections is a fairly mechanical operation. Therefore, it can be done either by draftsmen or can be subcontracted to board manufacturers, relieving the drafting staff of this burdensome task. There is one disadvantage to layout subcontracting; the circuit design engineer has less control over the routing of conductors with critical electrical requirements. This might be a problem when designing boards for high-frequency applications.

The preparation of the layout is a very interesting and tempting topological problem. A number of papers on the mathematical background for an optimum conductor routing and the use of computers for this purpose have been presented in past years. It appears that the number of variables and restrictions necessary for computer layout preparation is rather large and requires the services of complex installations. The programming is quite time-consuming and difficult. No information about successful multilayer layouts prepared by computers has been published to date and this task is still left in the hands of engineers and draftsmen. At the present, this appears to be the most efficient and economical layout procedure.

The manual task of transferring information from logic diagrams or wiring tables (which in many instances are ground out by computers) into conductor layouts for point-to-point interconnections is a drafting table chore. The procedure we generally use at Photocircuits is as follows:

A master template with all terminal points is prepared first. The scale of the template is such that it will be easy to work with and still provide the required accuracy of pad and conductor location after this preliminary master is reduced to a working master at 1 : 1 size. To prepare the circuitry layout for individual layers, a number of thin Mylar* sheets are placed over the terminal point master. The number of these sheets is equivalent to the expected number of layers and they are taped together in such a fashion that easy access to each layer is possible. This overlay package is then placed over a light table and layout work can start. It has been found that the most efficient method of layout preparation is to work with teams of two men per single board design. One man reads out the information about conductor originations and terminations from the diagram or the table. The other man concentrates on locating them on the master and routing conductors using regular pencil on the Mylar sheet overlays. Each is concentrating on a given segment of work and they are not distracted by going from the diagram to the layout and back. The routing of approximately 80% of the interconnections in a fairly complicated board goes rather fast, but the last 20% causes problems because a path must be cleared for them among the interconnections already laid out. This occasionally requires the transfer of existing connections from one layer to another to clear a path for the new ones. With this two-man method of operation a circuit layout for a board with eight layers and 2000 holes can be completed in 60 to 80 hr. This includes the check-out of the interconnections which is made after initial designs have been finished. It should be noted here that a single team has to work on one board from the start to the finish of the layout and this work cannot be subdivided among a number of draftsmen.

After the layout is completed and checked out, actual artwork preparation is started. It can be done by the conventional method of reproducing the master pad layout for each layer on Mylar, placing it over the pencil sketch which shows the interconnections and then taping the conductors in the same fashion as is done for regular boards. This part of the job can be distributed among many draftsmen and therefore lead time can be reduced. After the artwork is completed and the conductor widths and spacing are checked out, the matters are reduced

* Registered trademark of E. I. DuPont & Co.

by camera to 1 : 1 size and glass negatives made which will serve as tools for the production of the layers. The artwork operation usually goes somewhat faster than the circuit layout. For instance, the artwork preparation for the board described above would take approximately 50 hr plus about 10 hr of camera and touch-up time.

Photocircuits has developed a process and equipment which actually bypasses the laborious steps of artwork production. It is called the Master Circuit System and produces 1 : 1 negatives directly from pencil sketches. Since the information for pad locations is the same for all layers, this equipment achieves perfect layer-to-layer registration which is imperative for proper multilayer artwork. With this system, artwork preparation time is cut more than half and lead time is decreased still further.

The tolerances required on completed multilayer parts are so tight that the tolerances necessary for the manufacturing processes use all the available room and leave almost no allocation for any mistakes in the artwork. Ideally, the 1 : 1 glass masters should have the location of terminal areas, line widths, and spacings held within 0.001 in. from true. Therefore, the work on the enlarged artwork masters must be done with extreme care, utilizing the most accurate drafting equipment available. If this is not done, it is impossible to produce boards within the specified requirements.

It should be evident that very serious attention must be paid to artwork preparation and that the board design is a rather long process. Sufficient time must be allowed for those steps in order to ensure that satisfactory boards will be manufactured as the end result. Cutting-short and speeding-up these operations inadvertently leads to costly changes and redesigns later on and should be avoided.

PERFORMANCE OF MULTILAYER BOARDS

The reluctance observed in some quarters to switch to the multilayer concept is mostly caused by the impossibility of visual inspection of interconnections. Manufacturers of multilayers have been applying great effort to ensure that the boards have been properly constructed and will perform as required. To that end, numerous control points have been instituted during the manufacturing sequence to eliminate any potential rejects.

It should be pointed out that the multilayer printed circuits are prepackaged interconnection matrices and can be treated as separate components, which can be fully pretested to ensure that their performance is as expected and required. This testing is usually nondestructive and will not degrade the performance of the board for subsequent actual use. All manufactured boards are checked 100% before delivery for continuity and possible short circuits, and to make sure that the product is in compliance with specifications and electrical requirements.

The layer to plated-through hole joint is the most critical area in the whole concept of multilayers and opinions have been voiced that the reliability of these interconnections is not yet sufficiently high. It is true that in the earlier stages of multilayer printed circuit development

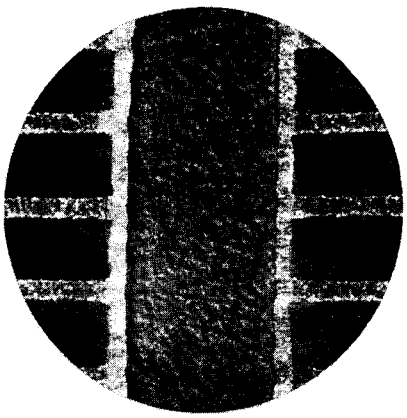

Fig. 5. Cross section of a plated-through hole in a six-layer Encapsulayer board. Approximate magnification 30 ×.

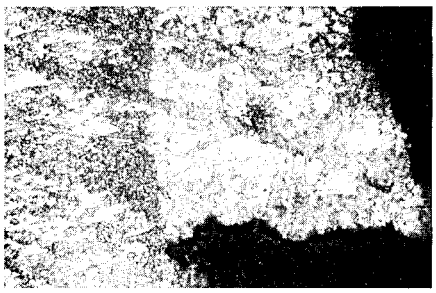

Fig. 6. Photomicrograph of the junction of a plated-through hole and a conductor on an internal layer. Approximate magnification 750 ×.

there were occasions when questionable joints were produced. This was due to smearing of plastic over the exposed copper in the hole when drilling conditions were not tightly controlled and occasionally generated excessive heat which melted epoxy during the operation. Since such occurrences could not be tolerated at all, extensive programs were initiated which led to exact control of drilling parameters to prevent overheating and a series of cleaning cycles of the drilled holes to ensure removal of all unwanted matter prior to plating.

But even before the drilling and cleaning methods were perfected, the incidence of poor connections was not extremely high. The results of early evaluations indicate that open circuits were experienced at a frequency of approximately 1 open hole per 20,000 holes. Also, in early stages of multilayer use, some resoldered holes opened after a heat-shock cycling, increasing the frequency of open holes to approximately 1 in 10,000. After process improvements were achieved in the last year or so, the results have been very encouraging. There has been no report of open circuits developing in recently manufactured boards and the number of interconnections tested and used is significantly over one million. To test the soundness of the joints, multilayer boards were subjected in our plant to various MIL-STD tests and then to plain nonstandard abuse, just to see what will break these interconnections. The plated-through joint did not break even after the boards were demolished and conductors broken through, which permits us to assert that if good joints are produced initially, they will not break open even under severe environmental conditions. To ensure that good layer to plated-through hole joints are being produced consistently, quality control check points have been established in the manufacturing sequence which keep close control over all processes and continuously sample the plated-through holes of production batches by microsection techniques.

To determine the MTBF of multilayer boards requires a very long program. This has been started, but meaningful results are not expected to be available until the program has passed the ten-month mark. It is also difficult to collect exact data about the performance of multilayer boards in systems which are in use. It is known that some systems completed over 2000 hr of bench testing. There are numerous systems which contain over 20,000 interconnections each that have been on test and in use for at least a year, but no exact values for joint-hours are available at the present time.

Highlights of the results of the more severe environmental tests to which multilayer boards have been subjected, either as individual boards or in a system, are given below. It is impossible in this space to present the full data, therefore, only a short description is given.

Tested multilayer boards have passed the following conditions without circuitry failures, delamination, or any other functional failure.

1. *Dip Soldering*
   Over 20-sec immersion in 500°F solder pot.
2. *Resoldering*
   Over 20 resolder cycles using a 37-W iron.
3. *Pull Tests*
   On hole diameters of 0.052 in., no hole has been pulled with less than 60 lb. The majority stood a 100-lb pull, at which point the wires broke.

4. *Shock*
   Sixty-five g's for 100 msec and 200 g for 1 msec in all six major directions.
5. *Vibration*
   Per MIL-STD 167 and MIL-E-5272, consisting of various cycling programs from 5 to 80 cps with amplitudes varying from 0.020 to 0.100 in., between 80 and 500 cps at 20 g's, and up to 2000 cps at 10 g's in all three axes.
6. *Storage*
   Ninety-six hours at 350°F and 96 hr at −80°F.
7. *Thermal Shock*
   Twenty cycles from 350°F to −80°F with half hours at each temperature and 1 min in between.
8. *Moisture Resistance*
   Ten cycles according to MIL-STD 202, Method 106, with minimum resistance of 100 m across 0.020-in. spacing horizontally and 0.007-in. vertically.
9. *Dielectric Withstanding Voltage*
   Fifteen-hundred volts for 0.030-in. spacing and 1000 V for 0.020-in. spacing between encapsulated conductors on internal layers.
10. *Pressure*
    Sixty-five psi and 0.169 mm Hg (200,000) ft.

We do not have any information about multilayer board performance under the salt spray, sand, and dust, and fungus requirements of military specifications. However, for those environments, the multilayer board is no different from a conventional two-sided board with plated-through holes and therefore should be able to pass these tests.

It should be noted that the environmental test results refer to multilayer printed boards manufactured with copper, nickel, gold plated-through holes. This has proved to be the most successful plating combination for use on multilayer boards. Nickel provides additional structural strength for the plated-through hole and has a good leveling effect for achieving a smoother hole. Many companies have reservations about the solderability of gold and prefer the use of solder as a finishing metal. The problem with solder is that its poor throwing power during plating precludes its use in small, deep holes and therefore it is not usable in a significant number of applications for multilayers. Experiments have been run with nickel-tin overplating with satisfactory results, but data are still insufficient to warrant full-fledged use of this plating technique. Also, some multilayer boards have been manufactured using copper, nickel, copper, solder plating.

The values given for resistance and dielectric withstanding voltage are for the circuitry on inner layers only, where the effects of moisture and outside environmental conditions are minimized. The performance of circuitry on outside surfaces is the same as on regular two-sided boards. It is strongly recommended that all circuit layers be encapsulated, thus providing a uniform and protected environment for all of the circuitry. Completely encapsulated circuitry also eliminates serious manufacturing and soldering problems created by dense packaging of conductors and holes and improves the tolerances which can be efficiently held.

In multilayer boards, copper conductors are etched from 0.0028-in. (2-oz) foil. This thickness has been selected to provide a larger area of contact between the conductors and plated-through holes. The boards can be made with thinner or thicker foils but the selected thickness was found adequate for the majority of current-carrying requirements of multilayers. The current-carrying capacity of conductors in multilayers is very close to the capacity of standard etched boards and existing guides and specifications can be used directly for determining the size of conductors.

Another aspect which is frequently mentioned is the capacitance between conductors. Actual results show that it is not very large and the amount of distributed capacitance was much less than expected in completed systems. For two parallel conductors on the same layer, capacitance is approximately 0.2 pF/in. at 0.010-in. spacing and 0.12 at 0.020-in. spacing. When conductors are one above another the capacitance is 0.005-in. vertical separation, 5 pF/in. for 0.020-in. conductors and 7 pF/in. for 0.030-in. conductors.

The possibility of changes and repairs on multilayer boards is a pertinent problem. It is impossible to repair a broken conductor trace inside the board. The faulty connection must be rewired on the outside of the board. Removal of components is not more difficult than with conventional boards, but the use of a high-wattage soldering iron should be avoided to prevent damage to the board and proper care must be exercised not to overheat the board or the hole. There is a problem, however, in the extraction of multipin modules from the boards. Specially shaped soldering irons which heat all the wires simultaneously have been successfully used. A sequential heating of pins and sucking out of the molten solder to free the wires has been used by a number of companies. Small solder pots designed to heat only the module areas are another approach. In any event, proper instructions and controls must be established for successful resoldering operations of multilayer boards.

Making changes of circuitry in completed multilayer boards is a rather cumbersome but not impossible task. It is preferable to have the multilayer boards manufactured only when the circuit design has been completely firmed up to minimize the number of changes after the boards are completed. However, working with prototypes which have been hand-wired and then switching to multilayer boards directly for production runs might lead to some difficulties since the electrical characteristics of the connections may be slightly changed. A recommended procedure for the adaptation of multilayer design would be to make and test out a limited number of prototype boards, determine their performance, incorporate the required changes into the already prepared artwork and then release the boards for the production run. With this sequence the lead time can be cut significantly, the cost of changes minimized and the same tooling which has been manufactured for prototype production is already available for the production run.

If, however, changes must be made on the completed board, the following procedure is recommended: first the module is removed, then the plated-through hole with the wrong connection is drilled out and an insulating sleeve is inserted into the hole. After the module is reinserted into the board, the required new interconnection is made by hand-wiring this isolated pin to any desired pin on the back of the panel.

ECONOMIC FACTORS

The economic aspect of electronic packaging methods, even the most advanced ones, are always pertinent. To evaluate the costs of multilayer boards, they must be considered together with other factors and the costs of the overall package. At this point it is rather difficult to present exact cost values for multilayer boards since the number of variables from design to design of these circuits varies significantly and only broad generalizations can be made.

Multilayer boards cost definitely more than regular two-sided printed circuit boards. This is caused by the nature of multilayer board manufacture which requires a long and tightly controlled process. The artwork preparation is also costly since a single board requires accurate masters for each layer. As a general rule, multilayer printed wiring boards cost approximately three times more than equivalent two-sided boards of the same size, number of holes, and ordered in the same quantities. If the total cost of the assembled board is taken into account, the ratio of this total cost to the cost of the board itself remains approximately the same since more expensive components and modules are being interconnected with multilayer boards.

Specific problems, such as the most economical size for the multilayer boards, should be analyzed in conjunction with the overall cost of the interconnections between the boards, supporting hardware, and the desired level of replacement. The question of the effect of an increase or decrease in the number of layers on the cost of the board is very often asked. Again, no direct answer can be given here since this problem is tied-in with the circuit complexity and the conductor density. In some cases, paradoxically enough, additional layers which enabled us to loosen up tight design areas made the multilayer boards actually less expensive. It should be borne in mind that for every increase in packaging density, a price must be paid. For instance, if the cost of multilayer boards of a given size with holes spaced on 0.100 in. centers is taken as a base, then a similar size board with hole spacings on 0.075 in. centers and tighter design will cost approximately 25% more. If the required density goes to the limit of the present

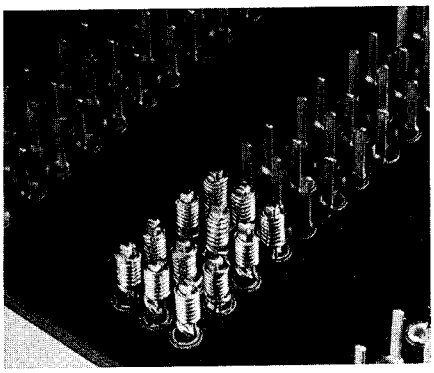

Fig. 7. Multilayer board with split, hollow pins for "Wire-Wrap" separable connections.

state of the art, i.e., to 0.050-in. spacing of holes and 0.010 in. conductor widths, the board will cost approximately 50% more than the base example.

In comparison with point-to-point interconnection methods, the cost of multilayer boards in small prototype quantities is usually close to the cost of the units made by other interconnection methods. But, for production quantities, especially when very complex circuitry is packaged, the multilayer concept does offer significant overall savings. Besides, many new methods of interconnection require setting up of new facilities, training personnel, special aids, etc., but multilayer boards are assembled using the facilities already available for the assembly of components onto regular printed circuits and no new skills must be developed. It should be noted also that the higher prototype costs of multilayer boards are usually offset by the fact that all artwork and tooling is immediately available for subsequent production runs.

Very frequently other packaging considerations or design requirements may outweigh the results based on pure cost analysis, but it is very important to include potential cost savings possible with multilayer boards when the selection of packaging methods is made.

NEW DEVELOPMENTS

The desire to extend the multilayer printed circuit concept into other interconnection methods, and not be limited to soldering only, prompted the investigations of various new schemes throughout the industry. Attempts to weld directly to printed circuit boards have been made by a number of companies and the work is still progressing toward developing some reliable means of doing this. However, there are a number of inherent problems involved in such an approach which make this operation rather difficult to control. Photocircuits Corporation has developed several unique techniques (patents applied for) which provide the possibility of connecting components or modules to multilayer boards either by "Wire-Wrap"* or by welding. In these methods, the need for direct welds to the board are bypassed.

One of the methods, to be used primarily for the connection of modules to multilayer boards using the "Wire-Wrap" pin technique, is as follows: Into plated-through holes, plated only with copper, split hollow pins are inserted which have a tab on top protruding over the board. This tab, depending upon the configuration, can be used to weld a wire which passes through the hole or can be wire-wrapped to a rectangular module pin going through the hole and mating with this tab (Sippican Corp. patent). The joint between the split pin and the plated-through hole can be achieved by one of two methods.

a. The pin of any acceptable metal is overplated on the surface with copper and then indium. At temperatures sufficiently low that the board material will not be damaged, indium has the ability to diffuse into and form an alloy with copper. Therefore, after insertion of the pin which exerts a radial pressure against the hole, the board is subjected to this indium diffusion temperature, the indium–copper alloy is formed and a continuous metallic joint is achieved

* Registered trademark of Gardner–Denver Co.

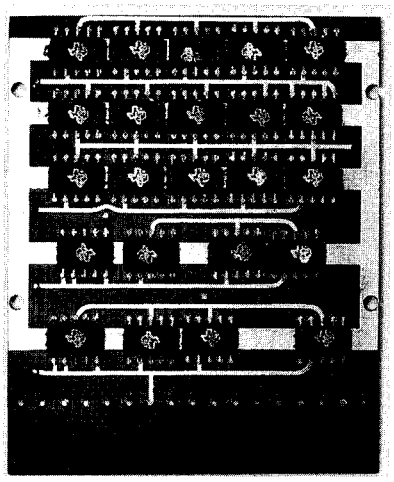

Fig. 8. Encapsulayer board with "Fusicon" pins for mounting of Texas Instruments "Semiconductor Networks" by resistance welding.

between the pin and the plated-through hole. This joint cannot be destroyed until a temperature of about 900°C is reached.

b. The pins and holes into which they will be inserted can be solder plated. After insertion of the pins, the solder is fused and connects the pin permanently to the board. This method certainly does not eliminate the solder joint and the additional interfaces of such type of joints, but it has found application in a number of companies.

One disadvantage of the above-described methods is that they do not lend themselves to a high degree of miniaturization. A sufficiently large hole must be provided for the pins or tabs. To this, the thickness of both the inserted split pin and plating in the hole must be added and then the pad around the hole. The minimum pin-to-pin spacing for which this interconnection method can be used is 0.125 in.

To provide multilayer boards with weldable terminations to which packages or components can be connected at spacings as low as 0.050 in., another proprietary method has been recently developed by our company. It is called "Fusicon" and is especially well adapted for the mounting of flat integrated circuit packages.

In this method, the copper plated-through holes which interconnect internal circuitry and are spaced on 0.050 in. centers are reamed out with a slight taper (approximately 0.0015 in./in.). After reaming the holes have a diameter of approximately 0.020 in. Tapered pins are

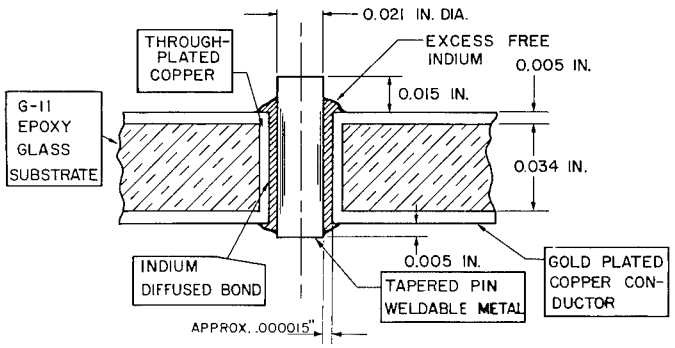

Fig. 9. Drawing shows cross section of "Fusicon" pin technique. The diffusion alloy is shown in exaggerated scale.

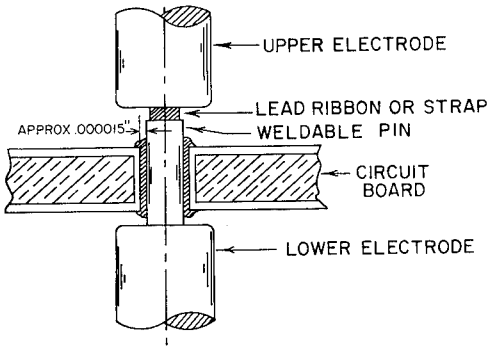

Fig. 10. Welding configuration used with "Fusicon" pins.

inserted which mate tightly with the reamed holes. The pins are made of carbon steel, which is an excellent welding material and are overplated with copper and indium. After insertion, the pins are cut off and ground to make the upper surfaces smooth and to keep the overall length of pins within a close tolerance. After this operation, the boards are subjected to indium diffusion temperature and the resulting indium–copper alloy bonds the pins permanently to the plated-through hole. The force necessary to pull a pin out of the plated-through hole after diffusion is over 50 lb (at which point the testing has been stopped).

The tabs of flat packages are placed over the pins and regular resistance welding is used with one electrode on the tab and the other underneath. The welds are easily controlled since the energy is going only through the pin, which always has the same dimensions. Therefore, the weld schedule, once established, will serve for welding the entire production run without need of any adjustments. The orientation of welds is always the same and, therefore, the movement of the board from point to point is always in the same plane. This simplifies the operation and suggests the possibility of automated assembly.

Many engineers frown upon the bending of the flat tabs coming out of integrated circuit packages. The "Fusicon" technique permits the welding of tabs in exactly the same plane as they are located on the package since the protrusion of the pin over the plane of the board can be adjusted to any desired height.

For a number of testing programs, gold-plated Kovar ribbons 0.003 × 0.010 in. and Nickel A ribbons 0.010 in. thick and 0.020 in. wide have been welded to the diffused pins in plated-through holes using Sippican Model 3 welder with number 16-M Head and Unitec

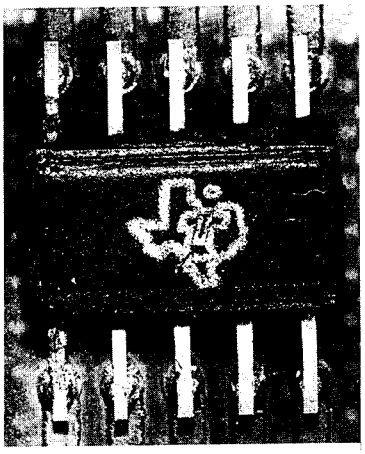

Fig. 11. Texas Instruments "Semiconductor Network" welded to "Fusicon" pins.

Model 1049-B welder with number 1032-B Head Electrodes used were RWMA alloy No. 2 with 0.040-in.-diameter tips. The pressure setting was $2\frac{1}{2}$ lb. For the Kovar tabs, the heat setting was $2\frac{1}{2}$ W-sec and for Nickel A, 3.0 W-sec. These test boards underwent a lengthy test program consisting of thermal storages up to 8 hr at $+175°C$ and 9.4 hr at $-65°C$. They were then thermal cycled between $-65°C$ and $+175°C$ for five cycles and, later in the program, for five more cycles between $-65°C$ and $+200°C$ with 30 min residence at each extreme. The vibration testing was done in several stages, the most severe being 10 *g*'s sine wave plus 20 *g*'s noise and later 20 *g*'s of sine wave only. The shock test was 200 *g*'s for 6.5 msec. There was no circuit breakdown during and after the testing and no degradation of joints was observed.

One important feature of this method is the possibility of removing defective integrated circuit packages and replacing them with new ones. On "Fusicon" boards, all mounted integrated circuits are easily accessible and can be removed by snipping the tabs or by pulling them off the pins. After removal, the top surface of the pin can be filed down and cleaned of the residue of the old weld, a new integrated circuit package put in place and rewelded back to the same pins. Five such rewelds to the same pins have been achieved without any difficulty and with a minimum of changes in the weld schedule. Since the welding operation with this method of packaging is simple and uses standard resistance welding equipment, the new technique opens the possibility of easy maintenance of the boards even under field conditions.

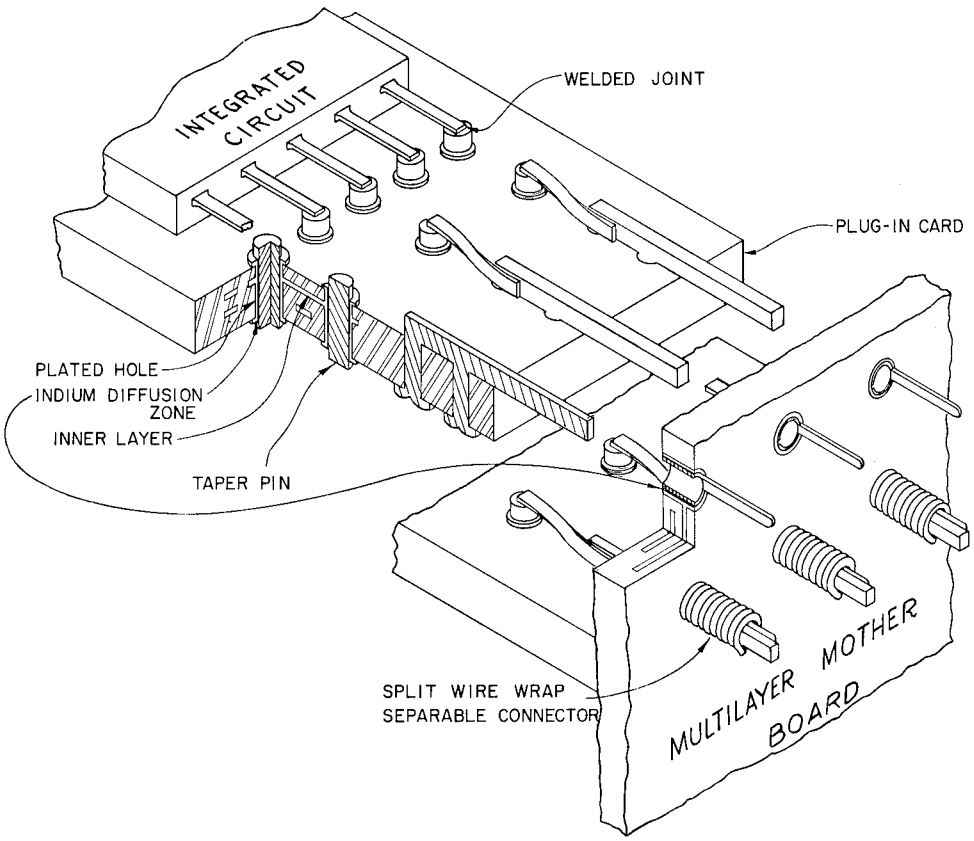

Fig. 12. One method of interconnecting modules containing integrated circuits mounted on a "Fusicon" multilayer board is by using a multilayer "mother" board and separable "Wire-Wrap" connections.

For efficient packaging of integrated circuits, it is important to achieve the maximum possible density of such circuits on a single card while still providing adequate space for interconnecting circuitry. In our plant, we have worked out layouts for the efficient placement of integrated circuits and are now trying to standardize this layout. This standardization permits us to have all tooling prepared in advance and decreases the time and cost of manufacturing "Fusicon" boards. We have standard tooling for TI packages and have prepared layouts, which permit a maximum of 210 of this type of integrated circuit to be placed in an area of 5 by 5 in. These are maximum dimensions and naturally the boards can be made smaller, or some areas left blank, depending upon the design requirements. As long as the location of the integrated circuit packages conforms to the standard pattern, all tooling and master templates are readily available.

The "Fusicon" pin concept is not limited to only the interconnection of flat integrated circuit packages, but has been extended to the interconnection of other integrated circuit packages or individual components. For the latter applications, the pins are not cut close to the surface of the board but are permitted to protrude on one side $\frac{1}{8}$ to $\frac{1}{4}$ in. above the plane of the board. In the vicinity of the plated-through hole with the diffused pin, another small hole is drilled just large enough to permit the component leads to go through. This lead is then bent and a cross-weld is made from the pin. With this technique both welding tips are positioned on the same side of the board which is necessary when the geometry of the component does not permit placing the tips on opposite sides of the board.

Input and output connections from a "Fusicon" board with components or integrated circuits can be made with special "Wire-Wrap" terminals inserted directly into the board or with any other conventional printed circuit terminations.

With the new approaches discussed in this paper, it is now possible to use multilayer boards for almost any type of interconnection requirement. The multilayer concept has become a highly versatile and adaptable packaging technique.

FUTURE DEVELOPMENTS

It appears that multilayer printed wiring has gained fairly wide acceptance in the three years it has been on the market. Most major military electronic systems being presently designed for airborne and ground support applications have some multilayer boards incorporated into them.

Further growth of multilayer use is definitely coupled with the increased usage of integrated circuits and the continuing industry trend toward miniaturization of electronic apparatus. It has been estimated that by 1970 over 25% of the total printed circuit market will be devoted to multilayer boards. On the technical side, there have been demands voiced for a further increase in the density of terminal points, down to 0.025-in. and 0.015-in. spacing. It is rather doubtful that this could be achieved in the near future with the present state-of-the-art. There is a good possibility that these demands are not realistic since separable modules must be handled and manipulated by technicians and there is a limit to human dexterity.

In any case, for the present and the immediate future, the multilayer printed circuit offers the design or packaging engineer a very versatile and compact interconnection technique. It is fully adequate for 0.050-in. spacing, has a large volume production capability, offers significant economic advantages through exact reproducibility and reduced wiring time and allows a high density of circuitry and terminal points. Just as the transistor was a vital factor in the increased use of conventional printed circuits, the integrated circuit will, in all probability, be the major factor in the increased use of multilayer circuits.

8076

The Role of Standards in Electronic Packaging

ROBERT GERLACH
AC Spark Plug Division, General Motors Corporation, Milwaukee, Wisconsin

The process whereby an operating method evolves into an industry standard is discussed in this paper—a standard being taken as a model or criterion established by authority, custom, or general consent. The common electrical standards, such as the volt, the ampere, and the ohm, are cited as those of which all are aware and appreciative, and the more highly complex extension of similar standardization into recent electronic developments is analyzed. The paper projects the process of standardization into the future, forecasting that many of today's revolutionary developments will be tomorrow's accepted standards.

INTRODUCTION

A STANDARD IS defined as a model or criterion which is established by authority, custom, or general consent.

Perhaps the best measure of the value of standards is to imagine for a moment the complete chaos that would result if no standards existed. We could not be here in Colorado today, because we came here by some standard means of conveyance, such as an automobile. It would be difficult, if not impossible, to buy anything, because there would be no basis for a monetary exchange. There would also be no customary apparel, so one of us might be dressed in a long cloak and ten-gallon hat.

These are extremes, yes, but only a slight departure from standards can be striking in its results. The beatnik is nonstandard only in relatively few ways, and yet he seems quite strange to many of us.

The role of standards is to provide a proven accepted method for handling all tasks not requiring a unique approach. Standards prevent useless duplication of effort and free the individual for creative assignments.

Most of you are directly responsible for, and all of you are interested in, the design and packaging of electronic products. In the field of electronics the volt, ohm, ampere, farad, and henry are basic to our work. The value of these building blocks is accepted as being self-evident. As we proceed farther down the path of standardization we find the origin, selection, and use of standards becoming more complex and their value, while just as great, becoming more indeterminate.

EVOLUTION OF A STANDARD

When a new process or material is developed there seems to be no time to evaluate and record the nature of the development. The designer is so busy with his experiments that he feels it would be a waste of time to fully describe what he has discovered.

Some time later the opposite extreme is reached. Upon learning of the advantages of the method or application, users are carried away with a creative spirit and want to standardize, immediately and exclusively, on the sparkling discovery. Considerable restraint must be exercised during this period so that a careful, accurate, and unbiased evaluation can be made.

Occasionally a major breakthrough occurs, but in a great majority of cases the new development proceeds in a quiet manner to take its rightful place among existing methods.

Some new developments never make the grade, but fall victim to competing actions. As an example, encapsulating compound A appears to have properties superior to existing formulations. About the same time compound B appears on the scene. Compound B has properties very similar to A, but costs only one-fourth as much. Under these circumstances, it is probable that compound A will pass into oblivion without having attained any status.

A standard is evolved from research and development to its final form by an orderly, careful evaluation. The standard is then published so it is available to all for their use.

PROPER APPLICATION OF STANDARDS

Like other useful things, standards have limitations. There are cases when they may be misapplied. A case in point is nameplates. If your customer has no preference and a standard nameplate is available, there is no problem. However, the customer may desire that certain information be included and may have a preference for a certain configuration. There is a cliche which applies here, "The customer is always right." While this quotation may not be 100% true, to furnish a customer equipment with an unexpected type of nameplate is to invite a complaint. Usually the results are that a special nameplate is supplied anyway, often on a rush basis.

A misapplication occurs when extensive standardization is attempted on an unstable base, such as small and variable quantities. An organization which is primarily a job shop must maintain its flexibility and therefore limit its stabilized practices to those that are common to the various jobs or products. Conversely, standardization is most easily applied when a relatively large number of similar units are to be made.

A common difficulty in the composing of standards is a tendency to be all-inclusive. A person discovering a precept is apt to try to give it a wide scope. The ambiguity of a standard is a function of the width of the scope. The scope must be limited to a particular situation, and then only when the basic principles are known and clear.

An error in the opposite direction occurs when one hesitates to adopt any standards because the perfect situation or application does not exist. One must not waste time and energy on insignificant details but rather make an extraction of value from information available.

The foregoing limitations are not to be construed to mean that suggestions for the use of well-established materials and processes should not be made during contract negotiations. The customer is always interested in a lower-priced contract. If the contractor can show savings in facilities and employee retraining that will result if existing standard methods are used, adoption of the contractor's standards are likely. In fact, acceptance of the whole contract is more probable.

STANDARDS AND THE INDIVIDUAL

There are those who theorize that standardization would stifle originality on the part of the individual. We who are in standards work do not subscribe to this theory. We hope new developments will arrive in a never-ending stream and at an accelerating rate, because we know that the latest developments of today are the standards of tomorrow.

You are called upon to create circuits and assemblies that will perform complex tasks, for long periods of time under adverse conditions. Such creativity demands that you utilize your effort and time efficiently, and that you concentrate only on those problems and those activities which warrant your attention. Some tasks can be relegated to routine since they have been previously done. It is highly advantageous to draw upon experience to handle your routine tasks, conserving the balance of effort and time to solve those problems which are unique. This experience is recorded for your use in the form of tables, charts, empirical data, mathematical derivations, specifications, and other standards publications.

Consider, for example, that you are a person responsible for electronics packaging and need a piece of ordinary hook-up wire in your assembly. There are literally thousands of wires that are available. Probably a hundred of them would be satisfactory for the application.

One way of selecting this piece of wire is to blindly specify a type. A far better way is to specify a type which is on your stock room shelf, a material which has reams of data supporting its quality, and scores of successful applications to instill confidence in its use. If you have a material standards department, you can obtain its services in the selection of the wire. Selection by one of the latter will permit you to rest assured that you will not be haunted at a future time with loss of performance and reliability. Moreover, the simple expedient described here will result in thousands of dollars of savings in procurement effort and inventory control.

Another example which follows the proper selection of wire is the identification of that wire. Again there are many satisfactory methods of wire identification, but the best is the one which your manufacturing group is prepared to do reliably and economically. This is another simple way to save dollars.

COMPANY STANDARDS

There are two general classifications of company standards, managerial and technical. Managerial standards are financial and procedural in nature. They are highly important from an economics standpoint. Technical standards are physical, electrical, or chemical in nature and are of direct interest to the people in this symposium.

Some of the fields that lend themselves to technical standardization are:

a. Dimensions, including complete and statistical interchangeability.
b. Tolerances on measurements of an electrical, mechanical, or chemical nature.
c. Materials.
d. Purchased parts.
e. Assembly techniques.
f. Quality and workmanship.

The foregoing are general in nature. More specific subjects for standardization in electronic packaging are:

a. Potting and encapsulating compounds.
b. Wire and wiring.
c. Electronic and electrical components.
d. Structural components.
e. Assembly techniques.
f. Nomenclature.

It must be emphasized that many of the foregoing are extensively covered in industry standards and in military standards. The company standards program utilizes these standards whenever practical, since this takes advantage of the following:

a. The broad coverage of research and ideas that industry and the military can offer.
b. Interchangeability of the company standards with those used throughout the industry.

One of the duties of a company standards program is to obtain alternate sources of supply or to recommend an item which has more than one supplier. It is invariably advantageous to have more than one source of supply for a part or material. A single source is often a precarious one which can be lost because of fire, flood, strike, or other causes. When the supply is lost, a substitute vendor or a substitute material is sought under panic conditions. This panic usually leads to undesirable compromises.

Another feature of company standards work is the storage of and the publication of information. In each program or project there are at least a few valuable designs, methods, and ideas which are worth preserving. However, unless an effort is made to record the ideas, they are lost when the project is closed out. A logical group to record the salient points of a project is the one composed of the people of that project, but the best custodian of such information is a standards group.

Some of the more fortunate and better-organized standards groups are the possessors of extensive files and either control or have access to a technical library. All departments of a

plant benefit from this source of information. Often just a telephone call to the standards department will answer a difficult question.

One of the greatest economic values of standards lies in inventory control. An otherwise profitable business may find much of its working capital tied up in inventory. In order to make this capital more fluid and at the same time ensure an adequate supply of raw materials and parts, a company attempts to purchase and stock its supplies in an orderly manner.

Suitable inventory control, however, cannot begin until the unnecessary variety and duplication of stocked items has been reduced. The reduced standardized parts and materials allow those responsible for stock control to gather data. These data are used to establish one of the commonly used techniques for providing an adequate but not excessive inventory.

Proper inventory control, then, is made feasible by reduction of duplication and unnecessary variety. Elimination of duplication is of obvious advantage and requires only that an effort be made to pinpoint the duplication. What constitutes unnecessary variety, however, is not so easy to determine. Factors such as economic sizes or ratings, provision for spare parts, and custom all enter into the selection of the variety of an item. When these factors are not present, or are present to a limited degree, a method known as preferred numbers is useful. Use of this method leads to an orderly expansion or contraction of a line of items.

The system of preferred numbers is based upon the general rule that in smaller sizes items must be closely spaced, whereas in the larger sizes they are widely spaced. This leads to a geometric progression or logarithmic basis for size or rating selection. An example will illustrate the method.

Electric Light Bulb Selection

Preferred No.	10	16	25	40	63		100
Actual Size	10 W	15 W	25 W	40 W	60 W	(75 W)	100 W

Note that each preferred number is approximately 1.6 times its predecessor. This is called the "5" series since there are five increments from 10 to 100, or in any other logarithmic cycle.

The actual available sizes in the example follow the preferred numbers quite closely with the exception of the 75-W lamp. The 75-W size is somewhat redundant, in that either a 60 or 100 W can substitute adequately. The 75-W size would not be stocked.

A similar arrangement could be made in the next logarithmic cycle, from 100 to 1000 W.

If the 5 series has increments that are too coarse for a given selection, the 10 series or 20 series may be employed. Finer series are available, but are of diminishing value since they permit an exceedingly large variety.

For reference purposes, Table I shows the 5, 10, and 20 series of preferred numbers. Preferred numbers between 1 and 10 are obtained by dividing the chart numbers by 10. Preferred numbers between 100 and 1000 are obtained by multiplying by 10.

Elimination of unnecessary variety leads to purchases of larger quantities of those remaining. Purchase of larger quantities permits taking advantage of quantity price differentials.

Every organization has a standards program, either formal or informal. Some companies standardize their products without an awareness of this activity. The most effective programs, however, are those that are organized and properly directed. The responsibility for a formal program of standardization is usually vested in a standards group whose functions include:

a. Furnishing information concerning reliable parts, materials, and techniques.
b. Assisting in the search for suitable sources of supply.
c. Evaluation of new developments.
d. Retaining the experiences of existing programs so that the same painstaking effort need not be repeated on the next program.
e. Reduction of unnecessary variety.

Companies that have evaluated their programs will often report savings ratios of 5 to 1 or greater. That is, each dollar invested in standards work produces a five dollar return. In addition, the improvements in reliability, quality, and performance are of considerable value.

TABLE I

Preferred Numbers (10 to 100)

5 Series	10 Series	20 Series
10	10	10
		11.2
	12.5	12.5
		14
16	16	16
		18
	20	20
		22.4
25	25	25
		28
	31.5	31.5
		35.5
40	40	40
		45
	50	50
		56
63	63	63
		71
	80	80
		90
100	100	100

STANDARDS AND THE NATION

Government agencies, particularly the military, procure great quantities and varieties of material. The Military have long recognized the need for established practices. Most military contracts call for systems built entirely of "standard" parts and materials. It is true that considerable leeway is allowed in the interpretation of the term "standard" but the intent is clear. Federal procurement agencies face a monumental task today in preventing duplicated procurement. For example, it is possible for the same transistor to be stocked under many different part numbers. This is obviously undesirable.

The role of standards in federal procurement is apparent. Use of standard nomenclature and standard parts will help a great deal in avoiding useless duplication.

INTERNATIONAL STANDARDS

Electronic packaging people of all countries who are attending this international symposium have a direct interest in international standards. International standards have the most potential value, but at the same time are the most difficult to obtain and apply.

Some progress has been made, and will continue to be made, by societies interested in international standards. Prominent societies actively engaged in international standards are the International Organization for Standardization (ISO) and the International Electrotechnical Commission (IEC). Member societies of the American Standards Association (ASA) furnish committees to the ISO. The fact that the task of obtaining international cooperation is formidable should not cause us to lose interest in a most worthwhile goal.

CASE HISTORIES

Let us examine what some firms are accomplishing at the present time. An electronics equipment manufacturer commenting on its resistor standardization program says, "The main points contributing to the program are:

a. Reduction of the number of body sizes
b. Reduction in variety
c. Limiting of resistance values to definite steps

The annual saving resulting from this program is estimated to be approximately $37,000."

Another organization reports, "Our industry has a great interest in interchangeability . . . . Interchangeability permits the use of multiple sources of supply in design and manufacture, making savings possible by avoiding changing construction if a change of source of components is necessary."

An aluminum-producing company states, "Important dollar savings are realized through the activities of our engineering standards group . . . . The following are a few examples . . . . We save about $325,000 a year through central manufacture and warehousing . . . . The results of this program include less work in purchasing, receiving, and storekeeping . . . . It is impossible to attach a dollar price to human safety, but the direct accident costs to the company as a result of safety standards has been reduced by $500,000 over a period of five years."

THE FUTURE

One of the greatest challenges facing all of you here today is the furnishing of a product which has both quality and low cost. This challenge must be met. Whatever other means you may use, standards will certainly play a vital role in meeting this challenge.

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Thin-Film Logic Units

R. W. BERRY, E. H. MAYER, E. E. MULLER,
H. J. SCAGNELLI, AND K. E. STIEFEL
Bell Telephone Laboratories, Incorporated, Whippany, New Jersey

This paper discusses the capability of tantalum thin-film integrated circuits, as demonstrated in the design of a twenty-four bit direct-coupled transistor logic arithmetic unit, containing approximately 3100 transistors and 4600 resistors. The unit is described in detail, and the method of sputtering tantalum nitride circuits onto substrates, and of bonding dual transistor gates to each substrate, is discussed at length. Test results and performance data are given, as are comparisons with existing assemblies, showing thin-film units to be competitive in cost with conventional units, and to possess increased reliability.

INTRODUCTION

THIS PAPER REPORTS the exploratory development of a digital data processing logic unit. The construction employs tantalum deposited in very thin films upon glass substrates. The deposition pattern and the resistivity of the tantalum are chosen to form the circuit resistance elements. Gold films overlayed onto other tantalum areas form the conductors. Transistors, packaged in thin pancakelike enclosures with flat ribbon leads, are soldered directly to the gold films on the glass substrate [1-10].

Thin-film circuits of this type are attractive for a number of reasons. Obvious advantages are the size and weight reductions possible with this technique in comparison to more conventional techniques. The reduced size also reduces certain electrical limitations of more bulky circuitry and allows performance at a higher speed. Thin films, in addition, offer potentially significant reductions in cost through continuous fabrication and assembly and an expected improvement in reliability [11]. The tantalum films also appear suitable for forming capacitors using tantalum oxide as the dielectric. Prototype trials of such capacitors are being conducted in the Bell System.

To provide a basis for evaluation of the potential and the problems of tantalum thin-film circuitry, an arithmetic unit of a digital data processor was chosen as a developmental project. A nearly completed, compact, wire-wrapped data processor was available for comparison (see Fig. 1), and the thin-film unit was designed to be identical in function.

A thin-film arithmetic unit, identical in function to eight bits of the wire-wrapped data processor arithmetic unit, was fabricated and tested. The other sixteen bits of the arithmetic unit would be merely a repetition of the first eight bits. This paper describes the thin-film arithmetic unit in terms of its circuit design, the basic substrate topology, the substrate construction and thin-film processing, the integrated cable connector, and the performance of an eight-bit thin-film arithmetic unit.

CIRCUIT DESIGN

The design of the thin-film logic circuitry is governed both by the electrical performance objectives and by the restrictions imposed by the thin-film fabrication techniques. The electrical

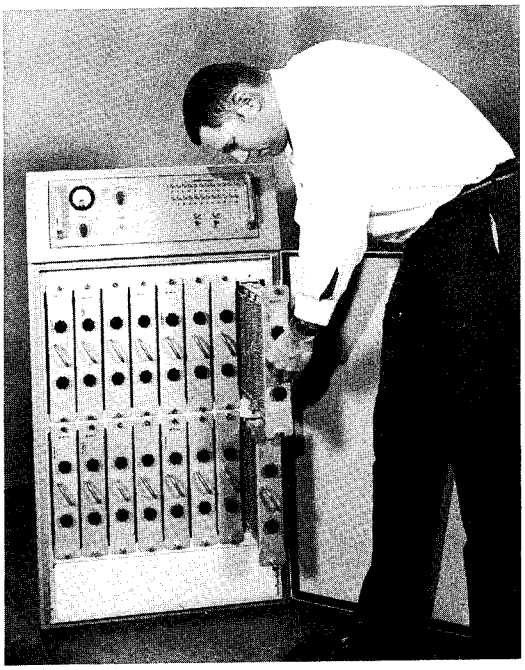

Fig. 1. Wire-wrapped model of the data processing unit.

performance objectives include the following: (1) The nodal power dissipation is to be held to a minimum while the logic speed plus propagation delay is maintained below about 50 nsec for the worst case, consistent with the needs of a reasonably high-speed data processor. (2) Logic flexibility is to be maintained through variable interconnections made at the slide or multinode level. (3) The thin-film Data Processing Unit (DPU) is to have interfaces compatible with those of the wire-wrapped version, facilitating direct interchange of like units for performance comparisons.

Thin-film fabrication imposes constraints not present with more conventional construction if the advantages of the process are to be realized. The number of nondeposited components, such as transistors, diodes, and inductors, must be kept to a minimum, both to restrict the number of soldered connections and to hold down size and cost. The number of power supplies should be limited as each power bus constitutes a barrier to signal paths in planar circuit layout that can be difficult to bridge. The range of capacitor values is restricted by size and yield difficulties associated with the deposition process. Precision of the deposited resistors is limited by cost considerations. Finally, dense packaging requires consideration of power and temperature levels.

The foregoing considerations have resulted in a simple NOR-gate design, utilizing direct-coupled transistor logic (dctl) and powered from a single 2.6-V $\pm$ 5% supply (see Fig. 2). Allowable fan-in is 4 and fan-out 3. Although the speed objective can be met without resort to dummy loading of low fan-out nodes to control storage times, dummy loading was used for this unit. Average propagation times of less than 25 nsec were achieved with nodal dissipations of 3 mW. Resistor values used are 560 and 910 Ω. Initial resistance tolerances of $\pm 5\%$ are adequate, since the aging and temperature variations are insignificant. Capacitors are not needed in the arithmetic unit, but deposited types seem feasible for the majority of applications in other logic areas.

The transistor chosen is a developmental silicon planar epitaxial wafer with low storage times and collector saturation voltages, and an f_t of over 150 Mc at 1 mA collector current (see Table I). The base-emitter voltage $V_{BE(sat)}$ is controlled to a tight 50-mV range of particular

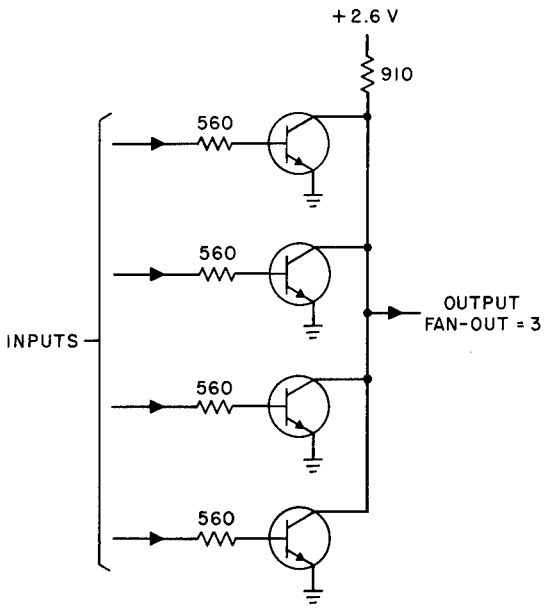

Fig. 2. Dctl NOR gate.

importance to dctl logic. These wafers are packaged two per can in a miniature pancake T051-type enclosure with four leads (Fig. 3). Both emitters, like both collectors, are paralleled and have a common lead.

The next step is to shape the overall logic into a suitable pattern for thin-film fabrication. Both electrical and packaging considerations are significant. For economy of manufacture, the logic breakdown should minimize the number of different slide codes. To minimize interconnections between slides, the logic within each slide should have some close functional relationship requiring few inputs and outputs. Where possible, assemblies of slides should also be identical, further reducing the cost through greater use of identical assemblies and components.

The arithmetic unit was chosen for initial consideration because its logic design was most advanced and least subject to change. It represents approximately 30% of the total components in the DPU. The distribution of the remaining components is shown in Fig. 4.

The resultant logic layout for the entire arithmetic unit logic uses only four different slide codes, one each of the four codes constituting one bit of logic. An average slide contains

TABLE I

Characteristics of the Dual Transistor

(Approximate Values for Each Transistor)

BV_{CEO}, minimum	10 V
$V_{CE(sat)}$, maximum	0.25 V
$V_{BE(sat)}$	0.65 to 0.70 V
h_{FE}	25 to 100
f_t minimum at 1 mA	150 Mc
t_s maximum	25 nsec

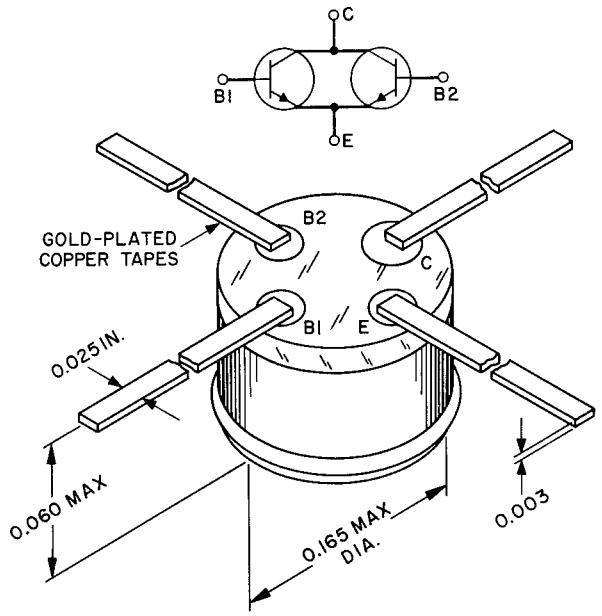

Fig. 3. Dual-transistor enclosure.

14 NOR gates with 18 signal input and output leads. The logic is also tailored so that 8-slide (2-bit) groupings will be identical for packaging considerations.

Although the arithmetic unit contains a high degree of repetition of basic slides and packages, the logic itself is varied. Diversity is achieved through the interconnection of identical slides and packages in different ways depending upon their logical function. To allow this flexibility the slides must have a component count somewhat greater than the minimum necessary if each were allowed to be different. The cost of having a limited number of slide codes in the arithmetic unit is, therefore, a certain number of unused components—in particular, approximately 5% additional transistors and resistors.

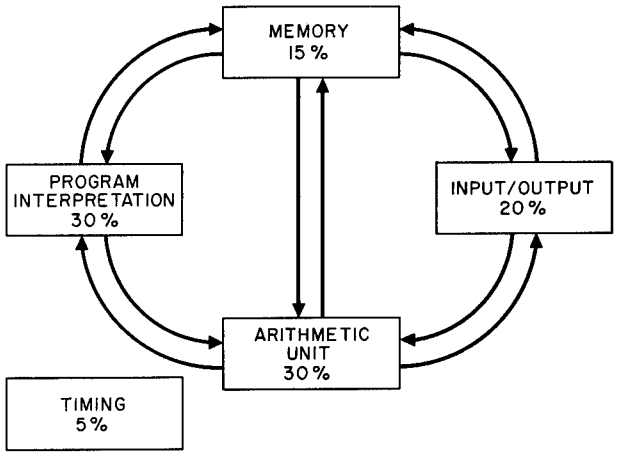

Fig. 4. Data processing unit, block diagram with percentage of total components.

LOGIC TOPOLOGY

The optimum basic topology for thin-film electronic systems must take into consideration not only the system design requirements but also the physical placement and juxtaposition of elements as well as the topological layout on the thin-film substrate. Some additional considerations for overall electromechanical circuit design include the means for internal and external connections; the size and location of power, ground, and signal circuits; power dissipation; in-process monitoring of components; component placement from an operational and fabrication viewpoint; and compatibility and environmental stability of materials and processes [12].

The thin-film integrated circuit is a hybrid that employs an insulating substrate onto which are placed separately fabricated, hermetically sealed, reliable elements (transistors, diodes, and so forth). The topology of the basic NOR gate used for the substrates of the arithmetic unit is illustrated in Fig. 5. The transistor element and enclosure are those previously shown in Fig. 3. A dual-transistor package is placed onto an area that is approximately 0.46 in. square. This modularly spaced pattern arrangement is designed especially to accommodate the solder-coated 0.025-in.-wide by 0.003-in.-thick leads that extend radially from the bottom of the planar transistor. The land areas to which the leads are solder-bonded, without the use of additional solder, are intentionally made large to be compatible with a $\pm 5°$ variation in transistor orientation and to provide adequate access for in-process fabrication or transistor replacement. The transistor body is electrically insulated from the substrate, as well as mechanically bonded to it, by means of a plastic disc that is precoated on both sides with a noncorrosive, pressure-sensitive adhesive.

Signal, power, and ground leads are all a minimum of 0.020 in. wide. Their possible arrangements and placement are illustrated by the five vertical and five horizontal paths shown in Fig. 5. A maximum of three of the five possible paths can be located beneath the transistor.

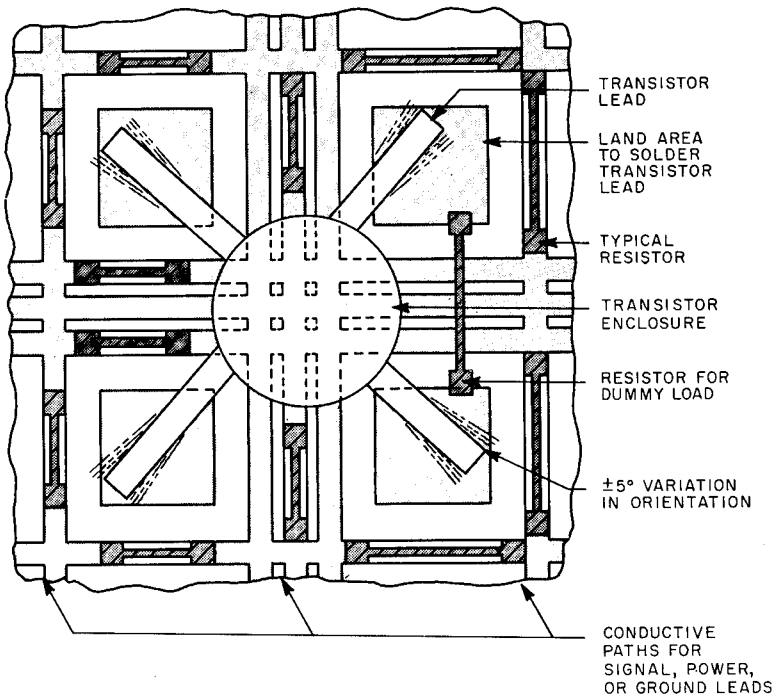

Fig. 5. Basic NOR-gate topology.

The arrangement for all possible resistor locations is indicated. All resistors have a straight-line design to simplify mask and pattern fabrication; the size of the resistor tab is kept approximately the width of the signal path to facilitate in-process monitoring and fabrication. To allow inspection after assembly, no passive elements are placed beneath the transistor. All base resistors are placed close to the transistor leads to satisfy electrical requirements. With this basic pattern, crossover (multilayering) of film passive elements and signal, power, and ground leads has in general been avoided. Accordingly, there are no interlayer feedback effects and no increase in the number of different metallic interfaces at the points of intraconnection. These steps taken to simplify the fabrication of the substrates also increase their potential reliability and decrease their cost.

CIRCUIT TOPOLOGY

The film circuit topology is influenced by the following factors:

1. The necessity to achieve a ratio of width to length that would provide for an adequate number of basic logic patterns for all slide codes; permit access to all logic patterns, even those in the center of the array; and be compatible with the arrangement of logic, signal, power, and ground circuits across the slide. An aspect ratio of 3 by 6 was chosen to meet these requirements.
2. The requirement that all passive elements with all their interconnections and terminations be made from a single deposition of tantalum so as to minimize cost and increase reliability.
3. The maximum area over which a tantalum film can be processed as a unit without special fabrication techniques being employed.
4. The intent to avoid crossovers and feed-through holes.
5. The need to place the circuit intraconnection burden within the thin-film circuit panel and thereby minimize the interconnections between (external to) the circuit panels.
6. The number of terminations permissible on the edge of the substrate.
7. The size and cost of the throw-away package.
8. The necessity for a satisfactory packaging density.
9. The requirement that it be possible to fabricate the remaining logic portions of an entire data processor with these same techniques.
10. Electrical design criteria such as requirements for multiple low-impedance ground paths, dummy loads, and so forth.

The aspect ratio must provide access to numerous grounds, supply voltages, and external connections. It is also necessary to avoid long feedback signal and power leads that could circumscribe and trap logic located at the center of the slide. A satisfactory aspect ratio will do much to overcome this natural constraint of thin-film circuits.

A typical thin-film substrate design is shown in Fig. 6. The glass substrate measures 1.7 in. by 3 in. by 0.060 in. thick. Each substrate contains a maximum of 36 transistors (18 dual-transistor packages) and associated elements. The basic pattern (Fig. 5) provides two vertical and two horizontal 0.020-in.-wide intracircuit conductors on 0.020 in. spacing between each row and column of the 18 dual-transistor packages. One additional horizontal and vertical intracircuit conductor is provided at the perimeter of each substrate. As indicated in Fig. 6, each column and row has a maximum of three additional leads. Seventeen horizontal conductors in seven rows and 32 vertical conductors in 13 columns are available on the 3 by 6 array of basic patterns on each circuit substrate. These conductive paths can be joined or broken at any point. To further facilitate intraconnections, conductors can be deposited onto the back of the substrate. The connections from front conductive paths to those on the back are made by horseshoe-shaped solder-coated beryllium copper clips.

Twenty-nine deposited conductor lands spaced on 0.100-in. centers are located at the lower edge of the substrate. Signal, power, and ground intraconnections all terminate on these lands. All interconnections are placed at one edge of the substrate to facilitate electrical test and inspection of any one slide or a group of slides prior to their being bonded or encapsulated into a module. The printed-wire connector used to test slides is shown in Fig. 7. The substrate

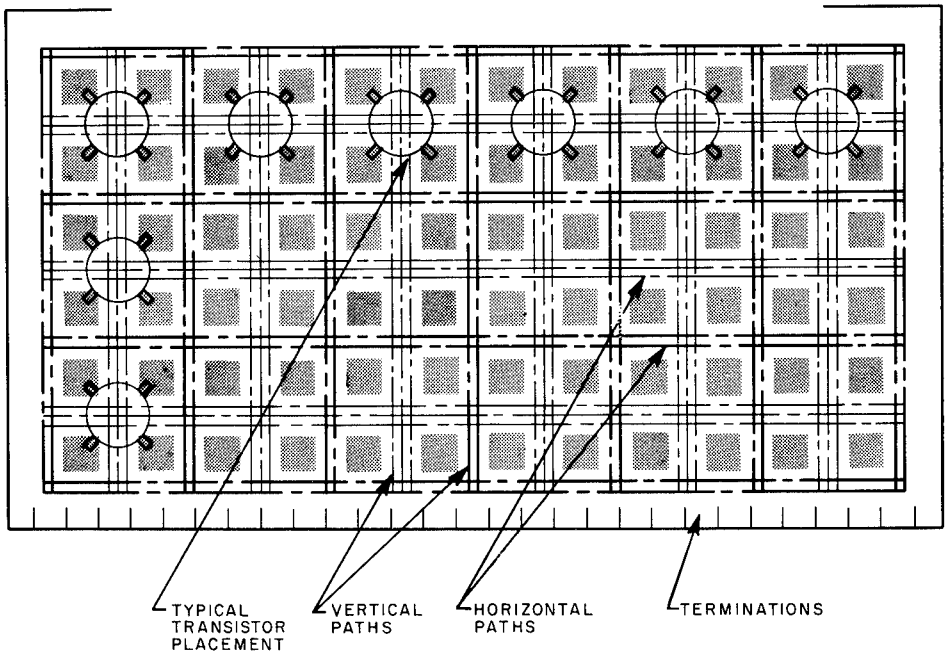

Fig. 6. Circuit topology.

is made 0.060 in. thick so that it will be compatible with this connector. Future substrates will be thinner.

MASTER LAYOUT AND THE PHOTOGRAPHIC MASKS

The designer's layout is used as a pattern for cutting a master for photography. This practice is more akin to engraving than to drafting since not only must the representation be accurate, but the dimensions of this layout will, in reduced form, be the actual dimensions of the resistive paths and thereby ultimately influence circuit tolerances. The masters are "cut"

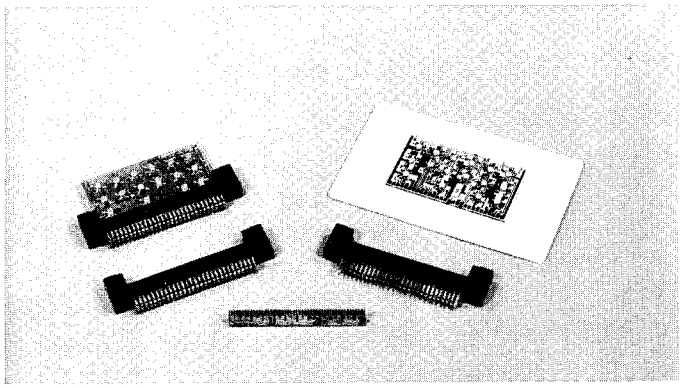

Fig. 7. Typical slides and test connectors.

on a coordinatograph by scribing lines halfway through a laminate of red upon clear Mylar. The scribing stylus is positioned and directed by a precision coordinate plotter and set to within ± 1 mil over a 40- by 47-in. carrier.

The scale to which the master is produced is determined by the reduction required to diminish the ± 1-mil error to an allowable tolerance at the final circuit size. In this case, a precise 10 to 1 photographic reproduction ideally reduced the 1-mil cutting error to 0.1 mil at the plane of the emulsion in the high-resolution spectrographic plates used in photography. This represents a degradation of circuit perfection at a level of $\pm 1.7\%$ for a 0.006-in. line width. Photographic negatives produced in this fashion are cemented to precision work-holding frames. Registration of successive processes to within 2 mils is easily obtained by preregistration of the photographic plates in the frames.

FILM FABRICATION

A typical deposited thin-film circuit is illustrated in Fig. 8. The production of the film circuit involves the following sequence of processes: (1) substrate selection; (2) film deposition; (3) pattern generation; (4) stabilization and adjustment; (5) attachment and soldering of transistors and jumper clips.

Glass is used as the principal substrate material because it is inexpensive and quite uniform chemically, and it has a surface both flat and smooth enough to be used directly as supplied. A ceramic substrate will probably be used in future applications.

Tantalum, a refractory metal with a melting point of 2995°C, is deposited for both resistive and capacitive films. Sputtering was selected for the deposition process because it is relatively simple and easy to control and does not require the high temperature necessary for the evaporation of tantalum. It is attractive also because of the large area that may be uniformly coated at one time and the ease with which nitrogen may be incorporated into the films [13]. Conductive films are evaporated directly onto the tantalum film immediately after the sputtering.

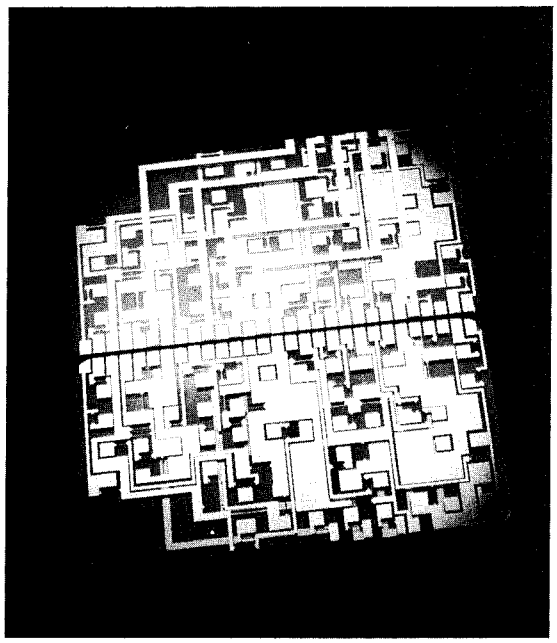

Fig. 8. Typical thin-film circuit (reverse at top, obverse, at bottom).

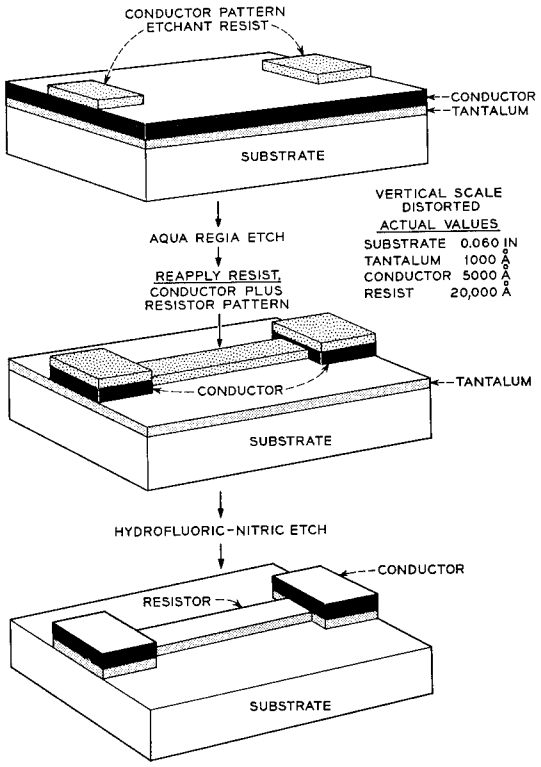

Fig. 9. Selective etching process.

A selective etching procedure is used to define tantalum resistors and the conductive areas. The unwanted conductive film is etched away with aqua regia, which does not attack tantalum. Tantalum is then removed from selected areas with a mixture of hydrofluoric and nitric acids. This is shown schematically in Fig. 9.

Stabilization is begun by production of an anodic oxide (Ta_2O_5) on the resistors. A heavy grease applied to the substrate through a precision silk screen covers the areas to be protected from the electrolyte. After anodization, the substrates are subjected to high-temperature aging in an air oven. Following this thermal stabilization process, the films exhibit aging properties superior to those found in deposited carbon resistors.

At this point, the entire group of resistors is brought to the proper level of resistance by another anodization. In this adjustment process, all resistors are anodized simultaneously. The adjustment process is monitored by an ohmmeter connected to one or more resistors. The anodization potential is increased until resistance reaches the desired level. Thus, the tolerances observed in the group are dependent upon the uniformity of initial sheet resistance and upon the accuracy with which the cuttings are reproduced; they are of the order of $\pm 5\%$.

TYPICAL HYBRID ASSEMBLY

A typical assembly of a hybrid thin-film circuit with 16 dual-transistor packages attached is shown in Fig. 10. The choice of resistor line width of 0.006 in. and sheet resistance of 40 Ω/square permits the resistors to be large enough for relative ease of processing while, at the same time, small enough so that approximately 50 resistors on each circuit substrate can be neatly positioned among the patterns of bonding lands for the transistors. These oversized lands and ground leads, along with the generous intraconnecting conductors, prove to be the

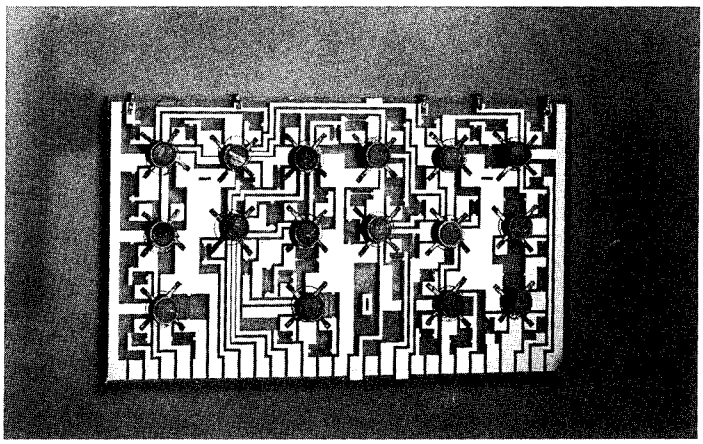

Fig. 10. Completed slide assembly.

principal area consumers. The precise location and orientation of transistor leads by a vacuum fixture will materially reduce the land areas needed to effect the bonds. Smaller lands and narrower conductors will, in turn, reduce the size of the present substrate or provide for a greater packaging density on the same substrate. The insulator discs are appliquéd and the transistors are soldered to the film circuit after all thin-film circuit processing is completed.

The present layout includes dummy load resistors (910 Ω) between the collector and emitter leads of the transistor whenever the fan-out is one. Improved transistor characteristics have made them unnecessary and, therefore, have simplified the problem of intraconnections and made possible the shortening of conductor lead lengths.

As indicated previously, the layout for the entire arithmetic unit uses only four different slide codes. A reduction in the number of basic patterns can be expected when tantalum thin-film circuits are uniformly deposited onto larger substrates intraconnected with multilayer crossover conductive paths. Larger substrates will mean more circuits per substrate, thereby reducing the steps in processing and the number of interconnections. Intraconnections with multilayer crossovers on the present 1.7- by 3-in. assemblies will immediately result in size and weight reductions and also recover most of the layout efficiency. At this time, however, the placement of logic without crossovers in the 3 by 6 array on a 1.7- by 3-in. substrate has been retained in order to demonstrate the capability of tantalum thin-film circuits and the associated intraconnection and interconnection techniques.

INTEGRATED CABLE CONNECTOR CONCEPT

The first eight-slide thin-film module containing 2 bits of logic assembled with connectors and hand-wired interconnections is shown in Fig. 11. The 8-bit assembly shown in Fig. 12 includes four 2-bit modules. The fifth module contains three additional hybrid thin-film circuit assemblies, which were added to facilitate direct replacement of the slide equipment drawer shown in Fig. 1. These circuits are power drivers which drive as many as 16 gates in parallel. The 8-bit hand-wired assembly, which met all electrical design objectives, contains 1100 transistors and 1600 resistors on 35 slides assembled from five basic slide codes; every bit consists of the same four slides, those shown uppermost in Fig. 13. A full-size arithmetic unit (24 bits) would consist of three 8-bit assemblies that are mechanically and electrically identical.

It was evident from the model in Fig. 11 that it was impossible to achieve a reasonable packing density in practice unless some means was found to interconnect groups of thin-film

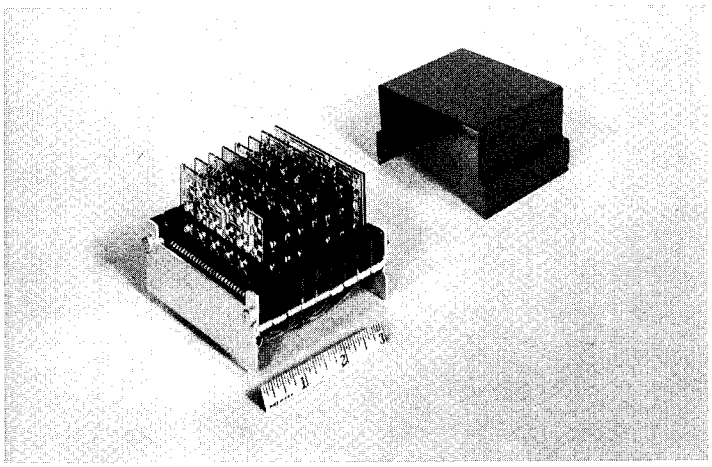

Fig. 11. Prototype 2-bit hand-wired assembly.

circuit assemblies into functioning modules without consuming a volume many times greater than that of the film assemblies themselves. It was desirable to retain the advantages gained from being able to insert the circuit into and withdraw it from a reliable connector, particularly during the period of inspection and electrical test that follows final assembly. However, at the time of this development, the available spring-type friction connectors were not satisfactory. The approach taken toward these seemingly contradictory objectives is the use of connectors which, after the equipment is tested, are converted to or replaced by permanent bonds.

The integrated cable connector is shown in Fig. 14. The multilayer board is bonded to the wire forms by a solder dip. The completed assembly supplants the heavy connectors and bulky hand-wired harness, yet occupies only a thin slice in space. The simple, self-supporting, self-aligning wire forms* have adequate spring tension and life to perform the function of a built-in connector until the thin-film circuits are ready for encapsulation. The front and rear solder connections at the base of each thin-film circuit assembly for all 29 wire forms on the integrated cable connector are made simultaneously in 25 sec by the application of a thin line of infrared heat. A photograph of the bond effected is shown in Fig. 15. The land areas on the thin-film assembly and the wire forms are precoated with solder in a nitrogen atmosphere. Consequently, these bonds are achieved without the use of a flux.

The multilayer cable† consists of a number of patterns of printed-wire conductors and terminations alternately sandwiched between insulating layers, but connected together by a copper bus (0.040 in. square) at predetermined locations dictated by the electromechanical requirements of the system. The thickness of each conducting and insulating layer is approximately 0.002 in. and 0.004 in., respectively. The matrix interconnection of three ground paths, one voltage supply, and all signal paths for 2 bits of logic is achieved by interleaving six layers of conducting paths with seven layers of insulation for a total thickness of 0.040 in. The multilayer cable is bonded to a suitable backing board to provide the required stiffness and heat dissipation. Subsurface intraconnections between conductors can be made at any point and between any two intermediate levels. The spring-wire forms (16 mils in diameter) are inserted into holes drilled into the solid-copper interconnecting buses. The circuit density achieved by these techniques exceeds that attained by most other multilayer printed wire

* Components Corporation, Denville, New Jersey.
† Intellux, Inc., Santa Barbara, California.

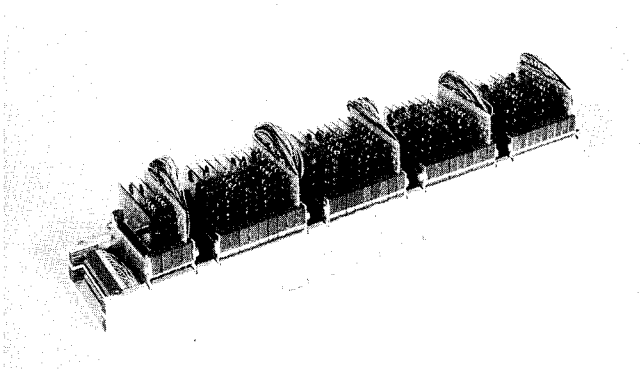

Fig. 12. Model of the 8-bit hand-wired assembly.

techniques. The thickness of the copper wall for each drilled hole (annulus) is 10 mils, which is about five times greater than that provided by the method of "plated-through holes."

Two bits of logic on an integrated cable connector are shown in Fig. 16; the mirrored images illustrate the assembly. The hybrid thin-film circuit assemblies are spaced on 0.180-in. centers. In future assemblies, these centers will probably not exceed 0.140 in. All the hand-wired interconnections and the connectors for 2 bits of logic have been replaced by more intimate metallic bonds formed during the electrochemical deposition processes used to fabricate the integrated cable connector. Reproducibility of interconnections is assured. Assembly time and labor have been reduced. Errors in wiring are eliminated. Consequently, there is a potential increase in reliability and further reduction in cost. A minimum of space and weight is used for insulation, connection, and their associated mechanical supports. Therefore, a

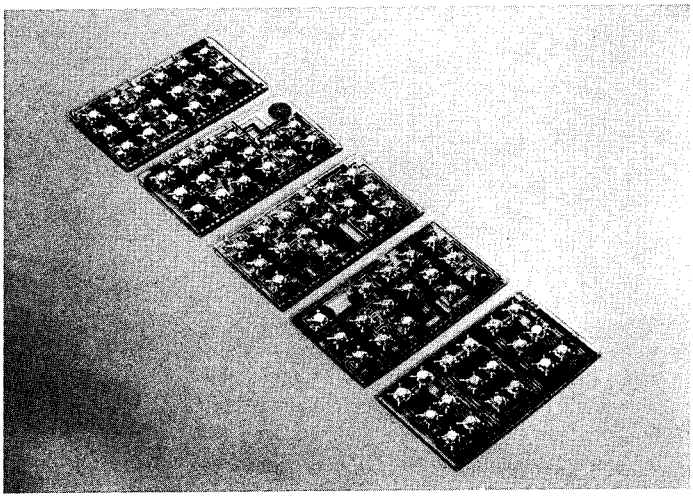

Fig. 13. Hybrid thin-film integrated circuits.

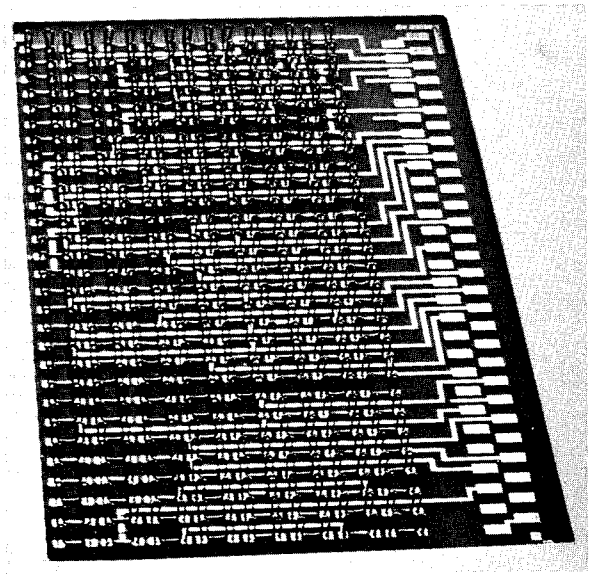

Fig. 14. Integrated cable connector (top insulating layer removed to expose intraconnections).

substantial decrease in size and weight is realized. During manufacture the exposed solder-covered buses (Fig. 17) are used as test points for both the thin-film circuit assemblies and the integrated cable connector.

The low-cost, readily available multilayer cable has other potential advantages. Incorporation of ground planes in conjunction with closely controlled dielectric thickness and precise

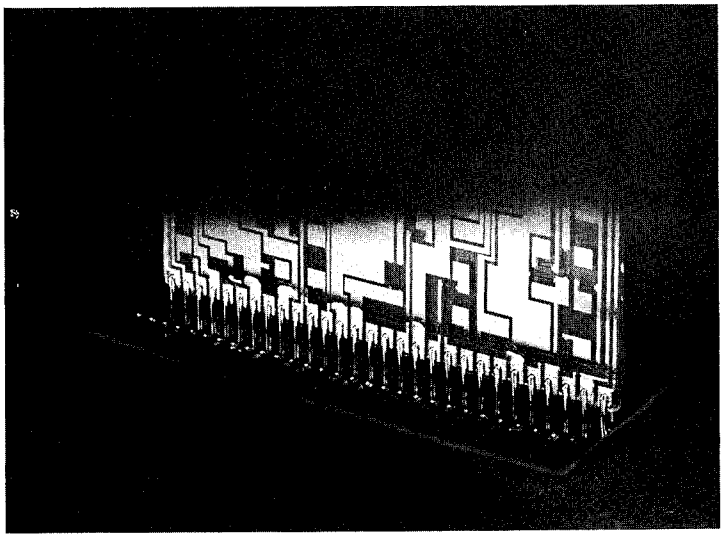

Fig. 15. Infrared-bonded clips.

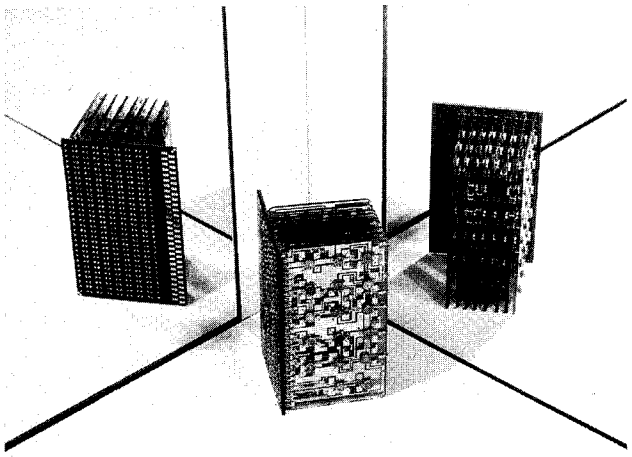

Fig. 16. Two-bit hybrid thin-film integrated circuit assembly with reflected views.

conductor widths could make the production of constant-impedance conductors (strip transmission lines) practicable. This feature will be especially important in future high-speed data processors. In addition, system design can be improved because of the greater flexibility of interconnections and the custom placement of wire forms specifically tailored for each circuit. Both these factors are under the control of the engineer and no longer need to be tailored to some arbitrary connector standard.

The wire forms along the edge of the hybrid film circuit assembly are spaced at 100-mil centers for compatibility with the connector used in the hand-wired model. New designs indicate that a 75-mil spacing is readily obtainable, and closer spacings can be obtained with a moderate redesign of the wire form.

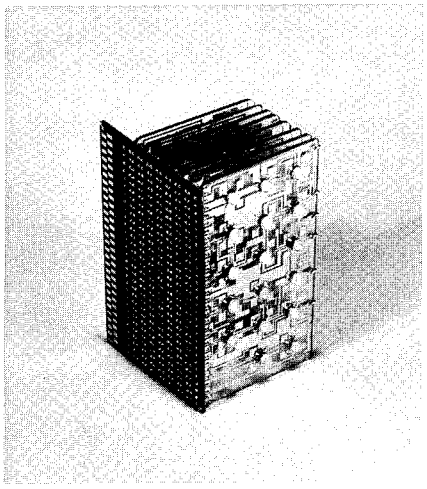

Fig. 17. Test points for 2-bit logic module.

ENCAPSULATION

Eight slides (2 bits of logic) are assembled and foamed into a readily removable, encapsulated "throw-away" package. Twelve such packages, all of which are electrically and mechanically identical, make up the 24-bit arithmetic unit. The throw-away package size resulted from a compromise among many factors, primarily cost, reliability, and simplicity of interconnection and field maintenance.

To protect these modular assemblies against moisture, they are first dipped in an acrylic. The acrylic also provides additional mechanical support for the appliquéd devices. The assemblies are then encapsulated in polyurethane foam, which protects them from damage due to shock, vibration, heat, moisture, normal handling, and other hazards.

A model of an encapsulated module containing 2 bits of logic is shown in Fig. 18. An 8-bit encapsulated assembly is shown in Fig. 19. These foamed assemblies have been mounted by conventional means on a supporting printed wire interconnecting board. All developmental modules fabricated during this exploratory development have performed satisfactorily.

The encapsulant can be designed to contain an appropriate heat sink, thermally connected to a plate or some suitable enclosure. However, no cooling medium or heat sink was necessary because of the low power dissipation.

Another variation in the encapsulated package can be obtained by controlling the overcharge of encapsulating foam in a closed mold. The resulting package has a rigid, noncellular surface that is capable of withstanding higher compressive loads than the ordinary foamed assembly. The package can be constructed in a wedge shape that permits it to be interlocked with similar adjacent packages, and the resulting units can be constructed so that, upon insertion into their assembly or container, they can be locked into a single, monolithic, self-supporting group.

Shielding, if required, can be provided by a metallized film that is either vacuum-deposited, sprayed, or painted onto the surface of the encapsulant. A second approach to shielding is to place the assembly into an enclosure that either is made of metal or has a metallized surface. Such an enclosure for the module or for the entire system, when suitably designed, can also serve as a heat sink and hermetically seal the assembly.

INTERCONNECTIONS

The 8-bit assembly as interconnected in its final design contains four 2-bit modules, each of which is terminated with a multilayer printed wire matrix. A fifth package has three sides

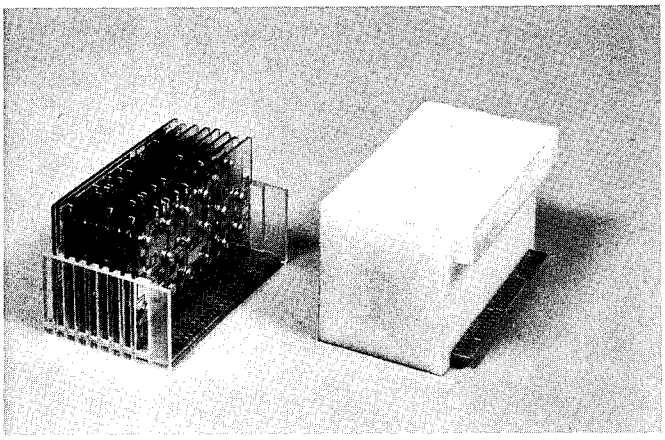

Fig. 18. Model of the 2-bit logic module.

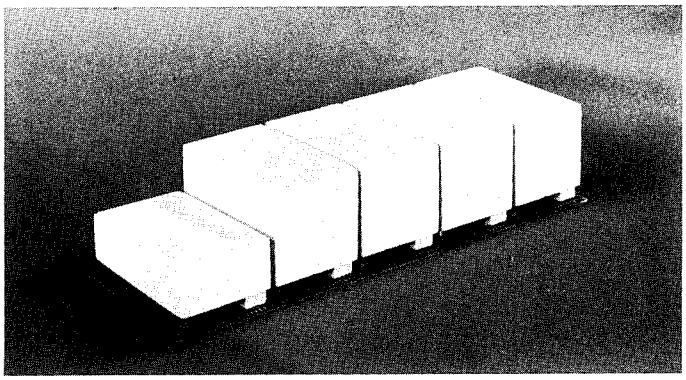

Fig. 19. Encapsulated 8-bit thin-film assembly.

terminated onto a standard printed wire board. The interconnecting wiring between these five subassemblies can be achieved by any one of three basic techniques. The first approach, the use of wire with connectors, was used to expedite testing and to facilitate any necessary wiring changes.

A second interconnecting medium is a conventional printed wire board. A staggered array of wire-formed clips (Fig. 20) designed for the terminations of the integrated cable connector (Fig. 14) replaces the conventional connectors; printed wire leads replace the temporary hand-wired cable. This second approach was used to demonstrate the interconnection technique because it was low in cost and required a minimum of development time.

The third approach involves the use of a multilayer matrix designed to terminate into an 8-bit interconnecting printed wire board using a wire-wrapped split-pin connection, as illustrated in Fig. 21. This arrangement will facilitate interconnection as well as simplify the design of the 8-bit interconnecting printed wire board. The more reliable wire-wrapped connection will replace the solder joint. In addition, this assembly is easier to repair and is of equivalent packaging density.

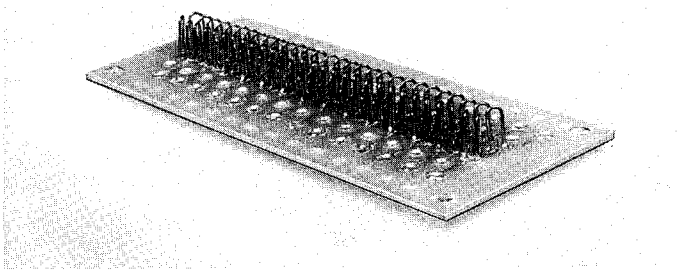

Fig. 20. Typical wire-form connector.

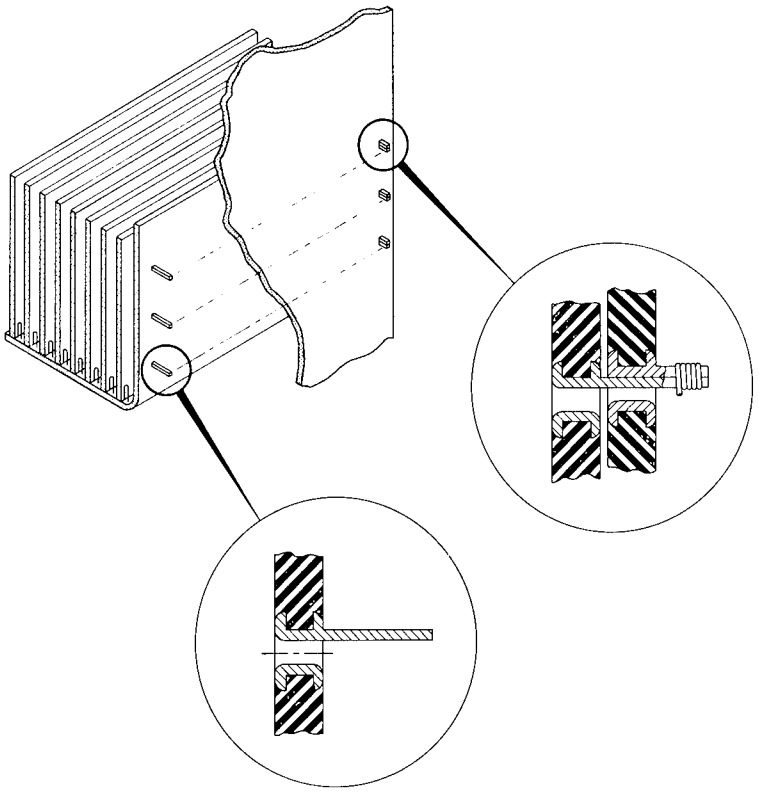

Fig. 21. Split-pin wire-wrapped printed circuit assembly.

A large number of interconnections used in the wire-wrapped DPU have been replaced by more intimate metallic bonds formed during the vacuum deposition process and the chemical deposition processes. This reduction in the number of interconnections should further contribute toward increased reliability and reduced cost.

PERFORMANCE

The completed 8-bit thin-film arithmetic unit has performed as expected in every test. It has been interchanged successfully with a comparable 8-bit slide drawer of the wire-wrapped DPU and exercised at rated speed with a representative program. The interconnecting cable to the hand-wired DPU was long (over 3 ft), simulating excessive ground-lead inductance. The performance of the assembly indicates that satisfactory rules have been generated for the interconnection and logical placement of active devices relative to their passive (resistor) elements, grounds, and power leads.

Maximum operational speed was not a design criterion; however, capability is well beyond the wire-wrapped DPU clock period of 0.625 μsec. One fundamental performance parameter is the average propagation delay per node; measurements on a portion of the 8-bit thin-film unit indicate a delay value of less than 20 nsec.

A comparison of the 8-bit wire-wrapped slide drawer assembly with the encapsulated unit containing 8 bits of thin-film logic is shown in Fig. 22. The thin-film unit has achieved a reduction of approximately 20 to 1 in volume and approximately 10 to 1 in weight over the comparable slide drawer assembly. Use of thinner glass or ceramic substrates in future systems should further decrease the weight. Ceramic substrates now becoming available will provide

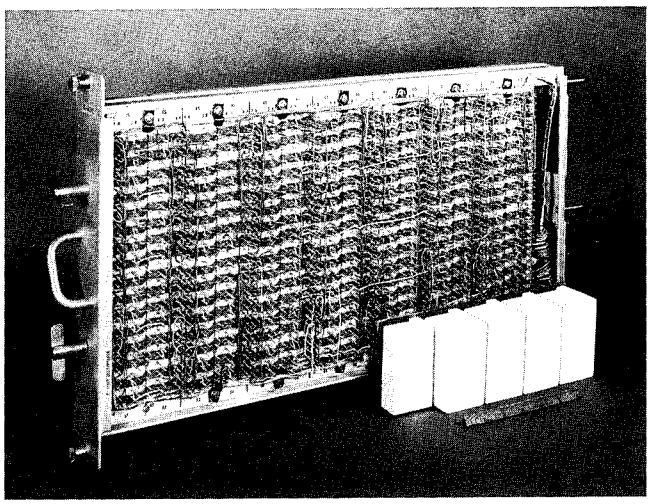

Fig. 22. Volume comparison between the 8-bit thin-film assembly and the 8-bit wire-wrapped assembly.

feed-through connections and facilitate intraconnections, thereby improving reliability as well as the density–volume–weight relationships. It is expected that future thin-film assemblies will be competitive in cost with their wire-wrapped counterparts and will also demonstrate their greater potential reliability.

SUMMARY

The thin-film Data Processing Unit has shown the attractiveness of tantalum films, when suitably interconnected, for the next generation of data processors. In comparison with conventional wire-wrapped techniques:

1. Costs of fabrication are currently comparable. For example, all passive components, all terminations, and almost all conductive interconnections have been deposited simultaneously for no greater cost than that of depositing the first element. The mechanization of these techniques should provide further substantial cost reductions.
2. Reliability has been increased by the replacement of all hand-wired interconnections for the DPU by more intimate metallic bonds formed by both the vacuum and the electrochemical deposition processes. (Use of these techniques should also contribute significantly to cost reduction.)
3. The speed of the thin-film unit has been kept equal to that of the wire-wrapped unit so that the 8-bit unit can be interchanged with the 8-bit slide drawer (shown withdrawn in Fig. 1).
4. Weight and volume have been reduced significantly by the reduction in space and weight necessary for insulation, connection, and their associated mechanical supports.
5. Design techniques, processes, and parameters have been selected that permit present-day fabrication of data processors with thin-film circuits. Furthermore, these units lend themselves to mechanized manufacture, which, with its inherent uniformity and control, is expected to increase the reliability of the units as well as reduce costs and lead time to operational systems.

The emphasis in this program has been on achieving a good compromise between practical objectives and on devising techniques suitable for future data processing machines. Speed,

TABLE II

Summary of the Characteristics of the Thin-Film dctl

Logic	Direct-coupled silicon transistor logic
DPU speed	Add and subtract—10 μsec; multiply and divide—135 μsec average
Circuit speed	20 nsec average nodal propagation time
Nodal dissipation	3 mW
Power voltages	One 2.6-V ± 5% supply
Transistor type	A silicon, diffused, planar, epitaxial type in a double-junction pancake miniature enclosure
Resistors	560 and 910 Ω ± 5%
Logic drive	Fan-in 4, fan-out 3
Approximate reduction (wire-wrapped/thin-film)	
Physical volume	20 : 1
Weight	10 : 1

as such, has not been emphasized, but the available speed per unit of power consumption is high and is greater than that of known solid-circuit miniaturization approaches. Although it does not achieve the compactness of some solid circuits, the thin-film circuit offers greater production economy, flexibility in handling circuit variety, and potential reliability. It is a fabrication technique that is in the early production stage now and, with relatively small risk, could go into larger-scale production.

Table II summarizes the significant mechanical and electrical parameters of the thin-film dctl circuitry.

ACKNOWLEDGMENT

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The Enhanced Micromodule: A Disciplined Approach to Microcircuit Integration

D. J. GARIBOTTI AND W. V. LANE

Hamilton Standard Division, United Aircraft Corporation, Broad Brook, Connecticut, and U.S. Army Electronics Research and Development Laboratory, Fort Monmouth, New Jersey

An all electron beam welded, hermetically sealed, interconnection–packaging system which is compatible with all approaches to microminiaturization has been developed and is now entering the pilot line production stage. The system which is referred to as the enhanced micromodule provides extremely high conductor and termination densities of demonstrated reliability. The structure permits interconnection and hermetic sealing of integrated as well as hybrid semiconductor and thin-film circuits on a standard microwafer form factor. Hermeticity and freedom from polymers make the system compatible with extreme environments, and the packaging of uncased discrete active devices and semiconductor circuits. Thus, relatively expensive individual enclosures are eliminated. The potential packaging density capability of the package is at least an order of magnitude greater than the present micromodule.

Standardization of the structural parts naturally led to the establishment of an automated assembly process without limiting electrical design freedom. The primary tool of the automated production facility is an electron beam machine which has both welding and machining capability. The latter is complemented by tape programmers which control both the work-table and the electron beam operating parameters. Production by standardized automated processes results in enhanced reliability and quality assurance, coupled with significant cost reductions over present techniques. Functional enhanced micromodules incorporating both semiconductor and thin-film circuits are available.

THE ENHANCED MICROMODULE—DEFINITION AND CHARACTERISTICS

THE ENHANCED MICROMODULE (EMM) is a hermetically sealed interconnection–packaging system which employs electron beam welded microconnections of demonstrated high reliability. The system permits interconnection of integrated as well as hybrid solid-state and thin-film circuits, and yet retains the principle of a standard wafer form factor.

Standardization of the basic structural parts of the enhanced micromodule has facilitated the establishment of an automated assembly system wherein the electron beam machine is the primary tool.

The EMM is a modular dimensioned electronic package which is composed of standard notchless wafers, which support discrete and deposited electronic parts or networks. The form factor of the EMM is a rectangular parallelepiped—0.390 × 0.390 × 0.800 in. (maximum)—with twenty external leads, which protrude from a glass-to-metal header at the base of the assembly. Hermeticity is imparted to the structure by electron beam welding a can to the periphery of the header.

Internally, a transfer wafer is joined to the header to permit transformation of the header pin layout which is on 0.075 in. centers to the 0.025-in. peripheral interconnection grid pattern of the microwafer stack.

The latter is joined to the header-transfer wafer assembly by means of 36 electron beam welded copper conductor ribbons. The completed microwafer stack consists of any combination

of up to ten microwafers, microelements, or microcircuits interconnected by conductor ribbons and supported by stack stabilizers. The wafers are either alumina, pyrex, or beryllia notchless substrates. On each wafer 36 terminations are fabricated by vacuum deposition and electroplating techniques. The nine terminations per side are located centrally on 0.025 in. centers and extend continuously from one surface of the substrate around the edge to the opposite side. The surface section of the terminations may be used for joining electronic components or electronic circuits.

The EMM is a hermetically sealed structure free of any polymeric materials, denoted by enhanced interconnection capability, heat transfer characteristics, structural rigidity, and electrical shielding capabilities. The structure is compatible with 200°C operating temperatures and the 0.4-in. center-to-center mounting established for micromodules. The salient features of the EMM are discussed below.

Packaging Characteristics

1. The EMM represents a packaging system that has been thoroughly developed from the basic microweld through each step of the assembly. It has not been hampered by sacrificing the detailed analysis of the interconnections and structure validity by demands to use it for functioning hardware before it was fully developed. Each critical aspect of the packaging system was subjected to thorough reliability testing.

2. The basic element of the EMM is a 0.310-in. square wafer with a standard edge termination pattern for interconnection within the microwafer stack. Standardization of the microwafer leads to the following advantages:

   a. The substrate can be made in large quantities for purchase as an off-the-shelf item with quick delivery, low cost, and assured quality control.
   b. The standard edged termination pattern permits the ultimate in process refinement, quality control, and reliability of the interwafer connections.
   c. With regard to thin-film microcircuits, the standard form factor of the wafer permits standardization of masks and associated fixtures, which allows quick changeover from one circuit to another at minimum cost.
   d. Permits the design of standard handling, testing, and shipping containers.
   e. It is naturally conducive to the use of mechanized assembly processes.
   f. It is compatible with the microelement processing and handling technique developed for standard micromodule microelements.

3. Hermetic sealing and freedom from polymeric materials result in a packaging system suitable for 200°C operation and higher storage temperature.

4. Stack stabilizers are provided to grip the microcircuit wafers on all four corners since the latter are in intimate contact with the enclosure can, thus permitting efficient removal of heat from the microwafer stack, effectively supplementing the heat removed by the electrical conductors. If still further heat transfer capability is required, the can can be backfilled with helium prior to hermetic sealing.

5. The vacuum environment within the can considerably reduces the harmful effects of radiation on the microcircuit wafers.

6. The exclusion of encapsulants eliminates the potential danger of harmful effects to the microcircuit wafer resulting from stresses arising because of dimensional changes of the encapsulant during curing and subsequent thermal cycling.

7. The hermetically sealed structure and the absence of polymeric materials permits the use of uncased semiconductor chips.

8. In the future, where lower costs are possible and circuit complexity warrant it, a larger size EMM can be readily introduced. The latter is equivalent to four standard EMM's. The larger microassembly (already established) comprises ten 0.600 × 0.600 in. square wafers each providing 80 microterminations, interconnected by 80 conductors. This structure entails a total of 800 microwelds in the microwafer stack. The input–output header terminals are doubled from 20 for the standard EMM to 40 for the larger microassembly.

Assembly Characteristics

1. Process control and resulting reliability can be obtained through experience with a process over long calendar time with small production quantities, or short calendar time with large production quantities. The standardized structure of the EMM permits the accumulation of a large amount of assembly process experience since this process is the same regardless of the circuit types produced.

2. The standard form factor of the EMM permits the design of universal test and evaluation equipments, thereby reducing the cost of jigs and fixtures for special test setups for a particular EMM design. In addition, since the ability of the EMM to withstand the rigors of military environments has already been established, many tests may be eliminated, yielding further reduction in costs. Along these same lines, the universality of the component elements of the EMM simplifies the preparation of test methods and specifications. Two levels of test equipment and specifications can be established—one for wafers and the other for the complete EMM.

3. The standardized microwafer form factor of the EMM will not inhibit the development of new devices, but rather will enhance this development. Improvements in microcircuit process technology can be applied to the usable area, 0.280 × 0.280 in., of the microwafer without affecting the overall EMM characteristics, provided the termination scheme of the microcircuit wafer is held constant. In addition, the acceptance of the EMM microwafer standard form factor will encourage the device manufacturer to develop new items since he will have a ready market for his product.

4. Most systems producers will eventually have thin-film circuit, solid-state circuit, and microassembly interconnecting capabilities in-house; however, some companies will specialize in unique microcircuit and microelement devices. These companies will be able to supply these special devices to the systems producers at a lower cost than the systems people can manufacture them. By having devices on the standard microwafer, the device manufacturer can produce the items in large quantities at low cost. Consequently, the systems producers can purchase them as off-the-shelf items in small quantities at reasonable prices.

5. A substantial factor in the cost of microcircuit equipments can be attributed to the individual hermetic sealing of the active devices. As stated previously, the absence of polymeric materials and hermetic sealing permits the use of uncased discrete active devices and semiconductor circuits. The simultaneous sealing of the semiconductors results in a substantial cost savings in the overall equipment by elimination of individual enclosures.

6. The EMM may be considered equivalent to a current-day printed wiring subassembly. As the cost of the EMM's is reduced, it will be practical to use them as plug-in modules. In some applications, the use of a plug-in throw-away module composed of microcircuit wafers with relatively low MTBF characteristics will be practical. This event could open the door to the extensive use of EMM's by commercial electronic products manufacturers. In addition, applying this plug-in capability to military-quality EMM's will have significant effects on the level of maintenance personnel required, and reduce the down-time and cost required to correct malfunctioning equipment.

Systems Capability

1. At present it is generally believed that integral electronics will ultimately comprise semiconductor as well as thin-film circuits and components. The EMM provides a form factor and interconnecting system that is compatible with either, or a combination of both (Hybrid-circuits). In addition, components in the microwafer form factor such as inductors, large-value capacitors and resistors, crystals, etc. can be combined in the EMM to overcome the limitations of solid-state circuits.

2. The EMM package can be mounted in the standard micromodule 0.400-in. square mounting area. In many instances, it will be desirable to utilize the standard micromodule for such applications as linear circuits, inductor circuits, or high-powered circuits, where performance capabilities of thin-film and solid-state circuits are limited. The compatibility of the two structures makes possible optimum second-order microcircuit assemblies.

3. The standardization of the micromodule and enhanced micromodule form factor makes possible the design of modular assembly hardware for second-order assemblies. The

standardization of connectors, structural designs, etc. will result in lower cost and higher reliability for the overall equipment for the same reasons enumerated for the standard MM.

4. An important aspect of the EMM that cannot be overemphasized is that the majority of the interconnections that must be accomplished by printed wiring in the TO-5 can and flat-pack approaches are incorporated in the microwafer stack. These joints are electron beam welds of demonstrated reliability in a standardized conductor matrix. It should also be noted that all the welds and conductors are located in a hermetic enclosure and are not subject to the problems of moisture and the temperature limitations of printed wiring assemblies.

5. It is generally conceded that commitment to a single-block, solid semiconductor circuit results in an extremely expensive item unless high yields and large production are assured. The EMM permits the integration of "chip components" and, if subsequent production demands warrant it, the "chip components" can be replaced by a fully integrated device on a wafer having an identical termination pattern. Thus, a direct replacement of the chips by the single block circuitry wafer can be accomplished without affecting the EMM assembly design. The same argument will apply to thin-film hybrid circuits when thin-film active devices become available.

6. The standard interconnection conductor matrix, coupled with the standard microcircuit wafer termination, permits the application of computer techniques to the layout and design of the microcircuit wafers and the EMM microwafer stack interconnections.

HISTORICAL BACKGROUND

One continuous and consistent trend in the history of electronics has been reduction in the size and weight of the assembly needed for any particular electronic function. Coupled with this trend there has been an ever-increasing effort to enhance reliability and decrease cost through standardization. Speculative talk about ultimate packaging densities—"the numbers game"—is no longer popular [1].

Many techniques for reducing the size, weight, and power consumption of electronic components, circuit assemblies, and functional units have been proposed, demonstrated and, occasionally, exploited [2]. In some cases, individual components retain their individualities and are interconnected by relatively standard, although sophisticated, wiring techniques (e.g., cordwood). In certain of the more refined approaches, a number of recognizable devices are combined into an integrated structure, or even into a complex structure in which the interconnecting medium between the devices contributes to the electrical properties of the structure [3].

Until recently, microminiaturization has taken many forms, almost as many as there are companies engaged in this work. Nevertheless, by taking a rather broad viewpoint, it is possible to classify the general approaches to microcircuitry in terms of the essential forms of the circuit elements as shown below.

Types of Microcircuitry Approaches [4]

A. "Conventional" elements with leads for use in printed wiring or welded assemblies.
B. Specially shaped elements to facilitate denser circuit assemblies:
    1. Uniform length of thickness ("dot" components of the Hughes and Mallory systems).
    2. Uniform cross section (wafer microelements of the Signal Corps micromodule program).
C. Complex or integrated circuits in which several circuit elements are formed *in situ* as part of a particular circuit–integral electronics [5]:
    1. Thin-film integrated or hybrid circuit.
    2. Solid-state circuit—semiconductor integrated or hybrid circuit.

Of the three microminiaturization approaches being considered, that which involves assembly of pretested components of special design in an improved packaging topology predates the others. Its origin may be traced to the "tinker toy" activity and is exemplified by the Signal Corps micromodule. It is the objective of this program to achieve a reasonable

reduction in size, weight, and cost, and an increase in reliability through standardization of parts, methods, and assembly techniques. At inception, the degree of miniaturization was maintained at a minimum; however, flexibility of the assembly concept allows higher component densities as new devices and processes evolve. For example, contemporary design generally provides for incorporation of only one component on the basic structural element; but, at the expense of extreme flexibility several components may be mounted on one wafer. At least six resistors, four transistors, or six diodes may be joined to a wafer and independently tested. Moreover, one wafer may contain an integrated solid circuit of one kind or another. Hence, the relatively low component packaging density of the current micromodule can be extended; however, in the final analysis, the limiting factor is the number of available riser wires.

The advantage of single electrical elements per basic assembly should not be underestimated. Flexibility of the package and circuit design is a striking advantage. Also, pretesting of basic assembly microelements prior to integration in the package is an attractive feature from a circuit quality assurance standpoint.

In the micromodule the majority of components required for electronic systems assembly are packaged in a standard configuration. Standardization is maintained at the component, or substrate, as opposed to the circuit level. This facilitates packaging. Since the form factor is fixed, automatic assembly of components to form circuits is relatively simple.

The standardization of processes for components fabrication and assembly is conducive to high reliability and cost reduction. At present the micromodule is production-oriented and will move into high-volume production at an earlier date than the other microminiaturization approaches.

The circuit design flexibility, potential low cost in either larger or small production, the attainment of reliability through high-volume standard production techniques and pretest of components under various conditions are the most important attributes of this system. The micromodule is an interconnection–packaging technique and as such should accept the best from the other microminiaturization approaches. However, the utilization of integrated and hybrid semiconductors of thin-film circuits requires an interconnection capability which is beyond the original scope of the micromodule. Furthermore, the early realization of low-cost systems strongly suggests the use of uncased devices. This approach in turn requires that provisions be made for protection from the environments.

These potential problems were recognized by the Signal Corps at an early date. As a consequence, very timely development programs were instituted several years ago to overcome these limitations. The problems undertaken at that time were:

1. Improve the interconnection capability.
2. Increase the number of components per wafer in order to realize the cost reduction accrued as device technology advanced.
3. Increase the number of terminations per microwafer to accommodate the increased number of components per wafer.
4. Improve the reliability of the interconnection joining process at a very high termination density.
5. Improve the encapsulation technique in order to utilize low-cost unencapsulated active devices and semiconductor functional blocks at the microwafer level, and utilize the micromodule in extreme environments.

Successful accomplishment of the above objectives has resulted in the *enhanced micromodule*.

The evolution of the EMM interconnection–packaging system has followed a logical sequence of chronological events:

1. Development of the interconnection process
2. Demonstration of the reliability of the process
3. Development of package system
4. Establishment of pilot line production capability

EVOLUTION OF THE ENHANCED MICROMODULE

This development was accomplished in three phases: Phase I [6] demonstrated the reliability and practicality of electron beam microwelds between copper conductor ribbons and metallized glass and alumina substrates. The reliability of the welds was statistically demonstrated in terms of electrical and mechanical characteristics. Phase II [7] was instituted to determine if the reliability levels of electron beam microwelds achieved in Phase I were maintained when applied to the interconnection of a stack of ten alumina or glass microcircuit support wafers simulating a functional module–microwafer stack. Phase III [8] provided for the hermetic sealing of the substrates–interconnection network to form a packaging system.

DEVELOPMENT OF THE INTERCONNECTION PROCESS

The inherent characteristics of electron beams—extremely fine diameters and high-power densities—appeared to offer a suitable tool for the interconnection of microminiature devices. Consequently, programs [6,7] were undertaken to develop electron beam techniques and associated fixturing to assure a reliable interconnection process.

Both 0.010 and 0.030-in.-thick alumina* substrates and 0.030-in.-thick glass† substrates were evaluated in the development process and reliability studies; however, only the data accumulated for the 0.030-in.-thick alumina are discussed since the conclusions, in general, apply to the other two substrates. In the process development effort the wafer size was 0.500 × 0.750 in. whereas in Phase II 0.600 × 0.600 in. substrates were used.

Individual OFHC copper ribbons—0.002 × 0.010 in.—were used in Phase I whereas in Phase II the interconnection matrices consisted of the same conductor ribbons spaced on 0.025 in. centers. The alumina and pyrex wafers were metallized respectively by the molymanganese and the platinum frit (Hanovia 130A New) techniques to obtain a conductive layer on the edges of the pyrex wafers. In these programs continuous pads were applied to the edges of the wafers instead of discrete terminations as required for actual service applications.

Following metallizing, both alumina and pyrex wafers were electroplated to an overall thickness of 0.001 ($^{+0}_{-0.002}$) in. of nickel from a low residual stress bath.‡ After electroplating, the edges of the wafers were ground to a uniform overall thickness to overcome the plating roughness which, in turn, was due to the metallizing operation.

Welding Fixtures and Processes

The welding fixture used in Phase I held six wafers at a time and was designed to load the ribbons in compression. In Phase II, considerable effort was devoted to the development of suitable fixturing for the welding of substrate stacks made up of ten wafers. A fixture was developed (Fig. 1) which permitted the welding of interconnection matrices on all four sides of a stack in a reliable and practical fashion. The finger hold-down device illustrated in the insert (Fig. 1) consists of two pointed tungsten fingers which were positioned by means of an externally actuated rocker arm. The function of this device was to ensure intimate contact between the conductor ribbons and the metallized wafer edge; however, no upset pressure was required during welding.

A typical manual electron beam welding process was accomplished in the following way:

Step 1: The operator positions the copper ribbon–metallized ceramic weld pad intersection under the preselected beam location by manual manipulation of the table control. A 40× power optical viewing system is used during the locating process.

Step 2: The operator actuates a switch which brings the hold-down finger into contact with the ribbon at a point immediately adjacent to that at which the weld is to be made. A preprogrammed machine parameter schedule is then energized and completed after which the

* Alsimag 614 (96% Al_2O_3), American Lava Corporation, Chattanooga, Tennessee. 98% Al_2O_3, Ceramics for Industry, Mineola, New York.

† Pyrex, Corning Glass Co., Corning, New York.

‡ Sulfamate Nickel, Barrett Chemical Company, Ansonia, Connecticut.

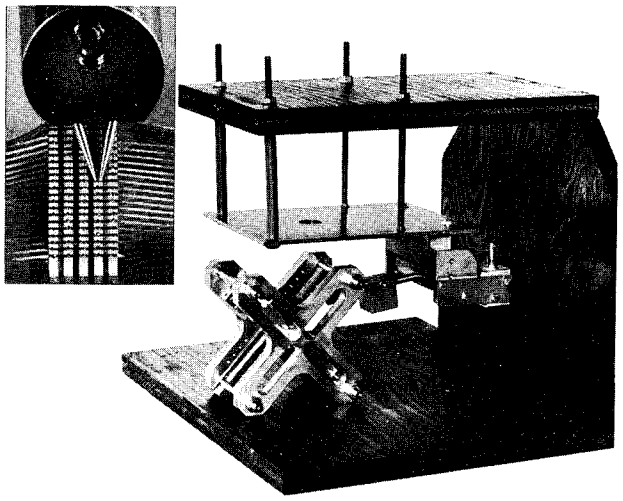

Fig. 1. Complete access fixture with finger hold-down device mounted outside the electron beam vacuum chamber to simulate actual operations.

hold-down finger is manually reset to the noncontacting position and Step 1 carried out. These steps were repeated a total of 200 times in the welding of one side of a ten-wafer stack.

Using this technique, several operators have achieved a weld rate of one per second on joining conductor ribbons on one edge of a stack. A typical average time per weld was two to three seconds.

Electron Beam Welding Parameters

A Hamilton–Zeiss electron beam welder (Fig. 2) was used in Phase II, whereas a Zeiss welder had been used for Phase I. During process development to define machine settings

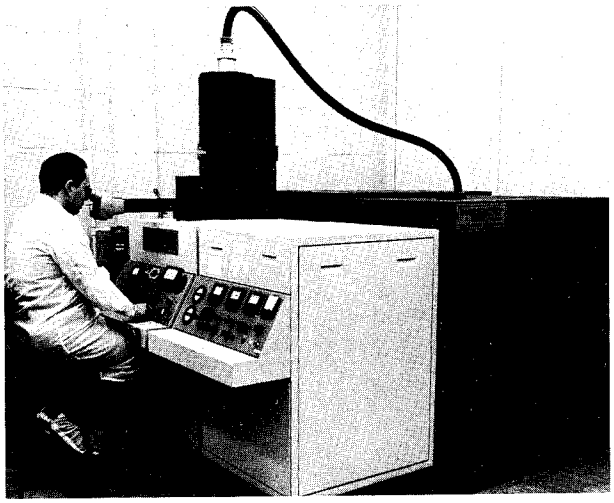

Fig. 2. Hamilton–Zeiss electron beam welder.

for the fabrication of reliable and reproducible welds, the following electron beam welding machine parameters were studied: cathode–anode accelerating voltage, beam current (pulse height) or electron flow, beam on-time (pulse width) or time during which electrons are directed from the source to the weld area, and beam deflection or pattern. The electron beam was programmed to deflect in the plane of the workpiece.

The following machine parameters were adopted:

Accelerating voltage	90 kV
Beam current	0.4 mA
Welding time (beam on-time)	5.3 msec
Energy delivered to workpiece	0.19 W-sec
Beam diameter	~ 0.003 in.
Beam deflection	± 0.0045 in. normal to ribbon axis at 1100 cps
Area scanned	0.003 × 0.009 in.

ELECTRON BEAM WELDING EVALUATION

After electron beam welding, each copper ribbon–electroplated nickel joint was examined optically at a 20× magnification and accepted or rejected on the basis of the following factors: (a) degree of conductor necking immediately adjacent to the weld nugget; (b) displacement of weld nuggets relative to the axis of the conductor ribbon because of poor alignment of area to be welded with electron beam axis; and (c) presence of severe blowholes. After the acceptance test the welds were submitted to mechanical and electrical test.

Weld Pull Strength and Resistance Testing Procedure

The strength of the welds was determined by testing the nugget in shear and the conductor in tension. In Phase I, interconnections were made at variable separations by welding eight copper ribbons to the 0.75-in. metallized edges of individual wafers. Welds of this type will henceforth be referred to as individual welds. In Phase II, ten wafers of a microassembly stack were interconnected with three copper ribbons on 0.025 in. centers, and the pull strength samples were prepared by cutting the ribbons as illustrated in Fig. 3. Weld pairs were tested

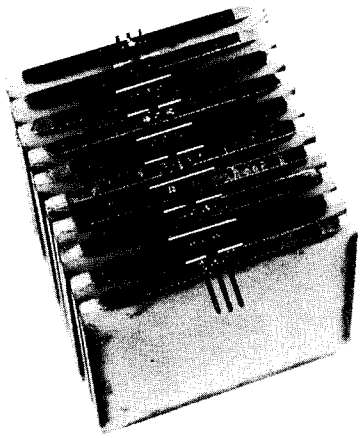

Fig. 3. Pull strength samples prior to separating into discrete units for testing.

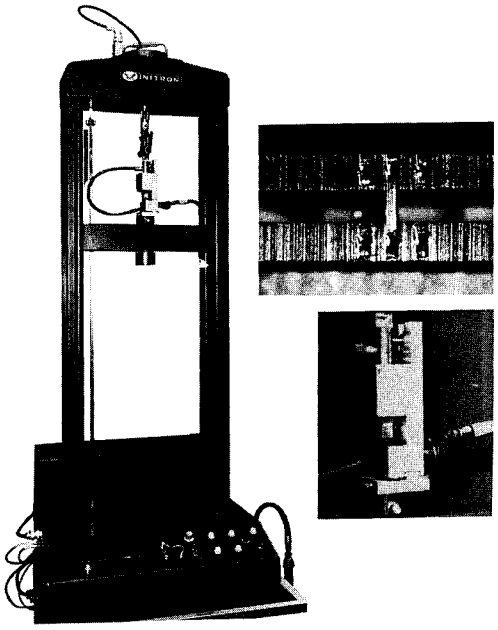

Fig. 4. Instron tensile testing machine (inserts illustrate (a) pull test weld pair; (b) vacuum chuck sample holder).

by holding the two wafers within vacuum chucks during pull testing, as illustrated in Fig. 4, in conjunction with the Instron Tensile Testing Machine, Model TM. Strain rate and chart speed were held constant at 0.5 in./min throughout all the tests. The accuracy of the recorded pull strength was $\pm 0.5\%$ of full scale reading (500 g).

The weld resistance of all the pull test samples was determined prior to pull strength testing. All resistance measurements were made by the standard four-point method with a Kelvin milliohm bridge. The experimental setup is illustrated schematically in Fig. 5. The accuracy of the measurements was $\pm 0.25\%$.

Both individual and microassembly weld pair samples on alumina and pyrex substrates were subjected to thermal shock tests to establish if any degradation in pull strength and weld joint resistance occurred during this environmental exposure. The samples were subjected to twenty cycles of thermal shock (-55 to 200°C) in accordance with the schedule of MIL Std 202A, Method 107, Test Condition C. Pull strength tests were also carried out after thermal shock exposure.

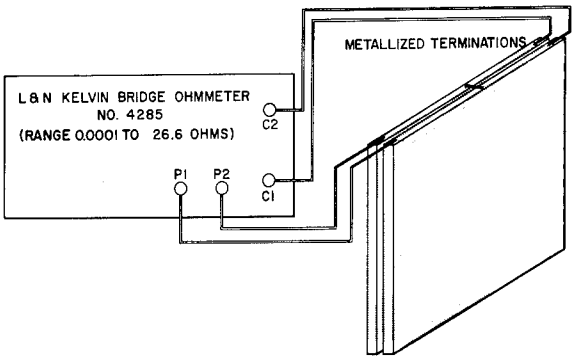

Fig. 5. Schematic illustrating weld resistance measurement technique.

Weld samples were mounted within a transite fixture and the changes in weld joint resistance measured from −55 to 200°C. Copper ribbons were connected from the wafer edges to terminals which were connected to a selector switch to permit rapid data-gathering. Sequential resistance measurements were taken at −55°C, room temperature, and 200°C after thermal stabilization was reached at each temperature.

Wafers with copper ribbons welded to the metallized edges as well as microassembly stacks were submitted to vibration tests in accordance with MIL Std 202A, Method 204A, Test Condition B. Fixturing of the microassembly stacks on the vibration table was designed to simulate the actual mounting of such a structure within a hermetically sealed can.

DEMONSTRATION OF PROCESS RELIABILITY

In Phase I electron beam processes with associated fixtures were developed to join eight copper ribbons at random spacings to the metallized edges of alumina substrates. Process development was followed by demonstration of the reliability of the electron beam welding techniques.

The highlights of the Phase I reliability program are presented below:

a. It was predicted at a 90% confidence level that no more than 3 welds out of 100,000 would fail below a 200-g load.

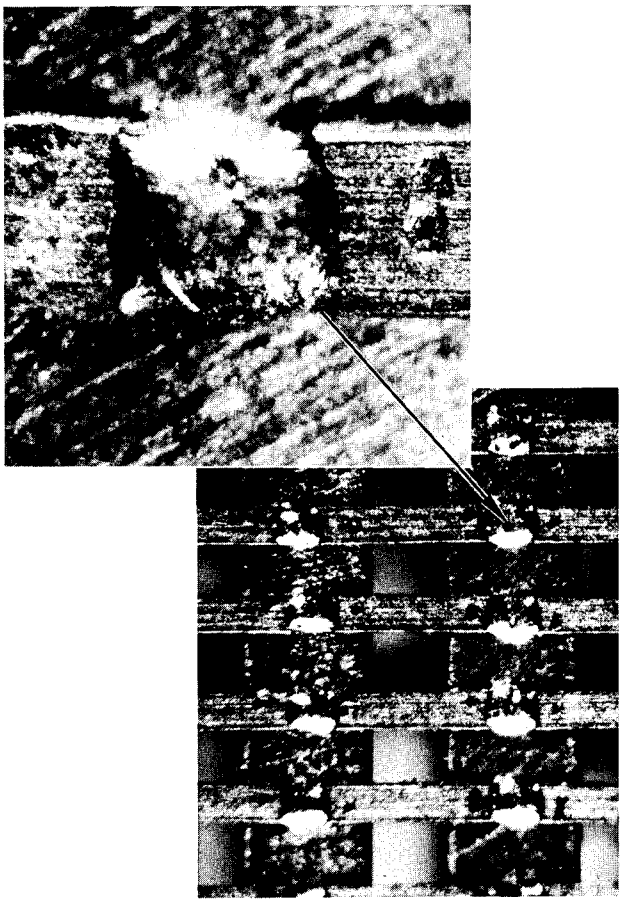

Fig. 6. Closeup of several electron beam welds: 0.002 × 0.010 in. copper ribbons joined to 0.030-in.-thick metallized alumina.

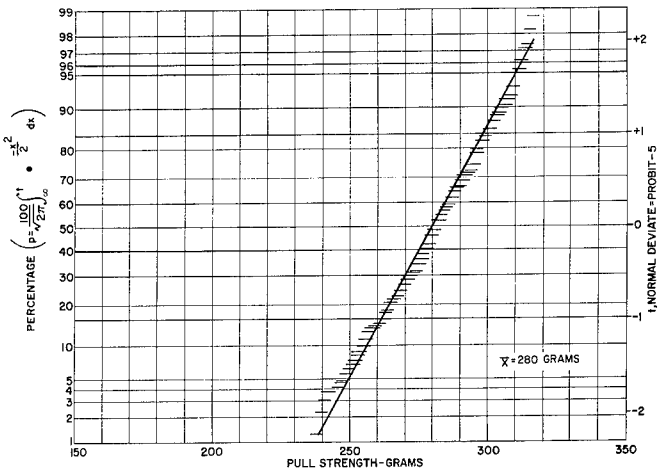

Fig. 7. Cumulative distribution of weld pair pull strength—0.030-in.-thick alumina.

b. It was demonstrated at a 90% confidence level that no more than 3 welds out of 1000 would have a resistance greater than 0.010 Ω at room temperature.
c. It was predicted at a 90% confidence level that less than 3 welds out of 1000 would increase in resistance by more than 1 mΩ after thermal shock.
d. The pull strength after thermal shock was degraded by approximately 12%; however, oxidation of the copper ribbons was responsible for this deterioration.

In view of the practicality of the process and the reliability which was achieved, a followup program was undertaken to develop techniques for the fabrication of wafer stacks with ten substrates each.

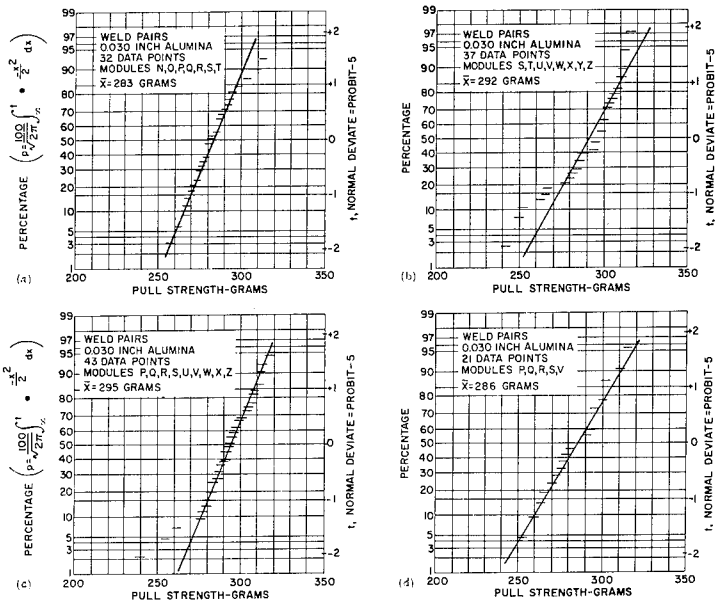

Fig. 8. Typical weld pair pull strength plots of 0.030-in.-thick alumina.

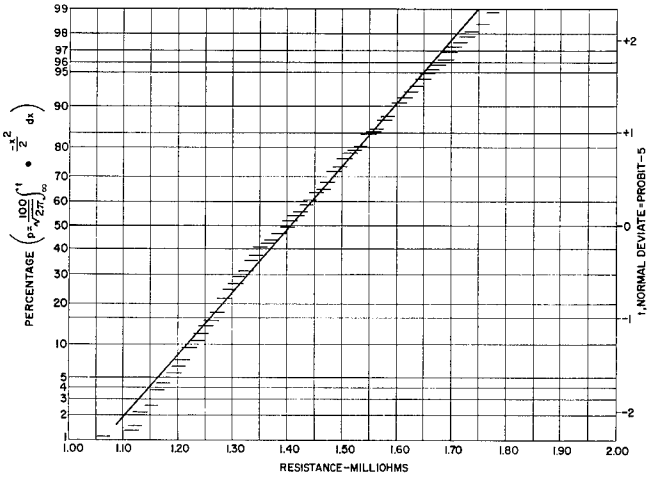

Fig. 9. Cumulative distribution of weld resistance from weld pairs—0.030-in.-thick alumina.

The characteristics of the joints fabricated in the subsequent phase were determined in the as-welded condition and also after various environmental exposures. It was of particular interest to establish whether the interconnection weld density and proximity had any degrading effect on the weld characteristics. A closeup of several welds is presented in Fig. 6.

The electron beam welds fabricated in Phase II were evaluated from the standpoint of mechanical and electrical characteristics and the following conclusions were reached.

Pull Strength: Statistical analysis of a relatively large sample population demonstrated at a 90% confidence level that less than 2.6 welds out of 200,000 would fail below 200 g. None of the welds failed in the fusion zone or at a load less than 200 g. The cumulative distribution of weld pair pull strength from 0.030-in.-thick alumina is illustrated in Fig. 7. Typical weld pair pull strengths for individual populations are shown in Fig. 8.

Weld Resistance: It was demonstrated at a 90% confidence level that less than 3 out of 1000 weld pairs would exhibit a resistance of 0.010 Ω or greater. The cumulative distribution of joint resistance for weld pairs on alumina wafers is given in Fig. 9.

Thermal Shock: No degradation of pull strength was observed. From the statistical evaluation of the resistance measurements before and after exposure, it was demonstrated that no more than 4.5 welds out of 1,000,000 would exhibit an increase of 0.001 Ω or greater.

Extreme Ambient Temperature Tests: All welded pair resistance measurements from −55 to 200°C were well below 0.010 Ω.

Vibration Test: Microassembly stacks vibrated according to Method 204B of MIL Std 202A did not exhibit any visible degradation.

Thus at this stage of the overall program a modular interconnection system had been developed and demonstrated to be reliable. Essentially, the interconnection structure consisted of ten stacked alumina or pyrex wafers—0.020 × 0.600 × 0.600 in.—interconnected on 0.025 in. centers by 20 electron beam welded copper ribbons on each of the four sides of the assembly. The modular system is compatible with both thin-film and semiconductor integrated approaches to microminiaturization; nevertheless, standardization is maintained at the wafer level. The process and interconnection techniques are not confined to the 0.600 × 0.600 in. substrates but, rather, are applicable to practically any wafer dimension and geometry.

The next natural step in the program was the development of a packaging system and the demonstration of its capabilities.

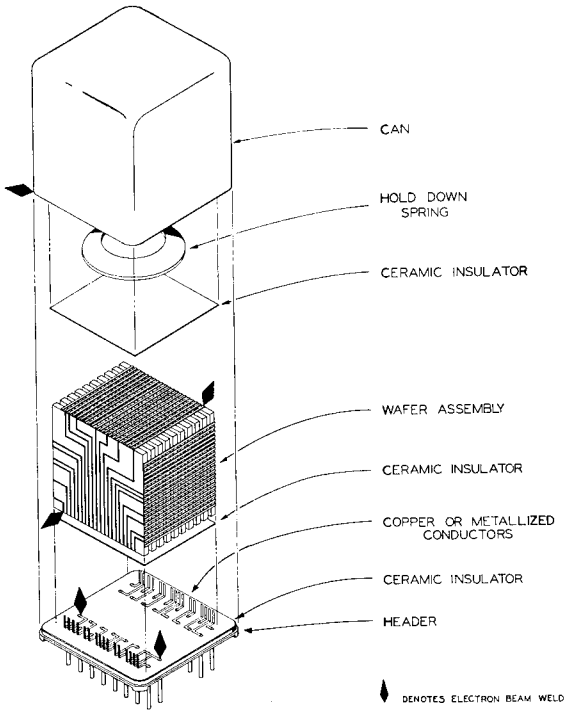

Fig. 10. Hermetic packaging of microassemblies utilizing electron beam processes.

DEVELOPMENT OF PACKAGE SYSTEM

Initially a packaging system—microassembly—was developed which was designed to accept 0.600 × 0.600 in. wafers. Subsequently, the same general approaches have been redirected toward the development of an interconnection–packaging system wherein 0.310 × 0.310 in. wafers are the basic element of the structure. The latter has been defined as the enhanced micromodule.

DEVELOPMENT OF THE MICROASSEMBLY

The microassembly [8] is defined as a hermetic interconnection–packaging structure which comprises ten wafers joined by 80 peripheral electron beam welded conductor ribbons to form a microassembly stack. The latter, in turn, is electrically connected to the pins of a hermetic header by means of interconnection media which transform the 0.025-in. conductive matrix of the microassembly stack into the 0.075-in. grid layout inherent to the 32-pin hermetic header. The composite, in turn, is hermetically sealed within an electron beam welded can. As illustrated in Fig. 10, lateral mounting of the stack coupled with the use of the transform wafer concept imparts considerable flexibility of the interconnection (microassembly–header) network since it is possible to interconnect preselected but randomly located conductor ribbons about the periphery of the stack to one edge of the end wafers. Lateral mounting of the stack imparts a common height to all modules and, furthermore, permits the lateral incorporation of additional wafers within the same can. The microassembly components and their fabrication are described in the following section, and are illustrated in Fig. 11.

Microassembly stacks were fabricated in accordance with previously developed processes [8]. For demonstration purposes, continuous pads rather than discrete terminations were employed. The wafer edges were metallized by the molymanganese technique and electroplated with nickel on all four edges in accordance with previously developed techniques [7].

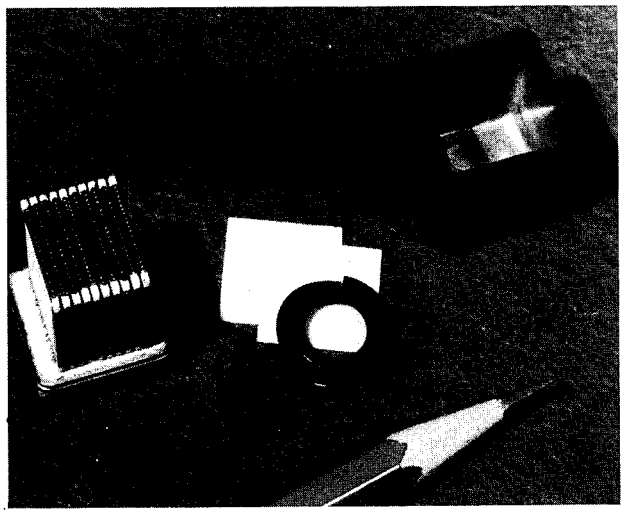

Fig. 11. Microassembly prior to hermetic sealing.

The wafers were spaced on 0.050 in. centers within the stacks and interconnected by twenty 0.002 × 0.010 in. OFHC copper conductor ribbons electron beam welded on 0.025 in. centers to each of the four edges of the alumina wafers.

Headers: Communication between the hermetically sealed microassembly and external circuitry is accomplished through a glass-to-metal header equipped with 32 pins; however, 40 pins can be supplied if required. The overall dimensions of the header are 0.700 × 0.700 × 0.064 in.

Transform Interconnection Media: Electrical continuity between the header pins and the terminations of the transform wafers on the microassembly stack is provided by means of an interconnection matrix consisting of twenty L-shaped copper ribbons (0.002 × 0.010 in.) which are welded to both the header pin extensions and the end transform wafers (Figs. 10 and 11). A ceramic insulating layer separates the conductor ribbons from the header and the microassembly stack.

Eccoceram CS* was selected as a suitable material for the application. This cement is free of polymeric additives and is able to withstand temperatures up to 2000°F; furthermore, it displays excellent adhesion to both metals and ceramics. The cement was applied in the form of a slurry, dried at 170°F for two hours, and then cured at 300°F for 12 hours. After drying and curing the ceramic cement was ground flat to expose the header pin extensions to which the interconnection matrix was electron beam welded. The matrix was fabricated by photoetching the desired network on 0.002-in.-thick copper foil. An alumina wafer (0.010 in. thick) was firmly affixed to the header on top of the conductor ribbons with ceramic cement to ensure electrical isolation between the interconnection matrix and the microassembly stack. Integration of the header with the microassembly stacks was accomplished by welding the copper ribbons to the continuous termination of the two end wafers on the stack, as previously illustrated in Fig. 11.

Hermetic Can: Hermeticity is imparted to the header–microassembly stacks by electron beam welding a stainless steel can to the periphery of the header. The overall dimensions are 0.700 × 0.700 × 0.728 in. Rigidity is imparted to the internal structure by use of a spring, which holds down the microassembly stack within the can (Fig. 11). A ceramic wafer is used to insulate the copper ribbons from the spring.

* Trademark Emerson & Cummings, Inc., Canton, Massachusetts.

Microassemblies: Hermeticity was imparted to the header–microassembly stack composite by sealing within an electron beam welded can. The result and structure were submitted to vibration tests without any evidence of structural or electrical degradation. Helium bomb exposure followed by mass spectrometer tests revealed leak rates lower than 10^{-9} cc/sec.

At present, the microassembly is an interconnection–packaging structure of demonstrated reliability ready for complex functional applications; however, the cost of present integrated and hybrid semiconductor and thin-film circuits does not justify the adoption of this package as a throw-away module at this time.

Consequently, the processes and techniques required for the fabrication of the microassembly interconnection–packaging system were directed to the development of an assembly—enhanced micromodule—based on a 0.310-in.-square notchless micromodule wafer. By so doing, the improved packaging techniques already demonstrated by the microassembly program were naturally integrated into the proven micromodule concept. In this way the technology distributed throughout the industry for the fabrication of microelements can be utilized in an improved package with higher termination density and a more reliable low-cost interconnection joining method.

DEVELOPMENT OF THE ENHANCED MICROMODULE (EMM)

The enhanced micromodule has been previously defined as a hermetically sealed electron beam welded structure wherein up to ten ceramic or glass wafers and associated circuitry are stacked and interconnected by means of nine welded ribbons on a side. A metal-to-glass header provides communication with the external circuitry through twenty pins. The enhanced micromodule is illustrated schematically in Fig. 12, and its components are described below.

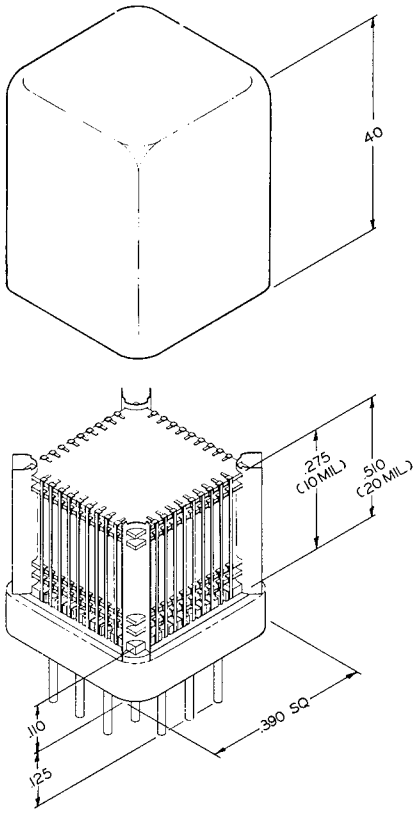

Fig. 12. Schematic of enhanced micromodule.

Microwafer is the generic term given to the basic element of the microwafer stack. This element is 0.310 × 0.310 in. square with groupings of nine terminations on 0.025 in. centers, one group on each edge of the wafer. The wafer thickness is generally 0.010 in. for alumina and 0.020 in. for glass.

A Microelement Wafer is a microwafer consisting of one or more discrete parts or a simple network.

A Microcircuit Wafer is a microwafer consisting of one or more solid state or thin film circuit functions (e.g., flip-flop, gate, etc.). Thus, for instance, a solid state microcircuit may be a microwafer comprising one or more hybrid or integrated semiconductor circuits.

A Microwafer stack is the structure formed when the stacked microwafers are interconnected by welding the conductor ribbons to the appropriate microwafer termination.

The Transfer wafer–header assembly is composed of an hermetic header with twenty 0.017 in. diameter terminal pins located on a 0.075-in. grid. A transfer wafer 0.310 × 0.310 in. with the same termination pattern on its edges as the microwafer is mounted on the hermetic header. The metallized edge terminations of the transfer wafers are connected to the header pins by means of metallized surface conductors which are brazed to the pin extensions.

FABRICATION OF ENHANCED MICROMODULES

The fabrication of the EMM's is presented in a schematic fashion in Fig. 13. In the subsequent sections a detailed discussion of the fabrication steps is included.

Fabrication of Microwafer and Microcircuit Wafers

The basic element of the enhanced micromodule is the substrate which may be either ceramic, such as Al_2O_3 (96%), beryllia* or glass† 0.310 × 0.310 in. on a side and 0.010 or 0.20 in. thick, respectively. Edge terminations are provided to permit communication between the active and passive components on the surface of the substrate and the conductor ribbons which interconnect the stacked wafers, as illustrated schematically in Fig. 12.

After incoming inspection, the substrates are loaded in polymeric tote trays, which serve both as storage bins and holders during the cleaning cycles. After drying, the substrates are stacked in a cross-arm-type fixture, which permits vacuum deposition of chromium and gold on discrete sections of the edges and periphery of the wafer surfaces. Definition of the vacuum deposit on all four edges of the stacked wafers is achieved by means of "comb" masks which are placed in contact with the wafers. Corresponding discrete pads on the surfaces are obtained by means of spacer masks, which are inserted between each substrate. The wafer holding fixture is designed to hold the substrates at the corners. Wafer tolerances are taken up by referencing all the substrates against two perpendicular edges.

After loading of the wafers and positioning of the surface masks, up to six fixtures are loaded in the "ferris wheel" device (Fig. 14) which is mounted within a 4-in. Veeco vacuum system. Operation of the overall structure is such that while the "ferris wheel" is revolving, the wafer holding fixture also rotates about its own axis. Thus, all four edges of the wafers are impinged upon by the evaporant flux emanating from two sources located outside the "ferris wheel" and below its axis. Both chromium and gold sources are located at these two points. Chromium is deposited first to assure a tenacious bond between the metallic coating and the ceramic. A heater assembly employing quartz lamps envelops approximately two-thirds of the "ferris wheel" surface. According to standard practice, the substrates are outgassed at 350°C for approximately one-half hour after a pressure of 10^{-5} torr has been reached. Deposition of the chromium (~100 Å), and gold (~1000 Å) follows at approximately 300°C. After cooling to room temperature, the microwafers are again loaded in the "ferris wheel" with their surfaces unmashed except for a small "picture frame" strip around the periphery. When a pressure of approximately 10^{-5} to 10^{-6} torr is reached, aluminum is deposited on the inner exposed surfaces of the microwafers from a source placed within the rotating "ferris

* Beryllium Corp., Reading, Pennsylvania-Brush Beryllium Corp., Cleveland, Ohio.
† Pyrex, Corning Glass Co., Corning, New York.

wheel." The outer surfaces of the microwafers are coated from a source placed underneath the "ferris wheel." The aluminum area film is deposited to interconnect or short-out the terminations for electroplating. The system is brought up to atmosphere and the microwafers are subsequently loaded in an electroplating fixture. The loaded fixture is placed in an anodizing bath to promote build-up of an oxide coating on the vacuum-deposited aluminum interconnecting film. Consequently, the latter is not electroplated during the subsequent operation. The fixture with the anodized wafer is subsequently rinsed off and placed in the plating facility, wherein the discrete terminations are electroplated to an overall thickness of 0.001 ($\pm$0.0002) in.

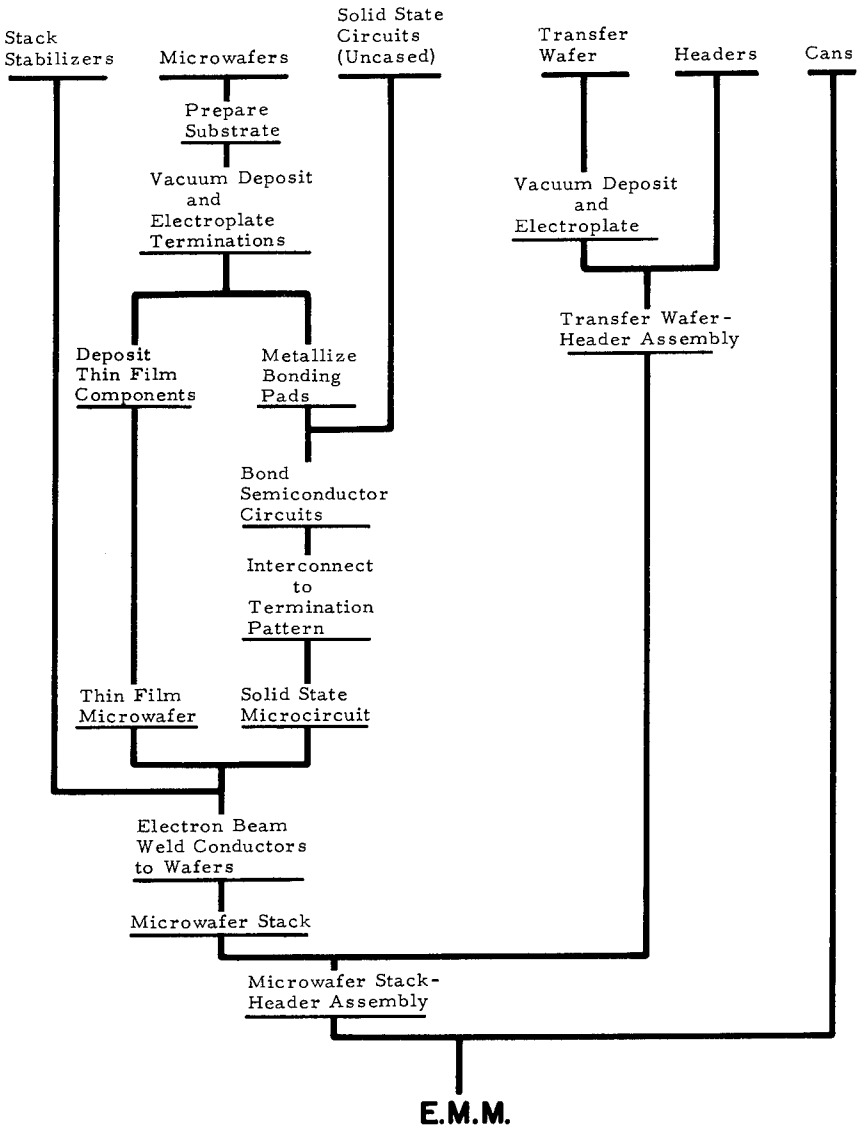

Fig. 13

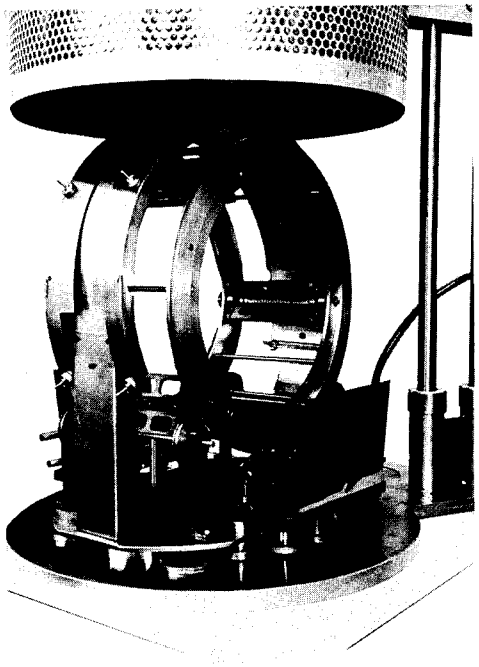

Fig. 14. "Ferris wheel" fixture for vacuum deposition of terminations on microwafers.

The fabricating of the microcircuit wafers requires additional metallic coatings and paths on the surface of the microwafer to permit bonding and interconnection of the uncased semiconductor circuits. Consequently, an additional coating operation is required; i.e., after application of the terminations the wafers are again loaded in the "ferris wheel" with the surfaces exposed to the evaporant, and a gold-chromium area film is deposited on one or both surfaces.

Microwafers compatible with thin-film and solid circuits are illustrated in Fig. 15 in the as-received condition and also after vacuum deposition and electroplating of the discrete terminations.

After fabrication, both microwafers and microcircuit wafers are optically and electrically inspected and stored.

Fabrication of Solid-State Microcircuits

Solid-state microcircuits are fabricated by eutectic bonding (Au–Si, 370°C) the uncased functional electronic blocks to the gold film on the microwafer surface. Other techniques employing solders are available; however, the eutectic technique is most commonly used in view of its reproducibility. After the semiconductor is bonded to the microwafer, interconnections are made between functional blocks and microwafer terminals by thermocompression bonding.

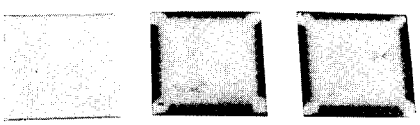

Fig. 15. Microwafers for thin-film and solid-circuits integrations at various stages of termination application.

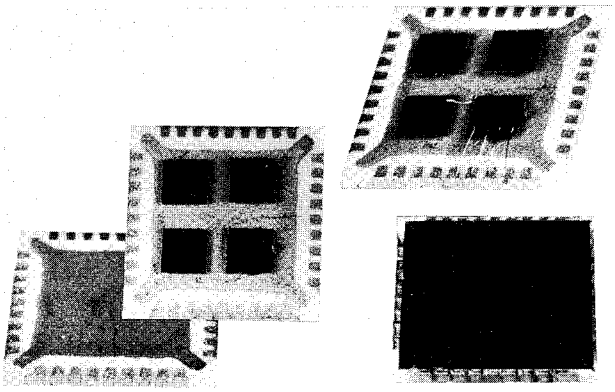

Fig. 16. Solid-state microcircuits.

A sample of a solid-state microcircuit is illustrated in Fig. 16 in conjunction with thin-film passive component microelements. Four Fairchild "S" circuits were bonded to the illustrated microwafer. Bonding was accomplished by heating the substrate on a hot post to about 400–425°C, at which time each functional block was picked up sequentially with a vacuum probe, which upon bringing the chip in contact with the wafer imparted a vibrational motion to the chip thus disrupting any surface contamination and promoting bonding. Subsequently, at lower temperatures (~300°C) gold leads were thermocompression bonded to the proper terminals on both the semiconductor circuit and on the microwafer. The semiconductor terminals are vacuum-deposited aluminum on SiO_2, whereas the microcircuit wafer terminations are gold–chromium coatings. Chip mounting and lead attachment thermocompression bonding machines are used for this task.

Fabrication of Thin-Film Microcircuits

Thin-film passive resistors and capacitors may be deposited on either the same terminated microwafer or separate ones depending upon the circuit requirements. In actual applications several approaches may be pursued: (a) resistor and capacitors on the same microwafer, but opposite surfaces with or without active components, and (b) capacitors and resistors on separate microwafers with or without active components. In the former case the surface upon which the capacitor is to be deposited is provided with a glass finish over the ceramic, whereas in the latter case, a glass substrate may be used for the capacitors. In addition to alumina and glass, beryllia, sapphire, etc. may be used, depending upon the particular application.

Several approaches may be pursued in the fabrication of thin-film microcircuits and, actually, the latter may be used in conjunction with semiconductor circuits. Furthermore, in any one module, thin-film and solid-state microcircuits can be used interchangeably since a common wafer form factor has been standardized.

The passive components may be fabricated by vacuum deposition, sputtering and anodizing, pyrolytic reactions, cermet firing, etc. The technique which has been developed and standardized at Hamilton Standard is based on vacuum deposition of resistive and capacitive area films followed by electron beam scribing into individual units, which are, in turn, trimmed to value by the same subtractive process.

Chromium has been selected and used extensively as the thin-film resistive material with silicon monoxide as the protective overlay. The vacuum deposition of chromium thin film resistors has a relatively long history since it has been pursued by several investigators [9–12]. Furthermore, these investigations have shown that chromium films are stable up to 300 to 400°C with low temperature coefficients. A program designed to fabricate reliable chromium thin-film resistors has been underway at Hamilton Standard. Chromium on alumina represents a good compromise of the previously outlined requirements. Chromium can be readily

vaporized in a controlled and reproducible fashion with an electron gun heat source; furthermore, it is particularly well suited for electron beam scribing of resistive patterns.

Aluminum and silicon monoxide constitute the electrode and dielectric materials of the capacitor.

The vacuum-deposition system used for the fabrication of the thin-film resistors is illustrated in Fig. 17. A similar facility is used for capacitors. Both systems are provided with controls and instrumentation to permit deposition of the thin films in a quasi-automatic fashion. Specifically, the instrumentation is designed to monitor and/or control the rate of evaporation, period of evaporation, substrate temperature during outgassing, deposition and annealing, film resistance, residual gas pressure and composition, thickness of the dielectric layer, and electrical characteristics of the resistive films. Since cleanliness and controlled atmospheric conditions are essential, all critical operations are performed in a "white room" facility.

After the deposition cycle, the area films are loaded in magazine-type dispensers which are loaded within an electron beam system equipped with a machine which has both microwelding as well as scribing or etching capabilities (Fig. 18). The machine is complemented with a high-speed tape programmer for control of the electron beam deflection and parameters. An additional tape reader is provided for the work-table motion programming. Typical passive components prepared by the described technique were previously shown in Fig. 16.

At present, one type of component is mounted on any one microwafer; however, techniques are under development to integrate thin-film passive components with uncased active devices on the same microwafer to form hybrid microcircuits.

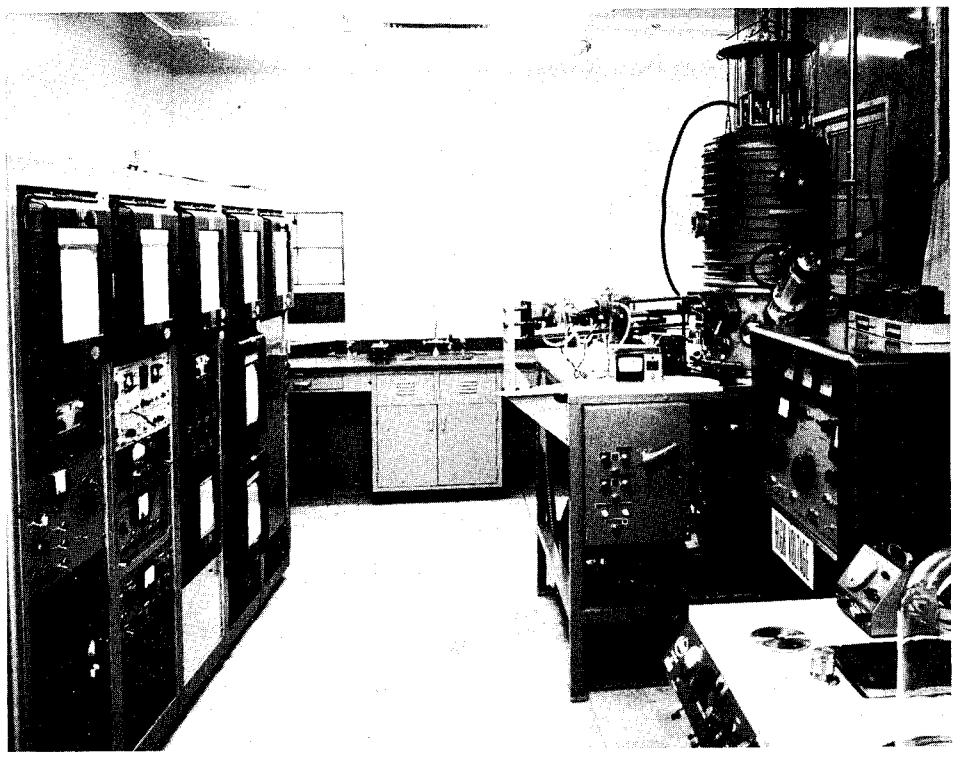

Fig. 17. Vacuum-deposition system.

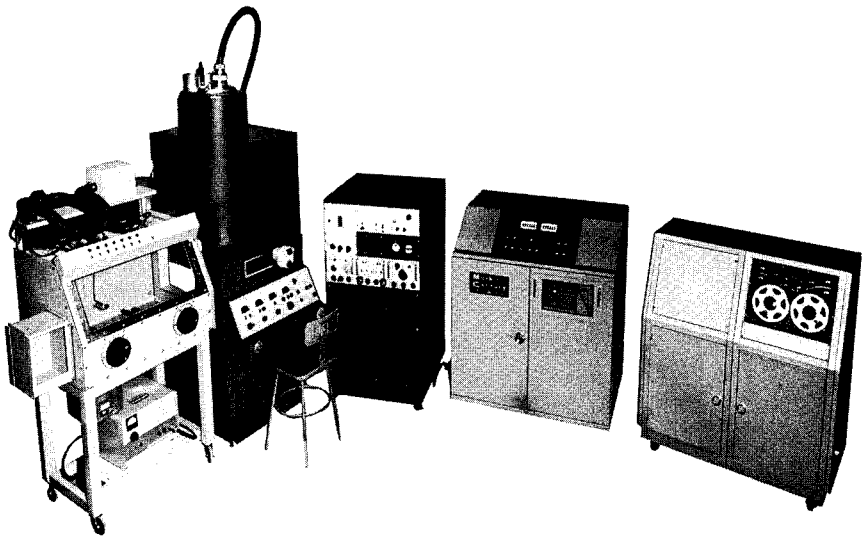

Fig. 18. Electron beam system.

Fabrication of Microwafer Stack

The microwafer stack is the structure formed by interconnection of the microwafers by means of conductive ribbons electron beam welded to the appropriate terminations.

The previously fabricated microwafers and microcircuits are assembled in a fixture, and interconnection matrices are placed over the four edges of the stack so as to match the terminations pattern. The OFHC copper matrices are prepared by photoetching techniques. It is

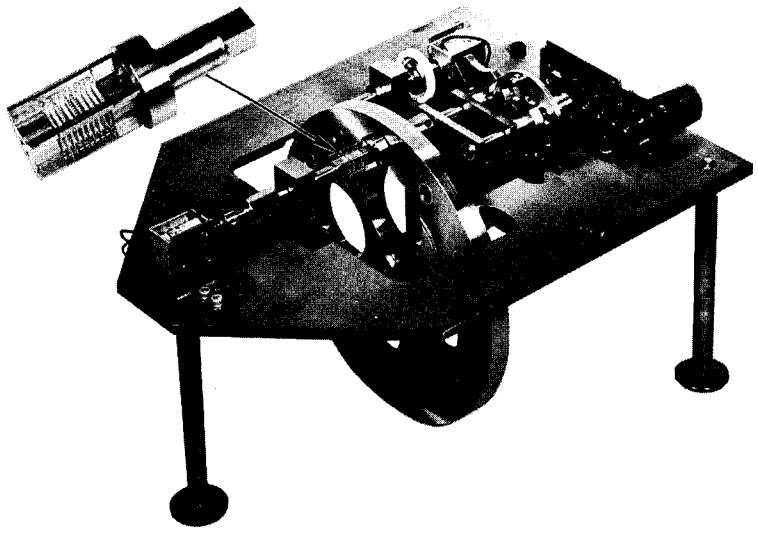

Fig. 19. Multimicrowafer stack welding fixture.

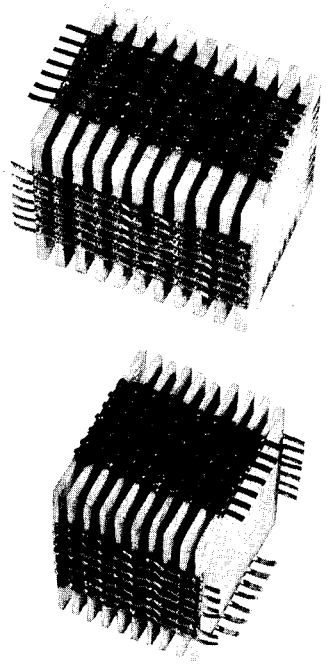

Fig. 20. Microwafer stacks—0.010- and 0.020-in.-thick alumina wafers.

recalled that the nine 0.002 × 0.010 in. ribbons are spaced on 0.025 in. centers so as to match the terminations on the microwafers. The fixture, in turn, is inserted within the multiweld apparatus (Fig. 19), which is accurately positioned by means of dowel pins on the electron beam machine programable table. Subsequently, welding of the conductor ribbons to the microwafer terminations is carried out incrementally in a mechanized fashion; i.e., after each welding operation along the edge of any one wafer the work table is stepped 0.025 in. to the next welding station, at which time the electron beam is activated and made to go through its preprogrammed welding cycle [7]. After a row of microwelds has been completed the table is stepped to bring the next microwafer edge into the welding sequence. The table steps either 0.025 or 0.050 in., depending on the microwafer center-to-center distance. Two microwafer stacks are illustrated in Fig. 20. The former illustrates a stack composed of ten 0.010-in.-thick microwafers on 0.025 in. centers, whereas, the latter consists of ten 0.020-in.-thick microwafers spaced on 0.050 in. centers.

As previously shown in Fig. 12, the microwafer stacks are to be equipped with stack stabilizers to impart rigidity to the structure, prevent shorting of the conductor ribbons to the can, and provide a thermal path directly from the microcircuit to the header assembly. Techniques are under development to use the stack stabilizer in conjunction with the microwafer stack welding jig to serve both as a wafer spacer and fixturing aid.

Fabrication of Transfer-Wafer Header Assembly

The purpose of the transfer wafer is to permit translation of an interconnection system on a 0.025-in. grid layout to one on a 0.075-in. matrix. The former is inherent to the microwafer stacks periphery, whereas the latter is the center-to-center distance between the feed-throughs or pins of the hermetic headers. Twelve of the twenty stack-to-header connections are made directly to the header pin extensions. The remaining eight interconnections are achieved through

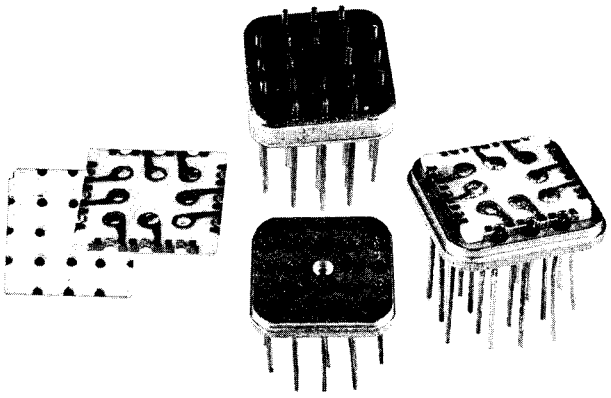

Fig. 21. Header–transfer wafer component.

the transfer wafer. The latter is a notched 0.020 × 0.310 × 0.310 substrate with eight openings on the 75-mil grid defined by the pattern of the notches (see Fig. 21). The peripheral and edge terminations are applied in the same manner as for the microwafers, whereas the surface conductors are deposited through a mask or obtained by electron beam scribing or photoetching of an area deposited film. The notches of the transfer wafers need not be electroplated since the copper ribbons protruding from the microwafer stacks are welded directly to the header pin extensions.

The basic element of the assembly is the header. Compression and matched types of seal headers have been developed and are available.

Integration of the transfer wafer with the header is accomplished by mounting of the composite within a fixture, insertion of alloy spheres, and brazing within a hydrogen furnace. A header-transfer wafer assembly is illustrated in Fig. 21, at various stages of fabrication.

Fabrication of Header Assembly—Microwafer Stack

The fabricated header-transfer wafer assembly is integrated with the microwafer stack within the same basic fixture which was illustrated previously (Fig. 19); however, one of the end plates is replaced with a jig which accepts the header-pins. The process is basically the same as for the welding of the microwafer stacks.

Hermetic Sealing—Enhanced Micromodules

Header–stack assemblies composed of semiconductor and/or thin-film microcircuits with uncased devices are vacuum baked prior to hermetic sealing to minimize the amount of entrapped water vapor (dew point is 100°C). After vacuum baking the assemblies are passed

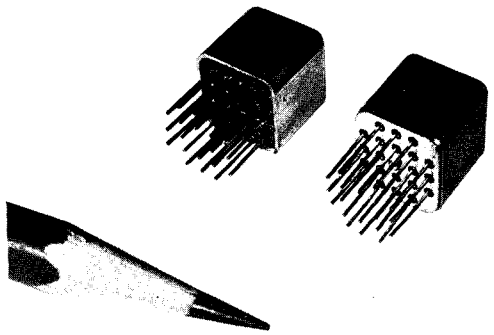

Fig. 22. Enhanced micromodules.

through the previously illustrated dry box (Fig. 18) and transferred to the electron beam machine, where the cans are end welded to the header. The dimensions of the nickel which can be used for hermetic sealing of the assembly are 0.390 × 0.390 × height (up to 0.8 in. max). Hermetically sealed enhanced micromodules are illustrated in Fig. 22. Dimensions were given previously in the schematic in Fig. 12.

After electron beam sealing, the units are leak checked by placing within a helium bomb for about four hours followed by leak checking in a Veeco mass spectrometer. Typical leak rates are lower than 10^9 cc/sec.

PILOT LINE PRODUCTION CAPABILITY

A pilot line for the production of 50 enhanced micromodules or 200 microcircuits per eight-hour shift has been designed and is in the final process of installation. Actually, this step represents the integration of a number of individual techniques and processes which, for the most part, have been developed and demonstrated to be practical and reliable throughout the course of previous programs [6-8]. The primary tool of this facility is the electron beam machine with auxiliary equipment for automatic operation. In addition to the vacuum-deposition systems, the pilot line embodies electroplating and photoetching facilities and special tools required to fabricate, assemble, and test the functional enhanced micromodules at various stages of fabrication.

A program is underway to enhance the capability of the present pilot line to a production capacity of 100 enhanced micromodules per eight-hour shift. Each module will comprise ten microwafers.

The tools and fixtures which constitute the pilot line being assembled have been previously described in the section wherein the fabrication of enhanced micromodules was discussed. In the initial design of these tools and associated techniques, provisions were made so that in most cases their capability could be extended to fabricate 100 enhanced micromodules per eight-hour shift. Specifically, the "ferris wheel" fixture, which is used to vacuum-deposit the edge terminations can be readily adapted to terminate well over 1000 microwafers per run. In addition, several hundred solid-state microcircuit wafers may be supplied with metallized pad for bonding of uncased semiconductor devices.

The electroplating facility and associated fixturing have a production capability well in excess of the requirements. The vacuum-deposition systems and electron beam scribing machines are capable of producing well over 1000 passive microelements per eight-hour shift. It is recalled that scribing of both resistors and capacitors is carried out in an automated facility; i.e., the microwafers with area films are inserted in a magazine, several of which are loaded within the scribing unit. Successive microwafers are positioned under the electron beam and scribed to exact value by monitoring during the actual scribing process. When the preset value of resistance or capacitance has been reached, the etching process is stopped immediately, and the next area film brought under the beam.

The fabrication of the transfer wafer-header element is accomplished in two steps: wafer metallizing and assembly of components. Metallizing is carried out in the "ferris wheel" production device previously described. Integration of the wafer to the header is carried out by furnace brazing within suitable fixtures.

Bonding and interconnection of the uncased semiconductor devices and circuits are carried out, respectively by the standard eutectic brazing and thermocompression bonding techniques. At present, the bonding process is a standard manual operation as practiced throughout the industry.

The required production capability is available; however, these operations, at present, are relatively time consuming when compared to the other steps in the process.

Electron beam welding of the microwafer stack as well as the hermetic sealing operation are automatic processes which inherently have capabilities compatible with present and future requirements. At present, contact during welding between the copper ribbon and the metallized termination during welding is assured by means of a finger hold-down fixture which is automatically energized prior to and after each microweld operation. Successive welds are made

by bringing the next ribbon-termination intersection under the beam and repeating the above procedure. This technique produces welds at rates considerably in excess of one weld per second. It is recalled that the actual welding time is only about 5 msec. The overall weld time will be drastically reduced when all the welds along one edge of a microwafer are made entirely by progressive beam deflection, and table motion is used only to step from one wafer edge to the next one. This approach requires refinement of ribbon holding-down concepts now under development.

Inherently, electron beam processes are denoted by high speed and programming capability. In general, the time required to carry out any one operation is extremely short provided the proper fixtures are available. The latter may be fairly complex to permit the full realization of the tool's capabilities. Standardization of the interconnection–packaging structural elements and accompanying electron beam assembly processes results in universal tooling and, consequently, reliable, low-cost electronic equipment.

Several linear and analog functional modules are in the process of becoming available in the enhanced micromodule package. Typical units comprise two 5-Mc flip-flops, or four gates per structure. A 3.0 W servo-amplifier, as well as differential amplifiers, is also being packaged in this fashion. For high-thermal-dissipation analog circuits, the module is backfilled with helium prior to hermetic sealing. The above units encompass thin-film passive components and uncased transistors and diodes. In addition, a larger number of ten-bit adder enhanced micromodules are also in the developmental stages of assembly. The latter embody integrated semiconductor circuits.

As the cost of semiconductor and thin-film circuits decreases, it will be possible to package more circuitry per enhanced micromodule and still retain the throw-away concept. The interconnection capability of the structure can be increased by severing of the copper ribbons so that the same conductor can accomplish several interconnection functions. This operation can be accomplished quite readily with suitable templates without degrading the structural integrity of the microwafer stack since the latter is strengthened with the stack stabilizers.

CONCLUSIONS

An interconnection–packaging system—enhanced micromodule—has been developed which is compatible with integrated and hybrid semiconductor and thin-film circuits. The salient features of the module are flexibility and demonstrated reliability of the interconnection system as well as the extreme environment capability which naturally results from the fact that the package is hermetically sealed and free of any polymeric materials. In addition, the structural parts of the enhanced micromodule are standardized down to the microwafer level; however, complete freedom exists at this level in terms of electrical design and type of microcomponent and circuit which can be used.

Standardization of the parts has been conducive to the establishment of an automated assembly system with high production rates. The primary equipment of this system is an electron beam machine which has been complemented with work table and electron beam programming capabilities. The standardization of the structural components and production assembly processes and tools assure high reliability and low cost.

In addition, the enhanced micromodule offers another significant cost advantage, since by the use of uncased semiconductor circuits and devices, the need for the relatively expensive flat packs and TO 5 cans is obviated. Very high microminiaturization efficiencies result. Furthermore, most of the interconnection is accomplished within the module rather than through expensive multilayer printed boards.

Thus, the enhanced micromodule provides a highly versatile, low-cost interconnection–packaging system for relatively complex integral electronics.

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This program was conducted under technical cognizance of Messrs. R. A. Gerhold, S. S. Bassler, United States Army Electronic Research and Development Laboratory, Fort Monmouth, New Jersey.

Figure 11 is through the courtesy of the U.S. Army Signal Research and Development Laboratory, Fort Monmouth, New Jersey, and is a U.S. Army Photograph.

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Packaging a Thin-Film High-Speed Counter

H. G. STECH
Microelectronics Section, Orlando Division, The Martin Company, Orlando, Florida

The packaging design of a high-speed counter, 9 in.^{3} in volume, with a substrate density in excess of 10^6 parts/ft^3 and an overall packaging density of 170,000 parts/ft^3, is described in this paper. The packaging concept, modular breakdown, substrate layout, and interconnections of the 3 by 6 by $\frac{1}{2}$ in., 6-oz counter are discussed, and the design of the external package for protection and for integration with the rest of the overall system is covered.

IN THE EARLY stages of their thin-film program the Martin Company recognized the possibility of combining high-speed transistors and thin films in special counter and computer applications for missiles, test and check-out equipment, and other devices. The counter was required to have minimum size, weight, and power consumption, and operate over a temperature range of -45 to $+55$°C. In addition it had to withstand a 3-msec shock of 50 g's applied in the three mutually perpendicular planes. Vibration tests including a 10 g acceleration at frequencies from 10 to 500 cps for periods of 30 min in each of three mutually perpendicular planes were also a requirement.

Priority of requirements was established as follows:

1. Functional performance including reliability and accuracy.
2. Delivery time.
3. Performance over environmental range.
4. Minimum size, weight, and power consumption.

The packaging concept originally proposed included the readout portion and counter electronics in one unit. Total volume of 10.3 in.^{3} and a weight of $4\frac{1}{2}$ oz without potting was anticipated. Potting to ensure that the shock and vibration requirements could be met would increase the weight to 8 oz.

Martin–Orlando was particularly concerned at this point about heat dissipation as this amount of thin-film electronics had not been assembled in one package previous to this time. Thermal studies had been ultraconservative and indicated that we would have a temperature problem. The weight and volume criteria were also tight and would require careful design consideration.

Finally, two packages were decided upon. The display package used nixie tubes mounted either vertically or horizontally. Counter electronics would be in a separate package.

A package system study was made to determine the modular (substrate) breakdown, substrate size, interconnection method, maintenance provisions, and overall package design.

A study of the circuit was made to determine the functional breakdown of the circuit. The study was to indicate if repetitive modules or modules that could be used in more than one place in the system could be adapted to the design.

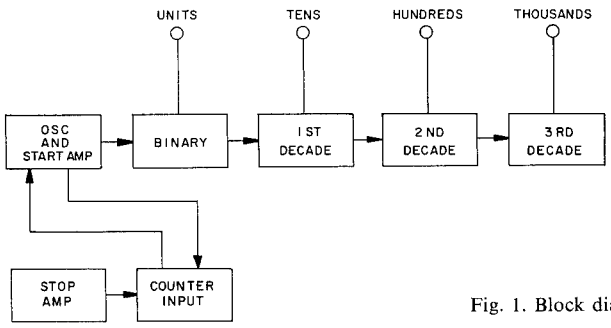


Fig. 1. Block diagram of thin-film high-speed counter.

The study revealed that three decades of counting following the highest frequency counting stage could be designed so that they would be identical. Remaining functions would not permit repetitive circuits. Figure 1 is a block diagram of the thin-film high-speed counter.

The binary is the functional circuit element of the initial counting stage. This element is repeated in each of the other three counting stages or decades. It was assumed that the binary could be a functional module in each decade. Consequently, the components of the binary were not included in the counting decades for the purpose of the functional circuit block component study (Table I).

It was believed probable that the counter might be maintained by replacing a defective module with a new one and disposing of the faulty module. However, costs of components in the counting decade blocks would be too great for this maintenance approach.

To reduce costs, counting decades were further broken down into a nixie driver block and a ring counter block (Table II). Attached component costs for the nixie driver is $220.00 and for the ring counter, $3100.00. Cost of the components on the ring counter was on the high side but it was decided to proceed with the thought that quantity prices could very possibly be lower.

The counter circuits were then breadboarded (Fig. 2). All modular functions previously established were maintained in the breadboard assembly. This procedure was used so that the breadboard would be equivalent to the thin-film unit. It was hoped that this would minimize circuit problems that might result from the conversion from discrete off-the-shelf components to thin-film components. The breadboard circuits were analyzed for worst-case conditions and temperature tested over the required range. All possible care was taken to firm the circuit design before starting on the thin-film layouts.

TABLE I

Functional Circuit Block Component Study

Block	Components				Attached component cost*
	Deposited		Attached		
	Resistors	Capacitors	Transistors	Diodes	
Oscillator and start amplifier	40	13	12		$120.00
Stop amplifier	22	12	6	2	64.00
Counter input	37	2	21	4	218.00
Binary	41	4	22	4	228.00
Counting decades	103	0	51	10	530.00

* Assumed quantity costs: Transistors $10.00 each, diodes $2.00 each.

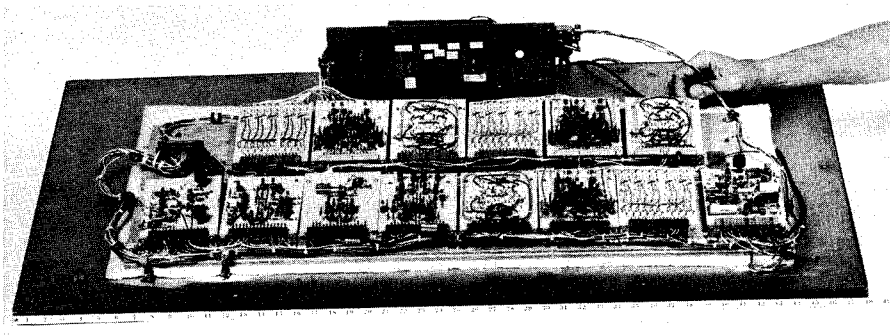


Fig. 2. Breadboard.

After breadboard tests were completed and the circuit design and component selection adequately proven, packaging design of the counter was begun.

It was necessary that maintenance be accomplished without a soldering iron or use of similar joining techniques. Consequently, this required the use of some type of connector. The means of interconnecting from connector to connector was then considered. More than one method of interconnection was possible. For example, welded matrix, multilayer printed boards, and point-to-point wiring could be used. There was a space in the system that would accommodate a thin flat package approximately 3 in. in one dimension and within 6 to 9 in. in the other dimension. We would not achieve maximum packaging density with this configuration, but it would be the best configuration for this particular application. This package type had other potential advantages in that a two-sided printed board could be used both for interconnection and supporting structure. With the substrates mounted parallel to this board, there would be sufficient access for trouble-shooting with all modules assembled in the unit.

Center-to-center distance of module-to-board connections was established as 0.100 in. This distance would permit the use of 0.062-in. pads on the board and a 0.015-in. line going between the pads with 0.012-in. clearance on each side under nominal conditions. A two-sided board was desirable because this could be made in-house within the schedule requirements. The modular functions were again reviewed to determine the number of input–output connections (Table III).

The determination of the maximum number of input–output connections and the connector pin spacing of 0.100 in. enabled the first step to be taken toward substrate size determination. The substrate with the maximum number of input–output connections, the nixie driver

TABLE II

Revised Functional Block Breakdown

Function	Number Used
Oscillator and start amplifier	1
Stop amplifier	1
Counter input	1
Binary	4
Ring counter	3
Nixie driver	3

TABLE III

Input–Output Connection Study

Modular Function	Number of Connections
Oscillator and start amplifier	13
Stop amplifier	9
Counter input	22
Binary	15
Ring counter	19
Nixie driver	24

with 24, was considered and so there was 2.4 in. of lineal edge distance required per substrate for connections. We had concluded as a result of previous studies that the maximum substrate size we would use would be 1.20 × 2.00 in. Since 2.4 in. exceeded these dimensions, it was decided that the connections would be placed on opposite edges of the substrates tentatively establishing one dimension as 1.2 in. The area required for the deposited components and conductors was another factor to be considered in determining substrate size.

At this point, a trial layout was made to assist in the determination of substrate size. Trial layout proceeded from the previously determined dimension of 1.2 in. Capacitors, in general, require more area than resistors. Consequently, the functional module with the greatest number of capacitors was selected for the trial layout. The oscillator and start amplifier had

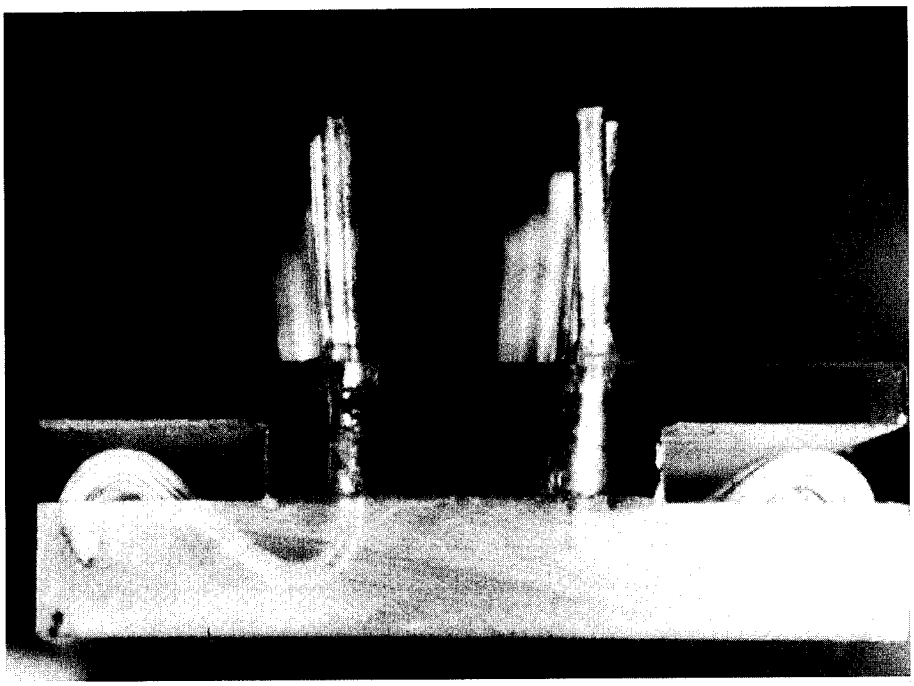
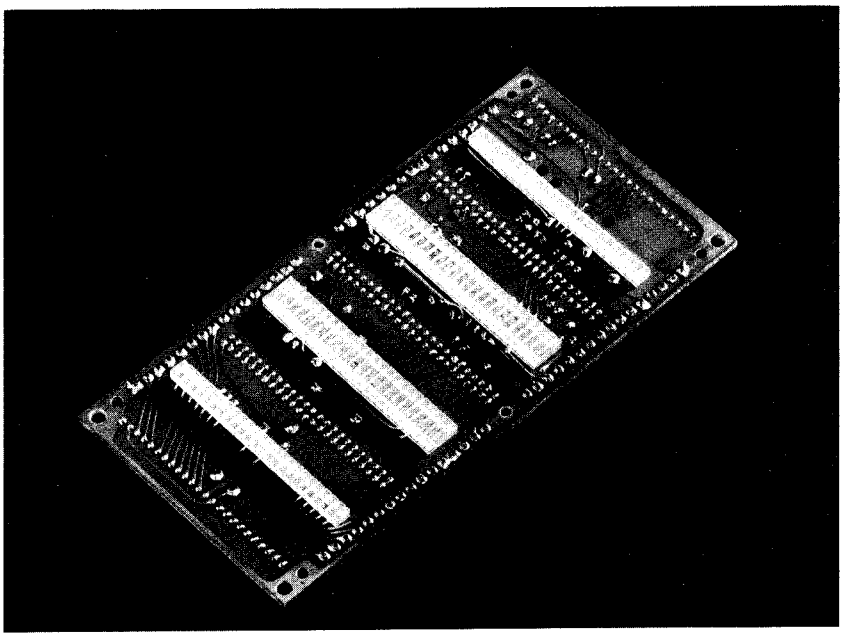


Fig. 3. Connector, magnified.



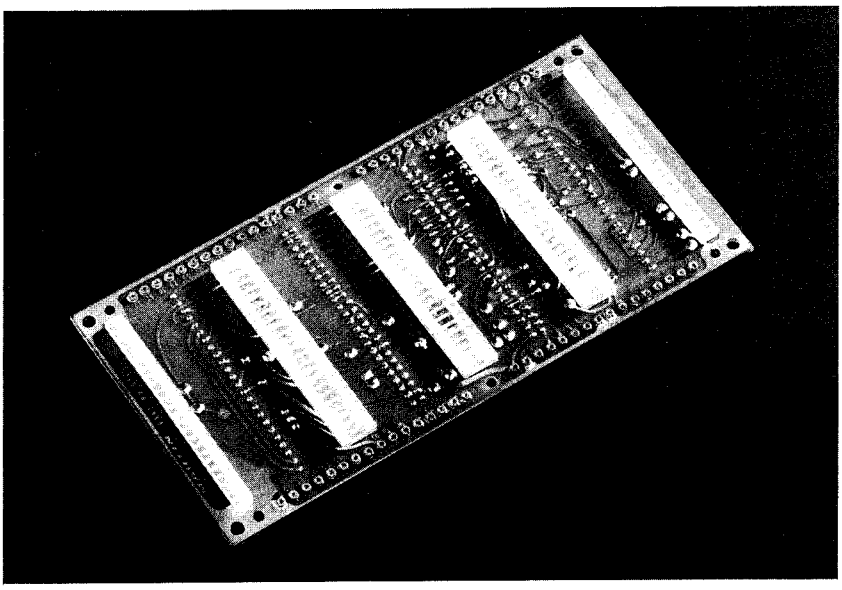


Fig. 4. Board and connectors.

approximately twice as many resistors as the function with the next greatest number of capacitors, which was the stop amplifier. The oscillator and start amplifier layout was incorporated on a 1.2 × 1.2 in. substrate of soda lime glass, 0.030 in. thick. One discrete 0.01-μF capacitor was attached for electrical reasons.

As the oscillator and start amplifier had the greatest number of components, it was logical to assume that the other functions could also be laid out on this size substrate. With connections on opposite edges of the substrate, the most suitable plug-in system was deposited edge connections. Each substrate had 12 pads 0.060 in. wide on 0.100 in. centers deposited on opposite sides of the substrate. A connector with the ends of the contact slot open and pins extending from the connector at 90° to the slot was soldered to the printed interconnection board. The connectors would be mounted on the board with slots facing one another and the substrate would be inserted between these connectors. Space approximately 3 in. in width was available in the system and this would accommodate two substrates side by side. There would be several rows of two substrates each; consequently, two types of connectors were needed, one with contacts and a slot for insertion of substrates on one side only and another that would take a substrate on each side. A standard connector of the type desired was not located and connectors were designed to provide a spring-loaded contact with 0.015-in.-diameter beryllium copper wire in a plastic body as shown in Fig. 3.

As the substrates entered from the end of the connector, the first substrate pad passed all 12 contacts, and it was anticipated that this would wear the gold contact pads on the substrates. An overcoat of chrome was deposited on the pads to reduce this effect. The corners of the substrates were also beveled to provide entry to the contacts.

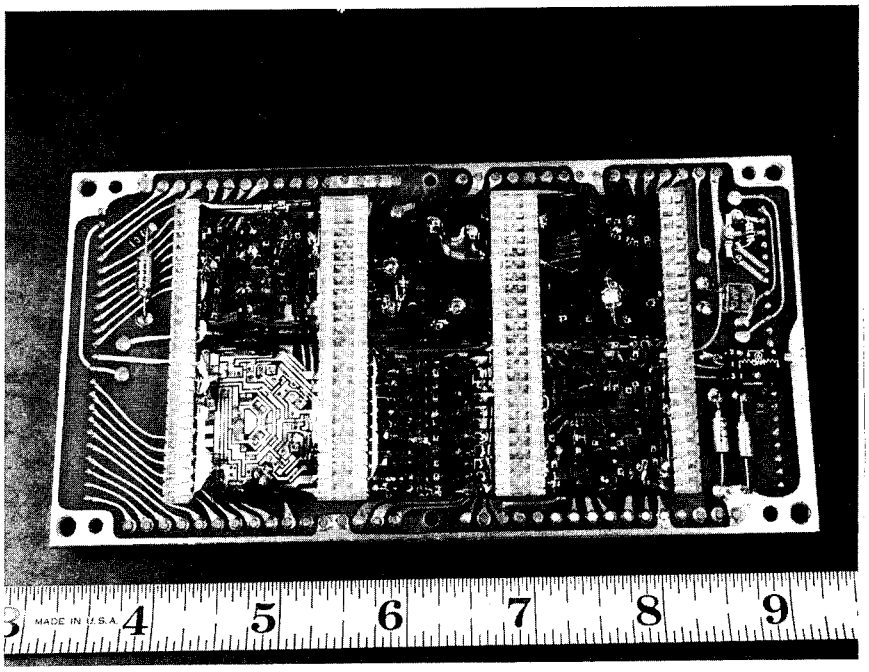
A $\frac{3}{32}$-in.-thick epoxy resin fiberglass board, copper clad both sides, was used for interconnections between substrates. A minimum line width of 0.022 in. was maintained wherever possible with short narrowed sections in particular areas of congestion. The 2-oz conductors were gold-plated (Fig. 4) and connections from one side to the other on the board were made by feed-through "Z" wires.

The board was laid out to accommodate four rows of substrates on one side and three rows on the other. Thirteen substrate modules had to be assembled and interconnected. Seven were placed on one side of the board and six on the opposite side with space for one spare substrate. It was necessary to offset the connectors on one side in relation to the other so that the pins would be clear for the printed wires (Fig. 5).

The outer case or overall package was designed so that it would be suitable for die-casting if quantity procurement were to develop. The first model was made by machining the desired cover contours in a $\frac{3}{16}$-in.-thick aluminum plate. The balance of the counter functions were designed and the layouts completed on a 1.2 × 1.2 × 0.030 in. glass substrate with a surface finish of 1 rms maximum. Figure 6 is an exploded view of the counter assembly.

The sizes of the resistors and capacitors were calculated using the following thin-film constants: Resistance: 500 Ω/square, 8 W/in.^{2}; Capacitance: 0.129 μF/in.^{2}; Conductors: 0.02 Ω/square. In addition, it was specified that the minimum dimension of a resistor would not be less than 0.010 in. This minimum was used for any thin-film deposition and for separation between deposited components. The parts were laid out on the substrate in a process similar to that used for printed board component locations, and conductors were planned accordingly. Conductor resistance was checked and the branch current was determined. This permitted increasing conductor width where losses would occur that might influence circuit performance. The leads of attached components, such as transistors and diodes, were used to bridge conductors to eliminate crossovers in the deposited pattern. Crossovers can be fabricated in the thin-film deposition but they represent additional capacitance in the circuit and normally require an additional step in the deposition process. Resistors were essentially chromium deposits and conductors were gold. The thin-film capacitors consisted of two deposited aluminum plates separated by a layer of deposited silicon monoxide.

A few discrete components were used on the interconnection board for various reasons. A trimpot and crystal were mounted as they could not be made in thin-film form and were too large to put on a substrate. Three large-value capacitors and two resistors were added later when testing indicated they were required.



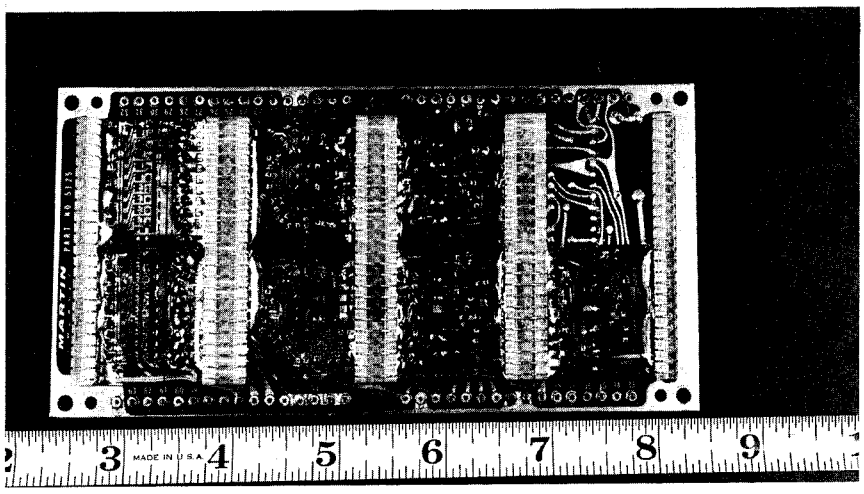


Fig. 5. Board with substrates assembled.

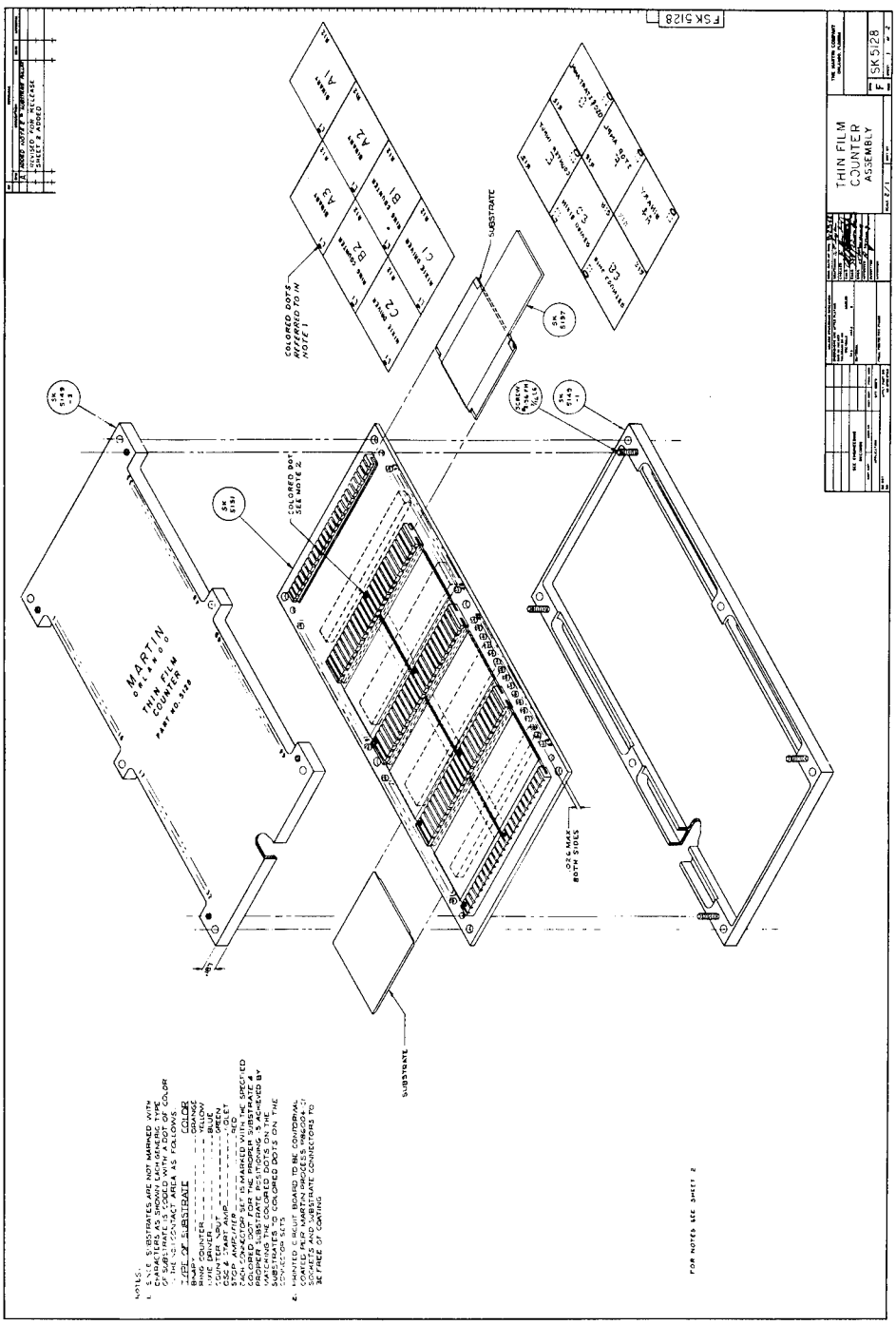


Fig. 6. Exploded view—counter assembly.

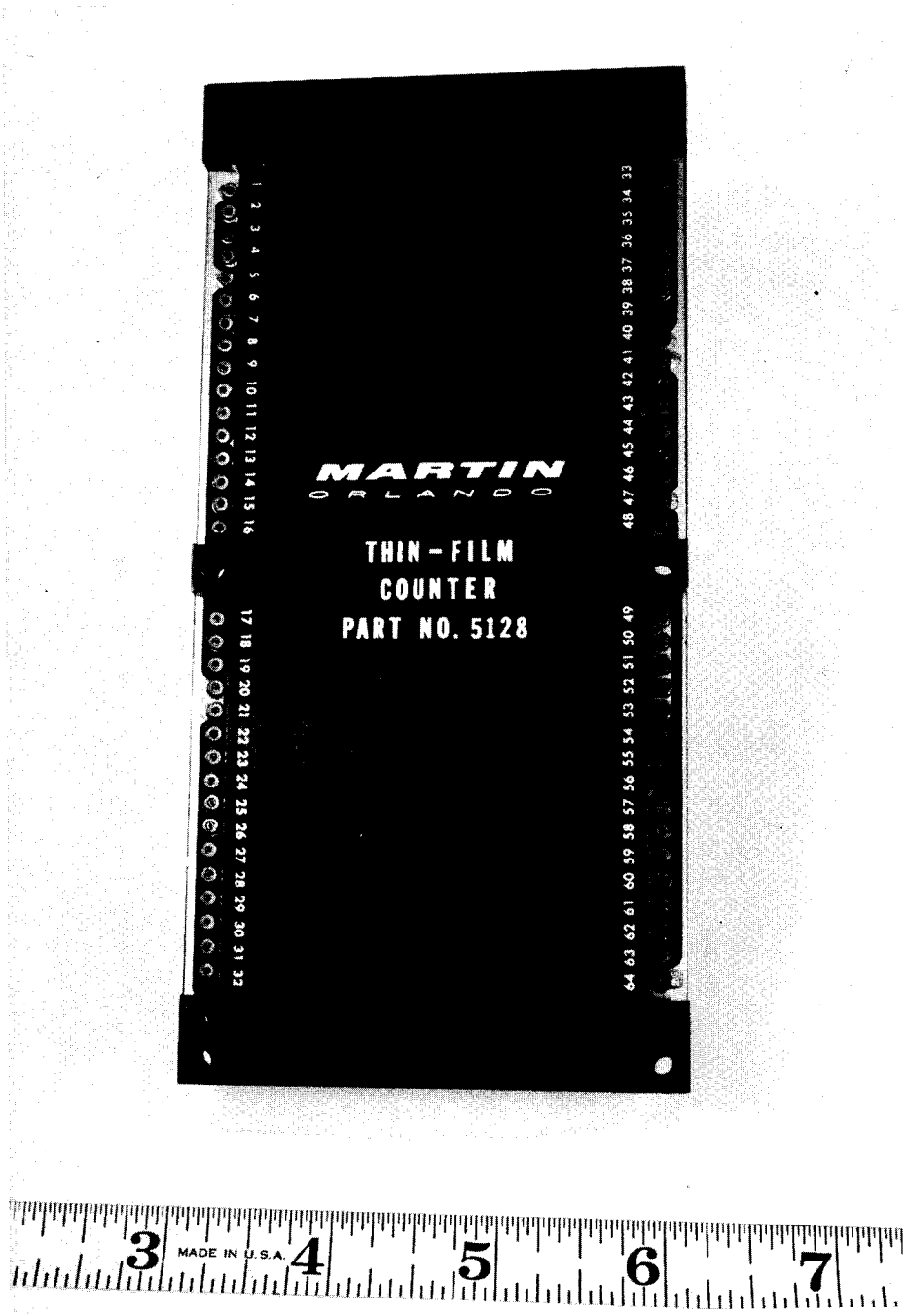


Fig. 7. View of complete package.

Master artwork for making deposition masks was planned to reduce registration problems. Circuits with resistors, capacitors and conductors normally require the following masks: resistor mask, first-conductor mask, second-conductor mask, capacitor-electrode mask, capacitor-dielectric mask, and capacitor-counter electrode mask.

Various means were adopted to reduce registration problems from deposition to deposition. Means for mechanical registration for the substrate with the holder and mask with the holder were provided. The width of resistors was established by the resistor mask and the length by one of the conductor masks. One dimension of a capacitor was determined by the mask for the electrode and the other dimension by the mask for the counter electrode. Sufficient overlap was allowed in conductor, electrode, and dielectric masks so that shifts of a few thousandths of an inch would not be critical.

The master artwork was taped at a 20 : 1 scale on 0.005-in.-thick Mylar. The overall artwork dimensions were 70 × 40 in. Focal points for checking the accuracy of photoreduction

TABLE IV

Revised Functional Block Component Study

Functional module	Deposited components		Attached components	
	Resistors	Capacitors	Transistors	Diodes
Oscillator and start amplifier	40	13	12	0
Stop amplifier	22	12	6	2
Counter input	36	2	21	4
Binary	41	4	2	4
Ring counter	53	0	31	0
Nixie driver	50	0	20	10

TABLE V

Package Data

Thin-Film Package	
Size	3 × 6 × 0.5 in.
Volume	9 in.^{3}
Packaging Density	176,000 parts/ft^3 (921 parts) 1,120,000 parts/ft^3 max. substrate packaging density
Weight	6 oz
Power	3.6 W 0.4 W/in.^{3}
Display Package	
Size	1.5 × 3.12 × 0.87 in.
Volume	4.08 in.^{3}
Total Volume	
Thin-film package + display package	13.08 in.^{3}
Proposed Package	
Thin-film section and display in one package	10.3 in.^{3}

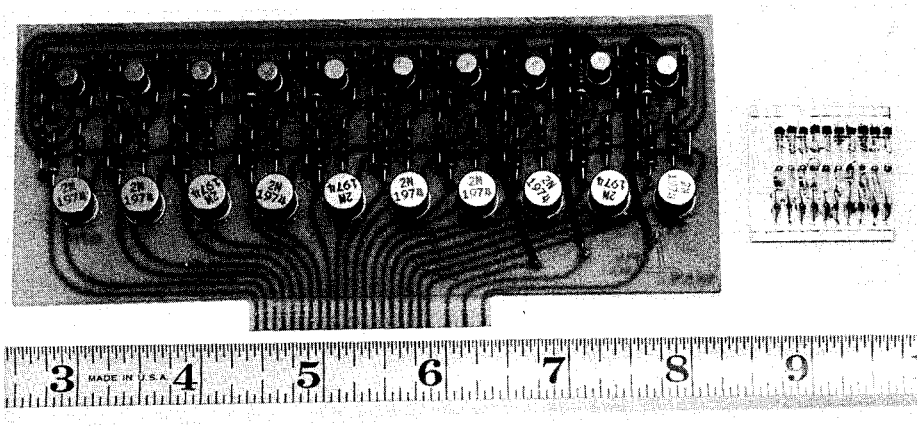


Fig. 8. Nixie drive—printed circuit and thin-film modules.

were used, and these points were later used as mask registration tooling holes. The master drawings were made using the layouts as a guide and the layouts were later used as assembly drawings with the transistors and diodes and their attaching points shown.

The transistors and diodes are attached to the substrate after completion of the deposition process. A Kulicks and Soffa thermal compression bonder was used for attachment of components. Transistor and diode leads were 0.001-in.-diameter gold wire. The substrate was heated to 220°F and the chisel to 600°F with 150 g pressure to make the bonds.

The substrate area between the connector pads was coated with Hysol 12007 to protect the deposited and attached components, to insulate the transistor and diode leads, and to provide protection from physical damage.

The interconnection board with 13 substrates mounted was sandwiched between two aluminum covers (Fig. 7). The display portion was a separate package with nixie tubes mounted in line in a block of RTV material. The tubes had an interference fit in the block of plastic and the block could be mounted either horizontally or vertically and the tubes rotated 90° to provide proper viewing orientation. Packaging data is provided in Table V.

A theoretical printed circuit model of the thin-film counter was established for comparison of size and weight reduction. The card size was determined as a result of direct conversion of some of the thin-film modules to printed circuits (Fig. 8).

The printed circuit model used the same transistors in whatever can styles were available and standard off the shelf resistors and capacitors. Plastic card guides and connectors were used to design the theoretical package. This indicates the potential of thin films in reducing size and weight in equipment with adaptable circuitry and it can be concluded that this technique is excellent in applications where such reductions are of prime importance (Table VI).

TABLE VI

Table of Comparison

Type packaging	Weight	Volume
Printed circuit	7.1 lb	266 in.^{3}
Thin film	6 oz	9 in.^{3}
	Volume reduction—96.7%	

One general area of use would be in man-carried equipment, where bulk and weight are usually the limiting factors in the employment of such equipment. The promise of substantial improvement in reliability as a result of replacing many connections of various kinds with deposited ohmic junctions also exists. The deposition of thin films can be automated and substantial cost reductions can be made, but after some point is reached in this phase of the process, the cost of active components and the cost of attaching them becomes the major item.

The flexibility of thin-film design is such that fabrication of more different types of circuits, such as digital, linear, and analog, can be achieved, and such design through engineering and fabrication will normally take a shorter time than with some other microminiature techniques. In many instances, thin-film circuits will be more economical than other types of microelectronic circuits when relatively small quantities are involved. System cost may also be reduced as a result of reduction of interconnections external to the thin-film element.

8080

A New Flat Package for Monolithic Integrated Circuits

GLEN R. MADLAND
Motorola Semiconductor Products Division, Phoenix, Arizona

Continued research into the problems of suitable packages for integrated circuits has led Motorola Semiconductor Products to develop an improved flat-package configuration. Among the important advances incorporated in this package are extreme ruggedness of external package, terminal bonding, and external leads, according to the paper's description. The somewhat detailed processing schedule for assembly of the hermetically sealed glass-and-ceramic package is discussed in the paper, along with some typical circuit interconnecting methods.

INTRODUCTION

INTEGRATED CIRCUITS offer the possibility of orders-of-magnitude size and weight reduction as compared with conventional fabrication. The small die size ($0.100 \times 0.100 \times 0.005 = 0.00005$ in.^{3}), which may contain 10–30 components, requires new ideas in packaging to utilize integrated circuits to full advantage. Since most integrated circuits are made by the transistor manufacturers, the TO-5 transistor case with the number of leads increased to eight or ten, has been used to package integrated circuits. This method uses the manufacturing experience and proven reliability of the widely used transistor package.

Continued research into the problems of suitable packages for monolithic integrated circuits has led to the development of an improved flat-package configuration. Among the important advances incorporated in this package are extreme ruggedness of both the package itself, from the standpoints of materials and assembly, and of the bonding medium utilized to connect to the integrated circuit terminals. Of equal importance is the development of a high-quality seal, which, to be acceptable for integrated circuits, must be entirely leakproof under a wide range of environmental conditions.

Another important aspect of the new package concerns the external leads, which are able to withstand considerable flexing and bending without either breaking off or rupturing the package seal. The leads are readily connected into external circuitry by conventional methods such as welding or soldering.

The development of the new package resulted from an extensive integrated circuits packaging development program at Motorola's Semiconductor Products Division. It is based on the most advanced techniques and processes, which in combination with the compatible design and processing of the integrated circuit blocks, will provide the utmost in reliability, performance, and ease of integration into electronic systems.

THE PROBLEM AND ITS SOLUTION

The TO-5 transistor package has several limitations. It is large compared with the integrated circuit die size. The form factor is poor for high packing densities. The thermal path available in the TO-5 makes cooling of high-density packaging difficult.

Because of the limitations of the TO-5 transistor package, a ceramic-glass package has been developed by Motorola with the following as a design objective:

1. The most favorable form factor possible.
2. A size that can be handled with standard production skills.
3. Leads that can be welded or soldered, using commercial printed circuit boards and spacing to avoid leakage problems, yet leads short enough for ease in testing and handling.
4. Internal area for the Motorola hybrid (multichip) circuits equivalent to the TO-5 (approximately 30,000 square mils).
5. Better thermal and system design possibilities.
6. Reliability equal to or better than the TO-5.
7. External leakage paths equivalent to the TO-5.
8. Cost comparable to the TO-5.

A flat form factor was selected as the best packaging density possible. Allowing 30,000 mils of internal mounting area, a dimension of $\frac{1}{4} \times \frac{1}{4}$ in. allowed five leads to be placed on each side with 0.050-in. spacing. The package is expandable to 18 leads, if all four sides are to be used. A study of circuits indicated that 18 leads will handle almost all circuit functions.

A body material of alumina (Al_2O_3) was chosen for the following reasons:

1. Good thermal conductivity.
2. Low electrical leakage.
3. Longer electrical leakage paths as compared with metal-glass packages.
4. Good high-temperature glass-seal characteristics.
5. Ease of internal metalization for multichip printed circuit patterns.
6. Mechanical ruggedness.
7. Low cost (comparable with TO-5).

Gold-plated Kovar or Sealment leads appeared desirable, as our customers are most familiar with handling this material and the leads have satisfactory temperature coefficient and glass-sealing characteristics.

Of extreme importance was the method of sealing. The ceramic-glass technique with Pyroceram as sealing agent was selected for the following reasons:

1. Hermetic reliability.
2. Low-temperature sealing—400 to 500°C.
3. Ease of application and assembly.
4. Seals dissimilar metals, ceramics, and glass with high reliability.
5. Seals readily in inert atmospheres.
6. Has higher mechanical strength than vitreous sealing glasses.
7. Has higher thermal conductivity than standard glasses.
8. Has excellent insulating properties.
9. Can pass all environmental tests now required for packaging.

Although the planar passivated structures have reasonably good unencapsulated life characteristics, the maximum reliability can only be obtained using a good hermetic seal. The minimum sealing temperature of a reliable glass hermetic seal is 400–500°C. While the silicon die has no problem withstanding this temperature, the small gold bonding wires used would not. The gold wires form a eutectic with the aluminum metallization and "Purple Plague" results. The purple compound is formed almost instantaneously at 450°C and open leads result. One solution to this problem is the use of aluminum wire to replace the gold wire. The all-aluminum system was found to be stable at 600°C. It was necessary to put aluminum on the Kovar leads to provide good bonding (see Fig. 1).

Another solution is the use of "finger" bonding (see Fig. 2). The fine (1 mil) wires still appeared as a possible reliability problem and a bonding clip was designed. This clip still uses the all-aluminum system, but the flexible finger is directly bonded to the silicon die. This

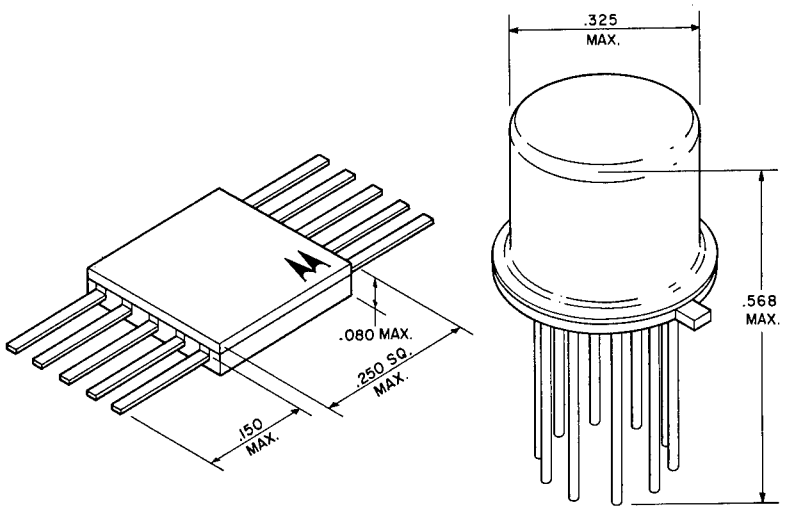


Fig. 1. Comparative physical sizes.

appears to be a very rugged method, and tests comparing the finger and wire bonding techniques are being made.

ASSEMBLY METHOD

A review of the assembly methods will be informative. First, the silicon integrated circuit die is bonded to the bottom of the flat package, using glass frit as shown in Figs. 1 and 2. Glass is applied all around the frame.

Second, the finger clip is positioned on the bottom plate with the fingers extending to the proper bonding pads. The assembly is then passed through a 450°C furnace to form the glass seal around the leads.

The next operation is to ultrasonically weld each finger contact or bond the wire connection. This is an aluminum-to-aluminum contact. After shearing the frame, an electrical test can be made to ensure a complete set of contacts.

Glass frit is then applied and the cover put in place for final seal. The unit is again passed through the 450°C furnace and the unit is sealed. Gold-plating the leads, painting, testing, and stamping complete the process (see Fig. 3).

Tests have shown the complete hermeticity of the seal using helium leak-detection methods.

An interesting method has been used to evaluate the finger contacts. A special test pattern (Fig. 4), essentially a short circuit, is used to determine contact quality. The low resistance of the test pattern (2–3 Ω) gives a better indication of contact deterioration than a circuit where 10 to 100 Ω of lead resistance may be a factor.

THERMAL CHARACTERISTICS

The thermal resistance of this package to still air is 400°C/W. The thermal resistance junction to case is approximately 8°C/W. In high-density packaging, the low thermal resistance junction to case can be used to advantage by running heat conducting strips through the package for heat conduction.

SYSTEM CONSIDERATION

The flat package will provide packaging densities of 100 circuits/in.^{3}, as against 20 circuits/in.^{3} for the TO-5.

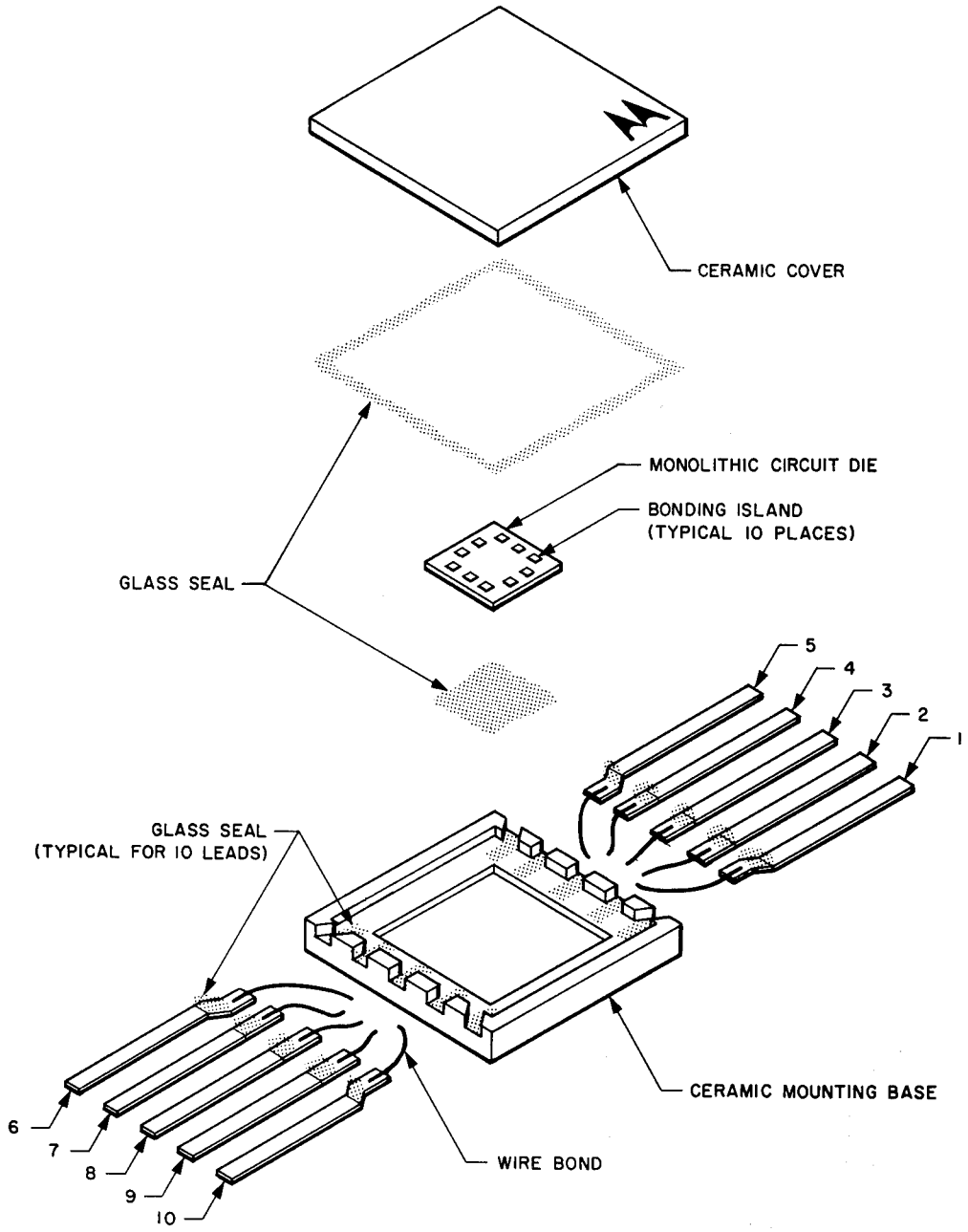


Fig. 2. Monolithic wire bond. Integrated circuit glass ceramic flat package.

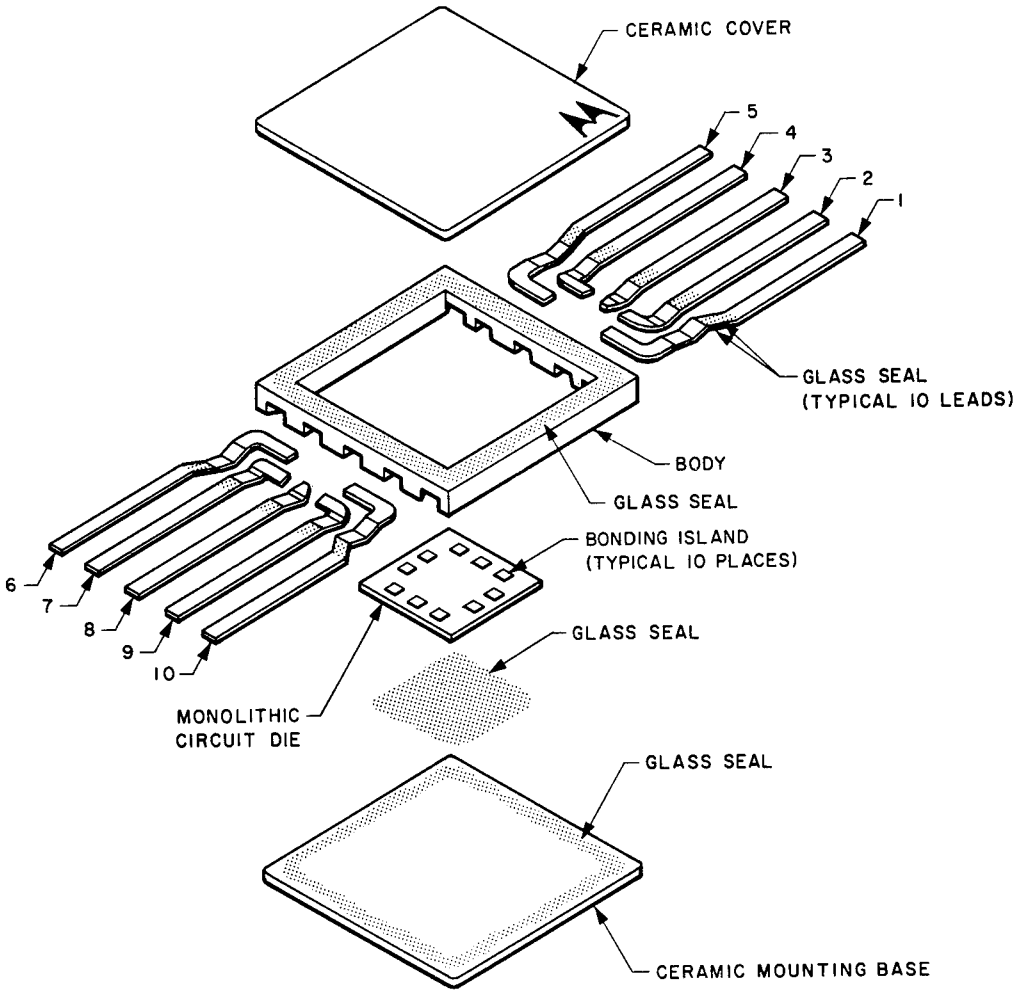


Fig. 3. Monolithic contact-bond. Integrated circuit glass ceramic flat package.

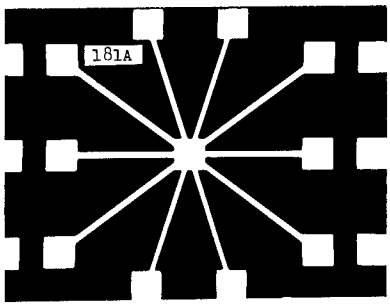


Fig. 4. Special test pattern for contact studies.

The flat package leads may be soldered or welded in place. Units may be replaced if required, at a reasonable cost level. The high order of reliability will reduce total operating costs, making replacements few and far between. Large computers are being constructed with integrated circuits with MTBF of 2.5 years.

SUMMARY

A new high-temperature package has been developed using glass-ceramic technology. This package offers high reliability and practical handling from an equipment manufacturers' point of view. The acceptance that the industry has given the flat package proves the soundness of its design.

8081

Encapsulation of Electrical Components by Transfer Molding vs. Precision-Formed Encapsulation Shells

MILTON I. ROSS
The Milton Ross Company, Southampton, Pennsylvania

This paper develops two methods of encapsulation: one using encapsulating shells and headers, the other using the transfer molding process. Without pitting transfer molding against encapsulation, the paper shows how encapsulation is done with various types of dispensing machines as well as with numerous standard shell applications marketed by three or four manufacturers. A comparison time for each technique, and general cost of the basic shell is shown, with no attempt to interpret overhead, profit, and other related factors in detail.

SHELLS AND HEADERS

FOR MANY YEARS potting and/or encapsulation of electronic components was being done under severe handicaps. Building machined molds was expensive, and hardly a suitable method for large production and the high quality needed by the industry. Other methods using less expensive mold forms did not overcome the inherent problems for the industry, which found these techniques costly for encapsulating and lacking in the sophistication of the newer miniature components. When the investment warranted, a number of companies would have special shells made for specific needs. It was not until 1956 that the first truly standard line of encapsulating shells and headers was introduced. With the number of standard encapsulation shell types and sizes increasing daily, it is relatively easy for a manufacturer of almost any product to find the particular size he needs from stock.

Some companies manufacturing standard shell sizes welcome customers who will give them orders for shells that fall within their basic standard designs and specific size ranges. The shell manufacturer will tool these at his own expense with absolutely "no charge" to the customer, if minimum orders are placed. Why is this possible today, but not practical a few short years ago? It is because industry and the military have ever-increasing demands for reliability and quality through a better packaged product. Chances are if one manufacturer has standardized a size, either through his own development or through joint manufacturers' agreement and/or military specifications, other manufacturers will follow the same trend. Standard encapsulating shell manufacturers have found new markets in noncompeting products packaged in the same shell.

If round thin-walled shells were required, they were machined from phenolic or epoxy rod. In the past it was difficult to obtain thin-walled standard molded shell sizes, but today a number of manufacturers are making dozens of round sizes from $\frac{1}{16}$ to over $2\frac{1}{2}$ in. diameter. Even thin-walled slotted precision wire-wound resistor shells are being molded.

As an inexpensive potting form, the encapsulating shell has excelled. It is superior because it helps prevent deterioration of the component being encapsulated, reducing the possibility of moisture penetration while ensuring minimum protection via the wall thickness of the shell itself. Generally, the higher temperature resistance of the shell offers additional protection, as well as added strength. The many shell colors available allows one the flexibility of coding

the components without making different-colored encapsulating resins. Once the shell is potted it is not tying up expensive production equipment; cure time, therefore, is of minor importance.

In some instances a shell could make practical the use of an excellent low-shrink resin with a low exotherm, such as room temperature, or low oven temperature for curing. The number of plastic resins being used to mold encapsulating shells is broad enough to cover the entire price range of resins and electrical products manufactured. Some might be thermosetting, special flameproof types, and even offer high heat resistance. Alkyd, phenolic, and diallyl phthalate have military approval; other types are thermoplastics such as polycarbonate or polypropylene. The ability of epoxy to adhere to the shell of alkyd, diallyl phthalate, and epoxy has been proven many times, although some companies still insist on having the internal area sandblasted. However, due to the design of basic types of electronic components, there have been a number of configurations standardized by the industry. These products are being improved in many ways, upgrading the shell resin, decreasing the wall thickness, making more room for the component, and using standard plastic molded headers with the pins firmly molded into place.

Molded-in-place pins reduce the possibility of moisture penetrating around the pins. Pins pressed into holes can cause strain and thus crack the header if they are too tight, while the pins might easily push out if too loose a fit. Molded-in-place pins are supported vertically and can be molded to center distance tolerances of ± 0.002 in. noncumulative, depending upon the size. Numerous styles of pins are available with various types of plating, depending on the base metal. Lately there has been a trend to 0.031-in.-diameter pins, but 0.040 in. diameter is still the most popular size. We have not used rigid pins under 0.020 in. diameter for standard headers as their general acceptance to industry has not been confirmed.

Molded-in-place threaded inserts for mounting components or for securing onto printed circuit board or chassis is very practical. Many companies requiring copper wire leads have specified O.F.C. (oxygen-free copper) as they require the wire to bend five 90° bends without breaking. The longer soft copper wire is, the more difficult it is to mold, because the pressure of the plastic against the wire tends to bend it. When headers are made to plug-in sockets or solder in place on the printed circuit board, they perform another important function as a support to mount the components, in order to weld or solder the leads to the header pins. This also provides an excellent way to test the assembled component prior to encapsulating. They can be easily plugged into a test socket for rapid, on-the-line testing. Many headers are in standard seven- and nine-pin spacings. In some cases, they duplicate the pin configuration of glass-to-metal seals and can be used wherever hermetic seals are not required. In small quantities they are about one half the cost of standard seals and in volume probably one third the price, depending upon the type of header. The industry leans towards 0.100-in. grid spacing, but also utilizes 0.075-in., 0.150-in., and 0.200-in. grids.

The size of standard components used in module assemblies has helped effect the maximum width, so that no wasted space is lost within the module by leaving open space. The bottom of the header can have molded feet to keep it off the printed circuit board, allowing space for solder fillets, circulation of air, room to wash out solder flux, less moisture entrapment, and dissipation heat. At times, holes for pouring the encapsulant and air vents are molded into the header. The shell can have through holes and even a chimney which can be filled to compensate for the shrinkage of the epoxy; the chimney is then ground flush to the surface. In instances where a header is not required, feet can be molded on the shell. When a size is standard, and purchased in quantities of 1000, it is practical to mold a part number or trade name within the shell. Most shells are designed with a stepped area at the open end.

The header and shell are made to mate together by means of a stepped area around the perimeter, so the header can then press fit into the shell. In most instances the fit is sufficient so that it will not pull out. If required, the fit can be made tighter so that little epoxy, if any, leaks out during encapsulation. At times, transformers or magnetic amplifiers require holes to be drilled into the side of the shell for lead wires or terminal mounting. Where numerous hole configurations are desired in the bottom, partially molded through holes are made with

0.002 in. to 0.005 in. flash over them. Then as the customer requires, these holes can be punched through. The ingenuity of the engineer is not limited—at times only the practicality of producing some of the designs creates a problem. Those companies making standard shells know many ways to achieve cost savings by improving the production, quality, and reliability of a package.

Many companies have found the cost of blending epoxy and maintaining proper quality control a considerable expense. They have searched for more practical methods, such as epoxy pellets, or dispensing machines that meter, mix, and then discharge the precise volume of epoxy required. Small components are best suited for epoxy pellets, since the pellets are the exact weight and volume of resin to properly fit and fill the shell. The compressed pellet can have a hole to accommodate the component lead as on a resistor or diode. Pellets can be made for a specific application, to melt at a given temperature, to cure at a given oven temperature, and have certain physical and electrical properties deemed necessary by the user. Dozens of components could be assembled with pellets and loaded on trays, then, in volume, placed in an oven. Heat is the only thing necessary to cause the epoxy to flow, in order to completely encapsulate the component—no pressure is required. It is not as practical a method with large products. For easily handled components, production rates are thousands per hour with just a few people; in many cases vibrating feeders can be used to automatically insert both the pellet and the component into the shell.

Most companies have found suitable epoxy resins through experimenting; however, we do suggest investigation of the newer resins such as polyurethane foams, silicones, and the endless number of fillers. Many papers have been presented telling how various filler sizes and types helped solve a particular problem. There are hundreds of resins available; not all would be suitable for each application. The field of capital equipment finds dispensing manufacturers growing each day as new ideas develop. Some products warrant the investment to automate the encapsulating procedure, and this has been done utilizing a conveyor system. One conveyor and dispenser manufacturer is able to encapsulate 30 shells per minute, dispensing a total of 10 g of epoxy, each shell measuring approximately $1\frac{1}{2}$ in. long $\times$ 1 in. wide $\times$ $\frac{11}{16}$ in. high, total weight 28 g.

There are two basic ways air bubbles find their way into the epoxy: (1) in stirring the resin with the filler and hardener (catalyst) and (2) when pouring during encapsulation. Vacuum ovens help remove the excess air in very critical products. Generally, medium to large size products require this added precaution. Ordinarily, the resin is subjected to the vacuum prior to encapsulating and/or the products during encapsulating are put in the vacuum oven for degassing and curing.

Epoxy resins are thermosetting, requiring dispensing machines that are easily cleaned, with inexpensive replacement of dispensing heads, etc., should the resin cure within the mixing chamber area. There are a number of manufacturers offering very precise metering, in grams, to large heavy-duty machines metering gallons. In some instances, small hand devices are used. One type in wide acceptance uses a caulking gun principle; that is, resin is put into a polyethylene container and placed within the gun; a trigger device puts pressure on a plunger in the cylinder, dispensing the epoxy in small doses.

Sometimes, when components are assembled, apparently in order, welds or soldered connections may still need corrections. After the unit is completely encapsulated is no time to find the error. Engineering cannot fairly blame the department doing the encapsulation for the component failure. Therefore, some companies have found it advantageous to spray a fine coat of epoxy over the entire module; this resin shrinks, setting up minimum stresses which often point out critical areas. Some companies use elastic epoxies, and test prior to complete encapsulation. To protect and improve shock resistance in more sensitive components, such as glass diodes, a coating of silastic rubber is used. This thin coating acts as a cushion when the entire module is completely and thoroughly encapsulated.

Unfortunately, this technique has its pros and cons, and we again emphasize investigation. Repairing modules or a component prior to encapsulation is the most practical, and can save and reduce rejects if done in time. In some instances, where volume and investment permit, automatic test stations are used, testing numerous electrical characteristics and stopping

whenever there is a failure. In all cases the equipment I have seen has been custom built for the application. One simple method for filling, is to place the shell on a balance scale, then fill the shell to the predetermined point of balance. The resin in this case is very thick, and the component (a module) is placed on the surface of the epoxy. The walls of the shell have ribs to ensure centering of the module during encapsulating. The small printed circuit boards, to which the component module is assembled have holes throughout to allow the epoxy to enter deep within the module. When these are put into an oven, the heat causes the epoxy to become more viscous and the weight of the module helps it settle to the bottom of the shell. Any air bubbles will tend to rise; that is why some companies include in their process, before the encapsulant is fully cured, the breaking of these bubbles.

One company was concerned with the position of the leads after encapsulation and felt the transistor should be exposed. The holes in the bottom of the shell accepted the leads from the components, and in order to reduce the flow of epoxy from and around the leads, the outside of the shell with the assembled unit is partially dipped into a peelable plastic such as butyrate, and then encapsulated. After the epoxy cures, the peelable plastic is easily removed.

TRANSFER MOLDING

The technique of encapsulation by transfer molding did not have to wait for advance designs in molding presses, but for advances in the resins that were and are being used.

Components themselves have changed very little over the years. As far as withstanding the pressures and heat required to properly encapsulate them without jeopardizing their quality and reliability. Countless types of products can be transfer encapsulated; some of them are:

1. Semiconductors—silicone and germanium transistors, and diodes.
2. Transformers.
3. Toroids—coils, magnetic amplifiers, and solenoid coils.
4. Resistors—metal film, carbon deposited, and wire wound.
5. Capacitors—mica, polyester, ceramic, and paper tantalum.
6. Potentiometer—delay lines, RF chokes, printed circuitry, thin-film *RC* networks, reed relays, motors, modules, etc.

Five basic resin types have been most successfully used to transfer encapsulate components. They are alkyd (rope, putty, and granular forms), epoxy, diallyl phthalate, phenolic, and silicone.

Each has its own distinct advantages, and many overlap one another. Careful scrutiny of the physical, electrical, and mechanical properties of each, in relation to the component, is the safest way to get the best result. Alkyd is the fastest curing of all the resins. Resin manufacturers are continually improving characteristics of their resins and we advise regular examination of all materials to determine which suits each job best.

Miniaturization being what it is, size of the component has become more critical. The contour of the molded component is dependent on the shape of the product being encapsulated. The electrical component as manufactured will often deteriorate when subjected to stresses, therefore the encapsulant offers a very substantial protection. In some cases proper selection of resins would appreciably upgrade the physical and electrical conditions under which the component might operate.

Changes take place in epoxy, and the molding grade differs somewhat from the normal casting encapsulating grade even though similar basic chemical formulas may exist. For example, in order for the epoxy to be moldable, that is, for the mold to open after proper cure, it is necessary to incorporate release agents within the resin to offset the adhesive nature of the resin. Other changes were needed to improve shelf life and permit storage in nonrefrigerated areas. These release agents (talc might be one) helps the molded components eject smoothly from the cavities and improves the flow characteristics of the resin. It also helps release flash from the mold surface. In cases where it is important to have an extra strong bond of epoxy

to the component itself, the component can be spray coated or dipped into liquid epoxy and cured prior to transfer encapsulation.

Plunger pressures require changes according to the type of resin used, and the greatest variation would be in alkyds. The putties need only 700 psi, whereas the granular resin needs 1500 to 2000 psi. Epoxies, silicones, diallyl phthalate, and phenolic are all available with a broad range of flows.

Temperature molding pressure and cure time are interrelated. In terms of the broad temperature range over which a resin will flow, the lower temperatures require the longest cure time, and permit the longest flow, at the least pressure. At higher temperatures, less cure time is needed, plasticity of the resin decreases, and greater molding pressures are required.

The material suppliers can be of the most service regarding the particular resin one might find suitable. The most important point to emphasize is the ability to control both of these factors as closely as possible. The quality of a transfer molded component is very closely related to how precisely pressure can be increased and decreased and regulation of the on–off periods of the thermostats. Our company uses heating cartridges that are 1000 W, $\frac{5}{8}$ in. diameter, 8 in. long, in order to reduce the time required to get and to keep the mold within ± 1 deg of proper molding temperature. Temperature will drop as long as a mold is kept open. If cold, or relatively colder, fixtures are put into a mold they must heat up to proper molding temperature, particularly if they might also act as runner sections. We have found that inserts tend to "chill" the plastic when the plastic will not weld properly around them, whereas if they are left in the mold a few seconds prior to closing of the mold, the welding or knitting of the resin is excellent. Shrinkage can be increased or decreased somewhat depending upon the temperature, but most important, just because the product may be cured on the surface does not mean it is properly cured internally. Improperly cured components can break down under stress and considerably reduce component reliability. Shrinkage for each resin will vary according to the filler. After-shrink characteristics of the resin being used must be checked carefully, subjected to various conditions since stresses can be set up within the part due to molding. At times the position of the gate, the type of gate, and even the number of gates can have a critical effect on the shrinkage. Runner size plays no small role in the quality of product produced. There are about as many runner designs as there are geometric designs: rectangular, half round, full round, round "V" and others. How does one know which one to use? One might ask three people: the press manufacturer, the material supplier, and the mold builder. If one design can solve all attendant problems, change is inadvisable. If, after experience, it is felt that there can be improvement, the feasibility of other designs should be studied. We prefer full round; they are the easiest to maintain. Generally, we make them as insert sections to the mold, particularly because of ease of replacement in case of wear. A radius dressed wheel on a surface grinder can be a simple way of increasing the size if the steel is hardened, or even a ball nose carbide cutter can be used. We suggest balanced runner design whenever practical. In thinking of runners and gates, one should consider the advantages of three-plate molding and of gating through the third plate with a vertical runner directly into the part. Gates can be as small as 0.010 in. diameter and are automatically degated as the parts are ejected. We have used chromewear steel inserts to increase the life of the gate area. This costs more, but it can save the expense of early replacement of worn cavities, and ensure a cleaner-looking molded part over a longer period of time. The esthetic beauty of a molded part for a customer helps establish in his mind the quality of the encapsulated component. The finish in the gate area is just as critical as the precision finishing of the cavity. The smooth flow of plastic entering the cavities should be uniform and/or balanced, depending upon the design of the components being encapsulated. For example, flat rectangular-shaped miniature capacitors should be gated so the flow above and below the ceramic wafer is uniform. If the gate is only on one side, it is probable the pressure of the plastic entering will force the component against the far side of the mold and therefore will result in poor, less protected, unbalanced embedding, creating a more vulnerable condition.

Fan-type gating has received wide acceptance, and in some cases it will almost equal the full length of the component being encapsulated. The advantages are uniform filling of the cavity, less filling time required, better knitting of the resin with less chance of internal voids,

paper thin gate areas to clean, and, depending upon the length and thickness, less pressure is required to fill the cavity.

The technique of through-gating is being done successfully by many, although we do not prefer it. The gate wear is too great. Through-gating may sometimes cure faster because of friction heat and the transfer of heat from the mold, as well as through the transfer of heat through the thin gates and flat runner areas. The design requires the resin to be transferred from the plunger, entering the cavities by means of long fan-type runners, then through each cavity, through the runners, again through the cavity, passing around each component, until it might pass through 15 cavities. The resin will still be soft and flowing until the last component is embedded. This process is used to encapsulate diodes where 60 can be put into a relatively small area. The flash around the component can be hand-cleaned or rolled between two soft rubber rollers, which offers some advantage on axial lead units; since less pressure is used to encapsulate, flash on the lead wires is easier to remove without scraping the wire.

Depending upon the number and type of component being encapsulated, specific needs determine the technique of loading the mold for encapsulating. If they are heavy transformers, sliding bottom mold sections or rotating platens designed as part of the molding press can be utilized. One section is left molding with a common permanently mounted top cavity section while the second section is being loaded with the components. At the completion of the cycle, the mold opens and the first section slides away; the second section, now loaded and at the opposite end of section one, locks in molding position while the first section is being unloaded—the second section is being encapsulated. Another method is to have loading frames which can be outside while the press is on cycle. Possibly these frames could become an integrated part of an earlier manufacturing process so that the loaded frames are brought into the production area without the necessity of rehandling the components.

Although the pressures used are low in relation to other types of plastic molding they are sufficient to require full support of the component by means of its lead wires. Care must be taken in the building of the mold to see that loading fixtures line up properly with the mold and that the grooves of the mold do not crimp or score the lead wires. There must also be a few ten-thousandths squeeze of the wire by the mold to prevent the encapsulant forming an insulation around the entire wire. The *V*-shaped groove helps in the rapid loading of the components and automatically centers the components and their axial leads. If the lead wires are continually flashed, this area will wear excessively, requiring replacement sooner, and resulting in loss of pressure as well as insufficient resin to properly encapsulate, leaving voids and poorly molded parts. Air vents are necessary but they must be controlled and put in the areas where they are needed.

Building of molds for encapsulating is not nearly the task of building regular transfer molds. This does not mean precision, hardened cavities, knock pins, etc. are not necessary, because they are—only the general shape is more simple. Our experience has not been very satisfactory using hobbed cavities with alkyd, epoxy, or diallyl phthalate because the abrasion of the cavities by the resin is too great. The steels we have been using, such as chromewear, BR 4, and others, are very difficult to machine, and the best solution we found is electrical discharge machining. Corners can be very sharp with radii of only 0.005 in.; laminated molds are generally not necessary and we appreciably improve the lasting quality of our molds. These steels as a rule, do not require chrome plating. They do cost more to make initially, but have been proven to cost less overall.

Building the mold to the low side of the tolerance is done for many reasons: predicting the shrinkage is not always accurate, the mold will wear larger, and if by chance an edge is damaged there could still be enough tolerance to correct it. We do not generally recommend family molds, although their use grows each day. With hindsight we always say we'll never build another one. Care should be taken in the design of the nonaxial lead mold, which is not necessarily easier or harder to build than axial ones. By planning ahead, investigating all possibilities, the task of molding will be easier.

Generally speaking, a press manufacturer will give his customer any type of molding press he requests because it is the customer's responsibility to produce the product. Most press manufacturers will of course make suggestions, even design the mold, and give the

customer excellent field service. A number of manufacturers should be consulted to get their recommendations. One well suggests top transfer, another bottom transfer, and even a third, horizontal equipment. At times a design created six months ago can be considered out of date today.

We prefer bottom transfer presses for insert loading and molding for the following reasons: the press is controlled by one automatic operation; resin is poured into the plunger pot hole and is slowly preheated, the cycle button is pressed to close, and after the press closes the plunger is automatically activated as part of the cycle, whereas with top transfer, the press must first be closed, while the plastic resin is loaded through the pot opening in the top of the mold; the resin can then preheat until the operator presses the button to cycle the plunger. It then takes an approximate total of twice as long for the plunger to reach pressing stage to transfer the resin into the runners and cavities. We feel a lot of time and control is lost. Another factor is the exposure of the plunger to air. This tends to keep the temperature of the plunger well below that of the rest of the mold, in as much as generally no heating cartridges are in the plunger itself.

Much of the quality inherent to good molding rests with the ideal transfer of heat from the plunger to the resin being transferred. Even the cure time of the cull is dependent on plunger heat. Bottom transfer plungers are surrounded by heat and if more heat is necessary a $\frac{3}{8}$-in.-diameter cartridge heater can be placed within the plunger itself. We also tend toward plunger diameters $1\frac{1}{4}$ in. and up because more preheating surface is available. One must keep in mind that as the plunger diameter increases, the transfer pressure available is reduced. In order to prevent loss of plastic behind the plunger, two or three grooved rings can be ground around the diameter of the plunger. We suggest mixing 5 to 10% molybdenum disulfide with the resin as it will help break in the mold and lubricate the plunger and transfer pot. Only one or two shots are necessary since it will last indefinitely. What features should be incorporated into a molding press is not quite like deciding what extras one might or might not want on a new car. Although they may appear to be costly extras, the uninitiated will find if he eliminates them, even higher costs in lost production time, high reject rate, low quality, and poor reliability. Not listed in order of importance, they are:

1. Precise temperature controls, with ± 1 deg.
2. Hydraulic operated plunger; not air (too variable).
3. Precise valves to make minor pressure adjustments.
4. Dual safety push-button close.
5. Platen safety gates.
6. Wide platen area between tie rod.
7. Bronze or hardened-steel bushings.
8. Platen area working height.
9. Platen thickness sufficient to prevent giving under load.
10. Working daylight sufficient for all mold designs and future products.

Other features in the press, such as low pressure close, and more automatic and predictable operation, will show in the quality of the encapsulated component and be more consistent from operator to operator. This may not make much sense to the uninitiated, but we have found that daily and seasonal changes affect the consistency of the product produced—due to changes in the weather and from season to season. Seemingly unimportant details, such as shutting down for lunch or starting a cold press in the morning, can cause rejects for a number of shots or even hours. The more trouble-free a job can be made, the better for all concerned.

CONCLUSION

Based on his own product evaluation, the user must decide which technique will best suit his needs. He must know his present costs, and the projected new costs. This can be determined by amortizing future production requirements against the total capital expenditure and daily production realized. Evaluation of his products, utilizing each method, can generally

be done by working with the potential shell, plastic resin, and equipment suppliers, then purchasing sample materials at a reasonable cost. Honest understanding of his own company's shortcomings and its ability to tackle new jobs as well as solve new production problems—because no technique is foolproof—is vitally important.

8082

Design for Space Applications

E. B. SMITH
Electronic Systems and Products Division, Martin Company, Baltimore, Maryland

This paper illustrates certain high-density airborne packaging techniques currently being developed by the Electronic Systems and Products Division of the Martin Company. The advent of military programs dealing with space flights and missile weapon systems has dictated that electronic equipment be designed to meet more stringent specifications and environments. Airborne electronic equipment has to satisfy the requirements of proper operation, reliability, and packaging density, while not overlooking the additional factor of designing toward manufacturing techniques for volume production. Major design areas discussed include an avionics module concept using standard microcomponents and multilayer printed circuit boards for high-density interconnections. Emphasis in this paper is placed on design techniques, manufacturing processes, and environmental testing and evaluation of test data.

AVIONICS MODULE DESIGN

ONE OF THE first considerations in any electronic design used in aerospace applications is the method of assembling the electronic components in modular form. The avionics component module design represents a method where component densities and the associated problems of intramodule connections and heat transfer are considered of prime importance. Such factors as reliable operation and producibility at reasonable costs are also considered important.

The avionics module design uses conventional three-dimensional microcomponents mounted on ceramic substrates. Interconnections at the module level are achieved by an electroplated copper process. The design approach consists of a series of alumina (Al_2O_3) substrates fabricated in a family of sizes. The sizes range from 0.7 to 1.4 in. in length in 0.1-in. increments, and the width is a constant 0.5 in. The thickness of the substrate is 60 mils.

In the fabrication of the component module, several important steps are required. Figure 1 illustrates the fabrication steps from the initial substrate to final encapsulation. The basic component substrate is first cleaned or degreased in an acetone solution for approximately 60 sec, and then it is immersed in a solution of hydrochloric acid for 15 sec. Next, the substrate is placed for 20 min in an electroless copper solution at room temperature to obtain a copper deposition over the entire substrate surface. The thickness of the copper plating is 50 to 70 millionths of an inch. It is important that the substrate be clean, to allow for good adhesion between the alumina and the electroless copper. The electroless copper provides a conductive surface for the subsequent process of electroplating an additional 2 mils of copper to form a heavier base. The substrate edges are broken slightly to eliminate sharp corners so the plating can build up evenly over the entire substrate. At this point, the required conductor pattern is silk-screened with screen ink resist on both the front and rear surfaces, as well as the top and bottom edges. After the resist is screened, the substrate is etched in a modified chromic sulfuric acid solution leaving the required interconnection pattern. (The copper conductors on the substrate edge are shown in Fig. 1.) The resist is then removed with an acetone or carbon tetrachloride solution. The silk screen equipment and typical screens used in the laboratory for making the conductors are illustrated in Figs. 2 and 3. The left screen in Fig. 3 is used for

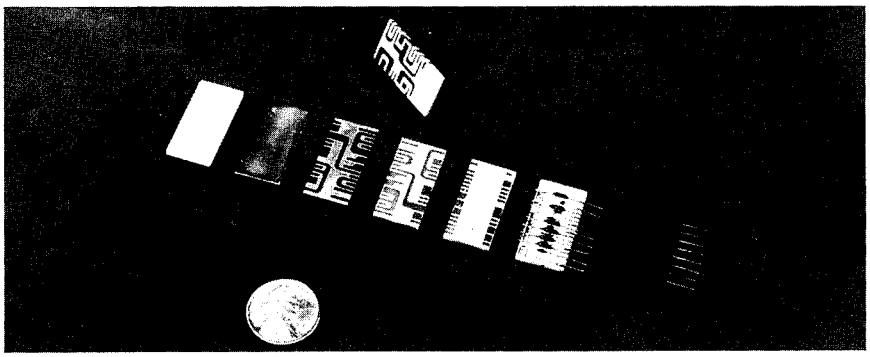


Fig. 1. Avionics module design.

the conductors on the avionics module substrate; the other is used in the fabrication of multilayer boards which will be discussed later.

The next step in the process is to prepare the module for flame spraying alumina on the substrate to build up an insulating surface above the copper conductors to prevent shorting when mounting the components into position. The substrate first receives a light sandblasting of silicon carbide to create a roughened surface for better adhesion or bonding properties for the subsequent ceramic flame spraying operation. (Isopropyl alcohol is used to clean the substrate after the silicon carbide is used and prior to flame spraying.) The ceramic spraying provides extremely good electrical insulation characteristics while also maintaining a good heat transfer path with thermal conductivity equivalent to the basic substrate. The thickness of the sprayed aluminum oxide coating is 5 mils, and it covers the entire length of the substrate with only the copper pads along the edge exposed for joining the component leads by dip-soldering. Figure 4 illustrates the laboratory flame-spraying apparatus. The distance from

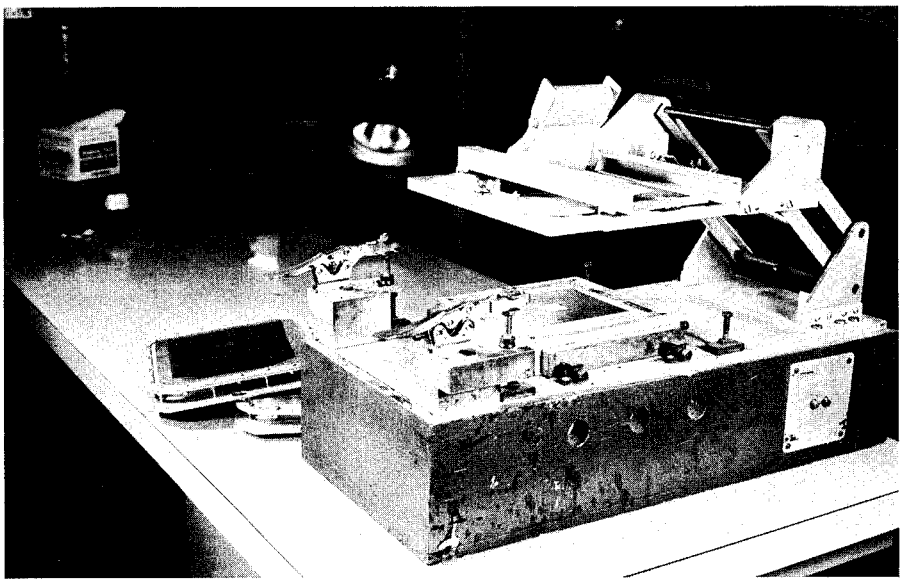


Fig. 2. Silk-screen equipment.

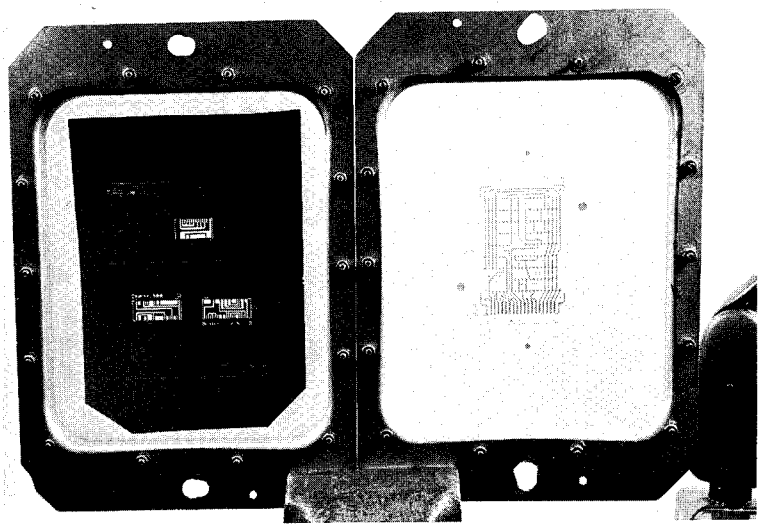


Fig. 3. Silk-screen masks.

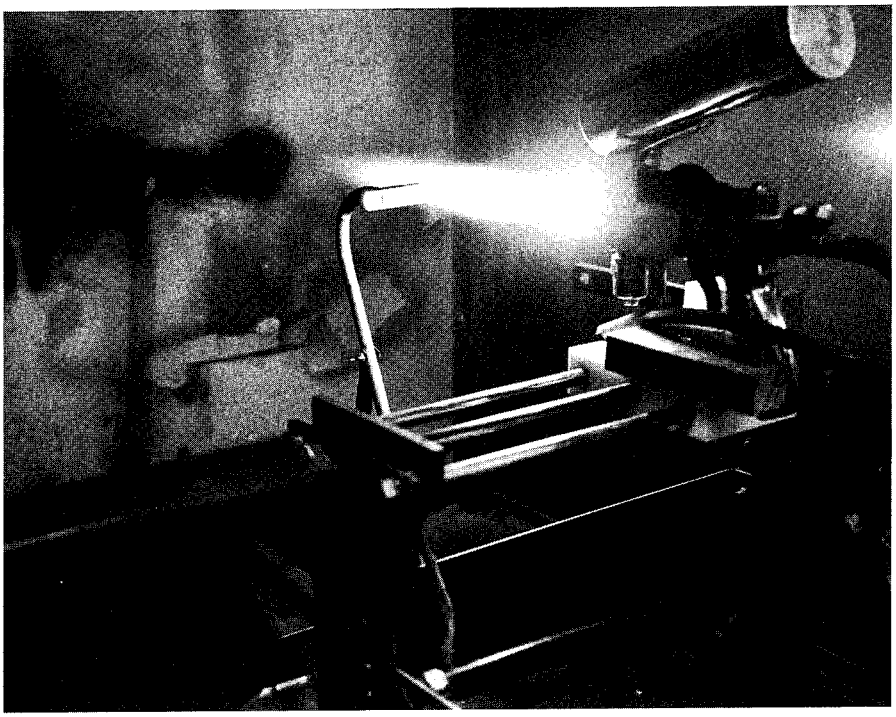


Fig. 4. Flame-spraying equipment.

the gun nozzle to the substrate surface located behind an aluminum mask is approximately 7 in. The gun and material storage cannister automatically pass across the work at a constant rate to give an even distribution of particles (thus eliminating the problem of excessive build-up or void areas). The temperature at the flame outlet of the oxyacetylene system is approximately 4000°F—well above the melting point of the alumina; however, the surface temperature of the substrate where the sprayed particles will fuse is no more than 160°F.

To properly assemble microcomponents with minimum trouble, a holding fixture (Fig. 5) is used. This fixture permits assembly of components above the substrate with the leads going between the teeth at $\frac{1}{10}$ in. centers. All the components are mounted on a $\frac{1}{10}$-in. grid (which may sacrifice the density to some extent), but manufacturing ease is realized with this system. In this design, no tooling is required for bending the component leads, for all components

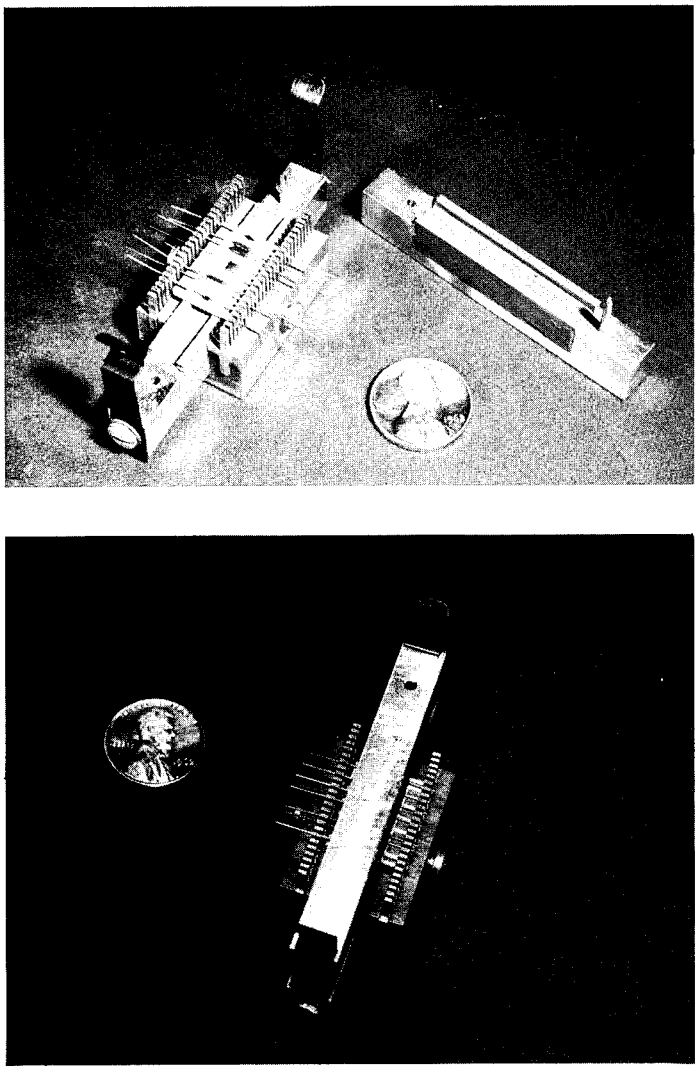


Fig. 5. Component assembly tool.

are handled just as received from the vendor. After the components are placed into position, the upper portion of the tool is assembled, and the components and substrate are sandwiched between silicone rubber inserts so the assembly can be handled freely for dip-soldering the components. The same basic procedure is followed for mounting components on both sides of the substrate. In this case, components for the underside of the substrate are first mounted on the silicone rubber pad between the locating teeth before mounting the substrate and remaining components for the upper side. As mentioned previously, components may be mounted on both sides of the substrate, but for ease of assembly of the modules to a motherboard it is necessary to have the component leads come from only one side of the substrate. All module leads are also on a $\frac{1}{10}$-in. grid.

For this design approach, component densities at the module level range from 40,000 to 50,000 components/ft^3. This is a density level that will certainly meet the requirements of most current applications. Moreover, it should be reiterated that overall density factors were sacrificed somewhat to obtain design flexibility for volume production and assembly of component modules. In all areas discussed, it is possible to fabricate large quantities of a given module at one time. In the application of the silk-screen resist material or flame spraying of aluminum oxide, for example, it is possible to perform these tasks in large-quantity lots with only small additional expenditures. Also, if the quantities warrant high-production techniques, it is possible to use flow soldering tanks and set up assembly stations and conveyor belt systems using nothing more than a larger number of the holding tools.

MULTILAYER INTERCONNECTION DESIGNS

To develop an operational system, it is necessary to consider the major problem of intermodule connections. One way to obtain reliable connections and not sacrifice system density is to use multilayer interconnections. Although there are several multilayer techniques available, this paper discusses two approaches currently being designed by Martin to help in solving the problem of high density and reliable interconnections. The two methods are the plated-through-hole technique and the clearance-hole approach.

In the plated-through-hole multilayer board (Fig. 6), the assembly consists of a series of five 8-mil glass epoxy circuit boards clad with 2-oz copper foil. The individual laminates are bonded together under heat and pressure to form a final assembly.

Each of the epoxy laminates is etched to form the required conductors and land patterns. An epoxy adhesive in sheet form (3 mil thickness) is placed between each of the circuit layers

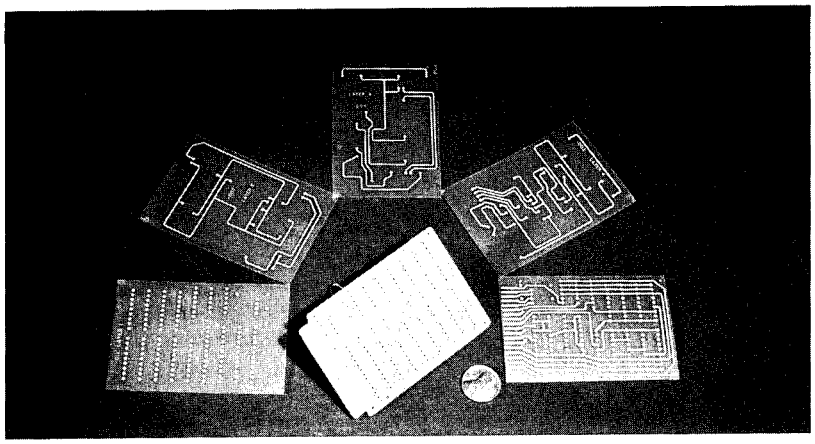


Fig. 6. Five-layer circuit board plated-through-hole techniques.

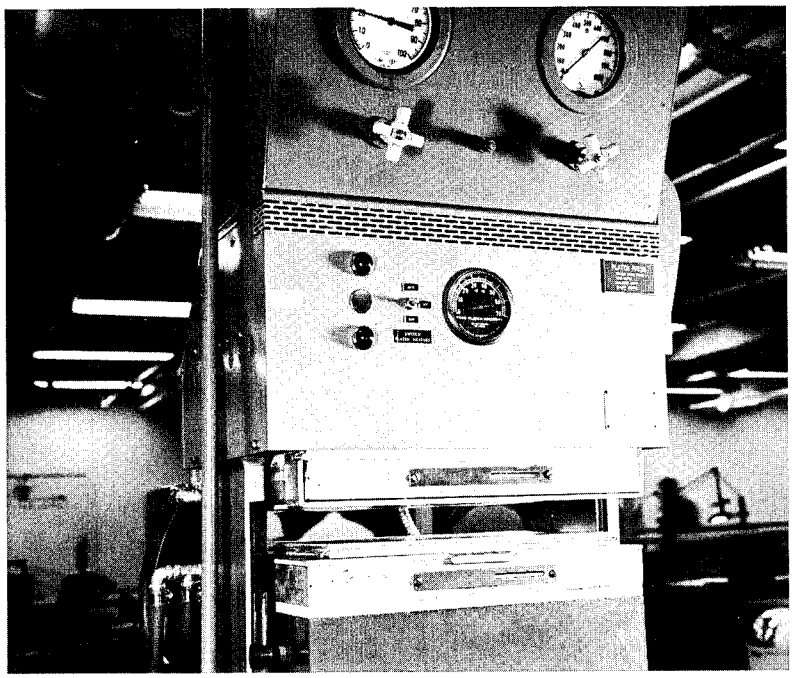


Fig. 7. Hydraulic press.

to be bonded, and the entire assembly is placed in a holding fixture to obtain proper registration. The holding fixture is then placed between the preheated platens of the press (Fig. 7). The holding fixture, 16 by 12 in., is capable of producing eight multilayer boards for each machine cycle. (Each board is 3 by 5 in. and is similar to that shown in Fig. 6.) The temperature of the platens is maintained at 350°F, and the pressure is raised to 500 psi and kept at these conditions for 30 min. After this time period, the platens are cooled to 150°F before removing the fixture and multilayer assemblies. This procedure allows the adhesive to set and gives the required bonding characteristics. The holding fixture and the epoxy laminates are illustrated in Fig. 8.

After the assembly is removed, locating holes are drilled for each of the eight individual multilayer boards to allow for placement of the drill template for the required plated-through interconnecting holes. In any design of this type it is important that the process be developed and closely followed to achieve proper registration and adhesion between layers with no air entrapment and adhesive void areas. After drilling, electroplating the copper, and gold plating

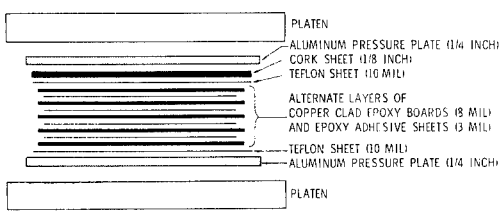


Fig. 8. Holding fixture for multilayer laminate.

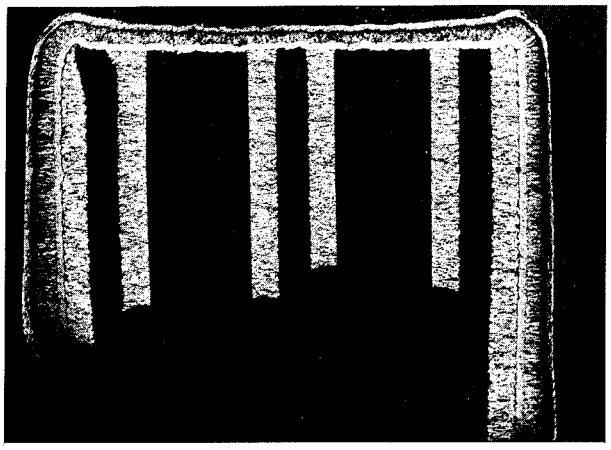


Fig. 9. Cross section of a plated-through hole (magnification 50 ×).

the holes, the boards are checked for continuity between the various levels. A typical section showing a plated-through hole making contact with the various land patterns is illustrated in Fig. 9. The figure represents six levels of interconnecting patterns used in preliminary tests where adhesive bonding and electroplated copper processes were to be studied. This figure illustrates only the continuity pattern, for the thickness of the adhesive and the circuit laminates in this photograph are not the same as previously discussed.

It is suspected that a breakdown might occur in this area because of the small amount of contact between the plated-through hole and the cross section of a typical land pattern. Preliminary tests to date in accordance with MIL-STD-202B indicate that the plated-through copper adheres to the cross section of the land and will not fail under humidity, temperature cycling, thermal shock, and vibration. (Test data are discussed in the next section.) Figure 10 shows an assembly (5-Mc, 4-stage digital counter) consisting of a series of avionic component

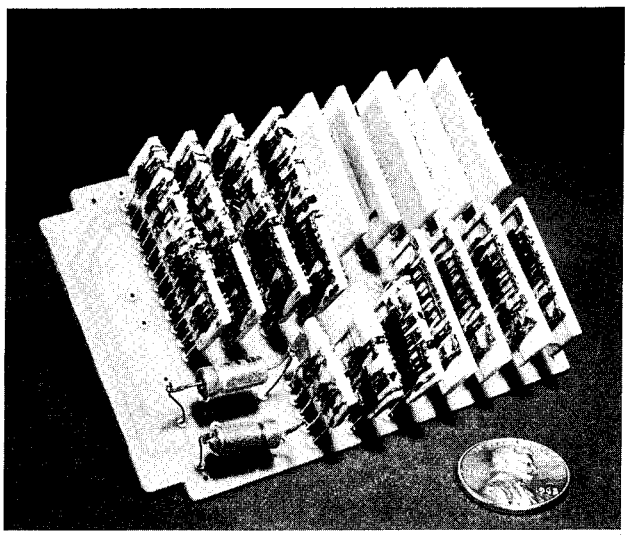


Fig. 10. Five-megacycle, four-stage digital counter assembly.

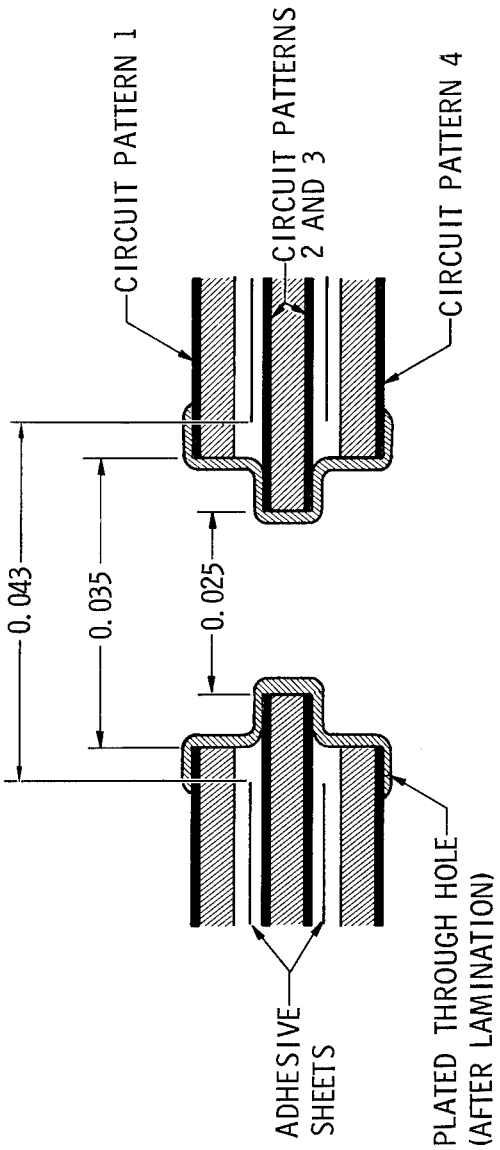


Fig. 11. Clearance-hole design cross section.

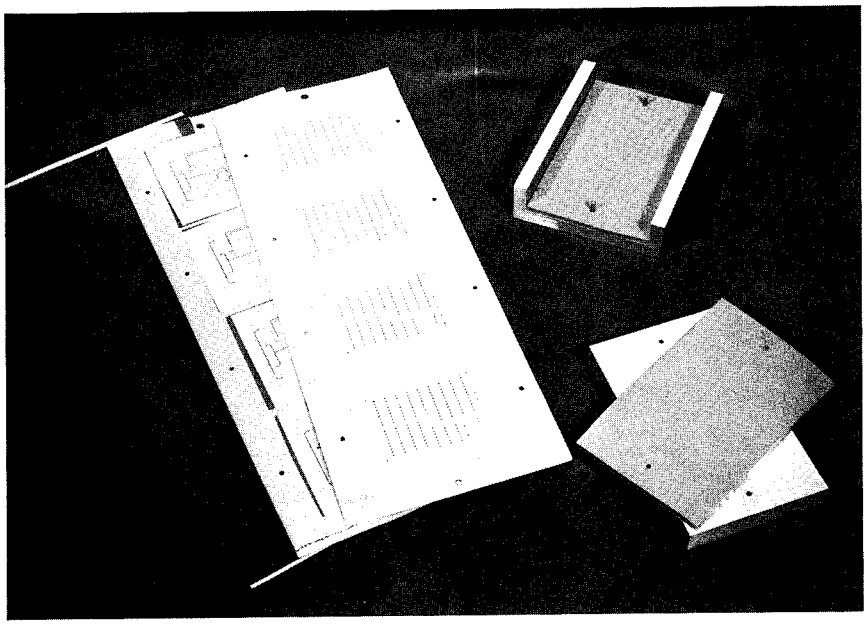


Fig. 12. Four-layer circuit board—clearance-hole technique.

modules interconnected by means of a five-layer board. This assembly was made for functional tests to determine wave shape characteristics and operational speeds for a specific line of digital circuits. The plated-through-hole design gives flexibility in being able to consider 10 to 15 separate levels of conductors fabricated into one assembly. In the initial design stages of the plated-through-hole approach, there was a certain amount of concern over the bonding of the plated copper to the copper foil. It was felt that the contact area might have been insufficient where the plating butted against the cross section of the land to achieve continuity between any two levels. For this reason, another approach was considered as a parallel effort in conjunction with the plated-through-hole design.

This second technique is called the clearance-hole method. The design still uses electroplated copper to permit continuity from one level to another, but the number of levels is limited to four. Experience in laying out circuit patterns indicates that a high quantity of circuit levels is seldom required, and four levels will answer the majority of the design problems. In the clearance-hole method, the holes are predrilled in the laminates and then aligned in proper registration for bonding into one assembly (Fig. 11). An epoxy adhesive, similar to the one used in the plated-through-hole process, is used for bonding the three laminates into a four-level circuit board. Because the boards are predrilled to the diameters specified in Fig. 11, it is necessary to obtain strict registration and also to prevent the flow of adhesive from entering the holes. If the glue enters the hole it will impair a good surface for the subsequent copper plating. This design allows a greater surface area upon which to plate to achieve electrical continuity from one level to any or all three of the other levels. It is also important that the sheet adhesive be drilled to the correct size to permit uniform bonding with good control of the adhesive flow. The diameter of the holes in the adhesive is 43 mils, exceeding the major diameter shown in Fig. 11 by 8 mils. Figure 12 shows the three laminates which comprise the four circuit levels using the clearance-hole design. To contain the adhesive flow, the laminates are sandwiched between layers of silicone rubber (which deform under pressure), causing the rubber material to fill the hole pattern and restrict the flow of glue into the hole.

The difference in the contact area for each of the multilayer techniques is significant. This is where continuity is made and where the copper foil of the etched circuit pattern makes contact with the electroplated copper. The major advantage of this approach over the plated-through-hole method is that the contact area for any two levels is approximately four times greater in the clearance-hole design.

This design was developed as an alternative for insurance purposes. Tests to date indicate that the plated-through-hole design does pass environmental tests, so reduced emphasis will be placed on the clearance-hole design. Unless additional testing gives a counterindication, it is anticipated that only the plated-through-hole approach will be studied further. The clearance-hole approach satisfied the requirement for a larger surface area for plating, but the costs associated with the manufacturing of the predrilled assemblies are considerably higher than the plated-through-hole concept.

ENVIRONMENTAL TESTS

The avionics module and the plated-through-hole multilayer boards were tested in accordance with MIL-STD-202B, "Test Methods for Electronic and Electrical Component Parts." These tests were conducted to determine the effectiveness of the design and the manufacturing processes for use in military programs where ambient conditions are similar to the test parameters outlined in the following paragraphs.

Avionics Module

Four high-speed digital circuits which included flip-flops, AND gates, emitter followers, and power inverters were designed, and samples (six of each) were fabricated for environmental tests. These units (unencapsulated) were checked at ambient temperature, and then were operated through the temperature range of 85 to −55°C (Method 102A) to determine the effect on circuit characteristics and mechanical design. Two temperature cycles were run and all the circuit modules performed satisfactorily. The next step was to encapsulate the six flip-flop modules and run an additional five cycles. As the modules were subjected to the extreme temperatures, the encapsulation (Stycast 2850 FT) developed fine hairline cracks, and the circuits ultimately failed. During the first cycle, the series of modules generally became marginal in the high temperature ambient; however, when the temperature was returned to 25°C, the circuits again operated properly. During the second cycle, the circuits began to fail throughout the entire temperature range. The tests were stopped at that point to determine possible causes and a solution to the problem.

X-ray photographs were taken to determine if the ceramic substrates also cracked or if component leads were damaged, causing open or short circuits. The photographs gave no indication of defects, but the photographs could not account for all component lead interconnections. Preliminary temperature tests on dummy modules without the ceramic substrate did not cause cracking or breaks in the plastic encapsulant. The six encapsulated flip-flop modules were then visually inspected as segments of the encapsulant were removed to determine possible causes for failure. This procedure did not prove the actual cause of the module failures because of the damage that may have occurred in removing the encapsulant, rather than the damage brought on by temperature extremes. The processes for mixing the epoxy resin should be re-evaluated to ensure that the proper characteristics are obtained. Stycast 2850 FT was selected originally for its thermal characteristics, and it is felt that this material best satisfies the requirements. The results of these tests indicate the failures may have occurred because of the stresses placed upon the components and the component leads from expansion and contraction characteristics of the cured epoxy resin and the ceramic substrates. For this reason, it is felt that a protective semirigid conformal coating may be considered for the components prior to encapsulation. In addition, the use of another encapsulant with different hardening characteristics may be evaluated to alleviate this problem.

Multilayer Interconnections—Plated-Through-Hole Design

Tests performed on the multilayer boards included temperature cycling between 125 and −65°C (Method 102A), thermal shock between 172 and −65°C (Method 107A), vibration of

TABLE I

Step	Temperature, °C	Time, min
1	−65	30
2	25	15
3	125	30
4	25	15

10 to 2000 cps with an amplitude of 0.030 in. to 70 cps and an acceleration of 15.0 g beyond 70 cps (Method 204A), and humidity for a continuous 10-day period at 80 to 98% R.H. with the temperature varying between 25 and 65°C (Method 106A). The tests were run in the order mentioned.

Temperature Cycling Tests. Temperature cycling tests were run on a dozen sample units with circuit continuity being measured. On each multilayer assembly, three individual circuits were selected and wired to electrically monitor continuity with a differential voltmeter. The 12 boards were all wired in the same manner. Testing of the circuits was accomplished by applying a constant current of 1 mA to the circuit board. A change of 1 mV on the differential voltmeter was equivalent to a resistance change of 1 Ω on the circuit being measured. The circuit resistance was monitored closely throughout the tests as the temperature cycled between the extremes of 125 and −65°C. Five cycles of 90 min each were run; resistance readings for each of the three circuits were taken during the cycle at temperatures of 125, 20, and −65°C. Each cycle consisted of the steps shown in Table I.

The circuit resistance may vary for two reasons when a particular multilayer pattern is subjected to temperature extremes: it may vary because of a gradual degradation of the multilayer pattern while being subjected to high and low temperatures, and/or because the resistance of a particular copper conductor pattern will vary with a change in ambient temperature.

For this reason, it is necessary to determine the expected resistance change of the copper conductor under evaluation to establish what additional increase in resistance, if any, may be attributed to conductor breakdown as a result of temperature cycling.

Resistance variation due to temperature change is calculated by the following expression.

$$R_2 = R_1[1 + \alpha(t_2 - t_1)]$$

where R_2 is the resistance (ohms) of a copper conductor at a temperature t_2 (°C); R_1 is the resistance (ohms) of a copper conductor at an ambient temperature t_1 (°C); and α is the temperature coefficient of resistance of copper at ambient t_1 (°C)—0.00393 at 20°C.

Table II indicates the resistance variation to be expected for one of the multilayer test boards and the three conductor patterns subjected to temperature extremes.

Tests on the multilayer circuit patterns for the 12 sample boards revealed no open circuits. The test data for one of the boards, outlined in Fig. 13, indicates the resistance measurements throughout the five cycles.

TABLE II

Conductor pattern resistance values, Ω	R_2 [125°C(t_2)]	R_1 [20°C(t_1)*]	R_2 [−65°C(t_2)]
1	0.57	0.4	0.27
2	0.85	0.6	0.40
3	1.13	0.8	0.53

* Initial resistance measured at 20°C.

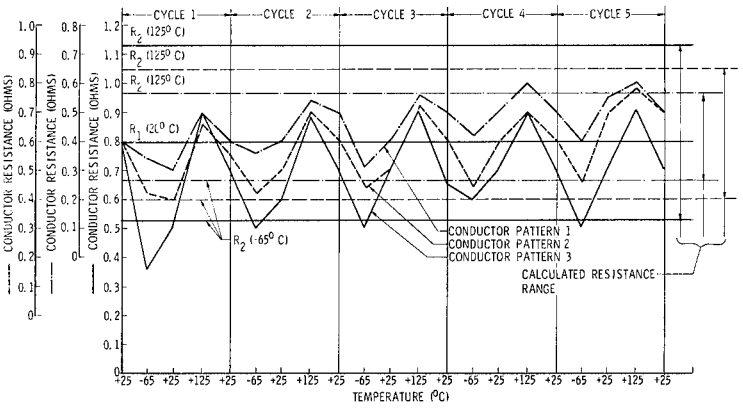


Fig. 13. Resistance measurement–temperature cycling tests.

It should be noted that the resistance of the conductor patterns did not stabilize at the end of the tests at the same point as measured before the tests began. The resistance level for the boards was usually higher by a small amount, as indicated by conductor patterns 1 and 2 of Fig. 13. The small increase in resistance noted in all sample boards is most likely caused by oxidation of the copper conductor and gold plating. The final reading for conductor 3 was an exception; that is probably caused by a variation in the measuring equipment. The initial reading at 20°C for conductor 3 was 0.8 Ω, and at the end of the fifth cycle the resistance measured only 0.7 Ω.

Thermal Shock Tests. Upon completion of temperature cycling, the same 12 boards were subjected to thermal shock between the extremes of 172 and −65°C. The 172°C value was used instead of 200°C, as called out in the specification, because of the melting point of solder. Five cycles of 70 min each were run in accordance with the schedule in Table III.

The procedure for monitoring and measuring resistance values with the differential voltmeter was the same for this test as the temperature cycling. Resistance variations caused by temperature changes again were calculated using an initial resistance measured at 20°C.

TABLE III

Step	Temperature, °C	Time, min
1	−65	30
2	25	5
3	172	30
4	25	5

TABLE IV

Conductor pattern resistance values, Ω	R_2 [172°C(t_2)]	R_1 [20°C(t_1)*]	R_2 [−65°C(t_2)]
1	0.80	0.5	0.33
2	1.12	0.7	0.47
3	1.12	0.7	0.47

* Initial resistance measured at 20°C.

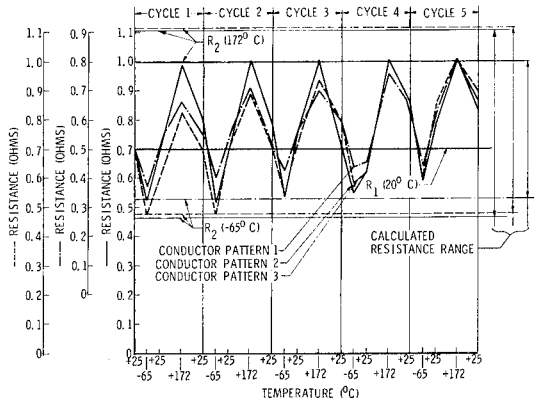


Fig. 14. Resistance measurement—thermal shock tests.

Table IV outlines the resistance values calculated for the temperature range of 172 to −65°C. During the thermal shock tests, no open circuits developed and no delamination of the laminates occurred on the multilayer boards. Figure 14 represents the resistance measurements during thermal shock for the same sample board previously run through temperature cycling. The resistance levels again indicate a small but continued increase caused by the extreme environments and oxidation of conductors.

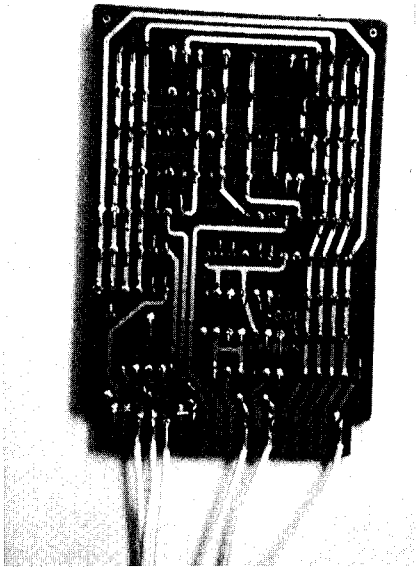
Figure 15 illustrates one of the sample test boards photographed before and after the thermal shock tests. The only visible difference is a discoloration or darkening of the assembly.

Vibration Tests. Six boards were selected from the 12 samples, and they were subjected to vibration in the major planes. Vibration tests were calculated over the frequency range of 10 to 2000 cps with an excursion of 0.060 in. for a range of 10 to 70 cps and an acceleration of 15.0 *g* between 70 and 2000 cps. The sweep time from 10 to 2000 cps and return was 20 min, and 12 cycles were conducted. This procedure was carried out for each of the three mutually perpendicular directions. After the 12th cycle, the test specimens were vibrated at resonance (1010 cps) for 5 min in the vertical plane (Fig. 16). Throughout the vibration tests, no abnormal resistance readings were observed for the sample boards under test. Resonance in the vertical plane, the most severe direction, also had no effect on the continuity of the circuits being measured. The resistance remained constant throughout the test.

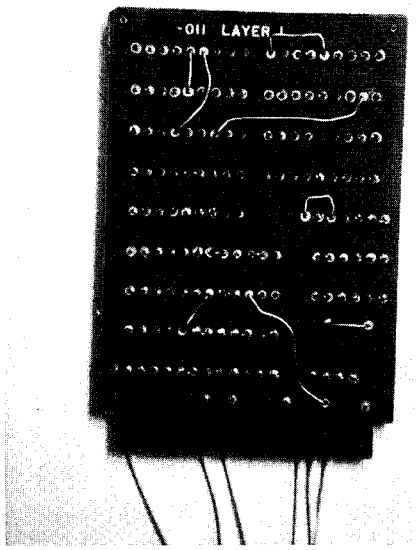
Humidity Tests. For these tests, the 12 sample multilayer boards were subjected to a continuous 10-day humidity test with the circuit resistance automatically recorded (Table V). Each cycle lasted 24 hours. Step (8) was run only for the third, fourth, sixth, seventh, and ninth cycles in a dry-ice atmosphere in accordance with Method 106A of MIL-STD-202B. For the remaining five cycles, Step (8) was replaced with three additional hours at 25°C.

TABLE V

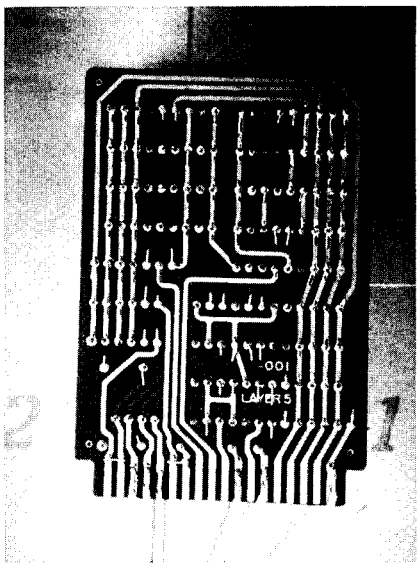
Step	Temperature, °C	Relative humidity, %	Time, hr
1	25 to 65	90 to 98	2.5
2	65	90 to 98	3.0
3	65 to 25	80 to 98	2.5
4	25 to 65	90 to 98	2.5
5	65	90 to 98	3.0
6	65 to 25	80 to 98	2.5
7	25	90 to 98	2.0
8	−10	Uncontrolled	3.0
9	25	90 to 98	3.0



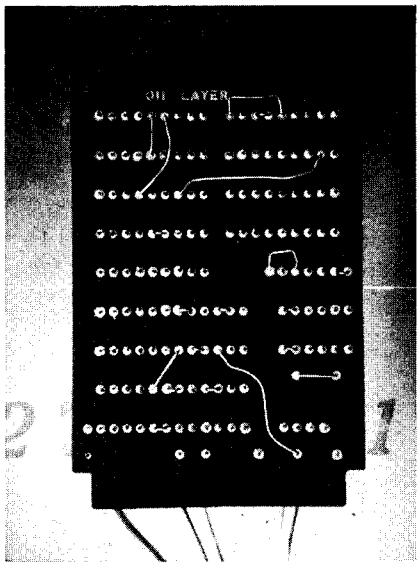
Before Temperature Cycling
(Circuit Side)



Before Temperature Cycling
(Module Side)



After Temperature Cycling
(Circuit Side)



After Temperature Cycling
(Module Side)

Note discoloration occurring after third cycle of temperature cycling

Fig. 15. Multilayer test board—thermal shock.

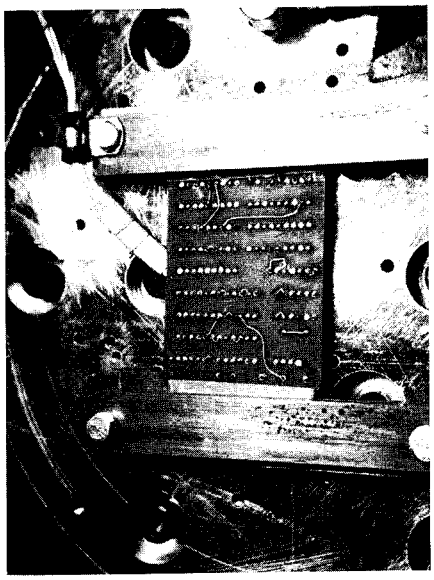


Fig. 16. Multilayer test board—vibration tests.

The resistance of the circuit patterns was calculated; the following tabulation gives the values at the temperature extremes of 65 to -10°C for these tests. The R_1 resistance values for the same circuit board are evaluated for temperature cycling and humidity.

The same 12 multilayer boards used for temperature cycling and thermal shock were tested for humidity. Two multilayer boards (3 of 36 circuits being tested) indicated momentary open circuits. In addition, there was a progressive increase in resistance during the 10-day period for the three marginal circuits; resistance values measured as high as 9 Ω and remained at that level after completion of humidity testing. Visual inspection did not reveal any damage or delamination of the boards, and there were no permanent breakdowns or open circuits. It may be necessary to run additional humidity tests before considering the use of a conformal coating for the multilayer boards.

CONCLUSIONS

Further evaluation on each of the design areas is anticipated by the Electronic Systems & Products Division before the work is completed. Additional evaluation of manufacturing processes and environmental testing is considered necessary to complete the designs, and further investigation of the material or the processes used for encapsulation of the avionics module is necessary. In addition, it may be wise to consider a conformal coating for the multilayer boards, especially where high humidity will be encountered.

TABLE VI

Conductor pattern resistance values, Ω	R_2 [65°C(t_2)]	R_1 [20°C(T_1)*]	R_1 [-10°C(t_2)]
1	0.94	0.8	0.71
2	1.06	0.9	0.79
3	1.18	1.0	0.88

* Initial resistance measured at 20°C.

ACKNOWLEDGMENTS

The author is indebted to those who worked on many of the technical areas and assisted in the preparation of this paper: G. E. Duman, T. P. Iodice, and R. A. Stephens of the Advanced Manufacturing Technology Section and G. P. Pankoff and R. E. Sauvageot of the Engineering Department.

8083

Recent Developments in Swiss Cheese Microcircuitry

BOB G. BENDER AND ROY W. DREYER
Hughes Aircraft Company, Semiconductor Division, Newport Beach, California

The well-known concept of pellet component circuitry known as "Swiss Cheese" has been considerably advanced and refined by the development of several processing techniques described herein. These developments include interconnection methods, repair techniques, and design ideas that are unique to the concept.

INTRODUCTION

THE "SWISS CHEESE" concept of microcircuit fabrication has always enjoyed a wide acceptance by production and engineering people, who are responsible for designing, building, and delivering hardware. However, not everyone was willing to embrace any or all of the connection techniques that have been available until now. The authors have spent the year since the last Packaging Symposium at Boulder seeking methods which would improve the ease of fabrication and the universal acceptance of pellet circuitry.

Since our first association with this project, we have sought a means for making low-cost connections simultaneously in large numbers, with a high order of reliability. Neither welding, connective adhesives, nor soldering are capable of answering all the needs of this new system. However, by applying several old, established processes which have been proven in other applications we feel the Swiss Cheese technique is now capable of taking a long step forward. The purpose of this paper is to discuss these processes as they can be applied to pellet component packaging.

PLATED INTERCONNECTIONS

The printed circuit board industry and the plating industry have combined to provide techniques for making plated-through holes. Such plated-through holes have been produced by the millions and have countless hours of field experience in Hughes' products and those of other companies. By applying this very simple technique to Swiss Cheese or Microseal* circuitry, the ease of fabrication and cost of such assemblies are substantially improved. The acceptance of the technique for interwiring by potential users of the system is greatly enhanced.

A Microseal circuit module is constructed from a drilled substrate and pellet components. The drilled substrate should be one which is amenable to accepting electroless copper plating. Our first choice and longest experience is with glass epoxy material 0.030 in. thick, clad on each major surface with a layer of copper 0.0005 in. thick. Devices are glued into their holes by use of an epoxy. Figure 1 shows the loading of such a substrate with devices.

After the epoxy has cured, it is necessary to thoroughly clean the surfaces of the substrate and the exposed faces of the devices of any residual glue, and to roughen the surfaces in an effort to prepare the board for subsequent electroless copper plating. This is accomplished by sandblasting, or by other suitable abrasive processes. Chemical cleaning of the board follows.

* Trademark—Hughes Aircraft Company.

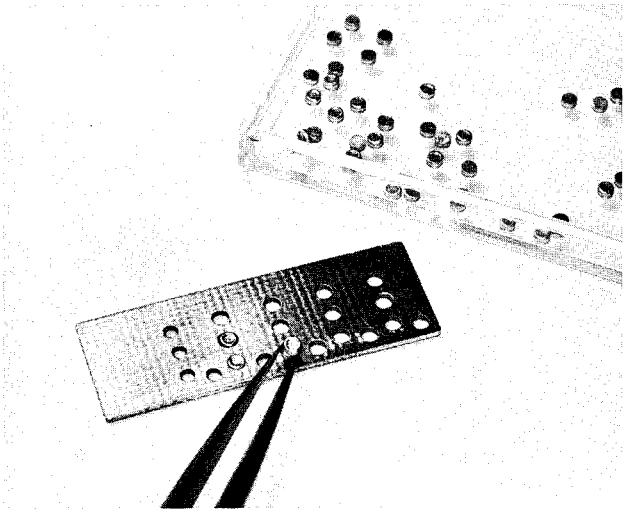


Fig. 1. Microseal diodes being loaded into copper clad glass epoxy card.

To sensitize the board for electroless copper plating, dips in stannous chloride and palladium chloride are necessary. This plating is accomplished in about ten minutes. Figure 2 shows the board after sandblasting and ready for the electroless plating step.

SCREEN PRINTING OF RESIST

At this time, the board is ready to be screen printed with a plating resist, such as vinyl ink, in the mode known as "reverse printing." This material is called the plating resist to differentiate between itself and the etch resist which will be described below. In this process, the screen pattern is such that plating resist is deposited over all areas of the circuit card not needed for wiring. Figure 3 shows a typical single image on a stainless steel screen and a single subject circuit card in position for screening of resist. The resist is then oven-dried so that

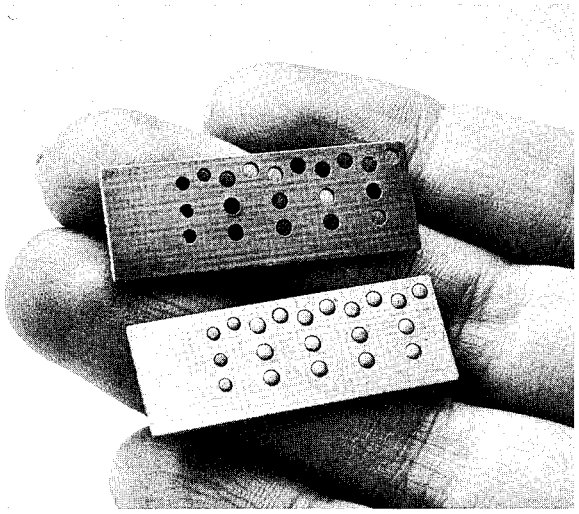


Fig. 2. Microseal diodes in their sites ready for plating.

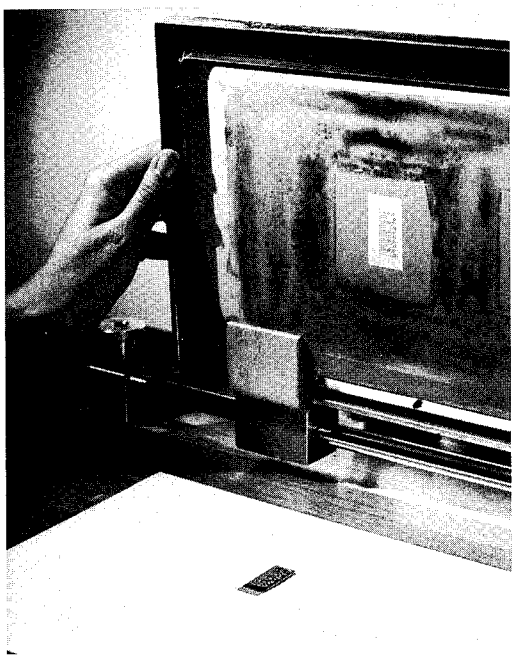


Fig. 3. Setup for screen printing of plating resist on Microseal circuit module.

the process of screen printing may be repeated for the reverse side, with the appropriate mating screen pattern. Figure 4 shows the reverse printed module ready for patterned electroplating.

Electrodes are attached to the board and the familiar copper electroplating process is allowed to proceed until the proper thickness of copper is obtained on the unscreened areas. Usually 0.0015 to 0.002 in. is sufficient. Incidentally, where feed-throughs are required in the circuit, a hole, the diameter of which is not less than the thickness of the board, will plate through in this process quite nicely. Thus, feed-throughs are obtained for the price of the drilling.

To provide an etching mask for the copper plated wiring, it is desirable to cover the plated copper with a plating with a tin–nickel alloy until a bright, continuous, pinhole-free surface

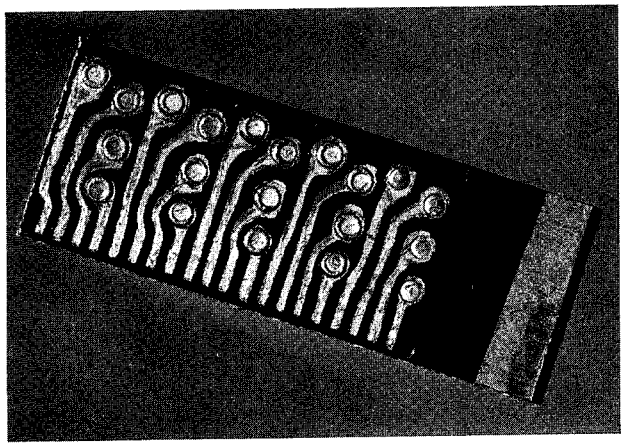


Fig. 4. Microseal circuit module with plating resist applied, ready for electroplating.

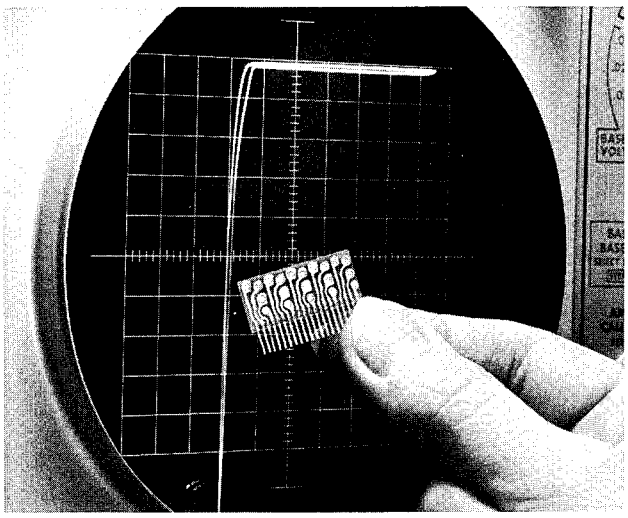


Fig. 5. Finished Microseal circuit module made by the plating process.

is obtained. A coating of 0.0002 in. thick is a minimum satisfactory thickness. At this point the organic plating resist is removed and the part immersed in warm ferric chloride or other suitable etchant to etch away the unwanted copper from the exposed areas of the card. Because plating has been done selectively, and because the tin–nickel serves as an effective etch mask, the etching process will proceed rapidly and cleanly, with little danger from overetching. Figure 5 shows the finished module with plated interconnections as described above.

PROCESSING IN MULTIPLES

The technique described above lends itself admirably to the processing of Swiss Cheese circuit modules in multiples. The principal advantages of this system are in handling, screening, and plating economies derived from the manufacture of as many modules at a time as possible.

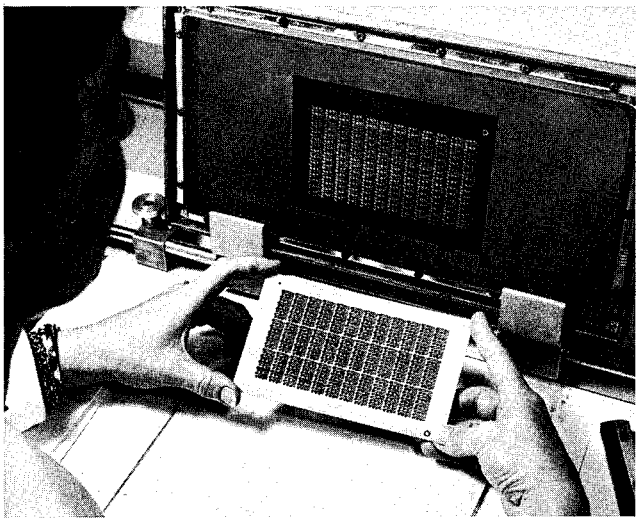


Fig. 6. Multiple image mask formed by screen printing for etching of Microseal plated modules.

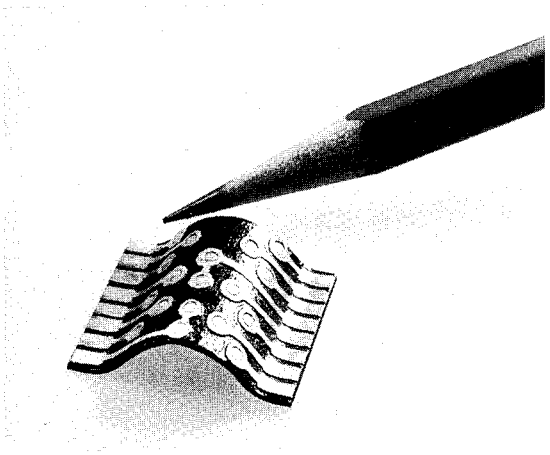


Fig. 7. Microseal circuit, hard anodized aluminum substrate—showing compound radius of curvature.

The practical limitations are usually those of screen sizes and plating bath facilities available. The 36-image module shown in Fig. 6 might be made in multiples of 75 to 100 as an example before being subject to "diminishing return" factors. The advantages in general are obvious.

THE BIG BOARD CONCEPT

A natural consequence of processing Swiss Cheese modules in multiples is the big board concept. Having successfully made large numbers of multiple modules of identical circuit layout, it is inevitable that one should begin to think of laying out more circuitry on a single card. Such complex layouts are interconnected so that more functions are accomplished by the single large card, rather than severing it into individual modules.

The principal advantage of the big board concept is that it allows maximum utilization of this technique for simultaneous creation of low-cost mass interconnections while minimizing the number of out-connections.

Individual pellet devices are conditioned and tested before being committed to circuit card manufacture. This, and the fact that the circuit cards can be repaired with ease, permits us to think of building modules of large numbers of components. Other microelectronic techniques are prohibited from using as many components as are possible by the Swiss Cheese

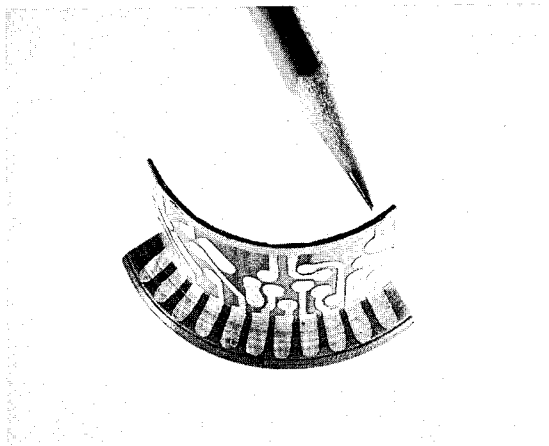


Fig. 8. Microseal circuit on laminated phenolic—top view showing 2 in. radius of curvature.

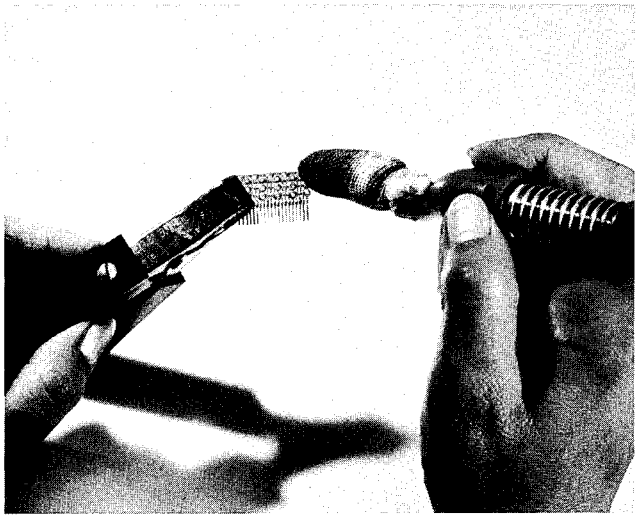


Fig. 9. A plating repair being accomplished by means of the Dalic technique.

technique, simply because the yield factor on complex processes and individual devices would make the cost prohibitive.

The principal disadvantage of the big board concept is that it is hard to trouble-shoot to find a failed component. This disadvantage is not unique to pellet component circuitry, but is true of any circuit card which contains a large number of components.

CONFORMAL CIRCUITRY

Occasionally a systems designer is confronted with putting a given amount of electronics into an irregularly shaped cavity. The pellet component approach offers a good deal of flexibility for this purpose. The circuit card can be made of curved shapes or compound curved shapes as shown by Figs. 7 and 8. It is not only possible to accomplish a peculiar cut of the shape of a card, but also the contour of the card can be patterned.

PLATING REPAIR

One of the outstanding advantages of the "Swiss Cheese" concept has been the ease with which effective repairs of faulty single components are made, in the factory or in the field. The plating process does not compromise this advantage at all. While the plated module can always allow the emergency repair of a component by replacement and skillful use of a soldering iron, there exists a technique by which the component may be replated in place.

To effect a repair, the part is carefully punched from the substrate, leaving the plated pad surrounding the hole intact; a fresh part is inserted, and by means of the Dalic plating system a plated repair is made in minutes. It is only necessary to fix an electrode to the circuit path in which the replaced device lies, and apply the plating solution to the affected area with the padded stylus, as shown in Fig. 9. The plating proceeds at moderate temperatures and provides a bridged joint of any desired thickness. After the module is washed with water, it is ready to be tested and restored to service.

CONCLUSIONS

All of the technologies necessary to interwire pellet components into useful electronic arrays are now known. For the most part they are composed of processes and materials which are familiar and have been proven with years of field experience. A particular example is that of plated-through holes. Hughes has made millions of plated-through holes and has

an enormous amount of field experience with them. Reliability of these known proven processes constitutes a forecast of the kind of reliability one can expect from using these processes and materials for making pellet microcircuits.

Since tooling is reasonable in cost and circuit design is extremely flexible, it is reasonable to anticipate that this technique will enjoy a bright and enduring future in microminiature packaging of electronics. This should prove especially true of circuits which are of special design or not highly repetitive.

8084

3-D Welded Module Design and Manufacturing Control Parameters

H. F. SAWYER
General Dynamics/Pomona, Pomona, California

This paper comprises in effect an advance report on an extensive study undertaken by General Dynamics/Pomona under contract with the U.S. Army Electronics Research and Development Laboratory, which has long recognized a need for establishing design, process and control standards for 3-D welded modules. The paper discusses in detail the purpose of the research, the research tasks as these were defined, the methods employed in testing, and the results obtained. A handbook which resulted from the completed study is appended.

INTRODUCTION

THE U.S. ARMY Electronic Research and Development Laboratory has recognized a need for establishing design, process, and control standards for 3-D welded modules. A research program was established which summarizes and clarifies the most important factors in this form of electronic miniaturization. The Research Program was implemented to derive appropriate guidance in some controversial subjects.

A size comparison was made which establishes the range of expected volumetric differences between cordwood packaged electronics intraconnected by welding and by soldering. A particular set of digital modules was chosen as a basis for this comparison. A gate module, a flip-flop module, and a driver module were used in the comparison because a soldered version had previously been studied. The welded version used parts which were nearly identical in size, but which were selected primarily for the controls exercised on the lead coating, dimensions, and material.

A number of each of these modules were constructed for demonstration of the techniques and as test items. The sample modules contained four materials for component leads which are representative of general industry use acceptable for 3-D welded modules.

A comprehensive weld sample test program was completed to allow accurate reliability estimates on all material combinations tested. A number of ancillary characteristics were defined and tested during the joint testing research. A valuable conclusion to the test program was the realization that normal statistics should not be used for reliability estimates. Reliability estimates were made for each material on the basis of allowing no more than three welds in a thousand having strengths lower than 30% below the mean. The distribution free statistic was found to be a method of estimating reliability not subject to gross errors. Joint testing included a measurement of the shift in the mean due to 100 cycles of thermal shock exposure on copper. Joint resistances were investigated and compared with joint strength both before and after thermal shock exposure. The pull testing rate was studied and tests were conducted to ascertain the effect of pull test rate on joint strength measurements. Operator effects were seen to cause major changes in joint minimum strength while between operators effects were shown to be insignificant for very limited testing with two operators on one material. Vibration

tests of three test modules verified that none of the weld joints would fail at 30 g or below at test conditions. Shock tests are yet to be performed by USAERDL.

Design Process and Parameter Controls were summarized and documented. The purpose of formalizing the important factors involved in obtaining high reliability is to permit universal use of these controls whenever the method is employed in manufacture. A handbook resulted from this research which is included as an appendix to this paper.

The main factors considered are:

1. Engineering design
2. Parts selection
3. Manufacturing aids
4. Lead control
5. Weld schedule development
6. Part handling
7. Manufacturing environment
8. Qualification of manufacturing equipment
9. Process controls
10. Quality control

MODULE SIZE COMPARISON

Three sample modules were designed using the design requirements established in the General Dynamics/Pomona "3-D Welded Module Design Standards" and the Signal Corps Specification SCL-7641. In addition, special lead preparations were necessary to meet the requirements of SCL-7641 in order to make the welded modules compatible with the soldered versions. Component leads and jumper wires were crimped and coated with Dow Corning DC-271 to relieve stresses as the result of thermal differential expansion.

Module header pins were located on a 0.100 grid for standardization and simplification of module distribution system. Resultant sizes, volumes, and space densities of the welded modules compared to the soldered modules of the same type are tabulated in Table I. The table shows a difference in total component body volume in the case of the Driver-Type B Module indicating the use of other than maximum component dimensions on the soldered module. The comparison of space density illustrates the similar utilization of volume by both techniques. It is observed that the difference in volume achievable is primarily based upon the layout design and will not exceed $\pm 15\%$. The flip-flop module is shown in Fig. 1 and is representative of the design and construction of all three.

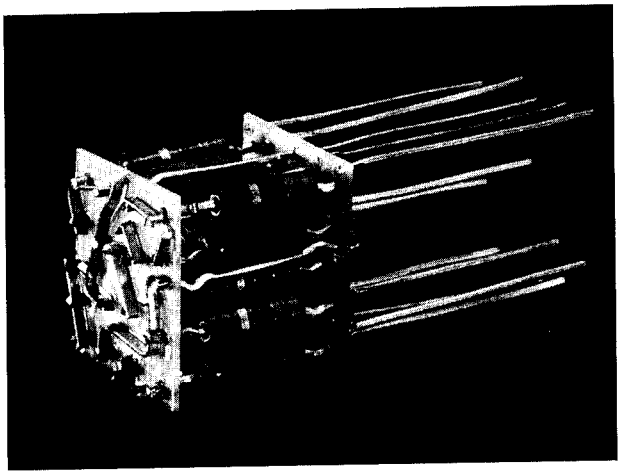


Fig. 1. Flip-flop module.

TABLE I

Size Comparison Soldered vs. Welded Modules

Module type	Dimension, in.	Volume, in.^{3}	Total component body volume, in.^{3}	Space density, %
	Welded Modules			
Flip-flop	(0.550 × 0.500 × 0.651)	0.179	0.050	28
Two-input gate	(0.360 × 0.500 × 0.651)	0.117	0.024	20.5
Driver-Type B	(0.540 × 0.585 × 0.651)	0.205	0.066*	32.2
	Soldered Modules			
Flip-flop	(0.525 × 0.600 × 0.578)	0.182	0.050	27.5
Two-input gate	(0.524 × 0.450 × 0.578)	0.136	0.024	17.6
Driver-Type B	(0.524 × 0.600 × 0.578)	0.182	0.052*	28.6

* See text.

COMPONENT LEAD DATA

The selected lead materials specified for the sample modules are applicable to any welded module design without reservations. Other lead sizes are to be expected as components may dictate but it should be possible to limit materials to the four selected. Component parts were selected primarily for size compatibility with the SD4 solder module components to provide an equitable basis for the sizing study. The lead materials chosen range from the most weldable materials, "A" nickel wire, to the most difficult, copper. The weld combinations are all made with 0.012 × 0.030 "A" nickel ribbon which is used throughout as an interconnect medium. The selection of this interconnect material is based on the following factors:

1. Good structural results with nearly all common lead materials.
2. Acceptable metallurgical conditions at the interface.
3. Compatibility with lead size ranges in common subminiature parts.
4. Experience at General Dynamics/Pomona with this material.

The selection of this interconnect material does not imply that other materials or sizes would not yield as good results.

Selection of lead materials without regard for other factors in component part parameters was not done. The selection of parts with considerable historic data available on part performance preserves their reliability and allows the use of their design parameters. In particular, heat dissipation of components is mostly by conduction along the lead wire. Specifying lead wire for weldability alone without regard to other conditions is not acceptable. Changing to a lower thermal conductivity material requires derating the power capacity of the resistor.

The selection of copper, where appropriate, is based upon the best combination of conditions, including an assurance that welding of copper to the interconnect medium can be done with good strength, minimum scatter, and acceptable metallurgical conditions.

The degree or ease of achieving a high-strength weld using lead materials typical on electronic components will vary depending on the material composition and the diameter and plating of the lead. Some materials are readily weldable over a wide range of diameters, while others are less flexible. A knowledge of material *vs.* its weldability is required in order to establish the importance of these variations.

A material desirability rating is supplied as follows for the component lead materials and joining media:

Material welded to 12 × 30 mil nickel ribbon	Desirability order (Min. strength/sample size)
Nickel wire	15.5/300
Kovar	11.0/800
Copper (0.032 dia.)	8.6/784
Dumet	8.0/800
Copper	7.0/793

The above numerical comparison or order is based exclusively on minimum strength, weight, and sample size. Each material is rated when welded in a cross wire configuration using 0.012 × 0.030 nickel ribbon. The series of numbers under the heading, "Desirability order," indicates the minimum breaking strength of a given material combination together with its sample size. A complete guide is required for all material combinations used compared at the same sample size. In addition, it is desired to have these comparisons for various sample sizes. The costs and methods of obtaining and maintaining the reliability of each weld combination may be different.

Due to the large number of component manufacturers currently supplying industry, a wide range of component lead diameters exists. It has become desirable to limit the number of different lead diameters available to effect reliable welding at reasonable costs. Unless such a limiting control is placed on component lead diameters, many costly and unnecessary control data must be generated, such as weld schedules and metallurgical, chemical, and statistical analyses.

Satisfactory results can be experienced for most applications by limiting the lead diameters to a few sizes in a specified range. The preferred nominal diameters are 0.016, 0.020, 0.025, and 0.032. The above lead sizes will accommodate nearly all components currently being manufactured for modular application.

Component lead plating cannot be directly associated with any basic lead material. One type of lead material may be found with a variety of finishes or coatings. Dumet, as an example, can be supplied with a gold plating, a solder coating, or unplated finish, depending on the component manufacturer. The selection of preferred components with emphasis on meeting *standard* finishes will automatically decrease the number of different lead plating types. The uniformity of the lead coating is just as important as the coating itself. Requirements should be established to control the uniformity with respect to the chemical composition or purity of the different materials being used. Acceptable limits must be defined describing maximum and/or nominal allowable percentages of each element including trace elements. Generally, there are applicable military specifications completely describing the quality levels and necessary controls. For applications not as yet outlined in military specifications, appropriate standards will have to be introduced.

In most cases, the military specification describing plating thicknesses is adequate. However, these specifications usually do not include requirements necessary for welded module application. As an example, Specification MIL-G-45204, Type I, Class 1, specifies a plating of 50 μin. minimum and no maximum thickness restriction. Class 6 specifies 1500 μin. minimum and no maximum. In reality, Class 6 plating conforms to the previous five; therefore, maximum limits should be determined on the thickness of all plating materials chosen for needed module applications. All lead plating material having applicable military specifications should use these specifications as a basis for determining the necessary controls. In some instances, the military specification as written may suffice.

Intermixing of leads on the same weld schedule with different plating materials or thicknesses cannot be tolerated and care must be exercised to assure consistent lead physical properties. The tests of one of three dumet materials used in the sample modules yielded poor results due to variability in plating. Thirty out of 800 dumet welds had pull strength less than 9 lb. The low weld strengths tended to occur in pairs, corresponding to two welds on the same lead, which indicated a material problem. The low-value strengths were caused by failure to penetrate

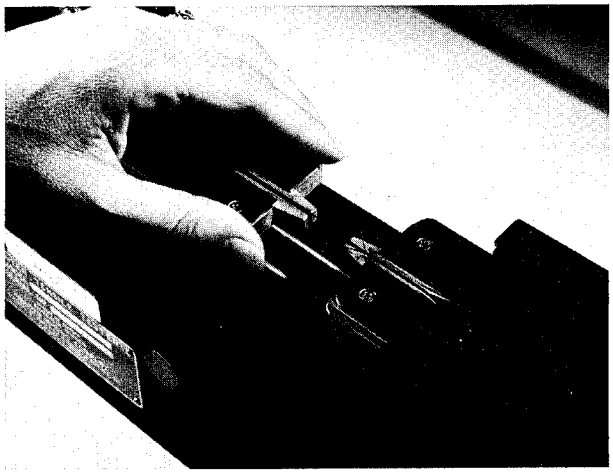


Fig. 2. Torsional shear test.

the copper sheath of dumet during welding. All 12 of the weld specimens observed exhibited this condition. A reliable dumet-to-nickel weld requires joining of the ribbon to the iron–nickel core material. The weld schedule for this combination was made for dumet with core material, copper sheath, and gold plating. The poor welds resulted by welding a similar dumet to the same schedule; this similar dumet was the same except for a 250-μin. silver plating between the copper sheath and the gold. Micrographic analysis should be employed on all lead materials used in a welding program as one of the production checks on lead material consistency.

WELD SCHEDULE PROOFING

There are several steps to be taken in determining the quality of a welded connection. These steps include mechanical testing, visual inspection, and metallurgical analysis. Each of these must be included in the development of an optimum weld schedule.

Weld schedules were developed for the materials used by the use of isostrength diagrams, metallurgical analyses, and torsion-shear weld joint pull testing.

The most discerning of the mechanical test procedures available is the torsion-shear test, in which the coupon is stressed as shown in Fig. 2. This places the weld coupon under combined tension, torsion, and shear stresses. The manner in which the coupon fails is significant, and this information, as well as the numerical value obtained from the pull tester, is recorded. A tension failure indicates that the weld and adjacent areas are stronger than the parent material; a torsion failure shows insufficient fusion, and a shear-tension failure indicates a weakness in the parent material adjacent to the weld. The most desirable condition is usually obtained when coupons from the same group fail from a combination of causes, such as tension and shear-tension failures.

It is incorrect to generalize the requirements of such factors as deformation, type of interface, and structure. Optimization of each material combination should include the optimum physical characteristics which are *discovered* by metallurgical analyses by a professional metallurgist. Metallography should be employed to each material and geometric combination for the purpose of photographically recording the micrographic appearance of optimum welds. The procedure involves determination of optimum metallurgical appearance for each material combination, then confirmation by comparison with the appearance of other catalogued similar material combination.

The basic considerations found applicable to all resistance weld processes involve (a) heat balance—influence of electrode materials and electrode face, and (b) extent of heat-affected

zone. Limitations here are applied where (1) insufficient large heat zone causes low weld strength while the structure may be "excellent" and (2) an excessively large heat-affected zone may degrade the properties of the parent metal cross section out of the weld zone. Excess heat can cause undesirable electrode contamination.

In welding process control, duplication of a condition previously determined as acceptable is sought rather than "optimum" structure. For example, the basic object of a dumet-to-nickel weld is to (a) expel the copper sheath exposing a nickel-to-dumet core interface, and (b) limit overheating of the copper sheath (of dumet) to prevent electrode contamination due to skin melting. Metallographic analysis coupled with mechanical analysis will corroborate (a) above; similarly, weld strength consistently should corroborate (b).

The isostrength diagram is a tool that can be used to understand development. The isostrength diagram provides a method of showing a three-dimensional picture on a two-dimensional surface in a manner analogous to an aerial map showing contours of the earth's surface.

The isostrength diagram appears as a series of steps ascending a hill. Each step represents the average value of a sample of welds taken at some specific energy and electrode force setting. As the energy and force are increased in proper proportion, the height of the steps becomes larger, until some optimum energy and force setting is obtained. At that point, the peak of the hill has been reached and the highest average weld strength is obtained. This does not necessarily mean that the optimum weld schedule is always found at that point. If excessive deformation results from using that weld schedule it may be necessary to compromise; likewise, if the high value is followed by a sharp drop-off to some undesirable value, it would be preferable not to operate in that area.

Each point on the isostrength diagram is found by averaging the strengths of 60 welds (smaller samples are often used, but the results are then too broad to permit a valid choice between adjacent points) made at the corresponding energy and pressure settings. The differences in strength between each point on the isostrength diagram are quite close and one must

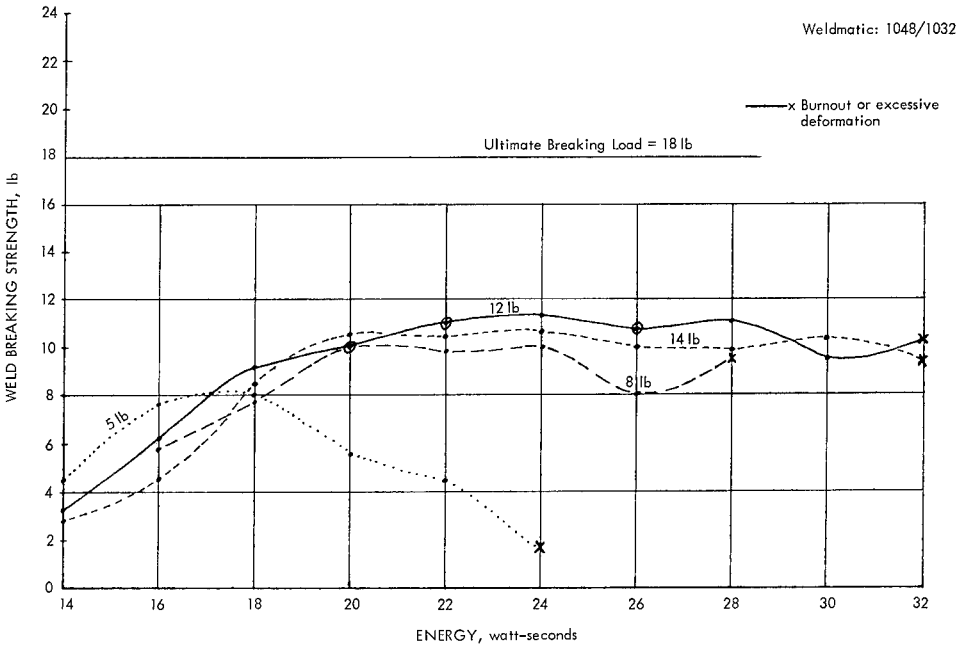


Fig. 3. Weld parameters profile (25 mil copper to 12 × 30 mil nickel).

be sure he is getting a difference, not merely reading the normal variability in the materials. In order to minimize other variables such as operator effects, power supply differences, and others, a complete isostrength should be made by one operator on one machine all at one time with a supply of lead materials deliberately randomized. If an interruption in the process occurs, repeats of certain points should be made to determine degree of compatibility with prior conditions.

A weld profile method of establishing an optimum weld schedule is recommended as a means of providing a more efficient and simplified approach than that of the isostrength diagram. The weld profile is a plot of weld breaking strength *vs.* energy at constant electrode pressure as shown in Fig. 3.

The weld profile method is actually more meaningful than the isostrength diagram since the dependent variable, weld strength, is plotted permitting its variations to be read directly.

Through the use of a weld profile it is possible to completely analyze the average weld strength and the range of strengths at each energy setting. A line drawn through the average strengths will usually establish a plateau of high-average-strength values. The plateau is then examined and a point is selected which shows a combination of high average strength and low spread from the high to the low value within the sample. A sample of ten welds is usually made at each energy setting on the chart and the profile is plotted as the joints are made and pulled so that additional points may be called for as indicated by the plotted curves.

Weld schedule proofing consists of making weld samples in a prescribed large sample size, 800 for this program, where all production personnel and equipment variables are included. The sample should include different machines which have been qualified to the same schedules, different qualified operators and qualified materials which have been deliberately randomized.

There has been concern regarding the effects of pull test rate on the test weld samples. A test was formulated to determine the effects and the variability contributions, if any, for three pull test rates. One hundred and eighty welds of 0.025 copper wire to nickel ribbon were randomly divided into three groups of 60 each. The three groups were then pulled on a Hunter tensile tester at pull rates of 1 in./min, 30 in./min, and 60 in./min. The sample standard deviations for each point were compared by Bartlett's test and the hypothesis that there were no significant differences was not rejected at 0.10 level of significance. The deviations were then pooled and a straight line was fitted to the data. Figure 4, the line,

$$y = 0.0103\,X + 8.81$$
$$y = \text{Number} = \text{Pull strength result}$$
$$X = \text{in./min} = \text{pull rate}$$

passed through the means of the samples at each of the three points (to 2 decimal places). As a result, the hypothesis of linearity was not rejected and a confidence limit on the slope was obtained.

A 90% confidence interval on the slope is 0.0058 to 0.0148. This corresponds to a 0.62-lb. increase $\pm$0.268 lb from 1 in. to 60 in./min. The average breaking load $\bar{y}$ ranged from 8.81 $\pm$ at 1 in./min to 9.45 $\pm$ at 60 in./min; the change in $\bar{y}$ is 6.6% over this range.

SAMPLE WELD TEST RESULTS—SCHEDULE PROOFING

The weld samples made on each lead combination of the three sample modules were tested and the proofing results are shown in Table II. The uncorrected percent standard deviation did not exceed 12% for any material, with 0.025 copper and 0.020 nickel exhibiting the lowest values.

JOINT RESISTANCE TESTING

The requirements for joint resistance which were stated as a goal for all joints used in the sample modules are that, at a 90% confidence level, no more than three joints out of a thousand shall have resistance differing by more than 30% from the mean value of resistance. This resistance was to be measured initially and after every 25 cycles of thermal shock; the measurements were to be made at an accuracy of 0.1 mΩ.

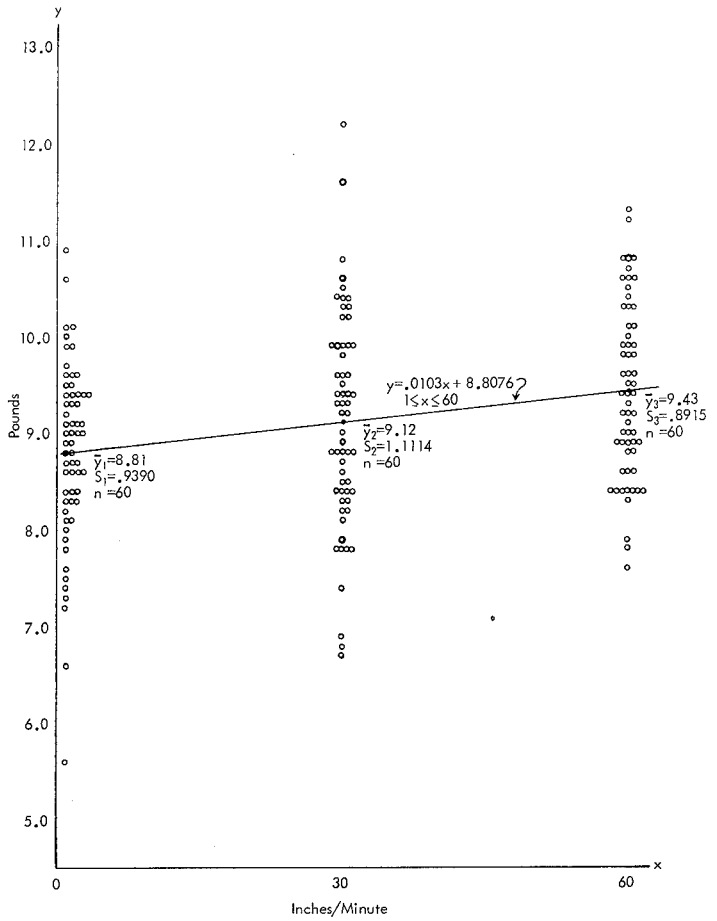


Fig. 4. Hunter tensile tester—pull rate *vs.* weld strength for 0.025 Allen & Bradley solder-coated copper welded to nickel ribbon.

The initial testing was performed to determine (1) the magnitude of values to expect, (2) the repeatability of the measurements, and (3) correlation with joint pull strength. Resistance measurements were taken on 100 welds of 0.020 nickel to 0.012 + 0.030 nickel ribbon. The test setup consisted of supplying a steady-state current through the sample and reading a voltage drop across the weld. Repeatability was good for this sample and the results were as follows:

1. Maximum repeatability error—13 $\mu\Omega$
2. Average repeatability error—$<4\mu\Omega$
3. Average resistance—46.1 $\mu\Omega$
4. Standard deviation—5.1 $\mu\Omega$

A waiting period of one minute was required for stabilization before measuring each resistance, particularly on dissimilar materials. Resistance measurements at the specified accuracy level of 0.100 mΩ would be meaningless since no statistical analyses could be made. Correlation of weld strength for the combination was shown to be nil over the range of weld strengths tested. The testing plans were accordingly modified so that resistance analyses and correlation with strength could be measured as desired.

TABLE II

Sample Weld Test Results of All Component Lead Materials

	Lead material	Mean $\bar{X}$, lb	Standard deviation (uncorrected), lb	% Standard deviation (uncorrected)	Sample size
(1)	0.025 copper	10	1	10	1296
(2)	0.032 copper	17	1.6	9.4	1300
(3)	0.020 nickel	17.6	1.6	9.1	1301
(4)	0.020 T.I. dumet	16.7	1.7	10.2	1348
(5)	0.020 Glenco dumet	16.1	1.9	11.8	1304
(6)	0.020 Raytheon dumet	16.5	1.95	11.8	1380
(7)	0.017 Kovar	16.9	1.8	10.7	1315
	0.020 dumet*	16.7	2.0	12	1153

* Mixed, all manufacturers.

All resistance readings should be interpreted as apparent resistance. There are other factors entering into the voltage drop across the weld which may be much larger than the ohmic resistance. Actually, the voltage measured between the non-current-carrying ends of the test samples proved that the interface resistivity was of the order of the bulk material resistivity and that no measurable interface resistance was evident. When like materials are joined, other contributing factors are minimized so that an analysis of the results may be made.

One hundred weld samples for each of four materials (0.020 nickel, 0.025 copper, 0.017 Kovar, and 0.020 mixed dumet) were pulled after thermal cycling, and the weld pull strengths plotted against apparent resistance. The plots are given in Fig. 5. The plots indicate that there is no practical correlation between weld pull strength and apparent weld joint resistance.

Apparent weld joint resistance was also measured after every 25 thermal cycles for samples of the above four materials. The change in apparent resistance was significant at the 10% level of significance for 0 to 25 thermal cycles. It was suspected that this significant change could have been due to a drift in the test process. A control sample was incorporated to check this hypothesis. The control sample indicated that from 50 to 75 to 100 thermal cycles, the test process drifted more than could be accounted for by repeatability error. Therefore the apparent change from 0 to 25 cycles is viewed with suspicion, and reporting of any other results would be dependent on bringing the process under control.

Considering the delicacy of the experiment, repeatability was good, which indicates that the extraneous factors other than resistance were relatively constant. The average repeatability error over all materials on a sample of 45 was only 6 $\mu\Omega$. However, this repeatability was over a short time interval (1–4 hr) and longer-term repeatability was not evaluated.

For the evaluation of resistance change with thermal shock, the normal distribution was assumed since comparison tests of this type are relatively insensitive to deviations from normality.

All the voltages read on the resistance tests for 0.020 nickel to nickel ribbon gave negative values. The observed differences in the polarity of voltages read across other joints were studied and an explanation is given. A constant current power source was used in the test circuit; a current of 2 A was provided through each joint and the voltage was measured across the joint with a Model 203 Kintel microvoltmeter (Fig. 6).

As shown, the test connections were made expecting a voltage drop in the joint. The voltage gradient which exists along the wires where they overlap is greater than the interface voltage drop, if any. The polarity of the reading is then appropriate for a section of a continuous wire instead of a weld joint where the non-current-carrying ends of the joint act only as voltage probes (Fig. 7).

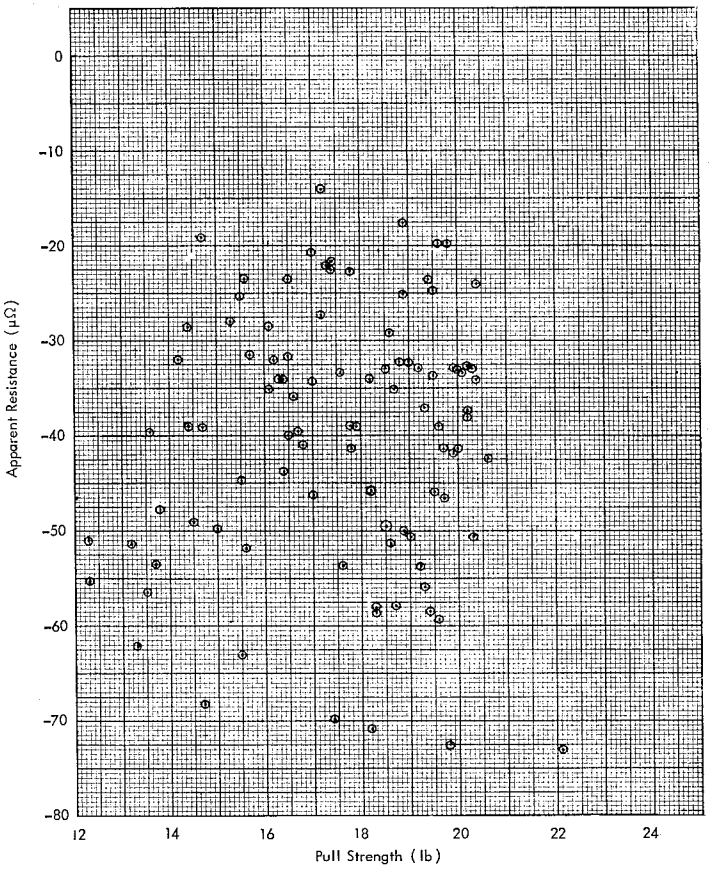


Fig. 5a. 0.017 Kovar weld resistance *vs.* pull strength for a sample of 100.

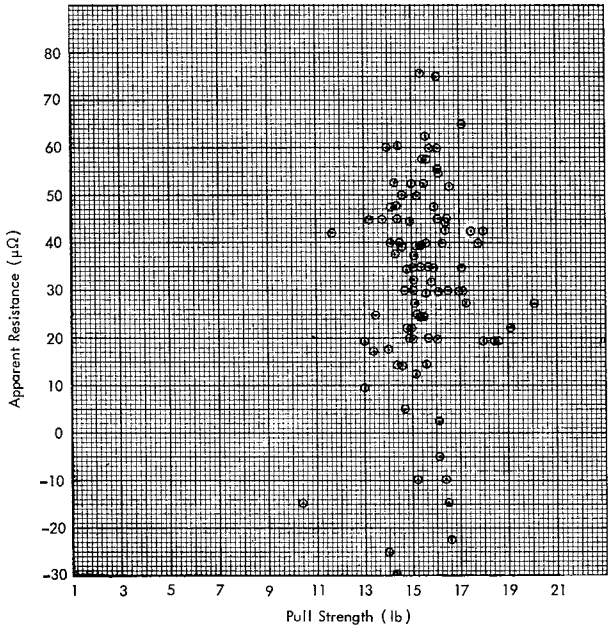


Fig. 5b. 0.020 dumet weld resistance *ps.* pull strength for a sample of 100.

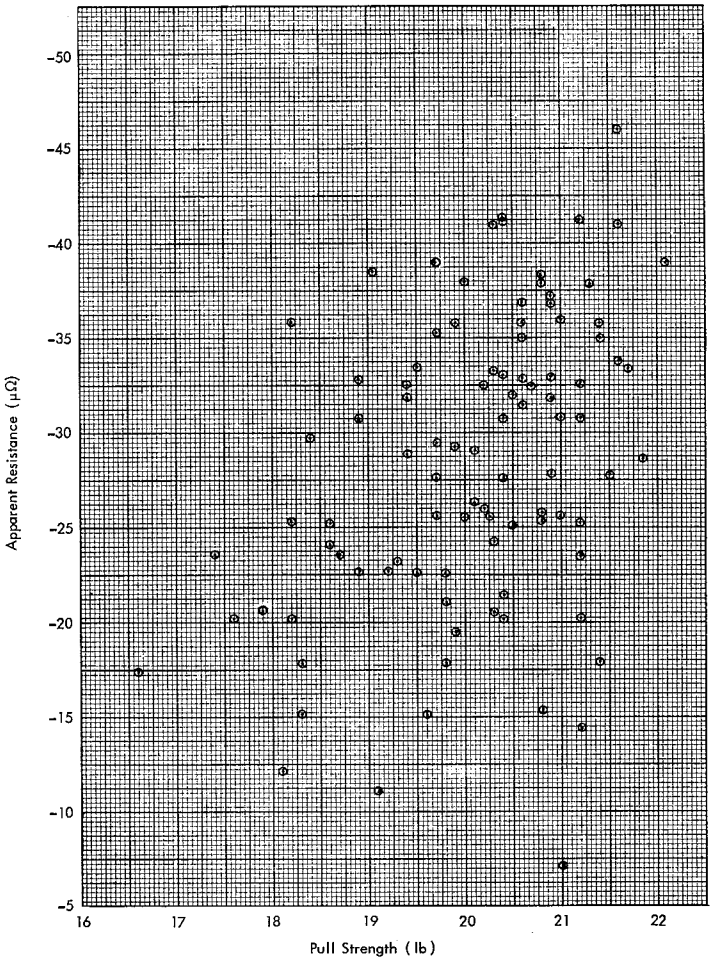


Fig. 5c. 0.020 nickel weld resistance *vs.* pull strength for a sample of 100.

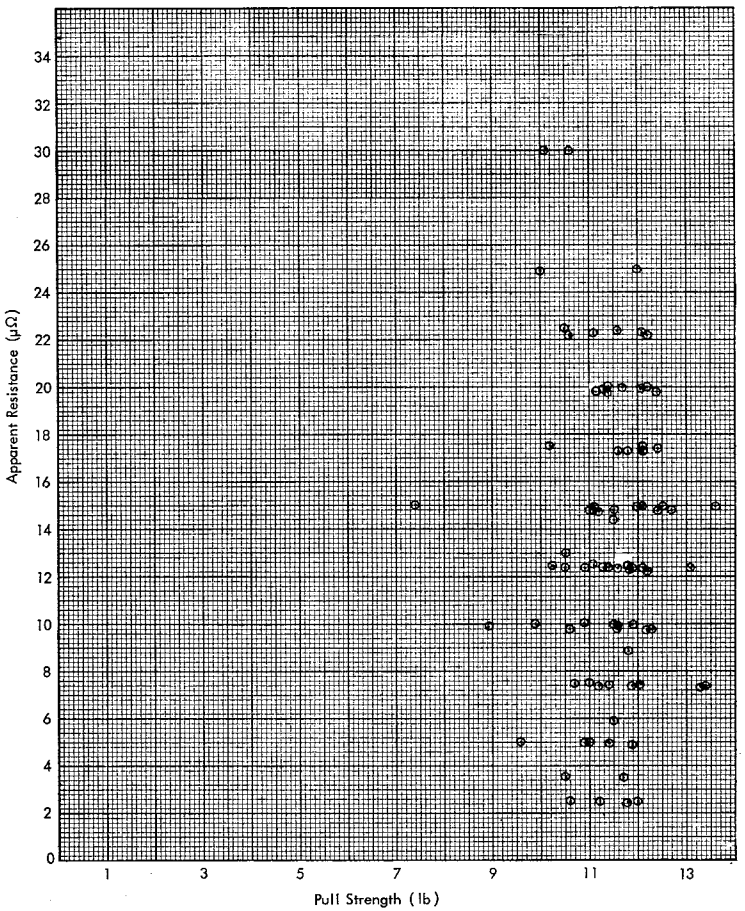


Fig. 5d. 0.025 copper weld resistance *vs.* pull strength for a sample of 100.

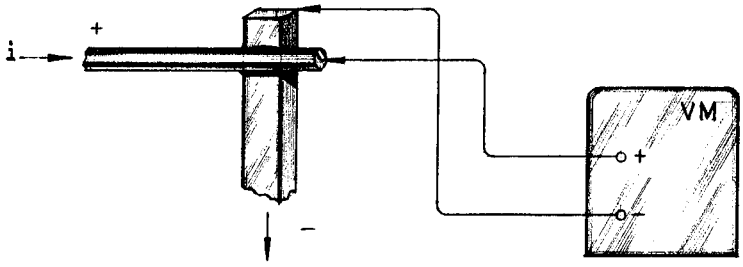


Fig. 6

With the other material combinations, Kovar, copper, and dumet, dissimilar metal couple voltages, which are temperature-dependent, sometimes caused polarity reversals indicating the presence of other voltage sources in the joint.

WELD PULL TESTS AFTER THERMAL CYCLING

The seven materials which were welded with 12 × 30 nickel ribbon, in test samples, were exposed to thermal shock as prescribed by SCL-7641, paragraph 3.3.1.1 (100 cycles −65°C, +25°C, 200°C, 25°C). The requirements of joint strength after shock are that no more than 3 out of 1000 welds shall have a pull strength differing by more than 30% of the mean. The amended specification allowed an additional 8%, to 38%, providing there were compensating effects. Comparisons are provided on several bases for this requirement. If we assume normality for the specified requirement, it is necessary to perform transformations for each distribution in order to effect a comparison.

From the lack of positive correlation between the standard deviation S and minimum strength, it is evident that it is not sufficient to consider only the sample mean and standard deviation in predicting weld reliability. For example, Kovar exhibited a high minimum strength (11.1 lb or $\bar{X} - 37.6\%$) even though S was quite large (1.828 lb), whereas copper exhibited a low minimum strength (2.6 lb or $\bar{X} - 75.2\%$) even though S was small (1.164 lb). This was not unexpected since the distribution of pull strengths was not expected to be normal for many reasons. The most obvious reason is the physical truncations at 0 lb and at the parent material strength.

In addition to the non-normality, no two material samples had similar distributions. This lack of similarity indicates that a somewhat different physical phenomenon is responsible for the pull strengths for each different material. The lack of a satisfactory explanation of these marked differences makes the selection of an empirical distribution of pull strengths a hazardous task. Any assumption regarding the form of the distribution can result in gross errors, especially if predictions are made outside the range of the data. Therefore, distribution-free estimates [1], (pp. 385–390) of the population percentiles are given for all the materials. The estimates in these circumstances have a high producer's risk and are only available at discrete points. These objections, however, are minor considering that the estimates are free from serious error.

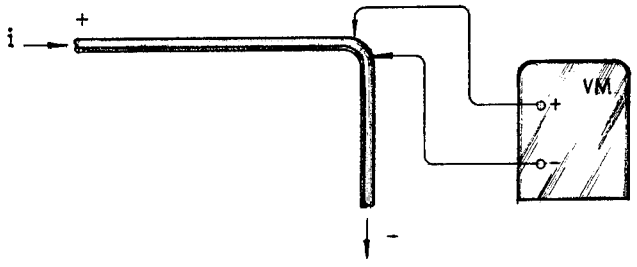


Fig. 7

TABLE III

Sample Weld Pull Test Data Summary

(Pull strengths were recorded to the nearest 0.1 lb except as noted.)

Material	Sample size		Average pull strength* $\bar{X} = \frac{\Sigma X_i}{n}$		Standard deviation* $S = \sqrt{\frac{\Sigma(X_i - \bar{X})^2}{n-1}}$		$S = \%\bar{X}_4$		Distribution-free estimates of X/1000 points†		Distribution-dependent estimates of 3/1000 points	Minimum strength‡ (lb/qty)	
	Prior	Shock	Prior, (lb)	Shock, (lb)	Prior, (lb)	Shock (lb)	Prior	Shock	X	%		Prior	Shock
0.020 nickel	1301	300	17.6§	20.1	1.60§	1.01	9.1§	5.0	7.7	22.4	$\bar{X}$-18% tr nor.	12.0/1301	15.6/300
0.032 copper	1300	400	17.0§	—	1.60§	—	9.4§	—	—	—	—	10.5/1300	0.5/400
0.032 copper rerun	110	784	15.0	16.2	1.58	2.11	10.5	13.0	3	46.9	—	10.4/110	8.6/784
0.025 copper	1296	612	10.0§	10.5	1.00§	1.16	10.0§	11.0	3.8	75.2	$\bar{X}$-32.4% nor.	6.0/1296	2.6/612
0.025 copper rerun	106	793	9.9	10.0	0.81	0.84	8.2	8.4	3	29.7	—	8.4/106	7.0/793
0.017 Kovar	1315	800	16.9§	17.8	1.80§	1.83	10.7§	10.3	3	37.6	—	10.0/1315	11.1/800
0.020 dumet (R)	1380	800	16.5§	15.4	1.95§	1.29	11.8§	8.4	3	45.5	$\bar{X}$-24% nor.	8.0/1380	8.4/800
0.020 dumet (G)	1304	800	16.0§	16.2	1.90§	1.80	11.8§	11.1	3	45.7	—	8.5/1304	8.8/800

* Comparison of statistics is given for general interpretation and interest but is subject to gross errors if consideration is not given to equalize sample sizes, distribution shapes, etc.

† Distribution-free statistics is the recommended basis for comparison and reliability estimation. Entries in the % column are the distribution-free estimates computed as a percent decrease from $\bar{X}$. See text for further explanation.

‡ Minimum strength comparisons must include the sample size effects.

§ Pull strengths were recorded to the next lowest $\frac{1}{2}$ lb. See text on weld joint tests prior to thermal shock.

For the samples for which a good fit (0.10 significance level) could be found distribution-dependent estimates of the percentiles are also given based on the distribution of the estimators of the population parameters. These statistics may be contrasted with the distribution-free results. In cases of disagreement between the estimates more weight should be given to the distribution-free estimates.

Table III provides a summary of the thermal shock test results together with prior sample testing performed to determine weld schedule acceptance.

Weld pull strengths were recorded by the serial number of the weld. Five different mechanisms of failure are recorded and are labeled 1A, 1B, 2A, 2B, and 3 on the histograms (see "Results by Material" below). "1" refers to a breakaway from the heat-affected zone, "2" refers to a break in the heat-affected zone, and "3" refers to a weld break. A and B refer to a failure in the material and in the nickel ribbon, respectively.

A distribution-free result for 0.020 nickel is that at a 90% confidence level not more than 7.7 out of 1000 welds will have pull strength less than 15.6 lb or $\bar{X} - 22.4\%$. Figure 8 is the histogram of the pull strengths of welds.

It was expected that 0.025 copper would be more critical than 0.020 nickel. Therefore, a larger sample size (612) was chosen. However, the results after thermal cycling were not as expected. The expected minimum strength was 6 to 7 lb and the actual minimum was 2.6 lb with three weld strengths below 6.1 lb. This low minimum strength was attributable to weld positioning control. A rerun on this material was made with better results.

Available distribution-free estimates at a 90% confidence level are that not more than 3.8 out of 1000 welds will have pull strength less than 2.6 lb or $\bar{X} - 75.2\%$ and not more than 10.8 out of 1000 welds will have pull strength less than 6.1 or $\bar{X} - 41.9\%$. Figure 9 for 0.025 copper shows the histogram of the weld pull strength data.

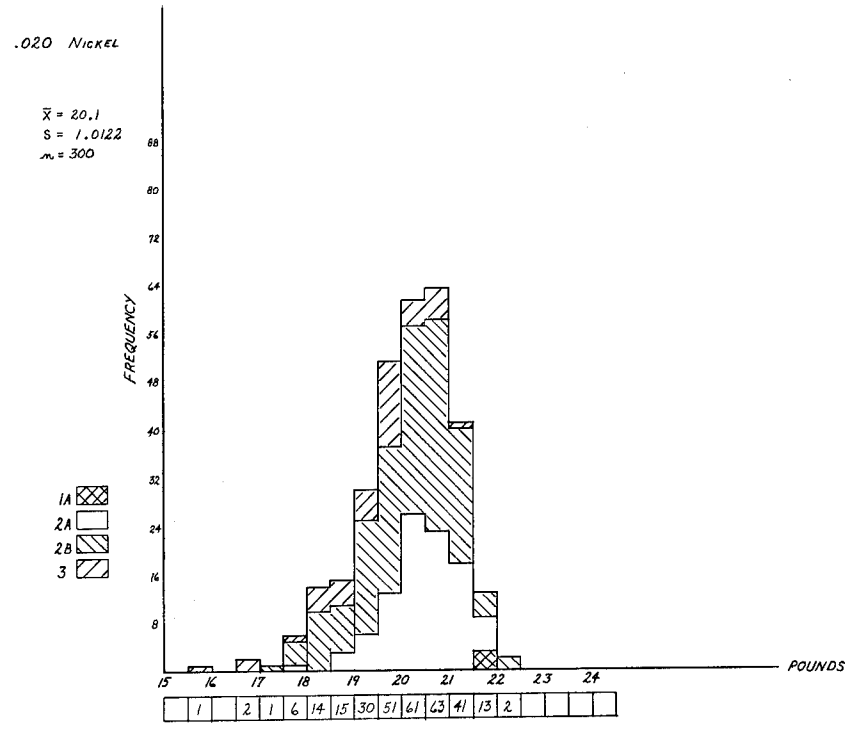


Fig. 8. Histogram of weld pull strength for 0.020 nickel.

The distribution-free results for Kovar are at a 90% confidence level not more than 2.9 out of 1000 welds will have pull strength less than 11.1 lb or $\bar{X} - 37.6\%$ and not more than 4.9 out of 1000 welds will have pull strength less than 12.0 lb or $\bar{X} - 32.6\%$. Figure 10 is the histogram of weld pull strengths.

Figure 11 is the histogram of the weld pull strengths for dumet (Raytheon). The distribution-free results are that, at a 90% confidence level, not more than 2.9 out of 1000 welds will have pull strength less than 8.4 lb or $\bar{X} - 45.5\%$.

Figure 12 is the histogram of 0.020 dumet (Glenco) weld pull strengths. The distribution free results are that, at a 90% confidence level, not more than 2.9 out of 1000 welds will have pull strength less than 8.8 lb or $\bar{X} - 45.7\%$ and not more than 4.9 out of 1000 welds will have pull strength less than 9.9 lb or $\bar{X} - 38.9\%$.

Twenty-two out of four hundred 0.032 Cu welds had pull strength less than 9 lb with 12 of the 22 being below 5 lb. The low-strength welds did not occur in any obvious pattern. Metallurgical analysis showed that the nickel ribbon was overheated on all the low-strength welds. Operator positioning error was suspected since welding in strings (Fig. 13) requires positioning in two dimensions, while previous weld samples had been made in a jig, which required positioning in only one dimension (Fig. 14).

Welding in strings was employed in order to facilitate resistance measurements, but it is not ordinarily practiced in making weld samples. An attempt was made to repeat the results prior to thermal shock, given in Table II (Weld Schedule Proofing) without success, until the samples were made as shown in Fig.14; then the results were nearly identical. It was desired by General Dynamics/Pomona to repeat the thermal shock tests on the two copper materials, 0.025 and 0.032, in order to determine, conclusively, the acceptability of these materials.

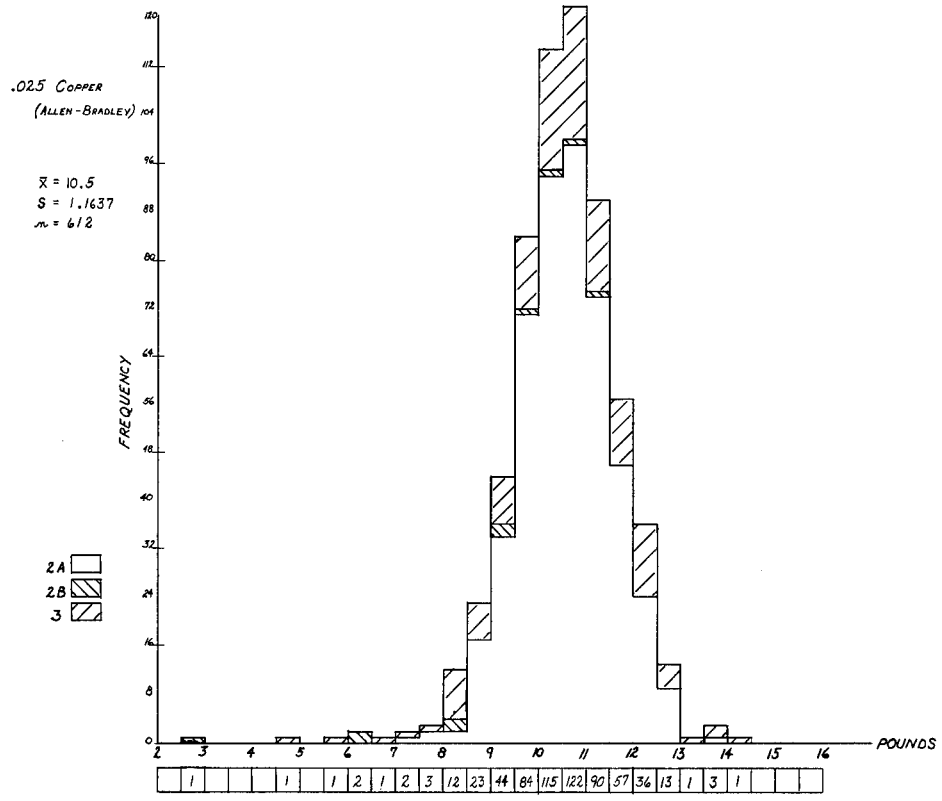


Fig. 9. Histogram of weld pull strength for 0.025 copper.

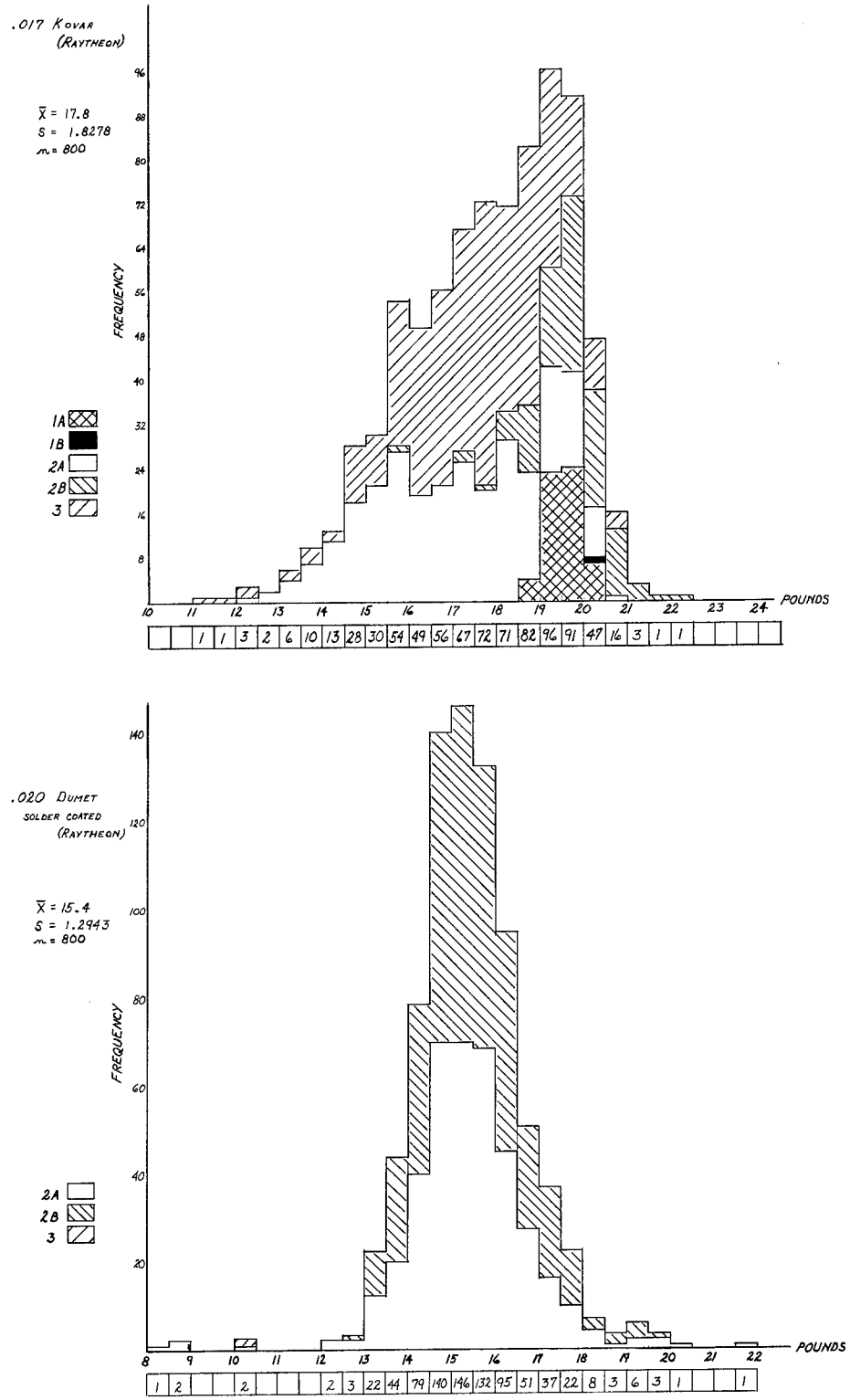


Fig. 11. Histogram for dumet (Raytheon).

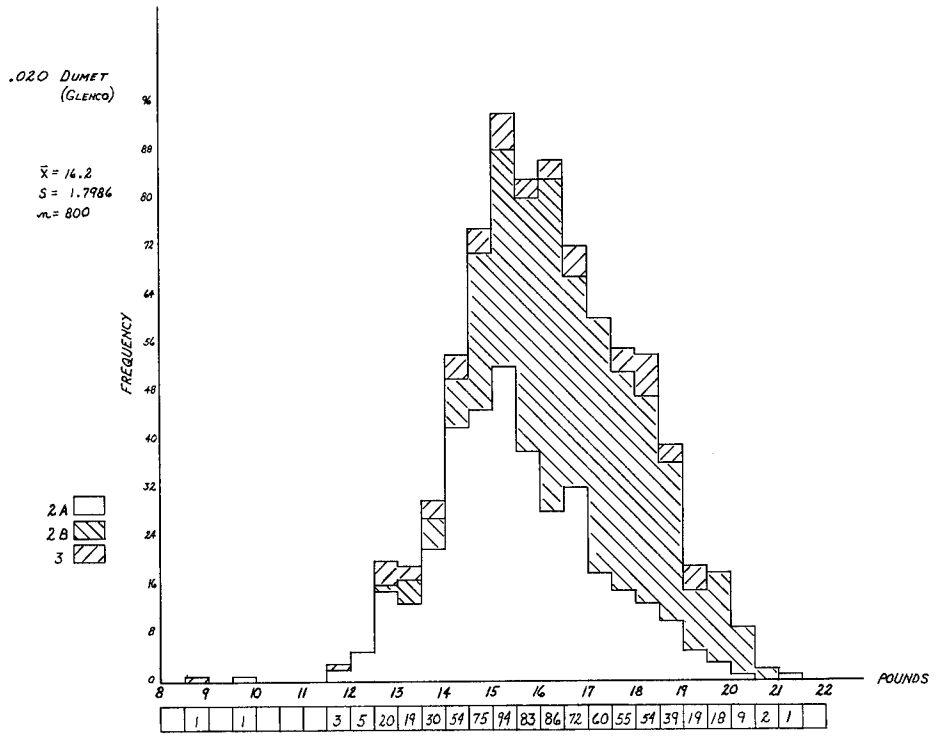


Fig. 12. Histogram for dumet (Glenco).

The retesting of 0.032 and 0.025 copper gave improved results over the tests where positioning control was not exercised.

Figure 15 is the histogram of the weld pull strength of 0.032 copper (Corning Glass). The distribution-free result is at a 90% confidence level not more than 3 out of 1000 welds will have pull strength less than 8.6 lb or $\bar{X} - 46.9\%$.

Figure 16 is the histogram of the weld pull strengths of 0.025 copper (Allen & Bradley). The distribution-free result is at a 90% confidence level not more than 3 out of 1000 welds will have pull strength less than 7.0 lb or $\bar{X} - 29.7\%$.

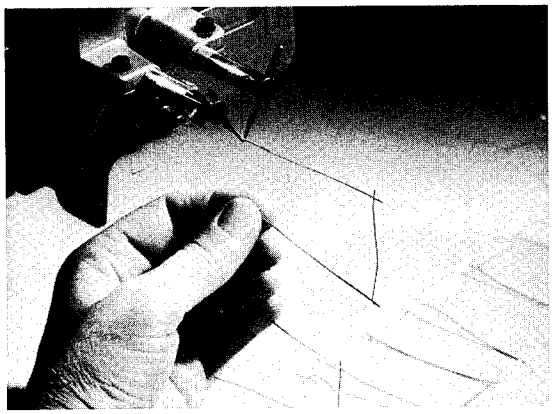


Fig. 13. Lattice for thermal cycling.

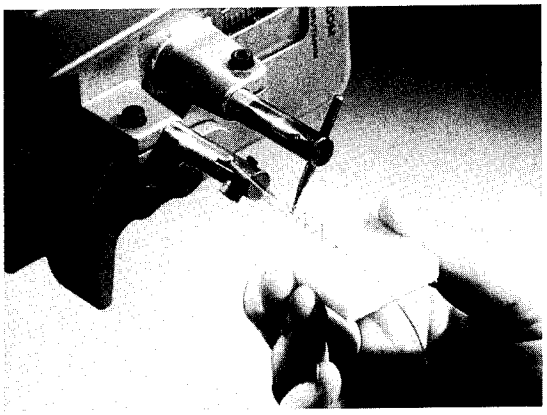


Fig. 14. Welds for weld schedule.

Specification SCL-7641 pull strength requirements were for thermally exposed samples and specific comparisons of means before and after exposure were not required. The results of the thermal shock test on the seven materials showed that this effect should be measured because of an apparent increase in mean strength for most materials. The rerun tests on copper detailed herein were planned to include a test of shift in the mean. Nine hundred samples of each material weld combination were made and approximately 100 samples of each were randomly selected from both groups and were withheld from thermal shock for control. Additional samples were retained for possible metallurgical sectioning and analysis.

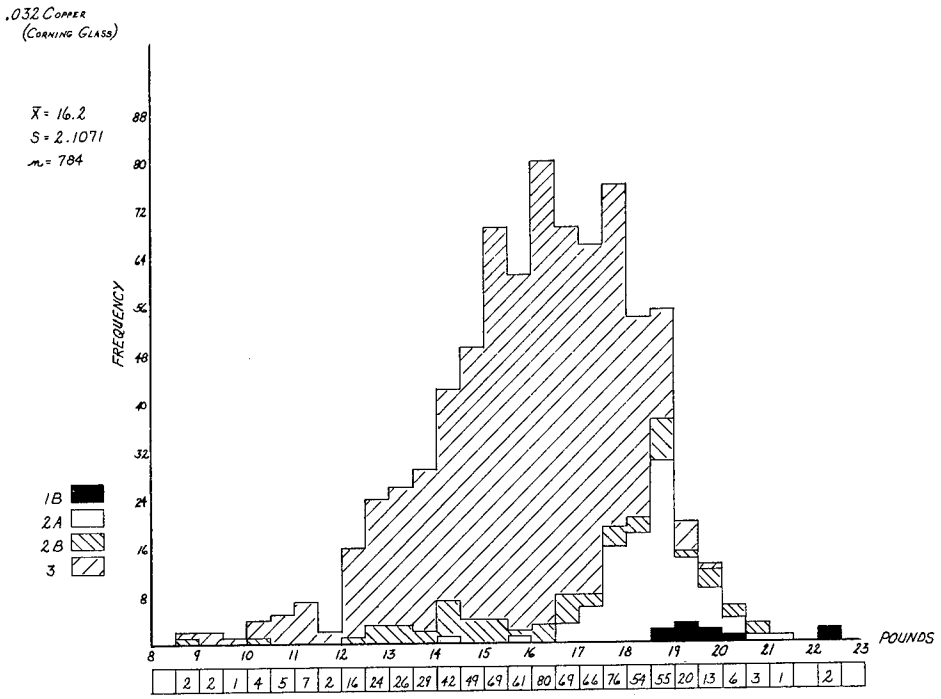


Fig. 15. Histogram of weld pull strength for 0.032 copper (Corning Glass).

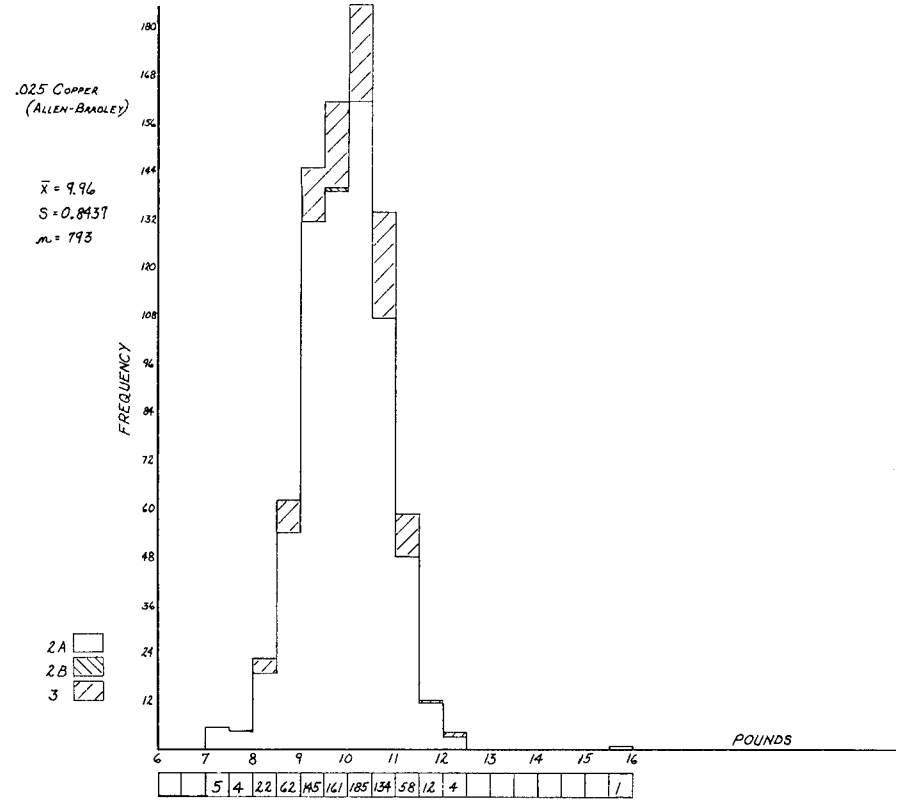


Fig. 16. Histogram of weld pull strength for 0.025 copper (Allen & Bradley).

For 0.025 copper, no significant difference in the means was detected. The hypothesis that the means were equal was not rejected at the 0.10 level of significance. For 0.032 copper, an apparent significant increase in the mean after thermal shock was detected $\bar{X} = 15.0$ lb increased to $\bar{X} = 16.2$ lb. The hypothesis that the means were equal was rejected at the 0.10 level as well as lower (0.01) significance levels. This increase in the mean was not expected, and when the result was detected, all of the data sources were reviewed to assure the accuracy of the change. Further testing of the detected increase in sample pull strength is necessary to ascertain the physical basis.

WELD STATION STATISTICAL CONTROL

Application of the pull test results should be made to production processes in order to maintain the desired reliability. The distribution-free statistic is most useful in establishing a weld schedule and in making comparisons with strength requirements in a module. A study was made to determine the best method to effect continuous control of the production process. Occasionally the process should undergo a check comparison with prior distribution-free results. In addition, a simple and accurate control utilizing data directly from periodic checks will afford an immediate indication of loss of control. Pull strength data was analyzed with regard to process control, but was not extensive because the scope of the contract did not include more analyses. However, in view of the fact that statistical control is necessary for predictions, and considering that some correlation between adjacent (with respect to time) welds is physically feasible, it was desirable to analyze at least one material in some detail. The material chosen was 0.020 solder-coated dumet (sample size of 800). Figure 17 shows the

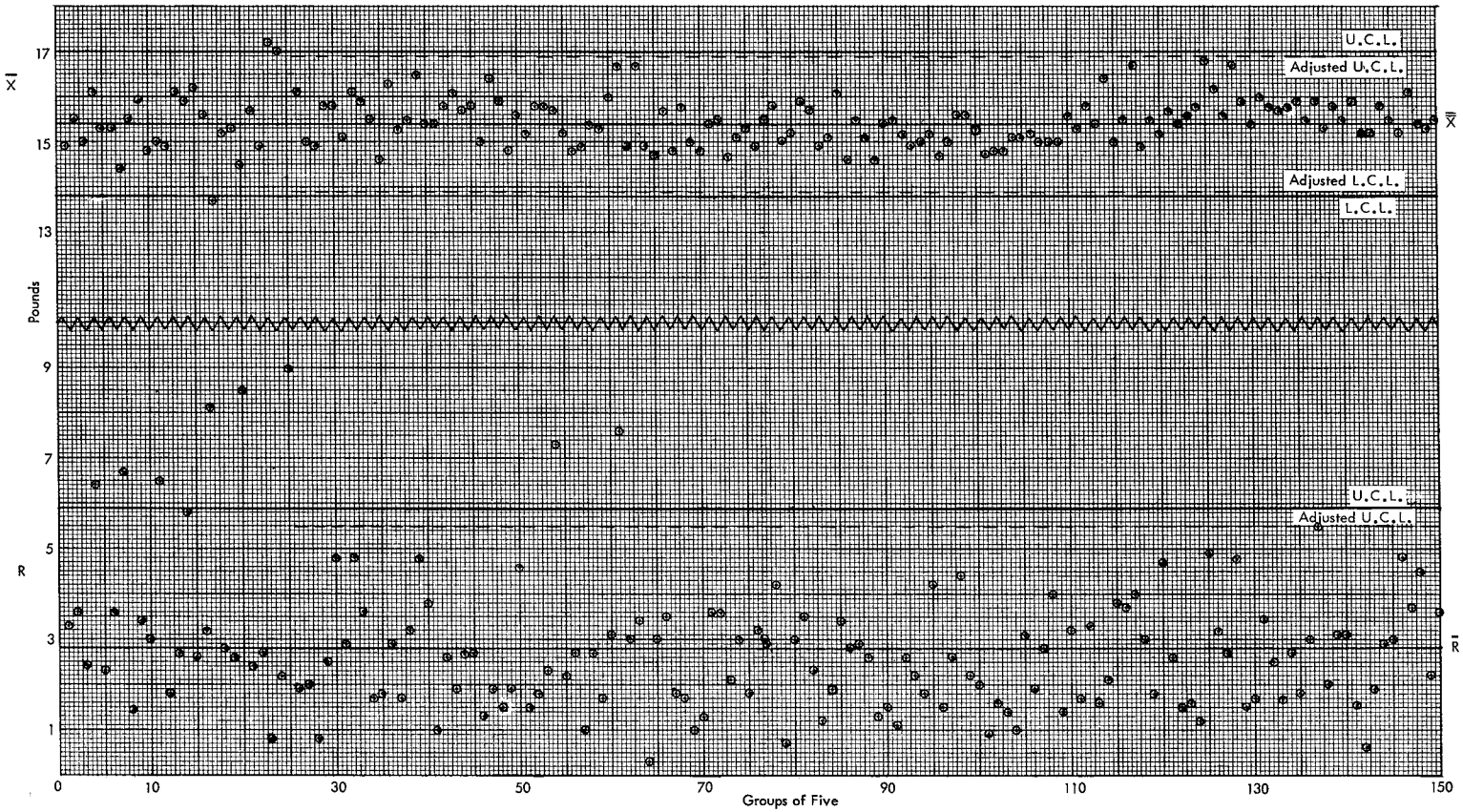


Fig. 17. $\bar{X}$, R control chart for 0.020 solder-coated dumet welds.

plot of ranges of groups of five weld pull strengths from 1 to 150 (the last 10 groups were discarded for plotting convenience) and the plot of average pull strength of each group of five from 1 to 150.

Two tests for randomness were made (p. 169 ff [2]). One test was for runs of $\bar{X}$ above and below the median. The chi-square value was not significant for this test at the 0.10 level. The other test on the $\bar{X}$'s was for runs of first differences of like signs. The chi-square value for this test was also not significant at the 0.10 level. The control chart (Fig. 17) supports this evidence if the first 25 points are eliminated and new control limits calculated. This is an indication that the process may have been out of control in the early stages and then "settled" down. This method of statistical process control should be employed for effective use of the four-hour checks. No extra work is required to employ this method which will visually indicate out of control conditions when they occur. With the addition of minimum strength to the other parameters, $\bar{X}$, R, the control chart will give a continuous display of the weld strength parameters and their drifts.

THE BETWEEN OPERATORS EFFECT

The variability which can be introduced into the weld reliability by an operator is considerable and must be limited by effective training and the employment of appropriate aids. As was previously seen in a positioning problem where 0.032 and 0.025 copper weld strengths were affected by malpositioning, it is imperative that these type characteristics be defined and controlled. When the operator choices are limited and constant, there remains a factor which is called "between operator effects" and which must be considered in the weld variability analysis.

The between operators effect was checked on one material (0.032 copper) for a sample of 100 for each of two operators. The sample means for each operator were 16.8 lb and 17.5 lb. The hypothesis that the true difference in the population means was zero, was not rejected at the 0.10 significance level.

VIBRATION TESTS

Three test modules containing two welds of each of seven weld designs were vibrated in three mutually perpendicular planes. Sweep frequencies from 55 to 3000 cps were applied at 30 g continuously for 8 hr in each plane at 10 min per sweep. The weld joints were monitored with an oscilloscope so that joint-generated noise could be detected. A series current of 1 A was maintained through all joints continuously. The tests showed no evidence of noise or of weld joint failure at any time during or after the tests.

CONCLUSIONS

1. Minimum strength as a function of sample size is concluded to be the most accurate measure of weld strength acceptability. This statistic would make a simple and accurate basis for grading the weldability of material combinations and in evaluation of data for weld schedule development.

2. Distribution-free tests accurately estimate the strength properties of welds, are easily obtained, and are free from serious errors. The low cost for large sample sizes permits the desired confidence range. Distribution-dependent methods are accurate only if the assumed distribution is the true distribution. Very slight differences in the distribution may produce serious errors in the estimates.

3. There is no correlation between weld joint resistance and weld pull strength. The values of weld joint resistances in microhms* were: (−)13 to (−)73 for Kovar, (−)30 to (+)76 for dumet, (−)7 to (−)46 for nickel, (+)2.2 to (+)30 for copper. An estimate of the maximum range expected for any of the materials was not made because of the instrumentation long-term drift detected.

* Joint resistance includes all contributing phenomena.

4. The bias in results obtained by pulling welds on the Hunter Spring tester is a linear function of pull rate on the range tested. There is no disadvantage of using a 60-in./min rate, but intermixing data obtained at different rates is inaccurate. The maximum average difference measured between 1 in./min and 60 in./min was 6.6%. No significant difference was observed in the variability at any rate measured.

5. The thermal shock test was not specifically designed to evaluate changes in pull strength due to thermal shock; however, gross changes in before and after results would have been detected. No gross changes were, in fact, detected that could not be assigned to other causes. A special test on 0.025 copper and 0.032 copper welded to 0.012 × 0.030 nickel ribbon was designed to detect changes in pull strength due to thermal shock; in these two cases no detrimental change was detected.

6. Operator effects have a profound bearing upon the welded module reliability. Proper training and applied constraints on operator decisions are needed to minimize the latitude of these effects. Checks were made on "between operator" effects when adequate training and proper welding controls were exercised. These "between operator" effects were *not* significant for the test prescribed using two operators and one material combination.

7. General application of lead materials studied will result in satisfactory reliability of weld joints. The bus and lead sizes are directly related to the weld strength results and generalization of material alone is not possible. 0.020 nickel wire, 0.017 Kovar wire, 0.020 dumet wire, 0.025 copper wire, 0.032 copper wire, and 0.012 × 0.030 bus material were tested and are acceptable.

8. Vibration testing has not revealed any susceptibility of the welded joints to failure at 30 *g*. It is thought that considerably higher *g* levels are necessary to generate vibration failures.

ACKNOWLEDGMENTS

The author is indebted particularly to the following individuals for their contributions to this Applied Research Program: V. G. Bateman, Senior Design Engineer; R. J. Conti, Research Engineer; F. C. Fichter, Senior Development Engineer; A. E. Flanders, Design Specialist; D. R. Oldaker, Senior Design Engineer; L. G. Settle, Research Engineer; and W. V. Lane of the United States Army Electronic Research and Development Laboratory.

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Handbook of 3-D Welded Module Design and Manufacturing Control Parameters*

DESIGN, PROCESS, AND PARAMETER CONTROLS

THE SUCCESSFUL manufacture of high-reliability welded modules is achieved only through the introduction and continued maintenance of rigid process controls. These controls must be maintained throughout all phases of module design and manufacture. Special emphasis should be placed on the factors influencing product quality and reliability in the production areas. However, some of these factors are associated with engineering investigation and design.

The level of importance of each of the different phases of engineering and manufacturing that influence product quality and yield are described in the following pages together with appropriate methods of exercising the necessary controls. The major headings are as follows:

Engineering
Parts Selection
Manufacturing Aids
Lead Control
Weld Schedule Development
Part Handling
Manufacturing Environment
Qualification of Manufacturing Equipment
Process Controls
Quality Control 7

The level of importance of each of the influencing factors is described by a weighting of 125 points for the most important downward. A listing of paragraphs in declining order is given in the index. Each subject includes a weighting factor in a 1 to 5 ranking in order of importance. The weight ranking is applied at each level of indenture so that the final paragraph weighting is the product of the three levels. The highest number being 125 (5 × 5 × 5) which represents the highest degree of importance.

Each area of responsibility in the manufacture of welded modules is indicated by reference to a number which corresponds to the block diagram of a typical factory.

A diagram (Fig. 0–1) is provided to assist in applying the principles detailed in this handbook. Accordingly the weighting index also includes the related blocks of the typical factory for each subject discussed.

Section 1.0

ENGINEERING

Product quality yield is measured by the type and quantity of controls applied to each phase of design and manufacture. Factors influencing this yield are extremely important particularly in the early stages of product design. These factors and their methods of control must be recognized to produce a product of high quality and high reliability.

1.1 System Design

The volume and weight goals of a system are usually initially determined in the design proposals. When these limitations are known, the designers should begin preliminary layouts to establish physical configuration of the overall system. These layouts will include the module shape and size, interconnecting harness type and location, and mechanical connecting and attaching methods. Several considerations must be included, each almost simultaneously, to achieve unity and compatibility with each part to the overall assembly. The more important factors are discussed in the following section on engineering.

* The design and process requirements presented herein are being processed for publication by USAELCTROLAB and will be published as Signal Corps requirement SCL-7741, titled "Design, Process and Parameter Control Requirements for 3-D Welded Cordwood Modules." This work was in cooperation with other programs at General Dynamics/Pomona and reflects a total coverage of the subject as developed over a five year period. Changes to this document which are appropriate as determined by USAERDL will be distributed periodically.

1.1.1 Standard Size. Optimum *system* volume utilization can be achieved by modular standardization in shape and size. This feature may reduce some volume efficiency at the *module* level, however, the small loss is justifiable to achieve overall consistency, uniformity and ease of assembly.

1.1.2 Interconnection Design. The interconnection method should be developed as early in the system design as possible. Each system configuration will dictate the type of interconnections most suited to the design requirements. Early development of the interconnection design may simplify later rearrangements due to unforeseen electrical and mechanical changes. In most cases, several methods are adequate and only close examination of the overall design will determine which type is most desirable.

1.1.2.1 Bundled cable interconnections are generally not recommended as most systems are designed for compactness and available space is at a minimum. Planar type harnesses are preferred and by causing less space to be used for the interconnections, additional room is provided for electronic part packaging. Welded interconnections may be incorporated in planar harnesses which will afford a higher reliability with a minimum of space consumption. Module and assembly groupings should be arranged to minimize the number of connections for ease of assembly and maintenance.

Planar harnessing is generally of several types, some of which are listed as follows.

1.1.2.1.1 Flat bonded cable—insulated wires individually bonded side by side in a flat parallel manner.

1.1.2.1.2 Printed wiring—a plastic board having specific conductor paths arranged in a general parallel manner by means of etching or depositing.

1.1.2.1.3 Cast matrix—a cross wire configuration separated by insulators providing high interconnection flexibility by permitting multiple point attachment locations. These matrices may also be separated by insulators to permit additional layers of interconnections. Subsequent casting of this multiple level matrix will provide a sealed, rigid and structurally sound interconnecting means.

1.1.2.1.4 Flexible cable—a series of mutually parallel conductors laminated between two flexible sheets of plastic material.

1.1.2.1.5 UXL (Universal Transmission Line, a Proprietary General Dynamics/Pomona Development)—The universal transmission line distribution system is a separable, rejoinable interconnection harness of welded nickel ribbon. The UXL interconnection method utilizes flat, ribbon-shaped conductors which are attached to flat, nearly flush terminals on the face of an encapsulated electronic module. Electrical tests of characteristic impedance and the various shielding parameters for balanced and unbalanced modes show the UXL is usable over the entire spectrum out to microwave frequencies.

UXL harnessing is achieved by an attachment technique called "surface welding." This process allows for nondestructive repairability at the module level. Rewelding may be accomplished many times at a given terminal while maintaining a high degree of reliability. Resistance welding parameters have been developed which allow for the same weld schedule on rewelds as on the original weld. The miniature UXL is established on 0.100 in. centers. A recently developed subminiature version is arranged on 0.050 in. centers, and a microminiature size on 0.025 in. centers.

1.1.3 Encapsulating Materials. Numerous plastic materials are available which are suitable for module encapsulation. The nature of the circuit has an effect in determining the appropriate compound. High-frequency and high-gain analog circuits usually require a light, low-dielectric-constant encapsulant. The selection of encapsulants used in modular assemblies must meet the electrical requirements and maintain structural integrity. The material properties of the encapsulant should be considered very carefully to avoid detrimental mechanical effects during fabrication. Attention should be given to exothermic reaction during the curing cycles as well as curing time and temperature and variations of properties attributed to exposure to temperature, humidity, moisture, shock, and vibration. The significant physical properties such as mechanical strengths, expansion coefficients, shrink factors, density, and thermal conductivity of each encapsulant being reviewed should be thoroughly examined by the designer prior to acceptance. Such examinations should result in an encapsulant that will not cause harmful stresses on the components, the weld joints, or the module terminations.

1.1.4 Mounting Methods. To a large degree, the size, shape, application (ground, sea, air, space), and maintenance philosophy of any given system will determine the method of mounting the modules. Generally, the methods of module mounting are bonding, strapping, or threaded fasteners. Where moderate shock, vibration, and thermal environments exist, and small light modules are used, a suitable plastic bonding agent is recommended, such as a pressure-sensitive or thermosetting material. Room temperature cured resins may be incorporated when employing "eggcrate" or "honeycomb" type structures. These latter configurations will necessitate multiple mounting surfaces to provide sufficient contact area.

1.1.4.1 Strapping may be used in modules of moderate size (see Fig. 1-1), where space is at a relative premium and where rigid resins can be used. This method will permit back-to-back mounting of several modules on a common chassis. Also, a frictional damping feature is incorporated by using a strapping technique which will reduce effects of more severe mechanical stresses.

1.1.4.2 Threaded fasteners are recommended for exposure where extreme mechanical stresses are to be encountered and where ease of assembly for serviceability is desired. Certain system requirements imposed may require mounting several modules to one common printed wiring distribution board and subsequently connected electrically and mechanically by soldering the module header leads to the etched conductors. This method is one where ease of assembly and serviceability is desired.

1.1.5 Functional Breakdown. System design parameters are determined after reviewing the customer requirements and completing preliminary breadboards and testing. The system functions are defined and should be broken down into assemblies, e.g., power supply, receiver, autopilot, computer, video. These electrical functional divisions will facilitate converting the system block diagram and design requirements into categorized electronic circuitry. Proper functional divisions will indicate all interconnections and, in

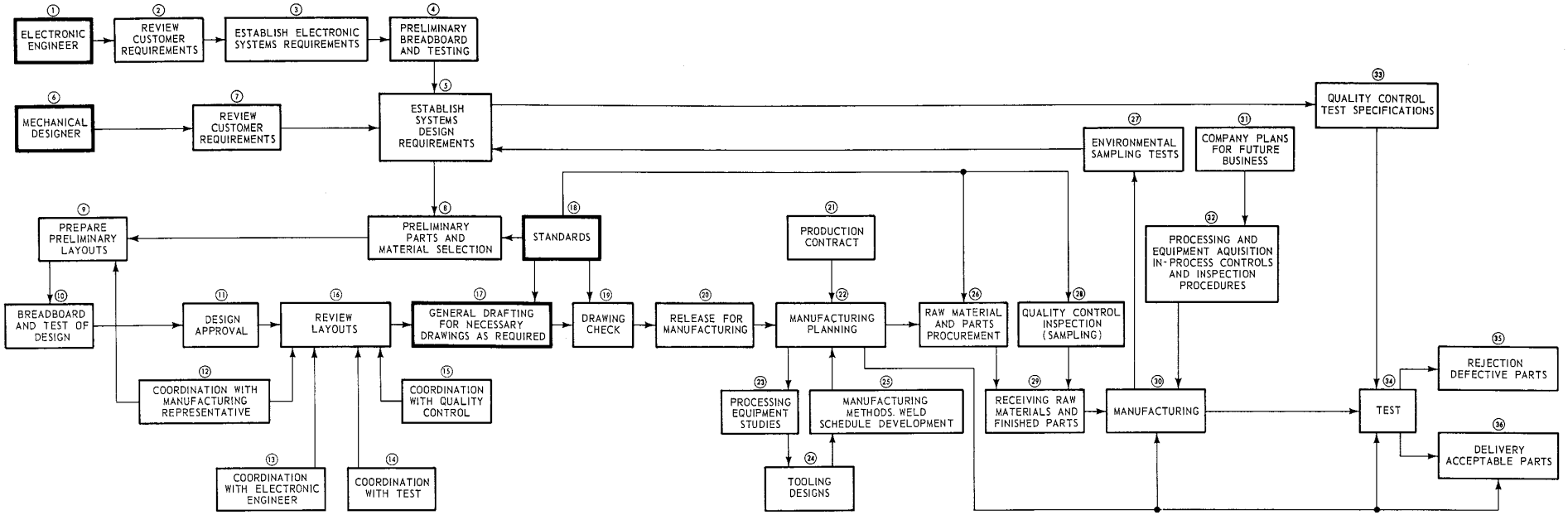


Fig. 0.1. Engineering and manufacturing flow diagram for 3-D welded module electronics.

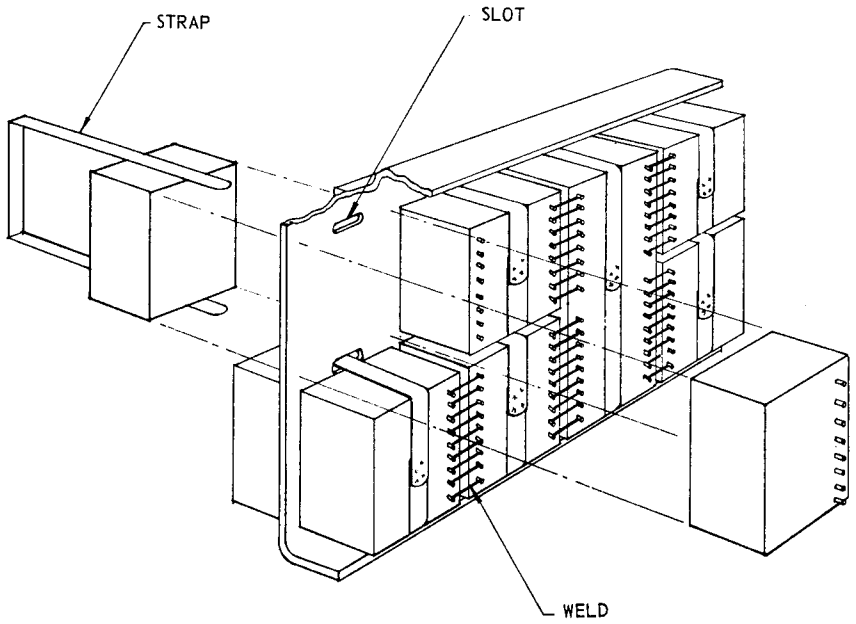


Fig. 1-1. Welded module electronics.

some cases, the module terminations which may or may not necessitate rearrangement to define the most suitable method. Optimizing the system functional breakdown early in the design will ease complexity at the harness level and permit a simple interconnection design. Attention to functional divisions and placement of module groupings will provide the most optimum interconnection method and afford minimum space for efficient serviceability and yield a higher reliability.

1.2 Electrical Design

Although electrical performance is the controlling criterion, the electrical design and the mechanical design should be a combined effort. A successful electrical design will depend on how well acquainted the electrical engineers are with modular design. With this concept in mind, the overall task will progress more efficiently with less cross liaison and fewer compromises necessary to satisfy the design in all areas. The electrical designer should study the following considerations.

1.2.1 Suitable Breakpoints. The modular division of the schematic is one of the most important steps in 3-D module design. Optimum points of division may be determined by careful consideration of the electrical requirements and system space limitations. To establish the design of the modules within the limits of the system, the designer should adhere to the following requirements:

1.2.1.1 The circuit should be broken at points of low voltage and low impedance. Impedance should be compatible with frequency. Radiation increases as frequency increases. Feedback due to stray capacity is undesirable in that circuit performance at high impedance levels depends critically on the properties of encapsulating materials. The circuit sensitivity to pick up due to this stray capacity can be effectively reduced by reducing input impedance as frequency is increased. To maintain acceptable levels of unwanted feedback voltages the impedance should decrease as the frequency is increased.

1.2.1.2 Maintain a minimum number of connections to individual modules.

1.2.1.3 Divide circuit at points which offer minimum feedback.

1.2.1.4 Avoid, if possible, areas which cause interelement coupling due to proximity effects.

1.2.1.5 Keep the throw-away cost of each module to a minimum without jeopardizing the electrical performance when establishing the number of components per module.

Generally the above conditions can be met. However, if they do not yield an optimum design, certain areas may be examined to provide a more suitable result. These areas include: Selection of alternate components carefully considering ratings and cost; special parts should be kept to a minimum; review the design for a different or modified circuit; examine the possibility of an alternate structure and method of module mounting; consider a different approach to the system functional requirements; request possible increase in volume allocation.

System breakdown is usually defined in the preliminary stages of design. Neither the electrical or packaging designer should have the prerogative to alter or change any system functional division. However, alternate modular divisions of the system subassemblies is quite within reason.

1.2.2 Proximity Effects. Volume reductions in electronic packaging brought about by the 3-D method has created problem areas peculiar to the modular technique. Self-oscillations and unusual electrical performances have appeared due to the radio frequency voltages in high-frequency and high-gain circuits. The proximity relationship of the input stages to the output stages sometimes causes appreciable resistive and capacitive feedback and the phase-gain stability criterion is exceeded. This is more prevalent in the 3-D technique due to the reduction in package sizes. Techniques which will aid the designer in solving difficult problems in smaller packages where the performance is near instability are available from several concerns. One such reference is available from General Dynamics/Pomona.

1.2.3 Power Dissipation. Consideration of the DC voltages applied to modular design should be accomplished so as to prevent unnecessary heat conditions due to additional voltage dividers.

The operation of certain modules may require heat dissipation simultaneous with heat insulation and therefore impose heat transfer problems. Thermal characteristics should be considered during the electrical design stages to permit a uniform treatment of power dissipation throughout the assembly. Care should also be exercised to avoid hot spots.

1.2.4 Minimum Connections. To achieve the optimum in reliability, all connections should be kept to an absolute minimum. An electronic system is no better than the weakest element within it. To ultimately effect this high reliability, available low failure rate components must be utilized. The interconnections should have failure rates that are negligible with respect to the best components. With all connections, each component will typically average three connecting points, two for the axial components and one extra for averaging the system interconnections and multileaded parts. This relationship indicates the necessity for high-reliability connections. Two methods of maintaining the level of high reliability is in the quality of the connection and the number of connections. Minimizing the number of connections will afford a more simple routing plan, and reducing the number of crossovers at the module termination level assures that all electrical connections are made in a simple compatible mechanical arrangement.

1.2.5 Trimming and Adjustments. The number of adjustable components in a system may be reduced by careful circuit design applications. All adjustable components must be accessible at the module surface; therefore, restrictions are placed on the component placement within the module. This is particularly true where more than one adjustable part is required. The circuit designer should consider the application of these component types very carefully by providing adjustments in areas of final system trimming and not for a substitute of choosing proper electrical values. Adjustment mechanisms should be sealed at the system level and *only* after the system has been assembled, tested, and adjusted.

Wherever possible, fixed component tailoring should be used. This procedure will eliminate the need for sealing of component adjustments as all attachment provisions are on the external surfaces of the module. The component attachments would have been previously sealed internally (in the module) prior to encapsulation, preventing any external moisture penetration or encapsulant leakage.

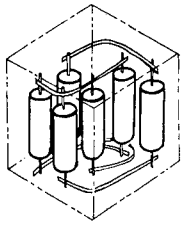
Unlike adjustable components, fixed-value tailoring is more reliable and accurate in that more precise values can be selected to compensate for circuit performance variations.

1.3 Mechanical Design

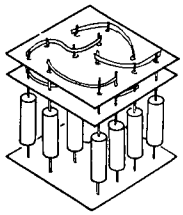
The most important phase of design is the conversion of an electrical circuit to a physical package. The designer must be aware of the mechanical and electrical requirements. This knowledge can greatly affect the reliability of the design. "Trade-offs" are necessary where the factors must be known and applied to achieve overall optimization, since an ideal condition in one area can reduce performance and efficiency in another. Ultimately, the aim is to produce a product incorporating the best combination of electrical and mechanical features. Individual areas which can affect the overall reliability are detailed in the following paragraphs.

1.3.1 Intraconnections. The placement of the components within the module must be done in a manner making the intraconnections as simple and as short as possible. There are several types of intraconnection techniques. The most common are as follows.

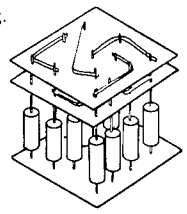
1.3.1.1 Point-to-point, no component positioners or wafers.



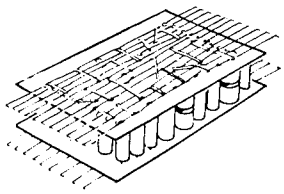
1.3.1.2 Point-to-point, single or double positioners with curvilinear bus routing.



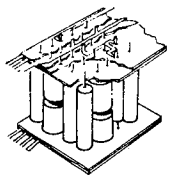
1.3.1.3 Point-to-point, single or double positioners with angular bus routing.



1.3.1.4 Wiring matrix with parts perpendicular and inaccessible.



1.3.1.5 Premanufactured positioners with a random intraconnection pattern.



1.3.2 Each technique has certain advantages and disadvantages which eliminate the possibility of any one type serving all electrical and mechanical requirements optimally. Arranging the components in "cordwood" fashion with no positioners does not provide a mechanical means of maintaining positive component location. Positioning the parts for the welding operation is difficult in that the parts as well as the intraconnecting medium must be hand-held. It does, however, lend itself to ease of any necessary repair as the components are fully accessible by the absence of a restrictive component positioner or end wafer. By incorporating essentially the same technique, but with the addition of a component positioner at each end, retention of the components is achieved. This eases the welding operation by eliminating hand-holding the components. One disadvantage in using a positioner is that the components are inaccessible, which restricts repair. The bus wiring for the point-to-point methods can be either curvilinear or angular. In either case the bus routing and connections must be made without crossovers at any one level. Curvilinear routing provides a direct point-to-point connection and can be used where density of components permit. Generally, curvilinear routing should be avoided in favor of straight runs with angular bends near the component lead. A straight section of bus should extend beyond the component lead in both directions to prevent any accidental shunting of the welder electrodes against the intraconnecting bus.

1.3.3. A wiring matrix having maximum electrical intraconnection flexibility may be used for high-density bus routing where end plates are included. This application necessitates carefully controlled conductor spacing with a minimum amount of lead location tolerances. As in the point-to-point method with positioners, the components are inaccessible for replacement or repair.

1.3.4. A premanufactured intraconnection board with random distributed conductors is most suited for high-rate production manufacturing. Trade-offs such as cost *vs.* density *vs.* quantity must be determined prior to using this method of intraconnection. Achieving high wiring densities is not possible due to the area required to bend up welding tabs. Conductor thicknesses are restrictive and in certain circuit applications may prove inadequate.

1.3.5 Module Shape. The system space allocation for the electronics will indicate the size and shape limitations for application of modular techniques. In most cases, a system will describe the module geometric configuration peculiar to the system individual characteristics. Although it could be highly desirable it is uncommon to standardize module size-shape that can be used in more than one system.

The following considerations are important in determining the module configuration for a given system:

1. Throw-away cost
2. Appropriate circuit division points
3. Module size relation to configuration of overall system package
4. Component size

The module geometry should be standardized in a *given* system to avoid a collection of odd-shaped modules which would be difficult to package efficiently into a compact volume.

1.3.6 Thermal Flow. The temperature limits are dependent primarily upon temperature limits of the most sensitive components being used. Proper handling of internally generated heat and external ambient

temperatures will permit operation of a module at a temperature close to the critical levels of these most sensitive components. There is no universal method to optimize the thermal flow for a module since some require insulation from external ambient and others may require good heat flow for external heat dissipation. Data such as storage environment, warm-up time, mission time, mission environment, individual component temperature limits, and mission variations will aid the designer in effecting a design with good thermal flow.

1.3.7 Shielding. Shielding requirements generally fall within two areas: electrostatic and electromagnetic.

1.3.7.1 Electrostatic shielding is effected by using metallic separators within the module and/or metallic enclosures on the external surfaces. This may be accomplished by clad boards on the appropriate module surfaces, overcoating the module with conducting material using plated encapsulation cups or using drawn cans. Isolation of adjacent conductor paths is provided when necessary by interposing a grounded line between the conductors. This line or plane should be connected to ground potential at one end only to avoid loops and coupling actions. AC grounds are effective isolators and may be employed to reduce the number of ground conductors.

1.3.7.2. Electromagnetic shielding is best achieved at the component level. Shell- or toroidal-type magnetic components should be used to avoid flux leakage and undesirable component performance due to influence of external fields. In some cases continuous metallic enclosures should be used to avoid coupling of air core magnetic components and all openings for electrical connections should be as small as possible.

1.3.8 Welding Access. Proper clearances for welder electrodes must be provided to avoid electrode contact with adjacent interconnection buses or leads. This type of contact may result in high currents taking an alternate path through a component and cause serious damage. Excessive stresses due to this contact may weaken a previous weld causing possible weld failure.

To avoid possible weld damage and subsequent weld failure, minimum welder electrode clearances have been established based on the most common electrode configuration ($\frac{1}{16}$-in.-diameter electrode tip set in the welding head at a 70° included angle). The electrode diameter and included angle indicated is not meant to be the only configuration yielding good welding conditions. However, considering component size ranges and ribbon bus dimensions, the 70° included angle seems optimum and will provide longer electrode life by permitting more separation between interference projections of electrodes and electrode holder for the dressing operations.

The mechanical stresses on the electrodes increase as the included angle is decreased, therefore accidental contact in areas other than the electrode weld surfaces are increasingly probable as the included angle is reduced. A minimum clearance of 0.050 should be maintained between any weld and an adjacent ribbon or component lead for lead and bus sizes described in the Section under "Lead Materials" and "Lead Diameter."

1.3.9 Component Orientation. The components may be oriented parallel or perpendicular to the module termination surface. When orienting the components parallel to the termination surface they should be perpendicular to the termination rows so that the interconnecting bus and the termination rows are in the same plane. This provides good welding accessibility when attaching the terminations at the next level of assembly. When orienting the components perpendicular to the termination rows it may be necessary to use additional jumper wires, or feed-throughs, between the component positioners or end wafers.

1.4 Production Orientation in All Design Areas

Consideration for producibility must be included in all phases of design and engineering. The measure of any product design efficiency is determined by how easily it can be mass-produced. Understanding of the steps necessary to simplify design features which will eliminate costly and complicated manufacturing operations will be beneficial to all persons associated with the design. Including discussions with manufacturing personnel early in the design will add to simplicity of assembly and eliminate needless revisions and modifications. The designer should be aware of several factory methods and procedures, examples of which are detailed.

1.4.1 Knowledge of Factory Equipment. To assure the best possible results of any design scheme, it is essential that the design personnel have full knowledge of the equipment used in the production areas. This includes all equipment such as fabrication, process, assembly, and test equipment. Familiarity with the equipment functions may eliminate costly manufacturing processes prescribed in a particular design approach that is not within factory capabilities.

1.4.1.1 Generally, standard sheets are provided by manufacturing personnel for numerous machine operations and tools that are more commonly used. These data are (or should be) included in an appropriate section of a design manual in an effort to ease the remaking of a design by standardization groups. Typical examples are hole sizes and tolerances, punch sizes and shapes, desired machining, casting tolerances, and other machining operation.

1.4.2 Cost *vs.* Method *vs.* Quantity. Most designs contain enough flexibility to permit fabrication and assembly in several ways. However, the designer should exercise caution in determining the most advantageous assembly technique. Proper trade-offs of suitable factors should be done to eliminate any unnecessary sophistication in any particular area and to assure the designer that the method chosen is optimum from the standpoint of cost and reliability.

1.4.2.1 The length of the production run (or best estimates) plays an important part in the cost and manufacturing method of an electronic assembly. Initially the cost breakdown and design approach are at the discretion of the designer and regulated by him hopefully based on the total quantity to be manufactured. Careful attention must be given to indirect costs incurred in manufacturing such as tooling. For

example, it may be necessary to choose an alternate, and more expensive, fabrication technique if tooling costs become prohibitive in order to achieve a low unit cost.

1.4.2.2 The manufacturing groups should be responsible for changes in tooling and methods on all follow-up orders. Quantity variations, if wide enough, will alter some phases in the manufacturing procedures prescribed by previous production runs, amortization, and fabrication methods. Inclusion of discussions with production personnel should be encouraged in the early concepts of the design.

1.4.3 Knowledge of Factory Future Planning. Future planning of the factory production flow layout processing stages and equipment procurement will aid the designer in determining the best method of producing an assembly at a given production rate. Newer and more efficient means of manufacturing and processing are almost constantly being introduced throughout the industry. Competition necessitates continuous research into easier and better methods of producing various types of equipments. Activity of this nature is typical of any company. By keeping abreast of the future plans in the manufacturing organization the designer gains a knowledge of methods which can reduce costs by orienting the new design toward factory procurement thereby maintaining a compatibility with projected manufacturing plans.

1.4.4 Knowledge of Manufacturing Yield. Engineering should be kept informed of the status of production yield at periodic intervals. Problem areas may arise during manufacturing that were not conceived or made known in the design sequences. After a design is released for production, certain important items of manufacture may require alterations which could increase the production rate, provide higher reliability, and reduce costs.

1.4.4.1 In cases where some operations are rather complex, being sufficient to cause a high rejection rate, inspection should notify Engineering of the nature of the problem requesting design modifications or revised processing procedures.

1.4.5 Knowledge of Test Equipment Design and Procedures. Familiarity with the test equipment in the manufacturing areas will aid the designer in providing welded assemblies that are compatible with available check-out and testing facilities. Modules that are initially designed to facilitate testing will eliminate modifications required in later phases when test requirements become more evident. Specific provisions for test points and other electrical check areas should be allocated in a manner which will avoid additional fixturing and setups. The electrical engineer in choosing the type of tests necessary should not require elaborate and costly test equipment and setups. However, if a specific piece of equipment is necessary, the knowledge of this additional equipment, when ordered, should be made available to all persons in similar design areas. Ignorance of available test equipment can unnecessarily cause costly procurement which can be avoided.

Section 2.0

PARTS SELECTION

During the development of any system design, the influence of component cost and reliability should be investigated to assure optimum operational performance. Careful selection of parts is necessary to determine that the system will survive and operate over the specified period of time. Part reliability and cost are of prime concern to the 3-D module since a single bad (unacceptable) part will frequently cause an entire module to be discarded. On the other hand a pointless insistance on reliability at any cost for all parts is uneconomical. Therefore it is desirable to continuously monitor parts used for both reliability and cost, and make appropriate adjustments during the production lifetime of a design.

2.1. Compatibility with Welding Process

The nature of the 3-D welded module technique requires that all component leads have controls for welding. The designer should limit his choice of parts to qualified components only. Parts chosen for peculiar electrical or physical requirements should be qualified before being committed to production. The items listed below should be considered by the designer prior to choosing of a part for welded module application.

2.1.1 Lead Material. To ensure consistently reliable welds, it is necessary for the selected component to have a weldable lead material. Components with stranded wire leads should not be used since only a small percentage of the strands are involved in the weld resulting in low weld strength. Recommended lead materials with their property advantages are listed below in order of weldability compatible with a standard lead joining medium such as 0.012 × 0.030 nickel ribbon.

Lead Material	Property Advantage
Nickel "200" (gold-plated)	High temperature coefficient of resistivity (excellent weld characteristics)
Kovar (gold- or tin-plated)	Glass seal
Dumet (gold- or tin-plated or solder-coated)	Glass seal, high frequency
Copper (gold- or tin-plated or solder-coated)	High thermal conductivity

2.1.2 Lead Diameter. A lead diameter range of 0.016 to 0.032 covers most subminiature components currently available. Within this range 0.020 represents the most common size.

2.1.3 Lead Tolerance. Changes in lead diameter have a direct bearing upon welder heat and pressure settings; consequently, permissible tolerances on the nominal lead diameter size are extremely important. Lead diameter tolerances of not more than $\pm 5\%$ on leads smaller than 0.020 and not more than ± 0.002 on leads 0.020 and above are recommended to ensure adequate process control. Unilateral tolerancing is permitted within these extremes.

2.1.4 Lead Plating. Lead plating can be of benefit to the welding operation depending upon the type and thickness uniformity. Where leads are coated by a dipping process, variations in thicknesses may result in inconsistent weld strengths. Therefore, selection of components with leads coated by dipping should be avoided unless there is assurance that the technique used provides a uniform coating. The amount of welder electrode contamination varies with the type of plating material used. Of five different materials recommended for plating—gold, nickel, tin, silver, and solder—the first four cause slight contamination whereas, solder of high lead content builds up a deposit after a few welds and may necessitate frequent electrode cleaning and changing. Hot dipping of leads is unacceptable because the surface roughness causes variations in diameter in excess of the allowable ($\pm 5\%$ or ± 0.002) and in addition results in occasional globules of coating material which interfere with the welding process. Of the five plating materials, the first four are the most desirable and are listed below, in order of preference, with applicable military specifications.

a. Gold Plating per MIL-G-45204, Type I, Class 1
b. Nickel Plating per QQ-N-290, Class II
c. Tin Plating per MIL-T-10727A, Type I
d. Silver Plating per QQ-S-365a, Type I, Grade A

2.1.5 Cleanliness. Weld locations along component leads must be free of coatings other than the lead plating. The maximum dimension of a component body must include the meniscus along the leads. This permits the inclusion of proper clearances in the module design to eliminate the possibility of welding on the coated area.

2.2 Vendor Guarantee of Size and Tolerance Consistency

Component space allocations within a 3-D module is much more critical than when using the conventional planar packaging techniques due to the proximities of adjacent parts. To assure that the component bodies are within the limits established by the positioner outline, it is necessary to use maximum envelope dimensions. These dimensions and associated tolerances must be guaranteed by the manufacturer to eliminate possible interferences.

The vendor will further be required to supply parts which will successfully pass the lead data inspections which will be part of the incoming inspection program. Lead control requirements are described elsewhere in this handbook.

2.3 Compatibility with Encapsulation Technique

Examination of all parts is necessary to assure component survival during the encapsulating process. Components whose inner elements are not completely sealed must be treated prior to encapsulation to eliminate the possibility of the encapsulant affecting the component function. If this type of preliminary processing cannot be accomplished, an alternate component must be chosen. Some components of all types are designed to be compatible with subsequent encapsulation operations, therefore, unless a requirement exists for a unique situation, special parts should not be necessary.

2.3.1 Adjustable Components. That portion of an adjustable component which is to be encapsulated within a module should be provided with an adequate seal to keep the encapsulant away from the component's moving parts.

2.3.2 Fragile Components. Components should not be used which are susceptible to damage by the differential thermal expansion between the part and the encapsulant during the curing process or during operation. Components in this category generally have glass bodies.

2.4 Environmental Resistance

A wise requirement of the welded module and similar electronic manufacturing is that parts must be at least compatible with conventional packaging techniques in resisting severe environments. Reducing this requirement to the component level necessitates careful examination of all parts data. Lowest-reliability components should be most closely reviewed and improvements sought since they effectively control the module reliability. Good numerical data are generally available from the military, which afford good comparative procedures.

2.4.1 Temperature. The effects of temperature on component reliability requires that components be used which will operate efficiently over a wide range of temperatures. For this reason, silicon devices are more desirable for use in 3-D modules than germanium. This also permits the use of encapsulants with higher curing temperatures. It is recommended that components be selected which will withstand exposure to temperatures of 125°C and greater without an adverse affect on their operating characteristics. In applications where it is necessary to use germanium devices, a maximum exposure temperature 85°C is required to avoid degradation of component life expectancy. This places a limitation on the encapsulants in that only materials of low curing temperature can be used. Thermal isolation of the part within the module may also be required.

2.4.2 Other Environments. As long as components meet or exceed the environmental requirements of military specifications they are adequate for 3-D module design.

2.5 Availability

All components and parts of a welded module design must be investigated as early as possible to determine the availability. The engineer should allow sufficient lead time for component delivery; particularly for any special part requirements. Special or nonqualified parts will require additional lead time so that proper part processing and qualification procedures can be performed.

2.5.1 Cost. Components should be selected which may be readily obtained to avoid any possibility of costly delays in production due to a long lead delivery time.

2.5.2 Reliability. Parts should be selected from sources where reliability history is known and acceptable. The procurement of special parts or special features on common parts frequently results in a serious degradation of reliability.

2.6 Alternate Sources Complying with Above

All designs should provide for component availability from several qualified sources. Continuous research by component manufacturers is providing parts of better quality and often more desirability for welded module application. Smaller parts of equal or higher reliability are sought after by persons engaged in miniaturization of electronics. Reliance on one source of very new but small parts may cause serious redesigns where larger volumes are resultant.

2.6.1 Safety Against Catastrophe. Parts available from at least two sources prevent a production stoppage due to strike, weather, or other causes of delivery delays. The emergency procurement of alternate unqualified parts seriously degrades the product reliability.

2.6.2 Competition. Alternate sources provide competition which leads to lower costs without sacrificing reliability.

Section 3.0

MANUFACTURING AIDS

To maintain high reliability with high-volume production, welded electronic modules will require specialized manufacturing techniques. These manufacturing techniques and aids will be developed to eliminate all possible operator error and to facilitate high-volume production and in-process testing.

The primary aim is to assure that each welded connection is properly made using the specified component and bus material, with an approved welding schedule.

3.1 Part Kits

Parts received from vendors are inspected by Receiving Inspection and placed in sealed kits prior to module assembly. This kitting technique simplifies stocking and dispensing to the factory and eliminates module assembly errors. The sealed kits also assure maximum cleanliness and minimize part handling.

The component quantity that is stocked in sealed kits is largely dependent on the rate of production, therefore no nominal kit quantity can be established and followed. Each kit contains sufficient quantities of parts (and raw material) for each production run of modules of an exact type.

3.2 Charts and Graphs

Various visual aids can be used in many phases of manufacturing and are not merely limited to the welding process. However, to increase the efficiency of the welding operation, the addition of appropriate aids should be incorporated. Weld schedule and weld sequence charts can be developed using a "cross reference" method to check proper location of a specified weld setting. Coding and correlating such data on both a supplementary document and the actual hardware (where applicable) will provide sufficient welding operator information.

3.3 Illustrations and Photographs

Where graphic aids give insufficient information, illustrations and photographs may be used to determine visually if all welds and assembly operations are correct. Additional data can be provided which includes component polarity, proper positioning in critical areas, excess lead length (if necessary), and connector or header provisions. A photograph of a completed weldment can serve as a visual self-check to provide process information to the operator, the inspector and supervisory personnel. The use of transparent overlays arranged in a sequence will expedite the determination of a proper assembly.

3.4 Audio-Visual

These aids can be used advantageously during initial production runs for operator familiarity. The automatic (timed) programming method enables the operator to be paced through various assembly and equipment maintenance steps. However, this method does not allow the individual to correct any error during the programmed sequence. The demand (operator actuated) method permits the individual to spend as much time as needed to perform each operation. However, spot time checks should be measured to establish a level of operator proficiency.

Prolonged usage of audio-visual aids is not usually an advantage after the operator has started on a long production run. Audio-visual aids should be discontinued when in such cases they may become an annoyance.

Section 4.0

LEAD CONTROL

One of the most important requirements in the manufacture of welded modules is the control of the quality (variations in weld strength) of all welds. Electronic components which are procured as the same type and which bear the same part number frequently exhibit variations in lead weld strength when welded with controlled equipment. These variations are due to differences in the physical properties of the leads. Rigid control of all component leads is therefore essential to maintain high reliability welded modules.

The influencing factors causing weld variation, and the necessary controls that must be exercised to reduce these variables are as follows.

4.1 Material Composition

Although it is desirable to use components in the "as-manufactured" condition, necessary parameters peculiar to the welding process must be controlled. To maintain economics of manufacture there must be sufficient latitude in these parameters to permit minimum modification of existing part manufacturing and control; further it is desirable to maintain such component parameters compatible for both welding and soldering.

4.1.1 Weldability. The degree of ease of achieving a high-strength weld using lead materials typical on electronic components will vary depending on the material composition and the diameter and plating of the lead. Some materials are readily weldable over a wide range of diameters while others are less flexible.

A knowledge of material *vs.* its weldability is required in order to establish the importance of these variations.

A material desirability rating is as follows for the component lead materials and joining media indicated below.

Material welded to 12 × 30 mil Nickel Ribbon	Desirability Order (min strength/sample size)
Nickel wire	15.6/300
Kovar	11.0/800
Copper (0.032 diameter)	8.6/784
Dumet	8.0/800
Copper (0.025 diameter)	7.0/793

The above numerical comparison or order is based on minimum strength and sample size. Each material has a different rating for each different bus size; the above order is for 0.012 × 0.030 nickel ribbon. The series of numbers under the heading "Desirability Order" indicates the minimum breaking strength of a given combination together with its sample size. The costs and methods of obtaining and maintaining the reliability of each weld combination may be different.

A complete listing of all material combinations, compared at the same sample size, should be established to provide this desirability rating. In addition, it is desired to have these comparisons for various sample sizes. A complete treatment of this subject is contained in Section 9.0. Further studies could alter the minimum strength values tabulated; however, relocation of the tabular order given is doubtful.

4.1.2 Preferred Materials. To maintain high-reliability welded connections, it is necessary to use materials which offer consistently good welding capabilities. The feasibility of minimizing the number of different lead materials and sizes has been proved. The above list represents the most common materials used for component leads in subminiature and some microminiature parts. Maintaining a minimum number of different component lead materials will facilitate setting up an efficient method of control. Several component manufacturers supply components with a variety of lead materials, coatings, shapes, and sizes. Performing analyses and establishing weld schedules for all of the possible combinations would be extremely time-consuming and to a degree, economically unsound.

Since weld requirements are only a portion of the total properties necessary, several different kinds of lead materials must be used. Each material has a particular characteristic(s) and is therefore more advantageous for use in meeting certain circuit, mechanical, or environmental requirements. These materials have been chosen by the component manufacturer and industry as being the most satisfactory.

The following data discuss the preferred lead materials and the factors that must be met to assure proper control.

All component lead materials must maintain consistent mechanical properties conforming to procurement specifications. The control should be on the ultimate breaking load of each wire size on which a knowledge of the chemical composition is known and prior testing has provided. The allowable elongation limits, also provided from prior testing, must be measured and recorded to determine that proper material "condition" is being supplied.

In the event that the control requirements on the ultimate breaking load and elongation are not met, a test should be made upon chemical composition to determine where the material has failed to meet specified composition or condition.

A visual control for workmanship should be exhibited for cleanliness and freedom from harmful grease, oil, dirt, surface defects, and any foreign matter.

4.1.3 Availability. Proper controls must be initiated to assure consistent availability of preferred lead materials and coatings on all components used for welded module application. Adequate preliminary

planning in this area will avoid both time delays due to manufacturers' shortages and enforced use of alternate lead materials which do not have the specified requirements. Consistency is as important as basic physical requirements.

Periodic checks should be made on the various component manufacturers' products to assure the availability of specific lead materials and coatings.

Each component type should be available from at least two qualified sources to avoid delays due to economic, material, or technical fluctuations typical of any manufacturer.

4.2 Dimensions and Tolerances

Prior to the inception of welding as a joining method, the lead size and diameter variations of components commercially available was a matter of little concern. Since the introduction of this technique, it has become necessary to place more stringent controls on lead diameters and tolerances to achieve necessary limitations on weld strength results.

4.2.1 Limitations of Lead Diameters. Due to the large number of component manufacturers currently supplying industry, a wide range of component lead diameters exists. It has become desirable to limit the number of different lead diameters available to effect reliable welding at reasonable costs. Unless such a limiting control is placed on component lead diameters, many costly and unnecessary control data must be generated, such as weld schedules, metallurgical, chemical, and statistical analyses.

Satisfactory results can be experienced for most applications by limiting the lead diameters to a few sizes in a specified range.

The preferred nominal diameters are 0.016, 0.020, 0.025, and 0.032. The above lead sizes will accommodate most components currently being manufactured for modular application.

4.2.2 Permissible Tolerances. To effectively utilize a predetermined weld schedule for maintaining repeatability and satisfactory welds, it is necessary to control the variations in lead diameters of all components. Large differences in component lead diameters will have an effect on the weld schedule and, therefore, on weld quality and weld strength.

The tolerances placed on component lead diameters should be determined by first considering the method of manufacture and the plating (or coating) technique, if any. It would not be practical or profitable to force a wire manufacture to adhere to stringent tolerance controls merely for the sake of achieving precise welding conditions resulting from unrealistic lead diameter tolerances.

The discussions on lead tolerances under Section 2.0 describes what is considered adequate for lead tolerances in keeping with best commercial manufacturing practices.

4.3 Plating and Coating Material

Component lead coating was initially provided as an aid for the soldering process, and to protect the base material from corrosive environments. Some lead coatings (tinned copper) are used as a lubricant during the component manufacturing process. Lead coatings are not necessary for the welding process; however, to maintain compatibility with soldering and to provide desired part processing needs, certain controls are required. The more important factors are outlined as follows.

4.3.1 Type and Uniformity of Plating. Component lead plating cannot be directly associated with any basic lead material. One type of lead material may be found with a variety of finishes or coatings depending on the component manufacturer. The selection of preferred components with emphasis on meeting standard finishes will automatically decrease the number of different lead plating types. The uniformity of the lead coating is just as important as the coating itself. Requirements should be established to control the uniformity with respect to the chemical composition or purity of the different materials being used. Acceptable limits must be defined describing maximum and/or nominal allowable percentages of each element including trace elements. Generally, there are applicable military specifications completely describing the quality levels and necessary controls. For applications not as yet outlined in military specifications, appropriate standards will have to be introduced.

4.3.2 Electrode Contamination. Frequent periodic checks should be made during the production phases to determine the amount of electrode pickup from various lead coatings. A definite procedure must be evolved to determine whether controls are being set on contamination of electrodes or deposition of the lead coating materials. Electrode tip pickup of lead coating material does not necessarily induce contamination. Contamination of the electrodes is quite typical when using solder coated copper leads. The relatively low melting temperature of the solder coating together with its affinity for copper (electrode material) will cause adhesion to the electrode face due to heat during the weld cycle. Emphasis should be placed on eliminating any possible build-up of other materials on the electrode faces. This includes any paint on the component leads caused by color coding and identification on the component body, any meniscus along the component lead resulting from manufacturing techniques, and dirt, grease or other foreign matter deposited on the leads as a result of in-process handling.

4.3.3 Preferred Material. Preferred component lead plating material controls should be based on the ability of the material to exhibit the desired weld characteristics with no detrimental effects on either the base lead material or the electrode surfaces. The data contained in "Lead Plating" under the heading "Parts Selection" in Section 2 describe the five recommended lead plating materials in order of preference.

The order of preference is based upon the susceptibility of the coating material to be transferred to the electrodes which would require frequent cleaning operations.

Since it is not practical to have one type of lead plating for all components, the referenced list of preferred lead coating material, when used, will assure good weld results.

4.4 Plating or Coating Thickness

Assurance of continuous good weld results requires additional emphasis on lead material coating thicknesses. The type and thickness of these coatings have an effect on the weld strength variations capabilities and therefore the thickness that exhibits the optimum "overall" conditions should be used. For example a heavy coating of solder over a copper base material is excellent for atmospheric corrosion resistance and is highly desirable for solder applications; however, excessive solder coating is not acceptable for welding due to electrode pickup creating frequent maintenance operations. Precious-metal plating should be relatively thin and of the soft type. A thicker and harder plating of these metals creates higher weld energy for the same weld, is vulnerable to cracking if bent sharply, and is needlessly expensive.

4.4.1 Thickness per Military Specifications. In most cases, the military specification describing plating thicknesses is adequate. However, these specifications usually do not include requirements necessary for welded module application. As an example, Specification MIL-G-45204, Type I, Class 1, specifies a plating of 50 μin. minimum and no maximum thickness restriction. Class 6 specifies 1500 μin. minimum and no maximum. In reality, Class 6 plating conforms to the previous five; therefore, maximum limits should be determined on the thickness of all plating materials chosen for needed module applications. All lead plating materials having applicable military specifications should use these specifications as a basis for determining the necessary controls. In some instances the military specifications as written may suffice.

4.4.2 Tolerance. Extremely tight tolerances on leads that are electrodeposited are very easy to achieve. Component lead coatings that are provided by a dipping process will require supplementary operations to achieve a like tolerance as those of plated leads. Controls should be relaxed in this area to permit economical means of coating lead materials. Proper determination of weld schedules can be sufficiently flexible to compensate for some variations in component lead coating thicknesses. Variations in lead coating thicknesses will usually cause inconsistencies in weld strengths. However, this is not to be considered as detriment in that, after determining the best weld conditions, the minimum strength figure should be well above the minimum allowable strength values provided by prior tests and statistical analyses.

4.5 Handling of Leads

Controls for the proper handling of leads should be introduced and maintained throughout all phases of manufacturing. These controls must minimize the possible contamination and damage resulting from the "in-process" functions peculiar to each phase. Prior organization as to polarity orientation and transistor lead positioning in handling equipment should be maintained.

4.5.1 Vendor Packaging. Handling methods must be devised which protect the parts from damage during transport within the manufacturing plant.

Controls must be initiated and maintained by all vendors supplying components for welded applications to keep from damaging parts. Coordinated controls must be set up between vendor and customer to assure that the necessary steps have been taken on these handling procedures. Areas of concern are bent leads, damaged leads, corrosion, contamination, and identification. Recognition of critical, major, and minor defects must be determined and fully understood by the vendor. Proper and careful component packaging enhances the economics of part supply and is not difficult to achieve.

4.5.2 Receiving Inspection. All component parts should be sample inspected where initial sampling should be 100% for all attributes. Suitable acceptable quality levels should be established after production runs have been started. These levels are based on part defect classifications provided by test histories to provide maximum latitude in manufacturing. Receiving inspection is performed to assure proper part type, ratings, condition, and lead data. Part procurement data sheets and previous test findings outline all component lead criteria and fully describe all controlling measures. All component lead materials must conform to these criteria for material composition, consistency, plating type, and plating thickness. The controlling factors will vary slightly for each different lead material. Certain lead materials will require additional inspection controls. For example, dumet must adhere to the same set of controls as other component lead materials, but additional requirements must be placed on the copper sheath thickness, consistency, and concentricity to that of the core material. Inconsistent cross sections in this material may alter a predetermined weld schedule established. To facilitate interchangeability of parts from alternate sources using the same weld schedule, controls are necessary.

4.5.3 Kitting and Stocking. Exercising adequate controls at the inspection level will eliminate the necessity of random sampling of the sealed kits to verify the condition of the component parts contained therein. As the production rate demands, the kits will be removed from the stock areas and all lead materials will be visually inspected along with all other inspection functions to assure that no physical damage has resulted during shelf life and/or possible mishandling.

4.5.4 Module Assembly. Production line surveillance inspection is required for all manufacturing operations which will include lead data. Verification must be made to assure that component lead materials have been determined and proper weld schedules have been established. No assembly should be initiated without verification of these requirements. Knowledge of lead data for each part is imperative for satisfactory use of predetermined weld schedules. In the event a part has been interchanged, and the lead material is in question, a metallurgical or chemical analysis may be required to verify the material type, composition, and plating. Proper in-process controls, however, should eliminate the possibility of alternate lead materials becoming intermixed in especially prepared kits. Process Control should conduct time-cycled examinations of each type of lead in production use. Parts that have been dropped or substituted from "free stock" should be rejected from use in manufacturing sequences unless proper qualification is made.

Section 5.0

WELD SCHEDULE DEVELOPMENT

The overall reliability of the electrical connections within an electronic assembly should be made high with respect to the component part reliability. Welding provides a process which is inherently suited to making high-reliability electrical connections. The ultimate success of the welding process will depend to a large degree on the quality of the weld schedule which is used. The weld schedule provides all the pertinent data which is required for setting the parameters of the welding equipment.

Before a weld schedule can be developed, the type and model of welding equipment to be used must be firmly established. The power supply and welding head must be selected which will fit the particular needs of the company. Upon selection of the proper equipment, the task of setting the necessary parameters for welding is begun. Such things as electrode length, electrode configuration, length of cables from power supply to welding head must be determined. After establishment of the parameters, it is necessary to establish process specifications which will assure that they remain constant. Several steps must be taken in determining the quality of a welded connection. These steps include mechanical testing, and metallurgical analysis. Each of these steps must be included in the development of an optimum weld schedule.

5.1 Mechanical Tests. Mechanical testing is the most important and in some ways the easiest step to perform. The main data which concerns the welding engineer is found from this type of testing. Mechanical tests yield numerical values from which the reliability and repeatability of weld joint strengths can be determined. The major factors which must be resolved to determine that a given weld schedule is the optimum schedule are: (1) the strength of the average weld, (2) the repeatability of the results, and (3) the strength of the minimum weld.

The mechanical test is a destructive test on sample welds which are made in the same manner as welds found in modules. The sample welds are torn apart in a manner which simulates the most adverse conditions under which a weld joint can be stressed and not necessarily typical of use in a module.

5.1.1 Type of Test. The most discerning of the mechanical tests is the torsion-shear test in which the coupon is stressed as shown in Fig. 5-1. This places the weld coupon under combined tension, torsion, and shear stresses. The manner in which the coupon fails is significant, and this information, as well as the numerical value obtained from the pull tester, is recorded. A tension failure indicates that the weld and adjacent areas are stronger than the parent material; a torsion failure shows insufficient fusion, and shear-tension failure indicates a weakness in the parent material adjacent to the weld. The most desirable condition is usually obtained when coupons from the same group fail in the parent material away from the heat-affected zone.

Another mechanical test which can be used in conjunction with the torsion-shear test is the cross-tension test. This test can be performed in two pulling modes, nickel ribbon cross-tension or lead material cross-tension. In the nickel ribbon cross-tension test, the ribbon is placed between the jaws of the tensile testing machine and pulled against the weld joint as shown in Fig. 5-2. In the lead material cross-tension test, the component lead material is pulled against the weld joint. This type of loading is less drastic than the torsion-shear test described above; consequently, its use in weld schedule development is not preferred. Additional weld information can be obtained using the cross-tension test by providing a comparison of weld shear strength to parent material tensile strength.

5.1.2 Equipment. The mechanical tests can be performed on any acceptable testing machine such as the Hunter, Model TT-H (Fig. 5-3). This tester is equipped with jaw-type grippers on each end that close upon the sample before exerting pressure, and release the sample when returned to normal position. The tester is operated by air pressure with a pull rate of approximately 1 in./sec. The pull test rate should be constant for all tests where comparisons are made. It has been shown that 1 in./sec is a satisfactory rate. Slower rates yield lower results by a small percentage (less than 10%); otherwise no differences exist.

The range of this machine is 0–50 lb. Details of the circular attachment used for the cross-tension welds are contained in Fig. 5-4. The proper slot must be selected in this attachment to reduce the amount of variation in the test results. The slot chosen must fit the weld area properly. It must not be overly wide to permit the lead to fold over and pull through nor so narrow as to eliminate the weld-affected zone from the test. This test method also suffers from errors due to the locking which is caused by deformation and depression of one lead into the other.

5.1.3 Visual Examination. A visual examination of the external appearances of the welded connection, as well as the fractured surfaces, will often reveal useful information. Visual examinations are usually performed using a binocular-type microscope of 10 and 20 power. The external appearance will reveal such defects as poor positioning of electrodes, expulsion, spitting, dirty leads, and electrode pickup. This can also reveal instances of underwelding and overwelding, but does not reveal much information on the in-between area.

The study of the fractured surfaces will reveal additional information such as internal defects, obvious solder inclusions, brazed joints that are ineffective and excessive weakening of either weld member. The presence of spitting or upsetting as revealed by visual examination is not cause for rejection, since a certain amount of upsetting is necessary if a weld is to be made.

5.2 Metallurgical Analysis. Metallurgical analysis includes metallography and physical testing as parts of the analysis. Generally there should not be preferential consideration given either of the metallurgical or mechanical results obtained in sample testing for the establishment of weld schedules. The metallurgical evaluation should involve acceptance criteria which all welds must meet. Because of the

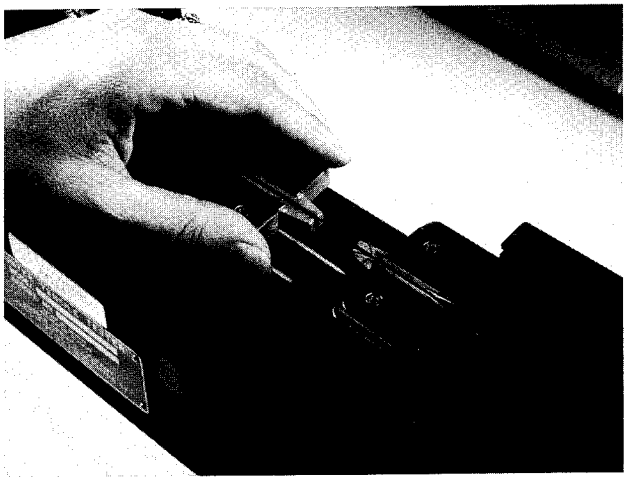


Fig. 5-1. Torsion-shear test.

varied material combinations encountered, there is particular significance about the interchangeability of qualitative data. For example, dumet wire may weld very well, yet characteristically may not exhibit much deformation, while a satisfactory Kovar-to-nickel weld may require more deformation.

A material combination such as nickel-to-nickel may exhibit a nugget, while nickel-to-dumet shows limited evidence of interface fusion.

It is incorrect to generalize the requirements of such factors as deformation and type of interface structure. Optimization of each material combination should include the optimum physical characteristics which are discovered by metallurgical analyses by a professional metallurgist.

Metallography should be employed on each material and geometric combination for the purpose of photographically recording the micrographic appearance of optimum welds.

The procedure involves determination of optimum metallurgical appearance for each material combination, then confirmation by comparison with the appearance of other cataloged similar material combinations.

The basic considerations found applicable to all resistance weld processes involve (1) heat balance—influence of electrode materials and electrode faces, and (2) extent of heat-affected zone. Limitations here are applicable where (1) insufficiently large heat zone causes low weld strength while the structure may be "excellent" and (2) an excessively large heat-affected zone may degrade the properties of the parent metal cross section out of the weld zone. Excess heat can cause undesirable electrode contamination.

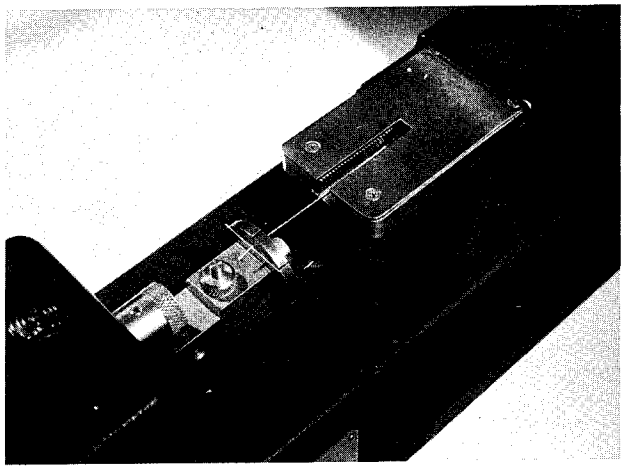


Fig. 5-2. Cross-tension test.

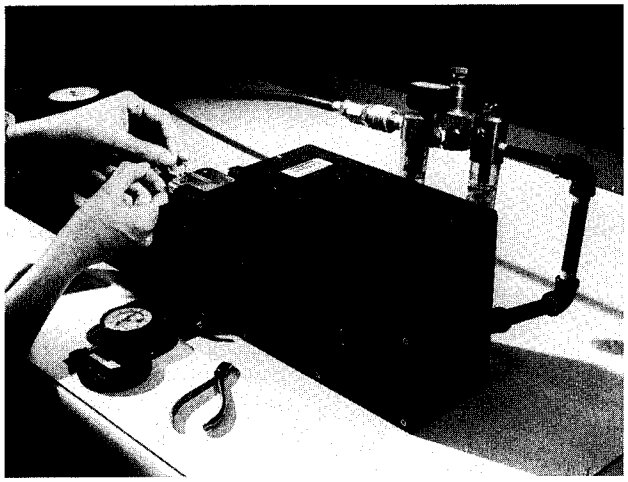


Fig. 5-3. Pulling samples.

In welding process control, duplication of a condition previously determined as acceptable is sought rather than "optimum" structure. For example, the basic object of a dumet-to-nickel weld is to (1) expel the copper sheath exposing a nickel-to-dumet core interface, and (2) limit overheating of the copper sheath (of dumet) to prevent electrode contamination due to skin melting. Metallographic analysis coupled with mechanical analysis will corroborate (1) above; similarly, weld strength consistency should corroborate (2).

Each and every weld schedule is required to have a metallurgical examination along with mechanical tests. Recorded metallographic data required as a part of weld evaluation is as follows:

a. Heat balance—maximum heat and fusion zone should appear as near the weld interface as possible.
b. Evidence of overheating—as seen around circumference of leads.
c. Evidence of overheating—determined by grain structure.
d. Extent of heat-affected zone.
e. Net deformation of combined leads.
f. Degree and extent of coating material included in the interface.
g. Other qualitative observations which can be made metallographically.

5.3 Weld Parameter Diagrams

The welding engineer responsible for developing these diagrams circumscribes the area of investigation because of his past experience in weld schedule development. Assuming common subminiature parts, rarely can an acceptable weld schedule be found at a pressure less than 5 lb; at pressures greater than 10 lb the electrodes may be subject to bending. The extent of electrode movement under higher pressures is dependent on such variables as electrode size and shape, electrode material and the degree of the included angle. Other electrode sizes, shapes, and materials may offer entirely different strength ranges and physical characteristics.

The following data are based on the information contained in Paragraph 8.2 (Fig. 8-2). As an example, when using two copper electrodes of the above referenced configuration, the limits of investigation should range between 5 and 10 lb.

The schedule has not been found to be particularly sensitive to pressure changes, and therefore electrode force changes are usually made in 2-lb increments. The limits of pressure which are applicable for one company may not be useful for another company using other equipment or a different electrode configuration. Each individual developer must establish his own parameters and then, through experimentation, decide upon the limits of pressure which he intends to investigate when developing a schedule.

The limits of investigation of energy settings is, again, a matter of the experience of the welding engineer. At low watt-second settings there is not enough energy available to make a good weld, and at excessive watt-second settings the energy is so great that disintegration of the weld joint takes place. The experienced engineer will select the range within which he knows good welds can be made, this range will be larger for those with less experience.

The interval between energy settings which should be investigated will depend upon the material being welded. For instance, when welding Kovar it is necessary to make welds at every $\frac{1}{2}$ W-sec interval. Dumet is usually tested with intervals of 1 W-sec between samples, nickel jumper wire 2 W-sec, and 0.032 diameter copper is investigated at 5 W-sec intervals.

There are several methods which may be employed to develop a welding schedule. The welding engineer who has considerable experience can develop a schedule rapidly because he can eliminate certain steps which the less-experienced developer will not care to skip. Two methods will be explained here, together with additions and variations which will be helpful to those in the beginning stages of a development

program. The weld profile method is recommended as the easiest to understand and the most efficient method.

In either case the selection of materials for use in weld schedule development and weld process proofing (Section 9) are of major importance. Sufficient material should be obtained for the complete diagram use and for the subsequent proofing. A range of quantitives usually sufficient is 1000 to 2000 welds for the profile method and 2500 to 3500 welds for the isostrength diagram method. The component lead materials should be obtained from typical component parts with as much allowed variability as is possible. The component lead materials should be obtained from typical component parts with as much allowed variability as is possible. The bus material should also reflect its allowed variations. These materials should then be deliberately randomized and used for schedule determination and proofing tests. Enough material should be saved from the lot for proofing, 800 for probabilities stated in Section 9. The sample welds should be made with one operator using one frequently calibrated welding station and all at one time (or extra tests to determine compatibility). The samples should all be tested using one operator on one pull tester at one pull test rate.

5.3.1 Weld Profile Chart. A weld profile is a method of establishing an optimum weld schedule which provides an efficient and simplified procedure. The weld profile is a plot of weld breaking strength *vs.* energy at constant electrode pressure (see Fig. 5-5). The weld profile method is actually more meaningful than the isostrength diagram since the dependent variable, weld strength, is plotted permitting its variations to be read directly. The least important independent variable, weld pressure, is constant for each profile, and by providing a separate curve for each pressure of interest, an entire field of welding parameters can be made and analyzed at considerable time saving over isostrength diagrams and their analyses.

Through the use of a weld profile it is possible to completely analyze the average weld strength and the range of strengths at each energy setting. A line drawn through the average strengths will usually establish a plateau of high average strength values. The plateau is then examined and a point is selected which shows a combination of high average strength and low spread from the high to the low value within the sample. A sample of ten welds is usually made at each energy setting on the chart. The profile method further allows the investigator to select more points as the curves are plotted or possibly eliminate unnecessary points. The range of values around the ten samples can be shown which is an indication of variability giving an indication of optimum weld regions.

5.3.2 Isostrength Diagram. The isostrength diagram is a graphic means of determining the optimum weld schedule which is indicated by a series of ascending steps. Each step represents the average value of a sample of welds taken at some specific energy and electrode force setting. The energy and force settings are increased in proper proportion until the maximum average strength is achieved. Response surface methods have been used to minimize the number of steps required to arrive at this maximum average strength. However, the optimum weld schedule is not necessarily found at the highest strength point on the diagram. Most material combinations will exhibit more than one good weld zone. These are usually shown at isolated locations in the diagram field. The welding engineer should give full consideration to all potentially good weld zones when attempting to determine the proper welding parameters.

The person beginning a new development program for weld schedules may wish to make a complete isostrength diagram on his first few schedules. If this is done it will afford an opportunity to see rapidly the extremes, weak welds, which should not be further investigated. As the engineer gains experience he gradually narrows the area of investigation until the complete isostrength diagram becomes unnecessary. Each point of the isostrength diagram is found by averaging the strengths of 60 welds (smaller samples are often used, but the results are then too broad to permit a valid choice between adjacent points) made at the corresponding energy and pressure settings. Figure 5-6 illustrates a typical isostrength diagram.

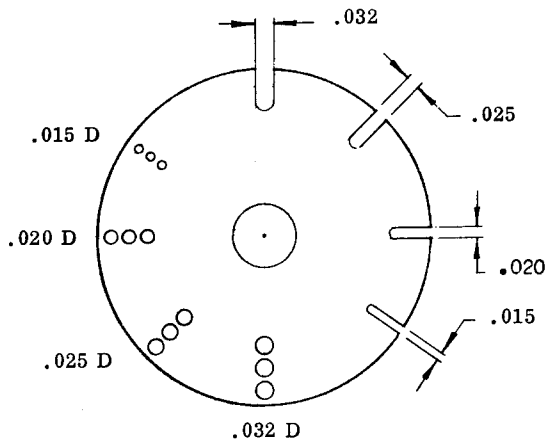


Fig. 5-4. Details of stationary gripper used on the Hunter tensile tester.

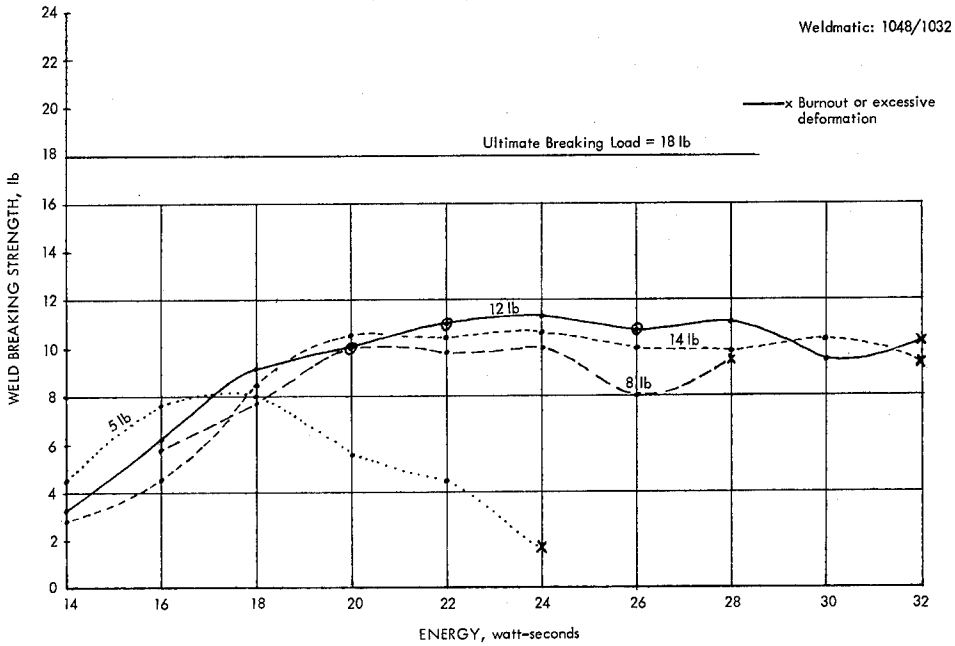


Fig. 5-5. Weld parameters profile.

5.4 Optimization of Weld Parameters

The data contained in the weld profile chart and/or the isostrength diagram when used with previously recorded data such as electrode sticking, electrode pickup, and overheating provides the preliminary information needed to optimize a weld schedule. It is desirable to reduce the number of settings required for all weld schedules to as few as practicable to minimize the setting operations (fewer changes in machine settings and less chance of operator error). Electrode pressure has been found to be a less critical factor than energy, which permits fewer standard pressure settings. The optimum point selected for a weld schedule is not at the highest strength or lowest scatter, but rather is very close to this point together with compromises which are important economically to the manufacturing operations. The following data discusses the factors necessary in determining the optimum weld parameters.

5.4.1 Examination of Graphic Data Supplied. The task of optimizing a weld schedule begins with a thorough examination of the weld diagrams. Each diagram will illustrate several weld strength profiles at different electrode pressure settings. Certain electrode pressures will exhibit a high-strength profile while other pressures show medium- and low-strength profiles with some drop off at higher energy limits. The profile groups on a single diagram will usually display two or more curves at close proximity and remaining somewhat parallel over the major portion of the field.

Similar information is available on the isostrength diagram. The average strength and the minimum strength is shown at each setting of the electrode force and energy. However, this necessitates interpolation between the individual points to determine the isostrength lines. The isostrength lines will indicate no weld conditions, usually at lower settings, as well as areas of burn-out due to excessive electrode force and/or energy. Both weld parameter diagrams must indicate the material combinations represented by the diagrams and should show equipment polarity and electrode type(s). The above data will aid the welding engineer in determining the most favorable weld conditions.

5.4.2 Selection of Weld Schedule Point. Several desirable points may exist on a single profile for a given material combination. The welding engineer must observe the changes in the range along the curve to select the most favorable point. Comparisons with diagrams of other material combinations should be made in the event the selection of a point on one profile would be applicable with minor adjustments. A critical weld diagram may be combined with a number of more flexible diagrams to permit several material combinations to be welded with a single setting. Combining weld schedules must be approached with caution. Consideration must be given to all influencing factors peculiar to each material combination to achieve the best possible set of weld conditions.

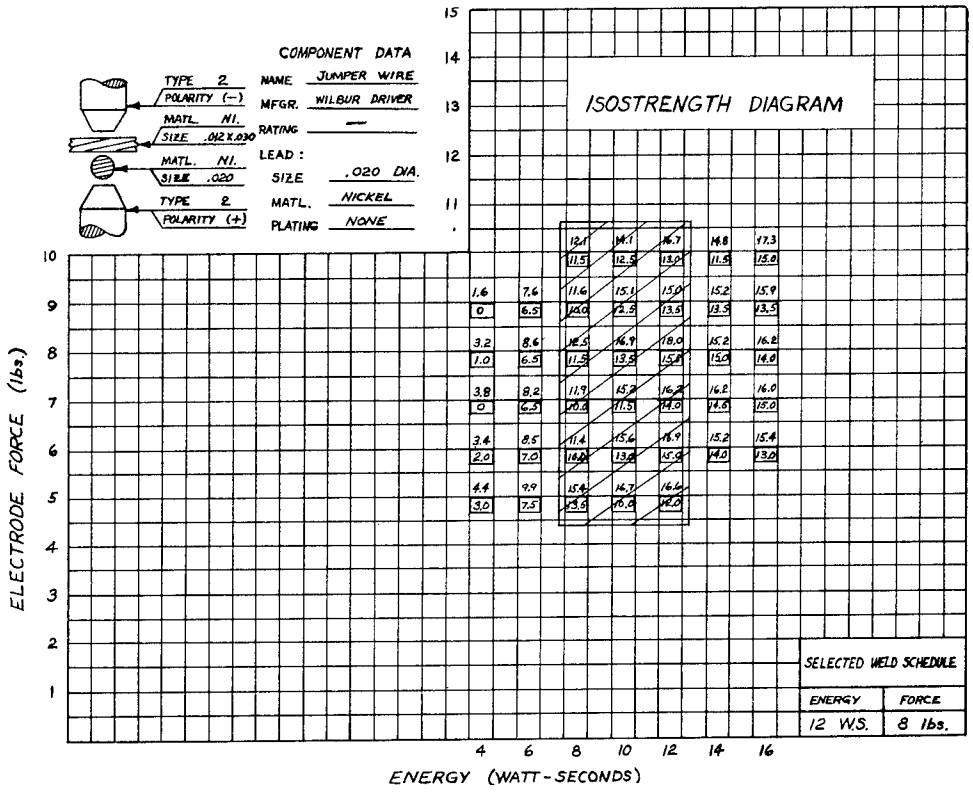


Fig. 5-6. Isostrength diagram.

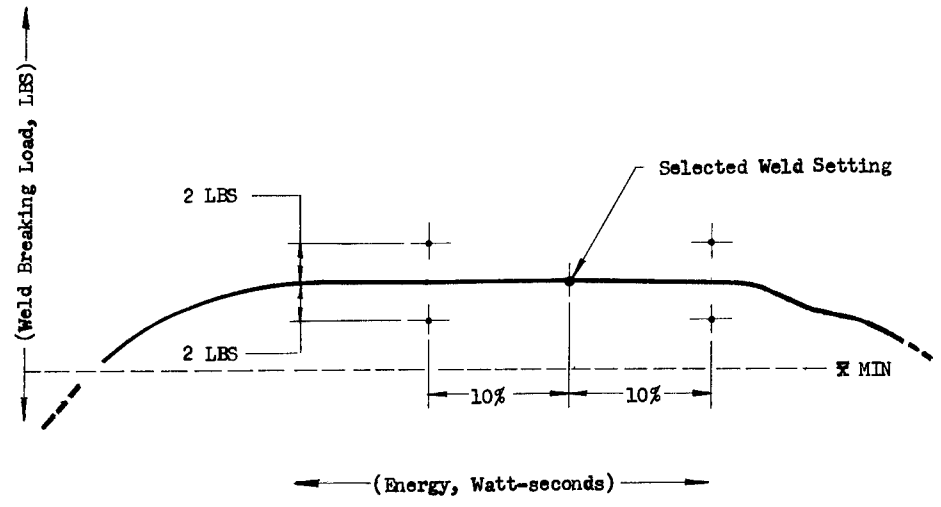


Fig. 5-7. Profile diagram point location.

5.4.3 Selection of Welder Settings. After preliminary information is recorded and displayed by either method discussed in Paragraphs 5.3.1 and 5.3.2, the welding engineer should further investigate the field of data to develop the optimum weld schedule. As an aid in selecting the profile point, certain applicable considerations should be observed which include:

1. Deformation—the percentage of reduction of cross section of either or both members being joined. Deformation is an indication of excessive electrode force which can otherwise weaken the average weld strength attainable.
2. Electrode sticking and tip pickup—the adhesion to the electrode(s) of a portion of the materials being joined or the coating of those materials. This sticking condition is evidenced by excessive energy especially at higher watt-second levels.
3. Compatibility with other weld schedules—a similarity of weld parameter diagrams for different material combinations. With slight modification this compatibility can reduce redundant weld parameter investigations.
4. Minimum number of electrode settings—the selection of a few standardized electrode settings that will cover sufficient area in the diagram field. Fewer settings of wide flexibility can eliminate unnecessary pressure changes. Comparatively, electrode pressure is less critical in establishing the optimum weld schedule.
5. Metallurgical comparison—a comparative check with known good welds of identical material combinations. Micrographic comparisions may not be required if the data being gathered is conclusive.

5.4.4 Weld Schedule Point Check and Strength Criteria. After considering the information outlined in Paragraph 5.4.3 the weld area can be determined. This weld area should be located at a point which has as much breadth as possible on the watt-second parameter with little or no resulting change in pull strength. The above point, and the adjacent area is evaluated by varying the electrode force ± 2 lb from the selected force setting and $\pm 10\%$ of the selected energy. At each of these points a sample of 50 welds are made and the pull strengths analyzed. The pull strengths at each of the five points should fall within the area of prediction provided by the previously mentioned considerations and should verify that (1) the sample size is sufficiently accurate to detect changes in pull strength adequately so that a weld schedule can be made, and (2) the changes recorded are indeed changes in pull strength and not a perturbation of data. This procedure will give a good evaluation of the weld strengths in the adjacent area to the selected weld settings. If any of the four corners yield weld joints which are different from the predicted strengths at the optimum settings it will be necessary to repeat the steps in the weld point selection as described in Paragraph 5.4.2.

The sample size at each point may be reduced in the following cases.

1. Where pressure changes have little effect on the weld strength as seen plotted on the weld profile chart or isostrength diagram, the box corners determined by pressure may be eliminated and only the watt-second variations surveyed.
2. In the event that the demonstrated ranges, as seen on the profile plots for watt-seconds, show relatively low variability in the regions of interest.
3. If the probability estimates and confidence limits exceed the minimum requirements for the low range zones (reference paragraphs 9.3.3 and 9.3.4).

5.4.4.1 Figure 5-7 illustrates a typical region where the most desirable weld results can be obtained. The initial location of the "Selected Weld Setting" on the graph is determined by the minimum acceptance level of the joint strength and should be above this level to warrant consideration. The minimum average weld strength, $\bar{X}$ of a material combination must be equal to or greater than 30% of the ultimate tensile strength of the weaker member being joined. In addition the minimum allowable strength requirements shall be achieved as specified in 9.3.3 and 9.3.4.1.

5.4.5 Use of Metallurgy. The selection of an optimum weld schedule should be conducted to include a metallurgical examination if possible. Although not a heavily governing criterion during the schedule development, it will assist in adjusting the weld schedule, if necessary, to arrive at optimum conditions.

Familiarity with metallurgy will give the welding engineer an understanding of the factors necessary to provide a good weld joint. If no similarity with specified parameters exist, a re-evaluation of the weld joint is necessary. This re-evaluation must be accomplished in accordance with Paragraph 5.2.

Section 6.0

PART HANDLING

The processing of electronic components through the various production operations has a bearing on the individual part reliability. This fact leads to the establishment of procedures which minimize the operations, deliberate or accidental, which are applied to the components. Mechanical parts do not require special handling, but may be included in the same procedures for continuity. Part handling equipment and accessories for welded electronic module production are designed for maximum flexibility in order to be usable for any size or type of module. The equipment is capable of handling component kits, assembled modules, and completed modules, and affords protection to the modules prior to potting.

6.1 Factors of Importance

The most important factor which has been found to contribute to part degradation is the mechanical mistreatment of the leads. Bending the leads produces stresses of unknown magnitude on part to lead terminations which suggests that leads should be straight and protected from initial shipment to final use. Lead mechanical mistreatment results in loss of coating and changes in shape and diameter along its length. This degradation is not of major import, but improvements in reliability can result in exercising care in stocking and handling. Tape mounted packaging is a good solution to the problem. Lot identification of parts is desired to facilitate isolation of as small a number of parts as possible if subsequent processing should show parts unacceptable.

6.2 Initial Testing

Repairs or part replacements to the 3-D cordwood assembly are undesirable and lead to unreliability therefore it is desirable to have assurance that component parts are acceptable prior to assembly. At receiving, parts should be tested for their critical attributes when it is economically sound to do so. Sampling at this level will be usually adequate in most cases since the part supplier should test all parts delivered.

6.3 Stocking, Kitting, and Distributing

The stocking of parts should be kept such that close control is effected on a first-in–first-out basis. Lot control should be applied on logically sized groups. Parts should be stored in a clean sealed condition in bulk prior to kitting. Kits should be used to provide assembly groups with properly organized and protected parts. Kits should not be made up before intended use because of the loss in inventory flexibility. Covered containers using polyurethane foam padding and eggcrate-type separators are used for this application. This handling equipment also permits transporting of the kits and modules avoiding contamination prior to welding or potting.

6.4 Assembly

The operator should assemble electronic parts with a minimum of lead bending. Fixtures should be provided which enhance easy assembly of parts. The usual method employs a holder of the end positioner which spaces them apart so that the extra long leads on the parts can be inserted first and held in place. When all parts are assembled the positioners should be positioned and held in their final spacing and position for all welding operations. Leads should be clipped off leaving excess material for welding so that the leads extend over the bus; after welding the leads are clipped off flush with the bus. Any parts which are accidentally damaged or mixed with other parts should not be used.

6.5 Reliability Monitoring

The part reliability can readily be followed if the reporting system is integrated with the processing steps. The call for much higher reliability than was obtained heretofore intensifies the needs to improve wherever possible the part reliability. By following each step of part exposure to handling it is possible to pinpoint operations which can make major improvements in the parts and subsequently the affected modules. It is desired to consider a flow line welding operation as a first instance as follows:

a. Welding operation—each station will perform only one welding operation or several welding operations to a single schedule.
b. Welding power—weld power will be set by the responsible engineer and will eliminate accidental welding to the wrong schedule. Also, machine adjustment by welding operators will be eliminated.
c. Welding station—it is anticipated that any high-volume module production operation will require several welding stations which are capable of welding any type of weld to any schedule. These stations will be in addition to the line flow stations and will require higher operator skills than the line flow stations.

Section 7.0

MANUFACTURING ENVIRONMENT

The specification on facility environments (Air Force T.O. 00-25-203, 7 February 1962) is desirable from a human engineering standpoint even though not required by the welding process. The environments listed in this specification that are recommended for a welding facility are:

7.1 Temperature and Humidity Control

Normal commercial air conditioning designed for temperature control of 72 $\pm$ 5°F is adequate for operator comfort. Humidity in excess of 50% relative is undesirable for operator comfort. Good welds are obtainable with a wide range of humidity (between 10 and 60%).

7.2 Air Filtration

Air filtration shall be the same as used for commercial air conditioning, however inlet and exhaust facilities shall be independent of adjacent shop areas so that oil fumes, vapors and/or air from outside "dirty" areas shall be excluded.

7.3 Room Finishes
Walls and ceilings shall be finished with a dust-resistant finish which is resistant to chipping, flaking, and powdering under abrasion.

7.4 Noise Level
Noise levels shall be such that machinery in adjacent areas do not interfere with normal-level conversations.

7.5 Lighting
Overhead lighting will be of the shadowless type and shall not be below 65 f.c. (foot-candles). Lighting used for welding or assembly of electronic components shall not be lower than 125 f.c. at the level of work. When binoculars are used during welding, the intensity of light at the welding electrodes shall be 150–200 f.c.

7.6 Benches
Welding and/or electronic assembly benches shall be finished with a smooth and preferably oil-resistant finish.

7.7 Work Station Uses
Eating and drinking at work benches designated for welding or electronic assembly shall be prohibited.

7.8 Part Kits
Containers or plastic trays shall be provided for all electronic components and interconnect materials used in 3-D modules.

7.9 Other Operations
Polishing, drilling, grinding, milling, or other dust creating equipment or operations shall be excluded from all welding and/or assembly areas.

7.10 Arrangement
Work benches, office furniture, cabinets, etc., shall be arranged so as to facilitate cleaning of 3-D module welding and assembly areas.

7.11 Encapsulation Area
Encapsulation of welded components shall be done in a separate facility so as to exclude fumes from welding and assembly areas.

7.12 Cleaning Period
Immediate welding and/or assembly areas will be cleaned daily using techniques which minimize raising of dust.

Section 8.0

QUALIFICATION OF MANUFACTURING EQUIPMENT

The equipment needs for manufacture of 3-D welded cordwood modules involves some special equipment but most of the facilities are familiar to the usual electronic manufacturer. The special equipment which has a major bearing on module manufacturing reliability will be discussed. The weld station is the critical item of importance and includes (1) the power supply, (2) the weld leads, (3) the electrode configuration, (4) the wiring, and (5) the actuation system. While the discussion is oriented to capacitor-discharge single-pulse welders no deliberate exclusion of other types is intended and the principles which follow are applicable to all apparatus as well.

8.1 Welding Machine Qualification Test
Each welding machine is accepted only when it passes a simple qualification test.
Requalification of the welding machine is required if the machine is rebuilt or if significant operational changes are made. When the machine has once been qualified, it need not be requalified for future production requirements provided no change in basic parts or range of settings are involved. For the purpose of qualification a power supply alone may be qualified by using a calibrated weld station with the power supply only replaced by the one under test.

8.1.1 Qualification Test. Tests are performed on welding machines to determine satisfactory operation of the machines over the required operating range. Each machine is qualified by the following two tests before any parts or materials are welded for production. Special materials are selected to be used for the test in order to obtain a measurable change in weld strength as a function of machine output variations. Both the lower and upper energy output ranges of the welding machine are used to weld the test material. The selection of materials for this test should be made from combinations which weld in the steep slopes of the weld profile; one combination for the low-energy end and another combination for the high-energy

ITEM NAME: ELECTRODE, WELDING TIP, MOLYBDENUM
BODY MATERIAL: RWMA class 2 copper alloy
TIP MATERIAL: Molybdenum - Molybdenum carbide 90B Rockwell hardness, 31% electrical conductivity
SIZE: Per figure
TYPICAL SOURCE: WELDMATIC DIVISION/UNITEK
950 Royal Oaks Drive
Monrovia, California

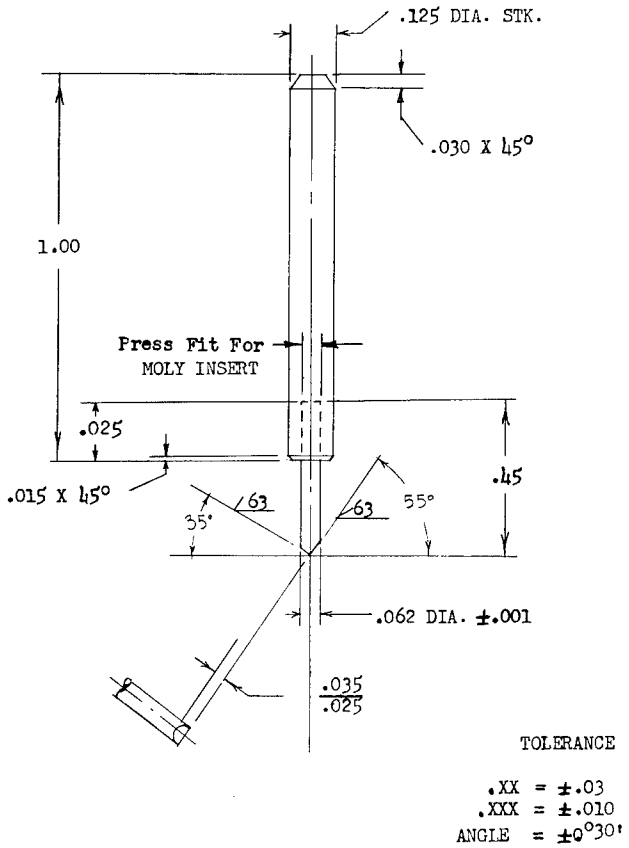


Fig. 8-1. Molybdenum welding tip electrode.

end. One-hundred and eight test specimens of material are welded. Fifty-four test specimens of one material are welded at prescribed nominal settings using the maximum usable energy output range and 54 test specimens of the other material are welded at prescribed nominal settings using the minimum usable energy output range. Fifty test specimens from each group of 54 are torsion-shear tested. The torsion-shear values of the test specimens must exceed the minimum requirements established by weld schedule development.

Four test specimens are taken from each group of 54. The four specimens are then cross-sectioned, polished, and etched as closely as possible through the center of the weld for metallurgical examination of the weld structure and presence of defects, if any. The weld structure under microscopic examination should show evidence of a metallurgical bond.

8.1.2 Test Weld Schedules. Weld schedules shall be developed for the two points for each equipment type in the manner described in 5.0 except the optimizing procedure is changed to obtain a weld point on the linear portion and in the middle of the steep increasing slope so that good transfer is possible between watt-seconds and weld strength. The material used should be checked for consistency and enough

should be on hand and stored for a long period of use so that comparisons between machines will not be dependent upon material variations. Weld schedule proofing shall be performed as in 9.3 except it shall be done on one machine known to be in good calibration. The data obtained from the proofing tests shall be used as acceptance criteria for the new machine. Each weld schedule shall have been developed on the same model machine. Acceptability of the first model of any machine type is based upon its ability to make acceptable welds on production materials described in 5.4.4.

8.1.3 Welding Head Qualification. The welding head is a significant portion of the weld station and must be qualified either as a combination with the associated power supply or separately using a recently calibrated power supply of the size planned for the application. The test welds made in accordance with this section shall meet the same requirements as for a complete combination. The wiring arrangement and electrode configuration is considered part of the weld head for this qualification.

8.2 Electrode Maintenance

Good electrode maintenance is vital to the welding process. The operator must be trained to recognize when cleaning, repositioning, or reshaping is needed.

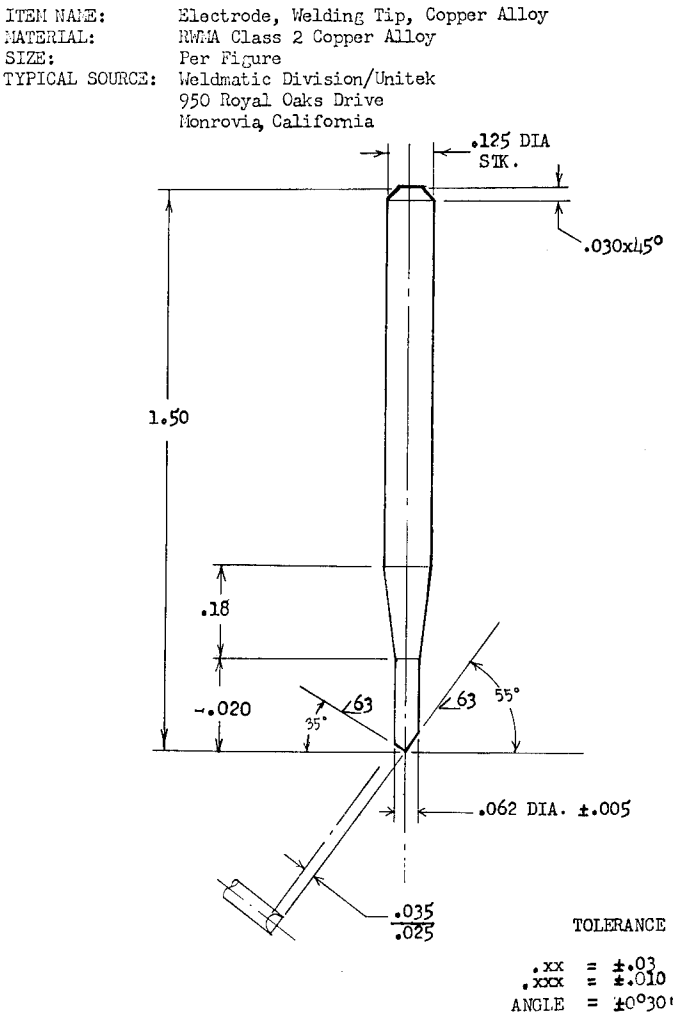


Fig. 8-2. Copper alloy welding tip electrode.

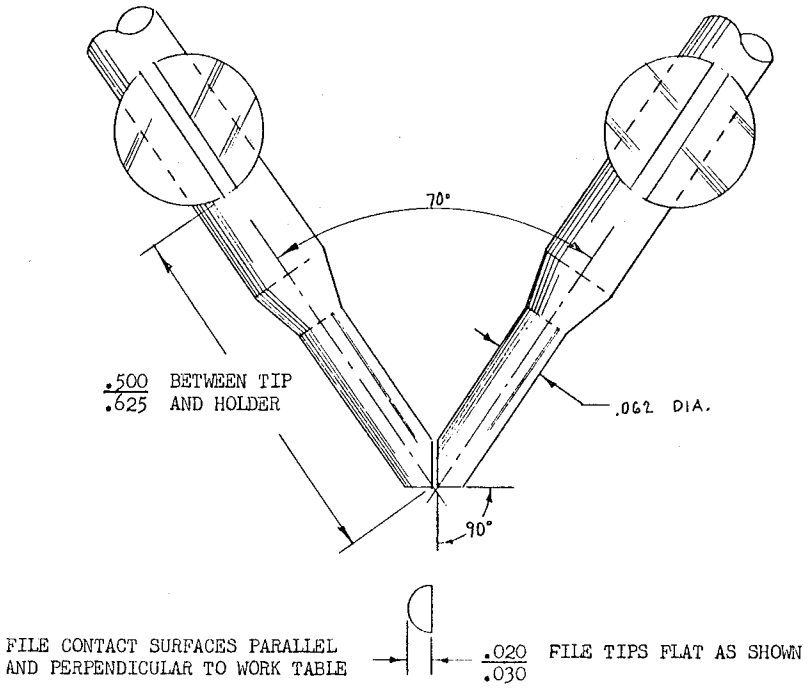


Fig. 8-3. Electrode tip configuration.

8.2.1 Electrode Parameters. The electrode shape, length, material composition, and mounting configuration are all vital to the development of a satisfactory weld. The parameters are largely determined by the type of welding, material combinations and circuit clearances. Once the design of the electronic package is established the electrode parameters may also be established. It is important to the reliability of the weld to hold the electrode parameters constant. One configuration and shape is illustrated in Figs. 8-1, 8-2, and 8-3.

8.2.2 Electrode Cleaning. The operator has the responsibility of maintaining the cleanliness of the electrodes. When the electrodes require cleaning a 600-grit emery cloth is used folded over so that a simple pull through the closed electrodes will clean both at the same time. The actual filing or major maintenance of the electrodes is performed by the setup technician. The operator is required to know when such maintenance is required. The frequency of cleaning is dependent upon the materials welded and the schedule used; however, the frequency is not usually high. Some material combinations, (0.020-in. dumet–solder coated, 0.017-in. Kovar–gold coated, and 0.032-in. copper–solder coated) can be satisfactorily welded for more than 100 cycles without electrode cleaning.

8.3 Weld Station Calibration

Each weld station must be calibrated periodically for the purpose of compensating for normal wear and electrical lifetime. The calibration should be performed on all parts of the weld station which includes the power supply, weld head(s), foot pedal and linkage, electrical wiring, and ancillary station equipment.

8.3.1. Manufacturer's Data. Manufacturer's specifications shall be used as a basis for checking internal parts such as power supply capacitor bank values, relays, output transformers, meters, and rectifier circuits. If the equipment calibration to these requirements has not made good welds as defined by control charts and changes are needed in equipment requirements, the manufacturer should agree to make and guarantee the changes so that future models of the same equipment will not require modifications.

8.3.2 Factory Data. The requirements for the application of conventional equipment such as wiring configuration, shall be specified to completely define the weld station assembly. This specification shall be used for periodic station calibration for the interface requirements.

8.3.3 Log Book. A log book shall be kept to record the calibration times, equipment condition, adjustments made, and hours of operation for each weld station.

Section 9.0

PROCESS CONTROL

Producing welded modules of high reliability requires rigorous manufacturing controls. These controls must be exercised not only in the welding operation, but in every process of manufacturing from the time the component parts are received until their encapsulation in the final module. Five major processes are required to complete a welded module.

1. Kitting
2. Loading
3. Welding
4. Encapsulation
5. Testing

These processes and their controls are detailed below.

9.1 Kitting

All components and materials procured for 3-D welded module application should be issued only in specially prepared kits. Each kit should consist of the exact quantity and type of components and materials necessary for module manufacture. The kits are identified and allocated for a particular scheduled processing line. Supplier lot numbers are correlated with the processing lot kit and recorded. This permits positive identification of all components for history studies.

9.1.1 Electrical Components. Preliminary processing of components are necessary to expedite the welding and loading operations. Such processing includes precutting and straightening leads, intercomponent shielding, and attachment of components to internal heat sinks. The shields and heat sinks become an integral part of the affected components and are placed in the kits as preassembled units. Kitting assumes delivery of all parts prior to assembly and assures proper sequencing of assembly operations. Inspection is facilitated by this method.

9.1.2 Processing of Intraconnection Parts. All circuit bus and jumper wires should be precut and/or preformed for placement in individual module kits. This operation reduces the number of tasks required during welding and aids in preventing bus routing errors. A production aid drawing and/or audio-visual aids can be used to perform this preliminary processing.

9.1.3 Part Arrangement and Identification. Component kits are filled according to a kitting instruction drawing provided for each module design. The kit consists of trays containing compartments which are identified by part name and number. The compartment arrangement is in sequential order of assembly to facilitate the loading process and reduce part placement errors.

9.2 Loading

The assembly of parts into a 3-D cordwood assembly is generally accomplished by inserting the leads of the components into appropriately sized holes in end plate positioners. The requirements for loading are based upon the need to assure correct conditions while the operation is taking place since a loaded module has many visually inaccessible parts.

9.2.1 Fixturing. Holding fixtures for component loading are required to simplify manufacturing and minimize part handling during welding. The fixture provides a means of holding the module positioners while the components are loaded and maintains accurate separation and alignment of positioners. Numerous fixture designs are possible which will satisfy these basic requirements.

9.2.2 Component Location and Orientation. Production aid drawings and/or audio-visual aids should be used to minimize errors in locating and orienting components. The components are taken from their respective location in the kits and sequentially loaded in the fixtures as prescribed by the above aids. The aids used to organize and simplify the loading operation reduce the incidence of error and permit random inspection.

Component polarity is maintained by a graphic symbol adjacent to the appropriate lead hole on the proper positioner. Orientation of lead holes on all nonaxial components (transistors) is controlled by either a lead hold pattern identically representing that of the actual component, graphic indication on the positioner, or variations of lead hole diameters compatible with those of the component leads. Additional control on proper component placement is obtained through factory visual aids provided which indicate pictorially all component locations, methods of placement, and any necessary sequential loading operations.

9.2.3 Positioner Separation. Accurate positioner separation and alignment, maintained by a holding fixture, is necessary for the welding operation to provide a reference plane for locating the interconnecting bus. This also controls the weldment envelope dimensions, which facilitates the encapsulation operation.

9.2.4 Loading Inspection. Inspection of the loading operation consists of checking the work of the operator as well as verifying that the factory aids are in accord with the design requirements. During a production run it is desired to effect nearly 100% inspection of all steps. When the quantity of production permits a measurement of in-process reliability, sampling inspection can be employed. When sampling inspection is employed, the product quality is dependent upon suitable factory aids; these aids must be inspected for conformance to each module design and such aids then constitute a process control.

9.3 Welding

The requirements of the welding operation are readily defined notwithstanding the many factors requiring control. Welding machinery is available from many makers which, when properly used, will yield predictably acceptable joints. The parameters to be controlled and a method of effecting their control are described in this section and in Sections 5 and 8. The individual equipment types selected will necessitate the establishment of the specific values for equipment qualification and calibration. The process controls which follow are independent of welding equipment and are generous enough to allow comfortable manufacturing tolerances and at the same time accurate for the reliability predications and control desired.

9.3.1 Welding Procedure. The correct welding procedure is taught to each operator during the initial training period which each operator must complete prior to doing production work. This training is designed to show the operator the proper equipment setup, the cleaning of electrodes, the proper foot motion for triggering the welder, and the positioning of the components and bus ribbon to be welded. Process Control personnel will assure that the operator is complying with proper methods, as taught in the training program and as specified in Section 10.4.

9.3.2 Electrode Cleaning. Process Control personnel will assure that the electrodes are cleaned and maintained properly. The included angle between electrodes and the flat at the bottom of the electrodes should be checked every four hours, or at the period specified for periodic checking of the weld station as specified below. Process Control personnel at the same time can determine if the electrodes have been receiving adequate cleaning. If deterioration of the electrode is noticeable at this check it is evident that proper care of the electrodes has been neglected.

9.3.3 Weld Process Proofing—Each Weld Schedule. Weld process proofing is the most important step in the welding operation since data are obtained to assure a proper weld schedule, reliability predictions are obtainable, the individual weld station variations, one to the other, are accounted for and control chart data are obtained.

9.3.3.1 *Sample Size*—The proofing tests require a sample size of 775 (5 for metallurgical examination) for a probability estimate of three welds in a thousand outside the minimum stated at 90% confidence. When other probability and confidence limits are desired, a new computation of sample size is necessary. Data obtained during normal production via the control charts may be used to increase the sample size and thus obtain more accurate probability estimates. Such extensions of the process data must not include changes of any kind in the processes which are not included in the acceptable original limits. The procedure for sample size computation is given in the Appendix.

9.3.3.2 *Strength Requirements*—The minimum allowable strength is established by a distribution-free statistical method for precision. The lowest strength in the sample shall be above 50% of $\bar{X}$ chosen in the weld schedule development. If this value is not achievable (1) the weld schedule is not good enough, or (2) the welding process is not acceptable, or (3) the wire combination should not be used.

9.3.3.3 *Selection of Sampling Conditions*—The samples made shall be from the same materials used in the weld schedule development. Alternately separate additional tests on materials variations are necessary to determine changes of $\bar{X}$ which are due to material selection alone. A minimum of three operators on a minimum of three weld stations shall be used with a maximum of stations and operators so that the smallest sample weld lot shall be 50. All sample welds shall be tested on one pull tester all at one time, by one operator and at the same pull test rate used in the weld schedule development.

9.3.3.4 *Computations and Compilation*—For the required sample size the necessary control data shall be recorded or computed, $\bar{X} = \Sigma X/n$, $S = [\Sigma(X_i - \bar{X})^2/(n-1)]^{\frac{1}{2}}$ and $\bar{X}_{\min}$. The value of $X_{\min}$ shall be compared with the requirement 9.3.3.2, and production shall not proceed unless the requirement is met. Each station shall be computed separately in addition to the combined results so that the control chart limits can be established.

9.3.4 Weld Station Control. Each weld station shall have control charts for each operator schedule. These control charts are to be used to monitor the important factors of welding parameters. The frequency of process testing is recommended at each four hours since operator changes and overnight shutdown periods are compatible with this planning. Each schedule used at a particular station must be checked periodically.

If more than one schedule is used they may be rotated for the four hour checks until all are covered in sequence. A sample control chart is supplied for clarity (Fig. A-1).

9.3.4.1 *Control Chart Data*—The data required for the control chart are obtained from the proofing tests. The charts shall have the operators name, the station number (equipment associated), the weld combination, and the appropriate dates. At each test the operator will make five welds. The factors to be controlled are $\bar{X}$, R, and $X_{\min}$. The original limits are to be set up from the weld proofing data, 9.3.3, and will include more variability than should appear at one station. The limits for each station should be recalculated after every 20 groups of 5 welds, for each schedule, to permit the controls to be more sensitive to sudden changes in the process and to suppress long-term changes in the process. A lower limit on $\bar{X}$ is provided for sample sizes of 100 (20 groups of 5) to control this long-term drift. The establishment of the $\bar{X}$ and R control limits are to be established from tabular data and in accordance with accepted procedures (Reference 3). The $X_{\min}$ limit is established by using either 50% at $X_{\min}$ observed in the proofing tests or 5 lb, whichever is higher. This limit is based upon the 3-D cordwood module described in this handbook using common subminiature parts of the 1963 time period. Modules and/or parts which are vastly different and where environmental loads have been determined will justify changes to these limits. The high reliability of the welded joint at least partially depends upon a large (5 ×) safety margin between minimum strength and actual applied loads.

9.3.4.2 *Acceptance Criteria*—The welding process should be stopped, and causes investigated and corrected for any of the following out-of-control conditions: (1) any X_{min} is lower than the chart control limit; (2) any two consecutive $\bar{X}$ plots are out of the control limit; (3) any two consecutive R plots are out of the control limit; (4) any single value of $\bar{X}$ is below 50% of the value of $\bar{X}$ determined in the weld process proofing, 9.3.3. (Note: this $\bar{X}$ includes the expected range of $\bar{X}$ due to full range of lead wire tolerances).

9.3.4.3 *Chart Use*—Each station shall have a chart associated with each operator and weld schedule. The chart shall be kept current by the operator. The welds to be tested shall be made from production material being used and the pull test shall be performed by another person, the same person who performs all the pull tests and on one pull test machine at one pull test rate. The chart shall be readily available for observation by the operator and inspection personnel. The operator shall notify the foreman at the time when any out-of-control conditions occur and request corrective action.

9.3.4.4 *Initial Certification*—The first two groups of five weld samples on all weld schedules, operators, and stations shall be required before the machine–operator–weld schedule combination can be released for production. The first two groups of five shall be made in sequence, but plotted on the chart as two groups. Certification is always required after correction of out-of-control conditions or major revisions to equipment. Fourteen test specimens are required so that four samples may be retained for metallurgical evaluation.

9.4 Encapsulation

Encapsulation of the completed weldment requires a material compatible electrically and chemically with final encapsulation requirements. The compound used must be properly degassed requiring a minimum of postencapsulation degassing to remove any remaining air entrapment except, of course, for foam encapsulants. Molds are designed to afford a minimum of flash and surface deformation to reduce post-molding operations and clean up.

The controls necessary to effect high-quality encapsulation depend upon the material and method of encapsulation. In any case, a process which permits voids or causes large thermal or mechanical stresses during the operation are unacceptable. Control of formulation and curing must be maintained to prevent the occurrence of latent defects.

9.4.1 Mold Preparation. Mold fixtures must be cleaned to remove all foreign matter prior to encapsulating. Appropriate control of this step is needed to ensure surface continuity and obtain required module environmental resistance. After cleaning, the mold inner surfaces are coated with a mold release lubricant to permit removal of the module after curing. This step also aids in maintaining a smooth module surface. Additional improvement in module removal and mold cleaning operations can be attained by coating the mold inner surfaces with Teflon prior to application of a mold release.

If encapsulation shells are used rather than permanent molds, the opposite inner surface preparation is required. In this case, it is desirable to have maximum encapsulant-to-surface adhesion. Therefore, a grease-free rough surface should be obtained in the initial preparation. The use of shells alleviates the need for module surface continuity controls for environmental protection since the shell walls satisfy this requirement.

9.4.2 Encapsulant Preparation. Since the pot life of most encapsulants are for short periods of time, only that amount of material should be mixed which will be used during the time limitation. The mixing operation for most encapsulants is improved by preheating the component parts to the curing temperature or slightly less. This operation should be performed as quickly as possible and any unused mixture should be discarded. After blending of the component parts, the material is evacuated to remove the air entrapped during mixing. This operation aids in eliminating air pockets and surface discontinuities in the completed module.

The preparation of foamed-in-place type resins differs from that of the filled resin materials due to expansion of the material during curing. Since air is necessary for the foaming action, no degassing is required. The extremely short pot life of foaming resins, generally one minute or less, makes it necessary to mix the component parts during the filling operation. This creates more difficult handling and requires more stringent controls to prevent mistakes which could be costly at this stage of manufacture.

9.4.3 Weldment Positioning. Adequate control of weldment positioning in the mold is an important step in the encapsulation process. Poor placement, where clearances between weldment and mold inner surface have been disregarded, could lead to module rejection. Cases where the weldment and mold are in contact result in module surface discontinuities, permitting moisture intrusion and possible loss of environmental integrity.

9.4.4 Filling and Degassing. Careful control of the filling operation is necessary to ensure proper homogeneity and density of the encapsulant. When filled resins are used, the molds and/or shells should be filled slowly with material to avoid air entrapment in the bottom of the mold and intricacies of the weldment. Filling the mold parallel to the positioner boards of a cordwood assembly is preferred since there is less obstruction to material flow in this direction. Further assurance can be gained that no air pockets exist after filling by performing a second degassing operation prior to curing.

Foamed-in-place resins require the use of molds with rigid walls, due to the positive pressures set up during the foaming action. Homogeneity and density control is achieved by providing a relief hold small enough to maintain sufficient pressure (approximately 0.250 diameter). This small relief hole also reduces differential pressures exerted on component bodies located in an area near the relief hole. These differential pressures could cause overstressing of welds and resultant weld failures. Equal pressure distribution and homogeneity can be attained by filling the mold with a predetermined amount of resin and allowing the foaming action and curing to take place with the mold partially sealed. Such a mold must have air leakage

via mold interface mating or small holes of approximately 0.001–0.005 diameter. In this case, pressure and density are functions of the amount of material used.

9.4.5 Curing. One of the basic requirements of encapsulants used in 3-D module manufacturing is that the curing temperature of the material must not exceed the critical temperature of the most heat-sensitive component. Consequently, accurate curing-temperature controls should be used to prevent rejection of completed modules whose components have been affected by overheating.

9.5 Testing

Testing applied to the 3-D welded module is divided into the following categories:

1. Components—upon receiving
2. Components—at or just prior to assembly
3. Module—prior to encapsulation
4. Module—after encapsulation
5. Module—fault isolation

Generally, testing will be on a sampling basis at receiving, and 100% for selected attributes at assembly. All modules will be tested prior to and after encapsulation to detect defects or perform necessary adjustments or tailoring.

9.5.1 Pre-Encapsulation Electrical Test. Based on economics of manufacture, pre-encapsulation testing need not be performed on all modules if sufficient control has been exercised during manufacture. This control can be used as a basis for using statistical sampling techniques per MIL-STD-105A having an acceptable quality level (AQL) in agreement by all concerned.

9.5.2 Post-Encapsulation Electrical Test. Post-encapsulation testing is required on all modules to assure that the design requirements have been met. At this point, before acceptance, some Government agencies may require that the modules be subjected to thermal cycling tests prior to functional testing.

The thermal cycling procedure requires that all modules be exposed to five thermal cycles. Each cycle consists of the following: Starting at room temperature then to −55°C for 10–15 min, then to 85°C for 30 min and back to 25°C. Measurements at room temperature are valid only after stabilization has been achieved.

Section 10.0

QUALITY CONTROL

A few new quality control operations are needed for 3-D welded module manufacturing over the usual requirements for other electronic manufacturing techniques. The most important new subjects are singled out for treatment. The assurance of welding parameters section, Paragraph 10.3, is unique insofar as other industry procedures are concerned. With proper use of the recommended recordings of $\bar{X}$, R, X_{min}, predictions of weld reliability may be improved materially as more data are recorded, and weld processing can be stopped before loss of reliability. The ideal situation is achieved when the manufacturing work, which includes aids and process controls, is giving a product yield which is in accord with predictions and is achieved without applying stringent special controls. The operations described in this section are therefore those deemed necessary to check the compliance of all requirements to their specifications. Sampling should be employed, based upon experience, to reduce inspection time wherever possible and should be continually changed as the needs change. Organization of the Quality Control functions into different areas of interest is desired to provide complete control of manufacturing. A three-level quality control program is recommended where the first level is called self-verification. Self-verification is provided in the 3-D welded module program by using $\bar{X}$, R, X_{min} controls, and other similar controls, as a production tool by production personnel to monitor their own success. The second level is accomplished by inspection personnel who check, test, and monitor production processes. The third level is a review of inspection and processing controls to determine if they are providing an adequate measure of product quality. This level is called Quality Assurance and is the most important since it affects the entire quality control planning.

10.1 Receiving Inspection—Parts and Material

All parts and material should undergo receiving inspection for important attributes on a sampling basis compatible with historical results. This requirement is not peculiar to 3-D welded module production, but some special attributes, such as component lead materials, are of importance.

10.1.1 Mechanical. Mechanical inspection shall be performed to verify part procurement specification. Such specifications which are of particular importance to the 3-D welded electronic parts are:

1. Verification of specified dimensions as described in Paragraph 2
2. Method of vendor packaging (for part protection)
3. Part handling during inspection

Mechanical inspection on parts should include all parts to be used in the module. No special or unusual inspection requirements are needed for mechanical parts.

10.1.2 Electrical. Electrical inspection should be performed to verify the performance of all parts. Replacement of parts in a welded assembly is undesirable; therefore, more emphasis should be placed on

assurance of electrical part and circuit requirements in a 3-D welded module program than other programs. It is therefore advisable to effect 100% inspection on critical electrical attributes at least in the initial lots of parts procured. Transistors are of particular importance since some of the parameters are subject to change in storage. Experience with each test parameter will permit reduction of inspection cost by sampling.

10.1.3 Raw Material. Some raw materials are more important than others because of their effects on a welded module. Bus and jumper material heads the list of importance because the weld reliability is directly related to the material dimension, hardness, and composition. The bus and jumper materials are easier to control than part lead materials and larger quantities can be procured at one time so that high weld consistency can be effected. Sufficient bus material can be procured at one time from one lot to last a long period of time, like a year, for most programs. Inspection of this lot is thus minimized and its use will prevent large variations in welding results due to frequent changes in dimensions, material composition, and condition, regardless of how small they may be. Encapsulation materials in a 3-D welded module program need special controls on some properties not usually critical. Some of these are:

1. Dielectric constant after casting
2. Mixed pouring viscosity
3. Exothermic reaction temperature limits
4. Homogeneity after curing
5. Shelf life
6. Pot life

10.1.4 In-Process Parts. As in any usual manufacturing operation, assembly operations involve the use of raw materials, finished purchased parts, and finished parts and subassemblies manufactured locally. A 3-D welded module employs some parts which are critical, which, when made locally, must be carefully controlled. Positioners, which contain the part location holes and the bus routing design, are most important. The lead holes should be properly identified to the required part, they should be the correct size and they must be located within the drawing tolerance. Overlays are a quick and accurate check on the positioner part. The bus routing can be shown on the overlay, so that all the requirements of the positioner can be checked simultaneously. Other in-plant manufactured items must be properly controlled to be compatible with module requirements specified on drawings.

10.2 Part Location

Part location in a module assembly prior to welding the leads to the busses, is critical because errors are difficult to correct. Patching of busses and rewelding cause unreliability. Controls for assurance of correct part positioning are therefore justified.

10.2.1 Visual Aids *vs.* Design Drawings. Visual aids and/or other instructions normal to the assembly operation should be reviewed to assure that they are complete and in agreement. The part *orientation*, where necessary, is usually more often missed than part *location*. Polarized parts such as diodes and capacitors require control in assembly. Transistors and multileaded parts are of major importance relative to lead position.

10.2.2 Kits. Kits should be checked to assure that they are organized to provide the assemblies with properly oriented and sequenced parts.

10.2.3 Orientation Requirements. The design drawings and the assembly should be compared to assure that *all* orientation and positioning requirements are specified and controlled.

10.2.4 Assembly Orientation and Location. A completed assembly should be examined at least on a sampling basis to assure that the manufacturing processes have resulted in a proper condition prior to welding. If prior controls are adequate, no errors should be found at this step of manufacture; therefore, sampling is recommended. Inspection at the assembly level is costly because of the relative inaccessibility of hidden parts.

10.3 Assurance of Welded Parameters

Welding parameters can be readily controlled and accurate statistical data can be inexpensively acquired. The important and controlling factor is the availability of sufficient lead materials together with their accepted variability. The use of spooled materials in lieu of component leads is unacceptable because of subsequent processing steps applied to the lead wires when applied to components. The following five areas of weld parameter control are considered complete and adequate for maintaining desired reliability at nominal cost.

10.3.1 Development of Weld Schedule. The development of weld schedules requires a set and detailed procedure which Q.C. must assure is being carried out as prescribed. Section 5 on Weld Schedule Development details the requirements which are of importance. Improvements are expected as new controls are exercised and as new developments are available on equipment. As these changes are introduced, they should be readily confirmed by the development of new weld schedules. The most important factor in developing the weld schedule is the selection of the production welding parameters. As stated in Section 5, the best point for production welding is a compromise of the many factors involved—not merely the strongest weld or the least scatter. A review of the choice should be made by Q.C. to assure that the proper trade-offs have been made.

10.3.2 Weld Process Proofing—Each Weld Schedule. The reliable weld does not automatically accrue from the optimization of a number of factors during the schedule development. It is necessary that the schedules be proofed using operation and equipment variations which are normal to the production operations. The *very* high reliability requirements of a joint used in electronic production suggests that a con-

siderable effort be made to measure and record the expected strength and strength variations of each weld and that then they be applied routinely. The proofing tests for any distribution where precise measurements in the tails are required can result in gross errors if the estimation method is not designed for this statistic. Distribution-free methods are precise and even though large sample sizes are needed, the extra complication is more than justified. A discussion on a distribution-free method of estimation is given in the appendix.

10.3.3 Weld Machine Qualification. Qualification of a welding machine is intended for original acceptance; however, a requalification should be performed when major changes have been effected on any set of equipment. Changes of the pulse transformer, capacitor bank, welding head, and firing circuit are considered major for a capacitor-discharge machine. Qualification testing provides a very close check on a machine over its range by special welds; therefore, materials used for the tests should be procured in one lot of sufficient quantity to last years and when new material is procured, it should be compared with the old material in one test lot. The qualification procedure is given in Section 8; the inspector should assure that the test is performed on each machine and that the results are acceptable.

10.3.4 Welding Station Calibration. The station calibration constitutes a check of each of the specified factors of the welding and weld position equipment. The calibration of electrical parts is done via conventional test equipment, while some special gages may be required for mechanical tests. The purpose of this test is to assure that all parts, meters, and equipment are within the manufacturers and/or users requirements. Details of this test are given in Section 8.

10.3.5 Weld Station Control. A continuous measurement of each weld station is desired to permit revisions to the production work station as early in the out-of-tolerance condition as can be detected. A control chart which has measurements and limits for $\bar{X}$, R, and X_{min} provides an inexpensive and suitable control method. The operator becomes a part of the system and each combination of operator, machine, and material requires a separate recording chart. The control system is detailed in Section 9.

10.3.5.1 *Weld Station Certification*—It is desired to prevent starting on production welding if the station does not have an initial agreement with the prescribed control; therefore, the first two sets of five welds are classed as weld certification. The inspector should assure that the certification tests have been run and that they are acceptable for each schedule, station, and operator. This procedure is detailed in Section 9.

10.4 Operator Qualification

The welding operation is not difficult nor does it require extensive special training. The operator effects are noticeable and important in the module weldment quality. To maintain high quality standards, operator training and monitoring is needed. The welding operation is the most important, but other operations require training and control as well.

10.4.1 Prior Training. The inspector should assure that all operators have had prior training and that their proficiency is acceptable.

10.4.2 Periodic Verification. The operator should occasionally be provided with new information and given an opportunity to discuss problems associated with the operation. New equipment and procedures which are expected to be introduced should be taught and a recheck of operator proficiency should prevent a gradual decay of high-quality work.

10.4.3 Control Chart Comparisons. A review of the control charts at each station will also indicate the operator characteristics of interest and *may* be a measure of operator proficiency.

10.4.4 Operator Characteristics. The following operator characteristics are either "must know" or "nice to know" specifically needed for the welding operator. Other usual characteristics for electronic production workers are necessary but not detailed.

A. Must know how to read and understand manufacturing instructions via verbal and audio-visual aids.
B. Must know welding equipment used and settings permitted.
C. Must know 3-D welded module manufacturing techniques.
D. Must know electrode maintenance requirements.
E. Must know about and understand the use of process controls, such as $\bar{X}$, R, and X_{min} charts.
F. Must know and recognize welding and polarity requirements.
G. Nice to know how to read and interpret color codes on electronic parts.
H. Nice to know how to read and interpret electronic part polarity markings.
J. Nice to know and recognize electronic parts by name; i.e., resistor, capacitor, transistor, diode, etc.

10.5 Visual Inspection

Visual inspection of each weld is not recommended because a good weld cannot be separated from a bad weld by visual criteria. It is also not economically advisable to commit the large inspection time necessary to quantitatively examine each weld made. Visual inspection is necessary on a sampling basis to assure that the processing procedures and controls are providing the desired results. The following items can be checked visually and are indicative of weldment quality. Inspection of weldments should be made at magnifications in the range of 10 to 20.

10.5.1 Missed Weld. A missed weld may result from omission altogether by an operator or by a power supply misfire. Some lead deformation may be evident on a misfire while no deformation is associated with an omission. In either case the inspector must ascertain whether the two pieces are attached, which *may* require light pressure on the lead wire or bus.

10.5.2 Incorrect Interface Area. A simple visual check of a weldment will reveal any welds made where the lead or bus is too short to fully overlap another. Weld energy is carefully determined for each weld combination via the weld schedule development and is directly related to the volume of material between the electrodes as well as the area of contact. Any changes in volume of material to be welded, such as insufficient material overlap, will cause weak or broken welds.

10.5.3 Misalignment. Any misalignment will degrade the weld; most misalignment can readily be seen under the specified magnification. Misalignment of electrode tips causes nonuniform lead deformation with some sharp discontinuities where lap welds are made in a bus; misalignment has the same effect as in 10.5.2 above. The degree of misalignment tolerated is difficult to specify for quantitatively; however, the conditions which are usually typical of joints made for proofing tests and weld schedule development should be used for comparisons.

10.5.4 Angularity Requirements. The joints within a module weldment should be either right angles or parallel. If other angles of joining are ever to be required, separate weld schedules are needed for each such special case. Weld schedules and proofing tests are conducted requiring a $\pm 10°$ tolerance on angularity, which requires that the same tolerance be maintained for production joints if the reliability estimates are to be precise. Overlap tolerances of parallel welds should be $\pm 10\%$ for equivalent control of these welds unless the weld schedule and proofing tests were done with wider tolerances.

10.5.5 Bus Installation. The bus installation should be welded in place so that the sequence does not result in residual stresses. Improper installation is evident by bent component leads and bowed bussing where three or more welds are in straight sequence.

10.5.6 General Appearance. Generalizations about the appearance of weld conditions cannot be made because each weld combination is different. Standards about deformation are impractical because the only important condition is the strength achievement. Comparisons of welds with pictures and conditions established in the weld schedule development are useful in judging and resolving welding problems. Comparisons can be made on expulsion, splatter, gas holes, discoloration due to overheating, and others to aid in trouble detection, rather than for rejection.

10.6 Conductor Clearance

The clearances of conductors within a welded module are usually for very low voltages, where any clearance at all is sufficient. The design drawings should specify where clearances are critical, otherwise precise matching of patterns on the positioners and similar aids are not necessary.

10.6.1 Clearance for Welding. Clearance for welding is based upon the bus size and the electrode size and mounting configuration, which requires each production arrangement to be treated separately. Where electrodes are as described in Section 8 (Electrode Maintenance) a 0.050-in. clearance is desired with a possible 0.030-in. if absolutely necessary. Clearance for welding can be obtained by sequencing the welding so that the weld is in the clear until another bus is applied.

10.6.2 Clearance Between Conductors. Design drawings should indicate areas where clearances are critical, but electrical clearance for insulation is of *least* concern. High-frequency high-gain circuits are subject to capacitive feedback when long runs are close together and very close conductors are hard to handle in manufacturing so that guarantees against shorting due to handling and potting can be made.

10.6.3 Clearance Between Conductor and Encapsulation. A cordwood module is encapsulated for several reasons, but one of the most important reasons is to protect the electronics from external environments, like moisture and atmospheric contamination. Clearance is required to assure that the leads or the bus do not break through the encapsulation or are not potentially apt to break through during service. A normal 0.030-in. clearance between the nearest projection and the encapsulation outline is necessary for this purpose. The inspector must assure that the encapsulation process provides centering in the mold so that the clearance specified is maintained; however, since measurements are impossible after potting the emphasis is on the process of molding.

10.6.4 Internal Clearances. The inspector must assure that the completed weldment does not have lead-to-lead and lead-to-case shorts in the assembly of components between the positioners. Transistor cases particularly are responsible for interference since all leads are usually on one side, and the case position is thus not accurately located unless it is flat against the positioners. Other interference conditions should be watched, such as crimps on component leads when they are employed. The crimps can touch each other on adjacent leads if the lead rotation is not controlled. Heat sink rods and inserts when used are also a source of shorting.

10.7 Pre-Encapsulation Test

The pre-encapsulation test may be on a sampling basis after the particular design has been proved in production. There is no particular need for pre-encapsulation tests unless there is a high incident of electrical failure after potting.

10.7.1 Continuity and Part Check. A brief and standardized test (not functional) is suitable to assure that all connections have been made, that the parts are workable and properly oriented, and that no shorts exist. Functional testing of the module is not desired at this point since many circuits will be changed by the encapsulation process. Excess electrical leakage in transistors and in wiring should be detected.

10.7.2 Application of Selected Parts. When required for the application of a part for final circuit adjustment, it will be necessary to perform a complete electrical test, and sampling can never be applied. In these cases the tests are more a part of the manufacturing operation than a quality check; however, the checking of electrical performance is simultaneously verified and no special additional quality control electrical checks are needed or desired.

10.8 Module Encapsulation

The completed and encapsulated module should be inspected on a sampling basis to assure that the purposes of encapsulation have been met. The dimensions of a module are deliberately noncritical since the application does not depend upon final dimensions. A few items of importance to the technique are described and should be checked.

10.8.1 Dimensions. Even though the dimensions are noncritical a check must be made to assure that the modules will fit in place and that header pin locations are correct. Where insert mounting is used a check should be made to assure its size and location.

10.8.2 Encapsulation. The encapsulation condition should be checked to assure that there are no bubbles or air holes which penetrate to internal parts, and that there is no evidence of voids as may be observed from the surfaces. The terminations should be free of flash and adjustment points should be clean and free-moving. Special boards for headers, test points, adjustable components, and shields should adhere well to the encapsulant without evidence of separation. The encapsulant should fill properly around mounting inserts, if any, and other mechanical pieces designed to extend through the potting. Shielding boards and thermal flow surfaces are examples of special mechanical parts requiring inspection.

10.8.3 Identification. The module must be identified and the inspector must verify that identification is correct. There are many different circuits encapsulated in the same mold with the same header pattern resulting in loss of identity by visual or sometimes electrical means.

10.8.4 Material. An assurance that the specified material was used is necessary. Variations of potting materials will frequently cause material changes in electrical performance.

10.9 Post-Encapsulation Electrical Test

The final point of acceptance of a module is at its testing. Frequently modules are delivered to the customer from this point. There is very little that can be done to the module at this point other than to accept or reject it. Unacceptable modules *may* be repaired and reprocessed, but any repairs will lower the reliability. Frequently the cost of repairs exceeds the cost of the module, thus justifying a throw-away philosophy.

10.9.1 Electrical Performance. The desired performance specified should be tested at this level rather than abbreviated tests for continuity. Extensive testing is not required except on a sampling basis, where the module should be tested over its full environmental range.

10.9.2 Setting of Adjustments. Where adjustments are provided they must either be set finally, as designed, at this final test or set to a test value to permit module testing. Usually adjustments are provided for matching with other modules in a system and in these cases it may be necessary to check the range of adjustment.

APPENDIX A

MINIMUM STRENGTH AND DISTRIBUTION-FREE METHOD

The only requirement for welded joints is that they not break (weld joint resistance is negligible compared to lead resistance) under specified environments. As a result, a minimum desired strength is the most realistic requirement for any proposed material combination and weld schedule. The object of any testing program for a given schedule is to predict the percentage of the parent population that will be below the minimum strength. Since weld reliability requirements are high, this entails predicting far out on the lower tail of the probability density function of the weld joint pull strengths. However, it is precisely in this area that "fitted" distributions are least accurate. A "fitted" distribution can be seriously in error out on the tails even though it passes a "goodness to fit" test at a high significance level.

The uncertainty associated with "goodness to fit" tests is caused by controlling only one error (the probability of making a wrong decision if the actual distribution is different from the "fitted" distribution) whereas, the error that is really of concern (the probability of making a wrong decision if the actual distribution is different from the "fitted" distribution) is dependent on the actual distribution and is, in principle, unobtainable. One way around this difficulty is to consider only distribution-free estimates of the percentage points of the true population. The error in these estimates is given by the confidence level and at, say, the 90% confidence level, the probability (fiducial) that the true population percentile is less than the estimate (lower 90% confidence limit) is *exactly* 0.10. This assurance of an exact error more than compensates for the drawbacks inherent in the method. One drawback is that large sample sizes are required to meet high reliability requirements. This is not serious since large sample sizes are obtainable. Another drawback is that estimates are only available at specific points that are not determinable in advance, i.e., the points (pull strengths) where breaks actually occur in the sample. Provided that this fact is considered in specifying weld strength requirements, it is also of minor importance.

Adoption of distribution-free estimates does not mean that other criteria are not useful. For example, statistical control is necessary in order to predict population parameters from sample characteristics. Standard criteria (e.g., $\bar{X}$, R control charts, see Fig. A-1) can be used to provide assurance that the welding process is in control.

An example of the distribution-free estimates of the population percentiles is as follows:

With a sample size n, let y_i represent the breaking load of the ith member of the sample. Then order the sample from smallest to largest and relabel the members from X_1 to X_n so that $X_1 \leq X_2 \leq X_3 \leq \cdots$

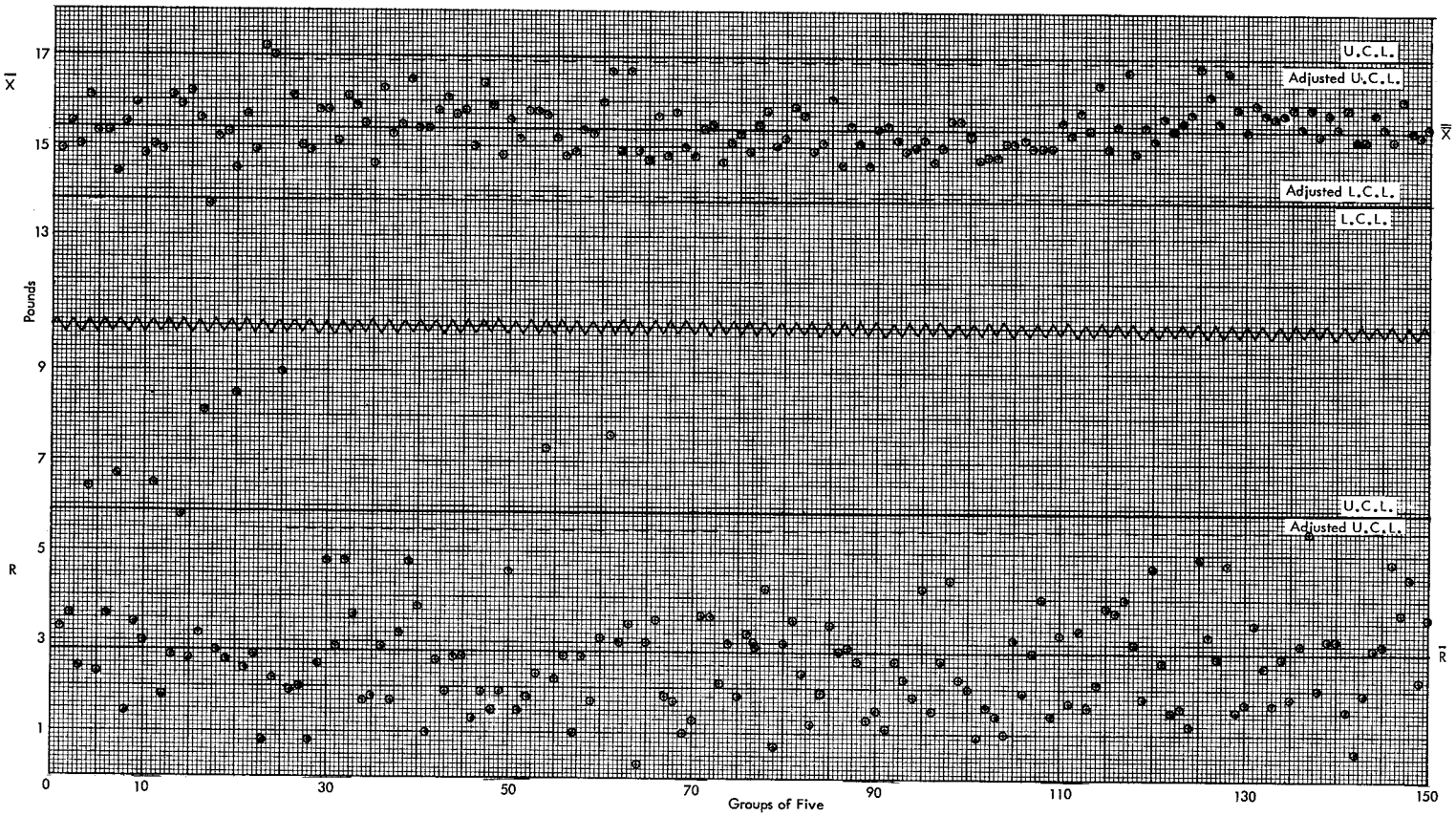


Fig. A-1. $\bar{X}$, R control chart for 0.020 solder-coated dumet welds.

$\leq X_n$. Call R_p the point in the parent population which cuts off p of the population on the lower tail (e.g., if $p = 0.003$ then 3/1000 of the population is less than $R_{0.003}$). Then

$$P(X_r < R_p) = \sum_{i=r}^{n} \binom{n}{i} p^i (1 - p)^{n-i}$$

where $\binom{n}{i}$ is the binominal coefficient, n things taken i at a time.

$P(X_r < R_p)$ is set equal to the desired confidence level. Given X_r and either n or p the equation can be solved for the remaining parameter.

In particular, if an estimate is desired at the lowest break strength X_1, at a confidence level of, say, 0.9, then,

$$P(X_1 < R_p) = \sum_{i=1}^{n} \binom{n}{i} p^i (1 - p)^{n-1} = 0.9$$

If, in addition, p is fixed and equal to, say, 0.003 (3 out of 1000) then,

$$P(X_1 < R_{0.003}) = \sum_{i=1}^{n} \binom{n}{i} (0.003)^i (0.997)^{n-i} = 0.9$$

and solving for n, $n \cong 770$.

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The Encapsulation of Electronic Components by Electron Beam Welding

F. R. SCHOLLHAMMER
Hamilton Standard Division, United Aircraft Corporation, Windsor Locks, Connecticut

The general characteristics and advantages of electron beam welding for electronic package encapsulation are outlined. Specific applications of this welding technique are discussed in some detail under three general headings; namely, Welded Relays, Encapsulation of Functional Electronic Blocks, and Packaging of Microminiature Modules.

INTRODUCTION

WITH THE DEVELOPMENT of more sophisticated electronic equipment, industry requires smaller electronic packages which maintain a high degree of reliability. This reliability can be achieved only with adequate encapsulation. Electron beam welding provides a packaging method which ensures a high confidence factor in producing optimum encapsulations since dielectric changes are minimized and the use of potting compounds can be eliminated. This method of welding has been demonstrated to be well suited for the encapsulation of electronic packages ranging in size from large relay modules to functional electronic blocks. Recent advancement in electron optical systems have permitted the development of unique electron beam techniques applicable to component encapsulation. For example:

1. Minimum heat input is required during welding. Electron beam spot sizes are so small and power density (W/in.^{2}) is so high that local fusion of materials is effected without significant heat transfer to adjacent components; in other words, welds are made with a low total thermal energy input.
2. Electron beam welding requires neither fluxes nor filler materials; consequently, corrosion and contamination caused by these materials are eliminated.
3. Electron beam welding is easily and precisely controlled. It readily lends itself to automation and the welding of components in production at an economical rate.
4. Since the electron beam welding process takes place in a vacuum chamber, a vacuum within the component module is produced.
5. As the electron beam process is not sensitive to surface irregularities and nominal material impurities, a welded joint having vacuum melted material qualities is obtained. The strength of the electron beam welded assembly provides a high resistance to vibrational stress and fatigue damage.
6. The use of potting material may not be necessary since a hermetic quality weld can be produced. This permits the design of a lightweight package, and also minimizes corrosion from entrapment of water vapor.
7. Components in an electronic package can be outgassed, vacuum dried, baked, welded, and then backfilled with an inert gas to minimize possible dielectric changes within the internal circuitry. All of the above operations can be completed in the same chamber with the electron beam weld process.

The sealing processes and techniques which will be described in this paper are directly applicable to the electronics industry.

DESCRIPTION OF EQUIPMENT

The system used for electron beam welding is illustrated by the schematic diagram shown in Fig. 1. The electron beam is formed by a triode electron gun. This gun consists of an electron-emitting hot tungsten filament (cathode) maintained at a high negative potential, a grid cup negatively biased with respect to the filament, and an anode at ground potential with an aperture in the center through which the highly accelerated electrons pass. By varying the negative bias potential applied to the grid cup, it is possible to control the flow of electrons (beam current) and also to turn the beam on and off. The shape of the electrostatic field formed by the grid cup is such as to direct the electrons into a converging beam. A variable strength electromagnetic lens is used to focus the beam to the desired diameter at the precise location required on the workpiece.

The magnetic deflection coil, mounted directly below the magnetic lens, is used to direct the beam over the surface of the work as desired. The deflection system permits the programming of the beam over specific regular or irregular geometric patterns.

Beam focusing is precisely controlled through the use of visual optics. The weld location is obtained by control of a precision table. These optics are designed so that the workpiece is viewed coaxially with the electron beam at magnifications of $20\times$ or $40\times$. This permits the accurate location of the beam impact point prior to welding, and viewing of the electron beam process as it occurs. In addition, the optical viewing system can be employed to inspect the workpiece before or after welding.

Generation and transmission of the electron beam takes place in the collision-free environment afforded by a high vacuum. Therefore, it is necessary that the work chamber, electron optical column, and vacuum pumping system be integrated to provide operation at vacuum levels of at least 10^{-4} mm Hg. An electron beam welding machine meeting these design requirements is shown in Fig. 2.

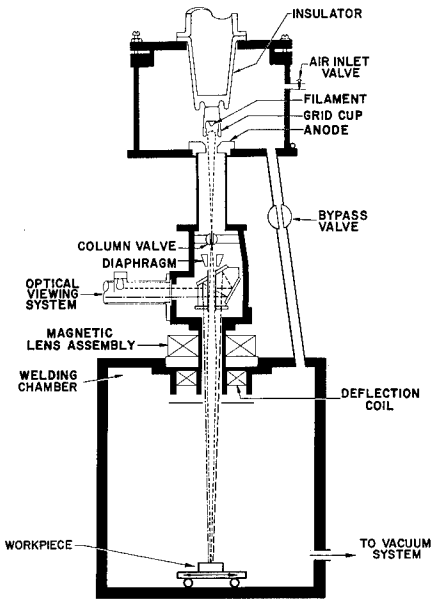

Fig. 1. Electron beam welding machine schematic.

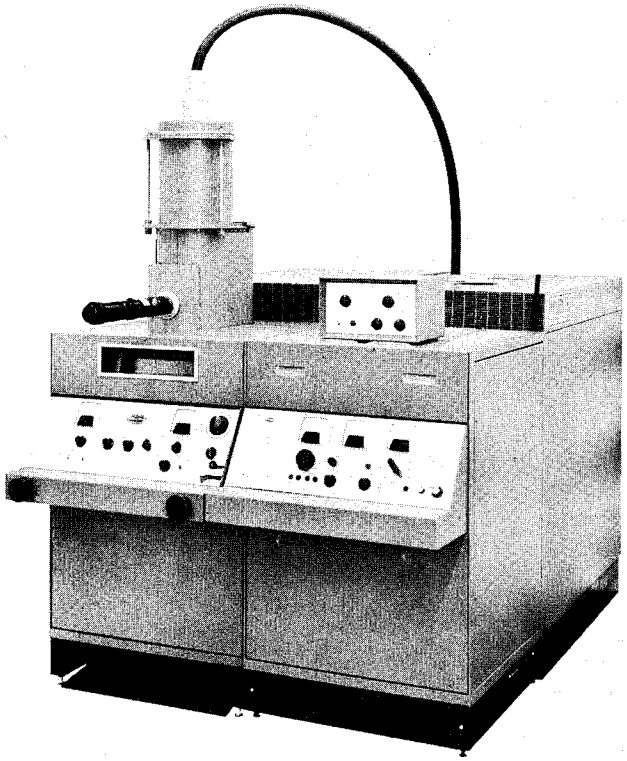

Fig. 2. Hamilton–Zeiss electron beam welding machine.

WELDED ELECTRONIC PACKAGES

Electronic packages which are fabricated from standard components, microminiaturized discrete elements, or solid-state devices, require packaging techniques that will provide high production rates and still maintain product reliability. With the present methods of encapsulation (soldering, conventional welding, bonding by the use of epoxy cements, etc.) a high quality hermetically sealed package is difficult to achieve. With the use of electron beam welding, Hamilton Standard has developed an encapsulation process which meets these design and production objectives. Several specific examples of unique encapsulations and techniques used are described as follows:

Welded Relays

A practical application of electron beam encapsulation is shown in Fig. 3. The 1.5-in. square relay was electron beam welded without distortion of the component, damage to the internal components themselves, or to the organic filler located immediately adjacent to the weld zone. This example illustrates the precise position and heat input controls that can be maintained during the welding operation. Dimensional measurements of the three axes of the module made before and after welding indicated no significant changes. The welding operation was accomplished by rotating the assembly for one complete revolution at a peripheral welding speed of 30 in./min. A fixed focus point beam was used, even though the part was rotated during welding. This illustrated beam depth-of-field and noncritical nature of exact focus. A helium-tight seal was achieved.

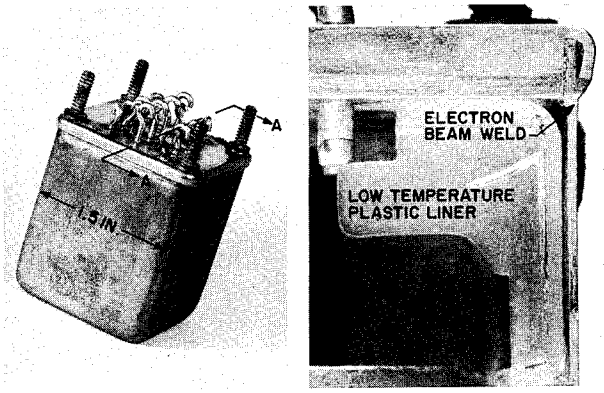

Fig. 3. Electron beam welded relay.

Another practical application of electron beam encapsulation is shown in Fig. 4. This precision relay is used in critical military equipment and requires a welded assembly void of flux residues which may cause deterioration of internal components, outgassing, and subsequent changes to the dielectric properties of the switch itself. Specifically, this application included:

1. Welding the cupro nickel housings to the carbon steel header by programming the electron beam around the rectangular seam.
2. Obtaining a high-quality hermetic seal with a leakage rate of less than 10^{-8} cc/sec (0.00097 μft^3/hr).
3. Preserving the required resistance (1000 V DC) between each pin and the header by preventing metallic deposition on the glass insulators.
4. Determining if the welding operation will affect the relay's electrical performance. This was the primary consideration of the welding work. The procedure used to complete the above was as follows:

Test units equipped with a copper-header vapor shield were welded by a pulsed beam operating at 100 kV, 0.5 mA (pulsing value), 2.1-msec pulse width, and 300-cps pulse frequency. The shield illustrated in Fig. 5 was used to maintain a high dielectric value between the glass

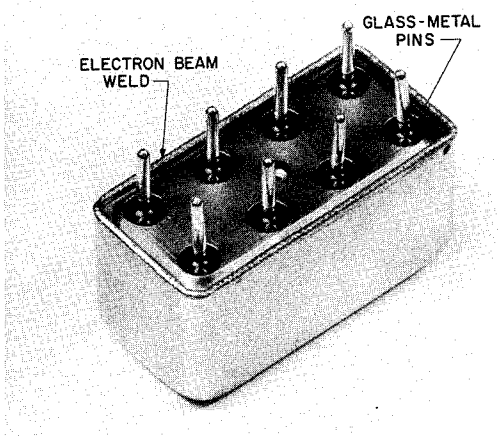

Fig. 4. High precision all-welded relay.

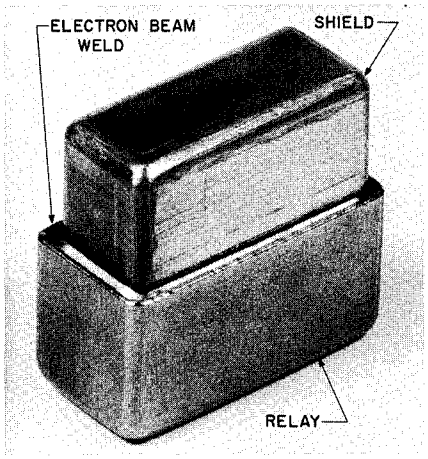

Fig. 5. Relay and deposition shield assembly.

sealed pin and cover assembly. Resistance measurements made between each pin and the housing with a 1000-V DC Megger meter both before and after welding, confirmed that infinite resistance was consistently achieved. When the assembly was welded without the shield, a light cleaning of the glass pin assembly was usually required to restore the required dielectric specification value. Hermetic testing of these same units with a helium mass spectrometer revealed that a percentage of units had leakage rates less than the customer's goal of 10^{-8} cc/sec. Fifty relay assemblies were then numbered with an ink marker, functionally checked on an electric check-out rig, and welded per above. After welding, each relay was again functionally checked and its leakage rate determined. Any relay which tested at zero on the mass spectrometer was interpreted as having less than the calibrator leakage rate of 0.0042 μft^3/hr. The results obtained from this welding application were as are given below.

Visual examination of the welds revealed the normal uniform bead commonly associated with the Hamilton–Zeiss electron beam process. A micrograph of the weld joint is shown in Fig. 6. The relay having a flange with 0.020-in.-wide V (located within 0.020 in. of the hermetic glass seals) was welded to a control depth of 0.015 in. The relays were determined by bench

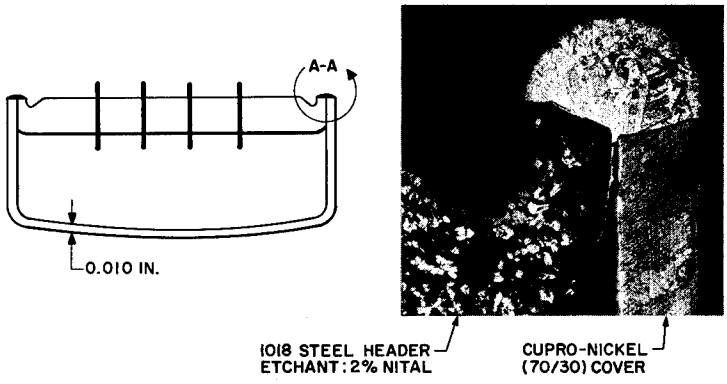

Fig. 6. Micrograph of relay cover welded to header assembly.

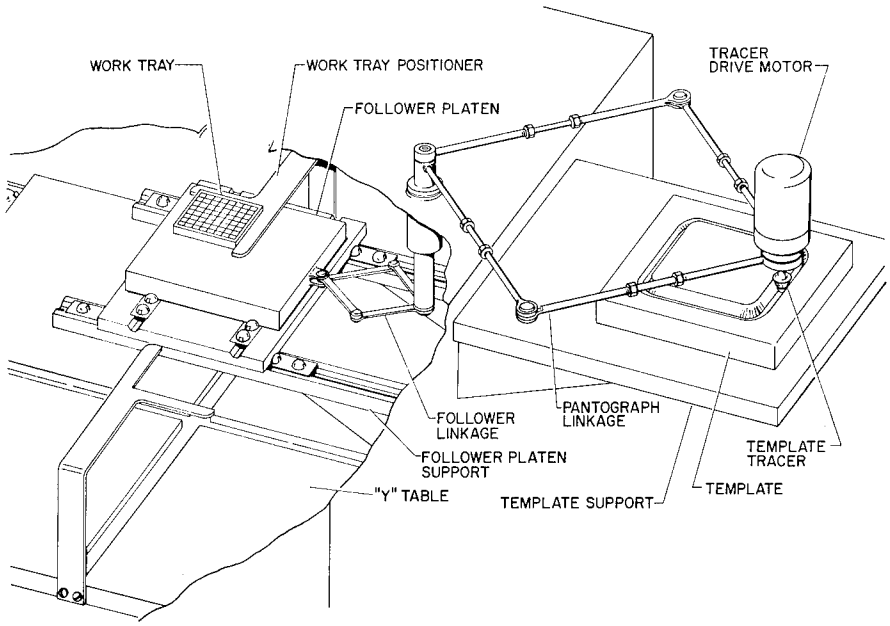

Fig. 7. Programming mechanism for relay housing welding.

test to function properly and to be well within the acceptable limits of operation. A high-quality hermetic seal, as obtained for the above test samples, was also demonstrated with the actual production relay assemblies.

With the successful welding process described above and with the use of a mechanical programming system, schematically shown in Fig. 7, a high production rate can be achieved. Several hundred relays can be positioned and processed from a loading hopper adjoining the vacuum chamber during one vacuum cycle. By use of this programming system, each of the above relays can be welded in a period of less than 3 sec. With additional refinements, a higher production weld rate could be realized. A design cost study of a relay similar to that iliustrated in Fig. 3 has indicated that a complete electron beam welding operation can effect considerable cost savings as compared to the present production fabrication technique.

In the event added structural integrity is required for high vibratory or shock loads, electron beam spot welds can be made through the cover to the relay frame assembly. Figure 8 indicates some of the structural reinforcement welds that have been completed on a typical relay assembly. These were completed by the operation of the beam in a pulsing mode at 1 cps, a pulse duration of approximately 17 msec, and a heat input of only 3.8 W/sec.

Figure 9 shows another example of a high-temperature switch which was electron beam welded without damage to the internal components or glass hermetic seals. Hundreds of these switches, which are used in high-performance aircraft have been successfully processed. Switches welded by the electron beam have successfully passed the required hermeticity leakage standards of 10^{-8} cc/sec and a dielectric test of 1000 V when applied between the external pins and header-case assembly. Table I lists the energy inputs to complete the welds of this switch and other similar applications described in this paper.

Typical Electron Beam Weld Energy Inputs

Configuration	Material	Kilovolts	Milliamperes	Watt-Seconds	Comments
1.5 × 1.5 × 1.75 in. (Fig. 3)	Cold-rolled to cold-rolled (~0.025 in.)	70	1.6	1345 (for complete assembly)	Continuous beam, welded at 5 rpm (30 in./min) with 0.015-in.-diameter circular deflected beam
$\frac{3}{8} \times \frac{3}{4} \times \frac{2}{5}$ in. (Fig. 4)	Cupronickel (0.010 in.) housing to carbon steel header	100	0.5 (pulsed at 2.1 msec and 330 cps)	33.0	45 in./min
$\frac{3}{8} \times \frac{3}{4} \times \frac{2}{5}$ in. (Fig. 4)	Steel 0.010 in. cover to cold-rolled steel header	60	1.0	180.0 (for complete assembly)	Continuous beam, 50 in./min with 0.015-in.-diameter steady-state beam
$\frac{3}{4} \times \frac{45}{64} \times \frac{23}{64}$ in. (Fig. 9)	17-7 pH Cover to cold-rolled header (~0.015 in.)	60	1.0	200 (for complete assembly)	Continuous beam, 27 in./min (focused)
Relay spot welds (Fig. 8)	0.010 in. Cupronickel to S.S.	80	1.4 (pulsed at 17 msec and 1 cps)	3.8	Approximately 2 pulses required per weld
FEB package 0.37 × 0.37 × 0.038 in. (Fig. 10)	Kovar to Kovar (0.004 in.)	50	0.2 (pulsed at 0.5 msec and 100 cps)	0.5	10 in./min with 0.010 in. diameter beam
Module—Circular (~0.75 in. diameter × 0.5 in.) (Fig. 11)	Nickel to steel	90	2.0	1550 (for complete assembly)	7 rpm at 0.75 in. radius (16.5 in./min)
Solid-state receptacle (~0.12 × 0.25 × 0.35 in.) (Fig. 12)	Kovar to Kovar (0.003 in.)	90	0.010	15 (for complete assembly)	27 in./min
2.2 × 0.65 × 0.95 in. (Fig. 13)	0.015 in. cold-rolled to cold-rolled header	90	0.40	504 (for complete assembly)	27 in./min
$\frac{1}{2} \times \frac{3}{4}$ × 0.7 in. Cordwood (Fig. 15)	Copper, nickel leads (~0.025 in. diameter) to 0.002 in. Ni on Al_2O_3	90	0.15 (pulsed for 100 msec)	1.35 (per lead)	
Glass-epoxy substrates (Fig. 17)	0.023-in.-diameter copper leads to copper plate (0.003 in.)	70	1.2 (pulsed for 15 msec)	1.26 (per lead)	
Nickel-plated (0.0025 in.) Al_2O_3 wafers (Fig. 20)	Nickel plate to nickel plate (0.0025 in.)	100	0.7–1.2	222 (per linear inch)	27 in./min

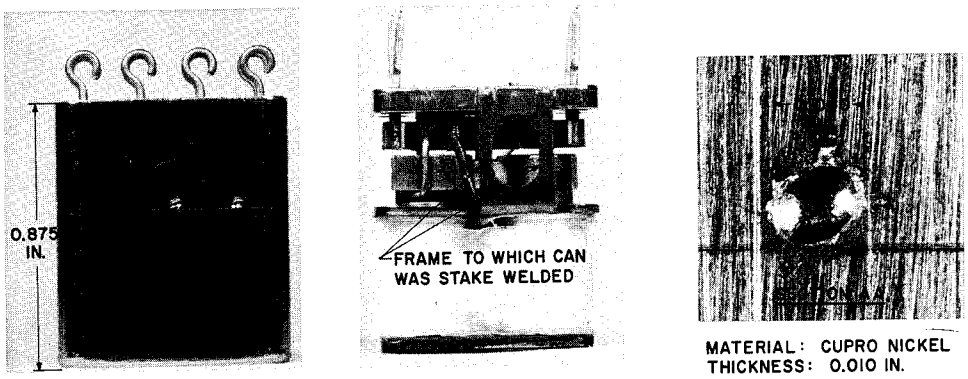

Fig. 8. Stake-welded relay modules.

Encapsulation of Functional Electronic Blocks

As a demonstration of the practicability of using electron beam welding techniques to assemble functional electronic blocks, several specific tests were conducted at Hamilton Standard utilizing standard Hamilton–Zeiss equipment.

A typical functional electronic block which was hermetically sealed by electron beam welding is shown in Fig. 10. The basic block consists of a borosilicate and Kovar laminate. A 0.002-in. Kovar cover was electron beam welded to the 0.002-in. Kovar peripheral rim, which had previously been bonded to the borosilicate basic block assembly. In order to obtain a hermetic joint, the electron beam was pulsed at a high frequency to minimize heat input to the block assembly during the welding operation. Hermeticity of the functional electronic

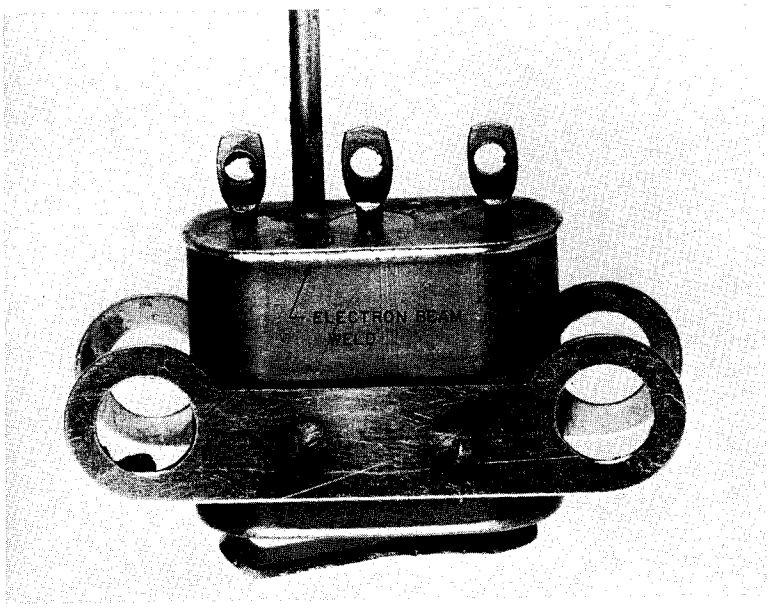

Fig. 9. Electron beam welded high-temperature switch.

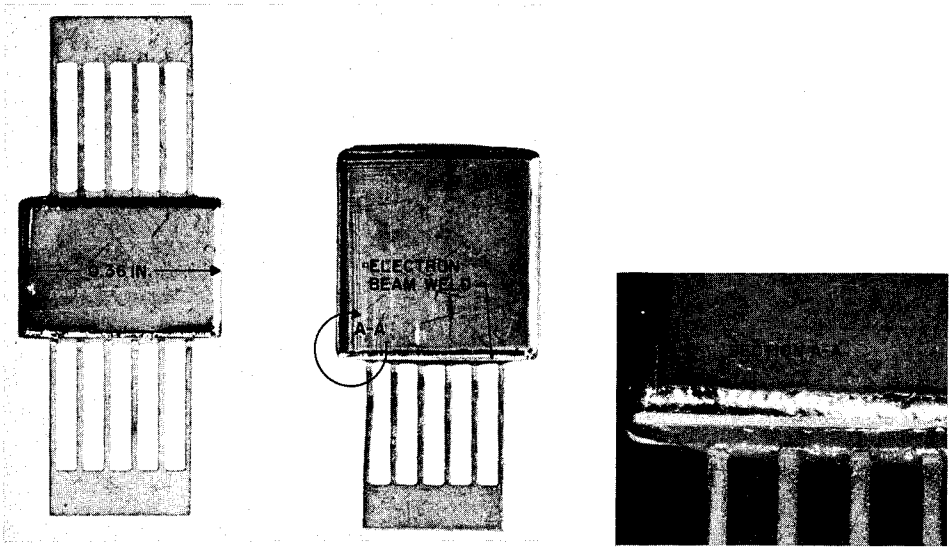

Fig. 10. FEB packages hermetically sealed by electron beam welding.

block was verified by pressurizing the block assembly to approximately 20 psig; the block assembly was then removed from the pressurized helium atmosphere and tested in a bell jar for helium leakage. No leakage at a sensitivity of less than 10^{-8} cc/sec, or 0.3 cc/year was indicated from the specimens tested.

Figure 11 illustrates the hermetic encapsulation of the unit containing solid-state circuitry. Previous methods of sealing the outer canister to the base header by epoxy cements did not prove satisfactory. Organic adhesives age and permit backstreaming of ambient gases, thus subjecting the solid-state components to corrosion, particularly the bismuth–antimony sensing terminals. Temperature measurements made on the cover of the functional electronic block package indicated an overall unit temperature less than the prebaking temperature of 250°F (which occasionally heat-damaged some of the critical circuitry). The maximum temperature recorded on the canister from the electron beam process was 270°F, extending only to a distance

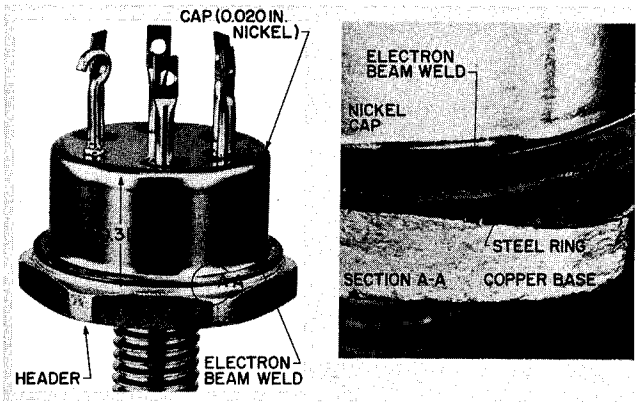

Fig. 11. Solid-state package hermetically sealed by electron beam welding.

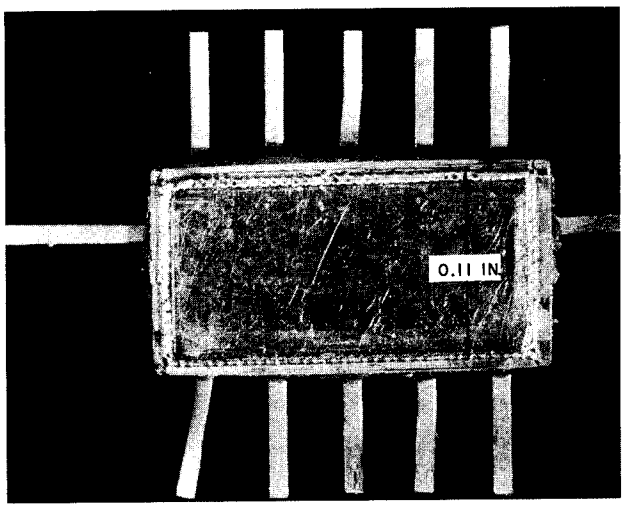

Fig. 12. Typical electron beam welds on FEB packages.

of 0.020–0.030 in. away from the weld beam proper. The width of the weld bead was estimated to be approximately 0.015 in.

Figure 12 shows a miniature 0.003-in.-thick Kovar cover welded onto a solid-state Kovar housing at a rate of 27 in./min, with a total heat input of 15 W/sec. The cover was fixtured to the frame assembly by use of a miniature knife-edge lever arm. When a series of solid-state assemblies required welding, a solenoid operated micromanipulator arm was employed. A limited degree of automation was thus achieved.

Packaging of Microminiature Modules

The application of electron beam welding to electronic microminiaturization is illustrated by the eight-bit digital adder shown in Fig. 13. The module shown contains 20 wafer assemblies of seven different circuits—inverter, flip-flop, and/or gate, two/or gates, clock amplifiers, two/and gate, and a multivibrator. The module contains a total of 1200 electron beam welds (approximately 700 of which were produced on wafers), an interconnecting motherboard, and

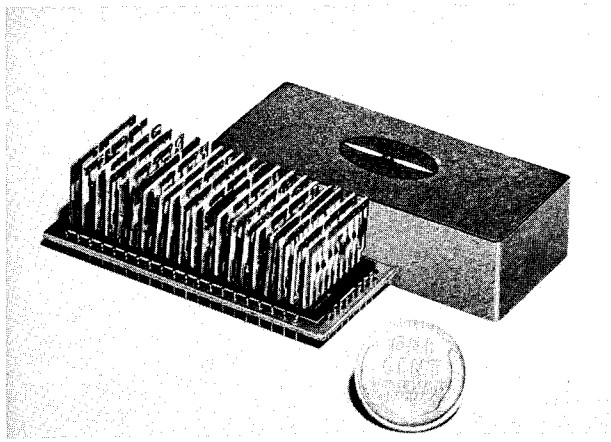

Fig. 13. Electron beam welded module, hermetically sealed.

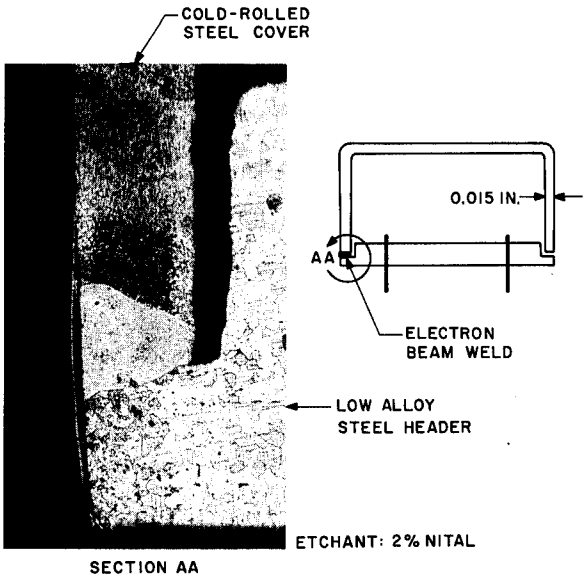

Fig. 14. Steel to steel micrograph illustrating hermetic steel header.

header assembly. The entire unit was hermetically encapsulated by electron beam welding a 0.015-in. steel cover to a cold-rolled low-alloy steel header. Figure 14 is a photomicrograph of the electron beam weld made between the steel cover and the header of the microminiature module. (Note weld penetration well into the base metal.) This type of weld will consistently produce a hermetic joint having leakage rates of less than 0.3 cc/year without damaging the internal microminiature components and interconnections.

As shown in Fig. 15, the cordwood design lends itself to packaging of microminiature modules by electron beam welding. With the cordwood concept, component leads can be

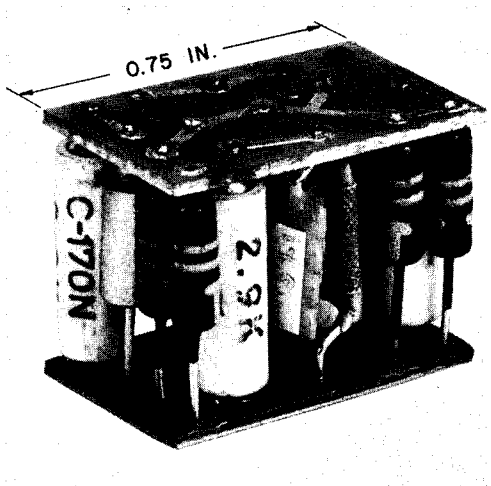

Fig. 15. Cordwood package-electron beam welded.

fitted through holes in metallized alumina or fiberglass epoxy wafers that serve as the end-plates for the module structure. After the components have been inserted through the wafer, the component leads are trimmed to approximately 0.020 in. above the metallized surface. The resulting weld forms a rivetlike cap over the feedthrough hole providing a strong mechanical joint, a low-resistance weld, and a hermetic seal. A simple end-welded miniature component assembly using this assembly and weld principle is shown in Fig. 16. The substrate used for this application was aluminum oxide. Figures 17 and 18 also illustrate that end welds can be successfully completed on fiberglass epoxy substrates although more precise machine control and fabrication practices must be exercised. Some of the lead materials, energy input, and

TABLE II

Typical Electron Beam Energy Requirements for Microelectronic Welding to Epoxy Substrates

Material	Kilovolts	Milliamperes	Pulse frequency, cps	Pulse width, msec	Comments
0.034-in.-diameter copper-tin lead to nickel tabs on glass epoxy	80	1.1	—	17	2 pulses
0.019-in.-diameter Kovar to nickel tabs on glass epoxy	80	1.1	—	17	1 pulse
0.020-in.-diameter dumet to nickel tabs on glass epoxy	80	1.1	—	17	1 pulse
0.025-in.-diameter copper-tin lead to nickel tabs on glass epoxy	80	1.1	—	17	1 pulse
0.0145-in.-diameter copper-tin lead to nickel tabs on glass epoxy	80	1.1	—	17	1 pulse
0.025-in.-diameter nickel wire to nickel tabs on glass epoxy	80	1.1	—	17	2 pulses
0.0031-in.-diameter polyurethane-insulated copper wire to silver-plated copper pins	60	0.8	—	17	1 pulse
0.003-in.-diameter gold-plated Kovar to 0.003-in.-diameter copper on glass epoxy	60	0.53	—	8	1 pulse
0.0025-in.-diameter gold-plated Kovar to 0.003-in.-diameter copper on glass epoxy	60	0.53	—	8	1 pulse
0.024-in.-diameter copper wire to 0.0035-in.-diameter silver-plated copper pad on glass epoxy	100	8	—	0.5	5 pulses
0.012-in.-diameter copper to <0.001-in. deposition of nickel on Al_2O_3 (end welds)	50	1	1	8	Beam was slightly defocused to 0.015 in. and required several pulses
0.0005-in.-diameter 1% InAu and 0.1% S6Au to silicon, germanium, and gallium arsenic wafers	50	0.5	1	8	Slightly defocused beam (~0.015 in.)
End welding of 0.016-in.-diameter tin-copper leads to 0.0025-in.-thick copper pads on fiberglass circuit boards	80	0.7–1.4	1	17	Slightly defocused to ~0.015 in.

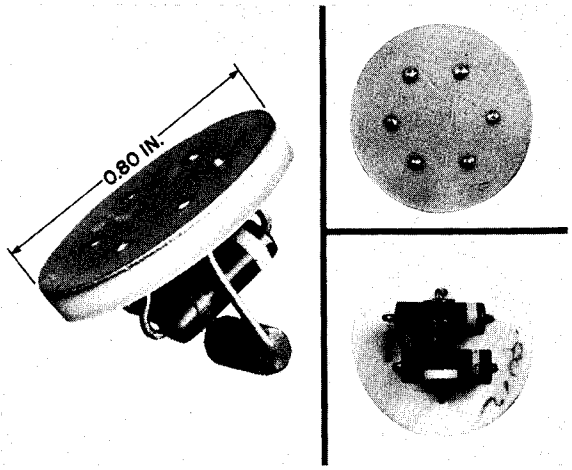

Fig. 16. Electron beam end-weld model.

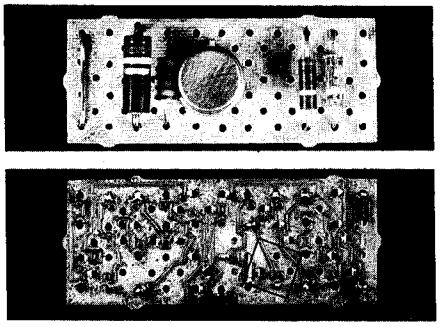

Fig. 17. Copper leads welded to printed copper epoxy board.

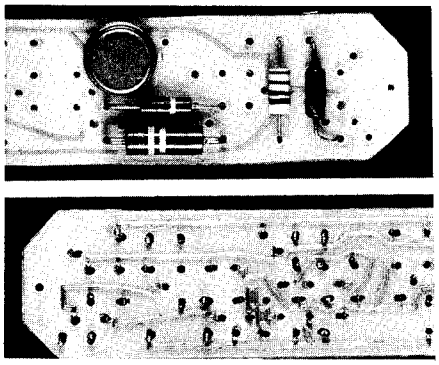

Fig. 18. Nickel lead welded to single layer epoxy board.

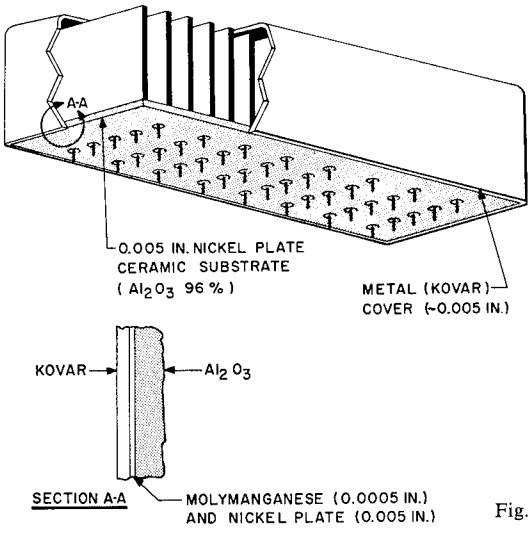

Fig. 19. Schematic of ceramic-metal encapsulation.

beam deflection parameters required to weld these types of plated substrate materials are listed in Table II. The advantage of the cordwood end-weld design is twofold:

1. It provides an overall package dimension (height) which is less than the height that can be obtained by conventional techniques (e.g., techniques which require pins or other means of providing interconnections).
2. If the module must be encapsulated, a cover assembly can be welded to the metallized substrates or metal end-plates. Welding to a metal header has been previously described (Fig. 4) but the joining of a metal cover assembly to a ceramic header substrate is considered to be unique and is described in the following section.

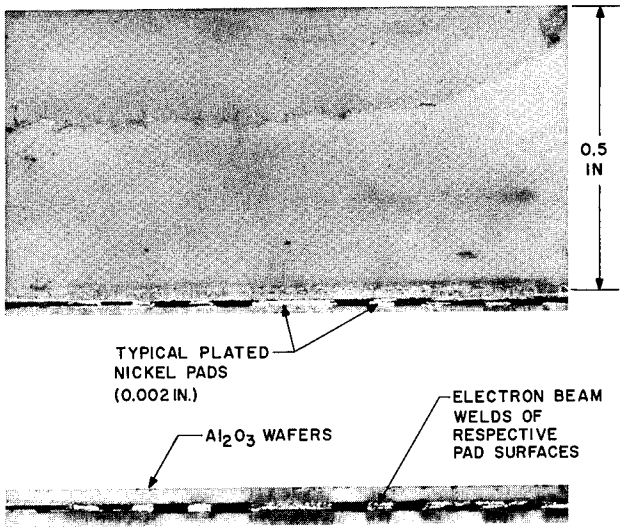

Fig. 20. Electron beam welding of electroplated nickel alumina wafers.

Modules which may require a special substrate or base header assembly because of high-temperature limitations can also be encapsulated by electron beam welding. This can be accomplished by welding the cover assembly to a thin electroplated nickel surface, as illustrated schematically in Fig. 19. A laboratory model which illustrates this design application is shown in Fig. 20. Two aluminum oxide surfaces, each having an interface nickel surface of approximately 0.003 in. thickness were welded together. For practical applications, only the alumina surface would require metallizing since the mating surface would consist of a thin (~0.010 in.) metallic cover. The nickel was electroplated over a 0.0005-in. layer of molymanganese. The molybdenum–manganese of 80/20 proportion was mixed with volatile organic binders to an approximate 4-to-1 ratio. After the slurry was applied to the ceramic, the wafer was fired, thus forcing the molymanganese into the ceramic and boiling off the organics. The two alumina substrates illustrated were joined together under controlled laboratory conditions. A heavier interface of nickel plate, approximately 0.005–0.010 in., should make it quite feasible to adapt this joining process to production applications.

CONCLUSIONS

The actual applications described in this paper have demonstrated that encapsulation of electronic components by electron beam welding is feasible and practicable. When this method of welding is applied to either relatively large relay modules or microminiature functional electronic block assemblies, a reliable and versatile production process can be utilized by the electrical and electronics industries. It is believed that the electron beam welding process cited in this paper will solve many of the difficult problems with which package designers are presently faced. As new and more advanced concepts evolve from the drawing board, the use of the electron beam for electronic packaging should provide the technological breakthroughs long sought by industry.

ACKNOWLEDGMENTS

The author wishes to acknowledge the contributions of Mr. N. Ballard and Mr. R. Duhamel who completed many of the laboratory applications illustrated. A special thanks is also extended to the Leach Corporation for granting permission to use some of the illustrations and information included in this paper.

REFERENCE

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8087

Sublimation of Materials Problem in Electronic Packaging for Spacecraft*

M. M. FULK AND K. S. HORR
Ball Brothers Research Corporation, Boulder, Colorado

Many packages of electronic gear enter outer space aboard spacecraft. These packages perform a function or gather data but should not interfere in the primary effort of the spacecraft. Therefore it becomes mandatory that electronic packaging techniques take into consideration the spacecraft function, so as not to incur an overall package penalty or even failure of the mission. The use of less than adequate materials in some packaging for spacecraft is encouraged by lack of data, short lead times, cost pressures, etc.

Sublimation data on some polymeric materials and metals used in electronic packaging are presented. The effects of the sublimation on the function of the primary and secondary packages are considered in some detail, including such aspects of the problem as activation of electrical contacts, mechanical and thermal balance of the spacecraft, and ultraviolet optics.

INTRODUCTION

THE EXPLORATION of our solar system by spacecraft has given a new urgency and motivation to the field of electronic circuit packaging. Never before have the requirements for minimum size and weight along with maximum reliability been so strict. As spacecraft lifetimes become longer and the in-orbit operations become more complex, the demands upon the electronic packaging engineer will become greater. Electronic packages must survive the space environment without adversely affecting the operation of the spacecraft in any way. Much work has been done on increasing the reliability of electronic components, and studies have been made of the effects of radiation on them [1].

Figure 1 shows the functional radiation dose thresholds for various parts and materials. It should be noted that Teflon has the least radiation resistance of the structural materials listed, but this low value is at least an order of magnitude greater than that for transistors.

Little has been done on studies of the compatibility of the materials used incidental to electronic packaging (i.e., potting compounds, circuit boards, paints, and adhesives) with overall spacecraft functioning. Many materials used in electronic packaging outgas or sublimate in the vacuum of space. These outgassed materials may have adverse effects on the sensitive mechanisms of the spacecraft. Their deposition upon slip rings (thereby increasing noise levels and contact resistance), upon thermal control surfaces (altering the desired thermal pattern of the spacecraft), or upon optical surfaces (decreasing their transmittance and reflectance) is among the harmful effects of outgassing that might accompany careless electronic packaging.

GENERAL REMARKS

The loss of material in vacuum by evaporation and/or sublimation is given by the Knudsen–Langmuir equation.

* This work was supported by NASA.

$$W = 5.83 \times 10^{-2} P \left(\frac{M}{T}\right)^{1/2}$$

where P, the vapor pressure of the material (in mm Hg), is given by

$$P = (\text{constant}) e^{-B/T} \qquad \text{or} \qquad \log P = A - \frac{B}{T}$$

W is the rate of loss in grams per square centimeter per second, M is the molecular weight (not the mass of the molecule), T is the temperature in degrees Kelvin, and A and B are constants for each material.

A critical and comprehensive compilation of vapor pressure data for the solid and liquid elements [2] is given in Figs. 2 to 4. Using these tables and the Knudsen–Langmuir equation, one can determine the weight loss rate for a simple material.

For most metals and pure simple organic compounds the vapor pressure and molecular weights are relatively well known or can be estimated with fair accuracy. For inorganic compounds the problem is often more complex because the loss of material can occur by several mechanisms, i.e., molecules of the compound can evaporate and/or decompose into elements or simpler compounds, which in turn can evaporate or not evaporate. Furthermore, when the space environment is considered, these mechanisms can be induced or accelerated by various types of radiation. Some organic materials of low molecular weight can evaporate in vacuum without decomposition, and if their thermodynamic properties are known, the Knudsen–Langmuir equation gives good estimates of losses in vacuum. However, most organic materials used in spacecraft are long-chain polymeric compounds that can be depolymerized or unraveled in the heat bath of the spacecraft into more volatile fragments of unknown structure and molecular weight.

The unraveling of these large molecules is a complex process and takes part throughout the body of the material. There is then a complicated diffusion and solubility problem coupled with the evaporative loss for each material. For polymeric materials, the calculations for weight loss in vacuum involve many data which are usually unknown, or if the values were known, the calculations might be too complicated to be useful. It is almost necessary to measure the weight loss in vacuum for complex compounds.

METHOD

This work was not intended as a basic research program on materials. Rather, it was a directed effort to evaluate materials for use in the Orbiting Solar Observatory spacecraft series. The OSO spacecraft presented a severe materials challenge since it is designed to carry

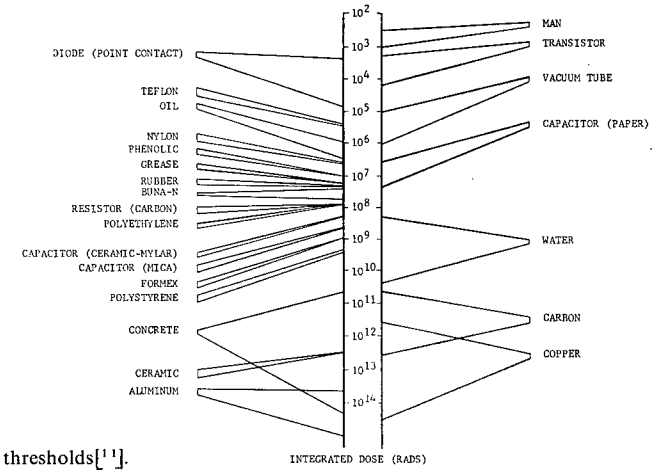

Fig. 1. Functional radiation dose thresholds[11].

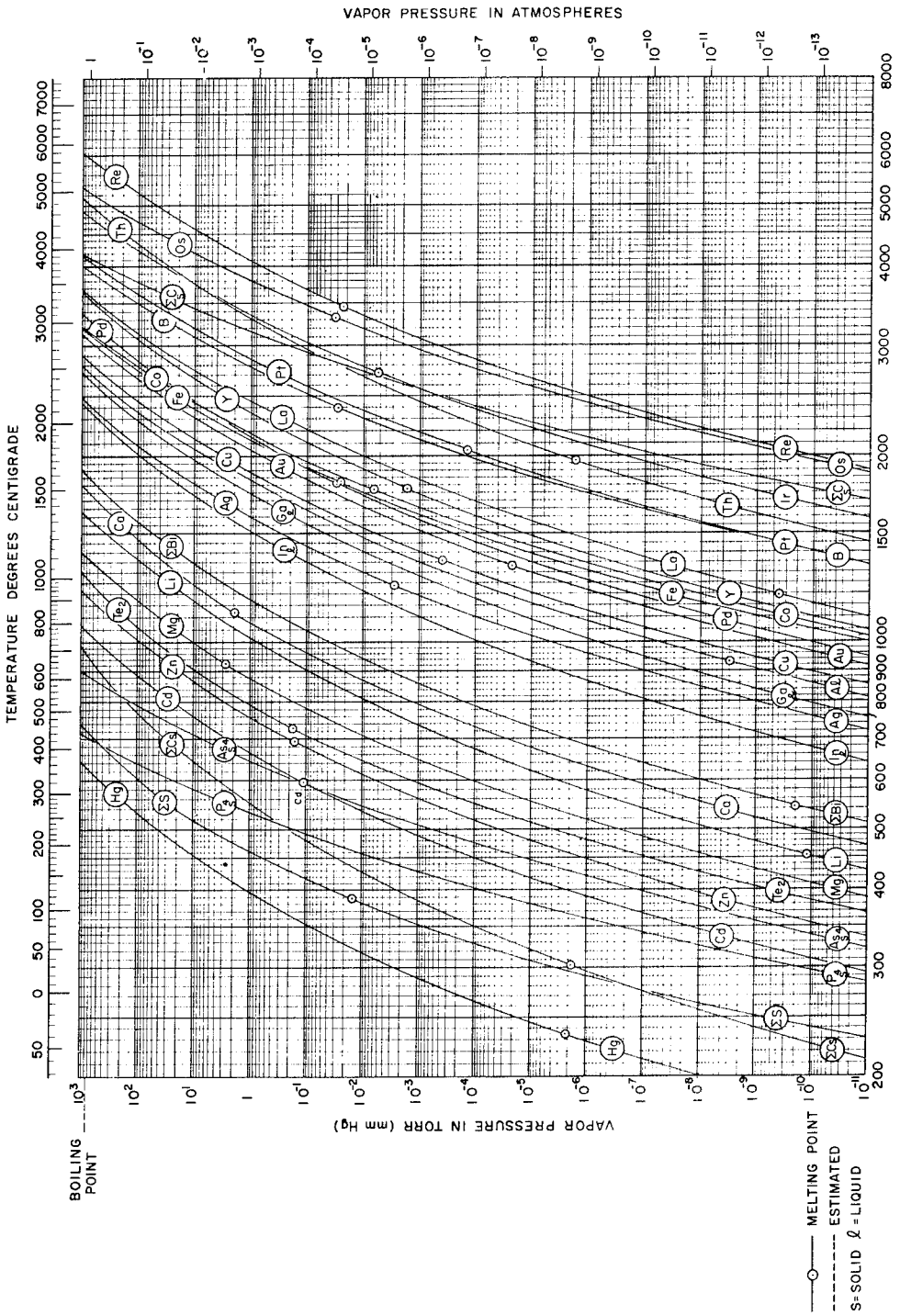

Fig. 2. Vapor pressure curves of the elements.

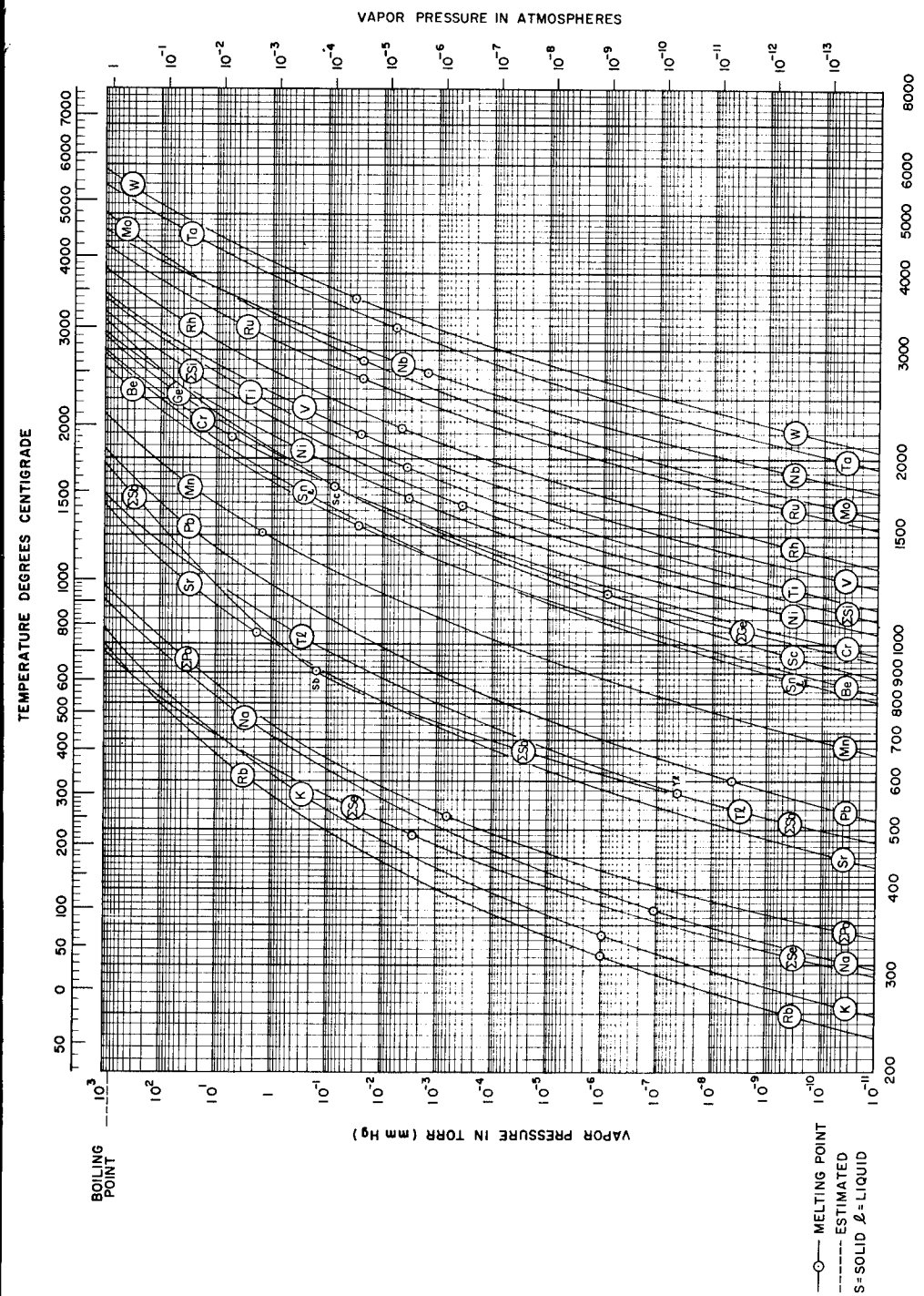

Fig. 3. Vapor pressure curves of the elements.

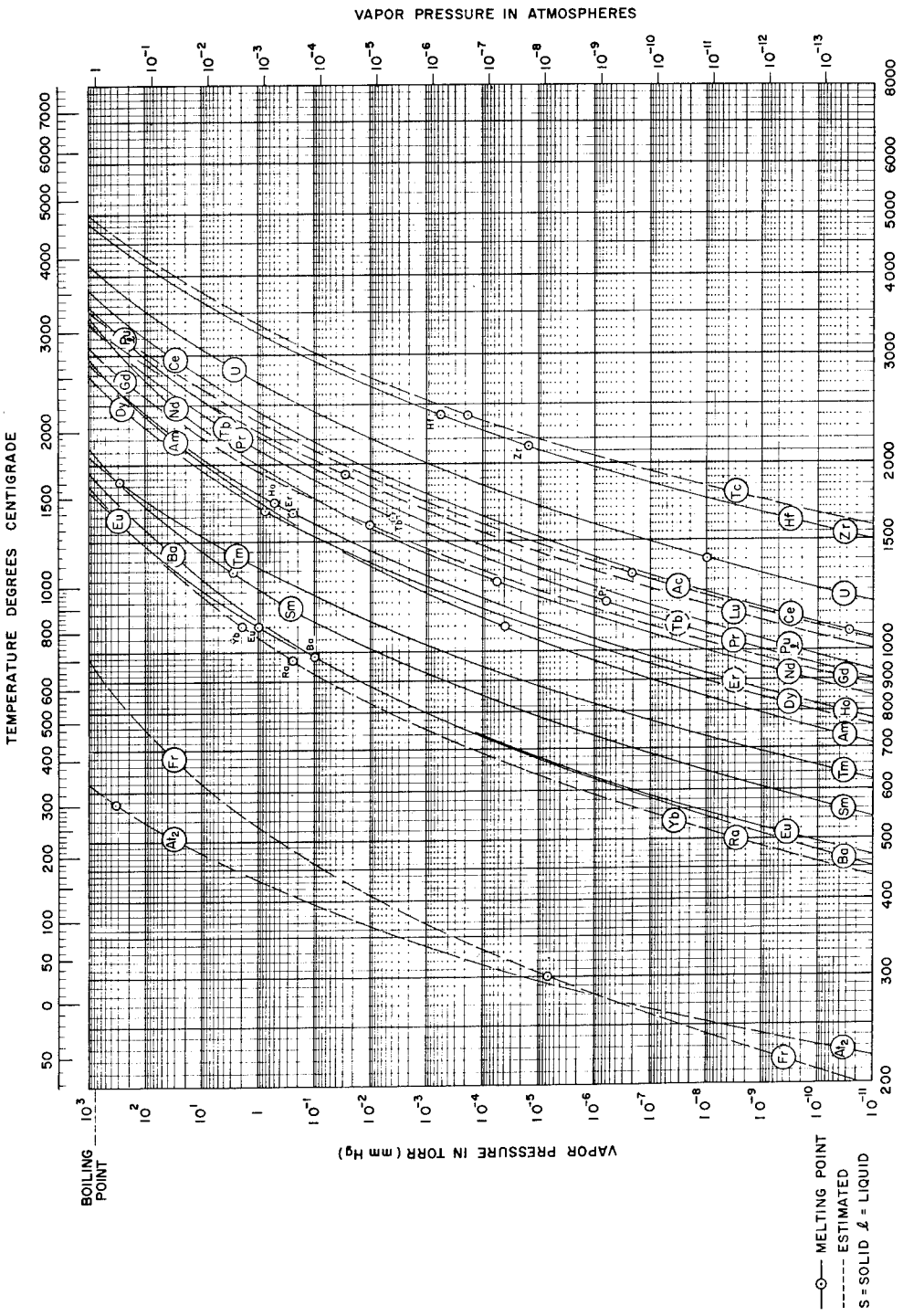

Fig. 4. Vapor pressure curves of the elements.

some of the most sensitive instruments yet placed in orbit. The primary function of the OSO is to study radiations from the sun.

Rather large and thick samples were used (Tables I and II) for the weight loss in vacuum studies described here. It has been shown that, for some materials, the initial outgassing rates are affected by thickness when samples are thinner than about 0.25 in. Decreasing the thickness from 0.25 in. to 0.05 in. has increased the initial weight loss rates by an order of magnitude for some materials [3]. Thicker samples more nearly characterize practical usage.

Samples were placed in a thermal vacuum system and maintained at pressures less than 5×10^{-6} mm Hg. Test runs were made at 50 and 100°C. These temperatures give readily observable weight loss rates with minimum thermal decomposition. Samples were weighed in air, using a carefully timed sequence, on a balance with a sensitivity of 0.5 mg. Very few organic polymers were hydrophilic enough to present a serious problem. The gross weight losses were so great that the error due to moisture adsorption during the in-air weighing could generally be neglected. Thus, weighing in air has been found to be satisfactory for preliminary tests of materials with high weight loss rates. For detailed studies of materials with low weight loss rates, or hydrophilic materials, continuous weighing in vacuum should be utilized.

RESULTS

Weight Loss in Vacuum

Figure 5 shows a typical weight loss *vs.* time curve for a polymeric material in vacuum. The time interval τ represents the time required for a material to reach its stationary-state weight loss rate. Prior to this time, the weight loss includes adsorbed gases, solvents, lower-molecular-weight fragments, etc. This time varied from twenty-five to several hundred hours for different materials. Tables I and II present weight loss data based on work done by the authors. They are presented in order of increasing weight loss rate. Table III presents weight loss data compiled from the open literature and converted, as nearly as possible, to be comparable with the authors' data.

Some work has been done [7] which demonstrates that when ultraviolet radiation is added to the vacuum environment, an increase in weight loss results.

Weight loss data in the open literature are frequently expressed only in terms of percent weight loss, with no mention of sample configuration or composition. While these data are helpful in general comparisons, they are of little value in a detailed analysis of a material.

Contamination

Rates of weight loss in vacuum can be misleading if other characteristics of the materials are not taken into account. An excellent example of this is furnished by the irradiated polyolefin materials. Their weight loss rates are among the lowest presented here, but experience

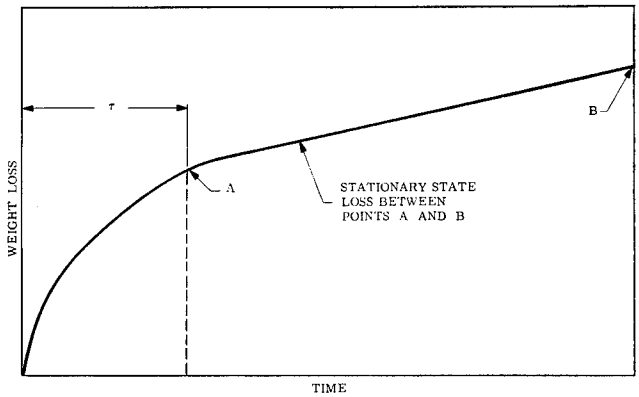

Fig. 5. Characteristic weight loss *vs.* time.

TABLE I
Weight Loss in Vacuum (Sample Temperature 50°C, Pressure $<5 \times 10^{-6}$ mm Hg)

Material	Mixing ratio or formulator, parts by weight	Sample size, in.	Surface area, cm^2	Original weight of sample, g	Total weight loss to stationary state, g/cm^2	Time to stationary state, hr	Stationary state weight loss rate, $g/cm^2/sec$	Ref.
Teflon TFE	W. S. Shamban & Co.	2 dia × $\frac{1}{4}$ thick	49.9	27.5361	7.4×10^{-5}	100	3.7×10^{-12}	10
Teflon FEP	W. S. Shamban & Co.	2 dia × $\frac{1}{4}$ thick	51.1	27.0880	5.4×10^{-5}	100	3.7×10^{-12}	10
Kel F 300	W. S. Shamban & Co.	2 dia × $\frac{1}{4}$ thick	51.5	27.7676	2.7×10^{-5}	100	3.7×10^{-12}	10
Kel F 81 Grade 2	W. S. Shamban & Co.	2 dia × $\frac{1}{4}$ thick	52.0	28.2008	2.9×10^{-5}	100	7.7×10^{-12}	10
Halon TVS	Allied Chem. Co.	2 dia × $\frac{1}{8}$ thick	46.2	12.4016	1.7×10^{-5}	50	3.2×10^{-12}	10
Halon VK	Allied Chem. Co.	2 dia × $\frac{1}{8}$ thick	46.6	14.5570	1.7×10^{-5}	25	8.2×10^{-12}	10
Kynar	Pennsalt Chem. Co.	3 × 3 × $\frac{1}{8}$	125.0	30.5082	4.7×10^{-5}	100	3.1×10^{-12}	10
Irradiated polyolefin wire insulation (Rayolin N 102E)	Raychem Corp.	2.0 dia × 0.08	42.4	3.662–4.166	$8.5–11.6 \times 10^{-5}$	138	$1.3–2.0 \times 10^{-11}$	9
Irradiated polyolefin shrinkable tubing Type RNF RT201	Raychem Corp.	4.0 × 4.0 × 0.02	192.0	6.211	4.6×10^{-5}	138	1.8×10^{-11}	9
Nylon (Zytel 105)	A. L. Hyde Co.	2.0 dia × 0.25	50.5	14.623	1.6×10^{-4}	141	3.3×10^{-11}	9
Epiall 1288 epoxy molding compound	Mesa Plastics Co.	2.0 dia × 0.12	44.0	11.789	3.9×10^{-5}	55	4.4×10^{-11}	9
Irradiated polyolefin experimental type	Raychem Corp.	2.0 dia × 0.08	42.4	3.913–4.063	1.1×10^{-4}	138	$4.7–9.5 \times 10^{-11}$	9
Delrin 500	A. L. Hyde Co.	2.0 dia × 0.25	50.5	18.172	3.0×10^{-4}	168	5.6×10^{-11}	9
Epiall 1459 epoxy molding compound	Mesa Plastics Co.	2.0 dia × 0.12	44.0	13.524	3.8×10^{-5}	55	7.2×10^{-11}	9
Nylon (Zytel 31)	A. L. Hyde Co.	2.0 dia × 0.25	50.5	13.903	2.2×10^{-4}	141	8.9×10^{-11}	9
Nylon (Zytel 101)	A. L. Hyde Co.	2.0 dia × 0.25	50.5	14.700	2.8×10^{-4}	188	9.4×10^{-11}	9
Delrin 507	A. L. Hyde Co.	2.0 dia × 0.25	50.5	18.707	3.6×10^{-4}	188	1.4×10^{-10}	9
DAP Type 3-2-530	Acme Resin Co.	2.0 dia × 0.12	44.0	11.616	1.1×10^{-4}	55	1.7×10^{-10}	9
DAP Type 52-01	Mesa Plastics Co.	2.0 dia × 0.20	49.0	23.667	1.3×10^{-4}	55	2.0×10^{-10}	9
DAP Type 1-530	Acme Resin Co.	2.0 dia × 0.12	44.0	9.843	1.0×10^{-4}	55	2.2×10^{-10}	9
DAP Type 1-503	Acme Resin Co.	2.0 dia × 0.12	44.0	9.254	1.2×10^{-4}	55	2.3×10^{-10}	9
Devcon F epoxy (room temp. cure)	9 resin 1 hardner 1 thinner	in cup 2.3 dia	27.0	75.382	7.0×10^{-4}	25	2.5×10^{-10}	9

DAP Type FS-5	Mesa Plastics Co.	2.0 dia × 0.020	49.0	22.556	2.6×10^{-4}	55	4.2×10^{-10}	9
Armstrong epoxy (room temp. cure)	7 C-7 resin, 2 "W" activator, 2 flex resin No. 1	in cup 2.3 dia	27.0	52.887	1.8×10^{-4}	25	1.1×10^{-9}	9
Phenolic laminate grade XX Natural	Synthane Corp.	2.0 dia × 0.13	46.2	8.728–8.771	$1.4–1.5 \times 10^{-3}$	138	$1.0–1.2 \times 10^{-9}$	9
Phenolic laminate Grade LBB Natural	Synthane Corp.	2.0 dia × 0.13	46.2	8.852–8.886	$2.3–2.4 \times 10^{-3}$	138	$1.3–1.4 \times 10^{-9}$	9
Permacel epoxy Type PRH 102 (cured 3 hr at 60°C)	10 resin 10 hardner 1 activator	in cup 2.3 dia	27.0	53.979	3.2×10^{-4}	25	1.7×10^{-9}	9
Permacel epoxy Type FR 3935 (room temp. cure)	1 resin 1 activator	in cup 2.3 dia	27.0	46.813	7.1×10^{-4}	25	2.7×10^{-9}	9
Permacel epoxy (Type PRH 102) (room temp. cure)	10 resin 10 hardner 1 activator	in cup 2.3 dia	27.0	56.665	6.6×10^{-4}	25	2.8×10^{-9}	9
Dow RTV 521 silicone rubber (room temp. cure)	96 resin 4 activator	in cup 2.3 dia	27.0	54.900	4.5×10^{-3}	68	4.4×10^{-9}	9
Dow RTV 503 silicone rubber (room temp. cure)	96 resin 4 activator	in cup 2.3 dia	27.0	46.118	4.2×10^{-3}	68	6.4×10^{-9}	9
GE RTV 40 silicone rubber (room temp. cure)	99 resin 1 activator	in cup 2.3 dia	27.0	59.989	5.0×10^{-3}	68	7.5×10^{-9}	9
GE RTV 60 silicone rubber (room temp. cure)	99 resin 1 activator	in cup 2.3 dia	27.0	62.386	5.3×10^{-3}	68	7.8×10^{-9}	9
Dow RTV 501 silicone rubber (room temp. cure)	96 resin 1 activator	in cup 2.3 dia	27.0	50.032	5.8×10^{-3}	68	1.0×10^{-8}	9
GE RTV 11 silicone rubber (room temp. cure)	99 resin 1 activator	in cup 2.3 dia	27.0	51.086	4.1×10^{-3}	44	1.0×10^{-8}	9
GE LTV 602 silicone potting compound (cured 16 hr at 100°C)	99.75 resin 0.25 activator	in cup 2.3 dia	27.0	41.859	1.2×10^{-2}	44	2.8×10^{-8}	9
Dow RTV 5313-5314 silicone potting compound (room temp. cure)	1 5313 1 5314	in cup 2.3 dia	27.0	47.700	4.3×10^{-2}	68	1.1×10^{-7}	9

TABLE II

Weight Loss in Vacuum (Sample Temperature 100°C, Pressure $< 5 \times 10^{-6}$ mm Hg)

Material	Mixing ratio or formulator, parts by weight	Sample size, in.	Surface area, cm^2	Original weight of sample, g	Total weight loss to stationary state, g/cm^2	Time to stationary state, hr	Stationary state weight loss rate, $g/cm^2/sec$	Ref.
Teflon TFE	W. S. Shamban & Co.	2 dia × $\frac{1}{4}$	49.9	27.4722	9.2×10^{-5}	25	1.2×10^{-11}	10
Teflon FEP	W. S. Shamban & Co.	2 dia × $\frac{1}{4}$	51.5	27.9108	8.6×10^{-5}	25	1.3×10^{-11}	10
Kel F 300	W. S. Shamban & Co.	2 dia × $\frac{1}{4}$	51.5	27.4053	7.2×10^{-5}	47	3.0×10^{-11}	10
Kel F 81 Grade 2	W. S. Shamban & Co.	2 dia × $\frac{1}{4}$	52.0	28.3227	7.5×10^{-5}	47	2.7×10^{-11}	10
Halon TVS	Allied Chem. Co.	2 dia × $\frac{1}{8}$	46.2	12.0139	4.6×10^{-5}	25	4.1×10^{-12}	10
Halon VK	Allied Chem. Co.	2 dia × $\frac{1}{8}$	46.6	13.9384	3.4×10^{-5}	25	5.9×10^{-12}	10
Kynar	Pennsalt Chem. Co.	3 × 3 × $\frac{1}{8}$	125.0	30.2138	6.6×10^{-5}	47	1.3×10^{-11}	10
Irradiated polyolefin shrinkable tubing Type RNF RT201	Raychem Corp.	4.0 × 4.0 × 0.02	192.0	6.510	4.3×10^{-4}	144	1.1×10^{-10}	9
Epiall 1552 epoxy molding compound	Mesa Plastics Co.	2.0 dia × 0.12	44.0	11.406	3.8×10^{-4}	64	1.3×10^{-10}	9
Epiall 1459 epoxy molding compound	Mesa Plastics Co.	2.0 dia × 0.12	44.0	13.522	1.5×10^{-4}	64	1.3×10^{-10}	9
Epiall 1288 epoxy molding compound	Meas Plastics Co.	2.0 dia × 0.12	44.0	11.782	4.2×10^{-4}	64	1.8×10^{-10}	9
Irradiated polyolefin wire insulation (Rayolin "N") 102E	Raychem Corp.	2.0 dia × 0.08	42.4	4.230–4.382	$8.9–9.4 \times 10^{-4}$	191	$1.8–2.2 \times 10^{-10}$	9
DAP Type FS-5	Mesa Plastics Co.	2.0 dia × 0.020	49.0	22.388	6.5×10^{-4}	88	3.1×10^{-10}	9
DAP Type 1-503	Acme Resin Co.	2.0 dia × 0.12	44.0	8.836	5.1×10^{-4}	88	3.1×10^{-10}	9
Nylon (Zytel 31)	A. L. Hyde Co.	2.0 dia × 0.25	50.5	13.936	6.3×10^{-4}	104	3.3×10^{-10}	9
DAP Type 3-2-530	Acme Resin Co.	2.0 dia × 0.12	44.0	11.469	4.2×10^{-4}	88	3.3×10^{-10}	9

Nylon (Zytel 105)	A. L. Hyde Co.	2.0 dia × 0.25	50.5	14.849	6.3×10^{-4}	104	3.3×10^{-10}	9
DAP Type 1-530	Acme Resin Co.	2.0 dia × 0.12	44.0	9.886	4.1×10^{-6}	64	3.3×10^{-10}	9
Nylon (Zytel 101)	A. L. Hyde Co.	2.0 dia × 0.25	50.5	14.696	7.5×10^{-4}	104	4.2×10^{-10}	9
DAP Type 52-01	Mesa Plastics Co.	2.0 dia × 0.20	49.0	23.482	3.1×10^{-4}	64	4.4×10^{-10}	9
Delrin 507	A. L. Hyde Co.	2.0 dia × 0.25	50.5	18.986	5.6×10^{-4}	104	4.4×10^{-10}	9
Devcon F epoxy (room temp. cure)	1 resin 1 hardner 1 thinner	in cup 2.3 dia	27.0	75.354	1.0×10^{-3}	28	5.0×10^{-10}	9
Delrin 500	A. L. Hyde Co.	2.0 dia × 0.25	50.5	18.383	5.3×10^{-4}	104	5.6×10^{-10}	9
Phenolic laminate Grade LBB Natural	Synthane Corp.	2.0 dia × 0.13	46.2	8.851–8.921	$4.6–4.8 \times 10^{-3}$	161	$1.1–1.2 \times 10^{-9}$	9
Armstrong epoxy (room temp. cure)	7-C 7 resin 3-"W" activator 2-Flex resin No. 1	in cup 2.3 dia	27.0	52.846	1.4×10^{-3}	28	1.8×10^{-9}	9
Irradiated polyolefin experimental type	Raychem Corp.	2.0 dia × 0.08	42.4	4.191–4.417	$3.5–4.0 \times 10^{-3}$	191	$2.2–2.3 \times 10^{-9}$	9
Phenolic laminate Grade XX Natural	Synthane Corp.	2.0 dia × 0.13	46.2	8.706–8.752	3.5×10^{-3}	161	2.5×10^{-9}	9
Permacel epoxy Type PRH 102 (cured 3 hr at 60°C)	10 resin 10 hardner 1 activator	in cup 2.3 dia	27.0	53.882	2.3×10^{-3}	28	8.1×10^{-9}	9
Permacel epoxy Type PRH 102 (room temp. cure)	10 resin 10 hardner 1 activator	in cup 2.3 dia	27.0	56.531	3.4×10^{-3}	28	9.5×10^{-9}	9
Permacel epoxy Type FR 3935 (room temp. cure)	1 resin 1 activator	in cup 2.3 dia	27.0	46.662	4.0×10^{-3}	28	$1.0–1.1 \times 10^{-8}$	9

TABLE III
Weight Loss in Vacuum Data from Open Literature

Material	Sample size	Pressure, mm Hg	Weight of sample, g	Weight loss, %	Temperature, °C	Duration of test, hr	Weight loss rate, g/cm²/sec	Ref.
Teflon PTFE*	$\frac{5}{8}$ in. dia × $\frac{1}{8}$ in. thick in ceramic cup	2×10^{-6} to 5×10^{-7}	—	—	10	—	5×10^{-10}	5
					93		1×10^{-9}	
					177		9×10^{-9}	
					260		1×10^{-7}	
					344		2×10^{-4}	
Epoxy cured with DETA*	$\frac{5}{8}$ in. dia × $\frac{1}{8}$ in. thick in ceramic cup	2×10^{-6} to 5×10^{-7}	—	—	13	—	$<1 \times 10^{-10}$	5
					93		1×10^{-7}	
					177		2×10^{-7}	
Teflon TFE*	10 in.² × 2–5 mm long cylinders of wire insulation	10^{-7}	3.2595	0.04	100	100	5×10^{-9}	6
Teflon FEP*	10 in.² × 2–5 mm long cylinders of wire insulation	10^{-7}	2.1376	0.08	100	102	7×10^{-9}	6
Teflon PTFE*	2 in. dia × 0.188 in. thick	3×10^{-6} to 3×10^{-7}	—	—	50	—	3×10^{-10}	3
					100		9×10^{-10}	
Epoxy (Epon 821)*	2 in. dia × 0.188 in. thick	3×10^{-6} to 3×10^{-7}	—	—	50	—	3×10^{-9}	3
					100		1×10^{-8}	
Nylon–Phenolic composite (50% nylon)*	2 in. dia × 0.188 in. thick	3×10^{-6} to 3×10^{-7}	—	—	50	—	1×10^{-8}	3
					100		5×10^{-8}	
Silica–Phenolic (70% silica)*	2 in. dia × 0.188 in. thick	3×10^{-6} to 3×10^{-7}	—	—	50	—	4×10^{-8}	3
					100		9×10^{-8}	
Lexan (Polycarbonate)*	2 in. dia × 0.188 in. thick	3×10^{-6} to 3×10^{-7}	—	—	50	—	2×10^{-10}	3
					100		1×10^{-9}	
Mylar A	0.013 cm thick × 37.8 cm²	$<10^{-5}$	0.330	—	ambient	560	1×10^{-11}	7
Epoxy Shell Epon 820 curing agent CL	0.0277 cm thick × 3.3 cm²	$<10^{-5}$	0.341	—	ambient	676	8×10^{-11}	7
Kel F 81	0.013 cm thick × 24.4 cm²	$<10^{-5}$	0.351	—	ambient	660	No weight loss detected	7
Teflon	0.081 cm thick × 4.27 cm²	$<10^{-5}$	0.325	—	ambient	562	No weight loss detected	7
Dow Corning Silastic Silicone No. 916-4-480	0.17 cm thick × 4.29 cm²	$<10^{-5}$	0.382	—	ambient	455	2×10^{-10}	7
Acrylic (Mil-P-5425)	1 in. × 1 in.	10^{-5} to 10^{-6}	1.9630	0.11	25	24	2×10^{-9}	8
			1.9161	0.29	50	24	5×10^{-9}	
			1.9426	0.44	100	24	7×10^{-9}	
Kel F Unplasticized	1 in. × 1 in.	10^{-5} to 10^{-6}	4.0038	—	25	24	None detected	8
			3.9047	0.01	50	24	3×10^{-10}	
			4.0535	—	100	24	None detected	
Kel F Plasticized P-25	1 in. × 1 in.	10^{-5} to 10^{-6}	3.7857	0.01	25	24	2×10^{-10}	8
			3.7793	0.12	50	24	3×10^{-9}	
			3.7116	1.68	100	24	5×10^{-8}	
Nylon Mil-P-17091	1 in. × 1 in.	$10^{-5} \times 10^{-6}$	10.2124	0.03	25	24	3×10^{-10}	8
			10.0486	0.09	50	24	1×10^{-9}	
			10.0389	0.24	100	24	3×10^{-9}	

* Interpreted from graphical data.

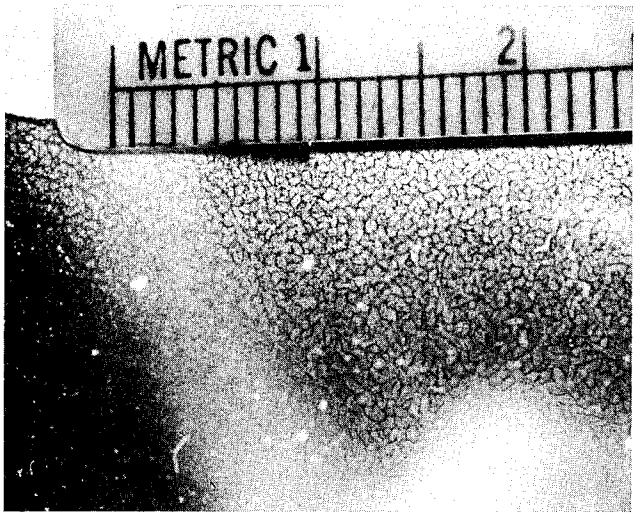

Fig. 6. Pattern of contamination on the bell jar of a vacuum system containing 750 ft of AWG 22 hookup wire with irradiated polyolefin insulation.

has shown that their outgassed products can severely contaminate nearby objects. Figure 6 shows the pattern of contamination on the bell jar of a vacuum system containing 750 ft of AWG 22 hookup wire with irradiated polyolefin insulation. This picture was taken after 162 hours with the wire at 75°C, a pressure of $<5 \times 10^{-6}$ mm Hg, and a bell jar at room temperature. Figure 7 shows a small sample of the contamination which has been scraped from the bell jar. This contamination is probably attributable, in part, to additives rather than to the irradiated polyolefin. The addition of flame retardants, antioxidants, "anti-rad" compounds, flexibilizers, and/or organic pigments to polymeric materials could cause similar contamination.

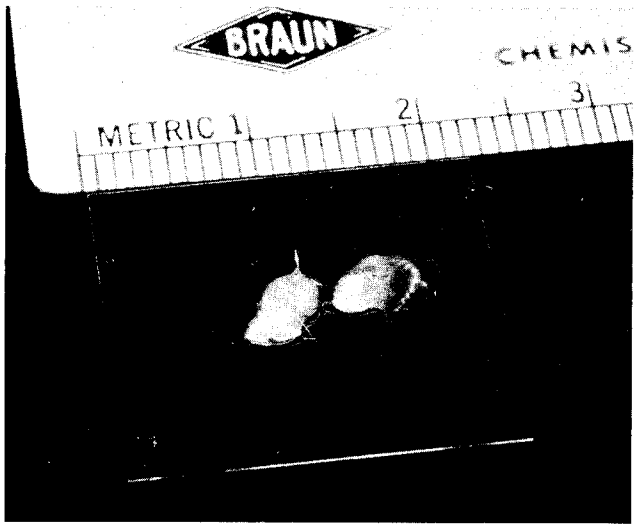

Fig. 7. A small sample of the contamination shown in Fig. 6.

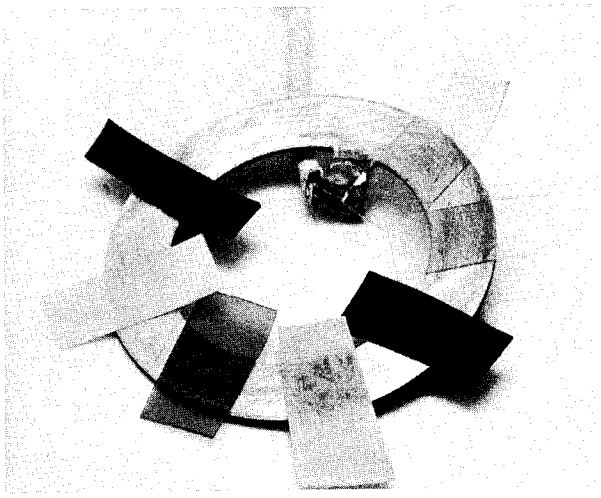

Fig. 8. Tape samples in place on coin silver slip ring. Clockwise from wire lead: 3M Transparent Tape No. 600, 3M "Magic Mending Tape," 3M Plastic Electrical Tape No. 31–445, Permacel Paint Masking Tape, 3M TFE Electrical Tape (Teflon) No. 61, 3M Polyester Electrical Tape No. 57, 3M Silicone Rubber Electrical Tape No. 70.

Other tests, using front-surface mirrors calibrated at 1216 Å as contamination monitors, indicated losses in reflectivity of up to 18% in the 1216 Å region. In these tests, the pressure was less than 5×10^{-6} mm Hg, the wire temperature was 35°C, and the temperature of the mirrors was about 10°C.

Corrosion

One factor often overlooked in electronic packaging for spacecraft is corrosion in its various forms. The most common form of corrosion found in electronic packaging is galvanic (two-metal) corrosion. Galvanic corrosion can occur when two dissimilar metals are in contact. Steel and copper in contact with aluminum can cause rapid failure of the aluminum parts.

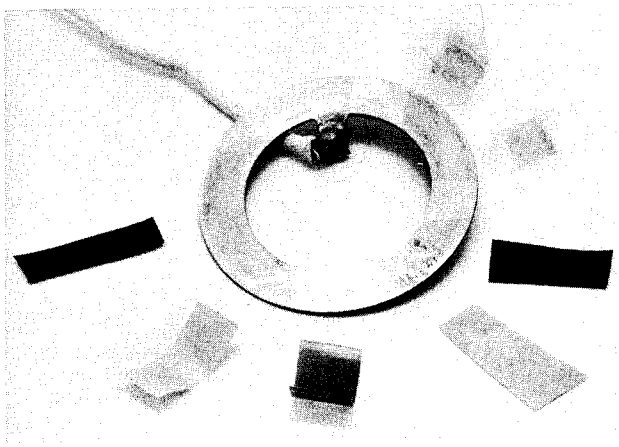

Fig. 9. Slip ring with tapes removed after 1000 hours at 50°C in air. (Slip ring has been solvent-cleaned to remove adhesive.)

Deposition of outgassed products from polymeric materials, acting as an electrolyte, can greatly accelerate the rate of galvanic corrosion. Passivation of all metal surfaces prior to assembly will, in most cases, minimize the possibility of galvanic corrosion.

It has been shown [4] that most plastics and rubbers have some corrosive effect on metals. Among the more corrosive plastics are phenolics, vinyls, alkyds, and polyesters. Cellulosic filters can add appreciably to the corrosiveness of plastics. Cadmium is one of the more susceptible metals to corrosion by plastics and this, together with its rather high vapor pressure, makes the use of cadmium-plated parts in electronic packages undesirable. While it may be argued that most of the work done on corrosivities of plastics has been carried out in air and is not applicable to the space environment, it must be remembered that galvanic corrosion needs only the presence of dissimilar metals and an electrolyte, in this case the outgassed products from polymeric materials. Air (oxygen) or moisture will accelerate the corrosion rate, but their absence will not eliminate corrosion.

Tapes and/or their adhesives can be a source of corrosion. Figure 8 shows a coin silver slip ring with seven types of tape attached to it. Figure 9 shows the same slip ring after 1000 hours at 50°C in air. This is an example of the possible corrosive effects of commonly used packaging materials.

CONCLUSION

Great care must be taken to select suitable materials for electronic packages in spacecraft. Improper materials selection could severely degrade satellite performance. Weight loss in vacuum data should be used as an aid in selecting materials for spacecraft use, as well as any available data on corrosion or contamination.

Every precaution should be taken to assure that the material which goes into the spacecraft is identical, in every respect, to the material used to obtain the test data. The addition of flexibilizers, antioxidants, pigments, etc., can alter the weight loss rate of a material by several orders of magnitude.

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8088

Thermal Characteristics of Electronic Module Design

C. S. LANKTON

Missile and Space Vehicle Department, General Electric Company, Philadelphia, Pennsylvania

This paper deals with the temperature rise of electronic parts, measured for encapsulated cordwood and metal frame modules operating in vacuum. The investigations include the effects of flexible buffer coatings on the parts, encapsulants of different densities and thermal conductivities, and variation of part size and spacing for cordwood modules. Effects of glass and ceramic resistors, flexible and rigid adhesives, and on- or through-web mountings are also covered for metal frame modules. Temperature rise correlations made from the data are presented in the paper to enable the module designer to achieve the smallest size and weight permitted by his parts temperatures objectives.

INTRODUCTION

ALL DESIGNERS OF electronic equipment must be concerned with performance and reliability. Reliability increases in importance in situations where maintenance becomes difficult and expensive, culminating in space vehicles where maintenance, or its effect through use of redundant circuits, is either very expensive or impossible.

Numerous references, including references 1 and 2, have discussed the effect of temperature on performance and reliability of electronic parts, all recognizing that temperature is of considerable importance. But what temperatures should a designer expect during the operation of his equipment? This investigation has been performed to answer the part of that question pertaining to the temperature rise of electronic parts encapsulated in modules when operated in a vacuum environment, with emphasis on the rise of the maximum part case temperature above the module mounting base.

Two basic types of modules have been considered; one the potted cordwood type in which the electronic parts are assembled in a circuit and then encapsulated, and the second, called the metal frame type, in which the parts are first attached to a metal support and then encapsulated in lightweight foam material. In the first type the encapsulating material provides the thermal path from the part to the module mounting base, while in the second type heat is conducted from the part to the metal support and then to the module mounting base. Resistors of $\frac{1}{8}$ and $\frac{1}{4}$ W have usually been used as the module heat producers, and the parts of some modules have been coated with flexible RTV 60 before potting.

The thermal characteristics of cordwood modules potted in two formulations of filled epoxy encapsulants providing different density and thermal conductivity values, and modules potted with urethane foam, have been experimentally determined. Metal frame module thermal characteristics have been determined for parts attached to the metal frame with both rigid and flexible adhesives.

THERMAL INVESTIGATIONS

At the moderate temperatures required for reliable operation by most electronic parts, the generated heat in a vacuum space environment is most easily removed by conduction from

the part to some temperature controlled mounting surface. The thermal resistance of this path, usually including the effects of interfaces between different materials as well as conduction through the part itself, its leads, and the encapsulating material, is complex to analyze. Reference 4 considers module resistance from an analytical standpoint. Considerable care must be taken with experiments in this area also, or experimental error may overshadow the results. To date, however, it has been easier to provide accurate thermal design information through careful interpretation of experimental results than through analysis alone.

In these experimental investigations temperatures were measured with 40 gage (0.003 in. diameter) chromel-alumel thermocouples attached to the cases of the parts. These thermocouple materials were chosen because of low thermal conductivity, resulting in less experimental error caused by conduction of heat away from the thermocouple junction. The small size of the lead wires directly contributed to reducing the conduction effects, and also permitted better contact of the thermocouple leads with the part cases, further blocking heat conduction from the thermocouple junction. Considerable care was taken with the construction of these fine-wire couples, and sample calibrations over the temperature range of interest indicated $\pm 0.5°F$ agreement with the NBS emf *vs.* temperature table. A recording digital voltmeter, accurate to several microvolts, was used for thermocouple readout, resulting in temperature determination with less than $\pm 1°F$ overall error.

Heat rejection from the test modules by means other than direct conduction to the mounting base was discouraged by surrounding the module with a reflecting "hat" made of aluminized Mylar, and by using only a minimum of externally connecting power leads. For one set of modules, the 24-resistor modules described later, each resistor had a separate power connection. Number 30 gage constantan wires were used to limit the thermal path that these leads would introduce. This material has about $\frac{1}{10}$ the thermal conductivity of copper, but the higher lead voltage drop had to be accounted for during the power production determination. Convection was eliminated during these tests, as it would be in a vented space vehicle, by operation at pressures of 1×10^{-4} mm Hg or less.

A good thermal connection between the modules and the mounting base was provided during these tests by using an interface layer of silicone grease. An appreciable increase in module thermal resistance will occur over the values given later on if dry interfaces are used between the modules and the base plate. Reference 3 gives some idea of the size of this possible thermal resistance.

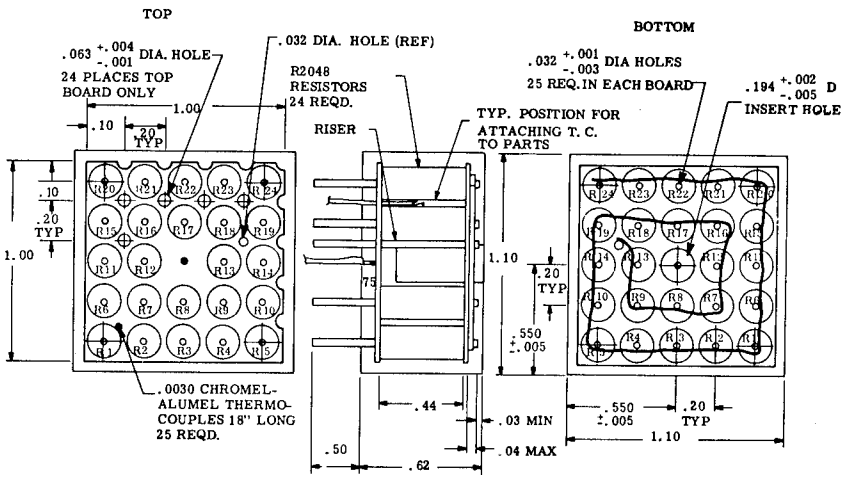


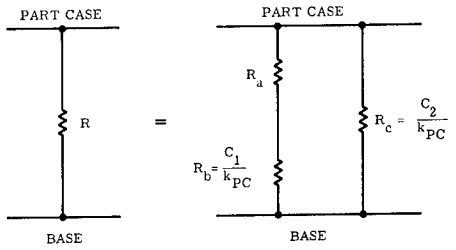
Fig. 1. Test program—Part IV: encapsulation evaluation test module.

RESULTS OF TESTS

Uniformly Powered Cordwood Modules

One group of tests that provided basic information for thermal correlation was performed with the 24-resistor module design shown on Fig. 1. These modules were built with $\frac{1}{8}$-W glass-cased resistors, and were potted in three different compounds after coating the parts with RTV 60. One compound MPC 52 was an alumina-filled epoxy with highest thermal conductivity, another of epoxy with a lower-density filler MPC 49, which has an accompanying lower thermal conductivity, and the third compound was 10 lb/ft^3 expanded urethane foam. Two modules were potted with each type compound. For each of these modules, the thermal resistances from the parts to the module mounting base were determined from the resistor power and the overall temperature rise of the parts above the base, after correcting for the heat lost by radiation and through the module leads. The resistance values, averaged among the parts of each module and between the two similar modules, are shown in Table I.

It was postulated that the thermal resistance to the base of each resistor could be divided into three components arranged according to the following diagram. R_a is the resistance of a part and constant for each module, R_b is in series with R_a and is inversely proportional to the



conductivity of the potting compound, and R_c is a parallel component also inversely proportional to the conductivity. After writing and solving the algebraic equations suggested by the above diagram, we find the resistance values shown in Table II for the three modules of Table I.

The 6-resistor module shown in Fig. 2, built with $\frac{1}{4}$-W glass-cased resistors, has also provided useful data. This design, with MPC 52 potting compound, yields an overall thermal resistance from part case to base of about 250°F/W per resistor, calculated from a 68°F temperature rise above base for a resistor to base heat flow of 0.272 W/resistor.

Note that the coarser spacing and larger size part has reduced the resistance by nearly 70% from that of the 24-resistor modules. In contrast, however, the power loading per square inch of module base area per degree temperature rise has also reduced as follows:

For 24-resistor modules

$$\frac{0.0273\ \text{W} \times 24\ \text{resistors}}{1.1 \times 1.1\ \text{in.}^2 \times 20°\text{F}} = 0.0271\ \text{W/in.}^2\text{-°F}$$

TABLE I

Potting Compound

Module	Density, g/cm^3	Thermal conductivity, Btu/hr-ft-°F	Thermal resistance to base, °F/W per resistor
MPC 52	1.31	0.24	743
MPC 49	0.66	0.09	1134
Foam	0.16	0.025	2077

TABLE II

Module	R	R_a	R_b °F/W per resistor	R_c
MPC 52	743	1185	123	1725
MPC 49	1134	1185	328	4600
Foam	2077	1185	1180	16550

For 6-resistor modules

$$\frac{0.272\text{ W} \times 6\text{ resistors}}{1 \times 1.5\text{ in.}^2 \times 68°\text{F}} = 0.0160\text{ W/in.}^2\text{-°F}$$

Thus the more nearly uniform module power distribution of the 24-resistor modules permits a higher power loading per unit module base area for a given part temperature rise, but the wider spacing and larger parts of the 6-resistor module permit a higher thermal loading of each individual part. In each of the above examples, radiation loss from the module surfaces and conduction along the power and thermocouple leads has been subtracted from the actual resistor power before the part to base thermal resistance was determined. Inclusion of these heat paths, present to some extent in every module, would decrease the overall thermal resistance. But since the strength of this secondary path would vary considerably with module hookup and installed environment, it seemed best to leave this path as an added thermal bonus or safety factor in the thermal data reduction.

When we attempted to modify the component resistances as given in Table II to fit the design of the 6-resistor modules, it was postulated that R_a should be inversely proportional to the part rating, R_b inversely proportional to the product of the potting compound thermal conductivity and the part rating, and R_c inversely proportional to the product of conductivity and the base area occupied by the part in the module. For the 6-resistor geometry, this would make

$$R_a = 1185 \times \tfrac{1}{8}/\tfrac{1}{4} = 593°\text{F/W per resistor}$$

$$R_b = 123 \times \tfrac{1}{8}/\tfrac{1}{4} = 62°\text{F/W per resistor}$$

$$R_c = 1725 \times 0.0504\text{ in.}^2/0.25\text{ in.}^2 = 348°\text{F/W per resistor}$$

as the MPC 52 potting compound was used in both modules. Use of these component resistances to calculate the overall resistor case to base thermal resistance yields

$$\frac{(593 + 62)348}{593 + 62 + 348} = 230°\text{F/W per resistor}$$

The good agreement between the resistance calculated above, based on modification of the 24-resistor module performance and the experimental value of 250°F/W per resistor previously mentioned for the 6-resistor module demonstrates the predictability of similar module designs using parts of a given type. Tests on other uniformly powered modules, with $\frac{1}{8}$-, $\frac{1}{4}$-, and $\frac{1}{2}$-W resistors potted in MPC 52 compound, but with different part spacings, have also shown that the above thermal correlation gives good agreement. However, the correlation does need to be confirmed for modules potted with materials that have thermal conductivities that differ from that of MPC 52.

Nonuniformly Powered Cordwood Modules—Results from 24-Resistor Modules

Although the results from the uniformly powered modules have been very interesting from the standpoint of developing an empirical understanding of the heat transfer process within an electronic module, most actual hardware modules are more likely to be spatially

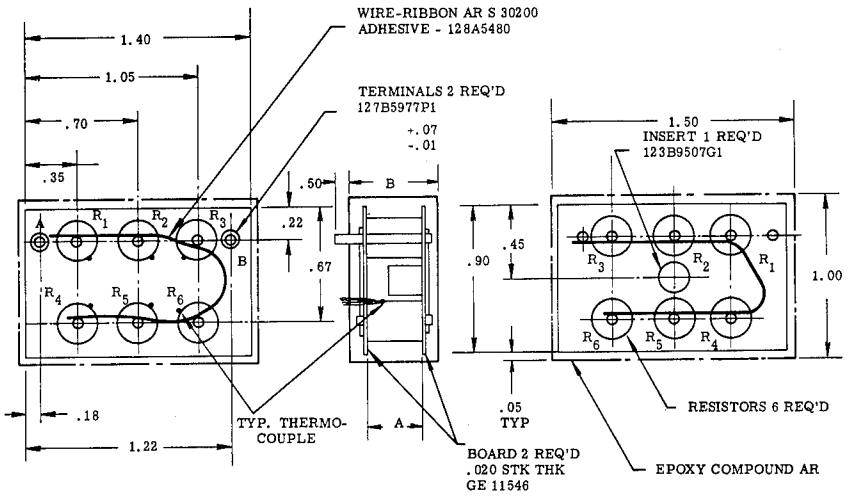


Fig. 2. Six-resistor test module.

nonuniform heat producers. Unfortunately, this author's efforts have covered only a small part of the work that needs to be done in this area before a broad understanding of the part temperature rise in nonuniformly powered modules can be developed. However, work to date has indicated some interesting avenues of approach.

During test of the 24-resistor modules described at the beginning of the previous section, some of the individual resistors were not powered for some test runs. These nonuniform power cases included runs with only three separated resistors powered to obtain isolated part data, with six resistors in one corner powered, and with alternate resistors powered. Typical temperature patterns for each of these cases are presented in Figs. 3 through 6, together with

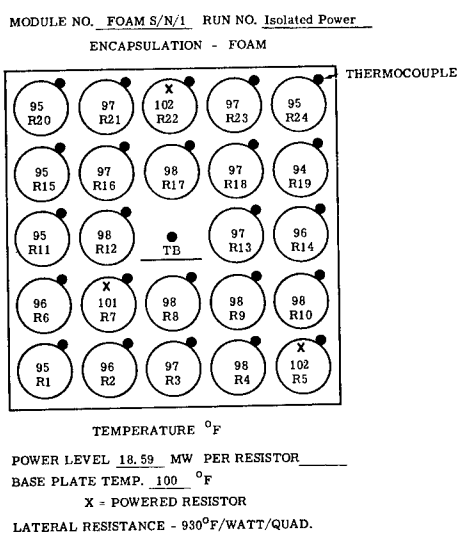


Fig. 3. Lightweight encapsulation test —isolated power.

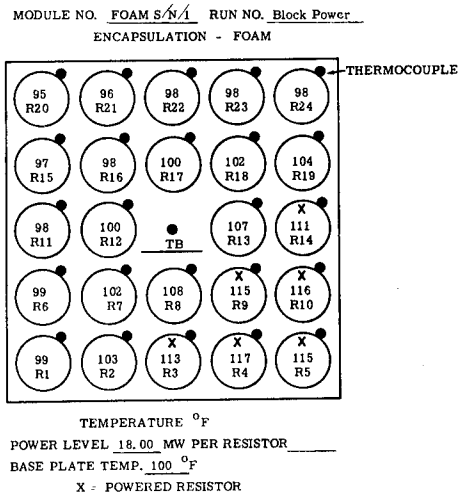


Fig. 4. Lightweight encapsulation test —block power.

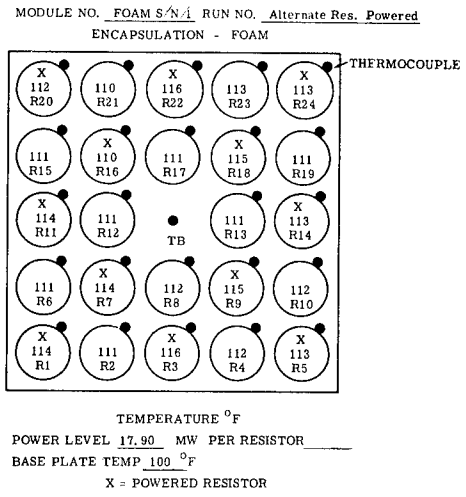


Fig. 5. Lightweight encapsulation test—alternate resistor powered.

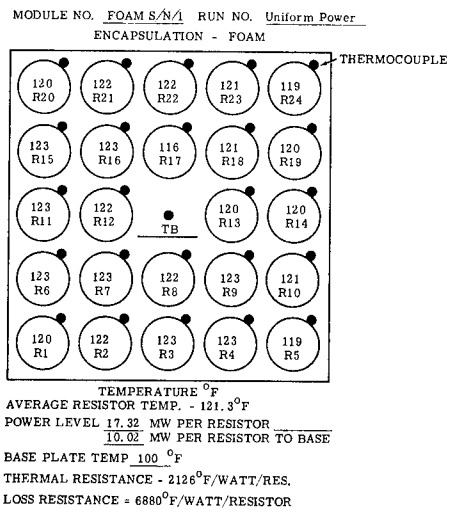


Fig. 6. Lightweight encapsulation test—uniform power.

the uniform power results for comparison. On the uniform power figure is shown the power in milliwatts generated in each resistor, and the calculated power per resistor transmitted to the base after subtracting the loss power defined previously from the generated power. Only the generated power is shown for the part power cases, as the loss power, although present, cannot be accounted for in such an easy fashion. The loss power per resistor can be readily computed, however, from the resistor temperature minus 75°F divided by the loss resistance value shown on the uniform power figure. Investigation of the strength of this secondary loss path has shown that, within the temperature limits measured, this loss is nearly linear with the resistor temperature rise above the module's surrounding environment, a bell jar held at about 75°F by the room ambient temperature.

The test results from the alternate powered resistor modules show that the thermal resistance from powered resistors to base has been cut approximately in half for the MPC 52 and MPC 49 modules, but has not been reduced at all for the foam modules. In each of these cases the external loss from all resistors is charged to the ones producing power in determining the heat flow from resistor to base. Computing the thermal resistance for these cases by using the component resistances from Table II, with R_c halved because of the increased effective base area per powered resistor, does not match the measured resistance values, although the trend of the computed values is in the direction of the measured values. For the modules with the two higher conductivity potting compounds, the calculated resistance does not fall as fast as the measured values.

An alternate approach that appears interesting is to introduce the concept of lateral thermal resistance. This resistance determines the ease with which heat can move laterally away from a part. An approximation to this lateral resistance is shown on the isolated power figure. This value was determined from the average temperature difference between an isolated resistor and its immediate neighbors and the amount of resistor power not accounted for by the sum of the external loss and resistor to base heat flows. The lateral resistance shown was the average of the values computed for the three powered resistors, assuming that heat could flow from a corner resistor through two quadrants, from a side resistor through three quadrants, and through four quadrants for an internal resistor.

Figure 7 shows a temperature pattern prepared for the block power distribution with the aid of a computer program using the loss resistance, base resistance, and lateral resistance

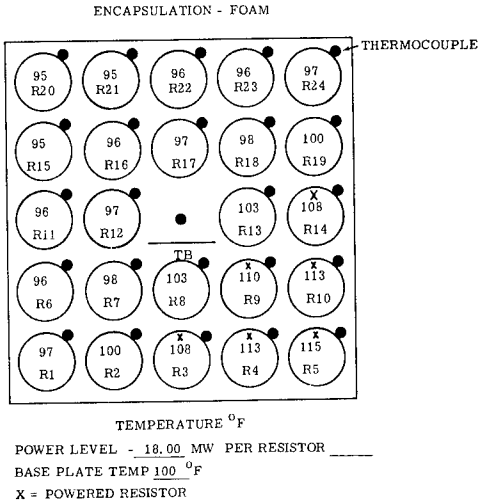


Fig. 7. Block power case computed from resistance data.

values from the foam module. Although the individual temperatures of this computed pattern differ somewhat from the observed values shown in Fig. 4, the computed values are close enough to give a designer a good reading on the thermal characteristics of his design.

Although the concept of lateral resistance appears interesting, it is hardly ready for widespread application. Sufficient work has not been done to prove the thermal diagram that relates lateral resistance to potting compound conductivity. Nor are data at hand that relates lateral resistance to part spacing and size. This area appears very fruitful for future investigation.

Results from 2 in. by 2 in. Modules. The MPC 52 potted modules shown in Fig. 8 have also yielded some nonuniformly powered thermal information. For instance E_1, a $\frac{1}{2}$-W resistor operating at 1 W was powered separately and produced a resistor to base thermal resistance of 42°F/W. This should be converted upward to about 52°F/W to put it on the same basis as the previously discussed modules, which included the thermal effects of a RTV 60 flexible buffer coating around the individual parts. The same resistance values can be calculated from the MPC 52 modules' results given in Table II after R_a and R_b have been corrected for the part size, and R_c corrected for an effective base area of four times the part radius.

The D_1 $\frac{1}{4}$-W resistor in this module is also quite isolated although it was powered with the other D and B resistors. The D_1 measured temperature and power produced a resistor to base thermal resistance of 80°F/W. Adjusting as before for the lack of buffer coating raises this value to 100°F/W. The thermal resistance of this resistor calculated from the Table II values after correcting R_a and R_b for resistor size and R_c for the effective base area of four times the part radius equals 95°F/W. Thus it appears that either size part makes good use of an effective base area equal to about sixteen times its projected area when the potting compound has a thermal conductivity of 0.24 Btu/hr-ft-°F. Expansion of this correlation to include other conductivity materials, and parts in other than vertical orientation with the base, is part of the job remaining to be done.

All the $\frac{1}{4}$-W D resistors were powered at 0.1 W each and the $\frac{1}{8}$-W B resistors were powered at 0.125 W each. D_2 and D_3, together with the B resistors, were grouped in one corner of the module, and produced the typical temperature values shown in Table III. From the temperatures and powers, averaged among the four similar modules tested, resistor to base thermal resistances of 160°F/W for D_2 and D_3 and 180°F/W for the B resistors were determined. These numbers would correct to 200 and 225°F/W respectively, if the effects of buffer coating were included. In attempting to calculate the thermal resistance values from previous tests, it would appear that 1.56 $in.^2$ is a reasonable area to assign to the above six resistors in the

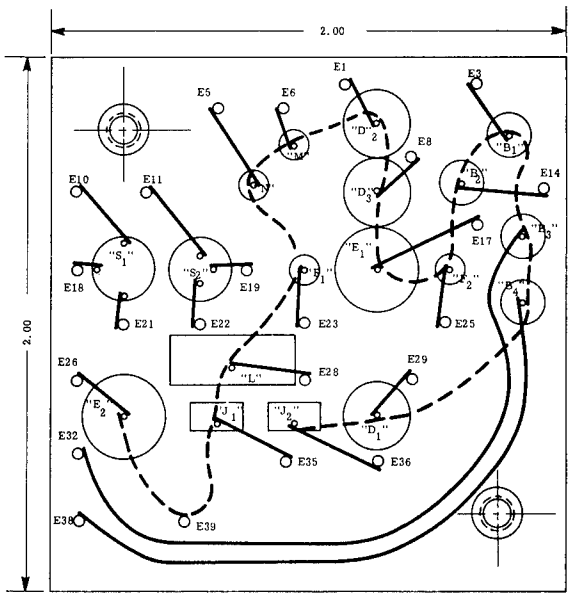


Fig. 8. 2 × 2 in. cordwood module. (Overall length of the module is 1.28 in.)

TABLE III

Part Temperature Rise above Mounting Base for Vacuum Tests of 2 × 2 in. Cordwood Modules*

(Mounting Base 100°F)

	1.0 W in E_1 Module Number		0.125 W each in B_1, B_2, B_3, and B_4 0.100 W each in D_1, D_2, and D_3 Module Number	
	CT01	CT04	CT01	CT04
B_1	112°F	112°F	123°F	125°F
B_2	114	120	125	122
B_3	114	115	122	126
B_4	113	115	119	121
D_1	112	—	108	—
D_2	114	117	115	118
D_3	122	121	115	117
E_1	140	144	111	110
E_2	104	104	101	101
F_1	—	119	—	106
F_2	122	121	113	117
J_1	105	—	102	—
J_2	107	107	104	105
L	—	111	—	104
M	110	112	107	109
N	110	109	105	105
S_1	104	103	101	101
S_2	106	106	102	102

* See Fig. 8 for configuration.

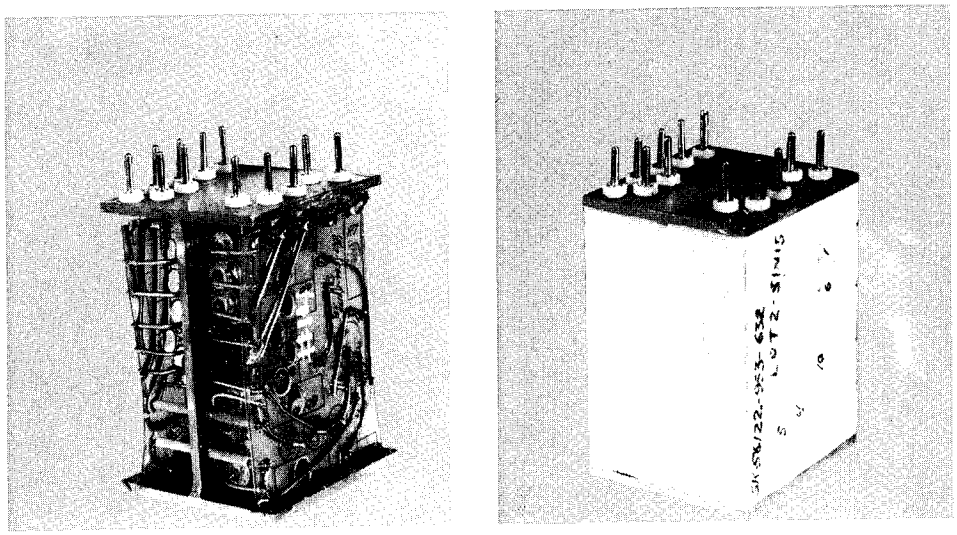


Fig. 9. Typical metal frame design—before and after encapsulating.

module. Correcting the data of Table II by that area divided equally among the resistors, as well as accounting for the $\frac{1}{4}$-W rating of the D resistors, yields computed resistance values of 221 and 266 for the D and B resistors. These values computed from Table II are not as much higher than the values based on the direct module test as the comparative numbers would indicate because no external loss was subtracted from the power generated in the 2 in. × 2 in. module's resistors. This loss was not measured and so is unknown, although believed small, and would actually increase the observed thermal resistance toward the calculated values.

Metal Frame Modules

In metal frame modules, the electronic parts are attached directly to a high thermal conductivity member (aluminum) which conducts the heat to the mounting base. A typical design is shown in Fig. 9. Since only a small portion of the part's temperature rise above the mounting base is due to the thermal resistance of the metal frame, parts can be stacked closely together without affecting one another's temperature to any appreciable degree. The beam flange makes a neat and solid support for the module pins. The foam encapsulant is soft enough to be removed if necessary to repair wiring or replace a module part, and its light weight results in an overall weight saving over high-power density cordwood modules that require the higher-density encapsulants. But the metal frame module does require some development.

The potential of the metal frame design is shown in Fig. 10. This module, carrying six $\frac{1}{4}$-W ceramic resistors, had a power loading per square inch of module base area per degree temperature rise of

$$\frac{0.272\ \text{W} \times 6\ \text{resistors}}{1.5\ \text{in.}^2 \times 17^\circ\text{F}} = 0.064\ \text{W/in.}^2\text{-}^\circ\text{F}$$

For comparison, the reader may recall the value of 0.0160 W/in.^{2}-°F for the six-resistor cordwood modules of the same base area. But in contrast to this fine performance, Fig. 11 shows a much lower level of thermal performance that results in a power loading factor of 0.0194 W/in.^{2}-°F, a value about equal to that of the previously mentioned cordwood module.

The module of Fig. 10 had three $\frac{1}{4}$-W ceramic resistors attached to each side of the web of the metal frame. Those on one side were attached by a rigid epoxy, and those of the other

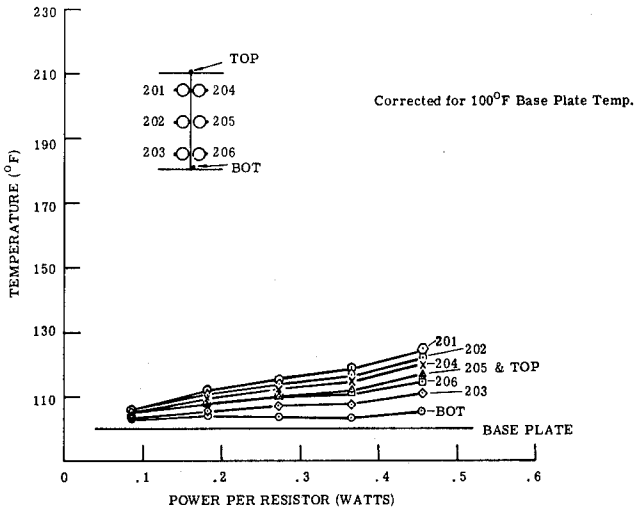


Fig. 10. Good metal frame thermal performance.

by a flexible adhesive, Pliobond. Either adhesive appeared to make a very good thermal connection between the part and the frame.

The module of Fig. 11 had three $\frac{1}{4}$-W resistors of the same type as the previous module on one side, and three $\frac{1}{4}$-W glass resistors on the other side. These glass resistors have smaller cases than the ceramic ones, and the cases are of lower thermal conductivity. Both sides used the flexible Pliobond adhesive, with the adhesive thickness greater on the ceramic resistor side. The reason the thermal performance of the module of Fig. 10 is superior is certainly not obvious.

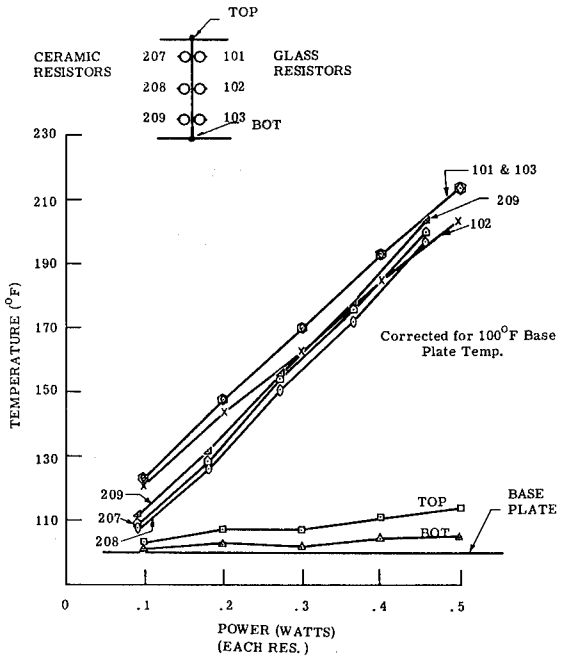


Fig. 11. Typical metal frame thermal performance.

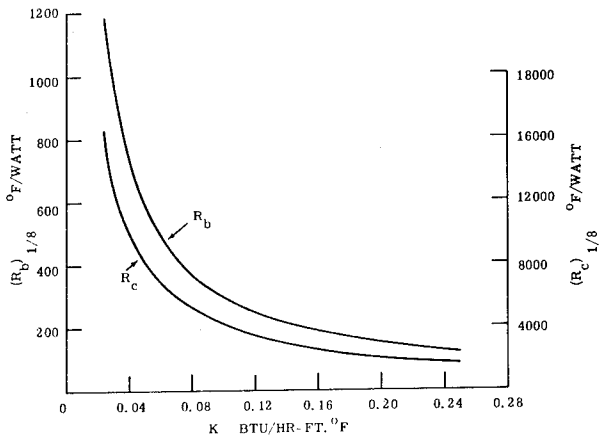
A development program is necessary to determine how to consistently produce modules with the better performance.

These few observations are about all that can be said about the thermal performance of metal frame modules at the present time. More work must be performed to develop the technique that will result consistently in improved thermal performance. When this technique is perfected, a considerable increase in packaging density can result, especially in components where low temperature rise is an important factor.

SUMMARY OF THERMAL RESISTANCE DATA

Figure 12 plots the component thermal resistance data for $\frac{1}{8}$-W glass-cased resistors in cordwood modules as a function of potting compound thermal conductivity. The accompanying component thermal resistance expressions permit adjustment for part rating and module base area assignable to the part. These expressions have conservatively agreed with all well-instrumented thermal data available, except for some part power runs with low conductivity modules. Caution is advised, however, as no checks have been made for modules potted in materials other than MPC 52, except for the modules used to derive Fig. 12. The resultant thermal resistances are applicable to parts coated with RTV 60 material, and may be reduced 20% if at the higher end of the conductivity scale, and if a buffer is not used.

Thermal performance information for metal frame modules is not presented because of the large spread in values. This type of module shows great promise for weight and space saving for high-power components, but the variable thermal resistance of the part attachment process must be corrected before this potential can be realized.



FOR APPLICATION TO OTHER MODULES

R_a = 148/part rating in watts

R_b = $(R_b)_{1/8\ Watt}$ x 1/8/part rating in watts

R_c = $(R_c)_{1/8\ Watt}$ x 0.0504 in.^{2}/A_p in.^{2}

$R = \frac{(R_a + R_b) R_c}{R_a + R_b + R_c}$

ΔT = Part Power (watts) x resistance °F

A_p = Part's proportional share of module base area

R = Thermal resistance from part case to base °F/watt/resistor

ΔT = Part temperature rise above base

Fig. 12. Component thermal resistances for $\frac{1}{8}$-W resistors with a module base area of 0.0504 in.^{2} per resistor.

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Some Practical Approaches to Thermal Problems in Airborne and Missileborne Electronics

PAUL F. ANDRUS
Minneapolis Honeywell Regulator Company, St. Petersburg, Florida

This paper discusses many of the more practical aspects of equipment cooling. Since many problems are imposed both by contract requirements and by designer inexperience, due consideration is given to minimizing their effect upon the program. In each case, the practical approach is stressed in the belief that the listener will find it easier to apply such solutions to his everyday problems.

INTRODUCTION

AS THE UNITED STATES improves her position of leadership in the field of missile and space-vehicle technology, national attention is more sharply focused upon the performance and reliability of our most advanced space systems.

Sharing in this increased attention, because of their acute effect upon performance and reliability, are the electronic systems and subsystems forming the nerve center of every advanced aircraft, missile, and space vehicle.

The role of the electronic packaging engineer in the design of these modern systems is assuming ever greater stature, year after year, because of the direct relationship between his efforts and system reliability. The competence of his design efforts in all packaging areas is borne out at each missile or space vehicle lift-off, orbit, and mission completion. Adequate and detailed thermal design, being a portion of this packaging effort, is becoming increasingly important in our modern electronic development programs.

Even as recently as the end of the Second World War, aircraft carried few electronic assemblies compared with the complex of electronic systems we know today. With the advent of supersonic speeds, air to cool these systems is no longer a readily available item, and often the cooling medium must be carried along and reconditioned after use within the vehicle.

Complicating the lack of cooling air, space limitations within a vehicle require extremely dense electronic packaging, making heat transfer by any means a difficult problem. In some installations provisions are made to remove heat from the electronic equipment by radiation cooling. This is most practical in a space environment.

The problems and complications of these types of cooling, both forced convection and radiation, are thrust upon the packaging engineer and have brought to him an acute awareness of the responsibility of adequate thermal design. The failure of even a small portion of one of the complex systems in a modern missile or aircraft can be the cause of the loss of millions of dollars worth of equipment. A much greater investment is represented in this complex, sophisticated equipment than could be imagined even a few years ago.

Setting aside all factors of equipment cost, one cannot ignore the possible loss of human life due to electronic system failure. Years ago, the simple electronic systems housed in an

aircraft were considered aids to the human pilot, and he could fly "by the seat of his pants" in the event of equipment failure. Today, however, even a slight failure or malfunction in a critical circuit may seriously risk the life of a pilot or astronaut.

While the problems of cooling (and the consequences of failing to cool) this modern equipment may seem to be unique to today's efforts both in Earth's atmosphere and space, the basic techniques of removing the thermal energy from the equipment has not changed. Conduction, convection, and radiation are modes of thermal transfer used by electronic equipment designers since the first hot component was packaged.

Today's problems probably require a closer study of each mode of thermal transfer, and how different modes may be combined to do a more efficient job. But the basic modes of transfer and the theoretical and analytical studies surrounding each are as valid today as ever.

It is the purpose of this paper to discuss methods and techniques of how to best utilize two of the basic modes of heat transfer to obtain the most efficient thermal design.

Certainly a background of electronic packaging, including the advanced state-of-the-art efforts being conducted at the Honeywell facility in St. Petersburg, Florida, is a significant experience upon which to draw for a discussion of this type. Serious thermal design efforts have been conducted at Honeywell, Florida, on such programs as the guidance systems for X-20 (Dyna Soar), Centaur, and Gemini. Such systems run the gamut of methods of cooling, but depend most heavily upon radiation and forced convection modes. These two modes, then, will be the scope of concern of this paper.

RADIATION COOLING

For space missions, radiation is often the only available means of finally disposing of heat from electronic equipment. To be sure, small conduction paths to the spacecraft exist at mounting interfaces but for purposes of design these are most often neglected. This assumption is reasonable in light of the small percentage of thermal energy likely to be transferred through these contacts and the uncertainty of the temperature or thermal capacity of the mounting area.

This lack of conduction paths away from the electronics package, plus the total lack of natural convection currents either inside or outside the equipment package while under zero gravity field, leave radiation standing alone as the one remaining useful method of heat transfer to space environment.

For any given size and shape of electronics package, the magnitude of heat transfer by radiation depends upon two factors. First, the built-in factors of emissivity and absorptivity of the package surface, and of the surfaces "seen" by the package. These coefficients will determine the efficiency of radiative transfer both to and from the package. Second, the difference in the absolute temperatures of the package and its surroundings. This second factor varies as the fourth power of the absolute values and is often not under control of the package designer.

Given that size and shape are not changed, and that surface finish absorptivity and emissivity remain fixed, then radiation of a given number of watts requires a certain minimum temperature difference between package and surroundings. If this temperature difference will not provide minimum thermal transfer required to maintain safe component temperatures within the electronic assembly, then some one of the previously fixed conditions, size or surface emissivity, must be altered.

CONDUCTION—ITS ROLE IN SPACE

In packages using radiation as final heat disposal, thermal conduction is most often used to transmit the energy to the outer surface through the structure. Since the outer skin temperature is determined by the amount of heat radiated from the package, and the factors mentioned earlier, it is important to keep the temperature differential over the conduction path as small as possible. A high temperature differential ΔT between components and outer skin means a higher component temperature which is a detriment to component life and reliability.

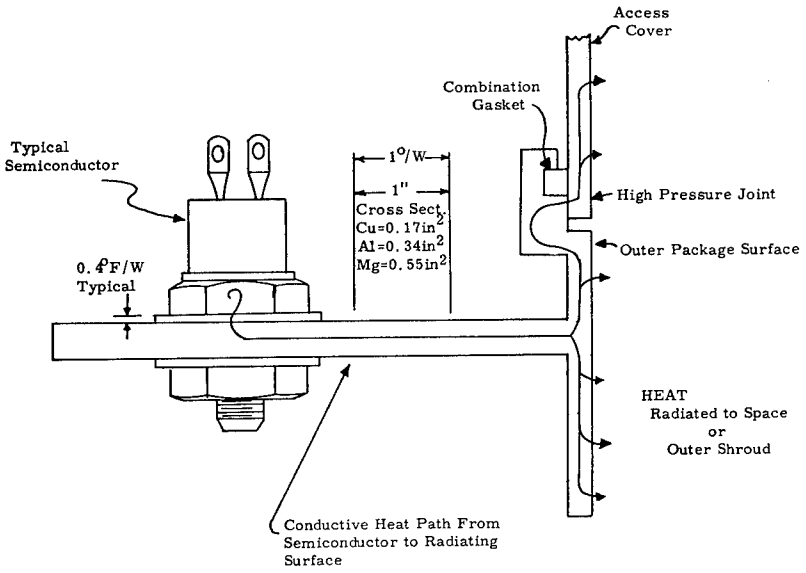

Fig. 1

Excellent conduction paths between heat-producing components and outer package surface are essential and usually not easily achieved. Because of weight considerations, conducting cross sections are sometimes smaller than needed, and because of structural joints, the thermal paths are not always solid and of low resistance. Some of these problems are illustrated in Fig. 1.

The electrical analog to thermal resistance is helpful in understanding the need for adequate design of the conduction paths within a package. A network of thermal conducting paths, as in an electrically conducting network, can be broken into several sections, each of which has a value of length, cross section, and thermal conductivity. The thermal resistance of each section is R_T.

$$R_T = \frac{\text{Length}}{\text{Cross Section} \times \text{Thermal Conductivity}}$$

The thermal resistances of the sections are then combined by the series and parallel laws of electrical resistance.

This process of analysis can show clearly where one of several conduction paths through solid material is inadequate. It will not point out, however, the large ΔT's which occur at poorly constructed joints in the thermal path. Every interface between structural parts requires a high pressure or better, a fused contact (as solder is used at an electrical joint to reduce voltage drop) to reduce ΔT. A gap or air film measuring only a few ten thousandths of an inch can cause a ΔT as large as that produced by several inches of conducting metal. Materials whose surfaces are to be joined should be machined flat, protected with noncorrosive film finishes, and are best if slightly malleable and closely bolted. It is often possible to thermally improve two joined surfaces using epoxy cements or silicone greases to eliminate the air gap.

The thermal resistance analog will also point up the rather large cross sections of metals which are required to transmit several watts of thermal energy with a small ΔT. Most solid-state modules used in spacecraft have very small heat output, but power stages are also used and they require generous structures to conduct their dissipated heat to the outer radiating surface.

Figure 2 shows the cross-section area in square inches necessary to conduct a certain number of watts of heat flow through a 1 in. length of copper bar with a certain ΔT along the

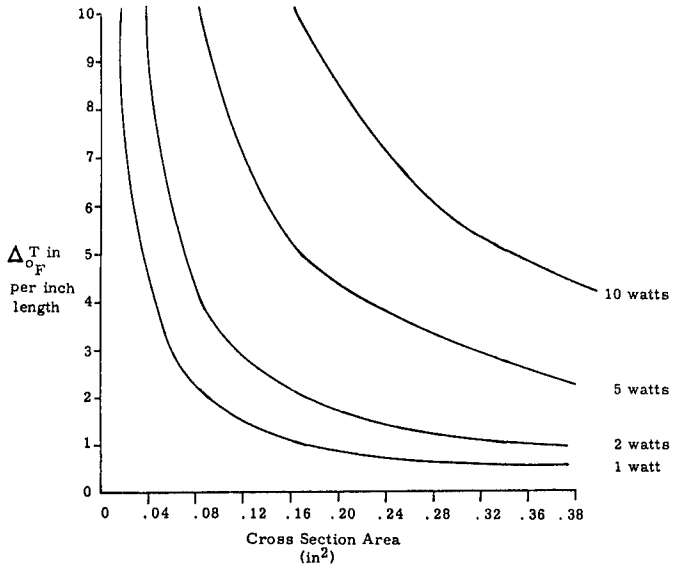

Fig. 2. Temperature rise (ΔT) *vs.* thermal conductor area of copper.

1 in. length. For a common power semiconductor dissipation of only 5 W, for example, it is seen that 0.17 in.^{2} of copper is required to keep ΔT to 5°F in each inch. Transporting this heat only 5 in. to a radiating surface will cause a 25°F rise, which is then aggravated by the problem of interface losses. A typical metal–mica–metal insulating joint in the structure, or under the semiconductor, will produce at least 4°F in addition.

Since copper has a thermal conductivity twice that of aluminum and magnesium, the total ΔT loss in our example case would be 52°F for an aluminum structure, even assuming only one joint. The example cross section of 1 in. by 0.17 in. is the smallest path that could be considered here, and yet is larger than the "thermal ground straps" used in most equipment. Changes in ΔT per inch of length with a change in material are shown in Fig. 2.

Another area of package design which requires careful application of the conductivity rules is outer surface walls. The heat generated by package components can be brought out to the radiating surface quite efficiently using the techniques outlined above, but it is necessary to distribute the heat flow throughout the surface. Without good conductivity in the outer package walls, hot spots will exist at the junctions of structure bulkheads and outer walls, with colder spots in between.

The temperature difference between these spots will not affect the radiating efficiency greatly because both cold and hot areas of the package surface are quite hot relative to outer space temperature. However, if radiation to a surface such as the spacecraft structure must be considered, then the cold spots will reduce the overall radiation effectiveness as they may almost match the temperature of the structure. In either case, hot spots will cause the package interior to be hotter, since the hot electrical components must be conductively cooled to the outer surface, which is now locally at a higher temperature.

Cold spots are the result of poor conduction in a wall section or through joints which are not good heat paths. Access covers on electronic packages are a prime example of the latter. Gasketed covers can be sealed against magnetic and radio frequency interference and environmental conditions, and still be thermally isolated unless a large-area high-pressure metal-to-metal joint is provided. Combination RF and environmental gaskets are not sufficient to distribute heat to the gasketed cover.

SURFACE FINISH—ITS ROLE IN SPACE

A final and most important factor in heat elimination by radiative transfer to the environment is the use of a proper surface finish. Selection of a finish is governed by the environment and by handling considerations during assembly, test, and prelaunch operations. Space is assumed to be the environment in this discussion because radiation cooling is usually chosen only for service above the atmosphere.

The radiating finish chosen must not deteriorate or evaporate when exposed to space environment since any such change would alter its radiation characteristics when exposed to space environment. If an organic finish is used, it must be formulated with a vehicle that will not discolor or sublime at zero pressure and temperatures up to 200°F. Its pigment must be stable under ultraviolet and cosmic radiation. Most plain metal finishes are very durable in space but must be protected before launch. Anodizing or passivating the metal gives surfaces resistant to change, but in common with plain metal finishes they do not have desirable emission and absorption properties and are difficult to change once the package is built. Ceramic depositions and ceramic/organic combinations form another important category of surface finishes for radiation and they are quite resistant to deterioration.

The other environmental consideration when selecting a finish is its radiation characteristic. Packages which must operate within the shroud or confine of a spacecraft have a difficult problem in achieving heat transfer from the package to the shroud, which may even be at a higher temperature than the package. Packages which radiate directly to space often have an opposite problem–that of reducing outward radiation to keep package temperature from going too low. Solutions to these problems lie in proper selection and ratio of the emissive coefficient and the absorptive coefficient.

These coefficients are sometimes listed as scalar values but must always be qualified as to wavelength. An emission function of a surface can show differences in level of emissivity at different wavelengths. Because of this, a finish can be selected to emit more efficiently at the wavelengths of concern.

Absorptive functions also vary with wavelength, and often a surface with very low absorptivity to the sun's energy will be highly absorptive to thermal energy from an adjacent electronic package. The difference lies in the wavelengths radiated from each. Wavelengths radiated from the sun and from an average electronics package are shown in Fig. 3.

Both shape and value of the absorption function are dependent upon the type of surface finish, and its roughness, chemical composition, and even its cleanliness. Packages that are subject to space environment must have finishes whose characteristics are not easily altered by micrometeorite erosion and ultraviolet radiation.

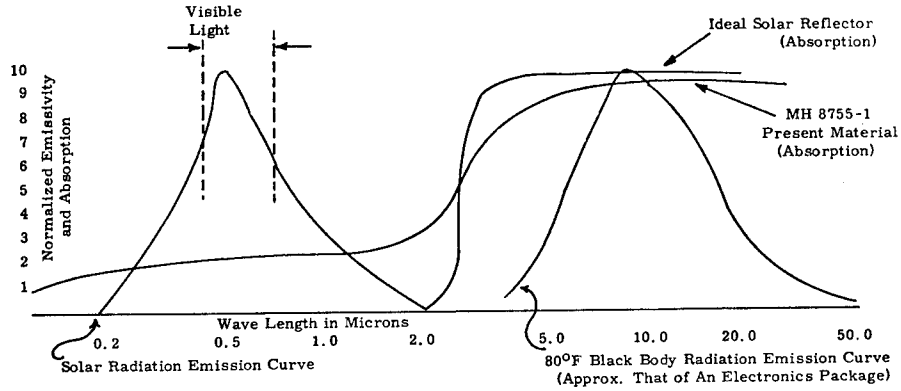

Fig. 3. Explanation of temperature control properties of a solar reflector finish.

The four general classes of finish mentioned earlier emit generally as follows: the organic paints such as Honeywell specification MH8755-1 (MIL-C-27227, coating, polyurethane, thermal resistant) are weak absorbers of incident solar radiation but emit strongly in black-body fashion as shown in Fig. 3. The plain metals, such as polished aluminum or deposited gold, are strong solar absorbers and weak flat emitters (flat meaning similar to a black body.) The black anodized surfaces emit much more strongly in general but individual analysis is required because of the interference effect present; and the ceramic coatings, used mainly where heating is present in re-entry, are strong flat emitters.

Electronic packages which create internal heat and are at least partially shrouded by the spaceframe should use a high-emittance, low-absorption coating to dissipate their heat in the most efficient manner to their surroundings, whose average temperature can be quite high compared to space. Discussion of the shape, orientation, orbit path, and other factors which strongly affect temperature control on unshrouded bodies such as satellites and spacecraft is not within the intended scope of this paper.

HISTORY OF 706

Several programs involving thermal cooling by radiation to space have been completed at Honeywell, Florida. One which incorporates many of the design features just discussed is the 706 Program, involving the design of a system composed of several units, one of which is a *digital coupler*.

The coupler as a unit was required to dissipate approximately 200 W of power entirely by radiation to space environment. The equipment was mounted, however, on a shelf of the supporting vehicle and so received radiated energy from other pieces of equipment.

A further thermal restriction was imposed by the need for large removable covers both on the top and bottom of the equipment package. A gasketed interface, required between the covers and the main housing, drastically reduced the thermal conductivity between the covers and the housing. With this requirement it was realized that variations in the skin temperatures of the entire package, including covers, would be severe.

Among the thermal design features incorporated in the equipment were low-impedance thermal paths from the heat sources to the equipment case. These paths were maintained in several ways, one of which is shown in Fig. 4. In this instance a power transistor was mounted in a cuplike heat sink, which was then cemented with an epoxy resin to the coupler case. Such a mounting provided several important requirements for low impedance thermal paths:

1. Large cross-sectional area through the heat sink itself.
2. Large contact area where epoxy resin was used to mount to the coupler wall.
3. Short length of thermal path from the heat sink to the wall.
4. Transistor body faces coupler wall for maximum radiation of heat from transistor to wall.

Another equally important rule of good thermal design is incorporated in this equipment and is also shown in Fig. 4. This is a heavy cast section in the outer wall of the case to readily conduct heat away from the area of the power transistor. As the distance away from the power transistor increased, the wall thickness became progressively thinner, unless the heavier section was required for structural strength. This provided a relatively constant cross-sectional area of material for thermal transfer away from the higher-temperature area. This practice has done much to reduce hot spots on the coupler surface.

A third area of thermal importance was planned for by the design of the outer surface finish of the coupler. From previous programs we had knowledge of the emissivity and absorptivity factors of several finishes. One of these is the white polyurethane paint per MIL-C-27227 mentioned earlier, and has to its credit an emissivity factor of 0.94 at approximately 10 μ, and an absorptivity factor of only 0.24 at approximately 0.5 μ. Use of this material as a finish permitted nearly ideal radiation from the coupler package to a colder medium, while permitting less than 25% of the theoretical maximum amount of energy absorption from the sun.

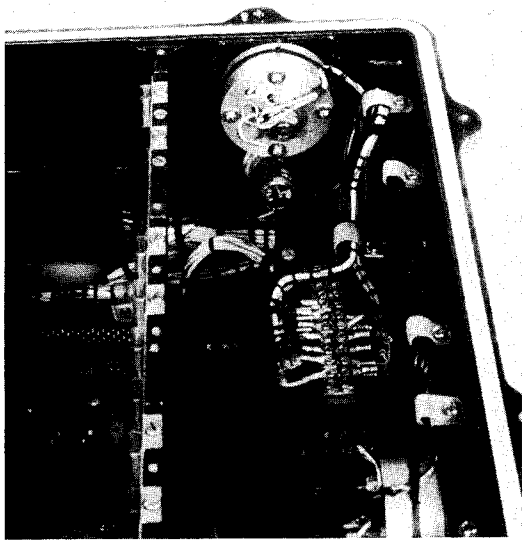

Fig. 4

The study effort for other programs and for the 706 program which determined the choice of a finish also produced interesting sidelights. For instance, it is equally possible to maintain a package at a higher temperature than normal by using a finish of gold plate which has a very low emissivity factor. Also, many interesting combinations of gold plate and the previously mentioned polyurethane finish can be used to control surface temperatures and reduce hot spots on equipment relying solely upon radiation for cooling.

It would, of course, be desirable to be able to perform a very thorough thermal analysis of all modes of heat transfer encountered in a piece of equipment. Unfortunately, most often the short duration and limited manpower and dollars available for the performance of a complete design forces the use of "standard" or "proven" thermal design techniques in hopes they will prove satisfactory again.

In a piece of radiation cooled equipment, however, the thermal analysis is not such a demanding effort as long as safe simplifications are made and only the mode of radiation cooling considered. This approach will provide reasonably accurate results and will prove satisfactory in most cases.

The appendix to this article is a thermal study made upon a Honeywell digital coupler. It shows that the case temperature after 3000 sec should average out to be approximately $+136°F$. It shows a real attempt to predict the case temperature at the ends of various time intervals of the flight program, inasmuch as the environmental conditions did change during flight.

The inclusion of the calculations for interim periods of time throughout flight made the calculations more lengthy than they otherwise might be. However, this effort is included here to show the possibility of developing a quick and reasonable thermal analysis during the earliest phases of a design program.

The proof of the success of the design effort and the accuracy of the calculated thermal results lies in the results of the thermal test program. On this program, the coupler was operated in a space chamber with ambient conditions of $-30°F$ and 50 μ pressure. After one-half-hour operations, the hottest case temperature was found to be $+145°F$ and the coolest case temperature was $+85°F$. These values were determined by surveying areas of the surface of the package including the somewhat thermally isolated covers. The average of these temperatures —$+115°F$—compares reasonably well with the calculated value of $+125°F$ after 1800 sec of

operation. The difference is probably due to the high thermal load assumed to occur during the early portions of the flight.

During the test, interior temperatures were found to be well below maximums. The hottest component within the entire unit was found to be a carbon resistor with a body temperature of +220°F. Among semiconductors, which are some of our most temperature-sensitive devices, the hottest case temperature was found to be +190°F, again well under our maximum limits.

The successful completion of this test program was demonstrated proof of adequate thermal design. The test was performed under simulated space conditions which, if anything, were slightly more severe than those to be encountered in actual space in that the chamber ambient temperature was considerably higher than the +4°R of space.

Further proof of adequate thermal design procedures is to be found in the recorded temperatures. All were well under acceptable upper limits, showing a reasonable factor of safety in the thermal design. Case temperature variations from hottest to coolest temperatures show a reasonable heat conductivity through and along the length of the case walls. Attention to the details of good thermal design as outlined earlier paid off in the design of this Honeywell coupler.

FORCED CONVECTION

One of the most practical methods of removing the heat generated in airborne electronic assemblies is by the technique of forced convection. This method of cooling has been widely used in aircraft and missile applications in years past and will no doubt continue to enjoy the same degree of popularity for future designs.

Miniaturization and the resultant increased concentration of thermal energy have aggravated the problem of cooling. The techniques of forced convection cooling of 20 years ago are no longer compatible with today's requirements. A more sophisticated approach to the problem of forced convection cooling is required to optimize equipment performance using a limited quantity of cooling air.

It should be emphasized that a purely theoretical mathematical approach to the problem of forced convection is not intended for this paper. Basically, there are two reasons for not pursuing this approach. First, most thermal problems encountered in today's applications will require many assumptions and modifications which will vary considerably from one situation to the next. While this does not invalidate the theoretical approach, it does make the practical approach more desirable. Secondly, almost any good heat transfer text book will treat the theory of forced convection in sufficient detail to allow the reader to obtain an understanding of the basic equations involved.

This is not to imply that the package designer should avoid the analytical approach to forced convection heat transfer. On the contrary, it is suggested that an analytical approach be developed at the beginning of each design. Frequently, the results of such an investigation will point out the presence (or absence) of problem areas and serve as the basis for making future decisions as the package design develops through the layout stages.

Once the thermal problem areas have been determined either by analysis or by testing of a mock-up, the next problem which confronts the designer is maximum utilization of available cooling air. Today's high-performance missiles and aircraft have available only a meager amount of cooling air, which is conserved and recycled through the heat-producing electronics. Consequently, the keynote for forced convection cooling in present airborne applications is *utilization* of available cooling air.

In order to achieve the maximum utilization, careful attention must be directed to certain details during practically all stages of development from layouts to test completion. Some of the more important design criteria for forced convection cooling are discussed below:

1. Incorporate good heat-sinking techniques for semiconductor devices. This applies whether the engineer designs the dissipator or elects to use a commercially available one. In either case, the dissipator specified must function efficiently in forced convection cooling applications at the specified ambient temperatures for the particular design. Caution should

be observed in the preliminary selection of a semiconductor heat dissipator since the manufacturer's data sheet or curves are usually based on tests conducted at *room-temperature* ambients. High-temperature ambient conditions will require careful consideration of the performance characteristics stated for a given dissipator.

2. Careful design of air ducts including sizing and routing so that the correct air mass is conveyed as directly as possible and at the desired velocities and pressure drops to each of the units which require cooling.

3. Avoid sharp bends, turns, sudden enlargements and contractions, and obstructions in the ducts which direct the flow to individual subassemblies.

4. Balance the total coolant distribution in the system in accordance with the individual thermal loads to make sure that each subassembly unit gets the correct mass flow of cooling air at the required inlet temperature.

Generally speaking, systems involving a common air supply plenum and parallel flow to different subassemblies will present the necessity for performing an accurate air flow balance. Unless careful attention is given to the regulation of air flow, it is entirely possible for one or two units to get more than their "fair share" of the cooling air. Each subassembly air discharge or air inlet must be adjusted in size such that the air mass flow can be accurately balanced while the system is under test. This technique will help assure the proper distribution and best utilization of air flow under normal operating conditions.

5. Always route or direct the cooling air through any enclosed subassembly package so that it "scrubs" all interior package surfaces. This will not only take care of existing hot spots, but will provide some safety factors for future changes which may involve additional heat-producing components.

6. Once the desired air paths for maximum utilization have been determined, the designer should make a concentrated effort to keep these flow paths free from obstructions. For example, a last-minute change may require the addition of a panel or cable which would block off a coolant path. Fortunately, most cases of this nature have an alternate solution if an effort is made to find one.

7. Proper design of joints, covers, and gaskets is another important phase of designing for maximum air utilization in forced convection cooling applications. Obviously, cooling air cannot be utilized to maximum extent if it is allowed to lead through poorly designed joints, covers or gaskets.

Such a summary as presented above involves no new or unique approach to designing for forced air cooling. Obviously, a satisfactory design for this method of heat transfer cannot be achieved by concentrating only on one of the foregoing details and neglecting the others. It should be emphasized that an ideal design and good utilization will result only when "across the board" application of all factors is realized.

HISTORY OF X-20

Several programs involving thermal cooling by forced convection have been completed at Honeywell, Florida. One of these programs which incorporated many of the desirable design features just covered is the X-20 (Dyna-Soar) guidance system. A review of the coupler electronics unit designed and built for this program will illustrate these points.

Of primary importance to the thermal design of the entire X-20 (Dyna-Soar) guidance system was the requirement that cooling air be utilized at a rate not to exceed 4 lb/min per kW of power dissipated. When this requirement was applied to the coupler electronics unit with a dissipation of nearly 800 W, the unit was limited to 3 lb/min of cooling air.

Another universal requirement for the entire system was that all units be designed to be capable of receiving their rated amount of cooling air flow at a pressure head of 2 in. H_2O above ambient. Discharge of this coolant was to be to the ambient.

In order to meet these design requirements and to best perform the entire heat transfer program, several design approaches were taken.

First, the entire coupler unit shown in Fig. 5 was designed so that all subassemblies within the unit would receive air directly from the supply plenum. In this manner, no one assembly

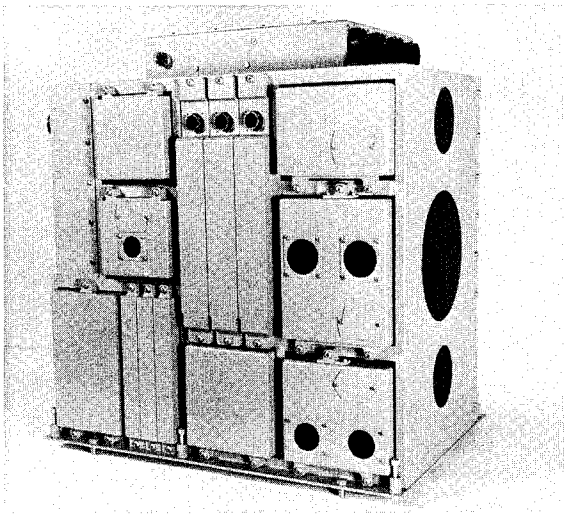

Fig. 5. Dyna-Soar coupler electronics unit.

would receive air at an elevated temperature due to the previous use of the air to cool another subassembly. Furthermore, by arranging the subassemblies in this parallel manner, any one of them could be removed from the coupler unit, the air discharge opening sealed, and complete electrical operation of all remaining units continued without fear of overheating. This approach is favored over a type of series flow in which coolant passes from one package to the next. In such a scheme, removal of one unit interrupts coolant flow for all following subassemblies (see Fig. 6).

Secondly, careful attention was given during the coupler design phase to assure unrestricted airflow passage through all supply ducts to the assemblies. This is especially important in order to minimize the pressure drop between the coupler interface with the vehicle cooling air plenum and each subassembly. Introduction of obstacles to airflow in this area could well

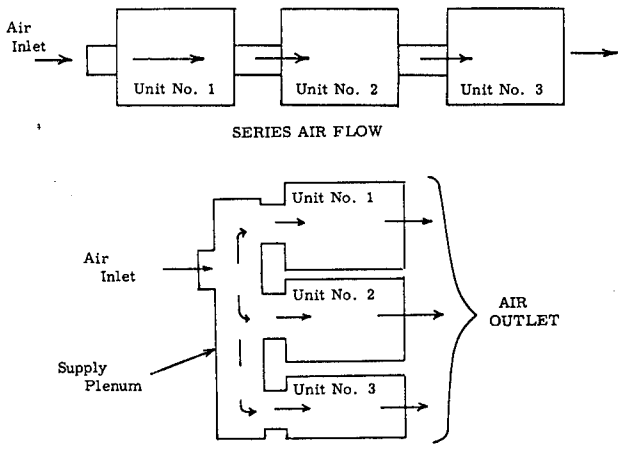

Fig. 6

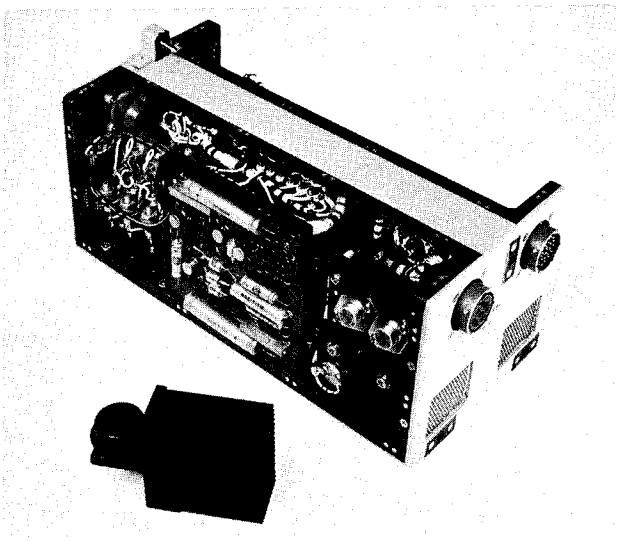

Fig. 7

have upset calculated values of orifice dimensions needed to control the airflow through each subassembly. These orifices were to be placed at each subassembly cooling air discharge in order to establish both total weight flow of cooling air through the coupler and to set up the rather delicate balance of weight flow between subassemblies.

Third, and equally important with the distribution of the cooling air supplied to the entire coupler, is the distribution technique used within the subassemblies. In each X-20 (Dyna-Soar) coupler subassembly the cooling air was routed through all areas of the package. This was done by a compartmentalizing of the subassemblies and the passage of the cooling air through these compartments one after another. In some subassembly units, the problems of such routing were minimized by introducing cooling air at more than one location. In this manner, all surfaces of the subassembly package were scrubbed thoroughly by cooling air. Heat was picked up from those surfaces to which heat generating components were mounted, but all surfaces were cooled and so were available for component mounting as future electrical design changes occurred.

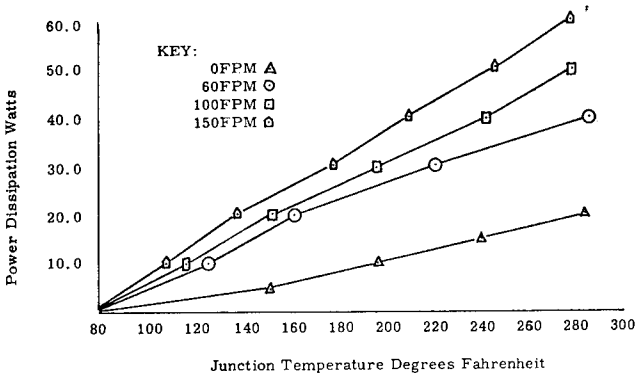

Fig. 8. Power dissipation *vs.* junction temperature curves at air flows from 0–150 fpm for 2N1016A transistor mounted in astro dynamics 2401 heat sink less mica washers. (Note: cooling air at room temperature.)

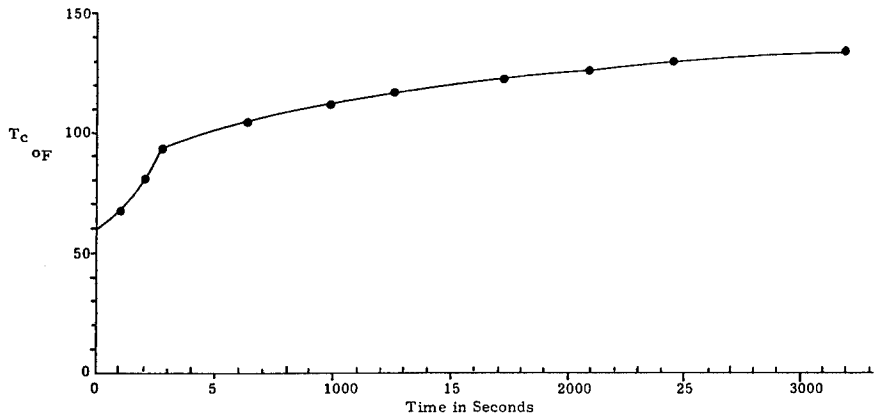

Fig. 9. Honeywell coupler case temperature through duration of flight-coupler painted white.

The X-20 (Dyna-Soar) coupler design program provided the opportunity for a rather complete study of transistor heat dissipators available commercially. These dissipators were required in the coupler design largely in the power supply subassemblies, one of which is shown in Fig. 7.

The tests were conducted under varying power dissipation levels and varying cooling airflow velocities. In this manner, a family of curves were generated for each dissipator tested; and, as the coupler design progressed, it was possible to choose the proper dissipator to be used in a given situation. A sample of such a family of curves for the dissipator shown in Fig. 7 is contained in Fig. 8.

As this paper is written, no thermal or airflow tests have been completed upon the coupler unit. Many hours of satisfactory operation under systems test have been completed, however, with cooling air supplied at room temperature and in amounts exceeding the required 3 lb/min.

A high degree of confidence exists in the ability of this equipment to perform to specification with the minimum allowable coolant. This optimism exists primarily because of the thorough thermal test program and design effort which was performed during the early phases of the program.

The past experience gained by Honeywell, Florida, engineers on programs such as 706 and X-20 (Dyna-Soar) has resulted in some basic approaches and a few deep-seated beliefs about thermal design that are worth discussion.

The basic approaches can be summarized in the following points and in their order of occurrence during a design program:

1. Analytical thermal investigation to determine the severity of the cooling problem.
2. Determine the best approach to cooling from those available; usually forced convection or radiation.
3. Construct a thermal mock-up which incorporates the final form factor and a realistic thermal load.
4. Test both the mock-up and any proposed special dissipators under worst case conditions of temperature and pressure.
5. Incorporate the necessary design changes in the final unit.

It is impossible to give more weight to the importance of one of these over another. They all combine to make up "thorough design," and so cannot be placed in order of importance.

Supplementing these approach points are some axioms which have come to be so meaningful to the success of any thermal design at Honeywell, Florida. While these thoughts may

seem to be self-evident, they are, none the less, fundamental and capable of standing considerable repetition.

1. The approach to thermal design is no mystery. Definite, scientific, orderly laws of thermodynamics and heat transfer are at work and if properly followed will remove the mystery from thermal problems.
2. Thermal design should not be a hit-or-miss effort. It is important that equal consideration be given to all potential thermal problem areas. None will disappear because they are ignored.
3. To ensure a successful design, make a careful approach to the use of the basics of heat transfer. Even though the thermal problems encountered may seem to be more severe than ever before, the same basics of heat transfer will solve the problem.

All these points are of maximum value to the designer only if the thermal "design loop" is closed, allowing him to learn just how successful the design is. If left to normal procedures, it may be years before field service reports or some other method of communication will allow him to learn these results. The better answer is to perform a thorough test program on the completed design after final unit assembly and electrical check-out are complete. During such a test, a thorough temperature survey will indicate the success of the overall design and the accuracy of the earlier test and analytical design work.

APPENDIX: HEAT TRANSFER ANALYSIS OF HONEYWELL COUPLER

1. Conditions:

a. Coupler case all (100%) white paint, per MIL-C-27227 ($\alpha = 0.24$, $e = 0.94$)
b. Box (case) will be cooled to 60°F (average) prior to launch by use of 40°F cooling air at the rate of 3 lb/min.
c. Heat will be absorbed by case from shroud during first 276 sec of flight. Shroud temperature during this time will vary.

2. Heat absorbed by case during first 100 sec of flight. It can be assumed shroud is at an average temperature of 250°F.

$$Q = 0.173A\alpha\left[\left(\frac{T_s}{100}\right)^4 - \left(\frac{T_c}{100}\right)^4\right]$$

where A is the area of case exposed to radiation. Assume this to be 3.85 ft^2; α is the absorptivity of finish = 0.24; T_s is the temperature, absolute, of the shroud. Assume to be 250°F or 710°R; T_c is the temperature case of coupler, absolute. This is 60°F or 520°R at start of run and

$$\begin{aligned} Q_1 &= 0.0173(3.85)(0.24)[(710/100)^4 - (520/100)^4] \\ &= 0.667(0.24)[2550 - 680] \\ &= (0.667)(1870)(0.24) \\ &= 299 \text{ Btu/hr} \end{aligned}$$

The heat from internal electronics is

$$Q_2 = 200 \text{ W} \times 3.42 = 684 \text{ Btu/hr}$$

Total heat rate into case while under the shroud is

$$Q_1 + Q_2 = 299 + 684 = 983 \text{ Btu/hr}$$

Total Q during first 100 sec of flight is

$$Q_t = 983 \times 100/3600 = 27.3 \text{ Btu}$$

Temperature of case after first 100 sec is

$$Q_t = WC_p\Delta T$$

Solving for ΔT, we get

$$\Delta T = Q_t/WC_p$$

where W is the weight of the case (13.6 lb) and $C_p = 0.25$.

$$\Delta T = \frac{27.3}{13.6 \times 0.25}$$

$$\Delta T = 8.03, \text{ or call it } 8.0°\text{F}$$

Temperature of the case after 100 sec of flight is

$$520°\text{R} + 8.0 = 528°\text{R}$$

3. Heat absorbed by case during second 100-sec interval of flight: T_s for this period is 450°F or 910°R. Case temperature T_c is 528°R.

$$\begin{aligned} Q_1 &= 0.173(3.85)[(910/100)^4 - (528/100)^4]\alpha \\ &= 0.667[6900 - 780]\alpha \\ &= (0.667)(6120)(0.24) \\ &= 980 \text{ Btu/hr} \end{aligned}$$

Heat from internal electronics is

$$Q_2 = 684 \text{ Btu/hr}$$

$$Q_1 + Q_2 = 1664$$

$$Q_t = 1664 \times 100/3600 = 46.3 \text{ Btu}$$

Temperature of case after second 100-sec interval is

$$Q_T = WC_p\Delta T$$

$$\Delta T = \frac{Q_t}{WC_p}$$

$$\Delta T = \frac{46.3}{13.6 \times 0.25} = 13.6°\text{R}$$

Temperature of case is

$$528°\text{R} + 13.6 = 541.6°\text{R}$$

4. Heat absorbed during the last 76 sec:

$$T_s = 500°\text{F} = 960°\text{R} \text{ and } T_c = 541.6°\text{R}$$

$$\begin{aligned} Q_1 &= 0.173(3.85)[(960/100)^4 - (541.6/100)^4]\alpha \\ &= 0.667[8520 - 865]\alpha \\ &= (0.667)(7655)(0.24) \end{aligned}$$

$$= 1225 \text{ Btu/hr}$$

$$Q_2 = 684 \text{ (from internal electronics)}$$

$$Q_1 + Q_2 = 1909 \text{ Btu/hr}$$

$$Q_t = 1909 \times 76/3600 = 40.4 \text{ Btu}$$

Temperature of case after all 276 sec

$$\Delta T = Q_t/WC_p = \frac{40.4}{13.6 \times 0.25} = 11.9$$

Temperature of case = 541.6 + 11.9 = 553.5°R = 93.5°F

At this time the shroud is ejected.

5. Heat transfer remainder of flight (276 sec to 3000 sec).

Equation for Equilibrium:

$$\text{Sun Load} + \text{Internal Electronics Load} = KA_2 fe\left(\frac{T_c}{100}\right)^4$$

where Sun Load (SL) = $442\alpha A_1$ (α for all white = 0.24, and A_1 = 3.30 ft²*). Internal Electronics = 152 W × 3.42 = 520 Btu/hr (lower than early phase of flight because of oven turn-off). K = 0.173, A_2 = 3.85 ft², fe = emissivity of white paint = 0.94, T_c = temperature of coupler case, °R.

Solving for T_c, we get

$$\text{SL} + \text{IL} = KA_2 fe\left(\frac{T_c}{100}\right)^4$$

$$(442)(3.3)(0.24) + 520 = (0.173)(0.94)(3.85)(T_c/100)^4$$

$$870 = (0.63)(T_c/100)^4$$

$$(T_c/100)^4 = 1380$$

$$T_c/100 = 6.1$$

Stabilization Temperature T_c = 610°R = 150°F

6. Now, for a more accurate determination of the temperature of the case at various times between 276 and 3000 sec, let us calculate the case temperature at each 0.1-hr interval.

Thermal transfer out of the coupler to space:

$$q = 0.63\left(\frac{T_c}{100}\right)^4$$

where $KA_2 fe = 0.63$. This q is total heat flow from coupler chassis, and when subtracted from the sum of SL plus IL, leaves a remainder which will cause a temperature rise according to the formula.

$$Q = WC_p\Delta T$$

where Q is the difference between SL + IL and q.

Solving for q with known T_c of 93°F at end of 276 sec, we get

* A_1 is area seen by point source sun.
† A_2 is area of box looking at space.

$$q = (0.63)\left(\frac{93 + 460}{100}\right)^4$$

$$= (0.63)(825) = 520$$

Then

$$Q = (\mathrm{SL} + \mathrm{IL}) - q$$

$$= 870 - 520 = 350$$

Solving for ΔT, we get

$$Q = WC_p\Delta T$$

(where $W = 13.5$ and $C_p = 0.24$)

$$350 = 3.24\Delta T$$

$$\Delta T = 350/3.24 = 108°\mathrm{F/hr}$$

But we are considering operation only over 0.1 hr so that $\Delta T = 108 \times 0.1 = 10.8$ at time 636(276 + 360) sec. Thus at 636 sec, $T_c = 93.5 + 10.8 = 104.3°\mathrm{F}$.

Repeating the calculation for each 0.1 hr gives the following results:

Elapsed Time (sec)	*Case Temperature (°F)*
996	111.18
1356	117.03
1716	122.08
2080	126.17
2436	130.54
2796	133.69
3156	136.31

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8090

Packaging and Magnetic Field Interference

DON E. LONGMIRE

Electronics Department, Arizona Division, Goodyear Aircraft Corporation, Litchfield Park, Arizona

This paper deals with the need for inclusion of a magnetic field interference study as a vital part of an electronic system analysis. Starting with the cataloging of the variety of magnetic or magnetic-sensitive devices in a system, the paper shows how their interrelationships can be coordinated, so that proper packaging considerations may be applied. Determination and control of magnetic field shape, field strength, and the sensitivities of each magnetic device in order to establish successful system operation are dealt with at some length, and methods of control through separation, physical orientation, and shielding are presented.

THE IMPORTANCE of properly dealing with magnetic field interference (MFI) in packaging is often overlooked. In many cases early in the system analysis stages of present-day electronic systems, packaging concepts which consider MFI should be developed.

Occasionally the system factors involving magnetic interference can be extensive. In a recent aircraft installation, the external field of a large and powerful klystron magnet was certain to degrade the performance of a cathode ray recording tube, which was mounted 12 in. away from the magnet. A static, unchanging field might have been tolerated, but in this example the klystron package was vibration mounted and the motion of the package relative to the crt presented another variable, that of a modulated magnetic field for which no compensation could be made.

The crt carried shielding, yet it became necessary to repackage the unit carrying the magnet to gain an additional separation of 12 in. between the two pieces of equipment. The relocation was not the first of the efforts to decrease the magnetic field at the crt. At first, a single plane of nickel–iron alloy was placed as a barrier between the crt and the magnet. Several gages of this high-permeability material were tried. There was little effect because the magnetic field filled the space around the shield as if no shield were there. The boundaries of the shield also exhibited some rather high field discontinuities. An enveloping shield was placed close to the klystron and its magnet. A minimum thickness of shielding was used because it was noted that the focusing field strength within the magnet poles decreased as shielding was applied. It was known that this would cause operational difficulties and some shifts in the tubes' operational parameters. The compromise between the operational effects and the shielding achievable was unsatisfactory in that the gauss level at the crt was still too high. The shield was being completely saturated and acted in some respects to carry the field closer to the item which was meant to be protected.

In another study, this shield was shifted to act as the main housing of the unit which held the klystron. In this case the increased weight penalty of shielding dictated the use of thin materials, and despite good separation between the magnet and the shielding (2 in. minimum), the saturation limit of the shield was exceeded and the external field was still too high to be considered acceptable. Studies of the amount of shielding required for a given external

flux was backed up by detailed three-dimensional mapping of the field strength using a precision Hall-effect gaussmeter. At one time in the program considerations were given to shielding the entire area in which the unit containing the magnet was installed.

The foregoing example of a shielding effort may be typical of many industry attempts at shielding. Each method mentioned increased the weight of the shielding without achieving the desired result. In cases such as the one given, it is almost impossible to shield the trouble source. An adequate shielding of the individual items affected by the disturbing field or an increased separation from the source of the disturbance are the only practical lightweight solutions.

It is necessary to recognize which electronic devices are susceptible to magnetic influences. The following list defines most devices without trying to say which are the most difficult to protect: backward wave oscillators, traveling wave tubes, magnetrons, RF isolators and circulators, garnet resonators and other ferrite devices, klystrons, photomultipliers, Hall-effect devices, meter movements, magnetic tapes and magnetic pickups, relays, core materials used in transformers, toroids, etc., masers, plasma devices, and vacuum tubes in general.

The susceptibilities are a function of the magnetic principle which is being used within the particular device. When an electron beam is being focused or directed as it is in cathode ray tubes, stray magnetic fields of comparatively low magnitude can degrade performance noticeably and shielding is called for. In the backward wave oscillators, traveling wave tube, magnetron, and klystron family, beam focusing is established by fairly sizable magnetic fields which can be distorted by external fields or ferrous masses. These items are usually difficult to shield as case histories will show. Some of the rather passive devices such as garnet resonators and photomultipliers are quite sensitive to external fields. For example, a multistage photomultiplier can sense the direction of the earth's magnetic field.

Backward wave oscillators, traveling wave tubes, and magnetrons react typically to disturbances introduced into their focusing fields by showing a loss of power output. If this does not occur over the entire range of the design frequency it may nevertheless occur at discrete points. The operating parameters have to be established with shielding in place or magnetic proximities firmly established as the tuning functions are changed. The application of shielding, through the effect of defocusing, can cause operating conditions to change enough that helix current, for example, can rise to an excessive level. Some of the tube types listed above seem to defy any attempt to apply shielding.

Meter movements can be influenced by external fields. While it may not be unusual to find a shielding band around the movement, this band may not be enough protection if the meter has been mounted in close proximity to the magnet of some large microwave item.

Magnetic taped information can suffer considerably or be garbled by unfortunate coincidence with strong magnetic fields. Shielding cans can be obtained for the storage of magnetic tapes.

In close, tight packaging, there are numerous ways in which relays can fail or malfunction because of strong magnetic fields. In such environments, knowledge of the principle magnetic axis of the relay and disturbing field can be used to avoid relay hang-up or slow action, provided that the relay can be oriented to minimize the disturbance. A trial-and-error approach using the actual components is suggested.

Open core magnetic devices such as a "C" core transformer can be disturbed in some degree by the presence of a strong biasing field. Closed core items, such as toroids, seem to have more resistance to stray fields. The rule to apply in so many of these situations is "design and test." If the device is designed or adjusted to a given environment, the device will function as long as that environment does not change enough to place operation out of the given tolerance.

During the breadboard stage of circuit design, it is sometimes very enlightening to approach the circuitry with a magnet which represents the nearest magnetic device. The effect on the circuit operation and the orientations which cause the fewest perturbations are easily seen. Once the problems are foreseen, one can package around the trouble.

If we set out to analyze packaging problems associated with magnet-equipped RF devices, it is necessary to understand the orientation of the principal magnetic axis and its strength.

There are a few RF component manufacturers who provide usable information in this respect. A caution note which usually says "keep all magnetic material x in. away" is all that is usually provided. Away from what? A better approach would be for the manufacturer to provide a three-dimensional field plot and some insight as to what constitutes the permissible extent and direction of external fields. Knowing this, a designer could proceed with greater confidence in setting up magnetic proximities and preserving the symmetry necessary for proper focus. Lacking this information from the manufacturer, one must wait until the component is available for an in-house magnetic survey.

General Electric makes a small and very convenient hand-held gauss meter which is ideal for field plotting in the range of 25 to 2500 G. For fine plotting there are electronic meters with wand-type detectors which can range from fractional gauss to very high levels. In the process of making measurements for the field plot it is necessary to orient the detector for the maximum field at each plot point. If the major magnetic axis is known it is possible to predict the proper orientation and thus hasten the plotting process. Speaking generally, for an efficient magnet the field strength within the poles will be 4000 to 5000 G. Away from the poles but on the surface of the magnet the field will be about 300 G. Two inches away from the magnet, the field may still be as high as 100 G.

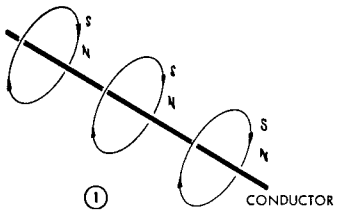
Backward wave oscillators have solenoid-shaped magnets with the RF tube lying in the main axis of the solenoid. In some models the solenoid is so short that the magnet resembles a flattened ball. Traveling wave tubes generally use periodic solenoid magnets (PPM), separated by pole pieces. The polarities of adjacent magnet poles are alike. It is possible to form the field using long, shaped bar magnets and soft iron pole pieces. Magnetrons are seen in both the "C" magnet and "double C" magnet versions. The latter shape is also used with some klystrons.

The primary field of a three-port circulator is perpendicular to the plane common to the three ports, and may be formed by disc-shaped magnets. The field of RF isolators is easily seen to be transverse to the waveguide or coax line.

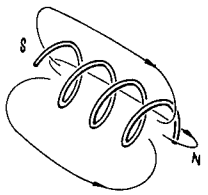
In practically every instrument or military application of cathode ray tubes, a magnetic shield will be found. These may vary widely in complexity from stock, single-layer shields to intricately formed multilayer envelopes. The metals used in these shields must have high permeability and low retentivity. High permeability is needed so that a large magnetic flux per unit area can be carried, and low retentivity is needed so that the shield will not retain a magnetic field permanently. It is necessary to know the quality of the magnetic disturbance to choose the type of shielding metal. For shielding the fields of permanent magnets (DC levels) a material must first have high permeability and low retentivity, but it may have moderate hysteresis losses. When shielding AC magnetic fields, the first two characteristics are desired and the requirement for low hysteresis loss is also important. It is often necessary, in the interest of economy of weight, space, and efficiency, to combine layers of the different shielding metals to shield for both AC and DC level magnetic fields. It is not uncommon to find three layers used. Occasionally it is desirable to add a layer of conducting material such as a thin copper shell, which can act as a conductor for eddy currents formed in the magnetic shield by AC induction.

The best shielding attainable will be that formed by a full and complete envelope. When this shielding is broken by holes and cutouts, discontinuities exist which can compromise the efficiency of the shield. Lapped joints in a shield can be tolerated if there is sufficient shielding metal used to avoid local saturation. The small gaps in these lapped joints should be practically tight, 0.005-in. gap for example. Spot welding of seams is one of the popular methods of shield fabrication. Welding of the seams is also commonly used. With some shielding metals a hydrogen atmosphere heat treatment after all fabrication and joining is required to develop the full magnetic properties of the metal. It is possible to degrade the performance of these particular shields by subsequent mechanical operations or by simple mishandling.

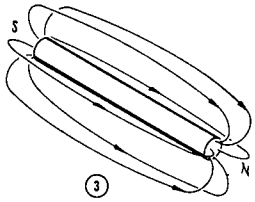
Shielding metals should not be considered to be magic flat sheets which one can place between the disturbance and the item being disturbed. This barrier approach is ineffective and inefficient. One cannot simply contain the pervasive field of a magnet. One should envelop the item to be protected or completely contain the disturbance.



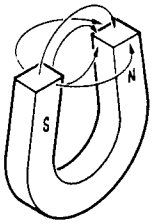
① MAGNETIC FIELD ABOUT STRAIGHT CONDUCTOR



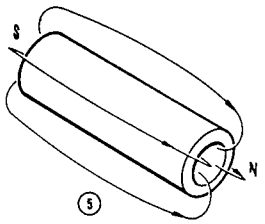
② MAGNETIC FIELD ABOUT CONDUCTING COIL



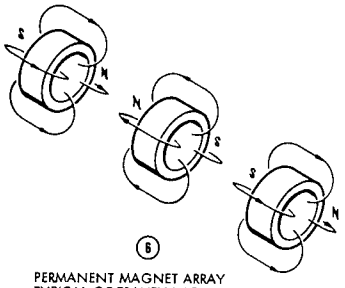
③ BAR MAGNET



④ C MAGNET

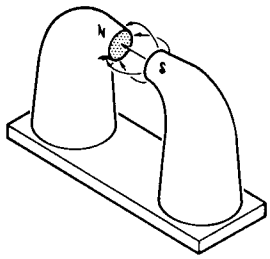


⑤ SOLENOID FIELD PERMANENT MAGNET (TYPICAL OF BACKWARD WAVE OSCILLATOR)

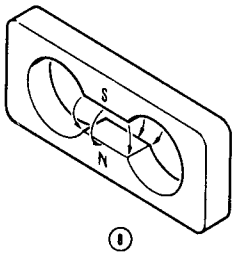


⑥ PERMANENT MAGNET ARRAY TYPICAL OF TRAVELLING WAVE AMPLIFIERS,

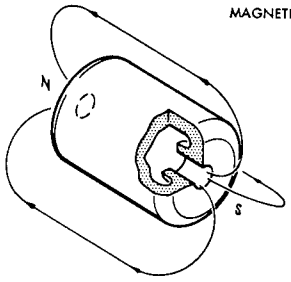
FIELD SHAPING POLE PIECES NOT SHOWN



⑦ MAGNETRON



⑧ MAGNETRON OR KLYSTRON



⑨ SOLENOID MAGNET BWO

Fig 1

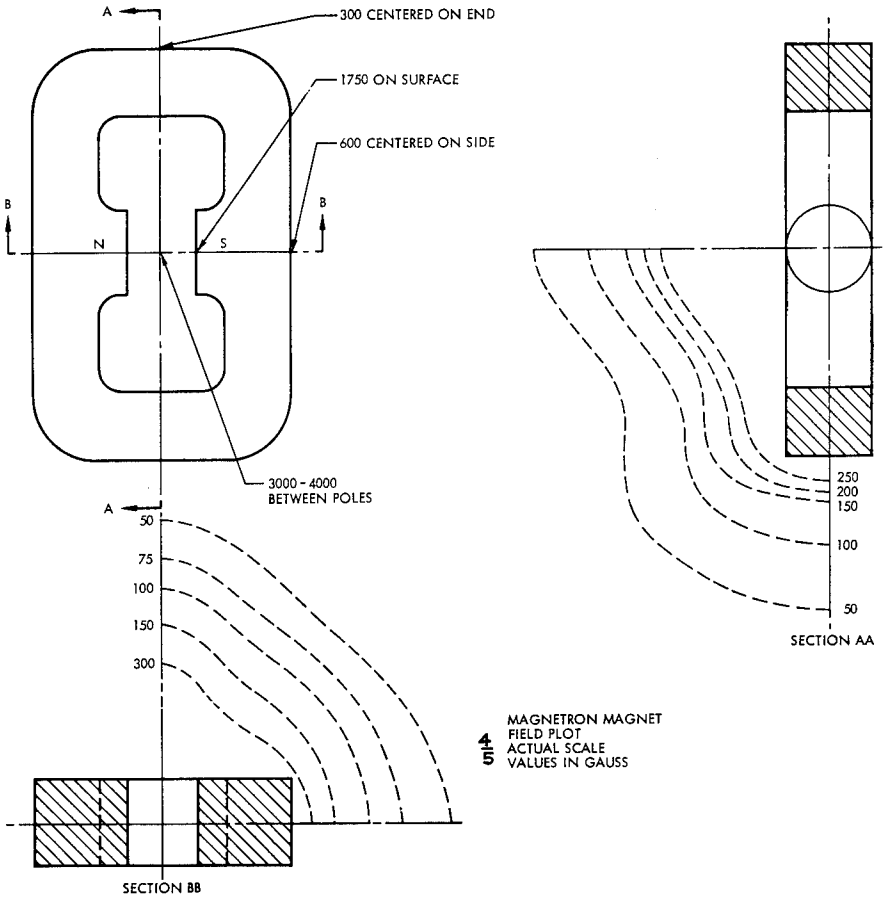


Fig. 2

In most RF devices it is quite necessary to keep the shield symmetric with the magnetic axis of the tube and to make the shield as large as can be tolerated so that the shield will not rob the focusing field of its strength. If the shield is not symmetric with the magnetic field, then the field may be distorted and defocusing will result. Determining the magnetic symmetry of the RF device can be difficult because of the varying parameters concerning the magnet, pole structure, and tube proper. The manufacturer moves the tube around in the field slightly to achieve proper focus. At times one will see tube structures which lie markedly out of line with the apparent symmetry of the magnet or housing. In these cases it is very difficult to apply shielding which does not affect the performance of the device. Be prepared to accept rather large and heavy shielding when it is mandatory to contain the field of a large magnet.

Past experience with shielding several types of backward wave oscillators has shown that the shield must be about twice the diameter of the magnet. Approximately one diameter is needed at either end of the magnet before the shield is encountered. Using lesser values, the operation of the backward wave oscillator was severely compromised. A backward wave oscillator or traveling wave tube operating in a shield can be expected to have a different set of operating parameters than one running on the bench unshielded. The thickness of the shield is arrived at by a consideration of the mounting stiffness required and the amount of shielding desired. To give an example, a solenoid backward wave oscillator magnet 3 in. in

diameter and 4 in. long was mounted in a 6-in.-diameter shield laminated with 0.035-in. Netic* material. The shield length was 12 in. On the outside surface of the shield the field ranged from 5 to 10 G. This was an attenuation of about 20 to 40 times the level within the shield.

Despite some rather strong caution notes which may be seen on the envelope of PPM focused traveling wave tubes concerning magnetic separation, these can be packaged quite tightly in parallel groups. For example, $1\frac{1}{2}$ in. center-to-center distance was used on three traveling wave tubes of 1 in. O.D. These items needed no magnetic shields, and operation was substantially the same as individual bench operation.

Because magnetic materials can be degraded by careless handling and mounting processes, nonmagnetic tools and hardware should be used at all times. Stainless steel hardware and tools Type 302 and 303 are generally preferred because of their strength and nonmagnetic properties. If magnetic hardware is used it can be annoyingly awkward to handle, and magnetic tools will invariably clang into the nearest magnetic-bearing microwave device, many of which are extremely expensive.

When air-freighting magnets or units containing them, certain precautions must be taken. Air lines and air freight companies require the marking of all such shipments to warn them of the presence of magnetic materials. They would like all magnets to have keepers but this is not possible. They also suggest arrangements of magnets to offer magnetic cancellation, which is rarely possible. Unless shielded containers can be used, little can be done except to label the packages with field strength and polarity or state compass safe distances. With the above bits of information the shippers can make the necessary arrangements and placement of the shipment where it will least affect the aircraft's compasses. In some instances involving large magnets, the shipments may be refused.

Figures 1 and 2 show several examples of magnetic field shapes which have been discussed. The purpose of the foregoing discussion has been to place emphasis upon the varied and often overlooked packaging problems which are caused by magnetic field interference. It is clear that an early concern and an intelligent approach to the solution of these problems is needed and that many problems exist only because they were not properly forecast in early system design stages. It is also clear that packaging to prevent magnetic field interference can take many forms, according to the type and amount of interference as well as to size, weight, and special considerations such as compass safe distances. The increasing importance and complexity of packaging is illustrated by the growing need to place careful consideration upon such problems as magnetic field interference. These considerations should become an early and integral part of system development procedures.

* Trade name of Magnetic Shield Division of Perfection Mica Corporation.

Discussions

EDITED BY LAWRENCE L. ROSINE
Editor, Electrical Design News (EDN)

Donald H. McHugh-The B-Module

Q. (Bill Volk, Westinghouse Electric Corporation, Baltimore, Maryland) The system is good for high production. What do you do for low-production items, and what is your break-even point?

A. For low production we chemically etch the grids instead of stamping them. It takes about 3 min per part to etch them with a sulfuric acid bath, and a small hand-punching station will make the appropriate punching operations. By using a plastic template you can program the hand-welding operation.

Q. What is your cost on an engineering model basis?

A. I cannot really answer this as all the modules vary depending upon the number of components.

Q. What is the average cost? We can build engineering models for about $50.00 a piece, including components, with cordwood and point-to-point wiring.

A. Well, we have some modules with $30.00 worth of components in them. I would guess we could build a prototype module in about one hour's time.

Q. (Carl McCann, Motorola, Inc., Scottsdale, Arizona) What is the approximate size of your module, and can you handle components of nonstandard size such as transformers?

A. I forget the exact dimensions, but these are in the paper. Nonstandard components, such as transformers, are usually placed at the end of the module. This is past the basket portion that is cut off. In the case of the transformer you may have four leads coming out to the top and bottom basket tabs. You get out of our range when you get a component that is longer than the module width. This takes a pretty good sized component.

Q. (Edward Moore, Martin Company, Orlando, Florida) How do you fixture the component to the basket assembly and hold it prior to welding?

A. The fixture is a nest type where the component drops down between the slots onto the basket tab. The leads stick out onto the basket tabs, where a welder will make the appropriate welds.

Q. (Bill Salsbury, McDonnell Aircraft, St. Louis, Missouri) How do you handle repair of your basket as opposed to replacement of a defective part, and secondly would you quote the military specs that this meets?

A. This will meet military specifications which are the equipment specifications for almost any military job we have had in house. As for repairing the baskets, at this stage we have about seven cents in the basket on an automated basis and they are just a throwaway item.

Q. (Leonard Katzin, Jet Propulsion Laboratory, Pasadena, California) Is it reasonable to assume that reliability will be considerably improved by automation and the reduction of the human element? For connecting two components don't you have to go through four welds in series rather than taking one ribbon and hooking it directly between the two leads?

A. This is basically true, depending upon where the component is being connected to the next component – for instance, to the opposite side of the basket assembly. It is true in this case. We do utilize more welds in a B-module than we do in a normal point-to-point cordwood module. We figured the increase in mean time between failure of the B-module over a standard module, just on the basis of the additional welds, and it came out to 0.41%.

Q. (Joseph Spicola, Grumman Aircraft, Calverton, New York) What is the material of the tab, and how does it compare to the many pigtail materials available in the component field?

A. We are presently using nickel. There are several materials that we can use for the basket tab. Some that we like are clad materials, and of course they are a little more expensive. You are asking about welding the tabs to the components. We have not found a weldable component that will not weld to nickel.

Q. (Otto Jahnke, ITT Federal Laboratories, Clifton, New Jersey) Can you tell me what your welding production rate is at the present time?

A. We have not tooled up for an automated process as yet. It is still in the planning stages. We anticipate 30 sec per module – this is finished parts off the end of the automated assembly line at a rate of 30 sec per module. The complete start-to-finish operation of a given module is roughly six minutes.

Q. How many have you made?

A. We have built roughly ten modules with all different circuit configurations, all of course on a prototype basis.

Q. You haven't any idea of course what the automated reliability of the welds would be then?

A. No, just the MTBF.

Q. What type of welding process do you use? Is it parallel gap type?

A. No, it is resistance-type welding, cross-wire welding, and capacitance discharge with parallel mating electrodes.

Q. (Mike Berberian, Sylvania Electronic Systems, Needham Heights, Massachusetts) In your transfer molding, what materials will you transfer-mold and what pressures do you expect to build up? Do you anticipate any problems in cracking glass diode seals? Do you anticipate any exotherm problems? How will you interconnect the B-modules into a system?

A. We have been transfer-molding for quite some time, not B-modules but other modules for military programs. We are using a Dow-Corning material, 1070 by number, that has been especially developed for Burroughs Corporation. We have had no problems with component failures due to the transfer molding from pressures. As far as interconnecting a B-module into a system is concerned, the leads are left long on the input and output pins, and then dip-soldered to a printed circuit motherboard. This of course will connect into a back board connector.

Q. (Ed Keonjian, American Bosch, Garden City, New York) You have mentioned seven cents as the cost of a throwaway module. Perhaps I misunderstood you. Could you please explain?

A. The cost of seven cents was the cost of the materials that go into the basket prior to the components being mounted.

Q. But at what cost level are your throwaway modules? What do you consider not worth repairing?

A. I would say that a few years back $100.00 was considered a throwaway module but I think today it is somewhere in the neighborhood of $25.00 to $35.00.

Q. (Joe Ingber, Airborne Instrument Lab., Deer Park, New York) You said you had no trouble welding any component leads to nickel-A. I wanted to be sure that I understood that statement.

A. Any weldable component leads, such as Dumet, Alloy 180, and Kovar.

Q. You are not using solder dip leads?

A. No, not for welding.

Q. How do you intend to automate welding leads of different materials, with necessarily different weld schedules?

A. There is a company with an automatic welder commercially available which is tape programmed to change schedules for both heat and pressures.

Q. A third question, if I may. All your welds to component leads are now flat welds, aren't they? Do you feel this lowers the reliability of the weld?

A. No, actually it is a cross-wire weld with flat material rather than a round wire. Due to the increased material surface area and increased electrode pressure and contact area that the electrode makes with the material, I think we get a considerably stronger and more reliable weld.

Q. (R. Shall, Martin Company, Denver, Colorado) What is the name of the automatic welding machine that you mentioned?

A. It is a Weldmatic unit.

Taichiro Atarashi-Interim Packaging Concept for Frequency Division Multiplex Carrier Telephone Equipment

Q. (Leonard Yuska, United States Naval Avionics, Indianapolis) What size wire did you use on your wire wrap and what was the size of the wire wrap post?

A. The diameter was 0.5 mm. The wire wrap posts were 1 mm square.

Q. (Mohi Sobhani, Litton Industries, Woodland Hills, California) Did you use flat cables in any one of these? The photos show just wire. Do you use flat cables or flex print?

A. We used only circular cable.

Q. It is just harness, not flat cables?

A. No, not flat cables.

Q. (A. J. Sechler, RCA, Cambridge, Ohio) Does each module contain both the receive and transmit functions?

A. It depends upon the case – sometimes separately and sometimes together.

Q. What techniques were used to reduce the size of the filters?

A. We spent most of our time improving the components so we could reduce the size.

Q. (Vince Galati, System Development Corporation, Santa Monica, California) I notice on your rack that you had quite a large packing density. Did you have any problems with heat? I did not see any cooling system in the rack.

A. In the carrier equipment the total output power is 150 W. There was no heat to worry about as temperature only goes up 5°C.

Q. What kind of frequencies are you using?

A. Voice frequencies to 108 kc.

C.F. Middleton-The Application of Welded Micrologic Modules and Wire Wrap Techniques to Ground Support Equipment

Q. (Loye Pierce, Gulton Industries, Hawthorne, California) Did you use capacitance discharge or AC to weld?

A. Capacitance discharge.

Q. Have you tried the AC welder?

A. Yes, but we favor the capacitance-discharge type.

Q. (Doug Grantham, Bristol Company, Waterbury, Connecticut) Is the connector with the riser wire a Raytheon connector? Does Raytheon make it?

A. Raytheon does not make the part. It is a Raytheon-designed part and it is being fabricated by National Connector for us.

Q. Does National also mold the mating female part?

A. The mating part is a Melco item. They are made up of multiple pieces.

Q. (Fred Brammer, IBM Corporation, Kingston, New York) What is the smallest size wire which you wire wrap?

A. 24 is our standard size.

Q. (Francis Brinker, United States Avionics Facility, Indianapolis, Indiana) What facilities, if any, were made for test points while the modules were in place?

A. That is the feature of the wire wrap assembly. By sliding these units out of the drawer you can expose every wire wrap pin on the far side of the assembly. The pins can be probed through the holes in the phenolic covers.

Q. (Jack Arabian, MIT Instrumentation, Cambridge, Massachusetts) What considerations influenced you to pick a connector with a cable on it as compared to a plug-in on the module itself?

A. I am afraid I do not understand what you are referring to.

Q. In terms of reliability or in terms of maintenance, it would seem more practical, or more serviceable, to use a plug-in module as compared to a moving flexible cable as you have shown in the diagram.

A. Mainly a manufacturing point of view. Everything is broken down to its lowest design entity so we can go through the whole design without having to make drastic changes in any one assembly. The second reason would be in the interest of testing– the ability to extend trays for test without affecting the length of interconnections that exist while the unit is in closed position.

Q. (Pete Gerlach, Automatic Electric Laboratory, Northlake, Illinois) I am a little confused as to whether or not your drawer assembly is electrically hot when it is pulled from the cabinet. Are these connections broken when you pull your drawer out?

A. Bendix connectors on the rear of the drawer are connected to the cabinet by means of a cable follower. The cable comes out with the unit and when it is in an extended position it is electrically hot.

Q. (Don Schnorr, RCA, Camden, New Jersey) I do not understand what you mean by thinking and nonthinking cables. Would you go over this again?

A. A thinking cable involves logic within it. A nonthinking cable is a point-to-point cable. Pin one goes to pin one and is essentially dumb. You do all your thinking on the far ends of it with the wire wrap process.

Q. (Bill Volk, Westinghouse Electric Corporation, Baltimore, Maryland) I noticed in your assembly, using micrologic blocks, stacking, and modules, you had two layers with wiring between them and also wiring between the pins. What happens if one of your blocks goes bad? How do you repair it?

A. When you refer to a block, what are you referring to?

Q. The module – the micrologic block itself. Consider the TO-5 can. You put four of those into a module, and then wire between the TO-5 cans and between the pins and the module. How do you repair it if one goes bad?

A. We have two levels of wire above the trans-a-pad which are ordinarily ground and B-plus. Those pins come directly out of the micrologic without bending. They can be repaired by clipping away and replacing. The other leads that go out to the riser wires are bent over the trans-a-pad and fan out. We can clip away the riser wires and reweld to it. It can be repaired.

Q. (Herb Seymour, Burroughs Corporation, Pasadena, California) Did you make any economic study on your Malco connectors to determine whether it was advantageous to omit unused pins? Or could you omit the pins that are not used in the plate itself?

A. We found by going to Malco on a quote basis that it is more effort for them to leave pins out. (They install this on a programmed machine that gang-assembles the pins into the plate.) If a standard pattern could be utilized for all plates, the price would not be as great as that of random patterns. It is more economical to buy the complete assembly, with the 1400 pins, in quantity.

J. Moore, M. Berberian, and F. Feigin-Mechanical Design and Integration of a Microelectronic Tape Control Unit

Q. (Leo Fiderer, Hughes Aircraft Company, Culver City, California) How long has that unit been in the field? Have you received any feedback on it?

A. No. It is the first unit, and it is not yet finished. It is in system test now and it will be delivered within a month. There is no feedback yet, except from our own internal use. There are 1200 wafers of this variety in this system, counting a few spares. We have been running small sections of the circuitry in the lab and they are doing pretty well. Next year we will have the feedback from the field.

Q. (John Hoefer, Bendix Corporation, Kansas City, Missouri) Could you explain in a little more detail the component-holding fixture or plate that is used during the welding of the component?

A. This is a beryllium copper sheet 10 mils thick. We precision etch to within 2 mils the maximum size of each component, whether it be a diode or a transistor. We then drop that component into the component locater. This is attached to the top of the wafer surface by the jig that you saw before. And this goes under the machine.

Q. (William Hall, Temco Electronics, Dallas, Texas) What is the material in the wire that goes from the connectors to your substrate?

A. This is gold-plated Kovar.

Q. (M. B. Purvis, Bell Laboratories, Holmdel, New Jersey) I am concerned with your paper and the previous paper. You both have adopted for your basic modular unit approximately 20, in their case, and 22 in your case, basic connections on your throwaway module. This would further imply that your connection is limited very quickly. As a result you waste a rather tremendous number of interconnections between the packages on the back of your wiring field. This then leads you into a flexibility of changes but on the other hand apparently introduces a worse reliability factor and that is in the interconnections themselves. The question is, do you trust your designers? Do you trust the people who have furnished you with your basic packages which are your circuit elements? Or do you trust your connections?

A. You have a good point. These are things we have been coming up against all along. First was the wafer size – what went into the wafer and how much of the logic we did internally and how much we did in the back wiring. From the point of view of flexibility, you are better off doing the logic in the back wiring because you can change it. But from a manufacturing point of view, it is hell if you do it all in the back wiring as it gets to be a rat's nest. The circuit and logic people did a pretty good job here. One slide shows that the back wiring accomplished at the module level accounted for 60% of the total wiring. We did not get into a rat's nest and we were pretty lucky I guess. But of course this is not a full-scale computer. It is just a group of logic circuits. Your point about the 22 pins being too small is right. The only reason we use 22 pins is that it is the most we could get in a small standard connector. The pins are on a one-tenth spacing. There is nothing available commercially on a fifty-thousandths spacing that gives you this crimp type, poke home application. You must have removable contacts when you are down this small or you get into a solid laminated wiring and welding. If you are using laminated back wiring you are pretty well up the creek when it comes to changes. I can only agree with you that the problems you pointed out are the real problems and we evaluate each job as it comes. We lucked out on this one.

R.C. Frank and R.E. Kalfayan-Interconnecting Complex Miniature Electronic Systems

Q. (Bill Salsbury, McDonnell Aircraft, St. Louis, Missouri) You mentioned tubular leads being available in the multilayer circuit boards. Can you tell me how the contact is made to these tubes from the inner layers and how you determine whether or not these are reliable connections?

A. We are not experts at the multilayer printed circuits as I mentioned. However, there are several different ways in which this is done. We know Globe Electrical Manufacturing Company located in a suburb of Los Angeles makes boards this way. A Colorado company, Fab Tool, Inc., I believe, works very closely with Martin, and they make boards with tube leads. I think there are several others. Each of these companies has its own techniques. We do not have much personal experience with it.

Q. (Dick Kirn, Electro Mechanical Research, Sarasota, Florida) We have used and done quite a bit of work on a tubelet printed circuit board built, I believe, by Littleton. This is an electroformed board and the tube and the flat sheets which are then etched are electroformed as one discrete sheet, eliminating any interconnections. I wonder if you are familiar with this?

A. I am personally not familiar with this. The kinds that I am familiar with are brazed or soldered.

Q. We have sectioned and cut up quite a few of these. As it is electroformed, with the tubes and the flat sheet all in one process, there are essentially no joints and it appears to be very good construction.

Q. (Tom Pallett, McDonnell Aircraft, St. Louis, Missouri) How do you maintain the distance between the module and the interconnecting matrix?

A. We started off by saying that the matrix is not a supporting or a mechanical member and therefore the matrix is supported and the module is also supported. Actually, they are supported by the same member and so they are mechanically spaced from one another by this mechanical member.

Q. (Michael Wadiaeff, RCA Astro-Electronics, Princeton, New Jersey) Have you developed any special techniques in reworking your multilayer boards or in reworking your cordwood type packages?

A. We have not made multilayer boards and so our experience has not been personal. We have not used multilayer boards and this particular program did not use cordwood modules. This afternoon Mr. Okada from Douglas will present a paper in which he will discuss a method of making cordwood modules which I think is not particularly unique but it is certainly a good method. He will comment on the possibility of reworking cordwood modules.

Q. Have you developed any methods of reworking them in your particular case, after welding or crimping your connectors?

A. No. If we get a faulty module, we can get it out by snipping the end of the tubes. If you are familiar with the original Polaris computer design, which was made at MIT, you know they used a technique similar to this. As a matter of fact, it is this technique on a larger scale and they said that "what we do when we get a failed unit is cut the ends off the tubes and because the tubes are of some length we can do this three or four times." If we do it more than this, we have to cut all the interconnections off and throw the interconnecting module away.

Q. (Edward Moore, Martin Company, Orlando, Florida) Have you any figures on a cross-over point in cost between a prepared matrix and an etched circuit board, either single or multilayer?

A. No, we have cost figures. The thing that becomes apparent is that they are much easier to build than you thought they were when you started. Your tooling possibilities are very good. What starts out looking like a complex job reduces to a rather simple one when you use minimum tools and fixtures. We do not have any quantitative numbers on this, however.

Q. (H. P. Shamrock, Lockheed Electronics Company, Los Angeles, California) I am a little curious as to the seating of these tubelets as you encapsulate. Do you have problems with the seepage of the resin around the seal or up the side wall of the tubing for welding purposes later on?

A. No. We have no difficulty with seepage along the side of the tube. Obviously we let the back end of the tube inside of the mold. We have to get a 100% seal. If we don't we have a tube full of resin and that is very embarrassing. As a matter of fact it is almost always fatal. We want to make sure that we get a good seal on the inside end of the tube. We use a latex rubber and it works very well. It has not really been a problem. The problem is, of course, if you are looking at the ends of 400 small tubes, that it is not too difficult to miss one of them. So you have to seal them in an orderly fashion.

Q. (Leonard Yuska, United States Naval Avionics, Indianapolis, Indiana) Are these holes prepunched in the rubber latex for the tubes?

A. No. I think you probably misunderstood me. We use a liquid latex to seal the back end of the tubes. We have to provide clearance around the front end of the tubes to get them through the front plate of the mold which is metal. Again, we seal with liquid latex. We do not use a sheet.

Q. (Joe Ingber, Airborne Instruments Laboratory, Deer Park, New York) How many welded wire matrices have you actually built?

A. I could not say how many we have built, but we have built quite a number of matrices on a development basis. We have encapsulated and checked out several of the welded wire ones.

Kenneth E. Harris-Electronic Packaging Design for the OAO Primary Processor and Data Storage Equipment

Q. (Carl Todd, Hughes Aircraft, Newport Beach, California) Is it possible that by taking your material and subjecting it to a vacuum environment before sending it out into space you might be able to use materials that you would not otherwise?

A. It is possible, and has been considered – preconditioning the material so to speak.

Q. (Jake Rubin, ACF Electronics, Randallstown, Maryland) Can you elaborate on the method of maintaining the AMP/MECA cells? Was the removal of the cells through holes in the printed board or are there auxiliary devices for extracting these cells?

A. In most panels we used a 3/8-in.-diameter hole in the base board to remove the cell and it is pushed out using a removal tool. There were a few panels, next to the memory array, on which it was necessary to use Mylar tape wrapped around the cell, being careful not to run it under the cell, which provided a bail for removing the cell.

Q. (Doug Allred, Sylvania Electronic Systems, Needham Heights, Massachusetts) Would you tell me what experiment it is that you are describing? What optical experiment?

A. There are presently under contract to Grumman two OAO satellites. Each satellite will contain particular experiments and the experiments will be used to provide, as I understand it, a better mapping of the heavens. There is a very good article in the last Space Technology magazine on the function of the OAO satellite.

Q. My question was, more specifically, was it the Goddard experiment or Smithsonian cellu-scope? Do you happen to know just which one of the seven proposed experiments it is?

A. I am afraid that I cannot answer that.

Q. Okay. I have a second question then. I read both the paper and listened to the description, and it is not quite clear to me how you managed to conduct the heat from your modules to the front panel. Could you briefly go over that again, please.

A. In the logic stack, the heat dissipated by the cell is conducted down through the cell case to the base board or conducting strip on the panel. It is conducted along the panel to the front and rear corners of the panel and from there it is tied to struts which tie to the heat sink surface at the front of the panel and tie to the top and bottom of the unit case at the rear of the unit.

Q. How do you get sufficient thermal pressure?

A. By inserting the cell on the panel the contacts maintain enough pressure on the base board to provide the conduction. I might add that there were a few cells where we did use

an interstitial material between the cell and the panel. These were higher-dissipating cells.

Q. (Wayne Plunkett, U. S. Army Missile Command, Redstone Arsenal, Alabama) In contrast to a lot of other companies, I notice you place a lot of confidence in the pressure connections. I was wondering if you based this on any experience, data, or tests?

A. Yes, we ran tests on typical cells which were inserted on a panel or on a panel containing a conducting strip and all of the thermal data considered this test. We measured delta T's from the cell components to the panel base board of individual cell tests.

Q. I am sorry, I was speaking of electrical connections, rather than the temperature connection.

A. You mean our leaf contacts from the cells to the side rail?

Q. Yes.

A. We have had very little trouble with this. There have been cases where contacts have been damaged but as long as the contact was not bent excessively, we set a limit of 9 or 10 thousandths on the spread, we allowed repair to the contacts. We have been successful to date in doing this.

Q. (Bill Tacy, General Electric, King of Prussia, Pennsylvania) Could you tell me what the material is in the AMP/MECA package you use, and secondly have you determined the effects of radiation in the thermal vacuum atmosphere on this material as far as dielectric constant is concerned?

A. The material in the AMP/MECA cell case is diallyl phthalate and the last examination of the environment in which the satellite would operate indicated that radiation environment was not a problem. I cannot say we have conducted any tests on this material in radiation environment. As far as I know there should be no problem. This is the indication we have had without tests.

Q. (Kelvin Horr, Ball Brothers Research Corp., Boulder, Colorado) Could you give me some idea of how you arrived at this 2% weight loss figure as being an acceptable one?

A. I would have to say that we had to pick a number and this sounded like a good one.

Q. Second part of the question. Did you precondition or preclean or bake any of your materials before your weight loss test?

A. Negative. We were not allowed to prebake any sample before vacuum exposure.

Q. (Bill Salsbury, McDonnell Aircraft, St. Louis, Missouri) Can you tell me the maximum wattage dissipation of any cell that you are using?

A. Eight hundred milliwatts, that is an average heat dissipation.

Q. (Jim Bennett, Defense Research Lab., Ottowa, Canada) I gather from the information in your pamphlet that the nine by six panels of the AMP/MECA circuits will not take vibration from the satellite environment. Do you have to resort to isolation pads?

A. The units are vibration isolated in the spacecraft.

Q. This was found to be necessary, was it, to meet the vibration levels that you expect or have to pass?

A. That is correct. It was felt that it was best to plan on vibration isolation for the equipment.

Q. (Russell Dawe, Jet Propulsion Lab., Pasadena, California) What did you consider or take as a maximum temperature for components and what was temperature difference from the components to the temperature control skin?

A. The maximum allowable temperature that we permit in the package is 185^{o} F.

Q. (Mark Hurowitz, Sylvania Electronic Systems, Mountain View, California) What was the material you filled the AMP cell with?

A. We used three different materials. We used Shell Chemical Epon 871 and 828 epoxy combination in one cell type or category. We used a Furane epoxy in a second cell type and we used the Epon 828 and 871 filled with lithafrax in another category. They were all epoxies – one was a filled epoxy.

Q. (Ron Kellis, Northrup Space Laboratories, Hawthorne, California) Did you run any specific checks on a resin system exposed to hard vacuum at various temperatures? And if you did, was it a filled resin rather than a simple straightforward resin?

A. I neglected to mention that one of the requirements for vacuum testing was that the material also be exposed to 100^{o} C temperature. This, it was felt, would accelerate any outgassing and weed out the bad materials during the tests. Specifically we tested the epoxies that were used in the cells and they were found to meet the acceptance criterion. There were several epoxies tested that are listed in the back of the paper and there are others I did not list.

Q. (Bill Tacy, General Electric Company, King of Prussia, Pennsylvania) Did you use any Corning glass resistors in your component?

A. To the best of my recollection we did not use Corning glass resistors but we did use Corning glass diodes.

Q. What protection did you use to keep the curing stresses of the epoxy from damaging the glass cases?

A. We tested epoxies used for encapsulating the cells that contained these diodes. In fact we potted one cell that had nothing but diodes in it and subjected it to temperature shocks. We potted with unfilled epoxy since it shrinks more than filled epoxy that we are actually using and it is clear so we were able to visually examine the diodes in the epoxy. We potted the cell with epoxy which contained diodes and we then broke the cell case off from the epoxy so we had a block of epoxy with the diodes in it. We then subjected this to temperature shock, that is, higher and lower temperatures than we actually expect to encounter, and examined the diodes for crazing. We found no evidence, nor have we to date found evidence of crazing or otherwise damaging the diodes.

Q. (Ray Bocchio, Douglas Aircraft Company, Santa Monica, California) I noticed there are quite a number of thermal interfaces between one cell and the cold plate. It seems to be pretty far away. Did you use any compounds between those interfaces, and what are the compounds?

A. Yes. We are using an interstitial material of RTV-11. I would not say that is the only material which could be used. We fill the RTV-11 with a lithefrax, not so much to improve the thermal conduction of the RTV but to control the outgassing.

Max Callen-Honeywell Electronic Packaging for Apollo

Q. (Roy Malarik, Lear Siegler, Inc., Grand Rapids, Michigan) Did you have to reform or reshape after dip-brazing?

A. We experienced a slight amount of distortion in the dip brazing. It has been easy to reshape, and the final machining of the base provides for the approximately ten thousandths TIR that is required for the cold-plate interface.

Q. (Tom Sawyer, General Dynamics, Pomona, California) I was not quite sure how you faced off the edges of your modules relative to the ends of components. Was this an electrical exposure to the outside of the module and used to obtain heat conduction through to the cold plate? Did this interfere with the electrical characteristics of the module?

A. None of the leads of the components are bent. We used a buss bar to interconnect them. Therefore, the leads of all the components extend out through the surface of the module. After the module is assembled it is machined off flush. There is no electrical connection made at that point, but we do get our thermal interface at that point.

Q. What environmental protection is afforded the assembly?

A. The cards are provided with a conformal coating after assembly.

Q. (Jim Patterson, Motorola, Inc., Scottsdale, Arizona) What would be a maximum condition of power dissipation per chassis or chassis assembly, and do you use anything between the bottom of the chassis and the cold plate for an aid to conduction?

A. The maximum power dissipation is approximately 20 watts per chassis. If you noticed the last slide, it showed up to 32 watts per card. We have some cards which have up to 32 watts dissipation, but the duty cycle is quite low so we end up with an approximate average of 20 watts per entire chassis.

Q. Do you use anything between the bottom of the chassis and the cold plate?

A. The cold plate is made up of small rubber tubing wrapped with twenty-thousandths copper material. The copper tubing is brazed to the cold plate that forms the interface between the bottom of our chassis and the cold plate.

Q. (Al Abel, McDonnell Aircraft Company, St. Louis, Missouri) What type connectors do you use on your cards?

A. The ones which we are presently using are the Amphenol Printcirk type connectors.

Q. (Jake Rubin, ACF Electronics, Randallstown, Maryland) You mentioned a postbrazing heat treatment on the dip-brazed assembly. Normally there is a cleaning process following the dip-brazing in which the assembly is subjected to boiling water or other devices for getting rid of the salts, and they are allowed to age harden in air. Is this the process you are speaking of or was there a subsequent heating-and-cooling cycle?

A. There is an air quench following the removal from the dip-brazing bath. Other than that I think it is as you stated.

Q. (Joe Kruzich, Bendix Systems Division, Ann Arbor, Michigan) Could you tell me what aluminum alloy and what thickness was used in the brazed chassis and what the brazing alloy was?

A. I can only answer part of that. The thickness of the material, for the top plate and for the superstructure, was 50 thousandths and the base plate was 200 thousandths and the base plate was 200 thousandths. The material of the chassis itself is 60-61. I cannot tell you what the brazing alloy is.

Q. Could you tell me how you maintained the thickness of the viscoelastic material between the two thin aluminum sheets of the cards?

A. I believe, in production, that this will be sprayed on.

Q. (Dave Craig, Rome Air Development Center, Rome, New York) The diagram of the card cross section showed that the heat path was from the cold plate through the aluminum plate, through rubber cement, another aluminum plate, fiberglass to the module. Is this a special rubber cement and fiberglass material to get heat flow?

A. The fiberglass material is much the same as used in printed circuit boards, but I believe it is only five or seven thousandths thick. We do not experience too much of a problem of a thermal interface across the contact cement between the two halves because there is such a large area in contact. For the purpose of thermal conduction it acts as a single piece of aluminum.

Q. (Joe Bubnekovick, Burroughs Corporation, Paoli, New York) Referring to your Figure 3, where you have your module assembled between the two plates in the structure you show another tab that looks like a piece welded to come out of the module. Is that right?

A. Yes. That is more symbolic than actual. If you care to look at one, I have a finished module.

Q. Are these pieces welded to the back of the component leads? I assume there are many in the module. Wouldn't this be the thermal path for the heat to escape and be entrapped in this center of the structure? You show nothing about a thermal path or heat being conducted out through this point.

A. That is right. Heat, like water, only flows downhill. If the center section becomes hotter than the component itself, the heat would flow back the other way. So the components, as it turns out from our tests, are the hot spots in this design.

Q. I understand that, and I understand the heat coming out of the component leads, but I still would like to know about the welded sections that come out of the module. Do you have any heat path there at all?

A. Oh, I am sure there is some. It is relatively small. This is the only connection into the internal wiring of the card and I am sure that some heat follows that path. Here again, if that becomes hotter than the component itself, the heat flows the other way. So there is no problem.

J.J. Okada-System Packaging Design of a Digital Flight Control Computer

Q. I do not understand the interconnection method you are using between the 1-in. module and the interconnecting block. Would you mind reviewing that, please?

A. I will be glad to. You will recall the paper by Russ Frank on the matrices. This interconnection is similar to the point to point connection he mentioned. The tubes are welded at right angles to nickel ribbons. In this case the ribbon was seven thousandths thick and twenty thousandths wide. This nickel ribbon is connected in the conventional manner on either side of an insulating film and is brought out from the assembly to wire wrap pins. For this prototype we are also evaluating a soldered method using tubes. You are not limited to tubes. A bridge method can be used for the wiring between two points. This method is not as clean because there are two wires for every termination. I would imagine that there are people here who could suggest six or seven more ways.

Q. (Joe Ingber, Airborne Instruments Lab, Deer Park, New York) If you have a single component failure, do you have to throw away the whole block with all the gates and flip-flops on it? How do you remove the 1 by 1 in. module from the rest of the block?

A. The 1 by 1 in. modules are bolted to the aluminum structure and these modules are removable – in this case by clipping the tube connection and removing the module. It depends upon when the component fails. The repair I propose for this system is that a high

quantity of these logic functions that were tested and completely qualified would be stocked. If a 1 by 1 in. module was found to be defective, the module could be replaced. This is the manufacturing repair level that has been set for the particular device.

Q. (Leo Grizel, Nortronics, Hawthorne, California) Did you say that your nickel ribbons were prefabricated on your 1 by 1 in. module?

A. No, this is not so. The interconnection of the 1 by 1 in. module is a point-to-point interconnect. We evaluated circuit similarities within the computer. It was not readily apparent that we would find many similar function groupings to make it worthwhile to buy interconnects of this type. The design aim was to keep interconnections simple so that the interconnect scheme could be arrived at quickly and the manufacturing be done easily. The interconnect pattern was nothing more than a grid of holes. You can visually indicate how these are connected by just showing these on microfilm slides.

Q. (Don Schnorr, RCA, Camden, New Jersey) You mentioned something about freeze coating your modules. Would you elaborate on this a bit?

A. Yes. We freeze coat the function module and also the 1 by 1 in. module to protect the interconnections. Unfortunately, the first material chosen for the freeze coating, that was commercially available, dissolved the body material on one of the components. Fortunately these components were in accessible areas and were replaceable. To eliminate the dissolving of the component material, we used an RTV clear silicone rubber compound. I think the number was RTV-602.

Q. (Dick Barba, Sperry Gyroscope Co., Great Neck, New York) How many wire wrapped terminals do you have to undo in order to remove an assembly and is this a reasonable function for a field repair?

A. The number of connections to a block have been approximated to be an average of 90 to 100 connections. This is based on the analysis of what the computer divisions would be. In a miniaturized airborne computer, you could not provide a less sensitive area to undo as a field repair break than a wire wrapped area. I would hate to have to ask the military services to clip tubes and make welds. Does that answer your question?

Q. (Bill Emmons, McDonnell Aircraft, St. Louis, Missouri) On these wire wrap interconnections, have you run any environmental tests on the requirements for the airborne applications?

A. Not yet, for several reasons. This is still downstream in the development program and there are other areas to work on first. Secondly, there are good companies working on wire wrap connections (companies like RCA and Gardner-Denver). There are several companies (like Lockheed) evaluating the split-pin approach in which two adjacent pins are wrapped to each other.

John R. Woods-Design and Construction of a Polaris Timer to Space-Available Configuration

Q. You indicated a marriage between a flex print and a matrix. Have you tried a nickel flex print carried out from the connector all the way around and through and becoming a part of the matrix, or several matrices? We have found that this can produce a very rapid solution to that type of problem without the extra set of pins.

A. We have used almost every method of getting to the outside world that you could think of. We have used the feed-throughs through matrices. In this particular instance the tape cable seemed to be the solution. This particular piece of hardware is such that it could not be tested at the module level. We actually had to assemble the unit before we could even test it. There are so many loops in the circuits it would have been impossible to test any other way, so we thought that a piece of tape cable would allow us to lay it off to

the side. Then if it worked before anything else happened to it, we could drop it back into the can.

Q. I don't know if you understood me. The flex print cable is available in nickel. It can be carried through and become a part of the matrix itself. So you have half of your matrix already there, without any connection whatsoever.

A. We have looked into this flex cable. As a matter of fact someone was telling us how they could make a matrix out of a couple of pieces of flex cable, and it looks like it does have possibilities. Unfortunately, again, I have to plead time as we have never had the time to go out and really investigate it.

Q. (Bill Volk, Westinghouse Electric Corporation, Baltimore, Maryland) You mentioned a freeze coat to coat your modules to find electrical shorts, or opens I should say, prior to electrical tests. How do you remove the freeze coat in order to repair the modules? Is it alcohol solvent?

A. I use my precision sandblaster.

Q. This costs money?

A. No, it is just that we have the thing right in the lab. It is just a matter of walking over if you have an open, blast it off. It is less than a minute.

Q. (Carter Ames, Sylvania Electric Company, Mountainview, California) You mentioned foam encapsulants and recommend them highly. We have experimented with those too and have found that in cases it is very difficult to control them as to foam cell size and how far they blow up. How do you handle this?

A. We have been using foam. We do not get too much uniformity. Frankly, it is no problem, the reason being that the final system is encapsulated anyway and the only reason for the foam is to take up a little volume with a minimum amount of weight.

Q. Yes, I agree to that. However, if you come out with a very uneven foam, then in places your components are not as well embedded as in other places where you have a very dense foam.

A. This again is true and I agree. The only answer really to that problem is the experience of the operator. Three people do this foaming and I can look at it and tell you who did what, primarily because it is a case of just handling it. You have to get it in there fast. We generally apply a little finger pressure to the two holes as described in the paper. It is a case of feeling when it starts to turn and experience is your only teacher. There is really no way you can control foam in an enclosed mold. You do not have the time to accurately measure the amount of foam you insert. You just have to push it in until it comes out the other side and hope you are right.

Q. Which foams do you generally recommend?

A. Well, we have been using FPH lately.

Q. I have never heard of it.

A. It is an Emerson-Cummings product.

Q. Oh, I see. It is most likely a urethane foam?

A. Yes.

Q. One final question. I didn't hear anything about the materials you use for insulation, between the different layers. Do you use Mylar insulation or have you experimented with more rigid types.

A. No. We use Mylar almost to the exclusion of everything else, for the simple reason that the art work is on Mylar which guides the operator. We use clear Mylar. A lot of people use a matte finish, but we use a clear Mylar.

Q. Incidentally, on the last statement, I might mention that Sylvania has developed a little sandblasting device which is very versatile and we even patented it. We have used it quite extensively, and I can only recommend it.

A. Good. Got a plug in.

Q. (Dick Kirn, EMR, Inc., Sarasota, Florida) With regard to the problem of the stabilization of the foam, Dow-Corning does make two stablizing agents for addition to urethane foams. They greatly enhance the cell size stability and the uniformity. I cannot think of their numbers off hand but I am sure one of their representatives could supply you with the information.

A. Yes, I have had a little discussion with people about these. I guess if we ever build an exposed system where the people can look at it, we will start worrying about it. But again, the reason we use it is basically to take up space.

Q. We use foam for a complete system and with the stablizer we get a very good finish on the surface and fairly good cell size stability throughout the whole package.

A. Good, we will have to try it.

Q. (Jim Adams, ITT, Clifton, New Jersey) I understood you to say that the housings for this receiver are all machined. Is that correct?

A. That is correct.

Q. If this was going into production what would you propose?

A. We had a foundry give us a bill on casting it and in quantities of about eight you reach a break over point. I believe you could cast this. The house we contacted only cast 90-thousandths walls and you still have to do a lot of finish machining. I think in production quantities you would cast this machine.

Q. (Don Schnorr, RCA, Camden, New Jersey) You said you use nickel in order to meet corrosion requirements and yet you say it is undesirable for a radiation environment. How do you justify this? Do you still use it?

A. Yes, we do use it. We were forced to find a solderable finish on the aluminum and we sent the list of materials (which are covered in the paper) to the materials group and asked for their recommendations for performance in this radiation field. They said there were two primary factors in radiation. One is that the material becomes a secondary source of radiation, and two, the material is physically degraded. We said we had to use something conductive, and they said nickel or gold are probably the best for solderability. However, they are probably not too satisfactory for radiation in that they do become activated. Gold is the worst since it does decay and nickel merely becomes activated. We said we would try one on nickel. We sent it to the Reactor Facility in Fort Worth and it performed satisfactory. The secondary activity of the nickel did not degrade the receiver.

Q. (Mark Hurowitz, Sylvania Electric, Mountainview, California) Did you use any RFI material between your sections?

A. No, we designed it out. We had some sad experiences with that and we tried to get rid of it in this receiver. I did not mention it, but I think it is in the paper, that the receiver sensitivity is -115 DBM; however, it has been developed with a new front end with -168 DBM and we have not had to use this material.

Q. (Otto Jahnke, ITT, Clifton, New Jersey) Have you investigated the tinning of aluminum over a copper initial deposition?

A. Yes, we have. Tin, unfortunately, turns out to have a rather high resistivity. I think the conductivity is 15% of copper and the circuit engineers said this was too high for them. So on the board materials we had to use the nickel materials, with gold over them. They relented, however, and let us go to nickel, which is 22% of copper, on the outside surfaces.

Q. (Mohi Sobhani, Litton Systems, Inc., Woodland Hills, California) Have you tried ultrasonic soldering or a technique which does not require any plating of aluminum joints?

A. We bought an ultrasonic welder. I have not done ultrasonic welding. We do have an ultrasonic welder in the lab at this time and we are evaluating it now.

Q. (Dick Yost, Univac, St. Paul, Minnesota) On welding on a cast unit, I would like to suggest that you may want to try investment castings. We have gotten very thin walls on these and they have done an admirable job for us on a computer that we built. There are a few capable investment casters who can make thin wall castings and are good for a job of this type.

Q. (Tom Gollete, McDonnell Aircraft, St. Louis, Missouri) What kind of problems did you have with moisture, or did you have any?

A. No, moisture did not develop into a problem as far as detuning of the RF circuitry. Once the epoxy material is on (it is Epon 828 with ZL-308, 100 parts to 50 parts), it satisfactorily prevented any damage from moisture or detuning of moisture.

Q. (Jim Patterson, Motorola, Scottsdale, Arizona) You mentioned using these rates at X-band radar and also in 2-kMc receiver. Are you using the techniques as they were in this receiver?

A. Yes, exactly the same techniques. I will hedge a little on the X-band receiver. The X-band multiplier goes up to 674 Mc and that is where you go into waveguide. That is as high as we go on that one. The 2-kMc receiver is built like this all the way to 2 kMc's.

Q. (Ron Pitman, Sylvania Electronics, Mountainview, California) What material are you using in your IF transformers? For the cores?

A. That I do not know. It is one of the standard core materials.

Q. I noticed that iron is on your list of materials considered unfit for radiation environment and I was wondering if a powdered iron or a ferrite would also come in this category.

A. I do not believe so. The ferrite has not acted up. Again in these tests the original core coils were made of fiberglass. It discolors in radiation but there was no degradation of the electrical performance.

Q. (Clyde Stroburg, Sr., General Dynamics Astronautics, San Diego, California) In your paper, you suggested that it was undesirable to seal against the vacuum. Would you care to elaborate on this?

A. The receiver has a lot of testing, a lot of manufacturing steps, tuning, and a little black magic by the circuit engineer. If you use a sealed unit you sort of limit yourself to the versatility of the unit and we really found no reason to seal it. We did not want to go to the added expense and troubles in the receiver. There is nothing that is degraded by vacuum or by radiation. So there was no need to seal it.

Q. (Jim Bennett, Defense Research Board, Ottawa, Canada) You stated the carbon composition resistors and paper capacitors are severely degraded by radiation. What are your replacements for these components?

A. We deposited metal film receivers.

Q. And for the tantalum capacitors, what are you using to replace those?

A. The tantalum capacitors were defective only in that they became leaky. It was in the sweep amplifier that they were used, and the leakage did not bother them. If it was in a very low leakage type circuit you would have to use something else. In this particular circuit it was not a problem.

Q. (Ray Bocchio, Douglas Aircraft, Santa Monica, California) I noticed that you had to design to a spectral density of about 0.5 over quite a large band width. Did you have any vibration problems?

A. That is one of the advantages of this heavier construction. We found on all planes the transmissibility was quite good to about 1 kc and it increased to 3 and stayed there to the end of the tests. I think 2 kc was the test. So our transmissibility never exceeded 2 anywhere in the receiver.

Q. (Bill Morgan, Hughes Aircraft Company, Culver City, California) You mentioned that your interstage shielding is provided by the compartment walls fitting tightly against the circuit board. How do you take up production tolerances and still get the tight fit?

A. There are screws which go through the board into the cover. We machine threaded inserts—I think they were helicoils — in the cover and the board is drawn against this cover by these screws. In most instances at IF frequencies of 40 Mc you can stand a gap approaching an inch between two contact points between a shield and a board. We had no trouble achieving this, even with manufacturing tolerances. We try to keep it about a half inch.

Kenneth W. Plunkett-Electronic Module Connectors

Q. (Bill Ladoulis, Raytheon Corporation, Wayland, Massachusetts) In this last slide you showed an application of the module which is a very clever design in keeping the connector size down. I was wondering how you locate with those two stand-offs? How do you polarize so the module is not put in backwards?

A. You have a good point and it obviously has no polarization. This is something that will have to be corrected if it is ever used in production.

Q. Is it possible that you could make one of those stand-offs square and the other one round?

A. We have considered using the stand-offs as one means. Another possibility is putting a pin in one of the corners of the header. In fact, there are several ways in which it could be done.

Q. (Ed Moore, Martin Company, Orlando, Florida) In the welded module application I notice the beryllium copper spring welded to the circuitry. Were any problems encountered in making this weld?

A. No. In making that particular circuit we did not have any problems. However, it is a good point because welding to heat-treated beryllium copper, which in this case was extremely brittle, is a problem. However, we just made a few simple weld schedules. We did not have an elaborate weld schedule. We were getting pull strengths of about 14 lb, and breaking the nickel wire. So I will not say it was a good weld but it was strong.

Q. (R. A. Morrison, Walter V. Sterling, Inc., Claremont, California) On the application of this spring to the printed circuit, were you able to run any tests that proved the wiping action to break a corrosive film on the printed circuit?

A. Specifically no. I do not think we had any tests that would demonstrate that. We had contact resistance tests of course as you have seen in the paper, but this was on a fairly clean board and all I can say is that we had a force of about a pound per spring. While theoretically you get a minute amount of wiping action, whether this would go through a corrosive film I could not predict. However, I feel pretty confident in using this in the internal construction of computers where I do not believe we are going to get that type of corrosion.

Q. (Winthrop McMaster, Bell Telephone Laboratory, Whippany, New Jersey) You very probably have noticed, Mr. Plunkett, that the effectiveness of a connector is pretty largely determined by how well it stands up in the hands of maintenance personnel. It occurs to me that in fear of twisting off a hold-down screw, a maintenance man is pretty apt not to pull up a screw tightly. The effectiveness of this connector is pretty largely dependent upon how well those hold-down screws are tightened. Do you have any data on the effect of the contact resistance when the screw is an eighth or a quarter turn off of being seated?

A. We did not document it in our report, but I did make some bench tests to try to discover the relationship between contact pressure and resistance. We also utilized some tests made on a different connector correlating resistance vs. pressure and found that the break-off point is around 50 to 200 grams to where you really start seeing a change in resistance. Now we have, as I say, about 1 lb, 450 grams or so.

Q. How were the guide studs fastened to the printed circuit boards?

A. They were pressed in. They have a straight knurled shank. They were pressed in and then swaged over on the bottom.

Q. (John Roderer, Sr., IBM Corporation, Kingston, New York) I notice that you have only partially utilized one corner of the circuit board or have you used the complete board for your circuitry in that particular module?

A. I do not understand the question. We only used that portion for the module connectors.

Q. It appears that more of the board could be utilized if such a unit were to go into production.

A. Right. This application, I will have to admit, is sort of an afterthought. The module connections were not designed for that application. We had an idea for a module connector and we made it and we felt it would be usable. On this particular prototype design, we use a similar connector called a becon connector, which is a pressure connection between perpendicular printed circuit boards. We used those throughout that particular application. The design did not lend itself too well to modularization other than the circuits we had there.

Q. (Howard Zimmerman, U. S. Naval Ordnance Lab., Corona, California) Was any consideration given to the exact length of the contact spring and its radius of curvature? It occurs to me that the pressure can be increased by increasing the radius of curvature.

A. You are correct. However, we do not need increased pressure. It takes quite a bit of pressure to bolt it down now, I think about 11 lb. I believe we will try a different kind of heat treatment to decrease the brittleness of the contact. That would also reduce the contact pressure and at that time I think we could shorten the length of it and perhaps put on a double row, instead of a single row.

Q. (Al Fitak, TRW, Computer Division, Canoga Park, California) In what manner was the contact spring assembled into the connector? Was it molded in or was it inserted later?

A. It was inserted later. The header was drilled out, the contact springs were inserted, and we used a little adhesive on the back side of the module just to hold it in place. I do not know the name of the adhesive.

Q. (Carl McCann, Motorola, Scottsdale, Arizona) Have you given any thought to the application of this module type connector to a double-sided printed circuit? If so, what are your thoughts about a conductive path from one side of the board to the other?

A. I am sure that it could be used there. As for getting from one side of the board to the other, I really do not know how well we would do it. I don't think I would use plated-through holes right now. We do not have a lot of experience with plated-through holes so we would probably use eyelets or wires or what have you.

Q. (Ralph Taynton, RCA, Morristown, New Jersey) Your connector seems to be particularly adaptable to a three-dimensional type module. Have you done any work along the lines of a planar type module and if you shortened the springs would you still be able to make this thing work? Also would you reap any volume savings in actual cubic inches per mating pair of contacts?

A. You can certainly design a smaller spring that would work with a planar type module. I have seen some at the Astrionics Lab in the Marshall Space Flight Center, in Huntsville. They have a smaller spring. With the proper design it would probably work with the planar module. I could not quote you any figures on the amount of volume you would save as it all depends on how you designed it.

Q. How about in your present configuration? Have you made any study of the actual volume savings rather than a planar area?

A. No. I have not played with any figures.

Q. (Doug Allred, Sylvania Electronic Systems, Needham Heights, Massachusetts) I think you have a novel and interesting approach. However, I wonder from looking at the attachment scheme for your module whether or not weight and the complexity of the attachment is of a primary consideration in your design approach? Would you comment either on how much importance it played in your original considerations or what are your plans for the future regarding attachments? It looks like it is exceedingly heavy.

A. It could be a factor. It obviously requires slightly more weight than would an embedded insert in the middle of the module which is commonly used. We did not really consider weight when we were using this. The main reason that we have it connected as we do is so that we could remove it without requiring access to the bottom side of the board. There has been some reconsideration and redesign as to exactly how we would arrange this. I cannot say if we would do it exactly the same way.

Q. (E. E. Garrett, Amphenol Borg, Broadview, Chicago, Illinois) In the case of the beryllium copper spring, did you carry out that heat treatment before you plated with gold or after?

A. It was before plating.

Q. (Jack Elsley, Cinch Manufacturing, Chicago, Illinois) I would like to ask a two-part question. First of all, would you care to state exactly how you measured contact resistance. How much is inherent in the material of the spring and the pad on the printed circuit board and how much is due to the mating of the two? The second part, what plating did you use on the contacts and on the board?

A. That is a very good question because it is very difficult to find what the contact resistance really is and I think that most of us expect to find it as the resistance between the input and the output leads of the device. In this case we did not have any real input or output leads except that we put in some dummy terminals at the top to get continuity from the PC board through to the top of the module. Now in the design that I was talking about, number 3 here, the way we arrived at the low contact resistance figures was to measure the resistance of the internal module connections. That is from right at the base of the contact spring up through the top of the module as one factor. We measured the conductor

pattern on the PC board from the point at which we were probing to about the middle of the spring. We subtracted these two factors from our total reading, trying to arrive at a contact resistance. We did not do this just to show that it was low, we were doing it to try and see if the contact resistance itself was changing throughout any of our tests. Now in the other designs, number 1 and 2, we did it differently, we just took the overall resistance from the PC board through the top of the module and let it go at that. The plating on the board was 100μ in. of gold plate over copper.

W. McMorran, D. Grassi, and B. Edgerton-Packaging Flyable Welded Miniaturized Computer Electronics

Q. (Ralph Taynton, RCA, Morristown, New Jersey) How do you envision getting the TI elements off the card?

A. You cut the leads up close to the body and parallel weld your replaceable unit directly on top of it. You don't have to do too much surgery.

Q. You said that you aspire to a better connector or a more applicable one. What type of connector do you aspire to?

A. It is pretty obvious what we would like. The module leads on our grids are on fifty-thousandths centers and we would like something along that line (That is a reliable connector that would exploit this size advantage.) There are one or two connectors that I think have been tried to solve this problem.

Q. Is all your welding done with nickel wire?

A. The wires in the cross-wire versions are all nickel. In the solid multilayer type they take nickel wire and copper plate it, so one end can be plated into the board. Later, the exposed portion of the wire has its copper stripped off so only the nickel remains.

Q. Do you find that you are having to make an adjustment on the TI bug lead?

A. No, because we are welding three by ten Kovar to ten-thousandths round nickel wire. We hope eventually to be able to easily semiautomate that, since all of the welding is on fifty-thousandths centers.

Q. In Bywaters presentation he had to measure the cross-sectional area of the TI bug and program his parallel gap welding equipment accordingly. You have not experienced this?

A. No, not when we use conventional resistance welding. We build the wire matrices fully automated now. We have some cases where we are welding twenty by twenty nickel to ten by twenty nickel, and five by twenty nickel to five by twenty nickel. But everything is at the same height and it's all the same material.

Q. (Carl Leonard, General Dynamics, Astronautics, San Diego, California) You mentioned a parallel-gap welding repair capability. In the paper I noticed that you have two circuit boards, back to back; how do you maintain welding electrode pressure with this setup?

A. That is entirely dependent on how the head comes down. Right?

Q. Isn't a backup required on the opposite side of your welding electrodes?

A. No. Can I take just a minute and explain this? If these are your two electrodes and this is your contact pressure, you are essentially blowing or melting two fuses together at once. We are talking about the parallel resistance along the bug lead and the printed board between your contacts. The current path is through here and through here. It works out better if you have the same materials; or lacking that, you would like the lower melting temperature to be on the bottom, so your contact pressure is purely mechanical from

the top; and in essence, you are half-blowing two fuses simultaneously. Yes, you do have to back it up mechanically. That is pretty important and the pressure you can use is variable. We use G-10 underneath and this is held just in a mechanical stop so it cannot yield any lower under pressure. The behavior of this pressure as you are making the weld is important.

Q. (Sam Francis, Sipicon Corporation, Marion, Massachusetts) You were talking about the two million welds before you had a failure in the field. In the old days we used to have failure reports come back from the field. This was the mechanism by which the user analyzed the performance of the manufacturer. Now that we have interconnections which have one in two million failures, as in the case of the wire wrap, I have never heard of a case being bad. These field reports are quite after the fact. They are of technical interest to the manufacturer and the user, but they have really nothing to do with the reliability of the gear. My question is about failures inside the plant before the equipment goes out the door? What is the ratio you find between those outside and those inside?

A. I think we are pretty close to Ivory soap there. We are about 99.44% pure. Seriously though, the process, as you yourself know, is to take away as many of the variables as possible. I think we now have the situation where a girl is much more apt to miss making a weld entirely than she is to make a bad weld. It varies day by day, of course, and we keep very good records. But I think we are something below three or four bad welds per thousand, for all welds rejected for all causes, including missed and wrong connections. Many of these welds are good welds, but for one reason or another fall below inspection limits. Incidentally, the worst day we had was an overtime day which was New Year's Day.

Q. (Bill Volk, Westinghouse Corporation, Baltimore, Maryland) I noticed you are using a lot of small chips in this package. The Navy has what they call the FIR, Functional Item Replacement; the Air Force has the LRU, Line Replacement Unit with throwaway costs ranging from $50.00 to $100.00. How do you justify putting $800.00 worth of components in and about $300.00 worth of manufacturing costs?

A. I think in this case it is a little closer to $400.00. I am sorry but I cannot really get into the customer uses. I am not allowed to talk about it.

M.E. Ecker, H.R. Kaupp, and D.P. Schnorr-Separable Multicontact Connectors for High-Speed Computer Circuits

Q. As you go through this etch board connector system you are passing over the DC power supply wipers before you get to the Co-ax at the bottom. Must all the energy be removed from these before you insert or remove a wafer?

A. This is correct. A danger exists of connecting a low-voltage circuit with a higher-voltage bus or of shorting power busses together if wafers are inserted or withdrawn without the power being turned off.

Q. (Irv Christensen, General Electric, Phoenix, Arizona) What dictated your selection of the characteristic impedance? Was it the cable, circuit design consideration, or just the mechanical considerations that you had to take?

A. It was the circuit design consideration. I would also like to mention that the coaxial cable that we used contributed somewhat to our choice. Initially we had some difficulty in obtaining this coaxial cable since we knew of no other applications for this type of wire. Our first attempts consisted of having a contractor draw copper tubing over lengths of Teflon-clad wire. Evidently, some trouble arises in keeping the characteristic impedance uniform, since impedance depends on the thickness of the Teflon, and tight manufacturing tolerances are very difficult to maintain when the wire used is very small in diameter, as ours was. So you may say that our selection of characteristic impedance was also somewhat determined or influenced by the kind of coaxial wire we could actually obtain.

Q. (Leonard Yuska, United States Naval Avionics, Indianapolis, Indiana) Who was the contractor?

A. This coaxial cable with a solid outer conductor was made by Precision Tubing of North Wales, Pa., and also Uniform Tubes, of Collegeville, Pa. The latter firm I understand now makes the complete product, instead of just performing the tube-drawing operation. Presently I believe it is possible to obtain, as a standard product, coaxial cable with an outside diameter down to about eighteen thousandths. However, as I mentioned previously, we did experiment with coaxial cable with an outside diameter of eight thousandths, but it becomes just too much of a problem in techniques to handle at such a small diameter.

Q. (Clarence Sieben, Univac, St. Paul, Minnesota) Did you have electrodeposited copper or drawn copper and does it make a difference in your high-speed computer?

A. We have used both electrodeposited and drawn copper and find that the drawn copper gave us by far the best results.

George Messner-Multilayer Printed Circuits

Q. (Tom Sawyer, General Dynamics, Pomona, California) Could you tell me the diffusion temperature for this taper pin with the indium on it?

A. The diffusing temperature is around 350^{o}. The epoxy board is not damaged by this temperature.

Q. (Leo Gidro, Hughes Aircraft Corporation, Culver City, California) Do you have any record of failure rates on the connection between the taper pin and the plated through holes after the welding of the TI "Bugs"?

A. We did submit the first samples to a university and they ran some very extensive tests on them. They subjected them to their regular testing regime and when the boards could not be damaged, they kept increasing the severity of the testing. They just could not break this type of joint. Now that is not a statistical evaluation, but it is a very good indication of the strength of this joint.

Q. (Bob Matzinger, Martin Company, Orlando, Florida) Do you have any comments on the reliability of the plated through holes on the multilaminate boards? What are the thermal shock and the vibration characteristics and thermal cycling?

A. I gave some of the results in my paper about what testing we, and some of our customers, had subjected the boards to. I will make only one comment: If the joint is made well, it will not fail and until we arrived at this stage of producing such joints well, we have had failures. I would say, for multilayer boards, a very severe test is heat shock. But as I just mentioned we sent 180 boards with holes on 50 mil centers through a hundred cycles of heat shock without a failure. I do not know how much further we can go.

Q. (Dean Joachim, Univac, St. Paul, Minnesota) It is generally accepted that there should be a three-to-one ratio between the board thickness and the hole size. What has been your experience in this area? Have you been able to exceed this ratio perhaps by four to six?

A. Yes, we have been able to exceed this ratio to approximately five to one and six to one under laboratory conditions. However, we limit it arbitrarily at three to one for production of boards. And we have very good results with this ratio.

Q. (Bill Salsbury, McDonnell Aircraft Co., St. Louis, Missouri) You stated a ratio, I believe, of approximately three times the cost of a conventional two-sided printed circuit board. Upon how many layers are you considering this cost comparison?

A. We made a price table using a six-layer board, with a certain number of holes. We went through the regular process of pricing this board and then two-sided boards, equivalent in size and with the same number of holes. In medium quantity ranges we were very close to this ratio. In large quantities, the ratio is smaller and for a smaller quantity it is somewhat larger. There are too many variables to account for when pricing multilayer boards, so it is hard to say how well this approximation will be reflected in each case.

Q. (Joe Kruzich, Bendix System Division, Ann Arbor, Michigan) I note in your paper that you show the Fusicon technique as being used in a board smaller than this which is applicable and what is the thinnest board you can use?

A. I would say that we should not go below about 1/32 in. in thickness as the joint between the pin and the hole then gets pretty small. On the other side, the ratio of three to one for a 20-mil hole holds true. Therefore, 62 mils is the upper limit.

Q. (Bill Ladoulis, Raytheon Company, Wayland, Massachusetts) What is the yield? You said you had made some for a system. How many do you start to get so many good ones out the end?

A. Recently we had no failures due to opening in the hole; however, we certainly had failures due to other things like nicks or pin-holes. That depends on the complexity of the board and is hard to generalize.

Q. (Walter Prise, Lockheed, Mountain View, California) I would like to have a more detailed description of your indium diffused bond.

A. The mechanism is that at fairly low temperatures indium has a property to diffuse into copper. As you know, the melting point of indium is about 310°F, so when this temperature is exceeded it will start diffusing. This diffusion process, once started, will continue at room temperature so the joint is growing stronger with time. However, you have to trigger it. Now diffusion will occur only when you have a close proximity of indium to copper. This taper pin provides a slight radial pressure, which is required to start the diffusion, and after this diffusion process has begun, it actually forms a new alloy structure. You have at the junction a copper layer first, then copper-rich indium alloy, then you have the same thing on the other side of the junction. I did not bring the slides, but we had some metallurgical specimens made which exactly show this new alloy. The slides show different shades between gray and orange of copper, depending on the amount of diffusion.

Q. (Roy Malarik, Lear Siegler, Grand Rapids, Michigan) What inherent advantages do you see in the plated-through technique over the multilayer board buildup by lamination of the "Intellux" technique?

A. I would say there are several limiting factors. Basically, Intellux has a very sound method, too. I would say the cost and size of the Intellux method are the limiting factors.

Q. What are the tooling charges?

A. The tooling charges are the same as for a regular two-side board with the exception that you will need an additional tool called a laminating fixture. It will cost you about $100.00 per fixture. This is the only extra tool which is needed for multilayer manufacture which is not conventional.

Q. (Dick Bywaters, International Data Systems, Dallas, Texas) What is the closest you have been able to plate through holes and on what center line?

A. Holes spaced on 50 mil centers.

Q. Just one other quick one, what is the closest you have been able to etch conductors in the multilayer process? What kind of center lines?

A. Ten-mil lines and 10-mil spacing.

Q. (Mori Sobhani, Litton Systems, Inc., Woodland Hills, California) By using the multilayer boards, aren't you limiting the repairability and maintainance to practically nothing? It would be very costly to use multilayer in any system unless you are sure that the circuits are not going to be changed.

A. Yes. There is a problem in repairability or changing the circuitry with multilayer boards, but that can be gotton around by proper steps in design and prototype sequence until you get this product into production. If you want to make changes in the existing board, you can rewire by eliminating the unwanted connections and then rewiring on the outside. It is a tricky process, but it can be done. It is not completely hopeless.

Q. (Fred Brammer, IBM, Kingston, New York) How would you eliminate those connections?

A. First you remove your module or component out of those holes. Then you drill out the plated through hole with a size larger drill than was originally used. Thus, you remove all the residual plating in the hole and then put an insulating sleeve into it and replace your module. The module pin will stick out on the other side and you can hand wire this isolated pin to other points. By this technique you might break a number of connections coming to the same hole, but usually, about 75% of the holes have only one connection to them, so that this case will not occur very often.

Q. (Tom Sawyer, General Dynamics, Pomona, California) Can you describe this wire-wrapped terminal that comes out of the printed circuit board? It does not appear to have the same dimensions as the other split pin wire wrap which I am used to seeing.

A. (Using the blackboard) In the shank of the hole there is actually a split eyelet which goes into the hole. A 0.025× 0.0125 in. tab protrudes out of the board for a half inch or so. The mating pin from the module comes through the hole and mates with the tab protruding from it. Now you interconnect them by the split-pin wire-up technique.

Robert J. Gerlach-The Role of Standards in Electronic Packaging

Q. (Fred Levy, RCA, Camden, New Jersey) You gave me a good lead with your remarks on international standards. What is your opinion about the metric system as possibly the most universally applied?

A. I am glad you said "your opinion," because that is exactly what it will be. It is a question that has been batted back and forth for many, many years. My opinion is that it is inevitable. Someday we will have the metric system. However, the question arises as to when. We, in England and the United States, are at a disadvantage. We are two of the few hold-outs in the world who are still using the inch system. We are at a particularly bad disadvantage in that not only do we have the inch system but we have the halfs, eighths, sixteenths, etc. A system which has been offered as an alternative to the metric system is the decimal inch system. You probably have heard of this. However, this seems to be a crutch rather than a true switch-over to a true international standard. Obviously there are many costs involved. For some of the larger firms to switch over would run anywhere from the millions into the billions. And this will not be done overnight.

Q. (Duard Woffinden, Utah State University, Logan, Utah) While we are getting opinions, don't you feel that government standards have gotten so far out of hand that we need some standards on standards to shrink them down so they can be understandable and useful?

A. That is an excellent question. Strangely enough, the popular opinion exists today that there is a central Standards Agency in the government which writes standards. In other words all we have to do to clean up MIL standards is to go to this agency and tell our ideas to them and they will clean up these standards and we will be all set. I posed the

very question which you asked to a fellow from the National Bureau of Standards and he said, "You know I have been wondering about that myself!" He said, "I have been looking for this agency which produces MIL standards and I have not been able to find it." Apparently the various services write their own standards. Ordnance writes its own, the Engineers write their own, the Signal Corps writes its own, the Navy writes its own, and so on. There is no central coordinating agency at this time. Perhaps sometime in the future we will have such an agency and then we will reach this ideal you are seeking.

Moderator – Jake Rubin: I would like to add one more comment on this. There is actually an additional agency which writes the standards for items common to two or more branches of the service and those standards cannot be written by the service that uses the item. That is the Defense Supply Agency in Dayton. They have their own share of headaches, too. We certainly have found that there is a combination of two effects in the standards business. One is that the government agencies each have their own standards which they want to control and write and second that they have a work load which is putting them in many cases one to two years behind the state of the art. This is a very severe problem.

Q. (Don Schnorr, RCA, Camden, New Jersey) Anyone who has ever been associated with standards feels a slight hesitancy on the part of the user groups to use these standards. I am talking about production and other people. What are your recommendations for making standards more palatable to the people who are actually using them, if you know what I mean?

A. Mr. Schnorr, you are a perfect straight man. I had rather hoped that someone would ask that question because we faced this problem some two years ago when we started building up the standards department that I am now in. The standards department had what we felt was a rather poor working relationship with the design projects and manufacturing and other people who they hoped would use their standards. As a result, they would maybe use them and maybe not. Since that time we have adopted the attitude that we are somewhat of a service group and we approach the design projects and we approach manufacturing to find out what their interests are and where they really need a standard. We then proceed to provide this. Now just recently, it was proposed that a management team consisting of the staff heads of manufacturing, engineering, and reliability get together and form a standards committee. This will be adopted and I think we will have even better results then because we will know exactly where the interest is and where the necessity is, and we will work accordingly.

Moderator – Jake Rubin: I would like to point out that regardless of your standardization from top management you still must get out and sell to the individual, who is going to specify something on a drawing, the use of standards. A product design area or a drafting room is the best place I have found to do this selling. The man on the board loves a standard whether he is a layout man, designer, detailer, or checker. That standard makes his job a lot easier and enables him to do his work well so this is a good starting point to get your standardization in product design.

Q. (Leo Grizel, Nortronics, Hawthorne, California) This is more of a specific question and more to the symposium than for Mr. Gerlach. In welding we have long been plagued by the question, what is the difference between a watt-second at the tips of the electrodes and that indicated by the watt-second meter. I don't know if there is a good answer for this or not but since watt-second seems to be the standard energy reference, is any work being done to relate it to the tip rather than to the meter?

Moderator –Jake Rubin: Any comments from the audience on that? I guess we put that down as a good question.

A. Actually, we can only say that there are many things in weights and measurements which remain to be standardized. The one you brought up is one, and various other measurements comprise a big field for company standards as well as industry standards.

Moderator – Jake Rubin: I might add that our previous speaker has introduced some new nomenclature that might be the basis for some new standardization. We now have mother boards, grandmother boards, great-grandmother boards and I guess we will have aunts and cousins soon.

Q. (Dick Yost, Univac, St. Paul, Minnesota) On this question of the welding, this particular problem plagues us as to what the watt-second reading might be at the electrodes. After giving some real thought to it, it really did not make too much difference as long as you had some indicator as the watt-second meter to get a repeat setting to give you the same results that you had obtained the first time. The strength of the welds is continually checked and by this we are able to repeat the reading. I sometimes think when we get down to the standards we are trying to get down too fine. As long as we have an indicator that we can set something by, it is sufficient for this particular case.

Moderator – Jake Rubin: There have been some items in literature on the relative standard or the pseudostandard which is very much in line with this. If you have some indication you may be all right.

Q. (Sam Francis, Sipicon Corporation, Marion, Massachusetts) It might interest some people to know that we do not actually use the watt-second in our shop. We use the voltage that is stored on the capacitors and then QC the whole thing. All our weld schedules are in volts.

Q. (Dean Joachim, Univac, St. Paul, Minnesota) At last year's Symposium some comments were made about the advantages of standardization in regard to component leads, as to their size and composition and shape. There were further comments made that something was being done to standardize this. Are you aware of anything about this and what is your opinion on this?

A. We have done quite a bit of work in attempting to get standardized leads on components. Actually, in answer to your question, it has not progressed nearly as far as we had hoped by this time. I know that on one program, the parts and materials standards people who work on this particular problem are attempting to get one or two leads of Dumet or nickel Kovar. The components, in general, are just not available.

Q. (Walter McDonald, Martin Company, Denver, Colorado) Regarding the watt-second output on weld techniques, we have developed at Martin-Denver a technique of measuring the thickness of the weld on the standard material. It has turned out to be quite accurate as far as determining the actual output or the energy at the weld tip.

Q. (Richard Yost, Univac, St. Paul, Minnesota) On the matter of the standardization of leads, we went through quite an extensive project in building several computers using welded construction and we were able to resolve the problem of the number of materials. We found in working with most of the vendors of the particular parts involved that they would give us the materials that we asked for in the lead materials. We were able to get down to using basically Dumet, Kovar, and nickel ribbon.

Q. Regarding the military standards, I have a suggestion and that is,as we mentioned before, there is quite a bit of duplication and on the other hand there is not enough coordination in military standards. I refer specifically to materials and other things. Maybe this could be coordinated if everyone of us would write his congressman so that he can take action in this respect.

A. If you have a company standards group may I suggest that you call on them, as that is one of the services they should provide for you. They should comb through all of these military standards that may be available on a given subject and perhaps write a digest for your use.

Q. Here is another technicality and that is management always has to back up this sort of thing and before it gets to management in many cases there is such a delay in paper work that the thing just runs out.

A. Of course there is nothing that puts steam behind a function like having management behind it. However, there is a lot of room for voluntary standards and for the voluntary use of them. Actually go out and sell your ideas. We have found that persons who have been spirited and somewhat independent are the very people who are now some of our staunchest allies.

R.W. Berry, E.H. Mayer, E.E. Muller, H.J. Scagnelli, and K.F. Stiefel-Thin-Film Logic Units

Q. (Carl Todd, Hughes Modular Circuits, Newport Beach, California) Did you experience difficulty in soldering to your gold film, in other words, absorbing the gold away from the tantalum?

A. Initially, we did experience gold brittlement. We solved this problem by solder-coating the leads on the transistor, thereby stripping the gold on the transistor leads prior to bonding them to the film surface.

Q. (Walter Prise, Lockheed, Mountain View, California) You mentioned reduction in weight and volume. Will you please indicate the reduction in your power consumption?

A. The logic diagram was initially designed and arranged so that the power was kept at a very low level, below three milliwatts per node. With this low power input it was not necessary to cool the modules. The temperature rise per module was ten degrees. You could hardly feel it with your hand. We have experienced no difficulty with thermal problems, principally because we did not put very much heat into the unit.

Q. (John McGuire, Huyck Systems Company, Huntington Station, New York) You indicated that you deposited approximately fifty resistors on one substrate to ±5%. I would like to know what your yield was. Secondly, I understand that this is a throwaway package, so what is the approximate price of this package after encapsulation?

A. We manufactured about two dozen slides on a prototype basis in the laboratory and we lost one or two. We turned this assignment over to our prototype line in Allentown, and on our first runs on a developmental basis we were getting about an 85% yield. This does not mean that we had to throw away the other 15%. They could be salvaged if necessary. On the question of cost, the reason for picking a two-bit module was to give ourselves a challenge for packaging. We could switch to a one-bit module and facilitate packaging at the sacrifice of number of interconnections. To go into production with this developmental transistor would cost no more than to go into production with any other good, reliable transistor. The units would probably cost several dollars apiece. There are, on an average, 16 to 17 transistors per slide, costing about $34.00. There are 8 slides per package and that amounts to approximately $280.00. The multilayer board would be around $10.00, and the slides themselves on a mechanized production basis would run about $2.00 a slide. So the modules would cost about $300.00 each if we were to package them in this size and in production quantities.

Q. (Bill Salsbury, McDonnell Aircraft, St. Louis, Missouri) In regard to your sputtered tantalum, what resistance per square are you using?

A. Forty ohms.

Q. Do you consider this an upper limit for tantalum?

A. No. One or two hundred ohms per square is an upper limit. We like to be conservative and stay on the low side.

Q. Are there any data available in regard to the wattage dissipation of tantalum at forty ohms per square, or at the higher levels?

A. "Electronics Magazine" in the February 1963 issue has a tabulation which compares tantalum films to a host of other films. I suggest that you be guided by the figure given in that article.

Q. (Ed Moore, Martin Company, Orlando, Florida) The use of nitrogen in lieu of flux for making the solder bond to the wire forms implies a reason for staying away from flux. Could you go into this as well as some test data that you might have to support it?

A. There is no reason for staying away from flux except that you would have a cleaning problem after you had made the bond to the slide. You can use flux if you find it more convenient. We did not want to face the cleaning problem, and we thought this was a simple way to get a good, reliable solder joint without the expense of cleaning.

Q. (Art Garret, Amphenol-Borg, Broadview, Illinois) Did you use a photo-resist mask or a metal mask?

A. We used both. The photo resist was used for the selective etching process to define the gold tantalum area, and the metal mask was used for the conductors on the back of the substrate.

Q. What variations did you experience with the resistors due to temperature? What is the TCR of the resistors?

A. Again I will refer you to the "Electronics Magazine" article, but I will quote from it. Negative 100 parts per million.

Q. (Ron Pitman, Sylvania Corporation, Mountain View, California) I have a question concerning the transistor which is mounted to the substrate and the method by which it is mounted. You are using a pressure-sensitive adhesive and I wonder what experience you have encountered with respect to temperature and vibration excursions?

A. The pressure-sensitive adhesive is applied between the transistor and the glass substrate. This mechanically holds the transistor in position while the leads are being bonded to the glass. There is also a conformal coating prior to encapsulation. Additional mechanical support is provided by the conformal coating and the encapsulating medium. I would say this about shock and vibration. Our encapsulating technique is not unique to this program. It has been employed in one of our most successful missile systems being used today, the Titan system. Since the Titan missile has performed so successfully in an airborne environment with severe shock and vibration effects, I don't think we will have a problem with this module, which is designed for a ground-based system.

Q. (Tom Briggs, Burroughs Corporation, Plainfield, New Jersey) On your chart of circuit topology, you show vertical and horizontal risers. Are these possible circuit paths on both faces of the substrate or just on one face, and do you cut these potential conductors by your masking?

A. Those paths are principally for the side we use. The back side is principally for the interconnecting conductors. We determine the paths by the pattern we cut on the coordinatograph. The risers are just possible avenues of intraconnection.

Q. (Jim Adams, ITT, Federal, Clifton, New Jersey) I am interested in the length of time it takes to make your infrared metal bond. Had inert hot gas been considered in making your bond?

A. We achieve them in 10 to 25 sec. We prefer to quote officially 25 sec, to be conservative. We have considered using hot inert gas, but this means that you have to move either the substrate past the spout or the spout past the substrate and it is a lot easier just to focus a quartz lamp with a thin line of infrared heat. So we use the latter technique.

Q. (J. P. Compton, Arizona State University, Tempe, Arizona) What kind of long-term stability do you get from your thin-film resistors?

A. Generally speaking 10 years and 2%. Incidentally, I might add that in this design we can get away with 5% initial life resistors because of the degree of stability. Normally, component parameters start with a 5% or a 2% resistor with a 10 or 15% end of life. In this particular design, because of its high stability, we can design for much wider tolerances of 8 or 10% and be sure that over a long period of time we will still have it.

Q. (Mohi Sobhani, Litton Industries, Woodland Hills, California) Could you explain more about the infrared technique and eliminating the flux? Do you have a unit for this infrared technique?

A. The infrared technique was developed by our manufacturing research people at Princeton, New Jersey, and basically it involved nothing more than a reflective lamp with a quartz source. The reflective lamp directs the energy to a pencil beam, which we direct onto the 29 or 30 contacts at the end of the substrate. We do this kind of bonding in a very short time. The reason for the nitrogen is to get rid of the oxide layer that normally forms on a solder coating. By getting rid of this oxide layer, or keeping the oxygen away from the solder, we find that we can cause two elements precoated with solder to fuse without flux. It is a matter of convenience.

Q. (Bob Burns, Signetics Corporation) Can you make more than one bond at the same time using the infrared technique? Will there be any papers published on this type of bond?

A. All bonds at the edge of any one substrate are made simultaneously within this time period. The pencil beam makes all of the connections on both the front and the rear of the substrate. The heat is intense enough to conduct through the wire forms onto the back of the substrate and make solder joints on both sides of the substrate. If we had sixty connections, it would make all sixty. As far as a paper is concerned, we are thinking of it. We haven't gotten around to it.

Q. (John Roderer, IBM, Kingston, New York) You have indicated here that in cutting masters on the coordinatograph you achieved a 1-mil tolerance. In your photographic reduction you come down to one tenth of this tolerance. Did you encounter any problems in holding this tolerance in photographic reduction?

A. Yes, normal problems that you encounter when you try to achieve these reduction. This was done on a spectrographic-type glass plate. We had to stay away from film. We had to go to a flat glass plate.

Q. What means did you use for measuring?

A. A toolmarker's microscope or a comparator such as those manufactured by our Japanese friends at Nikon.

D.J. Garibotti and W.V. Lane-The Enhanced Micromodule - A Disciplined Approach to Microcircuit Integration

Q. (Jim Bennett, Advanced Research Board, Ottawa, Canada) I notice from your notes that you do not encapsulate these in any form. What vibrations will they stand?

A. These packages have been subjected to thorough environmental testing. Specifically they have been subjected to thermal shock, thermal cycling, and vibration tests as per MIL-STD-202 Method 201A, and 204A. No degradation was observed after any of the above tests. The environmental exposure tests were carried out during the course of programs sponsored by a government agency. The tested modules were forwarded to the agency.

Q. (Leonard Yuska, United States Naval Avionics, Indianapolis, Indiana) Is this module aimed primarily at being a low-cost throwaway module?

A. The objective of this module is an interconnection-packaging system which is compatible with both thin-film and semiconductor circuits. The assembly cost itself is relatively low since standardization of the structure and consequently automated processes have been strived for. The cost of thin-film hybrid circuits is also fairly competitive at this time. However, the cost of the functional module which I have described, that is, the ten-stage binary divider, is quite high because of the inherent high cost of the semiconductor circuits at this time. When these circuits approach the projected cost of $3.00 to $5.00 per unit, then, of course, the Enhanced Micromodule will be a very good way to package these circuits into a relatively low-cost throwaway module with very high packaging densities.

Q. (Bill Salsbury, McDonnell Aircraft, St. Louis, Missouri) At what level are you making the vacuum deposition in the preparation of the wafers, and have you experienced any conductance problems, inductance problems, capacitance problems from the neat geometry of the riser wires when dealing with higher frequencies?

A. A standard vacuum system capable of 10^{-6} torr is used. Insofar as the other question is concerned, we have not assembled any functional devices in the extremely high-frequency range but we have built 5-Mc flip-flops without difficulty. We believe that the large number of conductor ribbons imparts considerable flexibility to the conductor location. Furthermore, when it comes to the integration and packaging of solid circuits, the limitations will not be the riser wire proximity, but rather the interelectrode capacitance which is inherent to these circuits.

Q. (John McGuire, Huyck Systems Co., Huntington Station, New York) My questions are related to the eutectic bonding of the silicon chip to the ceramic substrate. First of all, I notice that you had four chips bonded on one substrate and one plane. I would like an explanation of how you did that. Also, what is the conductive material that you bonded to, and thirdly what measures were taken to prevent the contamination of the uncased chip before the hermetic sealing of the unit was accomplished?

A. The bonding pads are gold on chromium. The thickness of the composite illustrated in the slides is 25,000 angstroms. In addition, we also use a preform which is gold doped with arsenic. All four semiconductor circuits (and we have attached more) are bonded simultaneously with standard die and thermal-compression bonding machines. The terminations around the edges of the microwafers are also vacuum-deposited gold on chromium followed by nickel plating. The semiconductor circuits are surface-passivated devices with the surface interconnection pattern already upon them. The latter is an aluminum photoetched pattern, which is deposited and defined by the supplier. As stated previously, all the assembly processes are carried out in a clean facility and prior to hermetic sealing the microwafer stack is vacuum-baked as per standard transistor technology.

Q. (Leo Fiderer, Hughes Aircraft Company, Culver City, California) Could you please elaborate on the method of interconnecting the ribbons on the edge of the wafer stacks and bonding them? You mentioned an automated welding machine. What kind of process has this established and how do you assure reliability between these ribbons and the edge of the wafer stack?

A. Typically, one weld is carried out as follows: The electron beam is positioned in the center of the edge of any one wafer. As you recall, there are nine terminations and nine ribbons on each edge. The electron beam is deflected, DC-wise, to coincide with the outermost intersection of copper ribbon and termination on the wafer edge. Then, an AC signal is superimposed on the beam to carry out the weld. Another DC deflection is subsequently applied to the beam so that it will impinge the next ribbon termination intersection, and the weld operation is repeated again. All the welds along one edge of

the wafer are accomplished in this fashion. The table is then stepped 25 mils and the same series of operations is repeated along the next row. The reliability of electron beam welds of this type has been demonstrated in a series of rigorous investigations. The results are detailed in the text.

Q. (Mark Hamilton, Electro Pack, Peterborough, New Hampshire) Are you promoting this as a standard packaging technique or is this a proprietary item of your own? If it is a standard technique, what does it cost to get into it?

A. For the most part the reported work has been and is being carried out in a series of contracts for the United States Army Signal Corps Agency, and as such it is not a proprietary technique. I would hesitate to guess how much it would cost to get into it right now since part of the equipment is of a custom nature and, consequently, cost figures are not available. Because of your particular needs, certain pieces of equipment may or may not be required. The representative from Hamilton Standard Electron Beam Systems attending this symposium, I am sure, will be able to answer your questions insofar as the cost of the electron beam machine itself is concerned.

Q. (Leo Grizel, Nortronics, Hawthorne, California) It did not show in the pictures, but do you use pressure fingers to hold the ribbons down to the wafer edges while you are making the welds?

A. Yes. In electron beam welding no pressure is required between the two parts to be joined; however, physical contact must be maintained. We have a fixture which comes all the way across one wafer to make contact between all the ribbons and all the terminations simultaneously. This approach makes it possible to obtain all the welds on one edge by deflection.

Q. (Bill Volk, Westinghouse Corp., Baltimore, Maryland) You indicated that you did not need multilayer circuits to interconnect your modules. You have twenty leads coming out in a half-inch square. How do you do it?

A. Actually the pins are on 75 mil centers. I said the need for multilayer boards is considerably lessened since most of the complex interconnections are achieved within the modules rather than outside on several multilayer boards. A reduced number of multilayer boards is required to interconnect the modules.

Q. If you had twenty leads as outputs, they would have to be interconnected at the bottom of the module and the header. It is not going to simplify the interconnections, especially on 75 mil centers. You still have the same basic problem as we have with any small system, that is, taking the guts and interconnecting them.

A. This will depend upon the specific system you have. We have designed some subsystems using this particular approach and we find that we have considerably reduced the number of six, seven, and eight layer multilayer boards since a considerable amount of interconnection is achieved within the modules.

Q. (Tom Briggs, Burroughs Components, Plainfield, New Jersey) You are, I believe, evaporating or sputtering the edge connections onto the edge of the substrate. Do you have any problems of fracturing or discontinuities between the conductors on the edge of the substrate and those on the surface of the substrate?

A. No, no such problem has been encountered. As I said, the edge terminations actually envelop the two surfaces around the edge. This is formed simultaneously by vacuum deposition followed by electroplating. Furthermore, the edge of each discrete termination is tapered on the wafer surface to obviate a steep gradient between the thin film and the edge terminations.

Q. Then you do chamfer the edge of the ceramic.

A. No, the edge of the ceramic is relatively square; i.e., the corners of the wafer edge are not broken in a separate operation. The thin film which goes around the two surfaces and over to the edge is deposited from two sources which are at an angle so as to give a slight gradient on the two surfaces of the wafer.

H.G. Stech-Packaging a Thin-Film High-Speed Counter

Q. (John McGuire, Huyck System Co., Huntington Station, New York) The configuration of your finished package seems to have the weakest axis, or the moment of inertia is least, in the plane of the weakest axis of your glass substrate. Have you vibration-tested this unit? What were the results?

A. I agree with your statement. We have vibration-tested dummy units. We have not tested the real functioning unit. We tested at 45 g's, ten to two thousand cycles, and had no problems.

Q. (Max Callen, Minneapolis Honeywell, Minneapolis, Minnesota) It appears that you slide the pages in so that each contact contacts the next connector. In other words, you do not slide it into the connector in the conventional manner, but you have to cross each connector as you push it in. Does this present a problem with the small spring wires?

A. We did not think we would have a problem with the spring wires but we thought we would have a problem with the gold pads rubbing off. So we did two things. We beveled the entering edge of the glass substrate and we also put an overcoat of chrome on top of the gold pads. This seems to be a satisfactory situation.

Q. Could you tell me what your substrate materials were and what types of depositive components you were using?

A. Our substrate materials were glass and in some instances quartz. The resistors were nichrome deposited at 500 ohms per square and the conductors were gold. The capacitors were aluminum silicon monoxide and aluminum.

Q. (Pete Gerlach, Automatic Electric Labs, Northlake, Illinois) Was your choice to build your own connector based on a peculiar geometry of your wafer rather than the lack of the availability of a commercial unit?

A. I would say it was based on the need to make a package flat configuration. We wanted to insert the substrate parallel to the package and we couldn't find a connector that we could get down into the board in a short distance so we made our own.

Q. (Dick Kirn, EMR, Sarasota, Florida) Did you use straight filament evaporation or electron beam apparatus for evaporation?

A. We used both. We used electron beam normally on everything except silicon monoxide evaporation.

Glen R. Madland-A New Flat Package for Monolithic Integrated Circuits

Q. (Leonard Yuska, United States Naval Avionics, Indianapolis, Indiana) Was this speech recorded? The text of your speech was very good and I wondered if we could get a copy of it. We give you an "A" for the speech and an "A" for the paper.

A. I am sorry, the speech was not recorded.

Q. (W. Roberson, Martin Company, Denver, Colorado) Did you have trouble in registering the finger tabs to the land pads on your chips and were the aluminum leads nail-head bonded and how were the finger type bonds made?

A. The larger chip is 100 by 100 mils, and the land pads are 10 by 10 mils. There was absolutely no difficulty in this registration. In further designs we intend to use the clip on the 50-mil chip. We do anticipate considerable problems in this area. I believe we have been able to hold a clip tolerance of about 1 mil and I think we will be able to hold an alignment tolerance of about 1 mil. The second part of the question: aluminum as far as I know cannot be nail-head bonded. These leads then are thermal-compression bonded in the case of the wiring. The third part was what the method of attaching the fingers or the heavy straps to the silicon die. This was done by ultrasonic welding. Remember that there is aluminum on the tips of the fingers and aluminum on the circuit so we were taking aluminum to aluminum in the ultrasonic weld.

Q. (Maurice Dumesnil, Fairchild Semiconductor, Palo Alto, California) How do you check for the hermeticity of your package?

A. The hermeticity of the package is tested with the helium bomb technique, with which I think most of us are familiar, as well as the dye penetration test for gross leaks. Most of you know the helium test will miss a big hole. You have to have a supplementary technique. The hermaticity of the package has been very good.

Q. Does this mean that you are sealing under a helium atmosphere?

A. No, although we do this in engineering for sample runs. In this case the method of test is that the units are placed in a bomb, and helium is put in under pressure. If you have a small hole, the helium goes in gradually and then you remove the units out and get rid of the helium that is in the air. You then pull in a vacuum and try to suck out the helium through the hole through a dector. I think some of you know much more about this than I do.

Q. I have one more question. How did you place the aluminum coating on the Kovar fingers?

A. If you looked at the slide carefully you would have detected that there is also aluminum at the edge of the frame. The aluminum is rolled in the Kovar and if you put it in the right place when you are all done rolling and you stamp it it comes out automatically.

Q. (Bob Burns, Signetics Corporation) I would like to know if you used the pyroceram in the vitreous or the devitrified state?

A. It is used in the devitrified state.

Q. (Fred Levy, RCA, Camden, New Jersey) You have shown a preformed glass seal in the melted state. This is a two-part question: what is the dimension of this glass and what do you consider the minimum for good mechanical reliability?

A. If I understand you correctly, you mean the length of glass along the lead?

Q. No, not the length – the thickness or the width – that portion of the glass that will achieve a seal over the leads.

A. We like to see as much as possible and we have gotten hermeticity in the 20 to 40 mil range. This is an application and you can put it on as thick as you want. I do not know what the minimum is.

Q. (Leo Fiderer, Hughes Aircraft Company, Culver City, California) The shape and form factor is quite similar to some of the integrated circuits manufactured by Texas Instruments, sometimes affectionately called TI bugs. Can you elaborate on the significant differences between this type of integrated circuit and the TI bug?

A. Texas Instruments uses a ceramic substrate, high-temperature glass sealing, and the lid is either solder-welded or stitch-welded. That is to say, it has a metal top and a ceramic bottom somewhat similar to ours. The Texas Instrument circuit uses gold wire.

I think we gave you the reason why we do not like this and we feel that it has two difficulties. One is that the creepage path is less. You have a metal lid and you have inferior creepage paths. We also feel that the hermeticity of the methods which are used to seal that package are open to question.

Q. (Bob Phillips, Martin Company, Orlando, Florida) One problem for the user is getting more than one source on a particular configuration. Now that you have introduced essentially a third configuration, what are you people doing as vendors to standardize to help us?

A. We are standardized with one other vendor who is present. This was done deliberately so you would have two sources for circuits.

Q. (Bob Morrison, Martin Company, Orlando, Florida) In presenting this newly packaged module, when can you come along with reliability figures? This is most important.

A. The reliability figures on the flat package are unfortunately not available. This is a reasonably recent development and has been in production a short while, so we will have several months to go before we will have the full story. Of course, the TO-5 has a tremendous history and all sorts of data.

Q. (William Hall, Temco Electronics, Dallas, Texas) Am I right to assume that you are bonding the circuit, the base, the lead frame, and the cover in one step as one hermetic seal or is it a two-step procedure?

A. It is ordinarily a two-step procedure.

Q. Do you have any problem with the fit being rough and do you go through any mechanical machining to make a good surface to bond the cover on?

A. No. We have had no difficulty with the circuits of ceramic.

Q. Is there any government spec which states what is a hermetic seal and what is not a hermetic seal?

A. I have no knowledge of this. We use the sensitivity of the helium leak detector, which as I remember is about 10^9 cc/min.

Milton I. Ross-Encapsulation of Electrical Components by Transfer Molding vs. Precision-Formed Encapsulation Shells

Q. (Phil Ladoulis, Raytheon Company, Wayland, Massachusetts) You mentioned that one of the processes was to put a premeasured amount of epoxy or plastic in a shell and then put the module on top of the premeasured amount and let it settle by changing the viscosity of the fluid with heat. You also mentioned that you increased the viscosity with heat. Is this incorrect?

A. That is incorrect. The material with heat becomes more fluid and the paper did state that. I said it became more viscous. I apologize.

Q. (Adolph F. Avondo, United Control Corp., Redmond, Washington) Do you build heaters into the mold?

A. Yes. We have special heat sticks of 1000 W 5/8 in. in diameter and about 8 in. long. They are built right into the mold as close to the cavities as possible. We use ± 1 deg, or closer if we can, for temperature control.

Q. Are your machine platens heated?

A. No, the platens on the machine are not heated. We use asbestos insulation in between the mold and the platens of the machine.

Q. (Earl Clemick, Centralab, Inc., Milwaukee, Wisconsin) If you take multiple lead devices with spacing of approximately 0.125 with 22-gage wires, package size of about 3/4 by 3/8 by 3/16 and a 40- or 80-cavity transfer mold die vs. your method of shells, then what do you think the practicality is of transfer-molding a device like this? The multiple-lead device is a substrate approximately 30/1000 thick.

A. The multilead device – are all of the leads on the same center line facing the same direction?

Q. And on the same plane, yes.

A. Then I would say you absolutely can mold it by transfer molding. You could use either method.

Q. If you did that, would you normally gate as you have illustrated and have the epoxy come in from the top or would you do it from the side? Is there any real feeling for this?

A. We still prefer what we call three-plate molding. We have found it most successful for all types of molding. It will require less pressure; it will be more uniform and, we feel, result in a superior product.

Q. As far as cost is concerned, what kind of savings would you have on transfer molding over a shell in volume of 500 thousand pieces per month? Would there be a decided difference in cost, say of 30%?

A. We supply some companies 100 to 200 thousand shells a week and they are very happy. Yet some of these same companies have decided to go into transfer moldings. It depends upon your product and what is best suited for you. It is a question which I feel does not have an answer because some people feel the quality is superior. You can use both methods and you can get very high production rates with both techniques.

Q. (George Gless, University of Colorado, Boulder, Colorado) Will the encapsulation of that capacitor be successful with the two holes rather than one? Has this been proved in practice?

A. The company that showed this technique is the Stokes Company, and I cannot disclose the manufacturer who uses it. But, as molders, we do suggest balanced molding. There are a few other companies that have recently put in transfer-molding equipment for capacitor manufacturing. I do not know what their techniques are.

Q. (Martin Camen, Bendix Corporation, Teterboro, New Jersey) Have you done or do you know anyone who is doing transfer molding using highly filled plastic systems as opposed to pure resin systems?

A. I do not believe anyone uses pure resin without fillers. To my knowledge there are five major epoxy resin manufacturers. You have Hysol, Mesa, Fiberite, Plenco, and Furane, all manufacturing excellent materials with high fillers. And I know that they have both glass- and asbestos-filled materials available. We have also molded with filled silicone and we find that it is a terrific material.

Q. Do you know of anybody specifically who has worked with Eccospheres as a filler in the transfer-molding process?

A. No, I do not.

E.B. Smith-Design for Space Applications

Q. (Joe Riddle, Librascope, San Marcos, California) You have mentioned the use of eight tooling holes in a circuit board. Is this correct?

A. No. Photographic silk screen techniques allow for fabrication of eight multilayer boards from one large laminated sheet. Two locating holes are drilled for each of the multilayer boards. The drill fixture for the plated through holes is located in accordance with the two locating holes. That allows you to drill just one multilayer board at a time.

Q. There are eight circuit boards on one large board?

A. Yes, your platen press can take an aluminum plate of 16 by 12 and the eight small multilayer boards.

Q. (Bob Bender, Hughes Aircraft Company, Newport Beach, California) I would be interested to know the effect on the adherence or the peel strength of the copper after flame spraying of the alumina powder.

A. We did not run into trouble when it came to thermal spraying the aluminum oxide on top of the copper. Adhesion is a problem in the initial process of depositing the copper on the substrate. That is why I pointed out that it is important that you use a degreasing agent to keep the substrate as clean as possible in order to get good adhesion.

Q. (Mark Hurowitz, Sylvania, Mountain View, California) In the photomicrograph of your multilayer board I noticed you had large discontinuities between the copper and the interface.

A. That was cuposit, I believe. There was a cuposit or electroless deposition of copper to provide continuity between the cross section of the land and the electroplated copper.

Q. A cuposit, did you say?

A. It is an electroless deposition of copper.

Q. It is an electroless copper that you use prior to the process?

A. Yes.

Q. (Joe Mecholl, Philco Corporation, Palo Alto, California) I noticed in the photograph of your boards you had the leads going across the edge of the board at somewhat of an angle. Do you use a special mask for this?

A. We use a stainless steel screen mask. We use a screen mask also to place the Dupont photoresist on the edge in addition to the front and sides. You actually have four squeegee operations if you want conductors on both the top and the bottom edge in addition to the front and rear surfaces of the substrate.

Q. This is a squeegee?

A. That is right. It is a laboratory squeegee application. There is no problem on control of thickness for conductors as you would have when dealing with resistors.

Q. (Al Abel, McDonnell Aircraft Company, St. Louis, Missouri) You stated, in testing your multilayer boards you dipped them in a dip-solder tank, I think at 500 F. The time that you dipped these is an extremely significant factor. I am curious as to how long you keep them in.

A. We kept them in for as long as you normally dip-solder boards – four or five seconds. We had problems with some of the adhesives and lamination. When we evaluate a new adhesive, one of the first things we do is to see what happens during dip-soldering.

Q. (Pete Gerlach, Automatic Electric Labs, Northlake, Illinois) Why did you go to such trouble to produce an alumina substrate rather than a more conventional material such as G-10?

A. This is a development for aerospace applications and we considered heat transfer as a design factor. Alumina has a thermal conductivity in the neighborhood of 19, which is much higher than G-10. The idea would be to heat-sink the various modules, once they have been encapsulated, to a metal enclosure. That is if we can get good heat transfer characteristics from the alumina substrate to an aluminum or sheet metal enclosure. You could use G-10 if heat transfer is not a problem.

Q. (Bill Emmons, McDonnell Aircraft Company, St. Louis, Missouri) What was the adhesive you used in the fabrication of the multilayer board and also what is the role of Teflon?

A. Teflon is used to prevent the adhesive from flowing onto the aluminum pressure plates.

Q. (Doug Grantham, Bristol Company, Waterbury, Connecticut) Do you advocate the exclusive use in multilayer boards of plated through holes or do you feel that in your circumstances this was better than another method of making contacts, or is there any other method?

A. Yes, there are other methods. There is a clearance hole approach and an explosive rivet approach. We used the plated through hole technique at Martin. The capital equipment that is required to make multilayer boards of this nature is basically the same equipment that is required in any photoresist laboratory for making one- and two-sided boards.

Q. My question was, do you think that the plated through hole is best for the application you illustrated?

A. I favor plated through holes.

Q. (Don Schnorr, RCA, Camden, New Jersey) You mentioned that you had trouble with your clearance hole method with the adhesive flowing into the hole. Have you tried precuring the adhesive immediately adjacent to the hole, and what is your recommendation for preventing this?

A. The material we have been working with lately, and we are not too sure of its success, is manufactured by Circuit Materials Corporation and is called CMC-10. It used to be known as X-152. We selected a thin adhesive, about 1.8 mils, which they claimed was partially cured to reduce the flow of the adhesive. We used silicon rubber pads. We tried to force the silicon rubber pads down into this cross section, in addition to having an adhesive that was partially cured. We thought this would retain the flow of glue out onto the smaller hole. You cannot have glue in the hole because you are going to require subsequent plating. This is a problem and if you are going to consider a method using the clearance hole approach, you have to contain this glue. The reason for going to a clearance hole approach is to get a larger cross-sectional area between the plated copper and the land pattern.

Bob G. Bender and Roy W. Dreyer-Recent Developments in Swiss Cheese Microcircuitry

Q. (Jim Bennet, Defense Research Tele-Communications, Ottawa, Ontario) How do you prevent the copper from going down between the walls of the substrate and the component?

A. We use a Selectron resin, made by Pittsburgh Plate Glass Company, as a glue to hold the devices in their sites. Our practice for a small module is to brush the resin onto both sides of the board so as to accumulate the resin in the holes. The excess is wiped from the surface. The devices are loaded into holes partially filled by the resin while the substrate is laying flat on a Teflon block. A certain amount of fluid back pressure thus created causes very tight filling of the cavity between the device and the walls as the resin flows to get out of the way of the entering device. Again excess resin is removed and the

resin is cured. A very light sandblast is used to remove any resin which remains on the metal contacts. This is probably the most laborious process and is the principal target for our present development efforts. We want to find better means for fixing the devices in their sites.

Q. (Ralph Taynton, RCA, Morristown, New Jersey) What is the availability of components in the pelletized form? How many different types of components are available and how does their price picture look at the present as well as in the future?

A. The principal drawback to the pellet approach at this time is the pricing and availability of components and also the lack of breadth in the availability of components. Resistors, for example, are available up to a quarter watt from four different companies and in values of 10 to 500,000 ohms. I am not aware of units that go beyond a half Meg or beyond a quarter watt. Capacitors are limited at this time from 5 pF to 20 μF-V. Hughes makes the Microseal diodes and transistors and we have been a lot slower in getting these to the market than we felt it would require. At present we are manufacturing both pnp and npn transistors of the small signal variety. An example would be the 2N869 of a pnp and the 2N706 family as an example of the npn series. These are presently available in small quantities. They are not available in quantities larger than a thousand pieces on short notice. The diodes we are currently making are Zeners, general purpose and planar-diffused epitaxial fast-switching diodes.

Q. (Bill Salsbury, McDonnell Aircraft Co., St. Louis, Missouri) Have you found the military receptive to Swiss Cheese, and are there any reliability data specifically on the type of repairs you outlined?

A. There have been a few raids on the military in an attempt to get some support funding. I am not aware of a successful effort. Computer Controls is building a portion of Mariner II using pellet diodes and pellet resistors. I am not prepared at this moment to state what their inner wiring technique is. Apparently, there has been some approval by at least one portion of the military for a vehicle to be built by this technique. I have forgotten your second question.

Q. On the repairs.

A. No, I do not have data on the repair connections.

Q. How do you bridge the gap between the clad copper and the device electrodes when making plated wiring?

A. The surface across which we plate constitutes the surface of the component, the surface of the resin, and finally the surface of the clad board. The surface, while it may not be level, is not discontinuous. It is continuous surface albeit it may be a raised area or for that matter a trough between the device and the walls of the holes. The use of the plated process permits us to follow exactly the contour of the substrate.

Q. (John Jones, Texas Instruments, Dallas, Texas) In your assembly it appears that you make interconnection off the surface of the pellet. Does this mean then that you have only two surfaces you can tie to and what about the multiconductor type components?

A. Our transistor has two conductors on one face and one on the other. So we will treat the collector connection essentially as if it were a diode or a resistor. The opposite surface, which contains both the base and the emitter, is plated across solidly as is the rest of the board. In the process of photoresist masking and etching, or screen printing and etching, we simply remove the plated copper from between the emitter and the base electrodes and accomplish electrical isolation again.

Q. That brings up another question. The keying of those components is very important. How do you accomplish that?

A. The orientation of a multilead device is accomplished by a red dot on the emitter, very much like the TI diode.

Q. (Don Berry, Boeing Company, Seattle, Washington) Would you care to comment on any possible chemical contamination of the board materials or entrapment around the particular components?

A. You are probably concerned about the palladium chloride and the stannous chloride penetrating around the devices. It has been our experience that the electroless copper plating has a faculty for depositing on the furthest reaches to which the solution is able to achieve. Therefore, if faults or crevices exist in the substrate, a device will either be shorted in the first process (and this will be apparent in the checkout of the circuit) or it will be acceptable thereafter. Further, the chemical resistivity of the board material is excellent and the devices hermetic. Thus, our rinsing and cleaning processes which follow plating are consistently able to provide contaminant-free surfaces. Some measure of the effectiveness of our ability to clean may be seen in our final rinse water which measures 5 Megohms.

Q. (Jake Rubin, ACF Electronics, Randallstown, Maryland) You mentioned the time-consuming activity of getting the adhesive between the Swiss Cheese board and the component. Have you gone into any technique for applying a premixed epoxy as an insert in the hole or around the component? And then insertion mechanically followed by a heating cure?

A. We haven't attempted any such process, although I have reason to believe it would not be successful.

Q. Does flexing of the board cause any trouble?

A. This is an area that we have not studied. I am sorry I cannot answer your question.

Q. (Mark Hamilton, Electropac, Inc.,[subsidiary of the Computer Control Company] Peterborough, New Hampshire) We are using this process, as you said, in the Mariner data processer and we have switched from the plating technique to a vacuum-metallizing technique for making the circuitry with very good results.

Q. (Bill Pinter, Temco Aero Systems, Dallas, Texas) We went to ribbon-attached devices for breadboard evaluation and later went to the plating process. This gave us a compatible test of what the circuits will do under actual usage.

Q. (Jack Bingham, Bendix Systems, Ann Arbor, Michigan) I want to ask one question of the man from Computer Control. Do you use printed-circuit type boards or do you use epoxy and pot your pellets together?

A. We precast the pellets in an epoxy substrate. They are put in between layers of a mold with resilient surfaces and epoxy is flowed in around them. In this way we are very sure there are no possibilities of shorts between the two layers.

Q. (Joe Kruzich, Bendix Systems, Ann Arbor, Michigan) About the difficulty of getting adhesion between the pellets and the board, have you investigated the use of anaerobic adhesives such as Lock-tite with which you might pretreat the pellet and then insert it in the boards?

A. No. I have not heard of this and I would be interested in talking to you about it later if you do not mind giving me the information.

H.F. Sawyer-3-D Welded Module Design and Manufacturing Control Parameters

Q. (Martin Camen, Bendix Corporation, Teterboro, New Jersey) I noticed on your curves you made reference to various vendors. I therefore assume that your weld schedules are made on component vendor lead material. Did you consider where along the component lead, relative to the component body, you made your weld schedule?

A. Yes. We have detected that there is variation along the lead. Therefore, all the weld schedules were made by purposely and randomly mixing the position along the lead.

Q. (Jim Bennett, Defense Research Board, Ottawa, Canada) You state you crimp the lead and also add a Dow-Corning chemical, for stress relief. We have found that type of crimp in this type of lead to be virtually useless. Do you have any tests to substantiate your statement?

A. The test program on the SD-4 module on soldering did result in a relief from the broken solder joints. We did not do this job. This was done prior to the time that we did the welding research. They did incorporate other things at that time so it is not certain that the crimps did relieve the problem. However, we went through two tooling stages in order to obtain the design crimp that is there. We are not happy with the second design or the first one.

Q. (Dick Kirn, FMR, Sarasota, Florida) Did you run any evaluation on pull rate on small-diameter five- or ten-mil material?

A. We ran only the pull rate evaluation on 0.025-diameter copper.

Q. Just as a matter of interest, we have recently run some as small as five mils and we still get a straight-line function. However, we get a much greater change as the size goes down, which I think you would expect.

A. This is entirely possible. The point I was trying to make is that whatever rate you choose you must maintain consistency. You cannot mix rates unless you are asking for trouble.

Q. (Bill Salsbury, McDonnell Aircraft, St. Louis, Missouri) I find your rapid pull testing experiments very interesting. I am curious as to whether or not your mode of failure was consistent throughout the range and what particular speed you have chosen to standardize on?

A. We have always used and did use in this testing 60 in./min as the standard speed. The mode of failure has been more or less randomly dispersed on the three described places of break (that is, on the lead itself, in the heat-affected zone, and at the weld).

Q. I notice you have a table of the weldability of materials and in both cases you indicate copper being ahead of Dumet and that this is because of some failures where you did not get a satisfactory Dumet weld. Now, isn't it true that in general practice the Dumet has much better weldability than copper?

A. The table which you read in the paper takes into account all the factors which result in joint strength. This includes size. Therefore, any material which will consistently and reliably weld at the minimum strengths, which were established at the number given (782 for the three in a thousand probability), will form itself in a table where it outranks some other material which may have better welding properties but which is lower in minimum strength. Does that answer your question?

Q. What I was really thinking was that the low weld strength which you observed on the Dumet was due to faulty welds and they were included in your analysis rather than in the analysis of the good-quality welds.

A. All the materials were on a more or less equitable basis of comparison, but the 0.025 copper rated this 0.020 Dumet in that table. The one that was higher was 0.032 copper, and it necessarily has to be higher or we cannot use it.

F.R. Schollhammer-The Encapsulation of Electronic Components by Electron Beam Welding

Q. What capital expenditures are involved in setting up for electron beam welding from scratch? What is the delivery time?

A. The machine I showed you this morning is a machine that has a capability of not only welding all the illustrations you saw, but it also has a capability of welding materials such as stainless steels up to one inch thick. A comparable machine, designated as a Wl-3, sells for approximately $68,000.00. The machine which Dr. Garibotti used for his enhanced micromodule approach is of a more sophisticated design. His machine has the capability of welding micro components up to 0.030 in. thick with a beam diameter as small as 1 mil. The same beam can be used for vaporizing or scribing thin films. Since this machine is more of a specialized unit, the machine cost is consequently greater. The individual application determines the type of machine and, consequently, the price. As far as the availability, I would say three months.

Q. (Bill Salsbury, McDonnell Aircraft Company, St. Louis, Missouri) You indicated that the package had been sealed by a pulse beam and that it could have been sealed by a continuous beam. How does one normally decide which of the two to use and what are the advantages of the applications of each?

A. A pulse beam is used primarily when one has to take extreme care in minimizing the heat input into the module or circuit that requires welding. When the beam is pulsed, the beam is normally on from 0.5 to 10 msec, depending upon the selection of the pulse duration. If the special welder-cutter machine is used, the beam pulse durations are limited to 2.5 to 80 μsec. The beam is actually off at least ten times the amount that it is on. For the majority of the cases illustrated, the beam was off at least a hundred times longer than it was on. This gives the process a change to dissipate the heat from one pulse to the next. I would say that for the larger relays and canisters, it would be more advantageous to use the continuous beam because it is slightly faster relative to welding speed. With a continuous beam, a welding rate of 60 to 100 in./min can be achieved. To make sure a hermetic seal is obtained with a pulsing beam, the pulses must be overlapped. The welding speed is thus limited to perhaps 15 in./min.

Q. (Don Schnorr, RCA, Camden, New Jersey) Continuous and pulse beam laser techniques are beginning to attract some attention in regard to microminiature welding. This is a relatively new technology. Do you think this might replace the more complicated electron beam welding techniques as the state of the art improves?

A. One of my other assignments at Hamilton is investigating the welding capabilities of a laser device. You must remember that continuous mode laser devices today will deliver output power of only a few milliwatts. To accomplish welds such as those illustrated today, a laser output of five watts would be required. To obtain this output on a continuous basis is going to take quite some time. Hamilton Standard is presently investigating laser welding with a device that will pulse a laser beam once per second or perhaps a little faster. Now you can see that at one pulse per second, a weld five inches in length or even one inch in length will take a long time to complete, particularly since the spots must be overlapped to guarantee hermeticity. There is a lot to learn about the metallurgical characteristics of a laser weld. It appears to be different than that of an electron beam weld.

Q. (Max Callen, Minneapolis-Honeywell, Minneapolis, Minnesota) Can you tell me the time required to pump down the chamber on these two welding machines?

A. For the majority of the machines you saw, the pump-down time is approximately ten to twelve minutes. If you are welding 200 to 300 relays, this is not too significant. However, there are machines that pump down in two or three minutes. This depends upon how much vacuum equipment you want to couple to the vacuum chamber.

Q. (Howard Zimmerman, United States Naval Ordnance Laboratory, Corona, California) The electron beam, because of its concentrated area of heat, apparently has a considerable advantage over the dip-brazing of fabricating small microwave RF heads. How would you propose to handle shadowed areas in a complex structure?

A. You would have to rotate or move the pieces in a vacuum. I did not mention this, but the electron beam can be focused to within a half inch from the top of the chamber and also down to a position fifteen inches inside the chamber. If one tries to operate in a shadowed area, this focusing capability will not work. The workpiece will have to be rotated beneath the beam so that a line of sight type of operation is achieved. There is some capability of deflecting the beam but this is limited to an angle of approximately five degrees.

Q. (Jake Rubin, ACF Electronics, Randallstown, Maryland) In vacuum deposition, a metal target is irradiated or heated and particles are driven off. Do you anticipate, or have you found, any difficulty in some of the delicate welds on microcomponents in a vacuum chamber becoming irradiated targets and giving metal off to the sides of the chamber?

A. What you describe will only happen when welding real heavy pieces, such as 1/2- to 1-in.-thick sections.

M.M. Fulk and K.S. Horr-Sublimation of Materials Problem in Electronic Packaging for Spacecraft

Q. (Jake Rubin, ACF Electronics, Randallstown, Maryland) Could you take a typical example of something we would normally work with, for instance a printed circuit board with etched copper laminate dip soldered – what are the general problems of tin sublimation and whisker growth you would anticipate in that design?

A. As electronic packages get smaller the conductors get closer together and in general the power levels get lower. Power levels are low enough now in certain packages for some metal whiskers to cause trouble. Metal oxide and sulfide whiskers could possibly modify signals through their semiconductor properties. The sublimation rates of metals can be estimated fairly acccurately by using the Knudsen-Langmuir equation and plugging in vapor pressure data given by Honig shown in Figs. 2, 3, and 4. One should remember that the "oxide skin" of some metals may impede the evaporation of the base metal. Tin-lead solders on copper seldom if ever grow whiskers – this is especially true if the solder coat is thick.

Q. (Joe Mecholl, Philco Corporation, Palo Alto, California) Do you have any feeling for the dimensions of these whiskers as they are grown on more common materials?

A. Metal whiskers vary in diameter, length, and rate of growth. Tin whiskers range from 1μ to many microns in diameter and grow as long as 200μ. Their rate of growth is about 0.01 to 0.1 Å/sec. Again, the growth rate of tin whiskers on electroplated steel under a compressive stress of 7500 psi can be as great as 5000 to 10,000 Å/sec. Tin whiskers will grow at -40°C with optimum growth rates at about 50°C – 125°C will stop the growth. The parameters that influence whisker growth vary with the metal – I used tin only as an example. The literature should be checked for the factors that influence any given metal.

Q. (Carl Todd, Hughes Aircraft, Newport Beach, California) You mentioned that you could not repress the growth of the whiskers even by a thin coating of paint. What about a hard conformal coating of some epoxy material?

A. A thick conformal coat of a "hard" epoxy material might slow down whisker growth. Under favorable conditions, I would guess that some whisker growth might penetrate a thin coat of a "soft" epoxy. Coats of oil, lacquer, Chromicoat, etc. do not stop whisker growth. (See Bell Telephone Systems Monograph 2635 by S. M. Arnold.)

Q. (John Roderer, IBM, Kingston, New York) You said these whiskers would grow under stresses. Were you discussing mechanical stresses, and are there any other stresses which will accelerate their growth?

A. The energy for whisker growth probably arises from the relief of strain energy and/or from external stress. These external stresses may originate from hydrostatic, vibrational, compressive, lattice misfit, temperature changes of plated materials on a dissimilar substrate, and anisotropic expansion of the noncubic polycrystalline metals, such as tin, cadmium, and zinc; there are probably more, this is all I can think of at the moment.

Q. (Bill McMorran, Raytheon Company, Sudbury, Massachusetts) One of the problems in trying to find information on this subject is that a lot are compilations of other people's compilations. It is very hard to get good facts. Do you have references or other authorities that you could recommend for persons looking for hard facts?

A. The best single book on whiskers that I can recall now is "Growth and Perfection of Crystals", edited by R. H. Doremus, et al., John Wiley, New York 1958. The Bell Telephone people have done a great deal of excellent work in this field and they have published a Bell Telephone System Monograph (2635), by S. M. Arnold (1956) on whiskers.

Q. (R. A. Morrison, Walter V. Sterling, Inc., Claremont, California) In the sublimation of some of these metals, have you run into any problems of redeposition on other materials surrounding these sublimating materials?

A. In our spacecraft and equipment, we avoid high-vapor-pressure metals that might cause trouble. There is the possibility of some of the more volatile metals, such as cadmium, evaporating and wandering around the spacecraft to condense out and plate optics with an opaque film of metal or to "short" out electronic gear with an electrically conducting film if the temperatures of the dielectric surfaces are low enough and the current density of the cadmium vapor high enough. Actually, the vapor of cadmium is about 10^{-10} mm Hg at room temperature and the heat of adsorption of cadmium on dielectrics is about one-fifth that for its own bulk metal. This indicates that the cadmium vapor would wander around without sticking long enough to condense into a film as long as the temperature of the dielectric surface is greater than about 200°K. This temperature increases if the current density of bombarding cadmium atoms increases. One has to be careful even if the above conditions indicate no film will form because the history of a surface is important also. For instance, glass will allow a film of cadmium to form at room temperatures if it has been previously cooled below 200°K in the presence of cadmium vapor. Deposition of cadmium on metals will be different from that of dielectrics. Each metal and surface should be considered separately.

Q. (Howard Zimmerman, Naval Ordnance Laboratory, Corona, California) Has anyone compiled a list of particular platings to be avoided on base materials to prevent the growth of whiskers? I ask you this because without revealing any manufacturers we obtained some switch contacts which are basically brass with silver plating. They apparently grew a black oxide hair at about twenty-five thousandths of an inch per week. You can knock this off until you are clear down to the brass and it still continues to grow.

A. The best compilation of information that I know about on whiskers in general will be found in the two references I gave to Mr. McMorran of Raytheon. Without seeing your switch contact, I would guess that the whisker was silver sulfide. Metal whiskers are most commonly grown from the solid on tin, zinc, cadmium, antimony, and their alloys at room temperature. Lead and indium don't seem to grow whiskers readily.

C.S. Lankton-Thermal Characteristics of Electronic Module Design

Q. (Sam Francis, Sippicon Corporation, Marion, Massachusetts) Did you take into account the heat which came out of the leads?

A. Yes, we did. The heat that came out of the leads was measured and subtracted from the generated power before arriving at the amount of heat that goes down to the base. The correlations are shown.

Q. And this was for each of the three different potting compounds?

A. That is correct. The amount of heat that comes out the leads turns out to be very similar for each of the different modules. For a module of the foam type, in which the power production is low, this lead loss becomes a very appreciable fraction of the heat that is generated.

Q. And all these leads came out from each component?

A. That is right.

Q. We conducted the same kind of an experiment some time ago. With respect to the problem of correlating the eighth-watt resistor to the others, we believe that this comes from the fact that the resistors were originally rated as eighth-watt, quarter-watt and half-watt under an environment between the two copper plates in free conduction. In effect, this means that you cannot extrapolate any of the data by the ratio of eighth, quarter, and half. You would have to run a new set of evaluations for each physical size of the component and this in turn means that the rating of the component not only is invalid when you put it into a cordwood module, but actually leads to bad design and failure. I know of one Polaris missile which failed because a designer took a resistor and used it with something like a sixty percent derating in a package. Of course, he was totally in error and it should have been designed differently.

A. It was called to my attention the other day that some quarter-watt resistors are no larger in diameter than an eighth-watt resistor. They are merely longer. This means that the bulk of the heat gets further away from the mounting plate. If you put more length in, then the ΔT of the top part of that resistor is certainly going to go above what it was for the eighth-watt case.

Q. (Leo Fiderer, Hughes Aircraft Company, Culver City, California) Did you ever find out what was the cause of the striking difference between one diagram and the other?

A. If you mean in the metal frame modules, the answer is no. I think the answer could be found but due to the pressure of other things, we have not been trying. It is an area that is open for investigation. If somebody investigates it, I would really be anxious to know how they make out.

Q. Could you come to any conclusions as to the recommended metal frame module design as the result of your investigation?

A. At this point, I am ignorant as to what made the difference in thermal performance. Apparently, with the same kind of glue materials put on in the same fashion, you can get drastically different performances. I do not know why this is so at this point.

Q. (Arnold Shlosinger, Northrop Space Labs., Hawthorne, California) Was this test performed in a vacuum?

A. Yes, these tests were all performed in vacuum, a hard enough vacuum so that convection was eliminated. It was strictly conduction and radiation modes of heat transfer.

Q. How do you account for direct radiation out of a direct component? What were the walls of your chamber? Were the walls of your chamber kept at the same temperature, or were they highly reflective?

A. I don't know how deeply to get into the answer to this question. The walls of the chamber were at room temperature. You might remember the base plates were at about 100 deg for the modules. I had an aluminized Mylar hat over the modules to reduce the radiation directly from the modules to the wall of the chamber. The leads all came out through the hat and were exposed to the chamber wall on the outside. As shown in the paper, for the foam module and the ones with nonuniform power distribution you will notice many of the temperatures below base-plate temperature. This is because the leads are sucking the heat out and cooling those resistors to below base-plate temperature. The heat is actually flowing in an inverse direction in the module, from the base to the parts.

Q. You kept the base plate at a constant temperature?

A. That is correct.

Q. (Max Callen, Minneapolis-Honeywell, Minneapolis, Minnesota) In the tests that we ran on the same type of arrangement we found that we got a similar spread of results and we found that this was due primarily to minute fractures in the cement or in the component bodies. Taking the heat out through the leads gave about the same results as the best performance that we got by cementing the bodies of the components to the heat sink itself.

A. Did you find a process that became more consistent?

Q. You mean in cementing?

A. Yes.

Q. We found that with proper cleaning and very careful preparation of cement that we could minimize this.

Paul F. Andrus-Some Practical Approaches to Thermal Problems in Airborne and Missileborne Electronics

Q. (Leonard Yuska, United States Avionics Facility, Indianapolis, Indiana) Who is the vendor of the paint, or is that classified?

A. I am sorry, I do not know. It is not classified.

Q. I would like to comment on the use of polyurethane coating. Have you made resistance tests in your laboratory?

A. No, we were not able to.

Q. Let me give you a little background to my question. Some time ago, I read an article or paper by a lady who works for Mr. Mathis which used to be Material Central in Dayton Air Development Center. Is that the paper you refer to?

A. I am not familiary with that paper, but I am familiar with Dayton.

Q. She wrote about the very good performance of Transit, in orbit. Later, I had the opportunity to talk to Mr. Mathis at Material Central and he refuted this article and said that they found on further testing that the polyurethane coating is miserable under ultraviolet exposure. This may be a lead for further investigation. It depends of course on the time factor. If the time is really short, a matter of weeks, there is no problem. But if it is of long duration, it could become one.

Q. (Clark Lankton, General Electric Company, Philadelphia, Pennsylvania) Did you have good reason for using the value for alpha when you calculated the temperature rise or the heat that would be transmitted from the shroud to the part? Why not use the emissivity?

A. You detected a weak point in that thermal analysis. We have no definite reason to believe that the emissivity and the absorbtivity are actually the same at a given wavelength. However, there is no reason to believe they are not. Our assumption that the absorbtivity of the finish would remain at 0.24 throughout all wavelengths is not truly valid and we realized this after the work was done.

Attendee Remarks (Sam Francis, Sippicon Corporation, Marion, Massachusetts) Your point about the thermal conduction path inside the box is well taken and often forgotten. I would like to re-emphasize, if I may, that people who think that a box that is a parallepiped or a square box is going to the best with the lightest weight should restudy the case. Because of this thermal path and the metal that you have to add to take care of it, we have placed a big sign in our Engineering Department, saying "Happiness is a long skinny box."

Additional Comment by Unidentified Attendee. I would like to add a remark to "Happiness is a long skinny box." There is another factor which, if you have a choice of geometry, is quite useful. If, for instance, you have a hemisphere as your container, your emission takes place by the whole surface while your solar reception is on the equivalent of the projected surface. In other words, there is a cosine angle when you calculate your absorption from the sun. This distributes over the hemisphere so your diameter circle is equivalent to what you get in solar radiation, but if you make it a hemisphere then you have the much larger surface of the hemisphere for radiation available.

D.E. Longmire-Packaging and Magnetic Field Interference

Q. (Mack Brown, Texas Instruments, Dallas, Texas) I wonder if you could give some dimensions of your field plot?

A. Yes, we can refer to the paper which has a small magnetron field plat. The scale is 4/5.

Q. Is that the scale?

A. Yes it is a small type. It was taken from a G.E. Magnet, a small magnetron at 3 kMc. Incidentally, a small hand-held gaussmeter which G.E. makes is extremely useful. It has a little probe sticking out an inch and a half and is about 1/16 in. in diameter. It is possible to move this around a magnet, and watch the meter face, and get a visual indication of where you are and what the direction and strength of the field is. It is very convenient. The other types are more expensive electronic devices where they have a hand-held wand. They are very good if you want to get down into the one-quarter and one-half gauss level.