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This report summarizes the progress made on the BN-$Al_xGa_{1-x}N$ based Heterostructure Field Effect Transistor (HFET) development program under contract number F49620-93-C-0059. The goal of this program is to develop high temperature heterostructure insulating gate (HIG) FET devices for integrated circuits operating in harsh environments. In particular, the insulator materials proposed for the device structure included CVD BN/AlN.

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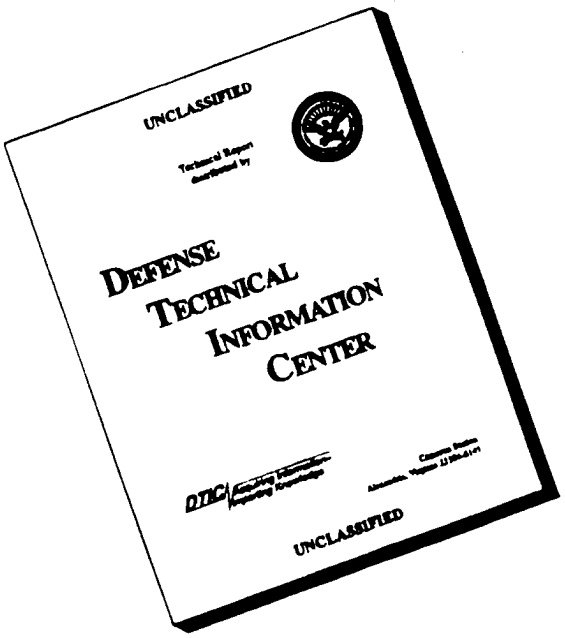


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# BN-$Al_xGa_{1-x}N$ Based Heterostructure Field Effect Transistor Devices for High Temperature (350 °C) Electronics Applications

FINAL TECHNICAL REPORT

SBIR PHASE - II CONTRACT NUMBER: F49620-93-C-0059

December 30, 1995



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# Table of Contents

# 1.0 Executive Summary

This report summarizes the progress made on the BN-$Al_xGa_{1-x}N$ based Heterostructure Field Effect Transistor (HFET) development program under contract number F49620-93-C-0059. The goal of this program is to develop high temperature heterostructure insulating gate (HIG) FET devices for integrated circuits operating in harsh environments. In particular, the insulator materials proposed for the device structure included CVD BN/AlN.

While the HIGFET processed with the MIS structures employing BN/AlN and $Si_3N_4$ as the insulators yielded low transconductances, tremendous progresses have been made on the optimization of AlGaN/GaN based FET structure growth and the following device processing. These are highlighted by the operation of AlGaN/GaN based heterostructure FETs (HFETs) at 300 °C. The same device also exhibited a cutoff frequency($f_T$) and maximum frequency of oscillation (fmax) of 22 GHz and 70 GHz at room temperature with a reasonable DC transconductance (23 mS/mm).

The understanding in the effect of the layer structure design on the operation of HFETs further led to the fabrication of first enhancement mode HFET based on AlGaN/GaN. Using a depletion and an enhancement mode HFET, we have demonstrated an inverter circuit which in itself is the build block for various applications. As can be seen in the sections that follow, the results from this work have pointed out the direction in which high transconductance HFETs with high current carrying capability can be realized.

## 2.0 Phase II Program Objectives and Goals

The goal of our program is to build GaN FET based integrated circuits such as operational amplifiers, inverters etc. for high temperature (350 °C) applications. In the Phase I program we demonstrated BN-GaN-$Al_xGa_{1-x}N$ hetrostructures and established their technical feasibility for a HIGFET (MISFET) device. We have also demonstrated high performance large area MESFETs based on GaN. Tungsten was shown to be a suitable metal for use in high temperature GaN based FETs. As an Ohmic metal it has the capability to withstand 350 °C operation. In Phase II we will fabricate and optimize short gate (0.5-2 micron) HIGFET (MISFET) devices and measure their high frequency performance under elevated temperatures (350 °C). These packaged devices will then be connected in a discrete fashion to fabricate high temperature GaN based ICs. The following is a list of specific program objectives:

(1) Deposit BN-GaN-$Al_xGa_{1-x}N$ MISFET (HIGFET) structures over basal plane sapphire substrates using low pressure MOCVD. The targeted channel carrier density is around $1x10^{17}$ $cm^{-3}$. for these epilayer (MISFET) structures both the channel thickness and the top insulator thickness is to be optimized. An insulating $Al_xGa_{1-x}N$ buffer layer is to be incorporated in all the structures.

(2) Characterize the MESFET epilayer structures to establish their conformance to designs. CV profiling is to be used to measure carrier density in the channel. Sputter Auger is to be used for verifying channel and insulator thicknesses. Hall measurements are to be used to establish carrier mobilities in the channel.

(3) Layout a mask for short gate (0.5-2 micron) BN-AlGaN-GaN MISFETs that is usable with cascade probes thereby enabling high frequency on-wafer device characterization. The mask set is to contain transistors with different gate lengths and widths. Several other test patterns for contact resistivity and Hall measurements to also be included on the mask set.

(4) Fabricate BN-AlN-GaN MISFET devices using the processing sequence as outlined in the Technical Approach section. The processing sequence consists of MESA isolation, source drain contact definition/metallizations and gate fabrication.

(5) Characterize DC and high frequency performance of fabricated MISFET devices. Characterization to include measurements of $f_t$ and $f_{max}$. Transconductance, specific resistances and barrier heights to also be measured. The characterization to be performed as a function of temperature up to 350 °C. This will be on-wafer characterization using high frequency probes. Part of the measurements will be carried out at AFWAL in collaboration with Dr. Chris Itos' group.

(6) Using the characterization data estimate the values of parameters needed to model device and drain current as a function of temperature. Use the models to further improve device designs and also to estimate performance of discrete and monolithic ICs based on GaN MISFETs.

(7) Package the fabricated MISFET devices for test market evaluation at other test facilities. The package development to conform with 350 °C operation.

(8) Evaluate feasibility of a simple op-amp and inverter circuit design. The op-amp to use a BN-AlN-GaN MISFET structure as a building block. The op-amp design to be analyzed as a function of operating temperature based on the device modeling.

(9) Fabricate some discrete IC circuits (such as op-amps) based on the MISFET devices resulting from the program. The objective will be to establish technical feasibility of future monolithic IC development efforts. No optimization will be attempted in Phase II.

## 3.0 Phase II Accomplishments

(1) Optimization of high quality AlGaN/GaN HFET structures using TEAl and TMAA as the aluminum source. These HFET structures exhibited 2DEG mobilities as high as 1600 and 5000 $cm^2$/V-s at 300 K and 150 K.

(2) Fabrication of short gate HFETs based on AlGaN/GaN. These devices were measured a dc transconductance of 23 mS/mm and showed microwave performance at $f_t$ and $f_{max}$ of 22 and 70 GHz.

(3) Growth, fabrication, and characterization of HIGFETs using $Si_3N_4$ as the gate insulator.

(4) Growth, fabrication and characterization of HIGFETs using BN as the Gate insulator.

(5) Demonstration of 300 °C operation of HFETs based on AlGaN/GaN with Schottky type gate.

(6) Demonstration of enhancement mode HFET and a direct coupled logic inverter employing both enhancement and depletion mode HFET.

(7) Investigation of HFETs under optical illumination. The data elucidated the importance of selective channel doping in further improvement of the HFETs.

(8) Growth, fabrication, and characterization of doped channel HFET structure and devices. The initial device results showed a dramatic improvement in the transconductance and current carrying capability, reaching $G_m$ of 50 mS/mm and saturated current density of 1 A/mm.

## 4.0 Technical Details

The following sections (4.1 through 4.8) describe the technical details in our development of the BN-AlGaN/GaN Based FETs to be used in high temperature applications.

## 4.1 HIGFET Structure Growth and Characterization

A basic structure shared by all the FETs developed during the course of this program is a simple AlxGa1-xN/GaN heterostructure as shown in figure 4.1-1. As seen this structure consists of an insulating (i)-GaN as the isolation buffer upon which the active devices are built. An n-GaN is then deposited followed by an AlxGa1-xN (200-300 A). We have established repeatable procedures to deposit the i-GaN in a separate program. These procedures are applied and refined as necessary. In the early development stage, the importance of the n-GaN channel layer was not realized. This layer was frequently grown unintentionally doped (without concentration control) or simply omitted. The reduced AlGaN/i-GaN structure still showed high mobility two-dimensional electron gas (2DEG) at the hetero-interface albeit a lower sheet charge density. For the top $Al_xGa_{1-x}N$ layer, the x value was 0.1 for most of the structures. The alloy was unintentionally n-type with carrier concentration around $5x10^{17}$ $cm^{-3}$.

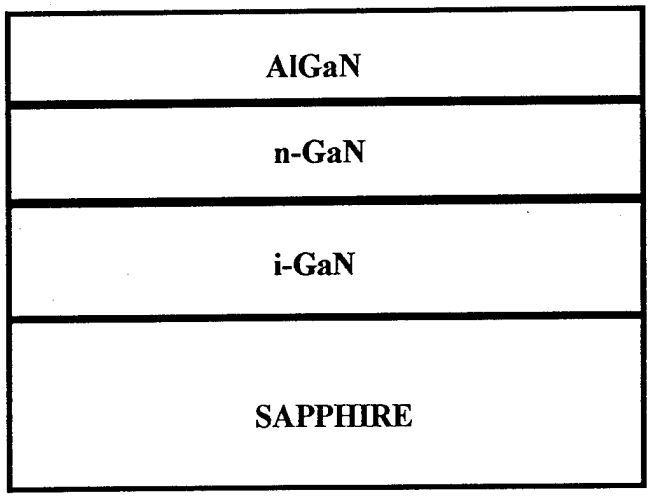



*Figure 4.1-1 Basic AlGaN/GaN Heterostructure used in the FET construction.*

For all the deposition described in this report, we used low pressure MOCVD technique. The growth system has been descried in detail in our several past publications (e.g. Khan et. al., Appl. phys. Lett., Vol. 58, 526(1991)). Ammonia (NH3) was used as the N source and triethylgallium (TEGa) as the Ga source. For the Al source, we have traditionally used triethylaluminum (TEAl). We had observed 2DEG at the AlGaN/GaN interface grown using TEAl as the Al precursor (Khan et. al., Appl. Phys. Lett., Vol. 58, 2408(1991)) with a low temperature (150K) electron mobility of 1600 $cm^2$/V-s. There were indications from these past work that the oxygen level in the TEAl grown AlGaN degraded the interface quality hence the electron mobility in our heterojunctions. To study this and to improve the heterostructure quality for HFET fabrication, we designed experiments in which trimethylamine-alane (TMAA) was used as the Al precursor. There are several reasons why this compound was chosen. In the past, Abernathy et al (Appl. Phys. Lett., Vol. 56, 2654(1990), J. Cryst. Growth, Vol. 107, 982(1991)) have successfully used TMAA for the deposition of very high quality AlGaAs layers and device structures in metalorganic molecular beam epitaxy (MOMBE). Roberts et al (J. Cryst. Growth, Vol. 104, 857(1990)) and Hobson et al (Appl. Phys. Lett., Vol. 58, 77(1991)) have also used TMAA in the metalorganic vapor phase epitaxy (MOVPE) of AlGaAs. The high quality of $Al_XGa_{1-X}As$ layers obtained using TMAA was attributed to a more complete decomposition of TMAA relative to trimethyl- or triethyl- aluminum during growth. The absence of Al-C bonds and the abundance of H-radicals (J. S. Foord, A. J. Murrell, D. O'Hare, N. K. Singh, A. T. S. Wee, and T. J. Whitaker, Chemitronics, Vol. 4, 262(1989)) in its decomposition is expected to lead to the reduction of carbon and oxygen impurity incorporation.

All the layers for the structure, shown in the Figure 4.1-1, were deposited at 76 Torr and 1000 °C. For the GaN layer, 1.8 μmole/min of triethylgallium (TEGa) and 1.25 L/min of ammonia flow were used. For the $Al_{0.1}Ga_{0.9}N$ layer, the TEGa and TMAA fluxes were 1.3 and 1.2 μmoles/min, respectively. These growth conditions are similar to those used in our previous work. Under such conditions, the typical carrier concentrations and Hall mobilities are $1x10^{17}$ $cm^{-3}$ and 450 $cm^2$/Vs and $5x10^{17}$ $cm^{-3}$ and 200 $cm^2$/Vs for the n-GaN and $Al_{0.1}Ga_{0.9}N$ layers, respectively. The use of TMAA did not result in noticeable deposit in the inlet of the reactor. At higher TMAA fluxes,

however, observable deposit accumulates in the inlet of the reactor. This is accompanied by a nonlinear dependence of the solid phase Al composition with respect to the gas phase Al/(Al+Ga) ratios as shown in figure 4.1-2.

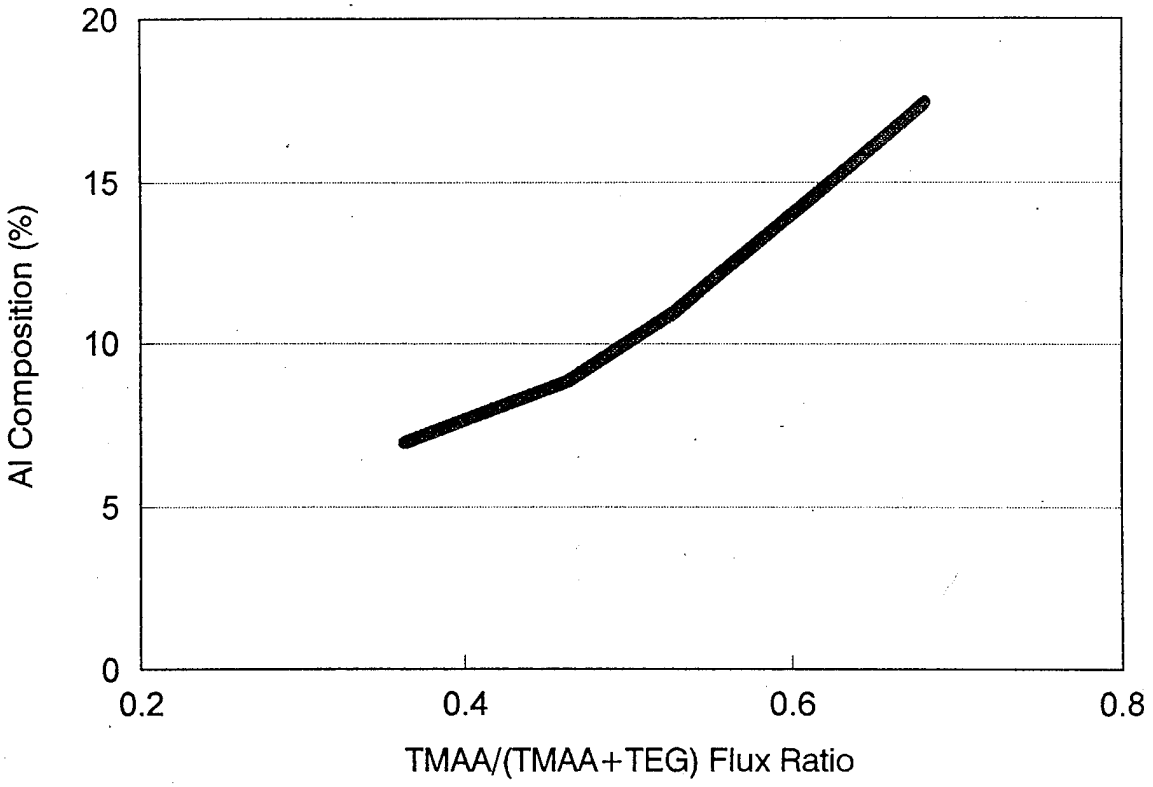



*Figure 4.1-2 The Al composition in the solid versus that in the gas phase in LP-MOCVD using TMAAl as the Al precursor.*

The heterostructures were then characterized for their electron mobilities as a function of temperature from room temperature to 80 K. The results of the Hall mobility measurements are plotted in Figure 4.1-3 (discrete points) along with those for a 4 μm thick n-GaN epilayer deposited over sapphire under conditions identical to those used for the growth of the GaN layer in the heterostructure. As seen, the mobility for the single GaN layer increases from 450 $cm^2$/Vs at room temperature to 1200 $cm^2$/Vs at 150 K. It then decreases for lower temperatures due to

ionized impurity scattering. On the other hand, the electron mobilities of the heterojunction increases to a value of 5000 $cm^2/Vs$ at 150 K and remains essentially constant for temperatures down to 80 K. We associate this enhanced electron mobility to the presence of 2DEG at the heterointerfaces. The 2DEG mobility enhancement is caused by a much higher volume electron concentration (compared to the bulk GaN), which results in a larger Fermi energy and a more effective screening.

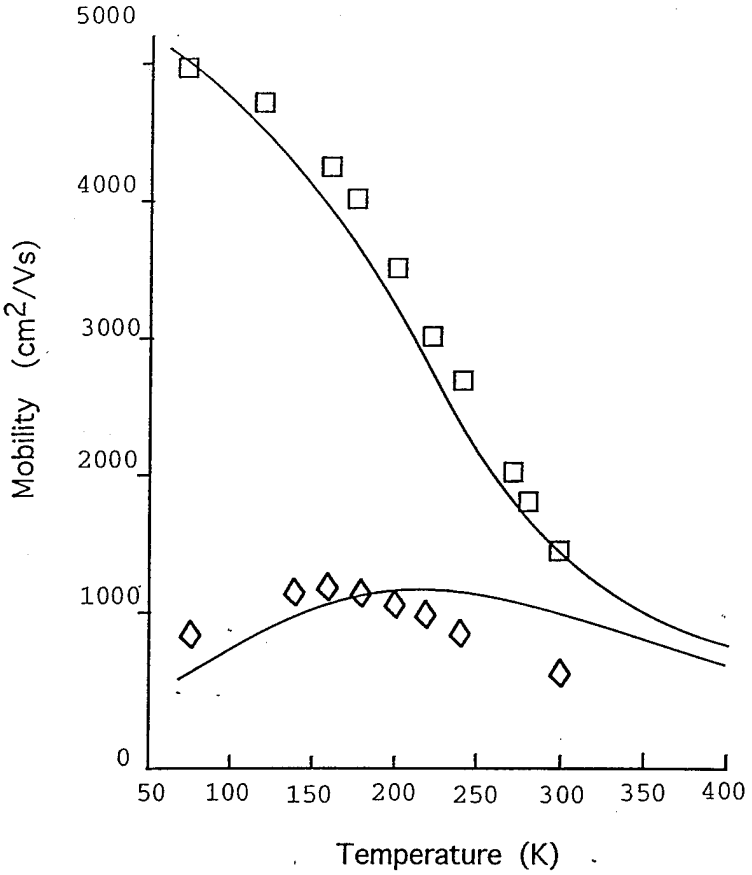



*Figure 4.1-3 Electron mobility as a function of temperature for AlGaN/GaN material system. The symbols show our experimental data for 2D (square) and 3D (diamond) electron gases The solid lines are from calculation.*

A secondary ion mass spectrometry (SIMS) analysis of the AlGaN layers of our heterostructures and the AlN layers grown using TMAA and TEAl showed the carbon and oxygen levels to be nearly identical for the two precursors. However, the photoluminescence (PL) of the AlGaN layer (in heterostructures with the AlGaN grown on GaN) grown using TMAA was superior to that

grown using TEAl. In Figure 4.1-4 we include the PL spectrum for an AlGaN/GaN heterostructure grown using TMAA. A pulsed excimer laser operating at 193 nm was used to excite the PL. Two strong emission peaks at 330 nm and 365 nm are clearly seen. These strong PL signals indicate good quality of the individual AlGaN and GaN layers in combination with an AlGaN/GaN interface relatively free from traps that are often the result of interface defects. We attribute the increase in the 2DEG mobility to this improvement in the interface quality of the AlGaN/GaN using TMAA.

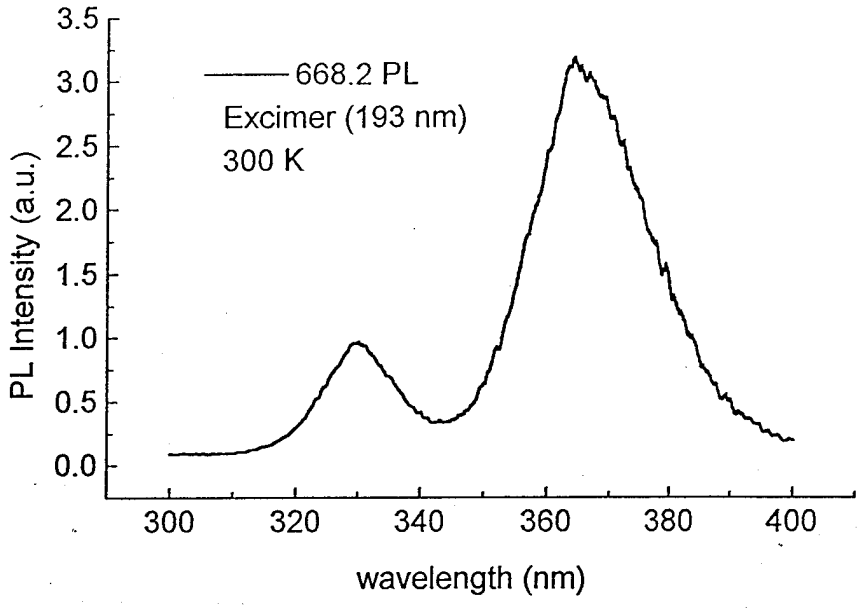



*Figure 4.1-4 Photoluminescence spectrum of an AlGaN/GaN heterostructure under 193 nm excimer laser excitation.*

The most important scattering mechanisms in GaN are optical polar scattering, ionized impurity scattering, and piezoelectric scattering. The mobility limited by the polar optical phonons was calculated using equations derived by Gelmont et al (J. Appl. Phys., Vol. 77, 657 (1995)) and the results are valid when the optical polar phonon energy (91.2 meV in GaN) is larger than the thermal energy. The piezoelectric scattering and ionized impurity scattering were calculated using a new approach developed by Shur and co-workers (unpublished). This approach allows us to account for ionized impurity scattering and piezoelectric scattering for an arbitrary degree of degeneracy. (A large electron concentration in the 2DEG leads to the electron degeneracy at

cryogenic temperatures whereas at room temperature the 2DEG is not degenerate.) Figure 4.1-3 shows the temperature dependence of the electron Hall mobility in GaN for the 2DEG and bulk GaN. Solid lines and open dots show the calculated dependencies and our experimental data, respectively. For the bulk calculation, we used $n=2x10^{16}$ $cm^{-3}$, $N_T=2x10^{17}$ $cm^{-3}$ and for the 2DEG calculation, $n=5x10^{17}$ $cm^{-3}$, $N_T=6.5x10^{16}$ $cm^{-3}$, where n is the free electron concentration and $N_T$ is the concentration of ionized impurities. The results of the calculation are in good agreement with our experimental data for the 2DEG. For the bulk GaN, the theory overestimates the electron mobility at elevated temperatures where the polar optical phonon scattering should be the dominant scattering mechanism. The most likely reason for this disagreement is our neglect of the temperature dependencies of the electron concentration and of compensation ratio. However, the agreement with experimental data clearly illustrates the mobility enhancement in the 2DEG.

## 4.2 Short Gate Heterostructure Field Effect Transistors (HFETs)

In the section 4.1, we described our effort in the growth and characterization of high electron mobility AlGaN/GaN heterostructures. To further confirm that these structures are suitable for the following insulating gate FET fabrication, we have processed part of the samples described in the section 4.1 into short gate HFETs before an insulator material is deposited. These short gated HFETs have attained state-of-the-art microwave performance and the result is described in this section.

The processing steps for these short gate HFETs are shown in figure 4.2-1. The source (S) and drain (D) were patterned first employing conventional UV photolithography, (a) and (b). Either Ti/Au bilayer or W single layer were used for the S-D Ohmic contacts, (c). The Ohmic contacts were annealed at 800 °C (1100 C for W) for 2 min. The wafer was then patterned again for the isolation level followed by H+ ion implantation. This gave electrical isolation from device to device (mesa to mesa). The gate level was written by electron beam lithography, (d). The nominal gate lengths were 0.2-0.25 μm. A final metalization and lift-off completed the HFET as shown in figure 4.2-2.

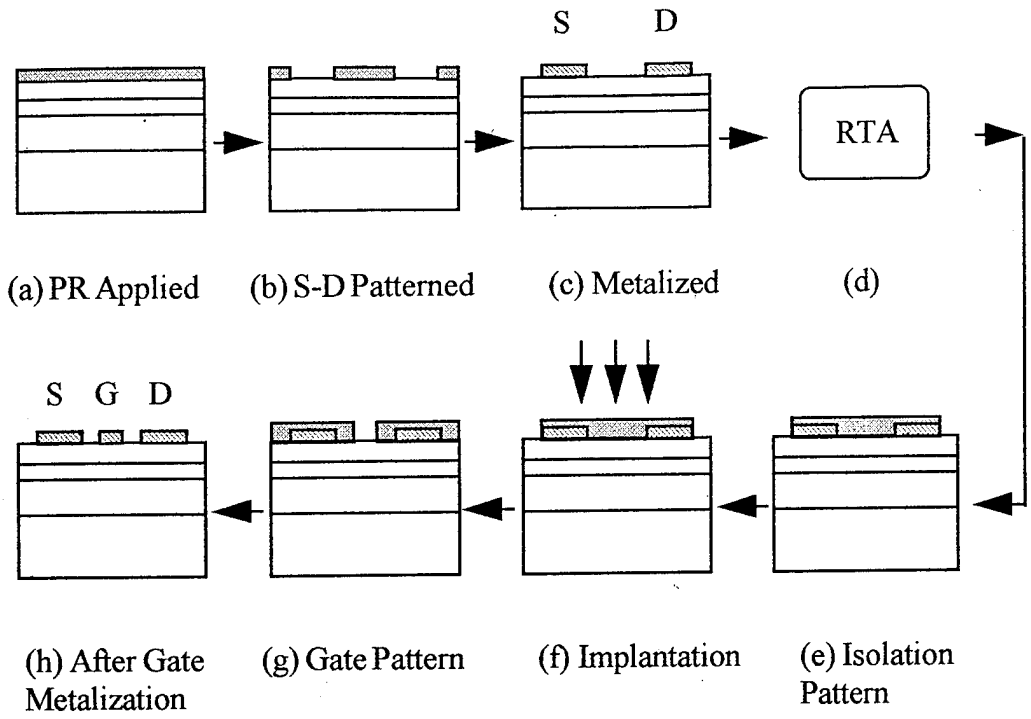



*Figure 4.2-1 Processing steps for the short gate HFETs.*

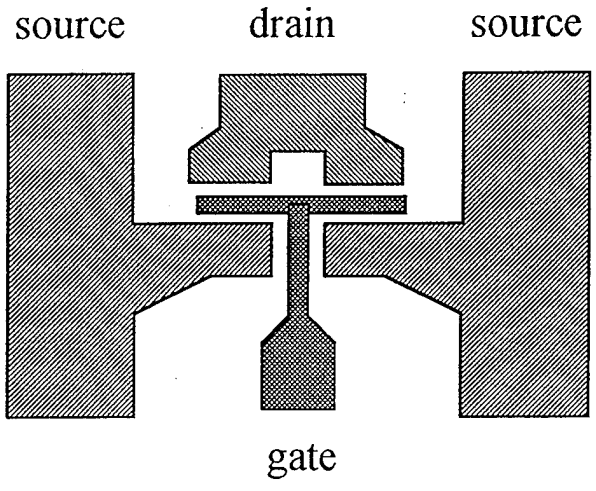



*Figure 4.2-2 Short gate HFET device layout.*

Typical measured S-D current-voltage (I-V) characteristics and the transconductance as a function of gate biases are shown in figure 4.2-3 (a) and (b) for a device with gate length and width of 0.25 μm and 150 μm, respectively. It is seen that the device has a respectable maximum transconductance (Gm) of 26 mS/mm and a maximum current density of 60 mA/mm. The device conductance at low drain biases is only weakly dependent on the gate bias for a wide range of values. This implies large source and drain series resistances, $R_s$ and $R_d$, which we estimate to be 30 Ω-mm from the source-drain I-V characteristics. We also observe a nonlinearity in the drain I-V curves indicating a non-Ohmic behavior for low drain biases. The device characteristic curves were analyzed using the universal HFET model (which was modified in order to account more accurately for very large series resistance) (Lee et al, in "Semiconductor Device Modeling for VLSI", Prentice Hall, 1993, p450). The fitting of the model to experimental data yielded $R_s = R_d$ = 28 Ω-mm width which was in good agreement with the simple estimate made above. The model also shows the maximum current in our device to be limited to approximately 60 mA/mm gate width. This limitation may be caused either by defect states at or near the AlGaN/GaN interface or by the properties of the non-ideal source and drain contacts.

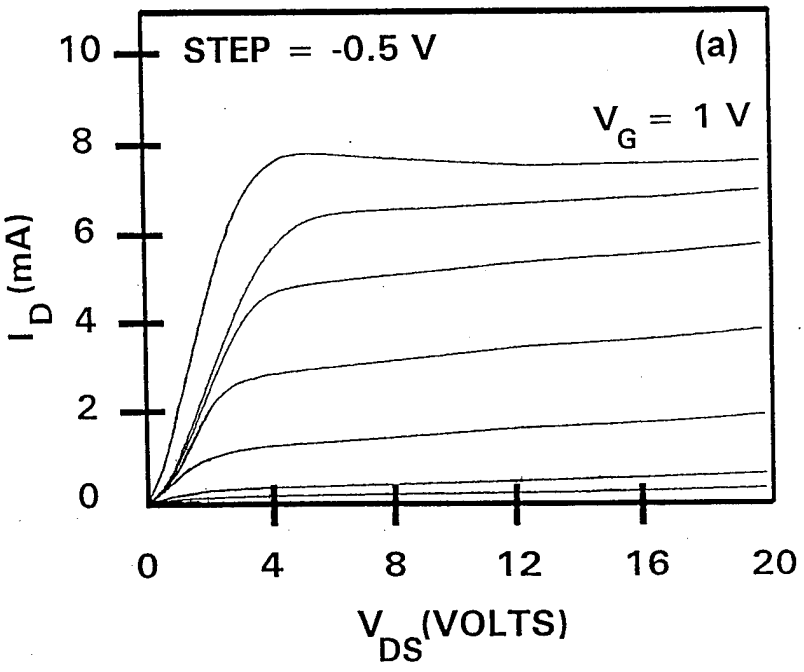



*Figure 4.2-3 (a) Source to drain I-V characteristics of short gate HFETS.*

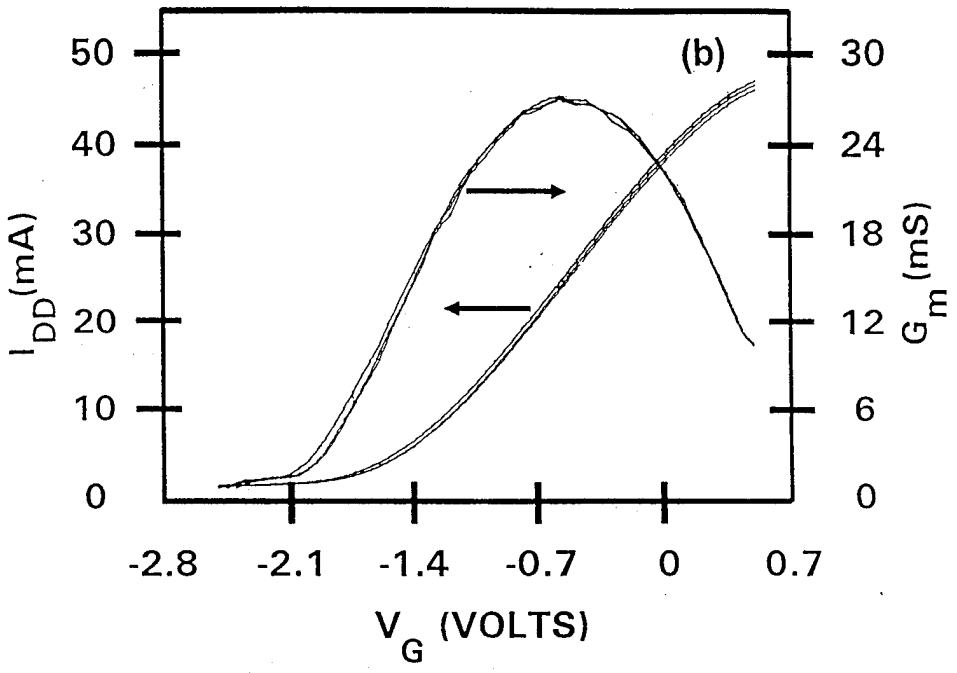



*Figure 4.2.3(b) transconductance as a function of gate biases.*

In Figure 4.2-4 we plot the measured gate current-voltage characteristics. As seen the turn-on voltage for the gate leakage current is around 3.5 V, characteristics of the high Schottky barrier formed between a suitable metal and a wide gap semiconductor. This makes possible the design of normally-off devices with positive gate swing for applications in digital integrated circuits operating at elevated temperature.

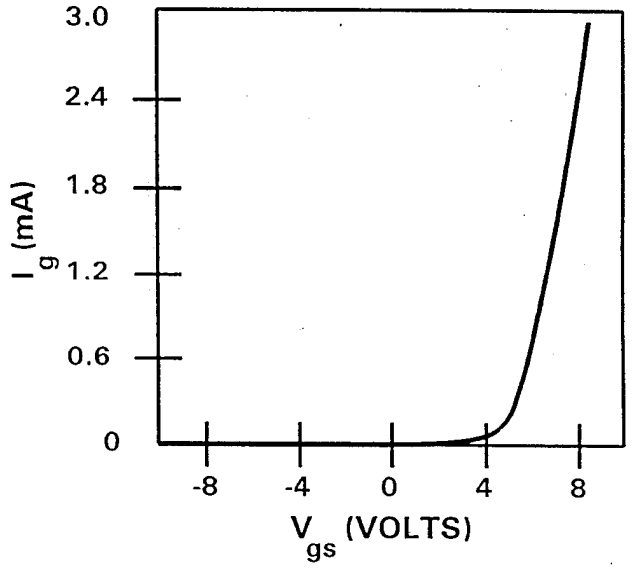



*Figure 4.2-4 Gate to source I-V characteristics.*

From the estimated values of the source resistance for our device, the maximum device transconductance ($g_{max}$) must be smaller than or equal to $1/R_s$ = 33 mS/mm. This number is in a good agreement with the maximum measured transconductance of 27 mS/mm (at room temperature). Hence, we conclude the extrinsic transconductance for our 0.25 um gate device to be limited by the series resistance. Also from Figure 2(b), the maximum measured transconductance corresponds to the extrinsic gate-to-source bias $V_{gs}$ = -0.5 V. The threshold voltage, $V_T$, is approximately equal to -2 V. The drain saturation current ($I_{sat}$) at $V_{gs}$ = -0.5 V is roughly 4 mA (= 27 mA/mm). Such a current leads to the voltage drop of 0.75 V across the series resistance. Hence, the intrinsic gate-source voltage swing, $V_{GT} = V_{gs} - V_T - I_{sat}R_s = -0.5 + 2 - 0.75 = 0.75$ V. Using this we estimate the concentration of the two dimensional electron gas, $n_s$, at the source as:

$$\mathbf{n_s = (\varepsilon V_{GT})/q(d_i + \Delta d) = 1.24 \times 10^{16}\ m^{-2}} \qquad \textbf{Eq. (1).}$$

Here q is the electronic charge, $\varepsilon$ and $d_i$ are the dielectric permitivity and thickness of the AlGaN layer, and $\Delta d$ is the effective thickness of the two dimensional electron gas which we estimate to be approximately 50 Å. At $V_{GT}$ = 0.75 V, the effective electron velocity $v_{eff}$ at the source end of the device is given by:

$$\mathbf{v_{eff} = I_{ds}/qn_sW = 13{,}500\ (m/s)} \qquad \textbf{Eq. (2).}$$

Since electron velocity increases from the source to drain the above value of $v_{eff}$ translates to a minimum cutoff frequency $f_T$ of:

$$\mathbf{f_T = v_{eff}/2\pi L = 12000/(2\pi \times 2.5 \times 10^{-7}) = 8.5\ (GHz)} \qquad \textbf{Eq. (3).}$$

In Figure 4.2-5(a) we plot the measured values of the current gain as a function of frequency for our 0.25 um gate length HFET device. As seen the measured $f_T$ value reaches 11 GHz (using 6 dB/octave rolloff), in good agreement with our earlier estimation. From the data of Figure 4.25-5(b), describing the measured gain versus frequency, we also estimate a value of 35 GHz for the

maximum oscillation frequency for our device. The relatively high value of $f_{max}$ is explained by a very low parasitic output conductance in the saturation regime (see Figure 4.2-3(a)). Also this $f_{max}$ value compares favorably with that of 10 GHz reported by Palmour et al (Proceedings of 2nd Int. Semicond. Dev. Res. Symp., Charlottesville, VA, 1993, pp. 695) for a 0.7 um gate length 6H-SiC MESFET device.

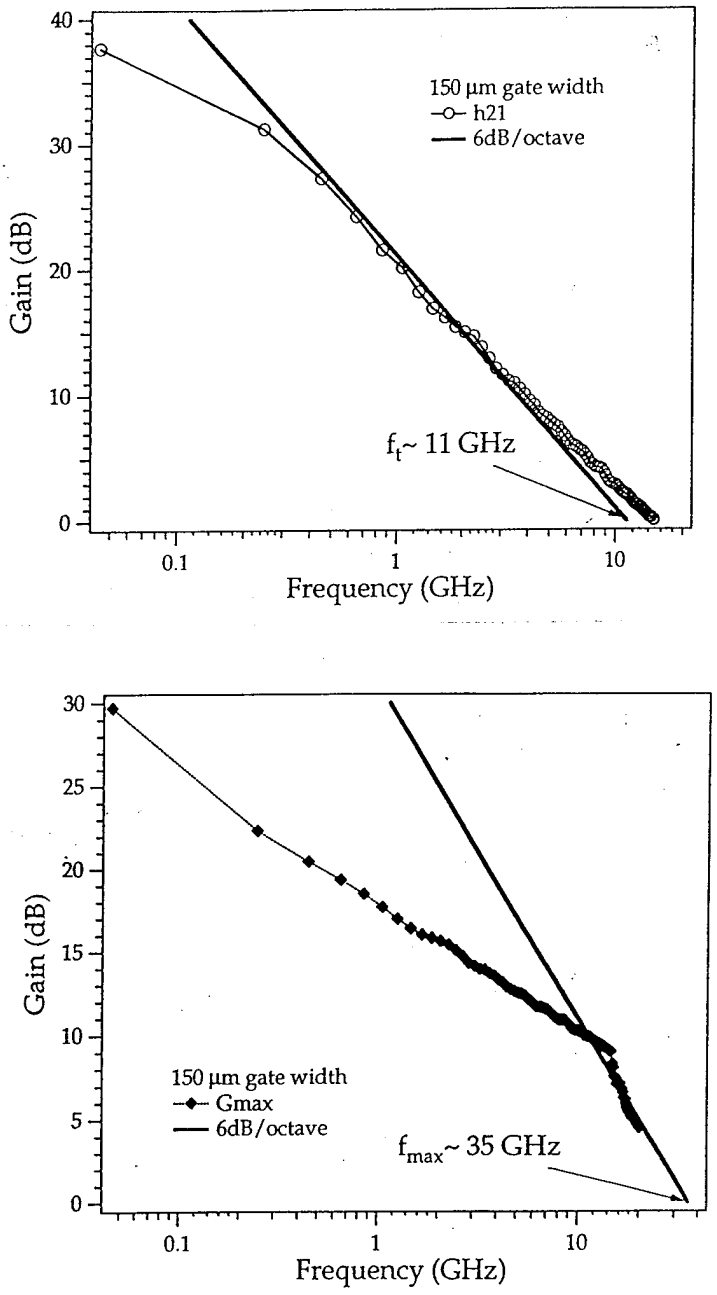



*Figure 4.2-5 Current (a) and Power (b) gains as functions of frequency.*

## 4.3 HIGFET Using $Si_3N_4$ as Insulator

In line with our phase II proposal to make heterostructure insulating gate FETs (HIGFET) for high temperature applications, we have attempted to use $Si_3N_4$ as the top (gate) insulator. The result of this study is described in this section.

Figure 4.3-1 is a structural representation of the HIGFET device. The device consists of a 500 Å thick silicon nitride ($Si_3N_4$) insulator grown on a 3000 Å of n-GaN which was deposited on a 3 μm insulating layer of GaN. The $Si_3N_4$ was epitaxially grown in the same LP-MOCVD system by switching in $Si_2H_6$ and $NH_3$. This thermal CVD insulator was grown at the same temperature as that used for the underlying structure (1000 °C). The resulting film is optically transparent and morphologically smooth free from cracks.

Shown in figure 4.3-2 is the extracted data from capacitance-voltage (C-V) measurement. The C-V meter operated at 1 MHz. As seen the zero volt depletion is at 1900 Å which places it in the n-GaN conducting channel. As the depletion bias is increased the channel begins to deplete until the depletion depth reaches the insulating GaN material at which point rapid expansion of the depletion depth is observed. The rapid expansion of the depletion depth occurs at a reverse bias of -5 V. Based on the C-V results, this structure was processed into a HIGFET.

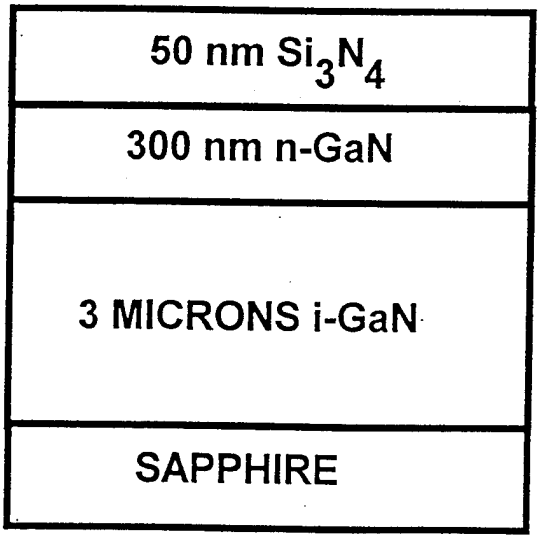



*Figure 4.3-1. HIGFET structure based on GaN.*

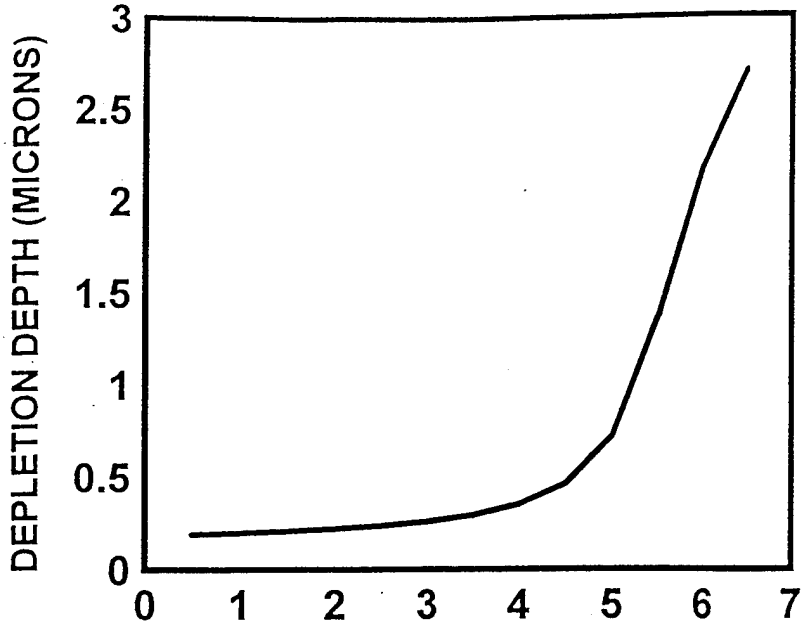



*Figure 4.3-2. Depletion depth vs. voltage for HIGFET structure.*

The processing of HIGFET is similar to the HFET processing steps shown in the figure 4.2-1 of section 4.2. Additional steps are added before the first Ohmic metal deposition to open windows through the $Si_3N_4$ insulator. Reactive ion etch (RIE) was used for this purpose. Conventional UV photolithography was used for the processing. Therefore the devices had some what larger dimension with a 4 μm gate length fitted into 10 μm S-D spacing.

The HIGFET devices were evaluated using a Tektronix curve tracer. Figure 4.3-3 shows the characteristics I-V curves which were measured for this device. Three curves are shown which correspond to gate voltages of +10, 0 and -2 volts. The measured transconductance for this device was 0.1 mS/mm. This value is much smaller than the 30 mS/mm we measured for a similar MESFET device. We feel the reduction in transconductance for this HIGFET device results from the thick insulator we deposited, 500 Å. Since the insulator is thick, a large percentage of the potential applied at the gate electrode is consumed across the insulator. This leaves a small amount of applied bias available for channel depletion.

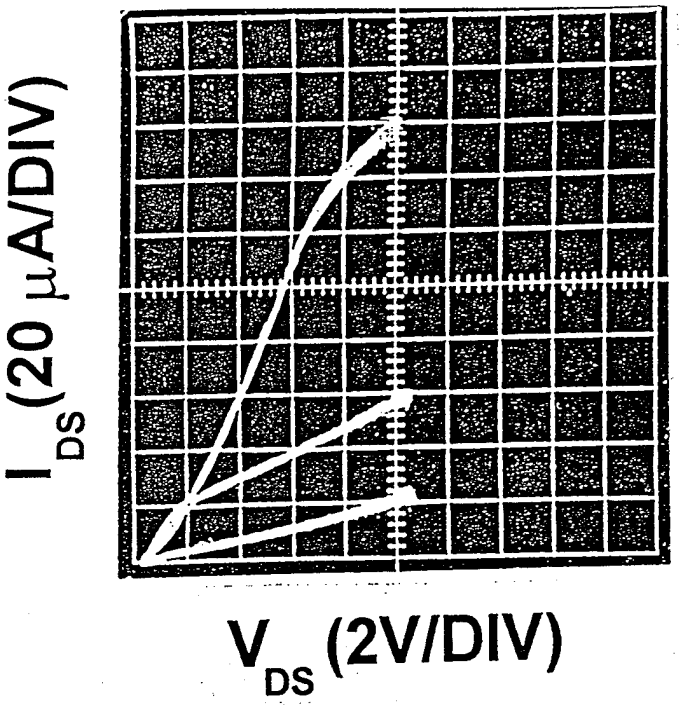



*Figure 4.3-3. I-V characteristics of the HIGFET using $Si_3N_4$ as the insulator on GaN.*

## 4.4 High Temperature Evaluation of Short Gate HFETs

Since the final goal of this program is to develop high temperature HIGFETs. It is relevant to evaluate the high temperature performance of HFETs in order to understand the issues that affect the high temperature operation of FETs. In this section we describe our results from such investigation.

Similar short gate devices were also processed and tested at elevated temperature. In these latter devices, the top AlGaN layer was 300 Å instead of 250 Å used in the devices described above. The devices showed similar DC characteristics at room temperature as those described above with Gm of 23 mS/mm and Rs=Rd=24 Ω-mm. Figure 4.4-1 shows the DC I-V characteristics at 25 °C, 200 C, and 300 °C, respectively. In addition to the expected decrease in the device transconductance with increasing temperature, there is also a sharp increase in the shunt conductance at 300 °C. This conductance at elevated temperature is thermally activated with an activation energy of 0.505 eV as can be extracted from figure 4.4-2. The shunt conductance is

practically independent of the gate bias. This is consistent with that the conduction is caused by the thermal activation of deep traps with a very large concentration.

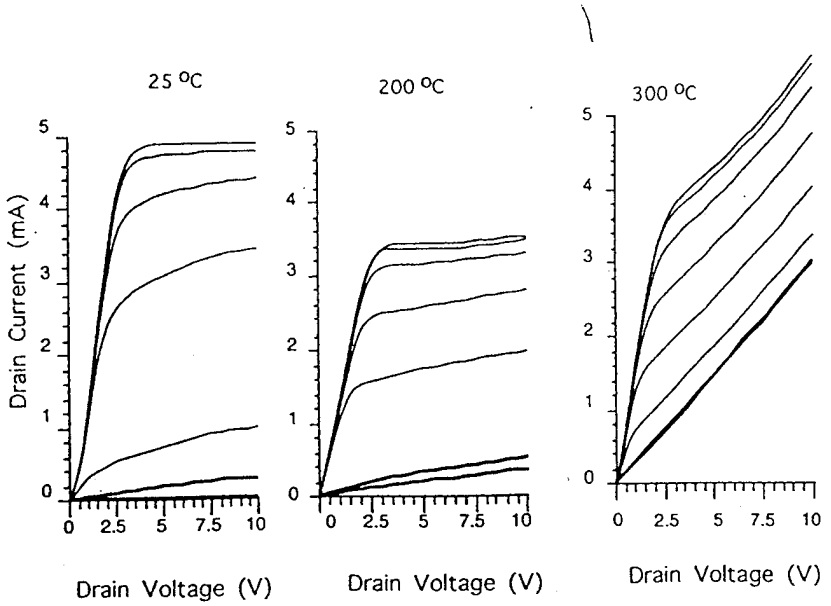



*Figure 4.4-1. DC I-V characteristics of short gate HFETs at 25 °C, 200 °C, and 300 ° C.*

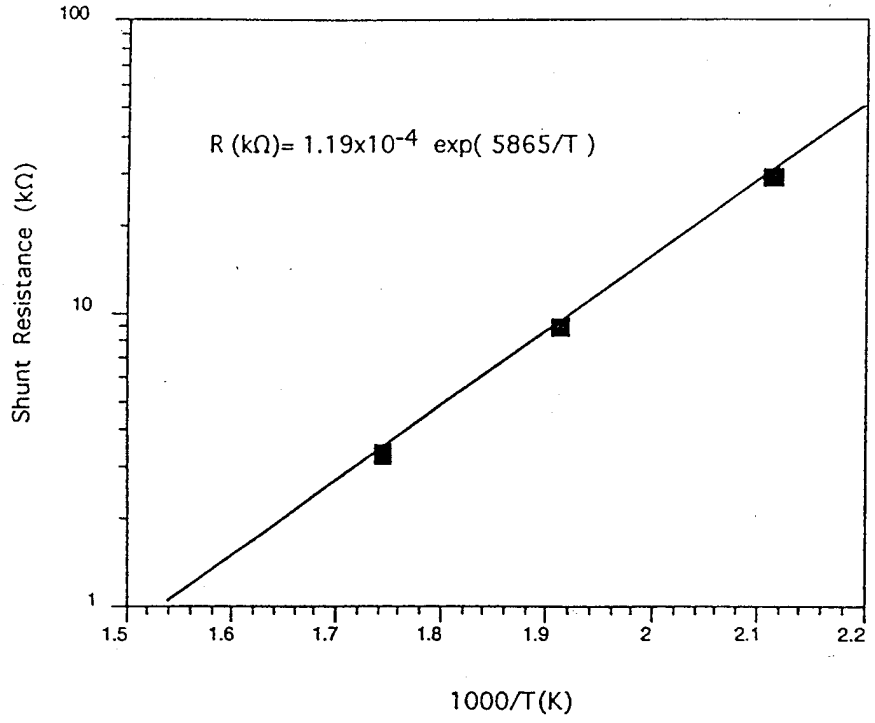



*Figure 4.4-2. Shunt resistance as a function of 1/T.*

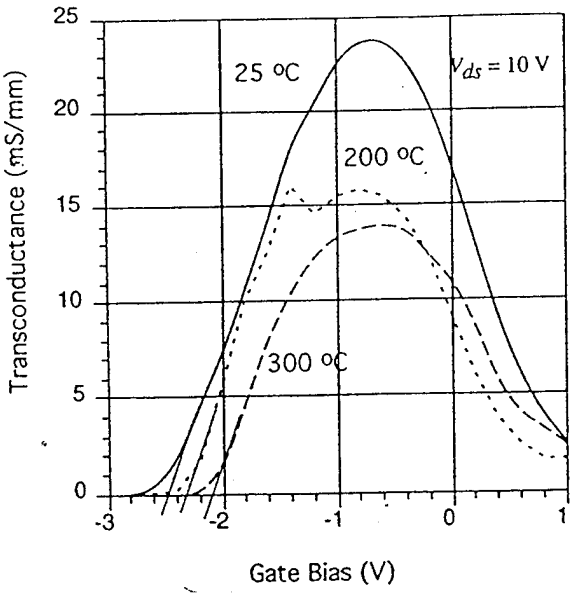



*Figure 4.4-3. Transconductance versus gate bias at 25 °C, 200 °C, and 300 °C.*

Transconductance versus gate bias is plotted in figure 4.4-3 for temperature at 25 °C, 200 °C, and 300 °C under $V_{SD}$ of 10 V. Here we observe a positive threshold voltage $V_T$ with temperature, which is that also observed in AlGaAs/GaAs HFETs and MESFETs (e.g. M. Shur, in "GaAs Device and Circuits", Plenum, New York, 1987). we also notice the double peak in the 200 °C data, which may be the consequence of the electron quasi-Fermi level crossing over trap levels.

These device also demonstrated microwave performance at elevated temperature as shown in figure 4.4-4. The $f_T$ and $f_{max}$, though decreasing with increasing temperature, retained respectable values of 5 GHz and 4 GHz, respectively, even at 300 °C. It must be pointed out that at 300 °C, the transistor characteristics is highly non-ideal and this temperature is also the very limit of our experiment setup. The $f_T$ and $f_{max}$ for these devices reached 22 GHz and 70 GHz respectively at room temperature.

In AlGaAs/GaAs HFETs, the gate leakage current presents one of the most important limitations of the device performance at forward gate bias. In contrast, in our devices, the gate current remained small (below 3V) even at 300 °C and is practically linear with gate bias in a semi-

logarithmic plot, figure 4.4-5. The characteristic resistance, Rgc=dVg/dIg is close to 1 MΩ at temperature up to 150 °C and is temperature activated above 200 °C with an activation energy of 0.88 eV. This, once again, shows an important role played by deep traps in the AlGaN/GaN material system. Nevertheless, Our data from these short gate HFETs demonstrates the superiority of the AlGaN/GaN material system for high temperature electronic devices and provides valuable information for the further improvement.

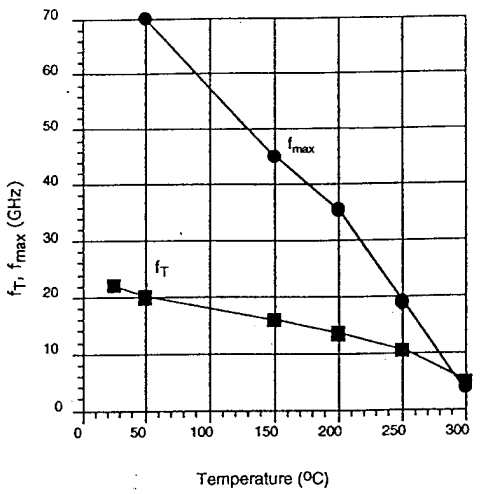



*Figure 4.4-4. FT and fmax as functions of temperature at $V_{ds}$=20V and $V_{gs}$=-0.8V.*

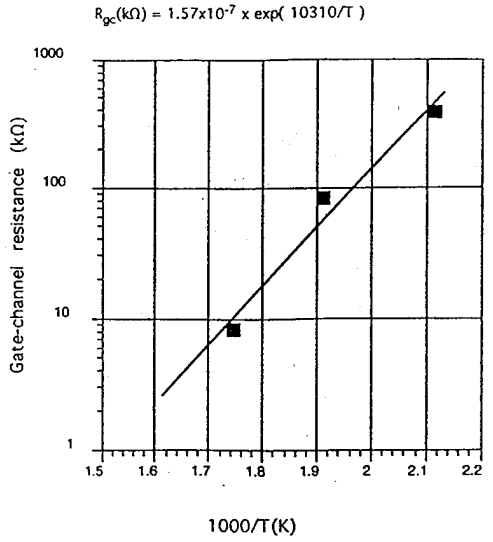



*Figure 4.4-5. Gate-channel resistance, $R_{gc}$ vs. 1/T at $V_{ds}$=6 V.*

## 4.5 HIGFETs Using BN as Insulator

In the Phase I program, we concluded that BN can be deposited on GaN (and AlGaN). Our initial electrical evaluation also showed promise of this insulator to be incorporated in a high temperature electronic device. However, the compatibility of BN with microelectronics processing has yet to be attested. In this Phase II program we have addressed this issue by fabricating HIGFETs with BN as the top insulator layer.

The structure used in the fabrication is basically the same as those HFET structure developed in section 4.1 adding a top BN insulating layer, figure 4.5-1. The BN was deposited in the same LP-MOCVD system using atomic layer epitaxy (ALE). The details of ALE of BN have been summarized in our Phase I final report. Only a brief description follows here. After the completion of the HFET structure at 1000 °C, the ALE commenced with the injection of triethylboron (TEB). At the end of the 1-sec. TEB injection, the TEB was switched out to effect a 1-sec purging. After the purge, $NH_3$ was injected for 1 sec followed by another purge of 1 sec long, which complete a full ALE cycle. The ALE cycle was repeated for 50 times to accumulate approximately 50 A thick BN.

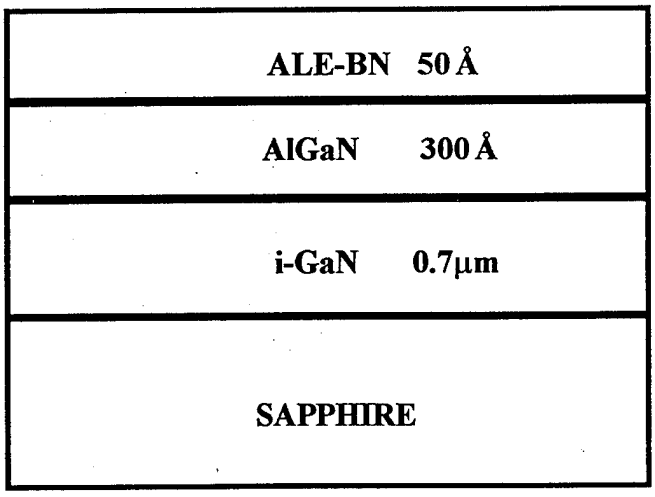



*Figure 4.5-1. HIGFET structure with BN.*

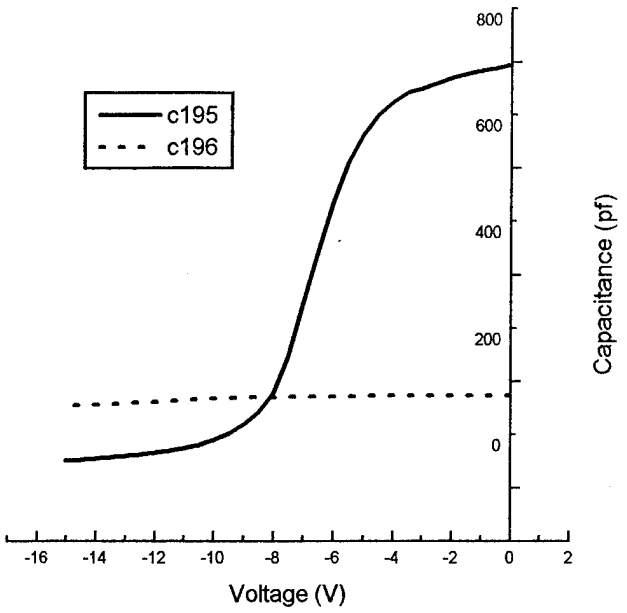



*Figure 4.5-2. C-V data of HIGFET structures with BN.*

C-V data, obtained on a Hg-probe station, from two of the samples are plotted in figure 4.5-2. As seen that sample c196 had virtually no variation under varying bias. It could have been 0 V depleted or have a high concentration of interface states pining the Fermi level. By scratching four contacts on such samples, Hall measurement can be performed. The measurement revealed a Hall mobility of 784 $cm^2/V\text{-}s$ and 1886 $cm^2/V\text{-}s$ for 300 K and 77K, respectively.

The processing steps in this context is the same as those used in the fabrication of the HIGFETs with $Si_3N_4$. One additional problem arose here, however. In some area the top BN layer started to peal off during the processing, due probably to the large mismatch in the lattice and thermal expansion coefficient between BN and the underlying AlGaN.

The source to drain I-V characteristics of a 4 μm long and 200 μm wide gate HIGFET is shown in figure 4.5-3. The gate biases were (from bottom to top) -10 V, 0 V, and 10 V. The curve family hardly separated with the scale shown, indicating a very small transconductance. In some area of the wafer, the gate-source I-V characteristics is Schottky like as shown in figure 4.5-4(a). This might indicate the area where the BN insulator has fallen off. There are areas on the wafer where the gate to source I-V exhibit high impedance with break down voltage better than 25 V.

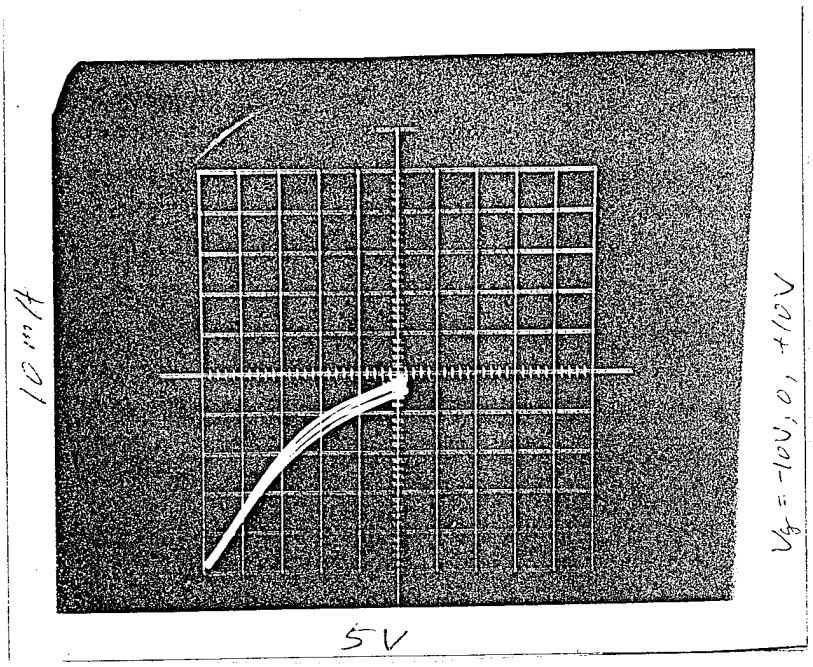



*Figure 4.5-3. S-D I-V characteristics of HIGFET with BN. The gate biases, from bottom to top, are -10 V, 0 V, and 10 V.*

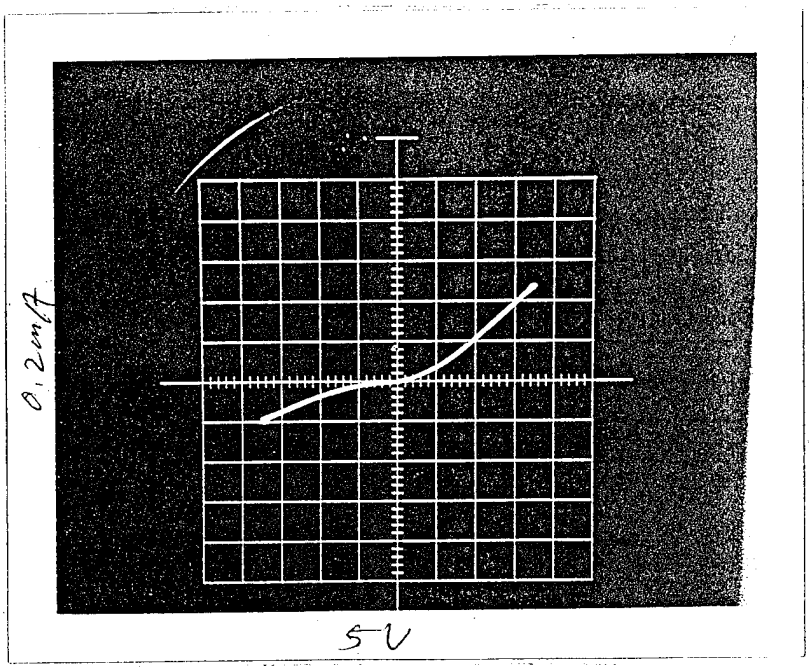



*Figure 4.5-4(a). G-S I-V characteristics of HIGFETs with BN in the area where the BN may have fallen.*

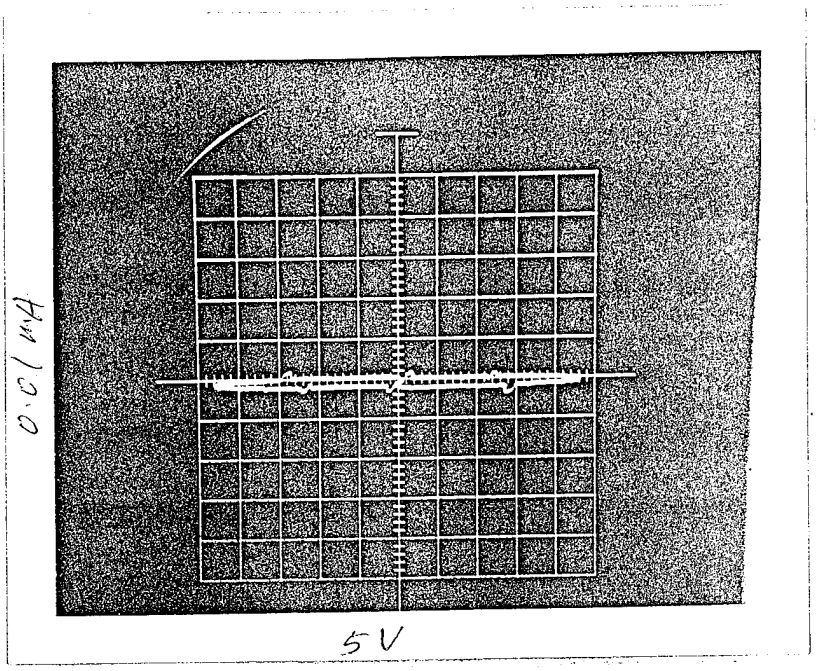



*Figure 4.5-4(b). G-S I-V characteristics of HIGFETs with BN in the area where the BN may still remain.*

## 4.6 Enhancement Mode HFETs and a Logic Inverter Based on AlGaN/GaN

We have seen from the data presented in section 4.2 that a relatively high positive swing of the gate voltage is possible and also unique for the wide gap HFETs. In this section we describe our attempt to explore this phenomenon to achieve enhancement mode operation of HFETs based on AlGaN/GaN.

The layer structure is similar to those used in section 4.2 (figure 4.1-1). To ensure a normally off channel condition (0 V depleted), the top AlGaN layer thickness was reduced to 100 Å (compared to 300 Å used previously). HFETs with varying gate lengths, gate widths, and S-D spacings were fabricated following the steps depicted in the figure 4.2-1. One exception here is that the isolation was achieved by mesa etching using RIE. Ti/Al was used as the S and D Ohmic contacts with a RAT at 800 °C for 2 minutes. Ti/Au bilayer was used as the gate Schottky contact without annealing.

A typical S-D I-V characteristics is presented in figure 4.6-1 for a device with gate length Lg. 1 μm and width W=150 μm. As shown, there is a complete pinch-off at 0 V gate bias (the threshold voltage is approximately 0.05 V). The positive gate swing reached 1.8 V without apparent gate leakage. The maximum transconductance for this device as shown is 23 mS/mm. This is the first time an HFET is shown to have a positive gate swing as high as 1.8 V.

Also note the nonlinear behavior of the S-D I-V at low VSD. This results from the non-Ohmic behavior the S and D contacts and can be overcome using better contact fabrication procedures. The device behavior can be explained by modeling the S-D contacts as diodes with a series resistance Rs and Rd, respectively. The device transconductance in the saturation region is affected by the high source series resistance, Rs. We roughly estimate Rs as follows. First, from the steepest slope of the I-V characteristics at the highest gate bias, we estimate $(R_s+R_d+R_{ch})$ to be 1300 Ω. Here, the $R_{ch}$ is the channel resistance and $R_s \approx R_d$. We estimate $R_{ch} \approx L/(q\mu n_s W)$, where L is the gate length, q is the electron charge, u is the low field mobility, ns is the maximum sheet carrier density in the channel and W is the device width. Using our measured value of 500 $cm^2$/V-s for μ and $n_s \approx I_{max}/(qV_{sat}W)$, where $I_{max}$ is the maximum saturated current and Vsat is the saturated electron drift velocity, approximately 105 m/s, we estimate $R_{ch}$ to be 400 Ω. This yields Rs to be about 450 Ω. This value of $R_s$ is larger than the measured value of $1/g_m$ ( 290 Ω). This implies the source series resistance $R_s$ to be drain bias dependent and hence is further reduced at high drain-source voltages in the saturation regime. This is further verified by the gate voltage dependence of our gm values.

Previously we have fabricated depletion mode HFETs (similar to those described in section 4.2 but with gate lengths from 1-5 um). We include one of the S-D I-V in figure 4.6-2. As seen the device operates in deletion mode with a threshold voltage $V_T \approx -0.4$ V. The availability of both the enhancement and depletion mode devices allows us to demonstrate, for the first time, an AlGaN/GaN direct coupled field effect logic (DCFL) inverter, which utilizes an enhancement mode device as a switching transistor and a depletion mode device as a load (figure 4.6-3(a)). The input and output wave forms are shown in figure 4.6-3(b), which clearly shows the inverter action.

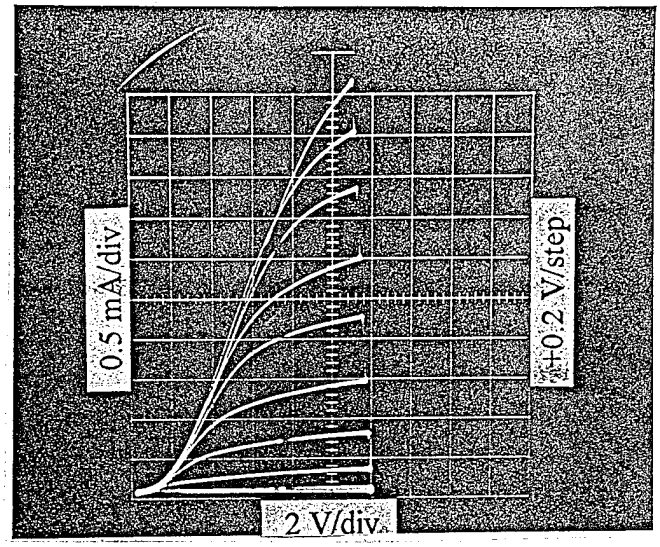



*Figure 4.6-1 S-D I-V characteristics of enhancement mode HFET.*

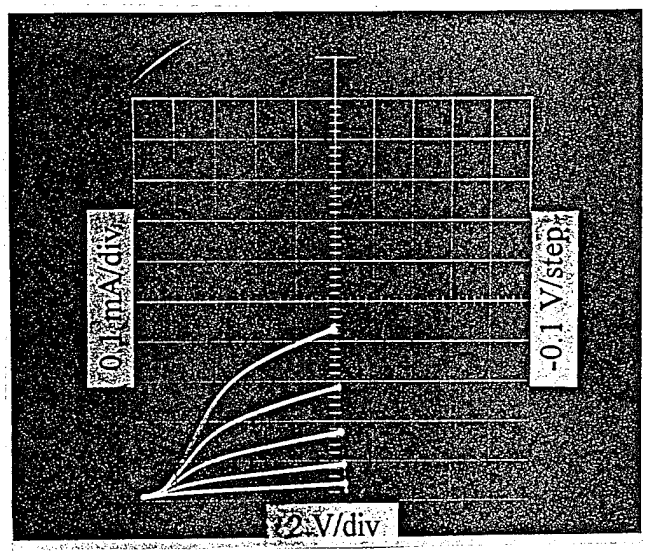
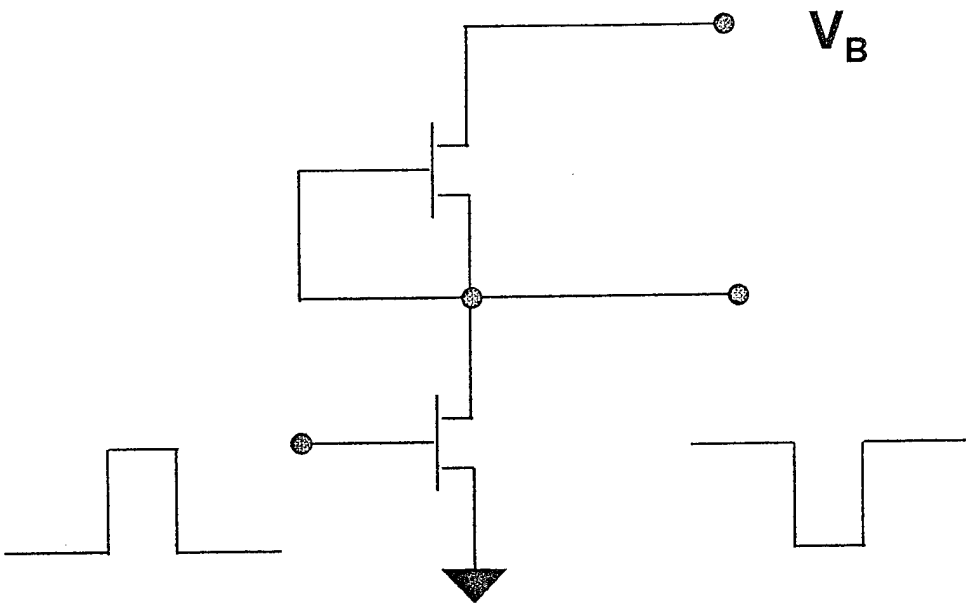



*Figure 4.6-2 S-D I-V characteristics of depletion mode HFET.*



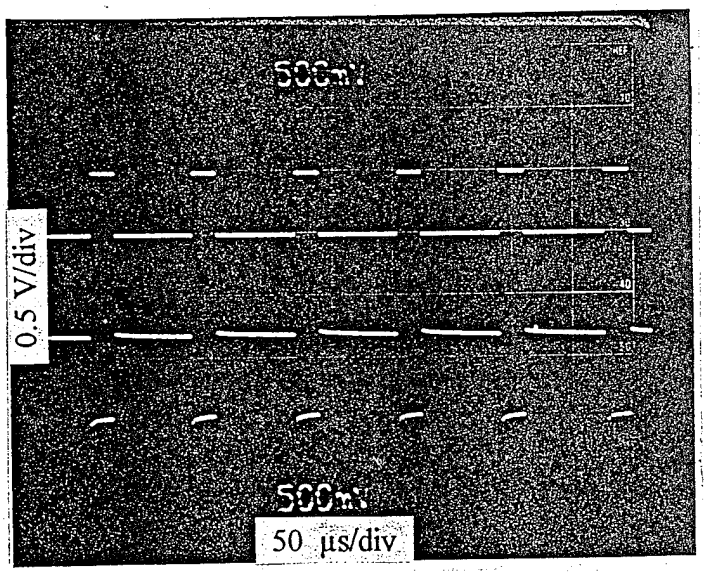




*Figure 4.6-3 (a) DCFL inverter based on AlGaN HFETs and (b) input and output waveforms.*

## 4.7 Characterization HFETs Under Optical Illumination

In our routine characterization of HFETs fabricated so far in this program, we have noticed a consistent UV light sensitivity of these devices. A following investigate revealed more interesting results which pointed out the direction to improve the dc transconductance of our HFETs.

The device investigated in detail was a HFET with relatively low threshold voltage, which in general displayed higher optical sensitivity. Shown in figure 4.7-1(a) and (b) are the measured S-D I-V characteristics of a 1 μm gate (150 μm wide) HFET without and with UV illumination. The UV light source was a He-Cd laser (325 nm, 2 mW) projected onto the back side of the wafer. Without UV illumination, the device has low transconductance (3.4 mS/mm) accompanied by a low threshold voltage (about -0.6 V). As seen the dc transconductance was greatly enhanced under UV illumination, reaching 75 mS/mm. This was accompanied by a shift of the pinch-off voltage to -1.4V. Notice also UV illumination improved the S-D characteristics at low S-D bias where the non-Ohmic nature of the contacts showed up more prominently.

This result can be explained by an "optical doping" of the channel effected by the generation of electron-hole pairs. The non equilibrium electrons drop into the 2D electron well while the holes are trapped in the i-GaN layer. To appreciate the effect of channel optical doping, we computed the band diagram (in real space) near the surface of the HFET structure under threshold condition. The results are shown in figure 4.7-2 for dark (solid line) and under UV illumination (dashed line). Parameters used in the calculations are dielectric permitivity of AlGaN, $\varepsilon_s = 7.9\times10^{-11}$ F/m, Schottky barrier height, $\Phi_b = 1.5$ eV, ionized donor density in AlGaN layer, $Nd=2\times10^{18}$ $cm^{-3}$, AlGaN layer thickness $x_n=300$ Å, conduction band discontinuity $\Delta E=0.273$ eV, and the trapped charge under illumination, $Nt=4\times10^{11}cm^{-2}$. As seen a relatively modest trapped charge is sufficient for a considerable shift in the threshold voltage. This shift in the threshold is a manifestation of the increase in the mobile charge in the channel ($n_s$). This leads directly to the dramatic improvement in the Gm under UV illumination. Since this optical doping affects the entire S-to-D conducting path, both the contact and series resistance are also reduced. One important implication of this finding is that the dc performance of the HFETs reported up to this

date is far from limited by the material parameters of the AlGaN/GaN system. By selectively doping the HFET structure and improving the contact procedure, a two to three folders of improvement in the dc transconductance is possible.

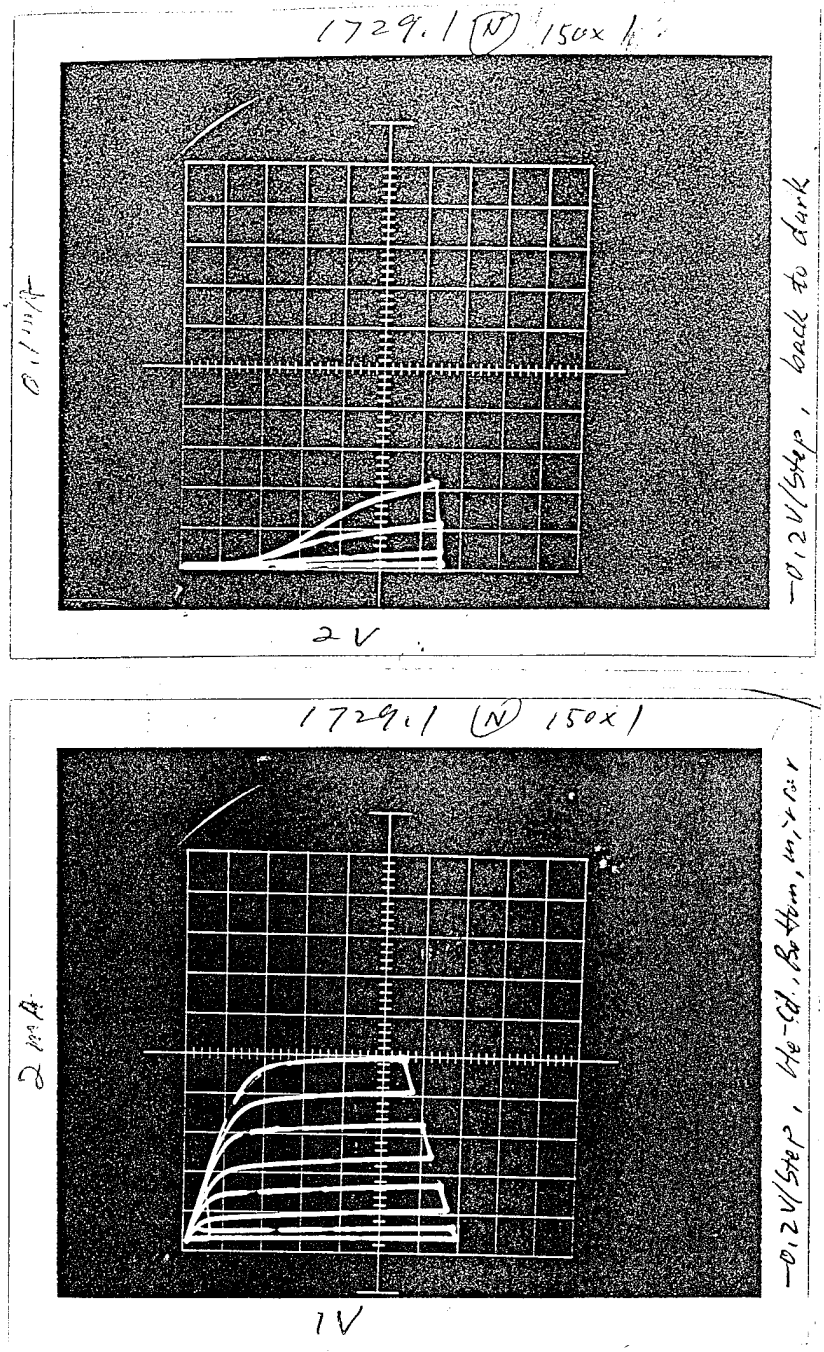



*Figure 4.7-1 Measured S-D I-V characteristics of HFET (a) in dark and (b) under 325 nm He-Cd laser illumination. Notice the dramatic enhancement in the transconductance and the shift of the threshold voltage.*

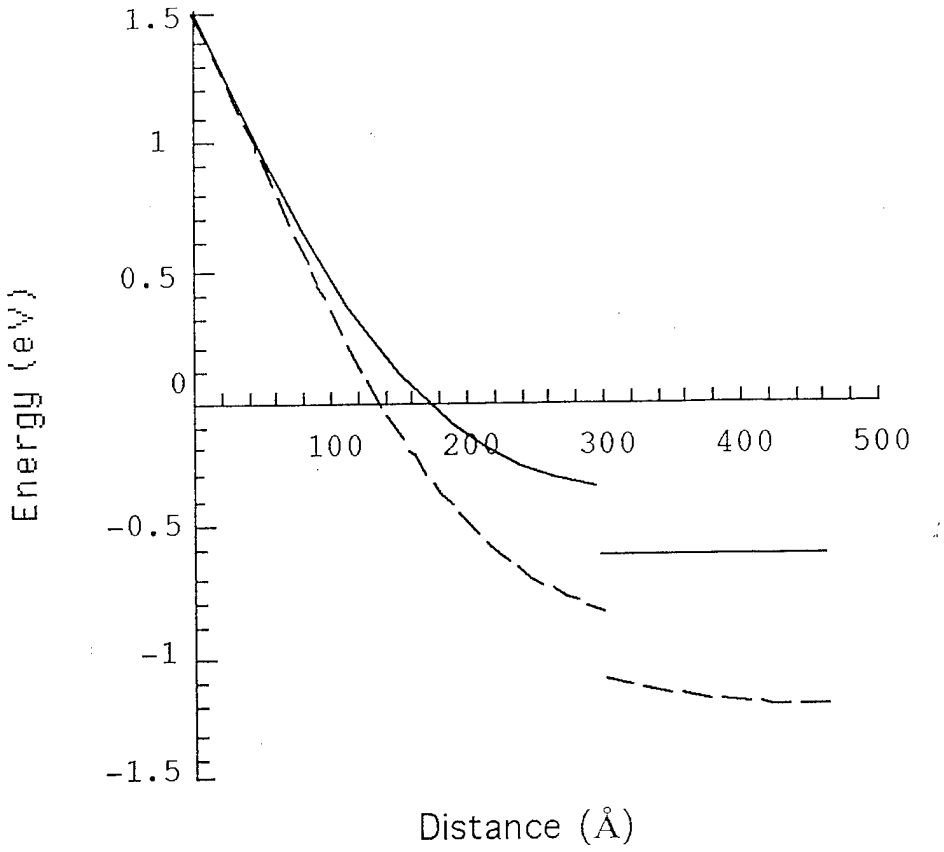



*Figure 4.7-2. Calculated band diagram near the surface of a HFET structure illustrating the effect of optical doping.*

## 4.8 High Current HFET for Power Amplification

There are number of advantages in using AlGaN/GaN HFET for power amplifications. As wide gap semiconductors, these include low thermal generation rate, high breakdown fields, and a large band off-set between AlN and GaN (estimated to be greater than 1 eV (Bykhovski et al, J. Appl. Phys., Vol. 77(4) 1616(1995)). However, the devices described in the forgoing sections have yet to realize such a potential. In this section, we shall describe our effort in increasing the current carrying capability of the HFET by intentional channel doping and by inserting an $n^+$-GaN contacting layer.

The first experiment involved a standard HFET structure (channel unintentionally doped only). The sample was taken to regrow 0.1 um thick highly doped $n^+$-GaN ($5x10^{18}$ $cm^{-3}$). The dopant used was disilane ($Si_2H_6$). Ohmic contacts of Ti/Al bilayer were made after the regrowth. The contacts were annealed at 800 C for 2 minutes. Show in figure 4.8-1 is the I-V characteristics

across a 3 μm gap with 200 μm width. As seen it is free from the non-Ohmic characteristics at low voltage as normally seen in our previous HFET structures. The total series resistance is measured to be only 33 Ω, considerably smaller than obtainable before. We estimate the resistance across the gap material to be less than 10 Ω. The contact resistance under each pad of 200 μm wide and 50 μm long (width and length in accordance with normal FET nomenclature) is a low of 12 Ω. This data also shows that a saturated current density as high as 1 A/mm is achievable.

The effect of the channel doping on the dc transconductance was studied using a doped channel HFET structure (DCHFET). Referring to figure 4.1-1, in the latter structure, the channel n-GaN and the barrier AlGaN layers were intentionally doped with $n=5x10^{17}$ $cm^{-3}$ and $6x10^{18}$ $cm^{-3}$, respectively. Hall measurement revealed an apparent sheet charge density of $2.6x10^{13}$ $cm^{-2}$ with room and 77K temperature mobilities 560 and 1259 $cm^2/V$-s. The exact 2D sheet electron density may be less than this number depending on the conduction band offset available. Nonetheless, this order of magnitude is much higher than what achievable in AlGaAs/GaAs material system.

The fabrication is the same as that described earlier using UV photolithography. The finished HFETs had gate length from 1 through 5 um in 5 μm and 7 μm S-D spacings. The S-D current-voltage characteristics of an HFET with 1x100 gate length and width is shown in figure 4.8-2. The devices exhibited a maximum dc transconductance of 50 mS/mm with a source to drain series resistance approximately 150 Ω. This represents state of the art working HFET(good $G_m$) with a saturated current density over 0.5 A/mm. The large output conductance is due to an unexpected condition variation during the i-GaN that often resulted in non-insulating material. Our experience has shown that it is necessary to refine the i-GaN growth condition from time to time in order to obtain nearly perfect insulating GaN layer. The mechanism behind this variation is still not fully understood. This data confirms our conclusion drawn based on our study of the HFET under optical illumination.

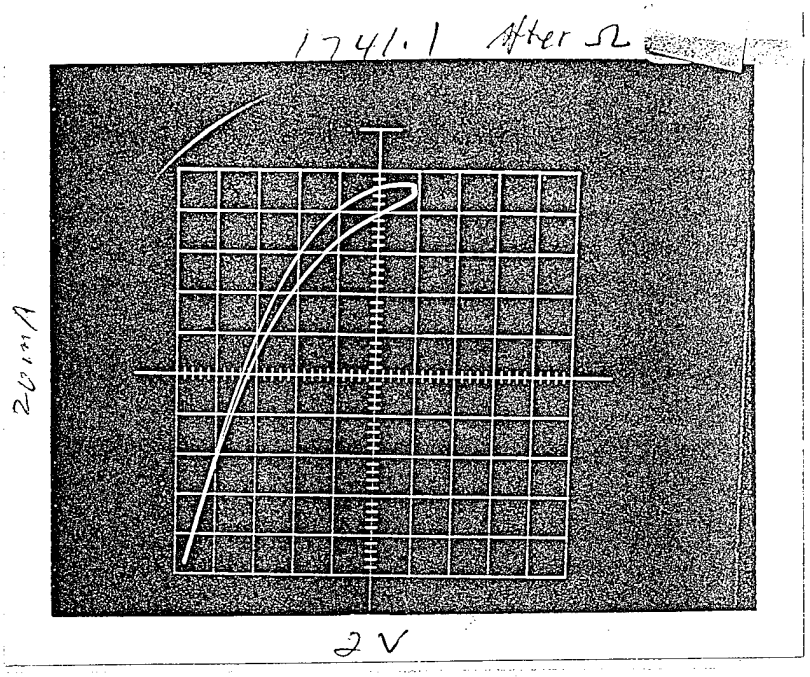



*Figure 4.8-1. S-D I-V characteristics of an ungated HFET incorporating n+-GaN contact layer.*

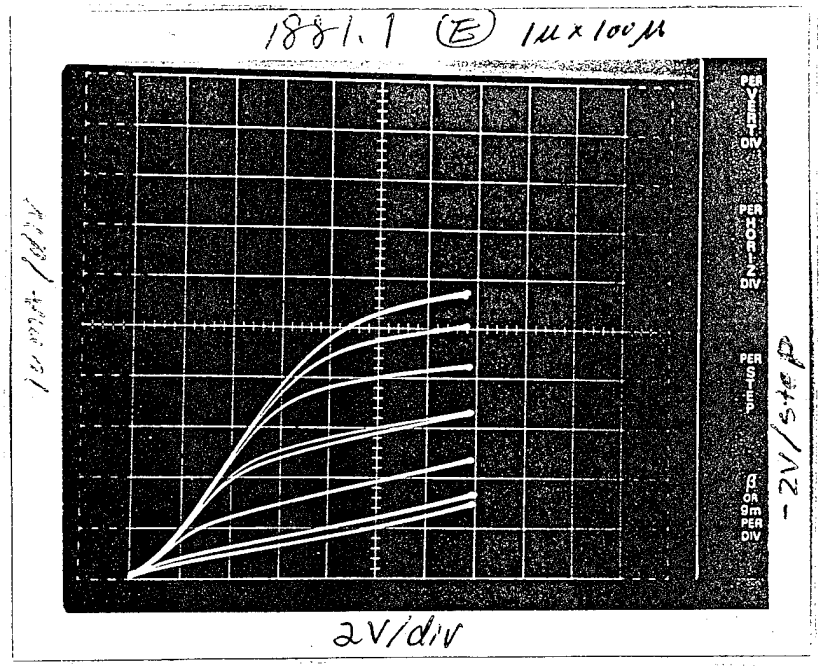



*Figure 4.8-2. S-D I-V characteristics of a doped channel HFET.*

# 5.0 Conclusions

The undertaking of this Phase II program has led to the optimization of the AlGaN and GaN materials and the relevant HFET structures. The availability of these high quality HFET structures has allowed us to refine the fabrication procedures unique to III-N wide gap semiconductor devices. The improvement in material growth and FET processing is reflected by the short gate HFETs with microwave performance at ft and fmax of 22 GHz and 70 GHz, respectively. Our high temperature testing of these HFETs further concludes that a 300 °C operation is possible even with a Schottky type gate in AlGaN/GaN based HFETs.

Encouraged and informed by the results from the HFETs, we have pursued vigorously in the growth and fabrication of HIGFETs structure and devices using both $Si_3N_4$ and BN as the gate insulators. The HIGFETs tested so far all showed low transconductance (less than 1 mS/mm). The ALE BN film also showed weak adhesion to the substrate during processing. Further work is necessary to find a better insulator for HIGFETs.

We have also demonstrated the first enhancement mode HFET in AlGaN/GaN by tailoring the HFET layer parameter design. Using an enhancement and a depletion mode HFET, we successfully implemented a direct coupled logic inverter based on AlGaN/GaN. A carefully analysis our data bears out the conclusion that HFETs (similarly HIGFETs) with much higher transconductance and high current carrying capability are possible with selective channel and contact layer doping.