REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	2/13/96	Technical Report: 5/1/95-2/13/96

4. TITLE AND SUBTITLE
Superconducting/Semiconducting Hybrids and Advance Memory Concepts for Superconducting Electronics

5. FUNDING NUMBERS

6. AUTHOR(S)
M. R. Beasley and M. Horowitz

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
The Board of Trustees of the Leland Stanford Jr. University
c/o Sponsored Projects Office, Stanford University
857 Serra Street
Stanford, CA 94305-4125

8. PERFORMING ORGANIZATION REPORT NUMBER
N00014-92-J-1886

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Department of the Navy
Office of the Chief of Naval Research, Code 414
800 North Quincy Street,
Arlington, VA 22217-5000
Dr. Deborah Van Vechten

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

The goal of this program is to explore advance alternatives to the standard approaches to memory in Josephson junction digital electronics. The work includes the systems, circuits, and materials aspects of the problem.

14. SUBJECT TERMS
Advance memory concepts for superconducting electronics

15. NUMBER OF PAGES
3

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	Unlimited

Technical Report
URI on Superconducting Electronics
N00014-92-J-1886

Superconducting/Semiconducting Hybrids and Advanced Memory Concepts for Superconducting Electronics

M. R. Beasley and M. Horowitz
Stanford University

Abstract:

The goal of this program is to explore advanced alternatives to the standard approaches to memory in Josephson junction digital electronics. The work includes the systems, circuits and materials aspects of the problem.

Report:

It is widely recognized that memory is the weak suit of digital superconductive electronics. Present concepts based on the storage of magnetic flux quanta have large cells and small margins. In this program we are investigating several alternatives to these conventional memories.

Superconducting/Semiconducting Hybrids.

In collaboration with the group of Van Duzer at Berkeley, we have been examining the potential of cold CMOS/JJ hybrid memories for use with Josephson digital logic. During the past year, we have analyzed the potential of this approach. We find that if one uses JJ SQUID circuits to sense the CMOS, the access time of the memory can be reduced by a factor of two. This increase should be maintained as CMOS memories are scaled down in size and thereby up in speed. We have also examined the trade off between speed, operating voltage and operating temperature. Speed favors higher voltage at the expense of power and therefore the refrigeration requirement. Our preliminary analysis suggests that the best temperature of operation will be around 40 to 50 K, even for use with low-Tc JJ logic circuits. We project that access times of about 500 ps at 350 mWatt dissipation should be possible in a 16 Kbit RAM using 0.4 micron CMOS technology with SQUID sense circuits. (This compares with 400ps at 40 mWatt for the same size conventional JJ memory.) At this operating temperature the SQUID sense circuits would have to be made from the high-Tc superconductors. Operating at the temperatures of low-Tc JJ logic increases the speed only marginally at a large expense in convenience of refrigeration. In the next year we plan to refine this analysis and to test the circuit ideas using low-Tc JJ SQUID sense circuits. We also plan to refine the models for low temperature CMOS.

Alternative Superconducting Memory Concepts.

We have examined the use of superconducting vortex flow transistors (VFT) for use in memory circuits. Their appeal lies in the greater gain they provide and the concomitant higher margins, hence potentially larger memories. We have found that the conventional VTF digital circuits are subject to a voltage state lock-up condition (both

devices locked in the finite voltage state) that prevents practical use. We have proposed an alternative approach based on the introduction of complementary JJ or VTF (CJJ or CVTF) devices that are the dual of CMOS. We are exploring various approaches to achieve practical CJJ and/or CVTF devices. A paper describing this work has just been submitted for publication.

A New Concept for Superconducting Magnetoresistive Memories.

Along with a visiting professor from Korea, we have conceived of a new approach to magnetoresistive memories using multilayers of superconducting and magnetic films. The concept of the device is based on the proximity effect between superconducting and magnetic films. The idea is analogous to the giant magnetoresistive effect in normal metal systems. Theoretically we find that by switching the relative magnetization of the layers in a magnetic bilayer in proximity with a superconducting film, the proximity effect is such as to suppress superconductivity in an adjacent thin superconducting layer or not depending on the relative orientation of the magnetization of the two magnetic films. Functionally the memory is a giant magnetoresisitive device with 100% modulation of the resistance of the device. We are in the process of preparing a patent disclosure on this invention. Also, experimental testing of this concept is underway.