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ELECTROMAGNETIC ENVIRONMENTAL EFFECTS MODELING OF ADVANCED PACKAGED MODULES

Stanford Research Institute, Inc.

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13. ABSTRACT (Maximum 200 words)
This report presents the results of an investigation of electromagnetic effects in boundary scan and other scan test sturctures embedded as test access ports (TAPs). The TAPs and test scan structures of interest in this study are those used in contemporary ICs and advanced packaged MCMs to enhance testability. This effort addresses the susceptibility issues associated with embedding boundary scan test circuits in MCMs, and its effect on the latent electromagnetic susceptibility of its host linear and digital circuits.

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DANIEL J. KENNEALLY

TABLE OF CONTENTS

OBJECTIVES

The objectives of this program are to investigate changes in circuit susceptibility to Electromagnetic Environmental Effects (EME) attendant with embedding test diagnostics circuitry as test access ports of multiport ICs and multichip modules (MCMs); and to identify CAD related, design concepts, rules, and caveats that can help to mitigate or to otherwise suppress those changes.

To support these goals, the following tasks were identified as reasonable steps necessary to develop an approach:

1. Evaluate commercial and military MCM design practices that currently use scan testability;
2. Investigate contemporary models of boundary scan (BS) test cells which are used in TAPS to enhance testability;
3. Develop CAD models of selected baseline functions with and without boundary scan, TAP structures and cells;
4. Define procedures and methodology to determine changes in EME susceptibility due to added TAP structures;
5. Determine model responses due to EME waveforms at any port on host MCMs and circuits during scan diagnostics;
6. Determine sensitivity to tolerance, accuracy, centering, layout, and identify enhancement opportunities; and,
7. Verify EME modeling using an MCM beta site.

SUMMARY

Design efforts for advanced packaged, multichip modules are in early engineering development, concentrating on functional performance, reliability and testability. The Rome Laboratory recognizes that this new packaging technology offers considerable promise for advanced, improved system design concepts. Examining and evaluating these advanced packaging designs now, in order to discover, assess, and fix any unknown design susceptibilities to EME, are prudent cost effective steps in any engineering research and development cycle.

Doing early design assessments before foundry commitment of these IC designs can identify the module circuits, nodes, and interfaces which are prone or susceptible to the degrading and damaging EME stresses. It is important to do these assessments with enough lead time to find and fix the susceptibility problems while still in the design stage and certainly before the final fabrication, test, and user acceptance. This way, manufacturers can avoid the unacceptably high costs of doing a major redesign or retrofit on a module found unacceptable due to susceptibility design problems discovered in final testing.

The following conclusions and recommmendations resulting from this study contribute to enhanced, robust designs for improving both electromagnetic and reliability quality of advanced packaged modules:

- EME assessments of MCMs should be done concurrent with the functional CAD to provide the functional (design) parameter data needed for the EME baseline modeling.

- EME assessments should be done concurrent with functional CAD to provide independent test, verification and validation of the baseline functional designs.

- EME assessments concurrent with functional CAD can find, identify, and characterize EME related problems.

- EME susceptibility of MCMs should be characterized early in the functional design phase in order to design and implement appropriate mitigation fixes, rules, algorithms, or caveats.

- EME assessments of advanced packaged modules which conform to IEEE Std. 1149.1 should comply with Air Force requirements for both module testability and rf assurance.

- Modeling an MCM requires lots of parameter data; formal ways to obtain these data should be defined and institutionalized in the procurement process.

- As the technology of advanced packaged modules expands and its literature grows accordingly, a design and analysis database of EME in MCM should be assembled and updated concurrently.

While today's technology of advanced packaged modules is growing so fast, its published literature is becoming equally enormous. With so many authors contributing so many results, on so many MCM related technologies, it is not surprising that an equally enormous body of MCM related reference material and terminology has evolved. For this reason, an MCM bibliography and a supporting glossary of MCM related terms are both included in this report. Both of these should prove very useful to anyone just entering the MCM field.

I. INTRODUCTION

The two most popular advanced packaged modules in current development and use are the transmit/receive (T/R) modules and multichip modules (MCM). T/R modules are used mostly in phased array, microwave antennas for performing command, control, and communications (C3) functions. These modules allow for active aperture, beam synthesis and steering agility, often with side lobes that are level and shape controllable. T/R modules also provide very compact, highly reliable, low noise rf front end receivers with much of their associated digital signal processing literally "up front". With highly reproducible and consistently good quality ICs, designed and fabricated in mature semiconductor processes, industry consensus is volume acquisitions of multichip modules will eventually drive attendant costs down considerably.

These advanced packaged, multichip modules (MCMs) are now fast becoming de facto standards for achieving high performance interconnections of very densely packed, integrated semiconductor chips. Manufacturers of digital systems first pioneered this new packaging technology and achieved very significant reductions in digital signal paths and associated parasitics. And at the same time, they achieved substantial increases in processing speed, as well as enhanced testability.

Very high performance, nanosecond computers with improved cycle time and minimum path delay are now possible using MCM packaging technology. Mixed bipolar and CMOS technologies are easily admitted with multiple, complex circuit functions sharing common substrata in very high density MCM packaging. Like T/R

modules, the industry consensus is that volume acquisitions of these modules will also drive their respective costs down.

While promising higher reliability and lower costs, modules must perform in many hostile environments which are spectrally dense and potentially degrading. These are the electromagnetic environments where unwanted, extraneous spectra penetrate into intended and unintended ports. The resulting effects (EME) are almost always degrading to performance functions of the victim systems, modules and circuits and, sometimes even fatal. Upset, waveform distortion, degraded SNR, digital latch-up, stuck-ats, control errors, timing skew, and permanent device damage occur in unprotected EME victims.

Gain compression (expansion), intermodulation distortion (IMOD), and cross modulation distortion (XMOD) are some of the more important nonlinear, EME responses in modules. Measuring or simulating this kind of distortion usually requires combining EM energy from an offending environment with the desired signals present at the input port. These two spectra are usually both injected at the intended input port, where they interact with each other and with the internal nonlinearities in the modules, and eventually corrupt the desired signal response at the intended output port. This is the conventional scaler distortion familiar to most, and is commonly used as an acceptance metric to determine quality performance of two port amplifiers.

In contrast, advanced packaged modules and ICs are, in fact, multiport packages that contain rf, LO, IF, digital, ground and bipolar DC bias, control, and other ports to service the various

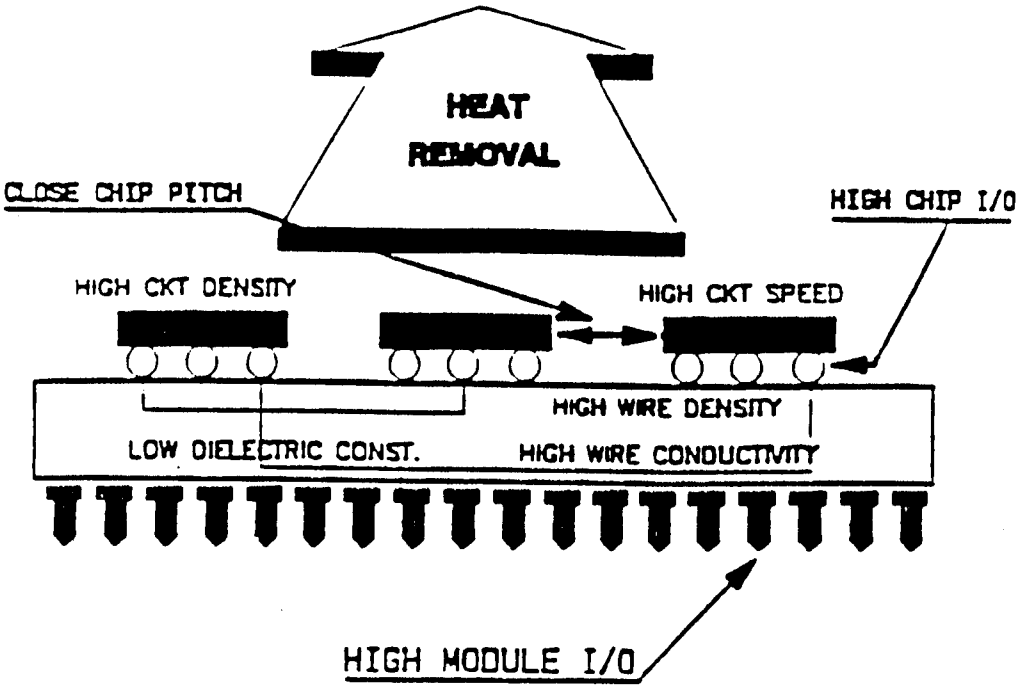
mixes of linear and digital circuits. In the case of multiports, EM energy incident at any port can cross couple to any other ports on the same package or module, and mix with the unintended (and even intended) spectra which may be present at those ports. This multiport cross coupling and mixing of the EM environmental spectra present at any port with signal spectra present at the desired port, through multiple nonlinear transfer paths in the MCM, cause desired signal distortion and upset at the intended output port and at other (unintended) ports. This is multiport distortion. It requires a vector susceptibility characterization to account for a matrix of all the possible nonlinear distortion responses on a multiport, multichip module.

II. MODULE TESTABILITY

MCMs continue to be driven by the (ever increasing) density and complexity of constituent ICs, and the attendant rising costs (and near impracticality) of performing discrete, manual methods of circuit testing. No discussion of advanced packaged, MCM performance can be complete without a discussion of testability. In fact, a major issue driving the realization and acceptance of high quality, cost effective MCMs is testability. Figure 1 shows some other important MCM technology issues.

Testability demands are pulling this packaging technology even further by exploiting potential benefits of MCMs embedded with built-in, self-test, diagnostics capabilities. Users now recognize the many possibilities of integrated diagnostics in advanced packaged modules and systems. Module testability and diagnostics are tightly linked together. They are indispensable attributes of any effective weapon system, and they are best implemented at the module level. The Air Force present position is clear: its recent announcement - "Policy on Design to Test" - ordains and requires designs for testability and diagnostics be inserted into all new Air Force systems down to the lowest level with performance verifications based on actual operational data.

Given the current emphasis on integrated product development and concurrent engineering, having embedded test and diagnostics capabilities designed into advanced modules offers considerable benefits to both manufacturers and users. The recent IEEE Std. 1149.5 on Test and Maintenance Busses and its companion standard 1149.1 on Test Access Port both provide good design guidelines for



Technology Issues in MCM

Figure 1

implementing embedded test diagnostics at IC, module, board and assembly levels of indenture. The next steps are to design, develop, and test advanced packaged modules which are embedded with test diagnostics; and validate the "designed-to" performance actually achieved with demonstrations in brass board, beta test modules.

While design efforts for advanced packaged modules are in early engineering development, their focus is understandably on achieving high levels of functional performance, reliability and testability at low cost. It would seem engineering prudent to investigate the MCM designs now in order to uncover, determine and assess any latent susceptibilities to unknown electromagnetic effects. Assessments done early enough, before committing CAD designs to foundry fab and assembly, can identify design flaws that make an MCM electromagnetically susceptible, and allow time to fix them. The bottom line is do these assessments with enough resolution to uncover all the potential susceptibility defects in a module design, and with enough lead time to fix them while still in the design stage, and certainly before incurring the high costs of major redesign and module retrofit, after-the-fact.

III. DESIGN FOR SYSTEM TESTABILITY

The Air force concept [1] for integrated test diagnostics is to systematically evolve an acquisition process that all of its developers and users will recognize, advocate and exploit as a value-added means of improving the combat readiness of Air Force assets through cost effective integrated diagnostics (ID).

Integrated diagnostics is a structured, design and management process for doing system acquisition and operation; it is not a process of structured (or rigid) design or structured management. The intent of system ID in the Air Force is to identify, exploit, integrate, and maximize the effectiveness of available diagnostic tests and supporting technologies in order to design, build, field, support, deploy, and fight a modern weapon system against any adversary, anywhere, and win.

Integrated diagnostics include test diagnostics for mission, safety, and maintenance needs. These include status/performance monitoring and testing, fault tolerance and troubleshooting, fault detection and isolation, and diagnostics data acquisition, storage, display and management. Integrated diagnostics may also includes assessments of on-board, diagnostics data by the crew for possible system reconfiguration in "near" real time.

Goals for system level ID include increased availability, increased mission effectiveness, and reduced costs. Availability (and reliability) are essential to successfully initiate, execute and complete an assigned mission. Mission effectiveness is the measure of how well, to what extent, and at what actual costs was the planned mission accomplished, including contingency plans.

Contingency plans may also include back-up modes, reconfiguration of "flight-critical" hardware and software, retargeting, abort, rerouting, and otherwise managing (and optimizing) the available on-board assets to accomplish the mission. These actions are made possible and enhanced by on-board ID.

After the testability requirements of a new system are determined and allocated to appropriate design levels, a key driver of ID in the system acquisition equation is to determine and partition "appropriate" diagnostic mixes. That is, how much test diagnostics should be allocated (embedded) to the platform, to external support equipment (ATE/ATS), or to field maintenance levels O, I, or D. These mixes can include electrical/electronic, mechanical, hydraulic, structural, and propulsion elements that make up the vehicle subsystems. Determining and partitioning the diagnostics mix goes down even further to the to the assembly, board, module, and IC levels. Optimizing mixes at all levels is very real challenge.

In analyzing requirements to determine the best diagnostic mix, all the essential diagnostics needed at each "action" level must be considered to assure a total diagnostic coverage. Here, "action" means sense, detect, isolate, repair, display, record, and reconfigure (the system) for contingency. Exploiting and integrating all these interrelated diagnostic elements requires that a well defined, working interface be set up among all the processes of design, engineering, manufacturing, maintainability, human engineering, and logistics support. The goal is to design into the new system a viable, cost effective capability to detect

and unambiguously isolate all the known and expected faults which can occur in all on-board systems during any mission, and in all operating environments. To these operating environments (used in the conventional sense), must be added degrading and debilitating electromagnetic environments, so often ignored as sources of on-board faults.

Integrated diagnostics can be thus reasonably expected to measure and display the health status of an operating system and its subsystems in near real (mission) time to the crew members. ID should also expected to detect locate and record component part failures, conditions with attendant operating environments. For example, these might include the need to do battle damage diagnostics with BIST (built-in-self-test), detect and isolate faulty cables and connectors, detect and isolate power switching transients, determine integrity of mechanical and hydraulic subsystems, and to perform embedded rf test diagnostics.

Another aspect of system ID which is often overlooked is the fact that about 70% of our current aircraft inventory contains nonelectronic, mechanical parts and assemblies. These too need integrated, embedded test diagnostics to detect, measure and record their operating status. It seems little or no appreciable work is being done toward achieving an embedded ID capability for nonelectronic subsystems. System design penalties of not doing this kind of ID are unknown. The damaging or degrading effects of electromagnetic environments on the embedded test diagnostics for nonelectronic subsystems, when and if they are implemented, are also risks of uncertain magnitude.

Of interest to the electromagnetics effects analyst is the often ignored reality that our aircraft platforms are dynamic, and have many moving, controllable structures and surfaces such as wings, rotor blades, flight control surfaces and rotodomes, as some examples. These moving surfaces can change the bore sight, radiation patterns, and related scattering of platform collocated antennas. Built-in adaptive antenna test diagnostics may be needed to measure and monitor antenna changes, in situ; and, possibly, to generate suitable compensation weights into existing beam synthesis algorithms.

The overall system design goal of ID then, is to achieve a cost effective capability to detect, isolate, and record all the faults that occur at all the levels of system indenture, in any environment. The current trend in systems acquisition is toward "integrated product development" or concurrent engineering, where testability and diagnostics are indispensable attributes equal only to system performance and safety. To reduce the system down time, an effective diagnostics script must test, detect, isolate, diagnose, and fix any system fault. In this regard, the current policy of the USAF is clearly stated in its "Policy on Design to Testability" [2]. The Air Force ordains and requires designs for integrated testability be embedded in all its new systems; and further requires testing to prove verification (and validation) of achieved, baseline testability. The message is integrated testability and diagnostics are now required in all new systems acquisition and at all levels of indenture.

IV. DESIGN FOR IC TESTABILITY

Integrated test diagnostics has two aspects: integrating the available technologies to develop maximally (and cost effective) testable systems and/or integrating (i.e., embedding) testability technology into all system levels. This report will focus on the latter aspect; and will concentrate on embedded testability at IC and module levels.

With growing impetus and demands for increasingly complex integrated circuits, board, modules, and assemblies, value added testing has become much more difficult and expensive. Compared with the ever increasing and spiraling costs of testing, costs of manufacturing seem to be steadily decreasing. In this regard, the associated economies of scale (i.e., "more is cheaper") certainly suggest that the components and parts for any system should be designed so they can be tested more easily and cheaply. "Testability" in this way becomes a legitimate circuit or module design parameter, and is now quite admissible to the repertoire of design requirements.

Testability and integrated diagnostics must also account for rf and microwave component performance in a systems implemented with embedded, compatible TM busses and test cells. RF test vectors might contain several "a priori" options that require an rf testability analysis of the system and its host circuits. As an example, embedded rf and microwave test diagnostics suggest using distributed test cells that will contain controllable rf sources, couplers, probes, detectors, analyzers, and a means of storing the measured response data. This is a big but necessary order, because

the local electromagnetic environments add stressful EM field and circuit drivers to fault and failure physics in victim, component parts. Spectral and temporal characteristics of these potentially degrading and damaging environments provide the failure analyst with some new dimensions to the failure data that may help resolve CNDs and other anomalous failure data. As an example of what may be needed, consider an embedded, distributed rf test cell based on a modified TSMD design that can measure and record the local EM environment which surrounds aging or failing parts in near real time. This test capability could provide the diagnostician with an EM "snapshot" at the instant of any part failure or upset; i.e., a spectral history or chronology of the local electromagnetic stresses which the part experienced during its operating time. In addition, these data could provide the EME analyst with bases for effective mitigation and suppression designs.

Circuit diagnostics, in general, is a test methodology to detect, verify, isolate, classify, record, and display electronic faults, failures or latent defects at IC, module, board, assembly and other levels of system architecture. Integrated testability is defined as a collection of structured processes of design and management which are necessary to achieve a maximum utilization of the inherent diagnostic test capabilities that are designed into the circuit (or system). Testability is thus to be designed or embedded into its hosts to achieve maximum benefits.

Design for testability (DFT) of mixed signal, integrated circuits is driven by the economies of scale associated with chip costs, densities and testing. The associated costs, time, and

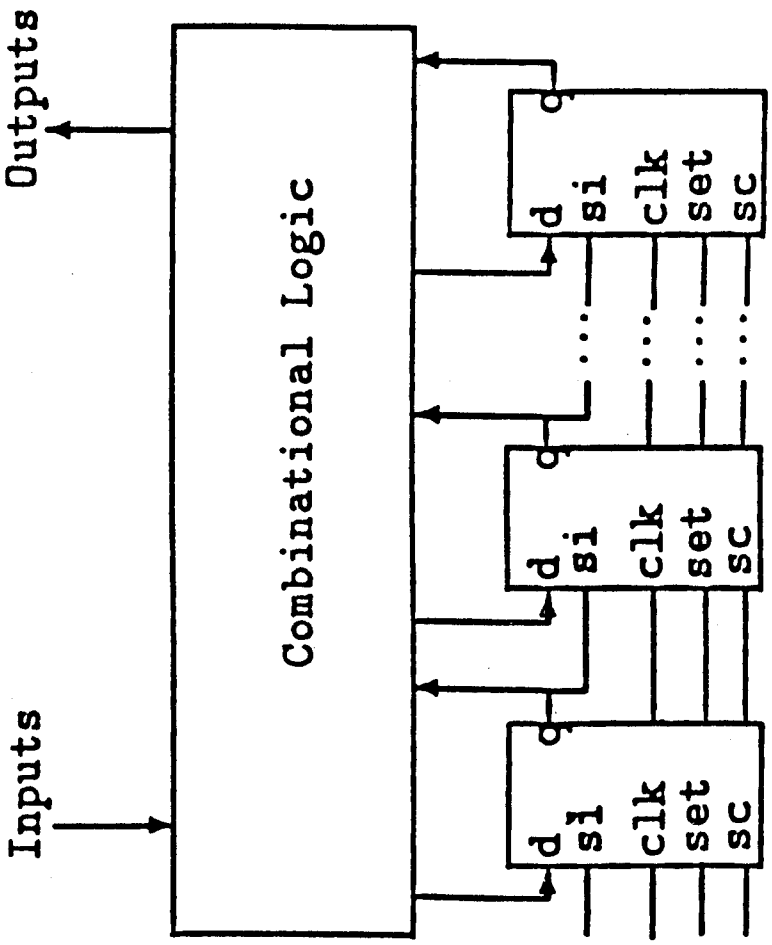
engineering impracticality for doing discrete probe or bed-of-nails setups to test chips, modules, assemblies, and boards are rapidly becoming too prohibitive. Thus, it is becoming more cost effective from the outset to integrate mixed digital and analog linear circuit functions into common packages, modules, and chips. It is also becoming more cost attractive to design-in whatever self-test circuitry are needed to provide embedded self-test, diagnostical capabilities. This is becoming especially prevalent in the new acquisition culture of doing "integrated product development", sometimes called "concurrent engineering", and in "total quality management" with its emphasis on device testability to generate the data for statistical process control.

DFT at the digital chip level usually involves test methods such as scan path, level sensitive scan design (LSSD), scan/set logic, and random-access scan [3]. Incorporating scan design in an IC, PCB, or MCM improves testability of its host by providing an easy access to serially address any state value stored in any gate selected for test. Access to the host chip can be achieved at the foundry by embedding D-type flip-flops which usually can be multiplexed between a normal signal mode and a scan-test mode. To enhance device testability which is consistent with increasing the complexity (density) of ICs and the prevalent use of surface mount technology, industry recognized a need for a standard test access port for IC chip level, scan design. The JTAG (Joint Test Action Group) was first formed to address this problem and was later succeeded by the Test Technology Committee (TTC) of IEEE. Sponsored by IEEE Computer society, the TTC issued IEEE standard

1149.1 [4] in 1990 which proposes a design and architecture for a test access port.

The IEEE proposed Test Access Port (TAP) is similar to the universal test connector that auto and truck manufacturers have standardized and designed into cars and truck engine compartments. It provides a standard access plug for fast and easy diagnostics of routine test, maintenance, or repair by measuring the host vehicle performance, and comparing resultant data with prestored failure codes based on windowed spec limits for that particular vehicle. Similarly, the TAP proposed for scan testing digital ICs, modules, and other assemblies is a standard interface port that provides host devices with externally controlled, scan test diagnostics which include boundary scan capabilities. Measured data from these TAPs are also compared with prestored, known good performance vectors in order to isolate and identify circuit defects, faults, or failures.

The purpose of any scan design for digital IC's is to make the host sequential circuits perform as combinational circuits when the IC under test is in a scan test mode [5]. At the chip level, this requires that a scan shift-register stage be placed adjacent to every input or output pin on each testable chip. This requires dedicated test circuits called "scan cells" to be embedded into the host IC. BS test cells are conventional D-type flip-flops, modified with two extra pins to provide access ports for "Scan Data-In" and "Scan Control". This is shown in figure 2. Serial data pins for Scan Data-In (SDI) and Scan Data-Out (SDO) as well as multiplexers and latches, are typically added as circuit overhead



Daisy Chained Boundary-Scan Test Cells

Figure 2

to the baseline functional design being so instrumented (or TAP'd) for enhanced testability. A Scan Mode Select (SMS) pin with its own clock is also added. The muxes select either the normal digital data signals being processed within the IC, or the serial scan data signals from the SDI pin.

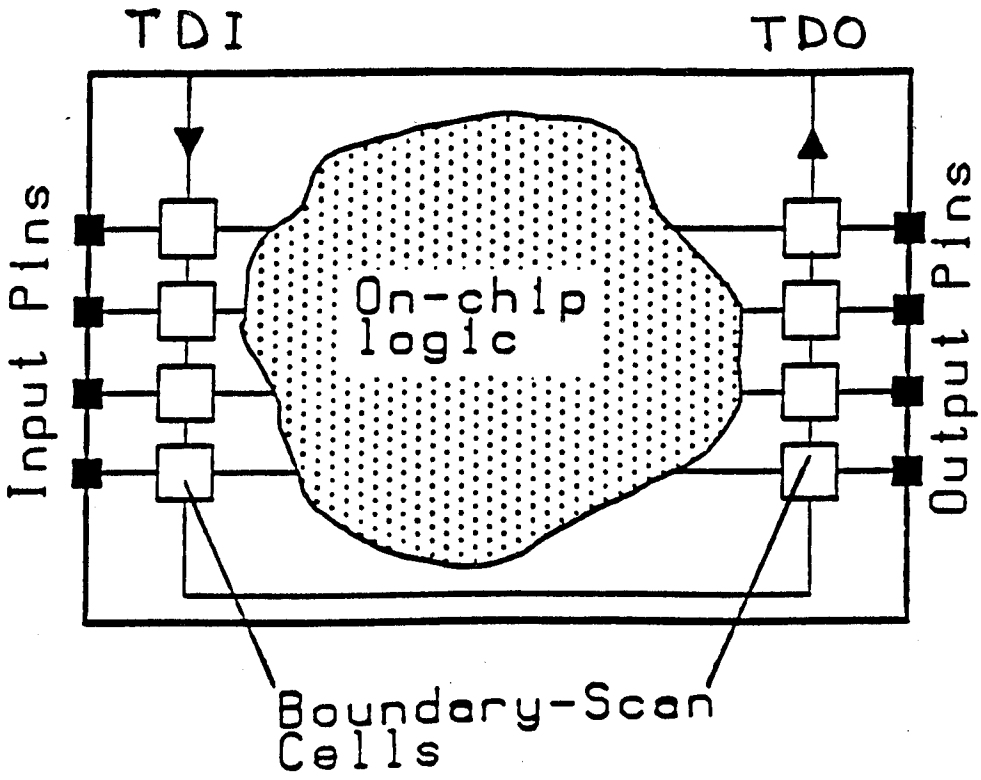
In scan mode, the intended (baseline) circuit function of the host is disabled on command, and a test mode selected for either testing the path integrity between chips or testing the internal logic connection integrity within the chip. In the normal signal mode, the intended circuit function is enabled and signal data goes directly through the scan test cell from SDI to SDO without any change or distortion, at least in principle. In contemporary IC scan designs, BS test cells are usually unilateral circuits, daisy chained to form a shift-register path around the perimeter or the boundary of the logic function to be tested. These cells contain clock controllable, serial data-in and serial data-out ports. To implement bilateral test cells, extra gates are required. A typical daisy chain is also shown in figure 2.

Boundary scan DFT at the board level is implemented much the same way as in a chip. Assuming that all the digital devices on the board have similar sequential logic functions, it is possible in a board level, scan design to connect them together in a daisy chain to form a block of combinational logic to be tested with one or more shift-register paths on the boundary of the card. The size of this block of logic so partitioned for scan can become substantial, and may add considerable costs and complexity to board level, design-for-testability.

At the board level, both test signals and functional signals can be controlled either by externally connected ATE or by an on-board chip. The latter serves as the bus master controller for the board by interfacing with the TAPs of all the chips on the same board, or with the adjacent bus masters on similar boards in an assembly. The scan modes available at chip-level TAPs can also apply to board-levels and higher indenture levels.

In the external scan test mode, TAP control bits to the muxes allow testing of interconnect wiring paths between IC packages. Three states of interconnect or external wiring fidelity are measured; stuck-low, stuck-high, and fault-free. Stuck-at states presently account for many latent defects, solder shorts, open traces, and wrong pin outs that occur in digital circuits. In the internal scan test mode, the scan cell muxes are set to allow testing of the logic circuitry internal to the IC package. With its own test clock usually running slower than the system clock and using a boundary path scan, internal logic circuitry can be tested as a combinational block. This is shown in figure 3. In the sample scan test mode, the muxes are set to allow the normal digital (functional) data to be sampled during its normal data throughput. This provides a built-in-test monitoring capability for an operating, functioning digital circuit.

At this point, it may be of interest to consider the real estate penalty typically associated with embedding a boundary scan architecture onto an IC. In one example [4], a TAP was to be implemented in CMOS for a 6mm x 6mm logic device. This TAP would require 16 bits for control, addressing, and testing. This word



TAP Controlled IC Boundary-Scan TEST

Figure 3

needed about 80 additional gates on the IC (i.e., assuming 5 gates per bit). The scan registers for the TAP required about 4 gates per IC data pin or, typically, about 160 gates per IC device (i.e., with 40 pins per IC package). Assuming that each additional gate occupies about .00375 square mm, which is fairly typical for a 2.0 micron technology, about 1 square mm is thus required to implement this particular TAP. This amounts to 3% overhead of available chip real estate. In another example [4] using a library-based, modified ASIC design, the overhead penalty for a comparable IC was estimated to be about 8%. In another example [4] that used an IC with an embedded scan path already present, the overhead penalty of embedding a BIST architecture was estimated between 17% for 12 square mm chips and 7% for 64 square mm chips.

The silicon gates required in the above scan cell designs are almost "free" in a semiconductor foundry processing sense (i.e., adding "more" transistors and diodes to a chip is still cheap). The effective penalty is that chip real estate devoted to the TAP embedded testability in no longer available to the functional designer. In either event, it would seem that this is a small price to pay to achieve the benefits of enhanced testability.

V. ELECTROMAGNETIC ENVIRONMENTAL EFFECTS

An important design factor in implementing test diagnostics with the IEEE 1149.1 standard for a test access port (TAP) is to consider the possible loading and coupling effects which may be attendant with embedding the host circuits or modules as such. TAP interfaces with embedded diagnostic circuit structures and test cells can adversely effect and degrade host performance when driven by EME signals. Embedded test circuits can change or alter the baseline performance and reliability of the functional circuits, and thus change the EME susceptibility of the host circuits for which the test diagnostics are designed to benefit. Thus, embedded testability must be design robust to offset the unintended and degrading consequences of BIST or TAP circuit loading due to electromagnetic environmental effects. Loading effects can cause unacceptable bit errors in the ADC portions of analog BIST sensors, amplifier distortion, sensor measurement errors, timing errors in the system and scan clocks, polling and ID errors in test scan architectures, increased noise floors in mixed mode IC devices, increased intermodulation and harmonic levels of distortion, bit errors in shift register latches, and cross talk induced distortion and phase errors.

To avoid the loading effects associated with embedded test diagnostics, we should seek testability designs and layouts that are uncoupled from host functions only until needed on "initiate scan" test cycle command. Test circuits should be orders of magnitude more reliable than the host circuits under test. Failure modes and processes of the embedded TAP or BIST circuits should be

statistically independent of the host circuits. Also, degrading electromagnetic effects in the baseline functional circuitry which may have been previously accounted for, may reappear in baseline designs that are modified for enhanced testability with added active or passive test circuits. Baseline susceptibility of functional circuits that are hosting scan test diagnostics should not be compromised nor degraded by embedding them with boundary scan or test cells which inadvertently enhance the IC susceptibility.

Advanced packaged MCMs with designs for testability [6] pose special problems for the EME designer. An MCM may be considered as a "stack" of multiple circuit layers or tiers containing trace and via connected IC chips, and interconnected electronically, mechanically, and thermally to form a compatible unit. Typically, IC are embedded into the MCM tiers which may be of conductive and dielectric thin films deposited on insulated substrates. The chips can be polyamide passivated and interconnected with aluminum metallizations. Integrating a cost effective test diagnostics design that uses boundary scan for enhanced testability is now rapidly becoming a major challenge to the MCM packaging industry.

Crowding more and more components into a smaller and smaller volume with higher and higher speed of operations in an MCM will most likely admit degraded susceptibility (to EME) through stray, uncompensated parasitic coupling. Design-for-testability [7] will add extra (boundary) scan test cells or circuits that may also degrade the susceptibility of the host circuits. TAPs on an MCM provide more added potential paths (i.e., scan path) for the EME

signals to enter, propagate on the MCM tiers, and couple into the victim circuits and devices. Since MCMs are certain to contain mixed-mode, digital and linear circuits [8], the susceptibility to attendant EME coupling is expected to be further aggravated.

Examples of unintended consequences of loading an original functional design and enhancing its overall susceptibility to EME are found in [9, 10]. Here, the functional designers intended to protect CMOS ICs from possible damage that is associated with electrostatic discharge (ESD). The more commonly accepted way of doing this is to embed an ESD protection circuit into the host ICs during the foundry build. ESD protection circuits are fast acting clamps tied to ground through the bias rails, and placed at the input gates of a potential semiconductor victim. The idea is to provide a fast acting path that can short or dissipate the excess nanojoules of energy in a static discharge. These buffer circuits are often fabricated with diffused resistors, avalanche diodes, and the gate inputs to the FETs to be ESD protected. Like boundary scan test cells, they too take up little silicon overhead but their presence can and do change the host circuit's susceptibility to rf induced EME.

In the above studies, it was found that certain wide band, impulsive rf waveforms cause ESD protected digital clock lines to upset with rf power thresholds in the range of +20 dBm to -40 dBm, for the frequency range of 10 MHz to 800 MHz where <u>without</u> the embedded ESD protection, it took almost +30 dBm to -20 dBm. So, here we see cases where the functional designer in attempting to design suitable protection against one kind of electrical stress

(i.e., ESD susceptibility) unintentionally created a new circuit susceptibility to another kind of stress (i.e., electromagnetic effects). In other words, providing ESD protection to CMOS devices actually made them more susceptible to (at least) impulsive EME waveforms by some 10-20 dB. The possibility of repeating this or similar response behavior in embedded TAP designs implemented in advanced packaged modules is a risk. It is prudent to investigate those possibilities now when TAP designs are still in the preliminary stages. One purpose of this effort is to help define that risk and to eventually resolve it with suitable mitigation.

VI. ADVANCED PACKAGING MODELING

Modeling and measuring EME susceptibility of multichip modules and their constituent IC chips are current initiatives in the Electromagnetic System Division of the Rome Laboratory. Of particular interest are advanced packaged MCMs and ICs that are embedded with boundary scan circuitry in test access ports and designed in accordance with IEEE Std. 1149.1. This effort focuses on the EME susceptibility of those ports, and assists Rome Laboratory's related investigations of EME in advanced packaged MCMs.

The objectives of this program are to investigate changes in circuit susceptibility to Electromagnetic Environmental Effects (EME), attendant with embedding test diagnostics as test access ports in multiport ICs and multichip modules (MCMs); and to identify CAD related, design concepts, rules, and caveats to mitigate those changes.

To further develop these goals, the following tasks were identified to help formulate an approach consistent with a viable methodology:

1. Evaluate commercial and military MCM design practices that currently use scan testability;
2. Investigate contemporary models of boundary scan (BS) test cells used to enhance IC and module testability;
3. Develop CAD models of baseline functions in an MCM, with and without boundary scan test structures and cells;
4. Define simulation procedures and methodology to determine changes in susceptibility due to added BS structures;

5. Determine model responses due to EME waveforms at any port on host MCMs and circuits during scan diagnostics;
6. Determine sensitivity to tolerance, accuracy, centering, layout, and identify enhancement opportunities; and,
7. Verify and validate EME modeling using an MCM beta site.

CAD software considered for these assessments included LIBRA, MICROWAVE SPICE, and PSPICE where the former two codes are frequency domain and the latter is time domain. Models for EME assessments must be both linear and nonlinear. Unfortunately, most device parameter data are usually not directly available in the open literature. Many baseline design parameters used in today's CAD are proprietary and empirically extracted in special tests and fixtures. The resultant data are design sensitive and zealously protected by manufacturers. Port performance data are often reported but it is very difficult to replicate the device baseline performance in CAD models without having active device and layout parameter values.

Reverse engineering baseline performance models is time consuming and involves a great deal of hit and miss "tweaking". This especially true for very high speed digital and microwave ICs where layouts and associated parasitics become important. Without detailed layout data and high frequency characterizations of the active devices in the baselines, modeling is handicapped. Simulating electromagnetic effects and associated interactions requires an acceptable baseline model be first devised, tested, and validated as representative of ICs and modules of the devices of interest. In this regard, a considerable effort was expended to

search and build a data base of MCM related information from the available literature. This effort was on-going throughout the contract and resulted in the very considerable bibliography which is contained elsewhere in this report. In addition, a glossary of MCM related terms is also provided to assist the reader with the specialized terminology of MCM, often tedious. Even though MCM technology is very fast moving, these collections should be useful, especially to new workers in the field.

Rome Laboratory performed EME measurements on various multichip modules. The susceptibility data indicated the MCMs exhibited low levels of upset due to cw rf on certain gates. These data compared favorably with data from the CAD models and methodology previously developed using PSPICE [11]. Measured MCM data provided good, preliminary benchmarks that helped refine our own approach to selecting an effective analysis methodology. The methodology selected and developed for this effort is based on using a PSPICE circuit simulator with supporting data to validate and verify predicted performance. The methodology used is as follows:

1. Model Normal Performance Baselines

   define simulation procedures
   dc and ac characterization data
   manufacturers' specifications
   extracted parameter data
   layout and schematic drawings

2. Validate Normal Performance Baselines

   run baseline model simulations
   compare with manufacturer's data
   compare with published data
   compare with Rome Lab data
   tweak baseline models into "conformance"

3. Model EM Effects' Sources

use simple Thevenin EM coupling
mixed Thevenin/Norton coupling
EM source waveforms; cw and modulations
modify baseline models with EM coupling
run simulations with EM source drivers

4. Compare EM Effects Performance

define assessment metrics and parameters
power thresholds of upset states
temporal thresholds of timing errors
noise, thermal, and sensitivity analyses
evaluate measured and simulated data

Both LIBRA and MICROWAVE SPICE codes are frequency domain circuit simulators and presented some special difficulties to modeling the hard nonlinearities typical of digital MCMs and some T/R modules. The problems we experienced were mainly getting those frequency domain codes to converge to a stable solution for hard nonlinearities, and even for moderately soft nonlinearities. Discussions with the software vendor reps proved of little help.

In addition, using realistic pulsed rf waveforms for offending environmental sources meant that the victim devices (and ports) would experience the nonlinear distortion modes only temporally; i.e., during the rf pulse duration plus any device and parasitics delay. Thus, it would require computing the total time duration a victim device sustains intermodulation, cross modulation, or gain compression (and expansion) modes of nonlinear distortion. This is very much a time domain problem, and an analysis approach that is based on using a frequency domain simulator is questionable from the onset.

In more recent (and related) Rome Lab efforts, PSPICE was used to simulate EME in MCMs and T/R modules. The measured data [12],

the modeling and simulation data [13], and the overall performance of PSPICE in all these cases were compelling. As a result, Rome Laboratory initiated a procurement action to obtain an on-site license for the PSPICE program. In the interim, and with the assistance of Rome Laboratory, we obtained an evaluation copy of PSPICE which has its same essential capabilities, with a smaller library in a graphics, limited version. The eval copy was tested and was used to help familiarize this author with its time domain capabilities. For example, we used the eval version to model a common electrostatic discharge (ESD) protection circuit, typically used in many of the digital circuits in MCMs. Modeling these and other circuits, and the simulation runs were straight forward.

As discussed previously, ESD protection circuits are very fast acting, Schottky (or avalanche) diodes that can clamp high level, and possibly damaging, bipolar transients to ground through the IC bias rails. They are normally placed between the chip bonding pads and the functional inputs to the gates of the particular FETs (or other ICs) that need to be ESD protected. When an ESD discharge impulse occurs, the fast acting Schottky diodes clamp the gate inputs to the bipolar dc rails, and thus short the ESD energy to ground through diffused (limiting) resistors in the chip substrate. In this way, logic gates which otherwise would be ESD vulnerable are internally protected and effectively buffered from the potentially lethal damage attendant with the ESD discharge event.

Previous studies [9] had shown that impulsive rf waveforms can cause ESD protected, clock lines to upset with reduced levels of rf power than are normally needed to upset those same clock lines when

they are ESD unprotected. Using an eval version of PSPICE, we developed a nonlinear model for the Schottky diodes by using data from the literature and tweaking other data for bias and voltage dependent, lumped elements which make up the equivalent diode capacitance and resistance. This model was developed using the PSPICE eval version and it was run on both MSDOS 386 and 486 PCs with no computational difficulty. The results confirmed previous data developed on the rf susceptibility of ESD protect buffers.

Another problem that was encountered during the TAP modeling was obtaining baseline data on the constituent circuits that make up a typical TAP. These parameter and layout data are necessary to model both the TAP circuits as well as their host functional circuits so TAP'd for scan testing. Rome Laboratory indicated that a good system candidate for an assessment of potential EME in an existing TAP'd machine is the RH32 microprocessor [14]. RH32 is a prototype 32 bit, fault tolerant, radiation hardened microprocessor developed for Rome Laboratory by the Space and Strategic Systems Operation of Honeywell Inc. It is a VHSIC class computer that executes ADA software for deep space and avionics applications where digital processing performance and reliability are paramount.

The RH32 chipset is composed of four separate, 352-lead SMT chips; a CPU, one each chip for instruction and data caches, and a floating point processor (FPP) chip which has an expansion capability to accommodate up to four more FPP coprocessors. These four chips are interconnected by processor data, instruction, memory, extended data, and test/maintenance busses. Each chip has

its own on-chip test monitor (OCM) and the CPU chip has an additional test interface unit (TIU). The OCMs on all four chips contain the IEEE 1149.1 TAPs of interest.

The data needed on these TAPs include schematic and layout drawings, extracted or specified parameters for transistors and diodes, CAD netlists, measured performance data, packaging data and related interface schema. The Rome Laboratory project office responsible for the RH32 program was contacted by us to discuss our intent and to solicit support in obtaining these needed data. Unfortunately, because of the scope of the data requested, the TAP data were not readily available. We did however receive an abundance of logic level, drawings and schematics in which it was very difficult to discern specific TAPs, test busses, and related interfaces in the chip set.

In addition, there was not too much useful reference to the actual OCM gates or test cell structures that are used to build or fabricate (implement) the TAPs, with actual active transistors and diodes identified as such in circuit schematics. The TAPs and related interfaces were identified only with logic level drawings that lacked circuit detail. It appears that the basic, detailed circuit designs of the TAPs and their associated interface test cells, may very well be proprietary to Honeywell. For example, the RH32 users manual makes a brief reference that the detailed circuit design of the TIU macrocell provided in the government version of RH32 was originally derived from a previous Honeywell TIU chip design built by Texas Instruments. This suggests RH32 proprietary data may not be available.

In developing a methodology for susceptibility analyses of advanced packaged multiport modules, it was found that most EME analyses assume an interfering voltage source to represent the environment is wire connected in series with the desired signal source at the same input port of the module. This is the same scalar susceptibility concept discussed earlier. A basic premise here is that the undesired signals in the MCM are resultants of electromagnetic fields that are "somehow" coupled to it from the electromagnetic environment. These exterior fields may have entered the system from either "front-door" or "back-door" ports. The former are the intended design ports of entry for intended signals; the latter are unintended ports such as rf leaky seams, shields, apertures, holes, access panels, windows, doors, and canopies in the skin surface. Once inside the platform, these external environmental fields combine with the internal environmental fields present, and couple to the avionics suite through bays, bulkheads, racks, cabinets, cabling trays, packaging, wire bundles, traces, etc. These unintended, (exterior) field dependent signals thus travel on complicated internal paths within the platform (and which may be considered conceptually as internal "transfer functions", some very likely nonlinear) to eventually arrive at the accessible ports of the victim modules and, subsequently, at the ports of the victim IC devices.

The randomness of the magnitudes, phases, and polarizations of these net resultant fields incident at the module port as well as random orientation of the module port itself, suggest that capacitive and inductive coupling modes into the victim port are

both viable means of invasive rf. Thus, some kind of voltage spectrum is assumed to be the net resultant signal at the victim port that is "induced somehow" from an exterior environmental field incident on the avionics platform. A natural question for the EME analyst is why use a voltage source to represent this EM field and, why connect it in series with a desired signal source? With both capacitative and inductive coupling of these offending environmental fields to victim ports, both current sources and voltage sources in different connection topologies, should be also admissible to the repertoire of equivalent EME drivers.

Source modeling is related to the methodology considered and was further pursued in discussions with EM fields' experts at Rome Laboratory. The consensus is that given capacitive and inductive coupling from exterior fields, both voltage and current sources should be considered. This suggests Thevenin and Norton, field dependent sources in series and parallel, respectively. A more general question might be posed: what are admissible shapes and geometry of a coupling aperture or scatterer that when driven by an incident EM wave, give rise to Thevenin voltage or Norton current sources on some "victim" wire located behind the aperture or the scatterer? The victim wire may represent a transmission line or an IC chip trace that carry a functional, baseline signal that will be combined and mixed with the equivalent of a signal "source" coupled from the exterior. This remains an interesting issue from both the modeling and measurements points of view, as well as from circuits and fields points of view. Solutions to this "inverse" fields problem or circuit synthesis problem, depending on view point,

could provide some useful insight into viable coupling shapes and scatters. Approximate solutions and modeling could add some practical credence to using mixed, voltage and current sources as models of unwanted circuit drivers induced from the environmental electromagnetic fields.

VII. CONCLUSIONS AND RECOMMENDATIONS

This effort was an investigation of electromagnetic effects in boundary scan and other scan test structures embedded as test access ports (TAP) in host ICs and MCMs. The test access ports and test scan structures considered are those used in advanced packaged, ICs and MCMs. The effort addresses the susceptibility issues of how and to what extent does embedding the boundary scan test circuits in TAPs on an MCM, effect or degrade the module susceptibility to electromagnetic environmental stresses.

The results obtained to date do not provide sufficient data to fully answer the issues raised, although some data do suggest that some ICs - i.e., line drivers, line decoders, enable gates, and D-type flip-flops, exhibit unacceptable EME susceptibility. Rather, the effort served well by articulating the problem, developing an approach, defining a simulation methodology, and identifying parameter data needed to accomplish an assessment of TAP susceptibility. In addition, the effort provided assistance and counsel to other related, on-going efforts at Rome Laboratory. Several technical papers were prepared and delivered during the course of this contract. Also, the literature search performed during this effort developed into an extensive bibliography of MCM related technology. In this regard, the very capable staff of the Technical Library at Rome Lab provided very helpful assistance. A glossary of terms and acronyms was also developed that specialized to MCM and electromagnetic environmental effects (EME) terminologies. In a technology area fast growing rich in acronyms, its best use is probably for the newer technologists to the field,

although the seasoned may also find it a useful refresher.

While limited in MCM simulation data, this effort was able to develop and support some reasonable conclusions:

- Computer aided EME assessments should be done concurrent with functional CAD to find, identify, characterize, and design fixes for any EME related problems.

- Computer aided EME assessments of MCMs should also be done concurrent with functional CAD to provide the (functional) design parameter data needed for the EME baseline modeling.

- Computer aided EME assessments should be done concurrent with functional CAD to provide independent test, verifications and validation of the baseline functional designs.

- EME susceptibility of MCMs should be characterized early in the functional design phase in order to design and implement appropriate mitigation fixes, rules, algorithms, or caveats.

- EME assessments of advanced packaged modules which conform to IEEE Std. 1149.1 should comply with Air Force requirements for <u>both</u> module testability and rf (EME) assurance.

- Modeling MCMs requires data on circuit parameters, layouts, materials, and structure, etc.: formalized ways to obtain these data should be defined and adopted into the Air Force procurement and logistics processes.

- As the technology of advanced packaged modules expands and its literature grows accordingly, a design and analysis database of EME in MCM should be assembled and updated concurrently.

- More work is recommended to investigate MCM susceptibility to EME: i.e., experimentation and simulation of the electromagnetic

environmental sources (and related coupling topologies) for use in contemporary circuit simulators should be vigorously pursued.

This report presents the results of an investigation of electromagnetic effects in test structures embedded in ICs and MCMs as test access ports (TAP). TAPS are used in contemporary ICs and in many advanced packaged MCMs to enhance their testability. Specifically, this effort defined and examined the susceptibility issues of how, where, and to what extent does embedding boundary scan, test circuits as TAPs on an MCM affect, change or degrade - if at all - the latent susceptibilities of its host linear and digital circuits to the electromagnetic environmental stresses.

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X. GLOSSARY OF MULTICHIP MODULE RELATED TERMS

ADAPTIVE DIAGNOSTICS A methodology of diagnostics wherein the strategies used for test generation, control, and observability will change and adapt to observed patterns in the resulting test data, in order to minimize the total test time and cost.

ADMISSIBLE PORT Any port or discrete pin pair on an MCM or its constituent circuits which permits entry of electromagnetic energy when operating in its intended environment.

ANALOG (OR LINEAR) An attribute of a circuit or module that describes a continuum of time and waveform levels necessary to perform its circuit function.

ATE Automatic test equipment.

ATS Automatic test system.

BASELINE The final status of a design or product as intended by the designer that performs in compliance with the specification.

BASELINE PERFORMANCE The set of measured or specified parameters that describe or characterize the normally intended operation of an item within its "designed-to" performance envelope: validated design performance of an item.

BED-OF-NAILS TESTER A planar array of spring loaded pins that make pressure and electrical contacts with the IC chip pins: an array of tester probes for isolating and controlling input test vectors, and detecting the subsequent test responses.

BISC Built-in-self-check is a design feature where an item under test has capabilities embedded to verify its logic states during operation.

BIST Built-in-self-test is a design feature where an item under test has capabilities embedded to do its own complete diagnostic testing.

BIT Built-in-test; a design feature where an item under test has some capabilities embedded to do its own testing or checking.

BS A boundary scan implementation for test diagnostics in which all the gates of the IC or module under test are interconnected together to form a daisy chain shift register: controllability and observability are provide by embedding extra gates or test cells near or around the IC or module pins (hence a "boundary").

BUS-STRUCTURED ARCHITECTURE A way of logically partitioning the functions of a logic system by interconnecting the functions with bidirectional paths for common data exchange: common busses are data, address and control.

C3 Abbreviation for Command, Control, and Communications assets and tactics; usually in a military sense.

C4 See C3 with additional Computer assets and tactics.

C3I See C3 with additional Intelligence assets and tactics.

CND Means a "cannot duplicate" fault condition of a component that fails in service but does not fail during simulated test: a transient (or "intermittent") fault event observed in a field operation that cannot be repeated in a maintenance environment.

CONTROLLABILITY An attribute of testing in which the unknown initial state of a CUT can be easily set to a desired state consistent with the test to be performed: ability to set all the initial conditions to some known vectors prior to testing.

COUPLED NOISE Unwanted electromagnetic interactions between signal lines close enough for capacitive or magnetic coupling effects to occur: signal lines themselves may carry unintended, extraneous environmental signals in addition to the desired ones.

CTE Coefficient of thermal expansion: a critical factor in determining heat generated stresses in polymer dielectrics and other structures in multilayer MCMs.

CULTURE A currently popular term used to describe a condition where many pragmatic procedures (i.e., accepted methods of the technology business) have become so widely used, accepted, and unquestioned (!) that they have become ingrained into the social, contemporary mindset.

CUT Circuit under test.

DAISY CHAIN A shift-register mode of testing in which all scan test flip-flops of an IC under test are effectively connected together in a serial chain and which can sequentially shift out arbitrary test patterns previously loaded and stored in the FFs.

AD HOC DESIGN-FOR-TEST Methods and testability designs for a specific and particular, local circuit function and which are generally not applicable nor portable to other designs.

DEGATING LOGIC Added logic gates on a chip to disable or disconnect one portion of the logic under test from another portion.

DELTA-I NOISE Wide band, switching noise spectra generated in equivalent inductive elements of digital circuits and modules by high speed, current switching transients.

DELTA-V NOISE Wide band, switching noise spectra generated in equivalent capacitive elements of digital circuits and modules by high speed, voltage switching transients.

DFR Design for (product) reliability is an up front, rigorous design process for achieving and validating specific reliability goals with specific fabrication and packaging technologies.

DFT Design-for-test is rigorous, structured process of achieving an optimal, cost effective degree of product testability.

DIAGNOSTIC TESTING Methodology and assets of testing needed to interrupt, detect, localize, record and correct performance faults or defects as parameter departures from the functional baselines.

DIGITAL An attribute of a circuit or module that describes a finite set of discrete time and discrete waveform levels (usually binary) which are necessary to perform its logic function.

DISTRIBUTED TESTING An approach to embedded testing that puts the test cells needed for generation, control, observability as close as possible to cover a maximum number of test nodes.

E3 or ELECTROMAGNETIC ENVIRONMENTAL EFFECTS The functional performance, degradation and failure responses from an operating circuit or system when it is exposed to EM environments that are outside of and extraneous to the intended design envelope.

EM Electromagnetic; usually with "fields".

EM SUSCEPTIBILITY Spectral functions or measured data that describe threshold levels and frequencies of an operating port which if exceeded by extraneous signal spectra from the EM environment will cause interference (EMI) effects at the same or other port: acceptable performance is usually restored when the offending environmental sources are removed.

EMC ASSURANCE A measure of user confidence that a product meets stated (EMI) safety margins for performance, or is in compliance with stated standards and regulations, achieved by intrinsic design and validated by formal test.

EMC Electromagnetic compatibility is the quantitative assurance that a system or circuit operating in its intended electromagnetic environment, performs as intended without causing or itself being a victim to electromagnetic interference.

EME Electromagnetic environment is set of spectral, temporal, and spatial characterizations of electromagnetic energy and power fields that normally surround and permeate the vicinity of an operating system or circuit: sources of EM environments can be system internal or external, intended or unintended, friendly or unfriendly emitters of electromagnetic energy.

EMI Electromagnetic interference is the response or effects of extraneous EM energy from any unintentional source(s) that cause any an unacceptable but recoverable response, degradation, upset, or malfunction in an operating system or circuit.

EUT Equipment under test.

FLOPS Floating point operations per second is a common metric to describe the speed on a digital processor: often with M for Mega (10^6) or G for Giga (10^9).

FUNCTIONAL TESTING The test methodology and assets needed to determine that an item performs to the design baselines in its intended environment as the designer intended.

GE-HDI General Electric High density Interconnect process is a proprietary process for interconnecting bare IC chips by imbedding and bonding them into a ceramic substrate.

GIMADS Generic Integrated Maintenance And Diagnostics System is a government initiative which attempts to combine innovative design-for-test with integrated logistical support.

GOLD CIRCUIT A reference circuit whose functional "goodness" has been previously established and which is used as the acceptance benchmark for comparative performance testing: response vectors from testing "gold circuits" are, by definition, always "correct" for any valid input test vector.

ID Integrated, or integrating diagnostics are loose terms that encompasses all technologies and components which are required to build, field, support and operate a modern system.

IMOD Intermodulation is a waveform distortion, nonlinear effect due to an electromagnetic environment in which the rf carrier of an interferer mixes with the desired signal; a scalar effect with both waveforms at the intended input port of the victim.

IN-CIRCUIT TESTING Another way of saying embedded diagnostics where each chip in a module or on a board is testably isolated and independent from the other ICs that happen to be present in the same module or on the same board: chips not under test are either disabled or are set to some known states.

INFORMATION AUTHORITY The administrative level in a maintenance structure that temporarily has the most test information about a system or product at any given time is the "authority".

IPD Integrated product development.

LEVEL-SENSITIVE A digital circuit is level-sensitive when its steady state response to valid input state changes is independent of any internal circuit delays: steady state response is the final state or values of all logic gate outputs after all change activity has terminated.

LEVELS OF INDENTURE A term to indicate that something can be subdivided into smaller pieces which themselves are again further divisible, etc. The use context of indenture comes from paragraph indenting commonly done in technical style writing.

LEVERAGING Another term that refers to a multifold increase in magnitude of some attribute, parameter, or capability of a system because of a minor change in another: military people may call it a "force multiplier" where capability to deploy only a few smart weapon systems is considered to match or outnumber a numerically superior but dumber (i.e. not similarly equipped with smart weapons) enemy force.

LRM Line repairable module.

LRU Line repairable unit, or sometimes "least" meaning one level above throw away.

MAINTENANCE LEVELS Air Force maintenance usually denoted "O" (organizational), "I" (Intermediate), or "D" (depot): O-level is on-base, I-level in-theater, and D-level Air Logistics Centers.

MCM A Multichip module is usually made up of insulating tiers of passivated substrates which contain the chip devices; IC devices in the tiers are interconnected in wiring planes and the tiers are usually interconnected vertically at edges and vias.

MCM FUNCTIONS It is generally agreed that the purpose of MCM packaging is to provide a stable and cost effective, protective environment for high density, high speed IC chips and components to perform reliably and with electromagnetic immunity.

MCM-L, -D, -C, -P (etc) Multichip modules fabricated with an L, D, C, P, and etc. technologies where L is a laminated, board-like technology in which chips are bonded by flip-chip, TAB, or wire; D is deposited thin film technology that uses polymers and metal to interconnect prepackaged chips; C is the silk screen, printed ceramic, thick film technology to interconnect the chips; P is a form of lamination process that uses plastic, quad packaged chips mounted on molded compounds and lead frames.

MCM-XY A generic multichip module fabricated with combinations of different technologies identified in MCM-L...P; i.e., MCM-DC.

MIPS Million instructions per second or 10^6/[(cycle time in sec) multiplied by (cycles per instruction)]; a speed quality factor for a digital processor.

MUT Module under test.

PACKAGING EFFICIENCY A measure of the chip density in a given MCM to achieve its specific function: packaging efficiency is a ratio of the total area for active silicon or GaAs, etc., to the total active area of MCM packaging.

PACKAGING A generic, inclusive term to describe the technologies and processes of interconnecting, powering, cooling, handling, and protecting semiconductor chips.

PARADIGM A popular term used extensively in the test business to denote an exceptionally clear or typical example of how similar things compare to each other: also, an original pattern or model representation from which similar copies are made.

PORT Any aperture, intended or otherwise in a device, module, or circuit through which electromagnetic energy can pass; i.e., for discrete conductors or wires, a port is a wire pair in which the current in one wire equals the current out of the other; for microwave waveguides, a port may be simply a hole or slot.

PROGNOSTIC MAINTENANCE A maintenance methodology in which otherwise good components are selectively replaced on a suitable time scale based on predictions of their expected failure.

RETOK Retest OKs is a transient (or "intermittent") fault event observed in field operation that passes retest OK in a benign lab or maintenance environment.

RISC Reduced instruction set for computing; a programming method of achieving higher processing speeds in a digital computer.

SCALAR SUSCEPTIBILITY Undesired responses at any admissible port of an MCM caused by an unintended electromagnetic source that is "wire" connected or "field coupled" into the same port.

SCAN DESIGN A design capability to generate, input, and shift arbitrary test bit patterns into and out of sequential circuits, and to observe all the subsequent states in the output response.

SILICON OVERHEAD The chip real estate needed to accommodate the extra gates or cells for embedded test diagnostics: technology sensitive; i.e., four to six gates per IC pin which for VLSI is about 10-15% of contemporary chip designs.

SRU Subassembly repair unit.

STRUCTURED DESIGN-FOR-TEST Generic methods and testability designs for solving the testability problem for a global class of functional circuits.

STUCK-AT-ZERO or STUCK-AT-ONE A binary fault coverage common in digital circuitry where a wire or pin goes to its intended logic level on command, but remains there when not intended.

SUT System under test (see XUT).

TAB Tape automated bonding is a method of handling and mounting prepackaged semiconductor chips onto MCM substrates.

TEST VERTICALITY In any given architecture, diagnostic testing which flows on paths that go up or down the system hierarchy.

TESTABILITY A quantitative measure or metric of how easily tests are performed or how cost-effective it is to perform testing.

TM Test maintenance; usually with built-in test busses.

TSMD Time Stress Measurement Device developed by Rome Laboratory that provides a temporal profile (data) of selected environmental stress levels on an electronic part during its operating history.

ULSI Ultra large scale integration: a chip fabrication process where feature size is typically submicron (< 0.5 micron).

UNACCEPTABLE RESPONSE An interference response of a system or circuit at a specified port that is user defined as critical, where a performance parameter is caused to deviate from or be outside its desired specification or design envelope.

UUT Unit under test (see XUT).

VALIDATION Empirical and analytical demonstrations that show the design of an item meets its intended performance requirements or specs: intended performance requirements or specs are the design baselines achieved by the designer - design validation confirms its compliance with requirements.

VALUE ADDED Incremental increases in value of a product as it passes through successful levels of test: each additional level or indenture of testing adds its own testing costs to the total accumulated value of the unit.

VALUE ROLL-UP See Value added.

VAPORWARE As used in the same context of hardware, software, or firmware, "vaporware" refers to a kind of fictional "ware" that only exists in the spoken words used to describe it.

VECTOR SUSCEPTIBILITY Undesired responses at any admissible port of a multiport MCM caused by an unintended electromagnetic source that is "wire" connected or "field coupled" into the same port or into any other port on the victim MCM.

VERIFICATION Empirical and analytical demonstrations that show the given design of an item was realized or fabricated without assembly errors: design verification confirms its compliance with parts assembly.

VLSI Very large scale integration: a chip fabrication process where feature size is typically less than 1 micron.

VULNERABILITY The characteristics of a system or circuit in a specific EM environment where port susceptibility levels are exceeded to levels that cause unrecoverable damage.

WALKING PATTERN A simple test vector that is made up of an alternating sequence of ones and zeros which are shifting into and out of a boundary scan, shift register: often used in scan testing of digital ICs in a sequential machine by making the machine under test essentially combinational.

WSI Wafer scale integration is the fabrication process of implementing and packaging circuit functions on entire wafers without dicing into chips.

XMOD Cross Modulation is a waveform distortion, nonlinear effect due to an electromagnetic environment in which modulation on an interferer signal mixes with the desired signal; a scalar effect with both waveforms at the intended input port of the victim.

XUT Generic item "X under test" where X = Circuit, Unit, Module, Equipment, System, Device, or any other test article.

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OF

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