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Defects and Impurities in 4H- and 6H-SiC Homoepitaxial Layers: Identification, Origin, Effect on Properties of Ohmic Contacts and Insulating Layers and Reduction

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13. ABSTRACT ***(Maximum 200 words)***

A CVD system is being fabricated for growth of 4H- and 6H- SiC homoepitaxial thin films. Most system components have been received. The design incorporates a load lock on which the growth and RHEED chambers are attached. The diffusion lengths of the minority carriers in n- and p-type 4H-SiC and 6H-SiC and their variation with T were measured using SEM in the EBIC mode and a Schottky barrier diode structure composed of Ti/Al contacts. The diffusion length for holes (L_p) was ≈0.4 mm in n-type 6H-SiC and L_n was ≈1.2 mm in p-type 6H-SiC. L_n in p-type 4H-SiC was 1.4 mm and L_p was 0.6 mm in n-type 4H-SiC. Thin layers (2–8 Å) of Pt ohmic contact material were deposited on p-type 6H-SiC(0001) surfaces which had and had not been exposed to H. Photoemission measurements indicated the presence of a downward band bending at the surfaces of both samples. Preliminary calculations indicate that the Schottky barrier height of Pt on the H-treated sample was substantially less than that on the non-H-treated sample. A mask set has been designed and received to fabricate MOS capacitors and MOS gated diodes for characterization of the SiO_2-SiC interface. Initial experiments indicate that the fabrication steps conform to the requirements of the device process, and the process has been started.

14. SUBJECT TERMS
chemical vapor deposition, CVD, 4H-SiC, 6H-SiC, homoepitaxy, thin films, growth system, diffusion lengths, minority carriers, ohmic contacts, Pt, photo-emission, MOS capacitors, MOS gated diodes, SiO_2-SiC interface

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I. Introduction

The two most important materials-related problems affecting the performance of all SiC devices and their associated components (e.g., contacts) are the defects and the undesired impurities which become incorporated in the homoepitaxial SiC layers in which all devices are currently fabricated. Bhatnagar [1] has shown that the reverse blocking leakage current in high voltage Schottky diodes is three orders of magnitude higher than theoretically predicted as a result of defects in the epi-layer. The formation of micropipes, stepped screw dislocations, interacting dislocation loops, polyganized networks of dislocations and growth twins as well as stacking faults during the sublimation growth of SiC boules are likely the root cause of some of the defects in the epitaxial layer. However, with the exception of the micropipes, the types and concentrations of line, planar and other three-dimensional defects and their effect on the performance of devices and individual device components in the important epi-layer have not been similarly determined. As such, it is not known which of the latter defects actually are translated from the wafer into the epi-layer during its deposition and, therefore, should be vigorously controlled during boule growth and which defects are generated during deposition.

The relatively uncontrolled occurrence of the n-type donor of N and deep level compensating impurities such as Ti in the epilayer have been identified via secondary ion mass spectrometry, photoluminescence and cathodoluminescence investigations. However, the origins of essentially all of these impurities are unknown. For high-temperature, -power and -frequency devices, it is highly desirable to control or eliminate these impurities such as to attain undoped films with uncompensated carrier concentrations of 10^{14} cm^{-3}—two orders of magnitude lower than what is, at present, normally achieved in standard commercial depositions.

The formation of low resistivity and thermally stable ohmic contacts to 4H- and 6H-SiC remains a serious problem in the development of SiC device technology. For SiC power devices to have an advantage over Si, the contact resistivities must be below 1×10^{-5} Ω-cm^2, as noted by Alok, *et al.* [2]. In addition, the electrical characterization of state-of-the-art SiC films depends on the ability to fabricate ohmic contacts on material with low carrier concentrations. Therefore, better ohmic contacts are needed both for improving device performance and for improving the quality of films which can be grown. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which have traditionally relied on low melting point Al or Al alloys to dope the SiC surface below the contacts. These materials are not suitable for devices intended for high-temperature operation. While the fabrication of ohmic contacts to SiC has also normally depended on the attainment of a very heavily-doped near-surface region, the introduction during deposition of high levels of dopants in the near surface device region of the epi-layer prior to the deposition of the contact or by ion implantation through the contact makes probable the introduction of point and line defects as a result of the induced strain in the lattice.

Based on all of these issues and recent experiments already performed at NCSU, our goals are to produce contacts which are thermally stable and have low contact resistivities while also reducing the need for doping by ion implantation.

To fabricate most microelectronic devices, the growth or deposition of stable insulators is needed to provide both passivating layers and gate dielectrics. Silicon carbide is almost invariably thermally oxidized, albeit at a slower rate, in the same manner and temperature range that is employed for Si. Most of the previous studies regarding the oxidation of SiC have been concerned with polycrystalline materials. It has been shown by Harris and Call [3] and Suzuki, *et al.* [4] that the (0001) face of 6H-SiC oxidizes according to the same linear-parabolic equation reported for Si by Deal and Grove [5]. The model states that the initial stage of oxidation is reaction rate limited and linear, but becomes parabolic as the diffusion of the oxidant through the oxide becomes the rate limiting factor. Research at NCSU by Palmour *et al.* [6] has demonstrated that the oxidation process on SiC in wet and dry oxygen and wet argon obeys the linear-parabolic law. Both wet processes had a slower rate than dry oxidation at 1050°C and below. The dry oxides exhibited a very flat surface; in contrast, SEM and TEM revealed that wet oxidation preferentially oxidizes dislocation bands, causing raised lines on the oxide and corresponding grooves in the SiC. It was proposed that the much higher solubility of H_2O in SiO_2 as compared to that of O_2 allows wet oxidation to be preferential.

All of the oxidation studies on all polytypes of semiconductor quality SiC have been conducted on n-type material with the exception of the investigation by Palmour *et al.* [6]. The objective of this study was the determination of the redistribution of the common electrical dopants of N, P, Al and B during thermal oxidation of SiC films at 1200°C in dry O_2. Experimental segregation coefficients and interfacial concentration ratios were determined. Secondary ion mass spectrometry revealed that B and Al depleted from the SiC into the growing oxide while N and P were found to pile up in the SiC as a result of the loss of the SiC to the oxide formation. Aluminum is now used almost universally as the p-type dopant in SiC. The electrical properties of oxides thermally grown on n-type SiC normally have reasonably favorable characteristics of high breakdown voltage and low leakage currents. However, the reverse is true for thermally grown oxides on p-type SiC, as shown by Baliga and his students at NCSU. It is believed that at least two of the causes of the poor performance on a p-type material are the existence of the Al in the oxide and at the oxide/SiC interface and the dangling oxygen bonds which this species creates in the oxide as a result of a difference in oxidation state (+3) compared to that of Si (+4) and the existence of C at the SiC/insulator interface. Methods of effectively cleaning SiC surfaces prior to oxidation to deposit and grow oxides on p-type material under UHV conditions and determine the effect of Al redistribution and C concentrations at the interface on the properties of the oxide must be determined. In addition,

the effect of existing line and planar defects in the SiC epi-layer on the properties of the thermally grown and deposited oxide must be ascertained.

The research conducted in this reporting period and described in the following sections has been concerned with (1) design of a new CVD SiC system for the deposition of 6H- and 4H-SiC films, (2) measurements of diffusion lengths and calculations of carrier lifetimes of holes and electrons in n- and p-type 6H- and 4H-SiC, (3) effects of prior exposure of p-type 6-H SiC(0001) surfaces to atomic H on the Schottky barrier height of Pt thin layers, and (4) the design and receipt of a mask set to fabricate metal oxide capacitors and metal oxide-semiconductor gated diodes for determination of the interface electrical properties between insulators and SiC. The following individual sections detail the procedures, results, discussions of these results, conclusions and plans for future research. Each subsection is self-contained with its own figures, tables and references.

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II. Growth of 4H- and 6H-SiC Homoepitaxial Thin Films

A. Introduction

A silicon carbide system is being designed and built in order to grow silicon carbide thin films of high quality. At present, the necessary components for the proposed system are being obtained. The design is being modified as suggestions are received for optimizing the process.

B. Experimental Procedure

The system design will comprise a six-way cross serving as the loadlock from which two separate chambers are attached. Off this loadlock, to one side, will be the growth chamber. To another side, perpendicular to the axis of the loadlock and growth chamber, will be the second chamber where RHEED (reflection high-energy electron diffraction) analysis will be performed. The sample will be transferred to and from the various chambers on a SiC-coated graphite susceptor platform. The transfer mechanism will consist of a platform which will move from chamber to chamber by means of a manipulator rod. The manipulator rod will be screwed to the side of the susceptor.

The growth chamber will consist of a rotating module to which the susceptor is placed. Growth will occur on the sample in an upside-down position, with gases flowing upward, while the susceptor is being rotated. The susceptor will be attached to the rotating rod assembly from the groove into which the susceptor slides when sample transfer takes place. The sample will be transferred to the rotating rod. The rod will then be brought down to the quartz portion of the sample, located below the area where the sample was transferred into the growth chamber. Here, the sample will be heated by an RF coil. Gases will be introduced from the bottom of the reactor. Growth temperature will be monitored by means of a standing pyrometer mounted outside the quartz chamber and aimed at the sample. Growth processes, such as gas flow rate and pressure, will be monitored by electronic components. Gas flow will be controlled by mass flow controllers and pressure by capacitance manometers.

The RHEED chamber will monitor film crystallinity, crystal structure and the formation of new surfaces. Since growth of high-quality crystalline SiC films will be attempted, the RHEED chamber will be useful to characterize the film. The RHEED chamber will be attached to a nominal high vacuum to prevent direct exposure to atmosphere after growth. The SiC growth process will consist of introducing SiH_4 and C_2H_4 as the reactive components carried by a H_2 carrier. Nominal flow values will be on the order of 1 to 10 sccm for each. Carrier flows of H_2 will be on the order of 3 liters per minute. Other gases which will be included on the system will be NH_3 and an N_2/H_2 mixture for doping, and Ar. Also used for doping will be TEA which will be kept at constant temperature by a heater bath.

C. Results

To date, a design has been developed where sample transfer, growth, and RHEED analysis have been determined. Some of the major components have been received, see Table I.

Table I. List of Components Received for SiC System

Vendor	Component
MKS	(2) 1000 Torr Baratrons (2) 10 Torr Baratrons 937 gauge system (2) 660 single channel gauges 640 integral pressure controller (2) cold cathode gauges throttle valve throttle valve controller 647 8-channel MFC controller various cables
Unit	(6) metal sealed MFC's
Cross	100 ft stainless steel tubing
Air Products	50g TEA, adduct grade
Fisher	(1) heating/cooling bath for TEA
A&N	(2) 6-way crosses, various flanges and parts
Balzers	(1) TMH 064 pump
Matheson	(1) Gas cabinet
Raleigh Valve	various valves

Items currently in progress are:

(1) A frame has been designed and is being built to provide structural support to the system;
(2) A quartz chamber-to-cross assembly is currently being machined which will provide a sealed interface between two parts of the growth chamber;
(3) Flange parts are currently on order to hold the pressure gauges and pump connections,
(4) An RF generator is in the process of being refurbished to be used to provide RF heating to the susceptor.

D. Discussion

The proposed design was developed with many sources of input. A number of constraints determined the design configuration and materials used in the system.

One of the main concerns was the high operating temperature of the growth chamber. Since temperatures around 1600-1700°C will be used to grow SiC thin films, it was determined that

quartz would be the best material for the growth portion of the chamber. A double-walled quartz vessel, water cooled around the perimeter, was determined to be the optimum mode of cooling the chamber.

Another concern was the transfer mechanism of the susceptor and the placement of samples on the susceptor surface. It was decided that small silicon carbide screws would be the most flexible for the purpose of accommodating various sample sizes. For the transfer mechanism, a simple tongue-in-groove assembly was deemed simplest and most practical. It will be moved between chambers by means of a transfer arm which will be screwed into the side of the susceptor.

E. Conclusions and Future Research Plans and Goals

A design to deposit SiC thin films has been developed. Various components have been received and others are being ordered at this time. Some parts are currently being machined. Building of the system will begin when necessary components are received.

III. Measurement of Minority Carrier Diffusion Length in Silicon Carbide

A. Introduction

Diffusion lengths (L) and lifetimes (τ) of charge carriers in a semiconductor determine many important characteristics of the devices under operation. Although silicon carbide has emerged as a highly successful candidate for high temperature, high power and high frequency applications [1], there has been very little literature available on diffusion lengths and lifetimes in SiC and particularly on variation of these parameters with temperature. A. M. Strel'chuk [2] reported τ and L values for 6H-SiC and their variation with temperature. However, diffusion lengths in this work were calculated using the photocurrent method. The disadvantage of using light source for generating carriers is the poor resolution of such a technique, especially while dealing with very small diffusion lengths as is the case in SiC. In this work, the use of the Electron Beam Induced Current (EBIC) technique for determining the minority carrier lifetimes in two polytypes of SiC (4H- and 6H-SiC) for both n- and p-type material is reported. One of the configurations for the determination of the bulk minority carrier diffusion length in a semiconductor using EBIC is shown in Fig. 1 [3,4]. It utilizes an electron beam incident on the semiconductor surface adjacent to a current collecting Schottky barrier. The planar configuration can also be used for imaging defects. It enables a direct correlation to be made between the characteristics of defects and material parameters.

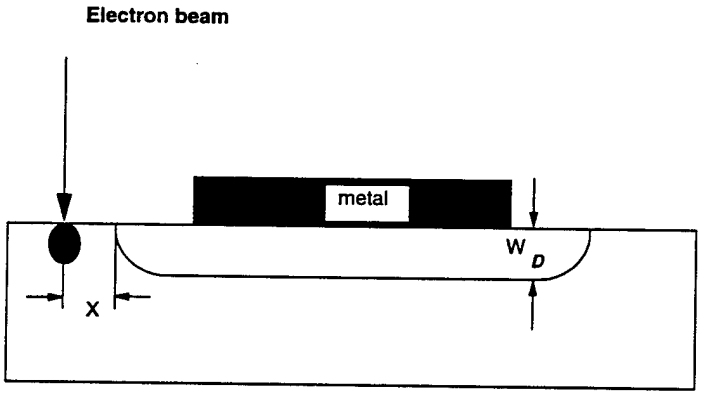

Figure 1. Planar configuration of the Schottky diodes used for measurement.

Advantages of EBIC. One of the primary advantages of EBIC is its high resolution which is determined by the radius of the generation volume [3] in the semiconductor created by the incident electron beam (~ 0.05 μm). Secondly, this technique is simple and requires no high

temperature processing as sample preparation consists only of Schottky barrier metal deposition, thereby allowing characterization the material without altering its properties.

Methodology. Carriers generated by the electron beam of the SEM in the vicinity of the junction diffuse to the depletion region where they are collected and consequently induce a current in an external circuit. EBIC variation with distance should follow the diffusion equation including the effect of surface recombination velocity (v_s):

$$I=I_0 \, x^{-\alpha} \exp(-x/L) \; ; \quad \text{where } \alpha = 0 \text{ for } v_s = 0 \text{ and } \alpha = 3/2 \text{ for } v_s = \infty.$$

Hence, the inverse of the slope of a plot of ln(I/Io) versus x should give the diffusion length after accounting for α.

B. Experimental Setup

The setup used for the measurement of diffusion length is shown in Fig. 2. The electron beam is scanned along the desired region on the surface, such that the point of approach is at least two diffusion lengths away from the depletion edge. The direction of approach must be perpendicular to the edge of the depletion region. The scanning circuit in the microscope controlling the rastering of the electron beam is used to trigger the oscilloscope as shown. Carriers are generated by the incident electron beam and these carriers diffuse to the depletion region. This current is collected, amplified and outputted by the EBIC amplifier to the oscilloscope where a plot of EBIC current vs. the time is obtained. The oscilloscope is interfaced to the PC through a GPIB card and, hence, the data from the oscilloscope can be downloaded on to the PC for interpretation.

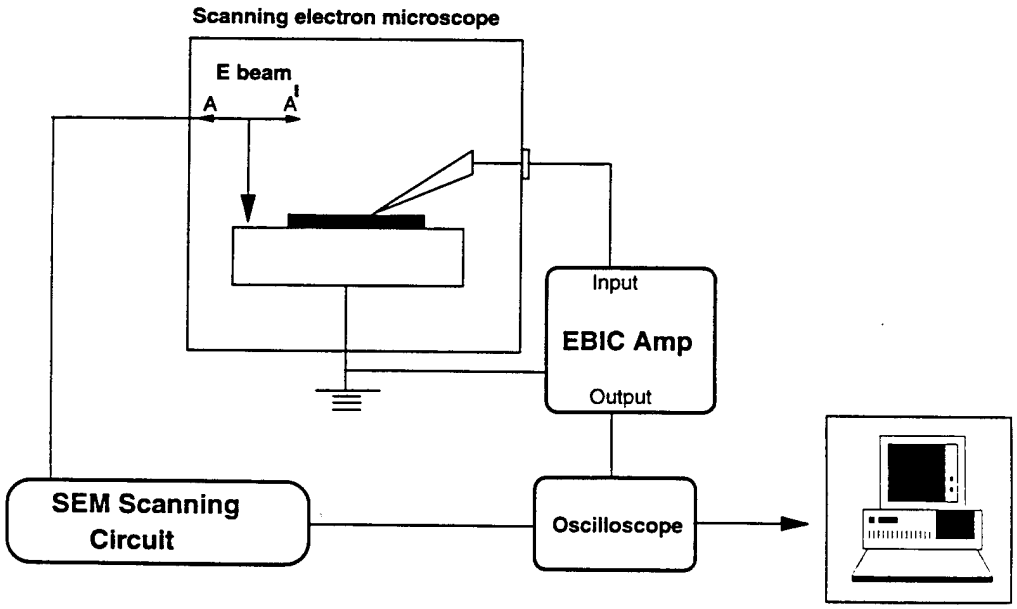

Figure 2. Schematic of the experimental setup.

C. Experimental Procedure

The setup was designed and interfaced with the PC in order to allow the data to be digitized. The unique capability of this setup is its ability to measure diffusion length at different temperatures with a heating stage that has been specially configured for the SEM. In this work, Schottky barrier diodes were fabricated using a shadow mask with sequential evaporation of Ti (1000 Å) and Al (1000 Å). Blanket evaporation of Ti/Al layer was done on the heavily doped substrate for backside ohmic contact. The material used for the fabrication of these diodes were nitrogen-doped 6H-SiC (1.1×10^{16}) and 4H-SiC (1.4×10^{16}); and Al doped 6H-SiC (6.0×10^{15}) and 4H-SiC (9×10^{15}) epitaxial layers obtained from CREE Research, Inc. Measurements were made on all four structures and a variation of the minority carrier diffusion length with temperature was studied.

D. Results

Diffusion lengths in 4H- and 6H-SiC were extracted using various values of α. It was found that the extracted value of L was insensitive to the variation in α, as shown in Fig. 3.

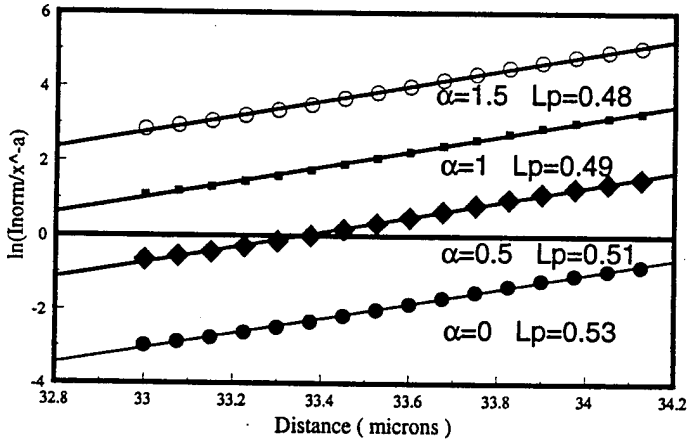

Figure 3. Impact of varying α on the extraction of Lp for n-type 4H-SiC.

It is important to use low energies for the electron beam so that the generation volume is small in order to obtain high resolution for the measurement. Secondly, since SiC is anisotropic, it is essential to generate carriers close to the surface so that only the lateral diffusion length is measured. Measurements made in order to study the variation of L_p in 6H- and 4H-SiC for accelerating voltage of 4, 5 and 6 kV show that it is not sensitive to variations in beam energy as shown in Fig. 4. Hence for measurement purposes, α was assumed to be 0 and an accelerating voltage of 5 kV was used. The extracted value of L_p for n-type 6H-SiC was 0.39 μm and 0.6 μm for n-type 4H-SiC. Similar measurements were made for p-type 6H-and 4H-SiC. L_n for 6H-SiC was calculated to be 1.19 μm and for 4H-SiC was

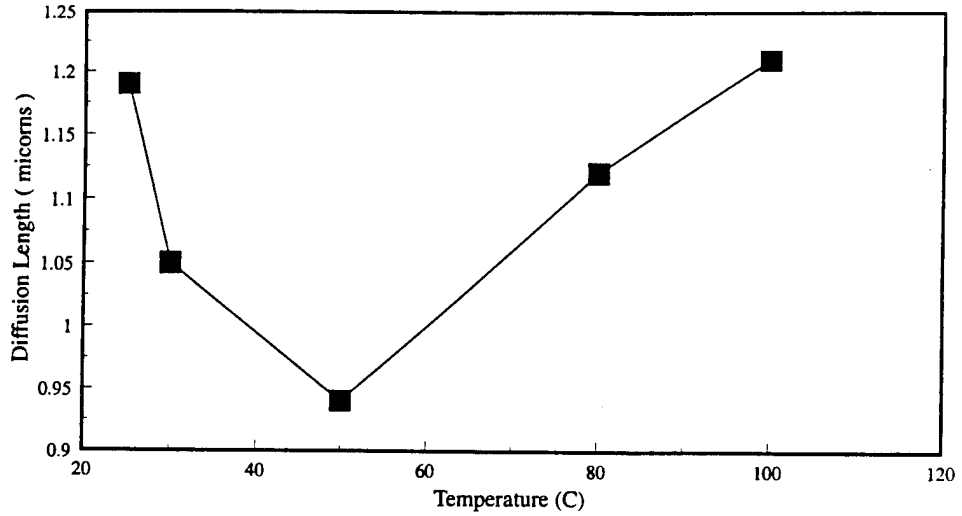

Figure 4. Variation of diffusion length (Ln) with temperature for p-type 6H-SiC.

found to be 1.4 μm. The variation of L_n and L_p with temperature was studied for the two polytypes and was found to be non-monotonic as also observed by Strel'chuk [2] for n-type 6H-SiC grown in Russia. Figures 5 and 6 show the variation of L_p with temperature for n-type 6H- and 4H-SiC, respectively. This variation was found to be non-monotonic, as can be seen in the figures. L_n in 6H-and 4H-SiC, on the other hand, was found to be monotonically increasing with temperature, as seen in Fig. 6 and Fig. 7, respectively. All wafers were obtained from CREE Research, Inc.

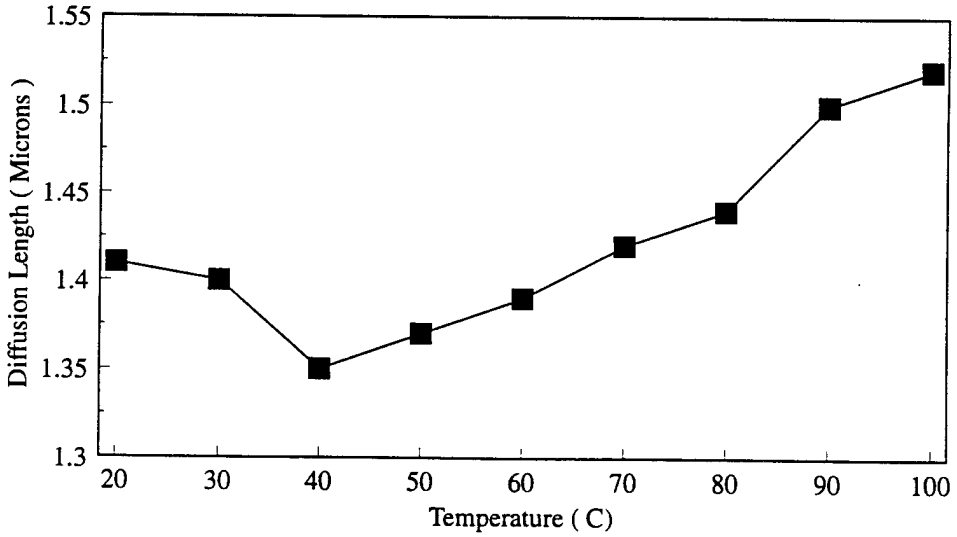

Figure 5. Variation of diffusion length (Ln) with temperature for p-type 4H-SiC.

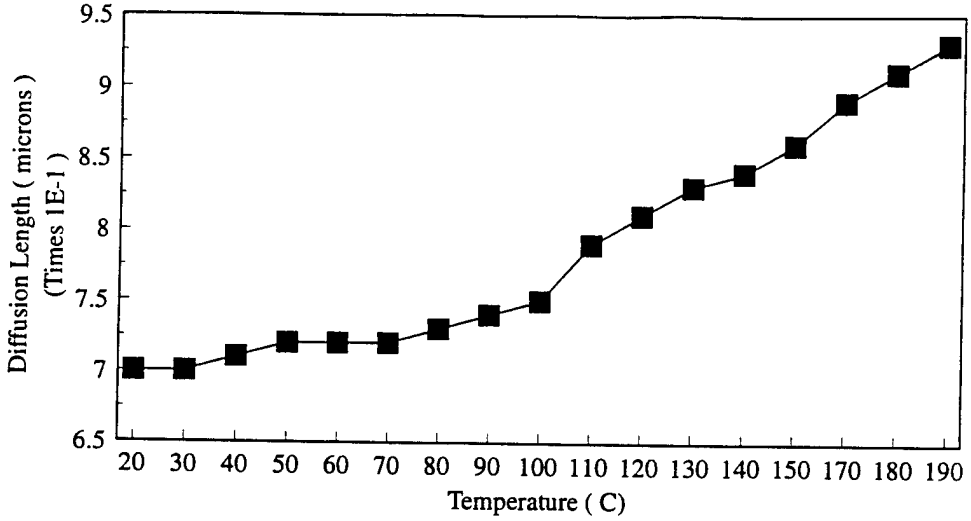

Figure 6. Variation of diffusion length (Lp) with temperature for n-type 6H-SiC.

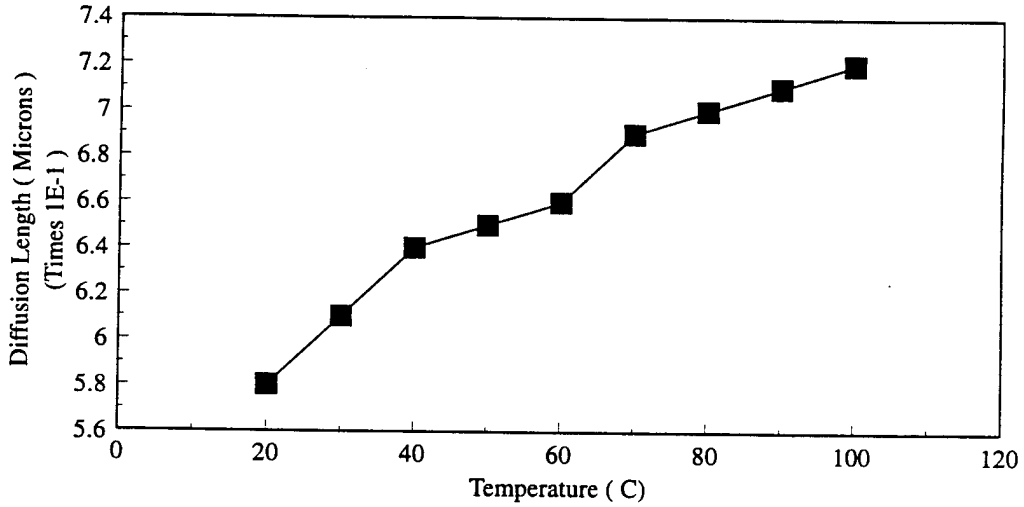

Figure 7. Variation of diffusion length (Lp) with temperature for n-type 4H-SiC.

E. Discussion

An attempt is being made to understand the non-monotonic variation of diffusion length with temperature for p-type SiC. For n-type 4H-SiC, Strel'chuk *et al.* reported non-monotonic variation for temperatures below 300 K. All measurements were made at temperatures above 300 K and this could possibly be the reason this characteristic behavior is not observed in n-type 6H- and 4H-SiC. Strel'chuk *et al.* reported that this non-monotonic behavior reflects the recombination properties of the material most reliably. Diffusion length of the minority carriers

is governed not only by their lifetimes but also by their mobilities. Diffusion length is related to the lifetime and the mobility given by the relation:

$L = (D^* \tau)^{1/2}$ where D is the diffusion coefficient,

D is related to the mobility by

$D = (kT/q)^*\mu$ where μ is the mobility.

The effect of temperature on each of the coefficients D, μ and τ has to be understood in order to obtain insights into the non-monotonic variation of the diffusion length with temperature.

F. Conclusions

Schottky barrier diodes were fabricated on n- and p-type 6H- and 4H-SiC by sequential evaporation of the Ti/Al using a shadow mask. Minority carrier diffusion lengths measurements were made on these diodes and their variation with temperature was studied. A special setup was configured that will allow measurement of the temperature variation of diffusion lengths using the SEM. The extracted value of L_p for n-type 6H-SiC was 0.39 μm and 0.6 μm for n-type 4H-SiC. Similar measurements were made for p-type 6H-and 4H-SiC. L_n for 6H-SiC was measured to be 1.19 μm and for 4H-SiC was found to be 1.4 μm. The variation of L_n and L_p with temperature was studied for the two polytypes and found to be non-monotonic. Attempt is being made to understand this behavior.

G. References

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IV. Contacts on P-type Alpha (6H) Silicon Carbide

A. Introduction

While the wide bandgap of SiC is responsible for its use in opto-electronic, high power, and high temperature devices, this property also adds to the difficulty of controlling the electrical properties at the metal-semiconductor contacts in these devices. The primary parameter used to quantify the electrical relationship at these interfaces is the Schottky barrier height (SBH), or the energy barrier for electrons traversing the interface. A small SBH is desired for an ohmic contact, while a relatively large SBH is necessary to create a good rectifying contact.

There is significant evidence for the presence of surface states in SiC at a level sufficient to reduce the control over SBHs from the ideal Schottky-Mott behavior but not sufficient to completely pin the Fermi level [1]. This reduced control over the SBHs due to surface states makes it especially difficult to form contacts to p-type SiC with low enough SBHs to make good ohmic contacts. Previous work at NCSU [2] showed that hydrogen termination of the n-type 6H-SiC (0001) surface resulted in a passivation of surface states. We have recently extended these experiments to study the effects of H-termination of the p-type 6H-SiC (0001) surface on its SBH with Pt. A comparison of the photoemission results of Pt deposited on H-treated and non-H-treated samples will be presented.

B. Experimental Procedure

A single-crystal, p-type 6H-SiC ((0001), 3.5° off-axis) wafer provided by CREE Research, Inc. was used as a substrate in the present research. The wafer was doped with Al during growth to yield a carrier concentration of 2.7×10^{18} cm^{-3}. A homoepitaxial layer (0.9 μm thick) was grown on this substrate by chemical vapor deposition (CVD) and also doped with Al, yielding a carrier concentration of 2.6×10^{15} cm^{-3}. To prevent a reduction in Al concentration at the surface due to reaction with O, the surface was not thermally oxidized.

Because the surface cleaning procedures were different for each sample and were integral to the experiments, the details of these procedures will be explained in the Results section. With the exception of the 15 min. submersions of the substrates in 10% HF to remove the surface (native) oxide, all surface preparations, sample transfers, metal depositions, and surface analyses were performed in systems with ultra-high vacuum base pressures.

Platinum was deposited by electron beam evaporation at a rate of 10–20 Å/min. The samples were analyzed by x-ray photoelectron spectroscopy (XPS) and ultra-violet photoelectron spectroscopy (UPS) made by VG Instruments. In the XPS and UPS analyses Al Kα (1486.6 eV) and He I (21.2 eV) photons, respectively, impinged on the sample, resulting in elastic scattering of electrons near its surface. A detector positioned close to the

sample measured the kinetic energies of the emitted electrons (In XPS the kinetic energies are converted to binding energies by subtracting the kinetic energy from the energy of the incident photons.).

C. Results

Platinum on Non-hydrogen Treated SiC. A piece of a p-type 6H-SiC wafer with a carrier concentration of 2.6×10^{15} cm^{-3} in the epilayer was submersed in 10% HF for 15 min. to remove the native oxide at the surface and immediately loaded in the vacuum system. The sample was then heated to 700 °C for 15 min. to remove hydrocarbon contamination and subsequently analyzed by both XPS and UPS. The XPS survey spectrum showed residual O (submonolayer) to be the only surface contaminant. Thin layers (total thicknesses = ≈2 and ≈8 Å) followed by a thick layer (1000 Å) of Pt were deposited on the SiC substrate. The sample was analyzed by photoemission after the deposition of each metal layer.

The amount of band bending at the surface was determined from the UPS spectra of the clean SiC surface and of the sample after depositing 1000 Å of Pt (Fig. 1). Because the UPS spectrum represents the electron density of states at the surface of the sample, the position where the intensity goes to zero for a semiconductor represents the position of the valence band maximum (VBM). The VBM for the clean SiC surface relative to the Fermi level was determined by comparison to the spectrum obtained after depositing 1000 Å of Pt. The

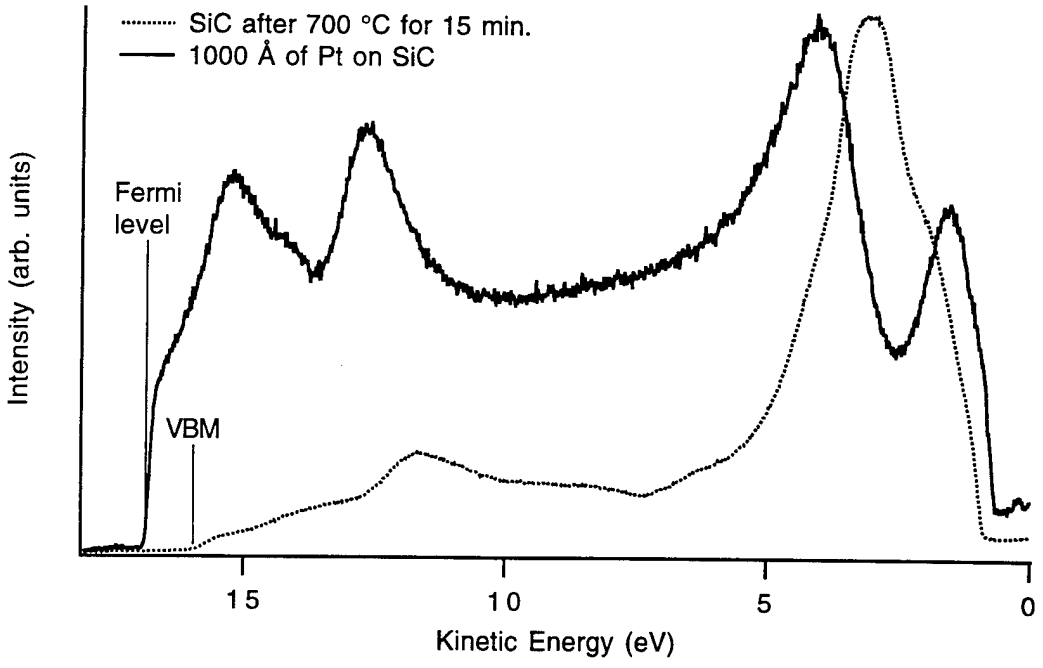

Figure 1. UPS spectra from a p-type (2.6×10^{15} cm^{-3}) SiC sample (a) after 15 min. in 10% HF followed by heating at 700 °C for 15 min. in UHV and (b) after subsequent deposition of 1000 Å of Pt.

difference in these energy positions equals 0.85 eV and represents their relative positions at the surface. Within the SiC epilayer, the VBM is only 0.22 eV below the Fermi level as calculated from the carrier concentration. The difference between the relative surface positions indicates that there is a downward band bending of ≈0.6 eV.

The SBH at the Pt/SiC interface was calculated from the shifts in the XPS C 1s and Si 2p peaks from the SiC after depositing the thin Pt layers. The SBH is equal to the position of the VBM at the SiC surface relative to the Fermi level, and the VBM should shift by an amount equal to the shift of the electron core levels in the substrate. Curve fitting using a combination of Laurentian and Gaussian fits was performed to eliminate any shifts due to chemical reaction. Thus, the C 1s and Si 2p peak positions and corresponding shifts listed in Table I represent the C-bound-to-Si and Si-bound-to-C components, respectively. Both the C and Si peaks shifted by 0.57 eV to higher binding energy, corresponding to SBH of ≈1.42 eV.

Table I. XPS Binding Energies of C 1s and Si 2p Electrons Originating from the Surface of the SiC Substrate Before and After Depositing Thin Layers of Pt.

	C 1s Binding Energy (eV)	Si 2p Binding Energy (eV)
After 700 °C for 15 min.:	281.52	99.43
After 2 Å of Pt:	281.61	99.52
After 8 Å of Pt:	282.09	100.00
Total shift:	+0.57	+0.57

Platinum on Hydrogen Treated SiC. For this experiment the same surface preparation and Pt deposition procedures described for the previous experiment were used except that a hydrogen surface treatment step was added prior to depositing Pt on the SiC surface. The passivation of surface states in n-type 6H-SiC (0001) by terminating the surface with H was previously reported [2]. As in this previous report, the hydrogen termination procedure in the present research employed a remote hydrogen plasma system at 20 W of rf power, with 80 sccm of H_2 for 15 min. and a substrate temperature of 450°C.

The band bending at the SiC surface after the hydrogen exposure was calculated from the UPS spectra (Fig. 2) as described for the non-hydrogen treated sample after surface cleaning. The energy difference between the Fermi level and the VBM (0.85 eV) in the former sample was calculated to be the same as that for the latter.

After depositing thin layers of Pt, the SBH was again calculated from the shifts in the C 1s and Si 2p peaks. The total average shift in the C and Si peaks (Table II) after depositing 8 Å of

Pt was -0.03 eV. This energy shift added to the Fermi level–VBM energy difference corresponds to a SBH of ≈0.82 eV.

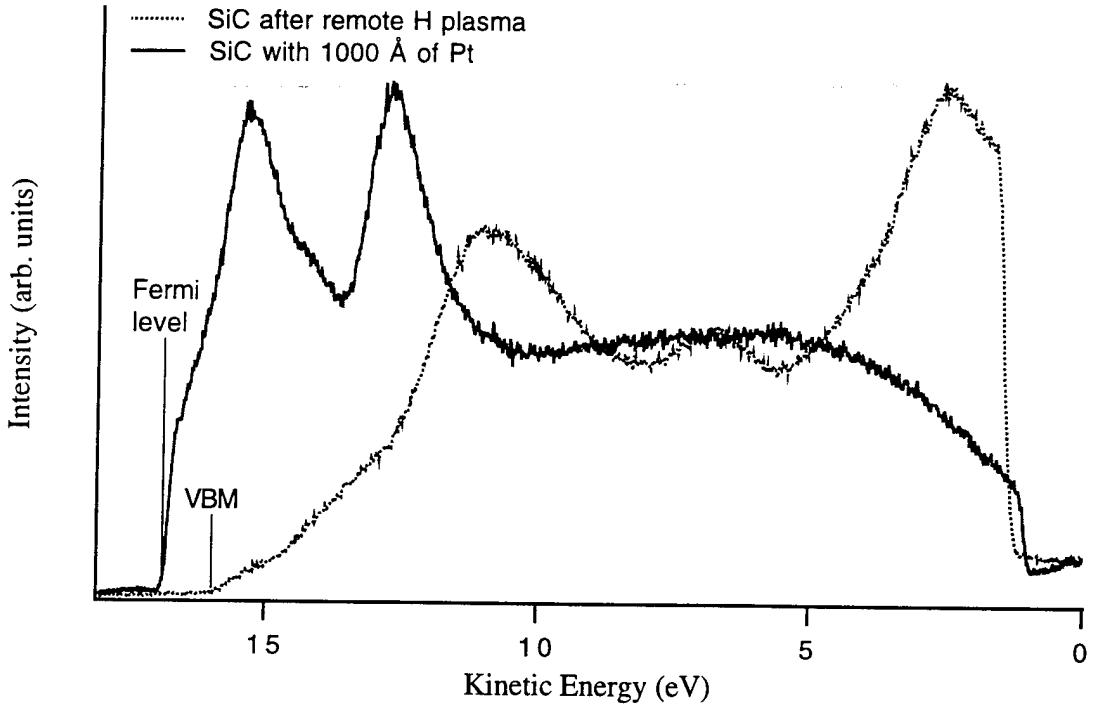

Figure 2. UPS spectra from a p-type (2.6×10^{15} cm^{-3}) SiC sample (a) after 15 min. in 10% HF, heating at 700 °C for 15 min. in UHV, followed by remote H plasma exposure and (b) after subsequent deposition of 1000 Å of Pt.

Table II. XPS Binding Energies of C 1s and Si 2p Electrons Originating from the Surface of the SiC Substrate Before and After Depositing Thin Layers of Pt.

	C 1s Binding Energy (eV)	Si 2p Binding Energy (eV)
After H exposure	282.57	100.43
After 2 Å of Pt:	282.52	100.39
After 8 Å of Pt:	282.53	100.41
Total shift:	-0.04	-0.02

D. Discussion

The downward band bending calculated for the p-type SiC surfaces prior to the deposition of Pt indirectly indicates that donor-like surface states are present in the band gap. An upward band bending in n-type SiC after similar cleaning procedures was previously determined [3],

band bending in n-type SiC after similar cleaning procedures was previously determined [3], indicating the presence of acceptor-like surface states. The combination of these results indicates that both acceptor-like and donor-like states are present on these surfaces, but the neutrality of these states depends upon the position of the Fermi level in the band gap.

The reduced SBH calculated for the hydrogen-treated sample may be associated with a passivation of surface states in p-type SiC. However, the equivalent band bending for the non-hydrogen-treated and hydrogen-treated SiC surfaces does not seem to support this theory. An understanding of the effect of H on the interface between Pt and p-type SiC requires further investigation. The potential for a reduced SBH for contacts to p-type SiC is encouraging because the large band gap of SiC has prevented sufficient reduction of p-type SBHs for producing low resistivity ohmic contacts.

A photovoltaic effect [4-5] appears to play a role in the photoemission results of these samples and the possibly the corresponding band bending calculations. If the incident photon energy is greater than the band gap energy, the illumination in photoemission studies can produce electron-hole pairs which then become physically separated if there is a built-in field (i.e. band bending at the surface of the semiconductor). This results in a photovoltage which opposes the voltage associated with the surface band bending, thus reducing the amount of surface band bending. The difference in the Fermi level positions (edge of the UPS spectrum) for the thin (8 Å) and thick (1000 Å) Pt overlayers can likely be attributed to a photovoltaic effect. Performing these analyses at elevated temperature should eliminate the photovoltaic effect because the emission current becomes high enough to compensate for the tendency for charge separation.

Both samples showed the same energy shift in the UPS Fermi level positions. However, the XPS core level binding energies were significantly different for the two samples (Tables I and II). It is also unknown whether this effect requires an adjustment in the SBH calculations. Thus, these results should be considered preliminary. Further investigation into the binding energy shifts and the Schottky barrier height effects will be pursued.

E. Conclusions

Preliminary investigations of the effect of hydrogen exposure of the p-type 6H-SiC (0001) surface on its SBH with Pt have been performed. These experiments are an extension of previous work at NCSU which showed that surface states were passivated in n-type 6H-SiC (0001) when the surface was terminated with H. Calculations based on XPS and UPS results yielded a substantially reduced SBH value for the hydrogen-treated sample (0.82 eV) from that of the non-hydrogen-treated sample (1.42 eV). However, further investigations are required to understand the discrepancy between XPS binding energies for the two samples and its possible effect on the SBH calculations.

F. Future Research Plans and Goals

Studies involving Pt contacts on non-hydrogen-treated and hydrogen-treated, p-type 6H-SiC (0001) surfaces will be continued and extended to include n-type SiC as well. Thick layers of Pt will be deposited on these surfaces for current-voltage and capacitance-voltage measurements from which SBHs will be calculated. The results of these measurements will be compared to those obtained from the photoemission results for thin layers of Pt on similarly prepared substrates.

While Al is conventionally used in ohmic contacts to p-type SiC, Al causes severe problems from oxidation. To reduce this problem, we have chosen to investigate selected materials which contain B as an alternative to Al.

The main reasons for choosing B are: 1) it is also a p-type dopant in SiC, 2) its oxide is not as stable, and 3) it is a much faster diffusant in SiC. Table III compares some important properties of B, Al, and their associated oxides. Although the B acceptor level in 6H-SiC is substantially deeper than that of Al, the fact that B is an acceptor makes it worth investigating as a component in p-type ohmic contacts. Also, boron compounds tend to be more stable at high temperatures than aluminum compounds which suffer from the low melting point of Al. As shown in Table III, the diffusion coefficient of B is at least three orders of magnitude greater than that of Al. Therefore, more B than Al will diffuse into the SiC at lower temperatures. A major problem with Al-based contacts is the strong driving force for forming an insulating oxide layer. This situation is shown by the extremely low equilibrium partial pressure, p_{O2}, for Al_2O_3 formation. While B_2O_3 also has a low p_{O2}, it is significantly higher than that for Al_2O_3, indicating that the driving force for B to form an oxide is significantly lower. In addition, the melting point of boron oxide is notably low.

Table III. Selected Properties of B, Al, and Associated Oxides.

Element	Activation Energy in 6H-SiC (meV)	Solid Source Diffusion, D_{SiC} @ 1800°C (cm^2/s)	Equilibrium partial pressure of O_2, p_{O2} @ 700°C (torr)	Melting temp. of the associated oxide, T_{melt} (°C)
B	700	10^{-11} [10-11]	10^{-35}	450
Al	240	$<10^{-14}$ [12]	10^{-47}	2040

Several boron compounds possess reasonably low resistivities and high melting temperatures. Of these compounds the simpler ones to form by electron beam deposition are probably CrB_2, VB_2, and ZrB_2. The refractory nature of these compounds increases the

chance of forming ohmic contacts which will be stable at high temperatures. Chromium and B have been placed in the evaporation system and will be deposited on p-type SiC for contact measurements.

Another alternate approach to Al-based ohmic contacts for p-type SiC will incorporate p-type semiconducting interlayers. The goal of this approach is to find a semiconducting material which has a favorable band lineup with SiC (i.e., reduce the band bending) and to which an ohmic contact can easily be made. We have chosen to examine the $In_xGa_{1-x}N$ system for interlayer materials because of the lower density of surface states (and hence less band bending) and the range of band gaps over the composition range. It is planned to measure the valence band offsets and electrical characteristics between various compositions of $In_xGa_{1-x}N$ (starting with x=0) and SiC. If a low energy barrier at the interface results, metals will be investigated for ohmic contacts for the interlayer / SiC structure.

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V. Characterization of Oxides on N- and P-Type 4-H and 6-H SiC

A. Introduction

Silicon carbide (SiC) has been shown to be an excellent material for the fabrication of devices for high power, high frequency and high temperature applications [1]. The advantages of SiC metal oxide semiconductor field effect transistors (MOSFETs) has also been discussed [2]. The successful operation of these devices hinges on the interface and bulk properties of the gate dielectric, usually an oxide. Previous researchers have reported results on thermally grown oxides on N-type [3-6] and P-type 6H-SiC [5,7-11]. While the results obtained on N-type 6H-SiC have shown that those oxides are of high quality, oxides grown on P-type 6H-SiC exhibit large flatband voltage shifts and are thus unsatisfactory for application as gate dielectrics. Oxides deposited under special conditions with surface preparation specific to the particular deposition might show improved interfacial properties over thermally grown oxides.

The SiO_2-SiC interfaces will be characterized using capacitance-voltage (C-V) measurements [12]. A Mask set has been designed to fabricate the MOS structures required for accurate and complete electrical characterization. The Mask set, fabricated at DuPont Photomasks Inc., was delivered during this period.

B. Experimental Procedures

In the proposed process, the wafer would first be subjected to a sacrificial oxidation to clean the surface. This sacrificial wet oxidation was performed both on the 6H-SiC and 4H-SiC wafer, as well as a monitor 6H-SiC wafer. The wafers were first subjected to an RCA clean (5 minutes in $NH_4OH:H_2O_2:H2O::1:1:5$ at 75°C followed by a 5 minute rinse followed by 5 minutes in $HCl:H_2O_2:H_2O::1:1:5$ at 75°C followed by a 5 minute rinse) with no subsequent BOE dip. The wafers were then subjected to dry-wet-dry oxidation for 5-240-5 minutes at 1100°C. The resultant oxide thicknesses were ellipsometrically measured using a Gaertner ellipsometer. The 6H-SiC wafer had a mean oxide thickness of 266A with a std. deviation of 3.3A and the 4H-SiC wafer had a mean oxide thickness of 311A with a std. deviation of 4.4A. The mean oxide thickness on the monitor 6H-SiC wafer was 267A with a std. deviation of 8.1A.

A low temperature oxide (LTO) of thickness 6000A will then be deposited on the wafer. This LTO acts as a mask for the subsequent implant step. Subsequent to patterning this layer of LTO, a further 1000A of LTO would be deposited to act as a pad oxide during the source implant to keep the maximum dopant concentration at the surface and not inside the semiconductor. While the mean thickness of the first LTO layer can have some variability since its only function is to act as an implant mask, the mean thickness of the second LTO layer must be very close to 1000A as the doses and energies of the subsequent implant steps have been

designed and optimized taking into account a pad oxide thickness of 1000A. Experiments were performed to determine optimal conditions and wafer configurations at which the deposited LTO would be within ±10% of the nominal designed LTO thickness. This oxide will be then patterned so that the regions to receive the N+ implant are exposed. Another layer of LTO of thickness 1000A will be deposited on the wafer. This 1000A of oxide acts as a pad oxide during the implant step.

The patterned wafer will be subjected to a nitrogen implant to form the N+ highly doped regions. In order to account for the inevitable variability in the pad oxide despite our best efforts, a multiple energy implant step was designed to give a flat dopant profile. The two-implant step is as follows: (dose=2×10^{15} cm^{-2}: energy = 80keV :: dose= 1×10^{15} cm^{-2}: energy = 40keV). The simulations to check the implant profiles were done on Suprem3 and the resultant profiles are shown in Fig. 1. The wafer will be then subjected to a high temperature anneal to activate the dopant. The oxide will be further patterned to define the gate region and the gate dielectric thermally grown or deposited on the SiC.

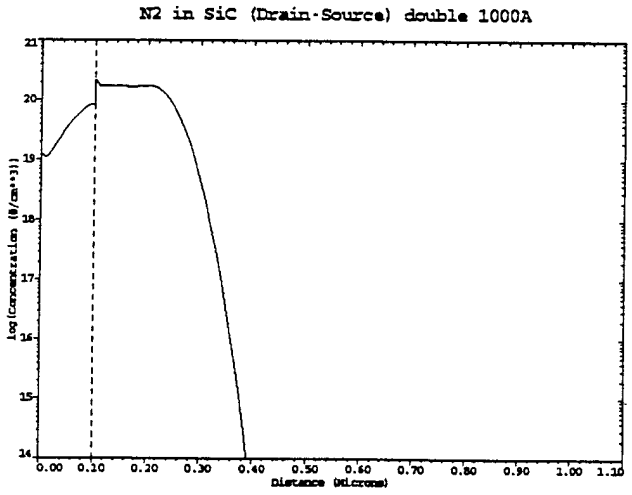

Figure 1. Nitrogen profile in SiC using 2 implants with parameters (80keV, 2E15:40kEv,1E15) through 1000A of LTO.

A blanket deposition of polysilicon will be then done and heavily doped N+ with phosphorus disks. The poly will be then patterned to form the gate. Using the poly as a mask, the gate dielectric not covered by the poly will be etched off. The RIE system used to etch poly is based on end-point detection. Therefore, uniformity of poly deposition is crucial to obtaining a clear end-point so that the RIE maybe be stopped before excessive etching of the underlying layers. Once again, due to the small size of the SiC wafers compared to the conventional 4" Si wafers, there will be an alteration of the gas flows and temperature gradients within the furnace changing the deposition that would be normally expected for the Si wafers. One-inch Si wafers

were first thermally oxidized to get a thermal oxide of 1000A and then used to optimize the deposition conditions.

Furthermore, the reflectivity of the SiC substrate is different from that of Si. Hence, exposure times for lithography must also be optimized. L-bars designed on each mask can be used to determine whether a particular dimension can be realized for that particular exposure time. Experiments were performed on different exposure tools for different times and the optimal exposure time was determined using a SiC substrate wafer.

D. Discussion

The design of the 4-level Mask set was completed in the first quarter. The first level of the Mask set will be used to define the area receiving the N+ nitrogen implant required for the source regions of the MOS-gated diodes. The second level of the Mask set will be used to define the area of the SiC on which the gate oxide would be thermally grown or deposited. In other words, this level would act as the active area mask. The third level of the Mask set will be used to define the polysilicon gate regions and the fourth level of the Mask set will be used to define the metal regions for contacts and pads. The Mask set (glass plates) arrived this quarter.

An order for 6H-SiC and 4H-SiC wafers from CREE Research, Inc. was also placed. The fabrication of the MOS devices will be on these wafers. The wafers were received in the current quarter.

Due to the excellent uniformity of thermal oxide grown on the SiC wafers during the sacrificial oxidation and the correlation between the oxide thickness on the device wafer and the monitor wafer, the monitor wafer can be confidently used to determine the gate oxide thickness on the device wafers during the gate oxidation step.

Various configurations of the 1" wafers were tried to obtain the best uniformity during the LTO deposition. The best results were obtained using the following configuration. A 3" wafer furnace quartz boat was taken and a 4" Si wafer was placed horizontally on it. Five 1" Si wafers were then placed flat on the 4" wafer in the form of a "+". The LTO thickness was measured using a Gaertner ellipsometer. Excellent visual uniformity was obtained both within each wafer and from wafer to wafer. The overall mean thickness was 2178A and the std. deviation from wafer-to-wafer was 42A and the std. deviation on each wafer varied between 15A to 46A. As can be seen from the data, the uniformity is about 2% and is more than adequate for the process.

An identical configuration was also tried for the poly uniformity experiment. The poly thickness was measured using Nanometrics. Excellent visual uniformity was obtained both within each wafer and from wafer to wafer. Out of the 5 1" wafers, the 1" wafer the furthest away from the furnace door had low deposition and high non-uniformity. Hence, data from that wafer is treated as "outlier" data and is disregarded in the following calculations. The

overall mean thickness was 4310A for a deposition time of 40 minutes and the std. deviation from wafer-to-wafer was 45A and the std. deviation on each wafer varied between 33A to 93A. Once again, the std. deviation is around 2% which is more than adequate for the process.

E. Conclusions

A Mask set was designed to fabricate devices that would enable accurate characterization of the SiO_2-SiC interface. Devices that will be fabricated include MOS capacitors and MOS gated diodes. The wide band-gap of SiC and the attendant modifications that this fact introduces in the characterization of the interface as opposed to the characterization of the SiO_2-Si interface have been recognized. The Mask set was delivered and various preliminary experiments were conducted to ensure that the fabrication steps conform to the requirements of the process, and the process was started.

F. Future Research Plans and Goals

The fabrication will be completed as speedily as possible and the characterization of the oxide films started.

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