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Investigation of Radiation Effects in Microelectronics

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13. ABSTRACT (*Maximum 200 words*)

Electronic components implemented in space borne and military applications are often required to operate in a hostile radiation environment, and are therefore subject to the degradation and failure mechanisms associated with such environments. This report discusses radiation-effects research in the areas of (1) single-event burnout of power MOSFETs; (2) single-event gate rupture of power MOSFETs; (3) total-dose degradation of power MOSFETs (including mobility degradation, cryogenic operation, $1/f$ noise, and termination structures); and (4) total-dose gain degradation of bipolar junction transistors. Experiment details and modeling and simulation results are given in these areas. This work is intended to (1) facilitate selection of appropriate components for radiation environments; (2) provide design techniques to improve the radiation hardness of power MOSFETs and bipolar junction transistors; and (3) advance the technical base with new physical insights in radiation effects in microelectronics.

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I. Introduction and Executive Summary

This final report describes work for Contract No. DNA001-92-C-0022. The start date for this effort was 8 May 1992.

The objectives for this effort as detailed in the statement of work were: (1) Investigation of natural space total ionizing radiation dose effects on power MOSFETs, BJTs, and integrated-circuits; (2) Characterization of single-event upset burnout effects in power MOSFETs, BJTs, and integrated circuits; (3) Investigation of radiation and temperature on MOS transistor mobility; and (4) Characterization of single-event gate rupture in power MOSFETs.

For the purposes of this final report, the major technical thrusts are organized as: (1) Modeling of Single-Event Burnout of Power MOSFETs; (2) Modeling of Single-Event Gate Rupture of Power MOSFETs; (3) Investigating Total-Dose Effects in Power MOSFETs; and (4) Investigating Total-Dose Gain Degradation in BJTs.

Heavy ions, ubiquitous in a space environment, can cause single-event burnout (SEB) in power MOSFETs. This is a catastrophic failure mechanism that is initiated by the passage of a heavy ion through the device structure. This event generates a current filament that locally turns on a parasitic npn transistor inherent to the power MOSFET physical structure. Subsequent high currents and high voltage in the power MOSFET induce second breakdown of the parasitic transistor and meltdown of the power MOSFET. During the course of the work described in this final report, a model was developed to describe the burnout mechanism and to predict the SEB threshold in terms of linear energy transfer (LET) of the incident heavy ion for a specified device structure and operating condition to make the device radiation tolerant. This is discussed in Section II.

In addition to SEB, power MOSFETs are vulnerable to another single-event phenomenon called single-event gate rupture (SEGR). SEGR can occur when a heavy ion strikes the neck region of the power MOSFET. The neck region constitutes the gate-drain overlap region of the device. Following the ion strike, the electric field due to the applied positive drain bias causes the generated holes in the silicon to move toward the silicon - silicon oxide (Si-SiO_2) interface and the electrons toward the drain contact. The holes leak off only slowly toward the source contact and therefore start to pile up at the Si-SiO_2 interface. This hole accumulation effect at the Si-SiO_2-interface creates a pool of positive charge which results in a transient field increase across the oxide at the track position. If this transient field increases above a critical value, oxide breakdown occurs heating the structure locally. If the breakdown current lasts long enough, a permanent short-circuit through the oxide results. For this program, a model incorporating a two-dimensional device simulator was developed to predict failure bias levels for SEGR to help design radiation tolerant devices. This is discussed in Section III.

Ionizing radiation results in charge generation in the oxide regions of electronic devices. As part of this program, several total-dose effects in power MOSFETs resulting from ionizing radiation are investigated. One topic that is investigated extensively in this task is mobility degradation due to ionizing radiation. Charge separation techniques were used to show that interface states and oxide trapped charge contribute to mobility degradation. It is shown that mobility degradation is more pronounced at 77 K than at room temperature. In addition to mobility degradation, increases in the subthreshold leakage current and $1/f$ noise, and the integrity of the termination structure following total-dose ionizing radiation were investigated. Furthermore, the consequences of extrapolating higher dose-rate, total-dose response, to typical space environment dose-rate response of power MOSFETs was investigated. The effects of cryogenic operation during irradiation in power MOSFETs were also investigated. These topics are discussed in Section IV.

consequences of extrapolating higher dose-rate, total-dose response, to typical space environment dose-rate response of power MOSFETs was investigated. The effects of cryogenic operation during irradiation in power MOSFETs were also investigated. These topics are discussed in Section IV.

Bipolar junction transistors (BJTs) continue to play an important role in integrated circuit technology. BJTs are important for many systems that may be exposed to ionizing radiation. Previous studies of modern BJTs have shown time-dependent effects following irradiation that differ from those seen in MOS devices. Some types of BJTs show greater gain degradation after low dose rate irradiations with low electric-fields than after high dose rate irradiations. Moreover, high dose rate irradiation followed by annealing can not simulate the low dose rate response of many BJTs. The base current in modern BJTs increases in an ionizing radiation environment due to increased recombination in the emitter-base depletion region. The recombination current results from two interacting effects: (1) increased surface recombination velocity, and (2) spreading of the emitter-base depletion region. For this task, extensive experimentation and modeling of trench-isolated silicon-on-insulator BJTs from vertical, lateral, and substrate technologies were performed to characterize these devices for radiation-induced gain degradation. This is discussed in Section V.

Like radiation, hot-carrier stress degrades the current gain in BJTs by increasing the base current while affecting the collector current negligibly. Mechanical stress has been reported to be strongly linked to the radiation hardness of MOS capacitors. In this program, through rigorous experimental characterization, computer simulation, and modeling, hot-carrier effects in poly- and single-crystalline npn bipolar transistors were investigated with regard to radiation damage and device geometry. A physically-based comparison between hot-carrier and radiation-induced degradation in BJTs is made which emphasizes the mechanisms of gain degradation by each stress type. Additionally, mechanical stress-related radiation effects were investigated in single-crystalline emitter BJTs that were subjected to repeated cycles of irradiation and anneal. This is also discussed in Section V.

The following sections provide detailed information on the items briefly introduced in this Introduction and Executive Summary. Section II covers Modeling of Single-Event Burnout of Power MOSFETs, Section III describes Modeling of Single-Event Gate Rupture of Power MOSFETs, Section IV covers Investigating Total-Dose Effects in Power MOSFETs, and Section V discusses Total-Dose Gain Degradation in BJTs. A Summary is given in Section VI, and Section VII contains Acknowledgments.

II. Modeling of Single-Event Burnout of Power MOSFETs

II.A. Introduction

Single-event burnout of double-diffused MOS (DMOS) power transistors occurs due to turn-on of the parasitic bipolar transistor in the DMOS structure by a heavy ion. As part of this program, a model for single-event burnout was developed that offers a clear picture of the relationships between the device structural parameters and the properties of the ion-induced current filament. This understanding is necessary for the production of power MOSFETs with decreased susceptibility to single-event burnout.

The parasitic bipolar transistor is formed by the n^+ source (emitter), the p-body (base), and the n drain (collector). When a heavy ion passes through the device, it generates a filament of charge along its path. The electrons in the filament are transported to the drain terminal by the electric field, while the holes move toward the p-body. Before the holes can be removed from the device, they must flow laterally through the parasitic resistance of the body region. The source and body regions are shorted together at the surface of the device by the source metallization, preventing turn-on of the parasitic bipolar transistor in normal device operation. However, the resistive voltage drop generated by the returning holes is of the polarity required to forward bias the emitter junction of the parasitic BJT.

When the emitter of the parasitic BJT is forward biased, electrons are injected into the base and collected by the reverse-biased drain-body (collector) junction. These electrons undergo avalanche multiplication in the drain-body depletion region, generating additional holes that must flow through the parasitic body resistance to ground. If enough holes are generated, the process becomes self-sustaining, the drain current locally increases to a very high level, and the device burns out. The parasitic resistance of the body region is extremely important in determining the critical ion LET (linear energy transfer) at which the device will burnout. The parasitic resistance can be reduced by extending a p^+ plug from the body contact toward the channel region of the power MOSFET.

The process by which the parasitic bipolar transistor turns on is controlled by avalanche generation of carriers in the drain-body depletion region and the voltage drop developed along the body region by the return of the avalanche-generated holes to ground. A feedback model that describes this process was developed under this contract and described in detail in several technical publications. The model predicts that the device is more susceptible to SEB with increasing drain-source bias and decreasing lateral extent of the p^+ plug. These results are consistent with those obtained with two-dimensional simulations. The effects of elevated temperature on SEB were incorporated into the model. As temperature increases, the impact ionization rate for a given electric field decreases due to a shorter mean free path between collisions. A decrease in the impact ionization rate results in a decrease in the avalanche multiplication rate which leads to a decrease in the SEB susceptibility. The papers describing the model are included in Sections *II.B* through *II.D.* A brief overview of each paper is included here to guide the reader through this material.

Section II.B.: G.H. Johnson, R.D. Schrimpf, K.F. Galloway, and R. Koga, "Temperature Dependence of Single-Event Burnout in N-Channel Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 1605-1612, 1992.

> This paper shows that the single-event burnout susceptibility of power MOSFETs decreases with increasing temperature. This is caused by a reduction in the impact ionization rate at elevated temperature, due to increased phonon scattering.

Section II.C.: G.H. Johnson, J.H. Hohl, R.D. Schrimpf, and K.F. Galloway, "Simulating Single-Event Burnout of N-Channel Power MOSFETs," *IEEE Trans. Electron Devices*, vol. 40, pp. 1001-1008, 1993.

> This paper presents the most complete description of the model. It begins with an overall discussion of the burnout process and the heavy-ion-induced current filament. A model is presented for the parasitic-BJT operation, including the feedback mechanism, generation of holes due to avalanching, and the turn-on time of the device following an ion strike. Finally, some typical burnout thresholds are calculated and the critical LET for burnout is plotted vs. the extent of the p+ plug.

Section II.D.: G.H. Johnson, J.R. Brews, R.D. Schrimpf, and K.F. Galloway, "Analysis of the Time-Dependent Turn-On Mechanism for Single-Event Burnout of N-Channel Power MOSFETs," in *RADECS 93 Proc.*, 1993, pp. 441-445.

> This paper investigates the time-dependent mechanisms involved in single-event burnout. A first order dynamic model including a lumped-parameter RC charging circuit representing the resistance and capacitance of the base-emitter junction of the parasitic BJT is used. The model shows that an increase in the junction capacitance or a decrease in the base resistance of the parasitic BJT leads to a reduction in single-event burnout susceptibility.

II.B. Temperature Dependence of Single-Event Burnout in N-Channel Power MOSFETs

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TEMPERATURE DEPENDENCE OF SINGLE-EVENT BURNOUT IN N-CHANNEL POWER MOSFETs †

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ABSTRACT

The temperature dependence of single-event burn out (SEB) in n-channel power metal-oxide-semiconductor field effect transistors (MOSFETs) is investigated experimentally and analytically. Experimental data are presented which indicate that the SEB susceptibility of the power MOSFET decreases with increasing temperature. A previously reported analytical model that describes the SEB mechanism is updated to include temperature variations. This model is shown to agree with the experimental trends.

I. INTRODUCTION

It has been known for some time that single-event burnout (SEB) of power metal-oxide-semiconductor field effect transistors (MOSFETs) is a catastrophic failure mode that can be triggered by the passage of a single heavy ion through the device [1]. This phenomenon is of concern to space-born system designers since heavy ions are ubiquitous in the space-radiation environment [2]. In addition, the broad range of temperatures that may occur on board a system in flight necessitates an investigation of the temperature dependence of the SEB mechanism.

Power MOSFET burnout has been attributed to the turn-on of the parasitic bipolar-junction transistor (BJT), inherent to the double-diffused metal oxide semiconductor (DMOS) structure, when the power MOSFET is turned off (blocking a large drain-source bias) [3]. Previous burnout modeling has been performed for an ambient device temperature of 300 K. This paper reports the temperature dependence of the burnout mechanism in n-channel power DMOS devices.

Observation of SEB in p-channel power MOSFETs has not been reported in the literature. It is believed that the much lower impact-ionization rate for holes than electrons is responsible for the apparent hardness to SEB seen in p-channel power MOSFETs [3]. For this reason, the temperature dependence of SEB in p-channel devices will not be presented in this paper.

The non-destructive burnout experiment method, with a means to control the ambient temperature of the device, was performed on IR6766 and IRF150 power MOSFETs. The SEB cross-section was measured as a function of drain-source voltage and temperature. The temperature was varied from 300 K to 373 K. Due to the difficulty (or impossibility) of cooling devices within the experimental chamber, only temperatures at and above room temperature are investigated herein. The experimental results indicate that the burnout susceptibility of a given device decreases with increasing temperature for a given applied drain-source voltage.

The details of the testing technique are given in Section II. The experimental results are presented in Section III. The burnout mechanism for the power DMOS device structure is reviewed, and the temperature dependence of the model is discussed in Section IV. The temperature dependence of the SEB threshold is then calculated for a typical DMOS device in Section V. Finally, conclusions are given in Section VI.

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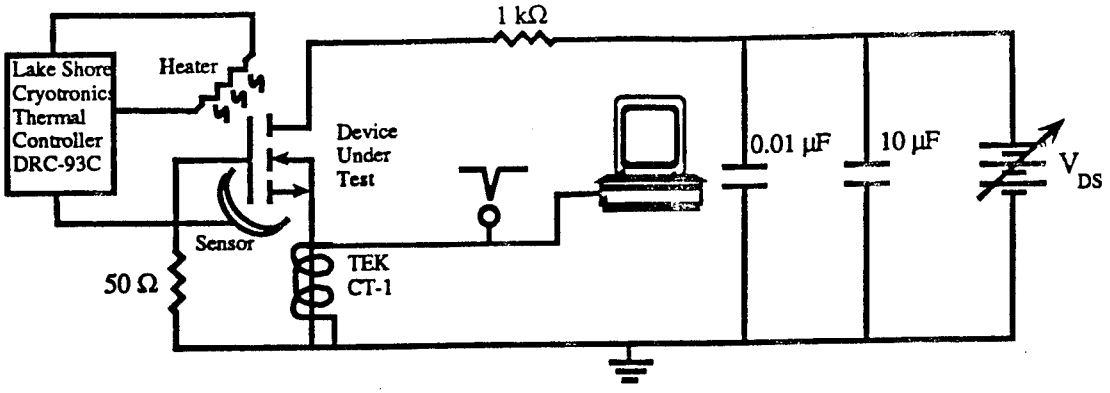


Figure 1: Non-destructive, temperature controlled SEB test set-up.

II. Burnout Experiment

The IR6766 and IRF150 n-channel power MOSFETs with breakdown voltages, BV_{DS}, of 200 V and 150 V, respectively, were subjected to heavy ion bombardment in the 88-inch cyclotron facility at Lawrence Berkeley Laboratories. A monoenergetic beam of 380 MeV Kr ions at a fixed LET of 41 MeV-cm²/mg was used to characterize the devices. The devices were de-lidded prior to heavy ion exposure. Each test was performed until a total fluence of 10^7 ions/cm² was obtained, or an error of ~ 100 pulses were counted.

The ambient device temperature was maintained using the Lakshore Thermal Controller DRC-93C. The temperature controller consisted of a resistive heater and thermal sensors connected in a feedback loop. The heater and sensors were attached directly to the TO-240 package of the device under test, (DUT). It was determined that if the temperature was allowed to equilibrate for several minutes, the temperature was very uniform across the surface of the chip. This provided a reliable indication of the device temperature.

The non-destructive burnout test method was used in order to obtain SEB cross-sections for a given device type [4, 5]. The non-destructive test technique employs a current limiting resistor in the drain lead of the DUT so that the drain-source current can not rise sufficiently to induce second breakdown of the parasitic bipolar transistor and consequently burnout. The current-limited pulses were monitored at the drain terminal of the DUT using a Tektronix TEK-CT1 current transformer. SEB cross-section measurements were made by varying the applied drain-source voltage, since the SEB cross-section increases with increasing drain-source voltage. The SEB cross-section was found by the usual method of dividing the total number of nondestructive current pulses per device by the beam fluence to yield units of cm²/device. The experimental test set-up is shown in Figure 1.

III. Experimental Results

SEB cross-section measurements were obtained for the devices at device temperatures of 300 K, 333 K, 353 K, and 373 K. The cross-section versus drain-source voltage for the IR6766 and IRF150 are shown in Figures 2 and 3, respectively. In each case, the V_{DS} threshold for burnout increases with increasing temperature. Also note that in each case, for a given applied drain-source voltage, the SEB cross-section decreases with increasing temperature. Furthermore, as the drain-source bias

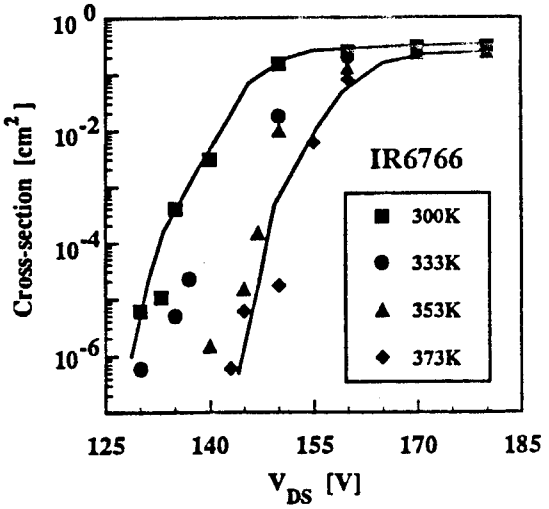


Figure 2: SEB Cross-section versus V_{DS} and temperature for the IR6766 power MOSFET (solid lines drawn to guide the eye).

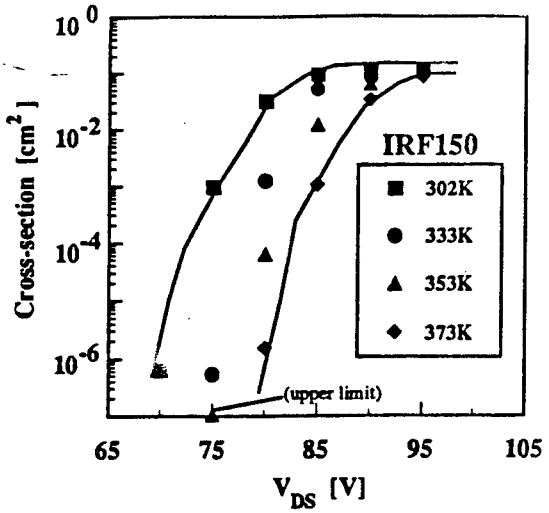


Figure 3: SEB Cross-section versus V_{DS} and temperature for the IRF150 power MOSFET (solid lines drawn to guide the eye).

increases, the amount of change in the cross-section decreases. In other words, the burnout susceptibility decreases with increasing temperature, and the change in burnout susceptibility due to temperature decreases with increasing drain-source bias. This can be explained physically through the dependence of the impact ionization rate for electrons on temperature and electric field. The impact ionization rate for electrons decreases with increasing temperature and decreasing electric field. The data presented in Figures 2-3 are consistent with previously reported data [6]. These points and their relevance to the SEB mechanism will be explained in more detail in the next section.

IV. Burnout Modeling

This section will focus on the physical model of the burnout mechanism. First, the mechanism leading to burnout via the turn on of the parasitic bipolar transistor will be reviewed. Next, the manner in which temperature dependence is incorporated into the model will be discussed.

IVA. Burnout Mechanism of DMOS Structure

The cross-section of one cell in an n-channel DMOS power transistor is shown in Figure 4. A positive bias applied to the gate forms an inversion layer in the p-body region below the gate oxide, allowing electrons to flow from the source to the drain. Inherent to the DMOS structure is a parasitic npn bipolar transistor, as shown in Figure 4. The source, body, and drain regions of the MOSFET comprise the emitter, base, and collector regions of the parasitic BJT, respectively. In normal operation of the power MOSFET, this parasitic BJT is always turned off. This is accomplished by the common source-body metallization, which shorts out the base-emitter junction of the parasitic BJT.

If lateral current flows in the body (base) below the source (emitter) region, the base-emitter junction becomes forward biased and the parasitic BJT turns on. Single-event burnout of the DMOS structure has been attributed to the turn on of this parasitic BJT [3]. If the parasitic BJT is turned *ON* when the MOSFET is turned *OFF*, second breakdown of the BJT and hence thermal meltdown (burnout), may occur. The mechanism leading to SEB will now be discussed.

Figure 4 shows the DMOS structure with a heavy ion passing through the parasitic BJT. As the heavy ion traverses the device, electron-hole pairs are generated along its track length, creating an ionized plasma filament. This plasma filament supports a short-lived current source in which holes flow up towards ground via the lateral base region, and electrons flow down towards the positively biased collector. The short-lived current source initially drives the parasitic BJT, locally turning on one cell of the DMOS structure [7].

Depending on how 'hard' the BJT is initially turned *ON*, the currents within the device will either regeneratively increase until burnout occurs, or the currents will die out leaving the

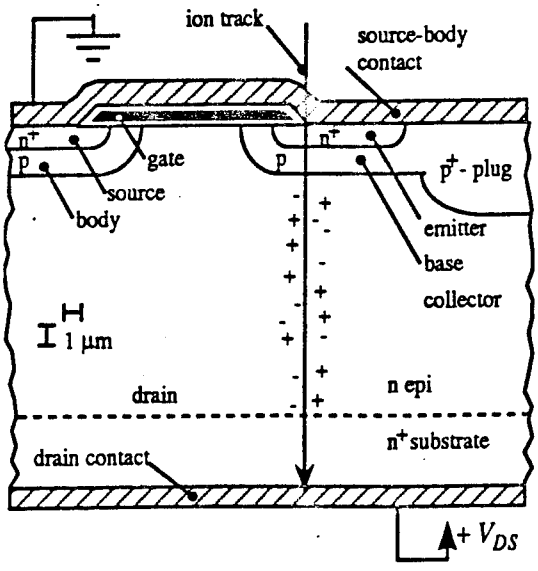


Figure 4: DMOS structure showing parasitic BJT and ion track.

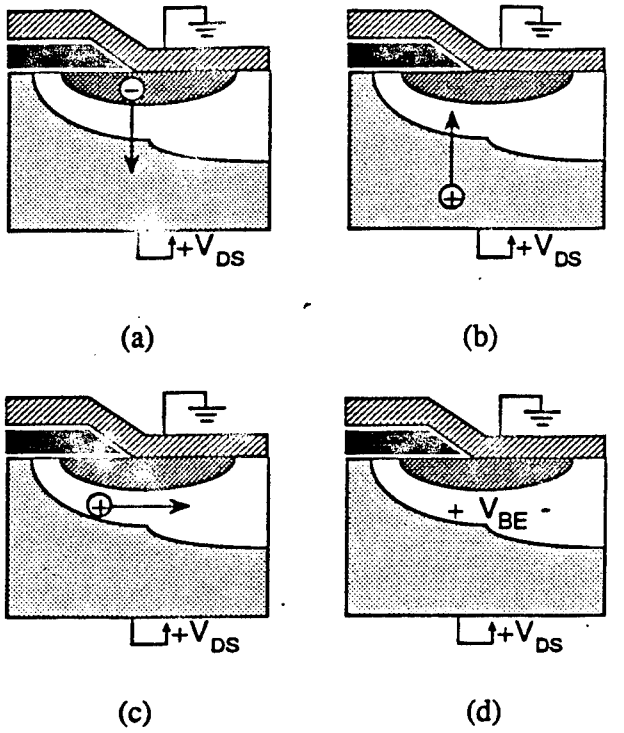


Figure 5: Components in feedback mechanism: (a) electron injection; (b) avalanche generated holes; (c) base current; (d) base-emitter voltage.

device unharmed. A feedback mechanism inherent to the vertical structure of the parasitic BJT will determine whether the currents will regeneratively increase or die out. The feedback mechanism consists of four basic components. These components in terms of the parasitic BJT are: (1) electron injection from the emitter across the active base into the collector; (2) avalanche-generated hole current returning from the collector into the base; (3) subsequent lateral hole current through the base to its contacts; and (4) the induced base-emitter voltage resulting from the lateral base current. The four components of the feedback mechanism are illustrated in Figure 5.

When the equations governing the feedback mechanism are solved, electron and hole current density distributions within the parasitic BJT are obtained which define the threshold for burnout [8]. The current density distributions at the threshold for burnout are called the critical condition. If the parasitic BJT is initially driven by the heavy-ion-generated current source such that currents are larger than the critical condition, then burnout occurs. If not, then the currents within the parasitic BJT die out and burnout does not occur [8].

It should be noted that in this model it seems that the position of the incident ion strike may influence how hard the parasitic BJT is driven. Incidence at the outer edge of the source region is worst case in the sense that an incident ion with the lowest LET capable of initiating burnout must strike there. At the source edge, an incident ion with a relatively low LET may induce burnout, but the same ion could not induce burnout if it were incident closer to the ground edge of the source. As one moves to positions more interior in the source region, incident ions must have higher and higher values of LET to initiate burnout. Positions more interior in the source region correspond to larger effective sensitive regions. Experimental cross-section versus LET curves show a similar trend. As the LET of the incident ion is increased, the measured cross-section increases. This same argument can be made with the cross-section versus drain-source bias curves for a constant LET that are given in this paper. As the drain-source bias is increased, an ion with the same LET can strike futher into the source region and still initiate burnout. Thus, as the drain-source bias increases, so does the sensitive region.

The temperature dependence of the burnout mechanism can be readily introduced into this feedback mechanism and will now be outlined.

IVB. Temperature Dependence

In the foregoing discussion, it should be emphasized that the primary component of the burnout mechanism is the base current density flowing in the parasitic BJT. In order for the parasitic BJT to turn on and remain turned on, it must have a source of base current. Unlike 'normal' BJT operation, the base current is not supplied from a device terminal; rather, the base current is supplied through avalanche multiplication in the base-collector space charge region (SCR). It will later be shown that the hole current generated in the base-collector SCR is a function of the doping density and thickness of the collector region, the applied drain-source bias, and the local injected electron density [8]. In the following discussion on the temperature dependence of the burnout mechanism, the focus will be on the base current generated through avalanche multiplication. In other words, the injected electron density will be held 'constant' as a function of temperature, and the change of avalanche generated holes will be

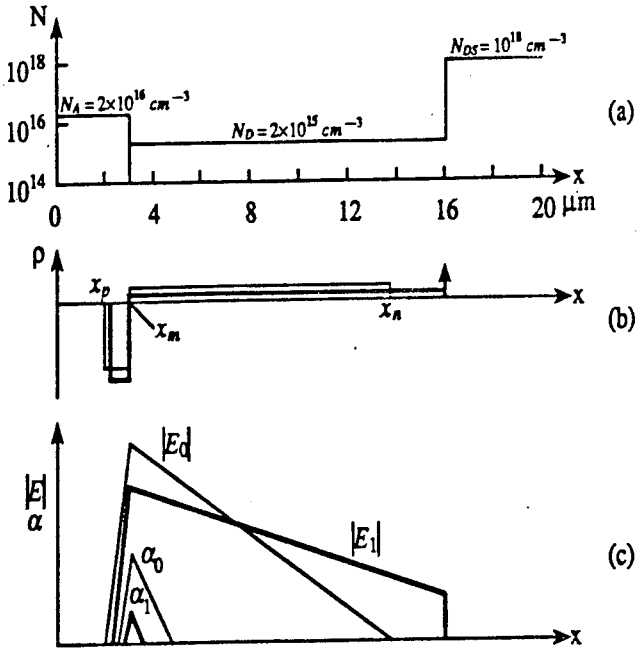


Figure 6: (a) idealized doping densities in base-collector space charge regions; (b) charge densities for zero and nonzero currents; and (c) electric field and impact ionization rate profiles for zero and nonzero currents.

monitored as a function of temperature. This is equivalent to accounting for the 2-3mV/°C decrease of base-emitter voltage in the parasitic BJT.

As mentioned previously, the avalanche generated hole current is a function of the doping density and thickness of the collector region, applied drain-source voltage, and the local injected electron density within the base-collector space charge region. The complete details for calculating the avalanche generated hole current appear in [8]. Only the major points will be described here.

The one dimensional Poisson equation is solved across the base collector depletion region taking into account the space charge associated with the mobile carriers. When the space charge of the mobile carriers is considered, the electric field across the base collector space charge region will be somewhat altered, depending on the density of mobile charge compared to the density of background impurity charge. A qualitative illustration of how the electric field is changed is shown in Figure 6 [8]. An idealized impurity profile through the base, collector, and substrate of the parasitic BJT in a typical power MOSFET is shown in Figure 6a. The two cases of zero and non-zero current are depicted in Figures 6b and 6c. The light lines correspond to the zero current case, and the heavy lines correspond to the non zero current case. The electric field and ionization rate plots are further labelled with the subscripts 0 and 1 to distinguish between zero and non-zero currents respectively. The total charge density for the non-zero current case, shown in Figure 6b, has changed to reflect the electrons in transit across the junction. The total charge density to the left of the metallurgical junction, x_m, is more negative (the electrons add to the total charge), and the total charge density to the right of the metallurgical junction is less positive than for the zero current case (the electrons subtract from the total charge).

The change in the total charge density is also reflected in the electric field distribution, shown in Figure 6c. Since the total charge density is more negative to the left of x_m for non-zero current, the electric field in this region will have a steeper slope than for the zero current case. This effectively lowers the peak electric field at x_m and moves x_p to the right. Similarly, since the total charge density is less positive to the right of x_m for non-zero current, the electric field in this region will have a lower gradient than for the zero current case. Since the reverse bias for each case is the same, the area under each electric field plot must be equal. This equal area constraint and the lower slope to the right of x_m, push the right edge of the electric field, x_n, deeper into the collector region. In the example shown in Figure 6c, x_n, has reached the epi-substrate boundary at which point the electric field can penetrate no further. The electric field will assume a non-zero value at the epi-substrate boundary to satisfy the equal area constraint imposed by the boundary conditions of the Poisson equation. Therefore, two important phenomena occur in the reverse biased base collector junction when non-zero current flows: (1) the peak electric field at the metallurgical junction decreases, and (2) the electric field assumes a non-zero value at the epi-substrate interface. These two consequences significantly affect the avalanche multiplication, as will be shown later.

The impact ionization rate, α, throughout the depletion region for zero and non-zero current is also shown in Figure 6c. The impact ionization rate, α, is exponentially related to the local electric field [8]. This is why the value of α decreases significantly when the peak electric field drops with increasing current. The avalanche multiplication rate, M, significantly decreases with increasing current as well. The functional relationships between carrier densities, electric field, ionization rate, applied

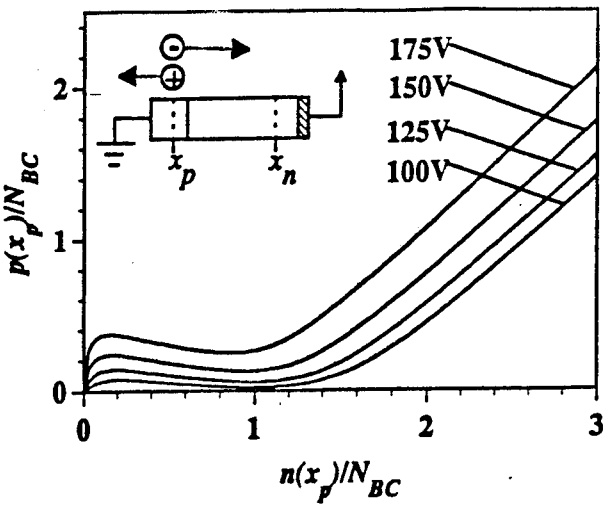


Figure 7: Avalanche curves at 300K for 100 V, 125 V, 150 V, and 175 V for device with nominal breakdown voltage of 190 V.

voltage, and the physical geometry of the parasitic BJT must be simultaneously solved to determine the avalanche multiplication rate, i.e., the density of avalanche generated holes returning to the neutral base for a given injected electron density.

Recall that the desired result is the hole concentration at x_p, $p(x_p)$, as a function of electron concentration at x_p, $n(x_p)$, or:

$$M = \frac{p(x_p)}{n(x_p)}. \qquad (1)$$

There are six arrays of typically 300 points used in the calculation (the depletion region is discretized into 300 points). These arrays are: (1) space charge, $\rho(x)$; (2) electric field, $E(x)$; (3) potential, $V(x)$; (4) ionization rate, $\alpha(x)$; (5) electron concentration, $n(x)$; and (6) hole concentration, $p(x)$. Given the impurity profile, the applied drain to source voltage, V_{DS}, and the electron concentration at x_p, the profiles of $\rho(x)$, $E(x)$, $V(x)$, $n(x)$, $p(x)$, and $\alpha(x)$ are calculated for self-consistency [8].

The equations, sample calculations of electric field, ionization rate, potential, carrier densities, and other details of this calculation appear in [8]. The end result is plotted in Figure 7, which shows the calculated avalanche curves for a device with a nominal BV_{DS} of 190 V. There are three distinct regions present in each avalanche curve shown in Figure 7. The first region is the distinct hump appearing for values of $n(x_p)/N_D < 1$. This corresponds to an initial decrease in the avalanching rate with increasing current. The second region is the valley region or local minimum appearing for values of $n(x_p)/N_D \approx 1$. This corresponds to a near zero avalanching rate at a current level where the injected electron density and collector doping density are comparable. The third region of the avalanche curve appears for values of $n(x_p)/N_D > 1$, where the hole concentration increases at approximately the same rate as the electron concentration.

In terms of the feedback mechanism for SEB, the appropriate value for M can be obtained from a curve similar to Figure 7. Note that it is necessary to calculate a separate avalanche curve for each device structure and each applied drain-source bias when solving the equations governing the feedback mechanism.

The temperature dependence is included in the aforementioned calculation via the impact ionization rate. The impact ionization rate (number of electron-hole pairs generated per unit path length) decreases with increasing temperature [9]. This is attributed to the shorter mean free path of the carriers. Since the impact ionization rate is used explicitly in the solution to the Poisson equation, the avalanche-generated hole current density decreases with increasing temperature for the same injected electron current density and applied drain-source bias. A measure of the reduction in hole current density is shown in Figure 8. The ratio of the hole density retuning to the base at 400 K, p_{400}, and the hole density at 300 K, p_{300}, is plotted as a function of the electron density, n, injected into the base-collector space charge region of the parasitic BJT. The electron density has been normalized to the doping density in the collector, N_D. Note that the hole density at 400 K ranges from 30% to 90% of the hole

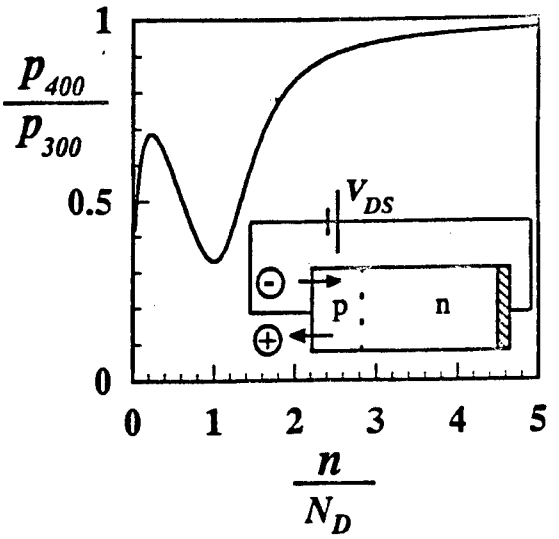


Figure 8: Ratio of avalanche curves at 400 K and 300 K.

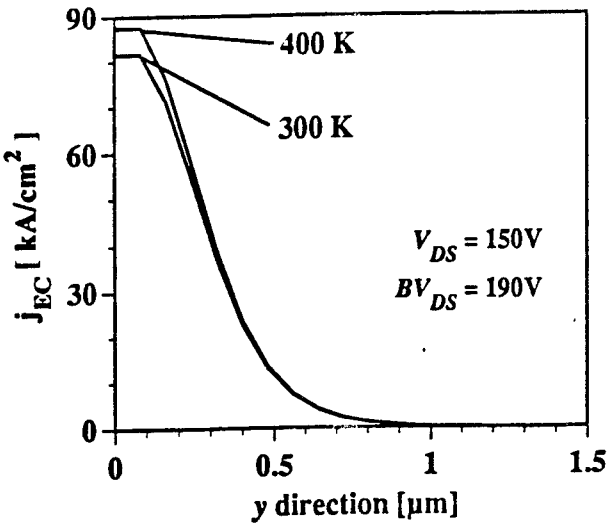


Figure 9: Critical electron current density distribution in the collector at the threshold for burnout with drain-source bias of 150 V at 300 K and 400 K.

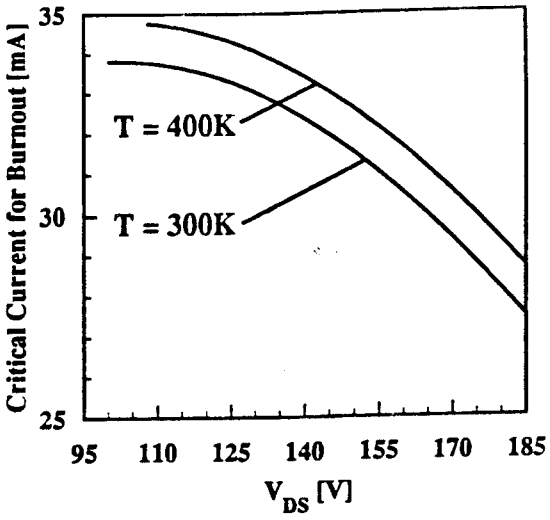


Figure 10: Calculated SEB threshold as a function of temperature and drain-source bias.

density at 300 K over much of the operating region. This reduction of the source of base current at higher temperatures is equivalent to an increase of the burnout threshold of the device (ie, in order to achieve the same level of base current, the electron current density in the collector must increase). The calculated temperature dependence of the burnout threshold will be presented in the next section.

V. Calculated Temperature Dependence

The relationships governing the feedback mechanism can be solved to yield a collector current density distribution at the threshold for burnout, j_{EC}, for a given DMOS device structure [8]. Figure 9 shows the threshold j_{EC} plotted against position in the parasitic BJT for temperatures of 300K and 400K. These calculations indicate that the peak j_{EC} increases from 81.5 kA/cm^2 to 87.5 kA/cm^2 when the temperature increases from 300K to 400K. When the critical collector current density is integrated around one cell of the DMOS structure, a critical collector current for burnout is obtained. The critical collector current for burnout, calculated as a function of drain-source voltage and for ambient temperatures of 300K and 400K, is plotted in Figure 10. The device structure used in these calculations has a nominal breakdown voltage of 190V. The device structure used in the calculations is similar to the experimental samples only in the sense that they each have similar values of BV_{DS}. No attempt was made to determine actual dimensions and doping distributions of the experimental samples. For the calculations, the average doping densities in the source, p-body, p$^+$-plug, and drain region are 10^{21} cm^{-3}, 2×10^{17} cm^{-3}, 2×10^{19} cm^{-3}, and 2×10^{15}cm^{-3}, respectively. The thickness of the drain region is 13 μm. As shown in Figure 10, the SEB threshold increases with increasing temperature and decreasing voltage. Note that an increase of the critical current increases the SEB threshold. Furthermore, the increase of the SEB threshold is more pronounced at the lower drain-source biases. Once again, this is a result of the temperature and electric field dependence of the impact ionization rate for electrons. Therefore, the SEB threshold has increased by approximately 2.9% for a 100 degree temperature increase at the higher drain-source biases, and the SEB threshold has increased by approximately 4.4 % at the lower drain-source biases. These results are consistent with the experimental trends previously discussed.

VI. Summary and Conclusions

In this paper, the temperature dependence of SEB in power DMOS devices was discussed. Experimental data for the IR6766 and IRF150 power MOSFETs were presented. The data indicate a definite temperature dependence of the burnout cross-section and in the threshold value of drain-source bias required for burnout. Temperature dependence was included in an existing SEB model through the impact ionization rate, and the

calculated results agreed with the experimental trends.

From the results presented in this paper, one can conclude that power DMOS devices are more resistant to SEB when operated at an elevated temperature. This is an important issue for systems that may be operated outside of the 300 K regime in the space radiation environment.

VII. ACKNOWLEDGEMENTS

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II.C. Simulating Single-Event Burnout of N-Channel Power MOSFETs

Simulating Single-Event Burnout of n-Channel Power MOSFET's

Gregory H. Johnson, *Member, IEEE*, Jakob H. Hohl, *Senior Member, IEEE*, Ronald D. Schrimpf, *Member, IEEE*, and Kenneth F. Galloway, *Fellow, IEEE*

Abstract—**Heavy ions are ubiquitous in a space environment. Single-event burnout of power MOSFET's is a sudden catastrophic failure mechanism that is initiated by the passage of a heavy ion through the device structure. The passage of the heavy ion generates a current filament that locally turns on a parasitic n-p-n transistor inherent to the power MOSFET. Subsequent high currents and high voltage in the device induce second breakdown of the parasitic bipolar transistor and hence meltdown of the device. This paper presents a model that can be used for simulating the burnout mechanism in order to gain insight into the significant device parameters that most influence the single-event burnout susceptibility of n-channel power MOSFET's.**

Nomenclature

α	Impact ionization rate.
E	Electric field.
ϵ	Dielectric constant of silicon.
I_{on}	Current that turns on parasitic bipolar transistor.
i_B	Local base current density.
j_{EC}	Electron current density in collector.
j_{HB}	Incremental hole current density in base.
j_{HC}	Avalanche generated hole current density.
j_{HE}	Back-injected hole current density in emitter.
k	Boltzmann constant.
M	Avalanche multiplication factor.
μ_n	Electron mobility.
μ_p	Hole mobility.
N	Total number of carriers per unit filament length.
N_{BC}	Background concentration in collector.
n_i	Intrinsic carrier density.
N_{AB}	Average doping density in base.
n	Electron density.
p	Hole density.
q	Electronic charge.
R_B	Base sheet resistance.
ρ	Charge density.
V_{BE}	Base-emitter voltage.
V_{BI}	Built-in junction potential.
v_{sat}	Saturation velocity.
w	Epitaxial region thickness.
w_B	Active base width.
x_m	Metallurgical junction.
x_p	Base edge of base-collector space-charge region.
y_e	Lateral extent of p^+ plug.
y_p	Position of p-body and p^+ plug interface.
y_s	Length of n^+ source region.

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I. Introduction

THE double-diffused metal-oxide-semiconductor (DMOS) power device is capable of conducting large currents when turned on and withstanding large voltages when turned off [1]. As system designers began using DMOS devices for space applications, heavy-ion-induced single-event burnout (SEB) was identified as a catastrophic failure mechanism [2]. Following SEB, the drain and source contacts of the MOSFET are typically shorted together, and the device can no longer function as a switch. If SEB were to occur in the power supply system of a satellite or a high-altitude aircraft, the results could be catastrophic.

Since heavy ions are always present in space [3], devices operating in this environment should be designed to be immune to their effects. An overview of the SEB mechanism in the DMOS device is presented in Section II of this paper. It will be shown that the SEB mechanism can be separated into two parts: 1) the initial heavy-ion-induced current filament which drives the parasitic BJT, and 2) the feedback mechanism inherent to the parasitic BJT. The heavy-ion-induced current filament is briefly discussed in Section III of this paper. The feedback mechanism determines whether the transient currents in the parasitic BJT will regeneratively increase until burnout occurs or whether the currents decrease to zero. The feedback mechanism is presented in Section IV of this paper where the operation of the parasitic BJT is discussed. The two parts of the SEB mechanism are then combined in Section V to determine the SEB threshold in terms of the linear energy transfer (LET) of the incident ion for a given device structure and operating conditions. Finally, conclusions of this work are drawn in Section VI.

II. Burnout Mechanism

The cross section of one cell in an n-channel DMOS power transistor is shown in Fig. 1. Since this is an

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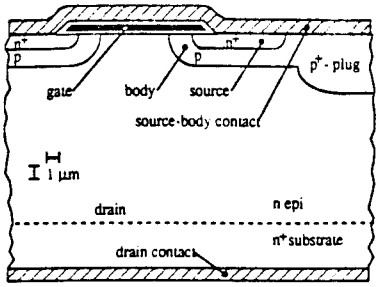


Fig. 1. Cross section of a typical DMOS cell.

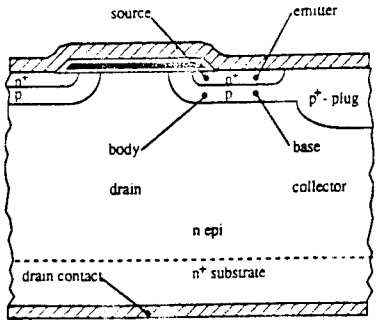


Fig. 2. Parasitic n-p-n transistor inherent to DMOS structure.

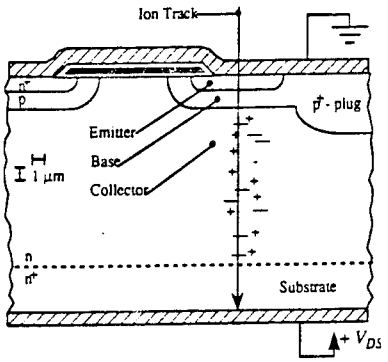


Fig. 3. DMOS structure with heavy-ion track.

n-channel device, a positive gate bias will invert the body region under the gate, and enable electrons to flow from the source to the drain in each of the cells in the DMOS device. Inherent to the DMOS structure is a parasitic n-p-n bipolar transistor, as shown in Fig. 2. The source, body, and drain regions of the MOSFET comprise the emitter, base, and collector regions of the parasitic BJT, respectively. In normal operation of the power MOSFET, this parasitic BJT is always turned off. This is accomplished by the common source–body metallization, which shorts out the base–emitter junction of the parasitic BJT.

If lateral current flows in the body (base) below the source (emitter) region, the base–emitter junction can become forward-biased and the parasitic BJT can turn on. If the parasitic BJT turns on while the power MOSFET is in the *OFF*-state, the simultaneous high current and high voltage may induce second breakdown, hence thermal meltdown. This was the motivation for the prominent p^+-plug region of the DMOS structure [4]. Many power MOSFET applications require the device to switch currents through highly inductive loads. This can result in large current spikes while in the *OFF*-state. These current spikes are directed through the p^+-plug regions and not through the parasitic BJT because of the lower impedance path. This prevents second breakdown of the parasitic BJT, and hence damage to the power MOSFET, when switching inductive loads.

Single-event burnout of the DMOS structure has been attributed to this parasitic BJT [5]. The mechanism leading to SEB will now be briefly discussed. Fig. 3 shows the DMOS structure with a heavy ion passing through the parasitic BJT. As the heavy ion traverses the device, electron–hole pairs are generated along its track length creating an ionized plasma filament. This plasma filament supports a short-lived current source in which holes flow up towards ground via the lateral base region, and electrons flow down towards the collector. The short-lived current source initially drives the parasitic BJT locally turning on one cell of the DMOS structure [6].

Depending on how "hard" the BJT is initially turned *ON*, the currents within the device will either regeneratively increase until burnout occurs, or the currents will die out leaving the device unharmed. A feedback mechanism inherent to the vertical structure of the parasitic BJT will determine whether the currents will increase or decrease. The feedback mechanism consists of four basic components. These components in terms of the parasitic BJT are 1) electron injection from the emitter across the active base into the collector, 2) avalanche-generated hole current returning from the collector into the base; 3) subsequent lateral hole current through the base to its contacts; and 4) the induced base–emitter voltage resulting from this lateral base current. The details of each part in the SEB mechanism will be discussed in the sections to follow.

III. Heavy-Ion-Induced Current Filament

The parasitic BJT is turned on by a localized current source generated by the passage of the heavy ion. This heavy-ion-generated current filament will be referred to as the initial current source henceforth. A simple model that discusses the time evolution of the initial current source is given in [5]. In this model, the evolution of the current source is governed by the radial diffusion of the filament. This model serves as a first-order analysis, and its intent is to lend basic insight into this phenomenon. A more detailed description of the current filament evolution certainly merits an investigation in itself. As developed in [5], the resulting current that drives the parasitic BJT in terms of the energy deposited by the heavy ion is expressed as

$$I_{on} = qv_{sat}N. \tag{1}$$

IV. Parasitic BJT Operation

This section will address the operation of the parasitic BJT following an ion strike. First, the feedback mecha-

nism that governs whether the currents within the parasitic BJT will regeneratively increase or die out to zero will be discussed. In the development of the feedback mechanism, it will become apparent that an expression for avalanche-generated hole current in the base–collector space-charge region of the parasitic BJT is necessary. This relationship will be described in the second subsection.

A. Feedback Mechanism

Depending on how hard the parasitic BJT is initially turned on, currents within the device will either 1) regeneratively increase until the simultaneous high current and high voltage in the device trigger second breakdown and consequently thermal meltdown; or 2) the currents will die out to zero leaving the device unharmed. A feedback mechanism inherent to the device structure dictates whether the currents will regeneratively increase or decrease.

The feedback mechanism relates 1) electron injection from the emitter across the active base into the collector; 2) avalanche-generated hole current returning from the collector into the base; 3) subsequent lateral hole current through the base to its contacts; and 4) the induced base–emitter voltage resulting from this lateral base current [7]. The equations governing the feedback mechanism will now be discussed.

The coordinate system for this discussion is shown in Fig. 4. The origin is defined at the point of the ion strike, which is assumed to be at the drain edge of the MOSFET channel. The regions labeled E, B, and C are the emitter, base, and collector of the parasitic BJT. The region R_{B2} in the base is the p^+-plug region, and the region R_{B1} is the p-body region. The length of the source region in the y direction is defined as y_s, and the p-body p^+-plug interface is defined as y_p. The extent that the p^+-plug extends under the n^+-source region, y_e, is defined as the difference between y_s and y_p.

Now, assuming a potential $V_{BE}(y)$ exists that is large enough to locally turn on the parasitic BJT, the electron current density injected by the emitter $j_{EC}(y)$ can be expressed to first order by [8]

$$j_{EC}(y) = \frac{qD_n n_i^2}{N_{AB} w_B} \exp\left[\frac{V_{BE}(y)}{kT/q}\right]. \tag{2}$$

Note that this current density is not shown in Fig. 4 to avoid confusion.

Since the base–collector junction has a large reverse bias applied across it, the electric field will be large throughout much of the collector region. Therefore, for each electron injected across the base into the collector, there will be avalanche-generated holes returning to the base region. The avalanche-generated hole current density $j_{HC}(y)$ is given by [7]

$$j_{HC}(y) = Mqv_{\text{sat}}\left\{\frac{D_n n_i^2}{v_{\text{sat}} N_{AB} w_B} \exp\left[\frac{V_{BE}(y)}{kT/q}\right]\right\}. \tag{3}$$

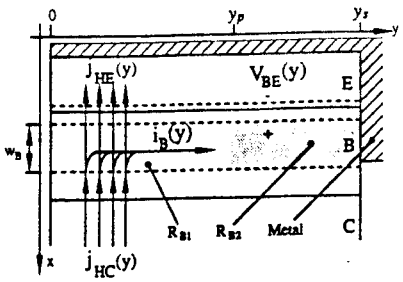


Fig. 4. Feedback model of parasitic bipolar junction transistor.

The multiplication factor M in (3) is defined as the ratio of the hole density to the electron density at the base side of the base–collector space-charge region. M is a function of the electric field, ionization rate, and the injected electron density, and is obtained numerically [7]. The multiplication factor M will be discussed later in this section. The term within the curly brackets in (3) is the electron density at the base edge of the base–collector space-charge region, including the Kirk effect [9].

Due to the forward bias $V_{BE}(y)$, there also exists a back-injected hole current density $j_{HE}(y)$. This current density is expressed to first order by [8]

$$j_{HE}(y) = \frac{qD_n n_i^2}{N_{DE} L_p} \exp\left[\frac{V_{BE}(y)}{kT/q}\right]. \tag{4}$$

There is one remaining current in the feedback mechanism to be described. This is the incremental hole current density which flows laterally through the neutral base region to the ground contact and develops the Ohmic drop necessary to keep the base–emitter junction foward-biased. The value of this incremental current density $j_{HB}(y)$ at any point y is simply the difference between the avalanche-generated hole current density and the back-injected hole current density, which is

$$j_{HB}(y) = j_{HC}(y) - j_{HE}(y). \tag{5}$$

A second-order differential equation can be formulated that relates the Ohmic drop to the current density in the neutral base region [7]. First, the incremental lateral base current is just the local incremental base current density

$$\frac{di_B(y)}{dy} = j_{HB}(y). \tag{6}$$

Second, the incremental voltage drop is given by

$$\frac{dV_{BE}(y)}{dy} = -R_B(y) i_B(y). \tag{7}$$

Equations (6) and (7) can be combined to give

$$\frac{d^2 V_{BE}(y)}{dy^2} = -R_B(y) j_{HB}(y). \tag{8}$$

Equations (3)–(5) and (8) can be solved to obtain a critical condition necessary to initiate burnout [7]. This calculation will be illustrated for a specific device structure. Note that this calculation will involve numerically obtained values of the avalanche multiplication factor M.

The critical condition will now be calculated for a typical DMOS structure. The following parameters are used in the calculations: source doping density = 2×10^{20} cm^{-3}, p-body doping density = 2×10^{16} cm^{-3}, p^+-plug doping density = 2×10^{18} cm^{-3}, drain doping density = 1.1×10^{15} cm^{-3}, source diffusion depth = 1 μm, p-body diffusion depth = 2 μm, p^+-plug diffusion depth = 4 μm, and epitaxial layer thickness = 22 μm. The average doping densities needed in this abrupt junction calculation were obtained from Gaussian-type doping profiles.

The solution to (3)–(5) and (8) is shown in Figs. 5–7. The collector bias for this case is 250 V. Shown in Fig. 5 is the incremental hole current density profile in the base region. The base current per gate width is shown in Fig. 6, and the base-emitter voltage is shown in Fig. 7. These curves represent the critical condition for burnout because any heavy-ion-generated perturbation in the system larger than that given in Figs. 5–7 will result in regeneratively increasing currents within the device and thus burnout will occur [7]. If the heavy-ion-generated perturbation is less than that given in Figs. 5–7, the currents will decay to zero and burnout will not occur.

B. Avalanche-Generated Holes

This section of the paper will discuss the avalanche multiplication factor M, which appears in the equations governing the feedback mechanism. As mentioned previously, M is a function of the electric field, impact ionization rate, and electron density within the base–collector space-charge region. The complete details of this calculation appear in [7]. Only the major points will be described here. The one-dimensional Poisson equation will be solved across the base–collector depletion region taking into account the space charge associated with the mobile carriers.

When the space charge of the mobile carriers is considered, the electric field across the base collector space-charge region will be somewhat altered, depending on the density of mobile charge compared to the density of background impurity charge. A qualitative illustration of how the electric field is changed is shown in Fig. 8 [7]. An idealized impurity profile through the base, collector, and substrate of the parasitic BJT in a typical power MOSFET is shown in Fig. 8(a). The two cases of zero and nonzero current are depicted in Fig. 8(b) and (c). The light lines correspond to the zero current case, and the heavy lines correspond to the nonzero current case. The electric field and ionization rate plots are further labeled with the subscripts 0 and 1 to distinguish between zero and nonzero currents, respectively. The total charge density for the nonzero current case, shown in Fig. 8(b), has changed to reflect the electrons in transit across the junction. The total charge density to the left of the metallurgical junction x_m is more negative (the electrons add to the total charge), and the total charge density to the right of the metallurgical junction is less positive than for the zero current case (the electrons subtract from the total charge).

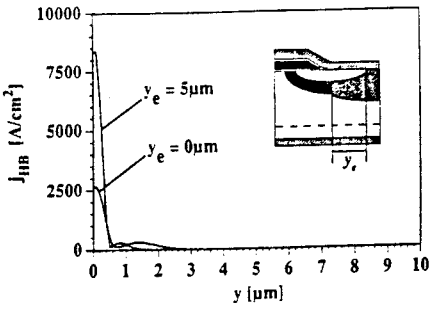


Fig. 5. Critical incremental base current density for burnout.

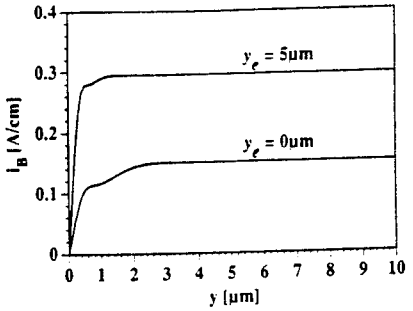


Fig. 6. Critical base current density for burnout.

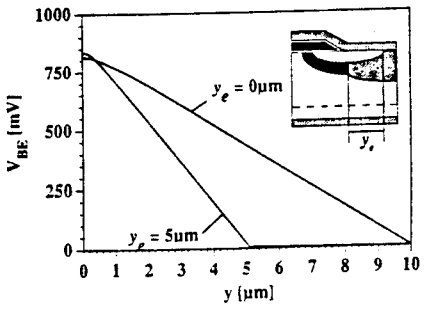


Fig. 7. Critical base-emitter voltage for burnout.

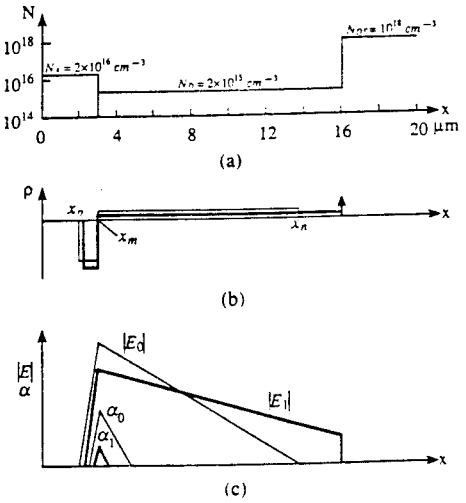


Fig. 8. (a) Approximated p-n-n^+ impurity profile. (b) Charge density in space-charge region for zero and nonzero currents. (c) Electric field and ionization rate in space-charge region for zero and nonzero currents.

The change in the total charge density is also reflected in the electric field distribution, shown in Fig. 8(c). Since the total charge density is more negative to the left of x_m for nonzero current, the electric field in this region will have a steeper slope than for the zero current case. This effectively lowers the peak electric field at x_m and moves x_p to the right. Similarly, since the total charge density is less positive to the right of x_m for nonzero current, the electric field in this region will have less of a gradient than for the zero current case. Since the reverse bias for each case is the same, the area under each electric field plot must be equal. This equal area constraint and the lower slope to the right of x_m push the right edge of the electric field x_n deeper into the collector region. In the example shown in Fig. 8(c), x_n has reached the epi-substrate boundary at which point the electric field can penetrate no further. The electric field will assume a nonzero value at the epi-substrate boundary to satisfy the equal area constraint imposed by the Poisson equation. Therefore, two important phenomena occur in the reverse-biased base-collector junction when nonzero current flows: 1) the peak electric field at the metallurgical junction decreases, and 2) the electric field assumes a nonzero value at the epi-substrate interface. These two consequences significantly affect the avalanche multiplication, as will be shown later.

The impact ionization rate α throughout the depletion region for zero and nonzero current is also shown in Fig. 8(c). The functional dependence of α is exponentially related to the local electric field. This is why the value of α decreases significantly when the peak electric field drops with increasing current. We would expect the avalanche multiplication rate to significantly decrease with increasing current as well. The functional relationships between carrier densities, electric field, ionization rate, applied voltage, and the physical geometry of the parasitic BJT must be simultaneously solved to more precisely determine the avalanche multiplication rate.

Recall that the desired result is the hole concentration at x_p, $p(x_p)$, as a function of electron concentration at x_p, $n(x_p)$, or

$$M = \frac{p(x_p)}{n(x_p)}. \tag{9}$$

There are six arrays of typically 300 points used in the calculation (i.e., the space-charge region is discretized into 300 intervals). These arrays are: 1) space charge, $\rho(x)$; 2) electric field $E(x)$; 3) potential, $V(x)$; 4) ionization rate $\alpha(x)$; 5) electron concentration $n(x)$; and 6) hole concentration $p(x)$. Given the impurity profile, the applied drain to source voltage V_{DS}, and the electron concentration at x_p, the profiles of $\rho(x)$, $E(x)$, $V(x)$, $n(x)$, $p(x)$, and $\alpha(x)$ are calculated for self-consistency [7].

The equations, sample calculations of electric field, ionization rate, potential, carrier densities, and other details of this calculation appear in [7]. The end result is plotted in Fig. 9. There are three distinct regions present in each avalanche curve shown in Fig. 9. The first region

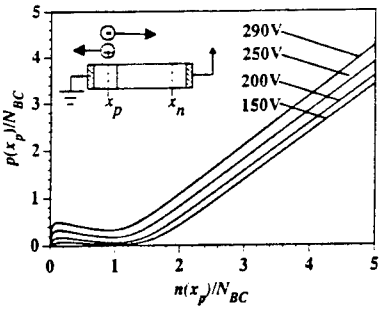


Fig. 9. Avalanche curves: normalized hole concentration at x_p versus normalized electron concentration at x_p, for different values of VDS.

is the distinct hump appearing for values of $n(x_p)/N_D < 1$. This corresponds to an initial decrease in the avalanching rate with increasing current. The second region is the valley region or local minimum appearing for values of $n(x_p)/N_D \approx 1$. This corresponds to a near-zero avalanching rate at a current level where the electron density and collector doping density are comparable. The third region of the avalanche curve appears for values of $n(x_p)/N_D > 1$, where the hole concentration increases at approximately the same rate as the electron concentration.

In terms of the feedback mechanism for SEB, the appropriate value for M can be obtained from a curve similar to Fig. 9. Note that it is necessary to calculate a separate avalanche curve for each device structure and each applied drain-source bias when solving the equations governing the feedback mechanism.

V. Calculated Burnout Thresholds

Now that each part of the model has been developed, the burnout threshold for a particular device may be calculated. The burnout threshold will be defined in terms of the linear energy transfer (LET) of the incident ion. For a first-order analysis, LET is the stopping power divided by the volume mass density of the target material (i.e., silicon in this case) [8]. The LET will be expressed in units of MeV $\cdot$ cm^2/mg for these calculations.

It is necessary to compare the magnitude of the current in the plasma filament at time t_{on} with the critical condition for burnout given by the feedback mechanism. Given the V_{BE} profile in Fig. 7, one can readily calculate the corresponding electron current density in the collector j_{EC}. This is shown in Fig. 10. To find the electron current in the collector given by the feedback mechanism, the current density shown in Fig. 10 must be integrated over one cell in the DMOS structure. A top view of the DMOS structure is shown in Fig. 11 for a square-cell geometry. An actual DMOS device may incorporate a different cell geometry (i.e., hexagonal), but a square geometry is sufficient for this discussion.

The integration of the electron current density in the collector over the DMOS cell is approximated in the following manner. First, the current density is numerically integrated in the y direction of Fig. 10. This result is then multiplied by the perimeter of the n^+-source region shown

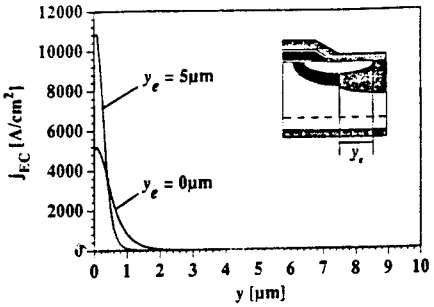


Fig. 10. Critical collector current density for burnout.

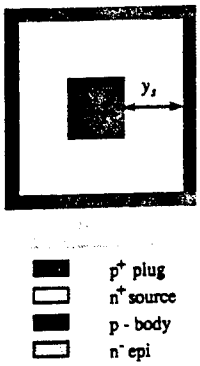


Fig. 11. Top view of a DMOS cell with metallization and gate regions omitted.

in Fig. 11. This perimeter will equal 120 μm in the following calculations. The current that is calculated in this fashion is defined as the critical current for burnout. In other words, if the ion strike results in a current greater than the critical current, then the transient currents within the parasitic BJT will regeneratively increase until second breakdown sets in. If the ion strike results in an initial current less than the critical current, then the transient currents within the parasitic BJT will die out to zero.

The following algorithm is used to calculate the LET burnout threshold for a given DMOS structure: 1) Given the structural parameters and drain–source voltage, the critical condition is calculated as in Section IV-A. 2) Given the critical condition, the critical electron current density in the collector is calculated. 3) Given the critical collector current density, the critical current is calculated as described above. 4) Equation (1) is used to calculate the LET necessary to initiate the critical current. A non-ideal scaling factor γ can be introduced at this point. This factor may be used to scale part 4) in the above algorithm when comparing to part 3). In this fashion, the model can be fitted to measured data. The device structure that will be used in the following calculation is that used for finding the critical condition in Section IV-A, with one exception. The lateral extent of the p$^+$ plug y_e where

$$y_e = y_s - y_p \tag{10}$$

(i.e., the length that it extends under the n$^+$ source as shown in Fig. 4) will be varied. For example, $y_e = 0$ μm means that the p$^+$ plug does not extend under the source region and $y_e = 5$ μm means that the p$^+$ plug extends 5 μm under the source region.

The LET burnout threshold is calculated as a function of y_e and V_{DS} using the algorithm above with $\gamma = 0.2$. The results of this calculation are shown in Fig. 12, where y_e is varied from 0 to 8 μm and V_{DS} is varied from 150 to 290 V.

VI. Discussions and Conclusions

The information contained in Fig. 12 can be helpful in designing a DMOS device to be more resistant to SEB. The LET burnout threshold for a given device structure increases with increasing y_e for a fixed drain–source bias. As one increases the extent that the p$^+$ plug extends under the source (emitter), i.e., increases y_e, the total resistance seen in the base region of the parasitic BJT decreases. When incorporated into the feedback mechanism, this necessitates higher current densities in the base region for the critical solution (i.e., the lower resistance requires a higher current to drop a comparable voltage). This suggests that p$^+$ plug should extend as far as possible below the source region to prevent burnout. The p$^+$ plug cannot extend so far as to influence the threshold voltage of the MOSFET, however. The base resistance of the parasitic BJT can also be influenced by the length of the n$^+$ source. As the length of the n$^+$ source is decreased, the base resistance is also decreased. Therefore, the LET burnout threshold increases with shorter n$^+$-source lengths. The burnout susceptibility as a function of base resistance has been shown experimentally for the case of power bipolar junction transistors. Since power BJT's have a vertical structure almost identical to that of the power MOSFET, the burnout mechanism is the same. It was shown that as the base resistance of the power BJT was reduced, the burnout susceptibility was reduced [10].

Fig. 12 also indicates that the LET burnout threshold decreases with increasing drain–source bias for a given device structure with y_e held constant. This is due to the higher electric fields associated with the increased drain–source bias. Higher electric fields increase the impact ionization rate and hence the avalanche-generated hole current that flows to the base region from the collector region of the parasitic BJT (i.e., more current is generated within the device for the same base–emitter bias). Therefore, when included in the feedback mechanism, the current required to initiate burnout decreases with increasing drain–source bias. Note that the drain–source bias dependence on the LET burnout threshold is less than the parasitic base resistance dependence. The drain–source bias dependence on the burnout susceptibility of power MOSFET's has been shown experimentally [11]. Fig. 13 shows the single-event burnout cross section versus the applied drain–source bias for the IRF150 n-channel power MOSFET. In this experiment, the nondestructive test technique was employed and a monoenergetic beam of 41 MeV · cm^2/mg Kr ions was used to irradiate the device. The cross sections were obtained by dividing the total

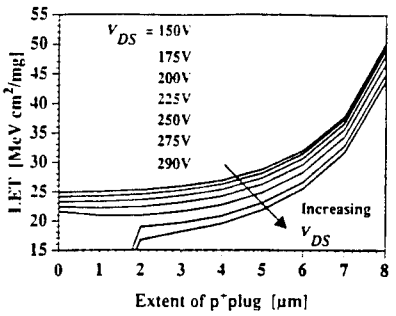


Fig. 12. LET burnout threshold as a function of y_e and V_{DS}.

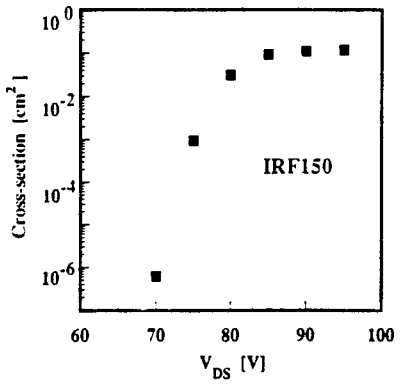


Fig. 13. Single-event burnout cross section versus applied drain-source bias irradiated with 41 MeV · cm^2/mg krypton ions.

number of nondestructive events by the total ion fluence seen by the device [11]. Therefore, the cross section is a measure of the likelihood that single-even burnout will occur. Note that as the drain-source bias is increased, the single-event burnout cross section also increases. This is in agreement with the simulated results.

In summary, a method for analyzing single-event burnout of n-channel power MOSFET's has been described. The purpose and merits of this model are intended to lend insight into the key device parameters and operating conditions that determine the single-even burnout vulnerability of a given n-channel power MOSFET. It was shown that the feedback mechanism, which related transient currents and voltages in the parasitic BJT, could be solved for a critical solution for burnout. If the currents given by the critical solution are exceeded by the heavy-ion-generated current source at the turn-on time of the parasitic BJT, then currents would regeneratively increase. The simultaneous increasing high currents and voltages trigger second breakdown of the bioplar and finally meltdown of the DMOS structure. If the initial current source does not exceed the currents given by the critical solution, then the transient currents in the parasitic BJT will die out to zero. Finally, the simulation results indicate that the LET burnout threshold increases with decreasing base resistance (either by extending the p^+ plug further under the source region, or by decreasing the n^+-source length), and that the LET burnout threshold decreases with increasing drain-source bias. The concepts can be used to design n-channel power MOSFET's with a lower sensitivity to single-event burnout.

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II.D. Analysis of the Time-Dependent Turn-On Mechanism for Single-Event Burnout of N-Channel Power MOSFETs

ANALYSIS OF THE TIME-DEPENDENT TURN-ON MECHANISM FOR SINGLE-EVENT BURNOUT OF N-CHANNEL POWER MOSFETs†

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ABSTRACT

For the first time, this paper investigates the time-dependent mechanisms involved in single-event burnout (SEB). SEB of power metal-oxide-semiconductor field-effect transistors (MOSFETs) is a catastrophic failure mechanism initiated by the passage of a heavy ion through the device structure. In previous work, analytical models have been developed to explain the regenerative feedback mechanism that induces second breakdown of the parasitic bipolar junction transistor (BJT). In this paper, a first order dynamic model is presented to lend insight into the turn-on of the parasitic BJT by the heavy ion.

I. INTRODUCTION

This paper clearly describes, for the first time, the time-dependent mechanisms involved in single-event burnout (SEB). SEB is triggered when a single heavy ion passes through sensitive regions of n-channel power metal-oxide-semiconductor field-effect transistors (MOSFETs) or npn power bipolar junction transistors (BJTs) [1-7]. Previous work has focused on developing an analytical model that explains the regenerative burnout mechanism, but has neglected the turn-on process of the parasitic bipolar transistor. This paper shows that the time constant of the bipolar transistor plays a critical role in determining burnout thresholds.

A cross-section showing the vertical structure of a typical double-diffused MOS (DMOS) n-channel power MOSFET is shown in Figure 1 [8]. The power MOSFET is vulnerable to SEB only when it is turned OFF and when it is blocking a large drain-source voltage, V_{DS}, as shown in Figure 1. Inherent to the power DMOS structure is a parasitic BJT. The source, body, and drain regions of the power MOSFET form the emitter, base, and collector regions of the power BJT. As the heavy ion passes through the parasitic BJT region of the device, electron-hole pairs are generated along its track length. The electron-hole pairs constitute a short-lived current source which acts to forward bias the parasitic BJT. Once the parasitic BJT is turned on, a regenerative feedback mechanism, relating internal device currents and voltages, exists that determines the outcome of the single-event [2, 9-10]. If the parasitic BJT is turned on hard enough, the collector current and base-emitter voltage regeneratively increase until the local power dissipation is sufficiently high to melt the device; otherwise, the currents die out and the device is unharmed [10].

Previous work has been focused on what happens after the parasitic BJT is turned on (*i.e.*, how the relationship of avalanche multiplication and BJT action lead to second breakdown of the parasitic BJT) [2, 5, 10]. In this paper, a first-order model describing the time evolution of the parasitic BJT turn-on is presented. This model shows that the strength and characteristic lifetime of the heavy ion-generated current filament, and the RC time constant of the base-emitter junction interact to determine if the parasitic BJT is forward biased sufficiently high enough to initiate SEB.

In Section II, the model is developed and the corresponding assumptions are outlined. In Section III, the model is used to generate several curves relating the base-emitter voltage versus time for various parameter changes. In Section IV, the implications of this model is discussed. Finally, the paper is summarized in Section V.

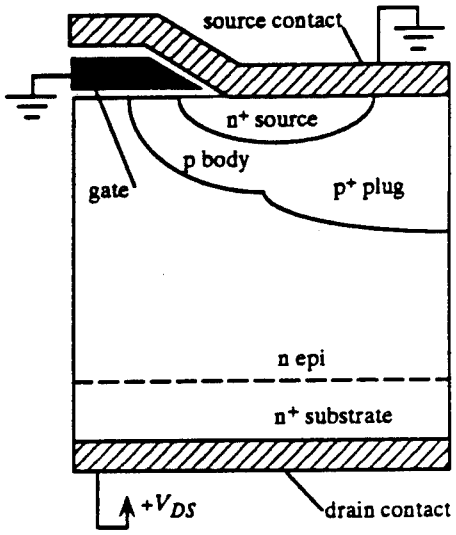


Figure 1: Cross-section of DMOS cell. The device is biased off and is blocking V_{DS}.

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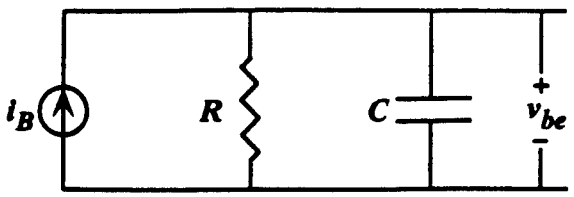


Figure 2: Circuit model for turn on analysis.

II. Modeling Parasitic BJT Turn-On

In this section, the first-order model that describes the turn on of the parasitic BJT is developed. The process of turning on the parasitic BJT by a current filament is a fairly complicated phenomenon. Two-dimensional or possibly three-dimensional device simulation codes (e.g., PISCES or PADRE) would be required to investigate all of the nuances associated with the dynamic process of turning on a comparatively large surface area device by a small radius current filament. However, the impact of this model, as with most first-order models, is the ability to understand and identify the key physical parameters that play a role in this problem. This understanding is required before production simulation can be performed.

There are two major components in this model: (1) a lumped-parameter RC charging circuit representing the resistance and capacitance of the base-emitter junction of the parasitic BJT; and (2) a voltage and time dependent current source representing the base current of the parasitic BJT. The simple circuit for the model is shown in Figure 2. The objective is to then solve for the resulting base-emitter voltage as a function of time given by:

$$C\frac{\partial v_{be}}{\partial t}+\frac{1}{R}v_{be}=i_b(v_{be},t), \tag{1}$$

where R is the junction resistance, C is the junction capacitance, v_{be} is the base-emitter voltage, and i_b is the base current. The interesting part of equation (1) (*i.e.*, the underlying physics of the problem) is the form that $i_b(t)$ takes. The components of $i_b(t)$ are: (1) a representation of the heavy ion-generated current filament; (2) the avalanche generated holes returning from the collector into the base region; and (3) the back-injected hole current into the emitter due to v_{be}. The components of the base current are illustrated schematically in Figure 3. A brief discussion of each component of the base current, including the corresponding analytical form, will follow.

The heavy ion-generated current filament is approximated as an exponentially decaying source. This approximation may not duplicate the actual shape of the current filament, but it is understood that the electron-hole pairs generated along the track length diffuse radially and drift along the track length rapidly [11]. Thus, this approximation describes the basic nature of this current filament. The equation governing the current filament, i_{ion}, is:

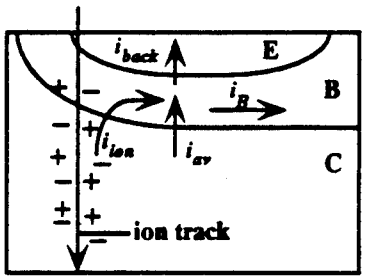
$$i_{ion}(t)=I_{ion}e^{-t/\tau_f}, \tag{2}$$

where I_{ion} is the initial current value, and τ_f is the characteristic lifetime of the current filament.

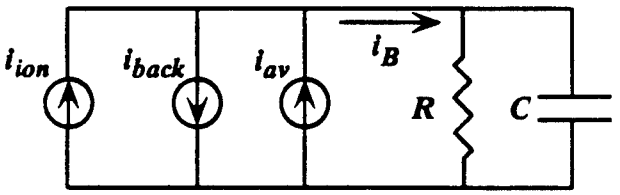
The second component of the base current is the avalanche-generated hole current. This current arises because of the large reverse bias on the base-collector junction of the parasitic BJT (recall the power MOSFET is blocking a large V_{DS}). The high electric fields present in the space charge region of this reverse-biased junction will generate electron-hole pairs for any electrons entering this region [9]. There are two components of avalanche generated hole current: (1) holes generated due to injected electrons from the emitter; and (2) holes generated due to electrons in the current filament. Thus, the avalanche generated hole current, i_{av}, is given by:

$$i_{av}(v_{be},t)=M\frac{qAD_n n_i^2}{N_{AB}w_B}(e^{v_{be}/V_T}-1)+MI_{ion}e^{-t/\tau_f}, \tag{3}$$

where M is the avalanche multiplication factor, q is the electronic charge, A is the active device area of one cell, D_n is the electron diffusivity, n_i is the intrinsic carrier density, N_{AB} is the acceptor doping density in the base region, w_B is the active base width, and V_T is the thermal voltage of the junction. Note that the first term in equation (3) is the product of the injected electron current from the emitter and the avalanche multiplication factor, and the second term is simply the product of



(a)



(b)

Figure 3: Components of the base current in (a) parasitic BJt, and (b) circuit model. In (a), the emitter, base, and colector are labeled Eand C, respectively.

equation (2) and the avalanche multiplication factor.

The third component of the base current is the back-injected hole current from the base into the emitter due to v_{be}. The back-injected hole current, i_{back}, is given by:

$$i_{back}(v_{be}) = -\frac{qAD_p n_i^2}{N_{DE}L_p}(e^{v_{be}/V_T} - 1), \quad (4)$$

where D_p is the hole diffusivity, N_{DE} is the density of donors in the emitter, and L_p is the diffusion length for holes in the emitter. The minus sign is present in equation (4) because this component of base current does not flow through the base region to ground, rather it is bled back into the emitter.

The model can now be assembled into its final form. Combining equations (1-4) yields:

$$C\frac{\partial v_{be}}{\partial t} + \frac{1}{R}v_{be} = \xi(e^{v_{be}/V_T} - 1) + (M+1)I_{ion}e^{-t/\tau_f}, \quad (5)$$

where

$$\xi = qAn_i^2\left(\frac{MD_n}{N_{AB}w_B} - \frac{D_p}{N_{DE}L_p}\right), \quad (6)$$

The initial condition for equations (5-6) is:

$$v_{be}(t=0) = 0. \quad (7)$$

III. Calculated Results

The time evolution of the base-emitter voltage of the parasitic BJT is obtained through the solution of equations (5-6). Since $v_{be}(t)$ appears in the exponential in equation (5), there does not exist an analytical solution for $v_{be}(t)$. The standard fourth-order Runge Kutta method for initial value problems was used in the following calculations [12]. The following parameters remained constant in the calculations: D_n=15.1cm²/s, D_p=5.98cm²/s, N_{AB}=10^{17}cm^{-3}, N_{DE}=10^{20}cm^{-3}, q=1.6x10^{-19}C, n_i^2=2.1x10^{20}cm^{-6}, V_T=0.026V, L_p=1μm, w_B=1μm, τ_f=10ps, and A=800μm². In Figure 4, $v_{be}(t)$ is calculated with R=50Ω, C=0.73pF, and I_{ion} (the initial strength of the ion-generated current filament) is varied from 4mA to 32mA. In Figure 5, $v_{be}(t)$ is calculated with R=50Ω, I_{ion}=28mA, and C is varied from 0.731pf to 7.31pF. Finally, in Figure 6, $v_{be}(t)$ is calculated with

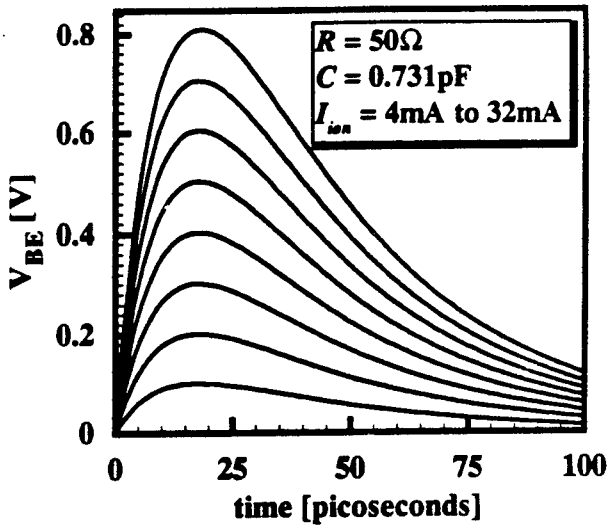


Figure 4: $v_{be}(t)$ with R and C constant. The value of I_{ion} varies from 4mA to 32mA.

C=0.731pF, I_{ion}=28mA, and R is varied from 10Ω to 90Ω.

IV. Discussion

A discussion of the calculated results shown in Figures 4-6 will now follow. Figure 4 represents the case when one device is struck by a variety of incident ion species or energies. The values of R and C are held constant and the initial strength of the heavy ion-generated current filament, I_{ion}, is varied from 4mA to 32mA. Note that the shape of each curve is the same. In fact, if the voltage scale of each curve was expanded to the appropriate value, the curves would lie right on one another. The peak voltage level is proportional to the value of the current. These results are to be expected since the time constant of the current filament and the time constant of the R-C circuit do not change. If the critical value of v_{be} (the level necessary to trigger the regenerative feedback mechanism [9,10]) were around 0.7V, only the highest curve would initiate burnout. This makes sense, since each device type has an associated threshold LET for which SEB occurs.

Figure 5 represents the case where several device types with different values of junction capacitance are struck by the same incident ion. The highest curve corresponds to the lowest capacitance and *vice versa*. An increase in the capacitance results in a decrease in peak v_{be} and a flattening out of the response. Note also that as C is increased, the initial ascent and final descent of the response decrease. These results make sense because by increasing the capacitance, the time constant of the R-C circuit increases with respect to the time constant of the heavy ion-generated current source. These results imply that if the junction capacitance is increased, the power MOSFET is less vulnerable to SEB. The junction capacitance should be increased through an increase in cell size, since the capacitance per unit area is generally fixed for a given channel length and

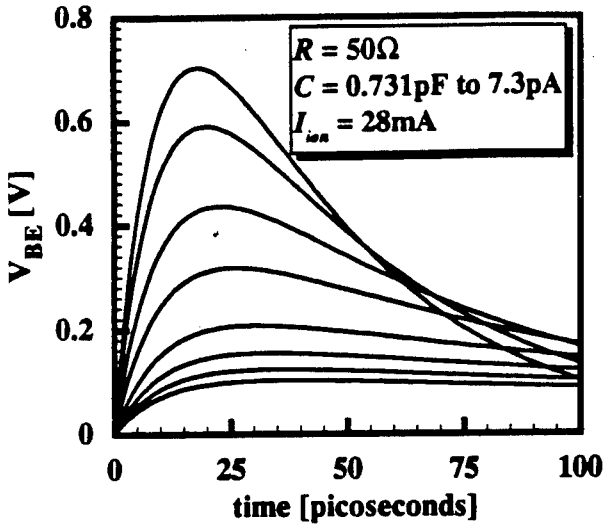


Figure 5: $v_{be}(t)$ with R and I_{ion} constant. The value of C varies from 0.731pF to 7.31pF.

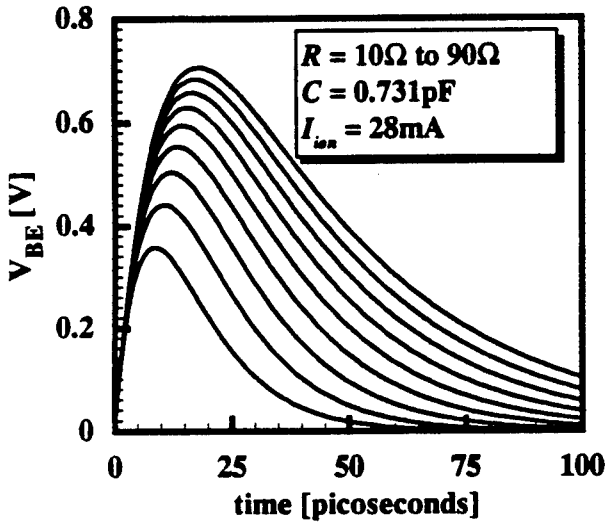


Figure 6: $v_{be}(t)$ with I_{ion} and C constant. The value of R varies from 10Ω to 90Ω.

threshold voltage of the MOSFET.

Figure 6 represents the case where several device types with different values of resistance are struck by the same incident ion. The highest curve corresponds to the highest value of resistance. As the value of R is increased, the peak value of v_{be} increases and the final descent of the response decreases. These results make sense because by increasing the resistance, one would expect the voltage to increase for the same current. Also, the flattening out in the response during the final descent is a result of the increase of the R-C circuit time constant with respect to the time constant of the heavy ion-generated current filament. Note that the initial ascent of the response remains constant when R is varied (it only depends on the value of C). This is a result of the form of equation (5). If one divides equation (5) through by C, a $1/C$ term remains on the right hand side of the equation. These results indicate that if one reduces the value of R, the power MOSFET is less vulnerable to SEB. These results complement previous findings that decreasing R increases the critical v_{be} in the regenerative feedback mechanism [3, 10].

An interesting point can be made between this work and that in [3, 10]. In modeling the regenerative feedback mechanism, a 50% reduction in base resistance of the parasitic BJT resulted in approximately a 10% increase in the base-emitter voltage necessary to initiate burnout (as determined by the regenerative feedback mechanism) [13]. In this paper it is shown that a 50% reduction in base resistance results in approximately a 30% decrease in the peak base-emitter voltage generated by the heavy-ion-generated current source. This means that the burnout threshold is more sensitive to the parameters involved in the turn-on of the parasitic BJT than to the parameters involved in the regenerative feedback mechanism.

V. Summary

A first order lumped-parameter model has been presented to help illustrate the pertinent parameters involved in the turn-on of the parasitic BJT which leads to SEB of n-channel power MOSFETs. The base-emitter junction of the parasitic BJT was modeled as an R-C circuit. The base current of the parasitic BJT was modeled as a combination of the heavy ion generated current filament, avalanche generated hole current, and back-injected hole current due to the forward bias of the base-emitter junction. This model is an essential component in determining the burnout threshold. Previous work [9] deals with the critical base-emitter voltage required for burnout. This work estimates the value of the base-emitter voltage that will result for a specific set of ion and device parameters. The results in this paper indicate that the burnout threshold is more sensitive to the parameters involved in the turn-on process than it is to the critical value of the base-emitter voltage. The major findings of the model indicate that if one increases the junction capacitance and/or decreases the base resistance of the parasitic BJT, the vulnerability of the power MOSFET to SEB decreases.

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III. Modeling of Single-Event Gate Rupture of Power MOSFETs

III.A. Introduction

Single-event gate rupture (SEGR) of double-diffused MOS (DMOS) power transistors occurs when a heavy ion passes through sensitive regions of the device. As part of this task, a model for single-event gate rupture was developed that offers a clear picture of the relationships between the device structural parameters and the properties of the ion-induced current filament.

Single-event gate rupture can occur when a heavy ion strikes the neck region of the power MOSFET. The neck region constitutes the gate-drain overlap region of the device. Following the ion strike, the electric filed due to the applied positive drain bias causes the generated holes in the silicon to move toward the silicon - silicon oxide (Si-SiO_2) interface and the electrons toward the drain contact. The holes leak off only slowly toward the source contact and therefore start to pile up at the interface. This hole accumulation effect at the Si-SiO_2-interface creates a pool of positive charge, which results in a transient field increase across the oxide at the track position. If this transient field increases above a critical value, oxide breakdown occurs heating the structure locally. If the breakdown current lasts long enough, a permanent short-circuit through the oxide results.

Two complimentary models for SEGR of power MOSFETs have been developed under this contract: (1) a charge-sheet model that used a distributed *R-C* line to model the path that holes follow on the way towards ground and showed that gate oxide electric fields in the MV/cm range lasted for times in the picoseconds range; and (2) a prediction algorithm based on a two-dimensional numerical device simulator that shows excellent agreement with experimental data. The charge-sheet model provided the physical insight of the SEGR mechanism necessary to develop the two-dimensional model. The two-dimensional simulations showed that an increase in gate oxide thickness, t_{ox}, resulted in a decrease in SEGR vulnerability and the simulations showed very little temperature dependence of SEGR; both of the simulation results are in agreement with experiment.

The papers describing these models are included in Sections *III.B* through *III.F.* A brief overview of each paper is included here to guide the reader through this material.

Section III.B.: J.R. Brews, M. Allenspach, R.D. Schrimpf, K.F. Galloway, J.L. Titus, and C.F. Wheatley, Jr., "A Conceptual Model of Single-Event Gate Rupture in Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1959-1966, 1993.

> A physical model of hole-collection following a heavy-ion strike is proposed to explain the development of oxide fields sufficient to cause single-event gate rupture in power MOSFET's. It is found that the size of the maximum field and the time at which it is attained are strongly affected by the hole mobility.

Section III.C.: M. Allenspach, J.R. Brews, I. Mouret, R.D. Schrimpf, and K.F. Galloway, "Evaluation of SEGR Threshold in Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2160-2166, 1994.

> This paper presents a method for evaluating the single-event gate rupture threshold in power MOSFETs. Two-dimensional numerical simulations are used to show that very short time oxide field transients occur for ion strikes with non-zero drain-source bias applied to the device. These transients can affect single-event gate rupture through hole trapping and redistribution in the oxide.

Section III.D.: I. Mouret, M. Allenspach, R.D. Schrimpf, J.R. Brews, K.F. Galloway, and P. Calvel, "Temperature and Angular Dependence of Substrate Response in SEGR," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2216-2221, 1994.

> This paper examines the role of the substrate response in determining the temperature and angular dependence of single-event gate rupture. The likelihood of single-event gate rupture is shown to increase when the angle of incidence is made closer to normal incidence.

Section III.E.: M. Allenspach, I. Mouret, J.L. Titus, C.F. Wheatley, Jr., R.L. Pease, J.R. Brews, R.D. Schrimpf, and K.F. Galloway, "Single-Event Gate-Rupture in Power MOSFETs; Oxide Thickness Dependence and Computer Simulated Prediction of Breakdown Biases," *IEEE Trans. Nuc. Sci.*, vol. NS-42, pp. to be published December 1995.

> This paper presents a method for predicting the critical gate bias for a given drain-source bias necessary to trigger single-event gate rupture. The model predicts that susceptibility to single-event gate rupture decreases when the gate oxide thickness is increased. The simulation results agree very well with experimental data.

Section III.F.: I. Mouret, M.C. Calvet, P. Calvel, P. Tastet, M. Allenspach, K.A. LaBel, J.L. Titus, C.F. Wheatley, Jr., R.D. Schrimpf, and K.F. Galloway, "Experimental Evidence of the Temperature and Angular Dependence in SEGR," *presented at RADECS 1995.*

> Heavy ion experiments were used to investigate temperature and angular dependence in SEGR. They show that a normal incident angle favors SEGR. The influence of elevated temperature on the SEGR phenomenon is shown to be immaterial..

III.B. A Conceptual Model of Single-Event Gate Rupture in Power MOSFETs

A Conceptual Model of Single-Event Gate-Rupture in Power MOSFET's *

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Abstract

A physical model of hole-collection following a heavy-ion strike is proposed to explain the development of oxide fields sufficient to cause single-event gate rupture in power MOSFET's. It is found that the size of the maximum field and the time at which it is attained are strongly affected by the hole mobility.

1. Introduction

For the first time, a simple model of hole build-up and its induced image charge in the gate electrode of a power MOSFET is shown to lead to large enough oxide fields to cause oxide breakdown. These holes are collected from the plasma sheath of electron-hole pairs generated along the strike path of an incident heavy ion. This model replaces the picturesque but unquantifiable visualization of the sheath of mobile pairs as a "plasma wire" or a "depletion-layer collapse" that short-circuits the depletion-layer voltage, allowing the drain bias to become applied directly across the oxide.

In power MOSFET's, two types of single-event damage are known: single-event burnout (SEB) and single-event gate rupture (SEGR). In the case of SEB, the currents stemming from charge collection cause a voltage drop sufficient to turn "on" a parasitic bipolar transistor inside the device, a parasitic inherent in the construction of the power MOSFET. If the strike occurs while the device is subject to a large drain bias, sufficient carrier multiplication occurs to cause runaway, creating a short-circuit through the MOSFET that allows current from the external power supply to destroy the device [1].

In the case of SEGR, the ion-generated electron-hole pairs are separated by the applied bias. For discussion, assume an n–channel device with gate grounded and drain positively biased, as shown in Fig. 1.

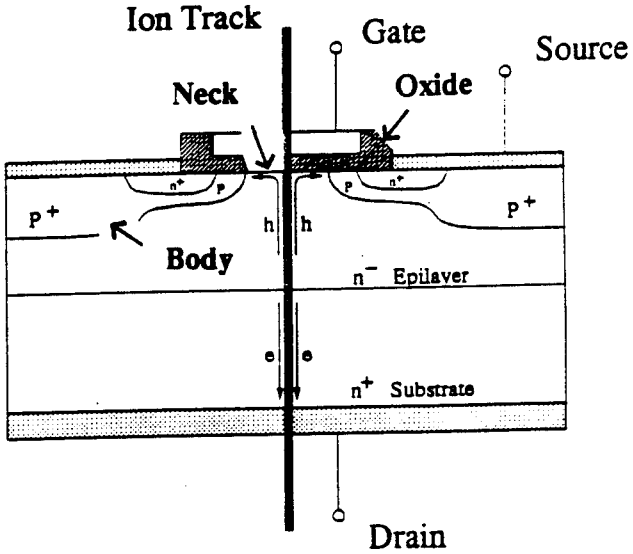


Figure 1. Power MOSFET structure, showing an ion-strike filament at the center of the n- neck region, with holes moving upward and electrons downward under the influence of the positive drain voltage.

The electrons are drawn toward the drain and the holes are driven toward the gate, along the axis of the strike filament. The effects of this charge collection commonly are visualized by picturing the sheath of electron-hole pairs surrounding the ion track as a conducting filament capable of short-circuiting the drain to the Si–SiO_2 interface. The

* This work was supported by the Naval Surface Warfare Center and the Defense Nuclear Agency

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idea of the strike filament as a "depletion-layer collapse" [2] or as a "plasma wire" [3,4] grew out of modeling of single-event upsets and was applied to SEGR by Hohl and Galloway[5]. As a result of this localized short-circuiting action of the filament, the ion strike results in a large fraction of the drain voltage dropping across the gate oxide, causing an increase in oxide field in the immediate vicinity of the filament.

If the transient increase in oxide field is large enough and lasts long enough, oxide breakdown occurs near the filament. A significant fraction of the charge stored in the MOSFET capacitor then can discharge, elevating the temperature in the neighborhood of the filament, locally destroying the oxide, short-circuiting the gate to the substrate.

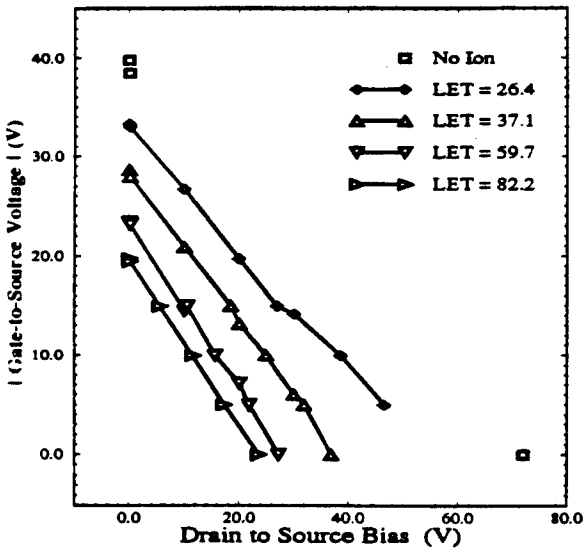


Figure 2. Observed magnitude of gate-to-source bias for SEGR in power MOSFET's *vs.* drain-to-source reverse bias with ion-*LET* as parameter. The control sample experienced no ion strike, and shows an intrinsic breakdown strength estimated from the $V_{DS}=0V$ datum point of $\approx 7.7\times10^6$V/cm. The control datum point at $V_{GS}=0V$ represents junction breakdown. The oxide thickness was 50nm, BVDSS = 70V, as limited by junction avalanche [10].

2. Experimental Work

Fischer[6] observed SEGR in power MOSFET's and Wrobel[7] in MOS capacitors. Both authors suggested that SEGR occurs only if an ion strike occurs while the oxide is subject to an oxide field greater than a critical value E_{CR} estimated as

$$E_{CR} = \frac{41}{(LET)^{1/2}} \times 10^6 \text{ V/cm} \qquad (1)$$

where LET is the linear energy transfer of the ion in MeV-cm^2/mg. A typical test ion is 285 MeV Br, which has an LET of 37 MeV-cm^2/mg, resulting in an E_{CR} of 6.7 MV/cm. This figure can be compared to a typical intrinsic breakdown strength of 8 – 12 MV/cm for gate oxides grown on surfaces of typical microroughness [8]. Fischer[6] tested (1) on p-channel power MOSFET's with source shorted to drain and positive gate bias. In this configuration, the MOSFET behaves like an inverted MOS capacitor. Wrobel[7] observed (1) in studies of gate rupture in both accumulated and inverted MOS capacitors.

The data of Fig. 2 show that the critical field for SEGR in power MOSFET's decreases with an increase in drain-to-source bias V_{DS}, even when the device is biased in inversion. However, these devices with doping levels $\approx 10^{16}$/cm^3 remain in inversion despite the V_{DS}-variation, so V_{DS} does not affect the oxide field *prior* to the ion strike. That is, Fig. 2 shows that when drain-to-source bias is applied, SEGR occurs at lower pre-strike critical oxide fields.

As mentioned earlier, the "plasma wire" model of the strike filament provides a picturesque view of how an oxide field approaching E_{CR} could arise in a localized region *during* or *after* the strike by short-circuiting the drain voltage to the Si–SiO_2 interface in the vicinity of the oxide-end of the filament. This model is misinterpreted, however, if the plasma filament is thought of simply as a "wire". The mechanism that transfers the applied voltage from the substrate to the oxide is the piling up of holes at the Si–SiO_2-interface. Analysis of this hole storage leads to the simple model discussed below.

3. Conceptual Model

Following an ion strike in the n$^-$ neck region, the electrons are drawn toward the drain by the positive applied bias, and the holes are driven to the oxide interface beneath the grounded gate electrode (see Fig. 1). The electrons experience a spreading resistance as they drift and diffuse from the localized filament into the entire drain region. The resulting localized resistive (I·R) voltage drop accompanying the electron flow pushes the equipotentials deeper. That is, at the drain-end of the filament, the drain voltage is spread out over a longer distance, leading to an overall lowering of the field [2,3].

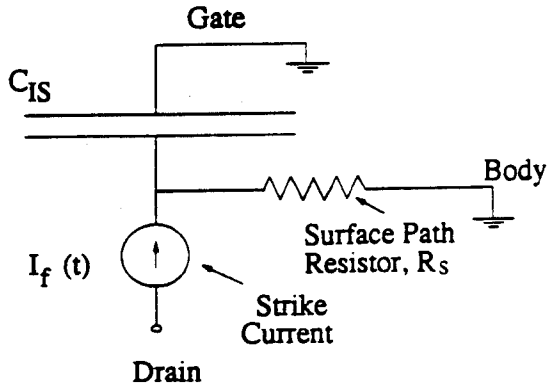


Figure 3. A lumped version of the equivalent circuit representing the hole storage at the end of the strike filament by a capacitor, and the leakage path to the grounded body by a lumped resistor.

To understand the *increase* in oxide field, we consider hole collection. Holes are driven toward the oxide-end of the filament, at the interface between the n–neck region and the gate oxide, where they induce an image charge in the gate electrode, increasing the oxide field. This "pool" of holes at the interface is fed by the continued hole collection from the strike filament, and spreads radially across the interface with time, moving toward the p–body region, which is at ground potential.

A simple circuit model of the situation is shown in Fig. 3. The lumped capacitor C_{IS} in this circuit represents the storage capability of the interfacial region neighboring the oxide-end of the filament. The resistor R_S represents the leakage path along the Si–SiO_2 interface from the strike filament to the grounded body. The extent of the oxide field build-up depends on the difference between the arrival rate of the holes (determined by $I_f(t)$) and the exit rate of the holes to the ground contact, determined by the RC–time constant of the circuit, $R_S C_{IS}$.

The basic model assumes that the strike filament forces a current $I_f(t)$ to the surface of the MOSFET. Although a general time dependence can be used, for simplicity $I_f(t)$ is modeled as a simple expression,

$$I_f(t) \approx I_{fB} + \left[I_{f0} - I_{fB} \right] e^{-t/T} \qquad (2)$$

where T is the filament lifetime, determined by drift and diffusion within the plasma sheath, I_{f0} is the filament current at $t=0$, and I_{fB} is the filament current following the early transient decay ($t>T$). During the time when oxide field is large, this form for $I_f(t)$ fits the results obtained from numerical simulations using MEDICI (the TMA version of PISCES), as discussed later. Of course, for long times the current must vanish, unlike (2). Because the RC–time constant of this circuit is long compared to the filament lifetime T (typically a picosecond or so), the voltage across the capacitor will rise far enough to allow oxide fields in excess of the intrinsic breakdown strength.

The ion strikes most likely to cause SEGR occur far enough from the p–body that a considerable "pool" of holes collects before diffusion brings them into contact with the p–body. Under these conditions, the interfacial storage capacitor is connected to ground *via* a distributed RC–line, representing the surface inversion layer. This distributed RC–line models diffusion from the filament toward ground, rather than allowing immediate access to ground, as implied by the lumped circuit of Fig. 3. The next section describes the modeling of this distributed RC–line by a charge-sheet model developed to describe the hole collection from the filament by the body contact. The charge-sheet model shows that the hole collection satisfies a nonlinear diffusion equation. The nonlinearity increases the diffusion of the holes for larger hole densities due to their self-field.

4. A Charge - Sheet Model for Hole Collection

At the Si–SiO_2–end of the filament, we assume that the current flows radially outward from the filament toward ground in an interfacial charge sheet. A distributed RC–circuit corresponding to this analysis is shown in Fig. 4.

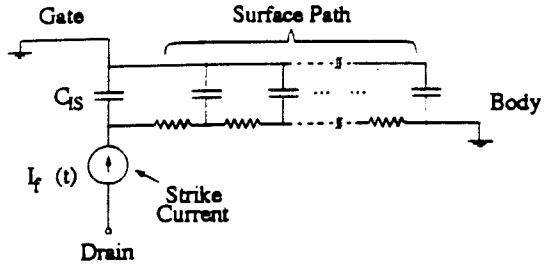


Figure 4. A distributed RC–circuit model that generalizes the lumped circuit of Fig. 3. The parameters of the distributed *RC*–line are calculated using a charge-sheet model that relates the distributed resistance to the hole density/cm^2 in the inversion layer.

The distributed part of this circuit is modeled using a charge-sheet description of the inversion layer, analogous to that used for the MOSFET [9]. This approach leads to a nonlinear diffusion equation for the transport of the holes radially away from the strike filament, along the interface, toward the grounded body region. The mathematical description of this model is contained in the Appendix.

5. Numerical Simulations

Using MEDICI, numerical simulations of an ion strike were made in a cylindrical (r, z) geometry. The ion is taken to be normally incident, with the centerline of its track coincident with the z–axis. The ion track at $t=0$ is modeled by placing a filament of electron-hole pairs along the z–axis from the gate to the drain in the region $0 \le r \le r_f(t=0)$, where $r_f(t=0) \approx 0.124\mu m$ in our simulation. For times $t>0$, the mobile carriers are transported in the self-consistent fields according to the usual drift + diffusion equations. This treatment of the carriers is not valid for very short times, as it ignores the transit time of the ion and the complicated processes that allow the initially energetic carriers to thermalize. However, the oxide field peaks in a time of the order of picoseconds, when most of these transients will be over. An idealization of a power MOSFET is used with a cylindrical geometry. The source contact of the power MOSFET is irrelevant, because it is shorted to the body contact, and because the holes are collected by the body, which is grounded. The body is modeled as a cylindrical interfacial p^+–contact of radius $r \ge a$, with $a \approx 14.64\mu m$ in our simulation. Electrons are collected by the drain, which is positively biased. The drain bias is sufficient to completely deplete the device, and before the ion strike all the equipotentials are parallel to the interface. A diagram of

our geometry is shown in Fig. 5, for an arbitrary choice of dimensions.

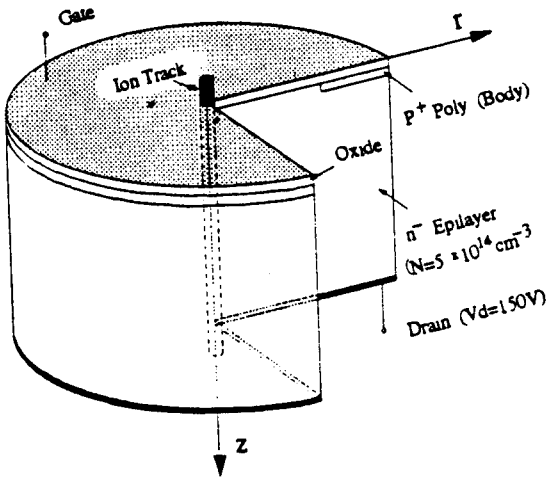


Figure 5. Cylindrical geometry for numerical simulations. The body contact is idealized as a shallow, cylindrical ring around the axis of the strike filament. To simplify analysis, the device is chosen to be fully depleted prior to the strike. The drain bias is 150V, gate and body are grounded, and the doping level is $5\times10^{14}/cm^3$.

The initial track density was chosen as $1.2 \times 10^{19}/cm^3$, which is not large enough for 285 MeV Br. (For this ion, the electron-hole pair density should be $2.4\times10^{10}/cm$ or $5\times10^{19}/cm^3$ for the chosen radius of 0.124μm.) However, larger densities caused non-convergence of the solutions.

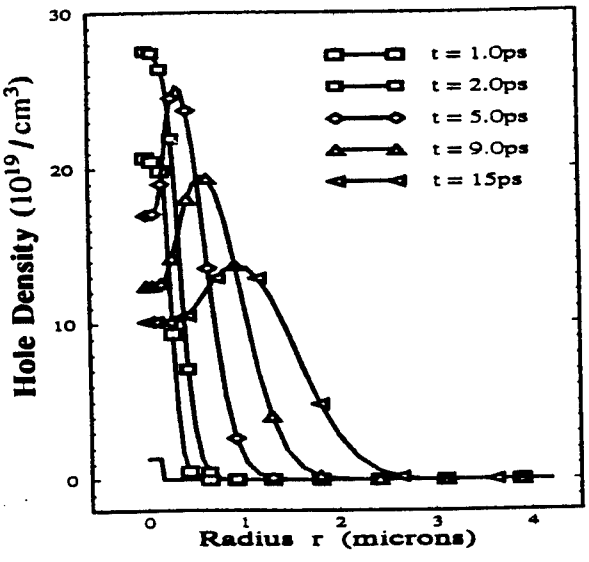


Figure 6. Hole density at the interface in units of $10^{19}/cm^3$ *vs.* radial distance with time as parameter.

In Fig. 6 the calculated hole density/cm^3 at the interface is plotted vs. distance for several times following the ion strike. As Fig. 6 shows, The holes diffuse radially toward the body, but they do not reach ground during the time the oxide field is large. Unlike the lumped circuit of Fig. 3, the distributed circuit of Fig. 4 includes this diffusion.

The interfacial hole diffusion is accompanied by subsurface radial expansion of the filament. Isoconcentration lines for the holes at 10 ps are illustrated in Fig. 7.

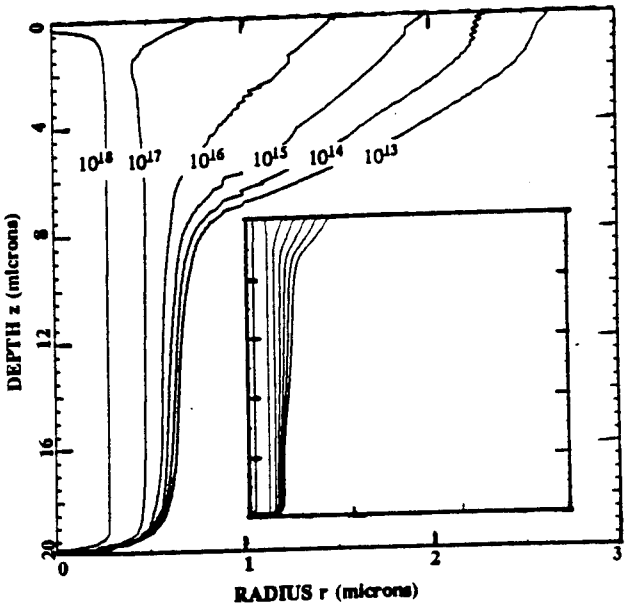


Figure 7. Contours of constant hole concentration at a time of 10 ps. Comparison with Fig. 6 is not possible, because the high-density hole contours are compressed in a thin inversion layer, not visible in this figure. In the n- epitaxial layer, the holes move radially outward with time, at the same time that they are traveling toward the top of the filament. Insert: same contours at 1ps.

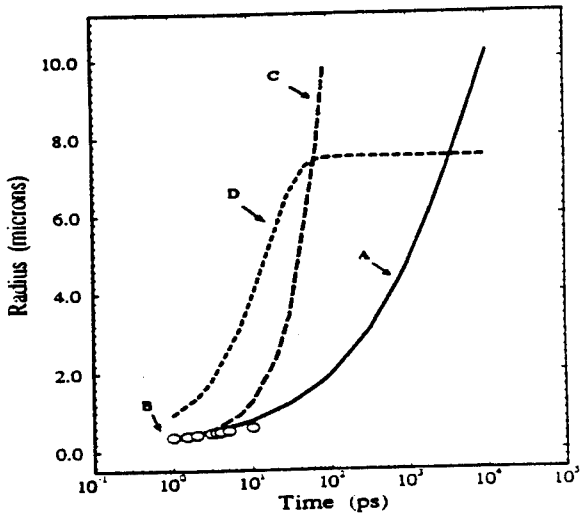


Figure 8. The radius of the hole concentration contour $r_f(t)$ for $p = N_D = 5\times10^{14}/cm^3$ *vs.* time at a depth of z = 10μm. Solid line *A*: one-dimensional, ambipolar, radial diffusion model [5]. Open circles *B*: MEDICI output. Dashed line *C*: radius $r_f(t)$ of the interfacial storage region as determined from MEDICI by fitting (A3) of the Appendix. The curve *C* is for field-dependent mobility, the curve *D* for constant mobility.

As the oxide field is building up sufficiently to cause SEGR, the radial motion of the carriers 10μm below the interface is approximately described by the cylindrical ambipolar diffusion model of Hohl and Galloway [5]. In Fig. 8 a comparison of this diffusion model with the numerical results is shown.

The current flowing from the filament to the interfacial storage capacitor is found by integrating the hole charge over the entire filament, and differentiating it to obtain the current $I_f(t)$. The computed charge at various depths is shown in Fig. 9.

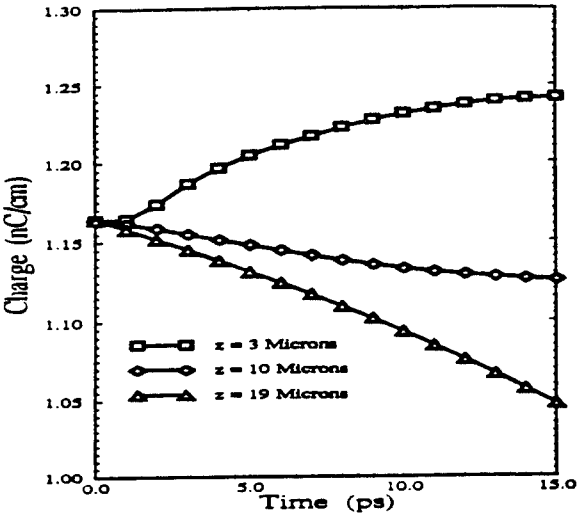


Figure 9. Charge per unit length at various depths *vs.* time from numerical simulation

It can be seen that the charge at deeper z-values decays more rapidly, because holes are driven toward the surface, depleting the deeper part of the filament first. Integrating over depth, the total charge in the filament as a function of time is shown in Fig. 10 Taking the derivative of the hole

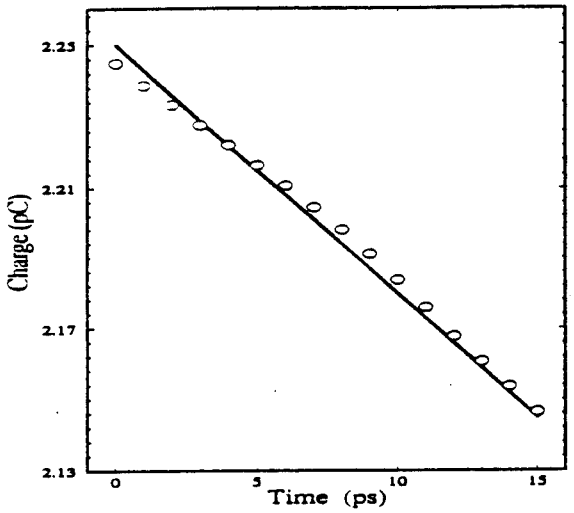


Figure 10. Total charge in the filament as a function of time. Solid line: numerical result, dashed line: approximate fit related to (2).

charge, Q(t), we find $I_f(t)$ is fitted well by (2). For the particular example we are presenting here, we find $I_{fB} \approx 6.3$ mA, $I_{f0} \approx I_{fB}$, and the filament time constant is not required.

The collecting pool of holes at the oxide-end of the strike filament induces an image charge in the gate electrode. The resulting field between the holes and their image charge appears in the oxide, raising the oxide field to values approaching the intrinsic breakdown field, as shown in Fig. 11.

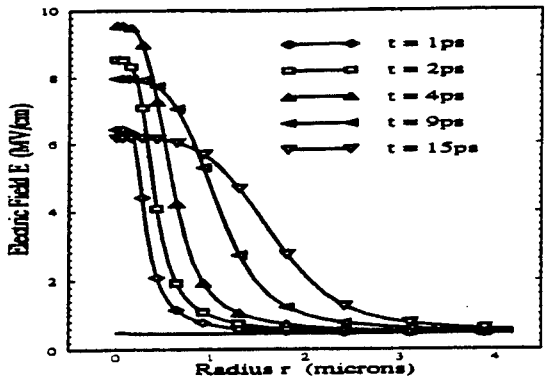


Figure 11. Oxide field *vs.* radial position with time as parameter from numerical simulation using a saturation velocity of $\approx 10^7$cm/s. The maximum field is E≈9.5MV/cm.

Figure 12 shows the same results for the case of constant mobility (no velocity saturation). It is apparent that the field is much lower and peaks much earlier in time, showing that the saturation of the hole mobility at large lateral fields is important.

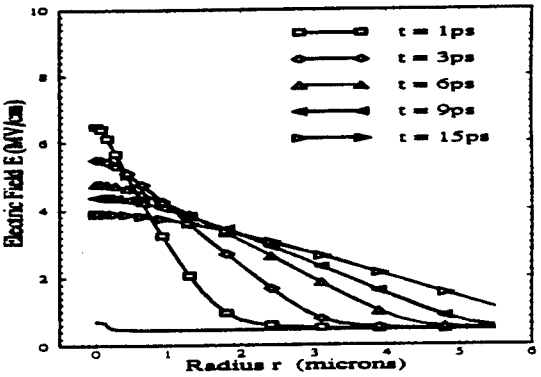


Figure 12. Oxide field *vs.* radial position as for Fig. 11, but with a constant mobility of $\mu = 500 cm^2/V \cdot s$. Maximum field E ≈ 6.6MV/cm.

6. Comparison with Simple Model

The distributed circuit model described in the Appendix has been solved using Newton's method, as outlined in the Appendix. The results agree qualitatively with the numerical results of MEDICI. For example, the result for the oxide field *vs.* time from the simple model is shown in Fig. 13. Although the agreement is rough, the two calculations provide the same order of magnitude for the field, the time scales, and the rate of diffusion of the holes from the filament toward the ground contact. It is hoped that the

agreement can be improved by a more careful treatment of the interfacial storage capacitor, and of the radial expansion of the filament with time.

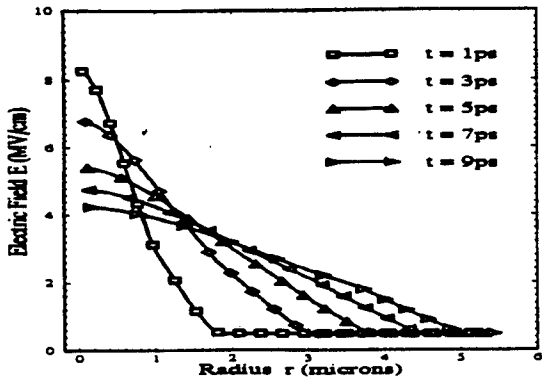


Figure 13. Oxide field *vs.* radial position with time as parameter from the distributed circuit model with $\mu = 500 cm^2/V \cdot s$.

7. Conclusions

A numerical simulation of an ion strike in a power MOSFET has been interpreted in terms of a simple model of hole collection. It has been shown that oxide fields larger than the intrinsic breakdown strength of the oxide can arise from the holes collecting at the interface and their image charge in the gate electrode. These high fields persist for times of the order of picoseconds. It is not known how long these fields must persist to initiate SEGR.

The model shows that the extent of the field build-up depends on several factors which must be considered if SEGR sensitivity is to be reduced. SEGR sensitivity will be reduced if the diffusion of the holes to ground is easy, allowing the holes to drain off before too many are collected at the interface. This point is well illustrated by the mobility dependence of the field build-up, as discussed earlier. Removal of holes could be expedited to make SEGR less likely if the hole mobility at the interface were increased, or if the geometry of the neck region were altered to make ground contacts closer, or if impediments in the path to ground were avoided, such as n^+–implants from other parts of the structure. SEGR sensitivity also can be reduced if the oxide or depletion-layer capacitances are reduced, not primarily because voltages are dropped across larger distances (*e.g.* larger oxide thicknesses), but because the circuit RC–time-constant is reduced, so fewer holes are stored at the surface. Additional reduction in SEGR sensitivity is provided if fewer of the generated holes reach the interface, *e.g.* if the recombination rate in the silicon substrate can be increased, or if subsurface hole collection can be provided.

8. Acknowledgements

The authors are pleased to thank R. Pease for helpful discussions.

9. Appendix: Simple Charge-Sheet Model of SEGR in Power MOSFET

A1. Charge-Sheet Transport

In the oxide there is no charge so the potential $\phi(r,z,t)$ satisfies Laplace's equation:

$$\nabla^2 \phi(r,z,t) = 0 \qquad \text{(A1)}$$

where $\phi(r,z,t) \geq 0$ for the condition of large positive drain bias. The boundary conditions on $\phi(r,z,t)$ at all times are
(i) At the gate electrode, $\phi(r, z=d_{OX}, t) = 0$. Here d_{OX} = oxide thickness.
(ii) At the Si–SiO_2–interface,

$$-\left.\frac{\partial \phi(r,z,t)}{\partial z}\right|_{z=0} = \frac{q}{\varepsilon_{OX}} P(r,t) \qquad \text{(A2)}$$

where $P(r,t)$ is the hole density / cm^2 at the interface.

For $r \leq r_f$, we assume that the hole distribution at the interface is described by

$$qP(r,t) = \frac{Q_{IS}(t)}{\pi r_f^2(t)} \cdot \frac{\exp\left[-(r/r_f)^{1.8}\right]}{0.614946} \qquad \text{(A3)}$$

where $r_f(t)$ is the filament radius determined by MEDICI (*i.e.* it is a given function of time). The first factor in this equation is the average hole charge / unit area, and the second factor describes its radial distribution. The second factor is normalized so Q_{IS} is the amount of charge stored in the region $0 \leq r \leq r_f$.

The value of $Q_{IS}(t)$ is determined by current balance as

$$Q_{IS}(t) = \int_0^t \left[I_f(t') - 2\pi r_f(t') J_r(r_f, t') \right] dt' \qquad \text{(A4)}$$

In this equation both $I_f(t)$ and $r_f(t)$ are given functions of time.

We must find $J_r(r_f, t)$ by solving the transport equation that decides how fast the charge leaks off to ground. This equation is the continuity equation

$$\frac{1}{r}\frac{\partial}{\partial r}\left[r J_r(r,t) \right] + \frac{\partial}{\partial t} qP(r,t) = 0 \qquad \text{(A5)}$$

In this equation the radial current density is taken from the charge-sheet model as

$$J_r(r,t) = -qD\,f(F_r)\left[\frac{qP(r,t)}{kT}\frac{\partial}{\partial r}\phi(r,z=0,t) + \frac{\partial}{\partial r}P(r,t)\right] \quad (A6)$$

with D = zero-field diffusion coefficient and with

$$f(F_r) = \frac{1}{1+(F_r/F_0)}$$

to account for the radial field ($F_r = -\partial\phi/\partial r$) dependence of the hole mobility. The continuity equation then becomes, using (A6) and (A2),

$$\frac{1}{r}\frac{\partial}{\partial r}\left\{r\,f(E_r)\left[\frac{q}{kT}\frac{\partial\phi}{\partial z}\frac{\partial\phi}{\partial r} + \frac{\partial^2\phi}{\partial r\,\partial z}\right]\right\} = \frac{1}{D}\frac{\partial^2\phi}{\partial t\,\partial z} \quad (A7)$$

For large enough values of r, we suppose that the gradual-channel approximation is valid, so $\partial\phi/\partial z \approx -\phi/d_{ox}$ Then the continuity equation becomes

$$\frac{1}{r}\frac{\partial}{\partial r}\left\{r\,f(E_r)\left[\frac{q}{kT}\phi + 1\right]\frac{\partial\phi}{\partial r}\right\} = \frac{1}{D}\frac{\partial\phi}{\partial t}. \quad (A8)$$

Assuming the gradual-channel approximation works at $r = r_f$ we find

$$\frac{q}{\varepsilon_{ox}}P(r_f,t) = \frac{Q_{IS}(t)}{\varepsilon_{ox}\pi r_f^2(t)}\cdot\left[\frac{e^{-1}}{0.614946}\right] = -\left.\frac{\partial\phi(r_f,z,t)}{\partial z}\right|_{z=0} \approx \frac{\phi(r_f(t),z=0,t)}{d_{ox}} \quad (A9)$$

which determines the end condition for the continuity equation at $r = r_f$, in terms of $Q_{IS}(t)$ and $r_f(t)$:

$$\phi[r_f(t),z=0,t] = \frac{0.598\cdot d_{ox}Q_{IS}(t)}{\varepsilon_{ox}\pi r_f^2(t)} = 0.598\cdot\frac{Q_{IS}(t)}{C_{IS}[r_f(t)]} \quad (A10)$$

with $C_{IS}[r_f(t)] = \varepsilon_{ox}\pi r_f^2(t)/d_{ox}$ = interfacial storage capacitance.

A2. Solution Procedure

To solve the equations one approach is as follows:

(i) Assume that $J_r(r_f,t) = 0$.

(ii) Find $Q_{IS}(t)$ for all time steps t by integration of (A4) using the midpoint rule.

(iii) Set up the end condition using (A10) for $\phi(r_f(t),z=0,t)$ given $Q_{IS}(t)$ and $r_f(t)$.

(iv) Solve (A7) using this end condition.

(v) From the solution of (A7), find $J_r[r_f(t),t]$ for all time steps using (A6).

(vi) Recalculate $Q_{IS}(t)$ from (A4) including J_r (*i.e.* return to step (ii))

(vii) Repeat (ii) – (vi) until no change in Q_{IS} results.

To solve (A7) replace ϕ by

$$u(r,t) = [1 + q\phi/kT]^2 \quad (A12)$$

We also introduce the normalized length x by

$$x = r/a \quad (A13)$$

where a = radius to the ground contact. We introduce the new time variable τ

$$\tau = Dt/a^2 \quad (A14)$$

so (A7) becomes

$$\frac{\partial^2 u}{\partial x^2} + \left[\frac{1}{x} + \frac{\partial \ln f}{\partial x}\right]\frac{\partial u}{\partial x} = \frac{1}{f\sqrt{u}}\frac{\partial u}{\partial \tau} \quad (A15)$$

where now f is given by

$$f = \frac{1}{1+\left[\frac{kT/q}{2aF_0}\right]\left[\frac{1}{\sqrt{u}}\left|\frac{\partial u}{\partial x}\right|\right]} \quad (A16)$$

The initial condition for (A15) is

$$u(x,\tau=0) = 1 \quad (A17)$$

and the end conditions are

$$u(1,\tau) = 1 \quad (A18)$$

$$u(x_f,\tau) = \left[1 + \frac{2}{\pi}\frac{Q_{IS}(\tau)}{C_{IS}(\tau)kT/q}\right]^2 \quad (A19)$$

with

$$Q_{IS}(\tau) = \frac{a^2}{D}\int_0^{\tau}\left[I_f(\tau) + \pi x_f(\tau)\frac{kT}{q}\frac{\varepsilon_{ox}}{d_{ox}}D\,f\left.\frac{\partial u}{\partial x}\right|_{x=x_f}\right]d\tau \quad (A20)$$

and

$$C_{IS}(\tau) = \frac{\varepsilon_{ox}}{d_{ox}}\pi a^2 x_f^2(\tau) \quad (A21)$$

A3. Numerical Solution by Newton's Method

We linearize (A15) by letting $u = u_o + \delta u$ and $f = f_o + \delta f$, where δu and δf are the small departures of the exact solution u from a guessed solution u_o. Following linearization, (A15) becomes

$$\frac{\partial^2 u}{\partial x^2} + \left[\frac{1}{x} + \frac{\partial \ln f_o}{\partial x}\right]\frac{\partial u}{\partial x} - \frac{1}{f_o\sqrt{u_o}}\frac{\partial u}{\partial \tau} + \frac{u}{2f_o u_o^{3/2}}\frac{\partial u_o}{\partial \tau} = -\frac{\partial}{\partial x}\left[\frac{\delta f}{f_o}\right] - \frac{\delta f}{f_o^2\sqrt{u_o}}\frac{\partial u_o}{\partial \tau} + \frac{1}{2f_o\sqrt{u_o}}\frac{\partial u_o}{\partial \tau} \qquad \text{(A22)}$$

We discretize (A22) neglecting δf as follows. Let ε = time step, Δ = space step, $s = \Delta^2/\varepsilon$. Also, let $x(i) = x_f(\tau+\varepsilon) + i\cdot\Delta$, and let $u^{n+1}(i) = u(x(i), \tau+\varepsilon)$. Then at time $\tau+\varepsilon$,

$$u^{n+1}(i+1)\left[1 + \frac{\Delta}{2x_i} + \frac{1}{4}\ln\frac{f_o^{n+1}(i+1)}{f_o^{n+1}(i-1)}\right] + u^{n+1}(i-1)\left[1 - \frac{\Delta}{2x_i} - \frac{1}{4}\ln\frac{f_o^{n+1}(i+1)}{f_o^{n+1}(i-1)}\right] - u^{n+1}(i)\left[2 + \frac{s}{2f_o^{n+1}(i)\sqrt{u_o^{n+1}(i)}}\left[1 + \frac{u_o^n(i)}{u_o^{n+1}(i)}\right]\right] = \frac{s}{2}\frac{\sqrt{u_o^{n+1}(i)}}{f_o^{n+1}(i)}\left[1 - 3\frac{u_o^n(i)}{u_o^{n+1}(i)}\right] \qquad \text{(A23)}$$

To estimate u_o^{n+1} we use

$$u_o^{n+1} = u_o^n + \left[\frac{\partial u_o^n}{\partial \tau}\right]\varepsilon = u_o^n(i) + \sqrt{u_o^n(i)}\left\{\frac{1}{x}\frac{\partial}{\partial x}\left[x f_o \frac{\partial u_o^n}{\partial x}\right]\right\}\varepsilon \qquad \text{(A24)}$$

The function f_o is discretized using

$$f_o(i) \approx \frac{1}{1 + \frac{1}{\sqrt{u_o(i)}}\left|\left[\frac{u_o(i+1) - u_o(i-1)}{2\Delta}\right]\right|} \qquad \text{(A25)}$$

Equation (A23) is to be solved iteratively at each time step as follows: we start with the guess $u_o^{n+1}(i, \tau+\varepsilon) \approx u^n(i, \tau)$. Then we use this u_o^{n+1} in (A23) and solve to obtain $u_1^{n+1}(i, \tau+\varepsilon) = u^{n+1}(i, \tau+\varepsilon)$. As the next guess we take $u_o^{n+1}(i, \tau+\varepsilon) = u_1^{n+1}(i, \tau+\varepsilon)$. With this u_o, again we solve (A23) for the second approximation $u_2^{n+1}(i, \tau+\varepsilon) = u^{n+1}(i, \tau+\varepsilon)$. Then take $u_o = u_2$ and so forth until the change in $u(i, \tau+\varepsilon)$ is small. Once this occurs, we increment the time to $\tau+2\varepsilon$, find the new value of $x_f(\tau+2\varepsilon)$, redefine the index i, and continue.

For the case i = 1, (A23) involves u(0). We find u(0) from (A19). On the first pass through the loop of Section A3, we assume $J_r \approx 0$, so we obtain u(0) from (A19) with Q_{IS} from (A20):

$$Q_{IS}(\tau+\varepsilon) \approx \frac{a^2}{D}\int_0^{\tau+\varepsilon} I_f(\xi)\, d\xi \qquad \text{(A36)}$$

where ξ is a dummy variable of integration. On the next pass, in (A20) we need $\partial u/\partial x|_{x=x_f}$.

$$\left.\frac{\partial u}{\partial x}\right|_{x=x_f} \approx \frac{-3u(0) + 4u(1) - u(2)}{2\Delta} \qquad \text{(A37)}$$

with u(0), u(1) and u(2) from the last pass. To use the trapezoidal rule in (A20) for $Q(\tau+\varepsilon)$ we also need

$$\left.\frac{\partial^2 u}{\partial x^2}\right|_{x=x_f} \approx \frac{1}{4\Delta^2}\left[5u(0) - 11u(1) + 7u(2) - u(3)\right] \qquad \text{(A38)}$$

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III.C. Evaluation of SEGR Threshold in Power MOSFETs

Evaluation of SEGR Threshold in Power MOSFETs *

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Abstract

Bias values, determined experimentally to result in single-event gate rupture (SEGR) in power metal oxide semiconductor field effect transistors (MOSFETs), are used in 2-D device simulations, incorporating the experimental geometry. The simulations indicate that very short time oxide field transients occur for ion strikes when $V_{DS} \neq 0V$. These transients can affect SEGR through hole trapping and redistribution in the oxide.

I. Introduction

Single-event burnout (SEB) and single-event gate rupture are two catastrophic effects leading to power MOSFET failure in space. In both cases, the single-event failure mechanisms are initiated by a heavy ion traversing the device, creating electron-hole pairs along its path. In the case of SEB, the current from the generated carriers causes a voltage drop across the base-emitter region of the parasitic bipolar junction transistor (BJT), inherent to the structure of a vertical double-diffused metal oxide semiconductor (VDMOS) power transistor. If this parasitic BJT turns on, while the drain is under a large bias, sufficient carrier multiplication occurs resulting in excessive current flow that induces thermal destruction of the device [1].

In the case of SEGR, the ion strikes the device in the neck region, as shown in Fig.1. For an n-channel power MOSFET, the electric field, due to the applied positive drain bias, causes the generated holes in the silicon to move toward the interface and the electrons to move toward the drain contact. The holes diffuse toward the p-body at a slower rate than the holes drifiting toward the interface resulting in a hole pile-up condition at the interface around the strike area. This hole accumulation effect at the Si-SiO_2 interface creates a pool of positive charge, which results in a transient field increase across the oxide at the track position. If this transient field increases above a critical value, oxide breakdown occurs; and the collected holes discharge through the oxide, heating the structure locally. If the breakdown current lasts long enough, a permanent short-circuit through the oxide results [2].

The purpose of this paper is to present a physical picture of the effects in a power VDMOS transistor leading to SEGR. We compare simulation with measurements on stripe geometry VDMOS power transistors that show the SEGR breakdown dependence on drain-to-source (V_{DS}) and gate-to-source (V_{GS}) voltage for different values of linear energy transfer (LET) of the incident ion. Results from real device structures are used to investigate SEGR physics and mechanisms. SUPREM-4[1] data for the test structure were used in PISCES[2] simulations to make accurate comparisons of simulation results with experimental data. An extensive experimental data set for the test structure was provided by Wheatley, Titus, and Burton [3].

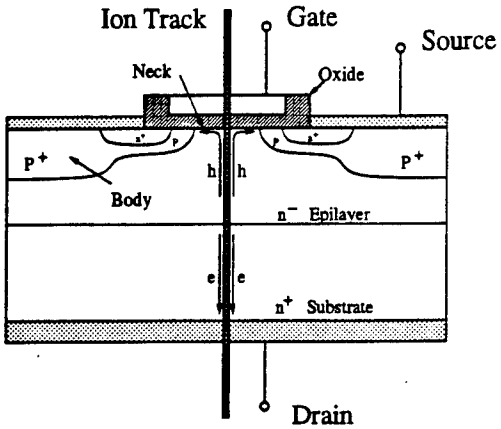


Fig.1 An ion traversing a VDMOS power transistor in the neck region can initiate SEGR. The vertical electric field due to the drain bias separates the carriers along the track.

II. Experimental Data

Experiments were conducted with stripe geometry n-channel power MOSFETs [3]. Figure 2 shows one half of the symmetrical cross section of the devices. The devices have a "50nm" gate oxide and were screened before irradiation to select those devices with a narrow distribution of threshold voltage, namely $2.9 < V_{TH} < 3.1$. During measurements, the source was grounded; and the negative gate voltage or the positive drain voltage were incremented in 1V steps until the device failed. The measurements were repeated for different LET values, and only points where

*This work was supported by the Naval Surface Warfare Center and the Defense Nuclear Agency

[1]The SUPREM-4 program ATHENA V-1.0.2 from Silvaco International

[2]The PISCES program ATLASII V-1.3.2 from Silvaco International

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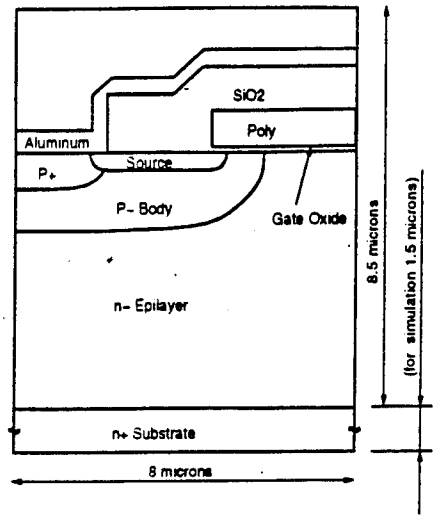


Fig.2 Cross section of the stripe geometry test device used in the experiments and simulations.

LET $\frac{MeV\,cm^2}{mg}$	V_{DS} [V]	V_{GS} [V]	*Ion Type*
7.8	20	-37.6	Silicon
	40	-31.7	
	60	-25.7	
26.4	0	-33.4	Nickel
	10	-26.9	
	20	-20.4	
	30	-13.9	
37.1	0	-29.4	Bromine
	10	-22.1	
	20	-14.7	
	30	-7.4	
82.2	0	-19.6	Gold
	7	-13.8	
	14	-8.0	
	20	-3.0	

Table 1 Bias points for the simulations at different LET values obtained from the measurements; the values correspond to the bias conditions where SEGR occurred [3].

SEGR (and not SEB) occurred were reported. The voltages at the failing point were evaluated by taking the median device only and averaging the last passing value and the first failing value.

The experimental data extend existing measurements on MOS capacitors [4] and on MOSFET's without significant substrate fields [5] to the case where substantial substrate fields are applied using a drain-to-body reverse bias. In these experiments, the pre-strike (dc) oxide fields and substrate fields are independently varied. Prior to strike, this independence of the field in the substrate from that in the oxide is assured because a dc interfacial layer of holes is maintained under all bias conditions, forcing the interface to be an equipotential held at the body voltage (see Section III). Because the body is short circuited to the source, the pre-strike oxide field is $F_{OXDC} = |V_{GS}/d_{OX}|$ and the pre-strike interface-to-substrate voltage is V_{SD}, where V_{GS} and V_{SD} are controlled independently.

The data shown in Table 1 are particularly interesting because they show that SEGR is strongly affected by the presence of substrate fields (a V_{DS} dependence). Our simulations show that the pre-strike oxide field F_{OXDC} is augmented during or after the strike by an amount dependent upon the pre-strike substrate field (determined by V_{DS}).

The basic mechanism behind this strike-induced increase in oxide field was shown earlier to be due to the interfacial collection of holes, which first are created by the incident ion and, then, are driven to the interface by the substrate field [2]. This earlier work, however, showed only that the oxide field was increased by this mechanism. In this paper, the simulated field versus time curves following a strike are calculated for the same LET value as the incident ion and the same biasing condition (V_{DS} and V_{GS}) as shown experimentally to result in SEGR. The correlation of the experimental and simulation data will be used to elucidate the charge collection effects at the Si-SiO_2 interface and also to discuss the importance of the charge separation effects in the gate oxide.

III. Demonstration of a Pre-Strike Inversion Layer

Fig. 3 is a plot of the experimental points where SEGR occurred as a function of V_{DS} and V_{GS} for different LET values of incident ions. The plot was generated by expression (1), derived by Wheatley, Titus, and Burton, by fitting their measurements [3], where d_{OX} is the oxide thickness in nm and LET is the linear energy transfer of the incident ion in MeV-cm^2/mg (see also Table 1).

$$V_{GS} = 0.84 V_{DS}\left(1 - exp\left[-\frac{LET}{17.8}\right]\right) - \frac{50}{1 + \frac{LET}{53}} \quad (1)$$

The oxide thickness dependence of expression (1) was not explored experimentally. The n-channel VDMOS transistors used in the experiments and in the simulations were biased with V_{GS} negative and with V_{DS} positive. In order to determine the bias conditions for which the Si-SiO_2 interface was inverted, we simulated the structures at different biasing conditions and extracted the biases at which the inversion layer carrier concentration at the Si-SiO_2 interface was equal to the background doping concentration (onset of strong inversion).

The upper dashed line in Fig. 3 indicates the boundary condition for the onset of strong inversion. Every biasing point underneath this boundary line is associated with a dc interfacial layer of holes that serves to establish the

interface as an equipotential with the same potential as the source. This condition assures a separate control of the pre-strike oxide field and the substrate field strength by V_{GS} and V_{DS}, respectively. The marked-out regions at the bottom and far right indicate the actual electrical breakdown limits of the device.

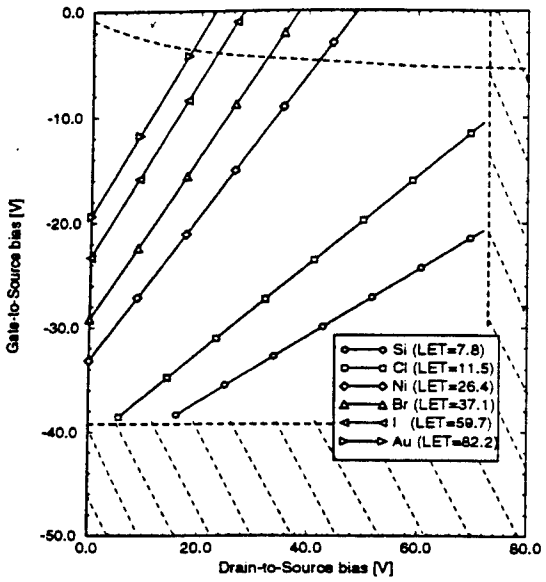


Fig.3 Solid lines represent biasing conditions where SEGR occurred with the LET of the incident ion as a parameter. This plot was created by applying expression (1), which is an empirical fit to the experimental data [3]. The top dashed line indicates the pre-strike boundary of the strong inversion onset. The filled regions at the bottom and right indicate an invalid operating region beyond the breakdown limits of the device.

If we fix a constant drain bias in Fig. 3, we can extract the critical externally applied pre-strike field across the oxide, $F_{crit} = \left|\frac{V_{GS}}{d_{OX}}\right|$, at the intersection point for any given LET curve. For the case of V_{DS}=0V, the plot of F_{crit} versus LET is similar to the MOS-capacitor measurements performed by Wrobel [4]. But, besides this LET dependence of SEGR due to charge generation/separation effects in the oxide (see Section VI), Fig. 3 clearly shows a V_{DS} dependence on SEGR breakdown. This experimental observation is extremely important because it seems to contradict the previous argument that the oxide field and V_{DS} are independent.

This contradiction can be removed if we notice that the previous argument is based on dc fields. That is, we now will argue that a transient oxide field occurs following an ion strike with a magnitude dependent upon the value of V_{DS}. This transient field increases the oxide field in a region localized near the ion track by a substrate charge collection mechanism outlined in Section IV.

IV. Transient Oxide Field

Fig. 4 shows an enlarged cross section of the device with an inversion layer at the interface (horizontal line of holes) as discussed in Section III. The filled and empty circles represent holes and electrons, respectively. The carriers in this figure have already started to separate under the influence of the drain-to-source field. While the electrons have been drawn toward the positively biased (with respect to the source) drain contact, the holes have moved toward the negatively biased gate electrode. Since the holes can-

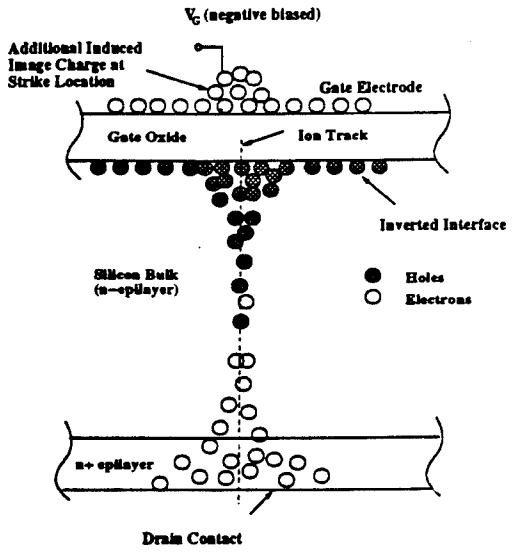


Fig.4 Simplistic view of substrate charge collection effect after ion strike.

not cross the oxide, they pile up at the interface at the ion track location. This local increase of positive charge at the interface induces an equal image charge at the gate side of the oxide and, thus, increases the field across the oxide [2]. In time, the holes drift and diffuse away from the track location toward the grounded body/source contact; and the local charge build-up decreases back to zero (pre-strike case). The peak of the transient field was determined by simulation (see Section V) to occur after approximately 2ps and lasts only 20–300ps for the LET values in the range of $7.8 \leq LET \leq 82.2$. As discussed in the Appendix, there are inaccuracies in the modeling of the transient field. Nonetheless, the basic mechanism of hole buildup is supported, regardless of these inaccuracies.

V. Simulation—Transient Substrate Effects

Transient 2-D simulations with ATLASII were performed. A cylindrical approximation for the device was used, with the ion passing through the center. The cross section, materials, and profiles of the simulated transistor were taken

from SUPREM-4 data of the experimental test devices to guarantee simulation conditions equivalent to the experiment (see Fig. 2). Impact ionization models have been tested in simulations for "worst-case" conditions of the applied bias to verify that this structure is designed for much lower voltages than the structure in [6] and so avalanche plays no role in our simulation; thus no impact ionization model was included in the SEGR simulations. The gate, drain, and source voltages were chosen to match the data points in Table 1. An initial filament radius of $r = 0.12\mu m$[7] was assumed, and equation (2) was solved for each LET value to find the carrier density per unit volume in the track generated by the passing ion in the epitaxial layer [7].

$$N = \frac{LET\left[\frac{eV\,cm^2}{gm}\right] \times 2.33\left[\frac{gm}{cm^3}\right]}{\pi r^2 \times 3.6\left[\frac{eV}{pair}\right]} \left[\frac{pairs}{cm^3}\right] \qquad (2)$$

To obtain convergence at such high ($10^{18} \leq n \leq 10^{20}$) carrier densities, the generation of the pairs was simulated as a time dependent ramp with a risetime of 4fs. The radial distribution of charge pairs in the track falls off from the center as r^{-2}[7]. A comparison of the simulated oxide field for the case of a uniform carrier concentration in the track and the case of a linearly decaying carrier concentration with the total number of carriers in the track fixed was done. The difference in these two results was minor (< 2%) and; therefore, a uniform radial distribution of the generated carriers was used in the simulation.

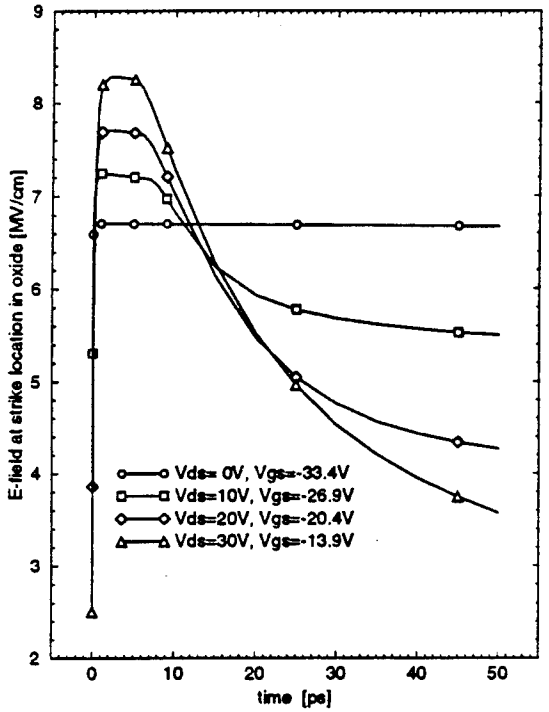


Fig.5 Electric field at strike location in the oxide versus time for the biases shown in Table 1 (Nickel ion, LET=26.4)

Figure 5 shows the simulated maximum vertical electric field in the oxide versus time for the nickel ion (LET=26.4) at the different biases from Table 1. This transient peak in the electric field occurred locally, where the ion passed through the oxide, and, as illustrated in Section IV, is due to the hole collection at the Si-SiO_2 interface. For all values of V_{DS}, at t=0, the value of the peak oxide field is just the pre-strike field determined by $F_{DC} = \left|\frac{V_{GS}}{d_{OX}}\right|$. Note that the horizontal curve in Fig. 5 corresponds to V_{DS}=0V. As mentioned above, the lack of a vertical electric field in the substrate for this case does not support the electron-hole separation in the bulk; and, therefore, hole "pile-up" at the surface does not occur. In other words, the transient character of the oxide field does not occur because no charge separation or hole pile-up occurs in the silicon substrate. For $V_{DS} \neq 0V$, the time for the transient electric field to reach the peak value is $\approx 2ps$ for the case of the nickel ion. The simulations of the other LET values listed in Table 1 show a similar time to reach the peak field. For the nickel ion of Fig. 5, we see that the transient field starts to decay after the peak value was reached and returns to it's pre-strike value after $\approx 50ps$. Simulations of the silicon, bromine, and gold ions result in transient lifetimes of approximately 30, 70, and 300ps, respectively.

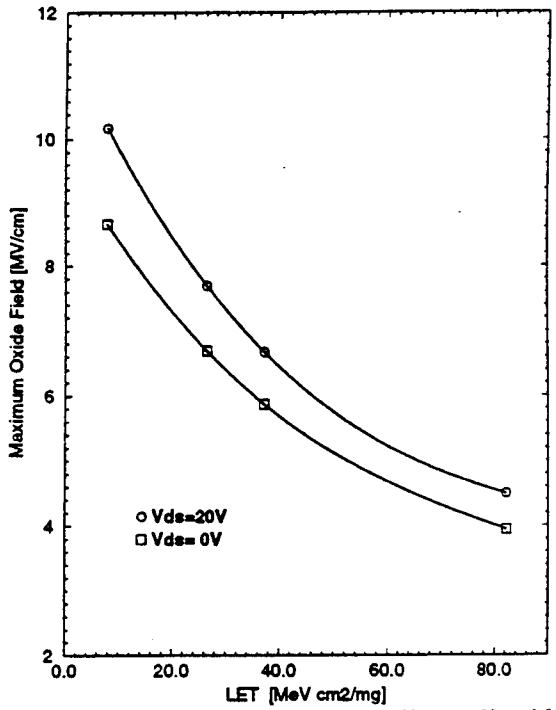


Fig.6 Maximum electric field across oxide for $V_{DS} = 0V$ and $V_{DS} = 20V$ versus LET value of the incident ion.

In Fig. 6, the maximum field is plotted versus LET from our transient simulations for $V_{DS} = 20V$ and with the corresponding $|V_{GS}|$ from Table 1. The peak fields are taken from curves like Fig. 5, generated for each LET. For $V_{DS} = 0$, Fig. 5 shows the field is time independent, but for $V_{DS} \neq 0$ the oxide field has a transient component and

peaks at a higher value than for $V_{DS} = 0$.

Figure 6 shows that the maximum value of the electric field across the oxide for SEGR decreases with increasing LET. For any given V_{DS} value, this trend is consistent with the trend for the dc field corresponding to SEGR from Fig 3. For the case of $V_{DS} = 0$, this peak value is just the dc-field F_{DC}. For the case of $V_{DS} = 20V$, the peak electric field is increased beyond this dc-field temporarily, as shown in Fig. 5. The transient component of the oxide field is due to the substrate charge separation effects. If the maximum oxide field had the same effect on the oxide regardless of its duration, the data points for $V_{DS} = 20V$ from Fig. 6 would coincide with the $V_{DS} = 0V$ data. The fact that the two curves in Fig. 6 do not coincide shows that the transient behavior of the oxide field for $V_{DS} \neq 0$ plays a role. To explain the V_{DS} dependence of SEGR, we need to understand what happens in the oxide during the time interval before the transient V_{DS}-dependent part of the field vanishes.

VI. Oxide Effects

The $V_{DS} = 0V$ data of Wheatley and Titus [3], as well as the earlier data of Fischer [5] and Wrobel [4], show that the oxide field and LET affect SEGR. Fig. 6 shows that, for transient oxide fields, larger fields are needed to cause SEGR than in the dc field case. To understand why transient oxide fields must be larger to cause SEGR, we need to examine what occurs in the oxide under transient field conditions. A basic difficulty in using the simulation results to interpret the physical effects after an ion strikes a VDMOS transistor is that the simulation does not model the evolution of charging or charge transport in the oxide itself.

Let us suppose that the effects of field and LET on SEGR are due to trapped hole charge and its distribution in the oxide. That is, we suggest an explanation of the V_{DS} dependence of SEGR depends on: (i) how many holes survive in the oxide and remain there as positive trapped charge and (ii) where the holes are located once they get trapped. This suggestion is motivated by yield experiments [8] that show the number of holes trapped in an oxide layer following an ion strike increases with increasing oxide field. These experiments also show that the number of holes trapped is a weakly increasing function of LET. These dependencies of hole trapping are somewhat similar to those of SEGR.

In addition (e.g., as discussed by Oldham [8]), analysis suggests that the results of these yield experiments can be explained by a numerical simulation of recombination in the presence of drift and diffusion. The correct treatment of transport and recombination of non-equilibrium pair distributions at sub-picosecond times is not well understood. However, the analysis shows that the effects on yield occur in times less than picoseconds, which is consistent with the speculation that the V_{DS} dependence of SEGR is due to the influence of short-time V_{DS}-related oxide field transients upon hole survival in the oxide.

The distribution of the holes in the oxide is also a possible contributing factor to SEGR. This distribution can be affected by the spatial variation in recombination. The distribution also could be affected by hole transport, which occurs by three different mechanisms, depending on the time scale of interest: for $t \leq 2ps$, "dry" hole transport with $\mu = 1cm^2/(Vs)$, for $2ps < t < 100ns$ small polaron transport with $\mu \approx 2 \times 10^{-5} cm^2/(Vs)$, and for $t > 100ns$ a dispersive trap-related transport [9]. Different hole distributions can lead to substantially different fields in the oxide (see Fig. 7) that could influence SEGR by changing charge injection conditions that contribute to oxide breakdown.

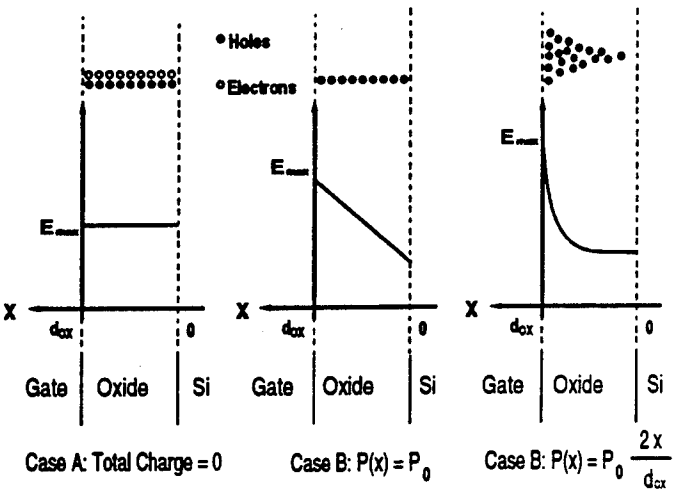


Fig.7 Case A shows the generated carriers in the oxide before they started to recombine or separate. The net charge is zero and therefore the electric field is the pre-strike field $|V_{GS}/d_{OX}|$. Case B pictures a later time after some holes have survived recombination. These trapped holes raise the electric field at the gate-side of the oxide. Case C shows a still later time where the holes had some redistribution, increasing the oxide field even more.

Based on the above considerations, our proposed SEGR mechanism is as follows. For the case of $V_{DS} = 0$, the pre-strike oxide field $F_{DC} = \left|\frac{V_{GS}}{d_{OX}}\right|$ determines the number of surviving holes in the gate oxide. These trapped holes increase the oxide leakage current (see Fig. 7). This increased leakage current can result in breakdown of the oxide at the strike location. If $|V_{GS}|$ is below the critical value for $V_{DS} = 0$, more holes in the oxide recombine before the electrons have been swept out by the field F_{DC}, and, therefore, no SEGR occurs. On the other hand, when $V_{DS} > 0$, the *substrate* charge separation (or interface hole pile-up) effect due to V_{DS} results in an increased oxide field for a few picoseconds. This transient field increase reduces recombination in the oxide and increases the number of trapped holes. This increased number of trapped holes in-

creases the oxide leakage current, so a given dc V_{GS}-bias will draw a larger oxide leakage current than before the transient. Thus, SEGR can occur for lower (dc) V_{GS} values once a V_{DS}-related transient has occurred. The lower the (dc) V_{GS} value, the larger the V_{DS}-related oxide field transient must be to reduce recombination in the oxide sufficiently to leave enough holes in the oxide to cause SEGR.

VII. Summary

Experimental data for SEGR on stripe geometry VDMOS transistors from Wheatley, Titus, and Burton have been compared with the results of an equivalent 2-D simulation. We have shown that these data cannot be explained on a dc basis. A transient field increase created by the hole collection at the Si-SiO_2-interface was demonstrated. The time-scale information for the transient oxide field increase due to V_{DS} extracted by simulation was used to suggest a mechanism for the V_{DS} dependence of SEGR. This mechanism is based on hole trapping and redistribution in the oxide at short times following the ion strike.

VIII. Acknowledgment

The authors acknowledge useful discussions with R.L. Pease, C.F. Wheatley, Jr. and J.L. Titus, and thank CFW and JFT for the support with extensive data sets for this stripe line structure [3].

IX. Appendix: Simulation Inaccuracies

As discussed, for example, by Lundstrom [10] for thin base transistors, where very large carrier concentration gradients exist, the conventional drift-diffusion equation (3)

$$\mathbf{J}_{n,p} = (n,p)q\mu_{n,p}\mathbf{E} \pm qD_{n,p}\nabla(n,p) \qquad (3)$$

is no longer valid if equation (4) is not satisfied,

$$\frac{8\mu_{n,p}^2 m^* T}{q^2}\left[\frac{d(n,p)/dz}{(n,p)}\right]^2 \ll 1 \qquad (4)$$

where T is the temperature, m* is the effective mass, $\mu_{n,p}$ is the mobility, and q is the unit charge of an electron. For the simulation of the gold ion, for instance, we have to deposit $\approx 1.2 \times 10^{20}/cm^3$ electron-hole-pairs along the track (for a track radius of $r = 0.1\mu m$). Even if we use a Gaussian distribution of the carriers in the radial direction to smooth out the gradient of the carrier concentration, we would still need to distribute the carriers over a large filament radius with a characteristic distance of over $10\mu m$ in order to validate Fick's law and expressions (3) and (4). To investigate the validity of the simulation results, we simulated a transient response of $5\times 10^{19}/\mathrm{cm}^3$ electron-hole-pairs deposited in a sheet along a straight path through the center of an intrinsic piece of silicon held at a grounded potential along its perimeter. Because of the equipotential boundary all around the structure, the transport of the carriers is mainly determined by diffusion rather than by drift. Figure 8 shows the structure at t=0 immediately after the deposition of the charge in the $0.2\mu m$ wide sheet. Fig. 9 and Fig. 10 are plots of hole concentration

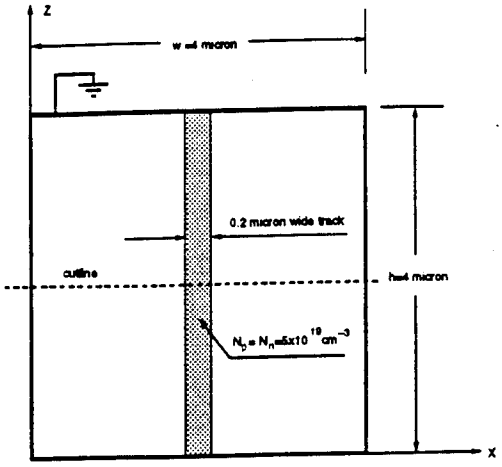


Fig.8 Enlarged section of square-shaped intrinsic silicon with a deposited charge sheet (N=P=$5\times 10^{19}cm^{-3}$) in the center with a width of w=$0.2\mu m$. Fig. 9 and Fig. 10 show the hole concentration and hole velocity along the cutline at z=h/2 for t=0ps and t=1ps, respectively.

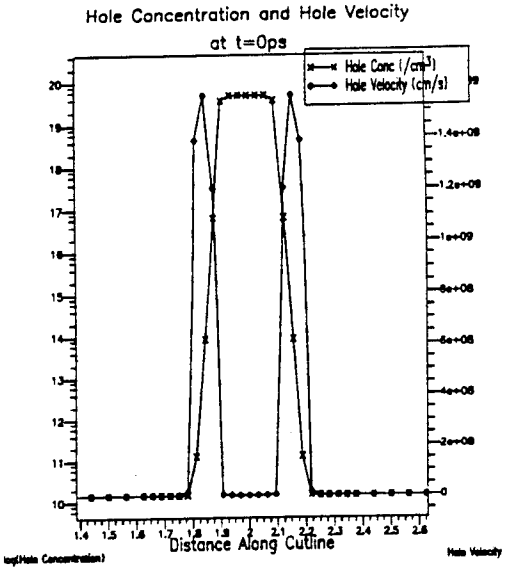


Fig.9 Hole concentration and hole transport velocity at t=0ps along the horizontal cutline in Fig. 8.

and hole transport velocity ($v_p = \frac{J_p}{qP}$) versus lateral distance along a horizontal cutline (X-direction) at z=h/2 in Fig. 8 for t=0 and t=1ps. The simulator employed the conventional drift-diffusion equation (3) together with Pois-

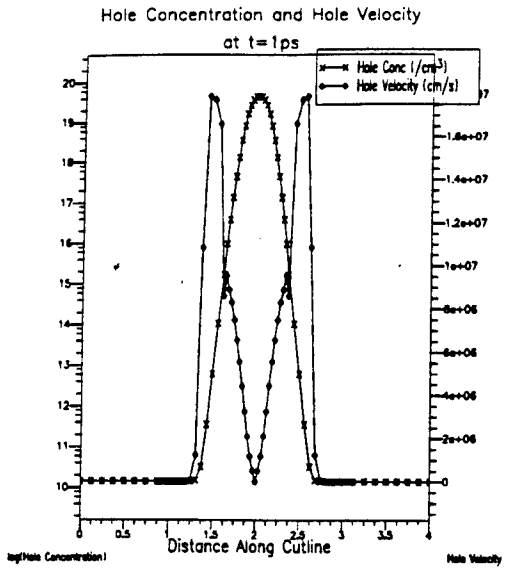


Fig.10 Hole concentration and hole transport velocity at t=1ps along the horizontal cutline in Fig. 8.

son's equation and the current continuity equation. We see clearly, in Figures 9 and 10, that the transport velocity of the holes at the location of high carrier concentration gradients has exceeded the thermal velocity of holes ($v_{th} \approx 8 \times 10^6 cm/sec.$). It is physically incorrect that such high velocities occur, demonstrating that the conventional drift-diffusion model (3) is inaccurate for single-event simulations.

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III.D. Temperature and Angular Dependence of Substrate Response in SEGR

Temperature and Angular Dependence of Substrate Response in SEGR†

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Abstract

This work examines the role of the substrate response in determining the temperature and angular dependence of Single-Event Gate Rupture (SEGR). Experimental data indicate that the likelihood of SEGR increases when the temperature of the device is increased or when the incident angle is made closer to normal. In this work, simulations are used to explore this influence of high temperature on SEGR and to support physical explanations for this effect. The reduced hole mobility at high temperature causes the hole concentration at the oxide-silicon interface to be greater, increasing the transient oxide field near the strike position. In addition, numerical calculations show that the transient oxide field decreases as the ion's angle of incidence is changed from normal. This decreased field suggests a lowered likelihood for SEGR, in agreement with the experimental trend.

I. INTRODUCTION

Double-diffused metal-oxide-semiconductor (DMOS) power devices are capable of conducting large currents when turned on and withstanding large voltages when turned off [1]. Power DMOS transistors are widely used in space applications. However, in the cosmic-ray environment, they are exposed to energetic heavy ions. The passage of a single heavy ion through the device can lead to significant permanent degradation of the device or cause catastrophic failure.

In power Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), two single event effects have been observed: Single-Event Burnout (SEB) and Single-Event Gate Rupture. These phenomena can be understood in terms of the physical structure of the device. A cross section of a power DMOS transistor is shown in Figure 1.

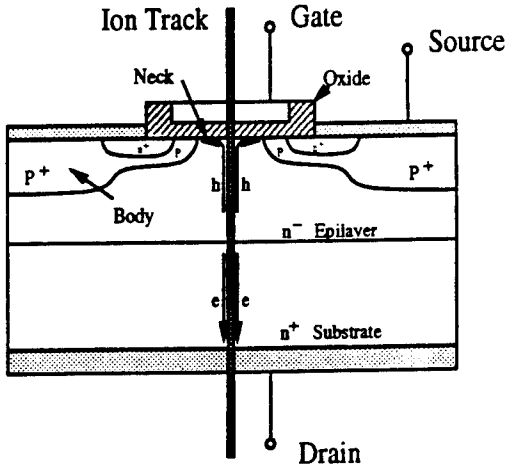


Fig. 1 Power MOSFET structure, showing an ion-strike filament at the center of the n-neck region, with holes moving upward and electrons downward under the influence of the positive drain voltage.

SEB can occur in n-channel power MOSFETs when a heavy ion strikes the device in the portion of the p-body where the channel is formed, in the p-body under the n^+ source, or in the neck region within close proximity to the p-body. The passage of this ion generates a current filament that locally turns on a parasitic npn bipolar junction transistor (BJT) inherent to the power MOSFET. Depending on how strongly this BJT is initially turned on, the currents within the device can regeneratively increase, through an avalanche process, until second breakdown of the parasitic BJT occurs, leading to failure of the device [2].

SEGR can occur when a heavy ion strikes the neck region of the device. The energy deposited by this ion creates a high-density filament of electron-hole pairs in both the oxide and the silicon. In this work, we focus attention on the response of the pairs in the silicon itself. When a positive bias is applied on the drain electrode of an n-channel power MOSFET, the pairs created along the ion track are separated; the holes are driven toward the gate and the electrons flow toward the drain, as shown in Figure 1. The accumulated holes at the Si-SiO_2 interface and their image

†Work supported in part by ALCATEL ESPACE, AEROSPATIALE, the Naval Surface Warfare Center - Crane, and the Defense Nuclear Agency.

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charge in the gate electrode cause the electric field in the oxide to increase. For large enough fields, oxide breakdown can occur. This model is supported by room-temperature simulations for normally incident ions [3].

Experimental data from irradiation of power MOSFETs with heavy ions at high temperature and with various incident angles have been reported by Nichols et al. [4]. These data for elevated temperature and for normal incidence are summarized in Table I.

Table I

Measured SEGR voltages at several temperatures for MOSFETs irradiated at normal incidence with heavy ions summarized from Nichols et al. [4].

Device	BVDSS (V)	Type	Number of parts	V_{GS}(V)	LET (MeV.cm²/mg)	Temperature	Failure V_{DS}(V)
IRH7150	100	n	4	15	40	room	60/80
	100	n	1	15	40	100 °C	70
IRH7250	200	n	4	15	40	room	120/140
	200	n	1	15	40	100 °C	100
FRM140D1	100	n	2	0	40	room	70/80
	100	n	2	0	40	100 °C	60/80
FRM240D1	200	n	2	0	40	room	80/100
	200	n	1	0	40	85 °C < T < 125 °C	60/80
FRM9240	200	p	5	0	26	room	none
	200	p	2	0	26	85 °C	120/180
IRF9240	200	p	2	0	40	room	80/100
	200	p	1	0	40	125 °C	80/100

The experiments suggest that SEGR occurs at lower drain biases when the devices are irradiated at high temperature, although the increment used for V_{DS} was too large to establish this result with certainty. In addition, the results of Nichols et al. for incident angles far from normal indicate a weak trend that a normal incident angle is the worst case. The large step size used for V_{DS} precludes making definite conclusions. These data show global trends that need further investigation.

It is difficult to examine these dependencies on temperature and angle experimentally because of the large number of experimental conditions that are required to establish general relationships. In this work, simulations are used to understand the effect of temperature on SEGR and the influence of the incident angle on SEGR is examined experimentally, and also discussed using a simple physical model. This work focuses on the role of the substrate response in determining SEGR response and does not address the dynamic response of the oxide. With the drain of the device positively biased and the gate grounded, the electrons generated in the oxide and driven toward the Si-SiO_2 interface are swept into the silicon. Because of the small absolute quantity of electrons created in the oxide (since the oxide is thin and the track is smaller in the oxide than in the silicon), the number of holes at the interface is not significantly modified. Moreover, simulations were performed to see the influence of fixed charge (positive or negative) in the oxide on hole transport in the substrate. The oxide charge did not change the results, showing that, to first order, the oxide effects do not affect the substrate response. Hence, it is reasonable to consider the mechanisms in the oxide and the substrate independently.

II. Temperature Dependence

A. Simulation Background

The numerical simulations were performed using ATLAS II (the 2D SILVACO version of PISCES) [5]. The simplified model, with cylindrical symmetry, that was used to represent the simulated device, is shown in Figure 2. The dimensions of the simulated structure, as well as the doping of the different regions, are also noted in the figure. The models used for these simulations are discussed in the Appendix. The simulated track has an initial radius of 0.124μm and a uniform density of electron-hole pairs of 1.2×10^{19} /cm^3. This corresponds approximately to an LET of 9 MeV-cm^2/mg. Although this is a relatively low LET, it allows illustration of the key trends in the SEGR phenomenon. The simulations were run at five different temperatures: 300K, 350K, 400K, 450K, and 500K.

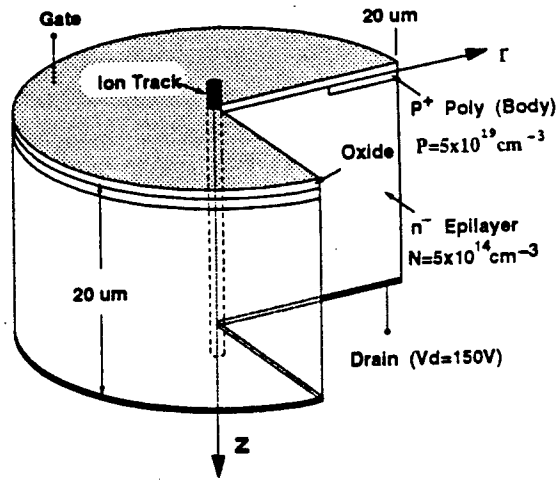


Fig. 2 Simplified model, with cylindrical symmetry, which was used to represent the simulated device. This figure also indicates the dimensions of the device, as well as the doping of the different regions.

B. Simulation Results

Figure 3 shows the electric field in the oxide as a function of the distance from the center of the ion track (radius). The electric field across the oxide at 5ps is shown for 300K, 400K, and 500K.

At 300K, the oxide electric field obtains its maximum value 5ps after the ion strike. At 400K and 500K, the maximum value is reached 6ps and 12ps after the ion strike, respectively. However, field plots for times of 6ps or 12ps are qualitatively similar. The plots clearly indicate an increase of the oxide electric field when temperature is increased. This field increase confirms that a higher operating temperature will lead to a larger probability for a device to be damaged through SEGR. An examination of the maximum value of the oxide electric field (which occurs in the center of the ion track) as a function of time shows that the maximum electric field is greater at higher temperature for all times (see Figure 4). For devices with lower breakdown voltages, the avalanche in the device is not significant. Thus, for such devices, the charge density, and so the electric field, decay more rapidly [6]. Figure 5 shows that the maximum oxide electric field varies approximately as the square root of temperature.

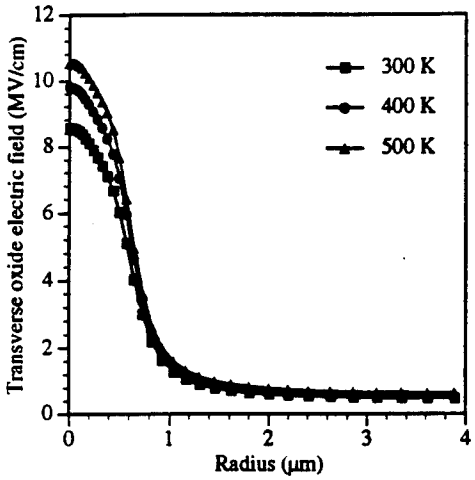


Fig. 3 Electric field across the oxide 5ps after the ion strike, as a function of the radius, for different temperatures. The simulation indicates that the oxide electric field increases as temperature increases.

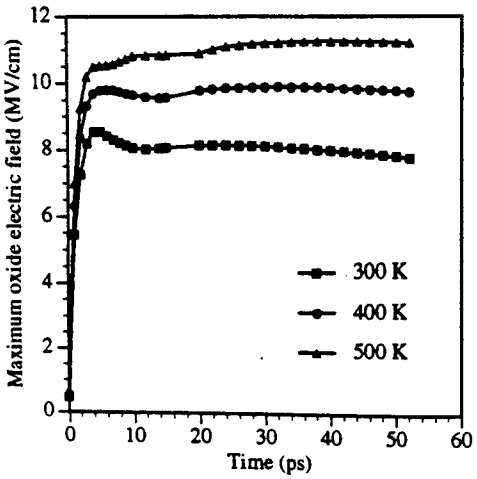


Fig. 4 Maximum transverse electric field in the oxide, as a function of time, for different temperatures.

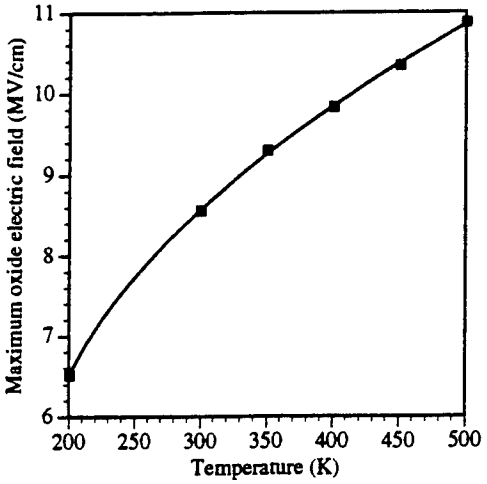


Fig. 5 Plot of the maximum electric field in the oxide as a function of temperature. The maximum electric field in the oxide varies approximately as the square root of temperature.

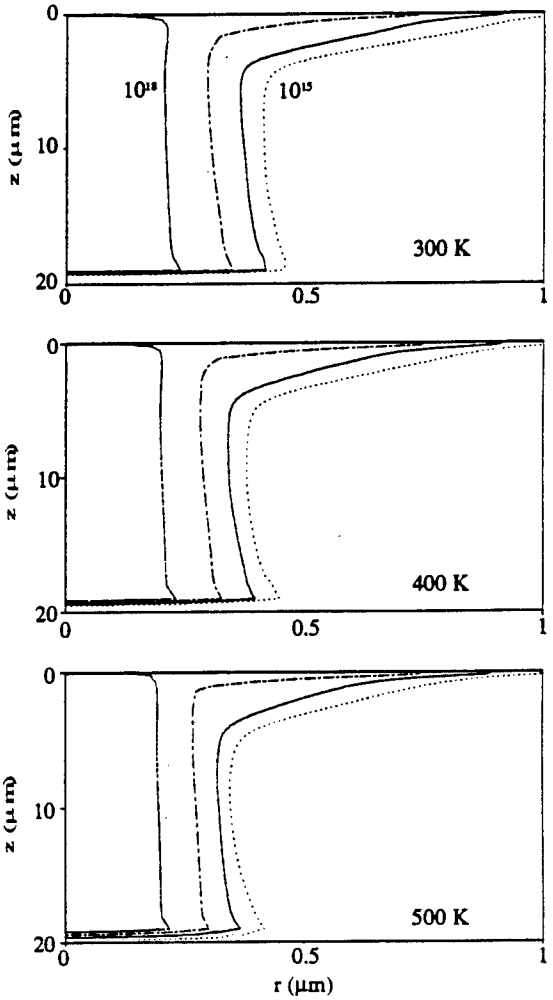


Fig. 6 Equi-hole-concentration lines in the device, 5ps after the ion strike, for three different temperatures. The distances are referenced to the center of the ion track (r) and to the Si-SiO_2 interface (z). These plots give insight into the hole motion in the device. They also illustrate that the hole motion is slower at high temperature.

C. Physical Interpretation

The simulation results show that the maximum oxide electric field increases when temperature is increased. According to Brews et al. [3], this larger field should be related to a larger hole concentration at the interface at higher temperatures. According to Kirchhoff's current law, this hole density is determined by the balance between the vertical inflow of holes from the track and the outflow of holes along the interface. Because temperature affects both currents, it is not obvious how the balance is affected by temperature. Below, we show that the hole storage increases, showing that the outward flow of holes along the interface is slowed down more than the vertical inward flow of holes. This higher concentration of holes at a given time leads to the increased electric field, as will be shown.

Figure 6 plots equi-hole-concentration lines in the device 5ps after the ion strike for the three temperatures of 300K, 400K, and 500K. These plots illustrate that the hole motion in the device is slower at high temperature. A numerical integration of the hole concentration over a 0.5μm deep silicon layer below the Si-SiO_2 interface has confirmed this trend. The result of this integration is shown in Figure 7. In this figure, the number of holes per unit area is plotted as a function of the distance to the track. This figure shows that, for a higher temperature, a larger number of holes is located next to the interface around the strike location.

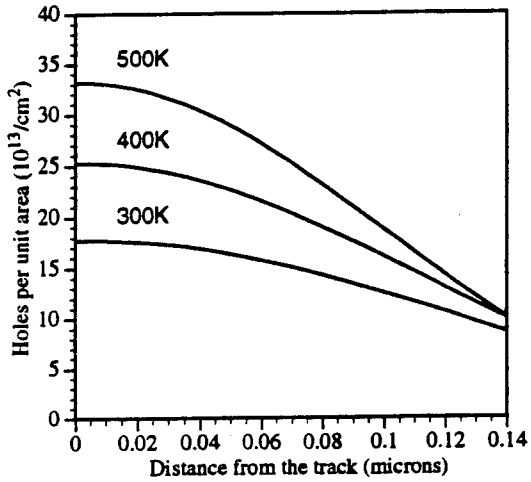


Fig. 7 Numerical integration of the hole concentration over a 0.5μm deep silicon layer below the Si-SiO_2 interface for three different temperatures, 5ps after the ion strike. This plot shows that, for a higher temperature, a larger number of holes is located next to the interface around the strike location.

III. Angular Dependence

A. Experimental Results

The data of Nichols et al. [4] also show a trend for the influence of the incident angle on SEGR. According to their data, it seems that ions with high incident angles (that is, with incident angles far

Table II
SEGR testing results with Br ion, for various incident angles. This table shows that when the incident angle is made further from normal, the probability for SEGR is lower.

Type	Manufacturer	VGS (V)	VDS (V)	Incident angle (°)	Failure
IRF440	Motorola	-30	240 < VDS < 260	0	SEGR
			276 < VDS < 280		SEGR
			VDS < 276		SEGR
			360	48	SEB
			300		SEB
			300	25	SEB
			VDS < 300	15	SEGR
IRF440	IR	-20	VDS < 260	0	SEGR
			VDS < 240		SEGR
			226 < VDS < 230		SEGR
			220 < VDS < 226		SEGR
			300	48	None
			306		SEB
			306		SEB
IRF440	Harris	-15	280 < VDS < 300	0	SEGR
			VDS < 270		SEGR
			250 < VDS < 256		SEGR
			266 < VDS < 270		SEGR
			246 < VDS < 250		SEGR
			320 < VDS < 326	48	SEGR
			326		SEB
IRF140	Harris	-25	VDS < 50	0	SEGR
			50 < VDS < 52		SEGR
			54 < VDS < 56		SEGR
			54 < VDS < 56		SEGR
			54 < VDS < 56		SEGR
			88	48	None
			72 < VDS < 74	25	SEGR
			76 < VDS < 78		SEGR

Note: $V_{DS}<V_1$ means that SEGR occurred on the first bias point, for $V_{DS}=V_1$. $V_1<V_{DS}<V_2$ means that no failure was observed for $V_{DS}=V_1$ and that SEGR occurred for $V_{DS}=V_2$. $V_{DS}=V_1$ refers to a bias point where SEB occurred.

from normal) have a lower probability to induce SEGR. To confirm these experimental results, additional heavy ion experiments were performed on four different kinds of power MOSFETs. These experiments took place at the IPN (Institut de Physique Nucléaire) component dedicated testing line, set up by the CNES (Centre National d'Etudes Spatiales), in Orsay, France. The parts tested were IRF440s (from Motorola, International Rectifier, and Harris) and IRF140s (from Harris).

The strategy of the test was first to perform an initial experiment on a given device. For this initial test, the temperature was set at 300 K and the heavy ion had a normal incidence. The gate bias V_{GS} was first set at -15V. The drain bias V_{DS} was increased in steps of 25V for the IRF440s and in steps of 10V for the IRF140s. If burnout was observed before SEGR (and stopped before destruction of the device occurred), V_{GS} was increased by a -5V increment and the test started again with this new value for the gate bias.

This test provided an initial starting value of V_{GS} and V_{DS} for SEGR failure of the device. Then, the test was performed at the V_{GS} obtained when SEGR was observed in the initial test, with a smaller increment in V_{DS} (5V for the IRF440s and 2V for the IRF140s). Two cases where examined: normal conditions (normal incidence, room temperature) and high incident angle (still at room temperature). The ion chosen for these experiments was the Br ion at 196MeV (LET = 40 MeV-cm^2/mg). The results obtained during these tests are summarized in Table 2. The expected trend appeared clearly: SEGR was observed later (that is, for higher values of V_{DS}) or not observed at all when the incident angle was different from normal.

B. *Geometrical Analysis*

As shown in Figure 8a, at normal incidence, the electron-hole pairs are deposited along a vertical line in the device. Under the influence of the electric field created by the positive bias on the drain, holes are driven vertically toward the gate and accumulate in a small region. However, when the electron-hole pairs are deposited along an oblique line, as shown in Figure 8b, holes are still driven vertically by the applied field, and, thus, are spread out in a wider area.

The experimental trend can be understood by considering a simple geometrical model. The assumptions used in this simple model are that all the holes located within a certain distance from the surface are transported by drift to the Si-SiO2 interface. Simulations show that the SEGR process is dominated by holes within about 1μm of the interface. Although this transport is not instantaneous, the time parameter has been ignored for this calculation. Recombination has not been taken into account as it is not significant for the time it takes these carriers to reach the interface (tens of picoseconds). This simple calculation assumes a constant carrier concentration within a track radius kept equal to its initial value.

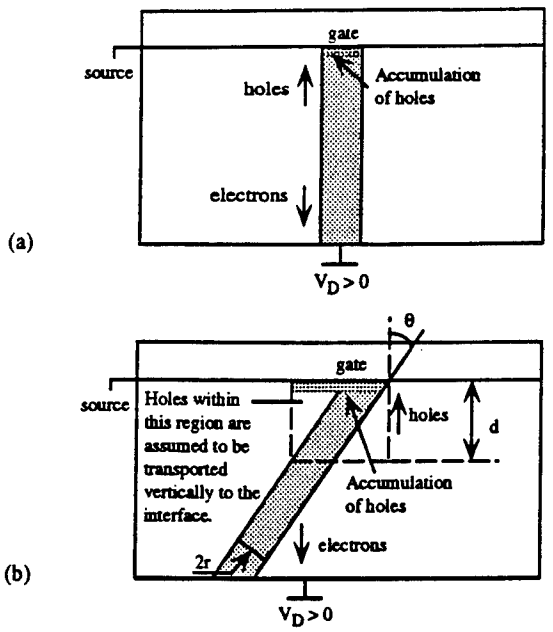


Fig. 8 Distribution of the holes accumulated at the Si-SiO_2 interface in the case of a normal incident angle (a) and in the case of an incident angle different from normal (b). Under the influence of the electric field, due to the positive bias on the drain electrode, the holes are driven vertically towards the Si-SiO interface. In the case of an incident angle different from normal, the holes spread out on a much wider area than when the incident angle is normal.

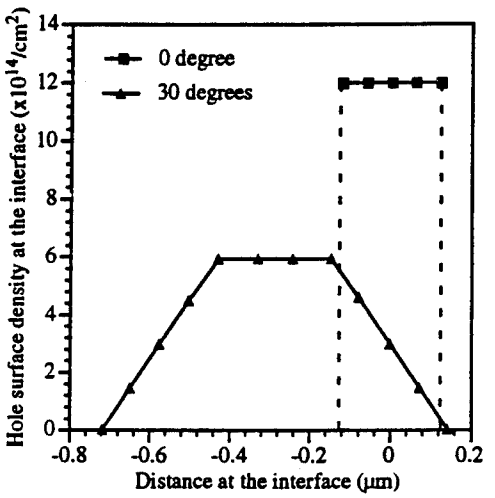


Fig. 9 Integration of the number of holes driven up to the interface over a depth of 1 micron, in the case of a normal incident ion and in the case of an ion with an incident angle equal to 30°. This figure indicates that the number of holes per unit area is larger when the incident angle is normal.

In the normal angle case, carrier generation is uniform throughout the shallow collection depth. In the case of an angle different from normal, two different situations can occur. If d sin θ > 2r (where d is the collection depth, r is the track radius and θ is the incident angle, relative to normal), only a portion of the integration depth has ion-generated holes, as illustrated in Figure 8.

However, when this relationship is not satisfied, there are ion-generated carriers throughout the collection depth. The areal density of carriers in this case is the same as in the normal incidence case. The trend exhibited by the experimental data suggests that the case where d sin θ > 2r is applicable here. Diffusion has not been included in this model. It would imply an increase in the radius of the track and a gaussian distribution of the carriers perpendicular to the track. This can be treated conceptually as an increase in the track radius.

Figure 9 shows a numerical example, where the track radius is 0.124μm, the electron-hole pair density is 1.2×10^{19} /cm^3 (which corresponds to the track previously described) and the collection depth is 1μm. In this figure, the origin of the x-axis corresponds to the point where the ion enters the silicon. Results are shown for normal incidence and also for an incident angle of 30°. As can be seen in Figure 9, when the incident angle is far from normal, the number of holes found in a given area is significantly lower than in the case of normal incidence. For high incident angles, the holes spread out over a wider area, so the number of holes per unit area is lower. This results in a lower electric field than for normal incidence, since the field due to the substrate response is proportional to the areal density of holes. These results were obtained for a case in which d sin θ > 2r, reducing the sensitivity to SEGR compared to normal incidence. However, it should be noted that this model only provides a possible explanation for the experimentally observed trends. One cannot state a priori that the condition d sin θ > 2r will be satisfied.

IV. Conclusion

Results from numerical simulations have shown, in accordance with experimental work, that an increase of temperature induces a higher oxide electric field which favors SEGR. The increased oxide field is due to a decrease of the carrier mobilities when temperature is increased. In addition, numerical calculation and heavy ion experiments indicate that track angles far from normal incidence lead to a lower electric field across the oxide and, thus, do not favor SEGR. In summary, simple physical arguments coupled with numerical simulations agree with the trends seen in experimental results on angular and temperature dependence of SEGR and give a better understanding of the physical mechanisms involved in SEGR.

V. Acknowledgments

The authors would like to acknowledge Marie-Catherine Calvet and Pierre Tastet for their contribution to this work and for their help and support for the heavy ion experiments. We would like to thank Frank Wheatley for assistance in obtaining the experimental samples. Finally, we would like to thank Frank Wheatley, Jeff Titus, and Ron Pease for useful discussions.

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Appendix: Models Used in the Simulations

Initially, in this work, simulations were performed with a very limited set of physical models. For these simulations, the models employed were: Boltzmann statistics, field-dependent mobility, concentration-dependent mobility, and temperature-dependent mobility. The goal of these first simulations was to obtain a preliminary understanding of the phenomena involved in SEGR.

However, to take into account additional effects that can take place in the device, several other models were added. Because of the high concentration in the track region, Boltzmann statistics do not apply and Fermi-Dirac statistics should be used. Carrier-carrier scattering, bandgap narrowing, and Auger and Shockley-Read-Hall recombination were also added. These models were added one at a time in the simulation. The addition of these models did not lead to any significant change in the results. Then, the impact ionization model, using the Selberherr relationship [7], was implemented. The addition of this model changed the time scale (with a maximum of the oxide electric field at 26ps instead of 4 or 5ps) and slightly decreased the amplitude of the maximum electric field in the oxide. The simulations were done with a 200-Å surface layer in the silicon in the interface area with impact ionization rates ten times lower than the values in the bulk silicon, in accordance with Slotboom et al. [8]. All of the results presented in this paper were obtained with all of these models turned on.

III.E. Single-Event Gate-Rupture in Power MOSFETs; Oxide Thickness Dependence and Computer Simulated Prediction of Breakdown Biases

Single-Event Gate-Rupture in Power MOSFETs: Prediction of Breakdown Biases and Evaluation of Oxide Thickness Dependence

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Abstract

Single-Event Gate-Rupture (SEGR) in Vertical Double Diffused Metal-Oxide Semiconductor (VDMOS) power transistors exposed to a given heavy ion LET occurs at a critical gate bias that depends on the applied drain bias. A method of predicting the critical gate bias for non-zero drain biases is presented. The method requires as input the critical gate bias vs. LET for $V_{DS} = 0V$. The method also predicts SEGR sensitivity to improve for larger gate-oxide thicknesses. All predictions show agreement with experimental test data.

I. Introduction

Single-Event Gate-Rupture can lead to power MOSFET failure in space. The SEGR process is initiated when a heavy ion strikes the device in the neck region. The neck region is the area between the p-body diffusions at the surface (see Fig. 1). The ion strike creates a filament of electron-hole pairs. For an n-channel power MOSFET, the generated holes drift toward the interface and the electrons toward the drain contact due to the electric field resulting from the positive drain bias. Upon reaching the interface, the holes start to 'pile up' at the interface and 'leak off', only slowly, toward the source contact. This pool of positive charge increases the electric field in the oxide, and when the field exceeds a critical value, oxide breakdown occurs. The collected holes then discharge through the oxide, heating the structure locally. If the breakdown current lasts long enough, a permanent short-circuit through the oxide results [1].

While progress has been made in empirically describing SEGR and modeling the mechanism [1]–[6], its dependence on structural parameters has not been elucidated. In this work, a simple model that utilizes two dimensional PISCES[1] simulations to predict SEGR breakdown condition for a given heavy ion LET is introduced. The predictions were used to investigate SEGR dependence on oxide thickness, LET of the incident ion, and the V_{GS} versus V_{DS} interrelation at rupture.

This work was supported by the Defense Nuclear Agency, Naval Surface Warfare Center – Crane, NASA — Goddard Space Flight Center, Aérospatiale, and Alcatel Espace

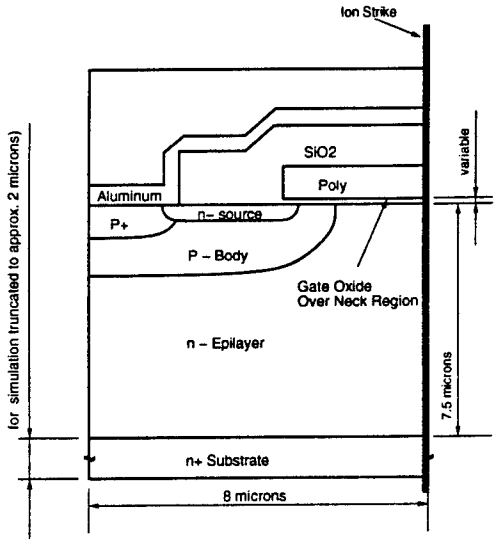


Fig. 1. One half of the cross section of the stripe geometry n-channel test device used in the experiments. For simulations, the device was approximated in cylindrical geometry to avoid time consuming 3-D computations.

A "base-line" cross section of the devices used in the 2-D simulations and in the experiments is illustrated in Figure 1. Device details for the simulated VDMOS transistors were based on SUPREM4[2] profiles for stripe geometry test structures that were built for experimental verification of oxide thickness dependence. The experimental data are reported fully elsewhere [3]. The following sections will further discuss the SEGR mechanism, present a methodology for predicting SEGR, and illustrate the excellent agreement between the prediction technique and experiment.

[1]ATLAS II, a PISCES version from Silvaco International
[2]ATHENA, a SUPREM4 version from Silvaco International

II. Mechanism of SEGR

When an energetic[3] ion strikes the VDMOS device through the neck region, it deposits energy along its track and generates electron-hole pairs in a cylindrical region surrounding the ion track. If the n-channel device is under positive drain-to-source bias V_{DS}, the generated carriers start to separate. The holes drift toward the interface and the electrons toward the drain contact as described in the Introduction. The charge separation in the silicon substrate and its consequent hole accumulation at the Si/SiO_2-interface is one of two contributors to the transient oxide field at the ion strike location. The magnitude of this first oxide field component is dependent on the drain-to-source bias V_{DS} and is a substrate charge collection effect. The second contribution to the oxide field is that due to carriers generated in the gate-oxide itself [4]. The charge separation in the oxide is different from the charge separation in the silicon substrate. The electrons are swept out rather quickly by the pre-existing field created by the applied gate-to-source bias V_{GS} (negative in our case). The holes, on the other hand, move slowly, probably by a complicated hopping mechanism, and for the time frame of interest ($< 100ps$) are effectively immobile in the oxide. These immobile holes change the oxide field locally [4]. The magnitude of this second component of the transient oxide field at the ion strike location is affected by the gate-to-source bias V_{GS}, and is an oxide charge-separation effect. It is not clear at present, how pronounced this contribution will be, nor its interaction with the charge separation mechanism in the substrate. However, the principle features of SEGR can be explained using the substrate response coupled with experimental information on oxide integrity in a radiation environment [5]. This will be demonstrated in the following sections.

III. Prediction Methodology

In order to evaluate SEGR hardness of power DMOS transistors, it is common practice to find the threshold biasing condition in a given radiation environment (LET of incident ion given). Operating a DMOS device below this threshold biasing conditions (V_{DS}, V_{GS}) guarantees safe operation whereas exceeding this threshold will result in gate rupture and, thus, destroy the DMOS transistor. One method to find these threshold biasing conditions is an experimental approach (see [2], [3], [6], [7]). However, these experiments are usually rather costly and time consuming. In this paper, we will show an alternative method to derive these threshold bias conditions by combining a fast and inexpensive prediction algorithm that utilizes 2-D simulation results (PISCES simulations) with measured oxide breakdown strength E_{cr} vs. LET data for $V_{DS} = 0V$. The method is based upon

$$V_{GS_{cr}} = d_{OX} \times (E_{cr} - E_{trmax}) \qquad (1)$$

where $V_{GS_{cr}}$ = critical gate-to-source bias for SEGR, E_{trmax} = maximum transient oxide field from 2-D simulation for $V_{DS} \neq 0$, E_{cr} = experimental input for $V_{DS} = 0$, and d_{OX} = oxide thickness. Each of these components is now to be described in detail.

[3]The amount of energy deposited by an incident ion per unit of track length is expressed in terms of its Linear Energy Transfer (LET) in units of $MeVcm^2/mg$

III. A Modeling the Transient Oxide Field ($V_{DS} \neq 0$)

SEGR dependence on LET, gate-oxide thickness, and V_{GS} versus V_{DS} interrelation in VDMOS n-channel power transistors was investigated through 2-D simulations. For all simulations, the ion was assumed to traverse the device at normal incidence through the center of the neck region. In the simulations, we used cylindrical geometry and generated the charge due to the passing energetic ion as a charge cylinder with a Gaussian lateral distribution of characteristic length $L = .07\mu m$ and uniform distribution in depth. Details of the simulation of the ion track are given in the Appendix.

An example of the transient oxide field obtained from 2-D simulations is shown in Figure 2. Input data supplied by a user

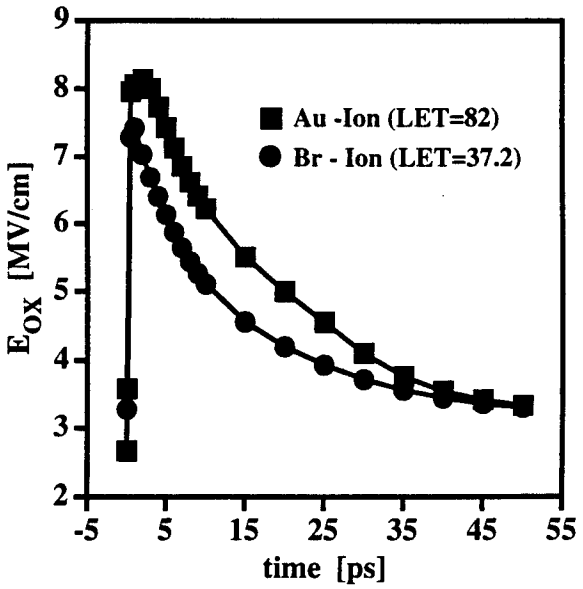


Fig. 2. Transient oxide field component at track location superimposed on DC component as a function of time after ion strike for bromine and gold as the incident ions. Typically, the peak field is reached within a few picoseconds. Parameters: LET=37.2(Bromine) and 82(Gold) $MeVcm^2/mg$, V_{GS}=-13.9V, V_{DS}=30V, d_{OX}=50nm.

for the simulation includes structural dimensions of the test device, energy and spatial information of a traversing ion, and bias conditions for the device. The simulator then computes various physical quantities including potential distribution, electric fields, and carrier concentration profiles. The result of practical interest is a critical biasing condition for a VDMOS device that leads to SEGR (for a given LET value of the incident ion). A difficulty in applying our 2-D simulation results is that no oxide breakdown model is included in the simulations. We now describe how we have dealt with this problem.

If we assume the total charge generated in the oxide is small compared to the filament charge in the silicon, then the electric field in the oxide is the sum of a transient field component due to substrate charge collection effects (related to V_{DS} [1]) plus a DC field component due to V_{GS} (see equation (2)).

$$E(t) = E_{tr}(t) + E_{DC} \qquad (2)$$

The DC part of the oxide field E_{DC} can be calculated with the simulator for any given biasing condition when there is no ion strike (zero charge generation). E_{DC} is approximately (neglecting workfunction differences)

$$E_{DC} \approx |V_{GS}|/d_{OX} \quad . \tag{3}$$

For sufficiently negative V_{GS} values (in n-channel devices), there is no dependence of E_{DC} on V_{DS} because the surface is inverted and the inversion layer places the Si/SiO_2-interface on the same equipotential as the grounded body contact [4]. The simulated transient component of the oxide field, E_{tr}, reaches its peak value within a few picoseconds after the charges due to the traversing ion are generated (see for example Figure 2). The transient field persists for a time of about 50ps which varies somewhat with LET and V_{DS}.

One might expect that oxide transients of such short duration would not be as fully effective as a DC oxide field in causing SEGR. However, comparison of 2-D simulations at biasing conditions where SEGR was detected experimentally with experimental results indicated that failure occurs when the transient oxide field exceeds a critical value, E_{cr}, made up of *any combination* of DC and transient components.

Using equation (5) for the LET-dependence of E_{cr}, and the empirical assumption that transient and DC oxide field contribute on the same basis to E_{cr}, it is simple to predict a critical gate-to-source bias $V_{GS} = V_{GS_{cr}}$ that initiates SEGR for a given heavy ion LET and a given drain-to-source bias $V_{DS} \geq 0$.

III. B DC Input Data ($V_{DS} = 0$)

For DC applied fields and for normal incidence of the ion, Wrobel [5] measured the dependence of E_{cr} on the ion's LET value. Equation (4) is Wrobel's empirical fit to experimental breakdown data on heavy-ion irradiated MOS-capacitors,

$$E_{cr} = 40.8 \frac{1}{\sqrt{LET}} \quad , \tag{4}$$

where LET is in $MeVcm^2/mg$ and E_{cr} is in MV/cm. This fitting function is inaccurate for low LET values where it predicts that E_{cr} is infinite as the LET value approaches zero. A better fit to the data that agrees with the intrinsic breakdown value of $E_{cr} = E_0$ for LET values of the incident ion approaching zero is,

$$E_{cr} = \frac{E_0}{1 + LET/B} \quad , \tag{5}$$

where LET and B is in $MeVcm^2/mg$ and E_{cr} and E_0 is in MV/cm. It is usually very difficult to measure the intrinsic breakdown field of a gate-oxide (LET=0) using MOS devices because the oxide usually tends to break down at a lower field strength at a defect related weak spot of the oxide [8], [9]. The breakdown location for irradiated oxides, on the other hand, will be at the strike location that usually does not coincide with a weak spot of the oxide. Therefore, to extract dielectric breakdown data of the gate-oxide (E_{cr} vs. LET), the breakdown field for $LET = 0$ will not be measured but extrapolated by fitting expression (5) through the experimental data points for $LET > 0$. Applying this procedure to Wrobel's [5] experimental breakdown data yields $E_0 = 11.1 MV/cm$ and $B = 62.1 MeVcm^2/mg$. The breakdown strength of different oxides varies somewhat due to different processing steps, and is a necessary input for our prediction algorithm. The solid line in Figure 3 was obtained by fitting equation (5) to the breakdown data for the devices used in this work ($E_0 = 9.1 MV/cm$, $B = 58.0 MeVcm^2/mg$). The symbols

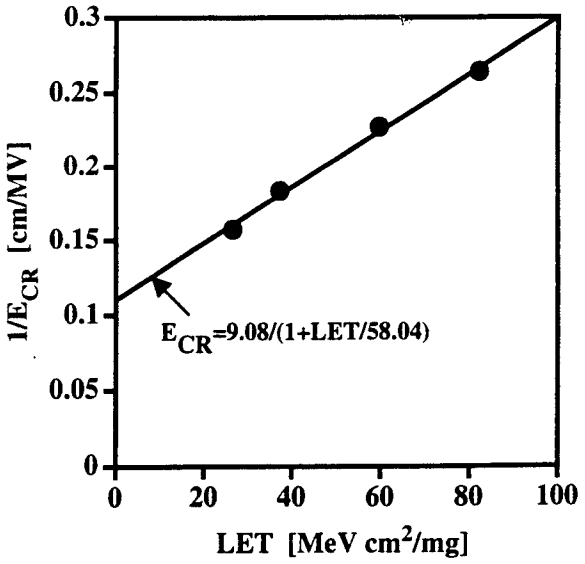


Fig. 3. Inverse breakdown field due to applied gate-to-source bias V_{GS} versus LET of the incident ion. Symbols show experimental data on irradiated devices with $V_{DS} = 0$ and solid line was obtained by a least square fit of expression (5) to devices with various oxide thicknesses.

in Figure 3 correspond to experimental data points taken from the stripe line geometry DMOS transistors used in this work. This oxide integrity information needs to be known accurately in order to make a prediction. For our data, E_{cr} varies by less than 6.4% for our samples with d_{OX} in the range 50nm - 150nm. Sensitivity to $V_{DS} = 0$ data increases as E_{cr} approaches E_{trmax} because the relative error $\frac{\delta V_G}{V_G}$ in V_G is

$$\frac{\delta V_G}{V_G} = \frac{\delta E_{cr}}{E_{cr}} \left(\frac{1}{1 - \frac{E_{trmax}}{E_{cr}}} \right) - \frac{\delta E_{trmax}}{E_{trmax}} \left(\frac{1}{\frac{E_{cr}}{E_{trmax}} - 1} \right) \tag{6}$$

Because the transient field E_{trmax} is closer to E_{cr} for large V_{DS}, large drain bias predictions are more sensitive to errors δE_{cr} in measured E_{cr} and to errors δE_{trmax} in modeled E_{trmax}.

III. C Outline of Method

Below, an outline is given that shows how to obtain a prediction for the maximum (critical) gate-to-source bias V_{GS} that can be applied to a VDMOS power transistor for a given heavy ion LET with a specified drain-to-source bias $V_{DS} \geq 0$. Exceeding this critical bias V_{GS} will initiate SEGR and cause destruction of the device.

1. Define input deck for 2-D simulator including
   - device geometry and dimensions.

- drain-to-source bias, $V_{DS} \geq 0$, where corresponding critical gate-to-source bias, V_{GS}, is sought.
- input parameters for charge distribution along the ion track (apply equations (A7)–(A10) shown in Appendix).
- arbitrary negative gate-to-source bias, V_{GS}, sufficient to invert the surface (The transient portion of the oxide field due to substrate charge separation computed below does not depend on the choice of V_{GS} at this point.) .

2. Run 2-D simulation
   - find the DC field component E_{DC} (LET=0).
   - initiate charge filament appropriate to the ion LET along ion strike path and continue with a transient simulation to compute oxide field versus time at the strike location.
   - extract the peak field magnitude E_p.
3. Compute peak magnitude of transient oxide field component (at given drain-to-source bias V_{DS})

$$E_{trmax} = E_p - E_{DC} \tag{7}$$

4. Compute critical oxide field E_{cr} for given LET of incident ion from equation (5).
5. Compute critical gate-to-source bias, V_{GS}, (for given V_{DS} and LET) with equation 1.

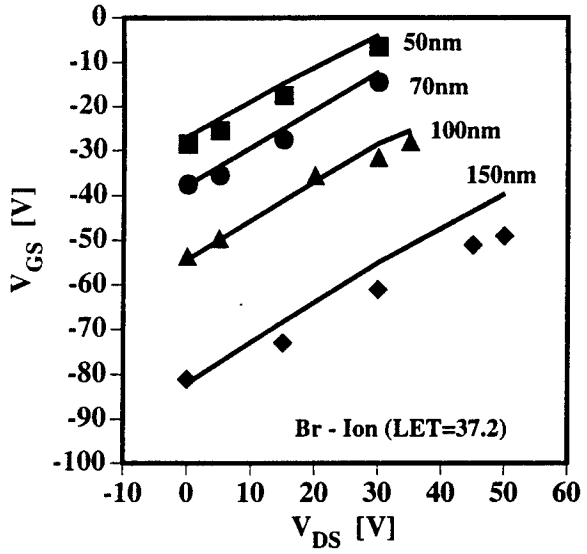


Fig. 4. V_{GS} versus V_{DS} at rupture point for bromine irradiation (LET=37.2 $MeVcm^2/mg$) with five different gate-oxide thicknesses. Symbols are from experiments and solid lines show prediction results.

III. D Simulation Results

Four different gate oxide thicknesses ranging from 50nm to 150nm as used in the experiments [3] were simulated. For every change in oxide thickness, the structure underneath the Si/SiO_2-interface was left unchanged and only the thickness of the gate-oxide was adjusted to the desired value. The drain bias V_{DS} was held at a bias of interest and the arbitrary value of the gate-to-source bias V_{GS} was chosen between -6.5V and -28.5V (sufficiently negative to invert surface prior to the ion strike). Simulations were performed for three different incident ions (i.e., Nickel (LET = 26.6 $MeVcm^2/mg$), Bromine (LET = 37.2 $MeVcm^2/mg$), and Gold (LET = 82 $MeVcm^2/mg$)) and for all the various oxide thicknesses the critical oxide breakdown strength was taken from the data shown in Figure 3.

Table I shows predicted values of gate-to-source bias sufficient for SEGR to occur, $V_{GS_{cr}}$, at several different drain-to-source biases, V_{DS}, for an incident bromine and gold ion.

IV. Comparison of Predictions with Experiments

All experiments were performed at the Brookhaven National Laboratories (BNL) tandem Van de Graaff facility and are reported fully elsewhere [3]. Figure 4 shows the threshold biases V_{DS} and V_{GS} for a bromine incident ion. The symbols in Figure 4 show experimental data points for five different gate-oxide thicknesses ranging from 50nm to 150nm. The solid lines in Figure 4 were obtained with our prediction algorithm (see also Table I). The predicted threshold biases are in excellent agreement with experimental data for all oxide thicknesses investigated in this work. Figure 5 shows the threshold biases V_{GS} at a drain bias of V_{DS} = 30V as a function of LET to further verify the usefulness and potential of this prediction algorithm. Again, the prediction are in excellent agreement with experiments for all three different gate-oxide thicknesses.

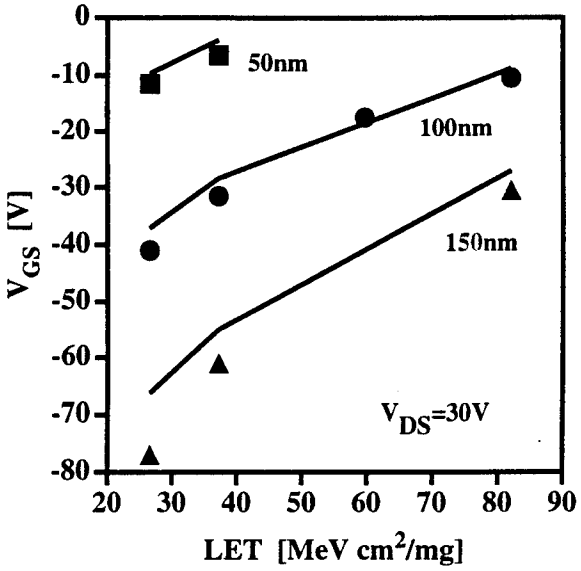


Fig. 5. V_{GS} versus LET of the incident ion at rupture point for V_{DS} = 30V and three different gate-oxide thicknesses. Symbols are from experiments and solid lines show prediction results.

V. Physical Basis of Trends

With the aid of our prediction algorithm, it is possible to predict various dependencies of SEGR in power VDMOS tran-

TABLE I

SIMULATION AND PREDICTION RESULTS FOR BROMINE AND GOLD IRRADIATION.

Bromine (LET = 37.2 $MeVcm^2/mg$)						**Gold (LET = 82 $MeVcm^2/mg$)**					
Simulation Input Data			**Simulation Results**		**Predicted $V_{GS_{cr}}$**	**Simulation Input Data**			**Simulation Results**		**Predicted $V_{GS_{cr}}$**
d_{ox} [nm]	V_{DS} [V]	$-V_{GS}$ [V]	E_P [MV/cm]	E_{DC} [MV/cm]	$-V_{GS_{cr}}$ [V]	d_{ox} [nm]	V_{DS} [V]	$-V_{GS}$ [V]	E_P [MV/cm]	E_{DC} [MV/cm]	$-V_{GS_{cr}}$ [V]
50	0	28.5	5.75	5.584	26.83	50	5	15.5	4.1	2.988	13.25
50	15	17.5	5.98	3.387	14.7	50	15	23.5	7.41	4.585	4.69
50	30	13.9	7.43	2.669	3.859	50	30	13.9	8.13	2.669	-8.50
70	0	37.5	5.42	5.274	37.71	70	5	15.5	2.95	2.136	20.64
70	15	17.5	4.38	2.421	25.02	70	15	23.5	5.35	3.276	11.82
70	30	6.5	4.65	0.857	12.18	100	5	15.5	2.07	1.496	31.89
100	0	53.5	5.39	5.292	54.35	100	15	23.5	3.79	2.295	22.68
100	15	17.5	3.12	1.696	41.09	100	30	13.9	4.22	1.337	9.13
100	30	13.9	4.03	1.337	28.4	150	5	15.5	1.39	0.999	50.58
100	35	20	4.93	1.945	25.48	150	15	23.5	2.55	1.531	41.16
150	0	81	5.43	5.361	81.96	150	30	13.9	2.85	0.893	27.09
150	15	17.5	2.11	1.132	68.32						
150	30	13.9	2.76	0.893	54.99						
150	50	20	4.19	1.298	39.61						

sistors. In this work, we have shown this to be true in predicting SEGR threshold values of V_{GS} versus V_{DS}, LET dependence, and gate-oxide thickness dependence. Figure 6 shows a circuit model for the SEGR mechanism proposed by Brews et al. [1]. All three dependences of SEGR sensitivity shown in this work (V_{DS}, LET, and d_{OX}) can be physically explained with the aid of this circuit model.

The magnitude of the filament current, I_F, resulting from the hole collection at the Si/SiO_2-interface, increases with larger drain-to-source bias V_{DS} because the increased substrate field will enhance hole collection at the Si/SiO_2-interface. A larger I_F results in a larger voltage drop across the oxide and therefore in an increased oxide field, thus explaining the trend shown in Figure 4.

A similar argument can be used to describe the LET sensitivity of SEGR in DMOS transistors. A larger LET value of the incident ion will yield a larger density of charge deposited along the ion track and therefore a larger filament current I_F can be anticipated. As a result, a larger LET value lowers the SEGR biases.

Figure 7 shows the gate-to-source threshold bias versus gate-oxide thickness at two different drain-to-source biases. The circuit model in Figure 6 explains the behavior seen in Figure 7 as follows. The charges from the filament current I_F that have collected at the interface leak off toward the grounded body/source region along an interfacial path that is modelled as a distributed RC-line. The faster the positive charges (holes) leak off, the smaller the transient oxide field will be. The leakage path time constant can be approximated by $\tau = RC$, where R is the surface

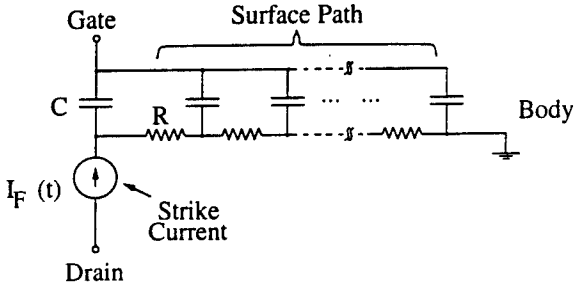


Fig. 6. Circuit model for the SEGR mechanism derived by Brews et al. [1].

resistance and C is related to the gate-oxide capacitance. Increasing the gate-oxide thickness decreases the capacitance C. A smaller capacitance C will result in a smaller leakage path time constant τ, thus verifying the trend of an increased likelihood of SEGR for thinner gate oxides.

VI. CONCLUSION

A simple prediction method for SEGR using a 2-D device simulator was presented. This prediction method utilizes oxide breakdown information (i.e. SEGR data for $V_{DS} = 0$) to predict critical rupture biases (V_{GS}, V_{DS}) for a given heavy ion LET on devices operated at a nonzero drain-to-source bias (i.e. $V_{DS} > 0$ for n-channel device). Prediction results showing critical threshold conditions to initiate SEGR in DMOS power transistors are in excellent agreement with experimental data. The observed

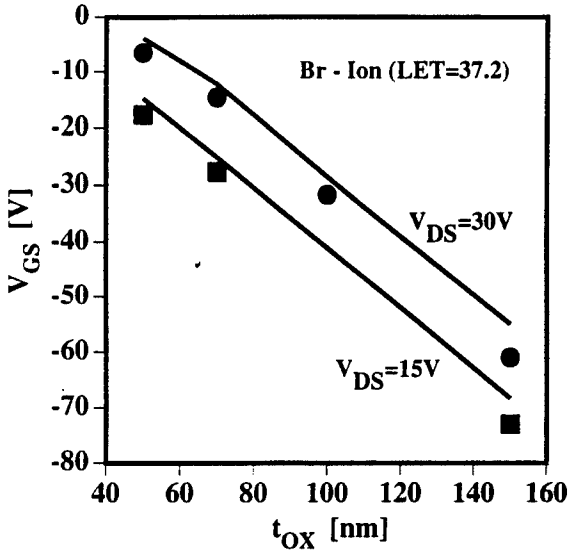


Fig. 7. V_{GS} versus gate-oxide thickness d_{OX} at rupture point for bromine irradiation (LET=37.2 $MeVcm^2/mg$) at two different drain-to-source biases V_{DS}. Symbols are from experiments and solid lines show prediction results.

dependence of SEGR on V_{GS} versus V_{DS}, gate-oxide thickness, and the LET value of the incident ion confirm the prediction algorithm.

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APPENDIX

Equation (A7) shows the mathematical form of the charge distribution, with r = radial direction, where r = 0 corresponds to the center of the track/neck region. Expressions (A8)–(A10) were used to calculate the carrier concentration per unit volume N_0 at the track center [10]. The charge distribution of the track is generated uniformly in depth. A more accurate representation of the charge generation along the ion track could be obtained by taking the energy loss of the ion along its path through the device into account. However, extensive 2-D simulations have shown that only the charges generated in approximately the first micron from the Si-SiO_2-interface contribute to the collected holes that raise the oxide field.

$$N(x) = N_0 \exp\left\{-\left(\frac{r}{L}\right)^2\right\} \tag{A7}$$

$$N' = \int_0^{2\pi} d\phi \int_0^{\infty} rN_0 \exp\left\{-\left(\frac{r}{L}\right)^2\right\} dr = N_0 \pi L^2 \tag{A8}$$

$$N' = \frac{LET[MeVcm^2/mg] \times 2.33[gm/cm^3]}{3.6[eV/pair]} \times 10^9 \tag{A9}$$

$$N_0 = \frac{N'}{\pi L^2} \tag{A10}$$

For convergence reasons, the charge column due to the traversing heavy ion could not be deposited instantly at time t = 0, but had to be ramped up to its final value over a short time interval, t_0 = 1fs. This was achieved by increasing the carrier generation rate constant locally in the track region and running a transient simulation up to $t = t_0$. For $t > t_0$, no further pair generation is allowed, and the electron/hole transport in the substrate is modeled using the simulator. Extensive tests of different mesh structures used for the simulation were done in an attempt to reduce the number of grid points and, thus, to speed up the computation time while still maintaining accuracy. The simulator has the ability to include various physical models (e.g., Shockley-Read-Hall (SRH) and Auger recombination, concentration dependent lifetimes, Boltzmann statistics versus Fermi-Dirac statistics, concentration dependent mobility, field dependent mobility, etc.). Of all the various models, only the field dependent mobility model had a noticeable effect on the simulation results for the structure and biasing conditions used in this work. The peak magnitude of the transient oxide field is slightly larger for the case where field dependent mobility is included and the time for which the peak oxide field persists is much larger when field dependent mobility is included. If the peak of the transient field persists for a longer time, it is more likely that the role of this transient field component is as effective as the DC component. However, the predicted threshold bias condition computed with our prediction algorithm agree within $\leq$ 10% (with and without field dependent mobility model included). For this reason, all the simulation results reported in this paper were obtained without inclusion of a field dependent mobility model.

III.F. Experimental Evidence of the Temperature and Angular Dependence in SEGR

Experimental Evidence of the Temperature and Angular Dependence in SEGR†

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Abstract

Heavy ion experiments were used to investigate temperature and angular dependence in Single-Event Gate Rupture (SEGR). They clearly show that a normal incident angle favors SEGR. The influence of elevated temperature on the SEGR phenomenon is shown to be immaterial. When oxide effects were separated from substrate effects, the trends remained identical. This demonstrates that both the oxide and substrate response play a major role in determining the SEGR sensitivity.

I. INTRODUCTION

Double-diffused metal-oxide-semiconductor (DMOS) power devices are capable of conducting large currents when turned on and withstanding large voltages when turned off [1]. Power DMOS transistors are widely used in space applications. However, in the cosmic-ray environment, they are exposed to energetic heavy ions. The passage of a single heavy ion through the device can lead to significant permanent degradation of the device or even catastrophic failure.

In power Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), two single event effects have been observed: Single-Event Burnout (SEB) and SEGR. These phenomena can be understood in terms of the physical structure of the device. A cross section of a power DMOS transistor is shown in Figure 1.

SEB can occur in n-channel power MOSFETs when a heavy ion strikes the device in the portion of the p-body where the channel is formed, in the p-body under the n^+ source, or in the neck region within close proximity to the p-body [2]. The passage of an ion through those regions generates a current filament that locally turns on a parasitic npn bipolar junction transistor (BJT) inherent to the power MOSFET. Depending on how strongly this BJT is initially turned on, the currents within the device can regeneratively increase, through an avalanche process, until second breakdown of the parasitic BJT occurs, leading to failure of the device [3].

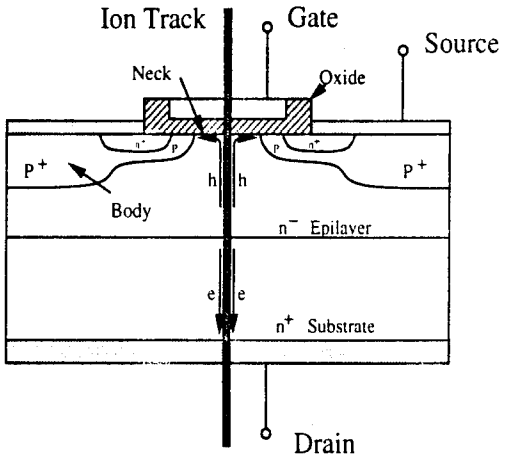


Fig. 1 Power MOSFET structure, showing an ion-strike filament at the center of the n-neck region, with holes moving upward and electrons downward under the influence of the positive drain voltage.

SEGR can occur when a heavy ion strikes the neck region of the device (see Figure 1). The energy deposited by this ion creates a high-density filament of electron-hole pairs in both the oxide and the silicon. When a positive bias is applied on the drain electrode of an n-channel power MOSFET, the pairs created along the ion track are separated; the holes are driven

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toward the gate and the electrons flow toward the drain, as shown in Figure 1. The accumulated holes at the Si-SiO_2 interface and their image charge in the gate electrode cause the electric field in the oxide to increase. For large enough fields, oxide breakdown can occur. This model is supported by room-temperature simulations for normally incident ions [4].

While the temperature and angular dependence of SEGR have been examined through preliminary experiments [5,6] and simulations [6], the evidence has been inconclusive. This paper reports on detailed experiments designed to determine the temperature and angular dependence of SEGR, and the oxide and substrate response is evaluated for these effects.

II. Experimental Conditions

A. IPN Experiments

Tests performed at the IPN (Institut de Physique Nucléaire) component dedicated testing line, set up by the CNES (Centre National d'Etudes Spatiales), in Orsay, France, had a triple objective. Angular dependence in SEGR, temperature dependence in SEGR, and oxide effects on angular and temperature dependencies in SEGR were investigated.

Six different commercial n-channel power MOSFETs were tested. They were IRF440s from three different manufacturers (Motorola: lots 9316 and 9307; International Rectifier: lot 9350; and Harris: lot 9404) and IRF140s from the same three manufacturers (Motorola: lot 9336; International Rectifier: lot 9339; and Harris: lot 9351), mounted in TO3 packages. The breakdown voltage of the IRF440s was between 550 V and 659 V (Harris: 550 V and 562 V; IR: 562 V and 579 V; Motorola: 560 V and 659 V); the breakdown voltage of the IRF140s was between 115 V and 133 V (Harris: 119 V and 133 V; IR: 120 V and 122 V; Motorola: 115 V and 120 V).

For each power MOSFET tested, SEGR was first examined for normal incidence at room temperature. Then, high incident angle tests (still at room temperature) and high temperature tests (normal incidence, temperature of about 110 °C) were done. To study the role of the transient oxide response in SEGR, the drain bias V_{DS} was set to 0 V, in order to prevent any contribution due to the DC bias of the substrate. High incident angle and high temperature investigations were done under $V_{DS} = 0$ V conditions.

The tandem Van de Graaff accelerator has the capability of providing many medium energy ions. The ions chosen for the experiments were Nickel (Energy: 182 MeV; Range: 30 µm (Si); LET (Linear Transfer Energy): 27.2 MeV-cm^2/mg) and Bromine (Energy: 196 MeV; Range: 31 µm (Si); LET: 36 MeV-cm^2/mg). During irradiation, the beam flux (typically, 500 to 2000 ions/cm^2/s) was indirectly measured by a detector located in the scattering chamber, in line with the beam. A diode placed in the vacuum chamber allowed the control of the homogeneity and energy calibration of the beam [7].

The setup used to monitor these experiments was STAM (Analogic Modular Test System)-MOS, provided by the CNES. This system allows experimenters to monitor and to control the device's temperature, gate and drain biases, and currents. Test values and maximum allowed values for these parameters were programmed. Every 2 ms, the values of the test parameters were compared to these limits. The power supplies were shut down as soon as a threshold was reached. The variations of the tests parameters were saved every 10 ms or less often, together with the ion fluence and the testing time. No parameter was recorded when no change was detected. The status of the test parameters was graphically displayed on the screen of a portable PC.

The value of a limiting resistor in series with the drain was chosen to be 100 kΩ to prevent destruction of devices due to SEB. During a test, current spikes in the drain lead (SEB events) were counted. There is no need for counting current spikes in the gate lead since an SEGR event cannot be interrupted, is catastrophic, and leads to permanent failure of the device. An event was counted on the drain each time the drain voltage decreased by 50 V. An SEGR event was defined to have occurred when the gate current was in excess of 2 µA and did not return to the range of several nA, when the test resumed.

The SEB or SEGR events could also be seen and saved on a digital oscilloscope (Tektronix TDS540).

The DUTs (Devices Under Test) were fixed on aluminum sockets which were thermally isolated from the circuit on the board and monitored in temperature. A resistive heater was used to increase the temperature of the devices. The heating power was 50 W per device. The highest temperature used in these tests was 116 °C.

The device to irradiate was selected with the positioning system TILT (Tests Ions Lourds Tandem). Four power MOSFETs could be put on the same board and tested one at a time. Once in the vacuum chamber, the board could be rotated, to get a beam incident angle different from normal. TILT also allows one to monitor the opening and closing of the shutter.

The test strategy was first to perform an initial experiment on a given device. For this initial test, the temperature was set at room temperature and the heavy ion had a normal incidence. The gate bias V_{GS} was first set at -15 V. The drain bias V_{DS} was increased in steps of 25 V for the IRF440s and in steps of 10 V for the IRF140s. If SEB events were detect

before SEGR occurred, V_{GS} was incremented by -5 V and the test started again on the same device with this new value for the gate bias.

This test provided an initial starting value of V_{GS} and V_{DS} for SEGR failure of the device. Then, a new device was selected and the test was performed at the V_{GS} obtained when SEGR was observed in the initial test, with a smaller V_{DS} increment (5 V for the IRF440s and 2 V for the IRF140s). V_{DS} was increased after a fluence of 50,000 particles/cm^2 was reached without failure.

B. Brookhaven Experiments

Additional temperature SEGR testing was conducted at BNL (Brookhaven National Laboratory), Long Island, NY, USA. The test objective was to determine whether temperature variation has no impact on the SEGR threshold, or whether the effect of temperature on SEGR actually exists, but is extremely weak, and, thus, should be neglected.

The parts tested were experimental n-channel power MOSFETs, with a stripe geometry, provided by Harris Semiconductor, mounted in TO3 packages. Since these devices are from the same wafer, the dispersion in the experimental results is very low. The gate oxide is 50 nm thick. The drain breakdown voltage is 73 V. The devices were electrically screened. They were tested for gate integrity, and for threshold voltage, V_{TH}. Wheatley et al. described these parts in detail [8].

For each of the tested devices, V_{DS} was fixed and V_{GS} was varied until SEGR occurred. Three devices were tested at room temperature (25 °C), with V_{DS} = 5 V, as well as with V_{DS} = 20 V. Likewise, three devices were tested at high temperature (90 to 92 °C), with V_{DS} = 5 V, as well as with V_{DS} = 20 V.

The tandem Van de Graaff accelerator of the SEU Test Facility at BNL provides various monoenergetic ions. The ion chosen for this test was Iodine (Energy: 311.7 MeV; Range: 30.4 μm (Si); LET: 59.7 MeV-cm^2/mg). During irradiation, the ion beam flux (typically 10^4 ions/cm^2/s), its fluence, the beam homogeneity, the opening and the closing of the shutter, the x-y-z position of the sample, and the vacuum system were controlled by an automated computer system.

The test system used to monitor these experiments has been previously described [8,9]. Drain and gate voltages, and currents were checked every 10 ms, as well as the device temperature. Currents as low as 1 nA could be measured. An SEGR event was recorded when the gate current exceeded 10^{-8} A. The status of the test parameters was displayed on the screen of a portable PC.

The temperature test board was built to hold 9 devices. The DUTs were fixed on zero-insertion-force sockets. A resistive heater was used to increase the temperature of the DUTs. The heating power was 10 W per device. The highest temperature used in these tests was 95 °C. The drain and gate electrodes of each DUT were electrically isolated from the other 8 test samples using a rotary switch.

The test methodology was to determine the V_{GS} threshold for SEGR of three devices at room temperature, for V_{DS} = 5 V, and also for V_{DS} = 20 V. This process was repeated at high temperature, for V_{DS} = 5 V and V_{DS} = 20 V. An estimate of V_{GS} for SEGR at room temperature, with these drain biases, was obtained from previous work [8]. The drain bias was set at 5 V or 20 V, and the magnitude of the gate bias was set 2 to 3 V below the expected failure value. The magnitude of the gate bias was then increased, in 0.25 V steps, until SEGR occurred. This is the smallest voltage step ever reported in SEGR experiments. V_{GS} was incremented after a fluence of 70,000 particles/cm^2 was reached.

III. Experimental Results

A. Angular Dependence

Figure 2 and 3 include the results of heavy ion experiments in the case of normal incidence (0°), and in the case of an incident angle different from normal (15°, 25°, or 48°) for the IRF440s and IRF140s, respectively. It should be noted that the starting incident angle was 48° in any case. When no SEGR failure occurred for this value, the incident angle was lowered to 25°, and to 15°. The incident ion was Bromine. It can be seen that, for every device, the sensitivity to SEGR is reduced when the ion incident angle is different from normal. SEGR was observed for higher values of V_{DS} when the incident angle was different from normal. For some parts, SEGR was not observed at all for high values of V_{DS} ($V_{DS} \geq 300$ V for the IRF440s; $V_{DS} \geq 80$ V for the IRF140s) when the incident angle was far from normal ($\theta \geq 25°$). This case refers to the absence of any event, or the onset of an SEB event at a value of V_{DS} higher than the value of V_{DS} for SEGR failure in normal conditions. However, lowering the incident angle below its initial value (typically 48°) lead to an SEGR failure of some devices.

These data experimentally show that the likelihood for SEGR increases when the ion incident angle is made closer to normal. This result is in good agreement with experimental results previously reported [5,6]. As shown earlier, this trend is due to a distribution of the carriers over a wider area at the Si-SiO_2 interface when the incident angle approaches normal [6].

These data are the most thorough experimental treatment of angular dependence that has been published. To our knowl-

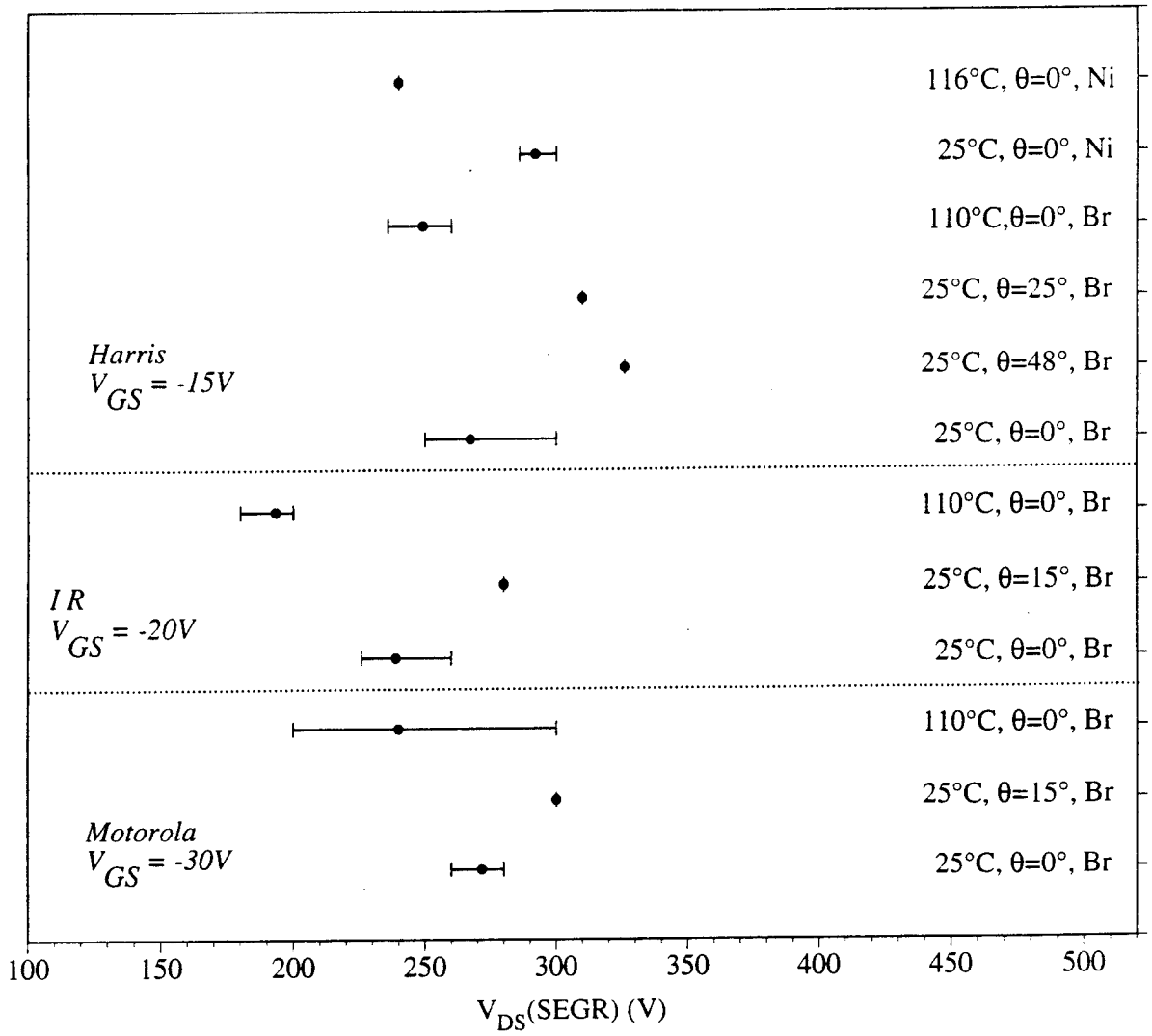


Fig. 2 Experimental drain voltage for SEGR failures for the IRF440s from Motorola, International Rectifier, and Harris. The bar symbols represent the minimum and maximum value of V_{DS} for which SEGR occurred. The filled circle symbols represent the average value of V_{DS} for which SEGR occurred. The ions used were Bromine and Nickel. Three different cases are represented in this figure: normal incidence at room temperature, incident angle different from normal at room temperature, and normal incidence at high temperature. The gate voltage used for each part type is also indicated.

edge, no experimental SEGR failure previously has been reported at incident angles different from normal. Other data available only mention no failure, or SEB failure, at incident angles different from normal. In this work, we have shown that SEGR can occur at nonzero incident angles, and that the V_{DS} for failure in this case is higher than in the normal incidence case. This trend is true for 100 V devices and for 500 V devices, from three different manufacturers.

B. Temperature Dependence

Figure 2 and 3 include the results of heavy ion experiments at room temperature (about 25 °C), and elevated temperature (about 110 °C) for the IRF440s and the IRF140s respectively. The incident ions were Bromine and Nickel. Most of the parts tested show a large amount of dispersion in their experimental temperature dependence.

For most of the parts, no general rule can be derived: as can be seen in Figures 2 and 3, the room temperature and the high temperature V_{DS} ranges are overlapping.

The reason that no clear experimental trend could be obtained may be due to the destructive nature of SEGR testing. For this reason, it is not possible to determine the bias dependence of SEGR in a single device. In addition, there might be a dispersion between parts from different diffusion lots. The absence of any clear trend could thus be due to a small magnitude of the temperature effect, compared to the part-to-part variability. In conclusion, no statistically significant temperature dependence was observed in this test.

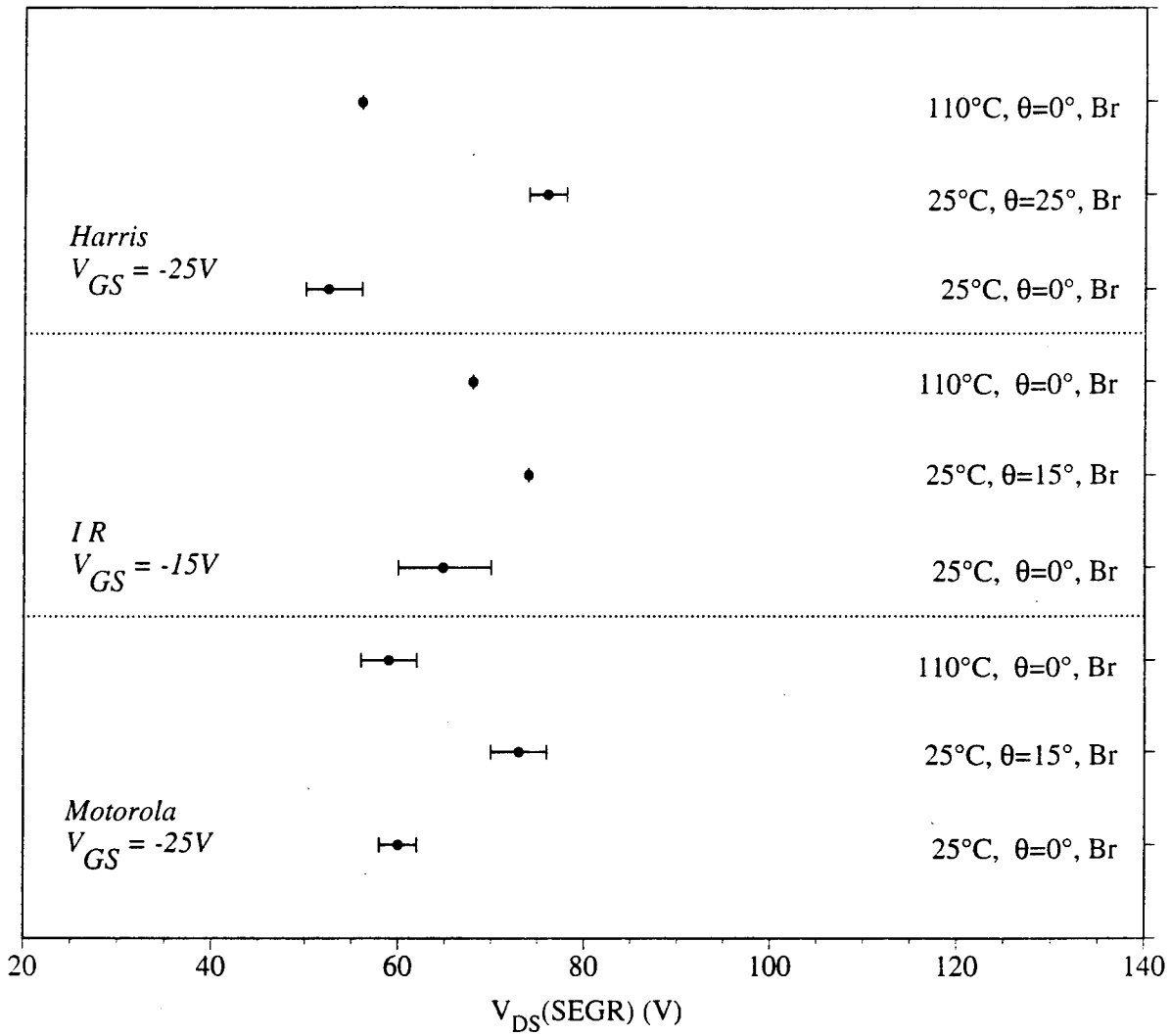


Fig. 3 Experimental drain voltage for SEGR failures for the IRF140s from Motorola, International Rectifier, and Harris. The bar symbols represent the minimum and maximum value of V_{DS} for which SEGR occurred. The filled circle symbols represent the average value of V_{DS} for which SEGR occurred. The ion used was Bromine. Three different cases are represented in this figure: normal incidence at room temperature, incident angle different from normal at room temperature, and normal incidence at high temperature. The gate voltage used for each part type is also indicated.

For this reason, additional tests were performed at BNL, on parts coming from the same wafer. The first results obtained with this part type showed little variability. In addition, the voltage step used was very small, to allow detection of even minor temperature effects on SEGR.

The results of these tests are presented in Table I and in Figure 4. As can be seen in Table I, the results show very little dispersion. These measurements point out the existence of a small temperature effect on SEGR. For this particular device, a higher temperature would be a slightly better case. When V_{DS} is fixed, the magnitude of the gate bias required to induce SEGR at 90 °C is a quarter volt larger than at room temperature.

The influence of temperature on the oxide electric field of the devices tested has been simulated, using ATLAS II, the 2D SILVACO version of PISCES [10]. The mobility model used included field-dependent mobility, concentration-dependent mobility, and temperature-dependent mobility. Simulations were run at three different temperatures: 300K, 400 K, and 500K. Figure 5 shows the maximum electric field in the oxide as a function of time. The maximum oxide electric field is slightly lower at higher temperature, in excellent agreement with the experimental results. This supports the existence of a minor temperature effect.

As stated, the temperature effect on SEGR is a second order effect. The very small voltage step used here demonstrates clearly how small this effect is. Numerical simulations are in agreement with this result.

Table I

Experimental V_{GS} for SEGR at room temperature, and at high temperature (90 to 92 °C). V_{DS} was fixed, and taken equal to 5 V and to 20 V. These results show that, for the device tested, V_{GS} for SEGR at high temperature is a quarter volt higher than at room temperature.

Device #	Temperature (°C)	V_{DS} (V)	V_{GS} (SEGR) (V)
1	25	5	-18.875
2	25	5	-18.875
3	25	5	-18.875
4	25	20	-6.375
5	25	20	-6.375
6	25	20	-6.125
7	91	5	-19.125
8	91	5	-19.125
9	92	5	-18.125
10	91	5	-19.125
11	91	20	-7.125
12	92	20	-6.625
13	90	20	-6.625

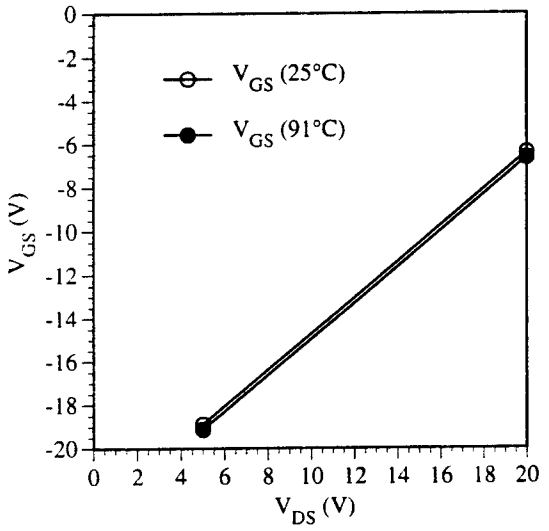


Fig. 4 Plot of V_{GS} versus V_{DS}, showing the experimental points where SEGR occurred, at room temperature and at high temperature. The value taken for V_{GS} is the median value.

C. Oxide Effects

The aim of this test set was to show a possible contribution of the oxide response to SEGR at high temperature or when the beam incident angle is different from normal. The parts tested were IRF440s from Motorola (lot 9307) and from Harris (lot 9404). The incident ion was Bromine. To decouple the effects of the oxide field from the substrate response, the drain bias V_{DS} was set to 0 *V*. This prevented any contribution from the transient substrate response. The (negative) gate bias was decreased, in 2 *V* steps, until SEGR failure occurred in the device.

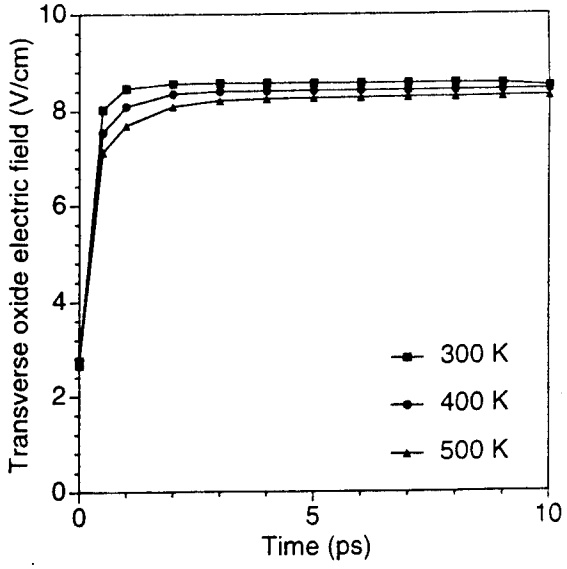


Fig. 5 Maximum simulated transverse electric field in the oxide, as a function of time, for different temperatures. The drain voltage was 30 V; the gate voltage was -13.9 V. The incident ion was Nickel. The maximum electric field in the oxide is slightly lower at higher temperatures.

The results of these tests are shown in Figure 6. The SEGR failure level occurred at about the same gate bias at room temperature and at high temperature, in the case of normal incidence. When the incident angle was different from normal, SEGR took place at a higher magnitude of the gate bias than in normal incidence conditions. These heavy ion results, with and without a substrate contribution to the response, exhibit the same trend for the angular dependence of SEGR. As for the temperature effect on SEGR, no trend could be seen. This suggests that the influence of the ion incident angle on SEGR is determined (at least in part) by the oxide response.

Allenspach et al.[11] derived a relationship between the critical oxide electric field for SEGR and the LET. This relationship can be written in terms of the critical gate voltage for SEGR, V_{Cr}:

$$V_{Cr}(\mathrm{V}) = E_0\,(\mathrm{V/cm}) \times t_{ox}(\mathrm{nm}) / (1 + \mathrm{LET}/53)$$

where $E_0 = 10^7$ V/cm.

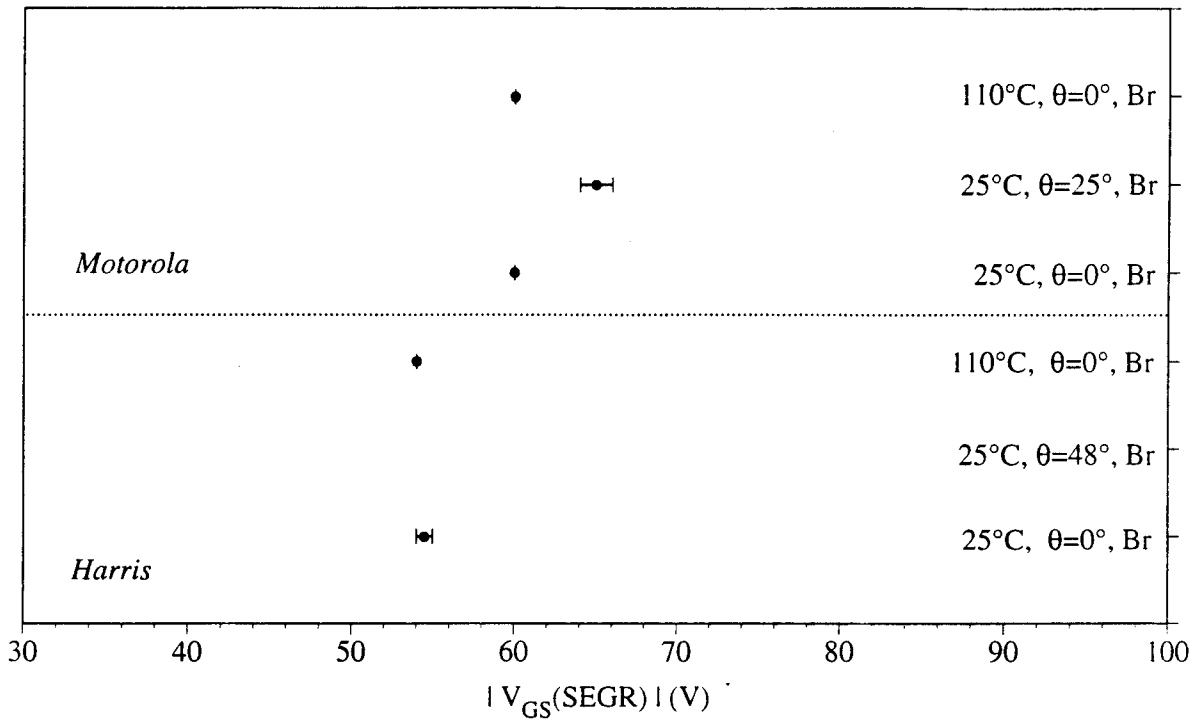


Fig. 6 Experimental gate voltage for SEGR failures when the drain voltage is set to 0 V, for the IRF440s from Motorola and Harris. The bar symbols represent the minimum and maximum value of $|V_{GS}|$ for which SEGR occurred. The filled circle symbols represent the average value of $|V_{GS}|$ for which SEGR occurred. The ion used was Bromine. Three different cases are represented in this figure: normal incidence at room temperature, incident angle different from normal at room temperature, and normal incidence at high temperature. For the Harris part, no failure occurred when the incident angle was 48°.

With Bromine, if we assume the oxide thickness of commercial power MOSFETs to be in the order of 100 nm, the value obtained for V_{Cr} is 60 V. This is comparable to the data we are reporting.

Additional tests were performed to check whether the failures earlier mentioned were actually SEGR events and not dielectric breakdowns due to the gate bias. Gate oxide breakdown experiments were done, with the STAM-MOS test system. The magnitude of the gate bias was increased in 2 V steps, with a 0 V drain bias and in the absence of irradiation. The gate bias for oxide breakdown was between -92 V and -96 V. It is larger than the -50 to -66 V required on the gate to get a rupture when the device was irradiated. This confirms the SEGR nature of the failures that occurred with irradiation.

IV. Conclusion

Heavy ion experiments indicate clearly that track angles far from normal incidence do not favor SEGR. In addition, a weak trend for the influence of temperature on SEGR seems to exist: for the device tested at BNL, a high temperature (90 to 95 °C) would be a slightly better case in terms of preventing SEGR. However, this effect is a second order one. Zero-drain-bias experiments gave the same trends as those observed for nonzero V_{DS}, indicating that both the oxide and substrate response play a major role in determining the SEGR sensitivity.

V. Acknowledgments

The authors would like to acknowledge Jean Garnier and Sophie Duzellier for their help and support for the IPN heavy ion experiments. We would like to thank Ron Pease for his assistance in obtaining experimental samples. Finally, we would like to thank Ron Pease and John Brews for many useful discussions.

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IV. Investigating Total-Dose Effects in Power MOSFETs

IV.A. Introduction

Ionizing radiation results in charge generation in the oxide regions of electronic devices. As part of this task, several total-dose effects in power MOSFETs resulting from ionizing radiation are investigated. One topic that is investigated extensively in this task was mobility degradation due to ionizing radiation. Charge separation techniques are used to show that both interface states and oxide trapped charge contribute to mobility degradation. It is shown that mobility degradation is more pronounced at 77 K than at room temperature.

In addition to mobility degradation, increases in the subthreshold leakage current and $1/f$ noise, and the integrity of the termination structure following total-dose ionizing radiation were investigated. Furthermore, the consequences of extrapolating higher dose-rate, total-dose response, to typical space environment dose-rate response of power MOSFETs is investigated. The effects of cryogenic operation during irradiation in power MOSFETs were also investigated.

The papers describing this work are included in Sections *IV.B* through *IV.N.* A brief overview of each paper is included here to guide the reader through this material.

Section IV.B.: D. Zupac, K.F. Galloway, R.D. Schrimpf, and P. Augier, "Effects of Radiation-Induced Oxide-Trapped Charge on Inversion-Layer Hole Mobility at 300 and 77 K," *Appl. Phys. Lett.*, vol. 60, pp. 3156-3158, 1992.

> This paper presents the effects of radiation-induced interface-trapped charge and oxide-trapped charge on the inversion-layer hole mobility in p-channel power MOSFETs operated at temperatures of 300 K and 77 K. The mobility degradation is more pronounced at 77 K than at 300 K due to an increased importance of Coulomb scattering from trapped charge when phonon scattering is significantly reduced.

Section IV.C.: D. Zupac, K.F. Galloway, P. Khosropour, S.R. Anderson, R.D. Schrimpf, and P. Calvel, "Separation of Effects of Oxide-Trapped Charge and Interface-Trapped Charge on Mobility in Irradiated Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1307-1315, 1993.

> An effective approach to separating the effects of oxide-trapped charge and interface-trapped charge on mobility degradation in irradiated power MOSFETs is demonstrated in this paper. A significant contribution of oxide-trapped charge to mobility degradation is demonstrated and quantified.

Section IV.D.: P. Khosropour, K.F. Galloway, D. Zupac, R.D. Schrimpf, and P. Calvel, "Application of Test Method 1019.4 to Non-Hardened Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 555-560, 1994.

> This paper presents the applicability of MIL-STD-883D Method 1019.4 to predicting the low-dose-rate radiation response of non-hardened power MOSFETs. It is shown that Method 1019.4 works well in providing bounds for the threshold-voltage shift. A modified method is proposed which can yield more information on the threshold-voltage shift at low dose rates for power MOSFETs.

Section IV.E.: D. Zupac, K.F. Galloway, R.D. Schrimpf, and P. Augier, "Radiation-Induced Mobility Degradation in p-Channel Double-Diffused Metal-Oxide-Semiconductor Power Transistors at 300 K and 77 K," *J. Appl. Phys.*, vol. 73, pp. 2910-2915, 1993.

> This paper presents the effects of radiation-induced interface-trapped charge and oxide-trapped charge on the inversion-layer hole mobility in p-channel power MOSFETs operated at temperatures of 300 K and 77 K. The mobility degradation is more pronounced at 77 K than at 300 K due to an increased importance of Coulomb scattering from trapped charge when phonon scattering is significantly reduced.

Section IV.F.: D. Zupac, S.R. Anderson, R.D. Schrimpf, and K.F. Galloway, "Determining the Drain Doping in DMOS Transistors Using the Hump in the Leakage Current," *IEEE Trans. Electron Devices*, vol. 41, pp. 2326-2336, 1994.

> The hump in the leakage current of DMOS power transistors observed for low drain biases is discussed in this paper. The hump is shown to be due to surface generation current of the gate-controlled diode formed by the base-drain p-n junction. The body effect is used to develop a new method for determining the drain doping in DMOS transistors.

Section IV.G.: S.L. Kosier, A. Wei, M.A. Shibib, R.D. Schrimpf, J.C. Desko, and K.F. Galloway, "Comparison of Termination Methods for Low-Voltage, Vertical Integrated Power Devices," *Solid-State Electronics*, vol. 37, pp. 1611-1617, 1994.

> The design issues associated with termination structures for low-voltage, vertical, integrated power devices are described and contrasted with common design guidelines for high-voltage devices. A comparison of single field plate, two-level field plate, field ring, and field plate/field ring methods is presented. It is shown that the field plate/field ring method is superior to the other methods unless extremely low area consumption is required.

Section IV.H.: P. Khosropour, D.M. Fleetwood, K.F. Galloway, R.D. Schrimpf, and P. Calvel, "Evaluation of a Method for Estimating Low-Dose-Rate Irradiation Response of MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2560-2566, 1994.

> In this paper, a simple method for estimating the threshold-voltage shift due to low-dose-rate irradiation is shown. Physical considerations used in the model are explained in the paper. Power MOSFEts from several different technologies are compared with the model.

Section IV.I.: S.R. Anderson, D. Zupac, R.D. Schrimpf, and K.F. Galloway, "The Surface Generation Hump in Irradiated Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2443-2451, 1994.

> This paper presents a method of quantifying near midgap-level interface traps, capture cross section, and changes in oxide-trapped charge in irradiated power MOSFETs. A surface generation hump (that results from the generation of carriers from traps at the depleted Si-SiO2 interface) in the subthreshold current curve is used in the model.

Section IV.J.: S.R. Anderson, R.D. Schrimpf, K.F. Galloway, and J.L. Titus, "Exploration of Heavy Ion Irradiation Effects on Gate Oxide Reliability in Power MOSFETs," *Microelectronics and Reliability*, vol. pp. accepted for publication, 1995.

> This paper investigates the effects of heavy ion irradiation on the gate oxide reliability in power MOSFETs. Time dependent dielectric breakdown measurements and charge separation techniques are used to show that heavy ion exposure does not result in a significant reduction in gate oxide reliability.

Section IV.K.: G.H. Johnson, W.T. Kemp, R.D. Schrimpf, K.F. Galloway, M.R. Ackermann, and R.D. Pugh, "The Effects of Ionizing Radiation on Commercial Power MOSFETs Operated at Cryogenic Temperatures," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2530-2535, 1994.

> This paper reports on the effects of ionizing radiation on n- and p-channel power MOSFETs while operating at cryogenic temperatures. The transistors were exposed to low energy x-rays while placed in a liquid nitrogen-cooled dewar. The results demonstrate significant performance and survivability advantages for space-borne power MOSFETs operated at cryogenic temperatures.

Section IV.L.: P. Augier, J.L. Todsen, D. Zupac, R.D. Schrimpf, K.F. Galloway, and J.A. Babcock, "Comparison of 1/*f* Noise in Irradiated Power MOSFETs Measured in the Linear and Saturation Regions," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 2012-2017, 1992.

> This paper investigates 1/f noise in n-channel and p-channel power MOSFETs as a function of total dose and annealing. All of the devices in this study are non-hardened commercial parts. A difference in evolution of the noise measured in the linear and saturation regions of operation is reported.

Section IV.M.: J.L. Todsen, P. Augier, R.D. Schrimpf, and K.F. Galloway, "1/*f* Noise and Interface Trap Density in High Field Stressed *p*MOS Transistors," *Electronics Lett.*, vol. 29, pp. 696-697, 1993.

> In this paper, experimental results for pMOS transistors subjected to high field stressing is reported. It is shown that 1/f noise and the interface trap density increase with stress time. A direct relationship between the increase in 1/f noise and interface trap density during the high field stressing is observed.

Section IV.N.: M.D. Ploor, R.D. Schrimpf, and K.F. Galloway, "Investigation of Possible Sources of 1/f Noise in Irradiated n-Channel Power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1902-1906, 1994.

> In this paper, 1/f noise in irradiated n-channel power MOSFETs is compared to interface- anc oxide-trapped charge densities. The noise did not correlate well with interface traps or oxide trapped charge. Border traps are investigated as a possible source of the noise.

IV.B. Effects of Radiation-Induced Oxide-Trapped Charge on Inversion-Layer Hole Mobility at 300 and 77 K

Effects of radiation-induced oxide-trapped charge on inversion-layer hole mobility at 300 and 77 K

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The effects of radiation-induced interface-trapped charge and oxide-trapped charge on the inversion-layer hole mobility in *p*-channel double-diffused metal-oxide-semiconductor transistors at 300 and 77 K are reported. The mobility degradation is more pronounced at 77 than at 300 K, due to an increased importance of Coulomb scattering from trapped charge when phonon scattering is significantly reduced. The mobility degradation is primarily due to interface-trapped charge, but the effects of oxide-trapped charge must be taken into account in order to properly describe the mobility behavior, particularly at cryogenic temperatures.

Ionizing-radiation exposure of metal-oxide-semiconductor field-effect transistors (MOSFETs) gives rise to a positive oxide-trapped charge buildup in the silicon dioxide and an increase in interface-trapped charge density at the silicon-silicon dioxide interface. While the threshold voltage of MOSFETs is influenced by both oxide-trapped charge and interface-trapped charge, the inversion-layer mobility is believed to be strongly affected by interface-trapped charge only.[1-3] In this letter, we report on the non-negligible contribution of oxide-trapped charge to mobility degradation in *p*-channel double-diffused metal-oxide-semiconductor (DMOS) transistors exposed to gamma radiation.

The devices used in this study were nonhardened IRF9130 *p*-channel power MOSFETs manufactured by Harris Semiconductor. The irradiations were performed in a Co-60 source. The dose rate was 15 rad(Si)/min. During both the radiation exposure and a subsequent anneal, the gates of the transistors were biased at +9 V, while the sources and drains were grounded. The irradiations and anneals were performed at room temperature, while the electrical characterization was performed at both room temperature and 77 K. Measurements at the two temperatures allow for a comparison between effects of a given density of radiation-induced defects (oxide charge and interface traps) on inversion layer mobility at these two temperatures. The densities of radiation-induced oxide-trapped charge ΔN_{ot} and interface-trapped charge ΔN_{it} were determined using the subthreshold charge separation technique of McWhorter and Winokur.[4] The slope of the $\sqrt{|I_{Dsat}|}$ vs V_G characteristics is proportional to $\sqrt{\mu}$, for small $(V_G - V_T)$, which was used to determine the ratio μ/μ_0, where μ_0 is the preirradiation value of the hole mobility in the channel. $|I_{Dsat}|$ is the magnitude of the drain current in saturation, V_G is the gate voltage, and V_T is the threshold voltage.

The most commonly used empirical expression modeling radiation-induced inversion-layer mobility degradation was introduced by Galloway *et al.*:[1]

$$\frac{\mu}{\mu_0}=\frac{1}{1+\alpha_{it}\Delta N_{it}}, \tag{1}$$

where α_{it} is the parameter describing the effect of interface-trapped charge on mobility. Equation (1) implies that interface-trapped charge is the primary contributor to mobility degradation, while the contribution of oxide-trapped charge is negligible. This model has been successfully applied to describe radiation-induced mobility degradation in both *n*- and *p*-channel integrated-circuit (low-power) MOSFETs,[1,2] as well as in *n*-channel power MOSFETs.[3] In both cases, the negligible effect of oxide-trapped charge was demonstrated by an apparent absence of correlation between (μ/μ_0) and ΔN_{ot}.

Figure 1 illustrates the hole mobility degradation (μ/μ_0) as a function of the radiation-induced interface-trapped charge. The data presented were obtained by irradiating two groups of devices; one group was irradiated up to a total dose of 26 krad(Si), while the second group was irradiated up to 16 krad(Si). The radiation-induced hole mobility degradation is more pronounced at 77 K than at room temperature. (Note that both sets of data are normalized by the corresponding preirradiation values of mobility; the actual mobility is higher at 77 K than at room temperature.) The enhanced mobility degradation at 77 K can be explained by an increased relative importance of Coulomb scattering at cryogenic temperatures when the phonon scattering is significantly reduced. Interface-trapped charge is established as the primary contributor to mobility degradation in these *p*-channel DMOS transistors based on the mobility behavior during anneal. Namely, the interface-trapped charge density increased and the mobility decreased during anneal. On the other hand, the density of oxide-trapped charge decreased during this anneal. Thus, no correlation between (μ/μ_0) and ΔN_{ot} is apparent in these data.

The dominant role of interface-trapped charge in mobility degradation suggests that Eq. (1) may be expected to adequately describe the mobility data presented in Fig. 1. A fitting program STEPIT[5] was used to determine the coefficient α_{it} from Eq. (1) using the irradiation data (closed symbols) presented in Fig. 1. The values obtained for α_{it} were 9.0×10^{-12} cm^2 for room temperature and 15.7×10^{-12} cm^2 for 77 K. The lines shown in Fig. 1 represent

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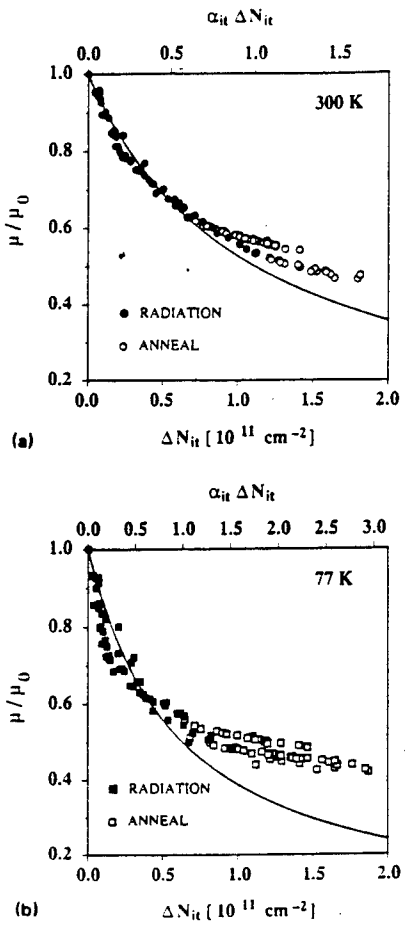


FIG. 1. Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) in p-channel power MOSFETs as a function of interface-trapped charge density: (a) at room temperature, and (b) at 77 K. The curves are the plots of Eq. (1) for $\alpha_{it}=9.0\times10^{-12}$ cm^2 (a) and for $\alpha_{it}=15.7\times10^{-12}$ cm^2 (b). The top x-axis shows the values of the dimensionless product $\alpha_{it}\,\Delta N_{it}$.

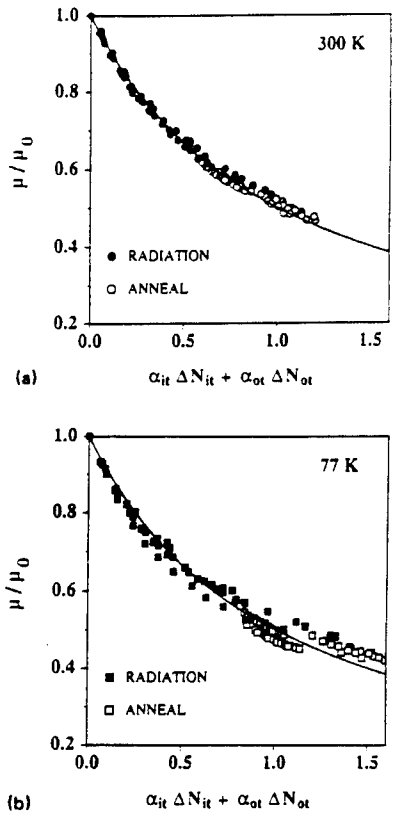


FIG. 2. Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) in p-channel power MOSFETs as a function of the linear combination $\alpha_{it}\,\Delta N_{it}+\alpha_{ot}\,\Delta N_{ot}$: (a) at room temperature, and (b) at 77 K. The curves are the plots of Eq. (2) for $\alpha_{it}=3.9\times10^{-12}$ cm^2 and $\alpha_{ot}=0.7\times10^{-12}$ cm^2 (a), and for $\alpha_{it}=3.4\times10^{-12}$ cm^2 and $\alpha_{ot}=1.3\times10^{-12}$ cm^2 (b).

plots of Eq. (1) for these values of α_{it}. It is obvious that Eq. (1) does not adequately describe the experimental data. The anneal data (open symbols) at both temperatures clearly cannot be modeled using the coefficient values obtained by fitting Eq. (1) to the irradiation data only. Note that using both the irradiation and the anneal data results in different values of coefficients, but the quality of fit does not improve since the data cannot be described by a single hyperbola. The disagreement between the model and the experiment is particularly pronounced for low-temperature mobility data [Fig. 1 (b)].

In order to properly model the mobility data presented in Fig. 1, effects of oxide-trapped charge must be taken into account. Thus, Eq. (1) must be generalized to include a term describing the contribution of oxide-trapped charge to radiation-induced mobility degradation. The approach to modeling mobility when significant densities of both oxide fixed charge and interface traps are present suggested in a classic paper by Sun and Plummer[6] is to use the sum of these two densities in an expression analogous to Eq (1). In the case of radiation-induced oxide-trapped charge and interface-trapped charge, that approach would imply that one and the same coefficient α should be used to describe effects of both ΔN_{ot} and ΔN_{it}, which counters the well-established fact that the interface-trapped charge plays the dominant role in mobility degradation. Thus, we believe that a linear combination of ΔN_{it} and ΔN_{ot} should be used instead of $\alpha_{it}\,\Delta N_{it}$, with the coefficient describing the effect of interface-trapped charge larger than that for oxide-trapped charge. Such an expression has been proposed by Dimitrijev *et al.*:[7,8]

$$\frac{\mu}{\mu_0}=\frac{1}{1+\alpha_{it}\Delta N_{it}+\alpha_{ot}\Delta N_{ot}}. \tag{2}$$

The values of the coefficients α_{it} and α_{ot} can be found by considering (μ/μ_0) as a function of two variables ΔN_{it} and ΔN_{ot}. Data fitting using STEPIT[5] yields $\alpha_{it}=3.9\times10^{-12}$ cm^2 and $\alpha_{ot}=0.7\times10^{-12}$ cm^2 for the 300-K data and $\alpha_{it}=3.4\times10^{-12}$ cm^2 and $\alpha_{ot}=1.3\times10^{-12}$ cm^2 for the 77 K-data. As expected from the previous discussion, α_{it} is larger than α_{ot} at both temperatures. In addition, α_{ot} is larger at 77 K than at room temperature. Figure 2 displays the

normalized mobility as a function of the linear combination of ΔN_{it} and ΔN_{ot}. Comparison between Figs. 1 and 2 clearly demonstrates that it is necessary to account for the effects of oxide-trapped charge in order to properly model the radiation-induced mobility degradation in these devices. Note that the value for α_{ot} found in Refs. 7 and 8 is negative, indicating that an increase in oxide-trapped charge density should lead to an increase in inversion-layer hole mobility. In contrast, the results presented in this letter clearly demonstrate that oxide-trapped charge contributes to a *decrease* in mobility.

Based on the mobility data taken on integrated-circuit MOSFETs irradiated at cryogenic temperatures, the increased contribution of oxide-trapped charge to mobility degradation at low temperatures has been demonstrated by McLean and Boesch[9] in *n*-channel devices, while Saks *et al.* [10] have shown that mobility in *p*-channel devices is degraded even though no interface traps are formed at the low irradiation temperature. These findings are in agreement with the results of this letter, which are obtained by irradiating devices at room temperature, and characterizing mobility degradation at both room temperature and 77 K.

In conclusion, we have investigated the radiation-induced mobility degradation in *p*-channel MOSFETs at room temperature and 77 K. The mobility degradation for given densities of radiation-induced defects is more pronounced at 77 K than at room temperature, due primarily to an increase in the relative importance of Coulomb scattering from the oxide-trapped charge. In accordance with previously published results, interface traps play the dominant role in radiation-induced mobility degradation. However, we have demonstrated that the effects of oxide charges cannot be neglected if the density of oxide-trapped charge is large, which is normally the case in nonhardened MOSFETs. The effects of oxide-trapped charge are shown to be more important at 77 K than at room temperature.

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IV.C. Separation of Effects of Oxide-Trapped Charge and Interface-Trapped Charge on Mobility in Irradiated Power MOSFETs

SEPARATION OF EFFECTS OF OXIDE-TRAPPED CHARGE AND INTERFACE-TRAPPED CHARGE ON MOBILITY IN IRRADIATED POWER MOSFETs†

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Abstract

An effective approach to separating the effects of oxide-trapped charge and interface-trapped charge on mobility degradation in irradiated MOSFETs is demonstrated. It is based on analyzing mobility data sets which have different functional relationships between the radiation-induced oxide-trapped charge and interface-trapped charge. Separation of effects of oxide-trapped charge and interface-trapped charge is possible only if these two trapped charge components are not linearly dependent. A significant contribution of oxide-trapped charge to mobility degradation is demonstrated and quantified.

I. INTRODUCTION

Performance of MOS transistors, especially speed and current drive, is critically dependent on inversion-layer carrier mobility. In ionizing-radiation environments, mobility may degrade sufficiently to cause parametric failure. Mobility degradation is caused by radiation-induced Coulomb scattering centers: interface-trapped charge and oxide-trapped charge.

Understanding of the roles these charges play in mobility degradation is essential for prediction of mobility behavior in ionizing-radiation environments different from those usually achievable in the laboratory. Interface-trapped charge and oxide-trapped charge have different time dependencies of buildup and different anneal properties. As a result, environments with different dose rates and temperatures give rise to different relative amounts of interface-trapped charge and oxide-trapped charge. Therefore, it is necessary to separately quantify the effects of both trapped charge components.

Until recently, radiation-induced mobility degradation at room temperature was attributed almost exclusively to interface-trapped charge [1]-[3]. Notable exceptions are the studies by Wilson and Blue [4], Dimitrijev *et al.* [5], [6], and McLean and Boesch [7]. Wilson and Blue [4] noticed that neither interface-trapped charge alone nor oxide-trapped charge alone could properly account for radiation-induced mobility decrease. They suggested that the sum of interface-trapped charge and oxide-trapped charge be used in mobility modeling. This approach, originally proposed in a classic paper by Sun and Plummer [8], implies that radiation-induced interface-trapped charge and oxide-trapped charge are equally effective in degrading mobility. This is contrary to the findings of numerous studies [1]-[3], [7], [9], [10], which have indisputably established the dominant role of interface-trapped charge. Dimitrijev *et al.* [5], [6] proposed a model which employs a linear combination, rather than the sum, of interface-trapped charge and oxide-trapped charge. This approach is certainly more plausible than using the sum of the two trapped charge components. However, the validity of the model was not directly demonstrated in [5], [6]. Instead, the mobility model was used as the basis for a charge separation technique, which was applied to devices subjected to high-field stress [5], or to ionizing radiation [6]. Finally, McLean and Boesch [7] showed that the effects of oxide-trapped charge are significant at early times ($\leq 10^{-2}$ s) following pulsed irradiation, while at late times ($\geq 10^{3}$ s), the effects of interface-trapped charge are dominant.

In recent studies [9], [10], we have demonstrated and quantified the non-negligible contribution of oxide-trapped charge to mobility degradation in irradiated *p*-channel power MOSFETs *at late times*, corresponding to the usual measurement times and dose rates typical of non-pulsed irradiation. Therefore, the effects of oxide-trapped charge must be explicitly modeled in order to properly describe mobility degradation. The inclusion of the oxide-trapped charge effects in models for radiation-induced mobility degradation requires a procedure for detecting these effects and separating them from the dominant effects of interface-trapped charge.

In this paper, an effective approach to separating the effects of oxide-trapped charge and interface-trapped charge on radiation-induced mobility degradation in MOSFETs is demonstrated. It is based on analyzing mobility data sets having different functional relationships between radiation-induced oxide-trapped charge and interface-trapped charge. In contrast to earlier results [1]-

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[3], significant contribution of oxide-trapped charge to mobility degradation is detected.

In Section II, the functional dependence of mobility degradation on the two trapped charge components is elucidated. Section III describes the experimental procedure used. The results illustrating the relative roles of oxide-trapped charge and interface-trapped charge are presented in Section IV. The universality and applicability of the model are discussed in Section V. Conclusions are drawn in Section VI.

II. Theory

Inversion-layer carrier mobility degradation in MOSFETs is one of the well-established effects of ionizing radiation. While there is a consensus on the dominant role of interface-trapped charge in radiation-induced mobility degradation [1]-[3], the extent of oxide-trapped charge contribution is not well documented. In general, the effect of oxide-trapped charge on mobility has been believed to be negligible, except in special cases where the formation of interface traps is inhibited or delayed (irradiation at cryogenic temperatures [11], and pulsed irradiation [7]). Consequently, oxide-trapped charge is not explicitly included in the most commonly used empirical expression modeling radiation-induced mobility degradation [1]-[3]:

$$\frac{\mu}{\mu_0} = \frac{1}{1 + \alpha \Delta N_{it}} \tag{1}$$

where μ is the effective inversion-layer carrier mobility, μ_0 is the pre-irradiation value of mobility, α is the parameter describing the effect of interface-trapped charge on mobility, and ΔN_{it} is the areal density of radiation-induced interface-trapped charge. This expression has been used to describe radiation-induced mobility degradation in both *n*- and *p*-channel integrated-circuit (low-power) MOSFETs [1], [2], as well as in *n*-channel power MOSFETs [3]. Recently, the non-negligible effect of oxide-trapped charge has been demonstrated in *p*-channel power MOSFETs [9], [10]. The following expression, originally proposed by Dimitrijev *et al.* [5], [6], which explicitly includes the oxide-trapped charge, was successfully applied to model radiation-induced mobility degradation [9], [10]:

$$\frac{\mu}{\mu_0} = \frac{1}{1 + \alpha_{it} \Delta N_{it} + \alpha_{ot} \Delta N_{ot}} \tag{2}$$

where α_{it} and α_{ot} are the coefficients describing the effects of interface-trapped charge and oxide-trapped charge, respectively, and ΔN_{ot} is the areal density of radiation-induced oxide-trapped charge.

Equation 1 describes radiation-induced mobility degradation as a function of one variable, ΔN_{it}, and in Eq. 2 mobility is expressed as a function of two variables, ΔN_{it} and ΔN_{ot}. While plotting the normalized mobility (μ/μ_0) as a function of one variable can easily be accomplished using a two-dimensional graph, Eq. 2 apparently necessitates the use of a three-dimensional graph. Figure 1 is a plot of (μ/μ_0) as a function of ΔN_{it} and ΔN_{ot}. The density of radiation-induced interface-trapped charge ΔN_{it} is plotted along the x-axis, the density of radiation-induced oxide-trapped charge ΔN_{ot} is plotted along the y-axis, and the normalized mobility (μ/μ_0) is plotted along the z-axis. The data plotted in Fig. 1 were obtained by irradiating one device (IRF150 power MOSFET) up to 11.8 krad(Si) at a dose rate of 0.60 rad(Si)/s and then annealing the device at 100°C for 168 hours. The radiation data are shown using closed symbols while the anneal data are represented by open symbols. In addition to the actual data points (triangles), also shown are the projections of the (μ/μ_0) vs. ΔN_{it} and ΔN_{ot} points to the ΔN_{it}–ΔN_{ot} plane (squares) and to the ΔN_{it}–(μ/μ_0) plane (circles). The thin projection lines connect the actual data points with the corresponding projections. The arrow in the ΔN_{it}–ΔN_{ot} plane points from the last radiation point (after 11.8 krad(Si)) to the first anneal point (after 10 hours of anneal). During irradiation, ΔN_{it} and ΔN_{ot} increase and the normalized mobility (μ/μ_0) decreases. During anneal, initially there is a large increase in ΔN_{it}, followed by a slight decrease in ΔN_{it} over the remaining anneal time. ΔN_{ot} decreases monotonically throughout the anneal. The normalized mobility decreases during radiation and during the initial stage of the anneal (when ΔN_{it} increases). During the remaining anneal time mobility increases since both ΔN_{it} and ΔN_{ot} decrease. The heavy line in the ΔN_{it}–(μ/μ_0) plane is the plot of Eq. 1 for $\alpha = 10.6 \times 10^{-12}$ cm^2. This value was obtained by using the radiation data (closed circles) only. This results in a good fit for the radiation data, but the normalized mobility degradation for the anneal data is significantly overestimated.

The three-dimensional plot shown in Fig. 1 is not convenient for illustrating the utility of Eq. 2. It is desirable to devise a procedure which allows plotting the normalized mobility as a function of two variables on a two-dimensional plot in a manner analogous to plotting (μ/μ_0) as a function of ΔN_{it} only. Note that the projection of the measurement data to the ΔN_{it}–(μ/μ_0) plane is traditionally used in conjunction with Eq. 1 [2], [3], because that is a plot of (μ/μ_0) as a function of ΔN_{it} only. Figure 2 shows a plane which can be used for a two-dimensional plot of normalized mobility as a function of the linear combination $\alpha_{it} \Delta N_{it} + \alpha_{ot} \Delta N_{ot}$. In contrast to Fig. 1, the x- and y-axes are dimensionless, and the measurement data are projected to the plane $\alpha_{it} \Delta N_{it} = \alpha_{ot} \Delta N_{ot}$. The heavy line in this plane is the plot of Eq. 2 for $\alpha_{it} = 2.7 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.3 \times 10^{-12}$ cm^2. Clearly, both the radiation data and the anneal data are well described by Eq. 2.

The assessment of the contribution of oxide-trapped charge to mobility degradation becomes possible only if mobility data obtained for different functional relationships between ΔN_{ot} and ΔN_{it} are compared. If the mobility data are characterized by a single, linear ΔN_{ot} vs. ΔN_{it} relationship (which is the case for the radiation data shown in Fig. 1), the use of Eq. 1 may result in a satisfactory fit, with α describing the effects of both trapped

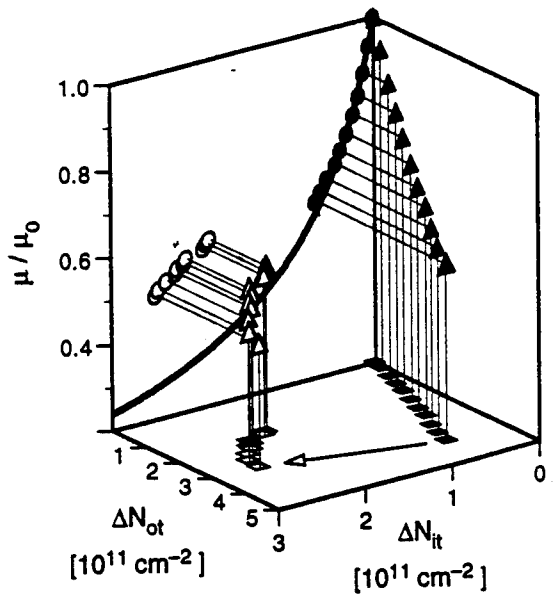


Fig. 1 Normalized mobility during irradiation (closed triangles) and anneal (open triangles) as a function of radiation-induced interface-trapped charge density (ΔN_{it}) and oxide-trapped charge density (ΔN_{ot}). Also shown are the projections of these measurement data points to the ΔN_{it}–ΔN_{ot} plane (squares) and to the ΔN_{it}–(μ/μ_0) plane (circles). The thin projection lines connect the actual data points with the corresponding projections. The arrow in the ΔN_{it}–ΔN_{ot} plane points from the last radiation point to the first anneal point. The heavy line in the ΔN_{it}–(μ/μ_0) plane is the plot of Eq. 1 for $\alpha = 10.6 \times 10^{-12}$ cm^2.

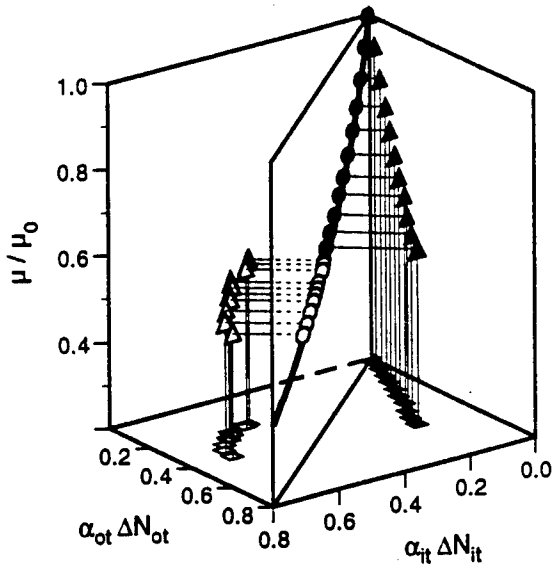


Fig. 2 Normalized mobility during irradiation (closed triangles) and anneal (open triangles) as a function of dimensionless quantities $\alpha_{it}\,\Delta N_{it}$ and $\alpha_{ot}\,\Delta N_{ot}$. Also shown are the projections of these data points to the ($\alpha_{it}\,\Delta N_{it}$)–($\alpha_{ot}\,\Delta N_{ot}$) plane (squares) and to the plane $\alpha_{it}\,\Delta N_{it} = \alpha_{ot}\,\Delta N_{ot}$ (circles). The thin projection lines connect the actual data points with the corresponding projections. The heavy line in the plane $\alpha_{it}\,\Delta N_{it} = \alpha_{ot}\,\Delta N_{ot}$ is the plot of Eq. 2 for $\alpha_{it} = 2.7 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.3 \times 10^{-12}$ cm^2.

charge components, and it may appear that it is not necessary to account for the effects of oxide-trapped charge in modeling radiation-induced mobility degradation. Namely, if

$$\Delta N_{ot} = m\,\Delta N_{it}\,, \tag{3}$$

Eq. 2 becomes

$$\frac{\mu}{\mu_0} = \frac{1}{1+\left(\alpha_{it} + m\,\alpha_{ot}\right)\Delta N_{it}}\,. \tag{4}$$

Comparing Eqs. 2 and 4, we obtain

$$\alpha = \alpha_{it} + m\,\alpha_{ot}\,. \tag{5}$$

Therefore, when there is a linear relationship between ΔN_{ot} and ΔN_{it}, the normalized mobility is no longer a function of two linearly independent variables, and consequently it is not possible to simultaneously obtain values of the two coefficients, α_{it} and α_{ot}. Instead, only one coefficient α given by Eq. 5 may be obtained. Thus, separation of effects of interface-trapped charge and oxide-trapped charge requires that these two trapped charge components be *linearly independent*. Note that the requirements for detection of effects of oxide-trapped charge differ from those for separation. Detection necessitates at least two mobility data sets with *different* (linear or nonlinear) ΔN_{ot} vs. ΔN_{it} relationships. In general, irradiation and anneal result in different ΔN_{ot} vs. ΔN_{it} relationships for a given device type.

III. Experiment

The devices used in this study were non-hardened *n*-channel power DMOS transistors IRF150 manufactured by International Rectifier. A sample of twenty five power MOSFETs were exposed to gamma-radiation in a Co-60 source. Two dose rates were used: five devices were irradiated at a dose rate of 0.60 rad(Si)/s while the dose rate for the remaining twenty devices was 150 rad(Si)/s. The gates of the transistors were biased at + 9 V, while the sources and drains were grounded during both the irradiation and the subsequent anneal. The irradiations were performed at room temperature. Two anneal temperatures were used—room temperature (approximately 23°C) and 100°C. All five devices irradiated at the dose rate of 0.60 rad(Si)/s were annealed at 100°C. Ten devices irradiated at the dose rate of 150 rad(Si)/s were annealed at 100°C, while the remaining ten devices were annealed at room temperature. For the devices irradiated at the lower dose rate (0.60 rad(Si)/s), irradiation was periodically interrupted to perform electrical characterization. For the devices irradiated at the higher dose rate (150 rad(Si)/s), irradiation was not interrupted. As a result, only two "radiation" data points are available for these devices—pre-irradiation (total dose = 0), and post-irradiation (total dose = 11.8 krad(Si)). The electrical characterization was performed at room temperature and it included threshold voltage measurements and subthreshold drain-current measurements. The threshold voltage was defined as the intercept of the extrapolated $\sqrt{I_{D\,sat}}$ vs. V_G plot with the voltage axis, as modeled by the following equation:

$$I_{D\,sat} = \frac{\mu W C_{ox}}{2L}(V_G - V_T)^2 \qquad (6)$$

where $I_{D\,sat}$ is the drain current in saturation, W is the channel width, C_{ox} is the oxide capacitance per unit area, L is the channel length, V_G is the gate voltage, and V_T is the threshold voltage. The slope of the $\sqrt{I_{D\,sat}}$ vs. V_G characteristic is proportional to $\sqrt{\mu}$, for small $(V_G - V_T)$. This was used to determine the ratio μ/μ_0. The subthreshold charge separation technique of McWhorter and Winokur [12] was used to decompose the threshold voltage shift ΔV_T into contributions from oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}). The oxide-trapped charge density (projected to the interface) ΔN_{ot} is defined as $\Delta N_{ot} = |\Delta V_{ot}|\, C_{ox} / q$, where q is the electron charge, and the interface-trapped charge density ΔN_{it} is defined as $\Delta N_{it} = \Delta V_{it}\, C_{ox} / q$.

IV. Results

In this section, the data obtained by using (a) irradiation and anneal, and (b) irradiation followed by anneals at two different temperatures are presented. The data unequivocally illustrate the non-negligible role of oxide-trapped charge in mobility degradation.

A. Radiation and Anneal

Figure 3 illustrates the behavior of one IRF150 power MOSFET irradiated at a dose rate of 0.60 rad(Si)/s. This behavior is typical of all devices irradiated at this dose rate. The device was annealed at 100°C. In non-hardened power MOSFETs irradiated at dose rates used in this study, the density of oxide-trapped charge is considerably larger than the density of interface-trapped charge ($|\Delta V_{ot}| > \Delta V_{it}$). Both $|\Delta V_{ot}|$ and ΔV_{it} (and thus ΔN_{ot} and ΔN_{it}) increase monotonically during radiation (Fig. 3 (a)); consequently, the normalized mobility (μ/μ_0) monotonically decreases during radiation (Fig. 3 (b)). During anneal, the density of interface-trapped charge rapidly increases during the first several hours, and slowly decreases during the remaining anneal time, while the density of oxide-trapped charge monotonically decreases throughout the anneal. The normalized mobility decreases during the initial stage of the anneal (when ΔN_{it} increases). During the remaining anneal time, mobility increases since both ΔN_{it} and ΔN_{ot} decrease. The relationship between ΔN_{ot} and ΔN_{it} resulting from Fig. 3 (a) is shown in Fig. 3 (c). During radiation (closed symbols) there is a linear relationship between ΔN_{ot} and ΔN_{it}, $\Delta N_{ot} = m\,\Delta N_{it}$. During anneal (open symbols) ΔN_{ot} and ΔN_{it} are not linearly dependent. Clearly, radiation and anneal lead to two different functional relationships between ΔN_{ot} and ΔN_{it}.

If the contribution of oxide-trapped charge to radiation-induced mobility degradation is negligible, Eq. 1 is expected to properly describe both mobility data sets, resulting in the same value of the coefficient α. The normalized mobility (μ/μ_0) as a function of the dimensionless product $\alpha\Delta N_{it}$ is displayed in Fig. 4. A fitting

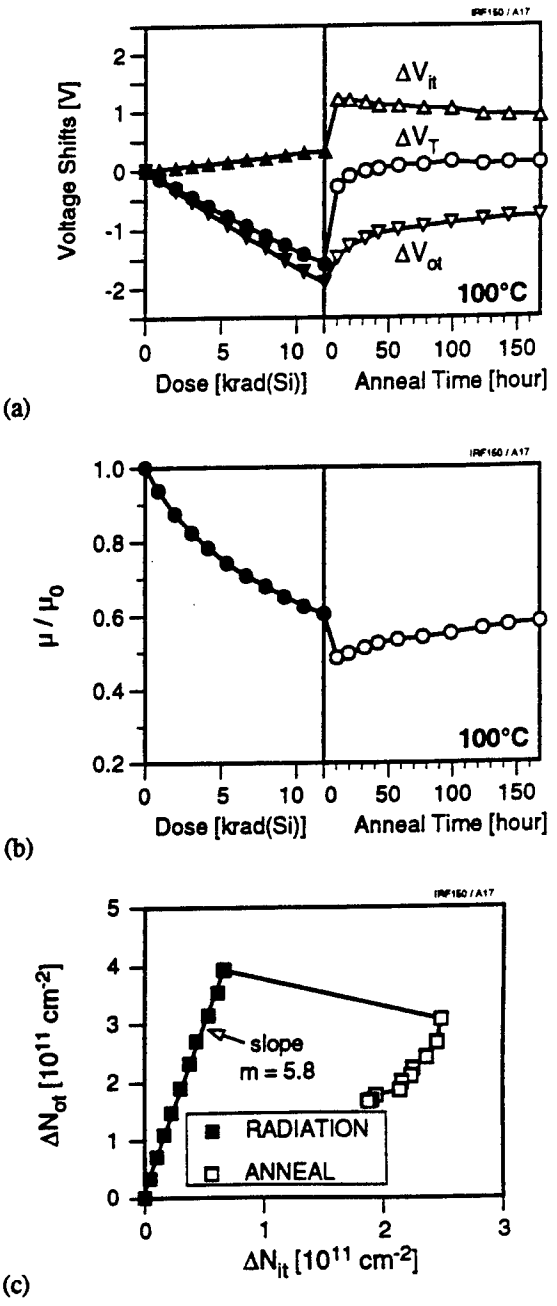


Fig. 3 (a) Radiation-induced threshold voltage shifts (ΔV_T), and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) to these shifts as a function of total dose and anneal time. (b) Normalized mobility as a function of total dose and anneal time. (c) Radiation-induced oxide-trapped charge density (ΔN_{ot}) vs. radiation-induced interface-trapped charge density (ΔN_{it}). The radiation data are represented by closed symbols and the anneal data are represented by open symbols. The irradiation was performed at room temperature (dose rate 0.60 rad(Si)/s), and the anneal was performed at 100°C. The gate bias was positive (V_G = + 9 V) during both the irradiation and the anneal.

program STEPIT [13] was used to determine the coefficient α using: (a) both the radiation and the anneal data, (b) the anneal data only, and (c) the radiation data only. Evidently, when effects of oxide-trapped charge are neglected, the value of the coefficient

α depends on which data set is chosen. In addition, the value obtained when both the radiation and the anneal mobility data are used does not properly describe either data set (Fig. 4 (a)). When only one data set is used, the fit is satisfactory for that data set, but it is very inadequate for the other data set (Fig. 4 (b) and (c)).

The differences in values of α are due to the effects of oxide-trapped charge. The radiation data are characterized by small ΔN_{it} and large ΔN_{ot} ($m = 5.8$ in Fig. 3 (c), which means that the density of oxide-trapped charge is almost six times larger than the density of interface-trapped charge). Small ΔN_{it} and significant mobility degradation observed during radiation exposure result in a large value of the coefficient α (Fig. 4 (c)). On the other hand, the anneal data are characterized by almost equal ΔN_{it} and ΔN_{ot}, which means that the observed mobility degradation can be described by a smaller value of α (Fig. 4 (b)). When both the radiation and the anneal data are used, the fit results in an intermediate value of α (Fig. 4 (a)).

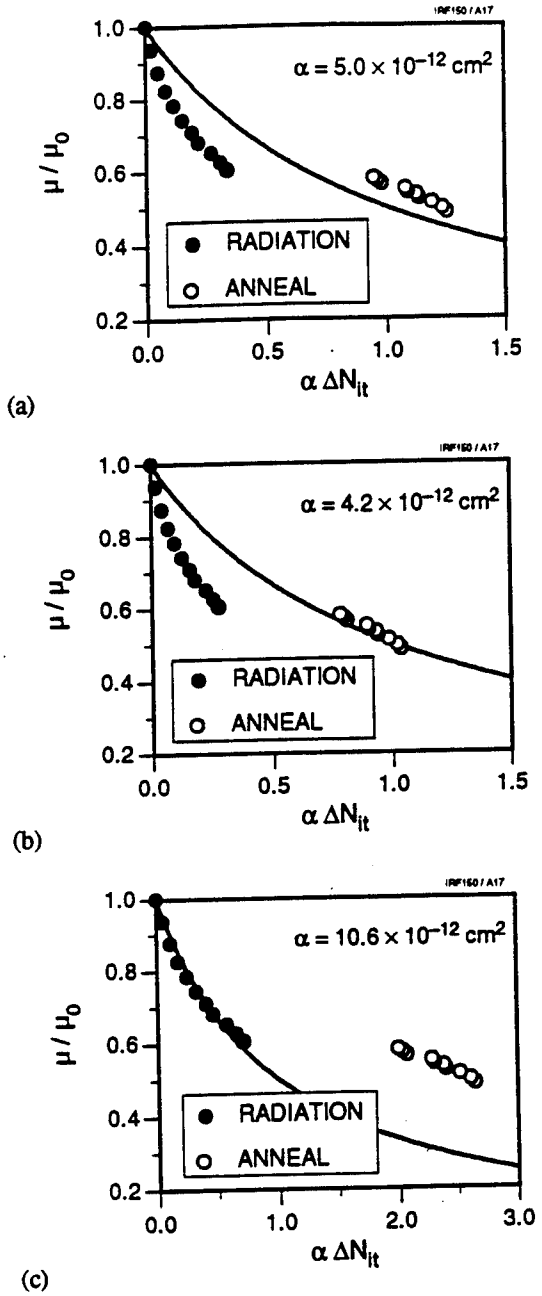


Fig. 4 Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) as a function of the dimensionless product $\alpha \Delta N_{it}$. The curves are the plots of Eq. 1 for α obtained using: (a) both the radiation and the anneal data ($\alpha = 5.0 \times 10^{-12}$ cm^2), (b) the anneal data only ($\alpha = 4.2 \times 10^{-12}$ cm^2), and (c) the radiation data only ($\alpha = 10.6 \times 10^{-12}$ cm^2).

Irrespective of which data set is used in conjunction with Eq. 1, it is not possible to properly model both the radiation and the anneal mobility data with a unique value of α. In contrast, if Eq. 2 (which explicitly includes the effects of oxide-trapped charge) is used, a very good fit is obtained. Figure 5 illustrates radiation-induced normalized mobility degradation as a function of the linear combination $\alpha_{it} \Delta N_{it} + \alpha_{ot} \Delta N_{ot}$. Note that plotting μ/μ_0 as a function of the linear combination $\alpha_{it} \Delta N_{it} + \alpha_{ot} \Delta N_{ot}$ is a convenient way of representing a function of two variables on a

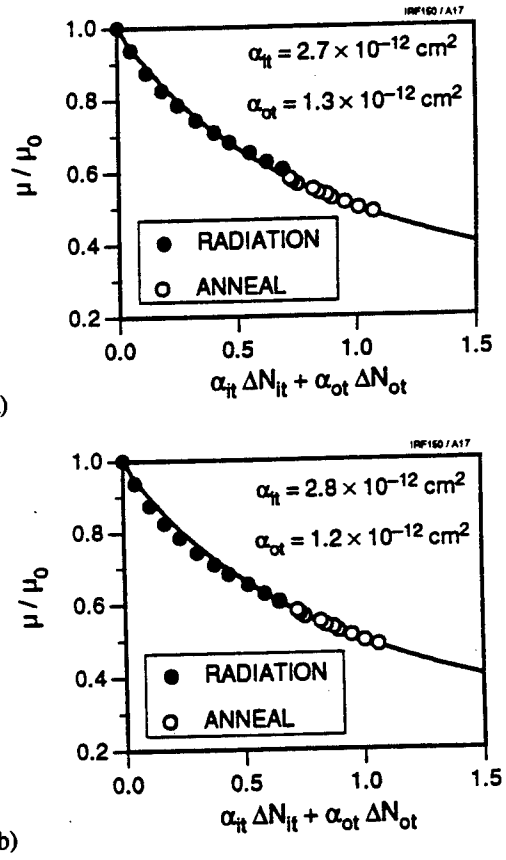


Fig. 5 Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) as a function of the linear combination $\alpha_{it} \Delta N_{it} + \alpha_{ot} \Delta N_{ot}$. The curves are the plots of Eq. 2 for α_{it} and α_{ot} obtained using: (a) both the radiation and the anneal data ($\alpha_{it} = 2.7 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.3 \times 10^{-12}$ cm^2), and (b) the anneal data only ($\alpha_{it} = 2.8 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.2 \times 10^{-12}$ cm^2). For reasons explained in Section II, the radiation data alone cannot be used to determine α_{it} and α_{ot}.

two-dimensional graph. In Fig. 5 (a) both the radiation and the anneal data are used to find the values of α_{it} and α_{ot}, while in Fig. 5 (b) only the anneal data are used to find the values of the two coefficients. In addition to having a good fit in both cases, the values of the coefficients are almost equal. This strongly supports the claim that mobility data sets characterized by different ΔN_{ot} vs. ΔN_{it} relationships cannot be properly modeled if the effects of oxide-trapped charge are neglected. As previously explained in Section II, it is not possible to find the two coefficients if the radiation data only are used, because in that case, the two variables are linearly dependent ($\Delta N_{ot} = m\,\Delta N_{it}$).

It should be noted that the data plotted in Figs. 3-5 describe one and the same device as those shown in Figs. 1-2. In particular, Fig. 3 (c) is the projection of the mobility data ((μ/μ_0) as a function of ΔN_{it} and ΔN_{ot}) to the ΔN_{it}–ΔN_{ot} plane, and Fig. 4 (c) is the projection of the mobility data to the ΔN_{it}–(μ/μ_0) plane (Fig. 1). Similarly, Fig. 5 (a) is the projection of the mobility data ((μ/μ_0) as a function of $\alpha_{it}\Delta N_{it}$ and $\alpha_{ot}\Delta N_{ot}$) to the plane $\alpha_{it}\Delta N_{it} = \alpha_{ot}\Delta N_{ot}$ (Fig. 2).

B. Anneals at Different Temperatures

Figures 6 and 7 illustrate the behavior of two power MOSFETs annealed at different temperatures. One device was annealed at 100°C (Fig. 6), while the other was annealed at room temperature (Fig. 7). The two devices were irradiated at the same dose rate (150 rad(Si)/s). Irradiations were performed in one step, with no interruptions. As a result, only two "radiation" data points are available—pre-irradiation (total dose = 0), and post-irradiation (total dose = 11.8 krad(Si)).

The behavior of the device annealed at 100°C is the same during anneal as that illustrated in Fig. 3 for a device irradiated at the lower dose rate. However, the device annealed at room temperature behaves quite differently. The density of oxide-trapped charge remains essentially unchanged, while the density of interface-trapped charge increases only during the initial stage of the anneal (the first 200 hours) and does not change during the remaining anneal time (Fig. 7 (a)). Consequently, following a decrease during the initial stage of the room-temperature anneal, the normalized mobility does not change over most of the anneal time (Fig. 7 (b)).

Clearly, the anneals at these two temperatures lead to two different functional relationships between ΔN_{ot} and ΔN_{it}, which are shown in Figs. 6 (c) and 7 (c). The corresponding two mobility data sets are, therefore, characterized by relatively low ΔN_{ot} and high ΔN_{it} (100°C-anneal, Fig. 6 (c)), and relatively high ΔN_{ot} and low ΔN_{it} (room-temperature anneal, Fig. 7 (c)).

Once again, if the contribution of oxide-trapped charge to radiation-induced mobility degradation is negligible, Eq. 1 is expected to properly describe both mobility data sets, resulting in the same value of the coefficient α. STEPIT [13] was used to determine the coefficient α using the anneal mobility data only. Normalized mobility (μ/μ_0) as a function of the dimensionless

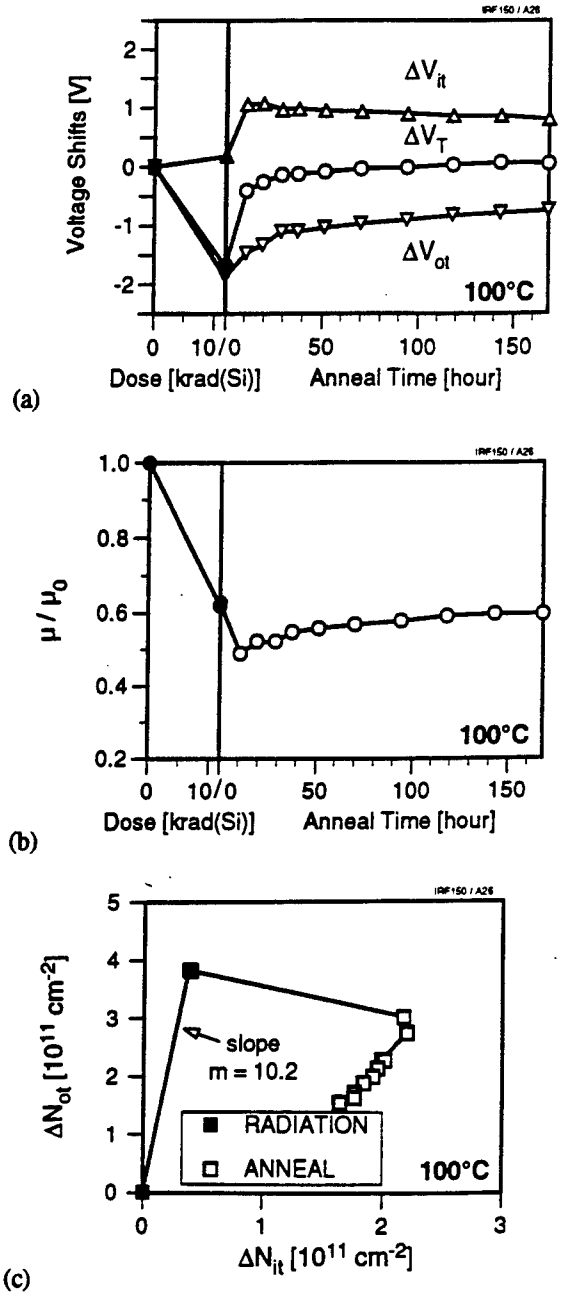
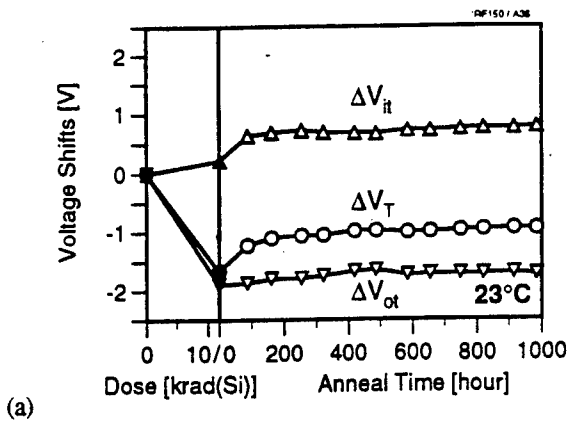
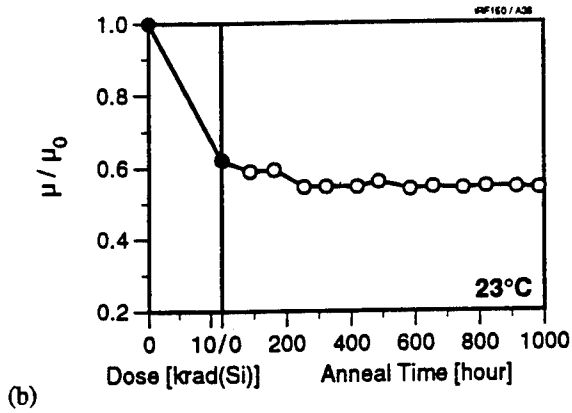


Fig. 6 (a) Radiation-induced threshold voltage shifts (ΔV_T), and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) to these shifts as a function of total dose and anneal time. (b) Normalized mobility as a function of total dose and anneal time. (c) Radiation-induced oxide-trapped charge density (ΔN_{ot}) vs. radiation-induced interface-trapped charge density (ΔN_{it}). The radiation data are represented by closed symbols and the anneal data are represented by open symbols. The irradiation was performed at room temperature (dose rate 150 rad(Si)/s), and the anneal was performed at 100°C. The gate bias was positive (V_G = + 9 V) during both the irradiation and the anneal.

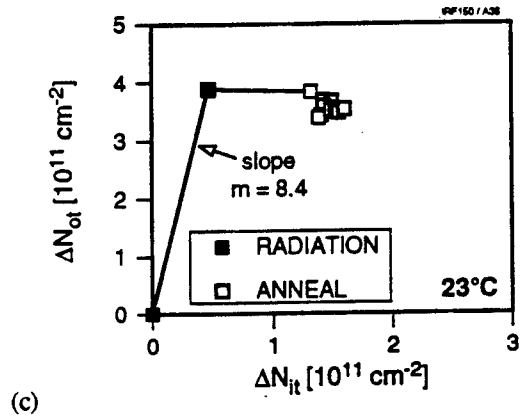
product $\alpha\Delta N_{it}$ is displayed in Fig. 8. The values of α obtained for the two mobility data sets differ by more than 30% and the value obtained for the 23°C-anneal is higher than that obtained for the 100°C-anneal. In addition, the post-irradiation mobility



(a)



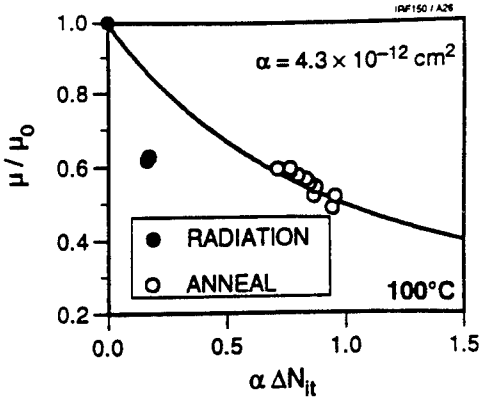
(b)



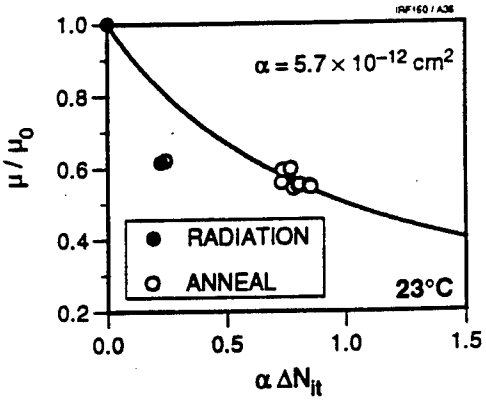
(c)

Fig. 7 (a) Radiation-induced threshold voltage shifts (ΔV_T), and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) to these shifts as a function of total dose and anneal time. (b) Normalized mobility as a function of total dose and anneal time. (c) Radiation-induced oxide-trapped charge density (ΔN_{ot}) vs. radiation-induced interface-trapped charge density (ΔN_{it}). The radiation data are represented by closed symbols and the anneal data are represented by open symbols. Both the irradiation (dose rate 150 rad(Si)/s) and the anneal were performed at room temperature. The gate bias was positive (V_G = + 9 V) during both the irradiation and the anneal.

value is considerably lower than Eq. 1 would predict. Both of these failures of Eq. 1 may be explained by significant effects of ΔN_{ot}. The density of oxide-trapped charge is higher for the 23°C-anneal, and thus a higher value of α is necessary to describe the measured (μ/μ_0). Also, ΔN_{ot} is considerably larger than ΔN_{it}



(a)



(b)

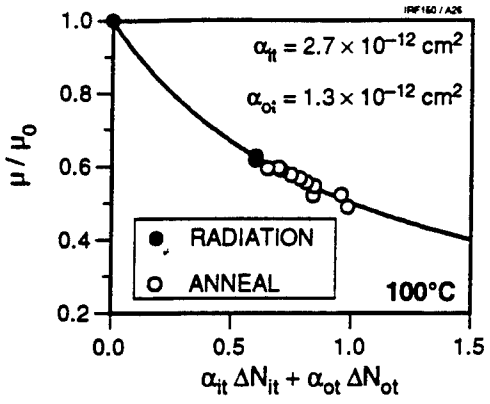
Fig. 8 Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) as a function of the dimensionless product $\alpha \Delta N_{it}$ for: (a) a power MOSFET annealed at 100°C, and (b) a power MOSFET annealed at room temperature. The curves are the plots of Eq. 1 for $\alpha = 4.3 \times 10^{-12}$ cm^2 (a), and for $\alpha = 5.7 \times 10^{-12}$ cm^2 (b).

during irradiation, and thus significant mobility degradation is obtained at relatively low densities of interface-trapped charge. As a result, Eq. 1 with α obtained using the anneal data only (when ΔN_{ot} and ΔN_{it} are comparable) will always underestimate mobility degradation during irradiation.

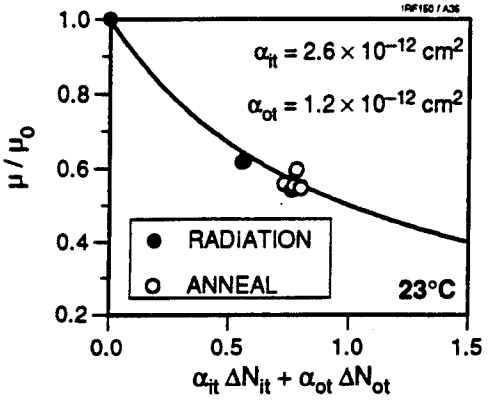
If Eq. 2 is used to model radiation-induced mobility degradation (Fig. 9), the agreement between the values of the coefficients obtained for the two mobility data sets is appreciably improved ($\alpha_{it} = 2.7 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.3 \times 10^{-12}$ cm^2 for the 100°C-anneal, and $\alpha_{it} = 2.6 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.2 \times 10^{-12}$ cm^2 for the 23°C-anneal). In addition, the post-irradiation mobility value (solid circle) is now properly predicted by the model.

V. Discussion of Results

An important issue regarding mobility modeling is whether a particular set of coefficients is valid for just one device or for all devices of a given type. The model in which oxide-trapped charge effects are neglected (Eq. 1) clearly fails to describe even a single device that is subjected to conditions leading to different relationships between ΔN_{ot} and ΔN_{it}. In contrast, the two coefficients from Eq. 2 change very little when different mobility



(a)



(b)

Fig. 9 Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) as a function of the linear combination $\alpha_{it} \Delta N_{it} + \alpha_{ot} \Delta N_{ot}$ for (a) a power MOSFET annealed at 100°C, and (b) a power MOSFET annealed at room temperature. The curves are the plots of Eq. 2 for $\alpha_{it} = 2.7 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.3 \times 10^{-12}$ cm^2 (a), and for $\alpha_{it} = 2.6 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.2 \times 10^{-12}$ cm^2 (b).

data sets are used. In the previous two subsections, the validity of Eq. 2 was demonstrated for the radiation and the anneal data obtained from one device (Fig. 5), and for the anneal data obtained by annealing two irradiated devices at different temperatures (Fig, 9). In Figs. 10 and 11, the data obtained using two different dose rates and two different anneal temperatures are plotted—a total of 217 points per figure representing thirteen devices. Once again, the necessity of including effects of oxide-trapped charge is obvious. The values of the coefficients describing the effect of interface-trapped charge and oxide-trapped charge are $\alpha_{it} = 2.6 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.2 \times 10^{-12}$ cm^2, respectively (Fig. 11).

Physically, it could be argued that the value of the coefficient α_{ot} should be smaller for the anneal data than for the radiation data. It is well known that the location of the oxide-trapped charge is not fixed throughout irradiation and anneal. As the "tunneling front" [14], [15] moves away from the interface into the oxide bulk, the average distance of oxide-trapped charges from the interface increases. Consequently, the ability of oxide-trapped charge to influence the inversion-layer carriers should decrease

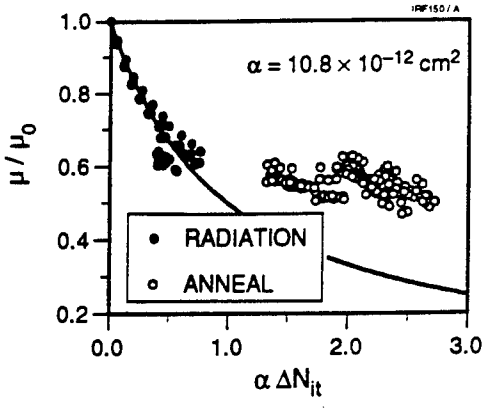


Fig. 10 Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) as a function of the dimensionless product $\alpha \Delta N_{it}$ for IRF150 power MOSFETs used in this study (13 devices, 217 data points; irradiations performed at two different dose rates, anneals performed at two different temperatures). The curve is the plot of Eq. 1 for $\alpha = 10.8 \times 10^{-12}$ cm^2. The radiation data only (closed symbols—71 points) were used to determine α.

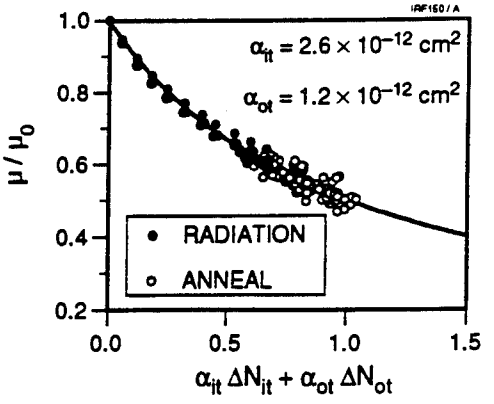


Fig. 11 Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) as a function of the linear combination $\alpha_{it} \Delta N_{it} + \alpha_{ot} \Delta N_{ot}$ for IRF150 power MOSFETs used in this study (13 devices, 217 data points; irradiations performed at two different dose rates, anneals performed at two different temperatures). The curve is the plot of Eq. 2 for $\alpha_{it} = 2.6 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.2 \times 10^{-12}$ cm^2. Both the radiation and the anneal data were used to determine α_{it} and α_{ot}.

and thus α_{ot} should decrease. However, if the tunneling front is assumed to move at a rate of 0.2 nm/decade [7], the tunneling front for the longest anneal times in this study (of the order of 10^6 s) is less than 1 nm away from its position when measurements "during irradiation" (solid symbols in all the figures) are performed (10^2–10^3 s after irradiation was interrupted). Therefore, the average distance of oxide-trapped charges from the interface is not appreciably different for the radiation data and the anneal data. This explains why the differences between the coefficient values obtained using different data sets (see Figs. 5 and 9) are very small. Consequently, the model given by Eq. 2 is capable

of properly describing both the radiation and the anneal data with the same set of coefficients.

The fact that the "tunneling front" does not move far from the interface allows the oxide-trapped charge density projected to the interface, ΔN_{ot}, to be used instead of the time-dependent $\Delta N_{ot}(t)$ used by McLean and Boesch [7]. The time-dependent $\Delta N_{ot}(t)$ is the areal density of holes remaining at time t at the distance $x_m(t)$ from the interface, where $x_m(t)$ is the time-dependent position of the tunneling front [7]. Assuming a relatively large $x_m(t) = 4$ nm, corresponding to long anneal times (of the order of 10^6 s), the difference between the two oxide-trapped charge densities for typical gate-oxide thicknesses in power MOSFETs is only about 4%. This is certainly less than the uncertainties in the values of the coefficients α_{ot} (in units cm^2) from this study and α_{ot} (in units cm^3) from [7], and significantly less than the uncertainties associated with the room-temperature value of $x_m(t)$. Therefore, Eq. 2 may be expected to work well in describing radiation-induced mobility degradation at late times for all MOSFETs except for those which have very thin gate oxides.

The experiments described in Section III have also been performed for IRF250 power MOSFETs manufactured by International Rectifier. Similar coefficient values are obtained: $\alpha_{it} = 2.2 \times 10^{-12}$ cm^2 and $\alpha_{ot} = 1.4 \times 10^{-12}$ cm^2.

Finally, note that it is not surprising that the addition of the second coefficient to the equation modeling radiation-induced mobility degradation leads to a better fit. However, the value of Eq. 2 is in its physical justification.

VI. Conclusions

A significant contribution of oxide-trapped charge to radiation-induced mobility degradation has been demonstrated. This result advances and improves understanding of the effects of interface-trapped charge and oxide-trapped charge on mobility and supersedes the earlier work [1]-[3]. The effects of oxide-trapped charge must be taken into account in order to properly describe mobility degradation when large densities of radiation-induced oxide-trapped charge are present. A systematic approach to detecting effects of oxide-trapped charge and separating them from the effects of interface-trapped charge is illustrated. Detection of oxide-trapped charge effects requires that mobility data sets having different functional relationships between ΔN_{ot} and ΔN_{it} be analyzed simultaneously. In this study, different relationships between ΔN_{ot} and ΔN_{it} for devices of the same type were obtained by using irradiation and anneal. Separation of oxide-trapped charge effects from those of interface-trapped charge necessitates that ΔN_{ot} and ΔN_{it} be linearly independent. These results are particularly important for mobility modeling in non-hardened devices in which ionizing radiation leads to large densities of oxide-trapped charge.

VII. Acknowledgments

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IV.D. Application of Test Method 1019.4 to Non-Hardened Power MOSFETs

Application of Test Method 1019.4 to Non-Hardened Power MOSFETs‡

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Abstract

The applicability of MIL-STD-883D Method 1019.4 to predicting the low-dose-rate radiation response of non-hardened power MOSFETs has been investigated. Method 1019.4 works well in providing bounds for the threshold-voltage shift. However, it is not intended to provide an estimate of the actual ΔV_T due to low-dose-rate irradiation. A modified method is proposed which can yield more information on the threshold-voltage shift at low dose rates for power MOSFETs.

I. Introduction

The electrical characteristics of power MOSFETs make them of interest for use in space systems [1]. Power MOSFETs, in general, have higher switching speeds than their power bipolar transistor counterparts [2]. Power MOSFETs also have a negative temperature coefficient of carrier mobility which reduces the potential for thermal runaway, second breakdown, and power hogging in parallel devices when compared to bipolar transistors [2]. In addition, power MOSFETs have simpler input drive requirements than bipolar transistors [3].

Space applications of power MOS devices require knowledge of the behavior of these devices when exposed to low-dose-rate ionizing radiation typical of natural space. There has been considerable work on the effects of ionizing radiation on MOS devices and a number of reviews are available [4-6]. Most work characterizing the effects of ionizing radiation on MOS devices has been done at the high dose rates normally available for laboratory experimentation. However, several researchers have focused on hardness assurance methodology applicable to the space environment [7-11].

Since low-dose-rate testing at dose rates typical of natural space is relatively time-consuming and expensive, an expeditious test procedure for microcircuits is described in MIL-STD-883D, Method 1019.4. Strictly speaking, Test Method 1019.4 has only been incorporated into MIL-STD-883D. Power MOSFETs, as discrete devices, are governed by MIL-STD-750C. Test Method 1019.4, appropriately modified for discrete devices, has not yet been incorporated in MIL-STD-750C. The main sequence for Method 1019.4 consists of a high-dose-rate (50-300 rad(Si)/s) irradiation followed by an elevated temperature anneal (168 hours at 100°C) [12]. The purpose of the anneal is to accelerate the time-dependent effects that are significant in determining the low-dose-rate radiation response of MOS devices. Fleetwood et al. [13], Barnes et al. [14], and Sexton et al. [15] have discussed the evolution of Method 1019 so that it is applicable to hardness assurance for devices intended for space systems. The main sequence of Method 1019.4 is further described in Appendix A.

This paper discusses the application of Test Method 1019.4 to non-hardened power MOSFETs. Data taken at a low dose rate approaching the natural space environment are compared directly with high-dose-rate data followed by high temperature annealing. Method 1019.4 is found to be extremely useful in providing bounds for the threshold-voltage shift. However, it is not intended to provide an estimate of the actual ΔV_T due to low-dose-rate irradiation. A modification to this method is proposed which can more accurately estimate the threshold-voltage shift at low dose rates for the commercial power MOSFETs used in this study.

II. Experimental Details

The device types used in this study were IRF150 and IRF250 power MOSFETs manufactured by International Rectifier. The devices came from the same wafer lot (6U1G for IRF150 and 0B3L for IRF250). The gates were biased at +9 V, while the sources and drains of all devices were grounded during both irradiation and anneal. The radiation exposure was performed at two different dose rates in a Co-60 source. One group of devices was irradiated at a high dose rate (HDR, 150 rad(Si)/s), and annealed in accordance with Test Method 1019.4. The second group was irradiated at a low dose rate (LDR, 3.6×10^{-4} rad(Si)/s). Irradiations were performed at room temperature. The total dose for both radiation exposures was 11.8 krad(Si). For devices

‡ Work supported in part by ALCATEL ESPACE under contract 393.550.986.

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exposed at a high dose rate, one group was annealed at 100°C for 168 hours, while the second group was annealed at room temperature for a period of 1 year.

Method 1019.4 specifies that after irradiation and completion of electrical characterization devices must be irradiated to an additional dose equal to 0.5-times the specified dose. The purpose of this test is to identify failures caused by a rebound of electrical characteristics to a value greater than the pre-irradiation value. However, extensive characterization of these parts indicates that threshold-voltage rebound does not occur. Figure 1 shows that there is no rebound in ΔV_T due to increase in the density of interface-traps during 100°C anneal. Therefore, this element has been eliminated on the basis of characterization testing, as permitted by Method 1019.4 [12].

Standard transistor threshold voltage and subthreshold current-voltage measurements were performed at room temperature using a HP4145B semiconductor parameter analyzer. The threshold voltage is defined as the voltage-axis intercept of the square root of the drain current versus gate voltage in saturation. The threshold-voltage shift due to oxide-trapped charge, ΔV_{ot}, and that due to interface-trapped charge, ΔV_{it}, were determined using the subthreshold charge separation technique of McWhorter and Winokur [16].

III. Results

Three different experiments were performed: a) High Dose Rate (HDR) irradiation followed by anneal at 100°C (10 IRF150's and 10 IRF250's); b) High Dose Rate (HDR) irradiation followed by room temperature anneal (10 IRF150's and 10 IRF250's); and c) Low Dose Rate (LDR) irradiation (15 IRF150's and 15 IRF250's). The data displayed for each experiment are the average of all devices tested. Standard deviations are typically too small to be visible on the plots.

A. HDR + 100°C Anneal

Figure 1 shows the threshold-voltage shift and contributions of oxide-trapped charge and interface-trapped charge during irradiation and during anneal. The high temperature anneal was at 100°C for 168 hours. During irradiation, the density of oxide-trapped charge is much larger than the density of interface-trapped charge. The high temperature anneal initially causes a significant increase in the density of interface-trapped charge. This interface-trapped charge decreases slightly during the rest of the anneal time. A decrease in ΔV_{it} at 100°C does not necessarily imply a decrease in the density of interface traps. The subthreshold charge separation technique [16] involves subthreshold current measurements which are relatively slow. This means that oxide traps located very close to the silicon-silicon dioxide interface can exchange charge with the silicon on the time scale of the measurements (several seconds). Traps which are located in the oxide, and behave electrically as "switchable states" have recently been termed "border traps" [17], [18]. These border traps cannot be resolved from the actual interface

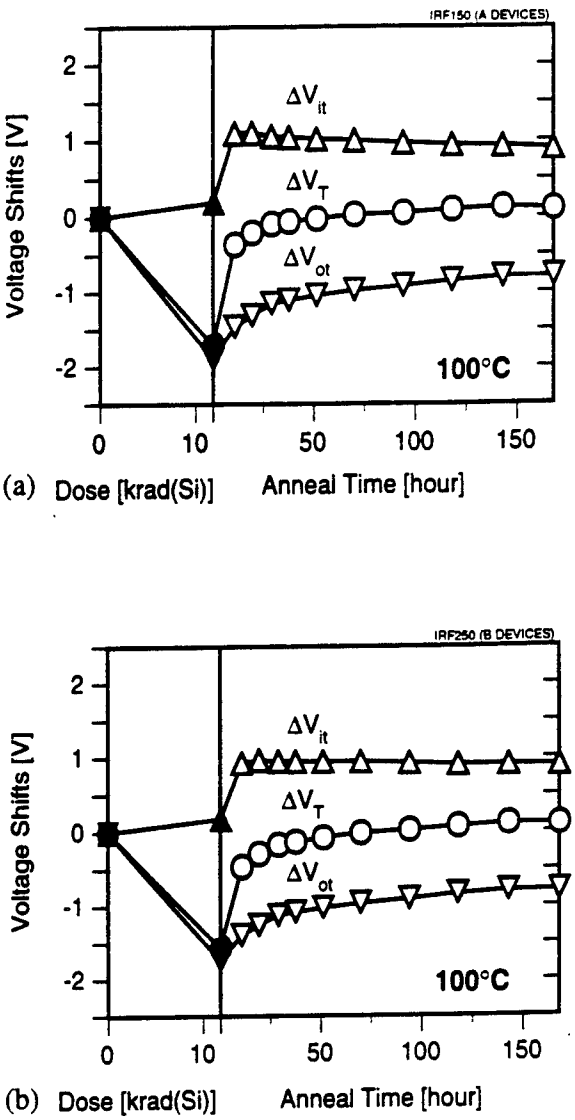


Fig. 1. Radiation-induced threshold-voltage shifts (ΔV_T), and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) to the threshold-voltage shifts during high-dose-rate irradiation (closed symbols) and 100°C-anneal (open symbols) for (a) IRF150, and (b) IRF250.

traps (located at the silicon-silicon dioxide interface) using the subthreshold charge separation technique. As a result, a decrease in the density of border traps during anneal cannot be distinguished from a decrease in ΔV_{it} using the subthreshold technique, if the density of actual interface traps does not change. The contribution of border traps to the total ΔV_{it} in these devices is estimated to be approximately 25%, assuming that the density of actual interface traps does not change during the last 150 hours of the 100°C-anneal. The density of the oxide-trapped charge decreases monotonically during the entire anneal time.

The maximum negative threshold-voltage shift occurs immediately after irradiation, when the oxide-trapped charge is at its

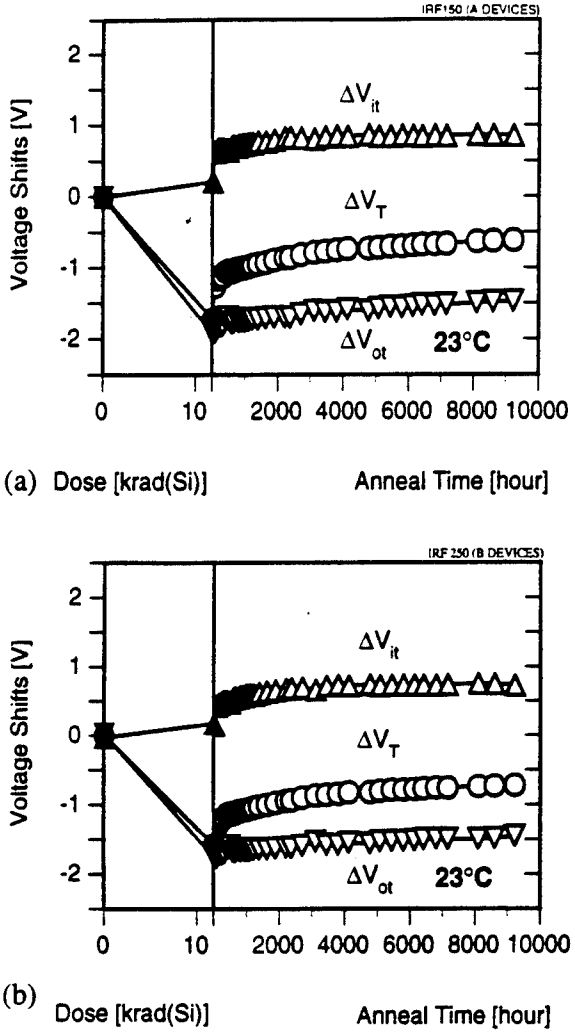


Fig. 2. Radiation-induced threshold-voltage shifts (ΔV_T), and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) to the threshold-voltage shifts during irradiation (closed symbols) at high dose rate and anneal at room temperature (open symbols) for (a) IRF150, and (b) IRF250.

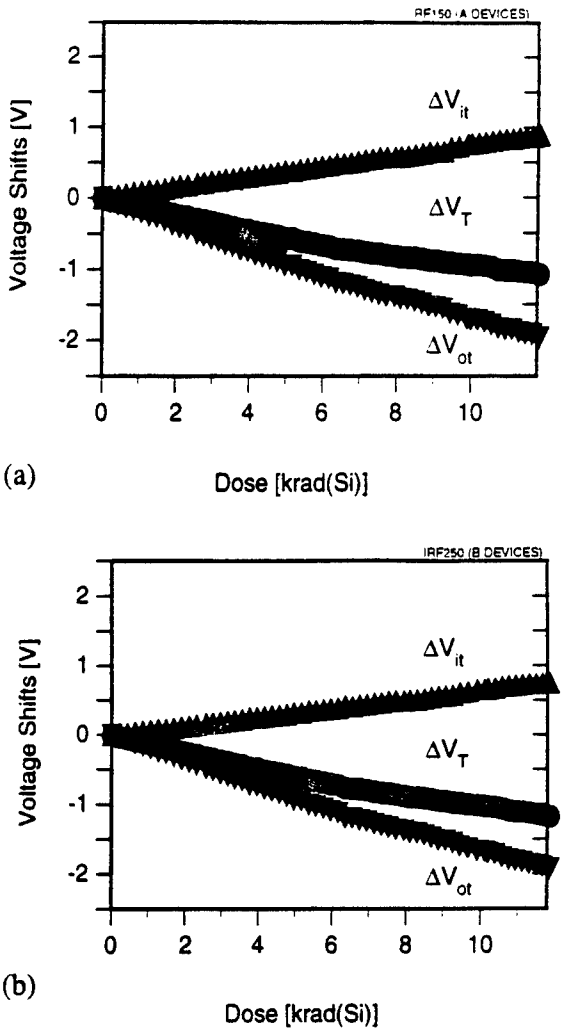


Fig. 3. Threshold-voltage shifts (ΔV_T) and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) to these shifts for power MOSFETs irradiated at a low dose rate for (a) IRF150, and (b) IRF250.

maximum and the interface-trapped charge buildup is not complete. At low dose rates, the failure mechanism may be an increase in the threshold voltage due to interface-trapped charge. The maximum positive threshold-voltage shift occurs if the oxide charge is completely removed by annealing and the interface trap formation is complete. This is estimated by measuring ΔV_{it} after annealing at 100°C to accelerate the formation of the interface-trapped charge. The actual low-dose-rate threshold-voltage shift will lie between these two bounds.

B. HDR + Room Temperature Anneal

Figure 2 shows the threshold-voltage shifts for devices irradiated at the high-dose-rate and annealed at room temperature. Again, during irradiation, the density of the oxide-trapped charge is larger than the density of interface-trapped charge. The interface-trapped charge density increases very slowly during the anneal time, while the oxide-trapped charge density essentially remains constant during the room temperature anneal.

C. LDR

Figure 3 shows the threshold-voltage shift and contributions of oxide-trapped charge and interface-trapped charge for ionizing radiation exposure at a dose rate of 3.6×10^{-4} rad(Si)/s up to the total dose of 11.8 krad(Si). The density of interface-trapped charge and the density of oxide-trapped charge increase monotonically.

IV. Discussion

By comparing Figs. 1 and 3, it is observed that the density of interface-trapped charge following HDR irradiation and high-temperature anneal is approximately the same as the density of interface-trapped charge following LDR irradiation. Therefore,

high-dose-rate irradiation followed by high temperature anneal predicts the build-up of interface-trapped charge due to low-dose-rate irradiation in this experiment. The magnitude of the oxide-trapped charge is significantly smaller after the high temperature anneal (Fig. 1) than after the low-dose-rate irradiation exposure (Fig. 3).

Figure 4 shows the threshold-voltage shifts for IRF150 devices due to interface-trapped charge (ΔV_{it}) and oxide-trapped charge (ΔV_{ot}) as a function of irradiation time plus anneal time at 100°C and at room temperature. This method is commonly used to show that irradiation and anneal data for interface-trapped charge or oxide-trapped charge fall on the same curve, independent of the dose rate at which the damage was introduced [19]. Figure 4 also shows the measured ΔV_{ot} and ΔV_{it} at 11.8 krad(Si) due to low-dose-rate irradiation. In Fig. 4 (a), it is observed that ΔV_{it} at the end of 11.8 krad(Si) for the low-dose-rate exposure falls very near the high-dose-rate exposure plus room temperature anneal curve. Furthermore, high-dose-rate irradiation followed by 100°C-anneal conservatively predicts the amount of shift due to interface-trapped charge. In Fig. 4 (b) the magnitude of ΔV_{ot} for the low-dose-rate exposure is the same as the magnitude of ΔV_{ot} for high-dose-rate irradiation followed by room temperature anneal. High-dose-rate irradiation followed by anneal at 100°C does not provide an estimate for ΔV_{ot}. This has been shown earlier for CMOS devices [20].

The threshold-voltage shift for IRF150's for the low-dose-rate irradiation at the total dose of 11.8 krad(Si) is -1.078 ± 0.04 V with ΔV_{ot} = -1.971 ± 0.06 V and ΔV_{it} = 0.893 ± 0.04 V. For the high-dose-rate irradiation, the threshold-voltage shift at the same total dose was -1.66 ± 0.08 V with ΔV_{ot} = -1.90 ± 0.10 V and ΔV_{it} = 0.24 ± 0.02 V.

The behavior of these power MOSFETs differs from that of typical integrated-circuit MOSFETs in that there is very little annealing of oxide trapped charge at room temperature. This is illustrated clearly in Fig. 2.

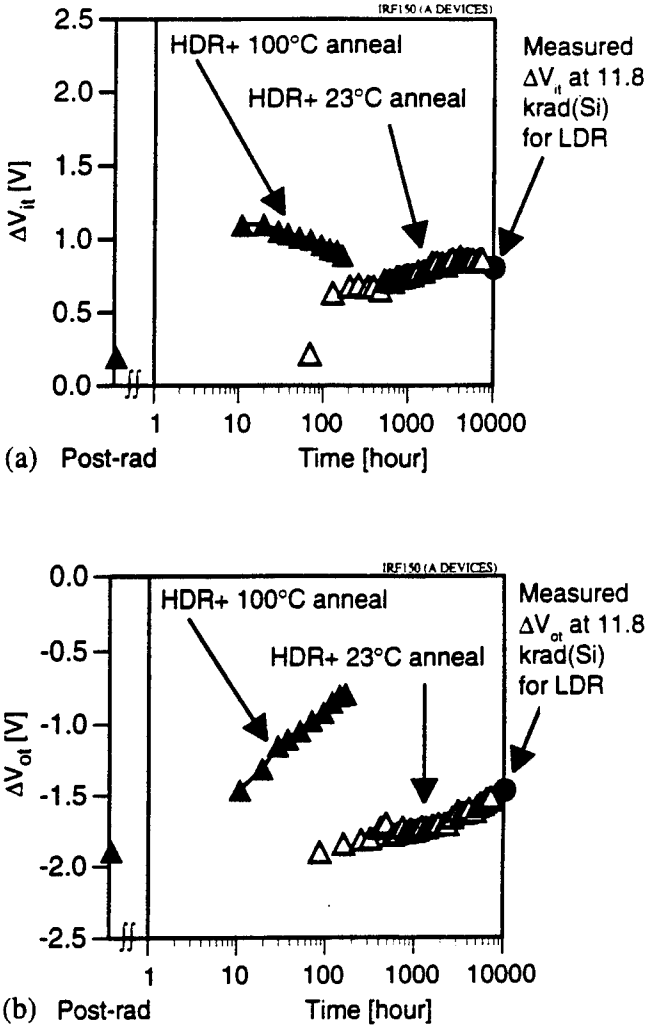


Fig. 4. (a) ΔV_{it} and (b) ΔV_{ot} as a function of irradiation time plus anneal time for IRF150 at room temperature (open triangles), and 100°C (closed triangles). Closed circle shows the measured (a) ΔV_{it} and (b) ΔV_{ot} at the total dose of 11.8 krad(Si) for low-dose-rate irradiation.

V. Proposed New Method

The high-dose-rate irradiation provides conservative bounds for the threshold-voltage shift, ΔV_T, for the low-dose-rate irradiation. However, the magnitude of the threshold-voltage shift is not accurately predicted by either high-dose-rate irradiation nor the ensuing high-temperature anneal. In these devices (as well as other commercial power MOSFETs that were tested), no rebound is observed; the failure mechanism is reduction of the threshold voltage due to oxide-trapped charge. Method 1019.4 provides a bound for this effect, but Figs. 1 and 3 illustrate that the actual threshold-voltage shift at low dose rates is significantly less than this bound. This may lead to rejection of parts that will function well in a space environment. It is important to obtain an estimate of the true low-dose-rate threshold-voltage shift to effectively select parts for space applications.

The high-temperature anneal following the high-dose-rate irradiation provides a good estimate for ΔV_{it} resulting from the low-dose-rate irradiation. Similarly, a good estimate for ΔV_{ot} may be obtained from the high-dose-rate irradiation. This suggests that a good estimate for the threshold-voltage shift resulting from the low-dose-rate irradiation can be obtained by combining ΔV_{ot} at the end of high-dose-rate irradiation and ΔV_{it} at the end of high-temperature anneal.

Method 1019.4 provides bounds for the radiation-induced threshold-voltage shift. The maximum possible negative shift occurs when the oxide charge is at its maximum and interface traps are minimized. Conversely, the maximum possible positive shift occurs when the oxide charge is entirely removed and the interface-trap density is maximized. In the power MOSFETs examined here, the annealing of the oxide charge is negligible at

room temperature; thus, the improvement of the device response at low dose rates depends on the negatively-charged interface-trapped charge to balance the positive oxide charge. The actual threshold-voltage shift at low dose rates can be estimated by using the arithmetic sum of ΔV_{ot} obtained immediately after irradiation and ΔV_{it} obtained following the high-temperature anneal.

Through this modification, the threshold-voltage shift due to low-dose-rate ionizing radiation exposure can be estimated. For example, using ΔV_{it} = 0.89 V at the end of high-temperature anneal and ΔV_{ot} = -1.90 V at the end of high-dose-rate irradiation, the threshold-voltage shift can be calculated as ΔV_T = -1.90 V+ 0.89 V = -1.01 V. The actual threshold-voltage shift at the end of low-dose-rate irradiation exposure is -1.078 V (Fig. 3). The difference between the actual threshold-voltage shift and the estimate obtained using the proposed new method is 6.3%. The above analysis was for IRF150 devices; IRF250 devices exhibit the same behavior.

VI. Conclusions

The application of Test Method 1019.4 to non-hardened power MOSFETs has been examined experimentally. The results would support incorporation of a similar methodology in MIL-STD-750C for discrete power MOSFETs. The results presented suggest that, even though 1019.4 is a very effective technique for bounding ΔV_T, an alternative method can provide more information than Method 1019.4 in estimating actual threshold-voltage shifts for non-hardened power MOSFETs in low-dose-rate environments.

Since oxide-trapped charge annealing is negligible during low-dose-rate irradiation, a simple prediction method is proposed. It combines ΔV_{ot} at the end of the high-dose-rate irradiation with ΔV_{it} at the end of the 100°C-anneal. By adding these two values, the threshold-voltage shift of power MOSFETs in a low-dose-rate radiation environment can be estimated. Additional testing is required to determine the applicability of this method to other device types and technologies.

VII. Acknowledgments

The authors would like to thank Prof. Jean Gasiot of the Université Montpellier II; Mr. Stuart Litwin of International Rectifier; Prof. Keith Holbert of Arizona State University; Prof. John Williams, Mr. Harry Doane, and Mr. Vernon Hull of the University of Arizona; and Mr. Michael Krzesniak of the Naval Surface Warfare Center for contributions to this work. The authors would also like to thank Dr. Dan Fleetwood and Dr. Peter Winokur of Sandia National Laboratories for critically reading the manuscript.

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APPENDIX A

Several researchers [13-15] have discussed modifications of Method 1019.4 for hardness assurance in space environments. This test method is only intended as a pass/fail method. However, the procedure does provide an estimate of a worst-case response at low dose rates, if the devices exhibit significant rebound effects. The main test sequence for Method 1019.4 is:

a) Irradiate devices in a Co-60 source under worst-case bias condition to the specified dose at a dose rate of 50-300 rad(Si)/s.

b) Remove bias. Maintain zero bias between irradiation and test.

c) Complete functional and parametric test within 2 hours after irradiation.

d) If the devices pass all tests in (c), irradiate the devices again under the conditions of (a) to an additional dose equal to 0.5-times the specified dose. This step may be omitted if the devices do not show significant rebound characteristics.

e) Bake the devices at worst-case static bias for 168 ± 12 hours at 100°C ± 5°C, or under conditions that have been demonstrated in characterization tests to cause equal or greater degradation in the parameter(s) of interest (e.g. speed, timing, and/or output drive).

f) Repeat the test of (c).

IV.E. Radiation-Induced Mobility Degradation in p-Channel Double-Diffused Metal-Oxide-Semiconductor Power Transistors at 300 K and 77 K

Radiation-induced mobility degradation in *p*-channel double-diffused metal-oxide-semiconductor power transistors at 300 and 77 K

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The effects of radiation-induced interface-trapped charge and oxide-trapped charge on the inversion-layer hole mobility in *p*-channel double-diffused metal-oxide-semiconductor power transistors at 300 and 77 K are investigated. The mobility degradation is more pronounced at 77 K than at 300 K, due to increased importance of Coulomb scattering from trapped charge when phonon scattering is significantly reduced. The mobility degradation is primarily due to interface-trapped charge, but the effects of oxide-trapped charge must be taken into account in order to properly describe the mobility behavior, particularly at cryogenic temperatures.

I. INTRODUCTION

Modeling of carrier mobility in inversion layers of metal-oxide-semiconductor field-effect transistors (MOSFETs) is important for simulating device performance under normal operating conditions, as well as under stress. Most of the research efforts aimed at understanding the mechanisms determining the inversion layer (channel) mobility have been directed either toward modeling its dependence on the surface electric field or toward elucidating the mobility degradation due to interfacial charges (oxide-trapped charge and interface-trapped charge).

Significant improvements of the on resistance, thermal conductance, switching speed, and switching efficiency of power MOSFETs at low temperatures have recently been reported.[1] The beneficial effects of cryogenic operation are due largely to increased mobility at low temperatures. This article investigates the effects of ionizing-radiation-induced interfacial charges on the channel carrier mobility in *p*-channel double-diffused metal-oxide-semiconductor (DMOS) power transistors at room temperature and at 77 K. Preliminary results were presented at the Radiation and its Effects on Devices and Systems (RADECS)'91 conference[2] and the effects of the oxide-trapped charge were discussed in letter format.[3] This article provides a more complete exposition of the experimental results and the resulting analysis.

II. EXPERIMENT

The devices used in this study were nonhardened IRF9130 *p*-channel power MOSFETs manufactured by Harris Semiconductor. The irradiations were performed in a Co-60 source. The dose rate was 15 rad(Si)/min. The gates of the transistors were biased at +9 V during both the radiation exposure and a subsequent anneal. The sources and drains were grounded throughout the irradiation and anneal. The irradiation and anneal were performed at room temperature, while the electrical characterization was performed at both room temperature and 77 K. Measurements at the two temperatures allow for a comparison between effects of a given density of radiation-induced defects (oxide charge and interface traps) on inversion layer mobility at these two temperatures. The electrical characterization included threshold voltage measurements and subthreshold drain-current measurements. The threshold voltage was defined as the intercept of the extrapolated $\sqrt{|I_{D\,\mathrm{sat}}|}$ vs V_G plot with the voltage axis, as modeled by the following equation:

$$|I_{D\,\mathrm{sat}}| = \frac{\mu W C_{\mathrm{ox}}}{2L}(V_G - V_T)^2, \tag{1}$$

where $|I_{D\,\mathrm{sat}}|$ is the magnitude of the drain current in saturation, μ is the effective hole mobility in the channel, W is the channel width, C_{ox} is the oxide capacitance per unit area, L is the channel length, V_G is the gate voltage, and V_T is the threshold voltage. The slope of the $\sqrt{|I_{D\,\mathrm{sat}}|}$ vs V_G characteristic is proportional to $\sqrt{\mu}$, for small $(V_G - V_T)$. This slope was used to determine the ratio μ/μ_0, where μ_0 is the preirradiation value of the hole mobility in the channel.

III. MOBILITY DEGRADATION AT 300 AND 77 K

Figure 1 illustrates the behavior of a DMOS transistor representative of the devices used in this study during irradiation (closed symbols) and anneal (open symbols). Figure 1(a) shows the radiation-induced threshold voltage shifts at room temperature, as well as the contributions of the oxide charge (ΔV_{ot}) and charged interface traps (ΔV_{it}) to the threshold voltage shifts. The gate bias was positive ($V_G = +9$ V) during both irradiation and anneal. In *p*-channel MOSFETs, both the oxide-trapped charge and the charged interface traps are positive, which gives rise to negative threshold voltage shifts ($\Delta V_T = \Delta V_{\mathrm{ot}} + \Delta V_{\mathrm{it}}$). Note that the density of radiation-induced oxide-trapped charge was considerably larger than the density of radiation-induced interface-trapped charge ($|\Delta V_{\mathrm{ot}}| > |\Delta V_{\mathrm{it}}|$). During irradiation, $|\Delta V_{\mathrm{ot}}|$, $|\Delta V_{\mathrm{it}}|$, and $|\Delta V_T|$ increase approximately in a linear fashion with total dose. Therefore, there is an approximately linear relationship between the density of oxide-trapped charge ΔN_{ot} (defined as $\Delta N_{\mathrm{ot}} = |\Delta V_{\mathrm{ot}}| C_{\mathrm{ox}}/q$, where $q = 1.6 \times 10^{-19}$ C is the electron charge) and the density of

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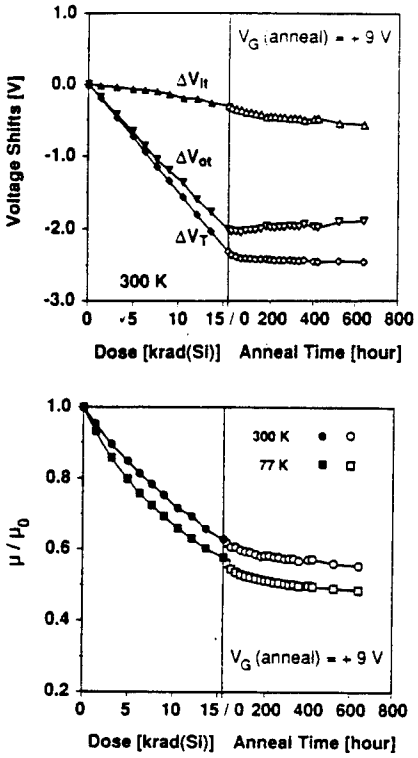


FIG. 1. (a) Radiation-induced threshold voltage shifts (ΔV_T), and contributions of oxide charges (ΔV_{ot}) and interface traps (ΔV_{it}) to the threshold voltage shifts, and (b) normalized mobility during irradiation (closed symbols) and anneal (open symbols). The mobilities are normalized by the corresponding preirradiation values. The gate bias was positive ($V_G = +9$ V) during both irradiation and anneal.

interface-trapped charge ΔN_{it} (defined as $\Delta N_{it} = |\Delta V_{it}| C_{ox}/q$) during irradiation. (Note that ΔN_{ot} is not a spatial charge density, but an effective oxide-trapped charge density—projected to the interface—in units cm^{-2}.) During the anneal, the density of oxide-trapped charge decreases, while the density of interface-trapped charge increases.

The subthreshold charge separation technique proposed by McWhorter and Winokur[4] was used to determine ΔV_{ot} and ΔV_{it}. Note that this charge separation technique was used for room-temperature data only. The nonlinearities of the subthreshold characteristic observed at 77 K adversely affect the reliability of this technique at cryogenic temperatures. In order to determine the densities of oxide-trapped charge ΔN_{ot} and interface-trapped charge ΔN_{it} at 77 K, we assumed that the contribution of the oxide charge (ΔV_{ot}) to the threshold voltage shift is the same at room temperature and at 77 K. The contribution of charged interface traps (ΔV_{it}) at 77 K was then determined by subtracting the room-temperature ΔV_{ot} from ΔV_T measured at 77 K.

Figure 1(b) illustrates the radiation-induced normalized mobility degradation at room temperature and at 77 K. The mobilities are normalized by the corresponding preirradiation values at either temperature [300 K mobility is normalized by μ_0 (300 K), and 77 K mobility is normalized by μ_0 (77 K)]. Obviously, the hole mobility de-

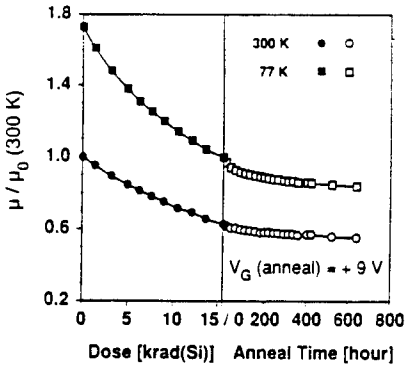


FIG. 2. Normalized mobilities at 300 and 77 K during irradiation (closed symbols) and anneal (open symbols). The mobilities were normalized by the preirradiation value at 300 K.

creases with increasing dose at both temperatures and it continues to decrease during anneal. Note, however, that mobility at 77 K degrades more than the room-temperature mobility. This enhanced mobility degradation at 77 K can be explained by a reduction in phonon scattering at that temperature, which makes the low-temperature mobility very sensitive to Coulomb scattering from ionized impurity atoms in the channel and from interfacial charges introduced by radiation. Therefore, the relative importance of scattering from interfacial charges is larger at 77 K, which results in more serious mobility degradation than at room temperature.

It should be noted that the mobility at 77 K remains higher than the mobility at 300 K, even after ionizing-radiation exposure. This is illustrated in Fig. 2, where the data from Fig. 1(b) are replotted using the preirradiation room-temperature mobility μ_0 (300 K) as the normalization constant. The preirradiation mobility at 77 K is 72% higher than the preirradiation mobility at room temperature. Due to more pronounced mobility degradation at 77 K, that difference is about 59% at the dose of 16 krad(Si), and is further reduced to 52% after 640 h of positive gate-bias anneal.

In order to understand the experimentally observed enhanced mobility degradation at 77 K, the temperature dependences of different scattering mechanisms need to be considered. The mobility μ may, in accordance with Matthiessen's rule, be expressed as

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{1}{\mu_{IC}}, \tag{2}$$

where μ_{IC} is the mobility limited by the Coulomb scattering from the interfacial charges introduced by ionizing radiation. This mobility is inversely proportional to the effective interfacial charge density, which is, in a general case, a linear combination of the oxide-trapped charge and interface-trapped charge. The preirradiation mobility may be written as

$$\frac{1}{\mu_0} = \frac{1}{\mu_{II}} + \frac{1}{\mu_L}, \tag{3}$$

where μ_{II} and μ_L are the ionized-impurity-scattering-limited mobility and phonon (lattice)-scattering-limited mobility, respectively. [The effective mobility in the saturation region is measured at low $(V_G - V_T)$, which results in low effective transverse electric fields, so that surface roughness scattering can be neglected.] Multiplying Eq. (2) by μ_0 results in

$$\frac{\mu_0}{\mu} = 1 + \frac{\mu_0}{\mu_{IC}}. \tag{4}$$

Thus, the extent of mobility degradation at a given temperature for a given density of radiation-induced interfacial charges depends on the value of the second term on the right-hand side of Eq. (4); the larger the μ_0/μ_{IC}, the larger the mobility degradation will be. The preirradiation mobility at 77 K is larger than the preirradiation mobility at 300 K [μ_0 (77 K) $> \mu_0$ (300 K)], because the phonon scattering is significantly reduced at 77 K, resulting in large μ_L and, according to Eq. (3), large μ_0 (77 K). This point is clearly illustrated in Fig. 2. In addition, the mobility limited by Coulomb scattering from the (radiation-induced) interfacial charges is proportional to a positive power of the temperature.[5] This means that μ_{IC} (77 K) $< \mu_{IC}$ (300 K). Therefore,

$$\frac{\mu_0(77\text{ K})}{\mu_{IC}(77\text{ K})} > \frac{\mu_0(300\text{ K})}{\mu_{IC}(300\text{ K})}. \tag{5}$$

According to Eqs. (4) and (5), the relative mobility degradation is expected to be more pronounced at 77 K, which is in agreement with the experimental results presented in Figs. 1 and 2.

IV. MODELING RADIATION-INDUCED MOBILITY DEGRADATION

The most commonly used empirical expression modeling radiation-induced inversion-layer mobility degradation was provided by Galloway *et al.*[6] based on a modification of the expression introduced by Sun and Plummer:[7]

$$\frac{\mu}{\mu_0} = \frac{1}{1 + \alpha_{it}\Delta N_{it}}, \tag{6}$$

where α_{it} is the parameter describing the effect of interface-trapped charge on mobility. Equation (6) implies that interface-trapped charge is the primary contributor to mobility degradation, while the contribution of oxide-trapped charge is negligible. This model has been successfully applied to describe radiation-induced mobility degradation in both *n*- and *p*-channel integrated-circuit (low-power) MOSFETs,[6,8] as well as in *n*-channel power MOSFETs.[9] In all cases, the negligible effect of oxide-trapped charge was demonstrated by an apparent absence of correlation between (μ/μ_0) and ΔN_{ot}.

The data presented in Fig. 1 indicate that interface-trapped charge plays a dominant role in radiation-induced mobility degradation in the *p*-channel DMOS transistors used in this study. Namely, the interface-trapped charge density increases and the mobility decreases during anneal. On the other hand, the density of oxide-trapped charge

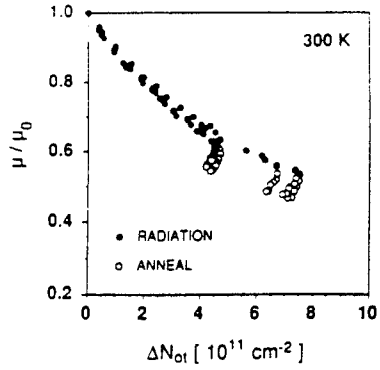


FIG. 3. Radiation-induced mobility degradation as a function of oxide-trapped charge density at 300 K during irradiation (closed symbols) and anneal (open symbols). The gate bias was positive ($V_G = +9$ V) during both irradiation and anneal.

decreases during this anneal. Thus, no correlation between (μ/μ_0) and ΔN_{ot} is apparent in these data. This is further illustrated in Figs. 3 and 4. The data presented were obtained by irradiating two groups of devices; one group

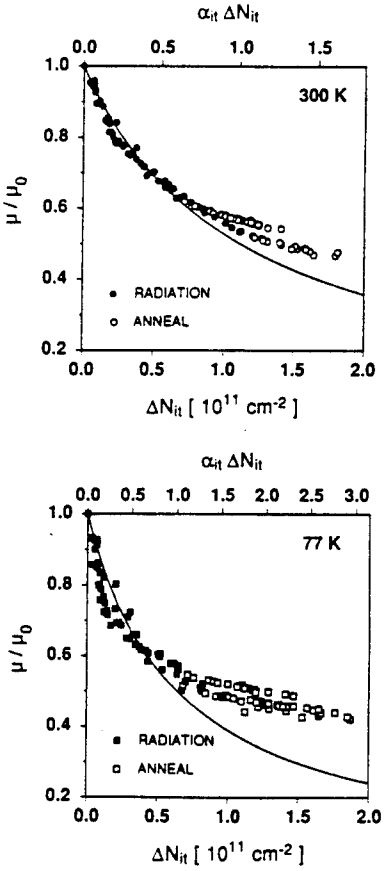


FIG. 4. Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) in *p*-channel power MOSFETs as a function of interface-trapped charge density: (a) at room temperature, and (b) at 77 K. The curves are the plots of Eq. (6) for $\alpha_{it} = 9.0 \times 10^{-12}$ cm^2 [(a)], and for $\alpha_{it} = 15.7 \times 10^{-12}$ cm^2 [(b)]. The top *x* axis shows the values of the dimensionless product $\alpha_{it}\Delta N_{it}$.

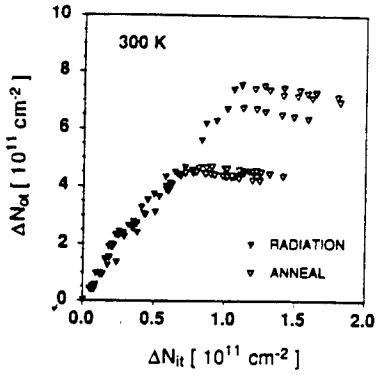


FIG. 5. Radiation-induced oxide-trapped charge density (ΔN_{ot}) vs radiation-induced interface-trapped charge density (ΔN_{it}).

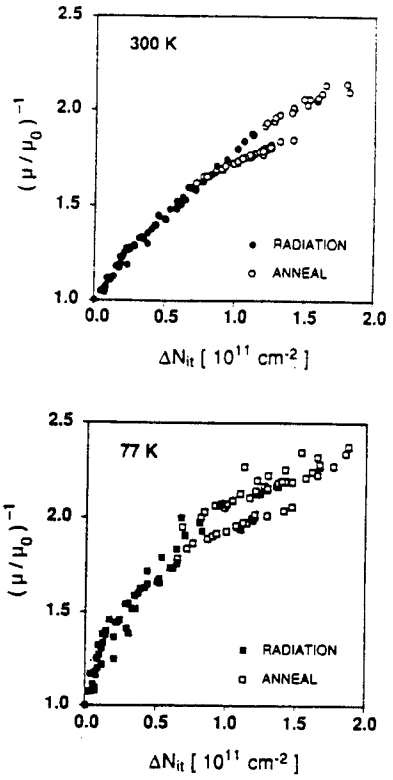


FIG. 6. The reciprocal of the normalized mobility as a function of radiation-induced interface-trapped charge density ΔN_{it} (a) at room temperature, and (b) at 77 K.

(four devices) was irradiated up to a total dose of 16 krad(Si), while the second group (three devices) was irradiated up to 26 krad(Si). The gate bias was positive ($V_G=+9$ V) during both irradiation and anneal. Figure 3 displays the hole mobility degradation (μ/μ_0) at 300 K as a function of the radiation-induced oxide-trapped charge density ΔN_{ot}. A comparison with Fig. 4(a), which illustrates the hole mobility degradation (μ/μ_0) at 300 K as a function of the radiation-induced interface-trapped charge ΔN_{it}, clearly demonstrates the dominant role of interface-trapped charge in radiation-induced mobility degradation. Note, however, that this may be established only by examining both radiation and anneal data. The dominant role of interface-trapped charge is not apparent if only the irradiation data are considered. As mentioned in Sec. III, there is an approximately linear relationship between the density of oxide-trapped charge ΔN_{ot} and the density of interface-trapped charge ΔN_{it} during irradiation, which is shown in Fig. 5. Thus, an expression analogous to Eq. (6) could conceivably be used to describe the radiation-induced mobility degradation as a function of oxide-trapped charge density ΔN_{ot}. During anneal, a different functional relationship between ΔN_{ot} and ΔN_{it} exists, which allows interface-trapped charge to be identified as the primary contributor to mobility degradation.

The dominant role of interface-trapped charge in mobility degradation suggests that Eq. (6) may be expected to adequately describe the mobility data presented in Fig. 4. A fitting program STEPIT[10] was used to determine the coefficient α_{it} from Eq. (6) using the irradiation data (closed symbols) presented in Fig. 4. The values obtained for α_{it} were 9.0×10^{-12} cm^2 for room temperature and 15.7×10^{-12} cm^2 for 77 K. The lines shown on Fig. 4 represent plots of Eq. (6) for these values of α_{it}. It is obvious that Eq. (6) does not adequately describe the experimental data. The anneal data (open symbols) at both temperatures clearly cannot be modeled using the coefficient values obtained by fitting Eq. (6) to the irradiation data only. Note that using both the irradiation and the anneal data results in different values of coefficients, but the quality of fit does not improve since the data cannot be described by a single hyperbola. The disagreement between the model and the experiment is particularly pronounced for low-temperature mobility data [Fig. 4(b)].

The reasons for the inadequacy of Eq. (6) may be better understood if the data presented in Fig. 4 are plotted as the reciprocal of the normalized mobility $(\mu/\mu_0)^{-1}$ vs ΔN_{it} (Fig. 6). Equation (6) predicts a linear dependence of $(\mu/\mu_0)^{-1}$ on ΔN_{it}. Also, based on Eq. (6) we have

$$\alpha_{it}=\frac{d}{d(\Delta N_{it})}\left[\left(\frac{\mu}{\mu_0}\right)^{-1}\right]. \tag{7}$$

A well-defined linear dependence is indeed observed for $\Delta N_{it}\geq 2\times10^{10}$ cm^{-2} [room-temperature irradiation data—closed symbols in Fig. 6(a)], but in contrast to Eq. (6), the y-axis intercept of such a line is larger than unity. Consequently, the slope of the $(\mu/\mu_0)^{-1}$ vs ΔN_{it} characteristic is larger at low interface-trapped charge densities (for $\Delta N_{it}\leq 2\times10^{10}$ cm^{-2}) than at higher densities, which according to Eq. (7) indicates that α_{it} is larger at low interface-trapped charge densities. As shown below, this can be explained by a significant contribution of oxide-trapped charge to mobility degradation during the initial slow buildup of interface traps. This initial slow buildup of interface traps is also apparent in Fig. 5 for $\Delta N_{it}\leq 2\times10^{10}$ cm^{-2}. An even larger y-axis intercept is obtained for low-temperature data [Fig. 6(b)], which indicates that the contribution of oxide-trapped charge to radiation-induced mobility degradation is more pronounced at 77 K than at room temperature.

The increased contribution of oxide-trapped charge to radiation-induced mobility degradation at cryogenic temperatures can also be inferred from the data presented in Fig. 1. The density of oxide trapped charge slightly increases (i.e., $|\Delta V_{ot}|$ increases) during the first several tens of hours of room-temperature anneal, and then monotonically decreases for the rest of the anneal time. This small increase in the oxide-trapped charge results in a large low-temperature mobility degradation, and only a moderate decrease in room-temperature mobility during the first 100 h of anneal.

V. CONTRIBUTION OF OXIDE-TRAPPED CHARGE TO MOBILITY DEGRADATION

In order to properly model the mobility data presented in Fig. 4, the effects of oxide-trapped charge must be taken into account. Thus, Eq. (6) must be generalized to include a term describing the contribution of oxide-trapped charge to radiation-induced mobility degradation. The approach to modeling mobility when significant densities of both oxide fixed charge and interface traps are present, suggested in a classic paper by Sun and Plummer,[7] is to use the sum of these two densities in an expression analogous to Eq. (6). In the case of radiation-induced oxide-trapped charge and interface-trapped charge, that approach would imply that the same coefficient α should be used to describe the effects of both ΔN_{ot} and ΔN_{it}, which counters the well-established fact that the interface-trapped charge plays the dominant role in mobility degradation. Thus, we believe that a linear combination of ΔN_{it} and ΔN_{ot} should be used instead of $\alpha_{it}\Delta N_{it}$, with the coefficient describing the effect of interface-trapped charge larger than that for oxide-trapped charge. Such an expression has been proposed by Dimitrijev *et al.*:[11,12]

$$\frac{\mu}{\mu_0}=\frac{1}{1+\alpha_{it}\Delta N_{it}+\alpha_{ot}\Delta N_{ot}}. \tag{8}$$

The values of the coefficients α_{it} and α_{ot} can be found by considering (μ/μ_0) as a function of two variables ΔN_{it} and ΔN_{ot}. Data fitting using STEPIT[10] yields $\alpha_{it}=3.9\times10^{-12}$ cm^2 and $\alpha_{ot}=0.7\times10^{-12}$ cm^2 for the 300 K data and $\alpha_{it}=3.4\times10^{-12}$ cm^2 and $\alpha_{ot}=1.3\times10^{-12}$ cm^2 for the 77 K data. As expected from the previous discussion, α_{it} is larger than α_{ot} at both temperatures. In addition, α_{ot} is larger at 77 K than at room temperature. Figure 7 displays the normalized mobility as a function of the linear combination of ΔN_{it} and ΔN_{ot}. Comparison between Figs. 4 and 7 clearly demonstrates that it is necessary to account for the effects of oxide-trapped charge in order to properly model the radiation-induced mobility degradation in these devices. Note that the value for α_{ot} found in Refs. 11 and 12 is negative, indicating that an increase in oxide-trapped charge density should lead to an increase in inversion-layer hole mobility. In contrast, the results presented in this article clearly demonstrate that oxide-trapped charge contributes to a *decrease* in mobility in these devices.

Finally, it should be noted that, while the dominant role of interface traps in radiation-induced mobility degradation is widely recognized, other researchers have noted the effects of oxide-trapped charge. In particular, McLean and Boesch[13] have shown that at early times following pulsed radiation, the effect of oxide-trapped charge may be dominant. In addition, based on the mobility data taken on integrated-circuit MOSFETs irradiated at cryogenic temperatures, the increased contribution of oxide-trapped charge to mobility degradation at low temperatures has been demonstrated by McLean and Boesch[13] in *n*-channel devices, while Saks *et al.*[14] have shown that mobility in *p*-channel devices is degraded even though no interface traps are formed at the low irradiation temperature. These findings are in agreement with the results of the present study, which are obtained by irradiating devices at room temperature, and characterizing mobility degradation at both room temperature and 77 K.

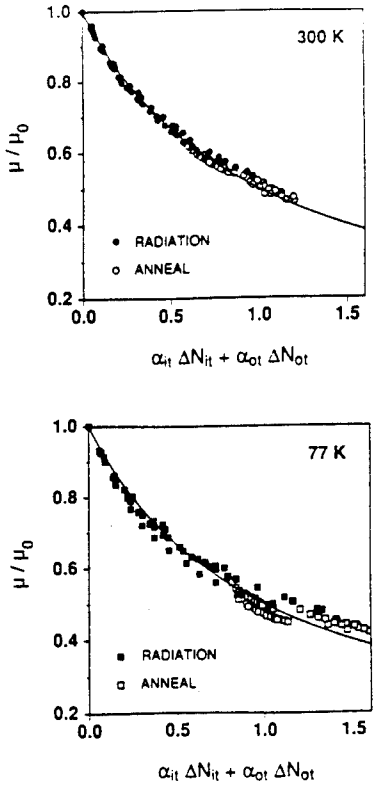


FIG. 7. Normalized mobility degradation during irradiation (closed symbols) and anneal (open symbols) in *p*-channel power MOSFETs as a function of the linear combination $\alpha_{it}\Delta N_{it}+\alpha_{ot}\Delta N_{ot}$: (a) at room temperature, and (b) at 77 K. The curves are the plots of Eq. (8) for $\alpha_{it}=3.9\times10^{-12}$ cm^2 and $\alpha_{ot}=0.7\times10^{-12}$ cm^2 [(a)], and for $\alpha_{it}=3.4\times10^{-12}$ cm^2 and $\alpha_{ot}=1.3\times10^{-12}$ cm^2 [(b)].

VI. CONCLUSIONS

Radiation-induced mobility degradation in *p*-channel MOSFETs at room temperature and 77 K has been investigated. The mobility degradation for given densities of radiation-induced defects is more pronounced at 77 K than at room temperature, due primarily to an increase in the relative importance of Coulomb scattering from the oxide-trapped charge. In accordance with previously published

results, interface traps play the dominant role in radiation-induced mobility degradation. However, in this article, and related studies,[2,3] we have demonstrated that the effects of oxide charges cannot be neglected if the density of oxide-trapped charge is large, which is normally the case in non-hardened MOSFETs. The effects of oxide-trapped charge are shown to be more important at 77 K than at room temperature.

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IV.F. Determining the Drain Doping in DMOS Transistors Using the Hump in the Leakage Current

Determining the Drain Doping in DMOS Transistors Using the Hump in the Leakage Current

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***Abstract*—The hump in the leakage current of double-diffused metal-oxide-semiconductor (DMOS) transistors observed for low drain voltages is explained. This hump is due to surface generation current of the gate-controlled diode formed by the base-drain p-n junction. The drain bias of the DMOS transistor is shown to have the same effect on the charge at the drain surface as the body bias in the conventional MOSFET. The body effect is used to develop a new method for determining the drain doping in DMOS transistors. This method is nondestructive, and does not require special test structures. Instead, electrical measurements are performed on conventional DMOS transistors. The method is ideally suited for determining the doping in the drain region of interest. Specifically, in DMOS transistors in which a surface implant is used to reduce the on-resistance, the method provides the doping concentration in the implanted region. In DMOS transistors which do not have the surface implant, the method yields the doping concentration in the drain epitaxial layer. In this study, the method is illustrated by determining the drain doping for six discrete power MOSFET device types from three different manufacturers.**

I. Introduction

THE double-diffused metal-oxide-semiconductor (DMOS) structure is widely used in discrete power MOSFET's and in power integrated circuits. High voltage capability is achieved by using a lightly doped drain drift region which also minimizes channel-length modulation. High current capability is obtained by connecting many DMOS cells in parallel. Fig. 1(a) shows the cross section of two adjacent cells of an n-channel DMOS transistor. The operation of the DMOS transistor biased with gate voltages above the threshold voltage (on-state) is well understood. Even though typical channel lengths are of the order of 1 μm, the absence of channel-length modulation allows application of the long-channel MOSFET theory to modeling of the drain current [1], [2]. More complex analytical [3] and seminumerical [4] models have been developed to account for effects specific to DMOS transistors operated under high current densities and high voltages, such as local heating, large voltage drop in the drift region, mobility degradation at high drain voltages, etc. On the other hand, no significant effort has been made to understand and model currents flowing through a DMOS transistor biased with gate voltages below the threshold voltage. In particular, the leakage current observed for zero gate voltage (off-state) is believed to be due to the reverse-biased p-n junction formed by the base region and the drain drift region. As long as this current remains within the manufacturer-specified limits, little attention is paid to its exact physical origins and its dependence on the bias voltages. In this study, the low-current operation of DMOS transistors biased with gate voltages below the threshold voltage is investigated. In particular, the "hump" in the leakage current observed for low drain voltages is explained. Fig. 1(b) displays the current-voltage characteristic of a typical IRF440 power MOSFET, and defines some terms which are used frequently later. The inset shows a magnified view of the hump. Note that the hump was first observed and qualitatively explained recently, in a study on effects of electrostatic discharge on power MOSFET's [5]. The present study provides a detailed quantitative analysis based on the gate-controlled diode theory. The drain bias of the DMOS transistor is shown to have the same effect on the charge at the drain surface as the body bias in the conventional MOSFET. The body effect is used to develop a new method for determining the drain doping in DMOS transistors. This method is nondestructive, and does not require special test structures. Instead, electrical measurements are performed on conventional DMOS transistors. The method is ideally suited for determining the doping in the drain region of interest. Specifically, in DMOS transistors in which a surface implant is used to reduce the on-resistance, the method provides the doping concentration in the implanted region. In DMOS transistors which do not have the surface implant, the method yields the doping concentration in the drain epitaxial layer. In this study, the method is illustrated by determining the drain doping for six discrete power MOSFET device types from three different manufacturers.

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II. Theory

A. Gate-Controlled Diode

The gate-controlled diode theory was developed by Grove and Fitzgerald [6], [7], and appended by Pierret [8]. A short description of the gate-controlled diode operation is given below. Fig. 2 shows the gate-controlled diode structure and the corresponding qualitative diode current versus gate voltage characteristic for a fixed positive voltage V_D. A positive

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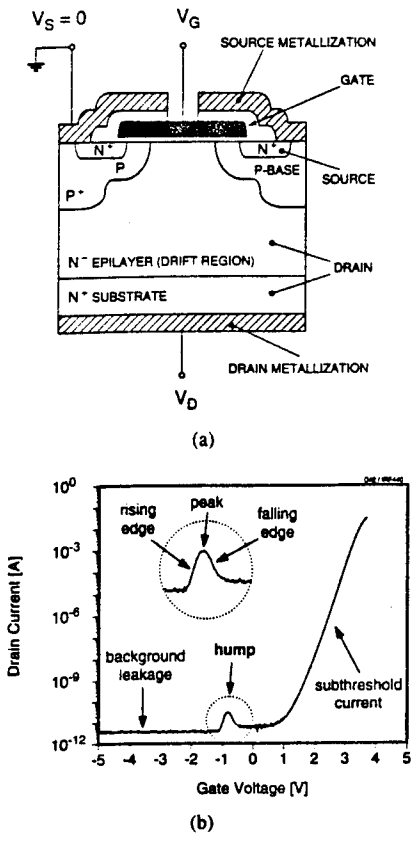


Fig. 1. (a) Cross section of the DMOS structure. (b) Drain current as a function of the gate voltage for a fixed drain voltage ($V_D = 0.1$ V) for an IRF440 power MOSFET. The inset shows the magnified view of the hump.

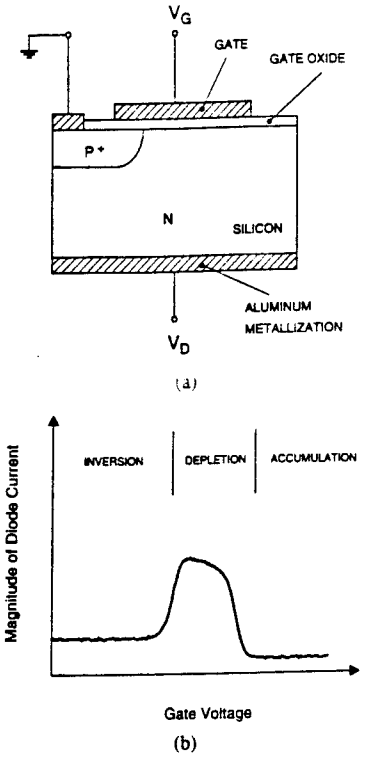


Fig. 2. (a) Cross section of the gate-controlled diode structure. (b) Qualitative diode current-gate voltage characteristic of the gate-controlled diode for a fixed positive voltage V_D. (After Grove and Fitzgerald [6], [7].)

V_D reverse biases the p-n junction. The diode reverse current at room temperature is predominantly due to Shockley–Read–Hall generation [9]. The magnitude of the current depends on the number of recombination-generation centers contained within the depletion region(s). These recombination-generation centers may be located in the silicon bulk or at the silicon surface (silicon-silicon dioxide interface). For a sufficiently positive gate voltage, the silicon surface under the gate is accumulated and only those bulk recombination-generation centers which are within the p-n junction depletion region contribute to the generation current. On the other hand, when the gate voltage is sufficiently negative, the silicon surface under the gate is strongly inverted. Now, there is a field-induced surface depletion region in the lightly doped n-region in addition to the depletion region of the p-n junction. The number of bulk recombination-generation centers enclosed by these two depletion regions is larger than that in the case of accumulation. Consequently, the reverse current is larger when the surface is inverted than when the surface is accumulated. When the silicon surface under the gate is depleted, surface recombination-generation centers add another component to the reverse diode current. As a result, the maximum reverse current is observed at gate voltages for which the silicon surface under the gate is depleted.

B. DMOS Structure—A Gate-Controlled Diode in Disguise

Fig. 1(a) shows the cross section of an n-channel vertical DMOS transistor. During normal device operation, a positive drain-to-source voltage results in electron flow from the source to the drain if a sufficiently positive gate-to-source voltage is applied. In all the measurements reported in this study, the source terminal was grounded ($V_S = 0$). Consequently, the gate-to-source voltage $V_{GS} = V_G - V_S$ equals the gate voltage V_G, and the drain-to-source voltage $V_{DS} = V_D - V_S$ equals the drain voltage V_D. By convention, the drain current is positive when it flows into the drain terminal.

Even though the DMOS structure is more complex than the gate-controlled diode, the latter structure can easily be recognized in Fig. 1(a). The P-base and the lightly doped N drain drift region form a p-n junction which is controlled by the polysilicon gate. To complete the analogy with the gate-controlled diode shown in Fig. 2(a), the source and the P-base of a DMOS transistor are shorted internal to the device by the source metallization. This results in a three-terminal device which is equivalent to the gate-controlled diode when the gate bias is not sufficiently positive to induce a conductive channel between the source and the drain. Note that the presence of the heavily doped N^+ source is essential for operation of the DMOS transistor, but it does not affect the properties of the gate-controlled diode formed by the P-base and the drain drift region.

C. Relationship Between Surface Potential in the Drain Drift Region and Gate Voltage

The properties of the drain drift region (most notably the doping level and the flat-band voltage) determine the values of the gate voltage required to bring the silicon surface to a given level of inversion. The surface potential in the drain u-

is related to the gate voltage V_G by the following expression:

$$V_{GD} = V_G - V_D = V_{FB} + \psi_s - \frac{Q_S}{C_{ox}} \quad (1)$$

where V_{FB} is the flat-band voltage, C_{ox} is the gate-oxide capacitance per unit area, and

$$Q_S = \pm F\sqrt{N_D} \times \left\{ \phi_t e^{\psi_s/\phi_t} - \psi_s - \phi_t + e^{2\phi_F/\phi_t}\left[\phi_t e^{-(\psi_s+V_D)/\phi_t} + \psi_s - \phi_t e^{-V_D/\phi_t}\right]\right\}^{\frac{1}{2}} \quad (2)$$

is the total charge (per unit area) in the semiconductor [10], which is the sum of the inversion layer charge and the ionized impurity-atom charge in the depletion region. N_D is the donor concentration in the N-drift region. ϕ_t is the thermal potential (approximately 0.026 V at room temperature), and ϕ_F is the Fermi potential for the N-drift region, defined by

$$\phi_F = -\phi_t \ln \frac{N_D}{n_i} \quad (3)$$

where n_i is the intrinsic electron concentration (1.45×10^{10} cm^{-3} at room temperature). $F = \sqrt{2q\epsilon_s}$ where q is the magnitude of the electron charge, and ϵ_s is the silicon permittivity.

Note that (1) and (2) are valid in all regimes (accumulation, depletion, and inversion). The plus sign in (2) is used when the surface potential is negative (depletion and inversion), and the minus sign is used when the surface potential is positive (accumulation). When the drain surface potential is negative with magnitude between several ϕ_t and $|2\phi_F - V_D|$ (drain surface not strongly inverted), (2) is greatly simplified. Using that simplified (2) in (1) we obtain:

$$V_G = V_{FB} + \psi_s + V_D - \gamma\sqrt{-\psi_s} \quad (4)$$

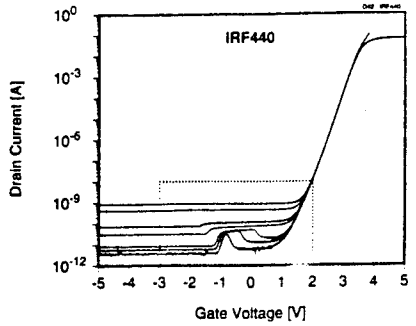
where γ is the body effect coefficient, defined by

$$\gamma = \frac{F\sqrt{N_D}}{C_{ox}}. \quad (5)$$

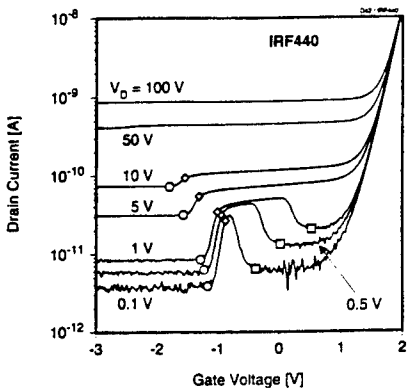
D. Experimental Results—Drain Current as a Function of Gate Voltage

All the measurements reported in this study were performed at room temperature using a HP4145B semiconductor parameter analyzer. In all of the measurements, the source terminal was grounded. A total of six discrete power MOSFET types from three different manufacturers were used: four n-channel types (IRF150 and IRF250 manufactured by International Rectifier, IRF130 manufactured by Harris Semiconductor, and IRF440 manufactured by Motorola), and two p-channel types (IRF9130 manufactured by Harris Semiconductor and MTM8P08 manufactured by Motorola).

Fig. 3(a) is the semilogarithmic plot of the drain current as a function of the gate voltage for several values of the drain voltage (V_D = 0.1 V, 0.5 V, 1 V, 5 V, 10 V, 50 V, and 100 V) for a typical IRF440 power MOSFET. Fig. 3(b) shows a magnified view of the portion of the current-voltage characteristics enclosed by the dotted frame in Fig. 3(a). The leakage current observed for negative gate voltages increases as the drain voltage increases. Two distinct regions of operation in the



(a)



(b)

Fig. 3. (a) Semilogarithmic plot of the drain current as a function of the gate voltage for several values of the drain voltage (V_D = 0.1 V, 0.5 V, 1 V, 5 V, 10 V, 50 V, and 100 V) for an IRF440 power MOSFET. (b) A magnified view of the portion of the current-voltage characteristics enclosed by the dotted frame in (a). The squares denote points where $V_G = V_0$, and $\psi_s = 0$ (flatband), the diamonds denote points where $V_G = V_1$, and $\psi_s = \phi_F - V_D$ (onset of weak inversion), and the circles denote points where $V_G = V_2$, and $\psi_s = 2\phi_F - V_D$ (onset of strong inversion). The values of gate voltages V_0, V_1, and V_2 were calculated using $N_D = 1.9 \times 10^{14}$ cm^{-3}, and $V_{FB} = -0.48$ V.

leakage current can be observed. First, for large negative gate voltages (drain surface strongly inverted) the leakage current does not depend on the gate voltage. This leakage current is due to the bulk generation in the depletion regions and it has been termed the background leakage in Fig. 1(b). Second, for small negative gate voltages (drain surface depleted) the leakage current depends on the gate voltage and a "hump" is observed. In this region, the leakage current is the sum of the bulk-generation component I_{bg} and the surface-generation component I_{sg}. When the gate voltage is sufficiently positive, the subthreshold conduction begins. In this region of operation, the drain current is approximately an exponential function of the gate voltage, and it does not depend on the drain voltage. The subthreshold operation region is observed for the drain current ranging from approximately several nanoamperes to several milliamperes. For larger drain currents, the above-threshold conduction sets in, where the logarithm of the drain current is no longer a linear function of the gate voltage.

The leakage current observed for large negative gate voltages (background leakage) increases as the drain voltage increases. This increase in I_{bg} is caused by an increase in the width of the depletion regions, leading to increased gener-

ation current due to bulk recombination-generation centers. In addition, the width of the hump increases as the drain voltage is increased. The effects of the drain voltage on the hump are discussed in more detail later. It should be noted here that for large drain voltages (above 10 V) the hump is barely discernible because the bulk-generation component of the leakage current increases as the drain voltage is increased, and the surface-generation component (responsible for the hump) does not increase.

In Fig. 3(b) some significant values of the gate voltage (V_0, V_1, and V_2) are marked as follows: the squares denote gate voltages resulting in the flat-band condition in the drain ($V_G = V_0$; $\psi_s = 0$); the diamonds denote the boundary between depletion and weak inversion ($V_G = V_1$; $\psi_s = \phi_F - V_D$); and the circles denote the boundary between weak inversion and strong inversion ($V_G = V_2$; $\psi_s = 2\phi_F - V_D$). Quantitatively, setting $\psi_s = 0$ in (2) results in $Q_S = 0$, so that (1) reduces to

$$V_0 = V_{FB} + V_D \qquad \text{for } \psi_s = 0. \tag{6}$$

Similarly, from (4) we obtain:

$$V_1 = V_{FB} + \phi_F - \gamma\sqrt{-\phi_F + V_D} \qquad \text{for } \psi_s = \phi_F - V_D \tag{7}$$

and

$$V_2 = V_{FB} + 2\phi_F - \gamma\sqrt{-2\phi_F + V_D} \qquad \text{for } \psi_s = 2\phi_F - V_D. \tag{8}$$

The values of gate voltages V_0, V_1, and V_2 were calculated using $C_{ox} = 3.14 \times 10^{-8}$ F cm^{-2}, $N_D = 1.9 \times 10^{14}$ cm^{-3}, and $V_{FB} = -0.48$ V. The oxide capacitance per unit area was calculated using the known gate-oxide thickness, while the drain doping and the flatband voltage were determined using a method which is described in Section III.

It is evident from Fig. 3(b) that the hump is observed at gate voltages for which the surface is depleted or weakly inverted. When the drain surface under the gate is strongly inverted (to the left of the circles), or accumulated (to the right of the squares), the leakage current component due to surface generation in the drain is negligible. Clearly, the contribution of surface generation to the leakage current strongly depends on the value of the surface potential. This surface-generation component of the leakage current is

$$I_{sg} = q|U_s|A_s \tag{9}$$

where U_s is the surface recombination-generation rate per unit area and A_s is the surface area of the drain under the gate. If the capture cross sections for electrons and holes are assumed to be equal and if the surface recombination-generation centers are assumed to have a uniform distribution in energy throughout the band gap, the surface recombination-generation rate is given by the following expression [7]:

$$U_s = \sigma_s v_{th} D_{it} \times \left\{ \int_{E_V}^{E_C} \frac{dE_{it}}{n_s + p_s + 2n_i \cosh[(E_{it} - E_i)/q\varphi_t]} \right\} \times (n_s p_s - n_i^2) \tag{10}$$

where σ_s is the capture cross section of the surface recombination-generation centers, v_{th} is the thermal velocity (approximately 10^7 cm/s at room temperature), D_{it} is the density of surface recombination-generation centers (interface traps) per unit area and unit energy, E_{it} is the energy level of surface recombination-generation centers, E_i is the intrinsic Fermi level, and n_s and p_s are the concentrations of majority carriers (electrons) and minority carriers (holes), respectively, at the surface of the drain under the gate. Equation (10) is based on the Shockley-Read-Hall theory of the recombination-generation processes in semiconductors [11], [12]. The integration limits are the top of the valence band E_V, and the bottom of the conduction band E_C. The strong dependence of the surface recombination-generation rate on the surface potential is due to the fact that the surface concentrations of electrons and holes depend exponentially on ψ_s:

$$n_s = N_D e^{\psi_s/\phi_t}, \tag{11}$$

$$p_s = N_D e^{-(\psi_s - 2\phi_F + V_D)/\phi_t}. \tag{12}$$

In accumulation, the surface concentration of electrons is large, and U_s is small. In strong inversion, the surface concentration of holes is large and, again, U_s is small.

Fig. 4 shows the energy band diagrams (when the drain voltage is fixed at $V_D = 0.5$ V) for some significant values of the surface potential, along with the corresponding drain current-gate voltage characteristic. The positions of E_V, E_i, and E_C at the drain surface are denoted by solid circles. The base-drain p-n junction is not in equilibrium when V_D is different from zero. Consequently, the single Fermi level which exists in equilibrium is replaced here by two quasi-Fermi levels: one for electrons E_{F_n}, and one for holes E_{F_p}. A positive drain voltage reverse biases this p-n junction. As a result, the quasi-Fermi level for holes is above the quasi-Fermi level for electrons. Their separation is determined by the value of the drain voltage, $E_{F_p} - E_{F_n} = qV_D$. The symbols on the current-voltage characteristic have the same meaning as in Fig. 3: the square denotes the flat-band condition, the diamond denotes the onset of weak inversion, and the circle denotes the onset of strong inversion. In addition, the triangle denotes the point at which the surface generation reaches maximum.

The drain surface is strongly inverted when the intrinsic Fermi level (E_i) at the surface is at least one Fermi potential (ϕ_F) above the quasi-Fermi level for minority carriers (E_{F_p}). At the onset of strong inversion (the energy band diagram in the upper left-hand corner of Fig. 4), E_i is exactly one ϕ_F above E_{F_p} at the surface. At the onset of weak inversion, E_i at the surface equals E_{F_p} (the energy band diagram is not shown in Fig. 4). At flat-band (the energy band diagram in the upper right-hand corner of Fig. 4), the surface potential equals zero and E_i is the same at the drain surface as in the drain bulk. The values of the surface potential corresponding to these energy band diagrams and the resulting gate voltages have been given in (6)–(8). The value of the surface potential corresponding to the maximum of the surface generation and the resulting gate voltage are obtained using (10)–(12) and (4). From (10), the surface recombination-generation rate reaches maximum for a value of the surface potential resulting in a minimum of the sum of the surface concentrations of electrons and holes.

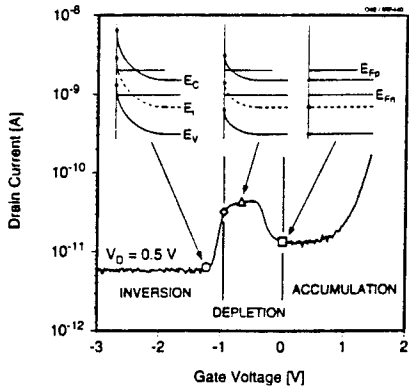


Fig. 4. The energy band diagrams for a fixed drain voltage $V_D = +0.5$ V and the corresponding drain current-gate voltage characteristic. The symbols have the same meaning as in Fig. 3: the square denotes the flatband condition, the diamond denotes the onset of weak inversion, and the circle denotes the onset of strong inversion. In addition, the triangle denotes the point at which the surface generation reaches maximum. The positions of E_{Fp}, E_i, and E_C at the drain surface are denoted by solid circles.

For n_s and p_s given by (11) and (12), the maximum surface recombination-generation rate occurs when

$$\psi_s = \phi_F - \frac{V_D}{2}. \tag{13}$$

Note that the same condition was derived by Fitzgerald and Grove [7] for a forward-biased gate-controlled diode, and by Reddi [13] for a forward-biased emitter-base junction of a bipolar transistor. From (11) and (12), it can be seen that this condition leads to $n_s = p_s$, i.e., the surface recombination-generation velocity has a maximum value when the surface concentrations of electrons and holes are equal. In the energy band notation, this means that the intrinsic Fermi level at the surface is exactly halfway between the two quasi-Fermi levels (the energy band diagram in the middle in Fig. 4). Finally, it should be mentioned that the condition given by (13) holds only when the capture cross sections for electrons and holes are equal, because (10) was derived under that assumption. Reddi [13] derived an expression more general than (13), which is valid when the capture cross sections of the surface recombination-generation centers for electrons and holes are not equal.

Since the inversion-layer charge is negligible for the surface potential given by (13), it is possible to use (4) to find the gate voltage resulting in the maximum surface generation rate:

$$V_{\text{peak}} = V_{FB} + \phi_F + \frac{V_D}{2} - \gamma\sqrt{-\phi_F + \frac{V_D}{2}}. \tag{14}$$

In this subsection, significant values of the surface potential have been identified and the expressions for the corresponding gate voltage have been given. The hump has been shown to exist only when the drain surface is depleted or weakly inverted. Thus the hump is bounded by strong inversion to the left and accumulation to the right (Fig. 4). Although the drain voltage appears in many of the expressions presented so far, its effects on the hump are discussed separately in some detail below. Proper understanding of the effects of the drain voltage is essential for development of the method for determining the doping in the drain described in Section III.

E. Effects of Drain Voltage on the Hump

The most obvious effect of increasing the drain voltage is the increase in the width of the hump. As shown in Fig. 3(b), when V_D increases, the flat-band point (squares) moves to the right (toward more positive gate voltages), and the point denoting the onset of strong inversion (circles) moves to the left (toward more negative gate voltages). The change in the gate voltage required to bring about the flat-band condition is easily understood from (6); an increase in V_D necessitates an increase in the gate voltage V_0 in order to keep their difference equal to the flat-band voltage V_{FB}. Similarly, from (8) we see that an increase in V_D makes the gate voltage V_2 more negative, i.e., increases its magnitude. The leading edge of the hump (observed for gate voltages between V_2 and V_1) moves to the left slower than the falling edge moves to the right. This is because both V_2 and V_1 contain the drain voltage under the square-root sign, whereas V_0 varies linearly with V_D. Note that (8) is equivalent to the expression for the threshold voltage of a p-channel MOSFET which has the body (substrate) bias equal to V_D. Fig. 1(a) allows this quasi-transistor to be identified; the two adjacent P-base regions (which belong to two adjacent DMOS cells) may be viewed as the source and the drain of a p-channel MOSFET, while the N-drift region serves as the body (substrate). This is actually not a transistor because the P-base regions are shorted together by the source metallization, and there can be no lateral current flow between them. However, in terms of its effect on $V_2 = V_T$, the drain voltage behaves exactly the same as the body bias of a conventional p-channel MOSFET. The dependence of the MOSFET threshold voltage on the body bias is commonly referred to as the body effect.

More insight into the effects of drain voltage on the hump may be gained by considering the dependence of the total charge in the drain on the bias voltages. Fig. 5 displays the magnitude of the total charge per unit area, Q_S, as a function of the gate voltage with the drain voltage as a parameter. The charge in the drain for a given value of the surface potential was calculated using (2), and the corresponding gate voltage was evaluated from (1). The current-voltage characteristics corresponding to the drain voltages used to calculate Q_S are also shown in Fig. 5. The dashed lines mark the points where the total charge changes sign; the charge is positive to the left of the dashed lines and negative to the right of the lines. Clearly, increasing the drain voltage causes the interval of gate voltages for which the surface is depleted to expand (this interval is bounded by the diamonds on the left and the squares on the right on the current-voltage characteristics). For the drain voltage larger than approximately 2 V, the falling edge of the hump cannot be seen because the subthreshold conduction begins before the drain surface can be accumulated. Therefore, for $V_D = 5$ V and $V_D = 10$ V, the charge in the drain remains positive for the whole range of the gate voltage shown in Fig. 5.

Finally, one significant difference between the gate-controlled diode shown in Fig. 2 (a) and the base-drain diode in a DMOS structure is discussed and its consequence to the hump is explained. The difference is in the doping level of the P regions. The P^+ region of the gate-controlled diode shown

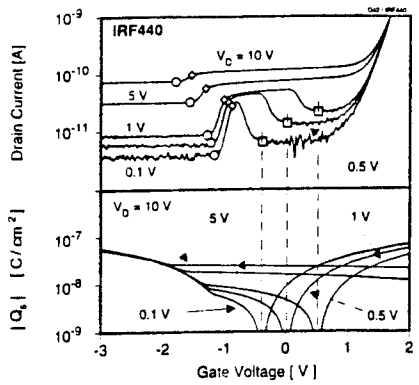


Fig. 5. The total charge per unit area in the drain as a function of the gate voltage with the drain voltage as a parameter. Also shown are the corresponding drain current-gate voltage characteristics. The dashed lines denote the gate voltages resulting in the flatband condition in the drain (zero charge) for a given value of the drain voltage ($V_G = -0.38$ V for $V_D = 0.1$ V, $V_G = 0.02$ V for $V_D = 0.5$ V, and $V_G = 0.52$ V for $V_D = 1$ V).

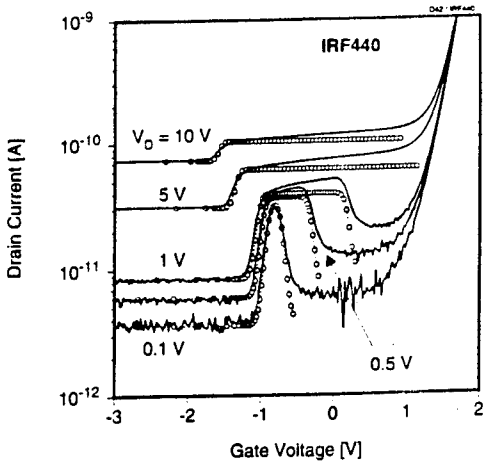


Fig. 6. The measured drain current (solid lines) and the calculated leakage current (symbols connected by dotted lines) as a function of the gate voltage with the drain voltage as a parameter.

in Fig. 2 (a) is heavily doped and cannot be depleted unless very large positive voltage is applied at the gate terminal. Consequently, for practical gate voltages this P^+ region does not contribute to the reverse diode current. It is therefore sufficient to consider the N region in analyzing the reverse diode current. In contrast, the P-base region in the DMOS structure is not heavily doped and the surface charge in this region can easily be modulated by the gate voltage. Therefore, the P-base may contribute a nonnegligible generation current to the reverse diode current.

Fig. 6 gives the comparison between the measured drain current (solid lines) and the calculated leakage current (symbols connected by dotted lines). The leakage current is the sum of the measured background leakage I_{bg} (to the left of the hump) and the calculated surface-generation component I_{sg}. The surface-generation component was calculated as follows: 1) for a chosen value of the surface potential ψ_s, the surface concentrations n_s and p_s were evaluated from (11) and (12), respectively; 2) these values were used in (10) to find the surface recombination-generation rate U_s; 3) this value of U_s was in turn used in (9) to calculate I_{sg}. Finally, (1) and (2) were employed to relate the chosen value of the surface potential to the gate voltage. This procedure was repeated for a number of different values of the surface potential. Note that the value of the product $A_s\sigma_s D_{it}$ was chosen so that the measured and the calculated peaks for $V_D = 0.1$ V coincide. The same value of this product was used in calculating I_{sg} for the remaining drain voltage values. As an example illustrating the order of magnitude of the quantities of interest, $A_s = 0.1$ cm^2, $\sigma_s = 10^{-16}$ cm^2, and $D_{it} = 3.3 \times 10^9$ cm^{-2}eV^{-1}, give the desired product.

The integral in (10) was evaluated analytically, replacing the integration limits E_V and E_C by $-\infty$ and $+\infty$, respectively. The error introduced in this way is negligible because the recombination-generation centers with energy levels near the middle of the energy band are much more efficient than those near the band edges [7]. Therefore, adding centers located ≈ 0.5 eV (or more) away from the middle of the energy band does not affect the value of the integral.

It is evident from Fig. 6 that the experiment and the theory are in good overall agreement. The contribution of the P-base region to the leakage current is not included in the theoretical analysis, and consequently the increase in the leakage current as the gate voltage increases, which is observed in the measured current-voltage characteristics, is not predicted by the calculations. In addition, the measured leakage current is larger to the right of the hump (when the drain surface is accumulated) than to the left of the hump (when the drain surface is strongly inverted) which is contrary to the predictions of the simple gate-controlled diode theory presented in Section II–A. This can also be explained by the contribution of the P-base region. Namely, the increase in the gate voltage results in an increase in the width of the depletion region in the P-base below the gate. As a result, the generation current in the depletion region in the P-base increases as the gate voltage is increased.

A comparison between the measured and the calculated humps reveals that the experiment gives a wider hump than the calculations (Fig. 6). Similar results were obtained by Fitzgerald and Grove [7], and by Reddi [13], for recombination current of forward biased p-n junctions. The proposed explanations were: (1) microscopic nonuniformities of the surface potential caused by the random spatial distribution of surface charges [7]; and (2) the nonnegligible contribution of recombination-generation centers with energies not equal, but close to midgap [13]. In the present study, a uniform density of the recombination-generation centers in energy was assumed in calculating U_s (in contrast to [13], where a single trap level located at midgap was assumed). This eliminates explanation (2). The most plausible explanation is based on the variation of the surface potential in the direction parallel to the semiconductor surface, but the cause is probably different from that given in explanation (1). Pierret [8] demonstrated that the quasi-Fermi level for minority carriers does not remain constant as one moves along the semiconductor surface away from the p-n junction. For the DMOS structure, this means that the maximum surface recombination-generation velocity may occur at different surface potential values, and thus different

gate voltages, for points near the base-drain junction and for points halfway between the cells. The existence of more than one gate voltage resulting in the maximum U_s leads to broadening of the hump.

III. Determining Doping in the Drain

A. Exact Analysis

The body effect may be used to determine the doping in the substrate of a MOSFET. The method is described in [14] and [10]. The threshold voltage of a p-channel MOSFET is

$$V_T = V_{FB} + 2\phi_F - \gamma\sqrt{-2\phi_F + V_{BS}} \tag{15}$$

where V_{BS} is the body-to-source voltage, or the body bias (positive for p-channel devices). If the threshold voltage is plotted as a function of $\sqrt{-2\phi_F + V_{BS}}$, a straight line is obtained, with the slope equal to the body-effect coefficient γ. The doping concentration in the substrate is found from (5) as

$$N_D = \left(\frac{\gamma C_{ox}}{F}\right)^2. \tag{16}$$

For the DMOS structure, the gate voltage required to bring the drain surface to strong inversion was given by (8). That expression for V_2 is equivalent to the expression for the threshold voltage of a p-channel MOSFET (15), with the drain voltage playing the role of the body bias. Apparently, V_2 could be measured for different values of the drain voltage, and plotted as a function of $\sqrt{-2\phi_F + V_D}$ to obtain γ. Unfortunately, it is not possible to reliably measure V_2, because the transition between the background leakage current (which is independent of the gate voltage) and the hump is gradual, and there is no single point which can with certainty be identified as the onset of strong inversion, where $\psi_s = 2\phi_F - V_D$. Therefore, the gate voltage corresponding to a different value of the surface potential should be chosen as the quantity which is measured as a function of the drain voltage. It is desirable to select a gate voltage corresponding to a point on the rising edge of the hump, where the slope of the current-voltage characteristic is large. In this way, small uncertainties in the drain current will result in small changes in the gate voltage. We select a point where the drain current equals:

$$I_x = \frac{I_{bottom} + I_{top}}{2} \tag{17}$$

where I_{bottom} is the drain current at the bottom of the hump and I_{top} is the drain current at the top of the hump. Clearly, I_{bottom} is equal to the background leakage, $I_{bottom} = I_{bg}$, and is independent of the gate voltage. On the other hand, I_{top} cannot simply be defined as the maximum value of the drain current on the hump. In contrast to the calculated current, the measured current is not constant when the drain surface is depleted (Fig. 6), because of the contribution of the depleted P-base to the total leakage current. We define I_{top} as the end point of the rising edge. Fig. 7 shows the points corresponding to the chosen values of I_{bottom} and I_{top} (plain crosses), and the resulting I_x (bold crosses), for the drain voltages ranging

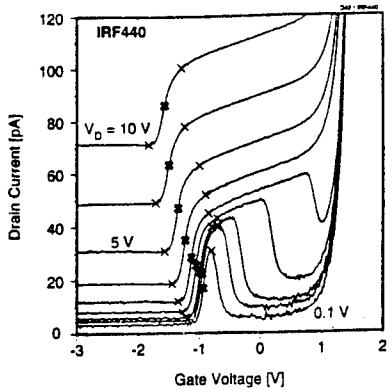


Fig. 7. Linear plot of the drain current as a function of the gate voltage for several values of the drain voltage (V_D = 0.1 V, 0.3 V, 0.5 V, 1 V, 1.7 V, 3 V, 5 V, 8 V, and 10 V) used in the measurements of V_x. The plain crosses denote values of the currents I_{bottom} and I_{top}, while the bold crosses denote points (V_x, I_x).

from 0.1 V to 10 V. Note that the precision with which I_{top} is chosen does not significantly affect the value of the gate voltage V_x corresponding to I_x. First, if the uncertainty in I_{top} is ΔI, from (17) we find that the uncertainty in I_x is only $\Delta I/2$. Second, small changes in I_x lead to small changes in V_x, because of the steepness of the current-voltage characteristics in the vicinity of I_x.

If the surface potential corresponding to the point (V_x, I_x) is denoted by $\psi_x = \phi_x - V_D$, the gate voltage V_x is obtained from (4):

$$V_x = V_{FB} + \phi_x - \gamma\sqrt{-\phi_x + V_D}. \tag{18}$$

Therefore, if V_x is plotted as a function of $\sqrt{-\phi_x + V_D}$, the slope of the straight line gives the body-effect coefficient, which can be used in (16) to find the doping concentration in the drain. However, the value of ϕ_x is not known in advance. Comparison between Figs. 3(b) and 7 suggests that ϕ_x is between ϕ_F and $2\phi_F$. Fig. 8 is the plot of V_x as a function of $\sqrt{-\phi_x + V_D}$ for one possible value of ϕ_x. Fig. 9 illustrates the need for knowing the exact value of ϕ_x. Different values of ϕ_x result in different values of γ, and thus, the doping concentration in the drain N_D depends on the choice of ϕ_x. Note that ϕ_x is not the only unknown quantity in (18). The flat-band voltage V_{FB} is also unknown. Therefore, two equations which contain ϕ_x and V_{FB}, and which correspond to two easily identifiable points on the hump are needed to find both of these quantities. The first equation is (18), which gives the gate voltage V_x corresponding to the current I_x. We choose (14) as the second equation, because for low drain voltages the hump has a well defined peak. Although ϕ_x does not appear explicitly in (14), both ϕ_F and γ depend on the choice of ϕ_x.

We denote the flatband voltage obtained from (18) as V_{FBx}, and the flat-band voltage obtained from (14) as V_{FBpeak}. Note that if a value of ϕ_x is known (or assumed), V_{FBx} is obtained from the y-axis intercept of the straight line in Fig. 8 (as seen from (18), the y-axis intercept equals $V_{FBx} + \phi_x$). On the other hand, if ϕ_x is known (or assumed), V_{FBpeak} is obtained by subtracting the *calculated* $V_{peak} - V_{FBpeak}$ from the *measured* V_{peak}. The calculated $V_{peak} - V_{FBpeak}$ is obtained from (14) as follows: for an assumed value of ϕ_x, γ is found from the

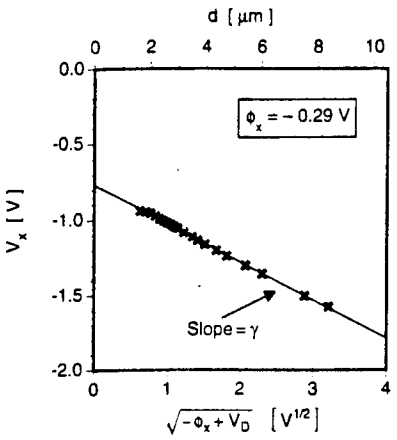


Fig. 8. V_x as a function of $\sqrt{-\phi_x + V_D}$ for one particular value of the potential ϕ_x. The top x-axis shows the surface depletion region thickness d.

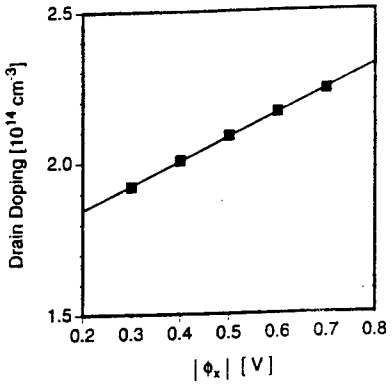


Fig. 9. Drain doping as a function of the magnitude of the potential ϕ_x.

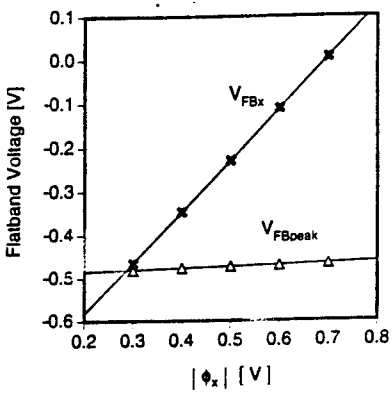


Fig. 10. Flat-band voltages V_{FBx} and V_{FBpeak} as a function of the magnitude of the potential ϕ_x. The intersection of these two plots gives the values of the potential $\phi_x = -0.29$ V, and the flatband voltage $V_{FB} = -0.48$ V.

plot V_x vs. $\sqrt{-\phi_x + V_D}$ (Fig. 8), while ϕ_F is found using (16) and (3). It is important that the drain voltage used when measuring V_{peak} be small in magnitude. As can be seen from Figs. 3(b) and 7, there is a well-defined peak only for low values of the drain voltage. We measured V_{peak} using three different values of V_D : 0.05 V, 0.1 V, and 0.15 V. For each chosen value of ϕ_x, three slightly different values of $V_{FB\text{peak}}$ are obtained corresponding to these three values of the drain voltage. (These differences are caused by the measurement uncertainty associated with V_{peak}, and by the approximative nature of (13) and (14), which are exact only when the capture cross sections for electrons and holes are equal.) A single value of $V_{FB\text{peak}}$ for a particular value of ϕ_x is obtained by finding the average of the three values of $V_{FB\text{peak}}$. Note that both V_{FBx} and $V_{FB\text{peak}}$ depend on the choice of ϕ_x.

Since ϕ_x is not known in advance, we plot the flat-band voltage V_{FBx}, obtained from (18), and the flat-band voltage $V_{FB\text{peak}}$, obtained from (14), as a function of ϕ_x. These two functions intersect at a point $V_{FBx} = V_{FB\text{peak}}$, which is the value of the flat-band voltage sought. The ordinate of this point gives the value of ϕ_x. Thus the nonlinear set of equations ((18) and (14)) is solved for V_{FB} and ϕ_x graphically. This approach is illustrated in Fig. 10. The plots of both V_{FBx} and $V_{FB\text{peak}}$ are straight lines, which intersect at the point $\phi_x = -0.29$ V, $V_{FB} = -0.48$ V. For this value of ϕ_x, the doping concentration in the drain obtained from Fig. 9 is $N_D = 1.9 \times 10^{14}\,\text{cm}^{-3}$.

It should be noted that Figs. 3 through 10 show the data obtained from a single IRF440 power MOSFET. The flatband voltage $V_{FB} = -0.48$ V and the doping in the drain $N_D = 1.9 \times 10^{14}\,\text{cm}^{-3}$ obtained using the method described above have been used to calculate V_0, V_1, and V_2 shown in Figs. 3(b), 4, and 5, and to calculate I_{sg} shown in Fig. 6. Also, the correct value of ϕ_x has been used to generate the data plotted in Fig. 8. None of the quantities V_{FB}, N_D, and ϕ_x is known in advance; they all had to be determined using the method described above before the calculations could be performed.

The top x-axis in Fig. 8 shows the depletion region width d at the surface of the drain corresponding to the measured values of the gate voltage V_x. The depletion region width corresponding to V_x, i.e., to the surface potential $\psi_x = -\phi_x + V_D$ is

$$d = \sqrt{\frac{2\varepsilon_s(-\phi_x + V_D)}{qN_D}}. \tag{19}$$

For $\phi_x = -0.29$ V and $N_D = 1.9 \times 10^{14}\,\text{cm}^{-3}$, we find that d ranges from 1.6 μm (for $V_D = 0.1$ V, which is the lowest value of the drain voltage used in measurements of V_x) to 8.4 μm (for $V_D = 10$ V, which is the highest value of the drain voltage used in measurements of V_x). From (18) we obtain

$$\gamma = -\frac{dV_x}{d(\sqrt{-\phi_x + V_D})}. \tag{20}$$

Thus γ evaluated for a particular value of the drain voltage gives the slope of the graph V_x vs. $\sqrt{-\phi_x + V_D}$ at that point. From Fig. 8 we see that the slope is constant, and thus, the doping is constant for d larger than approximately 2 μm. As mentioned above, for this drain doping ($N_D = 1.9 \times 10^{14}\,\text{cm}^{-3}$) and for the drain voltage ranging from 0.1 to 10 V, this technique probes the doping profile ranging from 1.6 μm to 8.4 μm. For the same drain voltage range, the profile depth is smaller in a more heavily doped drain (as found in power MOSFET's with lower voltage ratings). For a given

drain doping, the lower limit of the profile depth is determined by the lowest drain voltage value that allows reliable current measurements (the current resolution limit is 1 pA for the HP 4145B), while the upper limit is set by the drain voltage for which the background leakage increases to the extent that the hump can no longer be observed.

This method for determining the doping in the drain was employed to characterize six different types of discrete power MOSFET's. Table I summarizes the results. The sample size was five devices per device type. The drain doping shown in the table was obtained by averaging the doping values obtained from those five devices. The uniformity of drain doping among the devices of the same type was good: the difference between the highest doping and the lowest doping was 4% for "the most uniform" device type and 14% for "the least uniform" device type. Note that an effort was made to assure that all five devices per device type come from the same wafer lot. For IRF150 and IRF250, this was established with certainty, because the lot code is imprinted on the device package; for the remaining four device types this information was not available, but the devices likely were from the same wafer lot because the production date code was the same for all five devices of a given device type.

The drain doping is expected to decrease as the voltage rating of power MOSFET's increases. The data shown in Table I indicate that there may be an exception to this trend. IRF250 has higher voltage rating and higher drain doping than IRF130, IRF150, IRF9130, and MTM8P08. This is because in this device type an n-type implant at the surface of the drain is employed to reduce the series resistance of the drain, while the other device types used in this study do not have such an implant. The profile depth for this device is from 0.4 μm to 1.7 μm, for the drain voltage ranging from 0.1 V to 10 V. Therefore, the method described here allows the doping in the surface region of the drain affected by the ion implantation to be measured, which is of great interest in optimizing the series resistance of the drain. Note that the breakdown voltage, and thus voltage rating, is set by the doping value deep in the drain bulk. As expected from the discussion presented above, the profile depth is smaller in this device type than in IRF440, because the measured drain doping is significantly higher in IRF250 than in IRF440.

TABLE I
DRAIN DOPING FOR SIX DIFFERENT POWER MOSFET DEVICE TYPES. THE DOPING WAS DETERMINED USING THE METHOD DESCRIBED IN THE TEXT. THE DOPING FOR EACH DEVICE TYPE SHOWN IN THE TABLE IS THE AVERAGE VALUE FOR A SAMPLE OF FIVE DEVICES PER DEVICE TYPE

Device Type	Polarity	Manufacturer	Voltage Rating [V]	Drain Doping [10^{15}cm^{-3}]
IRF130	n-channel	Harris Semiconductor	100	2.1
IRF150		International Rectifier	100	3.1
IRF250		International Rectifier	200	4.7
IRF440		Motorola	500	0.19
MTM8P08	p-channel	Motorola	80	3.0
IRF9130		Harris Semiconductor	100	3.2

TABLE II
POTENTIAL φ_x, FERMI POTENTIAL φ_F, AND THE RATIO OF THESE TWO POTENTIALS FOR THE SIX POWER MOSFET DEVICE TYPES WHOSE DRAIN DOPINGS ARE GIVEN IN TABLE I. THE POTENTIALS ARE THE AVERAGES FOR A SAMPLE OF FIVE DEVICES PER DEVICE TYPE

Device Type	Polarity	φ_x [V]	φ_F [V]	φ_x/φ_F
IRF130	n-channel	-0.337	-0.309	1.09
IRF150		-0.356	-0.319	1.12
IRF250		-0.370	-0.330	1.12
IRF440		-0.286	-0.247	1.16
MTM8P08	p-channel	0.367	0.319	1.15
IRF9130		0.366	0.320	1.14

B. Fast Iterative Technique

When the dependence of the threshold voltage on the body bias (15) is used to determine the doping in the substrate of a MOSFET, the following iterative procedure, described in [14], can be employed. The initial guess for $2\phi_F = 0.6$ V is used to generate the plot of the measured V_T as a function of $\sqrt{-2\phi_F + V_{BS}}$. The slope γ of that straight line is used in (16) to find N_D. This value of N_D is in turn used to obtain a new value of ϕ_F from (3). A new plot of V_T versus $\sqrt{-2\phi_F + V_{BS}}$ can then be generated. The procedure is repeated until ϕ_F stops changing, which usually requires no more than two iterations.

The iterative procedure described above is possible because there is a known relationship between the result of any iteration and the guess used in the following iteration. The result of any iteration is ϕ_F; the guess for the following iteration is $2\phi_F$. If (18) is considered, no such iterative procedure appears feasible because the relationship between the potential ϕ_x and the Fermi potential ϕ_F is not known. Therefore, establishing this relationship is essential to constructing a fast iterative technique for determining the drain doping based on the exact analysis presented in the previous subsection.

Table II displays the values of the potential ϕ_x and the Fermi potential ϕ_F for the six power MOSFET device types whose drain dopings have been given in Table I. The values of these potentials for each device type were obtained by finding the average for the five devices of that type. The ratio of ϕ_x and ϕ_F for all device types is very close to 1.1; this establishes the relationship needed for the iteration procedure.

The fast iterative procedure based on the relationship $\phi_x = 1.1\phi_F$ is illustrated in Table III for the IRF440 power MOSFET used to generate Figs. 3 through 10. The choice of the initial value for ϕ_x is arbitrary; we have chosen $\phi_x = 0.5$ V which is a reasonable guess for common doping levels. Note that the correct doping is obtained after the first iteration; the second iteration is used to confirm that the procedure has been completed. This iterative technique, however, does not give a correct value of ϕ_x (the value listed in Table III is -0.27 V, while the correct value obtained from Fig. 10, and given in Table II is $\phi_x = -0.29$ V). The reason for this is the use of the approximation $\phi_x = 1.1\phi_F$, while from Table II the correct relation is $\phi_x = 1.16\phi_F$. In consequence of this approximation for ϕ_x, the flat-band voltage value determined from (18) may not be correct, because this equation contains ϕ_x.

TABLE III
ILLUSTRATION OF THE ITERATIVE TECHNIQUE FOR FINDING THE DRAIN DOPING DESCRIBED IN THE TEXT. THE MEASUREMENTS OF V_T WERE PERFORMED USING AN IRF440 POWER MOSFET

Iteration Number	ϕ_i [V]	γ [$V^{1/2}$]	Drain Doping [10^{14} cm^{-2}]	ϕ_F [V]	$\phi_i = 1.1\ \phi_F$ [V]
0	-0.5	0.266	2.1	-0.249	-0.274
1	-0.274	0.254	1.9	-0.247	-0.272
2	-0.272	0.254	1.9	-0.247	-0.272

IV. CONCLUSION

The leakage current of DMOS transistors is due to recombination-generation processes in the silicon bulk and at the silicon-silicon dioxide interface. The hump in the leakage current of DMOS devices has been explained on the basis of the gate-controlled diode theory. This hump is due to surface generation current of the gate-controlled diode formed by the base-drain p-n junction. The drain bias of the DMOS transistor is shown to have the same effect on the charge at the drain surface as the body bias in the conventional MOSFET. The body effect is used to develop a new method for determining the drain doping in DMOS transistors. This method has been illustrated by determining the drain doping for six different power MOSFET device types. This method gives the profile depth ideally suited for finding the relevant drain doping. In power MOSFET's which do not have a surface implant in the drain region, the method gives the doping in the epitaxial layer and in power MOSFETs in which an implant is used to reduce the on-resistance, the method gives the doping in this implanted layer. This method is nondestructive, and does not require special test structures. Since only electrical measurements are required, the method is equally applicable to wafer-level and packaged-device characterization.

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IV.G. Comparison of Termination Methods for Low-Voltage, Vertical Integrated Power Devices

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COMPARISON OF TERMINATION METHODS FOR LOW-VOLTAGE, VERTICAL INTEGRATED POWER DEVICES

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Abstract—The design issues associated with termination structures for low-voltage (200 V class), vertical, integrated power devices are described and contrasted with common design guidelines for high-voltage devices. A comparison of single field plate, two-level field plate, field ring, and field plate/field ring methods is presented. Performance criteria are breakdown voltage, manufacturability, oxide charge sensitivity, and area consumption. The combination field plate/field ring method is superior to the other methods unless extremely low area consumption is required. Extensive device simulations as well as experimental data confirm these conclusions.

1. INTRODUCTION

One of the problems faced by any power device designer is that of achieving high breakdown voltage. Termination structures are used around the periphery of the device to reduce the effects of junction curvature and thus raise the breakdown voltage to near its ideal, or parallel-plane value. The termination structure design issues for vertical, integrated power devices differ from those for discrete devices in several ways. First, the area consumed by the integrated power device is typically of major concern, and should be minimized. This reduction in area leads to a different potential distribution in the substrate and a lower breakdown voltage than in a discrete device[1]. Second, the source (or anode) contact must run over the isolation for the power device, which can severely limit the breakdown voltage of the device due to surface breakdown at the corner of isolation[2]. Third, since a contact must be made to the source (or anode) of the device anyway, it is natural to use the contact as a field plate termination structure. Fourth, the relatively high doping of the epitaxial region (typically greater than $10^{15}\,cm^{-3}$) means that oxide-charge sensitivity is inherently reduced[3]. Finally, the heavy epitaxial-layer doping coupled with the near-spherical geometry means that a substantial fraction of the applied voltage is dropped in the diffused side of the junction. This raises the maximum attainable breakdown voltage beyond the abrupt-junction parallel-plane limit[4–6], and alters the optimal placement of a single field-limiting ring.

In light of these considerations, four different termination methods are compared: single field plate, two-level field plate, field ring, and combination field plate/field ring. The comparisons are made in terms of breakdown voltage, manufacturability, oxide-charge sensitivity, and area consumption. The combination field plate/field ring structures are judged superior to the other methods, except when extremely low area consumption is required.

2. EXPERIMENTAL DEVICE STRUCTURE

A representative layout and cross-section of the devices studied in this work is shown in Fig. 1. Diodes were studied instead of DMOS devices to ensure that the observed breakdown voltage trends could be attributed entirely to the termination structure, and were not due to breakdown between adjacent DMOS cells[7]. These devices were fabricated in an oxide-isolated process that includes BJTs, CMOS transistors, power DMOS transistors, and power diodes[8]. It should be noted that although the fabricated devices were oxide-isolated, the conclusions and approach of this work apply equally well to junction-isolated devices. Relevant device parameters for the fabricated devices are shown in Table 1. Devices were fabricated with three different termination methods to facilitate a one-to-one comparison between the competing termination methods. The different termination methods are discussed in detail in subsequent sections. Results from approx. 25 devices with each type of termination method will be indicated on graphs with error bars.

3. UNTERMINATED JUNCTION BREAKDOWN VOLTAGE

It is useful to consider the effects of finite surface concentration and finite lateral dimensions on unterminated junction breakdown voltage, because both

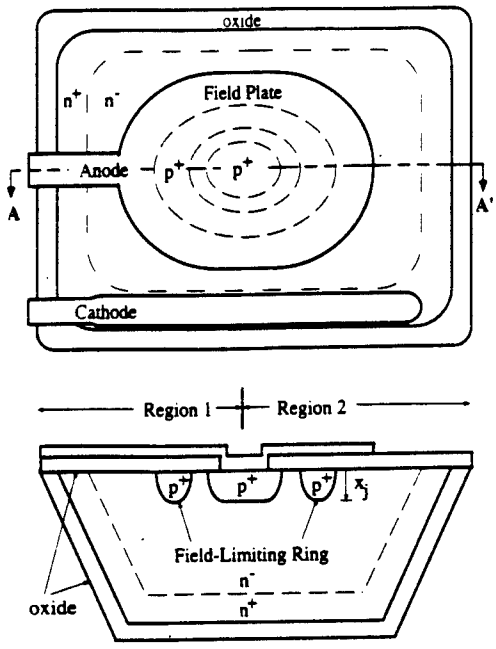


Fig. 1. Representative top and cross-sectional views of the devices studied in this work.

effects are important for low-voltage, integrated power devices. Figure 2 illustrates the definitions of lateral radius of curvature, R_m, and junction depth, x_j. In Fig. 3, 5-PISCES 2B-calculated breakdown voltages obtained from reverse I–V simulations of the device structure in Fig. 2 are plotted vs surface concentration of the diffusion. The impact ionization model used and the method of treating finite radius of lateral curvature, R_m, in the PISCES simulations are described in [9]. Three types of junctions are considered in Fig. 3: one-dimensional, or parallel-plane (very large x_j and R_m), cylindrical (very large R_m but finite x_j), and composite (finite R_m and x_j) junctions. The values of x_j, R_m, and N_{epi} used in the simulations are taken from Table 1 and correspond to the fabricated devices. The values of BV_{PP} and BV_{jcn} that appear in Table 1 are indicated in Fig. 3. The one-dimensional depletion-layer width at breakdown, W_{PP} in Table 1, was calculated as:

$$W_{PP} = \sqrt{\frac{2\epsilon_{Si} BV_{PP}}{qN_{epi}}}, \quad (1)$$

Table 1. Values and symbol conventions for fabricated device parameters

Device parameter	Symbol	Value
Junction depth	x_j	6.4 μm
Lateral radius	R_m	3 μm
Oxide thickness	t_{ox}	1 and/or 2.5 μm
Surface concentration of diffusion	N_s	2×10^{17} cm^{-3}
Anode to ring spacing	y_{AR}	6 or 9 μm
Width of ring diffusion window	y_{DR}	3 μm
Epi doping	N_{epi}	1.1×10^{15} cm^{-3}
Epi thickness	x_{epi}	20 μm
Junction breakdown voltage	BV_{jcn}	170 V
Ideal breakdown voltage	BV_{PP}	320 V
Depletion region width at BV_{PP}	W_{PP}	19 μm

where ϵ_{Si} is the permittivity of silicon and q is the magnitude of the electronic charge. Note that BV_{PP} is much larger than would be calculated by assuming abrupt, one-sided junctions and an approximation to the ionization integral[10]. The difference is due to the large potential drop on the diffused side of the junction.

From Fig. 3, it is seen that the breakdown voltage decreases with increasing N_s for all three junctions, reaching the abrupt limit for very large values of N_s. Also, the breakdown voltage of the composite junction is much lower than the cylindrical junction, which underscores the importance of taking the finite R_m into account in the PISCES simulations.

4. SIMULATION APPROACH

Figure 4 illustrates the dependence of breakdown voltage on oxide thickness, t_{ox}, at key locations in the device. There are three points in the device where breakdown may occur. These points are referred to in the text by letters A, B and C and in Fig. 4 by symbols ■, ▲, and ●, respectively. Points A and B represent surface breakdown, and should be avoided because of reliability issues[11]. Point C is where nondestructive bulk junction breakdown occurs. The termination structure for the device must avoid breakdown at points A and B, while providing the highest possible breakdown voltage at point C. The breakdown voltage of the complete device is the minimum of the breakdown voltages at points A, B and C.

In Figs 1 and 4, the device is shown divided into regions 1 and 2. In region 1, the anode metallization extends over the isolation oxide, while in region 2 the metallization ends before reaching this point. These two regions must both be considered when designing and comparing termination structures for integrated power devices. In the analysis that follows, regions 1 and 2 will be studied separately, and the results will be combined to yield the results for the entire device. This approach is taken for two reasons. First, it clarifies the interaction between the two regions of the device and the characteristics of each. Second, region 1 is best modeled by rectangular coordinates (two-dimensional simulation), while region 2 is best modeled with cylindrical coordinates (quasi-three dimensional simulation). Since coordinate systems cannot be mixed in PISCES, separation into two regions is necessary for accurate results. Finally, breakdown in region 1 is allowed to occur *only* at point B, while breakdown in region 2 may occur at either point A or C.

5. BREAKDOWN VOLTAGE COMPARISON

5.1. *Single-level field plate*

First, consider the simplest possible termination structure for the devices in this study: a single-level field plate (FP) structure. The FP structure is fabricated by simply extending the anode metallization

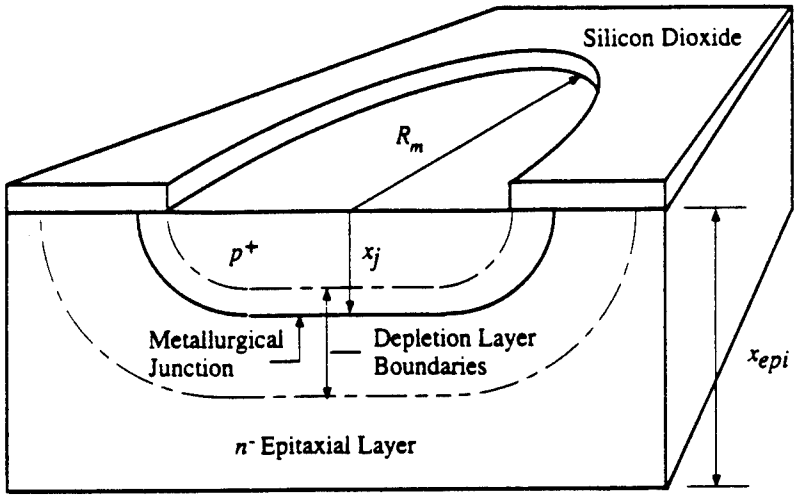


Fig. 2. Illustration of junction depth x_j, lateral radius R_m, and epitaxial layer thickness x_{epi}.

over the field oxide around the anode. The optimum field plate length was determined from simulations to be about 70% of the depletion region thickness at the ideal breakdown voltage, W_{PP}, as suggested in [12], or $0.7\ W_{PP} = 11\ \mu$m for these devices. The only variable is oxide thickness, t_{ox}. In Fig. 4, normalized breakdown voltage, BV/BV_{PP}, is plotted vs t_{ox} for both regions 1 and 2. The graph symbols correspond to the points in the device where breakdown occurs.

Four oxide thicknesses are important in the following discussion, and they are labeled t_{ox1}, t_{ox2}, t_{ox3}, and t_{ox4} in Fig. 4. In region 1, the BV vs t_{ox} characteristic is linear, while in region 2, the characteristic exhibits a maximum at $t_{ox1} = 0.4\ \mu$m. In region 1, the results are shown only up to $t_{ox3} = 1.8\ \mu$m, because breakdown in region 2 limits the breakdown voltage of the entire device to be less than or equal to BV_{PP}.

The optimum oxide thickness for region 2 is $t_{ox1} = 0.4\ \mu$m, which would be the optimal choice for a discrete device. However, this oxide thickness in region 1 yields an unacceptably low surface breakdown voltage at point B of 35% of the ideal breakdown voltage ($0.35\ BV_{PP} = 112$ V). When both regions 1 and 2 are considered, the optimal oxide thickness for the single-level field plate structure is $t_{ox2} = 1.0\ \mu$m, since that is the smallest oxide thickness for which breakdown occurs at point C. However, the breakdown voltage at t_{ox2} is only $0.7\ BV_{PP} = 225$ V.

5.2. Avoiding surface breakdown

In general, termination structure design for the device structure in Fig. 1 consists of ensuring that breakdown at point B is avoided by making the oxide sufficiently thick. This places a constraint on the termination structure design in region 2 that does not exist for discrete devices. For example, if a termination structure were employed to raise the breakdown voltage of the device beyond that obtainable with a

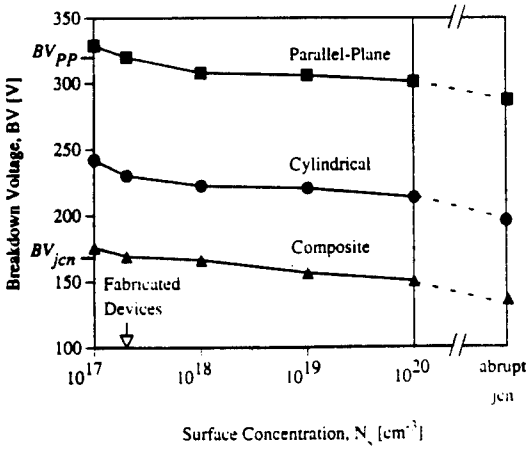


Fig. 3. PISCES-simulated breakdown voltage vs surface concentration of the diffusion for parallel-plane, cylindrical, and composite junctions.

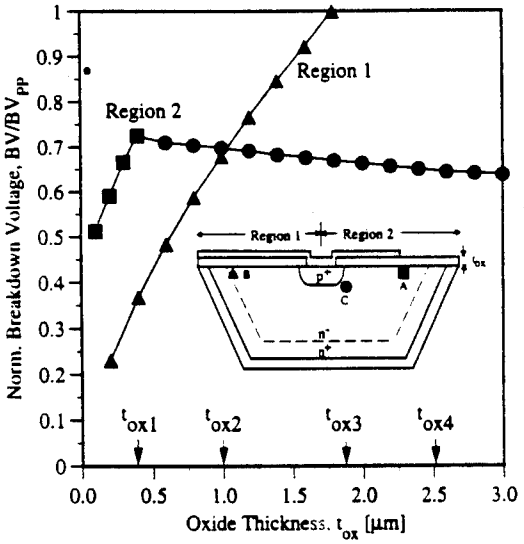


Fig. 4. Normalized breakdown voltage vs oxide thickness for regions 1 and 2. Graph symbols correspond to breakdown points within the device: A = ■, B = ▲, C = ●.

single-level field plate, the oxide thickness at point B must still be large enough to avoid premature breakdown at point B. As a limiting case, if the termination structure could achieve ideal breakdown voltage in region 2, then t_{ox} must be larger than $t_{ox3} = 1.8\ \mu m$ in region 1 to avoid surface breakdown at point B. In all the fabricated devices, surface breakdown was avoided because $t_{ox} = t_{ox4} = 2.5\ \mu m$.

It should be noted that the surface breakdown problem at point B could be addressed with a field reduction region[13] or floating metal field rings[2]. This approach was not taken in this work. If one of these techniques were employed, it would merely increase the slope of the breakdown voltage vs oxide thickness characteristic at point B, reducing the value of t_{ox3}. The design issues associated with the termination for the device would be unchanged.

5.3. Two-level field plate

To improve the breakdown voltage of a single-level field plate device, two-level field plate (2FP) structures are often used [13,14]. A representative cross-section of a 2FP structure is shown in Fig. 5. These structures are relatively simple to fabricate, since two levels of interconnection almost always exist in a power integrated circuit. The lower level of interconnection is used as the lower field plate. Layout and processing considerations other than device breakdown voltage may dictate the oxide thickness under the first level of interconnect, t_{oxl}, but this fact is ignored in the following analysis. The oxide thickness under the lower FP is treated as a free parameter.

The oxide thickness under the upper FP, t_{oxu}, is not a free parameter; it must be larger than $t_{ox3} = 1.8\ \mu m$ to avoid surface breakdown at point B. For the simulations, t_{oxu} was taken to be $t_{ox4} = 2.5\ \mu m$, since this is the thickness used in the fabricated devices. The lower field plate length, y_{fpl}, was $0.7\ W_{PP} = 11\ \mu m$, and the upper plate length, y_{fpu}, was $5\ \mu m$. These choices represent reasonable tradeoffs between field plate length and breakdown voltage, and are similar to the fabricated device dimensions. The oxide thickness under the lower FP was then varied in the simulations with fixed t_{oxu}. It was found

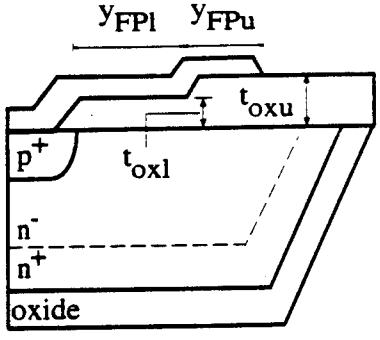


Fig. 5. Representative cross-sectional view of a two-level field plate structure.

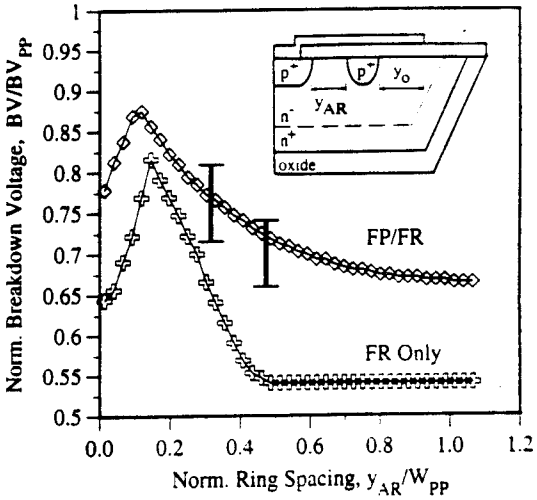


Fig. 6. Normalized breakdown voltage vs normalized ring spacing for field ring only and field plate/field ring devices. Experimental data from 25 devices at each spacing are indicated with error bars.

that the optimal oxide thickness for the lower FP was $0.4\ \mu m$, achieving a breakdown voltage of $0.74\ BV_{PP} = 236\ V$.

5.4. Field plate/field ring

By combining FP structures with field ring (FR) structures, hybrid FP/FR structures are obtained. Hybrid structures have received recent attention in the literature[15,16], and superior performance has been reported over field plate and field ring only techniques. Running a field plate that is at the potential of the anode directly over a field ring, however, is discouraged in [17]. The reason cited is that since the FR technique relies on punchthrough between adjacent rings to achieve high breakdown voltage, any distortion of the surface potential by a field plate would reduce the effectiveness of the structure.

The present work indicates that, in fact, a field plate directly over a field ring is an effective termination method. Since the field ring is diffused in the same processing step as the anode, the FP/FR structure requires no extra processing steps when compared to a field plate or a field ring structure. In Fig. 6, normalized breakdown voltage BV/BV_{PP} vs normalized anode-ring spacing y_{AR}/W_{PP} is shown for FP/FR and FR only structures. Experimental data taken from 25 FP/FR devices at two values of y_{AR} is shown with error bars. The simulation results for FR-only structures are included merely for comparison with FP/FR structures.

The FP/FR structure reduces the sensitivity of breakdown voltage to ring spacing when compared to a FR-only structure, and always achieves higher breakdown voltage than a FR-only structure with the same y_{AR}. In addition, the breakdown voltage of the FP/FR structure will never fall below the breakdown voltage set by the oxide thickness under the field

plate. Thus, the FP/FR structure guarantees a higher breakdown voltage than the corresponding field plate or field ring only structure, no matter where the field ring is placed. Thus, FP/FR structures are extremely easy to manufacture. Simulations indicate that the optimal FP/FR structure achieves a breakdown voltage of $0.88\,BV_{PP} = 281$ V which is significantly larger than that obtainable with either a field plate or a field ring only structure.

Note from Fig. 6 that the optimal ring spacing is about $0.12\,W_{PP} = 2.25$ μm. This is slightly less than the optimal ring spacing without the field plate, and much less than the often quoted design rule that says the optimal ring spacing should be $0.25\,W_{PP} = 4.75$ μm[17,18]. The difference in the optimal ring spacings for these devices is a result of their small area and relatively low surface concentration of the diffusion, as discussed in Section 3.

In Fig. 7, normalized breakdown voltage and optimal ring spacing are plotted vs oxide thickness. Possible surface breakdown at point B was not considered in this figure. The optimal ring spacing does not change with oxide thickness, although the breakdown voltage decreases with increasing oxide thickness. Thus, if the ring is correctly placed, small changes in oxide thickness will not substantially affect the breakdown voltage, which further enhances the manufacturability of the FP/FR structure. Also plotted for reference in Fig. 7 are simulation results for the FR-only device.

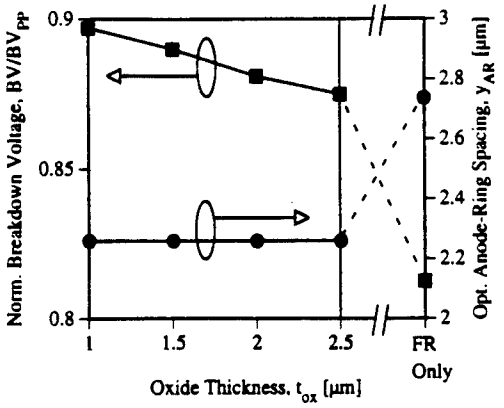


Fig. 7. Normalized breakdown voltage and optimal anode-ring spacing vs oxide thickness.

6. OTHER COMPARISONS

6.1. Oxide charge sensitivity

The breakdown voltage of power devices with n-type epitaxial regions degrades when positive oxide-trapped charge, N_{ot}, is introduced into the oxide[17]. This charge can arise from device processing[15] or from ionizing radiation[19]. It is thus of interest to examine the breakdown voltage sensitivity of the different termination structures to oxide charge. In Fig. 8, normalized breakdown voltage

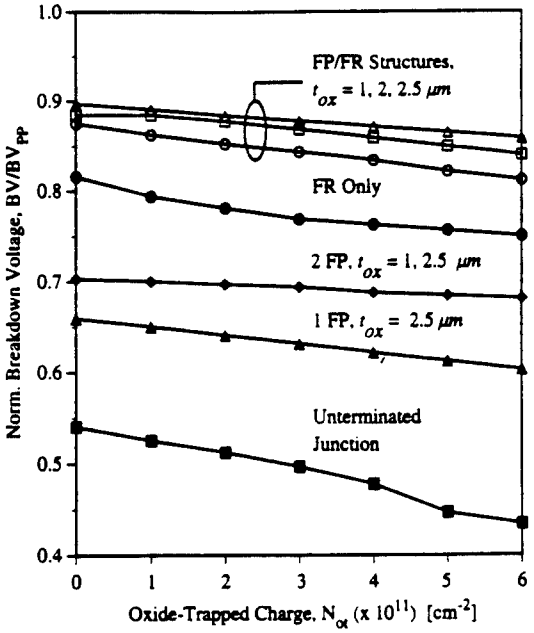


Fig. 8. Normalized breakdown voltage vs oxide-trapped charge for the termination structures described in the text.

obtained from S-PISCES 2B simulations is plotted vs N_{ot} for the structures discussed above. Several trends are apparent. First, the breakdown voltage degradation decreases with decreasing oxide thickness for both FP and FP/FR structures. This is because with thinner oxides, the field plate influences the surface potential more strongly. Charge in the oxide thus has less of an effect on the surface potential. Second, the FP/FR and FR-only structures have higher breakdown voltage than the field plate structures for all values of N_{ot}. One of the main drawbacks of FR-only structures in high-voltage devices is the sensitivity of breakdown voltage to oxide charge, as pointed out by many authors[15,20,21]. However, all of these studies have focused on high-voltage devices with lightly-doped epitaxial layers. In the devices studied in this work, N_{epi} is large enough that the presence of N_{ot} has relatively little effect on the breakdown voltage.

6.2. Area consumption

Area consumption is a prime concern for integrated power devices. Indeed, the termination structure that yields the highest breakdown voltage may not be optimal for the device if the area consumption is excessive. For the purpose of comparison, the area of the termination structure is defined as $\text{Area}_{TS} = \pi R_{TS}^2$, where R_{TS} is the radius of the termination structure measured from the center of the diffused anode. In Fig. 9, the normalized breakdown voltage BV/BV_{PP} for the termination methods studied in this work is plotted vs the normalized area of the termination structure $\text{Area}_{TS}/\text{Area}_{jcn}$. Again, error bars indicate the range of experimental data.

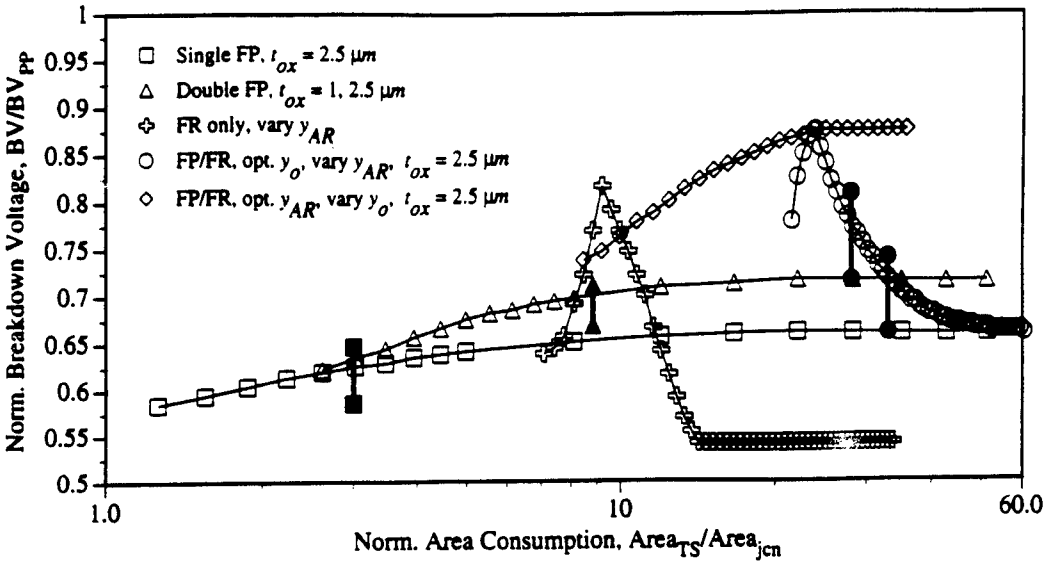


Fig. 9. Normalized breakdown voltage vs normalized area consumption for the devices investigated in this work. Error bars indicate the range of experimental data from 25 devices of each type.

The symbols on the ends of the error bars correspond to the symbols for the simulation results.

Since single and two-level field plate structures can be fabricated with any field plate length, the area consumed by a field plate structure can be freely chosen by the designer. For extremely low area consumption, the field plate technique is the best approach.

If higher breakdown voltage is desired at the expense of slightly more area consumption, then a combination field plate/field ring structure can be used. The FP/FR structure has a minimum area set by the requirement that the FR spacing y_{AR} be larger than zero. However, the area consumed by the optimal FP/FR structure is nearly the same as that consumed by the optimal 2FP structure. Note also that the area of the FP/FR structure can be varied in two ways. The FR spacing y_{AR} can be varied with a fixed overlap y_0, or the overlap y_0 can be varied with a fixed y_{AR}. Both cases are shown in Fig. 9. By varying the overlap y_0 with an optimally-placed field ring, the power device designer can obtain additional voltage handling capability at the expense of additional area consumption.

7. SUMMARY

The issues associated with termination structure design for vertical, integrated power devices were defined. The interaction of the oxide thickness running over the device isolation and the breakdown voltage of the device was explored. In light of these constraints, a comparison of single field plate, two-level field plate, field ring only, and combination field plate/field ring termination structures was performed. Combination field plate/field ring structures were seen to provide significantly higher breakdown voltage than other structures while consuming little additional area. The simple fabrication and design constraints for combination field plate/field ring termination structures make them attractive options for integrated as well as discrete power devices.

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IV.H. Evaluation of a Method for Estimating Low-Dose-Rate Irradiation Response of MOSFETs

Evaluation of a Method for Estimating Low-Dose-Rate Irradiation Response of MOSFETs‡

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Abstract

A simple method for estimating the threshold-voltage shift due to low-dose-rate ionizing irradiation was recently proposed for power MOSFETs. In this work, the physical considerations governing the applicability of the method are examined. In addition to the power MOSFETs discussed in the previous paper, the method is applied to integrated MOSFETs from two different technologies and critically evaluated. For this method to work, the oxide trapped charge due to low-dose-rate irradiation should be the same as that following irradiation at the dose rates specified in MIL-STD-883D Method 1019.4, and the interface-trap density following low-dose-rate irradiation should be the same as that following irradiation at 1019.4 rates and subsequent high-temperature annealing. Of the two integrated technologies evaluated, the method correctly predicts the low-dose-rate threshold-voltage shift for one, but not for the other. In the case where the method yields the correct result, the agreement appears to be coincidental. The results, coupled with the necessity for transistor-level test structures, suggests that the proposed method is applicable primarily to power MOSFETs that exhibit slow annealing of oxide-trapped charge and no rebound during low-dose-rate irradiation.

I. INTRODUCTION

Space applications of MOS devices require knowledge of the behavior of these devices when exposed to low-dose-rate ionizing radiation typical of natural space. There has been considerable work on the effects of ionizing radiation on MOS devices and a number of reviews are available [1-3]. Since characterizing the effects of low-dose-rate ionizing radiation on MOS devices can be time consuming and expensive, much of the work characterizing the effects of ionizing radiation on MOS devices has been done at the high dose rates normally available for laboratory experimentation [4-8].

A new method for estimating the low-dose-rate threshold-voltage shift in power MOSFETs was recently proposed [9], which is an attempt to exploit information acquired during irradiations and anneals per MIL-STD Test Method 1019.4 [10] to estimate low-dose-rate response. Briefly, the method consists of estimating the low-dose-rate threshold voltage shift by summing the threshold shift due to oxide trapped charge (ΔV_{ot}) immediately after irradiation and the shift due to interface trapped charge (ΔV_{it}) following irradiation and annealing at 100° C.

While the previous paper showed good agreement between the predictions of this method and actual low-dose-rate irradiation, it did not examine multiple technologies, nor discuss the physical considerations that determine the applicability of the method. This paper critically examines this new method for estimating the low-dose-rate radiation response of power MOSFETs for a range of total-dose exposures and also applies the method to two integrated MOS technologies. The background information and assumptions underlying the method are clarified. The results, coupled with the necessity for transistor-level test structures, suggest that the proposed method is applicable primarily to power MOSFETs that exhibit slow annealing of oxide-trapped charge and no rebound during low-dose-rate irradiation.

II. EXPERIMENTAL DETAILS

The device types used in this study were IRF150 power MOSFETs manufactured by International Rectifier (wafer lot# 6U1G) [9], nMOS transistors manufactured by the SNL Center for Radiation Hardened Microelectronics in the 4/3 μm process (SNL Lot # G1916A; wafer 22; 32-nm oxide; W = 16 μm; L = 3μm) [11], and n-channel transistors from Honeywell (RICMOS development lot; 25-nm oxide; W = 25μm; L = 2.5 μm) [12].

Standard transistor threshold-voltage and subthreshold current-voltage measurements were performed at room temperature

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using an HP4145B semiconductor parameter analyzer. The threshold voltage is defined as the voltage-axis intercept of the square root of the drain current versus gate voltage in saturation. The threshold-voltage shift due to oxide-trapped charge, ΔV_{ot}, and that due to interface-trapped charge, ΔV_{it}, were determined using the subthreshold charge separation technique of McWhorter and Winokur [13]. No attempt was made to separate effects of interface-traps and "border traps" [14,15] in this study.

For the radiation exposures, the gates of the International Rectifier power MOSFETs, Sandia transistors, and Honeywell transistors were biased at +9V, +6V, and +5V, respectively, during irradiation and anneal. The sources and drains of all devices were grounded during both irradiation and anneal, and the oxide field in all devices was approximately 1 MV/cm for power MOSFETs and 2 MV/cm for Sandia and Honeywell transistors. Additional details of the radiation exposures and anneals are given below.

II.A. *International Rectifier Power nMOSFETs*

The irradiations were performed at two different dose rates in Co-60 sources. Twenty devices were irradiated at a high dose rate (150 rad(SiO_2)/s). Thirteen devices were irradiated at a low dose rate (3.6×10^{-4} rad(SiO_2)/s). All irradiations were performed at room temperature. The maximum total dose for the low-dose-rate irradiation was 11.8 krad(SiO_2). The total doses for the high-dose-rate irradiation were 6, 9, and 11.8 krad(SiO_2). Following high-dose-rate irradiation, devices were annealed for 168 hours at 100°C [9-12]. The data displayed for each experiment are the average of all devices tested. Standard deviations are typically too small to be visible on the plots.

II.B. *Sandia nMOS transistors*

A total of six devices was irradiated; three at a low dose rate and three at a high dose rate. The low-dose-rate irradiation was performed in a Cs-137 source at a dose rate of 0.17 rad(SiO_2)/s to a total dose of 500 krad(SiO_2). The high-dose-rate irradiation was performed in a Co-60 source at 400 rad(SiO_2)/s to a total dose of 300 krad(SiO_2). Following the high-dose-rate irradiation, one group of devices was annealed for 168 hours at 100°C. Device-to-device response varied by less than ±5% [11].

II.C. *Honeywell nMOS transistors*

Four devices were irradiated in Co-60 sources. Two were irradiated at a high dose rate (240 rad(SiO_2)/s) to a total dose of 2000 krad(SiO_2). Two devices were irradiated at a low dose rate (4.7 rad(SiO_2)/s) to a total dose of 2000 krad(SiO_2). Following the high-dose-rate irradiation, devices were annealed for 168 hours at 100°C. Device-to-device response varied by less than ±5% [12].

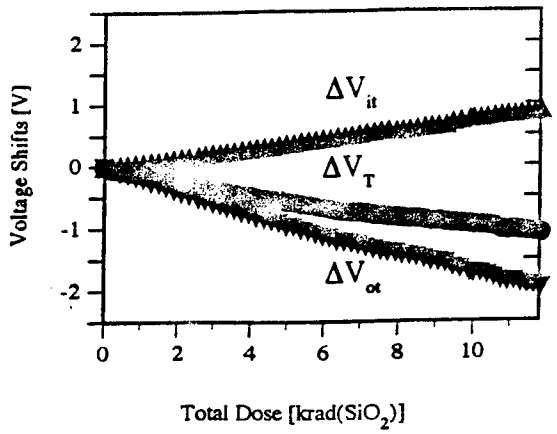


Fig. 1 Threshold-voltage shifts (ΔV_T) and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) for IRF150 power MOSFETs irradiated at the low dose rate.

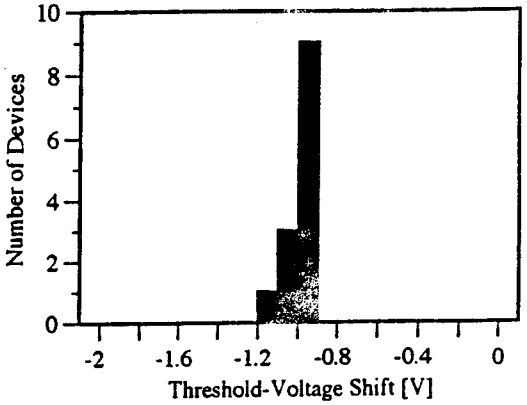


Fig. 2 Histogram of the threshold-voltage shift for low-dose-rate irradiation at a total dose of 11.8 krad(SiO_2).

III. RESULTS

III.A. *International Rectifier Power nMOSFETs*

Figure 1 shows the threshold-voltage shifts and contributions of oxide-trapped charge and interface-trapped charge to these shifts. The densities of interface-trapped charge and oxide-trapped charge increase almost monotonically. Figure 1 illustrates that the buildup of both oxide-trapped charge and interface-trapped charge is large in these devices, which results in a smaller net threshold-voltage shift. Figure 2 shows a histogram of the threshold-voltage shifts at 11.8 krad(SiO_2) indicating that the part-to-part variation in the threshold-voltage shift is relatively small.

Figures 3(a) - (c) show threshold-voltage shifts for high-dose-rate irradiation at 6, 9, and 11.8 krad(SiO_2) followed by high-temperature anneal at 100°C for 168 hours. From these figures, it is observed that there is a large buildup of oxide-trapped charge during irradiation which contributes to the large shift in the threshold voltage. During anneal, there is a reduction in the density of oxide-trapped charge, but the inferred interface-trapped charge density first increases rapidly in the first few

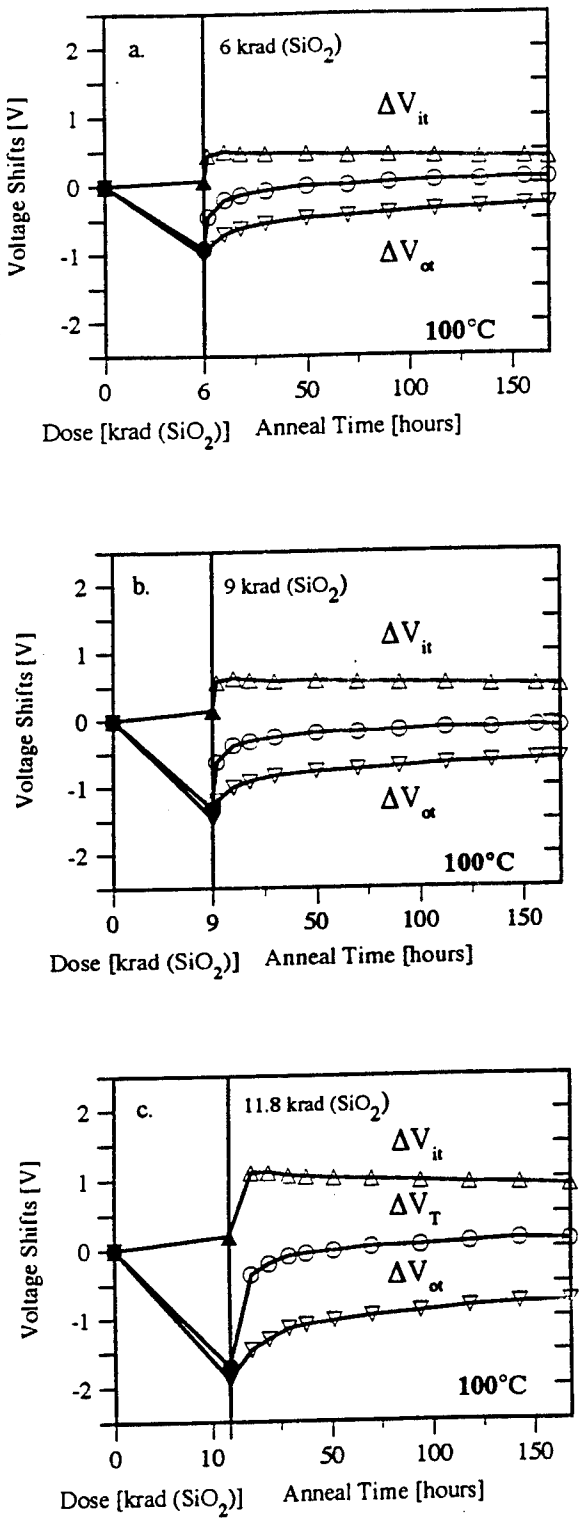


Fig. 3 Threshold-voltage shifts (ΔV_T) and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) for IRF150 power MOSFETs irradiated at high dose rate followed by anneal at 100°C for a) 6 krad(SiO_2), b) 9 krad(SiO_2), c) 12 krad(SiO_2) doses.

hours of the anneal, and then decreases slowly. A decrease in ΔV_{it} at 100°C does not necessarily imply a decrease in the density of interface traps, but may indicate the presence of border traps [14-16]. The density of the oxide-trapped charge decreases monotonically during the entire anneal time.

Figures 4 and 5 show contributions of oxide-trapped charge and interface-trapped charge to the threshold-voltage shift for low-dose-rate irradiation and high-dose-rate irradiation. Figure 4 illustrates that ΔV_{ot} for the low-dose-rate irradiation is approximated by ΔV_{ot} following the high-dose-rate irradiation. This near equality is consistent with the slow room-temperature annealing rate for trapped holes in these devices. Similarly, ΔV_{it} for the low-dose-rate irradiation is approximated by ΔV_{it} following high-dose-rate irradiation plus 100°C anneal (Fig. 5).

III.B. *Sandia nMOS transistors*

Figure 6a shows the threshold-voltage shifts for the Sandia transistors irradiated at the low dose rate (0.17 rad(SiO_2)/s) [11]. The contributions of interface-trapped charge to the threshold voltage shift are larger than the contributions of the oxide-trapped charge. This causes the threshold shift to be positive. Figure 6b shows the threshold-voltage shifts for Sandia transistors irradiated at the high dose rate (400 rad(SiO_2)/s). During irradiation there is a larger buildup of oxide-trapped charge than for the low-dose-rate case, as expected for these devices [6,8,11]. High-temperature anneal increases the density of interface-trapped charge.

III.C. *Honeywell nMOS transistors*

Figure 7a shows the threshold-voltage shifts for the Honeywell transistors irradiated at the low dose rate [12]. The buildup of both ΔV_{ot} and ΔV_{it} during low-dose-rate irradiation is small, which leads to a small shift in the threshold voltage. Figure 7b shows the threshold-voltage shifts for Honeywell parts irradiated at a high dose rate and annealed at 100°C for 168 hours. Here, the density of interface-trapped charge remains relatively constant during annealing, and may even decrease slightly.

IV. DISCUSSION

In the power MOSFETs tested here (as well as other commercial power MOSFETs that were tested), no rebound is observed; the failure mechanism is reduction of the threshold voltage due to oxide-trapped charge. Method 1019.4 provides a bound for this failure mechanism, but Fig. 8 illustrates that the actual threshold-voltage shift at low dose rates is less than this bound. This may lead to rejection of parts that will function well in a space environment [9, 17]. It would be valuable to obtain a better estimate of the low dose rate threshold-voltage shift to effectively select parts for space applications.

For the power MOSFETs tested here, ΔV_{ot} resulting from the low-dose-rate irradiation is approximately the same as that following high-dose-rate irradiation, as shown in Fig. 4. Similarly,

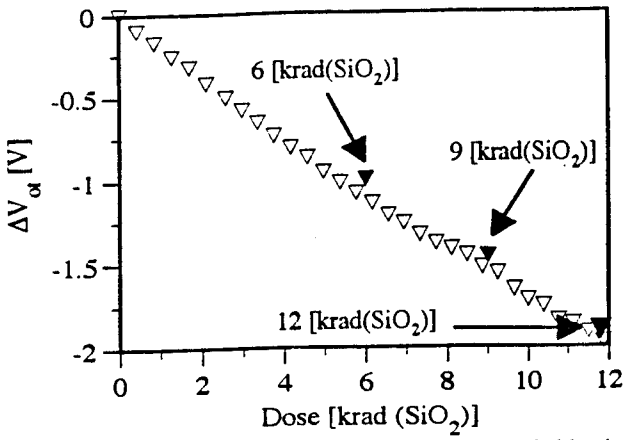


Fig. 4 Contributions of oxide-trapped charge to the threshold-voltage shift of the IRF power MOSFETs for high-dose-rate irradiation at 150 rad(SiO_2)/s (closed symbols), and low-dose-rate irradiation at 3.6×10^{-4} rad(SiO_2)/s (open symbols).

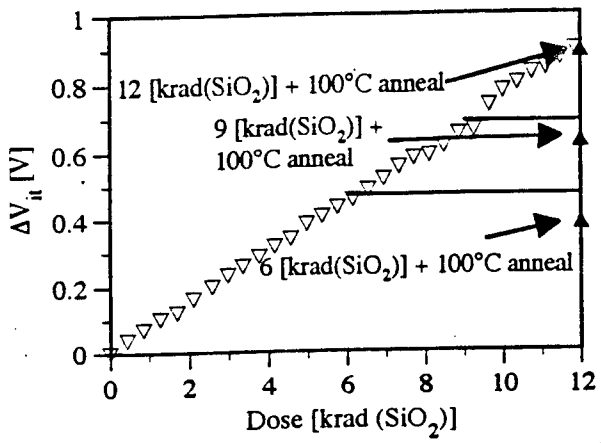
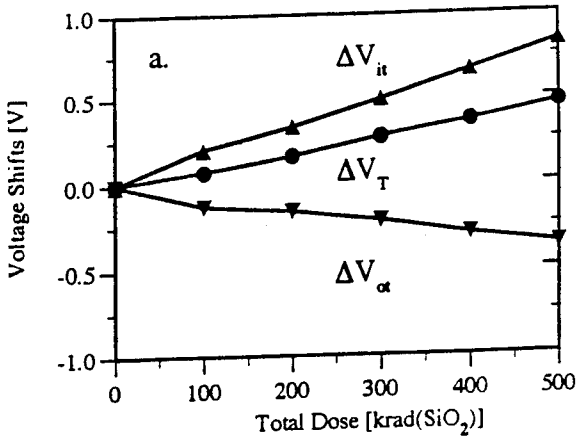


Fig. 5 Contributions of interface-trapped charge to the threshold-voltage shift of the IRF power MOSFETs for high dose rate irradiation (closed symbols) followed by anneal at 100°C for 168 hours, and for low-dose-rate irradiation (open symbols). The solid lines represent the value of ΔV_{it} at 6, 9 and 12 krad(Si) for low-dose-rate irradiation.



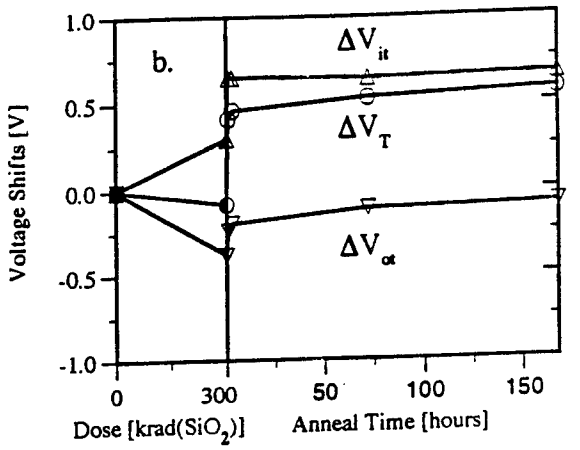


Fig. 6 Threshold-voltage shifts (ΔV_T) and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) for Sandia transistors irradiated at a) low dose rate to 500 krad(SiO_2), and b) high dose rate to 300 krad(SiO_2), followed by anneal at 100°C for 168 hours.

ΔV_{it} following low-dose-rate irradiation is approximately the same as that resulting from high-dose-rate irradiation followed by high-temperature annealing, as shown in Fig. 5. This suggests that, for these devices, a good estimate for the threshold-voltage shift resulting from the low-dose-rate irradiation can be obtained by adding ΔV_{ot} at the end of the high-dose-rate irradiation and ΔV_{it} at the end of the high-temperature anneal. In this case, the actual threshold-voltage shift at low-dose-rates can be estimated from the following equation, where ΔV_{ot} is obtained immediately after irradiation and ΔV_{it} is obtained following the high-temperature anneal [9]:

$$\Delta V_T(\text{LDR}) = \Delta V_{ot}(\text{HDR}) + \Delta V_{it}(\text{HDR} + 100°\text{C anneal}). \quad (1)$$

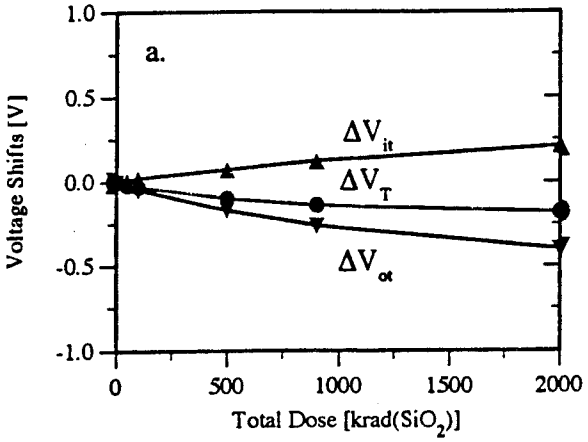
Table 1 demonstrates the application of this method to the data of Fig. 3 to estimate the threshold-voltage shift at doses of 6, 9 and 11.8 krad(SiO_2). Figure 9 plots the threshold-voltage shift vs. total dose and allows comparison with the predicted values from eq. (1). This figure shows that this method accurately estimates the threshold-voltage shift due to low-dose-rate ionizing radiation for these power MOSFETs. In these devices, rebound was not observed. This method is <u>not</u> appropriate for devices in which rebound occurs, for reasons discussed in Appendix A.

Equation (1) was also tested for the Sandia and Honeywell transistors. Table 2 and Figure 10 illustrate the application of eq. (1) to Sandia and Honeywell transistors. Figure 10a shows that eq. (1) produces an accurate estimate of the low-dose-rate threshold-voltage shift for the Sandia transistors at the dose rate shown; while for the Honeywell devices, the threshold-voltage shift is overestimated.

It is worthwhile to understand why the proposed method works for some device types, but not for others. For this method to work as intended, the oxide-trapped charge due to low-dose-

Table 1: The threshold-voltage shift for power MOSFETs at three different total doses.

Total Dose [krad(SiO_2)]	ΔV_{ot}(HDR)	ΔV_{it}(HDR + 100° C)	LDR ΔV_T(Estimated)	LDR ΔV_T(Measured)	% Error
6	-1	0.39	-0.61	-0.67	8.5
9	-1.47	0.49	-0.98	-0.89	10
11.8	-1.9	0.89	-1.01	-1.08	6.3



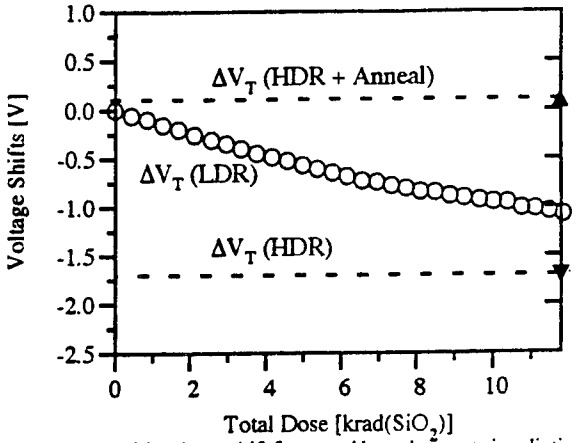


Fig. 8 Threshold-voltage shift for actual low-dose-rate irradiation (open symbols), and upper bound and lower bound at 12 krad(SiO_2) set by Method 1019.4 for power MOSFETs [9].

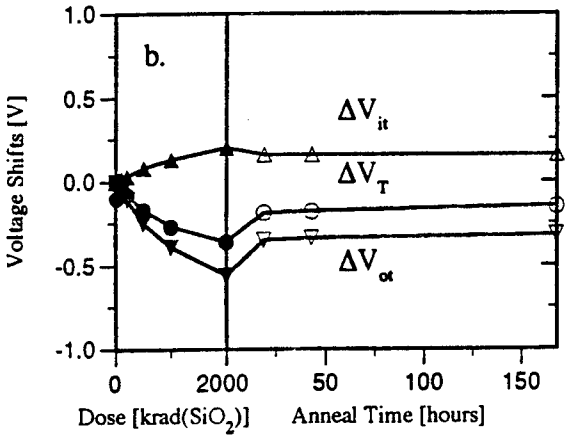


Fig. 7 Threshold-voltage shifts (ΔV_T) and contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) for Honeywell transistors irradiated at: a) low dose rate to 2000 krad(SiO_2), and b) high dose rate to 2000 krad(SiO_2), followed by anneal at 100°C for 168 hours.

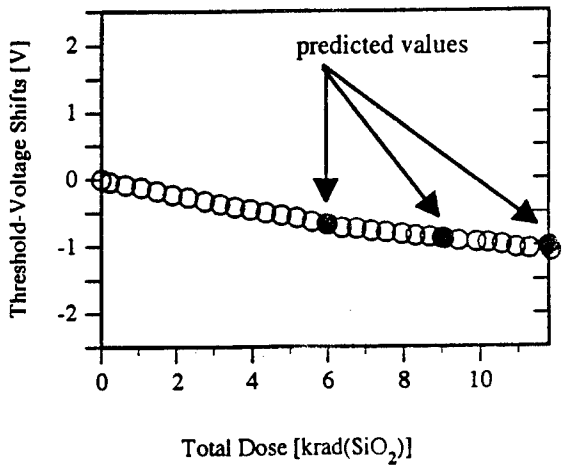


Fig. 9 Threshold-voltage shift for low-dose-rate irradiation (open symbols), and predicted threshold-voltage shifts (closed symbols).

rate irradiation should be the same as that following irradiation at the dose rates specified in MIL-STD-883D Method 1019.4, and the interface-trap density following low-dose-rate irradiation should be the same as that following irradiation at 1019.4 rates and subsequent annealing. In the case of the power MOSFETs, both of these assumptions are satisfied. In particular, the relatively thick gate oxide used in these power MOSFETs (approximately 100 nm) does not exhibit much annealing at room

Table 2: Threshold-voltage shifts for Sandia and Honeywell devices.

Device types	ΔV_{ot} (HDR)	ΔV_{it} (HDR + 100°C anneal)	ΔV_{ot} (LDR)	ΔV_{it} (LDR)	LDR ΔV_T (Estimated)	LDR ΔV_T (Measured)	% error
Sandia	-0.38	0.66	-0.22	0.49	0.28	0.27	4
Honeywell	-0.56	0.16	-0.4	0.21	-0.4	-0.18	122

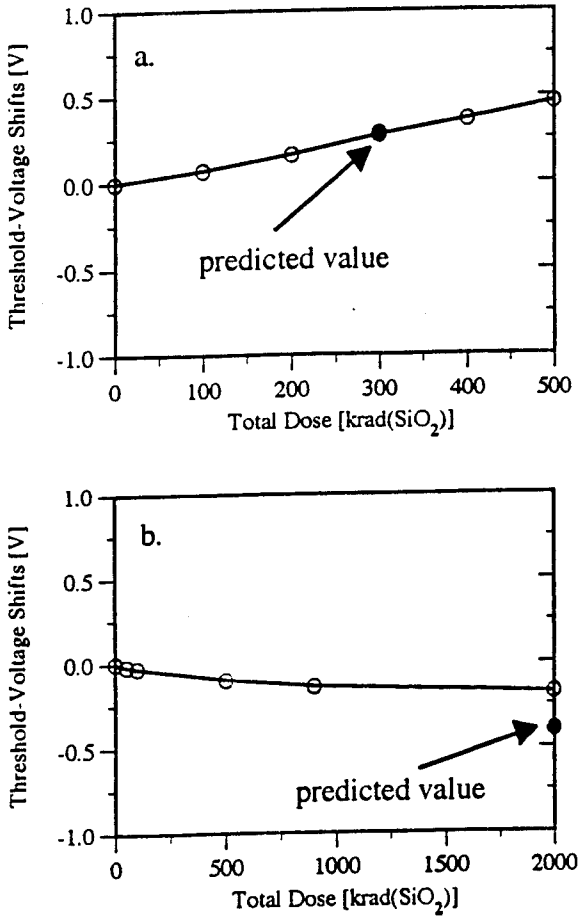


Fig. 10 Threshold-voltage shift (ΔV_T) for the low-dose rate irradiation (open symbols) and predicted threshold-voltage shift for (a) Sandia devices, and (b) Honeywell devices.

temperature, so the oxide-charge densities following irradiation at the different dose rates are approximately equal.

For the Sandia transistors neither of these assumptions is very accurate, as indicated in Table 2. Here, ΔV_{ot}(HDR) exceeds ΔV_{ot}(LDR) by 73% in magnitude, and ΔV_{it}(HDR + 100°C anneal) exceeds ΔV_{it}(LDR) by 35%. However, at the particular low dose rate used, the algebraic errors in estimating ΔV_{ot} and ΔV_{it} approximately balance each other, fortuitously producing an accurate estimate of ΔV_T. If another dose rate had been used for the low-dose-rate experiment involving the Sandia parts [6,11], the agreement would not have been as good. The threshold-voltage estimate for the Honeywell transistors is not very accurate because there is significant annealing of the oxide charge during the low-dose-rate irradiation (ΔV_{ot}(HDR) exceeds ΔV_{ot}(LDR) by 40% in magnitude), while there is a decrease in interface-trap density during the high-temperature anneal (ΔV_{it}(HDR + 100°C anneal) is less than ΔV_{it}(LDR) by 24%). This leads to an overestimation of the threshold-voltage shift. It is possible to assess the error made by using eq. (1) in some simple model cases. A more rigorous treatment of eq. (1) is included in appendix A.

IV. CONCLUSION

A method for estimating the shift in the threshold voltage in MOSFETs exposed to low-dose-rate ionizing radiation typical of space environments has been evaluated. The arithmetic sum of ΔV_{ot} after high-dose-rate irradiation and ΔV_{it} after high-dose-rate irradiation followed by 100°C anneal for 168 hours is compared to the threshold-voltage shift due to low-dose-rate ionizing radiation. This simple method was tested for three different technologies. The method is effective for commercial power MOSFETs which have very low annealing rates for oxide-trapped charge. Of the two integrated technologies evaluated, the method correctly predicts the low-dose-rate threshold-voltage shift for one, but not for the other. In the case where the method yields the correct result, the agreement appears to be coincidental. These results, coupled with the necessity for transistor-level test structures, suggests that the proposed method is applicable primarily to power MOSFETs that exhibit slow annealing of oxide-trapped charge and no rebound during low-dose-rate irradiation.

V. ACKNOWLEDGMENTS

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APPENDIX A

The threshold-voltage shift for the low-dose-rate irradiation is given by eq. (A1).

$$\Delta V_T(\mathrm{LDR}) = \Delta V_{ot}(\mathrm{LDR}) + \Delta V_{it}(\mathrm{LDR}) \quad \text{(A1)}$$

The predicted threshold-voltage shift for the low-dose-rate irradiation can be estimated from eq. (A2), assuming that $\Delta V_{it}(\mathrm{LDR}) \approx \Delta V_{it}(\mathrm{HDR} + 100°\mathrm{C}\ \text{anneal})$ and $\Delta V_{ot}(\mathrm{LDR}) \approx \Delta V_{ot}(\mathrm{HDR})$. Since this assumes that oxide-charge annealing is negligible, the lower the anneal rate, the better the approximation.

$$\Delta V_T(\mathrm{LDR}) = \Delta V_{ot}(\mathrm{HDR}) + \Delta V_{it}(\mathrm{HDR} + 100°\mathrm{C}\ \text{anneal}) \quad \text{(A2)}$$

The only other way that eq. (A2) can be accurate is if:

$$\Delta V_{ot}(\mathrm{HDR}) - \Delta V_{ot}(\mathrm{LDR}) = \Delta V_{it}(\mathrm{LDR}) - \Delta V_{it}(\mathrm{HDR} + 100°\mathrm{C}\ \text{anneal}), \quad \text{(A3)}$$

where $\Delta V_{ot}(\mathrm{HDR}) - \Delta V_{ot}(\mathrm{LDR})$ and $\Delta V_{it}(\mathrm{LDR}) - \Delta V_{it}(\mathrm{HDR}+100°\mathrm{C})$ are negative numbers, or equivalently if:

$$|\Delta V_{ot}(\mathrm{HDR})| - |\Delta V_{ot}(\mathrm{LDR})| = \Delta V_{it}(\mathrm{HDR}+100°\mathrm{C}) - \Delta V_{it}(\mathrm{LDR}), \quad \text{(A4)}$$

where $|\Delta V_{ot}(\mathrm{HDR})| - |\Delta V_{ot}(\mathrm{LDR})|$ and $\Delta V_{it}(\mathrm{HDR} + 100°\mathrm{C}) - \Delta V_{it}(\mathrm{LDR})$ are positive numbers. Equation (A4) indicates that eq. (A2) is accurate if, and only if, the amount by which $|\Delta V_{ot}(\mathrm{HDR})|$ overpredicts $|\Delta V_{ot}(\mathrm{LDR})|$ is equal to the amount by which $\Delta V_{it}(\mathrm{HDR} + 100°\mathrm{C})$ overpredicts $\Delta V_{it}(\mathrm{LDR})$. Even if eq. (A4) were satisfied at one total dose or dose rate, it would not have to be true at others.

As an additional simple example, consider a device that shows $\Delta V_{ot}(\mathrm{HDR}) = -1\mathrm{V}$ and $\Delta V_{it}(\mathrm{HDR} + 100°\mathrm{C}\ \text{anneal}) = +1\mathrm{V}$. Then, $\Delta V_T(\mathrm{LDR})$ predicted from eq. (A2) $= -1\mathrm{V} + 1\mathrm{V} = 0\mathrm{V}$. However, if the Co-60 irradiation takes approximately 10^3 s, and space lifetime is about 10 yr (3×10^8s), there are 5.5 decades of annealing. Assuming that $\Delta V_{it}(\mathrm{LDR}) \approx \Delta V_{it}(\mathrm{HDR} + 100°\mathrm{C}\ \text{anneal})$, and the anneal rate of oxide-trapped charge at room temperature is about 6%/decade, the actual $\Delta V_T(\mathrm{LDR})$ will instead be 0.33V (the difference is greater for higher annealing rates). The increase in the threshold voltage, combined with the reduced mobility due to scattering from radiation-induced charges, would reduce the current-drive capability. This emphasizes the importance of excluding devices that exhibit rebound from this test, even for cases where the annealing rate is relatively small.

IV.I. The Surface Generation Hump in Irradiated Power MOSFETs

The Surface Generation Hump in Irradiated Power MOSFETs*

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ABSTRACT

A method of quantifying near midgap-level interface traps, capture cross section, and changes in oxide-trapped charge using a surface generation hump in the subthreshold curve (I_d vs. V_g) of power MOSFETs is developed. The surface generation hump is a result of the generation of carriers from traps at the depleted Si-SiO_2 interface in a gated diode-type structure. The charge neutrality point of the hump is determined, and shifts of this point are due solely to changes in oxide-trapped charge. Another point is used to determine the stretchout of the hump, and thus the interface trap density. With the interface trap density determined, the capture cross section is extracted from the surface generation velocity.

I. INTRODUCTION

The space environment creates various types of damage in semiconductor devices [1]. For many years, separation techniques have been developed to quantify each of these effects and determine the impact of each on device performance. With the knowledge of how each effect alters the device performance, reliability and long-term use of electronic devices may be improved.

This paper describes a technique to quantify interface trap density, capture cross section, and oxide-trapped charge by using a hump which appears in the subthreshold (log I_d vs. V_g) curve of a DMOS (double-diffused metal oxide semiconductor) transistor, shown in Figure 1. The hump is a result of net generation of carriers from interface traps in a reverse biased gated diode region of the DMOS transistor (specifically, the neck region). When the gate bias in this region causes depletion of carriers under the gate, generation of carriers from interface traps occurs. However, when the gate bias causes inversion or accumulation, one type of carrier greatly outnumbers the other, and generation is extinguished. Thus a hump is created as the gate bias is swept from inversion to depletion to accumulation in the neck region of the DMOS transistor.

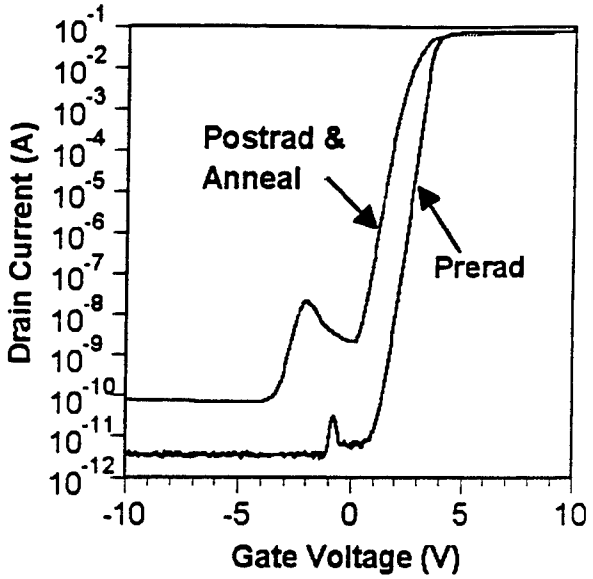


Figure 1. The drain current vs. gate voltage plot of a DMOS transistor. The subthreshold hump appears between the range of 0 and -1 volts.

A detailed model of the hump will be described first. The model is used to identify and quantify the different currents of the hump. The model uses theory developed by Grove and Fitzgerald [2,3]. However, certain aspects of the hump cannot be described by this theory. Grove and Fitzgerald assume that generation under the gate is constant laterally. The work of Pierret [4] corrects this assumption. The relevant parts of his work are added to the model.

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Using the hump model, the varying effects of interface traps and oxide-trapped charge can be separated through knowledge of how each affects the generation hump. Oxide-trapped positive charge shifts the hump negatively. Increases in interface traps have multiple effects: increasing the hump current while also stretching out the hump. Changes in capture cross section change only the hump current, not the stretchout of the hump.

The hump charge separation technique, as it will be called, simply extracts the three parameters from changes in the hump. Voltage shifts in the charge neutral point determine solely the oxide-trapped charge. Interface trap density is determined from the width of the hump. With the interface trap density determined, an average capture cross section can be extracted from the surface generation velocity, which is measured from the peak of the hump.

The effects of ionizing radiation on power MOSFETs are analyzed using the hump charge separation technique and the charge separation technique of McWhorter and Winokur [5]. The results indicate that the hump charge separation technique measures interface traps near midgap, which is different from other charge separation techniques. Possible uses for the technique are described.

II. HUMP THEORY

A. Gated Diode Effect

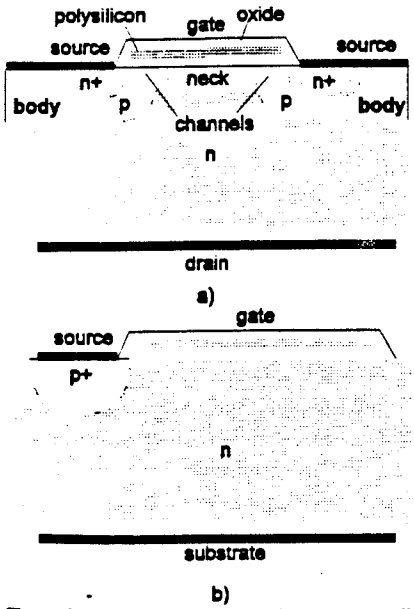


Figure 2. The device structures for a) a unit cell of the DMOS transistor and b) a gated diode. Both structures are similar when the channel of the DMOS is off and the drain-body junction is reverse-biased.

An unusual difference between subthreshold (log I_d vs. V_g) curves of DMOS and integrated MOSFETs is a small hump which appears in the characteristics of the DMOS transistor but which is not present in integrated MOSFETs. The subthreshold hump is shown in Figure 1 between -1 and 0 volts. This unusual hump ensues from the device structure of the DMOS device, shown in Figure 2(a). When biased with the channel turned off (drain-positive, source-grounded, and gate-less than the threshold voltage), the DMOS structure resembles a reversed biased gated diode, shown in Figure 2(b). As the gate voltage is swept from negative to positive, the neck region of the DMOS transistor progresses from inversion to accumulation. When the gate voltage causes depletion at the surface and the drain-body junction is reverse biased, generation from interface traps occurs.

The current components of a reverse biased gated diode are shown in Figure 3. A small, constant (with respect to the gate bias) current is generated from the depletion of carriers from the junction. Additional current occurs due to the generation of carriers in the gate-modulated depletion region. This current is zero when the gate bias causes accumulation, because there is no depletion region. The current rises as the gate bias causes the depletion region to expand until the interface is inverted, when the current remains constant. A third current arises only when the surface is depleted. Generation of carriers from interface traps occurs only when the surface is depleted. During inversion or accumulation, the surface is dominated by one type of carrier, thus no generation occurs. Combining these currents results in a hump when the gate bias is swept with the junction reverse biased .

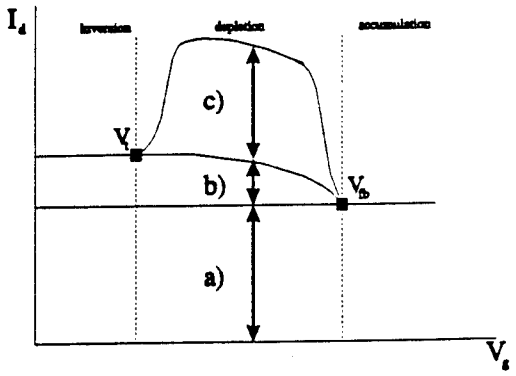


Figure 3. Typical characteristic of a gated diode fabricated on an n-type substrate. The current is composed of three components: a) a constant reverse biased junction current, b) a gate modulated generation current, and c) a surface generation current. Note threshold and flatband voltages bound the surface generation hump.

B. DMOS Hump

The hump which occurs in the subthreshold curve of a

DMOS transistor is due to the presence of a gated diode structure. However, due to the structure of the DMOS transistor, extra currents are also present in the gate voltage-drain current plot. At high gate voltages, the channel turns on. An exponentially rising subthreshold current flows as the gate voltage approaches the threshold voltage. Typically, this subthreshold current becomes significant at higher gate voltages beyond the range of the hump; thus the subthreshold current does not add to the hump current.

Another current adds to the hump when the channel region is depleted. The leakage on the inversion side of the hump is actually smaller than the leakage on the accumulation side for a DMOS device (note the difference between Figures 3 and 4). Also the magnitude of the hump is higher near accumulation rather than inversion. The added leakage occurs from surface generation from interface traps in the channel region, similar to the surface generation from interface traps in the drain region. The differences are that the channel area is smaller than the drain area and that the channel has different flatband and threshold voltages. This generation current in the channel increases similarly to the drain generation current when the device is damaged by radiation or other stressing.

C. Grove-Fitzgerald Model

The surface generation rate for a single interface trap at a single energy is given by [6]

$$U_s=\frac{\sigma_s v_{th} N_{it}(p_s n_s-n_i^2)}{p_s+n_s+2n_i\cosh(\frac{E_{it}-E_i}{kT})} \quad (1)$$

where n_s and p_s are the electron and hole surface concentrations for the area of interest, σ_s is the average capture cross section, v_{th} is the thermal velocity of carriers, N_{it} is the areal density of interface traps, E_{it} is the interface trap energy, and E_i is the intrinsic energy.

The recombination rate for a uniform distribution of interface trap energies is found by integrating (1) over the entire distribution of interface traps to acquire [3],

$$U_s=\frac{D_{it}\sigma_s v_{th} kT}{n_i}\frac{\arccos(\frac{p_s+n_s}{2n_i})}{\sqrt{1-(\frac{p_s+n_s}{2n_i})^2}}(p_s n_s-n_i^2) \quad (2)$$

where the rate is composed of three factors which represent three different physical effects. The first factor is characteristic of the traps, their density and capture cross section. The second factor depends on carrier concentrations and defines the shape of the hump. This factor peaks when the carrier concentrations are approximately equal. The third factor is the deviation from equilibrium. Converting recombination rate to current requires

$$I_s=qAU_s \quad (3)$$

where A is the area under the gate. Figure 4 shows the use of (2) and (3) in modeling the hump. The figure shows measured humps for different drain voltages and the results of the model overlaid upon them.

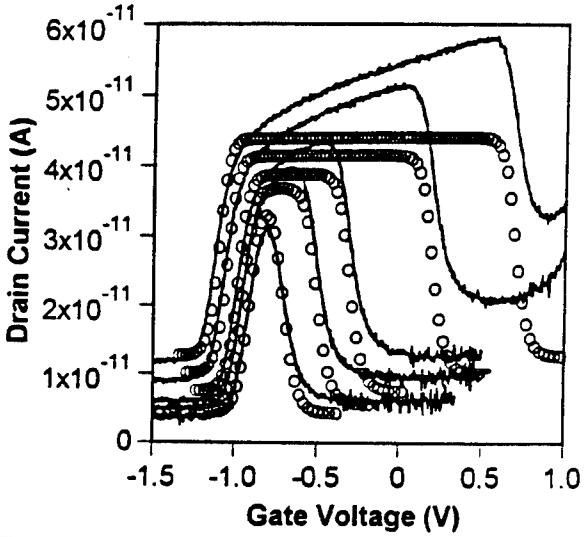


Figure 4. The modeling of the subthreshold hump in a DMOS device with equations (2) and (3). The model (circles) accurately describes the left side of the measured hump (lines); however, the added leakage from the channel surface generation cannot be modeled. Thus the hump current grows toward accumulation, while the model does not. The bulk constant current has been added to the model.

The peak current occurs when the concentrations of the holes and electrons are equal ($n_s=p_s$). Using this condition in (2) and (3), the peak current is

$$I_p=qAD_{it}\sigma_s v_{th} kTn_i\frac{\arccos(e^{-\frac{V_d}{2kT}})}{\sqrt{1-e^{-\frac{V_d}{kT}}}}(e^{-\frac{V_d}{kT}}-1) \quad (4)$$

where for sufficient junction bias, $V_d >> kT$,

$$I_p=qAD_{it}\sigma_s v_{th} kT\frac{\pi}{2}n_i, \quad (5)$$

which is the maximum surface generation current [2].

The hump expands with greater drain voltage because of the widening depletion region due to the body effect [7]. A biased substrate contact, like the drain contact of a DMOS

device, depletes the surface. In order for the surface to invert, $-2\phi_f + V_d$ in surface potential is required instead of just $-2\phi_f$. Thus the range of surface potentials for depletion increases with increasing substrate (drain) bias, and the hump widens.

D. Pierret's Correction

The model detailed in II.C. adequately describes surface recombination-generation processes in semiconductor devices for most cases. However, the model ignores the fact that carriers which are either generated or recombine must flow to the electrode to be counted as current. Typically these carriers must diffuse, thus requiring a slope in the quasi-Fermi level. The Grove-Fitzgerald model assumes constant quasi-Fermi levels laterally separated by the applied junction bias.

Pierret [4] modified the model of Grove and Fitzgerald to describe reduced generation from the lateral slope of the quasi-Fermi level. In order for carriers to diffuse, a slope of the quasi-Fermi level is required. This requirement arises directly from the current equation,

$$J_n = \mu_n n \frac{dE_{fn}}{dx}. \qquad (6)$$

When the carrier concentration is low (depleted), a large slope of the quasi-Fermi level is required. However, the slope of the quasi-Fermi level reduces generation farther from the junction, similar to lowering the applied junction reverse bias or raising the surface concentrations of holes and electrons. Thus a non-constant (laterally) generation rate occurs. Overall, the generation produced is less than that predicted by Grove and Fitzgerald. Thus the apparent surface generation velocity will be smaller than the true surface generation velocity. Figure 5 shows simulated results of the ratio of reduced surface generation velocity to true surface generation velocity. Simulations were performed using ATLAS II SPISCES with various gate lengths.

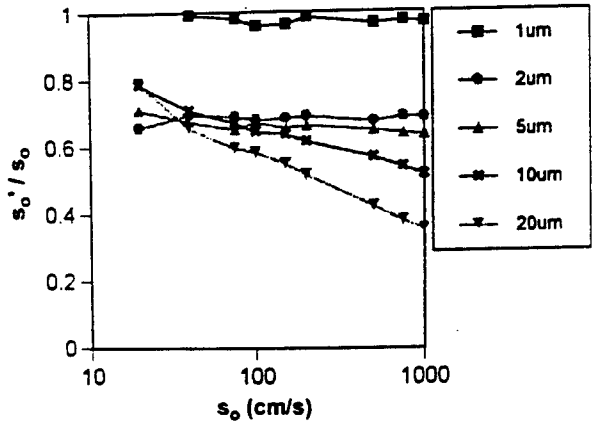


Figure 5. The ratio of measured s_o' to the true (input) s_o as a function of the true s_o. Various gate lengths are shown. s_o' was extracted from the peak of the hump.

The slope of the quasi-Fermi level occurs when the surface concentration is low. Thus when the minority carrier surface concentration (holes in n-type) is low, a large slope of the quasi-Fermi level is required. Simulations of one point on the hump where the minority carrier concentration is low is shown in Figure 6. The quasi-Fermi level slopes away from the junction. With greater surface generation velocity (indicated by the arrow), the quasi-Fermi level needs to slope more to attain a higher current.

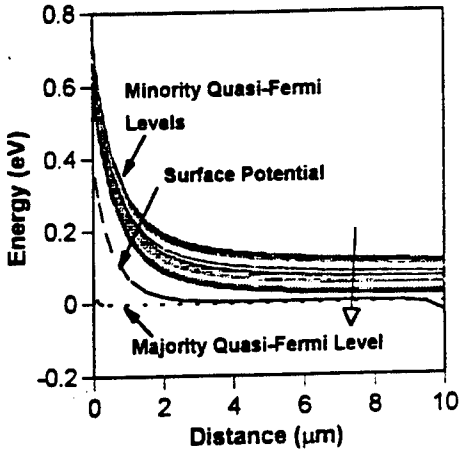


Figure 6. The lateral variation of the minority-carrier quasi-Fermi level. The surface generation velocity was at 1, 5, 10, 20, 40, 75, 100, 150, 200, 500, 750, and 1000 cm/s. The arrow shows the increase of surface generation velocity. The drain bias was 1.0 V and the drain doping was 1.9×10^{14} cm^{-3}.

As with the minority carriers, the majority carrier quasi-Fermi level also needs to slope when the majority carrier concentration is low. Figure 7 shows the quasi-Fermi levels of a point on the hump where the majority carrier concentration is low.

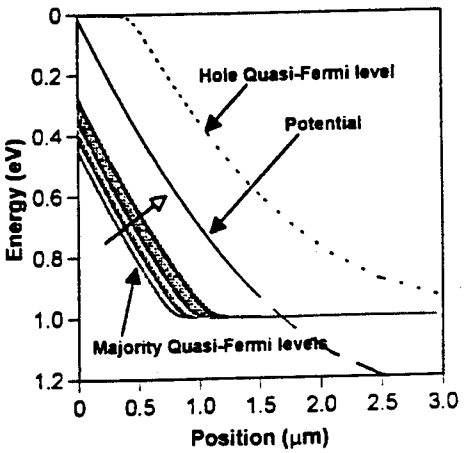


Figure 7. The variation of the majority-carrier quasi-Fermi level vertically. The majority-carrier quasi-Fermi level must be sloped because carriers move vertically to the substrate contact. The arrow indicates direction of increasing surface generation velocity. Simulations with a s_o of 1, 5, 10, 20, 40, 75, 100, 150, 200, 500, 750, and 1000 cm/s are plotted. The drain bias was 1.0 V and the drain doping was 1.9×10^{14} cm^{-3}.

III. Separation Technique

A. Charge Neutrality Point of the Hump

It is possible to use the subthreshold hump to quantify the effects of oxide-trapped charge, interface trap density, and capture cross section. In order to quantify these effects from the hump, a charge neutrality point must be determined. The hump charge separation technique relies on the same basic assumption that the McWhorter and Winokur charge separation technique [5] relies on: that interface traps are acceptorlike above the intrinsic energy and donorlike below the intrinsic energy. Thus at the midgap point (where the Fermi level equals the intrinsic energy at the surface), no charge can be attributed to interface traps. Voltage shifts in the midgap point are due solely to oxide-trapped charge.

With the surface generation hump, however, the Fermi level is split into two quasi-Fermi levels due to the deviation from equilibrium caused by the junction reverse bias. With the Fermi level split, questions arise as to what condition determines whether the interface traps are filled or empty. It can be shown that the probability of a trap being occupied is 0.5 when $n_s=p_s$ [8]. This occurs at the peak of the hump according to the Grove-Fitzgerald model; thus, the peak of the hump is the charge neutral point.

According to Pierret's correction, as discussed above, the true surface concentrations of minority carriers is increased due to lateral diffusion under the gate. Thus the true $n_s=p_s$ point occurs toward the accumulation side of the hump. We have calculated the point to be 0.3 to 0.4 V away from the peak for a hump reverse biased at 1.0 V with a doping of 1.9×10^{14} cm^{-3}. Thus the $n_s=p_s$ point seems to vary considerably from the peak voltage. However, because the interface stretchout from one side of the hump to the other is 0.15 V at most for our experiments, a very conservative estimate of the error in oxide-trapped charge is at most 0.15 V. For improved accuracy, a point toward the accumulation side of the hump could be used.

B. Midgap Voltages of the Hump

With the quasi-Fermi levels split at the interface, there are now two midgap voltages (see Figure 8). One midgap voltage occurs when the majority-carrier quasi-Fermi level equals the midgap energy, the other when the minority-carrier quasi-Fermi level equals the midgap energy. When referring to these two distinct points, we will define them as the majority-midgap and minority-midgap points, respectively.

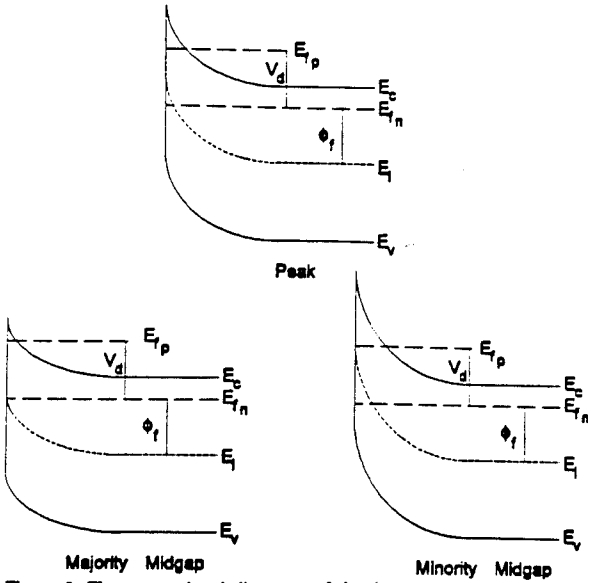


Figure 8. The energy band diagrams of the three critical points for the hump charge separation technique. The midgaps are defined where each of the respective quasi-Fermi levels equals the intrinsic energy at the surface.

The surface potential at which the minority midgap condition occurs is

$$\psi_s=\phi_f+V_d \tag{7}$$

where $-\phi_f$ is the bulk potential in the drain of the DMOS device. Using the appropriate surface concentrations for (7) and placing them in (2) and (3), one finds the midgap current of the hump,

$$I_{mid}=qAD_{it}\sigma_s v_{th} kTn_i \frac{\arccos\left(\frac{1+e^{-\frac{V_d}{kT}}}{2}\right)}{\sqrt{1-\left(\frac{1+e^{-\frac{V_d}{kT}}}{2}\right)}}\left(e^{-\frac{V_d}{kT}}-1\right). \tag{8}$$

Both midgap and peak (equation (4)) currents can be calculated, however, only if D_{it} and σ_s are known. The peak current can be found experimentally from the left side of the hump in DMOS devices (see Figure 9). In addition, if one examines both (8) and (4), the ratio of peak to midgap current can be found,

$$\frac{I_p}{I_{mid}} = \frac{\arccos\left(e^{-\frac{V_d}{2kT}}\right)}{\arccos\left(\frac{1+e^{-\frac{V_d}{kT}}}{2}\right)} \frac{\sqrt{1-\left(\frac{1+e^{-\frac{V_d}{kT}}}{2}\right)^2}}{\sqrt{1-e^{-\frac{V_d}{kT}}}} \quad (9)$$

The ratio is a very complex function of drain or junction bias voltage. However, the function does not depend upon D_{it} or σ_s. Thus when radiation or other stress causes changes in trap densities and capture cross section, the ratio of peak to midgap current remains constant. In other words, the hump increases proportionally when damaged. Thus the minority midgap current can always be found, because the ratio never changes with radiation, stressing, etc. For $V_d >> kT$, the ratio is about 1.3. For V_d = 0.1 V (typical drain voltage for subthreshold measurements), the ratio is about 1.2.

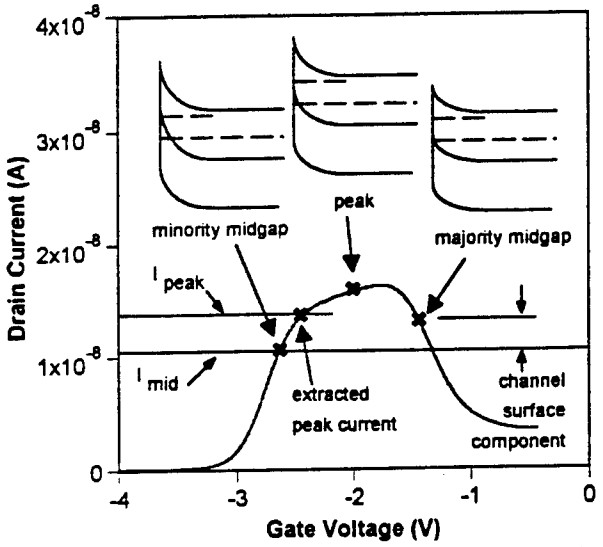


Figure 9. Subthreshold drain current vs. gate voltage, illustrating the subthreshold hump. The critical points for the hump charge separation technique are shown, minority midgap, majority midgap, and the peak voltage. The peak current is obtained from the left side of the hump away from the channel surface generation component. Midgap and peak currents are shown. Energy bands cut in the vertical direction are shown above the critical voltages to show the placement of the Fermi levels (dashed) and intrinsic level (solid middle).

The critical points for the hump are shown in Figure 9. The extracted peak current is found from the left side of the hump, because this part of the hump has the smallest current contribution from the body region. The peak voltage is found exactly in the middle of the hump, because this is where the intrinsic energy at the surface is halfway between the quasi-Fermi levels. The minority midgap voltage can be found by applying equation (9) on the left side of the hump. The majority midgap voltage has the same generation current as the minority midgap voltage because the product of the surface concentrations is the same. However, because majority midgap is on the accumulation side of the hump, the extra leakage of the channel region surface generation needs to be added. Thus the majority midgap current is the minority midgap current plus the extra channel region surface generation current.

C. Determining Interface Trap Stretchout

The width of the hump increases due to surface-potential-dependent interface charge. The minority midgap voltage is

$$V_{min} = V_{fb} - \phi_f - \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_d(-\phi_f - V_d)} + \Delta V_{ot} + \Delta V_{it(min)} \quad (10)$$

where ΔV_{ot} is the voltage shift due to oxide-trapped charge and $\Delta V_{it(min)}$ is the voltage shift at minority midgap due to interface traps.

The majority midgap voltage has a similar formula,

$$V_{maj} = V_{fb} - \phi_f + V_d - \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_d(-\phi_f)} + \Delta V_{ot} + \Delta V_{it(maj)} \quad (11)$$

except that it has a different interface-trap stretchout component, $\Delta V_{it(maj)}$. Thus with more interface-trapped charge, the majority midgap voltage moves farther away from the other midgap voltage. Note that both of these formulas have unknown quantities, V_{fb}, ΔV_{ot}, $\Delta V_{it(min)}$, and $\Delta V_{it(maj)}$. Subtracting equation (10) from equation (11) yields

$$\Delta V_{it} = V_{maj} - V_{min} - V_d - \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_d}\left(\sqrt{-\phi_f + V_d} - \sqrt{-\phi_f}\right) \quad (12)$$

where ΔV_{it} is the combination of $\Delta V_{it(min)}$ and $DV_{it(maj)}$. Thus, ΔV_{it} can be experimentally determined from the width of the hump since all other quantities are known.

D. Determining Interface Trap Density

In order to convert ΔV_{it} to a trap density one must know the separation between the intrinsic energy at the surface and the n_s=p_s level, or halfway between the quasi-Fermi levels. It was determined in III.A. that the n_s=p_s point determines whether the traps are filled or empty. From Grove-Fitzgerald theory [2,3], the separation between the quasi-Fermi levels at the two midgap points is $V_d/2$ from Figure 9. Using this assumption, the interface-trap charge component between majority and minority midgap is

$$\Delta V_{it} = \frac{qD_{it}}{C_{ox}} V_d \quad (13)$$

where V_d is drain voltage and also the portion of the bandgap in which the interface traps are charged.

However, Pierret has shown that the quasi-Fermi levels are not constant laterally, as discussed in II.D. Thus the separation between the intrinsic level and the n_s=p_s level must be determined from simulation. Using Figures 6 and 7, which are simulations of the majority and minority midgap points, the number of charged traps between the majority and minority midgap points can be found. Figure 10 shows the average energy interval for which the traps will change their charge state as the potential varies from majority to minority midgap, $\Delta\phi_t$, for various surface generation velocities and gate lengths. The energy $\Delta\phi_t$ should be used instead of V_d in (13),

$$D_{it}=\frac{\Delta V_{it}C_{ox}}{q\Delta\phi_t} \tag{14}$$

where $\Delta\phi_t$ is extracted using Figure 10.

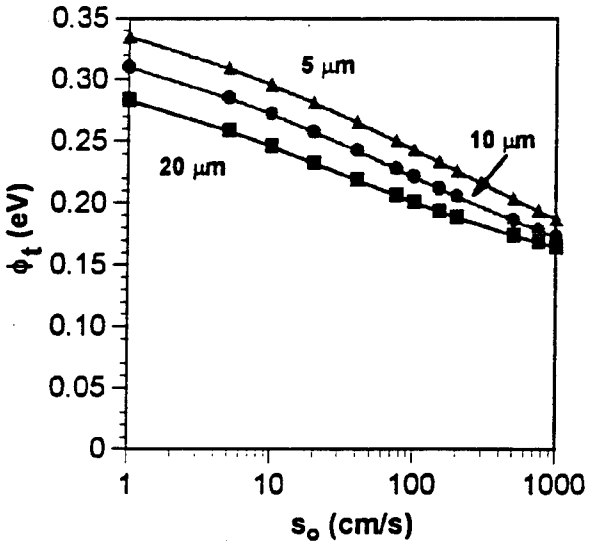


Figure 10. The average energy, $\Delta\phi_t$, of change in charged traps as the potential is varied from majority to minority midgap. The energy was determined with Figures 7 and 8 using the potential and the n=p point in energy.

E. Extracting Capture Cross Section

The surface generation velocity can be used to determine the capture cross section of the interface traps. The surface generation velocity is taken from the extracted peak current (see Figure 9) of the hump, equation (4). Capture cross section can be obtained from the surface generation velocity,

$$s_o=D_{it}\sigma_s v_{th}\frac{\pi}{2}kT \tag{15}$$

where σ_s is the capture cross section. Note that σ_s is the average capture cross section of all traps in the energy range being probed (i.e., around midgap).

IV. Experiment

Four IRF440 n-channel DMOS transistors were irradiated at a dose rate of 131 rad(Si)/s to a total dose of 12 krad(Si). The devices were irradiated with source and drain contacts grounded and with the gate bias set at +9 volts. Both threshold and subthreshold characteristics were measured as well as the subthreshold humps for drain biases of 0.1, 0.3, 0.5, 1.0, and 1.5 V. All measurements of threshold voltage, subthreshold I-V characteristics, and subthreshold humps were performed using an HP4145B semiconductor parameter analyzer.

Two different anneals were performed on the devices after irradiation. Both anneals were performed at a constant temperature of 100°C for 168 hours each. The first anneal after radiation was performed using a gate bias of +9 V, while the second anneal was performed after the first using a gate bias of -9 V. Both source and drain were grounded.

The method for determining drain doping in DMOS transistors [9] was used before irradiation, and all transistors had a drain doping near 1.9 x 10^{14} cm^{-3}. Drain area was determined using a C-V meter and found to be 0.1 cm^2.

V. Results

Figure 11 shows ΔV_t, ΔV_{ot}, and ΔV_{it} extracted using the midgap charge separation technique. After irradiation to 12 krad(Si), the threshold shifted negatively, mostly due to oxide-trapped charge. Afterwards, a positive bias anneal was performed at 100°C. During the anneal, the oxide-trapped charge was reduced, while the interface-trapped charge increased rapidly and leveled off. After the positive bias anneal, the gate bias was switched to negative. The oxide-

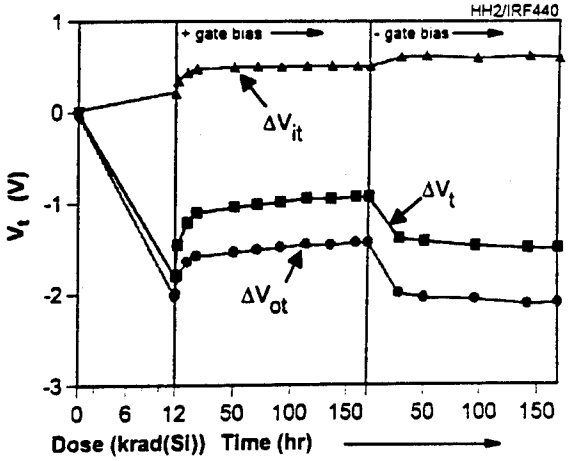


Figure 11. The results of the midgap charge separation technique upon irradiated and annealed transistors.

interface-trapped charge increased slightly. The reversibility of oxide-trapped charge during switched bias anneals has been attributed to border traps and charge compensation [10-12].

Hump measurements were also performed during the radiation and anneal experiments. The change in oxide-trapped charge, extracted from the hump, is shown in Figure 12. For comparison, the channel oxide-trapped charge taken from Figure 11 is also shown. Overall, the oxide-trapped charge over the drain is slightly lower than that over the channel due to the slightly lower electric field in the oxide during irradiation (in an n-channel device).

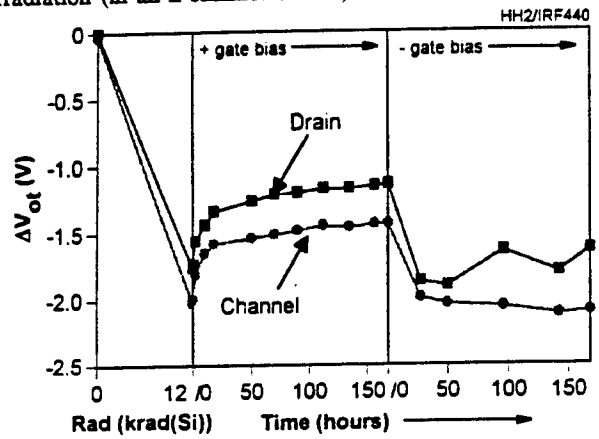


Figure 12. The changes in oxide-trapped charge during radiation and switched bias anneals for the midgap (channel) and hump (drain) charge separation techniques.

Immediately after irradiation, the hump did not widen sufficiently to allow estimation of the interface-trap density based on the width of the hump. Figure 13 shows the interface trap density throughout the two anneals after irradiation. Both measured trap densities increase during the positive bias anneal, yet with different magnitudes. During the negative bias anneal, the techniques indicate opposite trends.

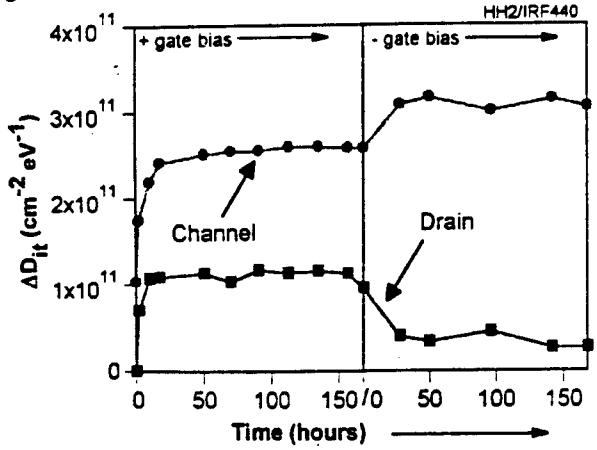


Figure 13. Changes in the density of interface traps for the midgap and hump charge separation techniques during the switched bias anneals after radiation.

The differences between the two methods can be understood by examining the part of the bandgap that each technique measures. It has been reported in many experiments [13-15] that radiation causes large differences in the energy distribution of interface traps. Specifically, a large peak in trap density typically occurs about 0.75 eV above the valence band. This falls within the measurement range for the midgap technique, which measures most of the conduction half of the bandgap. However, the hump is sensitive to trap energies within 0.1-0.15 eV of midgap. Thus the hump technique does not measure the large peak in the conduction half of the bandgap, and its D_{it} measurement is lower in Figure 13. The differences between the techniques during the positive bias anneal can be attributed to interface trap differences within the bandgap.

During negative bias anneals, reports have shown a reversibility of the peak at the 0.75 eV trap level [13,14]. Thus a decrease in interface traps would be expected for the channel measurement. However, a rise in interface trap density is indicated. The rise could be attributed to border traps in which the negative bias of the gate repels electrons from the border traps. Thus these unbonded border traps could communicate with the measurements [10]. The hump charge separation technique shows a decline in interface trap density, indicating a decline of midgap-level interface traps.

Once interface trap density has been determined, the capture cross section can be extracted from the surface generation velocity. Note again that the surface generation velocity is determined mostly by traps near midgap. The capture cross section is plotted in Figure 14, showing nearly no change during positive bias anneal and a slow increase during the negative bias anneal. The values are in the range of 10^{-15} cm^2, which is typical for irradiated capture cross sections of traps.

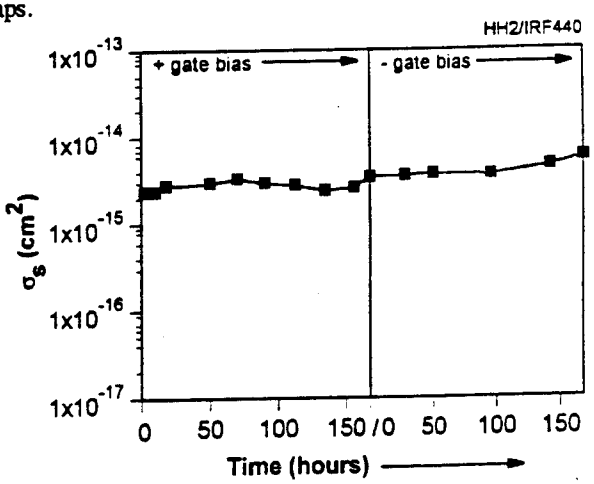


Figure 14. Capture cross section changes during the switched bias anneals after radiation.

The accuracy of the technique is not as accurate as McWhorter and Winokur, simply because the stretchout of the hump is smaller than the stretchout of the subthreshold hump.

The confidence of an extracted D_{it} occurs around 1-2 x 10^{10} cm^{-3}. Errors accruing from measuring small currents are minor, as proven with the model fitting well with the measured hump (Figure 4). Thus the technique is repeatable with little error.

VI. Conclusion

A technique of quantifying oxide-trapped charge, midgap-level interface trap density, and capture cross section has been developed. The technique uses the charge neutral point of the hump as the peak voltage. Shifts in this point are due solely to oxide-trapped charge. The stretchout due to interface traps is determined from changes in the width of the hump. Converting this stretchout due to interface traps to a density of traps requires knowledge of the quasi-Fermi levels at the surface. Once the density of traps is determined, capture cross section can be extracted from the peak of the hump.

Results for irradiation differ from the charge separation technique of McWhorter and Winokur. Each method measures a different part of the bandgap. Differences in the results are explained by the differences in the energy distribution of the interface traps. The hump is sensitive only to midgap-level interface traps, while the midgap technique measures interface traps and border trap effects.

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IV.J. Exploration of Heavy Ion Irradiation Effects on Gate Oxide Reliability in Power MOSFETs

Pergamon

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EXPLORATION OF HEAVY ION IRRADIATION EFFECTS ON GATE OXIDE RELIABILITY IN POWER MOSFETs

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ABSTRACT

Heavy ion irradiation effects on gate oxide reliability in power MOSFETs were explored. Devices were exposed to heavy ion fluences and LETs simulating exposure in spacecraft at bias levels not expected to cause catastrophic failure. Time dependent dielectric breakdown measurements and charge separation techniques resulted in no detectable changes. The gate voltage at which oxide breakdown occurs and the gate I-V curves suggest subtle changes in device characteristics that can be detected at high gate biases. However, there is no indication that heavy ion exposure results in a significant reduction in gate oxide reliability.

I. INTRODUCTION

Heavy ions are omnipresent in the natural space radiation environment [1]. When an energetic heavy ion passes through an electronic component, it loses energy along its track. In the silicon and silicon oxide layers of a silicon semiconductor device, a plasma of electron-hole pairs is created (or deposited) along its track length [2]. The energy spectrum of heavy ions and their associated flux are reasonably well known [3,4]. Typically, the effects of these ions on electronic devices are referred to as single-event phenomena.

In power MOSFETs, there are two types of single event phenomena: single-event burnout (SEB) and single-event gate rupture (SEGR). In the case of SEB, the currents stemming from ion-induced charge collection cause a voltage drop sufficient to turn on a parasitic bipolar transistor inherent in the construction of the power MOSFET [5], as illustrated in Figure 1. If the strike occurs while the device is subject to a large drain bias, sufficient carrier multiplication may occur to cause runaway, creating a short-circuit through the MOSFET that allows current from the external power supply to destroy the device.

SEGR can occur when the ion track passes through the neck region of the power MOSFET. This is the region where the n-type drain reaches the surface (Fig. 1). In the case of SEGR, the ion-generated electron-hole pairs in the silicon are separated by the applied bias. Recently, Brews *et al.* [6] presented a physical model of hole collection following a heavy ion strike that explains the development of oxide fields sufficient to cause gate rupture.

These two single event phenomena (SEB and SEGR) have received much attention. However, noncatastrophic damage which degrades the performance of the oxide due to heavy ions has not been identified. During the lifetime of a device in a spacecraft, it will be constantly bombarded with heavy ions. Questions arise as to whether these ions cause some noncatastrophic damage in the oxide or reduce the reliability of the oxide. The objective of this paper is to explore the effects of heavy ion irradiation on power MOSFETs in situations where SEB or SEGR do not occur. Devices were exposed to heavy ion fluences and energies simulating exposure in spacecraft at bias levels not sufficient to cause catastrophic failure.

This paper suggests heavy ions do cause subtle changes in characteristics of the oxide, though not easily detectable by normal techniques. Time dependent dielectric breakdown measurements resulted in no detectable changes. However, the gate voltage at which oxide breakdown occurs and the gate I-V curves indicate changes that can be detected at high gate biases. There is no indication that heavy ion exposure results in reduced gate oxide reliability.

II. EXPERIMENTAL DETAILS

For this experiment, thirty IRF440 power MOSFETs were irradiated with bromine (Br) ions at the Brookhaven National Laboratory. Three separate levels of exposure to heavy ion bombardment were conducted with each exposure level consisting of ten samples. The devices were bombarded at a flux of 2 to 2.5 x 10^4 ions/cm^2-s to three fluence levels: 1 x 10^5 , 5 x 10^5, and 5 x 10^6 ions/cm^2. Fluences were chosen to simulate applications in a space environment. These values estimate heavy ion exposure for a ten year mission. The energy of the ions was high enough to penetrate the entire oxide. The associated total ionizing dose from the ions was extremely small, at most 3 krad(Si), for the highest fluence. Gates were biased at +10 V with source and drain grounded during exposure. The gate area for the IRF440 is about 0.1 cm^2.

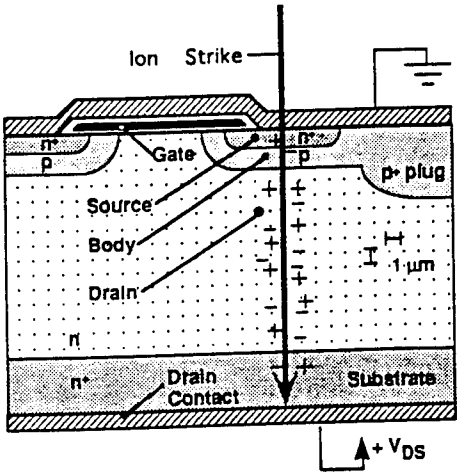


Figure 1:
Picture of heavy ion charge filament in a power MOSFET causing Single Event Burnout (SEB). The filament is capable of turning on the base-emitter voltage of the inherent parasitic transistor of the MOSFET.

Charge to breakdown tests were conducted with source and drain grounded. A constant positive 40 μA of current was driven into the gate using a HP4145B semiconductor parameter analyzer. Gate voltage was monitored during stressing. A voltage source was used to offset the gate voltage to avoid the 100 V compliance of the analyzer.

III. EXPERIMENTAL RESULTS

The time dependent dielectric breakdown measurements will be described first. Changes in gate voltage were monitored during stress. Figure 2 shows a typical stress test, where the gate voltage was plotted against the time. Constant current is forced through the oxide with source and drain grounded. Initially, hole trapping dominates and causes the gate voltage to drop. Afterwards, electron trapping from substrate injection becomes dominant and causes the voltage to rise [7,8]. Once the electric field becomes large enough, the oxide breaks down. Oxide breakdown occurs when the gate voltage drops to zero.

The cumulative percentage of failed devices is plotted vs. time-to-breakdown in Figure 3. Ten devices at each fluence level were measured, and an additional ten devices which did not receive irradiation were used as a control. A significant difference in charge-to-breakdown measurement between categories (irradiated and non-irradiated) would show as a shift in the curve toward lower breakdown times. However, all the lines nearly fall on one another. Thus, no significant reduction in time-to-breakdown is observed for MOSFETs exposed to heavy ions as compared to the control MOSFETs.

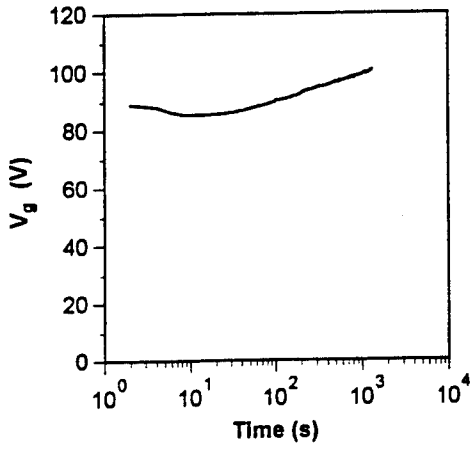


Figure 2:
The change of gate voltage during the stress is shown. Initially, hole trapping dominates and causes the gate voltage to decrease. At later times, electron trapping begins to dominate and causes the gate voltage to increase. The final gate voltage is the last voltage before breakdown of the oxide.

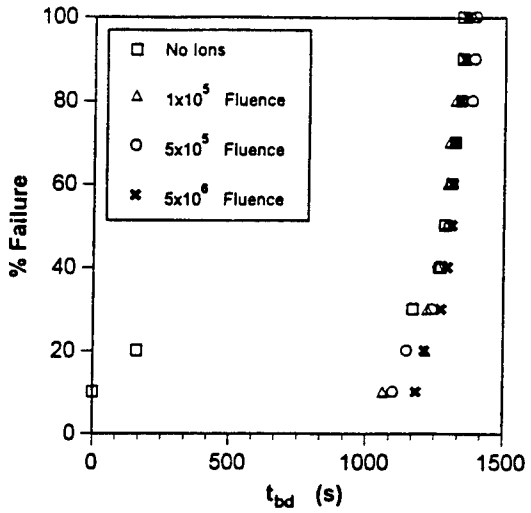


Figure 3:
Cumulative percentage of failed devices vs. time to breakdown for control and irradiated power MOSFETs. No significant differences between non-irradiated and irradiated MOSFETs appear.

Charge separation using the midgap technique of McWhorter and Winokur [9] was performed on all devices. This technique separates oxide-trapped charge and interface-trapped charge in MOSFETs using the subthreshold current that flows when the surface potential equals the intrinsic potential. Changes of the midgap voltage are equivalent to changes in oxide-trapped charge. The difference between the midgap voltage and the threshold voltage is used to determine the interface-trapped charge component. However, no change in threshold or subthreshold characteristics was detected. Gate current was also measured for gate voltages less than 20 V. No appreciable gate leakage was found after heavy ion bombardment, though drain-to-source junction leakage did increase. It is believed this increase is not associated with the oxide.

The gate voltage of the devices at failure was measured. The final gate voltage is the last measured gate voltage before the oxide is shorted due to failure. The final gate voltage plot (Figure 4) shows that, unlike the breakdown times which show no difference between irradiated and non-irradiated parts, the final gate voltages are slightly different between irradiated and non-irradiated MOSFETs. Note that the x-axis of Figure 4 has been enlarged to show the difference more clearly. The non-irradiated MOSFETs seem to

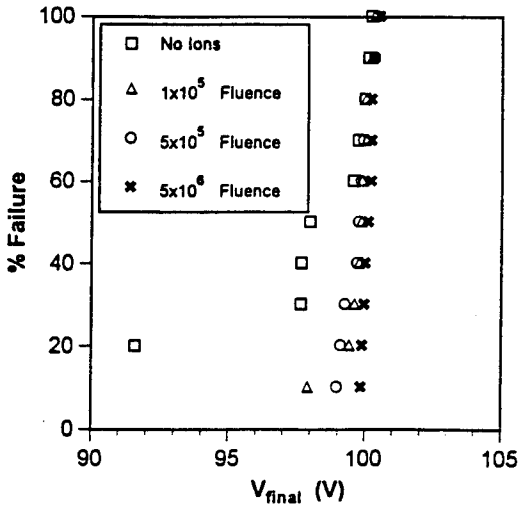


Figure 4:
Cumulative percentage of failed devices vs. the final gate voltage. Note the x-axis has been enlarged to emphaize the difference between groups. The non-irradiated parts seemed to fail at a voltage slightly lower than irradiated parts.

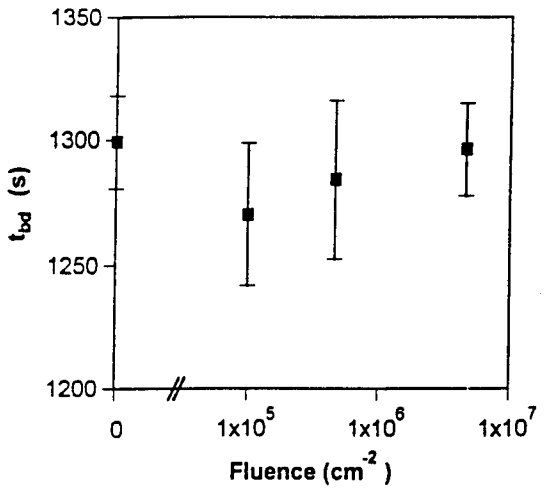


Figure 5:
Average time-to-breakdown vs. ion fluence with standard error bars indicating 95% confidence in the average value. Note all error bars can overlap, thus indicating that it is doubtful that any change is occurring in time-to-breakdown after heavy ion irradiation.

break down at a lower gate voltage than the irradiated MOSFETs. The gate voltage was monitored as the device was being stressed, and the irradiated MOSFET gate voltages (as a function of time) were on average about 1 or 2 volts larger than the non-irradiated. However, this difference was not seen in the breakdown times.

To more quantitatively reveal the difference between the non-irradiated and irradiated MOSFETs, the average breakdown time and final voltage, as well as their associated standard error bars are shown in Figures 5 and 6, respectively. The standard error indicates the 95% confidence level that the average of a particular group of samples is within the bounds indicated. The standard error is calculated from the standard deviation divided by the square root of the number of samples in the group. Note that the standard error determines whether the random nature of these measurements can explain the differences between the groups of samples. If the standard error bars of different groups do not overlap, then the random nature of these types of measurements cannot explain the differences.

From Figure 5, there are no significant differences between the irradiated and non-irradiated groups when examining breakdown times (t_{final}). This result suggests heavy ion bombardment does not affect time-to-breakdown. The plot of the voltage at which oxide breakdown occurs (Figure 6) shows that the groups of fluences do not all overlap within the standard error. Thus, there seems to be a general trend of increasing

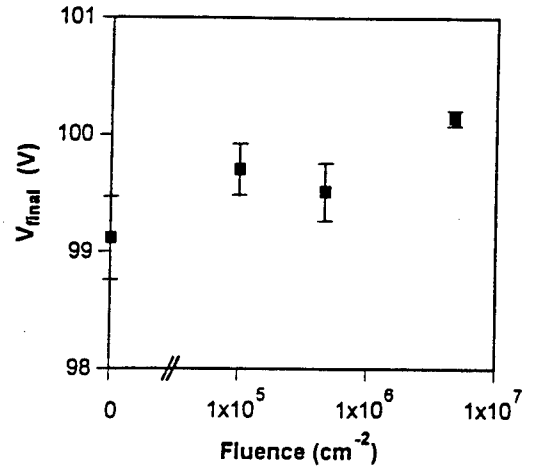


Figure 6:
The average final gate voltage (V_{final}) vs. ion fluence with standard error bars indicating 95% confidence in the average value. Note all error bars do not overlap, thus indicating that heavy ion irradiation does have an effect on the average oxide breakdown voltage.

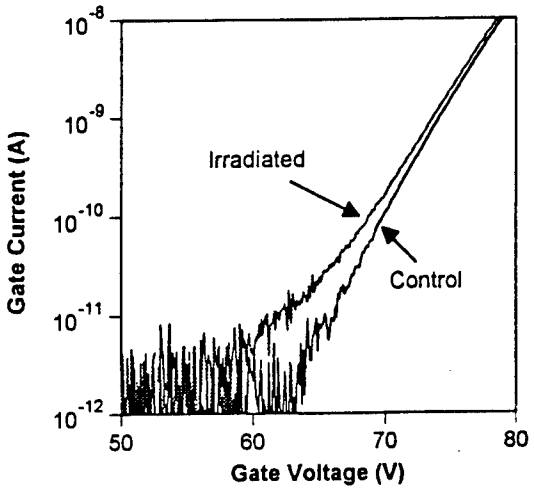


Figure 7:
Gate current vs. gate voltage is shown for a non-irradiated and an irradiated MOSFET. The irradiated MOSFET has a shallower slope at lower voltages than the non-irradiated MOSFET.

final gate voltage with increased heavy ion bombardment. This result is especially evident between the $5x10^6$ fluence and the non-irradiated group, where the final gate voltages differ by a volt. Note the averages for non-irradiated MOSFETs were modified by excluding the two devices which broke down very early in the test. The two devices did not seem representative of the group because they broke down extremely early. If the devices are included in the group, it would not change the interpretation of the results, because it would only lower the average of the non-irradiated group of devices.

Previously, it was stated there was no difference in gate current between irradiated and non-irradiated MOSFETs at gate voltages below 20 V. During normal operation, the gate voltage should not leave this range. However, we did measure the gate current out of this range to more fully explore differences between the MOSFETs. As can be seen in Figure 7, the irradiated parts have an increased leakage component at small current levels as compared to the non-irradiated parts. At higher levels, the difference is small and the gate current follows the Fowler-Nordheim equation [10]. The increased leakage has been attributed to positive charge residing near the injecting interface [11]. All irradiated devices followed the irradiated curve closely, while the control devices followed the control curve closely. Thus, variation between devices does not explain the difference. Note the gate voltages required to induce Fowler-Nordheim current in power MOSFETs are much larger than small signal MOSFETs for ICs due to the large gate oxide thickness (approximately 100 nm).

IV. DISCUSSION

When sufficient voltage is applied to the gate, a difference in gate current and breakdown characteristics between irradiated and non-irradiated MOSFETs can be detected. At smaller gate voltages (charge separation voltages), no significant change in threshold and subthreshold curves is detected. The differing results could be explained by a localized positive charge. Previous work has shown that heavy ions create positive charge, though not of the same magnitude of typical total-ionizing-dose experiments [12,13]. During irradiation, the ions cause electron-hole pairs to be created in the oxide which mostly recombine. The electrons which remain quickly move toward the positive terminal (gate electrode). If the remaining positive charge is localized (lateral non-homogenous charge distribution), the channel in that region inverts at a lower voltage. However, the entire channel is not affected because other parts of the channel still require a higher voltage to cause inversion. A localized positive charge also explains a slightly larger gate current at higher biases due to the barrier lowering for injecting carriers.

The localized charge does not explain increases in the final gate voltage. A localized positive charge would lower the barrier (as for the gate leakage measurements). Thus, a larger current would flow in that localized area. Since the stressing is a constant current stress, the remaining current through the gate would be slightly less. Yet a lower current would cause a lower gate voltage, not the higher gate voltage that was measured. Thus, the localized charge model is incomplete.

Note, however, that the gate voltage was monitored throughout the entire stress. The irradiated curves were higher and parallel to the non-irradiated curve. This effect suggests that charge from heavy ions was trapped in the oxide from the shift of the gate voltage. However, since the irradiated curves are parallel to the non-irradiated curves, no change in the mechanisms of charge trapping or trap generation has occurred. No change in the breakdown times (t_{bd}) also confirms this conclusion.

V. CONCLUSIONS

In summary, we have shown the results of heavy ion exposure on the gate oxide of power MOSFETs. Charge separation and dielectric breakdown techniques do not indicate any degradation due to heavy ion bombardment. Nevertheless, irradiated MOSFETs break down at a slightly higher gate voltage and also show an increase in gate leakage under high electric field conditions. Though results indicate slight changes in these characteristics, there is no indication of oxide reliability reduction from heavy ion bombardment.

VII. ACKNOWLEDGEMENTS

We would like to thank C. Frank Wheatley, Jr., Consultant, for useful discussions and for assistance with the heavy ion irradiations. We would also like to thank Dr. Dragan Zupac and Dr. John Brews of the University of Arizona for their valuable insights. The authors would also like to thank Dr. Jean Gasiot of the University of Montpellier for useful discussions on ion damage in insulators.

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IV.K. The Effects of Ionizing Radiation on Commercial Power MOSFETs Operated at Cryogenic Temperatures

THE EFFECTS OF IONIZING RADIATION ON COMMERCIAL POWER MOSFETs OPERATED AT CRYOGENIC TEMPERATURES

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Abstract

This is the first report of commercial n- and p-channel power MOSFETs exposed to ionizing radiation while operating in a cryogenic environment. The transistors were exposed to low energy x-rays while placed in a liquid nitrogen-cooled dewar. Results demonstrate significant performance and survivability advantages for space-borne power MOSFETs operated at cryogenic temperatures. The key advantages for low-temperature operation of power MOSFET's in an ionizing radiation environment are: (1) steeper subthreshold current slope before and after irradiation; (2) lower off-state leakage currents before and after irradiation; and (3) larger prerad threshold voltage for n-channel devices. The first two points are also beneficial for devices that are not irradiated, but the advantages are more significant in radiation environments. The third point is only an advantage for commercial devices operated in radiation environments. Results also demonstrate that commercial off-the-shelf power MOSFETs can be used for low-temperature operation in a limited total dose environment (*i.e.*, many space applications).

I. INTRODUCTION

Power Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) exhibit superior performance at cryogenic temperatures compared to room temperature. Significant improvements in on-resistance, thermal conductance, power handling, reliability, switching speed, and switching efficiency occur during low-temperature operation [1-3]. The double-diffused metal-oxide semiconductor (DMOS) power transistor is a key component in switched-mode power supplies, motor controllers, and power converters (*i.e.*, power distribution and control) for many space-borne systems [4].

A cross-section of one cell of the DMOS power transistor is shown in Figure 1 [4]. The DMOS device can withstand large off-state voltages because of the rather thick epitaxial region. Large on-state currents are accomplished by connecting many cells in parallel [4]. Previous work has shown that ionizing radiation induces threshold voltage shifts [5-7], degradation of carrier mobility [5, 8], loss of current drive capability [5, 8], and reduction in switching speed [8] in power DMOS devices at room temperature. Cryo-electronics are important for a number of space applications (particularly imaging), and there is significant potential for using commercial power MOSFETs in these

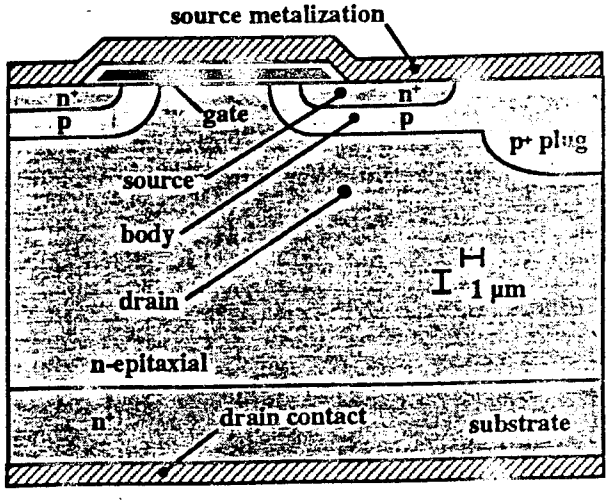


Figure 1: Cross-section of n-channel DMOS power transistor.

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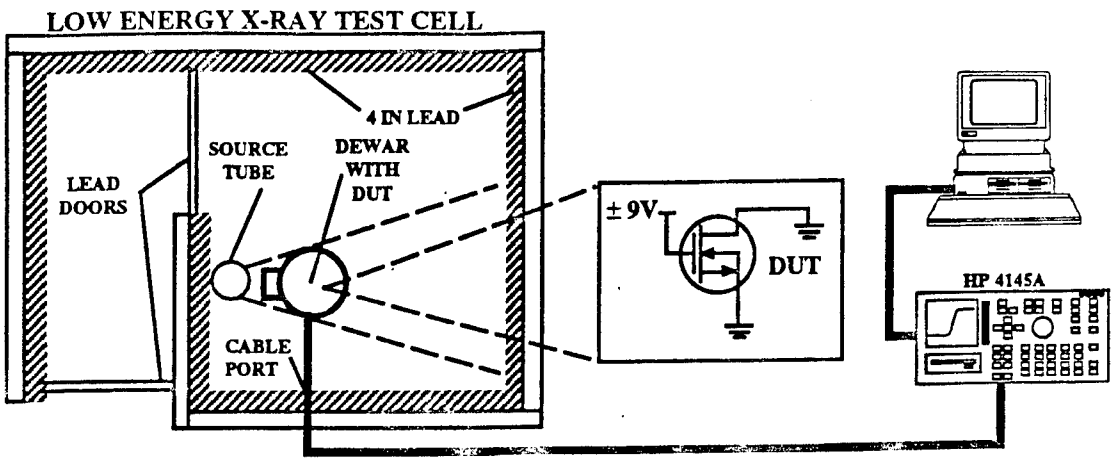


Figure 2: Experimental test set-up. The source tube, dewar, and data acquisition system are shown. The graph inset shows the bias conditions for an n-channel transistor. The p-channel bias conditions are identical.

systems. Furthermore, the increased switching speed achieved at low temperature allows for the design of lighter weight magnetic components which can lead to a higher power density (also important for space applications) [4]. This paper presents the first known results on commercial n- and p-channel power MOSFETs irradiated and characterized at cryogenic temperatures. This follows the current trend to try to identify commercial off-the-shelf electronics that may be suitable for use in the space radiation environment. Significant performance and survivability advantages associated with cryogenic operation of space-borne power MOSFETs are demonstrated.

II. EXPERIMENT

A. *Devices and Experimental Apparatus*

Commercial power MOSFETs manufactured by Harris Semiconductor (IRF9130 p-Channel and IRF130 n-Channel) were used for this experiment. A sample size of twelve devices was used in this experiment. The radiation source used was the Low Energy X-ray Facility at Phillips Laboratory, Kirtland AFB, NM.

The testing vessel used for this experiment was a dewar manufactured by Precision Cryogenics Systems. This is a dual coolant dewar with a 2 in diameter cold foot. The cold foot was at ground potential, and a special mounting technique was configured to test two devices of the same type at the same time. A base mounting fixture was attached to the cold foot with sapphire spacers between the cold foot and the mounting fixture. The sapphire provides good electrical isolation and excellent thermal conduction between the cold foot and mounting fixture. This allowed a potential to be applied to the drain, the case of the devices, during testing . The lowest temperature obtainable in the dewar is 10 K. A Lake Shore Cryotronic DRC-93C Temperature Controller was used to monitor the temperature of the cold foot and the devices. Temperature readings were taken with a Lake Shore platinum resistor (PT-103) that was mounted in the cold foot and on one of the devices under test. Data were taken with a Hewlett-Packard Semiconductor Parameter Analyzer (HP4145A) and the software package METRICS developed by Alliance Technologies. The experimental test set-up is shown in Figure 2.

B. *Experimental Setup and Test*

Once mounted in the test vessel, the devices were characterized at room temperature (293 K) with a vacuum applied to the test vessel. The test vessel was placed in the irradiation cell and liquid nitrogen (LN_2) was used to cool the devices. The devices reached a temperature of 81 K and were maintained at that temperature throughout the experiment. Note that all device characterization was performed *in-situ* within the cryogenic test vessel.

The devices were irradiated in the cryogenic test vessel to a total dose of 15 krad[Si]. Measurements were taken at prerad, 1, 2, 5, 10 and 15 krad[Si]. (The energy of the X-ray

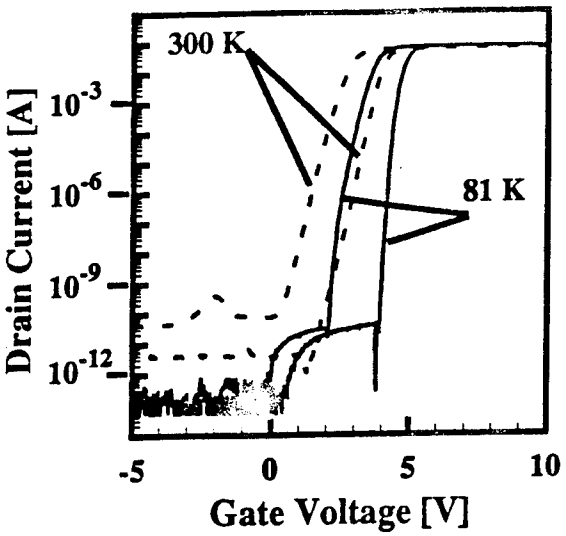


Figure 3: Prerad and post 15 krad [Si] n-channel subthreshold characteristics at 273 K and 81 K. The right most curve for each temperature is the prerad condition.

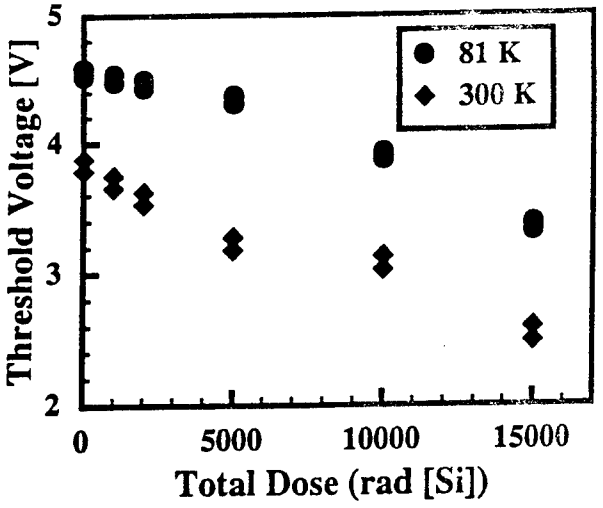


Figure 5: Threshold voltage versus total dose for 81 K and 273 K. Data for two devices is shown for each temperature.

source was 50 keV with the tube current at 10 mA; resulting in a dose-rate of 5.9 rad[Si]/sec.) Subthreshold and threshold voltage measurements were performed after each exposure. Experiments were performed with + 9 V or - 9 V bias applied to the gate electrode, V_g, and the source and drain electrodes were grounded. (Note that in the DMOS device structure, the body and source are common [4].)

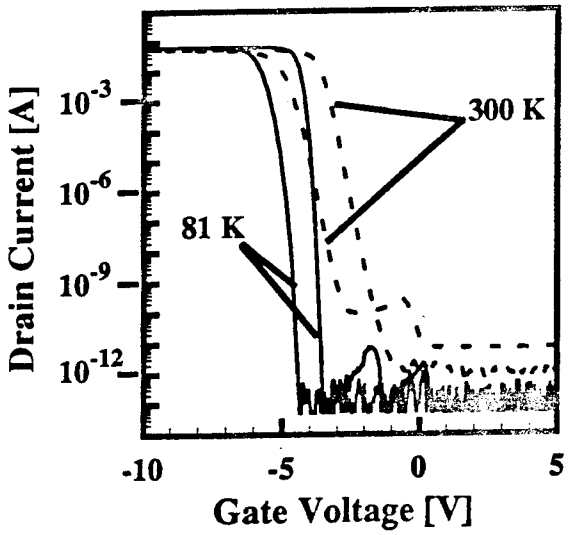


Figure 4: Prerad and post 15 krad [Si] p-channel subthreshold characteristics at 273 K and 81 K. The right most curve for each temperature is the prerad condition.

III. RESULTS AND DISCUSSION

Figure 3 shows the n-channel subthreshold characteristics for pre-rad and 15 krad[Si] exposure at room and cryogenic temperature. The corresponding data for p-channel devices are shown in Figure 4. The pre-rad threshold voltage at 81 K is 4.56 V compared to 3.83 V at 273 K for the n-channel devices and -4.20 V compared to -3.39 V for the p-channel devices. From these plots, it is obvious that there are three advantages for cryogenic power MOSFET operation. These advantages are: (1) steeper subthreshold slope before and after irradiation (improves switching efficiency); (2) lower off-state leakage currents before and after irradiation; (3) larger pre-rad threshold voltage for n-channel devices. The first two points are also beneficial for devices that are not irradiated, but the advantages are more significant in radiation environments. The third point is only an advantage for commercial devices operated in radiation environments. The steeper subthreshold slope helps to compensate for radiation-induced stretch-out and mobility reduction. In many circuits, the failure mechanism is defined as the reduction of the n-channel threshold voltage to the point of depletion-mode operation. The larger initial threshold voltage at cryogenic temperature increases the failure margin for total dose exposure. This point is illustrated in Figure 5, which shows threshold voltage versus total dose for room and cryogenic temperature operation for n-channel devices. While it is possible to fabricate power MOSFETs with higher initial threshold voltage, this is not consistent with the trend toward increased use of commer-

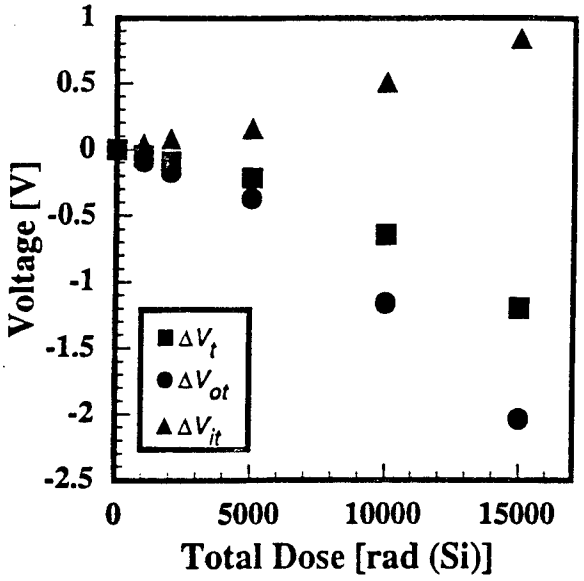


Figure 6: Separated charge for n-channel power MOSFETs (T=81 K). The change in threshold voltage, ΔV_t, change in oxide trapped charge component, ΔV_{ot}, and change in interface trap charge component, ΔV_{it}, are shown.

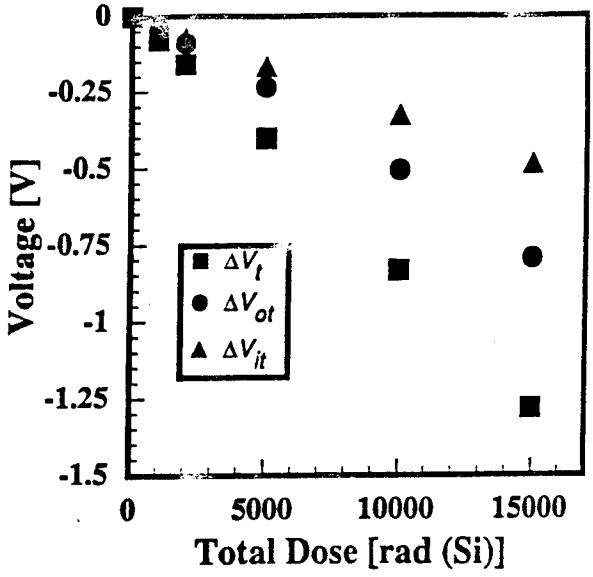


Figure 7: Separated charge for p-channel power MOSFETs (T=81 K). The change in threshold voltage, ΔV_t, change in oxide trapped charge component, ΔV_{ot}, and change in interface trap charge component, ΔV_{it}, are shown.

cial off-the-shelf technology in radiation environments. Note that the larger threshold voltage at cryogenic temperatures should be accounted for in the gate-drive circuitry. The amount of threshold-voltage shift at cryogenic temperature is comparable to that at room temperature.

The components of oxide charge leading to changes in the threshold voltage were separated using the midgap charge separation technique [9]. The current ranges used in this analysis were consistent with previous work involving charge separation on DMOS transistors [5-8]. The results of this analysis for the case with V_g =+9 V appear in Figure 6 and Figure 7 for the n- and p-channel devices, respectively. In Figure 6-7, the data from one device is shown. The spread in the charge separation data from device to device is less than a tenth of a volt. The total change in threshold voltage, ΔV_t, the oxide-trapped charge component, ΔV_{ot}, and the *apparent* interface trap component, ΔV_{it}, are shown.

Again, using the midgap charge separation technique, ΔV_t, ΔV_{ot}, and ΔV_{it}, are shown for the case of V_g = -9V in Figure 8 and Figure 9 for the n- and p-channel devices, respectively. In Figures 8-9, the data are shown from a representative device, and the spread in data is similar to that from Figures 6-7. For reference, the data for V_g = +9V are shown using solid symbols in Figure 8 and Figure 9 (for V_g = -9V the symbols are open). There is a gate bias dependence apparent in Figure 8 and Figure 9. For the n-channel devices (Figure 8), a negative gate bias results in larger shifts in ΔV_t, ΔV_{ot}, and ΔV_{it}. (The ΔV_{it} component becomes lower for negative gate bias at larger total dose). This result is surprising since a negative gate bias usually results in smaller shifts. For the p-channel devices just the opposite occurs. The positive gate bias results in larger shifts (approximately 25%) in ΔV_t, ΔV_{ot}, and ΔV_{it} for all total dose levels.

It is often believed that interface-trap formation at 77K is negligible because the positively charged species believed to be responsible are immobile at this temperature [10, 11]. However, the change in ΔV_{it} may not be due to the formation of interface traps, but may be due to lateral non-uniformities (LNU's) [10, 11], or the formation of border traps [12-14]. There have been reports of interface trap formation at cryogenic temperatures in gate oxides comparable in thickness to those found in power DMOS devices (750 Å - 1000 Å) [15]. A discussion of interface traps, border traps, and LNU's follows.

Interface traps are often associated with P_b centers, which are trivalent Si defects at the Si/SiO_2 interface [16, 17]. Since

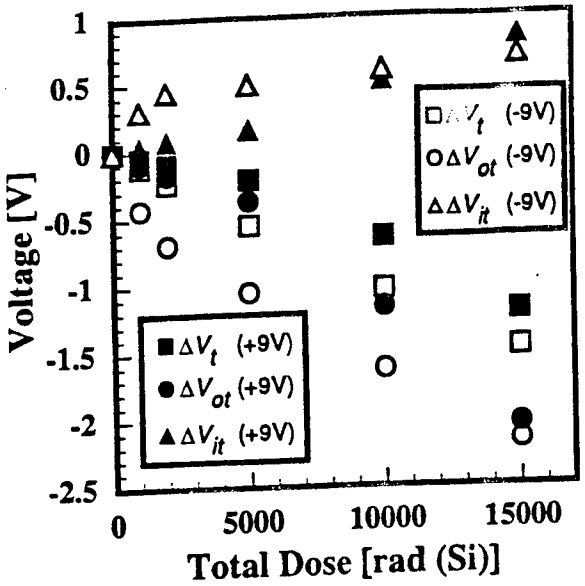


Figure 8: Separated charge for n-channel power MOSFETs (T=81 K). The change in threshold voltage, ΔV_t, change in oxide trapped charge component, ΔV_{ot}, and change in interface trap charge component, ΔV_{it}, are shown. The open symbols correspond to V_g=-9V and the closed symbols correspond to V_g=+9V.

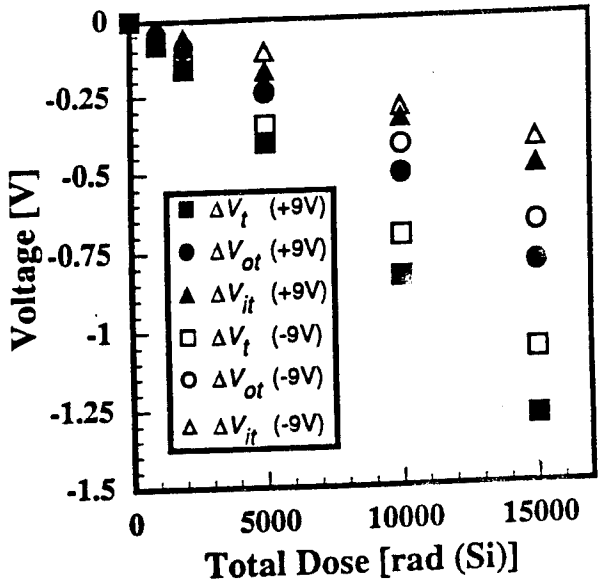


Figure 9: Separated charge for p-channel power MOSFETs (T=81 K). The change in threshold voltage, ΔV_t, change in oxide trapped charge component, ΔV_{ot}, and change in interface trap charge component, ΔV_{it}, are shown. The open symbols correspond to V_g=-9V and the closed symbols correspond to V_g=+9V.

interface traps have associated energies located within the Si bandgap, they are filled and unfilled with electrons depending on the level of the surface potential. This results in a gate voltage dependent charge component that causes stretchout in the subthreshold drain current characteristics. Prompt interface trap generation has been reported at cryogenic (4 K) temperatures in field-oxide transistors [15]. The oxide thickness in these devices is comparable to that in DMOS power transistors (≈ 1000Å). The results from this experiment suggest a considerable interface-trap component. Previous workers have reported that interface-trap creation by radiation is suppressed at cryogenic temperatures [10]; therefore, the measured increase in ΔV_{it} may be an artifact of the measurement technique whose possible causes may be border traps or LNU's.

It has been suggested that all traps which lie within about 30Å of the Si/SiO_2 interface and are in electrical communication with the Si be called border traps [12-14]. Since border traps may have donor or acceptor-type energy levels, they can exchange charge with the channel of the MOSFET. Therefore, border traps can introduce stretchout in the post-irradiation subthreshold drain current measurements. It is very difficult, if not impossible, to distinguish between interface traps and border traps in the DMOS structure using electrical measurements. An electrical method combining conventional threshold voltage measurements and charge pumping exists; however, charge pumping is not possible with the conventional DMOS structure [13]. Techniques such as electron-spin-resonance or spin-dependent recombination that bring forth the defect microstructure may be used to separate border traps from interface traps [12] but were not performed here.

The third defect suggested to be responsible for the stretchout in the subthreshold drain current is lateral non-uniformities in oxide charge (LNU's). LNU's are by definition fixed charge in the gate oxide that has nonuniform spacial density or random deviations in the charge trapped due to statistical fluctuations. The nonuniform distribution of fixed charge results in threshold voltage variations throughout the gate of the MOSFET. The variations in threshold voltage result in different regions of the channel achieving strong inversion at different gate voltages. Since different parts of the MOSFET turn on at different gate voltages, a stretchout (*i.e.*, a decrease in slope) occurs in the subthreshold drain current characteristics of the device. Furthermore, the effects of radiation-induced LNU's should be greater at cryogenic temperatures than at room temperature due to the

increased hole trapping at cryogenic temperatures (*i.e.*, the LNU component is greater in magnitude) [10]. The post-irradiation stretchout in the subthreshold drain current characteristics for p-channel MOSFETs with 260Å gate oxides operated at cryogenic temperatures was attributed to LNU's and not interface traps in the work of Saks [10]. Charge-pumping measurements, which are relatively insensitive to LNU's, were used to separate the radiation-induced charge components in this work. Charge-pumping, however, requires access to the body terminal of the MOSFET - which is not possible with the DMOS power transistor structure (Figure 1).

Three mechanisms: interface traps, border traps, and LNU's, have been identified as possible causes in the stretchout of the subthreshold drain current characteristics. The goal of this work is to point out the radiation response of power MOSFETs operated at cryogenic temperatures. Identifying the correct defect mechanism is left for future work. A key finding in this work is that it has been demonstrated that commercial off-the-shelf power MOSFETs may be suitable for limited total-dose environments when operated at cryogenic temperatures.

IV. SUMMARY

This paper presents the first known results for commercial n- and p-channel power MOSFETs irradiated and characterized at cryogenic temperatures. Significant performance and survivability advantages associated with cryogenic operation of space-borne power MOSFETs are demonstrated. There are three advantages for cryogenic power MOSFET operation in an ionizing radiation environment: (1) steeper subthreshold slope before and after irradiation (improves switching efficiency); (2) lower off-state leakage currents before and after irradiation; (3) larger pre-rad threshold voltage for n-channel devices. Perhaps most importantly, it has been demonstrated that commercial off-the-shelf power MOSFETs may be suitable for limited total-dose environments (*i.e.*, many space applications) when operated at cryogenic temperatures.

V. ACKNOWLEDGMENTS

The authors would like to express their appreciation to Al Hoffland and Roger Tallon from the USAF Phillips Laboratory for their assistance in operating the low-energy x-ray source. The authors would also like to thank C. Frank Wheatley for providing the devices for this experiment.

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IV.L. Comparison of 1/*f* Noise in Irradiated Power MOSFETs Measured in the Linear and Saturation Regions

Comparison of 1/f Noise in Irradiated Power MOSFETs Measured in the Linear and Saturation Regions[1]

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Abstract

1/f noise in n-channel and p-channel power MOSFETs is investigated as a function of total dose and annealing. All the devices used in this study are non-hardened commercial parts. The pre-irradiation noise dependence on the gate and drain biases is analyzed. A different evolution of the noise measured in the linear and saturation regions through irradiation and annealing is reported.

I. INTRODUCTION

1/f noise measurements on MOSFETs have been reported for a long time. 1/f noise is related to defects located at the Si/SiO_2 interface or in the oxide close to the interface [1-3]. Time constants describing the exchange of carriers between these traps and the channel depend on the location of these defects. The use of 1/f noise measurements as a characterization tool for irradiated devices stems from the various kinetics involved in the build-up of defects during irradiation and anneal, resulting in different behaviors of noise magnitude as a function of the total dose and annealing time [4-7].

Most 1/f noise measurements previously reported were done on integrated-circuit MOSFETs biased in the linear region [4-7]. Only saturation region noise measurements have been reported in power MOSFETs [8]. This bias simplifies greatly the noise measurement. Unfortunately, the underlying theory is not as well as understood compared to the linear region technique.

Measurements in power MOSFETs operated in the linear region involve the following problems specific to the structure of power devices:

(1) A power MOSFET contains thousands of identical cells operated in parallel which act as uncorrelated sources of noise. Thus, a power MOSFET is equivalent to a conventional lateral transistor with an extremely large gate area. As the noise level is inversely proportional to the gate area, the overall noise level of power MOSFETs is far below the noise level associated with integrated-circuit MOSFETs.

(2) The magnitude of the static drain current needed to properly bias the transistor in the linear region is drastically increased in comparison to that required in integrated-circuit MOSFETs. This is primarily due to the large gate width of power devices. Furthermore a trade-off must be made between the value of the applied drain and gate voltages needed to achieve a noise significantly higher than the background noise (high V_{DS} and low V_G-V_T), and the set of biases required for a device to be really working in the linear region (low V_{DS} and high V_G-V_T). This necessitates an improved power supply and a reduction in value of the drain load resistor. This in turn leads to heating problems in peripheral components and eventually in the device under test itself. The possibility of further instabilities and inaccuracies of 1/f noise measurements is therefore increased.

These problems are not so critical if noise measurements are taken when the transistor is biased in the saturation region. In that case, the static drain current can be reduced as the noise level increases in saturation by a few orders of magnitude. It is also much easier to meet the requirements for proper biasing in the saturation region. Assuming that the information obtained from saturation region noise measurement is similar to that obtained from noise measurement in the linear region, that method can become an interesting substitute for power devices. Please note that "similar information" means that the trends in the evolution of the noise magnitude agree. However, some differences are expected because of the non-constant surface potential along the channel in saturation.

The 1/f noise measurements in the linear region have been proposed as a characterization tool for radiation-induced defects in integrated-circuit MOSFETs [4-7]. Our goals in this paper are to demonstrate the feasibility of linear region noise measurements in power MOSFETs as well as to evaluate the

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reliability of noise measurements through irradiation and annealing in the saturation region as compared to those performed in the linear region.

II. Experimental Setup

The devices used in this study were non-hardened IRF440 n-channel power MOSFETs and MTM8P08 p-channel power MOSFETs manufactured by Motorola. The main electrical characteristics of these double-diffused vertical transistors are: V_{BR} = 500 V, I_D = 8 A, $r_{DS(on)}$ = 0.85 Ω for the IRF440 and V_{BR} = 80 V, I_D = 4 A, $r_{DS(on)}$ = 0.4 Ω for the MTM8P08. They were irradiated in a ^{60}Co source to a total dose of 17 krad(Si). The dose rate was 750 rad(Si)/hour. During both the radiation exposure and a subsequent anneal, the gates of the transistors were biased at +9 V, while the sources and drains were grounded.

The biasing conditions used for the 1/*f* noise measurements are given in Table 1. These values were kept constant for all measurements through irradiation and annealing. The choice of bias conditions in the linear region is critical for proper device characterization. The transistor must be biased so that pre-irradiation noise levels are significantly above the background noise level. On the other hand, the drain current must be kept low in order to avoid heating effects. The choice of bias conditions in the saturation region is not as critical, and the range of acceptable values is wider.

	IRF440	MTM8P08
Linear region	V_G-V_T = 0.5 V V_{DS} = 0.1 V	V_G-V_T = - 0.5 V V_{DS} = - 0.1 V
Saturation region	V_G-V_T = 0.2 V V_{DS} = 5 V	V_G-V_T = - 0.2 V V_{DS} = - 5 V

Table 1 Bias conditions during 1/*f* noise measurements.

It should be noted that the drain current is not constant through irradiation and annealing. This is due to the degradation of the mobility which is related to the interface trapped charge by a Sun-Plummer type relation proposed by Galloway et al. [9]. With the biases given in table 1 the pre-irradiation current is on the order of 70 mA for the IRF 440.

The biasing circuit is the usual common-source circuit often used for 1/*f* noise measurements. Figure 1 gives a simplified schematic of the experimental setup. Due to the large magnitude of the drain current, batteries have been replaced with an electronic power supply to avoid problems such as biasing variations during measurements and limited operating time. However, in order to maintain a low background noise, custom power supplies were developed. The biasing circuit is AC-coupled to a low noise pre-amplifier (EG&G PAR model113) which is connected to a HP 3582A spectrum analyzer.

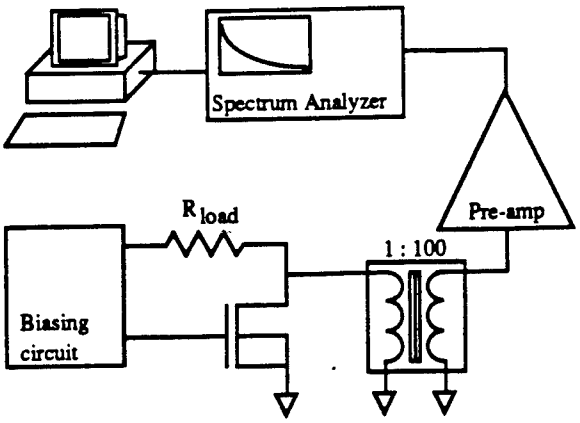


Fig 1 Experimental setup.

In some instances, mainly for pre-irradiation noise measurements, a low noise transformer (EG&G PARC model 1900) was inserted between the biasing circuit and the pre-amplifier to further reduce the background noise. That transformer improves the noise figure of the pre-amplifier when it is connected to a low impedance noise source. The use of the transformer was limited to measurements with a small noise magnitude. This is due to the necessity to add a few correcting factors to compensate the non linearity introduced by the transformer and other isolation circuits. All the measurements, acquisition, and data processing were done on a HP computer connected to the spectrum analyzer. Figure 2 shows the relative amplitudes for the background noise, and 1/*f* noise measured in the linear and saturation regions for a IRF440 n-channel power MOSFET. The background noise is measured by maintaining V_{DS} at 0V.

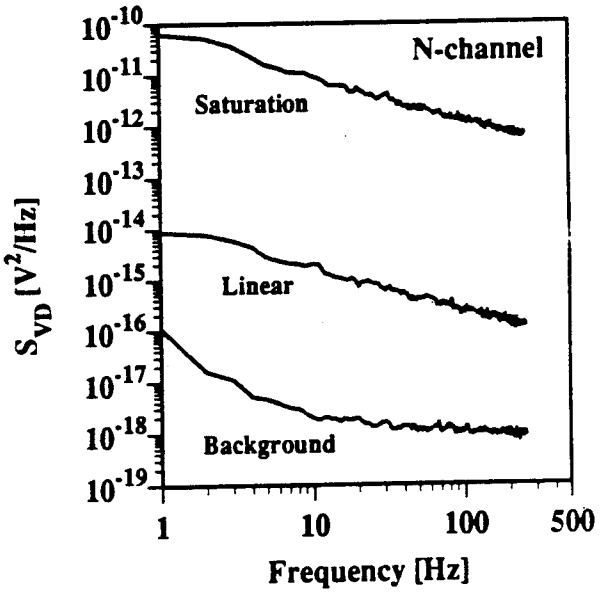


Fig 2 Magnitude of the 1/*f* noise measured in the linear and saturation regions for a n-channel power MOSFET IRF440 compared to the background noise.

For better accuracy, the background noise was always subtracted from the measurements done in the linear region. As the noise is higher by a few orders of magnitude when measured in the saturation region we can simply disregard the background noise. The actual background noise is mainly due to the preamplifier itself.

III. Pre-Irradiation Noise Dependence on Biases

A. Linear Region

The non-uniform doping along the channel of power MOSFETs results in different values of the surface potential along the channel for a given gate voltage. Even though this may be expected to adversely affect the applicability of models used for noise in integrated-circuit MOSFETs, we found that the pre-irradiation noise for n-channel and p-channel transistors as a function of the drain-to-source and gate voltages is well described by [3-7]:

$$S_{Vd} = \frac{K}{f^{\alpha}} \frac{V_{DS}^2}{(V_G - V_T)^2}, \qquad (1)$$

where, V_{DS} is the drain-to-source DC voltage, V_G is the DC gate bias, V_T is the threshold voltage of the MOSFET, f is the frequency, α is a coefficient close to 1, and K is the noise power.

It should be noted that in power MOSFETs, the value of the drain-to-source voltage V_{DS} must be modified by taking the effect of non-negligible drain series resistance into account. The parasitic drain resistance of the thick epi-layer is on the order of a few tenths of ohms. With a drain current close to 100 mA and V_{DS} around 100 mV typical of a noise measurement, the voltage drop across the parasitic resistance can be on the order of the voltage actually applied across the channel. For instance, when performing a measurement of the noise magnitude as a function of V_G -V_T (V_{DS} kept constant), the value of V_{DS} must be corrected to keep the voltage across the channel constant. When the parasitic resistance has been evaluated, its effects are taken into account by subtracting from V_{DS} the voltage drop across r_d due to the drain current. The result is the voltage actually applied across the channel and it must remain constant with V_G -V_T varying and used in equ.1.

Figures 3 and 4 compare the relationship between noise and biasing for a n-channel power MOSFET with and without taking the parasitic resistance, r_d, into account for a constant V_{DS} and V_G -V_T respectively. From the output characteristic of the power MOSFET IRF440 biased in the linear region, the parasitic resistance is found to be equal to 0.55 Ω. Figure 3 shows that S_{Vd} is no longer inversely proportional to $(V_G - V_T)^2$ if the parasitic resistance is neglected. The stronger dependence on V_G-V_T is due to an increasing voltage drop across the parasitic resistance leading to reduced voltage across the channel when the gate bias increases. However, Fig. 4 demonstrates that the relationship between S_{Vd} and V_{DS} shown in Eqn. 1 is quite accurate when V_G-V_T is kept constant. In that case, we slightly over-estimate the voltage across the channel.

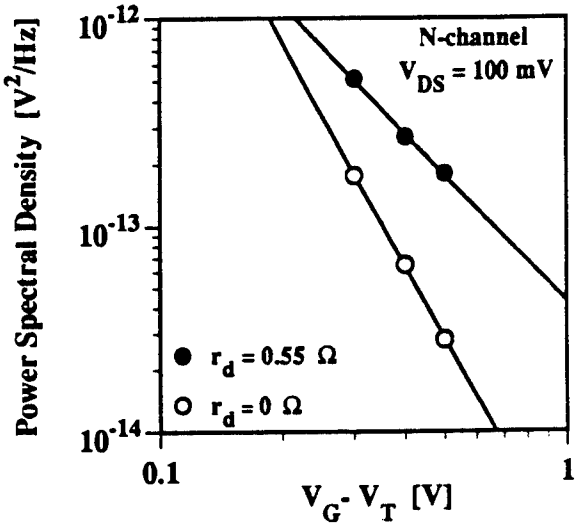


Fig 3 Power spectral density calculated at 1Hz from least-squares fitting of experimental data measured in the linear region as a function of V_G - V_T with V_{DS} kept constant. When the parasitic drain resistance is neglected, S_{Vd} is inversely proportional to $(V_G - V_T)^{3.6}$. If the parasitic resistance is taken into account, experimental data fit very well to Eqn. 1 with S_{Vd} inversely proportional to $(V_G - V_T)^{2.04}$.

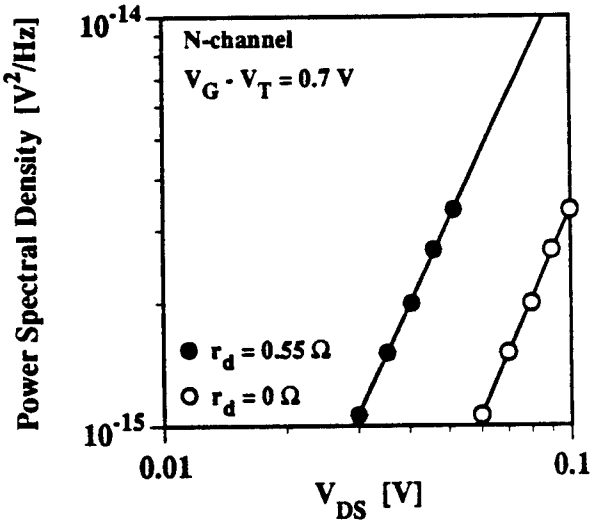


Fig 4 Power spectral density calculated at 1Hz from least-squares fitting of experimental data measured in the linear region as a function of V_{DS} with V_G - V_T kept constant. The fit of experimental data to Eqn. 1 is slightly improved when the parasitic drain resistance is included. S_{Vd} is proportional to $V_{DS}^{2.1}$ compared to $V_{DS}^{2.3}$ if that resistance is neglected.

B. Saturation Region

Pre-irradiation noise measured in the saturation region for the power MOSFETs was found to be an increasing function of (V_G - V_T) and independent of V_{DS} as shown in Eqn. 2. As is the case for linear region measurements, the voltage applied across the channel when the transistor is biased in the saturation region is over-estimated due to parasitic drain resistance. However, in the saturation region, the parasitic resistance has no effect on the noise measurement since the noise does not depend on V_{DS}.

$$S_{Vd} = \frac{K'}{f^{\alpha}}\left(V_G - V_T\right)^{\beta} \qquad (2)$$

Here β is a positive coefficient varying between 2 and 3 for the power MOSFETs.

IV. Results and Discussion

The midgap charge separation technique was used to determine the contributions of oxide-trapped charge (ΔV_{ot}) and interface-trapped charge (ΔV_{it}) to the threshold voltage shift (ΔV_T) [10]. As expected, for n-channel power devices as well as for p-channel devices, oxide-trapped charge and interface states are created during irradiation. The subsequent anneal was performed at room temperature for the n-channel devices. However, for the p-channel devices, even though most of the annealing was done at room temperature, a few measurements were taken after the annealing temperature was raised to 80°C to increase the very slow annealing rate. Figures 5 and 6 show the relative contributions of oxide-trapped charge and interface-trapped charge to the threshold voltage for n-channel and p-channel power MOSFETs respectively.

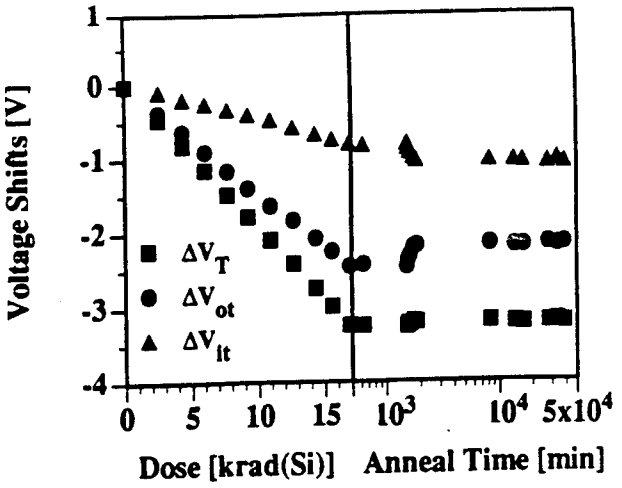


Fig 6 Evolution of ΔV_T, ΔV_{ot}, and ΔV_{it} for a p-channel power MOSFET MTM8P08 through irradiation and anneal. Most of the annealing was done at room temperature with a bias of +9V on the gate while source and drain were grounded. Due to the very slow annealing rate, some measurements were taken after the annealing temperature was increased to 80°C (from 1500 to 2000 min.).

The increase in the noise magnitude measured in the linear and in the saturation region as a function of the total dose is illustrated in Figs. 7 and 8 for n-channel and p-channel power MOSFETs respectively. In both n-channel and p-channel transistors, the noise measured in the linear region increases by more than one order of magnitude after a total dose of 17 krad(Si). However, the noise measured in the saturation region remains almost unchanged fluctuating around an average value.

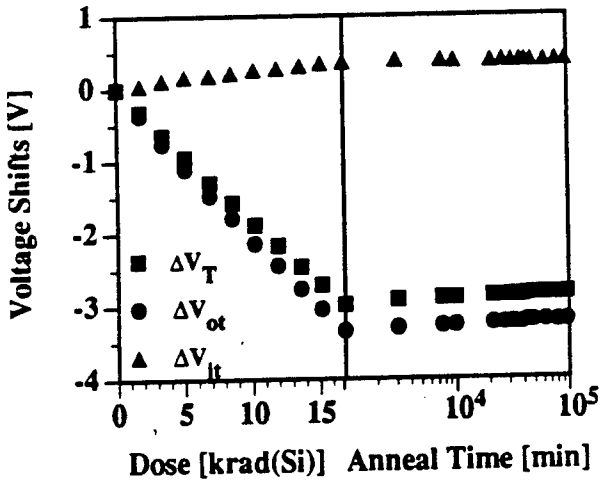


Fig 5 Evolution of ΔV_T, ΔV_{ot}, and ΔV_{it} for a n-channel power MOSFET through irradiation and anneal. The annealing was done at room temperature with a bias of +9V on the gate while the sources and drain were grounded.

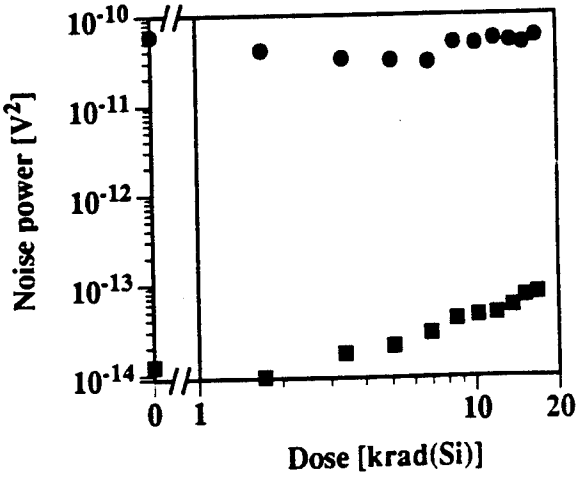


Fig 7 Comparison of the noise measured in the linear region (squares) and in the saturation region (circles) for a n-channel power MOSFET IRF440. The biases are those reported in Table 1.

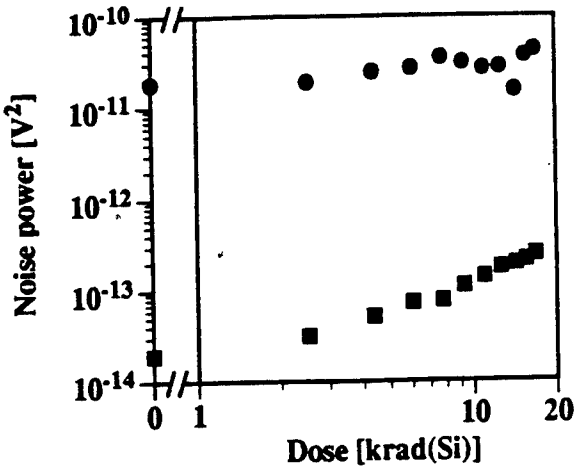


Fig 8 Comparison of the noise measured in the linear region (squares) and in the saturation region (circles) for a p-channel power MOSFET MTM8P08. The biases are those reported in Table 1.

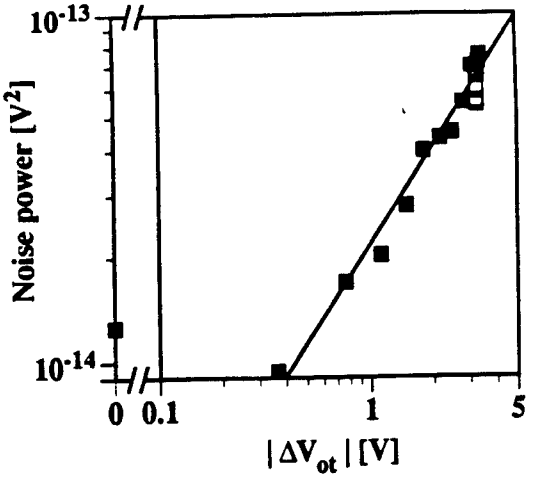


Fig 10 Magnitude of the 1/*f* noise measured in the linear region for a n-channel power MOSFET IRF440 as a function of ΔV_{ot} through irradiation (closed symbols) and annealing (open symbols).

A correlation between noise measured in the linear or saturation region and ΔV_{ot} and ΔV_{it} was investigated for both n-channel and p-channel power MOSFETs. Figures 9 and 11 show how the 1/*f* noise is affected by the irradiation and the subsequent anneal for the n-channel and p-channel power MOSFET respectively.

A comparison between Fig. 9 and Fig. 5 illustrates that the noise is increasing when the contribution of oxide-trapped charge to the threshold voltage shift is increasing during the irradiation and decreasing when the contribution of oxide-trapped charge to the threshold voltage shift is decreasing during the annealing. Figure 10 confirms that correlation showing that the noise is varying with ΔV_{ot} at the same rate through irradiation and annealing.

However, it should be noted that at the same time, the contribution of interface-trapped charge to the threshold voltage shift is increasing during the irradiation as well as during the annealing. Even though the build-up of interface-state charge is not obvious in Fig. 5 during the annealing, that trend suggests no correlation between interface-state charge and noise.

Considering now the p-channel power MOSFETs, Figs. 11 and 12 depict the evolution of the noise magnitude through irradiation and annealing. Comparing Fig. 6 with Fig. 11 shows that now the noise is increasing when the contribution of interface-trapped charge to the threshold voltage shift is increasing. That apparent correlation is well confirmed by Fig. 12 which shows that the noise is increasing with the same rate during irradiation and anneal.

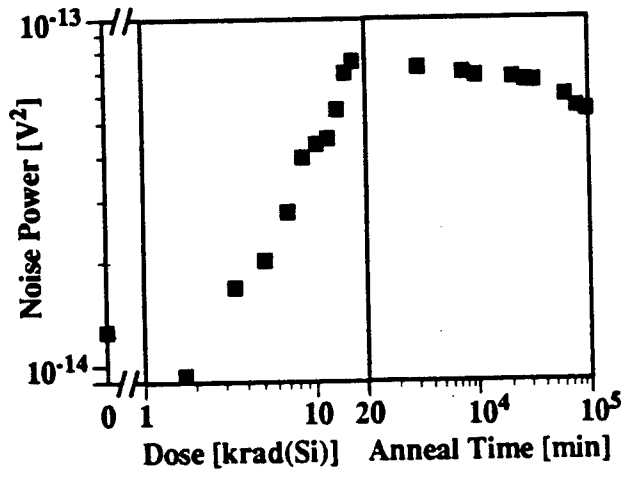


Fig 9 Evolution of the 1/*f* noise for a n-channel power MOSFET IRF440 biased in the linear region through irradiation and anneal.

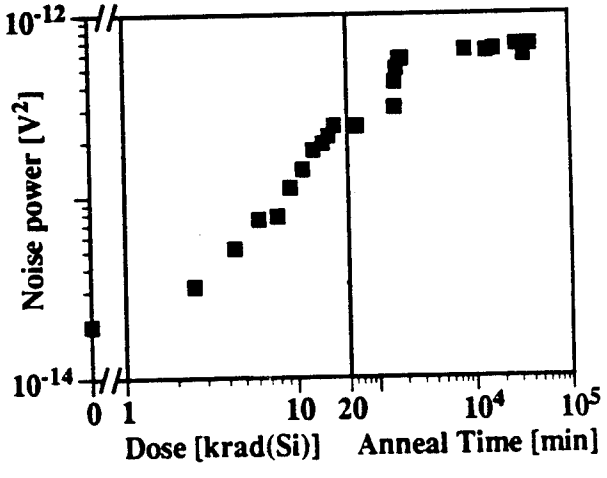


Fig 11 Evolution of the 1/*f* noise for a p-channel power MOSFET biased in the linear region through irradiation and anneal.

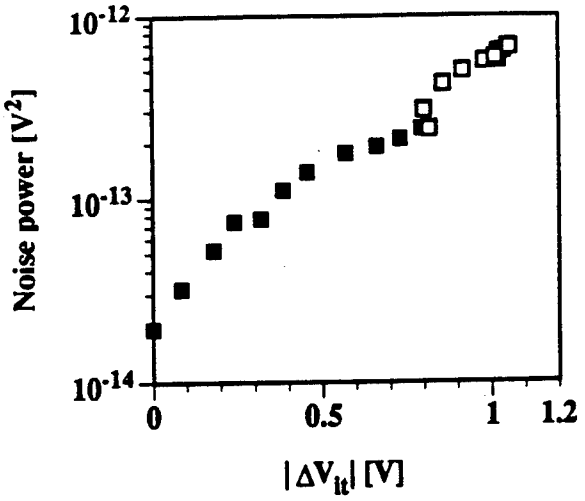


Fig 12 Magnitude of the 1/*f* noise measured in the linear region for a p-channel power MOSFET as a function of ΔV_{it} through irradiation (closed symbols) and annealing (open symbols).

In summary, the noise measured in the linear region correlates with ΔV_{ot} (and not ΔV_{it}) for the n-channel devices through irradiation and anneal [5,7]. However, for the p-channel devices, the noise continues to increase during annealing despite a decrease in ΔV_{ot}, indicating better correlation with ΔV_{it}. The change in the noise measured in saturation was much less pronounced for both n-channel and p-channel devices.

The distinction between interface traps and oxide trapped charge depends on the time scale over which the measurement is made. States that exchange charge with the silicon more rapidly than the measurement signal varies are identified as interface traps. The differences between n- and p-channel devices suggest that there may be differences in the time constants involved. Differences between linear and saturation region are the result of the strongly non-uniform potential distribution along the channel in saturation.

The noise slope (α in Eqns. 1 and 2) of all the parts was not significantly affected by irradiation and subsequent anneal and remained in the range from 0.85 to 1.09.

V. Conclusions

The noise behavior of both n-channel and p-channel power transistors is investigated. Noise measurements on power devices biased in the linear region are reported for the first time. A proper choice of bias conditions is essential for applicability of linear region 1/*f* noise measurements in these devices, in light of problems specific to power MOSFETs biased in the linear region.

Pre-irradiation noise and its evolution through irradiation and anneal are found to be in agreement with previously published results for integrated-circuit MOSFETs biased in the linear region [4-7]. Furthermore, the build-up of interface traps was found to correlate well with the increase of noise during annealing for the p-channel devices.

Measurements taken in the saturation region do not correlate as well with radiation-induced charge build-up, even though the overall noise increases slightly during irradiation.

VI. Acknowledgments

The authors would like to express their gratitude to Dr. J. Gasiot from the University of Montpellier (France) and to Mr. J. C. Boudenot from Thomson-CSF Electronic Systems Division for their help and support during this work.

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IV.M. 1/*f* Noise and Interface Trap Density in High Field Stressed *p*MOS Transistors

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1/f NOISE AND INTERFACE TRAP DENSITY IN HIGH FIELD STRESSED pMOS TRANSISTORS

J. L. Todsen, P. Augier, R. D. Schrimpf and K. F. Galloway

Indexing terms: Electron devices, Noise, Metal oxide semiconductor structures and devices, Transistors, Field-effect transistors

Experimental results for *p*MOS transistors subjected to high field stressing are reported. 1/*f* noise and interface trap density increase with stress time. A direct relationship between the increase in 1/*f* noise and interface trap density during the high field stressing is observed.

Introduction: Early in the study of 1/*f* noise in MOS devices, Klaassen [1] and Broux *et al.* [2] reported a direct relationship between 1/*f* noise and interface trap density D_{it} in *p*MOS transistors. The device under test (DUT) was biased in the saturation region. By modifying the fabrication process for the different test samples, they were able to produce a spread of D_{it} values in which they measured the corresponding 1/*f* noise. Recently, studies on power *p*MOS transistors subjected to ionising radiation show a similar direct relationship between the noise and D_{it} through irradiation and subsequent anneal [3].

This Letter presents the results of linear region 1/*f* noise and D_{it} measurements performed on *p*MOS transistors subjected to high electric field stressing of the gate oxide. High electric fields imposed across the oxide allow electrons to tunnel through the oxide via Fowler–Nordheim (FN) tunnelling [4]. These tunnelling electrons create additional traps in the oxide [5]. For the *p*MOS transistors studied, the 1/*f* noise increases during the high field stressing. By plotting the 1/*f* noise as a function of D_{it}, a direct relationship between the increase in these two parameters is observed.

Experimental details: The *p*MOS transistors used in the experiment had a gate oxide thickness of 180 Å and a surface doping concentration of $3 \times 10^{16}\,cm^{-3}$. The drawn dimensions of the transistors were $W = 10\,\mu m$ and $L = 1{\cdot}75\,\mu m$. The transistors were high field stressed by forcing a constant current from the gate terminal. With the source, drain and substrate grounded, a current source (HP 4145B) forced 1 mA/cm² out of the gate for a total of 5000 s corresponding to a total fluence of 5 C/cm² through the oxide. The average charge-to-breakdown Q_{BD} was measured with a current density of 10 mA/cm² and was found to be ~60 C/cm². The average measured electric field across the oxide as a result of the constant gate current was ~10 MV/cm. Periodic interruptions of the stressing allowed the 1/*f* noise and D_{it} to be measured.

Fig. 1 shows the setup used to measure the 1/*f* noise. During the measurements, the transistors were biased in the linear region with the following DC biases: $V_{DS} = -0{\cdot}1$ V and $V_{GS} = -1{\cdot}0$ V. The biasing circuit provided extremely low noise voltage supplies to the gate and drain resistor of the DUT. Typically, the system background noise was almost two orders of magnitude below the pre-stress measured 1/*f* noise. The value of the external biasing resistor R_D (500 kΩ) was much larger than the fluctuating channel resistance of the DUT and therefore did not significantly affect the noise measurements. The preamplifier (EG&G PARC Model 113) amplified the drain noise of the DUT by a factor of 5000 to levels more suitable for the spectrum analyser (HP 3582A). The spectrum analyser measured the noise in the range 2–250 Hz. The personal computer (HP 9816) controlled the spectrum analyser over the general purpose interface bus (GPIB). The power spectral density of the 1/*f* noise was calculated using a least squares routine.

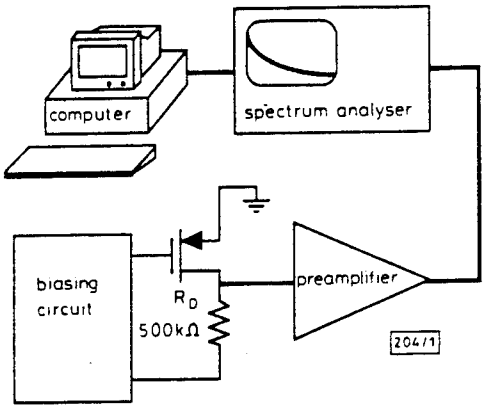


Fig. 1 *Block diagram of 1/f noise measurement system*

The measured 1/*f* noise followed the widely reported relationship [6–8]

$$S_{V_d} = \left[\frac{V_{DS}}{(V_{GS} - V_T)}\right]^2 \frac{K}{f} \quad (1)$$

where V_{DS} and V_{GS} are the DC bias conditions, V_T is the threshold voltage, f is the frequency in hertz and K the noise constant. Eqn. 1 assumes that the 1/*f* noise originates from fluctuations in the number of carriers in the channel as proposed by McWhorter [9]. The experimental results Section presents the 1/*f* noise results in terms of the noise constant K rather than the power spectral density S_{V_d} to remove the bias condition dependency shown in eqn. 1.

Average D_{it} was measured using the charge-pumping technique presented by Groeseneken *et al.* [10]. Verification measurements assured that no significant 'geometric component' was present in the charge-pumping measurements.

Experimental results: Fig. 2 shows the noise constant K as a function of log stress time for three identical devices. The break in the x axis in Fig. 2 on the left side indicates that the initial ($t = 0$) or 'PRE' value of K is included on the log time scale. From Fig. 2, K is seen to steadily increase with log

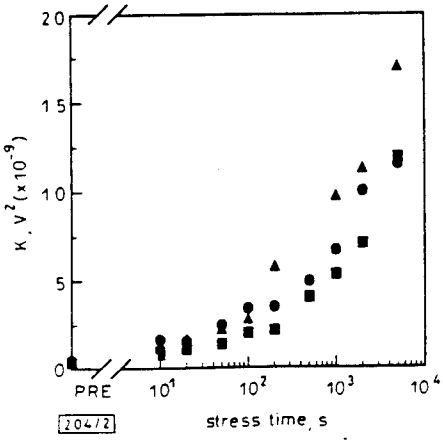


Fig. 2 *Noise constant K against log stress time*

● device 1
▲ device 2
■ device 3

stress time. The average D_{it} values as a function of log stress time for the same three devices are shown in Fig. 3, again with the 'PRE' value included. The observed increase in D_{it} with stress time agrees with previously published results [5].

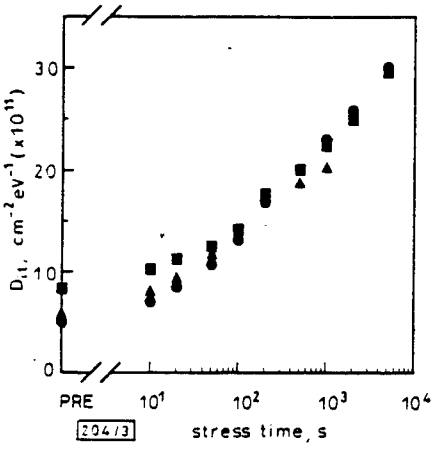


Fig. 3 *D_{it} against loss stress time*

● device 1
▲ device 2
■ device 3

Relating shifts or increases in K to D_{it} provides an easy way to directly compare the data of Figs. 2 and 3. In Fig. 4, the increase in the noise constant K is plotted as a function of the increase in average D_{it}. As can be seen, K and D_{it} increase in direct proportion during the high field stressing.

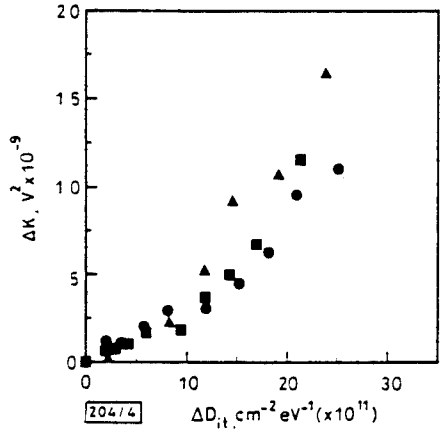


Fig. 4 *Increase in noise constant K against increase in D_{it}*

● device 1
▲ device 2
■ device 3

Conclusions: For *p*MOS transistors subjected to high field stress, a direct relationship between the increase in linear region $1/f$ noise and D_{it} is observed. This correlation during high field stressing is in agreement with measurements previously performed on differently processed devices and devices subjected to ionising radiation [1–3].

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PRMA EFFICIENCY IN ADAPTIVE TRANSCEIVERS

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Indexing terms: Transceivers, Signal processing, Adaptive systems

The effects of different speech source rates and various number of modulation levels on packet reservation multiple access (PRMA) efficiency in an adaptive transceiver are investigated under the constraint of fixed channel bandwidth and benign cochannel interference in office type cordless telecommunications (CT) environments. The number of PRMA users supported in a 200 kHz frequency slot ranges from 17 to 103, the required user bandwidth is between 11·8 and 1·94 kHz, and the number of PRMA users per slot is between 1·7 and 1·94, respectively.

Introduction: It is envisaged that in intelligent third generation personal communications networks (PCN) the transceivers can adaptively reconfigure themselves in order to meet time-varying optimisation criteria.* In this Letter the effect of using packet reservation multiple access (PRMA) in conjunction with adaptive transceivers incorporating full-rate, half-rate and quarter-rate speech codecs as well as 1, 2 and 4 bit/symbol modulation schemes is investigated.

System description: We focus our experiments on an adaptive cordless telecommunications (CT) transceiver, where the modulated signal fits in a 200 kHz channel slot used in the Pan-European mobile radio system, known as GSM. The full-rate speech source codec generates a 260 bit/20 ms = 13 kbit/s information stream, which is channel coded to 456 bit/20 ms = 22·8 kbit/s. However, instead of the complex GSM control infrastructure [2] here we opt for a low-delay, low-complexity control scheme using a 64 bit header, favoured in office-type CT schemes [2]. With this 64 bit header the source information rate becomes (456 + 64) bits per 20 ms, i.e. 520 bit/20 ms = 26kbit/s. Similarly, the half-rate codec generates (228 + 64) = 292 channel coded bits per 20 ms, yielding a

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IV.N. Investigation of Possible Sources of 1/f Noise in Irradiated N-Channel Power MOSFETs

Investigation of Possible Sources of 1/*f* Noise in Irradiated n-Channel Power MOSFETs†

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Abstract

1/*f* noise in irradiated n-channel power MOSFETs is compared to interface- and oxide-trapped charge densities. The noise follows the bias dependences predicted by an equation based on the number fluctuation model derived for noise in the saturation region. The magnitude of the noise switched between two distinct levels when the bias was reversed during post-irradiation annealing. The noise did not correlate well with interface traps or oxide trapped charge. Border traps provide a reasonable explanation, with charge compensation being an important effect. During positive-bias annealing, near-interfacial traps are compensated and no longer contribute to the 1/*f* noise. However, when the bias is reversed, the traps are decompensated and the noise increases again.

I. INTRODUCTION

Oxide defects in metal-oxide-semiconductor (MOS) devices are usually divided into two types: interface traps and oxide traps. Recently, however, Fleetwood has defined a third class of traps called "border traps" [1-3]. These traps may be physically identical to oxide traps (trapped positive charge), but are located close enough to the Si/SiO_2 interface that they can exchange charge with the silicon on a short enough time scale that they behave like interface traps in many electrical measurements. These traps lie within about 3 nm of the Si/SiO_2 interface, although the precise distance depends on the time scale of the measurement.

One of the measurements that might be expected to be most affected by border traps is 1/*f* noise. The exact cause of 1/*f* noise has long been debated, with some authors observing correlations between noise and interface traps [4-6], and others between noise and oxide traps [7-9]. An emerging consensus is that the noise is due to near-interface oxide traps that are capable of exchanging charge with the silicon on time scales that produce the observed low frequency 1/*f* noise [2]. Such traps are, by definition, border traps. To investigate the behavior of 1/*f* noise in power MOSFETs, devices were characterized following irradiation and during subsequent high temperature biased anneals.

In section II, a noise equation based on the McWhorter number fluctuation theory for a MOSFET biased in the saturation region is derived. Noise was measured in the saturation region because the noise is inversely proportional to gate area, and the gate area of the power MOSFETs used was very large [10]. Biasing the devices in the saturation region increases the noise magnitude, making it easier to measure. Section III describes the experiment. Then the results are presented and discussed in section IV.

II. NOISE THEORY

The noise equation derived here is for a MOSFET biased in the saturation region. Coordinates are defined as shown in Figure 1. The derivation is based on the McWhorter number fluctuation model [11], which attributes 1/*f* noise to carriers from the channel tunneling to traps in the oxide. The tunneling through the energy barrier has a characteristic time given by [12]

$$\tau_T = \tau_0 \exp(2\alpha x), \tag{1}$$

where x is the distance from the channel to the trap (the barrier thickness), τ_0 is a constant generally taken to be about 10^{-10} s, and α is given by [9]:

$$\alpha = \sqrt{\frac{8\pi^2 m_e^* \phi_B}{h^2}} \tag{2}$$

where m_e^* is the effective mass of the electron in the oxide, ϕ_B is the barrier height, and h is Planck's constant.

Begin by considering a small volume ΔV in the oxide, and an energy range ΔE. If this volume element is small enough that all traps within it are characterized by the same time constant τ_T, then the power spectral density of fluctuations in the number of carriers in this element is [11]:

$$S_{N_T \Delta V \Delta E} = \frac{\tau_T}{1 + \omega^2 \tau_T^2} N_T(x, E) f_T (1 - f_T) \Delta V \Delta E, \tag{3}$$

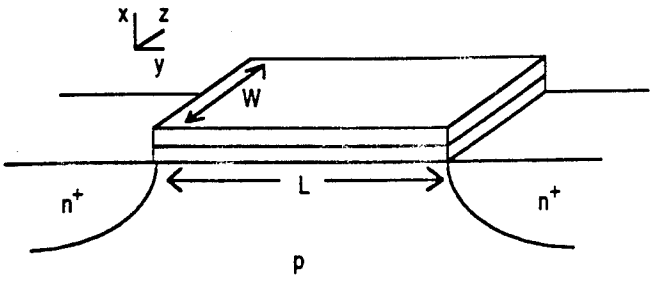


Fig. 1: Definition of coordinate system in MOSFET. Distances in x are measured from the Si/SiO_2 interface.

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where ω is the frequency in radians per second, $N_T(x, E)$ is the trap density (in $cm^{-3}eV^{-1}$), and f_T is the Fermi factor:

$$f_T = \frac{1}{1 + \exp\left(\frac{E_T - E_{Fn}}{kT}\right)}, \quad (4)$$

with E_T being the trap energy level, and E_{Fn} is the electron quasi-Fermi level.

For a MOSFET biased in saturation, a charge fluctuation will cause a drain current fluctuation given by

$$\delta I_D = \mu C_{ox} \frac{W}{L} (V_G - V_T) \delta V_T, \quad (5)$$

where μ is the mobility, C_{ox} is the oxide capacitance per unit area, V_G is the gate voltage, and δV_T is the change in threshold voltage due to fluctuations in channel carriers, given by

$$\delta V_T = \frac{q}{C_{ox}} \frac{\delta N_T}{WL} \Delta V \, \Delta E \ . \quad (6)$$

This assumes that each channel carrier fluctuation momentarily neutralizes a trapped hole in the oxide, affecting the threshold voltage. This gives rise to a drain current power spectrum of:

$$S_{I_D \Delta V \Delta E} = \frac{\mu^2 q^2 (V_G - V_T)^2}{L^4} S_{N_T \Delta V \Delta E} \cdot \quad (7)$$

Using eq. (3) in (7) and integrating over y and z gives:

$$S_{I_D} = \frac{2q^2\mu^2 (V_G - V_T)^2 W}{L^3} \int\int \frac{\tau_T}{1+\omega^2\tau_T^2} N_T(x,E) f_T (1-f_T) dx dE \quad (8)$$

The integral of $N_T(x, E)f_T(1-f_T)dE$ is approximately $kTN_T(E_{Fn})$. The remaining integral over x can be evaluated by changing variables to τ_T. Assuming a uniform trap distribution, this integral yields $1/4\alpha f$, resulting in

$$S_{I_D} = \frac{q^2 kT \mu^2 W (V_G - V_T)^2}{L^3 \alpha} N_T(E_{Fn}) \frac{1}{f} \cdot \quad (9)$$

Using the drain current equation for saturation and multiplying by R_D^2 (drain resistance squared), we obtain

$$S_{V_D} = \frac{2q^2 kT}{\alpha (WL) C_{ox}^2} \frac{R_D^2 I_D^2}{(V_G - V_T)^2} N_T(E_{Fn}) \frac{1}{f} \quad (10)$$

for the drain voltage noise power spectrum.

This noise equation predicts that the noise depends on the bias through the term $R_D^2 I_D^2/(V_G-V_T)^2$. This dependence is demonstrated in Fig. 2, which shows measured noise versus $R_D^2 I_D^2/(V_G-V_T)^2$ for a single MOSFET biased with different values of R_D, I_D, and V_G. The dependence is linear as predicted, but requires use of a value of V_T slightly lower (by approximately 0.2 V) than that obtained from linear extrapolation of the square-root-of-I_D vs. V_G curve.

Due to the MOSFET being biased in the saturation region, several inaccuracies are added to the noise equation. The main difficulty is that the potential along the channel is not constant in saturation. This is less a problem in the DMOS (Double-diffused MOS) devices used than in transverse MOSFETs, because the doping along the channel is nonuniform, so a nonuniform potential exists along the channel even with a linear region bias. Because of the saturation region bias and the nonuniform doping, the term $N_T(E_{Fn})$ should actually be a trap distribution for a range of energies along the channel.

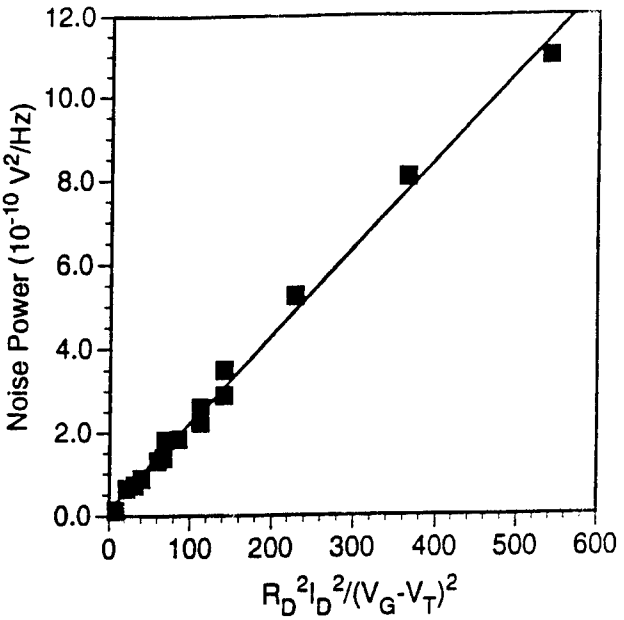


Fig. 2 : Noise from a single MOSFET versus $R_D^2 I_D^2/(V_G-V_T)^2$ for various biases.

Augier *et. al.* have previously compared noise measured in the saturation and linear regions in power MOSFETs, and found that noise measured in the saturation region changed very little during irradiation [10]. Measurements were made using a constant value of (V_G-V_T). The value of I_D, however, could not remain constant because of changes in the mobility during the irradiation. If Augier's noise measurements are corrected by dividing by the square of the normalized mobility (because $I_D^2 \propto \mu^2$ in eq. (10)), the saturation noise behaves very similarly to the linear region noise. In this experiment, the normalization affected only the magnitude of changes in the noise; the general trends were not affected.

Another approximation made in the derivation is the assumption that the traps causing the noise are uniformly distributed in the oxide. For a nonuniform distribution, the noise spectrum will not be $1/f$, but will rather be $1/f^b$, where the exponent b will be less than 1 for a trap distribution skewed towards the interface, and will be greater than 1 for a trap distribution skewed away from the interface [9,13].

III. EXPERIMENT

The transistors used in this experiment were commercial IRF440 n-channel power transistors produced by Motorola with gate oxide thickness of approximately 110 nm. The noise was measured from 2 Hz to 250 Hz on an HP3582A Spectrum Analyzer using 256 averaged measurements for each frequency. The noise was input to the spectrum analyzer through a PAR 113 amplifier, which amplified the noise by a factor of 5000. The transistor under test was biased using a specially-built low noise biasing circuit which provided a constant drain voltage. The transistors were biased with a drain current of 5 mA and a drain

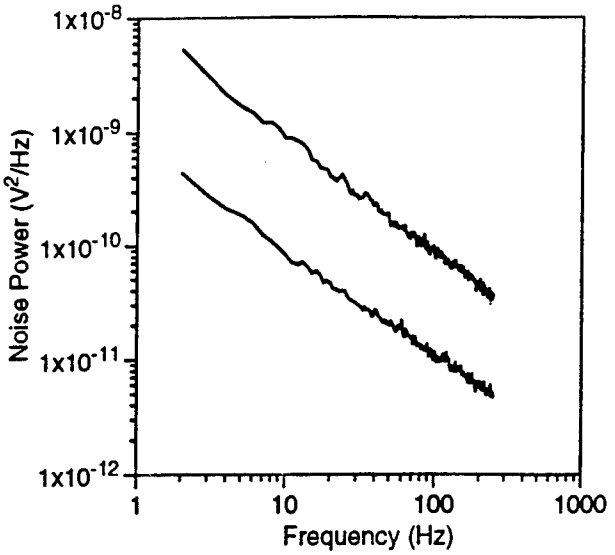


Fig. 3: Typical $1/f$ noise power spectra from 2 to 250 Hz. The lower curve is for an unirradiated IRF440 power MOSFET, the upper curve for the same device after irradiation and high temperature negative bias anneal.

voltage of 3 V during the measurement. The drain resistor used was 1 kΩ.

The measured noise at selected frequencies was downloaded from the spectrum analyzer by an HP9816 computer. The computer performed a least-squares line fit on the logarithm of the data to obtain the magnitude A and frequency exponent b of the noise, as defined in eq. (11)

$$S_{V_D} = \frac{A}{f^b} \tag{11}$$

Noise at 60 Hz and its harmonics were not used in the line fitting to eliminate noise pickup from external power sources. Typical measured $1/f$ noise is shown in Fig. 3.

As seen in eq. (10), the noise varies as $R_D^2 I_D^2/(V_G-V_T)^2$. The values of R_D and I_D were kept constant for each measurement, but (V_G-V_T) could not also remain constant, because of changes in mobility through irradiation and anneal. To account for this, noise magnitude measurements were divided by the normalized mobility. This method was chosen rather than dividing by $(V_G-V_T)^2$ because the required value of V_T was not the value obtained from the square-root-of-I_D vs. V_G curve, as discussed in Sec. II.

At the time of each noise measurement, I_D vs. V_G curves were also measured. These curves were measured on an HP4145B Semiconductor Parameter Analyzer, and were used to calculate threshold voltage shifts, and to determine the amount of shift due to interface trapped charge (ΔV_{it}) and oxide trapped charge (ΔV_{ot}) using the charge separation technique of McWhorter and Winokur [14]. The quantities ΔV_{it} and ΔV_{ot} are directly proportional to changes in the amount of interface trapped charge (N_{it}) and oxide trapped charge projected to the interface (N_{ot}), respectively. Border traps, of greatest interest here, are divided between the N_{ot} and N_{it} effects measured here. In addition, the square of the slope of the square-root-of-I_D vs. V_G curve was used as a measure of the mobility. All mobility values were divided by the initial pre-irradiation value to obtain a normalized mobility.

The devices were irradiated in a ^{60}Co source at a dose rate of 34 rad(Si)/min to a total dose level of 13.4 krad(Si). During the irradiation, the source and drain of each device was grounded and +9 V was applied to the gate.

After irradiation, the transistors were annealed at 100°C. High temperature annealing was used to accelerate the changes in the traps involved. Periodically, measurements of noise and I_D versus V_G were made at room temperature after the devices had cooled. During the anneal, the devices were biased at +9 V for positive bias anneals, or –9 V for negative bias anneals. The devices were annealed under positive bias for 80 hr, then negative bias for 80 hr, then positive and negative again, each for 80 hr.

IV. Results and Discussion

The noise magnitude measured for a typical device is shown in Fig. 4. The response is very similar to that seen in [7], with the biggest difference being during the first positive bias anneal. The magnitude clearly switches between two levels for positive and negative anneals. The values of ΔV_{it} and ΔV_{ot} are shown for the same device in Fig. 5. The noise clearly does not correlate with ΔV_{ot}, which decreases in magnitude during the initial positive bias anneal, while the noise increases. There is a qualitative correlation between the noise and ΔV_{it}, but it is quantitatively a poor correlation. During the first positive bias anneal, ΔV_{it} increases by 0.18 V, and the noise by 3×10^{-9} V²/Hz; when the bias becomes negative ΔV_{it} increases by 0.12 V, which is about two thirds of the increase under positive bias, but the noise increases by 14×10^{-9} V²/Hz, which is over four times as large as the increase under positive bias. Since the noise is directly proportional to the trap density, as seen in eq. (10), interface traps do not provide a good explanation for the $1/f$ noise.

The noise results can be explained simply in terms of border traps and charge compensation. Border traps can be measured using the dual-transistor border trap technique [15] or by capacitance-voltage hysteresis [16]. Neither of these techniques has been extended to power MOSFETs. Although border traps were not measured directly here, their expected behavior can be inferred from the measured values of ΔV_{it} and ΔV_{ot}.

The initial increase of noise during the first positive bias anneal is similar to the increase in ΔV_{it} during this time. This increase in interface traps is frequently seen, and often explained by mechanisms involving transport of hydrogen ions released from trap sites in the oxide. The positive bias moves the ions to the interface, where various theories hypothesize a reaction which produces new interface traps. It is likely that some of these ions might be captured after breaking strained Si-Si bonds, which should be relatively plentiful in the near interface region [17]. This would create new trapped positive charge in the near interface region, which, if close enough to the interface, will be border traps. Thus, border traps could be expected to increase during the early portion of a positive bias anneal. The increase in noise during the early positive-bias anneal matches the expected behavior of border traps.

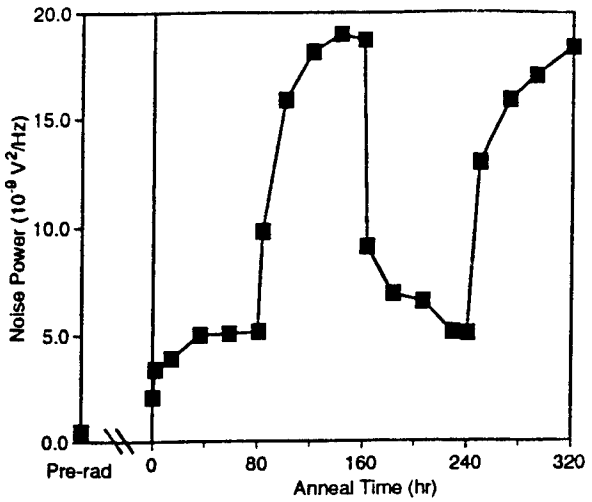


Fig. 4: Noise for a typic device irradiated to 13.4 krad(Si) and annealed at 100 °C. Anneal bias was +9 V for the first 80 hours, -9 V for the second 80 hrs, +9 for the next 80 hrs, and -9 V for the last 80 hrs. Noise has been divided by the normalized mobility to account for biasing.

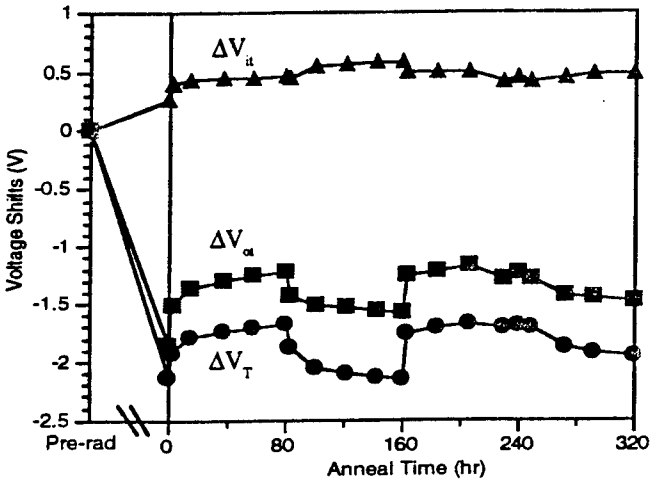


Fig. 5: Voltage Shifts for same MOSFET shown in Fig. 4.

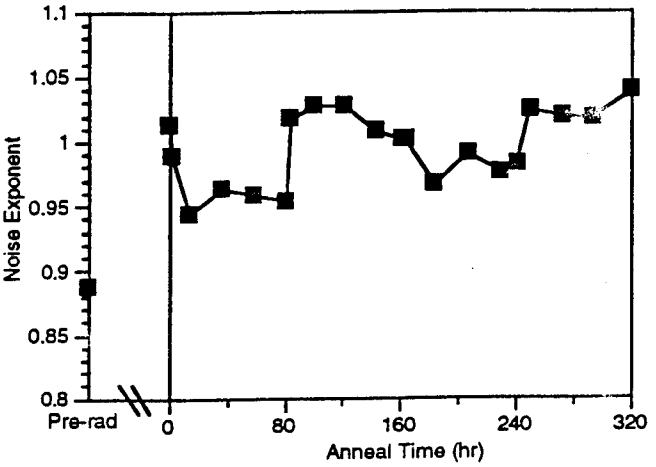


Fig. 6: Exponent for $1/f^{\alpha}$ noise for same MOSFET shown in Figs. 4 and 5.

When the anneal bias is negative, charge decompensation [18, 19] is responsible for the large increase in noise. During the positive-bias anneal, electrons are attracted into the oxide, where they can be trapped at or near trapped-positive-charge sites. The new electron electrically compensates the trap's positive charge, thereby neutralizing it as a source of carrier fluctuations in the channel. Fleetwood *et. al.* have shown that as many as 75% of traps in an oxide might be so compensated [20, 21]. When a negative bias is applied, the electric field can pull the electrons back out of the centers associated with the trapped positive charge and into the silicon, leaving the trap active again. This decompensation accounts for the large increase in noise under negative bias, as well as the increases in the measured ΔV_{ot} and ΔV_{it}, since some of the border traps will behave as interface traps and so be included in ΔV_{it}. Because charge compensation is reversible, it accounts well for the switching seen in the noise [2].

By definition, border traps can exchange charge easily with the substrate, so they are very susceptible to charge compensation. Indeed, if the border traps are the sole cause of the noise, the change in noise magnitude indicates that 75% of the border traps are being compensated. By comparison, only 25% of the bulk oxide trapped charge produced by the irradiation is being compensated (as measured by the midgap separation technique).

Use of a charge compensation model with the noise model implies a need for two types of electron trapping: a short-term (<1 s) trapping/releasing to produce the noise, and a longer-term trapping for the charge compensation. In the Lelis and Oldham model [18, 19], the compensation trapping is associated with the formation of an electron-spin pair. Once formed, this pair is stable enough to last long periods of time (minutes to days), with the duration both bias and temperature dependent. The second trapping mechanism, which produces the noise, is due to the trapped positive charge, which produces an energy level which electrons can tunnel into and out of with relative ease, creating $1/f$ noise. When the trap site is compensated, the net charge is zero, leaving the trapped hole ineffective (or at least greatly reduced in effectivity) in noise trapping.

The noise exponents seen during the experiment varied from approximately 0.88 (in unirradiated MOSFETs) to 1.04. The exponents measured for one device are shown in Fig. 6. Although the value change during the first bias switch is not large, it is larger than the variation in exponent values generally seen, which is about ±0.02. In addition, this behavior was evident in all the devices used, so we believe there is a definite, if small, correlation between the exponent and anneal bias. The pre-irradiation value indicates that the trap density is significantly skewed towards the interface. The radiation produces a fairly uniform trap distribution, making the exponent near unity. The positive bias anneal produces slightly lower exponents than does the negative bias, indicating that the positive bias moves the trap distribution towards the interface, and the negative bias skews it away from the interface. This is consistent with holes being pushed toward the interface under positive bias, and pushed away under negative bias. This may indicate that border traps, which are simply trapped holes, can be physically moved under the biased anneals. Alternatively, this may be an issue of changes in en-

ergy distributions due to the changes in charge distribution caused by charge compensation; the exponent has been found to depend on energy distribution as well as location distribution of the traps [13].

V. CONCLUSION

1/*f* noise measured during annealing of irradiated MOSFETs did not correlate well with either oxide or interface trapped charge, but is explained in terms of border traps. Charge compensation and decompensation were also found to be important mechanisms in interpreting the results. The concepts of border traps and charge compensation may be sufficient to explain a wide array of 1/*f* noise results. Because the border traps are located in the near interface region where stresses are greatest [17] and dependence on processing is strong, their properties may vary considerably from one technology to another [15]. The greatest usefulness of 1/*f* noise may be in investigating the properties of this region.

Acknowledgments

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V. Investigating Total-Dose Gain Degradation in BJTs

V.A. Introduction

Bipolar junction transistors continue to play an important role in integrated circuit technology, particularly in the areas of analog or mixed-signal ICs and BiCMOS circuits. These bipolar circuits and devices are important for many systems that may be exposed to ionizing radiation. Modern bipolar junction transistors have shown time-dependent effects following irradiation that differ from those seen in MOS devices. Some types of bipolar devices show greater gain degradation after low dose rate irradiations with low electric-fields than after high dose rate irradiations. Moreover, high dose rate irradiation followed by annealing can not simulate the low dose rate response of many bipolar devices.

In earlier bipolar technologies, the limiting factor for using BJTs in total dose environments was typically excess leakage caused by trapped positive charge in the field oxide. However, this problem can be solved by appropriate process design and layout techniques. For many current bipolar technologies, the total dose failure mechanism is reduction of the current gain. Ionizing radiation typically degrades current gain in the device by increasing the base current (the collector current is not affected much).

The base current in modern bipolar transistors increases in an ionizing radiation environment due to increased recombination in the emitter-base depletion region. The recombination current results from two interacting effects: (1) increased surface recombination velocity and (2) spreading of the emitter-base depletion region. The increase in surface recombination velocity is proportional to the density of recombination centers at the silicon - silicon oxide ($Si\text{-}SiO_2$) interface that covers the emitter-base junction. These recombination centers are related to, although not precisely the same as, the interface traps that are commonly discussed in relation to MOS technologies.

Since the net charge introduced into the oxide by ionizing radiation is positive, the depletion region spreads on the p-side of a p-n junction. For npn transistors, this means that the depletion region spreads into the relatively lightly doped p-type base region. As the depletion region increases in size, recombination current increases at the $Si\text{-}SiO_2$ interface over the base and in the newly-depleted silicon bulk. In contrast, vertical pnp transistors are relatively hard to ionizing radiation, since positive oxide charge accumulates the surface of an n-type base.

In this work, extensive experimentation and modeling of trench-isolated silicon-on-insulator bipolar transistors from vertical, lateral, and substrate technologies were performed to characterize these devices for radiation-induced gain degradation. The work focuses on how dose rate and factors such as processing, geometry, and electrical bias affect the radiation response of bipolar devices. In addition, MOS capacitors fabricated from several of the bipolar processes were characterized for radiation damage to aid in explaining the physical mechanisms leading to gain degradation in the transistors.

To gain physical insight, experiments were developed to compare ionizing radiation degradation with hot-carrier stress. Hot-carrier stress in integrated BJTs can occur whenever the emitter-base junction is sufficiently reverse-biased so as to create large electric-fields within the emitter-base depletion region. This occurs, for example, in the operation of certain emitter-coupled differential pairs in certain analog-to-digital converters and more readily in the pull-up transistors of certain BiCMOS gates used in digital circuits during pull-down transients. Energetic carriers

drifting through the emitter-base depletion region, especially near the emitter periphery, where doping in the extrinsic base is high, can suffer collisions which result in their scattering into the overlying oxide. Hot-carrier susceptibility is an increasing concern in modern BJTs, as vertical scaling of device dimensions dictates that higher base and emitter doping levels be used to shrink the emitter-base depletion region. Hot-carriers can increase the interface trap densities locally, resulting in larger surface recombination velocities and increased recombination current within the emitter-base depletion region in much the same way as radiation stress. In addition, injected carriers can become trapped in the oxide, either after surmounting the interfacial potential barrier or by tunneling through the barrier to traps in the oxide bandgap, where they can bend the energy bands and alter device characteristics. Like radiation, hot-carrier stress degrades the current gain in BJTs by increasing the base current while affecting the collector current negligibly.

To gain further physical insight into ionizing radiation degradation mechanisms, mechanical stress at the $Si\text{-}SiO_2$ interface was studied. Mechanical stress has been reported to be strongly linked to the radiation hardness of MOS capacitors. Correlations of stress and radiation hardness in MOS capacitors have been made, for example, by quantifying radiation-induced defects while systematically varying capacitor gate geometry, gate thickness and time lapse following post-metallization anneal. Since disclosure of these results, numerous improvements in the radiation hardness of MOS devices have been attributed to modifications in $Si\text{-}SiO_2$ interfacial stress. Furthermore, it has been suggested that radiation itself can act as an impetus for improving the radiation sensitivity of MOS devices through a change in $Si\text{-}SiO_2$ interfacial stress, although very little is actually known about the effects of ionizing radiation on mechanical stress in $Si\text{-}SiO_2$ structures. While much progress has been made in understanding stress-related radiation effects in MOS devices, no work prior to this had been done in relating mechanical stress and ionizing radiation effects in bipolar junction transistors.

In this work, through rigorous experimental characterization, computer simulation and modeling, hot-carrier effects in poly- and single-crystalline npn bipolar transistors are investigated with regard to radiation damage and device geometry. A physically-based comparison between hot-carrier- and radiation-induced gain degradation in bipolar transistors is made which emphasizes the mechanisms of gain degradation by each stress type. Additionally, mechanical stress-related radiation effects are investigated in single-crystalline emitter bipolar transistors that are subjected to repeated cycles of irradiation and anneal.

The papers describing the work on total dose gain degradation in BJTs are included in Sections *V.B* through *V.Q*. A brief overview of each paper is included here to guide the reader through this material.

Section V.B.: R.N. Nowlin, E.W. Enlow, R.D. Schrimpf, and W.E. Combs, "Trends in the Total-Dose Response of Modern Bipolar Transistors," *IEEE Trans. Nucl. Sci.*, vol. 39, pp. 2026-2035, 1992.

> This paper examines a number of factors that influence the total-dose response of bipolar junction transistors, including: emitter bias, transistor polarity, emitter technology, emitter geometry, base design, and dose rate. Physical mechanisms for each of the observed effects are given.

Section V.C.: R.N. Nowlin, D.M. Fleetwood, R.D. Schrimpf, R.L. Pease, and W.E. Combs, "Hardness-Assurance and Testing Issues for Bipolar/BiCMOS Devices," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1686-1693, 1993.

> In this work, the dose-rate dependence of bipolar current-gain degradation is mapped over a wide range of dose rates. Annealing experiments following irradiation show negligible change in base current at room temperature, but significant recovery at higher temperatures. It is shown that irradiation and annealing tests cannot be used to predict the low-dose-rate response of bipolar junction transistors.

Section V.D.: S.L. Kosier, R.D. Schrimpf, R.N. Nowlin, D.M. Fleetwood, M. DeLaus, R.L. Pease, W.E. Combs, A. Wei, and F. Chai, "Charge Separation for Bipolar Transistors," *IEEE Trans. Nucl. Sci.*, vol. 40, pp. 1276-1285, 1993.

> The role of net positive oxide trapped charge and surface recombination velocity on excess base current in bipolar junction transistors is identified in this paper. Two different approaches for quantifying the effects of surface recombination velocity are given. The results of the two approaches are compared to two-dimensional numerical simulations and experimental data taken from test structures.

Section V.E.: S.L. Kosier, R.D. Schrimpf, A. Wei, M. DeLaus, D.M. Fleetwood, and W.E. Combs, "Effects of Oxide Charge and Surface Recombination Velocity on the Excess Base Current of BJTs," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 1993, pp. 211-214.

> In this paper, the effects of positive oxide trapped charge and surface recombination velocity on the excess base current in bipolar junction transistors is investigated. The effects of the two types of damage can be detected by plotting the excess base current versus base-emitter voltage. Differences and similarities between ionizing-radiation-induced and hot electron-induced degradation are discussed.

Section V.F.: A. Wei, S.L. Kosier, R.D. Schrimpf, D.M. Fleetwood, and W.E. Combs, "Dose-Rate Effects on Radiation-Induced Bipolar Junction Transistor Gain Degradation," *Appl. Phys. Lett.*, vol. 65, pp. 1918-1920, 1994.

> Analysis of radiation damage in modern npn bipolar junction transistors at various dose rates is performed using a charge separation method and two-dimensional numerical simulations. The charge separation method is verified with measurements on metal-oxide-semiconductor capacitors. It is demonstrated that gain degradation is more pronounced at lower dose rates.

Section V.G.: A. Wei, S.L. Kosier, R.D. Schrimpf, W.E. Combs, and M. DeLaus, "Excess Collector Current Due to an Oxide-Trapped-Charge-Induced Emitter in Irradiated NPN BJTs," in *Proc. IEEE Bipolar/BiCMOS Circuits and Tech. Mtg.*, 1994, pp. 201-204.

> In this paper, excess collector current in irradiated npn bipolar junction transistors is linked to an oxide-trapped-charge-induced inversion layer acting as an additional emitter. Excess collector current is modeled by interpreting the inversion layer as an extension of the emitter.

Section V.H.: S.L. Kosier, W.E. Combs, A. Wei, R.D. Schrimpf, D.M. Fleetwood, M. DeLaus, and R.L. Pease, "Bounding the Total-Dose Response of Modern Bipolar Transistors," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1864-1870, 1994.

> In this paper, an upper bound for the total-dose response of modern bipolar junction transistors is presented. The radiation-induced excess base current is shown to saturate once a critical amount of charge accumulates in the oxide above the base-emitter junction. Circuit level implications for space applications are discussed.

Section V.I.: R.N. Nowlin, D.M. Fleetwood, and R.D. Schrimpf, "Saturation of the Dose-Rate Response of BJTs Below 10 rad(SiO_2)/s: Implications for Hardness Assurance," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2637-2641, 1994.

> In this paper, the gain degradation of modern bipolar transistors was investigated for dose rates ranging from 0.01 to 2000 rad (SiO2)/s. Low-dose rate gain degradation exceeds high-dose rate degradation for total doses less than 1 Mrad. It is shown that the gain degradation saturates at low dose rates.

Section V.J.: D.M. Fleetwood, S.L. Kosier, R.N. Nowlin, R.D. Schrimpf, R.A. Reber, Jr., M. DeLaus, P.S. Winokur, A. Wei, W.E. Combs, and R.L. Pease, "Physical Mechanisms Contributing to Enhanced Bipolar Gain Degradation at Low Dose Rates," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 1871-1883, 1994.

> This paper explains various physical mechanisms that contribute to the enhanced gain degradation in bipolar junction transistors at low dose rates. Capacitance-voltage and thermally-stimulated-current measurements were performed, and a physical model was developed to help explain this phenomenon.

Section V.K.: D.M. Schmidt, D.M. Fleetwood, R.D. Schrimpf, R.L. Pease, R.J. Graves, G.H. Johnson, K.F. Galloway, and W.E. Combs, "Comparison of Ionizing Radiation Induced Gain Degradation in Lateral, Substrate, and Vertical PNP BJTs," *IEEE Trans. Nucl. Sci.*, vol. NS-42, pp. to be published, 1995.

> This paper compares the amount of ionizing-radiation-induced gain degradation in lateral, substrate, and vertical pnp bipolar junction transistors. The dose-rate dependence of current gain degradation in lateral pnp bipolar junction transistors is even stronger than the dependence reported for npn devices. It is shown that the lateral devices degrade significantly more than the substrate devices.

Section V.L.: R.D. Schrimpf, R.J. Graves, D.M. Schmidt, D.M. Fleetwood, R.L. Pease, W.E. Combs, and M. DeLaus, "Hardness Assurance Issues for Lateral PNP Bipolar Junction Transistors," *IEEE Trans. Nucl. Sci.*, vol. NS-42, pp. to be published, 1995.

> In this work, several hardness-assurance approaches are examined and compared to experimental results obtained at low dose rates. The approaches considered include irradiation at high dose rates while at elevated temperature and high-dose-rate irradiation followed by annealing. The lateral pnp transistors are shown to continue to degrade during post-irradiation annealing, which contrasts sharply to their npn counterparts.

Section V.M.: S.C. Witczak, S.L. Kosier, R.D. Schrimpf, and K.F. Galloway, "Synergetic Effects of Radiation Stress and Hot-Carrier Stress on the Current Gain of NPN Bipolar Junction Transistors," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2412-2419, 1994.

> In this paper, the combined effects of ionizing radiation and hot-carrier stress on the current gain of npn bipolar junction transistors are investigated. It is shown that the hot-carrier response of the transistor is improved by radiation damage, whereas hot-carrier damage has little effect on subsequent radiation damage. A qualitative model is developed that implies that a bound on damage due to the combined stress types is achieved when hot-carrier stress precedes any irradiation.

Section V.N.: S.L. Kosier, M. DeLaus, A. Wei, R.D. Schrimpf, and A. Martinez, "Simple Technique for Improving the Hot-Carrier Reliability of Single-Poly Bipolar Transistors," in *Proc. IEEE Bipolar/BiCMOS Circuits and Tech. Mtg.*, 1994, pp. 205-208.

> This work presents experimental and two-dimensional simulation results that show that reduced screen oxide thickness leads to increased breakdown voltage of the emitter-base junction and reduced peak electric field at breakdown, which translates into improved hot-carrier reliability. It is shown that reducing the screen oxide thickness from 55 to 35 nm increases the emitter-base junction breakdown voltage by 0.2 V, improves the hot-carrier-induced excess base current by more than an order of magnitude, and degrades the peak cutoff frequency by only 3 percent.

Section V.O.: R.J. Graves, D.M. Schmidt, S.L. Kosier, A. Wei, R.D. Schrimpf, and K.F. Galloway, "Visualization of Ionizing-Radiation and Hot-Carrier Stress Response of Polysilicon Emitter BJTs," in *IEDM Tech. Dig.*, 1994, pp. 233-236.

> Process and device simulation software tools are used in this paper to produce an animated visualization of the mechanisms involved in the ionizing-radiation and hot-carrier stress responses of bipolar junction transistors. A physically base model is presented, which compares ionizing-radiation response with hot-carrier response in polysilicon-emitter bipolar junction transistors.

Section V.P.: S.C. Witczak, W. Wong-Ng, K.F. Galloway, R.D. Schrimpf, J.S. Suehle, and M. DeLaus, "Relaxation of Si-SiO_2 Interfacial Stress in Bipolar Screen Oxides due to Ionizing Radiation," *IEEE Trans. Nucl. Sci.*, vol. NS-42, to be published, 1995.

> In this paper, complementary single-crystalline emitter bipolar junction transistors of two emitter geometries were investigated for radiation-induced current gain degradation while undergoing repeated cycles of ionizing radiation exposure and high-temperature anneal. Current gain degradation was found to grow progressively worse with an increasing number of cycles. In conjunction with the current gain measurements, samples from a monitor wafer were characterized for mechanical stress while undergoing similar cycles of irradiation and anneal. The results suggest that mechanical stress may play an important role in determining the radiation hardness of bipolar junction transistors.

Section V.Q.: S.L. Kosier, A. Wei, R.D. Schrimpf, D.M. Fleetwood, M. DeLaus, R.L. Pease, and W.E. Combs, "Physically Based Comparison of Hot-Carrier-Induced and Ionizing-Radiation-Induced Degradation in BJTs," *IEEE Trans. Electron Devices*, vol. 42, pp. 436-444, 1995.

> This paper presents a physically based comparison between hot-carrier and ionizing radiation stress in bipolar junction transistors. Although both types of stress lead to qualitatively similar changes in the current gain of the device, it is shown that the physical mechanisms responsible for the degradation are quite different. Based on the physical model, implications for correlating and comparing hot-carrier-induced and ionizing-radiation-induced damage are discussed.

V.B. Trends in the Total-Dose Response of Modern Bipolar Transistors

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Trends in the Total-Dose Response of Modern Bipolar Transistors *

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Abstract

The primary degradation in modern bipolar transistors that are subjected to ionizing radiation is a reduction in current gain. There are many factors that influence the total-dose response of bipolar transistors, including emitter bias, transistor polarity, emitter technology, emitter geometry, base design, and dose rate. The effects of each of these factors are investigated. Physical mechanisms consistent with the observed effects are described.

I. INTRODUCTION

In this work, extensive experimentation on trench-isolated, silicon-on-insulator bipolar transistors of both polysilicon and standard (crystalline) emitter technologies has been conducted. Several varieties of these processes have been studied [1], [2]. This paper discusses the factors that affect the total-dose response of these modern bipolar transistors and examines the trends observed in testing these devices.

Planar, double-diffused (or implanted), junction-isolated bipolar technologies have always been relatively hard to ionizing radiation [3],[4]. The primary degradation caused by exposure to ionizing radiation is a reduction in current gain. As a result, digital technologies are usually relatively hard (1 Mrad(Si) or more) since digital applications do not require large current gains. On the other hand, linear technologies, which have more stringent gain requirements, may fail at significantly lower doses.

Early studies of radiation-induced degradation in these older bipolar transistors indicated that the decrease in current gain with increasing total-dose was dependent on device perimeter [5]. The degradation was caused by an increase in surface recombination velocity due to increases in the interface trap density over the base-emitter junction near the silicon surface. There was also a spreading of the field-induced depletion layer in the base due to positive trapped charge in the field oxide [6].

Later technologies used recessed field oxides to increase the speed and packing density of bipolar circuits. Under worst-case collector-junction irradiation bias conditions, failures in these technologies could occur at a total-dose as low as 5 krad(Si) [7]. The first-order failure mechanism was found to be an inversion of the p^+ channel stop under the recessed field oxide. This inversion layer provided a current path for buried-layer-to-buried-layer (transistor-to-transistor) leakage. The second-order failure mechanism was found to be an inversion of the intrinsic p-base along the sidewall of an NPN transistor with a walled emitter. The inverted base layer led to a collector-to-emitter leakage current. Devices could be hardened against buried-layer-to-

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buried-layer leakage by increasing the doping density of the p^+ channel stop. Collector-to-emitter leakage could be eliminated by fully nesting the emitters. These total-dose failure mechanisms still exist in some BiCMOS technologies today [8].

However, due to many recent process changes, the problems of buried-layer-to-buried-layer and collector-to-emitter leakage have been reduced. The dominant degradation in many modern bipolar transistors is again a reduction in current gain.

For example, transistors with polysilicon emitters have been introduced for their high gains, high switching speeds, self-aligned processing, and compatibility with BiCMOS processes [9],[10],[11]. There are several theories to explain the enhanced gain of poly-emitter transistors, many of which involve the presence of an interfacial oxide between the polysilicon and silicon [12]. These technologies are sufficiently different from the older technologies to warrant investigation of their total-dose response and hardening approaches.

In a recent study of polysilicon-emitter and standard-emitter transistors [1], it was shown that in these modern devices the decreases in gain were caused by increases in base current at the perimeters of the devices. Thus, in terms of the cause of degradation, modern devices are similar to the older technologies discussed above. Consequently, it was concluded in reference [1] that the oxides over the emitter-base junctions provide the primary mechanisms of degradation. These oxides are poorly grown, perhaps even deposited, and they are heavily implanted in the process of forming the base and emitter. The total-dose characteristics of implanted, poorly-grown oxides are virtually unknown. Furthermore, since these oxides lie over the base-emitter junctions, there are always fringing electric fields present to influence carrier transport and interface trap generation. Theories have been proposed to explain these phenomena for the older technologies [6], and for the most part are sufficient to explain many of the similar results in newer technologies. However, these theories do not explain the differences between poly-emitter devices and standard-emitter devices, nor do they explain the dose-rate effects noted in the newer technologies [1], [2].

In order to investigate these modern technologies more thoroughly, a fractional factorial matrix of experiments was performed for the variables and levels listed in Table I (for a discussion of factorial experiments see, for example, reference [13]). The analysis of the results of the fractional factorial experiment suggested that collector bias during irradiation was insignificant, and reverse bias on the emitter was the worst-case irradiation bias. The AC emitter bias yielded results intermediate to the reverse and forward bias effects. A full factorial matrix of experiments on the reduced set of variables (eliminating collector bias and AC emitter bias conditions) was conducted. Each experiment was replicated to provide an estimate of the experimental error. This standard error was used to determine the significance of the effects of the variables. An effect of a variable is found by first averaging the response of all experiments with the variable of interest at one level. This average response is then compared to the average of the responses of all experiments with the variable at the other level. For example, to determine the effect of transistor polarity, the responses of all NPN devices in the experimental matrix were averaged and compared to the average response of all PNP devices in the experimental matrix. If the effect was larger than 3-times the standard error, then it could be judged as a real effect

Table I Test variables and levels used in the factorial matrix of experiments. The AC emitter bias was a 1 Mhz triangle wave with 2.5 volts peak-to-peak.

Variable	Levels
Transistor Polarity	NPN, PNP
Emitter Technology	Polysilicon, Standard
Dose Rate	13.12, 243.6 rad(Si)/s
Collector Bias (V_{CB})	10.0, 0.0 volts
Emitter Bias	Reverse Bias, No Bias, Forward Bias, AC Bias
Emitter Geometry (P/A ratio)	2.67 μm^{-1} (square), 1.53 μm^{-1} (3 emitter stripes)
Base Doping and Layout	with and without a ring of highly doped material

with 99% certainty based on Student's t-distribution [13]. All the results presented in this work reflect the averaged effects that were larger than 3-times the standard error.

In addition to the factorial matrix of experiments, several other experiments were conducted using a range of dose rates. Control experiments also verified that there were no effects due to bias alone (such as hot electron degradation [14]).

This paper discusses the significant effects observed from the many experiments performed. The significant effects are those due to emitter geometry and base design, transistor polarity, base-emitter junction bias, emitter technology, and dose rate.

II. Discussion of Effects and Mechanisms

The process chosen for this study allowed polysilicon and standard emitter transistors of both NPN and PNP polarity to be fabricated in as nearly identical a process as possible. Though other processes have been studied ([1], [2]), this process was chosen for the availability of polysilicon and standard emitter devices of both polarities, and, judging from the results, was deemed representative of the other processes studied. Cross sections of trench-isolated, silicon-on-insulator, double-poly NPN and PNP devices are shown in Figure 1. Both polarities were available in two emitter perimeter-to-area ratios: 2.67 μm^{-1} (1.5 μm × 1.5 μm, square), and 1.53 μm^{-1} (3 rectangular emitter stripes, each 1.5 μm × 10 μm). The poly-emitter devices differed from the standard-emitter devices only in the emitter fabrication.

Basic Mechanisms

There are two basic mechanisms involved in all of the effects of total-dose on the gain degradation of bipolar transistors. These two mechanisms are the accumulation of positive trapped charges in the oxides, and the accumulation of interface states at the silicon-silicon dioxide interfaces. The interactions of these two mechanisms with the factors of polarity, emitter technology, base doping density, emitter bias, and dose rate can account for most of the observed effects. Figure 2 depicts the base-emitter junction of an NPN device before and after irradiation.

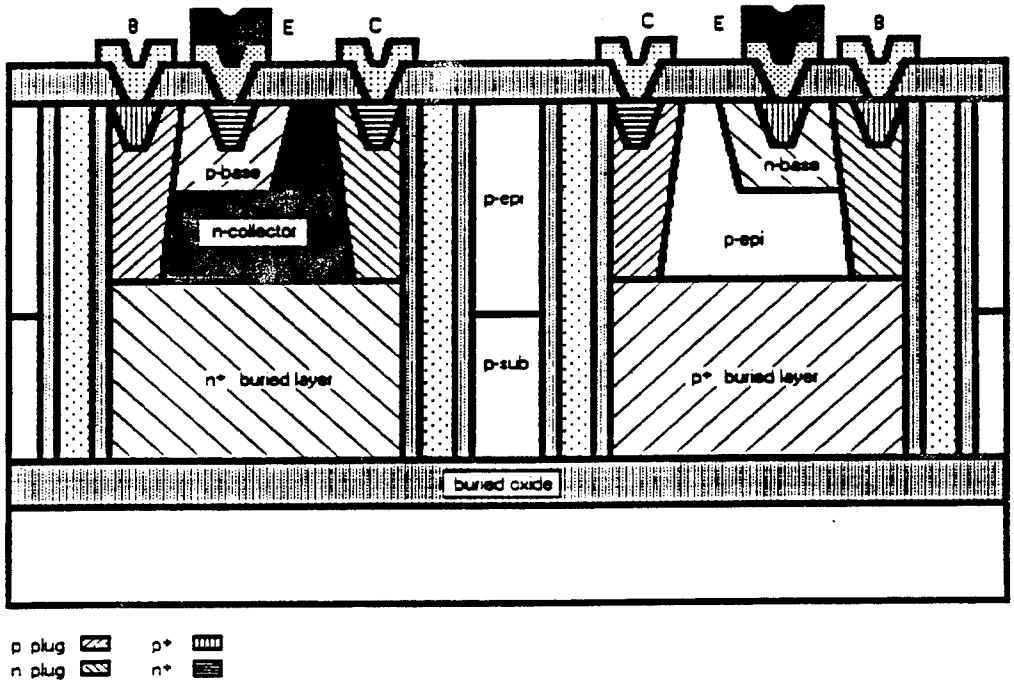


Figure 1 Cross sections of NPN and PNP, silicon-on-insulator, trench-isolated, double-poly bipolar transistors.

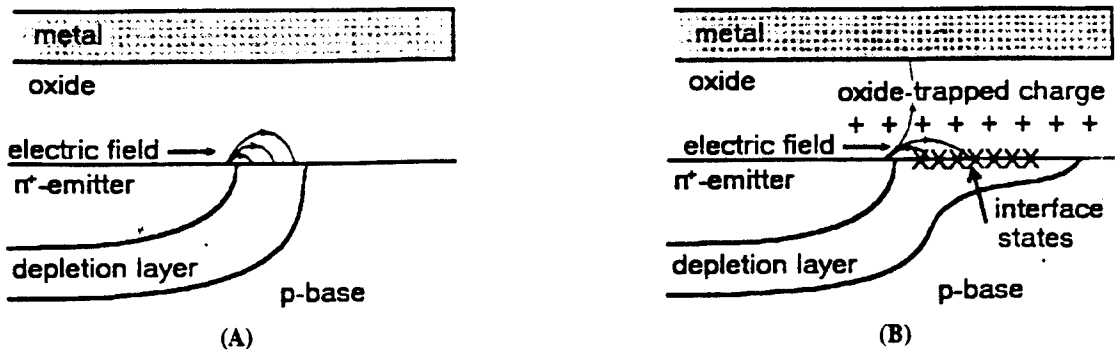


Figure 2 Magnified cross-section of the base-emitter junction of an NPN transistor. (A) Pre-irradiation. (B) Post-irradiation.

The fringing fields point from the emitter to the base (they point in the opposite direction in PNP devices). In the post-irradiation case, the positive oxide charge and interface states are shown. The fields are modified by the presence of the charges.

The buildup of positive trapped charge in the oxides over the emitter-base junctions will deplete lowly doped p-type base regions. As a result, the total depleted surface area in NPN transistors increases. This increase in the depleted surface causes an increase in the surface recombination current. The recombination reaches a maximum in forward biased junctions where the electron and hole concentrations are equal (called the cross-over condition). The location of the cross-over, as well as the width of the depletion region at the surface is dependent on the surface potential. The surface potential is in turn dependent on the distribution of charges in the oxide and at the interface, and the junction bias conditions. The surface recombination rate per unit area for a distribution of trap levels at the surface of a forward biased junction can be expressed as [6]

$$U_s = \sigma v_{th} n_i (e^{\beta V} - 1) \times \int_{E_v}^{E_c} \frac{D_t(E)\,dE}{\cosh\left[\frac{\beta}{q}(E - E_i)\right] + e^{\beta(\psi_s(x) - \phi_n)} + e^{-\beta(\psi_s(x) - \phi_p)}} \quad (1)$$

where σ is the effective capture cross section, v_{th} is the electron thermal velocity, n_i is the intrinsic carrier density, $\beta = q/kT$ (q is the electronic charge, k is Boltzmann's constant, T is the temperature), V is the forward bias on the junction, D_t is the trap density distribution, $\psi_s(x)$ is the surface potential along the surface (the x direction), ϕ_n and ϕ_p are the electron and hole fermi levels, E is the trap energy level, E_i is the intrinsic energy, and E_c and E_v are the conduction and valence band energy levels respectively. The recombination rate (U_s) is maximum where $n = p$, which occurs at the surface within the depletion region where $\psi_s(x) = (\phi_n + \phi_p)/2$. Since there is more recombination in the device, more base current will flow at a given base-emitter voltage. Furthermore, this recombination occurs at the periphery of the emitter. As oxide charge increases, the position of cross-over moves out further into the base until the entire base region becomes inverted.

The buildup of interface traps at the silicon-silicon dioxide interface increases the surface recombination velocity. These traps do not contribute surface current when they lie over undepleted surfaces, but they are effective recombination centers when they lie over depleted surfaces. Consequently, there is an interaction between the positive trapped oxide charge and the interface traps. As positive oxide charge increases (particularly over a p-type region), the surface depletion region increases, exposing more recombination sites due to interface traps. Thus, while oxide charges and interface traps may increase sublinearly or even linearly with total dose, base current may increase superlinearly with total dose. For example, if the total dose is doubled, the excess base current more than doubles. Mathematically, the surface recombination current is found by spatially integrating the recombination rate (1) over the width of the surface depletion region, and has the form $I_{s,rec} \propto W(D) \times D_t(D)$ where W is the surface

depletion width, and D is the total-dose. Due to this multiplication of mechanisms, the excess base current can be seen to increase superlinearly.

In addition, the oxide charges and interface traps interact with the fringing electric fields of the junction in the oxide. The positive trapped oxide charge shields the fringing electric fields in the oxide. Therefore, as positive oxide charge accumulates, the fields change, and subsequent accumulation of positive oxide charge occurs under different field conditions. The fields will also tend to concentrate the positive oxide charges and the interface states in the direction of the field (assuming the buildup of interface traps occurs due to a two stage H^+ process [15]). Specifically, the damage will accumulate over the base side of the junction in NPN devices, but over the emitter side of the junction in PNP devices. In other words, the oxide charges and interface states accumulate in spatially nonuniform distributions.

Both mechanisms cause an increase in base current through increased recombination. The collector current is unchanged. Therefore, the current gain decreases. The response of the current gain to total dose is shown in Figure 3 for a typical case. The current gain in Figure 3 is normalized to the peak pre-radiation current gain, β_{pk}. The decrease in gain shown in Figure 3 is the result of the increase in base current as shown in Figure 4.

The base current in a bipolar transistor can be expressed as

$$I_B = \frac{I_S}{\beta_{pk}} e^{V_{BE}/kT} + I_{SS} e^{V_{BE}/n_{SS}kT} \qquad (2)$$

where I_S is the collector saturation current, V_{BE} is the base-emitter junction bias, I_{SS} is a surface saturation current, and n_{SS} is a non-ideality factor characterizing the recombination. As the total-dose increases, values for n_{SS} increase from 1 to 2. I_{SS} also increases with total dose. The first term in Eq. (2) represents the ideal current component and is proportional to emitter area. The second term represents the non-ideal recombination processes described by Eq. (1) and is directly proportional to emitter perimeter [1].

Emitter Geometry and Base Design Effects

Figure 5 shows the normalized current gain, β / β_0, and the change in base current, ΔI_B (measured at $V_{BE} = 0.7\ V$), as functions of total-dose for devices with different emitter perimeter-to-area ratios. The temperature dependence of the base and collector currents is approximately the same and is given by $I(T) \propto T^3 e^{E_g/kT}$, where E_g is the silicon bandgap, and the temperature dependence of the diffusion length has been neglected [16]. To eliminate any variations in results due to temperature, the base currents were multiplied by a normalization factor of I_{C0} / I_C, where I_{C0} is an arbitrarily fixed collector current. In addition, the

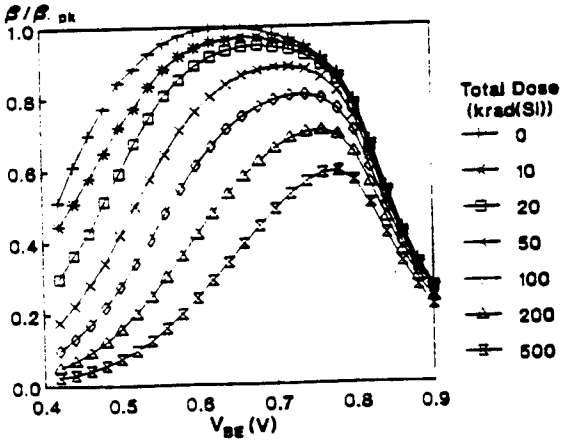


Figure 3 Typical current gain characteristics for various levels of total dose. β_{pk} is the peak pre-radiation current gain.

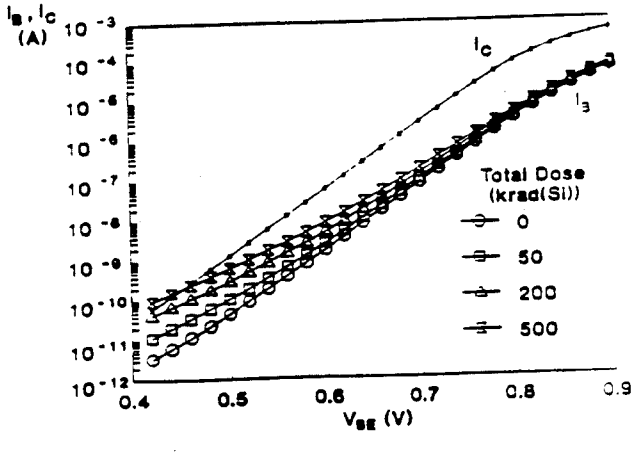


Figure 4 Typical Gummel characteristic showing the increase in base current with total dose.

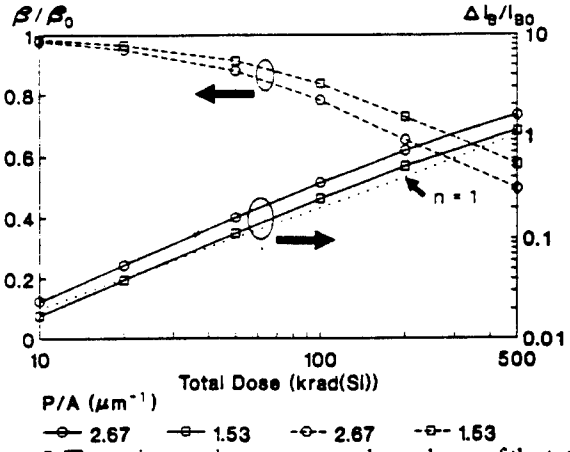


Figure 5 The emitter perimeter-to-area dependence of the total-dose response of bipolar transistors. $V_{BE} = 0.7\ V$.

changes in base current are presented as a fraction of the pre-radiation base current, I_{B0}, to eliminate part-to-part variations. (The fractional change in ΔI_B is exactly the same as the fractional change in $\Delta(1/\beta)$.) The current gain normalization, β_0, is the pre-radiation current gain at $V_{BE} = 0.7\ V$.

The two emitter geometries available in the technology studied in this work exhibit results consistent with similar technologies having a greater variety of perimeter-to-area ratios [1]. The increase in the normalized base current is directly proportional to the perimeter-to-area ratio. Devices with large perimeter-to-area ratios will experience larger increases in depleted surface area than will devices with smaller emitter perimeter-to-area ratios. Thus, devices with larger perimeter-to-area ratios have larger increases in base current. As discussed in the introduction, the effect of the variable of emitter perimeter-to-area ratio is simply the difference between the two curves of ΔI_B in Figure 5. This effect is greater than 3-times the standard error in these experiments.

Furthermore, the total-dose response of bipolar transistors can be slightly improved if the surface concentration of the base is increased. One means of accomplishing this without changing the doping of the bulk base region is to encircle the emitter with a ring of highly doped base material. Often such a region is used to provide an ohmic contact to the base and has been demonstrated to improve hot electron damage. In NPN devices, the proximity of this highly doped p^+ region to the emitter will terminate the spread in the depletion region caused by the positive oxide charge. Figure 6 shows that such a base ring does provide a slight increase in the transistor hardness. Though the effect is small, it is again larger than 3-times the standard error determined from the replicated experiments in the factorial matrix. The p^+ ring may be far enough from the base-emitter junction that most of the damage has occurred by the time the spread in the depletion region reaches the highly doped region. (The responses of PNP transistors, for which the base ring has little or no effect, have been averaged into this result and may also reduce the apparent magnitude of the effect.)

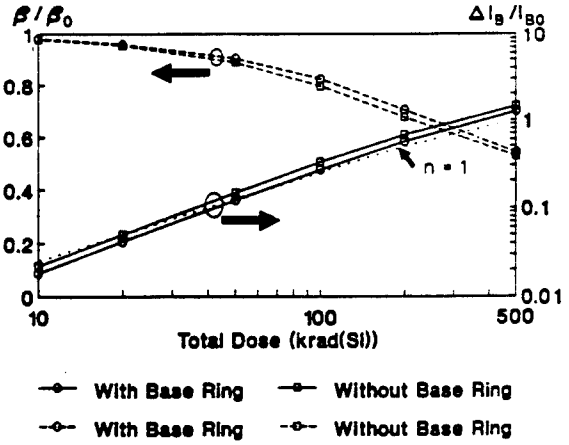


Figure 6 The effects of base design on the total-dose response of bipolar transistors. $V_{BE} = 0.7\ V$.

Transistor Polarity Effects

The differences in NPN and PNP transistors alluded to in the last paragraph are seen in Figure 7. Notice that the gain decreases significantly with increasing total-dose. The current gain of NPN devices is, on average, less than 40% of the pre-radiation gain after a total-dose of only about 200 krad(Si). On the other hand, PNP devices still have 60% of their pre-radiation gain at a total-dose of 500 krad(Si). Many linear applications will fail when the gains of individual transistors fall below 50% of the pre-radiation gain [17].

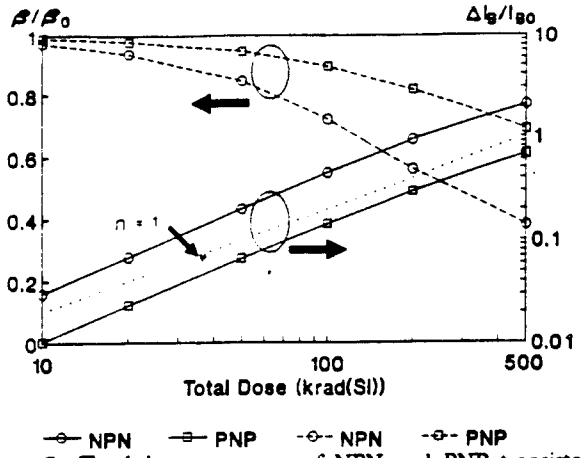


Figure 7 Total-dose responses of NPN and PNP transistors. V_{BE} = 0.7 *V*.

PNP devices are harder than NPN devices because the n-type base is not depleted. Furthermore, the p-type emitter is very heavily doped and very large densities of positive oxide charge will be required to deplete the surface. Therefore, the positive trapped charge in the oxide has a smaller effect in PNP devices than in NPN devices. In addition, the interface traps tend to be concentrated over the emitter side of the junction by the fringing electric fields. Since the PNP emitter depletion region is very small, the number of traps involved in recombination will be smaller in PNP devices than in NPN devices.

Bias Effects

In the studies of total-dose failures in bipolar technologies with recessed field oxides, the failure level was found to depend on collector bias since the collector was directly involved in the leakage failure mechanism. However, the collector is not involved in the gain degradation mechanisms. The gain degradation is caused by damage to the oxides over the base-emitter junction. Therefore, the gain degradation is not sensitive to changes in bias on the collector.

As mentioned above, the fields in the oxides over the base-emitter junctions, and the direction of the fields play significant roles in the degradation of bipolar transistors. The field cannot be reversed for a device of a given polarity, but its magnitude can be changed by the base-emitter bias. For example, forward bias decreases the field magnitude while reverse bias increases the field magnitude. Figure 8 shows the results of irradiating bipolar transistors under three different base-emitter bias conditions: forward bias, zero bias, and reverse bias. The reverse bias voltage was chosen so that there were no hot-electron effects present. It can be seen that a device under reverse bias exhibits greater degradation than a device under forward bias. The reason for this is that the reverse biased device has larger electric fields pointing toward the base side of the junction. Thus the buildup of traps and charges are enhanced in comparison to the case of forward bias. The degradation in the case of no base-emitter bias lies somewhere between the degradation of the reverse and forward bias cases.

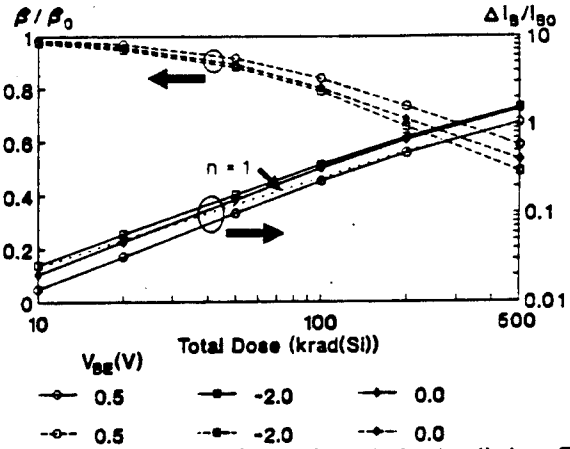


Figure 8 The effects of different biases during irradiation. The measurement bias was V_{BE} = 0.7 *V*.

A note should be made here about the characterization of the degradation, particularly the bias at which the change in base current is measured. Recombination is a voltage dependent process characterized by a non-ideality factor between 1 and 2 as in Eq. (2). Furthermore, in Eq. (1), the bias voltage appears explicitly in the exponent, but the surface potential is also dependent on the junction bias. Therefore, at small base-emitter voltages, the recombination current will dominate the I-V characteristics of bipolar devices (see Figure 4). As the voltage increases, the ideal current begins to dominate. Therefore, the change in base current is much larger at lower voltages. This result is shown in Figure 9 where the response of bipolar devices

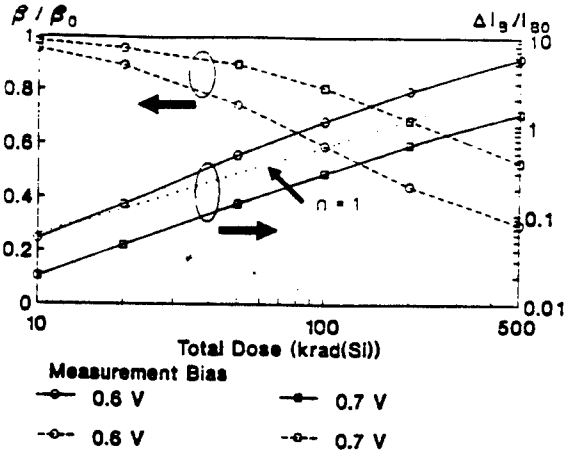


Figure 9 The effects of characterizing a device at different base-emitter voltages.

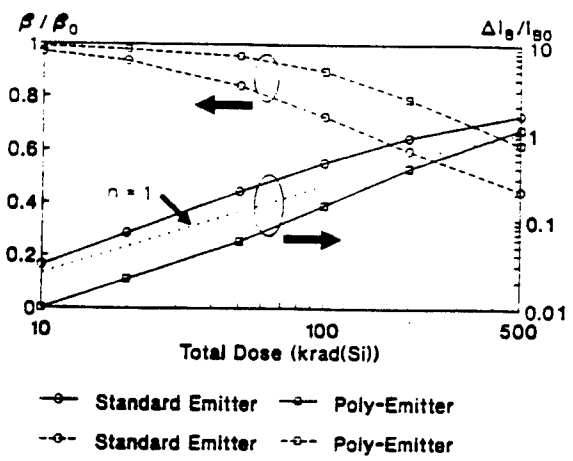


Figure 10 Comparison of the responses of poly-emitter devices with standard-emitter devices. V_{BE} = 0.7 *V*.

characterized at V_{BE} = 0.6 *V* is compared to the response of bipolar devices characterized at V_{BE} = 0.7 *V*. Note that the slope of the ΔI_B curves is steeper at the lower voltage. The lower voltage curves are more superlinear than the higher voltage curves as a result of the voltage dependence of the surface potential.

Emitter Technology Effects

Figure 10 shows a comparison of the total-dose responses of poly-emitter devices and standard-emitter devices characterized at a base-emitter voltage of V_{BE} = 0.7 *V*. The standard-emitter devices exhibit a larger change in base current for a lower total-dose. However, at larger total-doses the poly-emitter devices may become worse than the standard-emitter devices. The poly-emitter devices exhibit a more strongly superlinear response than the standard-emitter devices. Comparing this result to the results of Figure 9, it may be concluded that the same mechanisms are responsible for the degradation in poly-emitter devices as in standard-emitter devices. However, the magnitudes of the mechanisms are different in the two types of devices. The differences may be due to the different surface potentials caused by different surface doping concentrations, and different emitter implants in the oxides.

Dose Rate Effects

Figure 11 shows the differences in total-dose responses of bipolar transistors irradiated at two different dose rates. Devices irradiated at the lower dose rate exhibit larger degradation. This effect is not fully understood; however, there are several possible explanations. The interaction of the electric fields in the oxide with the damage generated by the radiation may serve as the key to understanding this phenomenon. These fields will change with the buildup of radiation induced damage, and subsequently influence future damage. The fields may also cause a migration of charge over long time to the base side of the junction. At low dose rates there may be sufficient time for the buildup of damage to occur simultaneously with the charge migra-

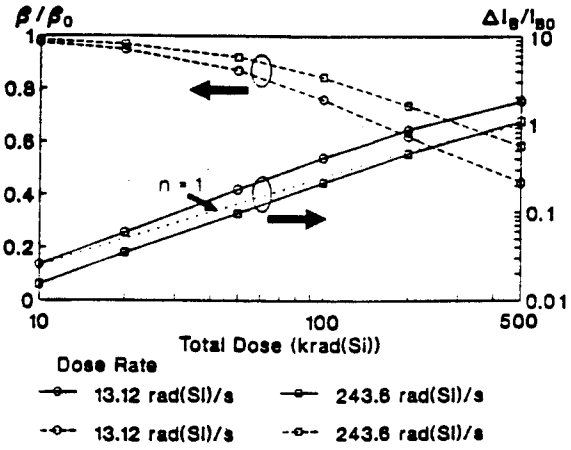


Figure 11 The effects of irradiating devices at different dose rates.

tion. At higher dose rates, the damage builds up first. Later, the migration of charges may cause further damage.

Since the dose rate affects the magnitude of degradation, it is necessary to consider very carefully what test conditions are most suitable for the intended application. MIL-STD-883B Test Method 1019.4 testing may not be appropriate for modern bipolar transistors. It requires testing at ^{60}Co dose rates of 50-300 rad(Si)/s under worst case bias conditions [18]. It also specifies an anneal procedure to test for the rebound observed in FET technologies. However, annealing studies of modern bipolar transistors have shown that there is no rebound for some cases. The post-radiation buildup of damage in devices irradiated at high dose rates did not achieve the levels of degradation observed in low dose rate experiments [2].

III. Summary and Conclusions

The various phenomena occurring in bipolar transistors when they are exposed to ionizing radiation have been discussed. In summary, the significant effects of total-dose damage in modern bipolar transistors are the following:

1. NPN transistors degrade more than PNP transistors.

2. Devices with highly doped base rings will be less susceptible to total-dose damage than devices without base rings, especially in NPN devices.

3. Devices with small emitter perimeter-to-area ratios will be less susceptible than devices with large perimeter-to-area ratios.

4. Collector bias does not affect gain degradation.

5. Reverse bias on the emitter is the worst-case irradiation bias condition.

6. The increases in base current are larger at small base-emitter voltages than at large base-emitter voltages.

7. Poly-emitter devices are initially harder than standard emitter devices, but may become worse than standard devices at large total doses.

8. Degradation is worse at lower dose rates.

Acknowledgments

This paper is dedicated to the memory of Ed Enlow. His contributions to this work, prior to his tragic death, were invaluable. He will be greatly missed.

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V.C. Hardness-Assurance and Testing Issues for Bipolar/BiCMOS Devices

Hardness-Assurance and Testing Issues for Bipolar/BiCMOS Devices[1]

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Abstract

Different hardness-assurance tests are often required for advanced bipolar devices than for CMOS devices. In this work, the dose-rate dependence of bipolar current-gain degradation is mapped over a wide range of dose rates for the first time, and it is very different from analogous MOSFET curves. Annealing experiments following irradiation show negligible change in base current at room temperature, but significant recovery at temperatures of 100°C and above. In contrast to what is observed in MOSFET's, irradiation and annealing tests cannot be used to predict the low-dose-rate response of bipolar devices. A comparison of x-ray-induced and ^{60}Co gamma-ray-induced gain degradation is reported for the first time for bipolar transistors. The role of the emitter bias during irradiation is also examined. Implications for hardening and hardness assurance are discussed.

I. INTRODUCTION

Bipolar/BiCMOS circuits and devices are important for many systems that may be exposed to ionizing radiation. Previous studies of modern bipolar transistors [1,2] have shown time-dependent effects following irradiation that differ from those seen in MOS devices [3,4]. Furthermore, the low-dose-rate response of bipolar transistors is not adequately covered by MIL-STD-883D Test Method 1019.4.

When bipolar transistors are exposed to ionizing radiation, trapped oxide charges and interface states accumulate in the field oxides that lie over the surface of the intrinsic base [1,2]. This leads to an increase in surface recombination current in the emitter-base diode. Consequently, there is an increase in the base current of the device, and the bipolar transistor suffers from a loss of dc current gain as in Fig. 1 and Fig. 2. Note in Fig. 2 that there is no change in I_C with dose up to 500 krad(SiO_2) for this range of V_{BE}.

The total-dose degradation can be characterized in terms of the change in the base current measured at a given V_{BE} for each level of total dose. The change in the base current, or the excess base current, increases with total dose as in Fig. 3. An increase in excess base current with increasing emitter perimeter-to-area ratio,

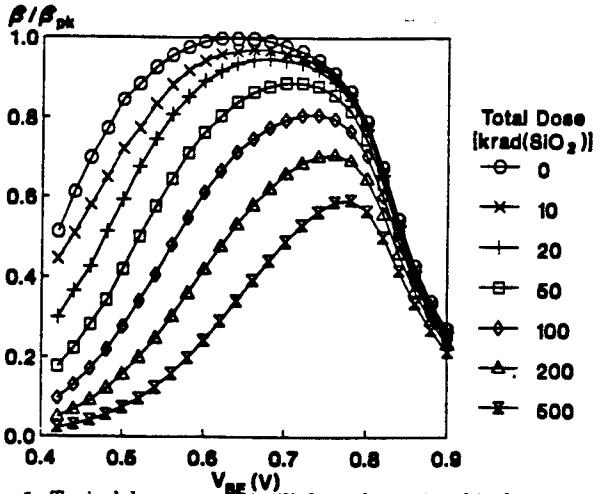


Fig. 1. Typical dc current-gain (β) degradation in a bipolar transistor exposed to ionizing radiation. β_{pk} is the peak pre-irradiation gain; V_{BE} is the base-emitter bias.

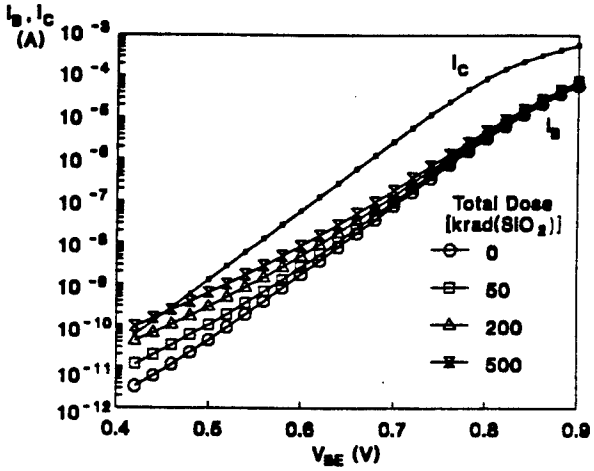


Fig. 2. Typical Gummel curves for a bipolar transistor exposed to ionizing radiation. I_B and I_C are the base and collector currents.

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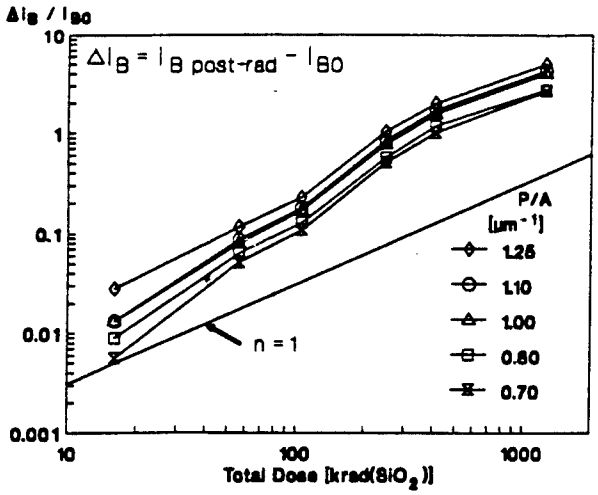


Fig. 3. Total-dose and device-geometry dependencies of the excess base current measured at $V_{BE} = 0.7$ V. I_{B0} is the pre-rad current.

P/A, is also indicated. Note that the base current increases superlinearly with total dose. That is, a factor of two increase in dose causes more than a factor of two increase in excess base current, for example. The significance of the device geometry for hardness assurance will be discussed in section V.

The increases in base current that are induced by the ionizing radiation depend on many factors. It has been shown [2] that changes in the base current depend on transistor polarity, emitter technology, base-emitter bias, base design, and dose rate. In this paper, the dose-rate and bias dependencies are examined more closely. In addition, the post-irradiation annealing response is presented and shown to be different from standard MOSFET annealing response. Recommendations for hardness assurance are made on the basis of the observed trends.

II. Experimental Details

Analog Devices' (ADI) XFCB bipolar transistors (see Fig. 4 and reference [5]) were exposed to 10-keV x rays in an ARACOR 4100 semiconductor irradiation source. The transistors tested had either conventional, implanted emitters (herein called standard emitters) or polysilicon emitters. Several transistors were also exposed to ^{60}Co gamma rays. The dose rate ranged between 10 and 1760 rad(SiO_2)/s for the x-ray exposures, and between 1 and 250 rad(SiO_2)/s for the ^{60}Co exposures. Irradiations were performed under three bias conditions: all terminals grounded, 2 V reverse bias, and 0.5 V forward bias on the emitter-base junction (the collector was grounded). The post-irradiation room-temperature annealing response was monitored, and several polysilicon-emitter NPN devices

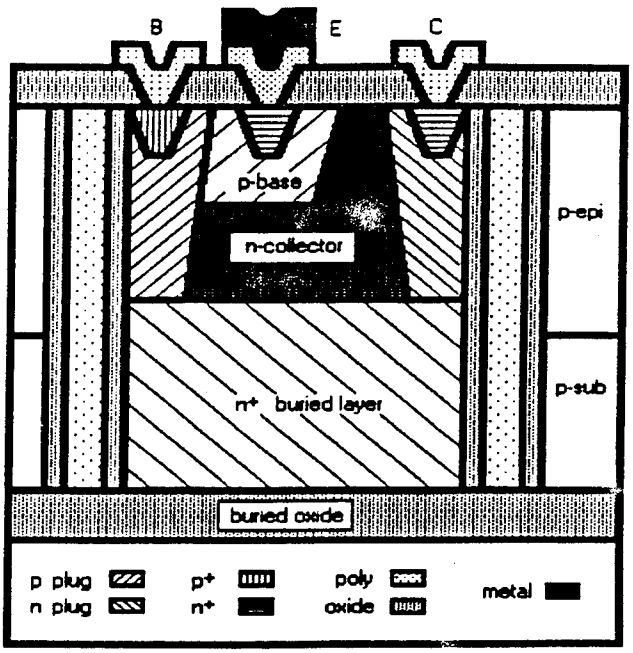


Fig. 4. Cross section of ADI's XFCB NPN transistor.

were isochronally annealed at elevated temperatures. The devices were characterized by measuring the changes in base and collector currents as functions of the total dose and the base-emitter voltage (standard Gummel measurements with $V_{CB} = 0$ V). The measurements were taken immediately following irradiation. The change in the current measured at $V_{BE} = 0.6$ V ($I_C \approx 1$ μA) is chosen as the figure of merit for the radiation-induced degradation in this work. The devices had an emitter size of 1.5 μm × 1.5 μm.

III. Results

It was mentioned in the introduction that MIL-STD-883D Test Method 1019.4 does not adequately cover the low-dose-rate response of bipolar technologies. Consequently, hardness assurance tests for bipolar technologies can be different than tests for MOS technologies. This is demonstrated in the following sections by two striking examples: (A) there is more degradation at lower dose rates than at higher dose rates, and (B) post-irradiation annealing reduces the degradation so that the low-dose-rate response cannot be predicted by high-dose-rate irradiation and annealing (as in 1019.4).

A. Dose-Rate Effects

Figure 5 shows the dose-rate dependence of the ionizing-radiation-induced change in base current at a total dose of 500 krad(SiO_2) for standard-emitter NPN

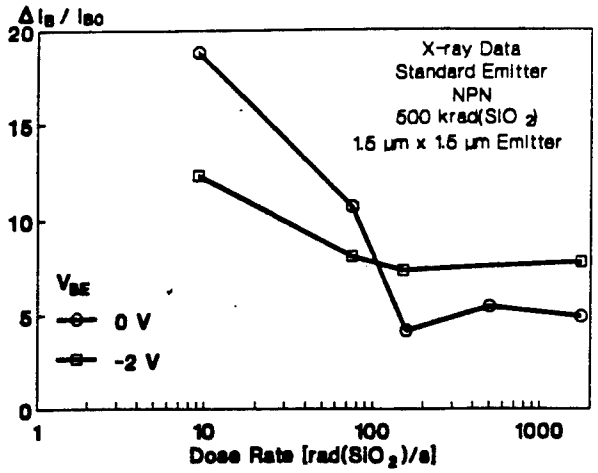


Fig. 5. Dose-rate dependence of the total-dose response of standard-emitter NPN devices irradiated in an x-ray source.

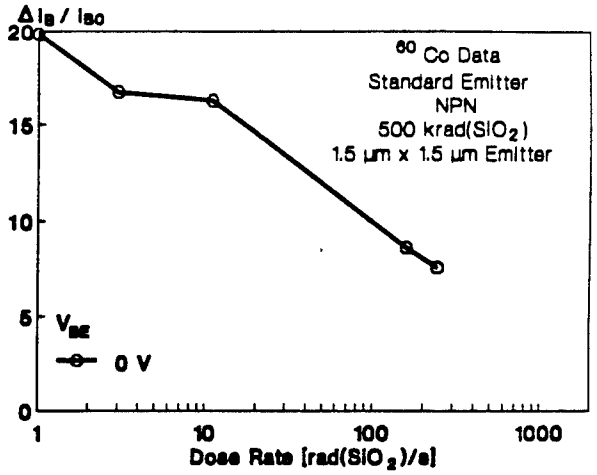


Fig. 6. Dose-rate dependence of the total-dose response of standard-emitter NPN transistors irradiated with ^{60}Co gamma rays.

transistors irradiated under two bias conditions in an x-ray source. (Each point on the curve represents an average of the excess base currents of two to four devices; the pre-irradiation, device-to-device variations in I_C measured at V_{BE} = 0.6 V were less than 20%.) Note that zero bias is the worst-case bias for low-dose-rate testing, while reverse bias is the worst-case bias for high-dose-rate testing. Note also that the magnitude of the degradation (excess base current) is greater at the low dose rates than at the high dose rates. In fact, the magnitude of the excess base current is nearly independent of dose rate above 150 rad(SiO_2)/s. Between 150 rad(SiO_2)/s and 10 rad(SiO_2)/s, the excess base current increases as the dose rate is lowered. The variation with dose rate is reduced in the reverse bias case. That is, in the zero-bias case, the excess base current at dose rates of 10 rad(SiO_2)/s or below is about 4 to 5 times the excess base current at dose rates of 100 rad(SiO_2)/s and above. On the other hand, in the reverse-bias case, the excess base current at dose rates of 10 rad(SiO_2)/s or below is only about 2 times the excess base current at dose rates of 100 rad(SiO_2)/s and above.

In ^{60}Co irradiations, the dose-rate dependence appears to weaken as the dose rate is lowered below 10 rad(SiO_2)/s. Figure 6 shows the dose-rate dependence of the excess base current for devices irradiated in several ^{60}Co gamma-ray sources. (The dose rates of the exposures in each source were confirmed by TLD measurements.) Comparing Fig. 5 and Fig. 6, note that for 150 rad(SiO_2)/s exposures of zero-biased devices, the ^{60}Co degradation is worse than the x-ray degradation by a factor of about 2. On the other hand, at the low dose rates, the magnitude of the excess base current is more nearly the same for gamma rays as for x rays. The correlation between x-ray and gamma-ray degradation is discussed in more detail in section IV.A. A possible mechanism for the dose-rate effect will be discussed in section III.C.

B. Annealing Response

The post-irradiation annealing response of standard-emitter, NPN transistors is shown in Fig. 7. At room temperature, the excess base current diminishes slightly. However, the excess base current is significantly reduced after a 30 minute, 100°C annealing cycle, and it continues to improve during subsequent

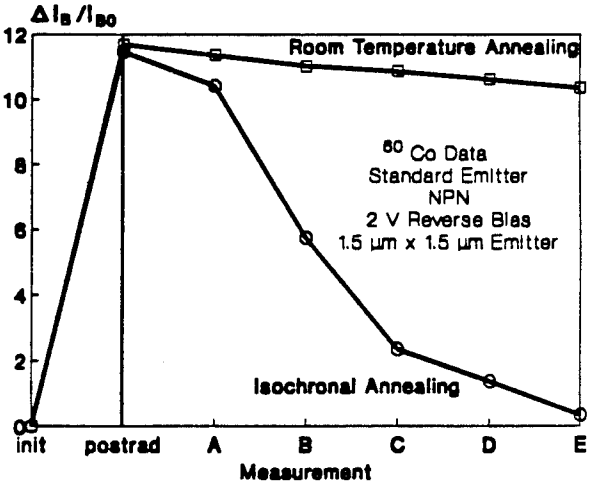


Fig. 7. Room-temperature and isochronal annealing responses of reverse-biased, standard-emitter NPN transistors. All measurements were taken after exposure to 500 krad(SiO_2) (post-rad) from ^{60}Co at 240 rad(SiO_2)/s, and after the isochronally annealed parts were annealed for 30 minutes at (A) 60°C, (B) 100°C, (C) 150°C, (D) 200°C, and (E) 250°C. The room-temperature parts were characterized at the same time as the isochronally annealed parts.

cycles, almost vanishing after the 250°C cycle. Similar results have been observed in the post-irradiation annealing response of polysilicon-emitter transistors. In addition, the post-irradiation annealing response is qualitatively independent of the dose rate at which the radiation exposure occurred. Furthermore, some of these devices have continued to anneal at room temperatures under bias for an additional 90 days after the termination of the elevated-temperature annealing cycles. No additional annealing has been observed in these parts.

The excess base current is sensitive to changes in the midgap-level interface-state density at the base surface and the net oxide-charge density in the base oxides [6,7]. The large improvement in base current after the 100°C annealing cycle suggests that, in addition to trapped-hole annealing, the midgap-level interface states anneal or perhaps transform in energy at temperatures at or above 100°C [8,9].

At first glance, the annealing of interface states appears to be contrary to what is observed in MOS technologies, where the elevated temperatures generally accelerate the formation of interface states. However, it must be noted that the gain degradation in bipolar devices is affected most strongly by the interface states *near midgap* [7]. MOS devices, on the other hand, are affected by the total charged interface-trap density at threshold. For zero-bias annealing experiments, McWhorter, *et al.* [8] showed that at 100°C, the interface-state density near midgap can decrease while that in the remainder of the gap actually increases significantly. Thus, the annealing results of Fig. 7 do not necessarily imply different interface-state annealing characteristics in these structures, but they certainly highlight the different effects of interface states on bipolar devices than on MOS devices.

MIL-STD-883D Test Method 1019 requires irradiating devices with ^{60}Co at dose rates between 50 and 300 rad(SiO_2)/s under worst-case bias conditions. It also specifies an annealing procedure to test for the rebound observed in MOS technologies, where oxide charges typically anneal and the interface states continue to accumulate [10]. However, these rebound effects are not observed in the post-irradiation annealing response of bipolar devices. Consequently, the dose-rate dependence of the total-dose response is *not* due to time-dependent increases in the interface state density. Therefore, in contrast to what has been observed in MOSFET's [11], the degradation achieved after irradiation and annealing does not provide a conservative estimate of the degradation obtained at lower dose rates.

Figure 7 demonstrates that the accelerated aging test in Test Method 1019.4 can not be applied to predict the low-dose-rate response of bipolar transistors. For example, if test method 1019.4 were applied to a bipolar device, instead of achieving the worst-case condition for low-dose-rate exposures, the device response would actually improve. Consequently, hardness-assurance approaches different than those used to predict MOS low-dose-rate response are required to predict the low-dose-rate response of bipolar devices and qualify BiCMOS parts for low-dose-rate applications.

C. Discussion

Dose-rate effects similar to those shown in Fig. 5 and Fig. 6 have also been observed in polysilicon emitter transistors as well as ADI-field-oxide capacitors irradiated with low-field conditions. For example, Fig. 8 shows what appears to be a dose-rate dependence of the midgap-voltage shift, ΔV_{mg}, in several ADI capacitors having 55 nm field-oxides. No clear trend in interface-state buildup was observed for these devices, but an increase in ΔV_{it} at low dose rates cannot be ruled out. As with the bipolar transistors, there is more shift at the lower dose rates. This suggests that the dose-rate phenomenon may be related to charge-yield in low-field thick oxides irradiated to high doses, a regime that has not been extensively studied in MOS technologies.

To date, the dose-rate effects of Fig. 8 have only been observed in MOS devices for these ADI field-oxide capacitors irradiated under zero-bias conditions. Positive-bias exposures for these capacitors and hardened capacitors from another technology do not exhibit

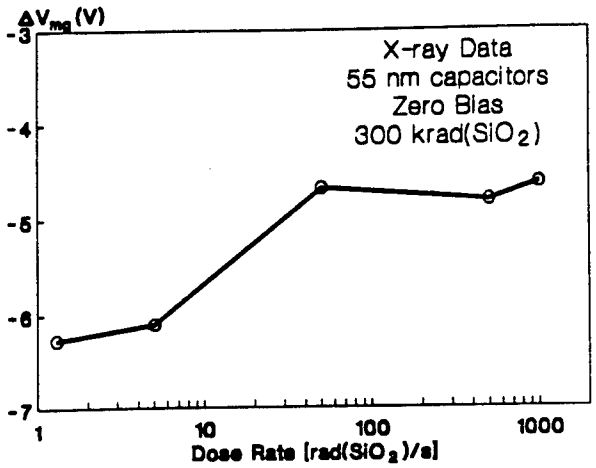


Fig. 8. Dose-rate dependence of the midgap voltage shift in ADI capacitors with 55 nm field-oxides at 0 V bias.

this dose-rate effect, consistent with other experience with MOS technology [11]. Furthermore, preliminary TSC studies [12] suggest that the dose-rate effect of Fig. 8 may be related to the charge distributions that develop in the thick oxides during the irradiations. These preliminary results indicate that, at the higher dose rates, more holes may accumulate in the bulk of the oxide and fewer may accumulate at the Si/SiO_2 interface. In contrast, at the low dose rates, fewer holes appear to accumulate in the bulk and more seem to trap near the interface. At the high dose rates, the larger hole density in the bulk tends to reduce the electric field in the bulk of the oxide. At the low dose rates, the bulk oxide electric field may be stronger due to the lower density of holes in the bulk. Therefore, at the low dose rates, the charge yield appears to be greater due to the larger electric fields, and the degradation at the interface is then worse than at the high dose rates. This unusual response may be associated with bulk damage to the oxide [13] due to the ion implantation through the base surface oxide.

This scenario is also supported by the x-ray to ^{60}Co correlation data discussed in section IV.A below in connection with Fig. 9 where the ratio of the x-ray degradation to the gamma-ray degradation increases from about 0.5 to 1.0 as the dose rate decreases. The increased ratio is consistent with an increase in field strength at the lower dose rates, since the x-ray-induced charge yield is more sensitive to the electric field than the gamma-ray-induced charge yield [14]. While this seems to be a consistent explanation of the dose-rate response of Figures 5, 6, 8, and 9, more work certainly is warranted on this topic.

IV. ADDITIONAL CONSIDERATIONS

A. X-ray to ^{60}Co Correlation

Since it is often convenient to perform high-dose-rate irradiations in 10-keV x-ray sources, the relationship between the x-ray response and the gamma-ray response needs to be studied. Figure 9 shows the ratio of x-ray-induced degradation to ^{60}Co-induced degradation as a function of total dose for standard NPN devices. Factors that influence x-ray to ^{60}Co comparisons at a given dose rate include dose-enhancement (typically greater in the x-ray case) and charge yield (typically greater in the ^{60}Co case) [14]. In the zero-biased devices irradiated at 150 rad(SiO_2)/s, the ^{60}Co-induced degradation is worse than the x-ray-induced degradation by factors ranging from about 1.5 at low total doses to 2 at higher doses. The ^{60}Co degradation is worse than

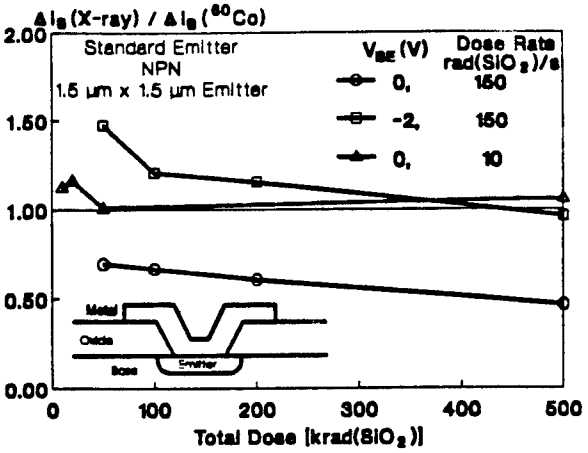


Fig. 9. Ratio of 10-keV x-ray-induced degradation to ^{60}Co-induced degradation. Inset shows cross-section of base surface oxides that are damaged by the irradiations. Electric fields in these oxides are significant factors in the radiation response. and the x-ray to ^{60}Co correlation.

the x-ray degradation since recombination of radiation-generated carriers in the oxide during x-ray irradiation at low fields is enhanced (*i.e.*, charge yield is reduced) over that which occurs during ^{60}Co exposures. For the reverse-biased devices, where the electric fields in the base surface oxides are stronger than in the zero-biased devices, the x-ray degradation is slightly worse than the ^{60}Co degradation for low total doses. The enhanced x-ray response suggests dose enhancement in these structures [14]. The polysilicon layers in the XFCB transistors are contacted by a platinum silicide. Platinum is a high-Z material that may emit secondary electrons and cause dose enhancement. Dose enhancement appears to dominate the comparison in Fig. 9 under the reverse-bias condition, while charge-yield appears to dominate under the zero-bias condition.

The results of Fig. 9 appear to be consistent with how the ratio, ΔV_{ox}(x-ray)/ΔV_{ox}(^{60}Co), depends on electric field for MOS devices [14]. At low fields, the ratio is less than that at higher fields because the x-ray results vary more strongly with charge yield at low fields than do the ^{60}Co results [14,15]. This may explain the decreasing ratios of ΔI_B(x-ray)/ΔI_B(^{60}Co) for the -2 V and 0 V bias cases at 150 rad(SiO_2)/s. At lower dose rates, there is a modest built-in field in the spacer oxides. As trapped holes build up in the oxide with increasing dose, space-charge effects in the oxide can decrease the electric field in the bulk of the spacer oxide [14]. As the bulk oxide field decreases with increasing dose, ΔI_B(x-ray)/ΔI_B(^{60}Co) also decreases due to the increasing difference in x-ray to ^{60}Co charge yield with decreasing electric field [14,15]. At 10 rad(SiO_2)/s, on the other hand, this ratio stays constant with increasing dose, suggesting that changes in the base-oxide field during

irradiation are not as significant in these devices at low dose rates as at higher rates. In addition to showing that the x-ray to ^{60}Co correlation for bipolar/BiCMOS devices can depend on the dose rate of the irradiation, these results also suggest that changes in the base-oxide electric field with total dose or dose rate may play a role in determining the unusual dose-rate response of bipolar devices illustrated in Fig. 5, as was discussed above in section III.C.

B. Switched-Bias Experiments

The results presented thus far in this paper show the response of standard emitter transistors. In general, polysilicon-emitter transistors exhibit qualitatively similar behavior. However, there is one notable exception in the XFCB technology, which may be present in other technologies as well. In addition to an increased base current as a result of exposure to ionizing radiation, there is also an increase in collector current during ionizing-radiation exposures of polysilicon-emitter transistors under reverse bias.

To further investigate the role of the emitter bias in hardness-assurance testing, polysilicon-emitter NPN devices were irradiated to 1 Mrad(SiO_2) with V_{BE} = - 2 V, and then subsequently irradiated to another 1 Mrad(SiO_2) with V_{BE} = 0.5 V. Figure 10 shows the response of both the base and collector currents during the switched-bias experiment. The collector current increases by a factor of five during the first Mrad(SiO_2), and then during the second Mrad(SiO_2), the initial damage is effectively removed. These results are strikingly similar to the radiation-induced charge neutralization observed in MOS switched-bias experiments,

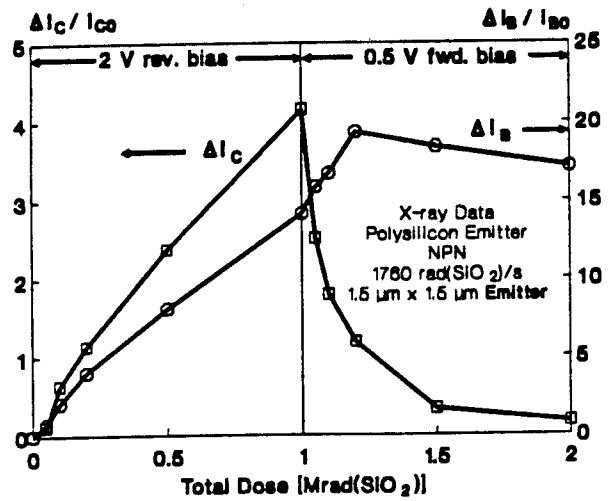


Fig. 10. Switched-bias experiment on poly-emitter NPN transistors irradiated with x-rays. The dose rate was 1760 rad(SiO_2)/s.

where the threshold voltage shifts were reversed when the gate bias was changed during irradiation [16].

The increased collector current is a voltage-dependent current, and it appears only in XFCB polysilicon-emitter, NPN transistors irradiated under reverse bias. It does not appear in the XFCB standard-emitter devices or in PNP devices. In addition, it does not appear in polysilicon-emitter devices fabricated in two different processes. Furthermore, in the XFCB process, there are differences beyond the emitter fabrication that distinguish the polysilicon devices from the standard devices: namely, the bases also have different design parameters. Consequently, this phenomenon is highly process dependent and may appear in other technologies. Therefore, in terms of hardness assurance, care should be taken to monitor the collector current to test for this effect.

V. Hardening and Hardness Assurance

Based on the observed trends summarized in sections III and IV, several recommendations can be made regarding possible hardening approaches and hardness-assurance testing for modern bipolar transistors.

A. Possible Hardening Approaches

Since the excess base current is sensitive to the base surface condition (*i.e.*, doping distribution, potential distribution, geometry, electric fields in the base surface oxides, and implanted-ion distributions in the base surface oxides), it may be possible to further improve the radiation hardness of bipolar devices by increasing the base surface doping. Furthermore, field oxides implanted with various ion species have been demonstrated to improve both hot-electron and radiation hardness [17,18,19]. In addition, reducing the thickness of the base surface oxides will improve radiation hardness.

Radiation hardness may also be improved by designing devices with minimum emitter perimeter-to-area, *P/A*, ratios or by using minimum *P/A* devices in circuit designs. The geometric dependence of the total-dose response was shown in Fig. 3 and is further demonstrated in Fig. 11. For example, large circular-emitter designs minimize the emitter *P/A* ratio, and thus minimize the relative increase in the base current due to irradiation. The next best possibility for designing for improved hardness would be to use large square emitter designs. The worst-case design for radiation hardness, which nevertheless is commonly used to increase the current drive capacity of the device, is to

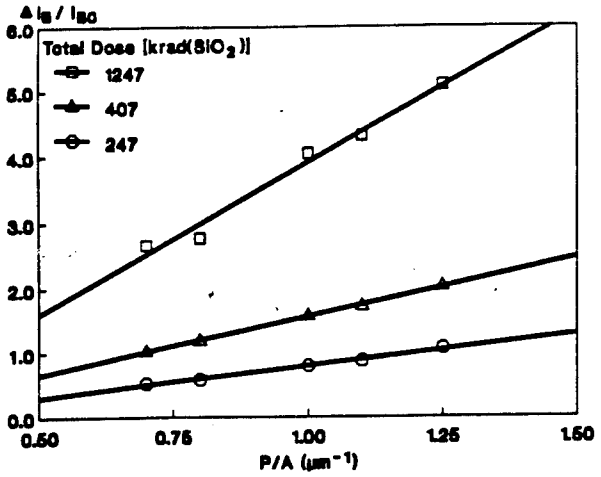


Fig. 11. Emitter perimeter-to-area dependence of the total-dose induced excess base current.

fabricate devices with several long and narrow emitter fingers. Such devices provide large area, but also have very large perimeters, giving a large *P/A* ratio.

A third possible hardening approach relies on using appropriate circuit design rules. Note in Fig. 1 that the peak gain shifts to higher collector currents as the total dose increases. Many circuits are designed to operate at collector currents slightly below the peak-gain bias condition. However, this is worst-case for total-dose gain degradation since it is the low current gain that degrades most severely. Instead, if slightly higher power consumption can be tolerated, circuits should be designed to operate slightly above the peak-gain condition to improve their radiation hardness. Since the peak gain shifts to higher currents during irradiation, the gain at the higher bias condition will not degrade so severely.

Of course, the design suggestions mentioned above imply tradeoffs. Designing for hardness assurance requires large-area, high-current devices. Such a design is incompatible with most BiCMOS applications. An alternate and preferable approach to hardening would be to minimize the intrinsic-base surface area between the base contact and the edges of the emitter, since it is this area that is susceptible to the ionizing-radiation damage. The reduction of the base surface area is compatible with scaling the devices down for higher packing density in a BiCMOS application.

B. Hardness-Assurance Testing Recommendations

The following recommendations are made for testing bipolar/BiCMOS devices. Though the discussion in this paper has concentrated on the results observed in one technology, four other technologies have been studied with many of the responses found to be qualitatively similar in terms of their dose-rate, geometry, and bias dependencies. Thus, the hardness assurance tests we recommend should provide a reasonable starting point for developing standard tests for bipolar hardness assurance. In this regard, it is important to remember that, because of the dose-rate effects and the failure of high-temperature annealing to predict the low-dose-rate response, the hardness-assurance testing approach will depend directly on the expected application of the device. In addition, these recommendations apply only to NPN devices. The dose-rate effects have not been observed in PNP devices, possibly because the recombination occurs at the emitter surface of these devices and the higher doping minimizes the device susceptibility [2].

Devices intended for high-dose-rate environments should be irradiated to the specified dose while under reverse-bias in a ^{60}Co source. The dose rate should be above 100 rad(SiO_2)/s. (Care should be taken not to reverse bias the device strongly enough to introduce hot-electron damage in addition to the ionizing-radiation-induce damage. A reverse-bias voltage that is around one-third of the reverse breakdown voltage should suffice for most modern devices.) Both the collector and base current should be monitored. The characterization should be performed at the circuit (forward) bias level at which the device is intended to be used. In other words, if the in-circuit base-emitter bias is expected to be around 0.7 V, for example, then the gain, excess base current, and excess collector current should all be measured at V_{BE} = 0.7 V.

A different testing approach is required if the devices are intended for low-dose-rate space applications. In this case, zero-biased devices should be irradiated to the total dose of interest in a ^{60}Co source at a dose rate of 10 rad(SiO_2)/s or below. Again, the change in the base current or the change in the dc current gain should be measured at the intended bias for the device. A factor-of-two margin should be used to account for the increased degradation at the lower dose rates. A larger factor may be necessary if the disparity between the test dose rate and the application dose rate is large.

Most significantly, to reiterate, do not bake bipolar devices in an attempt to predict the low-dose-rate response as in Test Method 1019.4 for MOS devices. In a bipolar device, the post-irradiation annealing will reduce the apparent damage, which is the opposite effect of lowering the dose rate.

VI. Summary and Conclusions

The dose-rate dependence of the total-dose gain degradation in bipolar transistors has been mapped for a wide range of dose rates for the first time. In addition, it has been shown that the post-irradiation annealing response does not simulate the greater degradation observed at the lower dose rates. Preliminary field-oxide capacitor studies suggest that the mechanism for the dose-rate effect may be related to charge yield in the base surface oxides, and studies of the correlation between x-ray and ^{60}Co degradation support this scenario. Based on the observed experimental trends, possible hardening approaches for bipolar technologies have been identified. Furthermore, recommendations for hardness-assurance testing of bipolar devices include testing at dose rates below 10 rad(SiO_2)/s and applying safety factors (margin) to estimate the space-environment response.

VII. Acknowledgments

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V.D. Charge Separation for Bipolar Transistors

Charge Separation for Bipolar Transistors

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Abstract

The role of net positive oxide trapped charge and surface recombination velocity on excess base current in BJTs is identified. Although the interaction of these two radiation-induced defects is physically complex, simple approaches for estimating these quantities from measured BJT characteristics are presented. The oxide charge is estimated using a transition voltage in the plot of excess base current vs. emitter bias. Two approaches for quantifying the effects of surface recombination velocity are described; the first measures surface recombination directly using a gated diode. The second estimates its effects using an intercept current that is easily obtained from the BJT itself. The results are compared to two-dimensional simulations and measurements made on test structures. The techniques are simple to implement and provide insight into the mechanisms and magnitudes of the radiation-induced damage in BJTs.

I. INTRODUCTION

Bipolar junction transistors (BJTs) continue to play an important role in integrated-circuit technology, particularly in the areas of analog or mixed-signal ICs and BiCMOS circuits. In earlier bipolar technologies, the limiting factor for using BJTs in total-dose environments was typically excess leakage caused by trapped positive charge in the field oxide [1, 2]. However, this problem can be solved by appropriate process design and layout techniques. For many current bipolar technologies, the total-dose failure mechanism is reduction of the current gain (I_C/I_B).

The current gain of modern bipolar transistors in an ionizing radiation environment decreases due to increased recombination in the emitter-base depletion region [3-6]. The recombination current increases because of two interacting effects: (1) increased surface recombination velocity and (2) spreading of the emitter-base depletion region. The increase in surface recombination velocity is proportional to the density of recombination centers at the silicon/silicon dioxide interface that covers the emitter-base junction. These recombination centers are related to, although not precisely the same as, the interface traps that are commonly discussed in relation to MOS technologies.

Since the net charge introduced into the oxide by ionizing radiation is positive, the depletion region spreads on the *P*-side of a *PN* junction. For *NPN* transistors, this means that the depletion region spreads into the relatively lightly doped *P*-type base region. As the depletion region increases in size, recombination current increases at the oxide interface over the base and in the newly-depleted silicon bulk.

In order to better understand these two degradation mechanisms and develop hardening approaches for a specific process technology, it is necessary to measure the effect of each mechanism separately. A similar situation exists in MOS devices; significant progress in understanding complex time-dependent effects and improving device hardness has resulted from the ability to separate the electrical effects of radiation-induced oxide trapped charge, ΔN_{ot}, and interface traps, ΔN_{it}. In recent years, several techniques have been developed to separate ΔN_{ot} and ΔN_{it} in MOSFETs [7-10] and ASTM standards have been developed for the subthreshold and charge pumping techniques. The reason for the success of multiple techniques for charge separation in MOSFETs is that the effects of ΔN_{ot} and ΔN_{it} are not interactive to first order. For example, ΔV_{th} is simply an additive effect of two voltage shifts ΔV_{ot} and ΔV_{it}. The room temperature long term ionization-induced change in transconductance, Δg_m, is mainly a result of the effect on mobility of ΔN_{it} [8, 9].

To date, no charge-separation technique for bipolar transistors is available. In BJTs, the combined effects of net positive charge in the oxide and interface states are strongly nonlinear. The main parameter affected by ionizing radiation, increased base surface recombination current (ΔI_B), is an interactive combination of ΔN_{ot} and near-midgap ΔN_{it} [3, 11]. The oxide charge changes the surface potential along the base surface, causing depletion in an *NPN* transistor. The interface states near midgap cause an increase in the surface recombination velocity. Since the surface recombination rate is strongly dependent on the surface potential, the effects of ΔN_{ot} and ΔN_{it} on ΔI_B are interactive and not simply additive. In addition, the quantities of interest in BJTs are not precisely the same as those in MOSFETs: ΔN_{it} in MOSFETs is a measure of the number of charged interface states at threshold. In BJTs, on the other hand, the excess base current depends on the number of interface states (recombination centers) near midgap, not the total number between midgap and threshold. The excess base current due to changes in surface potential depends on the total radiation-induced oxide charge at the bias condition and lateral position

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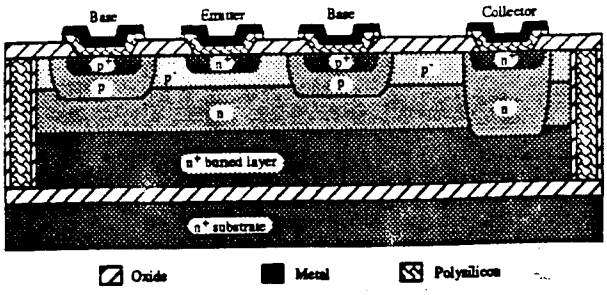


Figure 1. Representative cross-section of the devices studied in this work.

Table 1. Relevant device parameters for the two device technologies studied in this work.

	Technology A	Technology B	Units
e-b junction depth	0.3	0.3	μm
Intrinsic Base Surface Doping	9.0×10^{17}	7.5×10^{17}	cm^{-3}
Oxide Thickness	5450	550	$\AA$

of interest. In general, this includes contributions of both fixed oxide charge and charged interface traps. These considerations greatly complicate the development of a simple charge separation technique for bipolar transistors.

The charge-separation approach described in this paper uses easily measured changes in the ΔI_B vs. V_{BE} curve to estimate the effects of changes in surface recombination velocity and charge in the oxide. While the net charge in the oxide is certainly related to both ΔN_{ot} and ΔN_{it} and the surface recombination velocity is related to ΔN_{it}, it is essential to note that these quantities are not identical to the ones used to describe ionizing-radiation effects in MOSFETs. It is preferable to use natural quantities that describe the physics of the device instead of force-fitting quantities from other devices.

II. Experimental Details

Two device technologies were studied in this work. Relevant structural information for both technologies is summarized in table 1. A representative cross-section of devices from technology A is shown in figure 1. The devices are oxide-isolated polysilicon emitter bipolar transistors fabricated in a complementary bipolar process [12]. Process B is a related BiCMOS process.

The irradiations of devices from technology A were performed in a Co-60 source at a dose rate of 10 rad(Si)/s. Devices from technology B were irradiated with 10 keV x-rays at a dose rate of 1.7 krad(SiO_2)/s. All pins were grounded during irradiation. A Hewlett-Packard 4145B Semiconductor Parameter Analyzer was used for device characterization.

III. Overview of Recombination Current in BJTs

Exposure to ionizing radiation usually degrades the current gain in bipolar transistors by increasing the base current while leaving the collector current approximately constant [3-6]. A typical plot of common-emitter current gain, I_C/I_B, versus base-emitter voltage, V_{BE}, for several values of total ionizing dose is shown in figure 2. The current gain degrades substantially with increasing total dose, especially at lower V_{BE}. The decrease in

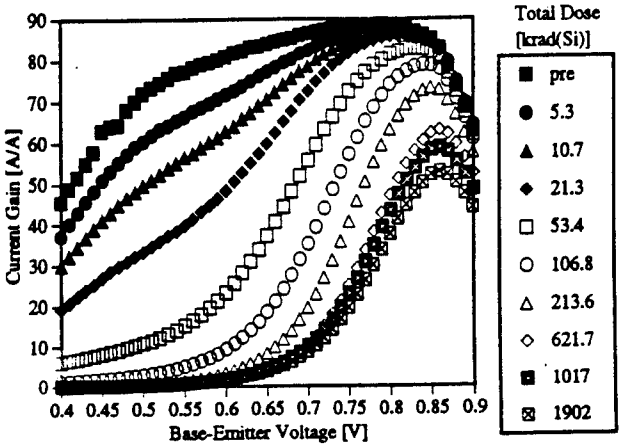


Figure 2. Current gain versus base-emitter voltage for technology A.

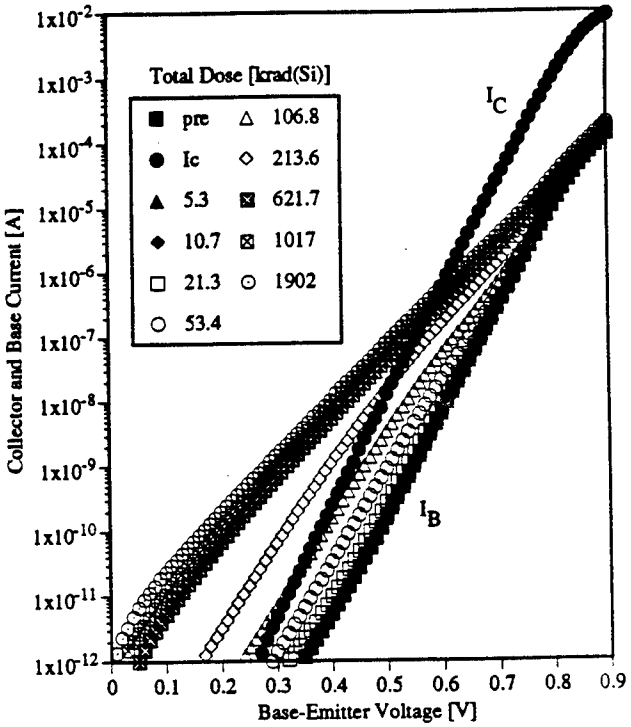


Figure 3. Gummel plot corresponding to figure 2.

current gain is primarily due to an increase in base current, as seen in figure 3.

For convenience it is usually assumed that recombination current in *PN* junctions varies as exp $[\beta V/n]$, where n, the ideality factor, is equal to two and β is the inverse thermal voltage (q/kT). In contrast, the ideal component of the current due to injection over the potential barrier associated with the junction has an ideality factor of one. In fig. 2, note that the pre-rad base current has a slope corresponding to $n = 1$, and the slope of the post-rad base current decreases for low V_{BE}, corresponding to $n > 1$. The fact that $1 < n < 2$ in many cases has important consequences for charge separation, as will be demonstrated below.

IV. A Simple Charge-Separation Method

To separate the degradation mechanisms, it is necessary to focus on the primary device parameter affected by ionizing radiation: the *excess* base current. The base current is written, in general, as the sum of the pre-irradiation base current plus the excess base current due to irradiation: $I_B = I_{B,pre} + \Delta I_B$. A plot of ΔI_B vs. V_{BE} is shown in fig. 4. In this figure, there are two different total-dose ranges to notice: (1) at relatively low total doses, the curves have two different slopes, corresponding to an ideality factor of two ($n = 2$) for large V_{BE}, and $n < 2$ for small

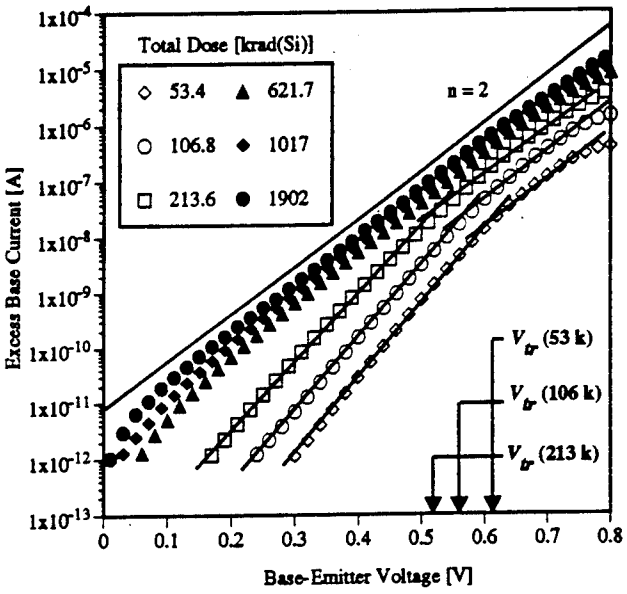


Figure 4. Excess base current versus base-emitter voltage corresponding to figures 2 and 3.

V_{BE}, and (2) for relatively high total doses, the excess base current has $n = 2$ for almost the entire voltage range of interest. Each region will be discussed in detail below, and the physics responsible for the behavior will be described. However, it is useful to describe the role these curves play in charge separation first to motivate the detailed analysis.

First, consider the ΔI_B curves that exhibit two distinct slopes (the lower total-dose curves). It will be shown that the slope corresponding to $1 < n < 2$ is a clear indication that surface recombination near the junction is dominant. The transition to $n = 2$ at higher values of V_{BE} is a signature of predominantly subsurface, rather than surface, recombination. The voltage at which this transition occurs is an indication of the amount of radiation-induced charge in the oxide covering the emitter-base junction and the intrinsic base. In fig. 4, the transition voltage, V_{tr}, is shown for three values of total dose. This transition voltage can be determined graphically by linearly extrapolating the low-voltage portion of the curve and noting its intersection with a linear extrapolation of the higher-voltage, $n = 2$, range. The shift in the transition voltage is a direct measure of the change in surface potential due to radiation-induced charge, and it can be converted to a value for the net charge in the oxide using a procedure described below.

The other parameter of interest is the surface recombination velocity, v_{surf}. It is straightforward to measure the surface recombination velocity using a gated diode, if one is available for the process technology of interest. A gated diode is simply a *PN* junction with a gate surrounding the junction. The voltage on the gate can be varied independently of the bias on the junction to allow direct control over the surface potential. The surface recombination velocity is directly proportional to the peak in the forward diode current. In this way, the contribution of surface recombination to the diode current can be determined and a value for surface recombination velocity can be obtained. The diode current is plotted vs. gate voltage in fig. 5 for a gated

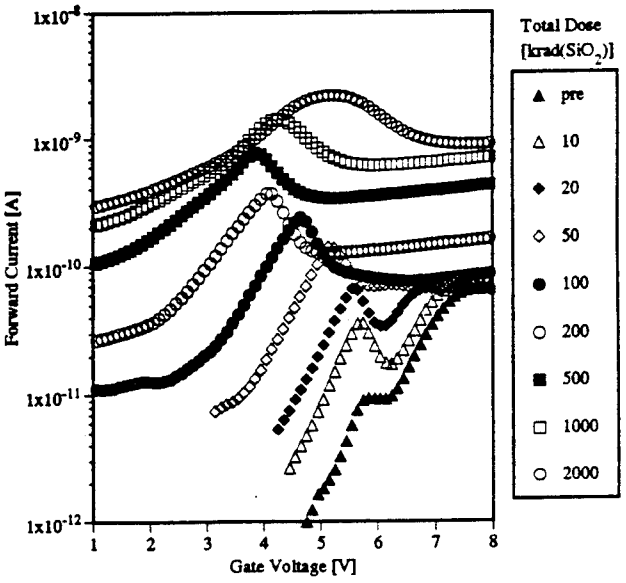


Figure 5. Gated diode current versus gate voltage for a gated diode from technology B. Diode is forward-biased at 0.1 V.

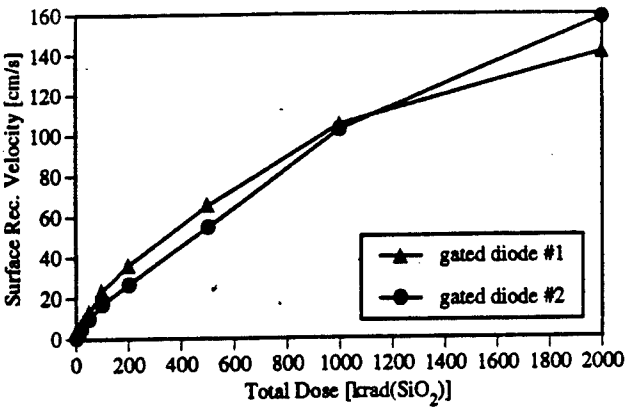


Figure 6. Surface recombination velocity calculated from the gated diode current in figure 5.

diode constructed with the same oxide that covers the emitter-base junction in technology B. Surface recombination velocity, measured using the gated diodes, is plotted vs. total dose in fig. 6.

If a gated diode is available for characterization, the surface recombination velocity can be measured as a function of total dose. However, if no gated diode is available, it is still possible to estimate the effects of variation of the surface recombination velocity using only measurements performed on BJTs. In this case, the relevant experimental parameter is the intercept of the ΔI_B vs. V_{BE} curve with the current axis. The intercept current, I_i, provides an indication of the effects of surface recombination velocity. Figure 4 shows that the intercept current increases monotonically with total dose, as does the surface recombination velocity plotted in fig. 6. Intercept current and surface recombination velocity will be compared in Section VI.B.

The total dose at which the transition to a ΔI_B-vs.-V_{BE} curve with a slope corresponding to $n = 2$ over most of the voltage region of interest occurs is also important. At this total dose,

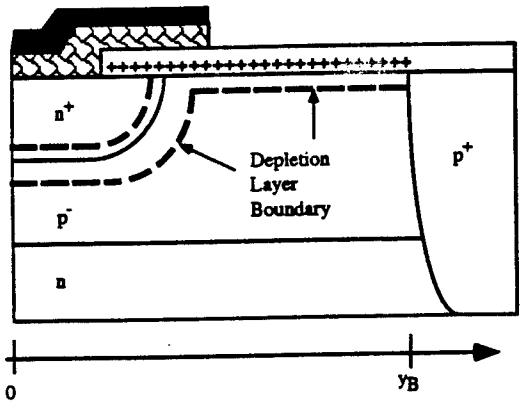


Figure 7. Schematic cross-section of the base-emitter junction showing effect of oxide charge on the depletion layer.

sufficient charge has been accumulated in the oxide to cause significant recombination to occur throughout the intrinsic base. Once this condition occurs, the excess base current is proportional to the total area of the intrinsic base, and further increases in ΔI_B with total dose are relatively small. This concept is illustrated schematically in fig. 7.

In summary, two simple approaches to charge separation have been outlined. Both require obtaining a plot of the log of the excess base current vs. the emitter-base voltage. The contribution of oxide charge is estimated from changes in an easily obtained transition voltage. If gated diodes are available in the technology of interest, surface recombination velocity can be measured directly from the change in the peak diode current. If no gated diode is available, the effect of changing surface recombination velocity can be determined from changes in the intercept of the excess gate current plot with the current axis.

V. Analysis of Surface Recombination

It is necessary to understand the factors contributing to the increased base current before the charge-separation techniques described above can be justified. The discussion that follows identifies the effects of surface recombination velocity, charge in the oxide, and applied bias on the recombination current. Following this discussion, it will be shown how the relevant parameters can be estimated from combined measurements of transistors and gated diodes, or if test structures are not available, from simple electrical measurements performed on transistors.

The excess base current is due to increased electron-hole recombination in the lightly-doped intrinsic base of the BJT. The increase is the result of two interacting factors: (1) increased surface recombination velocity and (2) spreading of the emitter-base depletion region. The increase in surface recombination velocity is proportional to the formation of recombination centers at the silicon/silicon dioxide interface that covers the emitter-base junction. Since the net charge introduced into the oxide by ionizing radiation is positive, the depletion region spreads on the P-side of the junction. For low total doses, the majority of the increased recombination occurs at the oxide-silicon interface around the periphery of the emitter-base junction. The recombination process is described by Shockley-Read-Hall (SRH) recombination statistics. It is shown in the Appendix that the recombination rate at a particular point along the surface can be represented by:

$$R_s(y) \approx \frac{\frac{1}{2} n_i v_{surf} \exp\left[\frac{\beta V_{BE}}{2}\right]}{\cosh\left[\beta\left(\psi_s(y) - \frac{V_{BE}}{2}\right)\right]}, \qquad (1)$$

where n_i is the intrinsic carrier concentration, β is the reciprocal thermal voltage, and ψ_s is the surface potential at a distance y

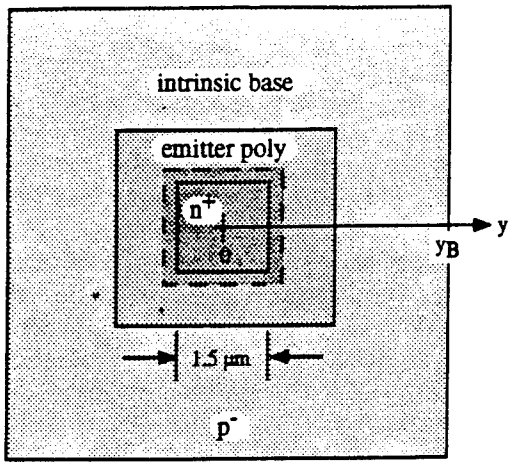


Figure 8. Top view of the BJT.

from the metallurgical junction. The reference for potential is defined in the Appendix. The recombination rate reaches a maximum value at the position where the electron and hole concentrations are equal, a condition described as cross-over. In eqn. (1), R_s is maximized when $\psi_s = V_{BE}/2$. The form of R_s, and thus the excess base current, clearly depends on the precise form of $\psi_s(y)$, which in turn depends upon the doping profile of the junction, V_{BE}, and the net positive charge in the oxide, N_{ox}. The interrelationship of these parameters is a key element in the development of a charge-separation technique.

In most analytical treatments of recombination near a *PN* junction, the spatial dependence is neglected; instead, it is usually assumed that the total recombination rate can be obtained from the behavior of the peak recombination rate [13]. In an ideal, abrupt one-dimensional junction the recombination rate decreases rapidly as the distance from the recombination peak increases. This justifies the usual assumption that the total recombination current can be described by the behavior of the peak. However, in an irradiated BJT, this assumption is subject to important limitations. First, the doping distribution is not abrupt, so the potential variation with position is more gradual than it is for an abrupt junction. Second, the presence of positive charge in the oxide covering the emitter-base junction increases the surface potential throughout the intrinsic base. As the surface potential increases, the recombination rate in the portions of the intrinsic base farther from the metallurgical junction increases. It is necessary to include the surface recombination current throughout the intrinsic base to adequately describe the effects of ionizing radiation. This can be done by integrating equation (1) with respect to position. The total excess base current is then obtained by multiplying the integrated recombination rate by the electronic charge, q, and the emitter perimeter, P_E:

$$\Delta I_B = \alpha \, v_{surf} \exp\left[\frac{\beta V_{BE}}{2}\right] \gamma(N_{ox}, V_{BE}) \quad , \quad (2)$$

where

$$\alpha = \frac{1}{2} q \, n_i \, P_E \quad (3)$$

and

$$\gamma(N_{ox}, V_{BE}) = \int_0^{y_B} \frac{dy}{\cosh[\beta(\psi_s(y) - V_{BE}/2)]} + \frac{2\pi}{P_E} \int_0^{r_B} \frac{r \, dr}{\cosh[\beta(\psi_s(r) - V_{BE}/2)]} \quad (4)$$

where $r_B = \sqrt{2}\, y_B$. A top view of the BJT illustrating the coordinate convention is shown in fig. 8. Note that the integral in equation (4) is a function of surface potential. While the peak recombination rate increases exponentially with voltage as exp $[\beta V_{BE}/2]$, the total recombination rate exhibits a somewhat different voltage dependence because of the contribution of the integral. This variation is seldom considered, but it plays an important role in surface recombination. Figure 9 plots the ideality factor (n) at a fixed base-emitter voltage for the surface recombination current vs. net oxide charge obtained from two-dimensional simulation of the devices (described in Section VI.A). The ideality factor never actually reaches the "ideal" value of two for this device; again, this is a consequence of the distributed nature of the recombination process. In contrast to the behavior of the total recombination rate shown in fig. 9, the peak value of the recombination obtained from simulations increases exactly with an ideality factor of two.

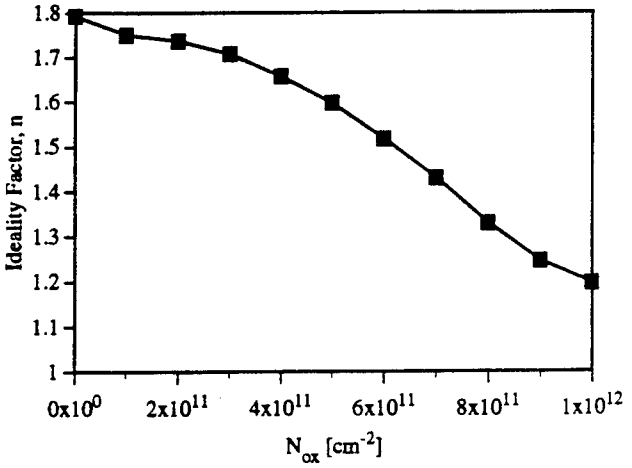


Figure 9. Diode ideality factor versus trapped charge.

In principle, the value of the ideality factor could be used as an indicator of the amount of net oxide charge at a given dose. However, this requires extensive (and extremely accurate) simulations of the device structure. It is difficult to obtain a level

of accuracy that permits reasonable confidence in charge values extracted using this method.

In earlier work, it was reported that the radiation-induced excess base current may increase superlinearly with dose [4–6]. This phenomenon was surprising because defect densities in MOS devices generally increase linearly, or more slowly, with dose. However, the discussion associated with equation (2) provides a possible explanation for this effect. The surface recombination velocity, and thus the excess base current, is directly proportional to the number of interface traps with energies near midgap. The increase in base current due to the interface traps is *multiplied* by the integral that describes the effect of the net charge in the oxide. This integral increases with total dose as the recombination peak broadens and spreads into the intrinsic base. Although each of these effects may be linear, or sublinear, with dose, the combined effect may be superlinear, consistent with the response often observed experimentally [4].

VI. Radiation Effects on Excess Base Current

A. *Effect of Net Positive Charge*

Oxide charge affects the excess base current by changing the spatial variation of the surface recombination. The potential distribution near the emitter-base junction is plotted in fig. 10(a) for several values of net positive charge in the oxide and fixed base-emitter voltage and the corresponding surface recombination rate is shown in fig. 10(b). These plots were obtained from S-PISCES 2B [14] simulations of the structures examined in this work. The doping profile of the junction was obtained with SUPREM simulations and verified with spreading resistance measurements. The effect of introducing the positive charge is to raise the surface potential in the silicon, especially in the region far from the junction. Far from the emitter-base junction in the intrinsic base region, ψ_s can be written as $\psi_{s,IB}$, where

$$\psi_{s,IB} = \psi_{N_{ox}} + V_{BE} - \frac{1}{\beta} \ln\left(\frac{N_s}{n_i}\right) . \qquad (5)$$

ψ_{Nox} is the band-bending caused by N_{ox} and is given by

$$\psi_{N_{ox}} = \frac{q\, N_{ox}^2}{2\, \varepsilon_{Si}\, N_s} . \qquad (6)$$

In these expressions, N_s is the surface concentration of the intrinsic base and ε_{Si} is the permittivity of silicon. The crossover point moves from the surface into the bulk at a transition voltage, V_{tr}, defined when $\psi_s = V_{BE}/2$ in the intrinsic base far from the junction. From eqns. (5) and (6), the value of N_{ox} for which this transition occurs can be expressed as:

$$N_{ox} = \sqrt{\frac{2\, \varepsilon_{Si}\, N_s}{q}\left(\frac{1}{\beta} \ln\left(\frac{N_s}{n_i}\right) - \frac{V_{tr}}{2}\right)} \qquad (7)$$

Equation (7) is plotted in fig. 11. Note that only a limited range

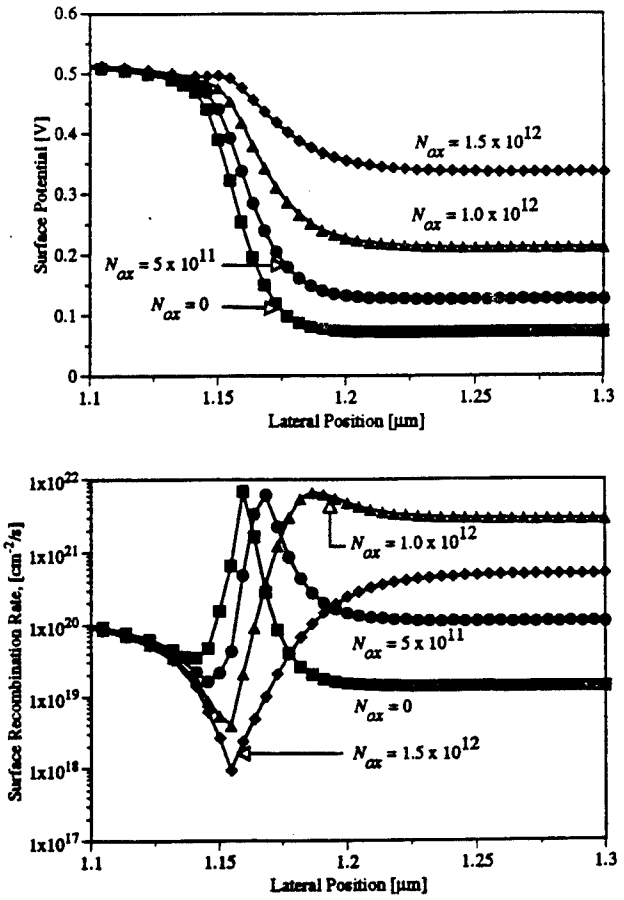


Figure 10. PISCES simulation results for the emitter-base junction from technology B. The junction is located at $y = 1.16$ μm. $V_{BE} = 0.5$ V with varying oxide charge in units of cm^{-2}. a) Surface potential versus lateral position. b) Surface recombination rate versus lateral position.

of V_{tr} can be observed in practice. For low V_{BE}, the currents are too small to be measured accurately, while for large V_{BE}, high-level injection sets in, which violates the assumptions made in the derivation of eqn. (1).

The changes in the potential distribution have a very significant effect on the recombination current, both in the depletion region near the junction and in the intrinsic base region farther from the junction. This can be seen in fig. 10(b) for the specific case of $V_{BE} = 0.5$ V and varying charge in the oxide. In this figure, the surface recombination velocity was selected so that the recombination time constants for electrons and holes at the surface are the same as the bulk lifetimes. The peak in the surface recombination current occurs at the point where the electron and hole concentrations equal each other ($n_s = p_s$), which is also the point at which $\psi_s = V_{BE}/2$. Note that the peak in R_s is independent of N_{ox} for low N_{ox}; this is because the peak value of R_s is set by V_{BE}. Also note that R_s ceases to be a peaked function for large N_{ox}. For R_s to have a maximum, ψ_s must equal $V_{BE}/2$. If ψ_s is always larger than $V_{BE}/2$, then R_s will not exhibit a maximum. In this case, the maximum recombination rate occurs in the

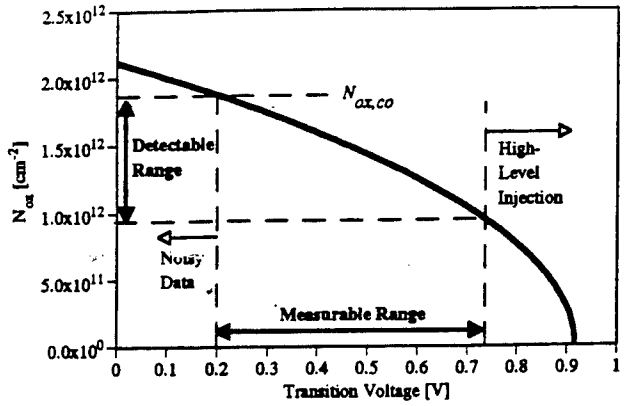


Figure 11. Oxide charge versus transition voltage for technology B.

below the surface, rather than at the surface, of the intrinsic base.

For a given V_{BE}, the integral exhibits a maximum value at a certain value of N_{ox}. At this combination of N_{ox} and V_{BE}, the peak in R_s has vanished and $\psi_s = V_{BE}/2$ over the entire intrinsic base. A subsequent increase in either N_{ox} or V_{BE} will cause R_s to decrease and force the maximum recombination point away from the surface and into the bulk. On the other hand, a decrease of either N_{ox} or V_{BE} will cause R_s to become more peaked. It is evident that the voltage at which the γ integral peaks for a given value of N_{ox} is significant, since it marks the transition between predominantly surface recombination and predominantly subsurface recombination.

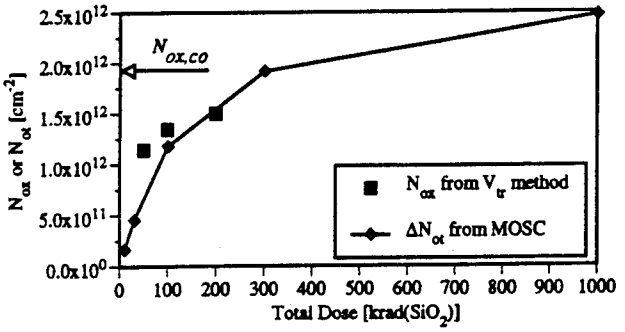


Figure 12. Oxide charge versus total dose for technology B.

To extract V_{tr} and thus estimate N_{ox}, ΔI_B must be plotted versus V_{BE} on a logarithmic scale, as illustrated previously in figure 4. The transition voltage has been obtained graphically in this figure by finding the intersection between a linear extrapolation of the low-current portion of the curve and an $n = 2$ line fit to the high-current range, where n is the diode ideality factor. The transition voltage is indicated on the graph for devices from Technology B. The portion of the curve with $n \neq 2$ is characteristic of surface recombination, while $n = 2$ is characteristic of bulk recombination. Thus, the transition voltage determined graphically from the ΔI_B data is the *same* V_{tr} that appears in equation (7). This fact allows N_{ox} to be estimated as a function of total dose, as shown in figure 12.

Also shown in fig. 12 is a quantity called the crossover charge, $N_{ox,co}$. The crossover charge is defined as the charge at which the transition voltage V_{tr} cannot be determined for any value of V_{BE}. This is also the value of N_{ox} for which the recombination peak is below the surface for all values of V_{BE}. $N_{ox,co}$ is estimated by setting $V_{tr} = 0.2$ V in equation (7), which gives $N_{ox,co} = 1.9 \times 10^{12}$ cm^{-2} for technology B. When N_{ox} exceeds $N_{ox,co}$, the majority of the recombination current occurs beneath the surface, not at the surface. The value of total dose at which N_{ox} first exceeds $N_{ox,co}$ is about 300 krad(SiO_2). Figure 12 also shows N_{ot} vs. total dose for MOS capacitors fabricated

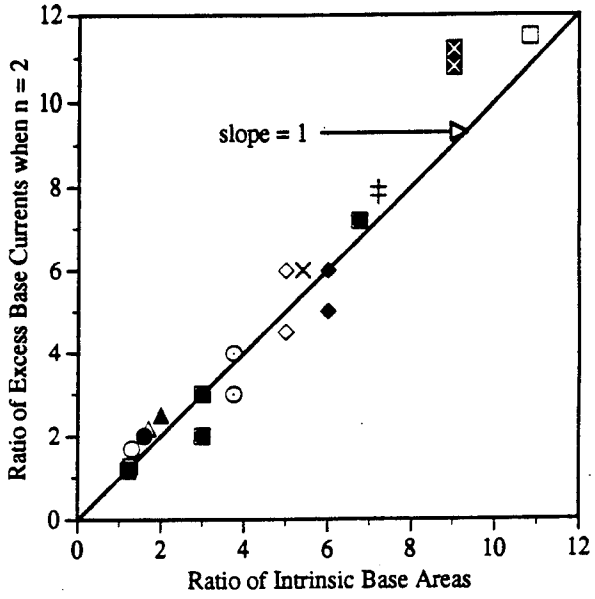


Figure 13. Ratio of excess base currents when n = 2 versus ratio of intrinsic base areas. Devices are taken from technologies A and B.

with the same gate oxide as that over the emitter-base junction of the BJTs. It is seen that N_{ox} is closely related to N_{ot} and that the calculated values of N_{ox} agree well with the measured values of N_{ot}.

Another confirmation that the recombination occurs primarily below the surface of the intrinsic base when the ΔI_B vs V_{BE} curve exhibits $n = 2$ is shown in figure 13. Here, ratios of ΔI_B for different size BJTs from the same process are plotted versus the ratio of their intrinsic base areas. If the recombination is occurring uniformly below the surface of the intrinsic base, then the ratio of ΔI_B between different devices should be the ratio of the area of their intrinsic bases. It is seen that the data fall on a straight line with slope = 1, indicating clearly that the recombination is occurring below the oxide-interface of the intrinsic base when $n = 2$.

B. *Effect of Surface Recombination Velocity*

The dependence of ΔI_B on surface recombination velocity is easily seen in equation (2): v_{surf} merely scales ΔI_B multiplicatively. The surface recombination velocity can be measured directly using a gated diode, but it is more difficult to extract the value directly from a BJT. The reason is that the γ integral must be computed numerically in order to solve for v_{surf}. For BJTs, however, the more relevant parameter is the extrapolated intercept of the plot of $\log(\Delta I_B)$ vs. V_{BE} with the current axis. The intercept current depends on surface recombination velocity and the value of the γ integral. The intercept current has the advantage of being easy to obtain from device characteristics. One merely performs a least-squares exponential curve fit to the $n \neq 2$ portion of the ΔI_B vs. V_{BE} data. Thus, the transition voltage should be indentified before finding the intercept current so that the correct range of data is used for the curve fit.

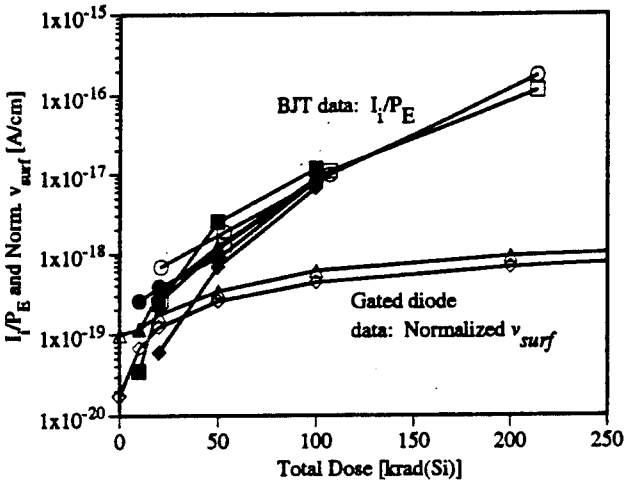


Figure 14. Scaled intercept current and normalized surface recombination velocity versus total dose. Devices are taken from technologies A and B.

When $n \neq 2$, the effect of changes in surface recombination velocity can be estimated by considering the intercept current defined in connection with fig. 4. The intercept current normalized by emitter perimeter is plotted vs. total dose in fig. 14, allowing multiple geometries to be plotted in the same graph. Also plotted are measured values for surface recombination velocity obtained from gated diodes in technology B. The effect of oxide charge is clearly seen in the difference between these quantities. Since excess base current scales with surface recombination velocity, the difference between the curves is a measure of the effect of changes in surface potential due to oxide charge. The intercept current is a more convenient measure of the amount of radiation induced damage than is v_{surf}, since it quantifies changes in the product of surface recombination velocity and the integral involving the surface potential. Thus, to characterize the effects of ionizing radiation on a bipolar technology, the two parameters that should be measured are the transition voltage and the intercept current.

VII. Summary of the Two Approaches

In this paper, two simple approaches for separating the effects of oxide charge and surface recombination velocity in bipolar transistors were described. Both are based on simple analysis of a plot of the log of the excess base current vs. the emitter-base voltage. The contribution of oxide charge is estimated from changes in a voltage that marks the transition from predominantly surface current to bulk current. If gated diodes are available in the technology of interest, surface recombination velocity can be measured directly from the change in the peak diode current. If no gated diode is available, the effect of changing surface recombination velocity can be determined from changes in the intercept of the excess gate current plot with the current axis.

In outline form, the charge separation technique proposed in this paper consists of the following steps:

1. Plot the logarithm of the excess base current versus base emitter voltage.
2. Identify the transistion voltage(s) by finding the intersection of two asymptotes: one for the $n = 2$ portion of the data and one for the $n \neq 2$ portion of the data.
3. Use equation (7) to calculate the value of N_{ox} from the transition voltage determined in step 2.
4. Obtain the intercept current by performing an exponential curve fit to the $n \neq 2$ portion of the data.
5. If a gated diode is available, plot the surface recombination velocity obtained from the gated diodes on the same scale as the intercept current obtained in step 4. The difference between the two curves is an indication of the effect of positive oxide charge.
6. Surface recombination velocity can be calculated directly from the intercept current obtained in step 4 if the γ integral in equation (4) is numerically evaluated for the value of positive oxide charge determined in step 3. This is an extremely laborious approach, since the γ integral requires precise knowledge of the surface potential, which can only be obtained from PISCES simulations of the devices under study.

VIII. Conclusions

Significant progress in understanding the radiation response of MOS technologies has resulted from the ability to understand, and to measure separately, the effects of interface- and oxide trapped charge. The lack of comparable analysis techniques for BJTs has made it difficult to understand some of the features of bipolar radiation response, including superlinear increases in base current with dose and degradation that appears to depend on dose rate.

The role of radiation-induced net positive charge and surface recombination velocity on the excess base current in BJTs was described. A simple method to estimate positive trapped charge vs. total dose using an easily measured transition voltage was presented. The effects of changing surface recombination velocity can be examined by means of an intercept current that is conveniently obtained from a plot of excess base current vs. base-emitter voltage. The insight provided by the charge separation algorithm should pave the way for more radiation-tolerant BJT processes.

ACKNOWLEDGMENTS

This work was supported by Sandia National Labs through their BMDO electronics MODIL program and by DNA and NSWC-Crane through a contract with MRC. The authors wish to thank Peter Winokur of SNL, Dale Platteter of NSWC, and Ken Galloway of UA for useful technical discussions. The experimental assistance of R.A. Reber, Jr. and L.C. Riewe of SNL is gratefully acknowledged.

APPENDIX

In this appendix, the form of the Shockley-Read-Hall (SRH) recombination rate given in equation (1) is derived, with particular attention paid to the assumptions made in the derivation. For simplicity, we assume that the recombination process proceeds through a single trap located in the middle of the forbidden gap; that is, the trap energy E_t equals the intrinsic energy E_i. The recombination rate is maximized for traps located at midgap. We further assume that the capture cross-sections σ_n and σ_p for electrons and holes are equal. The SRH recombination rate at the interface (in $cm^{-2}\ s^{-1}$) is

$$R_s = v_{surf}\,\frac{p_s\,n_s - n_i^2}{p_s + n_s + 2\,n_i} \qquad (1\text{-A})$$

where v_{surf} is the surface recombination velocity, p_s and n_s are the hole and electron concentrations at the surface, and n_i is the intrinsic carrier concentration. The surface recombination velocity is given by $v_{surf} = \sigma\, v_{th}\, N_T$, where σ is the capture cross section, v_{th} is the thermal carrier velocity, and N_T is the trap density.

To simplify (1-A) and apply it to devices, the following assumptions are explicitly made:

1. The recombination rate is not limited by the arrival rate of carriers to the surface. That is, the carriers at the surface are in equilibrium with those in the bulk.
2. Low-level injection conditions apply: $n_s \ll p_s$.
3. n_s is not a function of lateral position, y, far from the emitter base junction. That is, recombination of injected electrons in the bulk is neglected.

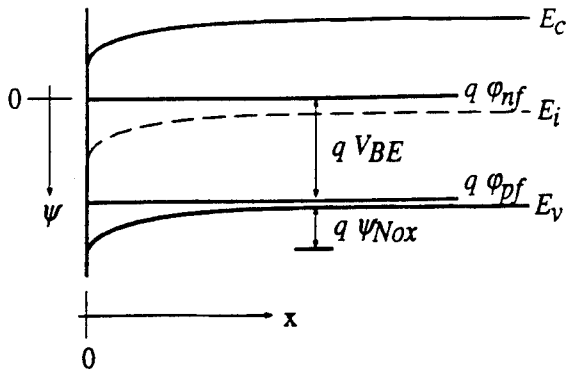


Figure 1-A. Band diagram showing potential references and conventions. The x-axis points from the oxide-silicon interface into the bulk of the intrinsic base.

The electron concentration at the surface is written as

$$n_s = n_i \exp\left[\beta\left(\psi_s - \varphi_{nf}\right)\right] \qquad (2\text{-A})$$

and the hole concentration at the surface is written as

$$p_s = n_i \exp\left[\beta\left(\varphi_{pf} - \psi_s\right)\right] \quad . \qquad (3\text{-A})$$

In these equations, φ_{nf} is the quasi-Fermi level for electrons and φ_{pf} is the quasi-Fermi level for holes. The potential, ψ, is always the intrinsic potential ψ_i. The reference for potential is φ_{nf}, which we define to be zero. The applied voltage appears as a splitting of the quasi-Fermi levels; $V_{BE} = \varphi_{pf} - \varphi_{nf}$. These conventions are illustrated in figure 1-A.

Using these definitions, R_s becomes

$$R_s = \frac{\frac{1}{2}\,n_i\,v_{surf}\left(\exp\left[\beta\,V_{BE}\right] - 1\right)}{1 + \exp\left[\frac{\beta\,V_{BE}}{2}\right]\cosh\left[\beta\left(\psi_s - \varphi_{pf} + \frac{V_{BE}}{2}\right)\right]} \qquad (4\text{-A})$$

Noting that $V_{BE} = \varphi_{pf} - \varphi_{nf} = \varphi_{pf}$, assuming $V_{BE} > 4/\beta$, and noting explicitly the y-dependence of ψ_s, R_s is written as

$$R_s(y) \approx \frac{\frac{1}{2}\,n_i\,v_{surf}\exp\left[\frac{\beta\,V_{BE}}{2}\right]}{\cosh\left[\beta\left(\psi_s(y) - \frac{V_{BE}}{2}\right)\right]} \quad , \qquad (5\text{-A})$$

which is equation (1).

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V.E. Effects of Oxide Charge and Surface Recombination Velocity on the Excess Base Current of BJTs

Effects of Oxide Charge and Surface Recombination Velocity on the Excess Base Current of BJTs

S.L. Kosier†, R.D. Schrimpf†, A. Wei†, M. DeLaus*,
D.M. Fleetwood#, and W.E. Combs††

Abstract

The role of net positive oxide trapped charge and surface recombination velocity on excess base current in BJTs is identified. The effects of the two types of damage can be detected by plotting the excess base current versus base-emitter voltage. Differences and similarities between ionizing-radiation-induced and hot electron-induced degradation are discussed.

I. Introduction

The current gain I_C/I_B of bipolar transistors is degraded when the oxide over the emitter-base junction is damaged. This can occur when the emitter-base junction is reverse-biased [1], as it is in normal BiCMOS circuit operation [2], or when the device is exposed to ionizing radiation [3 - 5]. The damage typically leads to excess base current in the device, ΔI_B, and no change in the collector current. Until now, authors have assumed that ΔI_B is caused primarily by interface states created during the stress [6 - 9]. The effects of net trapped positive charge, N_{ox}, have not been considered. Thus, the effects of N_{ox} on the current gain of the device have not been identified.

In this work, the separate effects of N_{ox} and surface recombination centers on the current gain of BJTs are identified. It is shown that ionizing radiation causes a large increase in net positive oxide charge and a relatively small increase in surface recombination velocity. Hot electron stressing, on the other hand, causes a relatively small increase in net positive oxide charge and a large increase in surface recombination velocity. Since the current gain depends on the product of the two stress-induced defects, both types of stress can lead to qualitatively similar changes in the current gain of the device.

II. Experimental Details

The devices studied in this work are oxide-isolated polysilicon emitter bipolar transistors fabricated in a complementary bipolar process closely related to that described in ref. [10]. A representative cross-section of the devices is shown in figure 1. Relevant structural information is summarized in table 1. The devices were irradiated with 10 keV x-rays at a dose rate of 1.7 krad(Si)/s up to a total dose of 1 Mrad(Si). All pins were grounded during irradiation. For the hot electron stress, a constant reverse current of 6 *mA* through the emitter-base junction for a total of 2048 seconds was used. A Hewlett-Packard 4145B Semiconductor Parameter Analyzer was used for device characterization.

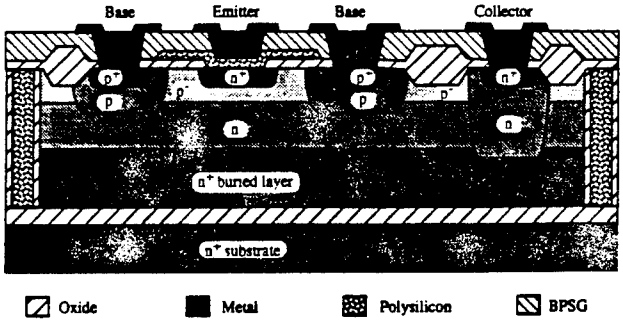


Figure 1. Representative cross-section of the devices studied in this work.

Table 1. Values of relevant device parameters.

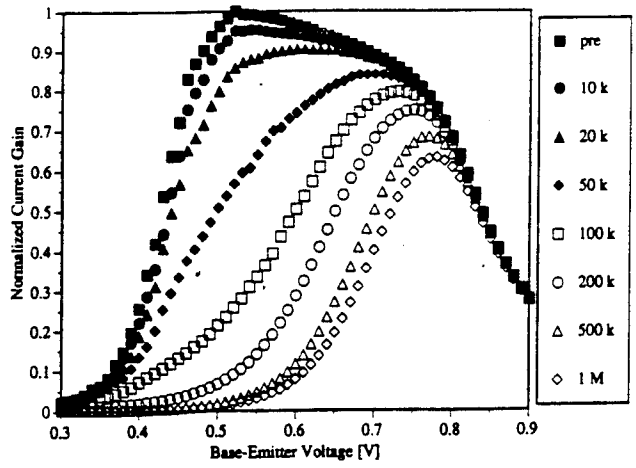
Device Parameter	Value	Units
Emitter-Base Junction Depth	0.3	μm
Intrinsic Base Surface Doping	7.5×10^{17}	cm^{-3}
Oxide Thickness	550	$\AA$
Emitter Size	3 x 3	μm
Nominal Current Gain	200	*A/A*

III. Analysis

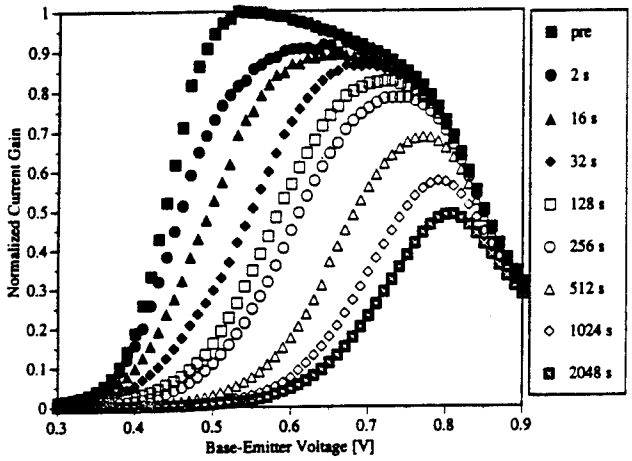
The common-emitter current gain, I_C/I_B, is plotted versus base-emitter voltage, V_{BE}, in figure 2 for increasing values of stress. Figure 2a shows the current gain for increasing values of total ionizing dose, while figure 2b shows the current gain for increasing values of hot electron stress time. The current gain degrades substantially for both types of stress, and the degradation is most severe at lower values of V_{BE}. Note that the current gain degradation tends to saturate for large values of total ionizing dose, but shows no tendency to saturate for large stress times. The trend, however, is qualitatively similar for both types of stress.

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(a)



(b)

Figure 2. Common emitter current gain for increasing stress levels. a) Increasing total ionizing dose (units are rad(Si)). b) Increasing hot electron stress time.

The collector current remains approximately constant throughout both radiation and hot electron stressing. The current gain degrades because the base current increases. The base current is written as $I_B = I_{B,\,pre} + \Delta I_B$, where the excess base current, ΔI_B, is recombination current in the emitter-base depletion region. The recombination current can be obtained analytically from Shockley-Read-Hall (SRH) recombination theory [11, 12]. Assuming equal electron and hole capture cross-sections, a single trap at midgap, and moderate forward bias, ΔI_B can be written as

$$\Delta I_B = \alpha\, v_{surf} \exp\left[\frac{\beta V_{BE}}{2}\right] \gamma(N_{ox}, V_{BE}) \qquad (1)$$

where $\beta = q/kT$ is the inverse thermal voltage, and v_{surf}, α, and γ are given by

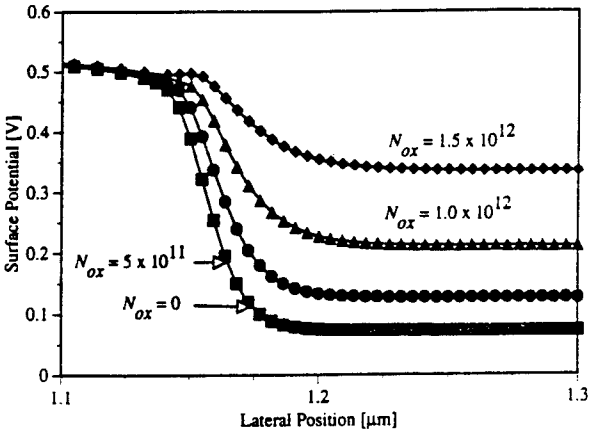
$$v_{surf} = \sigma\, v_{th}\, N_T \qquad (2)$$

$$\alpha = \frac{1}{2} q\, n_i\, P_E \qquad (3)$$

$$\gamma(N_{ox}, V_{BE}) = \int_0^{y_B} \frac{dy}{\cosh[\beta(\psi_s(y) - V_{BE}/2)]} + \frac{2\pi}{P_E} \int_0^{r_B} \frac{r\, dr}{\cosh[\beta(\psi_s(r) - V_{BE}/2)]} \qquad (4)$$

In these expressions, v_{surf} is the surface recombination velocity, N_T is the trap density, σ is the effective capture cross-section, v_{th} is the thermal carrier velocity, q is the electronic charge, n_i is the intrinsic concentration, P_E is the perimeter of the emitter, y is the lateral position variable, $r_B = \sqrt{2}\, y_B$, and ψ_s is the surface potential.

The dependence of ΔI_B on surface recombination velocity is easily seen in equation (2): v_{surf} merely scales ΔI_B multiplicatively. The effect of positive oxide charge is not so easily seen. The positive charge affects ΔI_B by increasing the value of the γ



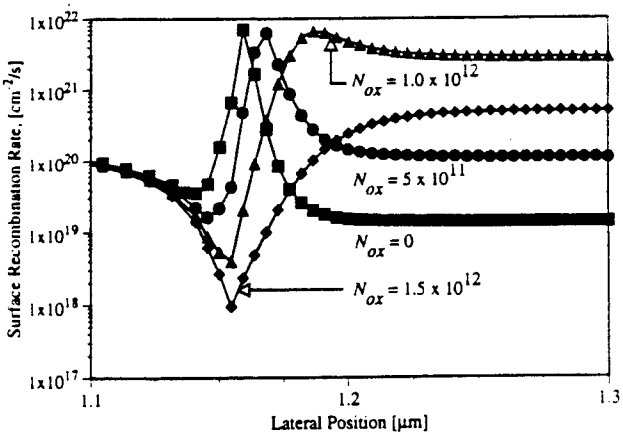


Figure 3. Surface potential (top) and surface recombination rate (bottom) versus lateral position, y, obtained from S-PISCES 2B simulations of the emitter-base junction. The metallurgical junction is at 1.16 μm. After reference [5].

integral. This integral is seldom considered when analyzing recombination current, but it is crucial to take the contribution of this term into account in order to account for the effect of positive oxide charge. Positive charge raises the surface potential ψ_s in the base of the BJT. This increases the surface recombination rate throughout the base. In terms of the γ integral, the integrand becomes a less sharply peaked function as oxide charge increases [5]. These trends are illustrated in figure 3, where PISCES-simulated surface potential and surface recombination rate are plotted versus lateral position for a fixed forward voltage and varying amounts of positive oxide charge.

Recombination current in *PN* junctions varies as $\Delta I_B = \Delta I_{Bo} \exp[\beta V/n]$, where n, the ideality factor, depends upon oxide charge and forward voltage. The shape of the integrand in the γ integral

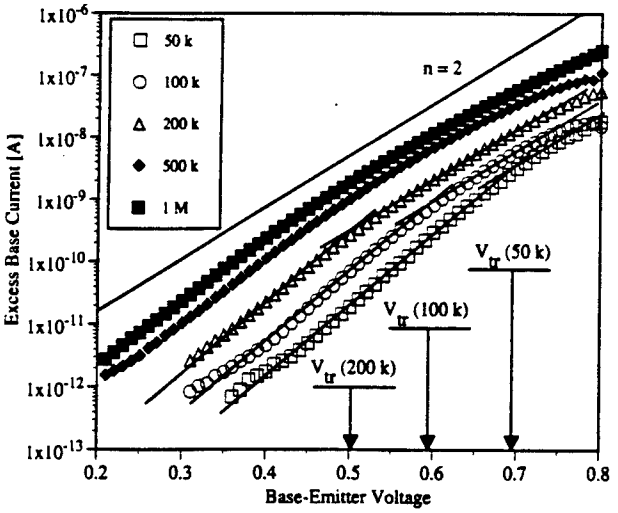


Figure 4. Excess base current versus base-emitter voltage for increasing values of total ionizing dose. The data correspond to those in figure 2a.

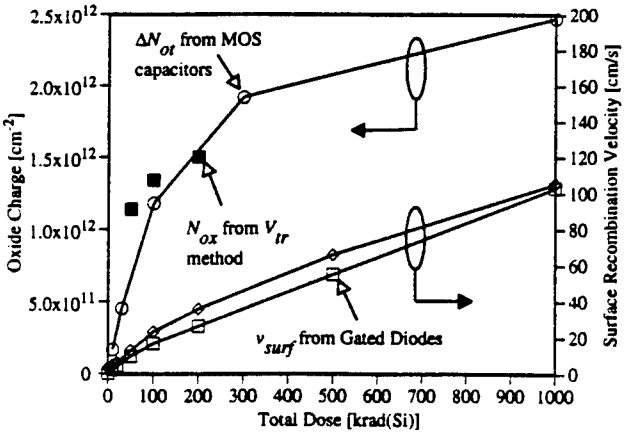


Figure 5. Oxide charge and surface recombination velocity versus total ionizing dose.

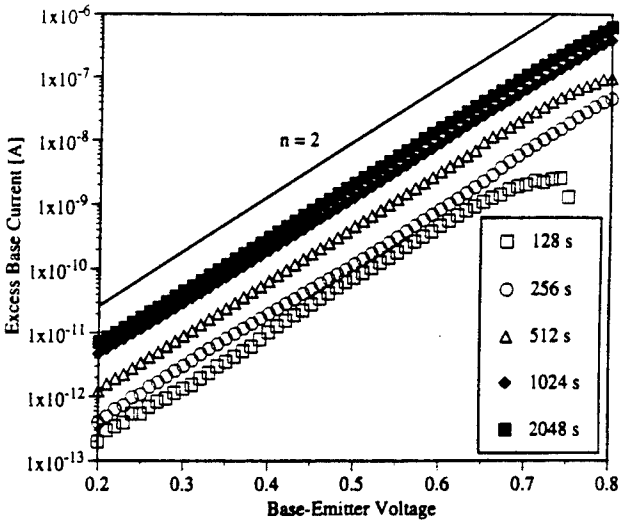


Figure 6. Excess base current versus base-emitter voltage for increasing values of hot electron stress time. The data correspond to those in figure 2b.

is what determines the ideality factor in the diode equation. In [5] it is shown that the value of oxide charge can be determined by plotting the excess base current versus base emitter voltage, as in figure 4. Three transition voltages, V_{tr}, are also identified. The transition voltages mark the transition between predominantly surface and predominantly subsurface recombination. These transition voltages are readily related to oxide charge [5]. In figure 5, oxide charge calculated from the transition voltages is plotted versus total ionizing dose. Oxide-trapped charge, N_{ot}, measured from MOS capacitors and surface recombination velocity measured from gated diodes from the same process is also plotted for comparison. It is seen that ionizing radiation causes a large amount of positive charge and relatively small increases in surface recombination velocity.

In figure 6, ΔI_B is plotted versus V_{BE} for several values of increasing stress time. The ideality factor is roughtly two for all stress times, and no transition voltage can be determined for any

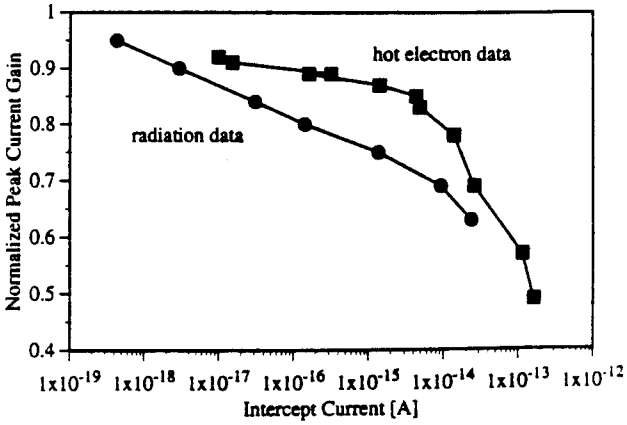


Figure 7. Normalized peak current gain versus intercept current ΔI_{Bo} for radiation and hot electron stress.

stress level. This indicates that the maximum recombination rate is at the surface for all values of forward voltage, and thus that the oxide charge remains small for all stress times. This is the assumption made by several authors, but until now, no direct evidence of this was available.

Additional evidence for the existence of distinctly different defects for each type of stress is shown in figure 7, where the normalized peak current gain is plotted versus ΔI_{Bo}. If the magnitudes of the stress-induced defects were the same for both types of stress, these curves would lie on top of one another. The difference is a result of the large amounts of positive oxide charge induced in the oxide by the radiation stress. The curves merge for large intercept currents because the ideality factors for both types of stress are approximately two.

IV. Summary and Conclusions

For hot electron stressing, the positive oxide charge remains small for all stress levels, indicating that the increase in base current is due primarily to increased surface recombination velocity. For radiation stressing, however, the increase in base current is due to both increased surface recombination velocity and increased positive oxide charge. The two types of stress lead to qualitatively similar changes in current gain because the effects of surface recombination velocity and positive oxide charge are multiplicative.

The separate contributions of net positive charge and surface recombination centers are detected by plotting the excess base current as a function of forward-bias base emitter voltage. By graphically finding the transition from a diode ideality factor of two to an ideality factor less than two, the amount of oxide charge can obtained. The presence of oxide charge can also be detected by plotting the normalized peak current gain against the extrapolated intercept of the excess base current for both types of stress.

Despite the fact the radiation and hot electron stressing produce qualitatively similar changes in current gain, the magnitudes of stress-induced defects for each type of stress differ considerably. These differences must be taken into account when designing stress-tolerant processes and correlating hot electron and radiation stress results.

Acknowledgments

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V.F. Dose-Rate Effects on Radiation-Induced Bipolar Junction Transistor Gain Degradation

Dose-rate effects on radiation-induced bipolar junction transistor gain degradation

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Analysis of radiation damage in modern *NPN* bipolar transistors at various dose rates is performed with a recently introduced charge separation method and PISCES simulations. The charge separation method is verified with measurements on metal-oxide-semiconductor capacitors. Gain degradation is more pronounced at lower dose rates. The charge separation technique reveals that depletion-region spreading and effective recombination velocity are both greater for devices irradiated at lower dose rates. © *1994 American Institute of Physics.*

Exposure to ionizing radiation degrades the current gain of bipolar junction transistors (BJTs) by increasing the base current while leaving the collector current approximately constant.[1-5] Prediction of this gain degradation in low-dose-rate space radiation environments from irradiations done at laboratory dose rates requires the understanding of time-dependent effects. Once time-dependent effects are understood, test methods for estimating total-dose failure in BJTs designed for operation in space radiation environments can be developed. However, time-dependent effects are not understood in BJTs.

In contrast, time-dependent effects in metal-oxide-semiconductor (MOS) transistors have been extensively studied.[6-8] Test standards have been developed which can qualify long-term performance in typical low-dose-rate space radiation environments by testing MOS devices with short exposures to high-dose-rate radiation, combined with annealing at elevated temperatures.[9-12] The development of these test standards resulted from the application of MOS charge separation techniques[13-15] to time-dependent effects.

In this work, we present the first detailed analysis of dose-rate effects on BJT gain degradation using charge separation techniques.[16] In MOS technologies, charge separation techniques can quantify the damage mechanisms ΔN_{OT} (fixed positive charge at the interface) and ΔN_{IT} (interface-trap density) and their corresponding threshold voltage shifts ΔV_{OT} and ΔV_{IT}. In BJTs, gain degradation is due to the excess base current (ΔI_B, where $I_B = I_{B,pre} + \Delta I_B$). The individual mechanisms which contribute to the excess base current are changes in the effective surface recombination velocity, $v_{s,eff}$, and the spreading of the depletion layer caused by the buildup of net positive charge in the oxide, N_{ox} (not necessarily the same as N_{OT}). The bipolar junction transistor charge separation method[16] is used to calculate N_{ox} at the dose rates studied. Accurate PISCES simulations are used to identify the dose-rate effect on $v_{s,eff}$.

The response of the excess base current to irradiations at various dose rates can be traced back to the combined dose-rate dependences of the individual manifestations of radiation-induced damage, N_{ox} and $v_{s,eff}$. The physical mechanisms leading to the dose-rate effect on the buildup of N_{ox} and on the changes in $v_{s,eff}$ are beyond the scope of this letter, but they appear to be related to a difference in charge distributions following high- and low-dose-rate irradiations. PISCES simulations were performed to separate the effects of the individual damage mechanisms and to quantify their relationships to the excess base current. Analysis shows that excess base current, oxide charge, and effective surface recombination velocity are highest at lower dose rates [<10 rad(SiO_2)/s] and decrease with increasing dose rate until they become independent of dose rate at higher dose rates [>100 rad(SiO_2)/s]. Indeed, these results confirm that the dose-rate response of BJTs is very different than the dose-rate response of MOSFETs,[17] where oxide charge tends to be reduced at low dose rates due to trapped-hole neutralization and/or interface-trap buildup.[7]

The BJTs studied in this work were NPN oxide-isolated polysilicon emitter bipolar junction transistors fabricated in a complementary bipolar process.[18] A representative cross section is shown in Fig. 1. Four dose rates were used, with four device geometries irradiated at each dose rate. The irradiations were performed in a Co-60 source at dose rates of 3, 30, 100, and 247 rad(SiO_2)/s up to a total dose of 1000 krad(SiO_2). All terminals were grounded during irradiation.

In addition, MOS capacitors from a closely related BiCMOS process were irradiated with all terminals grounded at dose rates of 1.3, 5, 50, 500, and 1000 rad(SiO_2)/s with 10 keV x rays up to a total dose of 300 krad(SiO_2). The positive oxide charge buildup in the MOS capacitors was determined by measuring shifts in the midgap voltage.[14]

Excess base current at a base-emitter voltage (V_{BE}) of 0.6 V is plotted against dose rate at total doses of 20, 50, and 100 krad(SiO_2) in Fig. 2. The excess base current is largest at low dose rates, with a tendency to become independent of dose rate at high-dose rates.

The excess base current due to surface recombination can be written as[16]

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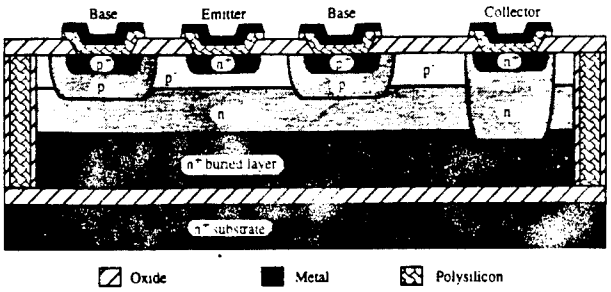


FIG. 1. Representative cross section of the devices studied in this work.

$$\Delta I_B = \alpha \nu_{s,\mathrm{eff}}(N_T, N_{\mathrm{ox}}, V_{\mathrm{BE}})\,\gamma(N_{\mathrm{ox}}, V_{\mathrm{BE}})\exp[\beta V_{\mathrm{BE}}/2],$$
$$\alpha = q n_i P_E/2, \qquad (1)$$

where q is the electronic charge, n_i the intrinsic carrier concentration, and P_E the emitter perimeter. The effective surface recombination velocity $\nu_{s,\mathrm{eff}}$ has units of velocity and accounts for the contribution of surface recombination velocity (defined as $\nu_s = \sigma \nu_{\mathrm{th}} N_T$, where σ is the capture cross section, ν_{th} the thermal carrier velocity, and N_T the interface-trap density evaluated at midgap). However, $\nu_{s,\mathrm{eff}}$ is not equal to ν_s because it also depends on N_{ox} and V_{BE} for reasons cited in previous work.[19–21] It is important to note that because $\nu_{s,\mathrm{eff}}$ is dependent on N_{ox}, the dose-rate dependence of N_{ox} will affect $\nu_{s,\mathrm{eff}}$. $\gamma(N_{\mathrm{ox}}, V_{\mathrm{BE}})$ is an integral over the intrinsic base which accounts for the spreading of the depletion layer and β is the inverse thermal voltage (q/kT). To understand the dose-rate effect on the excess base current, the dose-rate dependence of the individual manifestations of radiation damage, N_{ox} and $\nu_{s,\mathrm{eff}}$, must be examined.

The dose-rate dependence of N_{ox} can be directly determined from the charge separation method.[16] Oxide charge is plotted against dose rate in Fig. 3 at a total doses of 20, 50, and 100 krad(SiO_2). As with the excess base current, oxide charge is largest at low dose rates, with a tendency to become independent of dose rate at high dose rates. Measurements made on the MOS capacitors at a total dose of 300 krad(SiO_2) are also plotted in Fig. 3. The capacitors show approximately the same dose-rate trend in oxide charge buildup as the BJTs.

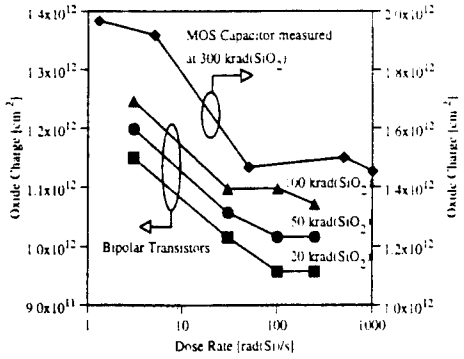


FIG. 3. Oxide charge vs dose rate at various total doses.

From Eq. (1), $\nu_{s,\mathrm{eff}}$ can be calculated as the ratio of excess base currents from experiment (which are due to increases in both $\nu_{s,\mathrm{eff}}$ and N_{ox}[5]) to excess base current due solely to increases in N_{ox}. The excess base current due solely to increases in N_{ox} is simulated in PISCES by fixing the recombination rate at the surface to a constant equal to that of the bulk; by not enhancing recombination at the surface, the simulations effectively fixes $\nu_{s,\mathrm{eff}}$ to a constant [the lowest possible value by the definition of $\nu_{s,\mathrm{eff}}$ in Eq. (1)].[19,22] To calculate $\nu_{s,\mathrm{eff}}$ from the experimental data, however, it is imperative that the device simulations be very accurate. The PISCES simulations in this work used process-simulation-generated doping profiles from a SUPREM simulation of the BJT fabrication process. Simulations were fine tuned to match the devices by matching simulated current gain to measured current gain.[23] Two-dimensional simulations provide current per unit length, so the simulation currents were multiplied by the appropriate length to account for the contributions of the lightly doped extrinsic base area.[22]

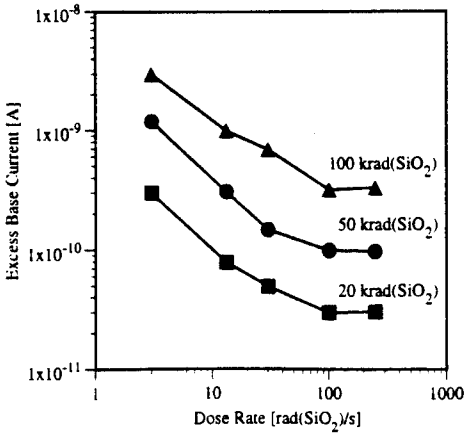


FIG. 2. Excess base current at V_{BE}=0.6 V vs dose rate.

Figure 4 shows the PISCES-simulated excess base current due solely to increases in oxide charge against oxide charge. Measured excess base currents at different dose rates are also shown in Fig. 4 against oxide charge (the measured excess base currents are known experimentally versus total dose; an approximate mapping of increasing total dose to oxide charge buildup is performed by using the charge separation method to observe trends in the experimental data set). The dose-rate effect on $\nu_{s,\mathrm{eff}}$ is evidenced by the differences in the excess base current at different dose rates in Fig. 4. Two important points arise from this figure. First, the PISCES-simulated current due solely to increased oxide charge matches the measured current at high values of oxide charge and total dose. The same effect is consistently observed in measured data irrespective of dose rate or device geometry. The high values of oxide charge force the recombination peak below the surface, eliminating surface contributions to the excess base current.[16] Additional PISCES simulation

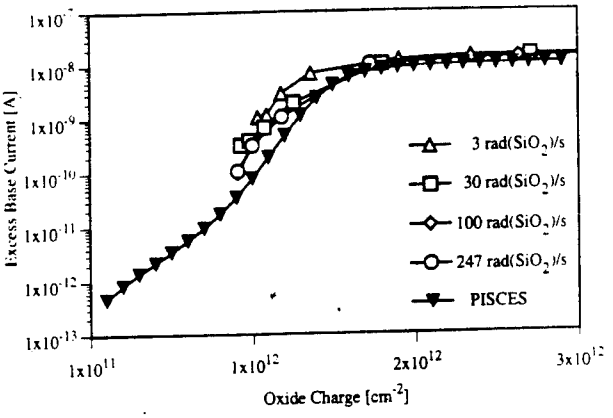


FIG. 4. Measured and PISCES-simulated excess base current at V_{BE}=0.6 V vs oxide charge.

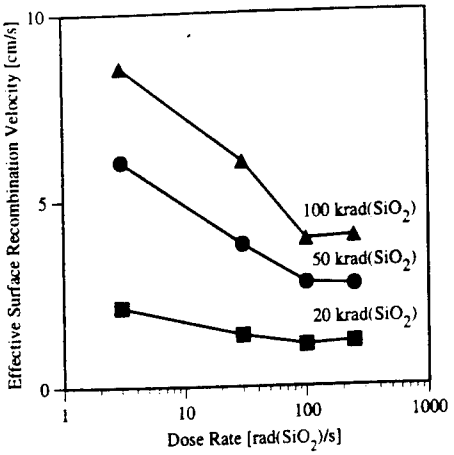


FIG. 5. Effective surface recombination velocity $\nu_{s,\text{eff}}$ calculated at V_{BE}=0.6 V vs dose rate.

shows no change of excess base current with increasing surface recombination velocity when large densities of oxide charge are present over the extrinsic base. Second, the measured excess base currents do not significantly differ from the PISCES-simulated excess base current due solely to N_{ox}. This demonstrates that the dose-rate dependence of the excess base current can be largely attributed to N_{ox}. This point is especially true in light of the aforementioned dependence of $\nu_{s,\text{eff}}$ on N_{ox}.

Figure 5 shows $\nu_{s,\text{eff}}$ calculated (by taking the ratio of measured excess base current to simulated excess base current due solely to N_{ox}) at V_{BE}=0.6 V plotted against dose rate. At these total doses, N_{ox} does not significantly decrease surface contributions to the excess base current. The dose-rate trend is similar to the trend of excess base current and oxide charge. $\nu_{s,\text{eff}}$ is largest at low dose rates, with a tendency to become independent of dose rate at high dose rates.

BJTs were irradiated at several dose rates to identify the dose-rate dependence of gain degradation. This work presents the first analysis of dose-rate effects on the individual mechanisms (increases in net positive oxide charge and changes in effective surface recombination velocity) responsible for BJT gain degradation. Both oxide charge and effective surface recombination velocity are highest at lower dose rates, with a tendency to become independent of dose rate at higher dose rates. The oxide charge dose-rate dependence in BJTs was observed by two independent methods: a charge separation technique and measurements made on MOS capacitors from a BiCMOS process. By comparing measured excess base currents (due to oxide charge and effective surface recombination velocity) to excess base currents (due to oxide charge and effective surface recombination velocity) to excess base current due only to oxide charge, it was found that excess base current due only to oxide charge accounts for most of the excess base current. This is due to the decrease of effective surface recombination velocity with increasing oxide charge. Thus the dose-rate effect on gain degradation in modern BJTs is in large part determined by the dose-rate response of charge buildup in the oxide over the lightly doped extrinsic base of BJTs.

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V.G. Excess Collector Current Due to an Oxide-Trapped-Charge-Induced Emitter in Irradiated NPN BJTs

Excess Collector Current Due to an Oxide-Trapped-Charge-Induced Emitter in Irradiated *NPN* BJT's

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Abstract—**Excess collector current in irradiated *NPN* BJT's is linked to an oxide-trapped-charge-induced inversion layer acting as an additional emitter. Excess collector current is modeled by interpreting the inversion layer as an extension of the emitter.**

I. Introduction

THE current gain (I_C/I_B) of BJT's is degraded upon exposure to ionizing radiation. The degradation is due to a buildup of net positive oxide-trapped charge (N_{ox}) and increases in surface recombination velocity [1]–[5]. Previous analyses of the physical mechanisms responsible for gain degradation have usually focused on the excess base current (ΔI_B, where $I_B = I_{B,\text{pre-rad}} + \Delta I_B$). Excess collector current (ΔI_C, where $I_C = I_{C0} + \Delta I_C$) is often explicitly assumed to be negligible, although this assumption has not been critically examined. The increase in excess collector current due to ionizing radiation has been observed by Nowlin, *et al.* [6]; however, the physical mechanisms responsible were not investigated.

The effect of assuming negligible excess collector current is demonstrated in Fig. 1. This figure shows the measured common-emitter current gain, normalized to the peak pre-irradiated value, plotted versus the collector current for a pre-irradiated device and for the same device at a total dose of 1 Mrad (SiO_2). The pre-irradiated current gain varies with operating point and degrades significantly with increasing total dose of radiation. The two curves shown at a total dose of 1 Mrad(SiO_2) demonstrate what the current gain looks like as a function of collector current when the excess collector current is accounted for and when assuming negligible excess collector current ($\Delta I_C = 0$, current gain = $I_{C,\text{pre}}/I_{B,1\text{Mrad}}$). Assuming negligible excess collector current clearly underestimates the current gain. Thus, a simple method to account for the excess collector current is necessary.

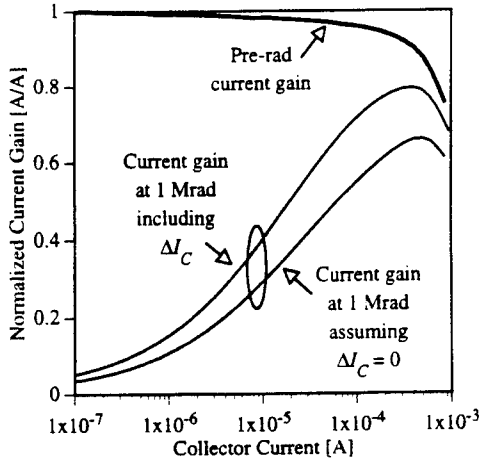


Fig. 1. Measured XFCB common-emitter current gain, normalized to the peak pre-irradiated value, versus the collector current. Shown are the pre-irradiated current gain plotted against the pre-irradiated collector current, current gain at a total dose of 1 Mrad(SiO_2) plotted against the actual measured collector current at 1 Mrad(SiO_2) (this accounts for the excess collector current), and current gain at a total dose of 1 Mrad(SiO_2) (assuming negligible excess collector current, i.e. current gain = $I_{C,\text{pre}}/I_{B,1\text{Mrad}}$) plotted against the pre-irradiated collector current.

Recent BJT charge separation work has shown that the N_{ox} densities necessary to invert the extrinsic base are significantly exceeded for typical device operating conditions [4] and [5]. The formation of this inversion layer is key to many of the characteristics of excess collector current because this inversion layer is ohmically connected to the diffused emitter and therefore acts as an extra emitter in the BJT. At higher total doses of radiation, this N_{ox}-induced emitter can be responsible for excess collector current magnitudes on the order of the collector current itself (the actual value is highly dependent on device geometry).

This work presents a detailed analysis of excess collector currents in irradiated BJT's. Simple equations for predicting the experimentally-observed increases in the collector current are derived. PISCES simulations are used to confirm the analysis.

II. Experiment and Simulation

Two BJT technologies were studied in this work. A representative cross-section of the devices is shown in Fig. 2

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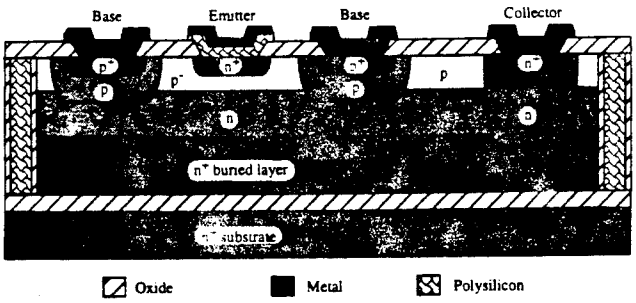
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	XFCB	RBCMOS
Emitter-Base Junction Depth	0.23 μm	0.25 μm
Oxide Thickness	5450 $\AA$	550 $\AA$
Emitter Size	1.5x1.5 μm	1.5x1.5 μm
Extrinsic Base Length	1.5 μm	1.0 μm
Extrinsic Base Surface Doping	9.0×10^{17} cm^{-3}	7.8×10^{17} cm^{-3}
GN_{IN}/GN_{EX}	0.25	0.13

Fig. 2. Representative cross-section and relevant parameters of the devices studied in this work.

along with a table of relevant device parameters. XFCB devices are oxide-isolated polysilicon emitter bipolar transistors fabricated in a complementary bipolar process described in [7]. RBCMOS devices are oxide-isolated polysilicon emitter BJT's fabricated in a BiCMOS process. A typical top view of both devices and definitions for the intrinsic base and the extrinsic base are shown in Fig. 3. Irradiation was performed in a Co-60 source with all pins grounded. I-V characteristics were measured *in-situ* immediately upon reaching the total doses at which measurements were taken.

The two technologies studied were simulated in PISCES using SUPREM-generated doping profiles. Two-dimensional simulations provide current per unit length, so the simulation currents were multiplied by the appropriate length to account for the contributions of the extrinsic base [8]–[10] (the devices studied in this work have square emitters so the two-dimensional simulation currents were multiplied by the perimeter of the emitter to obtain realistic three-dimensional currents). Radiation damage was approximated in the simulations with uniformly-distributed positive charge at the oxide-silicon interface. Charge densities used in the simulations were obtained from application of a charge separation technique to the technologies studied in this work [5], [10].

III. Analysis and Results

A. Temperature Effects

Variations in temperature with total dose of up to +3°C were observed in the measured I-V characteristics. Due to the combined cubic and exponential dependencies of the collector current on temperature, such small changes can have a large effect on the magnitude of the excess collector current.

The effect of temperature on the excess collector current magnitude was accounted for by assuming that

$$I_C \alpha T^3 e^{-\left(\frac{E_G - qV_{BE}}{kT}\right)}, \quad (1)$$

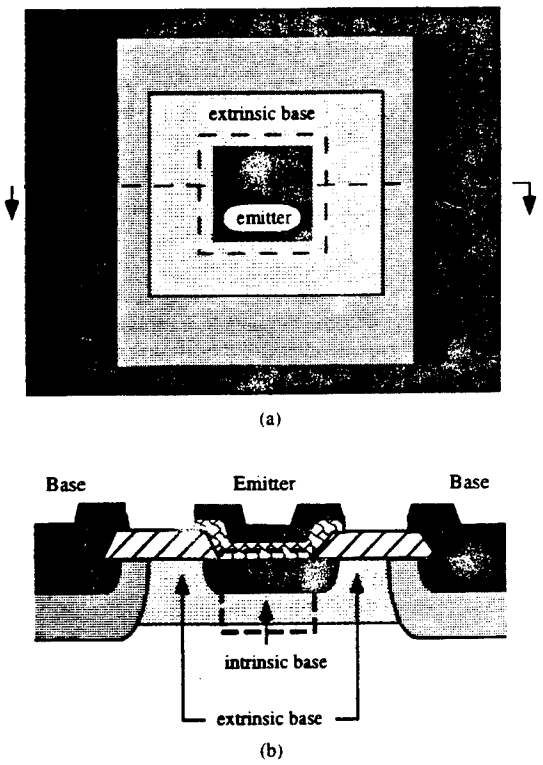


Fig. 3. (a) Top view of the devices studied and (b) definition of the intrinsic base and the extrinsic base.

where T is the temperature in K, E_G is the silicon energy band gap (the temperature dependence was assumed to be negligible for the small range of temperatures observed), q is the electronic charge, V_{BE} is the base-emitter voltage, and k is Boltzmann's constant. The excess collector current at each total dose was calculated by subtracting a pre-irradiation collector current, calculated at the measurement temperature, from the measured collector current. The excess collector currents at the measurement temperatures were then recalculated at $T = 300$ K. All PISCES simulations were also done with $T = 300$ K.

B. Physical Mechanism and Modeling

Fig. 4 shows experimental excess collector current plotted against base-emitter voltage. The exponential dependence of the excess collector current on V_{BE} (with an ideality factor, $n = 1$) indicates that ΔI_C is indeed a current due to injection of carriers over a potential barrier rather than a leakage current. Fig. 5 shows experimentally-measured excess collector currents plotted against increasing total dose at $V_{BE} = 0.6$ V. Fig. 5 also shows simulated excess collector current plotted against increasing N_{ox} at $V_{BE} = 0.6$ V. The trends demonstrated by the simulated excess collector currents concur with experiment (note that the linear scale for N_{ox} concurs with the log scale for total dose; a near-logarithmic relationship between oxide charge and total dose has been demonstrated experimentally in [4], [5] and is discussed in greater detail in [11]) and can be explained as follows [12]:

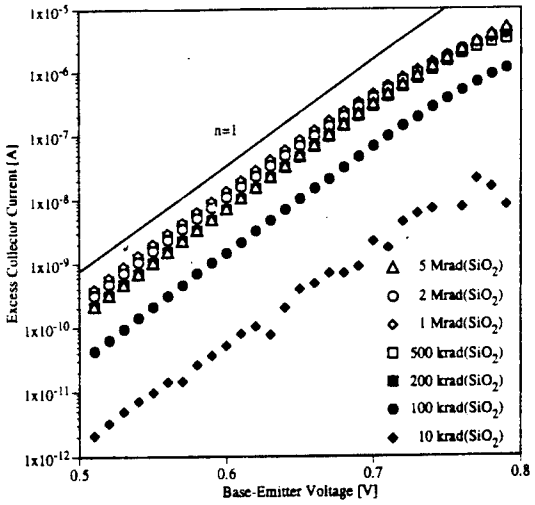


Fig. 4. XFCB experimental excess collector current versus V_{BE} at various total doses.

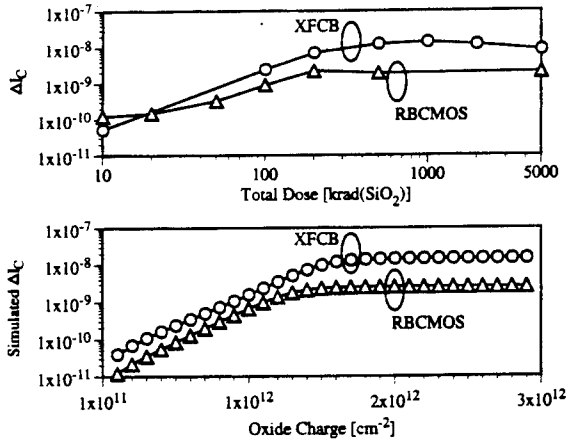


Fig. 5. Experimental excess collector current versus total dose at V_{BE} = 0.6 V and simulated excess collector current versus oxide charge at V_{BE} = 0.6 V for both technologies studied.

Upon irradiation, N_{ox} builds up in the oxide over the p-type extrinsic base. When sufficiently large positive oxide charge densities build up over the extrinsic base, an n-type inversion layer will be formed at the surface. The formation of the inversion layer with increasing oxide charge is shown by simulation in Fig. 6. The figure shows simulated electron concentration at V_{BE} = 0.6 V increasing with N_{ox} at the extrinsic base surface until, at high enough N_{ox}, it approaches the electron concentration at the edge of the diffused emitter. The inversion layer is ohmically connected to the diffused emitter region so this is equivalent to extending the emitter area. Forward biasing the emitter-base junction under this condition results in injection of electrons into the base not only from the diffused emitter, but also from the inversion layer. This is demonstrated in Fig. 7 which plots simulated total current density normal to a cutline near the collector at V_{BE} = 0.6 V. This excess collector current saturates (becomes independent of total dose) when the surface is heavily inverted so that the ohmic voltage drop along the

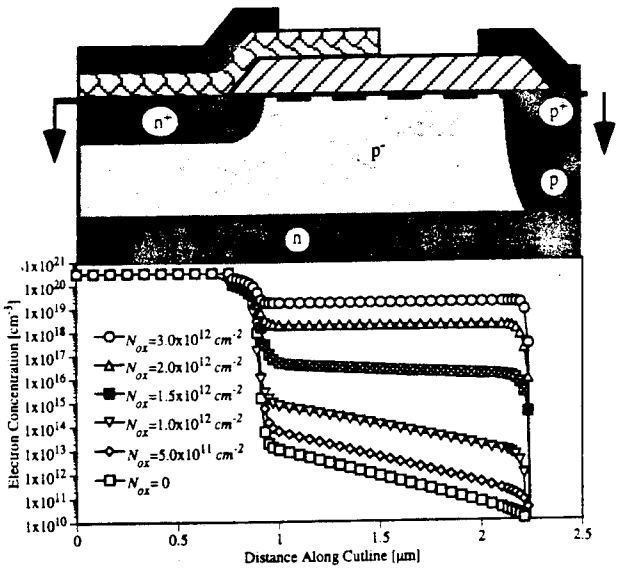


Fig. 6. PISCES simulated electron concentration along the oxide-silicon interface at V_{BE} = 0.6 V versus increasing oxide charge for an XFCB device.

inversion layer is negligible. At this point the efficiency of the N_{ox}-induced emitter approaches the emitter efficiency of the diffused emitter. This is shown in Fig. 7 where at high values of N_{ox}, the current density saturates and the ratio of the current densities across the intrinsic base (J_{IN}) and across the extrinsic base (J_{EX}), on average, is

$$J_{IN}\,GN_{IN} = J_{EX}\,GN_{EX}, \tag{2}$$

where GN_{IN} and GN_{EX} are the Gummel numbers which account for the nonuniform doping of the intrinsic base and extrinsic base, respectively. The validity of the above expression is strengthened by the simulations. They show virtually identical potential barriers between the inversion layer and extrinsic base and between the diffused emitter and intrinsic base when the excess collector current saturates.

The emitter action of the N_{ox}-induced inversion layer demonstrated by Fig. 7 allows the excess collector current to be expressed as

$$\Delta I_C = A_{EX} J_{EX}, \tag{3}$$

where A_{EX} is the area of the extrinsic base. This relationship between the excess collector current and the N_{ox}-induced inversion layer can be interpreted in terms of increases in the effective emitter area ($A_{E,eff}$). $A_{E,eff}$ is defined as

$$I_C = \frac{qn_i^2 A_{E,eff} e^{\beta V_{BE}}}{GN_{IN}}. \tag{4}$$

$I_C = I_{C0} + \Delta I_C$ (I_{C0} is the collector current from the intrinsic base under the emitter and ΔI_C is the excess collector current due to electrons injected from the N_{ox}-induced inversion layer across the extrinsic base) is the total collector current, n_i is the intrinsic carrier concentration, and β is the inverse thermal voltage.

The contribution of the N_{ox}-induced emitter to the effective emitter area is demonstrated in Fig. 8. The figure plots

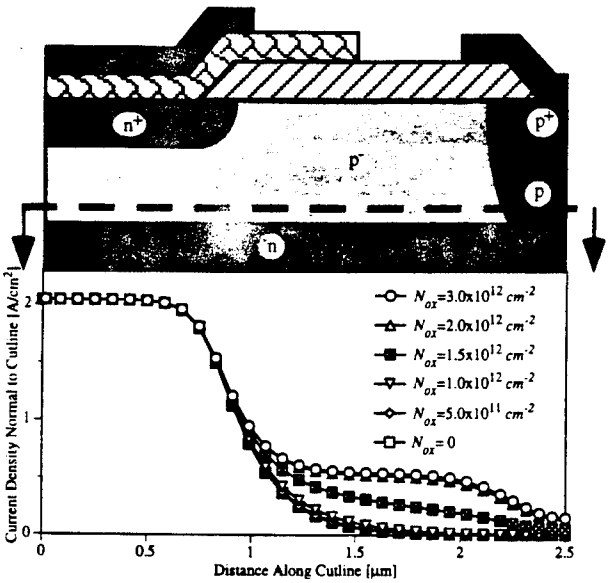


Fig. 7. PISCES simulated total current density normal to cutline at V_{BE} = 0.6 V versus increasing oxide charge for an XFCB device.

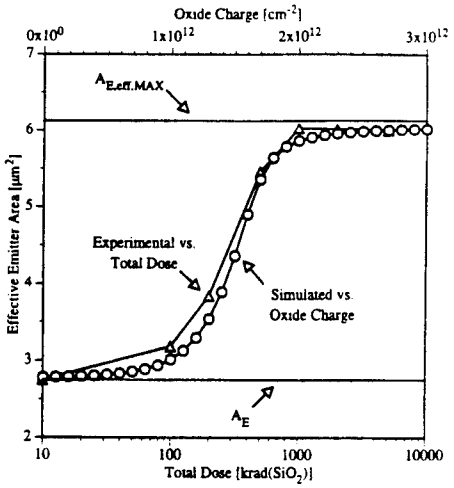


Fig. 8. Experimental effective emitter area at V_{BE} = 0.6 versus total dose and simulated effective emitter area at V_{BE} = 0.6 V versus oxide charge for an XFCB device.

experimental effective emitter area at V_{BE} = 0.6 V calculated from (4) against total dose as well as simulated effective emitter area at V_{BE} = 0.6 V against N_{ox}. The lower bound on $A_{E,eff}$ is simply the effective emitter area of the diffused emitter at V_{BE} = 0.6 V (which we call A_E). The upper bound ($A_{E,eff,MAX}$) is represented by

$$A_{E,\mathrm{eff,MAX}} = A_E + \frac{GN_{IN}}{GN_{EX}} A_{EX}. \tag{5}$$

with an A_{EX} estimated from the PISCES simulation results in Fig. 7. And, as demonstrated by the two-dimensional simulation in Fig. 7, A_E and A_{EX} are difficult to calculate due to three-dimensional current flow. The problem is bounded, however, because A_E is never smaller than the emitter diffusion mask area and A_{EX} is never larger than the difference between the extrinsic base diffusion mask and emitter diffusion mask areas.

C. Technology Differences

Based on the above explanation, the differences between the excess collector currents of the two technologies in Fig. 5 become apparent. The XFCB excess collector current saturates at a higher value because of a larger extrinsic base area and a larger ratio of Gummel numbers. The RBCMOS excess collector current saturates at a lower total dose because the extrinsic base surface doping is lower. Hence, the RBCMOS extrinsic base inversion layer requires smaller densities of oxide charge to approach the emitter efficiency of the diffused emitter.

IV. Summary

The physical mechanism for excess collector current in irradiated *NPN* BJT's was identified. A simple analysis based on collector current equations showed the effect of radiation on the effective emitter area. The excess collector current increases with increasing total dose. It saturates at magnitudes bounded by simple analysis based on the dependence of excess collector current on device geometry.

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R. D. Schrimpf, for photograph and biography, see p. 443 of the March 1995 issue of this TRANSACTIONS.

W. E. Combs, (M'78) for photograph and biography, see p. 444 of the March 1995 issue of this TRANSACTIONS.

M. DeLaus, for photograph and biography, see p. 443 of the March 1995 issue of this TRANSACTIONS.

V.H. Bounding the Total-Dose Response of Modern Bipolar Transistors

Bounding the Total-Dose Response of Modern Bipolar Transistors††

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Abstract

The excess base current in an irradiated BJT increases superlinearly with total dose at low-total-dose levels. In this regime, the excess base current depends on the particular charge-trapping properties of the oxide that covers the emitter-base junction. The device response is dose-rate-, irradiation-bias-, and technology-dependent in this regime. However, once a critical amount of charge has accumulated in the oxide, the excess base current saturates at a value that is independent of how the charge accumulated. This saturated excess base current depends on the device layout, bulk lifetime in the base region, and the measurement bias. In addition to providing important insight into the physics of bipolar-transistor total-dose response, these results have significant circuit-level implications. For example, in some circuits, the transistor gain that corresponds to the saturated excess base current is sufficient to allow reliable circuit operation. For cases in which the saturated value of current gain is acceptable, and where other circuit elements permit such over-testing, this can greatly simplify hardness assurance for space applications.

I. INTRODUCTION

Bipolar and BiCMOS technologies have important applications in space systems, particularly in linear and mixed-signal integrated circuits. The degradation of the current gain in modern integrated bipolar transistors due to ionizing radiation has received significant attention, with much of the effort focused on understanding the device response at low dose rates [1 – 6]. Predicting the response of these devices in low-dose-rate space environments is currently not possible with laboratory dose-rate irradiations and anneals [3]. Testing techniques for predicting the low-dose-rate response of MOS devices are not applicable to bipolar devices [3] due to the fundamentally different physics that determine bipolar device gain degradation [1]. Indeed, high temperature annealing following irradiation improves the characteristics of bipolar devices [3], in contrast to the enhanced degradation due to interface-trap effects observed for MOS devices, which may exhibit threshold-voltage rebound [7].

The increase in base current of modern bipolar devices at low total doses is dose-rate dependent [3, 6, 8], with lower dose rates causing more device degradation than higher dose rates. Testing devices at extremely low dose rates is unattractive, however, due to the large amount of time required to obtain reasonable total doses. On the other hand, if the worst-case increase in base current can be ascertained from laboratory irradiations, it may be possible to rapidly qualify parts for applications where the worst-case current gain is sufficient for reliable circuit operation.

In this paper we demonstrate that the maximum degradation that may occur due to excess base current in typical modern bipolar device geometries is independent of dose rate and bias during irradiation. Excess base current is the base current that is a result of the radiation-induced damge; mathematically, the total base current, I_B, is written as $I_B = I_{B,pre\text{-}rad} + \Delta I_B$. Physically, the saturation of excess base current occurs because once a critical amount of charge has accumulated in the screen oxide over the base region, the excess base current becomes relatively insensitive to surface conditions. Thus, although it may take different amounts of total ionizing dose to reach the necessary amount of oxide charge to cause the worst-case increase in base current, the maximum current that can flow once this condition is met is *independent* of dose rate

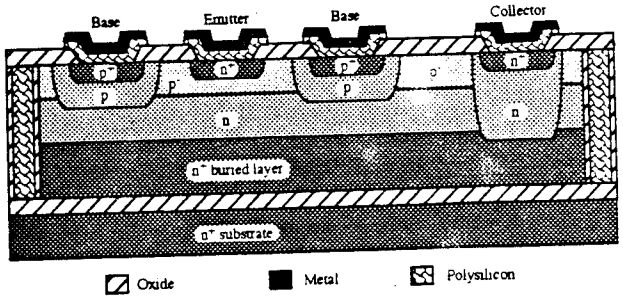


Figure 1. Representative cross-section of BJTs from technology A.

††This work was supported by the Defense Nuclear Agency, Sandia National Laboratories, and Naval Surface Warfare Center-Crane.

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Table 1. Relevant Device Parameters

Quantity	Technology A	Technology B	Technology C
Emitter Type	polysilicon	polysilicon	silicon
Emitter Size	1.5 x 1.5 μm	1.5 x 1.5 μm	1.5 x 1.5 μm
Ext. Base Surf. Doping	9×10^{17} cm^{-3}	7.8×10^{17} cm^{-3}	1×10^{18} cm^{-3}
Active Base Width	0.4 μm	1 μm	0.8 μm
Int. Base Length	1.5 μm	1 μm	1.5 μm
Oxide Thickness	545 nm	55 nm	545 nm
Nominal Current Gain	70 A/A	200 A/A	40 A/A

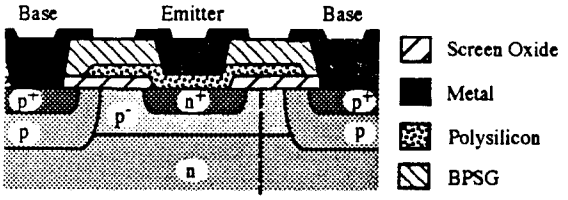


Figure 2. Schematic cross-section of the emitter-base region of technology B. The dashed line perpendicular to the oxide-silicon interface is germane to figures 6 and 7.

and bias during irradiation. Based on these observations, implications for hardness assurance testing of modern bipolar devices are discussed.

II. EXPERIMENTAL DETAILS

A representative cross-section of devices from technology A is shown in figure 1. These devices are single-poly polysilicon emitter NPN bipolar transistors from a complementary bipolar process described in [9]. Technology B is a related BiCMOS process, and technology C is a standard emitter process that is very similar to technology A, except that it uses a metal-contacted implanted emitter. All relevant device parameters are summarized in table 1. The devices were irradiated in a Pb/Al box with a Co-60 source at various dose rates with all pins grounded, except where other biases are noted.

In figure 2, a schematic cross-section of the emitter-base region from technology B is shown. In this technology, which is typical of all commercial single-poly BJTs of which we are aware, the oxide overlying the emitter-base junction serves as a screen oxide for the base implant. The oxide is not stripped after this step. Next, the emitter polysilicon is deposited and used as the diffusion source for the crystalline-silicon emitter region. This high temperature step, plus the damage done by the implant, combine to produce a poor quality oxide. The charge trapping properties of this oxide differ significantly from gate-quality oxides [10]. For this paper, it is sufficient to note that extremely large amounts of positive charge may be

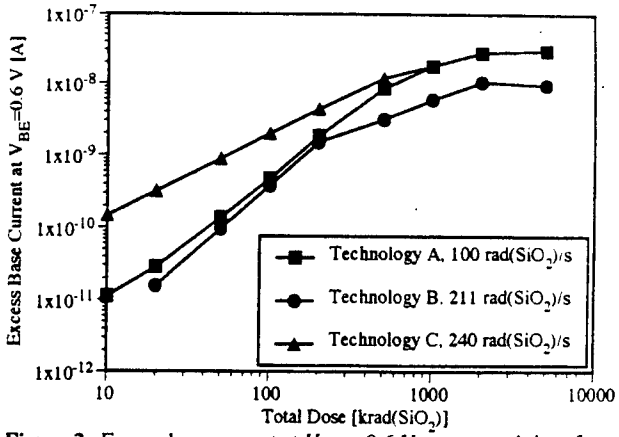


Figure 3. Excess base current at $V_{BE} = 0.6$ *V* versus total dose for the three technologies listed in table 1.

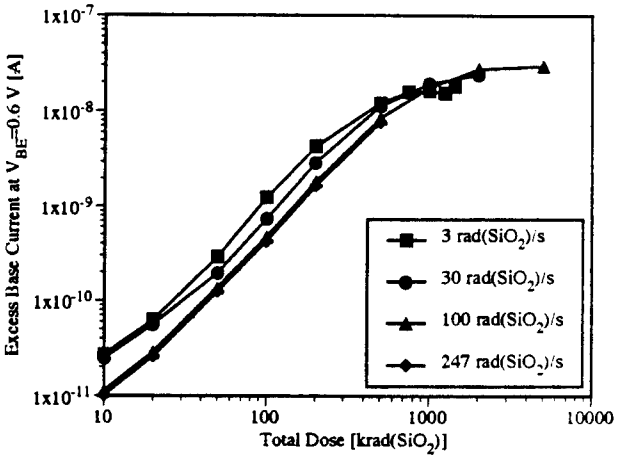


Figure 4. Excess base current at $V_{BE} = 0.6$ *V* versus total dose at four different dose rates for devices from technology A.

trapped in this oxide upon exposure to ionizing radiation. This has profound implications for the device response, as seen in the next sections.

III. EXPERIMENTAL RESULTS

The excess base current at a base-emitter voltage, V_{BE}, of 0.6 *V* is plotted in figure 3 versus total ionizing dose for technologies A, B, and C. For all technologies, the excess base current increases super-linearly with total dose for low total doses, but tends to saturate for very large total doses. This behavior is described analytically in [11]. Note that the value of excess base current at saturation is different for technologies A and B. Also note that, although technology C exhibits much more excess base current at low total doses than either technology A or B, the currents merge at high total doses. Finally, although the dose rates for the different technologies are slightly different, the differences in response in figure 3 are not due to these dose-rate differences, as discussed below.

In figure 4, ΔI_B at $V_{BE} = 0.6$ *V* is plotted versus total dose for

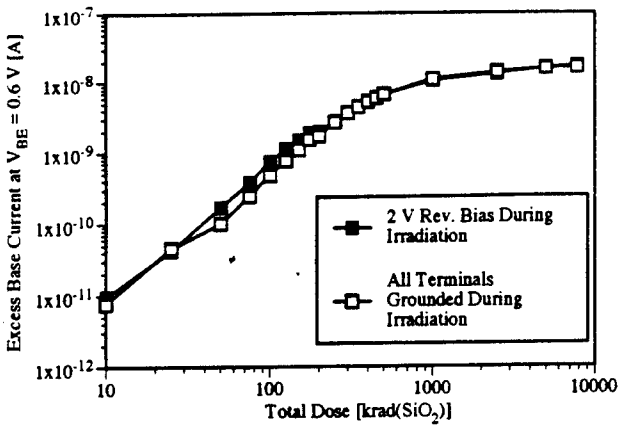


Figure 5. Excess base current at $V_{BE} = 0.6\ V$ versus total dose for two irradiation biases. The devices are from technology B.

devices from technology A, with dose rate as a parameter. For low total doses, the degradation is most severe at the lowest dose rates, as reported in [3]. This difference has recently been linked to the difference in oxide charge buildup as a function of dose rate [6, 10]. Note that there is little difference in device response as a function of dose-rate for rates larger than approximately 100 rad(SiO_2)/s, as reported in [3]. This behavior has been observed on all other technologies we have tested. The low-dose response differences will be discussed elsewhere [10]. Here we concentrate on the high total doses, where the excess base current in figure 4 saturates at a value that is independent of dose rate.

In figure 5, ΔI_B at $V_{BE} = 0.6\ V$ is plotted versus total dose for two different bias conditions during irradiation: (1) all pins grounded and (2) emitter-base junction reverse-biased at 2 *V*. The devices are from technology B and the dose rate is 11 rad(SiO_2)/s. Reverse bias on the emitter gives slightly worse degradation at lower total doses, but the excess base currents merge for high total doses at a value that is independent of bias. Note that the value of the worst-case (maximum) base current is consistent with that of the Technology-B devices irradiated at 211 rad(SiO_2)/s in figure 3 ($\approx 2\pm1 \times 10^{-8}$ A), further confirming the dose-rate independence of worst-case base current.

Although the results presented above are all for $V_{BE} = 0.6$ V, the conclusions are the same for other measurement biases. The specific saturation value of the excess base current depends on the value of V_{BE} at which ΔI_B is measured, but the saturation behavior is the same. Also, although a limited amount of data has been presented here, it is representative of an enormous amount of data taken over the course of this project.

To summarize the experimental results, the excess base current in an irradiated BJT increases super-linearly with total dose at low total doses [1, 11]. In this regime, the excess base current depends on the particular charge-trapping properties

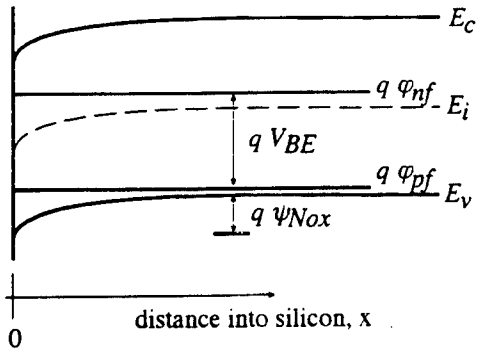


Figure 6. Energy band diagram normal to the oxide-silicon interface along the dashed line indicated in figure 2.

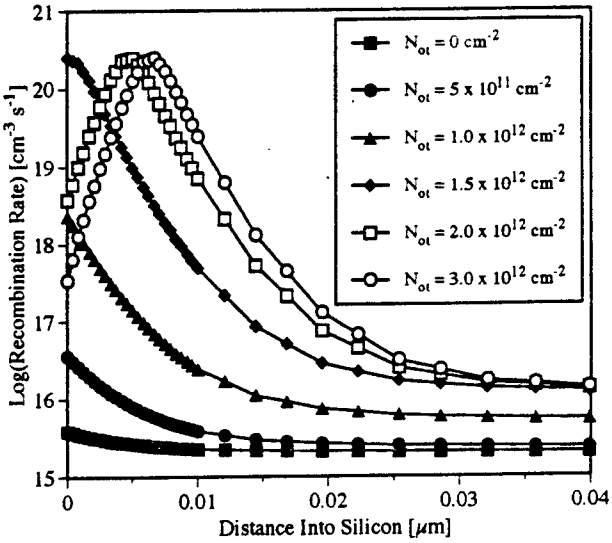


Figure 7. PISCES-simulated recombination rate versus position normal to the interface for $V_{BE} = 0.5\ V$ and various amounts of positive oxide charge.

of the oxide that covers the emitter-base junction [10]. The device response is dose-rate-, irradiation-bias-, and technology-dependent in this regime. However, once a critical amount of charge has accumulated in the oxide, the excess base current saturates at a value that is independent of how the charge accumulated. This saturated excess base current depends only upon device parameters, as seen in the next section.

IV. MODELING

To understand the above results, consider the effect of positive charge on the band bending normal to the oxide-silicon interface in the lightly-doped extrinsic base. Figure 6 shows energy bands along the dashed vertical line indicated in figure 2 for a fixed positive oxide charge at a fixed forward-bias voltage between emitter and base. The *x*-direction is taken to be normal to the oxide-silicon interface. Figure 7 plots PISCES-simulated [12] recombination rate along the same line for a

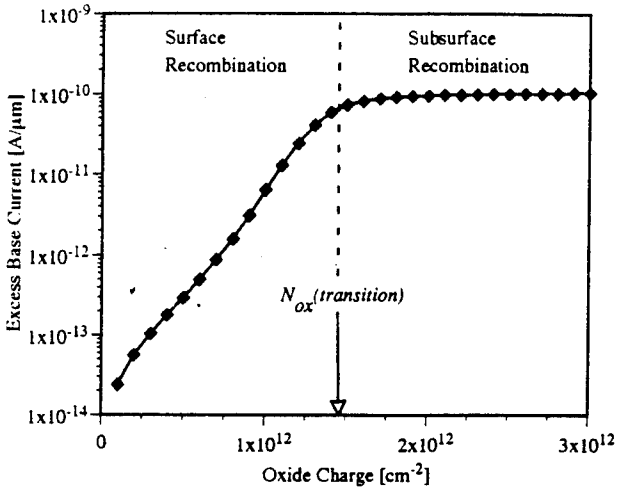


Figure 8. PISCES-simulated excess base current versus positive oxide charge at V_{BE} = 0.5 V for technology B.

fixed forward bias and increasing amounts of positive oxide charge. As oxide charge increases, the surface recombination rate in the lightly-doped portion of the extrinsic base (far from the emitter-base junction) increases to a value set by the applied voltage and the recombination lifetime in the silicon, as shown below. In these simulations, the lifetimes were adjusted to match the forward characteristics of the device. Also, the lifetime in the silicon was assumed to be uniform. Further increases in oxide charge push the peak of the recombination rate below the surface, into the silicon bulk. For the conditions in figure 7, the recombination peak is located below the surface for the curves corresponding to $N_{ot} \geq 1.5 \times 10^{12}$ cm^{-2}.

The excess base current is, quite generally, the integral of the recombination rate multiplied by the electronic charge. From figure 7 it is seen that, once the recombination peak moves subsurface, the integral of the recombination rate is largely unchanged, which translates into a saturation in the excess base current. Also note that the integral of the recombination rate is largely independent of the surface recombination rate when the peak moves below the surface. For example, an order of magnitude increase in the surface recombination rate (which could be due to e.g. interface traps) would still affect the total integral only slightly when the recombination peak lies below the surface.

In figure 8, PISCES-simulated excess base curent at V_{BE} = 0.5 V is plotted versus positive oxide charge. The excess base current saturates once N_{ox} exceeds $N_{ox}(transition)$, which may be expressed, using the depletion approximation, as [11]

$$N_{ox}(transition) = \sqrt{\frac{2\,\varepsilon_{Si}\,N_s}{q}\left(\frac{k\,T}{q}\ln\left(\frac{N_s}{n_i}\right) - \frac{V_{BE}}{2}\right)} \quad . \quad (1)$$

In this expression, ε_{Si} is the permittivity of silicon, q is the magnitude of the electronic charge, k is Boltzmann's constant, T is absolute temperature, n_i is the intrinsic carrier concentration, and N_s is the surface doping of the lightly-doped extrinsic base. For technology B, $N_{ox}(transition)$ at V_{BE} = 0.5 V is about 1.5 × 10^{12} cm^{-2}, as indicated in figure 8.

When the recombination peak moves below the surface, the excess base current becomes relatively insensitive to additional surface damage, as discussed in the preceding paragraph. This is a result of the sharply peaked nature of the recombination rate with respect to depth. The peak value occurs at the position where $n = p$ (the cross-over condition). Note that for N_{ot} = 2.0 × 10^{12} cm^{-2}, the recombination rate at the surface is approximately 1% of the peak rate. If the surface recombination lifetime were to decrease e.g. by an order of magnitude, the surface recombination rate would still only be 10% of the peak rate. When the cross-over point has moved beneath the surface, increasing the surface recombination velocity increases the recombination right at the surface, but the integrated recombination rate, which is the excess base current, remains largely unchanged. Thus, the excess base current when the cross-over point is beneath the surface may be written as $\Delta I_B(subsurface)$, given by [11]

$$\Delta I_B(subsurface) = \frac{q\,n_i}{2\,\tau}\,\Delta x\,A_{EX}\exp\left[\frac{q\,V_{BE}}{2\,k\,T}\right] . \quad (2)$$

In this expression, Δx is the effective thickness of the region where significant recombination occurs, A_{EX} is the surface area of the lightly-doped extrinsic base that surrounds the emitter, and τ is the bulk minority-carrier lifetime. An estimate for Δx is the depletion-layer width induced by the positive oxide charge in the depletion approximation, $\Delta x < N_{ox}/N_s$. Based on equation (2), an expression for the worst-case current gain is derived in the Appendix. This expression,

$$\beta(worst\ case) = 2\,n_i\frac{A_E}{A_{EX}}\frac{D}{GN}\frac{\tau}{\Delta x}\exp\left[\frac{q\,V_{BE}}{2\,k\,T}\right] , \quad (3)$$

agrees well with the data, as demonstrated in the Appendix, and further confirms the utility of this analysis.

Equation (2) indicates that $\Delta I_B(subsurface)$ is proportional to the area of the lightly-doped extrinsic (LDE) base, as shown in [1], and inversely proportional to the recombination lifetime. Recall from figure 3 that technology A had a higher value of saturation excess base current than technology B. The difference is explained by noting that the LDE base area for technology A is larger than technology B, and the LDE base is more heavily doped at the surface, which leads to a shorter recombination lifetime. These effects combine to produce a larger $\Delta I_B(subsurface)$ in technology A than technology B.

Technology C exhibits much larger excess base current at low total doses than either technologies A and B, which is attrib-

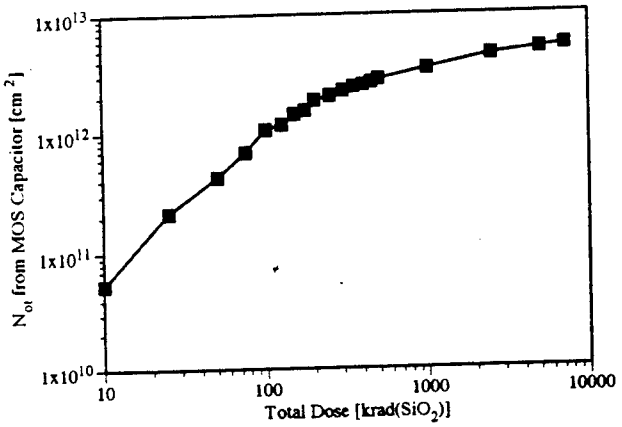


Figure 9. Oxide-trapped charge versus total dose from MOS capacitors from technology B. Both electrodes were grounded during irradiation.

utable to differences in the charge trapping properties of the oxide in this technology. Evidently, technology C accumulates positive charge more rapidly than either technology A or B. However, because technology C has the same LDE base area as technology A and similar LDE base surface doping, it is not surprising that the excess base currents for technologies A and C merge at high total doses.

The dose-rate and bias independence of $\Delta I_B(subsurface)$ evident from figures 2 and 3 is also easily understood from figures 7 and 8. Although the total dose required to exceed $N_{ox}(transition)$ depends upon the particular irradiation conditions, $\Delta I_B(subsurface)$ is only a weak function of N_{ox} beyond $N_{ox}(transition)$. In fact, beyond $N_{ox}(transition)$, the excess base current may be expected to increase by approximately a factor of 2 as more and more of the recombination occurs below the surface. Thus, although the saturated value of the base current is reached at lower total doses for low-dose-rate and reverse-biased irradiations, eventually all devices accumulate enough oxide charge to force the recombination peak below the surface.

This effect is confirmed in figure 9, where N_{ot} measured from midgap-voltage shifts in MOS capacitors with the same oxide as that over the lightly-doped extrinsic base is plotted versus total dose. It is seen that extremely large amounts of positive charge accumulate in the oxide, and the increase in N_{ot} does not saturate with increasing total dose. If we assume for simplicity that N_{ox} is the same as N_{ot}, which amounts to neglecting the contribution of charged interface traps, then $N_{ox}(transition)$ is reached at a total dose of about 200 krad(SiO_2). Referring to figure 5, we see that the excess base current has indeed begun to saturate at about 200 krad(SiO_2). The actual increase in excess base current beyond 200 krad(SiO_2), however, is about a factor of five instead of the predicted factor of two. Possible explanations for the discrepancy are non-negligible surface effects, a laterally nonuniform distribution of oxide charge, the limitations of the depletion approximation, and the contribution of charged interface traps. To first order, however, the theory and experiment agree quite well, as the excess base current saturates while the oxide charge continues to accumulate.

V. CONCLUSIONS

From the previous discussion, it is evident that the rate at which the charge builds up does not affect the worst-case excess base current in these devices. This result clarifies important features of the dose-rate dependence in BJT gain degradation that has been reported previously. The enhanced degradation at low dose rates occurs because more oxide charge is trapped at the lower dose rates than at higher rates, in agreement with measurements of oxide trapped charge in MOS capacitors formed using the oxide that covers the emitter-base junction [10].

In addition, we have shown that any convenient laboratory dose rate may be used to obtain the worst-case response of the device, as long as the total dose used is sufficient to produce saturation in ΔI_B. It should be noted that, at the high total doses required to observe saturation in ΔI_B, failure modes other than gain degradation of the transistors may limit circuit performance (e.g., leakage currents, especially in BiCMOS devices with non-hardened MOS field oxides). This fact does not affect the worst-case nature of the method proposed above for obtaining the excess base current, however. When the worst-case excess base current flows in a modern bipolar transistor, the current gain is still sufficient for many digital circuit applications [13, 14]. The results presented above indicate a potentially fast, reliable means to qualify bipolar devices in digital circuits for space applications.

APPENDIX

In this appendix, an expression for the worst-case current gain in an irradiated BJT is derived and compared to a previously-proposed expression, as well as experimental data.

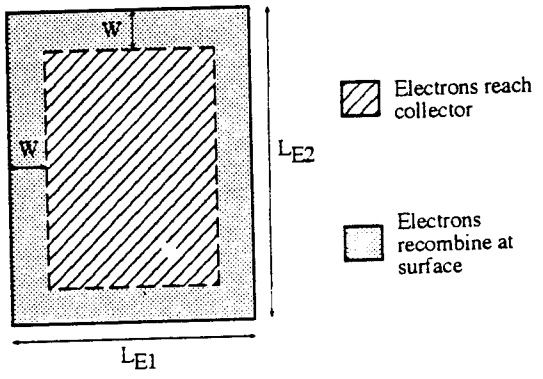


Figure A-1. Top view of an emitter illustrating the areas relevant to the no-depletion-region-recombination model.

A.1. NO DEPLETION REGION RECOMBINATION

A simple model was proposed in [15] for the worst-case current gain in an irradiated BJT. The model assumes that, in the worst-case, the oxide-silicon surface acts as an infinite sink for carriers injected from the emitter. If we consider the rectangular emitter geometry shown in figure A-1, with dimensions L_{E1} and L_{E2}, and an active base width W, the model assumes that all carriers injected into the base within a distance W of the edge of the emitter will recombine at the oxide-silicon interface. Carriers emitted in the interior region of the emitter will traverse the base and show up as collector current. It is assumed that the device has ideal emitter-injection efficiency (no back-injection of carriers into the emitter) and that, in the worst case, the total base current approaches the base current due to recombination at the oxide-silicon interface. Based on these assumptions, the collector current is proportional to the injected electrons that reach the collector and the base current is proportional to the injected electrons that recombine at the interface. The current gain is just the ratio of the areas:

$$\beta(\text{worst case}) = \frac{(L_{E1} - 2W)(L_{E2} - 2W)}{2W(L_{E1} + L_{E2} - 2W)}, \qquad (1\text{-A})$$

where the numerator is the area over which the injected electrons reach the collector and the denominator is the area over which the injected electrons recombine at the interface. This expression simplifies to $A_E/(W P_E)$ for large-area emitters ($L_{E1}, L_{E2} \gg W$), where A_E is the emitter area ($L_{E1} \times L_{E2}$) and P_E is the emitter perimeter ($2 \times (L_{E1} + L_{E2})$). This model does not include the voltage dependence of the current gain, since it neglects recombination in the emitter-base depletion region.

A.2. DEPLETION REGION RECOMBINATION

In this section, an expression is derived for worst-case current gain based on depletion-region recombination. To begin, we define the collector current as $I_C = I_{Co} \exp[q V_{BE}/(kT)]$, and the excess base current given in equation (2) as $\Delta I_B = \Delta I_{Bo} \exp[q V_{BE}/(2kT)]$. When the excess base current dominates the total base current, the current gain may be written as

$$\beta(\text{worst case}) = \frac{I_{Co} \exp\left[\frac{q V_{BE}}{2kT}\right]}{\Delta I_{Bo}}. \qquad (2\text{-A})$$

From equation (2), we have

$$\Delta I_{Bo} = \frac{q n_i \Delta x A_{EX}}{2\tau}, \qquad (3\text{-A})$$

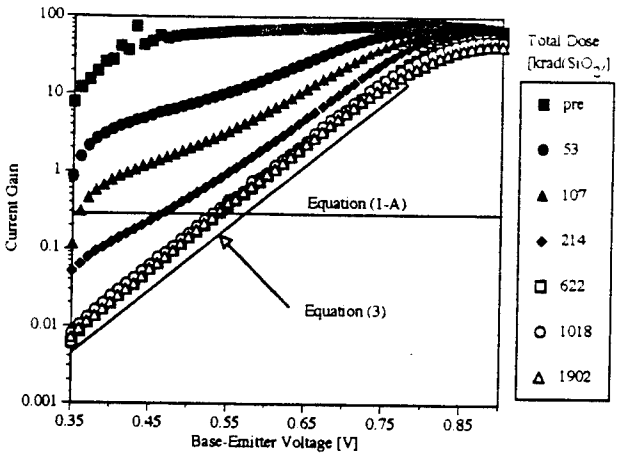


Figure A-2. Current gain versus base emitter voltage for technology A, with the two model predictions superimposed on the experimental data.

and the collector current prefactor, I_{Co} may be expressed as

$$I_{Co} = \frac{q D n_i^2 A_E}{GN} \qquad (4\text{-A})$$

where D is the diffusivity of electrons traversing the base, A_E is the area of the emitter, and GN is the Gummel number of the base defined by

$$GN = \int_{base} N_A(x)\, dx \qquad (5\text{-A})$$

Combining these expressions, we obtain the following expression for the worst-case current gain:

$$\beta(\text{worst case}) = 2 n_i \frac{A_E}{A_{EX}} \frac{D}{GN} \frac{\tau}{\Delta x} \exp\left[\frac{q V_{BE}}{2kT}\right] \qquad (6\text{-A})$$

In figure 2-A, the current gain versus V_{BE} for devices from technology A is plotted for several values of total ionizing dose. Relevant device parameters are given in table 1. At high total doses, the current gain exhibits the voltage dependence predicted by equation (6-A). Since D, τ, and Δx are difficult to determine analytically, the entire prefactor of equation (6-A) must be determined from the experimental data. Equation (1-A) is also plotted in this figure. It is seen that when depletion region recombination is neglected, the voltage dependence of the current gain is not accounted for. This means that the estimate of current gain does not bound the experimental values at low base-emitter voltages, and is overly pessimistic at the larger base-emitter voltages.

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V.I. Saturation of the Dose-Rate Response of BJTs Below 10 rad(SiO_2)/s: Implications for Hardness Assurance

Saturation of the Dose-Rate Response of Bipolar Transistors Below 10 rad(SiO_2)/s: Implications for Hardness Assurance

R. Nathan Nowlin[1], D.M. Fleetwood[2], and R.D. Schrimpf[3]

Abstract

The gain degradation of modern bipolar transistors was investigated for dose rates ranging from 0.01 to ~2000 rad(SiO_2)/s. Five different radiation sources were used for the exposures: three ^{60}Co sources, a 10-keV x-ray source, and a ^{137}Cs source. The ^{137}Cs exposures at 0.01 rad(SiO_2)/s are two orders of magnitude lower in dose rate than any previous irradiations for this process and thus facilitate comparison to the device response in space. Low-dose-rate gain degradation exceeds high-dose-rate degradation for total doses less than 1 Mrad(SiO_2), consistent with previous reports. For the first time, the gain degradation is demonstrated to be equivalent for dose rates between 0.01 and 10 rad(SiO_2)/s, suggesting that the dose-rate response saturates at ~10 rad(SiO_2)/s for the devices studied in this work. On the basis of a recent model, high-dose-rate irradiations at 60°C were performed and found to be consistent with the room-temperature, low-dose-rate, saturated response. These results suggest several promising new approaches to bipolar space-qualification testing.

I. Introduction

It has been demonstrated that for some modern bipolar transistors high-dose-rate irradiation followed by room-temperature or elevated-temperature annealing cannot estimate the low-dose-rate gain degradation [1,2]. Post-irradiation annealing at temperatures of 60 to 250°C reduced the magnitude of the excess base current (surface recombination current in the base) to nearly zero [2]. On the other hand, it has been shown that the magnitude of the excess base current is greater in devices irradiated at low dose rates (below 150 rad(SiO_2)/s) than in devices irradiated at high dose rates (above 150 rad(SiO_2)/s) [1-3]. In reference 2, the excess base current measured at constant bias and dose was shown to increase at each successively lower dose rate below 150 rad(SiO_2)/s down to 1-10 rad(SiO_2)/s. This paper presents data at a dose rate two orders of magnitude below any previously reported for these modern bipolar transistors. The dose-rate dependence of the gain degradation saturates below 10 rad(SiO_2)/s. That is, the magnitude of the degradation at 0.01 rad(SiO_2)/s is nearly the same as that at 10 rad(SiO_2)/s. Consequently, characterization at 10 rad(SiO_2)/s provides an effective estimate of the lower-dose-rate response in these devices. Furthermore, this paper presents data on bipolar transistors irradiated at high dose rates and elevated temperatures simultaneously in a successful attempt to simulate the low-dose-rate response. These data support a recent model for the physical mechanisms responsible for the dose-rate effect [4]. In addition, overtesting by a factor of 3 in total dose is found to be another way to conservatively estimate the low-dose-rate response of these devices.

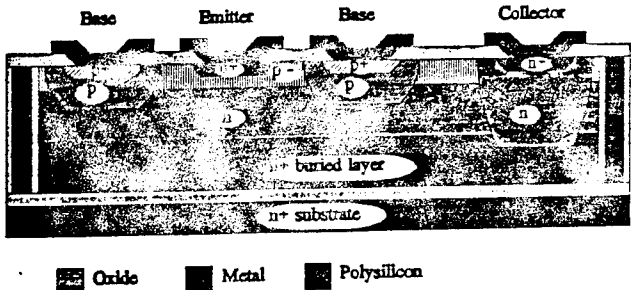


Figure 1. A representative cross-section of the devices studied in this work. The emitter layout dimensions are 1.5 μm × 1.5 μm. The oxide over the emitter-base junction is 545 nm thick.

II. Experiment

A dose rate of 0.01 rad(SiO_2)/s was achieved in a 20-Ci, J.L. Shepherd ^{137}Cs source. Dosimetry was performed using CaF_2:Mn thermoluminescent dosimeters with short exposure times followed by long fades [5]. Using this procedure, the dose rates in four different radio-isotopic sources (the Phillips Lab cesium source, the University of Arizona cobalt source, the Naval Surface Warfare Center-Crane cobalt source, and the Sandia National Labs cobalt source) have been cross calibrated, and the results are traceable to the National Institute of Standards and Technology. Dosimetry for the 10-keV x-ray irradiations was performed with a calibrated PIN diode [6,7]. Results from each of these sources were combined to determine the dose-rate dependence of the gain degradation over the dose-rate range of 0.01 to 1760 rad(SiO_2)/s.

For the cesium experiments, sixteen NPN bipolar transistors fabricated in a single-poly, silicon-on-insulator, complementary bipolar process (see Figure 1 and reference 8) were irradiated. There were both polysilicon emitter and crystalline emitter transistors available. This paper focuses on the results for the crystalline emitter transistors. Eight of these transistors were irradiated with all terminals grounded, and the other eight were irradiated while biased with 2 V (reverse bias) on the emitters. The devices were periodically removed from the source in order to track changes in the device parameters as the total dose increased. The dc I-V characteristics were measured at each level of total dose by sweeping the base-emitter voltage

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(V_{BE}) from 0 to 1 V and monitoring the base (I_B) and collector (I_C) currents using an HP4145 Semiconductor Parameter Analyzer. The base and collector terminals were grounded while the emitter was pulled negative during the characterization. The details of the experiments performed in the other sources have been described previously [1-3] and are similar to the procedures described above.

In addition to the above experiments, several new exposures were performed in this work using Sandia's ARACOR 4100 semiconductor irradiation source [4]. One set of devices was exposed to 10-keV x rays at dose rates of 0.4, 1.67, 20, and 200 rad(SiO_2)/s at room temperature (4-8 transistors per dose rate). Another set was exposed at dose rates of 1.67, 20, and 200 rad(SiO_2)/s as they were heated to 60°C by means of a resistive strip placed under the delidded package. The temperature was measured at the package surface with a calibrated Type-K (chromel-alumel) thermocouple. After the thermocouple registered a temperature of 60°C, the devices were allowed to equilibrate for about five minutes before the irradiations began. Similarly, they were allowed to cool to room temperature before the post-irradiation characterization was performed. The cooling was done in two stages. The packages were allowed to cool in the irradiation test fixture until the thermocouple registered about 40°C; then they were placed in the measurement test head and allowed to cool for another five minutes. It was confirmed that the devices were measured while at room temperature by noting that the post-irradiation collector current matched the pre-irradiation collector current [9]. (No changes to the collector current were observed as a result of irradiation. In addition, any residual temperature variations are normalized out of the data presented here by normalizing the excess base current to the pre-irradiation collector current [3].) Once cooled, the dc I-V characteristics were measured as described above. The devices were irradiated at 60°C to either 100 krad(SiO_2) or 300 krad(SiO_2) in a single exposure.

III. Results

Figure 2 shows the dc I-V characteristics for devices irradiated at 0.01 rad(SiO_2)/s for several levels of total dose up to 125 krad(SiO_2). Note that there are large increases in the base current at low bias levels due to increased surface recombination current at the base surface. An increase in the midgap-level interface-trap density in the low-field, thick, screen oxide over the p-type base (see Figure 1) increases the recombination current, but more importantly an increase in the positive-oxide-charge density modulates the base surface potential to even more strongly increase the surface recombination current [10]. The collector current remains unchanged by the irradiations.

Figure 3 shows the corresponding gain degradation for devices irradiated at 0.01 rad(SiO_2)/s. (The dc current gain $\beta = I_C / I_B$.) Note that there is significant degradation at levels well below 100 krad(SiO_2) at this dose rate. For example, Figure 4 compares the gain degradation at 20 krad(SiO_2) for

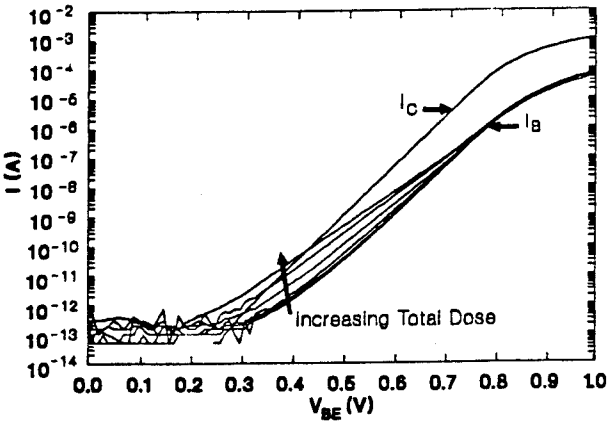


Figure 2. The dc I-V characteristics for square emitter devices for various levels of total dose up to 125 krad(SiO_2).

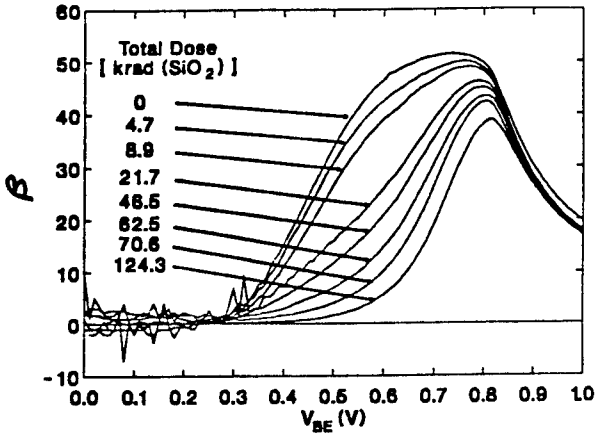


Figure 3. The dc current gain degradation for devices irradiated at 0.01 rad(SiO_2)/s.

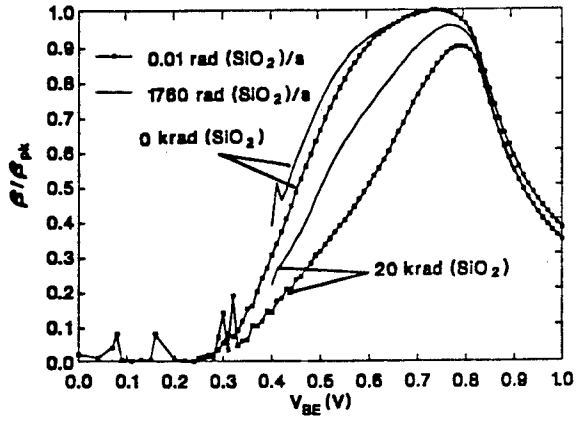


Figure 4. Gain degradation at two different dose rates compared at 20 krad(SiO_2). β_{pk} is the peak pre-irradiation current gain.

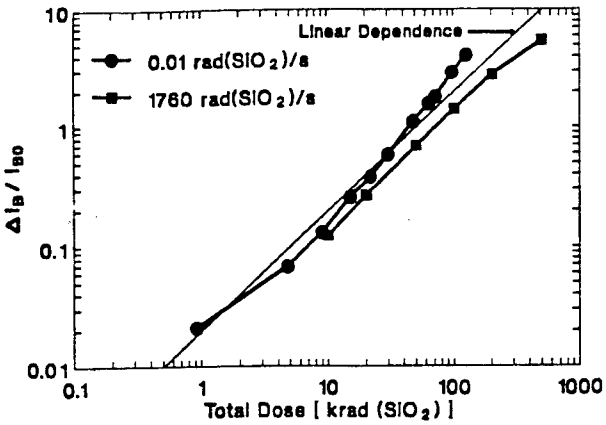


Figure 5. Comparison of the magnitude of the excess base current with increasing dose for devices irradiated at two different dose rates. V_{BE} = 0.6 V.

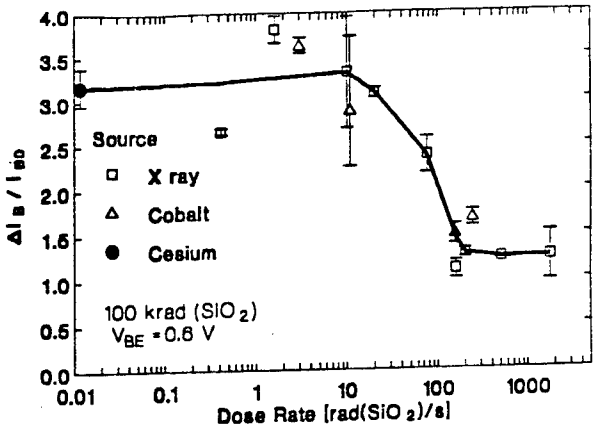


Figure 6. Dose-rate dependence of the excess base current for devices irradiated at room temperature. The line is a guide to the eye.

devices irradiated at 0.01 rad(SiO_2)/s and 1760 rad(SiO_2)/s. As measured at V_{BE} = 0.6 V, the gain is degraded by ~50% in the low-dose-rate case (at only 20 krad(SiO_2)!), but it is only degraded by ~25% in the high-dose-rate case. It should be noted that, although the magnitude of the damage is smaller for higher current densities (higher V_{BE}), a wide range of current densities will exist for the various transistors in a commercial integrated circuit. Consequently, the greater gain degradation at low dose rates suggests there may be reliability concerns for space applications of linear bipolar microcircuits as discussed in section IV.

Figure 5 shows the increases in excess base current with increasing dose for the devices irradiated at the two dose rates indicated in Figure 4. The excess base current ($\Delta I_B = I_{B,\,post\text{-}rad} - I_{BO}$) is normalized to the pre-irradiation base current, I_{BO}. Therefore, a ratio of one means that the base current has doubled. Note that the base current has doubled after about 40 krad(SiO_2) in the low-rate case and after about 80 krad(SiO_2) in the high-rate case. Also observe that at 100 krad(SiO_2), the low-rate degradation is about three times worse than the high-rate degradation. Similarly, the degradation in the high-rate case at a dose about 2-3 times higher than 100 krad(SiO_2) is comparable to that at 100 krad(SiO_2) in the low-rate case. These observations, which will be made more apparent in the following figures, suggest that an overtest by a factor of three could be used for hardness assurance for these devices, as discussed below. Finally, the divergence of the low-dose-rate and high-dose-rate curves above 10 krad(SiO_2) appears to be consistent with the space-charge effects predicted at the higher dose rates in the model of reference 4.

Figure 6 compares the magnitude of the excess base current measured at 100 krad(SiO_2) for devices irradiated at several dose rates ranging from 0.01 rad(SiO_2)/s (in the cesium source) to 1760 rad(SiO_2)/s (in the x-ray source). (Error bars indicate the range of the transistor-to-transistor variations.) As previously reported [2], the magnitude of the total-dose-induced excess base current is independent of dose rate above 150 rad(SiO_2)/s, and it increases below 150 rad(SiO_2)/s. This

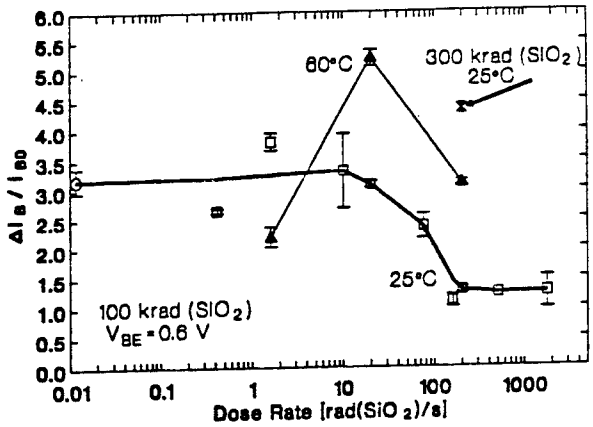


Figure 7. Dose-rate response of the excess base current after irradiation to 100 krad(SiO_2) at 25°C and 60°C. Also shown is a 200 rad(SiO_2)/s, 300 krad(SiO_2), 25°C data point representing a factor-of-3 overtest. (See also reference 4.)

is the first time gain-degradation data below 1 rad(SiO_2)/s have been reported for modern bipolar transistors. Note in Figure 6 that the degradation at 0.01 rad(SiO_2)/s is comparable to that at 10 rad(SiO_2)/s. Furthermore, the degradation at the low dose rates is about 3-4 times greater than that at the high dose rates. Similar results have been seen for both conventional-emitter and polysilicon-emitter transistors and for transistors irradiated under zero and reverse bias. Moreover, these results are relatively independent of irradiation source energy. The ^{60}Co results closely match the x-ray results at high and low dose rates [2]. The results in Figure 6 and the x-ray to ^{60}Co correlation data in reference 2 indicate that the differences in charge yield for the different energy sources do not play a major role in the dose-rate response.

Finally, Figure 7 shows the results of both the high-temperature (60°C) irradiations and a room-temperature

300 krad(SiO_2) exposure done at 200 rad(SiO_2)/s superimposed on the data of Figure 6 (without the ^{60}Co data). The 300 krad(SiO_2) point demonstrates the results of over-stressing the devices by a factor of three at high dose rates and room temperature. Such a test gives a conservative estimate of the low-dose-rate response in this case. Alternatively, irradiation at high dose rates and high temperatures also simulates the low-dose-rate response, as predicted by a recent model of enhanced gain degradation at low dose rates [4]. If the devices are irradiated at high temperatures and intermediate dose rates (20 rad(SiO_2)/s), the low-dose-rate response is overestimated. However, as one goes lower in dose rate at high temperature, annealing and charge-compensation effects [2,4] begin to dominate the response, and the test is nonconservative. The mechanisms for this temperature dependence as well as the mechanisms for the dose-rate effect are discussed in detail in reference 4.

IV. Implications for Hardness Assurance

There are several significant implications for hardness-assurance testing of these single-poly bipolar devices that can be drawn from the above observations. First of all, since the dose-rate response saturates at low dose rates, it is not necessary to test at even lower dose rates to determine the response of these devices in space applications. One may only have to test at dose rates around 10 rad(SiO_2)/s to obtain a worst-case response for these devices. Moreover, the low-dose-rate response is only about 3-4 times worse than the high-dose-rate response when these devices are exposed to 100 krad(SiO_2). Therefore, as shown in Figure 7, an overtest in dose by a factor of 3 can allow one to conservatively estimate the suitability of these devices for space applications if other circuit elements do not interfere by causing earlier failure. As an alternative to low-dose-rate testing or overtesting, one may test these devices at dose rates within the range specified by MIL-STD-883D Test Method 1019.4 (50 to 300 rad(SiO_2)/s) if the devices are heated *in-situ* to a temperature of about 60°C. For a very stringent test, an intermediate-dose-rate (between 10 and 50 rad(SiO_2)/s), high-temperature combination may be used. However, one should be careful not to lower the dose rate too far when using the high-temperature test, since annealing and charge-compensation effects may dominate the dose-rate response.

Although these results (particularly the specific dose rate and the relative magnitude at which the response saturates) are specific to the parts studied in this work, similar results have been observed in capacitors and transistors of four to five other (similar) technologies [3,4]. In addition, several types of linear integrated circuits (IC's) fabricated in more conventional technologies have demonstrated earlier failures and greater parametric shifts at low dose rates than at high dose rates [11-13], although IC's fabricated in the technology studied in this work do not appear to show this same dose-rate dependence [14]. In the conventional-technology IC's, the susceptible transistors have been identified as either substrate PNP's (used as input transistors [14]) or multiple-collector lateral PNP's [13]. Although the designs of these PNP transistors differ significantly from the transistors studied in this work, the radiation-sensitive features are similar. The common feature which has been shown to drive the dose-rate response [4] is the presence of a low-field, thick, screen oxide over a lowly doped p-type base diffusion (see Figure 1). In the IC's fabricated in the technology studied here [14], there are no substrate or lateral PNP transistors, since this is a complementary process [8]. Moreover, the vertical PNP transistors in this process have been demonstrated to have superior hardness [3], since, in contrast to the vertical NPN's and the substrate and lateral PNP's, the p-type emitter is very heavily doped (p^+). Nevertheless, the physical mechanisms behind the radiation responses of all these devices are the same. This suggests that similar approaches to space-radiation hardness assurance may also prove effective for other device types that demonstrate this dose-rate behavior due to the presence of a low-field, thick, screen oxide over a lowly doped p-type base diffusion. Clearly, however, more work is required to evaluate the general applicability of the approaches suggested here.

V. Summary and Conclusions

The gain degradation in modern bipolar transistors has been measured at a dose rate of 0.01 rad(SiO_2)/s, two orders of magnitude lower than any previously reported results for this class of devices. The magnitude of the degradation at this low dose rate indicates potential reliability concerns for space applications for these devices. The dose-rate dependence of the gain degradation saturates below 10 rad(SiO_2)/s. This suggests that bipolar hardness-assurance testing for space applications may need to be performed at dose rates below the 50 rad(SiO_2)/s limit specified in MIL-STD-883D Test Method 1019.4. Since for these devices the degradation at 0.01 rad(SiO_2)/s is comparable to that at 10 rad(SiO_2)/s, testing at dose rates around 10 rad(SiO_2)/s would provide a conservative estimate of the device response at lower dose rates. Alternatively, hardness-assurance testing at dose rates within the range specified in Test Method 1019.4 may be done if these devices are irradiated at moderately elevated temperatures (~60°C) or overtested by a factor of 3. Finally, the results of the high temperature irradiations support the application of a new model [4] for enhanced hole trapping at low dose rates in low-field, thick oxides to the dose-rate dependence of the gain degradation in modern bipolar transistors. These results suggest several new approaches to space-qualification testing for modern bipolar devices.

VI. Acknowledgments

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V.J. Physical Mechanisms Contributing to Enhanced Bipolar Gain Degradation at Low Dose Rates

PHYSICAL MECHANISMS CONTRIBUTING TO ENHANCED BIPOLAR GAIN DEGRADATION AT LOW DOSE RATES

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Abstract

We have performed capacitance-voltage (C-V) and thermally-stimulated-current (TSC) measurements on non-radiation-hard MOS capacitors simulating screen oxides of modern bipolar technologies. For 0-V irradiation at ~ 25°C, the net trapped-positive-charge density (N_{ox}) inferred from midgap C-V shifts is ~ 25-40% greater for low-dose-rate (< 10 rad(SiO_2)/s) than for high-dose-rate (> 100 rad(SiO_2)/s) exposure. Device modeling shows that such a difference in screen-oxide N_{ox} is enough to account for the enhanced low-rate gain degradation often observed in bipolar devices, due to the ~ exp(N_{ox}^2) dependence of the excess base current. At the higher rates, TSC measurements reveal a ~ 10% decrease in trapped-hole density over low rates. Also, at high rates, up to ~ 2.5-times as many trapped holes are compensated by electrons in border traps than at low rates for these devices and irradiation conditions. Both the reduction in trapped-hole density and increased charge compensation reduce the high-rate midgap shift. A physical model is developed which suggests that both effects are caused by time-dependent space charge in the bulk of these soft oxides associated with slowly transporting and/or metastably trapped holes (e. g., in E_6' centers). On the basis of this model, bipolar transistors and screen-oxide capacitors were irradiated at 60°C at 200 rad(SiO_2)/s in a successful effort to match low-rate damage. These surprising results provide insight into enhanced low-rate bipolar gain degradation and suggest potentially promising new approaches to bipolar and BiCMOS hardness assurance for space applications.

I. Introduction

In 1991 Enlow and co-workers [1] found that some types of bipolar devices show greater gain degradation after low-dose-rate irradiation at low electric fields than after higher-rate irradiation. Moreover, they found that higher-rate irradiation followed by room-temperature or high-temperature annealing could not simulate the low-dose-rate response of these bipolar devices [1]. These results have been confirmed and extended for several device types by Nowlin et al. [2,3] and Wei et al [4]. This enhanced bipolar gain degradation at low dose rates appears not to be caused primarily by interface-trap buildup. Instead, it appears to be due to an increase in net positive charge in the screen (also called the "spacer" or "sacrificial") oxide that overlies the emitter-base junction [4]. This result is very surprising, because MOS devices typically show reduced net positive charge at low dose rates due to trapped-hole neutralization and/or enhanced interface-trap buildup [5]. Moreover, under constant temperature and electric field conditions, it has been shown for several types of MOS devices (though mostly at electric fields greater than ~ 1 MV/cm) that high-dose-rate irradiation and room-temperature annealing can accurately predict MOS low-dose-rate response [6,7]. Indeed, this is one of the principles that underlies MIL-STD 883D, Test Method 1019.4 and other radiation hardness assurance test methods [8]. That bipolar devices show different dose-rate and annealing responses than MOS devices complicates the development of cost-effective hardness assurance programs for space electronics. This issue is becoming more pressing in view of even more recent reports [9-11] of a growing number of bipolar microcircuits of different types from a variety of manufacturers showing lower-dose failure at low dose rates.

In this work, we have performed thermally-stimulated-current (TSC) and capacitance-voltage (C-V) measurements to evaluate fundamental charge trapping mechanisms of capacitors with oxides fabricated to simulate bipolar screen oxides as closely as possible. A cross-section typical of modern dielectrically isolated bipolar technologies is shown in Fig. 1 [12-14]. The screen oxide overlies the base-emitter junction. In a radiation environment, it is a particular problem because the buildup of positive oxide charge can greatly enhance the surface recombination rate in the p- base region of NPN transistors. We note that a similar structure can occur in some types of lateral or substrate PNP transistors from other (especially older commercial) technologies, except that the vulnerable p- region lies in the

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emitter. Thus, not only do the results of this study apply to the NPN transistors considered here, but they may also contribute to similar dose rate effects observed recently in lateral and substrate PNP devices [9,11].

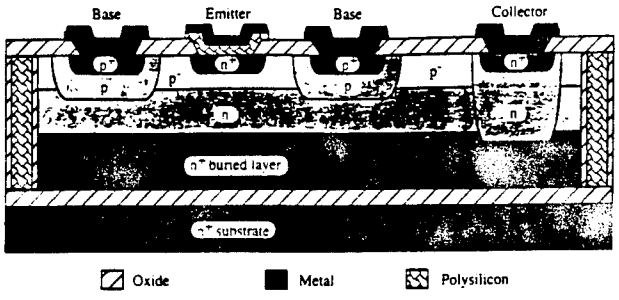


Fig. 1. Cross-section of bipolar devices built in ADI's XFCB process. The oxide above the emitter-base junction is ~ 545 nm (Refs. [12,13]). RBCMOS devices have similar cross-sections but ~ 54 nm oxides above the emitter-base junction (Ref. [14]).

Examining Fig. 1, we recognize that we may be limited in our ability to simulate screen-oxide response because capacitors have uniform electric fields (at least before the buildup of significant radiation-induced trapped charge); whereas, in actual device applications, fringing fields at the base-emitter junction often lead to non-uniform electric fields in the screen oxides [1-4,13]. Nevertheless, in this paper we will attempt to answer the following questions:

- Do MOS capacitors fabricated similarly to bipolar screen oxides show enhanced charge buildup at low dose rates, or is this response unique to bipolar screen oxides in real devices?
- Is this mechanism unique to (soft) bipolar screen oxides subjected to low-field irradiation, or will these oxides show similar effects after high-field exposure, and/or will other soft or radiation-hardened MOS oxides show a similar response?
- What is the mechanism for enhanced hole trapping at low dose rates, and what can be done about it?

In considering these issues, we compare screen-oxide TSC and C-V results with bipolar device modeling. Based on experimental results, we develop a physical model of the trapped-charge buildup and neutralization processes that evidently cause enhanced bipolar low-dose-rate gain degradation. We use this model to obtain additional insight into screen-oxide capacitor and transistor response, and (on the basis of a model prediction) compare 60°C irradiation at high rates to capacitor and transistor room-temperature low-rate response. Implications for screen-oxide hardening and hardness assurance testing for space applications are discussed.

II. Devices and Hardening

Three types of capacitors were evaluated in this study. Most notable are p-substrate capacitors with a final surface doping of ~ 8 x 10^{17} cm^{-3}, having ~ 54 nm wet oxides grown at 900°C. These were fabricated at Analog Devices, Inc. (ADI) to simulate RBCMOS (Radiation-hardened Bipolar CMOS) screen oxides. Before gate metallization, oxides were subjected to ion implantations simulating **(a)** a threshold-voltage implant (30-keV B to a dose of 2 x 10^{11} cm^{-3}), and **(b)** base-doping implants (40-keV B to 1.5 x 10^{13} cm^{-3} and 115-keV B to 1.5 x 10^{12} cm^{-3}). After these implants, the oxides received a 30-min, 1000°C N_2 anneal to simulate emitter drive-in. These implantation [15-17] and anneal [17-20] steps degrade oxide hardness significantly due to the formation of oxygen vacancies and vacancy complexes that serve as hole traps in SiO_2 [20-24]. It is possible that B contamination may further degrade screen oxide hardness [11], though previous work suggests it may be equally likely that implant-induced displacement damage is the primary culprit [17,25]. At an electric field of ~ 1 MV/cm, the radiation-induced-hole trapping efficiency (f_h) inferred from TSC measurements on these devices [26] is essentially 1.0. Thus, virtually every hole escaping initial electron-hole recombination is subsequently trapped, confirming that these screen oxides are indeed very soft. In purely MOS devices and ICs, oxide electric fields are much higher. Thus, similar oxides would cause circuit failure due to gate or field oxide leakage [5,7] at doses much less than where failure may occur due to gain degradation in typical bipolar applications [1-4,13].

MOS capacitors were also fabricated at Sandia National Laboratories (SNL). One set of capacitors was processed in SNL's radiation-hardened Mod-B process with a 45-nm dry oxide grown at 1000°C with f_h = 0.05 [26]. The other had a radiation-hardened 44-nm dry oxide grown at 950°C that was intentionally softened [17-19,24] with a 30-min, 1000°C N_2 anneal (but no ion implantation); for it, f_h = 0.17. This trapping efficiency is more than 3-times greater than that of the hard oxide, confirming the reduction in hardness expected for high-temperature annealing [20-24]. But it is ~ *6-times less* than the trapping efficiency of the implanted ADI oxides, showing the importance of the implants in degrading screen-oxide hardness [15-17]. If possible to do so without impacting device and IC performance and yield, minimizing implant damage to the screen oxide and reducing the thermal budget of the emitter drive-in (as

well as thinning the screen oxide as much as possible [18]) would improve the radiation tolerance of this and similar processes. While it is outside the scope of this paper to discuss screen-oxide hardening further, this clearly is an area for future study.

For comparison with capacitors, we also measured the gain degradation of bipolar transistors from ADI's RBCMOS and XFCB processes. Unfortunately, all capacitor data we have is for devices most closely simulating the RBCMOS process, which has a screen oxide thickness of ~ 54 nm. On the other hand, most of the transistor dose-rate data we have is for XFCB devices that have ~ 545 nm oxides above the emitter-base junction. Still, the bipolar portions of the two device cross sections are similar (but not identical [12-14]). So the common trends observed below in dose-rate response of RBCMOS capacitors and XFCB transistors suggest that, while the gain degradation varies for the two processes [1-4], the mechanisms that lead to enhanced low-rate gain degradation in the two cases are quite similar.

III. Experimental Details

Irradiations were performed at room temperature or (in a few cases) at 60°C with a 10-keV ARACOR x-ray irradiator. This system is equipped with a Nicolet XRD power supply that enables exposure at rates ranging from greater than 1000 rad(SiO_2)/s to less than 1 rad(SiO_2)/s. Dosimetry was performed with a calibrated PIN diode [27,28]. For 60°C irradiations, a simple resistive strip heated the device. The temperature was measured at the package or capacitor-mounting surface with a calibrated Type-K (chromel-alumel) thermocouple. All capacitor C-V and bipolar I-V measurements were performed at room temperature; this was closely monitored for the bipolar Gummel plots to ensure temperature variations did not mask (or mimic) dose rate effects [29]. Dose rate effects similar to those observed for x-ray irradiation in this study have also been reported for Co-60 and Cs-137 irradiation [1-4,30].

Capacitors were mounted for TSC measurements as described in Refs. [31,32]. All TSC runs involved heating capacitors from ~ 20°C to ~ 350°C in ~ 1 h; the TSC bias was large enough in all cases shown to avoid space-charge and capacitance-change effects [31,32]. Standard high-frequency (1 MHz) C-V measurements [33] were combined with TSC measurements (for negative bias TSC) to estimate the density of trapped holes and electrons near the Si/SiO_2 interface, via:

$$Q_{CV} \cong -AC_{ox}\,\Delta V_{mg} \quad (1)$$

$$Q_h \cong \int I_{TSC}\,dt \quad (2)$$

$$Q_e \cong Q_h - Q_{CV}, \quad (3)$$

where Q_{CV} is defined as the net "C-V" charge, A is the capacitor area, C_{ox} is the oxide capacitance per unit area, ΔV_{mg} is the radiation-induced midgap-voltage shift, Q_h is the radiation-induced trapped-hole charge measured via TSC, I_{TSC} is the TSC corrected for background and parasitic leakage sources [31], and Q_e is the trapped-electron charge near the Si/SiO_2 interface [26,32]. Values of ΔV_{mg} were estimated from high-frequency C-V curves swept from accumulation (negative bias) to inversion (positive bias) at 0.5 V/s for the p-substrate ADI capacitors, as commonly done in the literature [24,33]. Irradiated devices often exhibited C-V hysteresis due to slow border traps [24,34-36], as discussed below. Therefore, C-V sweeps on n-substrate SNL devices were performed at 0.5 V/s from inversion (negative bias) to accumulation (positive bias) to facilitate comparison with ADI capacitors. So, for all device types in this study, border-trap occupancy during C-V sweeps should be similar [36], minimizing difficulties in estimating the relative numbers of bulk-oxide and border traps on the capacitor response. We emphasize that C-V hysteresis was not observed in these devices before irradiation. Moreover, a full TSC cycle (ramping from ~ 20°C to 350°C) removed all measurable hysteresis. Thus, TSC measurement removed (or at least rendered electrically inactive) all oxide-, interface-, and border-trap charge in these devices. Finally, general trends in capacitor response with dose rate, annealing time, etc., did not depend upon the direction in which C-V curves were swept; reliable data interpretation only required measurements and analyses be consistent.

IV. Dependence on N_{ox}

In Fig. 2 we show ΔV_{mg} as a function of dose rate for 0-V irradiation of bipolar screen-oxide capacitors with ~ 54 nm oxides [3]. At the lower rates, the magnitude of ΔV_{mg} is larger than at higher rates. Because we expect the value of ΔV_{mg} to be proportional to the net trapped-positive-charge density (N_{ox}) in the bulk of the oxide [21,32,33], Fig. 2 indicates that N_{ox} is greater in these oxides after low-dose-rate irradiation than high-rate irradiation. Hence, even though we cannot fully simulate the detailed electric fields of bipolar screen oxides in device use, the dependence of N_{ox} on dose rate

in these capacitors is similar in form (magnitudes are discussed below) to the dependence of bipolar gain degradation on dose rate observed in many types of devices [1-4]. Because of the large doping densities of the p-substrate capacitors used for these screen oxides, it was difficult to estimate interface-trap densities using C-V stretchout or Terman analysis between midgap and inversion (the range of the band gap of most interest for relating p-substrate capacitor response to transistor response [33]), and midgap-to-flatband C-V stretchout was small compared to ΔV_{mg}. No consistent trend in inferred interface-trap densities could be observed for these devices to within ± 25%.

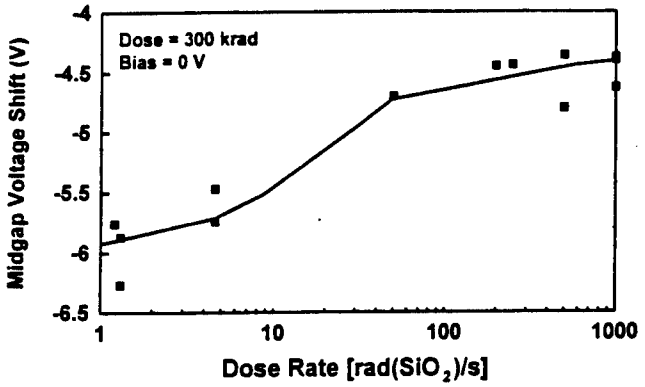


Fig. 2. ΔV_{mg} vs. dose rate for 0-V 10-keV x-ray irradiation of bipolar screen-oxide capacitors with non-radiation-hardened oxides. Capacitors were irradiated to 300 krad(SiO_2).

The data of Fig. 2 contrast starkly with what is commonly reported for MOS devices; that is, ΔV_{mg} almost universally decreases in magnitude with decreasing dose rate in studies of MOS devices (typically at positive bias) [5-8,37]. However, to our knowledge, the data of Fig. 2 represent the first extensive study of the dependence of ΔV_{mg} on dose rate for 0-V irradiation of oxides having such large hole-trapping efficiencies. Thus, while surprising, these data do not contradict previous experience on similar devices. Possible reasons for this response are discussed below.

With Fig. 3 we first address the practical issue of whether the 25-40% difference in C-V midgap shifts and thus in inferred postirradiation N_{ox} ($\cong \Delta N_{ox}$) is enough to cause the large enhancement in bipolar gain degradation often observed at low dose rates [1-4,9-11]. The results of Fig. 3 are for XFCB devices, which have thicker oxides overlying the emitter-base junction than the RBCMOS process, which the capacitors of Fig. 2 more closely simulate. However, it is still useful for discussing the general relationship between N_{ox} and the excess base current (ΔI_b) of bipolar junction transistors (BJTs). This should be valid not only for these NPN processes, but also for NPNs in many other modern bipolar/BiCMOS technologies [13] (and may also apply in modified form to lateral and substrate PNPs in older commercial technologies [9,11]). The ΔI_b data in Fig. 3 are extracted at a base-emitter voltage (V_{BE}) of 0.6 V from Gummel plots for 1.5 μm x 1.5 μm poly-Si emitter BJTs [4,38,39]. Similar trends are observed for crystalline emitters and other values of V_{BE}. The N_{ox} data on the x-axis of Fig. 3 are extracted from Gummel plots using the BJT charge separation method of Kosier et al [13]. Also shown are PISCES simulations for these device structures and charge densities [4,38,39]. Up to N_{ox} values above ~ 10^{12} cm^{-2} in Fig. 3, it is clear from both the charge separation data and the PISCES simulations that ΔI_b depends strongly on N_{ox}. Above ~ 2 x 10^{12} cm^{-2} in Fig. 3, corresponding to a total dose of ~ 3 Mrad(SiO_2) here [4,38], the dependence saturates. Reasons for this saturation are discussed by Kosier et al. [38,39], and are quite important to understanding and predicting BJT response at high doses, but do not apply to the lower-dose response in Fig. 3.

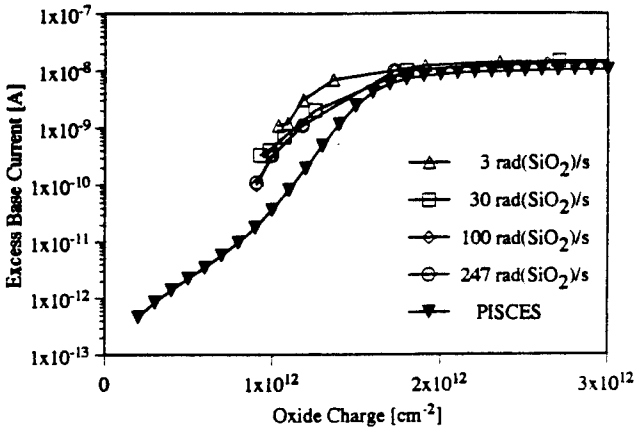


Fig. 3. Excess base current as a function of net oxide charge density inferred for ADI XFCB transistors irradiated at varying Co-60 dose rates using the charge separation technique of Kosier et al. and PISCES simulations (Refs. [12,35,36]). The maximum dose for the experimental data is 5 Mrad(SiO_2). (After Ref. [4].)

The important aspect of Fig. 3 here is the strong [$\Delta I_b \sim \exp(N_{ox}^2)$] dependence of excess base current on net trapped-positive-charge density. Due to the much smaller radiation-induced changes in the collector current, I_c [1-4,13,40], the gain degradation, $I_c/(I_b + \Delta I_b)$, where I_b is the pre-irradiation base current, shares this dependence. In the region of the curve showing the ~ $\exp(N_{ox}^2)$ dependence, for example, a ~ *40% increase* in N_{ox} can cause a ~ *2.5-times increase* in ΔI_b. (For more details on the data and modeling of Fig. 3, please see Refs. [4,13,38-40].) Thus, Fig. 3 confirms that the in-

crease in N_{ox} at low rates illustrated in Fig. 2 can indeed be great enough to cause the large enhancement in bipolar gain degradation often observed at low dose rates.

V. TSC/C-V Results

A. ADI Screen Oxides: 0 V Irradiation.

To try to understand what causes the behavior observed in the capacitors of Fig. 2 and, by extension, the BJTs in Fig. 3, we performed TSC measurements on the ADI screen-oxide capacitors in tandem with the C-V measurements of Fig. 2. Figure 4 shows TSC measurements for three devices. One was irradiated at a rate of ~ 4.6 rad(SiO_2)/s, another at ~ 1000 rad(SiO_2)/s, and the third was irradiated at ~ 1000 rad(SiO_2)/s and annealed at 0 V for 17 h at 25°C in an (unsuccessful) effort to simulate the low-rate response [5-7]. These results are typical of other TSC runs on these devices after high- and low-rate 0-V irradiation, and/or 0-V annealing. Note that the highest TSC peak is that of the *low-rate* irradiation. Moreover, high-rate irradiation and 17-h, 0-V anneal leads to a very different trapped-hole distribution in energy than the low-rate irradiation. Indeed, the trapped-hole energy distribution appears to have "spread" about the peak value during the anneal, indicating a possible redistribution of trapped holes during room-temperature anneal. The integrated TSC charge (Q_h) values in the low-rate, high-rate, and high-rate plus anneal cases from Eq. (2) are 1190, 1060, and 940 pC; respective trapped-electron densities (Q_e) from Eq. (3) are 65, 170, and 180 pC. From C-V measurements, the respective midgap voltage shifts are -5.5 V, -4.4 V, and -3.8 V. From these results we infer (converting total charges to number densities) that, for the 4.6 rad(SiO_2)/s data, $\Delta N_h \cong 2.3 \times 10^{12}$ cm^{-2} and $\Delta N_e \cong 1.3 \times 10^{11}$ cm^{-2}. For the 1000 rad(SiO_2)/s data, $\Delta N_h \cong 2.1 \times 10^{12}$ cm^{-2} and $\Delta N_e \cong 3.3 \times 10^{11}$ cm^{-2}. Finally, for the high-rate plus anneal data, $\Delta N_h \cong 1.85 \times 10^{12}$ cm^{-2} and $\Delta N_e \cong 3.4 \times 10^{11}$ cm^{-2}.* (A table of values for Figs. 4-8 is provided for reference in the Appendix.) Thus, ~ 10% more holes are trapped in these oxides during 0-V irradiation at low rates than at higher rates, and room-temperature annealing after high-rate irradiation only reduces the number of trapped holes. Also, *2.5-times more holes are compensated by trapped electrons* for high-rate irradiation, with or without annealing, than for low-rate irradiation. In support of this point, more C-V hysteresis at midgap is observed after high-rate irradiation (-1.1 V, or 25% of the midgap shift) than after low-rate irradiation (-0.9 V, or 16% of the midgap shift). This also is consistent with the association of at least some trapped electrons with border traps [26,35,36]. The additional holes in the oxide at low rates and the additional trapped-hole compensation at high rates combine to provide the ~ 25% increase in magnitude of ΔV_{mg} for the low-rate case.

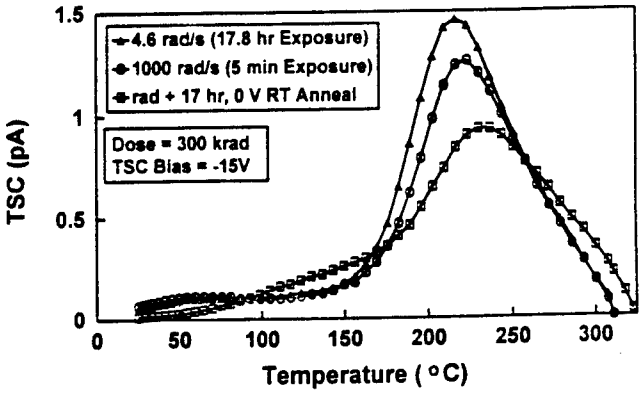


Fig. 4. TSC vs. dose rate and/or annealing time for bipolar screen-oxide capacitors with ~ 54 nm oxides irradiated to 300 krad(SiO_2) with 10-keV x rays at 0 V bias.

B. Soft SNL Capacitors: 0 V Irradiation.

Figure 5 shows TSC after 0 V irradiation for SNL capacitors with 44 nm oxides that received a 1000°C, 30 min N_2 anneal, but no ion implant damage. Again, the highest peak is for devices irradiated at low rate (here 31.7 rad(SiO_2)/s), and the TSC after irradiation and 17-h annealing does not match the low-rate TSC. From Eqs. (1)-(3), **(a)** Q_h = 5240 pC and Q_e = 3800 pC for the 31.7 rad/s case; **(b)** Q_h = 5000 pC and Q_e = 3180 pC for the 2000 rad/s case; and **(c)** Q_h = 4450 pC and Q_e = 3700 pC for the high-rate plus anneal case. These combine to give midgap shifts of -1.36 V, -1.75 V, and -0.76 V in the three cases, respectively. The midgap C-V hysteresis was ~ 1.2 V for the high- and low-rate exposures, suggesting similar slow border-trap densities in these cases. The hysteresis was ~ 0.75 V for the high-rate plus anneal case, indicating fewer slow border traps.

That the midgap shift in the low-rate case for these oxides is intermediate between higher-rate and high-rate

* That values of ΔN_h lie in the saturation regime of the BJT curves in Fig. 3 should not be taken too seriously because (a) trapped-electron and interface-trap densities partially offset trapped-hole densities in the calculation of "N_{ox}" in the charge separation method of Kosier et al. (Ref. [13]), and (b) the relative dependence of ΔI_b on N_{ox} is better defined in the device modeling that leads to the results of Fig. 3 than is the absolute calibration of the N_{ox} scale on the x-axis (Refs. [13,39]). What is more significant is that the total dose of 300 krad(SiO_2) to which the capacitors were irradiated is well below the doses at which BJT response is observed to saturate (Refs. [4,39]).

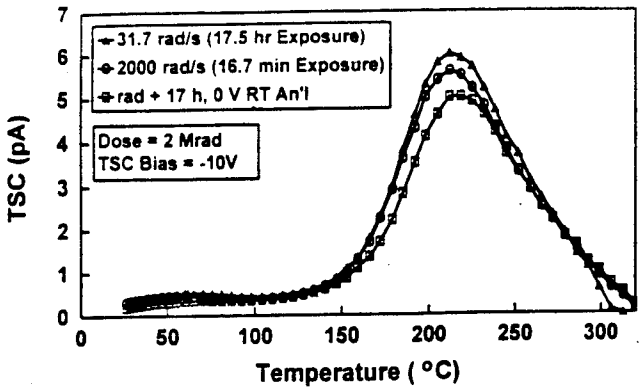


Fig. 5. TSC vs. dose rate and/or annealing time for SNL capacitors with 45-nm oxides that received a 1000°C, 30 min N_2 anneal after gate oxidation, but were not implanted through. X-ray irradiation and anneal biases were 0 V.

plus annealing cases occurs for the following reasons. While the low-rate enhancement of hole trapping observed in Fig. 4 for the (even softer) ADI capacitors is also observed for these devices, processing differences evidently have led to differences in trapped-hole distributions near the Si/SiO_2 interface and consequently in the trapped-hole compensation rates of the ADI and soft SNL capacitors [41,42]. The dramatic differences in trapped-hole compensation between high- and low-rate irradiation observed for the ADI capacitors in Fig. 4 are not observed in Fig. 5. Instead, for the soft SNL capacitors, more compensating electrons are found following low-rate irradiation or high-rate irradiation plus long-term annealing than after high-rate irradiation. This can easily be explained via standard models of electrons tunneling into compensating trap sites in the oxide as a function of time [37,41,42]. So, though these capacitors do not show the midgap shift increases at low rates that the softer ADI capacitors do, it is noteworthy that high-rate irradiation and room-temperature annealing cannot simulate low-rate response for these devices.

C. *Hard SNL Capacitors: 0 V Irradiation.*

Moving another step forward on the hardness scale, in Fig. 6 we show TSC curves for high- and low-rate 0-V irradiation of SNL capacitors with hardened oxides. Now the high-rate case has the higher TSC at both low temperatures (energies) and at the TSC peak. From Eqs. (1)-(3) we find **(a)** Q_h = 3240 pC and Q_e = 2240 pC in the 1000 rad/s case, and **(b)** Q_h = 3000 pC and Q_e = 2660 pC in the 4.4 rad/s case, leading to midgap shifts of -1.5 V and -0.5 V in the two cases, respectively. Though not shown in the figure for clarity, irradiation at high-rate and 0-V annealing at 25°C for equivalent times gives a response indistinguishable (to within less than ~ 5% experimental uncertainty in TSC curves) from the low-rate case. This response is exactly in line with expectations from previous MOS irradiation and annealing response studies [6-8], as discussed below.

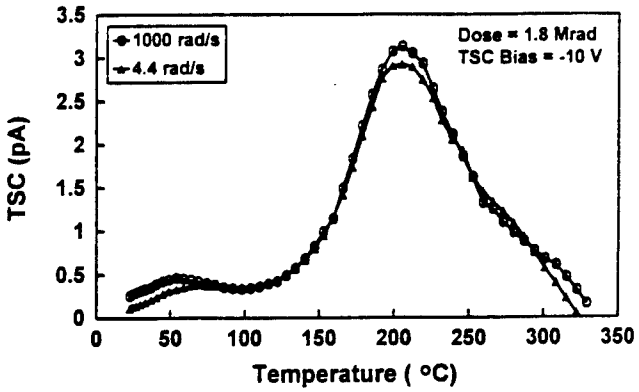


Fig. 6. TSC vs. dose rate for MOS capacitors with ~ 45-nm rad-hard oxides irradiated to 1.8 Mrad(SiO_2) with 10-keV x rays at 0 V bias.

D. *Implications of 0-V Irradiations.*

The results of Figs. 4-6 suggest that fabricating screen oxides having the hardness of the capacitors of Fig. 6 (~ 5% hole trapping efficiency, as compared to nearly 100% for the ADI capacitors of Fig. 4), which may not be possible given processing constraints [12,14], would have two beneficial effects. First, it would improve bipolar/BiCMOS device hardness due to a reduction in screen-oxide trapped charge. Second, Fig. 4-6 suggest that, as one reduces the screen-oxide trapping efficiency, one is also likely to reduce testing difficulties associated with predicting low-rate gain degradation from high-rate irradiation and annealing.

E. *ADI Capacitors: +6 V Irradiation.*

In Fig. 7 we show TSC for high- and low-rate irradiation of the ADI bipolar screen-oxide capacitors exposed to 50 krad(SiO_2) at +6 V bias (electric field > 1 MV/cm). Because of the reduced dose level, a smaller TSC bias of -10 V could be employed than in Fig. 4 without facing space charge problems during TSC measurement [31,32]. From Eqs. (1)-(3), we find **(a)** Q_h = 890 pC and Q_e = 135 pC for the 417 rad/s case, and **(b)** Q_h = 680 pC and Q_e = 125 pC for the 0.83 rad/s case, leading to midgap shifts of -3.8 V and -2.8 V in the two cases, respectively. In contrast to the 0-V data of Fig. 4, more holes remain here after the high-rate irradiation than after the low-rate radiation, consistent

with the trend one would expect from previous dose-rate and annealing studies of MOS devices at comparable electric field conditions [6-8]. For higher-rate irradiation plus room-temperature 6 V annealing for 17 h, results identical to the low-rate response were obtained (omitted from the figure for clarity). Similarly, for higher-field irradiation of 45-nm MOS oxides with hardened oxides (data not shown), greater TSC is also observed after high-rate irradiation than after low-rate irradiation, again as expected from previous work [6-8]. (Note that these results effectively eliminate dosimetry problems from serious consideration as potential causes of the results of Figs. 2 and 4.) We conclude that neither ADI bipolar screen oxides nor hardened MOS oxides show enhanced hole trapping at low rates for high-field irradiation. However, because these field conditions are unrealistic in operating bipolar/BiCMOS circuits or devices, the results of Fig. 4 are more relevant to predicting gain degradation.

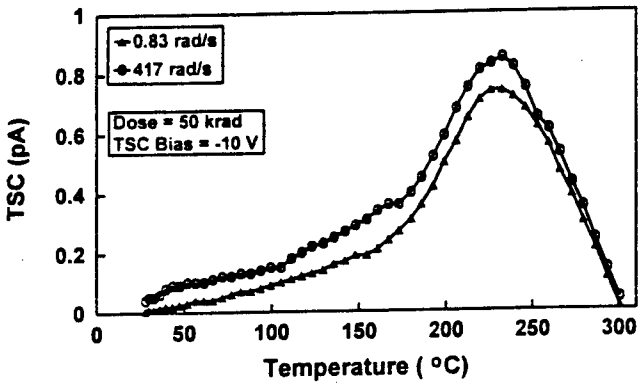


Fig. 7. TSC vs. dose rate for bipolar screen oxide capacitors with ~ 54 nm oxides irradiated to 50 krad(SiO_2) with 10-keV x rays at +6 V.

F. *ADI Capacitors: -6 V Irradiation*

A final case is useful to explore before discussing the physical mechanisms responsible for the effects observed in Figs. 2-4. In Fig. 8 we look at *positive-bias TSC* following *negative bias irradiation* (-6 V to 50 krad) for the ADI capacitors. While in previous cases (positive or zero bias irradiation followed by negative-bias TSC) results are weighted toward estimating trapped hole and electron densities near the Si/SiO_2 interface, irradiations at negative bias and TSC measurements at positive bias give preferential weight to charge trapped near the gate/SiO_2 interface [31]. Thus, if the magnitude of the TSC is larger in one of the cases, the interface weighted most heavily in the measurements must have had more charge trapped nearby. If the two TSC magnitudes are nearly equal, either relatively uniform trapping must exist throughout the SiO_2 bulk, or approximately equal amounts of charge must be trapped near each interface. (In either of these two cases, Eqs. (1)-(3) cannot be applied in their present forms [26,31]). However, the magnitude of the TSC in Fig. 8 is significantly less than in Fig. 7 (the current flow direction is opposite in the two cases, of course, due to the opposite TSC biases [31,32]), confirming that more charge is trapped near the Si/SiO_2 interface than the gate/SiO_2 interface. A similar conclusion is reached from 0-V irradiations of ADI capacitors to 300 krad(SiO_2) and positive-bias TSC measurements (data not shown).

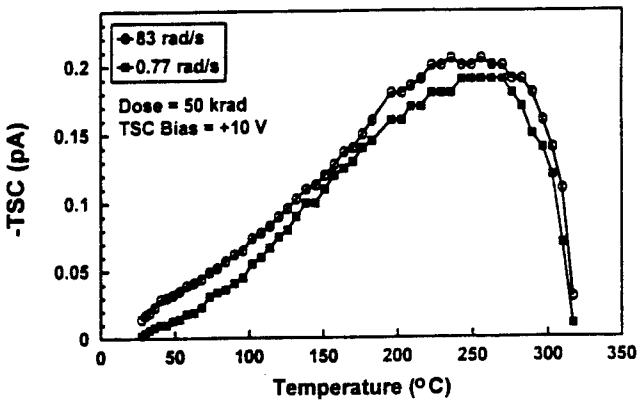


Fig. 8. TSC vs. dose rate for bipolar screen oxide capacitors with ~ 54 nm oxides irradiated to 50 krad(SiO_2) with 10-keV x rays at -6 V.

Quantitatively, in Fig. 8, Q_h = -330 pC in the 83 rad/s case, and Q_h = -280 pC in the 0.77 rad/s case. Midgap voltage shifts were -0.76 V and -0.72 V in the two cases, respectively. Estimates of trapped-electron densities cannot be obtained in Fig. 8 because TSC and C-V methods weight charge near the Si/SiO_2 interface differently for these bias conditions [31,32]. As a final note on Fig. 8, the low-rate TSC lies just below the high-rate at all temperatures, though the *relative* differences are much larger at low temperatures. For example, the high-rate TSC is roughly twice the low-rate TSC at ~ 50°C, which is well outside differences attributable to experimental error [31]. Differences are only about 5% near the peak at ~ 250°C, which is roughly equivalent to the experimental uncertainty at this temperature (the background parasitic leakage [31,32] is larger at high temperature than low temperature). Still, from the above values of ΔV_{mg}, it is clear that these low-energy differences in trap distributions in Fig. 8 do not cause significant differences in the net trapped-charge density estimated via C-V measurements.

VI. Physical Model

The preceding discussions suggest that many of the results of Figs. 2-8 cannot easily be explained in terms of standard hole transport, trapping, and neutralization models usually applied to MOS radiation response [37]. The difference in hardness of these screen oxides and the difference in operating electric field from normal MOS use (e. g., for gate or field oxides) are evidently what lead to their unusual dose-rate response. To understand Figs. 2-4, which are most relevant to enhanced low-rate bipolar gain degradation, we must account for the following observations based on the above results:

1) For 0 V irradiation, slightly more holes are trapped at low rates than at high rates for the ADI screen oxides (Fig. 4) and the soft SNL capacitors (Fig. 5), but not for the hard SNL capacitors (Fig. 6).
2) For 0 V irradiation, there are more compensating electrons in border traps following high-rate irradiation than low-rate irradiation for the ADI capacitors (Fig. 4), but not for the soft or hard SNL capacitors (Figs. 5 and 6).
3) High-rate 0-V irradiation followed by room temperature 0-V anneals cannot simulate low-rate response for the ADI or soft SNL capacitors (Figs. 4 and 5), but can for hard SNL capacitors (Fig. 6).
4) High-rate 6-V irradiation and room-temperature anneal simulates low-rate 6-V irradiation response for all types of devices examined (e. g., Fig. 7).
5) Excess *long-term* trapping in the bulk of the oxide or near the gate is small compared to the total trap density near the Si interface (Figs. 7 and 8).
6) The net trapped-positive-charge neutralization rate at 0 V is slow for ADI capacitors at 25°C (Fig. 4).

Points 1-3 represent results new to this work that are difficult to explain within the context of most previous MOS experience [6-8,37]. Points 4-6 provide additional information necessary to develop a physical model of the effects that lead to enhanced low-rate gain degradation in modern bipolar devices. These have led us to the model sketched in Fig. 9, which is applicable to ADI screen-oxide (or similar) capacitors irradiated at 0 V at ~ 25°C. Space does not allow us to discuss the detailed process by which this model was developed, so we limit our discussion to a general overview of the model and an evaluation of its consistency within the criteria of Points 1-6. In the next section, we also present corroborating evidence in support of the model that was obtained after the model was developed. This serves to reinforce (but certainly does not prove) its utility.

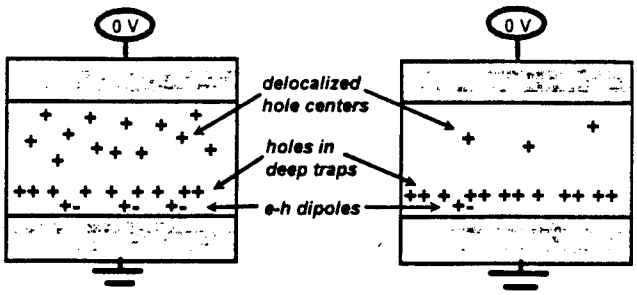


Fig. 9. Schematic illustration of mechanisms contributing to enhanced net positive charge in bipolar screen oxides at low dose rates. The left-hand side of the diagram refers to high-rate irradiation, and the right-hand side to low-rate exposure. Mechanisms apply to soft oxides irradiated at low electric fields.

A defining feature of the data is that there is a cross-over time corresponding to dose rates of ~ 10-100 rad(SiO_2)/s (see Fig. 2). This implies that there are time-dependent effects occurring during irradiation that are responsible for the difference in high- and low-rate response. This mechanism is not effective after irradiation, based on the lack of correspondence between low-rate data and high-rate plus annealing data for the ADI and soft SNL oxides (Point 3). One possible explanation for this behavior is the effect of space charge on hole transport, as we discuss below. However, to account for the results of Fig. 2, holes must transport out of the oxide, anneal, or be annihilated by radiation-induced electrons on time scales much longer than usual (~ 0.03 ms transit for this oxide thickness and electric field [37], assuming a transport parameter, α, of ~ 0.25 [37,43,44]). On the other hand, these time scales must be short compared to irradiation times corresponding to the "cross-over" between high- and low-rate response for the screen-oxide capacitors of Fig. 2 and (similarly) for BJTs [3] (Point 5). For example, the midpoint of the transitional region of the dose-rate response curve in Fig. 2 is ~ 30 rad(SiO_2)/s. It takes ~ 2.8 h to reach 300 krad(SiO_2) at 30 rad/s, defining an approximate upper bound for most of the delocalized holes to anneal.

Although it is possible that stretched-out transport due to polaron hopping with a lower than normal value of α could account for the long times associated with the space charge effects here, it is also interesting to consider another possibility (which might itself explain the presence of low α values [37,43,44] in oxides with very high bulk vacancy densities). We note that properties similar to the transport features outlined above have been associated in recent electron paramagnetic resonance (EPR) studies with E_δ' centers [23], which are oxygen vacancy complexes in SiO_2 thin films that can

serve as metastable, delocalized hole-trap sites [20,22,24,45-47]. Most importantly for our purposes in this discussion, these centers anneal or lose their hole to a more stable complex (like the classic E_γ' center) on time scales of seconds to hours during or after x-ray irradiation or hole injection [23,47]. Delocalized trapping centers like the E_δ' are vastly more common in the bulk of very soft oxides, like the ADI screen oxides, than in radiation hardened oxides [20,22,23] (Point 3).

During higher-rate irradiation (here for rates above ~ 100 rad/s), the large number of defects in the bulk of the oxide evidently retard the hole transport process by several decades over its normal duration [37]. The slowly transporting or metastably trapped holes in the bulk of the oxide act in conjunction with the building space charge due to more deeply trapped holes near the Si/SiO_2 interface to reduce the charge yield in the bulk of the oxide in the high-rate case, as compared to the yield in the low-rate case [37]. This reduction is due to the decreased local potential gradient (i. e., decreased local time-dependent electric field) between the trapped holes near the Si interface and the gate, caused by increased positive charge in the oxide bulk or near the gate interface, as shown on the left-hand side of Fig. 9. The slowly transporting and/or metastably trapped holes in the bulk of the oxides also provide additional electrostatic "back-pressure" during high-rate irradiation that causes holes to be trapped, on average, a little closer to the Si/SiO_2 interface than during low-rate irradiation. (The presence of space charge effects at higher rates is also suggested by the high- and low-rate dose dependencies of gain degradation in Ref. [30]).

The reduction in charge yield at high rates due to these space charge effects, coupled with the relatively slow trapped-hole neutralization rate at 0-V for these devices (Point 6), evidently accounts for the increase in trapped-hole density at low rates observed via TSC measurement (Point 1). That some holes are forced by the bulk space charge to be trapped a little closer to the Si at high rates than they otherwise would be at lower rates facilitates the formation of neutral trapped-hole/electron dipoles near the Si [26,35,36,42,48]. Some dipoles will function electrically as border traps and others will be electrically indistinguishable from annealed holes except during TSC measurement (and/or reverse-bias annealing [42,49,50]). This leads to the enhanced trapped-electron density near the Si/SiO_2 interface during the high-rate irradiations (Point 2). Finally, space-charge and electrostatic back-pressure effects only dominate device response at low fields because the applied electric field dominates local fields for higher-field exposure (Point 4).

Alternate models based on conventionally transporting holes ($\alpha \cong 0.25$) cannot explain why space charge effects become significant in ADI capacitors at dose rates of ~ 100 rad(SiO_2)/s, instead of the higher rates (generally greater than ~ 10^6 rad(SiO_2)/s) usually associated with transient space charge effects [37]. Models based on large trap densities near the gate interface are ruled out by the positive-bias TSC data of Fig. 8. Simple time-dependent charge redistribution effects are excluded by the absence of increases in the magnitude of ΔV_{mg} during 0-V postirradiation anneals (Figs. 4 and 5). Finally, models based on excess, relatively stable trapped electrons not associated with border traps [51,52] are similarly ruled out by the lack of increase in magnitude of ΔV_{mg} during 0-V annealing, and by the lack of a "turnaround" toward positive midgap shifts at higher doses. That high-rate irradiation and annealing cannot simulate low-rate response for the devices and irradiation conditions of Fig. 9 is consistent with the model presented above because the "true" annealing of a trapped hole (as opposed to compensation by a trapped electron) obviously cannot be reversed after irradiation. Also, the "excess" charged dipoles near the Si/SiO_2 interface formed at high rates cannot easily be separated during annealing by pushing the electron out of the compensating trap unless bias is altered [34,42,49,50].

VII. Test of Model: 60°C Irradiation

While the physical model outlined in the previous section can account for the differentiating features of the data in Figs. 2-8 listed above, all six points played significant roles in developing important features of the model. What is therefore needed is an independent check of the model. This is provided by the crucial dependence of the model on space charge and trapped-hole redistribution effects associated with slowly transporting or metastably trapped holes during irradiation. An interesting property of delocalized hole centers (as well as retarded hole transport) that has not yet been used in the development of the model is their strong temperature dependence. It is well known that hole transport is thermally activated [37,43,44]. Moreover, delocalized hole centers typically are neutralized at temperatures well below that at which deep hole traps anneal. For example, EPR studies show that E_δ' centers lose their spins at or below ~ 50°C, while E_γ' centers lose theirs at

~ 200°C [47]. (It is interesting that there are often minor and major peaks in TSC studies [26,34] at these same temperatures, suggesting a possible connection between the TSC peaks and EPR centers [23].)

Based on the above considerations, we decided to see if we could irradiate the capacitors at a temperature high enough to speed the transport and/or annihilation of the metastable holes in the bulk of the oxide without significantly perturbing the deeper trapped-hole distribution near the Si/SiO_2 interface. Based on their relative "annealing" temperatures, we selected ~ 60°C. The model of Fig. 9 makes a surprising prediction about ADI screen oxide capacitors irradiated at ~ 60°C. By eliminating the metastably trapped and/or slowly transporting holes responsible for the space charge effects that reduce the high-rate midgap shifts during 0-V irradiation, we should be able (if the model of Fig. 9 is correct) to *increase* the net positive oxide-trap charge in these devices by *slightly increasing* the temperature during irradiation! To our knowledge, such behavior has not been observed in MOS devices previously (though we do not know of a previous example of this experiment on this type of device). Indeed, it has been almost universally observed that raising the temperature above 25°C during irradiation or postirradiation annealing (though almost always at worst-case positive static bias) *decreases* the net trapped-positive charge density in MOS oxides [6-8,53,54]. Thus, the model of Fig. 9 leads us to a surprising prediction that can either invalidate the model or help to establish its self-consistency.

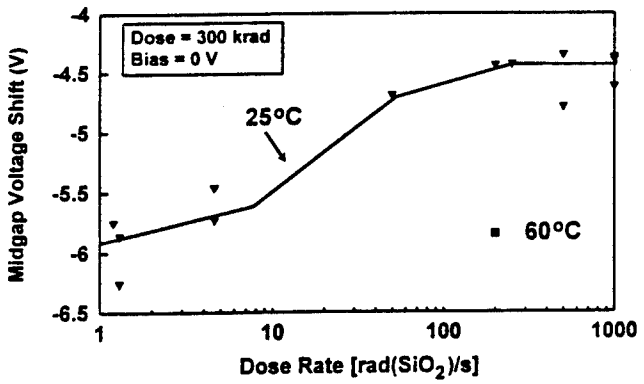


Fig. 10. Comparison of midgap voltage shifts for 25°C (triangles) and 60°C (solid square) 0-V irradiation of ADI capacitors with ~ 54 nm oxides at 200 rad(SiO_2)/s.

A. Capacitors.

For the first test, we irradiated the ADI capacitors of Figs. 2 and 4 at 60°C to 300 krad with 10-keV x rays at 200 rad(SiO_2)/s and 0 V. Results are compared with room-temperature midgap shifts in Fig. 10. Clearly, midgap shifts are larger in magnitude after 60°C irradiation than after 25°C irradiation (due to a slight increase in trapped-hole density and a significant reduction in trapped-electron density for the 60°C case), as predicted by the model of Fig. 9. Moreover, the 60°C irradiation shifts are almost identical to the low-rate shifts, further reinforcing the utility of the model.

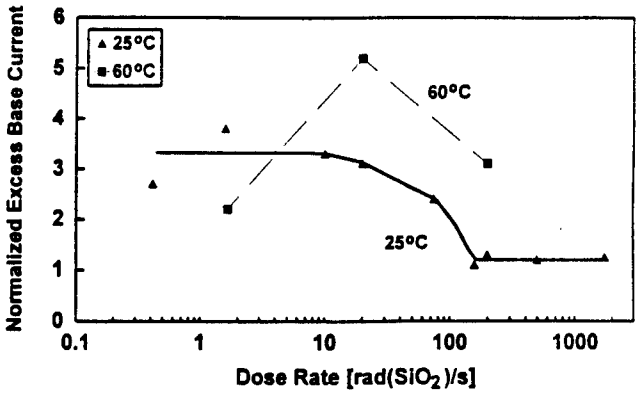


Fig. 11. Excess base current (normalized to preirradiation values) as a function of x-ray dose rate and irradiation temperature for ADI XFCB devices with 1.5 μm x 1.5 μm crystalline Si emitters irradiated to 100 krad(SiO_2) at 0 V bias.

B. BJTs.

Though the capacitor data of Fig. 10 are fairly convincing on their own, an even better test of the model of Fig. 9 is to see how real BJTs irradiated at 60°C compare to those irradiated at room temperature at varying dose rates. Though all of our capacitor data is more representative of the RBCMOS process, we show results here for XFCB transistors that have ~ 10-times thicker oxides overlying the emitter-base junction. We do this **(a)** because we have more BJT dose-rate data to show for comparison, and **(b)** to see whether model predictions made on the basis of screen oxides representing one process can be extrapolated to (still extremely soft) oxides in another technology. This comparison is shown in Fig. 11; the experiments and hardness-assurance implications are described further in Ref. [30]. Again, the 200 rad/s, 0-V x-ray irradiation at 60°C causes a ~ 3-times greater increase in excess base current (and hence in gain degradation, since the collector current is unaffected) than room-temperature irradiation, consistent with the capacitor results in Fig. 10. At 20 rad/s, the excess base current is even greater. But, at 1.7 rad/s, significant annealing or compensation [35,42,53] of holes in deep traps also occurs during the higher-temperature irradiations, reducing the excess base cur-

rent. Still, the results of Fig. 11 strongly reinforce the model presented above, and suggest that increasing the temperature to ~ 60°C during higher-rate irradiation may be a viable way to simulate low-rate gain degradation for some bipolar/BiCMOS devices and ICs.

Preliminary results on RBCMOS transistors also show enhanced gain degradation at 60°C (though by only ~ 20-40%, instead of the factor-of-three enhancement in gain degradation for XFCB devices in Fig. 11), consistent with the trends observed in Figs. 10 and 11. Obviously, it would also be useful to try to extend these results to microcircuits manufactured in these and other modern bipolar and BiCMOS technologies. This would allow the general applicability of the physical model developed here to be evaluated, and to see whether irradiating bipolar and BiCMOS devices at elevated temperatures could be an effective hardness assurance tool for space systems [30]. We note that, based on this work, Johnston et al. recently irradiated bipolar devices with substrate PNPs at 60°C at high rates. They find that the high rate response is significantly degraded at elevated temperature [11], again helping to support the model presented above. Figure 11 illustrates that annealing and charge compensation effects must be considered carefully in choosing appropriate temperature and dose rates via characterization testing in support of using elevated temperature irradiation as part of a hardness assurance program for space. Nevertheless, Figs. 10 and 11 represent the first time that bipolar low-rate response has been successfully simulated in the low-dose regime [38] with high-rate irradiation.

VIII. Summary and Conclusions

We have developed the first physical model of the mechanisms responsible for enhanced low-rate gain degradation in bipolar devices. Detailed capacitance-voltage and thermally-stimulated-current measurements on capacitors simulating bipolar screen oxides suggest the presence of slowly transiting or metastably trapped holes (e. g., in E_δ' centers) in the bulk of the screen oxides, consistent with recent EPR studies [23,47]. These act in tandem with more deeply trapped holes near the Si/SiO_2 interface to reduce the charge yield in the bulk of the oxide and increase the number of compensated holes in the oxide above the emitter-base junction. Strong corroborative evidence for this model was provided by capacitor and BJT studies. In these studies it was found that, in contrast with nearly all previous MOS experience (albeit mostly on much harder oxides and higher oxide electric fields), raising the temperature of the devices to 60°C during irradiation increases the net positive charge trapping in the oxide. This occurs because the transport and/or annealing of the slowly transporting and/or metastably trapped holes that help to reduce the midgap shifts during higher-rate irradiation is accelerated. On the basis of a model prediction, we demonstrate for the first time that the use of modestly elevated-temperature can enable irradiation of (at least some types of) bipolar devices at dose rates typical of the MIL-STD range (50-300 rad(SiO_2)/s [8]) to simulate exposure at space-like dose rates [30].

The results obtained here also have potentially significant processing implications. If screen oxides can be developed that do not contain such large densities of deep hole traps (and/or delocalized hole centers), it is clear that **(a)** the radiation hardness of modern bipolar and BiCMOS devices could be significantly improved, and **(b)** testing for low-dose-rate applications could be made easier. Obvious areas to examine include changes in implant conditions and/or use of rapid thermal processing. Using a thinner oxide over the emitter-base junction also would be beneficial to its hardness. Of course, the resulting structures must still be compatible with the remainder of device processing, as a bullet-proof screen-oxide in a zero-yield process or sub-par circuit performance does not benefit anyone. Meanwhile, modestly elevated-temperature irradiation, low-dose-rate irradiation [9-11,30], and/or margin via over-testing [30,38] must be applied to qualify bipolar and BiCMOS devices showing enhanced gain degradation at low dose rates for space environments.

Acknowledgments

We thank W. L. Warren, R. A. B. Devine, M. R. Shaneyfelt, H. E. Boesch, A. H. Johnston, F. W. Sexton, and J. R. Schwank for stimulating discussions, and L. C. Riewe and S. C. Witczak for experimental assistance. This work was supported by the Defense Nuclear Agency's hardness assurance and basic mechanisms programs, by the Ballistic Missile Defense Organization through its Electronics MODIL (Manufacturing Operations Development and Integration Laboratory) Program, and by the Department of Energy through Contract No. DE-AC04-94AL85000. This effort would not have been possible without the early significant contributions to this effort by the late Ed Enlow, who is greatly missed by us all.

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Appendix

Appendix Table. Trapped charge due to holes and electrons, as well as C-V midgap shifts, for MOS capacitors irradiated with 10-keV x rays as a function of irradiation, anneal, and TSC bias for the data of Figs. 4-8. These irradiations and anneals were performed at room temperature. The anneal bias, if applicable, was equal to the irradiation bias. Values of Q_h and Q_e were estimated using Eqs. (1)-(3) (Refs. [26,31]).

Process Type (Fig. #)	Dose [krad (SiO_2)]	Rad Bias (V)	Dose Rate rad(SiO_2)/s	Anneal Time (h)	TSC Bias (V)	Q_h (pC)	Q_e (pC)	ΔV_{mg} (V)
ADI (4)	300	0	4.6	None	-15	1190	65	-5.5
ADI (4)	300	0	1000	None	-15	1060	170	-4.4
ADI (4)	300	0	1000	17	-15	940	180	-3.8
Soft SNL (5)	2000	0	31.7	None	-10	5240	3800	-1.36
Soft SNL (5)	2000	0	2000	None	-10	5000	3180	-1.75
Soft SNL (5)	2000	0	2000	17	-10	4450	3700	-0.76
Hard SNL (6)	1800	0	1000	None	-10	3240	2240	-1.5
Hard SNL (6)	1800	0	4.4	None	-10	3000	2660	-0.5
ADI (7)	50	+6	0.83	None	-10	680	125	-3.8
ADI (7)	50	+6	417	None	-10	890	135	-2.8
ADI (8)	50	-6	83	None	+10	-330	--	-0.76
ADI (8)	50	-6	0.77	None	+10	-280	--	-0.72

V.K. Comparison of Ionizing Radiation Induced Gain Degradation in Lateral, Substrate, and Vertical PNP BJTs

Comparison of Ionizing-Radiation-Induced Gain Degradation in Lateral, Substrate, and Vertical PNP BJTs

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Abstract

A comparison is presented of ionizing-radiation-induced gain degradation in lateral, substrate, and vertical PNPs. The dose-rate dependence of current gain degradation in lateral PNP BJTs is even stronger than the dependence previously reported for NPN BJTs. Various mechanisms are presented and their relative significance for gain degradation in the lateral, substrate, and vertical PNPs is discussed. A detailed comparison of the lateral and substrate PNP devices is given. The specific lateral and substrate devices considered here are fabricated in the same process and possess identical emitters. Even though these devices have identical emitters and undergo the same processing steps, the lateral devices degrade significantly more than the substrate devices.

I. Introduction

Bipolar junction transistors (BJTs) continue to play an important role in integrated-circuit technology. These bipolar circuits are important components in spaceborne electronic systems. In earlier digital bipolar technologies, the limiting factor for using BJTs in total-dose environments was typically excess leakage caused by trapped positive charge in the field oxide [1]. However, for many current bipolar linear technologies, the primary total-dose failure mechanism is reduction of the current gain (I_C/I_B). The effects of ionizing radiation on gain degradation in vertical bipolar junction transistors have been studied extensively [2-9]. Vertical NPN transistors studied in previous work [2-7] exhibit very significant gain degradation, particularly when they are irradiated at low dose-rates (less than about 10 rad(SiO_2)/s) [10]. In contrast, *vertical* PNP transistors are relatively hard to ionizing radiation [3-4]. However, recent papers have attributed failures of linear integrated circuits irradiated at low dose-rates to degradation of *lateral* PNP transistors [11-13]. In this work, the effects of ionizing radiation on vertical, lateral, and substrate PNP transistors are compared experimentally.

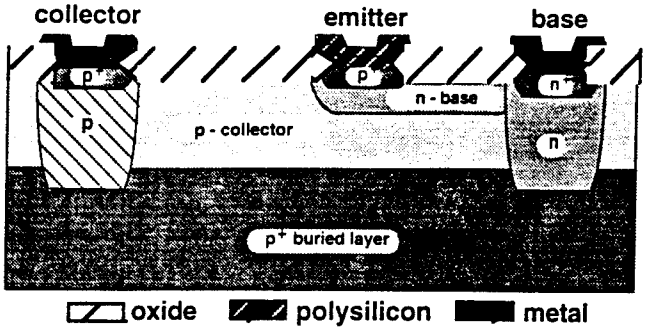
NPN BJTs have been studied extensively and may be used here as a frame of reference for the comparison of the PNP BJTs. Ionizing-induced gain degradation in the NPNs examined in [2-7] has been shown to be due to increased recombination in the emitter-base depletion region [2-7]. The increase in recombination is due to two mechanisms. First, interface states near midgap cause an increase in surface recombination velocity. Second, trapped oxide charge increases the surface potential which depletes the surface. Eventually, the condition is reached where the electron and hole concentrations are equal at the surface [7]. This condition, called the cross-over point, is where recombination is maximum. The cross-over point moves subsurface as positive oxide charge is added. The combined effect of these two mechanisms is a multiplicative combination of the individual effects. The excess base current increases rapidly as a function of the net charge in the oxide (approximately as $\exp(N_{ox}^2)$) and thus the oxide charge tends to dominate the radiation response [6-7].

In this work it is demonstrated that lateral PNP transistors can degrade severely at low total dose levels. For the devices considered here, the total dose required to degrade the lateral devices to half of their normalized current gain is 50 times less than that needed to observe the same current gain degradation in the vertical devices. Similarly, the total dose levels required to degrade the lateral devices to half of their normalized current gain is typically 20 times less than that needed to produce the same current gain degradation in the substrate devices. The lateral and substrate devices also exhibit strong dose-rate dependence of gain degradation such that as the dose-rate decreases, the current gain at a fixed total dose decreases. The lateral PNP transistor exhibits a stronger dose-rate dependence of current gain degradation than that previously reported in NPN transistors [2-4, 10].

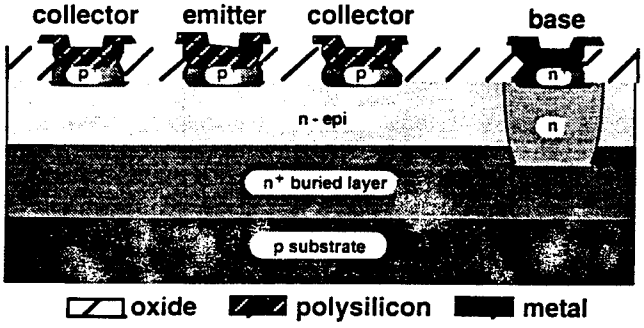
To assist in determining the cause of the ionizing-radiation-induced gain degradation in lateral PNP devices, the lateral PNP device examined in this work was modeled with processing and device simulation tools†. The simulations were coupled with experiments to examine the mechanisms responsible for the gain degradation. Figure 1 displays cross-sections and quantitative details for the vertical, lateral, and substrate PNP BJTs studied in this work.

Four mechanisms were identified as being responsible for the degradation: (1) depletion of the p-type emitter; (2) recombination at the base surface; (3) electron injection into the emitter; and (4) surface hole depletion. Each mechanism and its significance for each type of PNP transistor mentioned above is

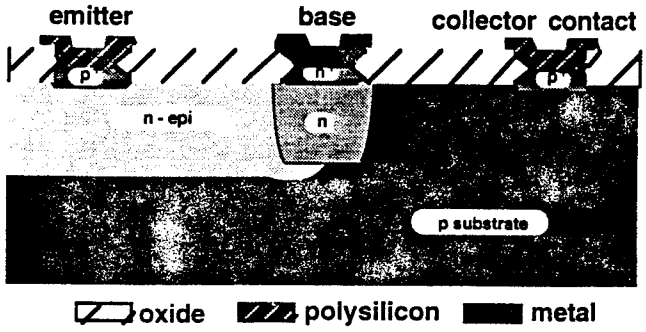
† Simulation tools provided by Silvaco, International



(a) VPNP



(b) LPNP



(c) SPNP

	XFCB VPNP	RF25 SPNP	RF25 LPNP
active base width (μm)	0.4	1.25	2.6
base surface doping (cm^{-3})	9.0×10^{17}	1.0×10^{16}	1.0×10^{15}
oxide thickness (nm)	545	600	600
nominal gain	70	100-150	20-40

Figure 1: Representative cross-sections of the (a) vertical (VPNP), (b) lateral (LPNP), and (c) substrate (SPNP) transistors.

examined. It is shown that these mechanisms are less significant in the vertical PNP than in the lateral and substrate PNP devices because the vertical structure has a heavily doped emitter and a vertical current flow pattern. The lateral PNP, however, is more significantly affected by recombination at the base surface and surface hole depletion than the vertical PNP, since the current flow pattern is lateral and directly under the oxide where radiation-induced charge is present. Even though the substrate and lateral PNP BJTs considered here have identical emitters, the lateral device exhibits more gain degradation and excess base current than the substrate device. The significant physical mechanisms responsible for current gain degradation of the lateral structure are determined from detailed comparison with the substrate device which shares the same emitter and fabrication process.

II. Experimental Details

Experiments were performed on development chips from Analog Devices, Incorporated, which include lateral and substrate devices. The results are compared with vertical devices from Analog Devices XFCB process [14]. The development process, RF25, features 25 GHz double polysilicon self-aligned NPN BJTs for RF and microwave applications, but no vertical PNP transistors [15]. Each RF25 test chip has two isolated lateral PNP transistors and a substrate PNP transistor which are the devices of interest here. One lateral PNP transistor has an emitter geometry of 1.2 μm x 1.2 μm and the other lateral PNP has five parallel emitters which are 1.2 μm x 1.2 μm each. The substrate PNP transistor has an emitter geometry of 1.2 μm x 1.2 μm.

Lateral and substrate PNP transistors from the RF25 process were irradiated with 10 keV X-ray and Co-60 sources. The dose-rates ranged from 0.01 rad(SiO_2)/s to 1670 rad(SiO_2)/s. Each packaged chip was irradiated with all terminals grounded. A preliminary experiment comparing devices irradiated with V_{EB} = -2V to devices irradiated with V_{EB} = 0 V indicated no appreciable differences. Device characterization for the lateral PNPs consisted of Gummel sweeps with the emitter grounded, the collector at -2V, the substrate at -3V, and the base voltage ranging from 0 to -1V. Device characterization for the substrate PNP consisted of Gummel sweeps with the base grounded, the collector at -2.5V, and the emitter voltage ranging from 0 to 1V. The common dose-rate of 1.8 rad(SiO_2)/s was used for comparison of the two sources. Capacitors from the RF25 process were also irradiated in order to examine the charge trapping properties of the oxide that lies above the base in the lateral and substrate BJTs. These capacitors were irradiated with a 10 keV X-ray source at dose-rates ranging from 0.83 to 355 rad(SiO_2)/s up to a total dose of 200 krad(SiO_2). The capacitors were grounded during irradiation.

The vertical PNP used for comparison in this work is from Analog Devices XFCB process. It was necessary to use a vertical device from a different process because the RF25 process includes only lateral and substrate devices. The vertical devices were irradiated with a 10 keV X-ray source [4]. The dose-rates were 111, 158, and 1667 rad(SiO_2)/s up to a total dose of 500 krad(SiO_2).

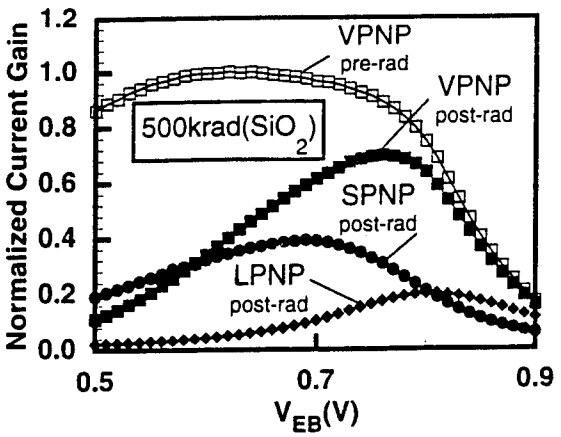


Figure 2: Normalized current gain, β, vs. V_{EB} for lateral (LPNP), substrate (SPNP), and vertical (VPNP) transistors for a total dose of 500 krad(SiO_2). Dose rate for VPNP device is 158 rad(SiO_2/s and for the LPNP and SPNP devices is 167 rad(SiO_2/s.

III. Experimental Results

III. A. Gain Degradation

The current gain, defined as $\beta = I_C/I_B$, where I_C is the collector current and I_B is the base current, is plotted vs. emitter-base voltage (V_{EB}) in Fig. 2 for the RF25 lateral and substrate PNP transistors and for a vertical PNP transistor from the Analog Devices XFCB process. The devices illustrated here received a total dose of 500 krad(SiO_2). For each device, the current gain has been normalized by the pre-irradiation maximum current gain for that particular device. The vertical PNP transistor exhibits the least gain degradation, while the lateral transistor exhibits the most degradation. The reduction in the current gain is most pronounced at low bias levels for all transistor types.

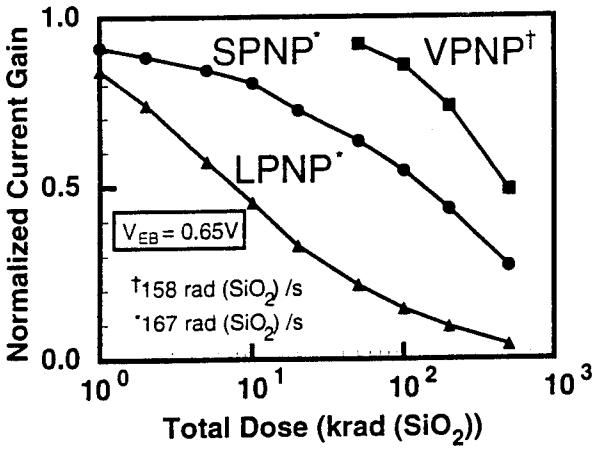


Figure 3: Normalized current gain, β, vs. total dose for lateral (LPNP), substrate (SPNP), and vertical (VPNP) transistors at dose rates of 167 rad(SiO_2)/s and 158 rad(SiO_2)/s.

Figure 3 shows normalized current gain vs. total dose for the three device types. The effect of total dose on the three devices at similar dose-rates and a fixed value of current gain degradation may be compared. If the current gain degradation for comparison is chosen to be one half of its original value, then Fig. 3 shows that the total dose required to produce this degradation for the lateral, substrate, and vertical transistors is approximately 7, 150, and 500 krad(SiO_2), respectively. Thus, for similar dose-rates, the total dose levels required to degrade the lateral devices to one half of their normalized current gain is about 50 times less than that needed to observe current gain degradation of the same extent in the vertical devices. For similar dose-rates, the total dose level required to degrade the lateral devices to one half their normalized current gain is as much as 20 times less than that needed to observe current gain degradation of the same extent in the substrate devices.

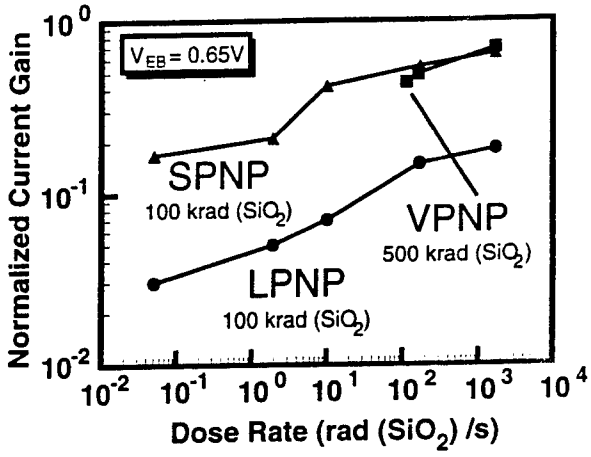


Figure 4: Normalized current gain, β, vs. dose rate for lateral (LPNP), substrate (SPNP), and vertical (VPNP) transistors. The total dose for the LPNP and SPNP devices was 100 krad(SiO_2), and the total dose for theVPNP device was 500 krad(SiO_2).

The lateral, substrate, and vertical devices not only show a dependence upon total dose, they also display a significant dose-rate dependence. The dose-rate dependences of the lateral, substrate, and vertical PNP transistors are illustrated in Fig. 4 where normalized β vs. dose-rate is plotted. The data point at 0.05 rad(SiO_2)/s was obtained by using Co-60 as the irradiation source, while all the other data points were obtained with an X-ray irradiation source. The Co-60 to X-ray correlation was completed at a common dose-rate of 1.8 rad(SiO_2)/s as illustrated in Fig. 5 where the total dose is 100 krad(SiO_2). Figures 5(a) and 5(b) illustrate that the Co-60 source produces greater current gain degradation, or equivalently, greater excess base current ($\Delta I_B = I_B - I_{Bo}$, where I_{Bo} is the pre-irradiation base current and I_B is the post-irradiation base current) than the X-ray source. The excess base current in Fig. 5(b) for the Co-60 irradiation is 2.73 times greater than that for the X-ray irradiation at V_{EB} = 0.7 V. This X-ray to Co-60 comparison agrees with previous results for thick oxides irradiated at low electric fields [16].

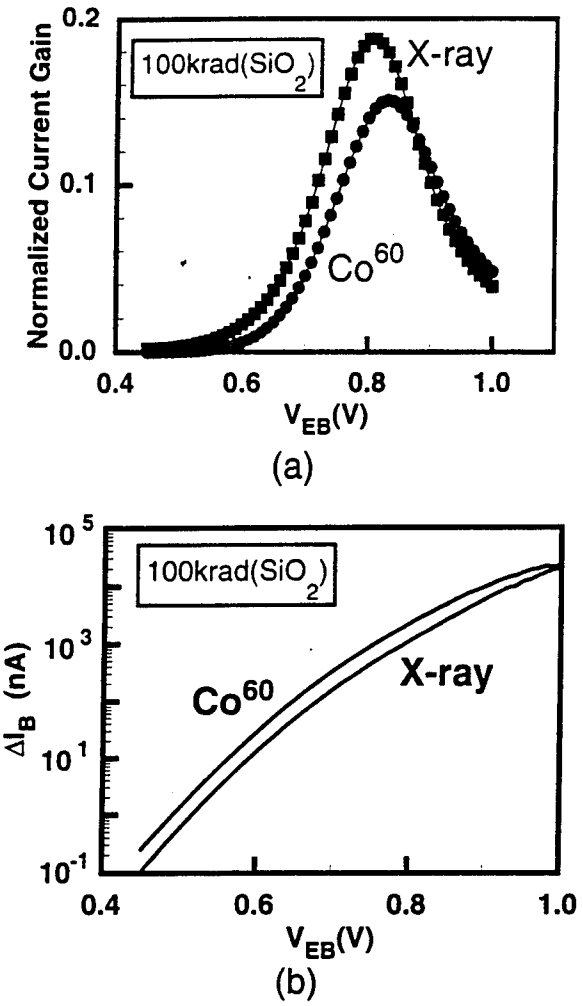


Figure 5: (a) Normalized current gain, β, versus V_{EB} for the LPNP at a dose rate of 1.8 rad(SiO_2)/s to a total dose of 100 krad(SiO_2). (b) Excess base current versus V_{EB} for the LPNP at a dose rate of 1.8 rad(SiO_2)/s to a total dose of 100 krad(SiO_2).

Therefore, the Co-60 data in Figs. 4 and 10 were multiplied by a factor of 2.73 to allow direct comparison between Co-60 and X-ray data. In Fig. 4, the total dose for the lateral and substrate PNPs is 100 krad(SiO_2) and for the vertical PNP is 500 krad(SiO_2). Note that if the total dose for the vertical device were 100 krad(SiO_2), the vertical dose-rate curve would lie above the substrate PNP curve due to the total dose effect explained above. The 500 krad(SiO_2) curve is, however, sufficient to illustrate the dose-rate trend. As the dose-rate decreases, the gain degradation of all three types of PNP BJTs increases, however, the lateral PNP shows the greatest degradation.

III. B. Excess Base Current

The gain degradation in the lateral device results from a combination of increased base current (I_B) and slightly decreased collector current (I_C). In the vertical PNP transistor, on the other hand, gain degradation results almost exclusively from increased base current. Figure 6 displays the Gummel plots (log I_C and log I_B vs. V_{EB}) for a dose-rate of 167 rad(SiO_2)/s and a total dose of 500 krad(SiO_2) for the lateral PNP device. The Gummel plot in Fig. 6 is separated for clarity into the pre-rad and post-rad base current in 6(a) and the pre-rad and post-rad collector current in 6(b). The collector current in the lateral PNP changes only slightly with respect to the base current. Figures 7(a) and 7(b) show Gummel plots at dose-rates of 167 rad(SiO_2)/s and 158 rad(SiO_2)/s for the substrate and vertical devices, respectively. The total dose for each plot is 500 krad(SiO_2). Only the base current portions of the Gummel plots are presented for the substrate and vertical PNPs since, relative to the base current, the collector current does not show an appreciable change as a function of total dose.

The ideality factor, n, is related to the base current through the following relationship :

$$I_B \propto exp\left(\frac{qV}{nkT}\right)$$

where V is the applied voltage and kT/q is the thermal voltage. The ideality factor may be extracted from the plot of ln(I_B) vs. V_{EB} as shown in Fig. 8. For reference, line segments

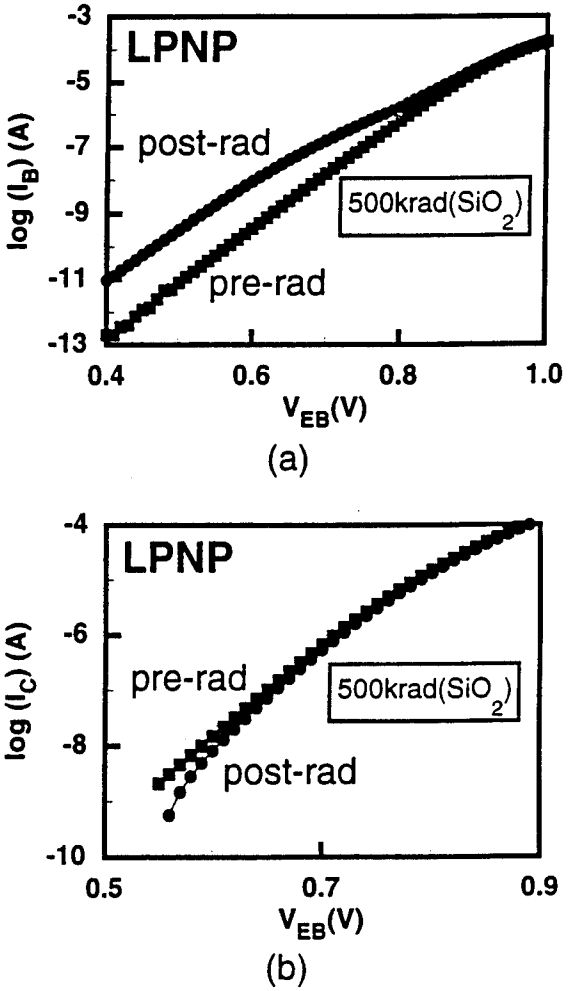


Figure 6: Gummel plots ((a) log I_B and (b) log I_C vs. V_{EB}) for the LPNP at a dose rate of 167 rad(SiO_2)/s to a total dose of 500 krad(SiO_2).

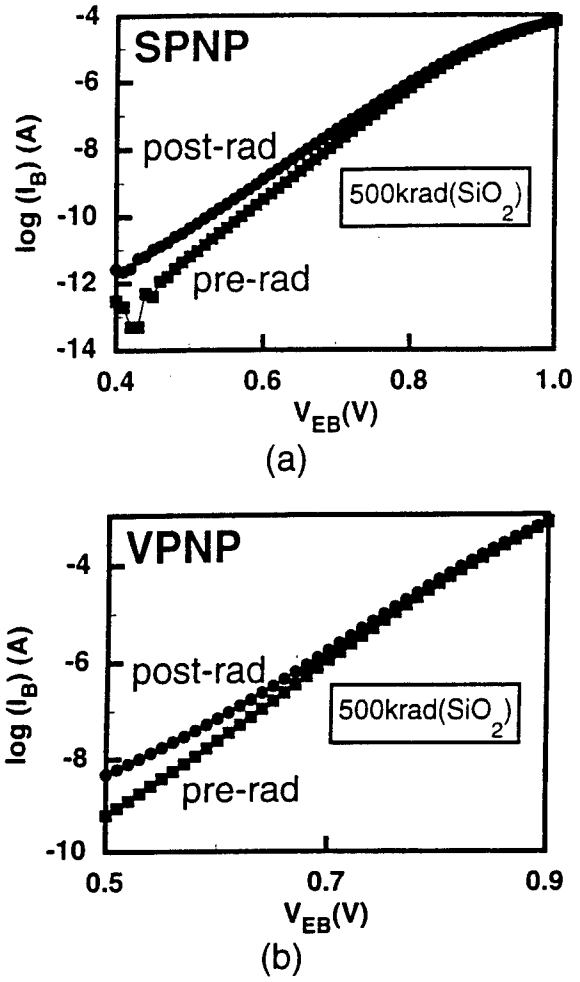


Figure 7: Gummel plots (log I_n vs. V_{EB}) for the (a) SPNP at a dose rate of 167 rad(SiO_2)/s and (b) the VPNP at a dose rate of 158 rad(SiO_2)/s to a total dose of 500 krad(SiO_2).

respresenting ideality factors of one and two have been included. For $V_{EB} < 0.7$ V, the excess base current exhibits $1 < n < 2$. For $V_{EB} > 0.7$ V, the excess base current displays $n = 2$. These two distinct regions of ideality factors are similar to that observed in previous work with NPN transistors [5-7]. For NPN devices, an ideality factor between one and two signifies surface recombination and an ideality factor of two indicates the recombination peak is beneath the surface [5-7].

Examining the base current of these devices more closely, Fig. 9 displays the normalized excess base current ($\Delta I_B/I_{Bo} = (I_B - I_{Bo})/I_{Bo}$, where I_{Bo} is the pre-irradiation base current and I_B is the post-irradiation base current) vs. total dose for the three types of devices. On comparing the curves in Fig. 9, the increase in I_B is observed to be much smaller in the substrate and vertical devices than in the lateral device. At 500 krad(SiO_2), the lateral device exhibits an excess base current approximately 50 times greater than the vertical device which represents the majority of the gain degradation seen in Fig. 3. In Fig. 10, which displays normalized excess base current vs. dose rate, the data point at 0.05 rad(SiO_2)/s was obtained with a Co-60 irradiation

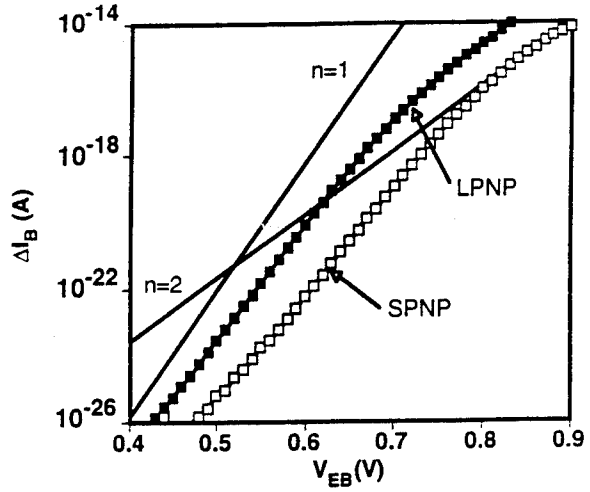


Figure 8: Ideality factor of LPNP and SPNP. Dose rate is 1670 rad(SiO_2)/s, and total dose is 100 krad(SiO_2). Straight line segments represent ideality factors of 1 and 2 for reference.

source, while all the others were obtained with an X-ray irradiation source.

III. C. Radiation-Induced Charge Density

In these devices, gain degradation, or equivalently, excess base current, is a result of trapped positive oxide charge density (N_{ot}) and interface charge density (N_{it}) in the oxide which covers the emitter base junction. Therefore, capacitors from the RF25 process were irradiated to study the effects of ionizing radiation on N_{ot} and N_{it} within the oxide [17]. The capacitors were irradiated with zero bias at various dose-rates and the voltage shifts after exposure to ionizing radiation were measured. The midgap voltage shift, ΔV_{MG}, was used to obtain radiation-induced oxide trapped charge, ΔN_{ot}, and excess interface trapped charge, ΔN_{it}. Figure 11 is a plot of ΔN_{ot} and ΔN_{it} vs. dose-rate.

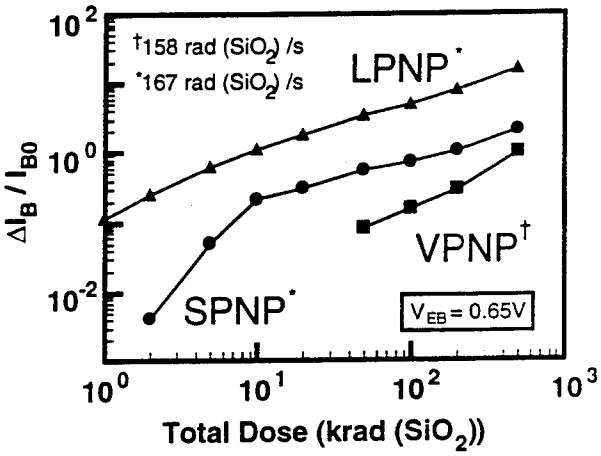


Figure 9: Excess base current, $\Delta I_B/I_{Bo}$, versus total dose for the LPNP, SPNP, and VPNP transistors at dose rates of 167 rad(SiO_2)/s and 158 rad(SiO_2)/s.

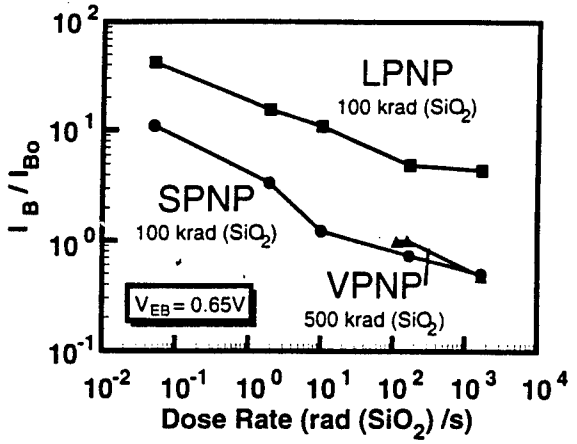


Figure 10: Excess base current, $\Delta I_B/I_{Bo}$, versus dose rate for the LPNP, SPNP, and VPNP transistors. The Co-60 data at 0.5 rad(SiO_2)/s has been reduced by the factor 2.73 for comparison with the X-ray data.

As dose-rate decreases, both ΔN_{ot} and ΔN_{it} increase. Figure 11 displays the same general trend in dose-rate as in Fig. 4, illustrating that current gain degradation in these devices is consistent with the presence of more radiation-induced oxide charge density and interface traps at lower dose-rates.

IV. Degradation Mechanisms

IV. A. NPN Degradation Mechanisms

Physical mechanisms responsible for ionizing-radiation-induced gain degradation in NPN BJTs have been studied extensively [2-7]. Current gain degradation has been attributed to an increase in recombination current which results in excess base current. There are two mechanisms responsible for increased recombination current in NPN BJTs. First, the formation of interface traps at the Si/SiO_2 interface which covers the emitter-base junction results in increased surface recombination velocity. Second, net positive charge accumulated in the oxide above the emitter-base junction causes the field induced depletion layer to expand into the p-type base. The p-type base in the NPN BJT is lightly doped with respect to the p-type emitter in the PNP BJTs considered here. Therefore, depletion of the p-type region will be a more significant mechanism in the current gain degradation of NPN BJTs than in the PNP BJTs in this work. Of the two mechanisms responsible for increased recombination current in NPN BJTs, positive oxide charge is the dominant mechanism [2-6]. Oxide charge dominates since it increases the recombination rate as $\exp(N_{ox}^2)$ when the surface is depleted before eventually saturating [5-6].

IV. B. PNP Degradation Mechanisms

Cross-sections of the vertical, lateral, and substrate devices, respectively, were shown previously in Fig. 1. The lateral PNP devices were modeled with SPISCES using the actual RF25 fabrication process. The lateral devices presented in this work are different from typical lateral devices because they have heavily doped p-type emitters. The lateral PNPs considered here have an emitter doping at the surface on the order of $1.0x10^{19}$ cm^{-3}, whereas typical lateral PNPs fabricated in older processes typically have an emitter doping at the surface on the order of $1.0x10^{15}$ to $1.0x10^{16}$ cm^{-3} [18]. The difference between the lateral PNP transistors studied in this work and older lateral PNP processes is in the formation of the emitter. The emitter of the lateral PNP studied in this work is formed from a p^+-polysilicon diffusion used to form the base contact of the NPN BJT. Since the p^+-polysilicon is used as a contact, the polysilicon is doped very heavily, resulting in a heavily doped p-type emitter when diffused into the silicon. Alternatively, in older processes, the lateral PNP emitter was formed from the base diffusion of vertical NPN transistors.

For each of the three types of PNP BJTs, there are four possible mechanisms which may cause current gain degradation. They are: (1) depletion of the p-type emitter; (2) recombination at the base surface; (3) electron injection into the emitter; and (4) surface hole depletion.

The first mechanism, depletion of the p-type emitter, is illustrated in Fig. 12(a). Upon exposure to ionizing radiation, positive charge accumulates in the oxide over the emitter-base junction. The trapped positive oxide charge repels holes in the p-type emitter and also accumulates the base, resulting in the depletion region spreading into the emitter along the surface. The depletion of the surface increases the recombination (as in the base of NPN BJTs), which results in an excess base current. This mechanism is most significant for lightly doped emitters such as those found in typical lateral PNPs fabricated in older processes. However, the emitter of the lateral PNP studied in this work is a heavily doped p-type emitter. Therefore, depletion of the emitter is not very great in the lateral devices considered here since the depletion region cannot spread very far into the heavily doped emitter. This mechanism is also small in the vertical and substrate devices since they both typically have heavily doped emitters. However, this may be a significant mechanism in other technologies.

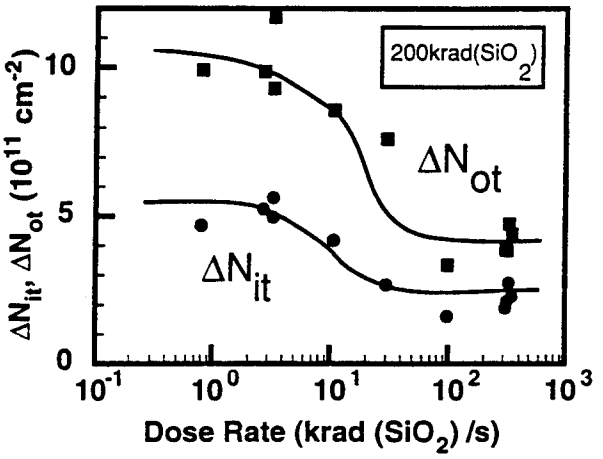


Figure 11: Change in number density of oxide trapped charge, ΔN_{ot}, and interface traps, ΔN_{it}, in test capacitors representative of the oxide above the base-emitter junction in the LPNP transistors.

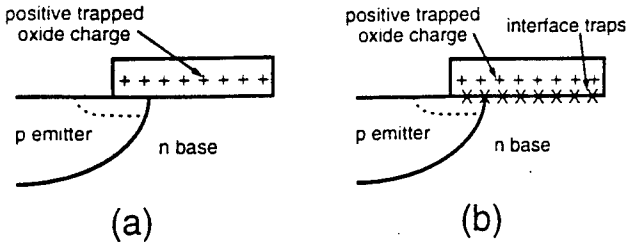


Figure 12: Illustration of positive trapped oxide charge (a and b) and interface traps (b) over the emitter-base junction and the resulting expansion of the depletion region into the emitter region.

The second mechanism for gain degradation in PNP BJTs is increased recombination at the n-type base surface. In this case, interface traps, schematically illustrated in Fig. 12(b), increase the current gain degradation. The interface traps cause the recombination velocity along the base surface to increase. However, the trapped positive oxide charge accumulates the base surface leading to a condition of a relatively low recombination rate at the surface since recombination is maximum when the electron and hole magnitude is equal. These are competing effects and it is impossible to identify the dominant effect without further modeling.

The discussion of the two remaining mechanisms utilizes SPISCES simulations. Simulations of the lateral PNP assume Shockley-Read-Hall recombination using concentration dependent lifetimes, and a concentration dependent mobility model. The lateral device was biased with the emitter grounded, the base at -0.65 V, the collector at -2.0 V, and the substrate at -3.0 V. Radiation-induced damage to the device is simulated by defining an areal density of charges in the oxide. The magnitude of the density of charges is defined to be $2x10^{12}$ cm^{-2}, which is on the same order as that obtained through experimental measurements as shown in Fig. 11. Surface recombination velocity is defined to be proportional to the inverse of the effective electron and hole lifetimes. As midgap traps increase, the effective lifetimes decrease, which results in an increase in surface recombination velocity.

The third mechanism is enhanced electron injection into the emitter. Positive oxide charge trapped in the oxide over the emitter-base junction accumulates the surface of the base. Accumulation of the base locally converts the emitter-base junction from a p^+-n junction to a p^+-n^+ junction. When a forward bias is applied to the junction, holes will be carried from the p-type emitter to the n-type base and electrons will be carried from the n-type base to the p-type emitter. However, since the base is accumulated, there now exist many more electrons which may be injected into the emitter, resulting in excess base current. Figure 13 is an SPISCES generated plot displaying the magnitude of the electron current density at the cutline shown in the corresponding lateral structure. Fig. 13 shows that with no net oxide charge present, the magnitude of the electron current density at the left end of the cutline, directly under the emitter-base metallurgical junction, is 0.7 A/cm^2. As the cutline is traversed to the right, away from the emitter, the magnitude of the electron current density falls to zero. Conversely, the curve which plots electron current density with charge present in the oxide ($2x10^{12}$ cm^{-2}) shows that as the cutline is traversed to the right, the magnitude of the electron current density increases from 0.7 A/cm^2 to a maximum of nearly 2 A/cm^2. This illustrates an increase of base current due to back-injected electrons.

The last mechanism to be discussed is related to the path followed by the holes injected into the base. As positive oxide charge increases, holes are driven away from the surface. As the holes are forced deeper into the structure, the path that the holes must travel to reach the collector becomes longer, in effect, making the base appear longer. A longer base gives the holes more opportunity to recombine before they reach the collector. Also, the recombination rate increases due to the holes traveling toward the n^+ buried layer. The lifetime of the holes is decreased since the holes are pushed to an area of heavier doping resulting in increased recombination. Figure 14 is an SPISCES generated plot showing the magnitude of the hole current density at the cutline shown in the corresponding lateral structure. The curve which represents hole current density with no net oxide charge, shows that directly under the Si/SiO_2 interface, at 0μm along the cutline, the magnitude of the hole current density is approximately 120 A/cm^2. The curve which represents hole current density with net density of charge in the oxide of $2x10^{12}$ cm^{-2} demonstrates that the holes are forced away from the surface, since at the same cutline position as above, the magnitude of the hole current density is 0 A/cm^2. Also notice that the peak of the hole current density has shifted approximately 0.2 μm below the surface when charge is present in the oxide. This demonstrates that the holes are forced subsurface and must travel a longer path when net oxide charge is present. This decrease in hole current density, or equivalently collector current density, was illustrated in Fig. 6(b) for the lateral PNP BJT. even though the change in collector current was shown to be much smaller

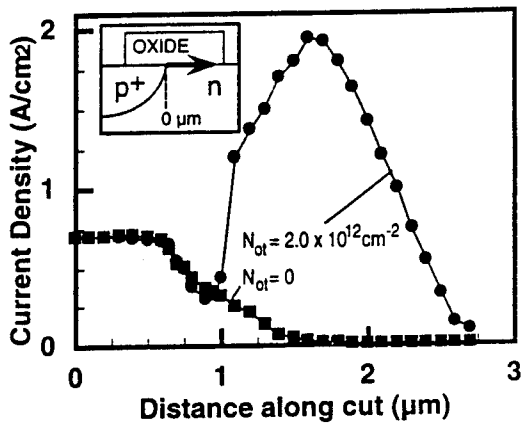


Figure 13: SPISCES simulation of *electron* current density near the base-emitter junction that shows effect of excess base current due to back-injected electrons. The cut-line (represented by the arrow) is just under the $Si-SiO_2$ interface below the base-emitter junction with the origin at the junction (see graph inset and Fig. 1).

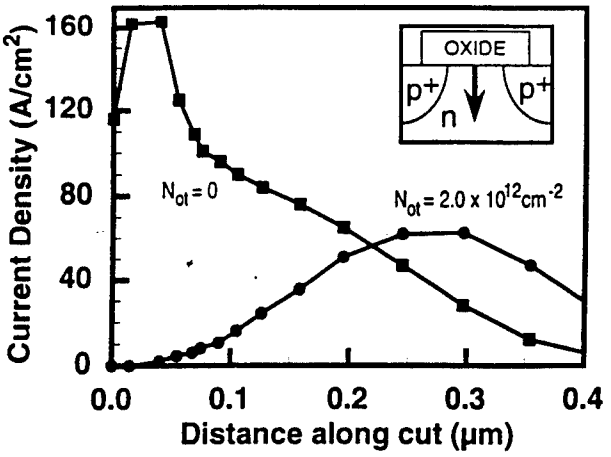


Figure 14: SPISCES simulation of *hole* current density midway between the base-emitter and base-collector junctions at the Si-SiO_2 interface. This illustrates how N_{ot} alters the path injected holes must travel en route to the collector. The origin of the cut-line (represented by the arrow) is at the Si-SiO_2 interface (see graph inset and Fig. 1).

than the change in base current for the lateral PNP. Although, the movement of holes with charge present contributes to excess base current. As holes are forced away from the surface, recombination is increased which results in excess base current.

IV. C. Lateral/Substrate/Vertical PNP Comparison

Due to their differing structures, each of the three PNP BJTs is affected by the mechanisms discussed above to differing degrees. The vertical and substrate PNPs have similar structures, but a very different structure than that of the lateral PNP. Since the substrate and lateral devices considered in this work were fabricated in the same process and have identical emitters, the comparison will focus on the differences in the ionizing-radiation-induced degradation mechanisms of the lateral and substrate devices. The vertical and substrate PNPs may be treated in the same way in these comparisons due to their similar structures.

If the lateral and substrate devices considered here share identical emitters, then why does the lateral device suffer more severe current gain degradation when exposed to ionizing radiation? The answer lies in the differing active base regions of the devices.

In the substrate PNP, the active base lies under the p-type emitter, resulting in the current traveling vertically. Therefore, surface effects such as recombination at the surface and surface hole depletion are minimized. The only current within the vertical structure which may be affected by the surface mechanisms mentioned above is the current which flows laterally from the sides of the emitter. The small influence of these mechanisms on the substrate PNP makes this device relatively hard to ionizing radiation. Also, depletion of the p-type emitter and electron injection into the emitter do not produce large amounts of degradation since the emitter is heavily doped.

For the lateral PNP device, the active base region is the portion of the base which lies between the p-type emitter and collector, resulting in current flowing laterally along the surface. The surface mechanisms, such as recombination at the base surface and surface hole depletion, which were not as great in the substrate device above, play much more significant roles in the lateral device. As holes travel laterally along the base from emitter to collector, they may be lost to recombination at the surface or may be pushed away from the surface. If the holes are forced away from the surface, they suffer a greater probability of recombining, since the path that they travel becomes longer and the depth to which they travel is a region of lower lifetime as shown in section IV.B. above. These two significant mechanisms combined make the lateral PNP suffer much more severe gain degradation than the substrate PNP. Depletion into the emitter and electron injection into the emitter are comparable for all the device types.

V. Summary

The effects of ionizing radiation on lateral and substrate PNP structures are different from the effects on vertical PNP structures. Of the three PNPs considered here, the current gain of the lateral PNP suffers the most current gain degradation while the vertical suffers the least current gain degradation due to ionizing-radiation. As the dose-rate decreases, the current gain decreases as a result of more trapped positive oxide charge and interface charge present in the oxide at lower dose-rates. The current gain degradation in the lateral, substrate, and vertical devices is mainly due to excess base current However, in the lateral PNP, a second order contributor to current gain degradation is present in that the collector current decreases slightly.

Experiment and simulation were coupled to provide insight into the physical mechanisms for ionizing-radiation-induced gain degradation in the lateral, substrate, and vertical PNPs. Four mechanisms were examined in detail. The lateral and substrate devices were compared since these two devices were fabricated in the same process and have identical emitters. Current gain degradation is more severe in the lateral PNP than in the substrate PNP due to the structure of the lateral device. In the lateral device, current flow is along the surface, and is affected by surface mechanisms, such as recombination at the surface and surface hole depletion. These surface effects lengthen the current path in the lateral device as holes are forced away from the surface. The substrate device, on the other hand, is harder to radiation due to the current flowing vertically through the device. The path of the vertical current flow is unaffected by the surface mechanisms which affect the lateral device.

Acknowledgments

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V.L. Hardness Assurance Issues for Lateral PNP Bipolar Junction Transistors

Hardness-Assurance Issues for Lateral PNP Bipolar Junction Transistors*

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Abstract

The dose-rate dependence of gain degradation in lateral PNP transistors is even stronger than the dependence previously reported for NPN BJTs. In this work, several hardness-assurance approaches are examined and compared to experimental results obtained at low dose rates. The approaches considered include irradiation at high dose rates while at elevated temperature and high-dose-rate irradiation followed by annealing. The lateral PNP transistors continue to degrade during post-irradiation annealing, in sharp contrast to NPN devices studied previously. High-temperature conditions significantly increase the degradation during high-dose-rate irradiation, with the amount of degradation continuing to increase with temperature throughout the range studied here (up to 125°C). The high-temperature degradation is nearly as great as that observed at very low dose rates, and is even greater when differences between ^{60}Co and x-ray irradiation are accounted for. Since high-temperature irradiation has previously been shown to enhance the degradation in NPN transistors, this appears to be a promising hardness-assurance approach for bipolar integrated circuits. Based on these results, preliminary testing recommendations are discussed.

I. Introduction

Early failure of analog integrated circuits irradiated at low dose rates has recently been attributed to current gain degradation of lateral PNP transistors (LPNPs)[1-3]. The LPNP is commonly used as an input device, active load, or current source in operational amplifiers, voltage regulators, comparators, A/D converters, and other analog ICs. This paper critically examines several hardness-assurance approaches for LPNPs irradiated at space-like dose rates.

When bipolar devices are exposed to ionizing radiation, oxide trapped charge accumulates in the oxides that cover the device surface. In addition, near-midgap states generated at the Si/SiO_2 interface increase the effective surface recombination velocity. These effects have been studied extensively in NPN transistors, where they combine to cause an increase in the base current, resulting in a reduction in DC current gain [4-9]. The current gain degradation in some NPN devices depends strongly on the dose rate—lower dose rates result in greater gain degradation. This dose-rate dependence and the inability of high-rate irradiation and anneal tests to simulate low-rate response [4,7] present challenges in devising hardness-assurance methods for analog ICs containing NPN bipolar transistors. It has been suggested, however, that irradiation at elevated temperature may provide a reasonable estimate of low-dose-rate response [10].

In this work, we examine hardness-assurance issues for lateral PNP transistors. The approaches considered include irradiation at high dose rates while at elevated temperature and high-dose-rate irradiation followed by annealing. As in NPN devices, high-temperature significantly increases gain degradation during high-dose-rate irradiation. The high-temperature degradation is nearly as great as that observed at very low dose rates (and is even greater when source differences are accounted for), which suggests that this is a promising hardness-assurance approach for bipolar integrated circuits. The results obtained from the lateral PNP transistors are compared to those for vertical NPN and substrate PNP transistors fabricated in the same technology. The lateral PNP transistors continue to degrade during post-irradiation annealing, in sharp contrast to NPN devices studied previously. However, degradation during post-irradiation annealing is not as great as that produced by high-temperature irradiation.

II. Experimental Procedure

Experiments were performed at the University of Arizona and Sandia National Laboratories. Transistors from the same wafer lot were tested in all experiments. The transistors tested were from a development version of the Analog Devices, Inc. ADRF process [11]. A cross section of the LPNP device is shown in Fig. 1. The thickness of the oxide covering the base region is 600 nm.

Each twenty-eight-pin DIP package contained five bipolar devices: two LPNPs, one substrate PNP, and two vertical NPNs. The LPNPs exhibit the most degradation, so the experiments

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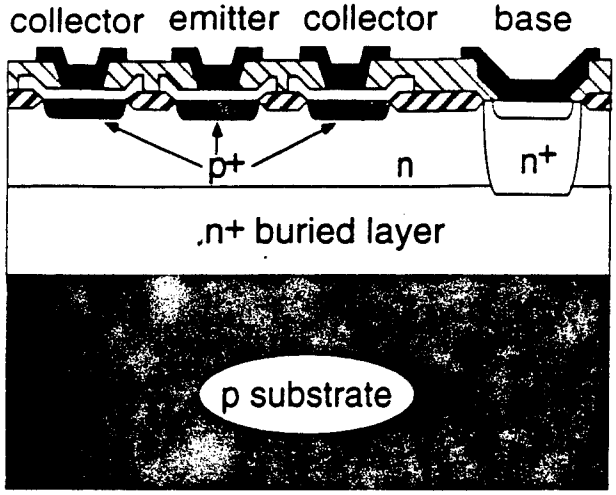


Fig. 1 Cross section of lateral PNP device from development version of Analog Devices ADRF technology.

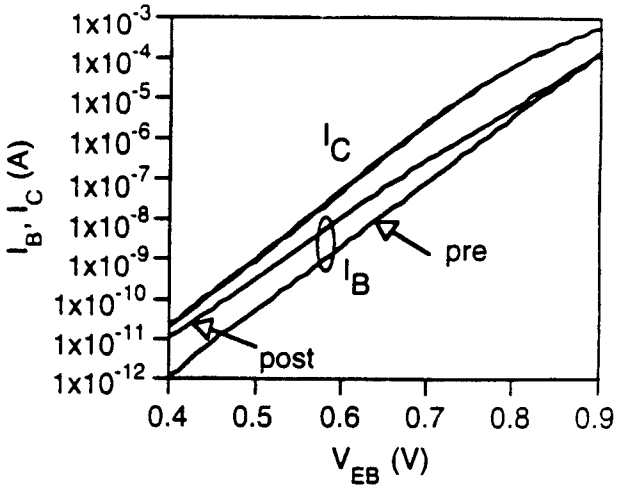


Fig. 2 Pre-irradiation and post-irradiation Gummel plots for a lateral PNP device irradiated to a total dose of 100 krad(SiO_2) at a dose rate of 167 rad(SiO_2)/s.

focused on understanding their response. However, the other device types were characterized and compared to the LPNPs. Device terminals were grounded during irradiation for all the results reported here, since negligible irradiation-bias dependence was observed in preliminary experiments during which devices also were irradiated with a reverse bias of –2 V on the emitter-base junction.

The experiments at Sandia National Laboratories were performed using a 10 keV ARACOR 4100 semiconductor x-ray radiation source. Devices were irradiated at 1.8, 10, 70, and 167 rad(SiO_2)/s. Additional devices were irradiated to a total dose of 100 krad(SiO_2); the irradiation temperature ranged from room temperature to 125°C. Some of the irradiated devices were subjected to isochronal annealing at temperatures ranging from room temperature to 125°C. At each temperature, the devices were annealed for 30 minutes.

Low-dose-rate tests were conducted at the University of Arizona using a ^{60}Co room source at dose rates of 0.01, 0.05, and 0.1 rad(SiO_2)/s, and in a ^{60}Co sealed pit source at a dose rate of 1.8 rad(SiO_2)/s. The highest total dose for these tests was 100 krad(SiO_2). The x-ray and ^{60}Co sources were compared using results from the 1.8 rad(SiO_2)/s irradiations conducted in the x-ray source at Sandia National Laboratories and the ^{60}Co source at the University of Arizona. Devices were unlidded during these tests, and dosimetry was similar to that described in previous work [12].

Device characterization for the LPNPs consisted of Gummel sweeps with the emitter grounded, the collector at –2 V, the substrate at –3 V, and the base voltage ranging from 0 to –1 V.

III. Results

III.A. Excess Base Current

Figure 2 shows pre-irradiation and post-irradiation Gummel plots (log (I_B and I_C) vs. V_{EB}) for a lateral PNP device that was irradiated to a total dose of 100 krad(SiO_2) at a dose rate of 167 rad(SiO_2)/s, where I_B is the base current, I_C is the collector current, and V_{EB} is the emitter-base voltage. Figure 3 shows the normalized current gain, β/β_0, vs. V_{EB} for the device of Fig. 2 and also for another device irradiated to a total dose of 100 krad(SiO_2) at a dose rate of 0.05 rad(SiO_2)/s. The current gain, β, is defined as the ratio of collector current to base current, I_C/I_B, and β_0 is the peak pre-irradiation current gain. In these devices, the gain degradation is significantly worse at low dose rates. Some of the increased degradation at low dose rates is due to a difference in initial charge yield for x-ray and ^{60}Co irradiations, as discussed below. However, this difference is sufficient to explain only a portion of the dose-rate effect illustrated here.

The gain degradation is primarily due to the presence of increased base current in irradiated devices, although there is also a small amount of reduction in the collector current that is not visible in Fig. 2. The excess base current, $\Delta I_B = I_B - I_{B0}$, is plotted vs. V_{EB} in Fig. 4 for the same devices considered in Fig. 3, where I_{B0} is the pre-irradiation base current. This quantity will serve as a convenient metric in comparing the different radiation and anneal conditions described above.

III.B. X-Ray–^{60}Co Comparison

X-ray sources provide a convenient means of performing high-dose-rate irradiations, including irradiations at elevated temperature. However, it is necessary to compare the x-ray and ^{60}Co responses. In previous work, it was shown that the ratio of $\Delta I_B(^{60}\text{Co})$ to ΔI_B(x-ray) for irradiated NPN transistors depends

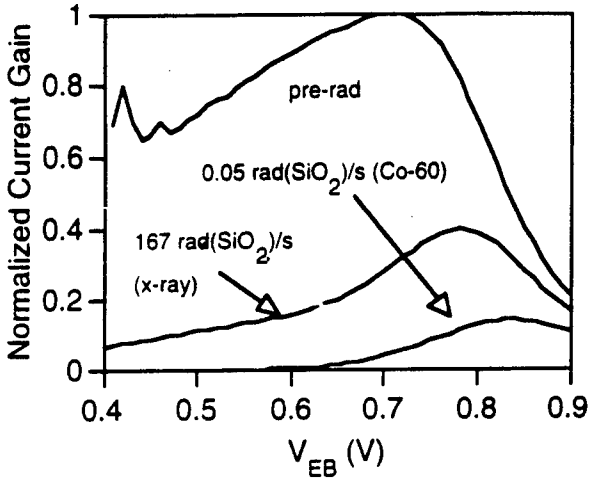


Fig. 3 Normalized current gain vs. emitter-base voltage for LPNP devices irradiated to a total dose of 100 krad(SiO_2) at two different dose rates. A pre-irradiation curve is shown for comparison. The dependence on source type is discussed in the text.

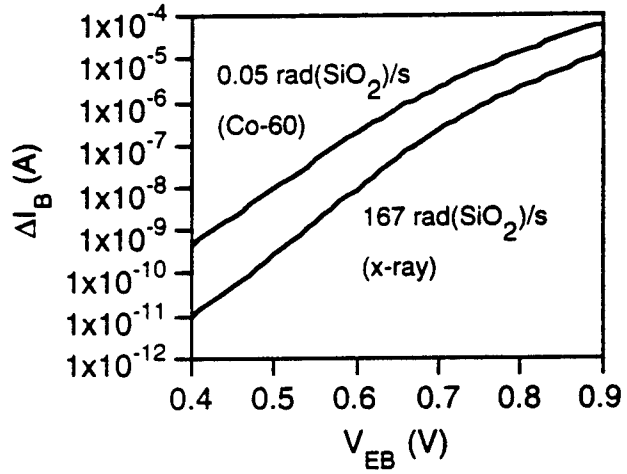


Fig. 4 Excess base current vs. emitter-base voltage for LPNP devices irradiated to a total dose of 100 krad(SiO_2) at two different dose rates. The dependence on source type is discussed in the text.

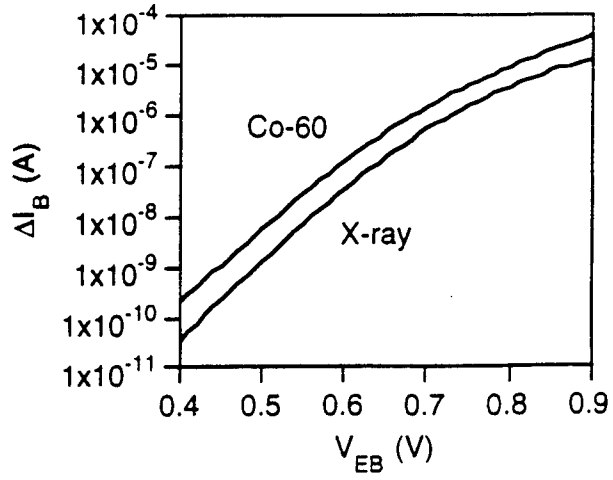


Fig. 5 Excess base current vs. emitter-base voltage for devices irradiated to a total dose of 100 krad(SiO_2) at a dose rate of 1.8 rad(SiO_2)/s. One device was irradiated in a Co-60 source while the other was irradiated in a 10 keV x-ray source.

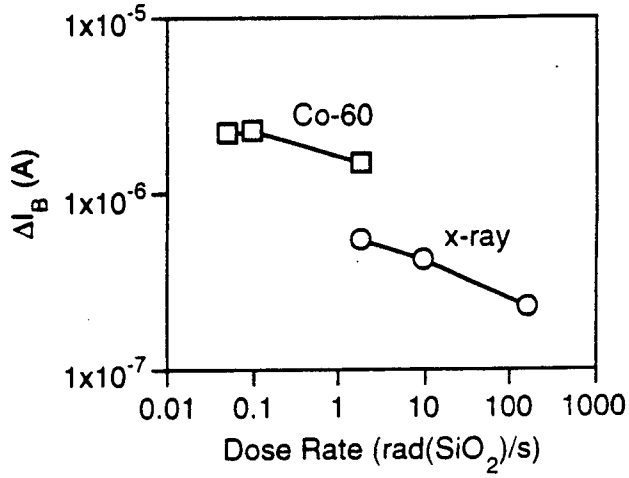


Fig. 6 Excess base current at V_{EB} = 0.7 V vs. dose rate for devices irradiated to a total dose of 100 krad(SiO_2). Data are shown for Co-60 and x-ray irradiations.

on dose rate, total dose, and electric field in the oxide [7]. In Ref. [7], the ratio was approximately two for devices irradiated with V_{BE} = 0 V at 150 rad(SiO_2)/s, but was close to unity for devices irradiated at 10 rad(SiO_2)/s.

Devices were irradiated to a total dose of 100 krad(SiO_2) at a dose rate of 1.8 rad(SiO_2)/s using the Sandia National Laboratories x-ray source and the University of Arizona ^{60}Co source. The excess base current is plotted vs. V_{EB} in Fig. 5. The excess base current for the ^{60}Co irradiation is two to three times greater than that for the x-ray irradiation. This result is consistent with a previous x-ray–^{60}Co comparison for a recessed-oxide bipolar technology [13]. In this work, the failure dose was about two times greater for devices irradiated using x rays than for those irradiated using a ^{60}Co source. It also agrees with previous results for thick oxides irradiated at low electric fields [14], which found significantly more degradation in buried oxides that were irradiated with ^{60}Co. In the buried-oxide devices, three times more dose was required to produce the same threshold-voltage shift when x-ray irradiations were used. The difference is due primarily to increased initial electron-hole recombination during low-energy x-ray irradiations [14,15].

It is important to note that the excess base current does not have to depend linearly on the total dose [9]. Thus, the factor of approximately three in the excess base current does not necessarily translate to a factor of three in dose equivalent. For comparison purposes, the x-ray data presented below have been scaled

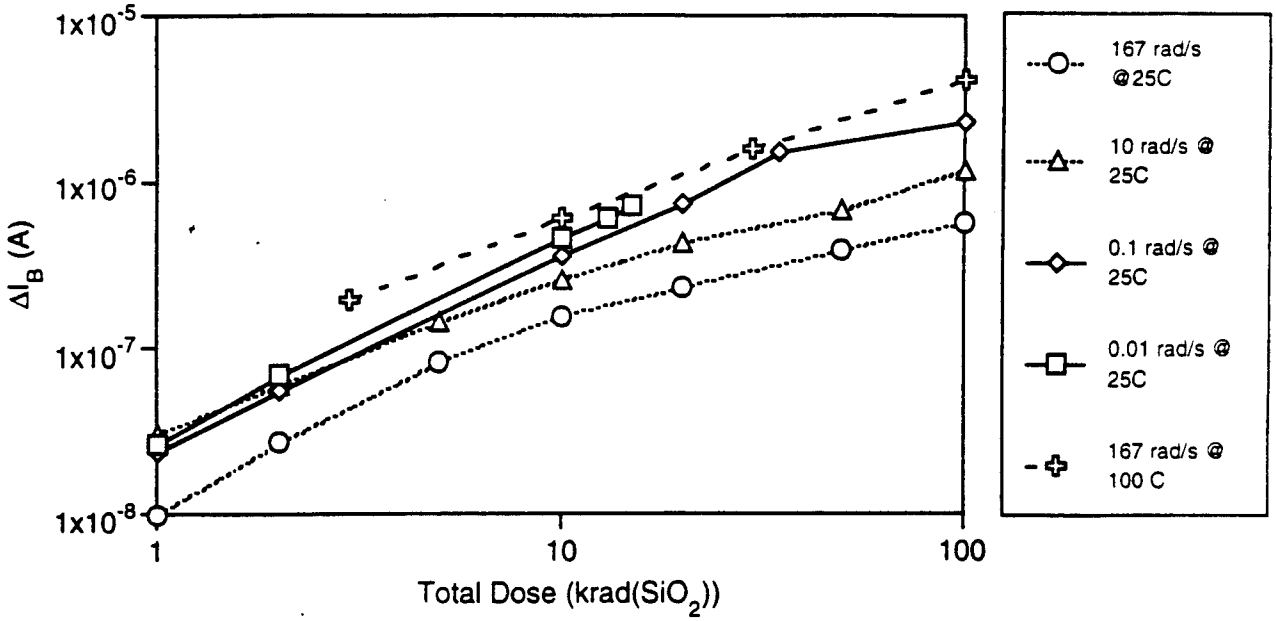


Fig. 7 Excess base current vs. total dose for devices irradiated at a variety of dose rates. The data at the two highest dose rates (dotted lines) are from x-ray irradiations and the two lowest dose rates (solid lines) are from ^{60}Co irradiations. The x-ray data have been scaled to account for the source dependence discussed in section III.B. A high temperature x-ray irradiation (dashed line) is included for comparison.

by the ΔI_B(^{60}Co) to ΔI_B(x-ray) ratio determined from averaging the excess base current at V_{BE} = 0.7 V for five devices irradiated at 1.8 rad(SiO_2)/s in the ^{60}Co source and comparing it to the average of two devices irradiated at 1.8 rad(SiO_2)/s in the x-ray source. The part-to-part variation was very small relative to the average difference between the sources. The ratio determined in this manner is 2.76. This ratio may be different for other technologies and it should also be studied as a function of dose rate. However, it provides a useful means of comparing the high- and low-dose-rate results discussed here.

III.C. Dose-Rate Effects

Much of the concern about hardness-assurance for bipolar integrated circuits has resulted from the presence of enhanced degradation in devices irradiated at low dose rates. For NPN transistors described in previous work, the degradation was significantly higher for devices irradiated below 10 rad(SiO_2)/s than for devices irradiated above 100 rad(SiO_2)/s [8]. The experiments described here were designed to obtain similar information about the dose-rate response of the LPNP transistors studied in this work.

Figure 6 displays the excess base current measured at V_{EB} = 0.7 V vs. dose rate for LPNP devices irradiated to a total dose of 100 krad(SiO_2). This figure also clearly indicates the difference between x-ray and ^{60}Co described above. The response is qualitatively the same at all values of V_{EB} examined (between 0.6 V and 0.8 V, the most usable portion of the device characteristics). There is approximately ten times more excess base current in the devices irradiated at the lowest dose rates using ^{60}Co than in the devices irradiated at 167 rad(SiO_2)/s using x-rays, illustrating the strong dose-rate dependence in these parts. Because this difference is partially due to the difference in source types, the data in the figures below have been scaled by the ratio determined in section III.B, as noted.

The excess base current is plotted vs. total dose for devices irradiated at several dose rates in Fig. 7. The x-ray data have been scaled to account for the source differences. The devices irradiated at the lowest dose rate (0.01 rad(SiO_2)/s) received a maximum total dose of 30 krad(SiO_2), while the devices irradiated at the higher dose rates received a maximum total dose of 100 krad(SiO_2). There is significantly more excess base current in devices irradiated at low dose rates for all of the total-dose levels examined. For comparison purposes, a curve is included for irradiation at 167 rad(SiO_2)/s at 100°C. This irradiation condition produces more degradation than any of the low-dose-rate irradiations, once source differences have been accounted for.

The goal of the remaining experiments described in this paper is to predict the degradation at the low dose rates using more convenient high-dose-rate measurements. The approaches considered are high-temperature irradiation at high dose rates and irradiation at high dose rates followed by annealing.

III.D. High-Temperature Irradiation

It was previously suggested that irradiating devices at elevated temperature may be an effective technique for predicting low-dose-rate gain degradation in NPN bipolar transistors [10]. The high-temperature irradiation method was proposed based on evidence that there is a higher density of net positive charge in the oxides covering emitter-base junctions when the devices are

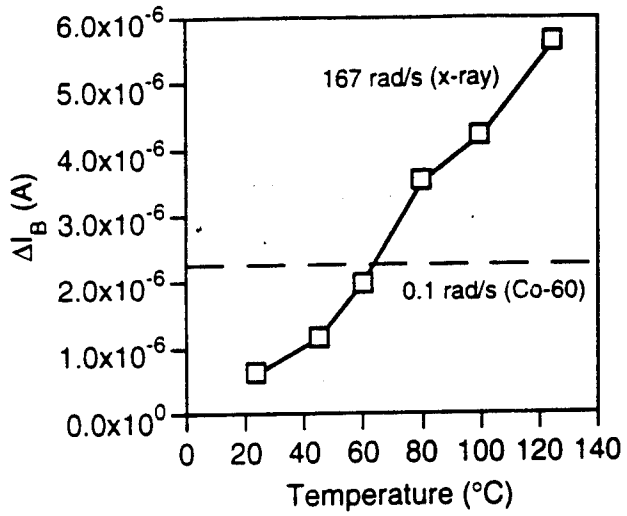


Fig. 8 Excess base current at $V_{EB} = 0.7$ V vs. irradiation temperature for LPNP devices irradiated to 100 krad(SiO_2) at 167 rad(SiO_2)/s in the x-ray source. The dashed line indicates the excess base current measured in devices irradiated at 0.1 rad(SiO_2)/s room temperature in the ^{60}Co source. The x-ray data have been scaled to account for source differences.

irradiated at low dose rates. This was attributed to space-charge effects associated with slowly transporting and/or metastably trapped holes in the oxide. There are more of these holes in the oxide at high dose rates, causing holes to be trapped (on average) slightly closer to the Si/SiO_2 interface where more of them will be neutralized by electrons from the substrate. At high temperature, the hole transport is speeded up and/or the delocalized hole traps responsible for the long-term hole transport are neutralized. Thus, high temperature irradiation should produce conditions more closely approximating those of low-dose-rate irradiation [10]. The experiment described here was designed to test the applicability of this theory for a different class of devices than that previously examined.

Devices were irradiated at temperatures of 24, 45, 60, 80, 100, and 125°C using a dose rate of 167 rad(SiO_2)/s in the x-ray source. Figure 8 shows the excess base current at $V_{EB} = 0.7$ V for LPNP devices irradiated to 100 krad(SiO_2). For comparison, the dashed line represents the degradation in devices irradiated at 0.1 rad(SiO_2)/s, but at room temperature. The excess base current increases approximately linearly with irradiation temperature in this temperature range. The excess base current for irradiation at 125°C is nearly equal to that occurring for irradiation at 0.1 rad(SiO_2)/s (the dose rate at which the greatest degradation is seen in Fig. 6), even without scaling to account for the difference in source types. When the data are scaled by the factor relating ^{60}Co to x-ray irradiation (as shown in Fig. 8), elevated temperatures conservatively estimate the low-dose-rate degradation. This suggests that high-temperature irradiation is a very effective technique for predicting the low-dose-rate degradation for these LPNP devices, as well as for the NPN devices in Ref. [10]. In addition, it was reported that irradiation at 60°C enhanced the degradation of LPNPs from another technology, but not as much as that produced by low-dose-rate irradiation [3]. The results shown here confirm that 60°C may not be sufficiently high to produce the desired amount of enhanced degradation.

The continued increase in excess base current as a function of irradiation temperature at the highest temperature used in these experiments is a surprising result, and it makes it more difficult to identify the "best" temperature for hardness-assurance testing. However, the results presented in the next section for devices irradiated at room temperature, but annealed at high temperatures, show that the damage begins to recover at 150°C. This recovery may take place in situ during irradiation at 150°C, but it was not examined during these experiments.

III.E. Annealing Response

MIL-STD-883B, Method 1019.4 is a well-established hardness-assurance technique that includes provisions for bounding the response of MOS devices irradiated at low dose rates [16,17]. This technique was developed for MOS devices, not bipolar devices. If the same procedure is applied to bipolar devices, it produces nonconservative results for some bipolar technologies [4,7]. A key part of Method 1019.4 is irradiating devices at a high dose rate, followed by an anneal at 100°C. The anneal removes some of the oxide trapped charge and also helps to speed up the formation of interface traps, thus providing a bound for the degradation that occurs in devices that have a low-dose-rate radiation response dominated by interface-trap effects [12,16,17]. A set of experiments was designed to examine the annealing behavior of the LPNP devices studied in this work. It was previously shown that NPN devices annealed at elevated temperature show improvement in their current gain, instead of the enhanced degradation observed at low dose rates. However, for the LPNP devices studied here, additional degradation is seen during room-temperature and high-temperature annealing.

Figure 9 shows the excess base current at $V_{EB} = 0.7$ V vs. anneal time, following irradiation to a total dose of 100 krad(SiO_2). The annealed device shown here was irradiated at 10 rad(SiO_2)/s, but the results were similar for devices irradiated at 1.8 rad(SiO_2)/s. The excess base current continues to increase following the end of irradiation, and approaches the amount of degradation in devices irradiated at low dose rates using ^{60}Co (0.05 rad(SiO_2)/s in this case), if the x-ray data are scaled to account for the difference in source type. However, this occurred in a device that was irradiated at a relatively low dose rate (10 rad(SiO_2)/s) in the x-ray source. At higher dose rates (50-300 rad(SiO_2)/s), the irradiation-plus-anneal prediction will be even worse. This loss of gain during room-temperature annealing is opposite the trend observed in NPN transistors [7], making it very difficult to base a general hardness-assurance method for bipolar integrated circuits on this approach. However, the loss of gain during post-irradiation annealing is similar to continued degradation in MOSFETs that are significantly affected by interface traps.

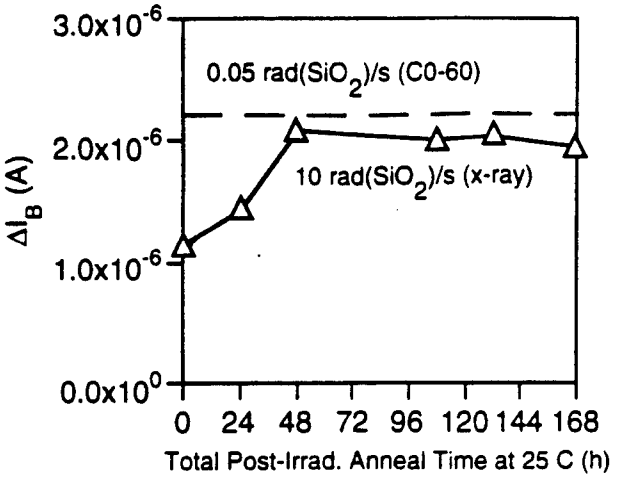


Fig. 9 Excess base current at V_{EB} = 0.7 V vs. post-irradiation room-temperature anneal time for devices irradiated to 100 krad(SiO_2) at 10 rad(SiO_2)/s in an x-ray source. The dashed line indicates the amount of excess base current measured in devices irradiated at 0.05 rad(SiO_2)/s in a ^{60}Co source, without annealing. The x-ray data have been scaled to account for the source difference.

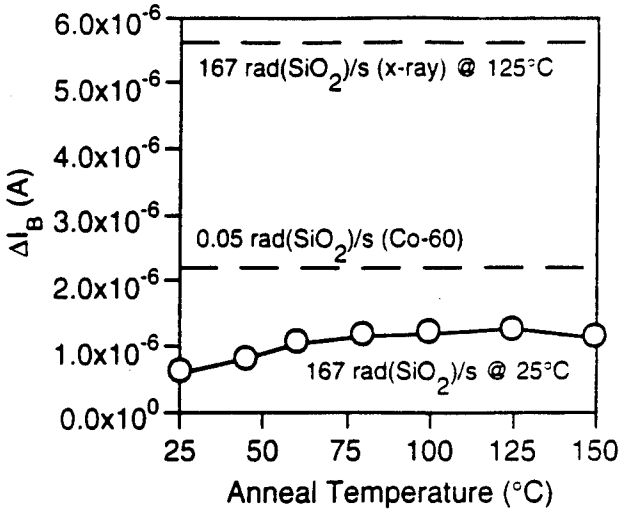


Fig. 10 Excess base current at V_{EB} = 0.7 V vs. anneal temperature for LPNP devices irradiated to 100 krad(SiO_2) at 167 rad(SiO_2)/s and room temperature. The dashed lines indicate the amount of excess base current measured in devices irradiated at low dose rate using ^{60}Co, and also at high dose rate and high temperature using x-rays.

Additional devices were irradiated to a total dose of 100 krad(SiO_2) at room temperature and then sequentially subjected to thirty-minute anneals at temperatures up to 150°C. Figure 10 shows the excess base current at V_{EB} = 0.7 V vs. anneal temperature. The base current slightly increases during the early anneal periods, before finally decreasing slightly during the 150°C anneal. In this case, the base current remains significantly lower than that in devices irradiated at the low dose rates using ^{60}Co, or at high dose rates and high temperatures using x-rays. This is a consequence of irradiating the devices at a higher dose rate than that used in Fig. 9 (167 rad(SiO_2)/s vs. 10 rad(SiO_2)/s). The reduction in excess base current at 150°C suggests that if high-temperature irradiations are conducted at this temperature, the enhanced degradation seen at 125°C may begin to reverse due to annealing processes.

The post-irradiation increase in the base current for devices annealed at elevated temperature suggests that combining high-temperature irradiation with high-temperature annealing may provide additional degradation. This was examined experimentally by irradiating devices at 80° and 100° C, followed by anneal cycles at the same temperature used for irradiation. In all cases, the excess base current decreased during the high-temperature anneal. Thus, high-temperature irradiation, without a subsequent high-temperature anneal, provides a better estimate of the low-dose-rate degradation.

III.F. Comparison to Other Device Types

In addition to the LPNP transistors used in the experiments described above, vertical NPN and substrate PNP transistors in the same packages as the LPNP transistors also were tested. It is very desirable that the same hardness-assurance method provide useful results for all bipolar technologies. Since high-temperature irradiation is the most promising technique for predicting the LPNP low-dose-rate response, the same information for the NPN and SPNP devices is shown in Figures 11 and 12.

For the NPN device, the excess base current at 100 krad(SiO_2) is much less than the initial base current in the unirradiated devices, as shown in Fig. 11. This illustrates that the NPN transistors fabricated in this technology are much harder than the LPNP transistors. Although the excess base current appears to be slightly higher for the NPN devices irradiated at elevated temperature, the small magnitude of the excess base current relative to the total base current means that obtaining an accurate estimate of the excess base current is difficult. Moreover, for integrated circuits fabricated in the technology considered here, the degradation will be dominated by the LPNP response. Thus, irradiation at elevated temperature will predict the circuit-level degradation, as well as the degradation of the LPNP devices.

The substrate PNP transistors are not usually incorporated in circuit designs fabricated in this technology. Their main purpose is to serve as a test structure. However, it is interesting to compare the response of the SPNP devices to the LPNP devices to determine if high-temperature irradiation also predicts the low-dose-rate degradation. As illustrated in Fig. 12, the behavior of the SPNP devices is qualitatively the same as that of the LPNP devices. Irradiation at high temperatures produces more degradation than that which occurs at low dose rates, once source differences are accounted for.

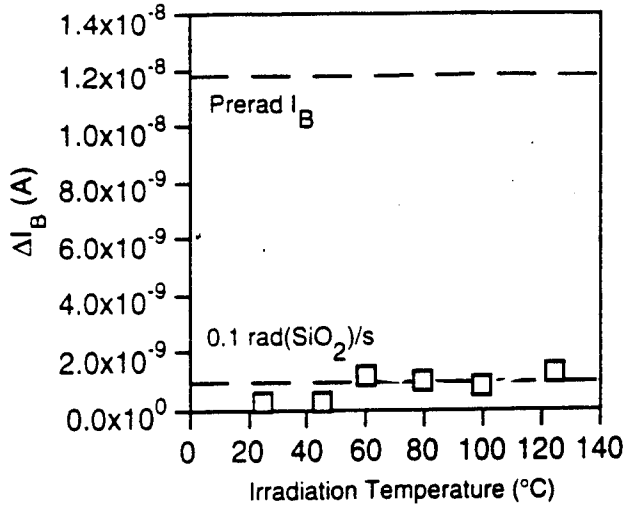


Fig. 11 Excess base current at $V_{EB} = -0.7$ V vs. irradiation temperature for NPN transistors irradiated to a total dose of 100 krad(SiO_2) at 167 rad(SiO_2)/s. The dashed lines indicate the pre-irradiation base current and the excess base current for low-dose-rate irradiation.

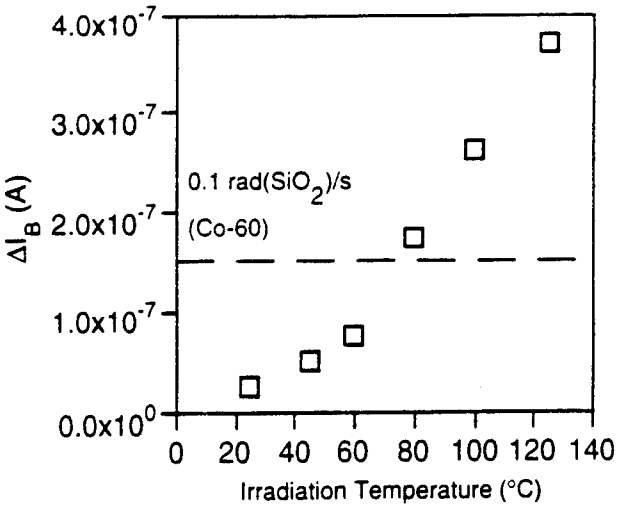


Fig. 12 Excess base current at $V_{EB} = 0.7$ V vs. irradiation temperature for substrate PNP transistors irradiated to a total dose of 100 krad(SiO_2) at 167 rad(SiO_2)/s using x-rays. The dashed line indicates the excess base current for irradiation at 0.1 rad(SiO_2)/s using ^{60}Co. The x-ray data have been scaled to account for source differences.

IV. Testing Recommendations

There are two classes of failure mechanisms that must be considered for bipolar integrated circuits in space-radiation environments: isolation-related failures [18] and gain-related failures. Testing to identify isolation-related failures can be accomplished using conventional test methods developed for MOS integrated circuits [16,17]. This paper describes approaches for dealing with gain-related failures. Since there are two failure mechanisms, two tests are required. This is similar to the situation with MOS devices, in which failures due to oxide trapped charge and those due to "rebound" must both be considered. However, for bipolar technologies, two sets of test devices must be used since radiation-plus-anneal testing does not predict the low-dose-rate response successfully.

Of the approaches considered here to predict gain degradation at low dose rates, irradiation at elevated temperature is the most promising. The excess base current increases approximately linearly with temperature up to 125°C, but high-temperature anneal experiments showed recovery at 150°C. High-temperature irradiation was shown previously to enhance degradation in NPN transistors. While these results represent a relatively small cross-section of bipolar technologies, enhancement of degradation for high-temperature irradiation was predicted in [10] using a physical model based on the presence of metastable hole traps in bipolar oxides, as decribed in Section III.D. The presence of a physically-based justification for this method increases the level of confidence associated with it.

Preliminary testing recommendations can be formulated, based on previous experiments that looked at isolation-related failures [18] and the gain-degradation results presented here and in previous work [8,10]. There have been no experimental reports of anomalous isolation-related failures in bipolar ICs irradiated at low dose rates, so the recommended test procedure includes the same test used to identify these failures in MOS ICs. The new feature proposed here is a high-temperature irradiation. These preliminary recommendations are summarized here:

(1) Irradiate one set of devices to the specified total dose at room temperature using a dose rate of 50 rad(SiO_2)/s or greater to check for isolation-related failures [18].

(2) Irradiate a second set of devices to the specified total dose at a temperature of 100-125° C with ^{60}Co. If an x-ray source is used, the total dose should be increased by a factor of three. The test should be conducted at a dose rate between 50 and 300 rad(SiO_2)/s. The purpose of this test is to identify gain-related failures.

This approach works for NPN transistors from Analog Devices' XFCB technology and LPNP devices from Analog Devices' ADRF technology. These are the most sensitive devices in these technologies; the vertical PNP transistors in the XFCB technology and the vertical NPN transistors in the ADRF technology degrade much less. The approach also may work for the PNP devices described in Ref. [3], but a higher irradiation temperature than 60°C (as done here) should be used to determine this.

V. Discussion

Predicting the low-dose-rate degradation of bipolar integrated circuits is a difficult challenge because of the greatly enhanced degradation compared to high-dose-rate irradiation. For the devices considered in this work, the excess base current in devices

irradiated below 0.1 rad(SiO_2)/s with ^{60}Co was ten times greater than that in devices irradiated at 167 rad(SiO_2)/s with x-rays. Two general hardness-assurance approaches were examined in this work: (1) irradiation at high dose rates and high temperature and (2) irradiation at high dose rates followed by annealing.

The results shown for high-temperature, high dose-rate irradiation suggest that irradiation at 100° C (or higher) may be a viable hardness-assurance method for predicting the low-dose-rate behavior of some technologies. Post-irradiation annealing of devices irradiated at room temperature caused the excess base current to increase, but not to the levels observed in devices irradiated at low dose rates. The maximum post-irradiation degradation was produced by annealing at 125°C, the same temperature that produced the maximum degradation in devices irradiated at elevated temperature. The excess base current decreased slightly during annealing at 150°C. This damage recovery during high-temperature annealing indicates the presence of a mechanism that may compete with that responsible for the enhanced degradation due to high-temperature irradiation. The annealing results suggest that the practical limit for high-temperature irradiation may be less than 150°C, but this should be examined experimentally for a range of bipolar technologies.

The results presented here indicate that high-temperature irradiation is a very promising approach for predicting low-dose-rate degradation in LPNP devices and in integrated circuits whose radiation responses are dominated by LPNP degradation. Combined with previous results showing accelerated degradation in NPN transistors irradiated at elevated temperature, this work suggests that the approach may be applicable to a range of modern bipolar integrated circuits. However, it is essential that this method be tested with other technologies to ascertain the generality.

VI. Acknowledgments

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V.M. Synergetic Effects of Radiation Stress and Hot-Carrier Stress on the Current Gain of NPN Bipolar Junction Transistors

SYNERGETIC EFFECTS OF RADIATION STRESS AND HOT-CARRIER STRESS ON THE CURRENT GAIN OF NPN BIPOLAR JUNCTION TRANSISTORS†

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Abstract

The combined effects of ionizing radiation and hot-carrier stress on the current gain of npn bipolar junction transistors were investigated. The analysis was carried out experimentally by examining the consequences of interchanging the order in which the two stress types were applied to identical transistors which were stressed to various levels of damage. The results indicate that the hot-carrier response of the transistor is improved by radiation damage, whereas hot-carrier damage has little effect on subsequent radiation stress. Characterization of the temporal progression of hot-carrier effects revealed that hot-carrier stress acts initially to reduce excess base current and improve current gain in irradiated transistors. PISCES simulations show that the magnitude of the peak electric-field within the emitter-base depletion region is reduced significantly by net positive oxide charges induced by radiation. The interaction of the two stress types is explained in a qualitative model based on the probability of hot-carrier injection determined by radiation damage and on the neutralization and compensation of radiation-induced positive oxide charges by injected electrons. The results imply that a bound on damage due to the combined stress types is achieved when hot-carrier stress precedes any irradiation.

I. INTRODUCTION

The effects of ionizing radiation on the performance of bipolar junction transistors (BJTs) have received considerable attention in the literature[1-4]. The radiation-induced defects associated with current gain degradation in modern bipolar structures are trapped net positive charge and interface traps in the oxide overlying the emitter-base junction and extrinsic base[5-7]. The positive oxide trapped charge spreads out the emitter-base depletion region, which results in increased recombination current under forward-biased operation of the junction. The rate of recombination increases with total dose according to the electrostatic potential induced in the depletion region[8]. The interface traps created by radiation that have energies near midgap are most relevant to current gain degradation, since they make efficient generation-recombination (G-R) centers. G-R centers further increase recombination current throughout the depletion region by enhancing surface recombination velocity[9]. Ionizing radiation degrades current gain, since the recombination currents which it causes increase the base current, especially for low base-to-emitter voltages, while the collector current remains relatively constant.

Hot-carrier stress in integrated BJTs can occur whenever the emitter-base junction is sufficiently reverse-biased so as to create large electric-fields within the emitter-base depletion region[10-13]. This occurs, for example, in the operation of emitter-coupled differential pairs in certain analog-to-digital converters[14] and more readily in the pull-up transistors of certain bipolar-complementary-metal-oxide-silicon gates used in digital circuits during pull-down transients[15,16]. Energetic carriers drifting through the emitter-base depletion region, especially near the emitter periphery, where doping in the extrinsic base is high, can suffer collisions which result in their scattering into the overlying oxide. Hot-carrier susceptibility is an increasing concern in modern BJTs, as vertical scaling of device dimensions dictates that higher base and emitter doping levels be used to shrink the emitter-base depletion region[17,18]. Hot-carriers can increase the interface trap densities locally, resulting in larger surface recombination velocities and increased recombination current within the emitter-base depletion region in much the same way as radiation stress[19,20]. In addition, injected carriers can become trapped in the oxide, either after surmounting the interfacial potential barrier or by tunneling through the barrier to traps in the oxide bandgap, where they can bend the energy bands and alter device characteristics[21]. Like radiation, hot-carrier stress degrades the current gain in BJTs by increasing the base current while affecting the collector current negligibly.

Although considerable progress has been made toward understanding the effects of ionizing radiation and hot-carrier stress acting individually on the operational behavior of BJTs, little is known about the combined effects of these two stress types. There exists a real need for such cognition, because, in many space, military, and nuclear power plant applications, BJTs are subjected to both of these stress types simultaneously. As such, the objective of this work was the experimental characterization of the current gain in npn BJTs which were subjected to various combinations of radiation stress and hot-carrier stress. Emphasis in the experiments was placed on assessing the

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importance of the stress type sequence in determining the extent to which the current gain was degraded. PISCES simulations were performed in conjunction with the experiments in order to lend support to the results.

It is shown that the effects of radiation stress and hot-carrier stress on current gain are not simply additive, i.e., the damaging mechanisms associated with the two stress types are interactive. Most prominent is the influence of radiation damage on diminishing the amount of degradation due to subsequent hot-carrier stress, meaning that the order in which the two stress types are applied is relevant to determining the resulting current gain. The results are used to develop a physical model to describe the interaction of ionizing radiation and hot-carrier stress as they relate to current gain degradation in npn BJTs. The model is consistent with established understanding of the separate stress types.

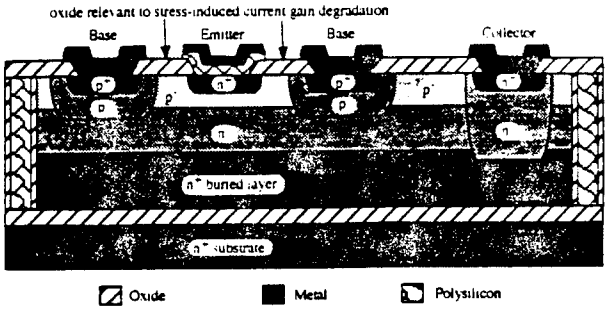


Fig. 1. A cross-section of the BJT used in this study. The cross-section is helpful in visualizing the physical mechanisms associated with stress-induced current gain degradation in the device.

II. EXPERIMENT

A. Description of BJT Technology

Fig. 1 shows a cross-section of the particular bipolar technology used in this study[22]. The cross-section is useful for visualizing the physical mechanisms by which radiation damage and hot-carrier damage occur in the device. The oxide immediately above the emitter-base junction, where damage due to the two stress types has the greatest effect on current gain degradation, is indicated for clarity. This oxide consists of two layers with a total thickness of 545 nm. The bottom layer is used as a screen through which the p-type base is implanted into the n-type epitaxial collector. The device is isolated dielectrically on all four sides by a trench etch and refill process and on the bottom by a buried oxide which was fabricated by a bond, lap-back, and polish technique. A poly-Si emitter is used to avoid Al spiking at the contact and to decrease the base diffusion current[23]. The n^+ emitter region was formed by thermal diffusion of the deposited poly-Si layer and has dimensions of 1.5 μm × 1.5 μm. The emitter-base junction depth is 0.3 μm, and the active base width is 0.8 μm. Doping in the extrinsic base at the Si surface, where hot-carrier effects are most prevelant, is 9.0×10^{17} cm^{-3}. The pre-stressed peak current gain in this device is approximately 95 and occurs at a base-to-emitter voltage of about 0.7 V.

B. Effect of Interchanging the Order of the Stress Types

Six pairs of BJTs were used to investigate the effect of interchanging the order of irradiation and hot-carrier stress on current gain. The pre-stressed base and collector currents were verified to be nearly identical between the transistors. The BJTs were stressed according to the parameters summarized in Table I. One of the BJTs in each pair was stressed first with hot-carriers and then with radiation, while the other was stressed first with radiation and then with hot-carriers under the same conditions as its companion. Hot-carrier stress was performed using a constant emitter current of 225 nA and an open-circuited collector, which placed the emitter-base junction just into avalanche breakdown. The devices were irradiated with all terminals grounded in a ^{60}Co γ-source at a dose rate of 4.0 krad(SiO_2) hr^{-1}. The devices were situated in a box made of Pb and Al during the irradiation. In order to assess the response to a wide range of stress levels, the stress times and total doses administered to the six BJT pairs were varied from 250 to 20,000 s and from 35 to 1,000 krad(SiO_2), respectively. Annealing of damage following hot-carrier stress was monitored in a non-irradiated BJT and was observed to be negligible. The ambient temperature varied less than 2°C from the starting temperature over the course of the experiment.

Table I
Stress Parameters

Device	Stress No. 1	Stress No. 2
1A	225 nA for 250 s	35 krad(SiO_2)
1B	35 krad(SiO_2)	225 nA for 250 s
2A	225 nA for 1,000 s	75 krad(SiO_2)
2B	75 krad(SiO_2)	225 nA for 1,000 s
3A	225 nA for 2,000 s	150 krad(SiO_2)
3B	150 krad(SiO_2)	225 nA for 2,000 s
4A	225 nA for 5,000 s	300 krad(SiO_2)
4B	300 krad(SiO_2)	225 nA for 5,000 s
5A	225 nA for 10,000 s	550 krad(SiO_2)
5B	550 krad(SiO_2)	225 nA for 10,000 s
6A	225 nA for 20,000 s	1,000 krad(SiO_2)
6B	1,000 krad(SiO_2)	225 nA for 20,000 s

Following the completion of each stress type, the resulting excess base current and current gain were measured. Excess base current is defined here as the increase in the base current of a virgin device due to stress, as expressed by the relation

$$\Delta I_B = I_B - I_{B_o}. \quad (1)$$

As usual, the current gain is defined by

$$\beta = \frac{I_C}{I_B}, \qquad (2)$$

where I_C is the collector current. When used with either ΔI_B or β in the results that follow, the superscripts ^{r}, ^{h}, ^{rh} and ^{hr} indicate degradation due to radiation, hot-carriers, or a combination of the stress types.

In Fig. 2(a), the excess base currents for the BJTs which were stressed first by hot-carriers and then by radiation are compared with those for the BJTs in which the order of the stress types was reversed. A base-to-emitter voltage of 0.7 V was chosen for the comparison, since this corresponds to the peak in the pre-stressed current gain. The abcissa value for each BJT pair in the figure represents the sum of the excess base currents which resulted from the radiation stress of the virgin device and the hot-carrier stress of its companion device. The dashed line drawn diagonally through the figure represents the condition that the effects of the two stress types on excess base current are simply additive.

It is clear from the figure that, at each level of combined stress considered, excess base current is greater when the device is stressed first by hot-carriers and then by radiation than it is when the device is stressed in the reverse sequence. The difference in excess base currents measured for the two sets of BJTs tested is smallest for the BJT pair which received the lowest level of combined stress and grows in magnitude as the amount of stress is increased. The fact that the data points corresponding to the devices which were stressed first by radiation and then by hot-carriers lie below the dashed line is an indication that radiation damage decreases the effectiveness with which subsequent hot-carrier stress increases base current. In contrast, since the data points corresponding to the devices which were stressed first by hot-carriers and then by radiation lie on or near the dashed line, hot-carrier damage is seen to have little influence on subsequent radiation stress degrading the device further.

A comparison of the corresponding current gains normalized by their pre-stressed values is shown in similar fashion in Fig. 2(b). The figure reflects the trends in excess base current noted previously. As expected, the current gain decreases with increasing excess base current regardless of the stress sequence. However, as a group, those BJTs which were stressed first by hot-carriers and then by radiation clearly sustained greater reduction in current gain than their counterparts. The order in which the two stress types are applied is of least consequence in determining the overall current gain in the BJT pair which received the smallest amount of damage. As the magnitude of damage increases, the effect of stress order on current gain grows in importance. The effect of interchanging the stress sequence on the measured excess base current and corresponding current gain was even more pronounced for base-to-emitter voltages below 0.7 V.

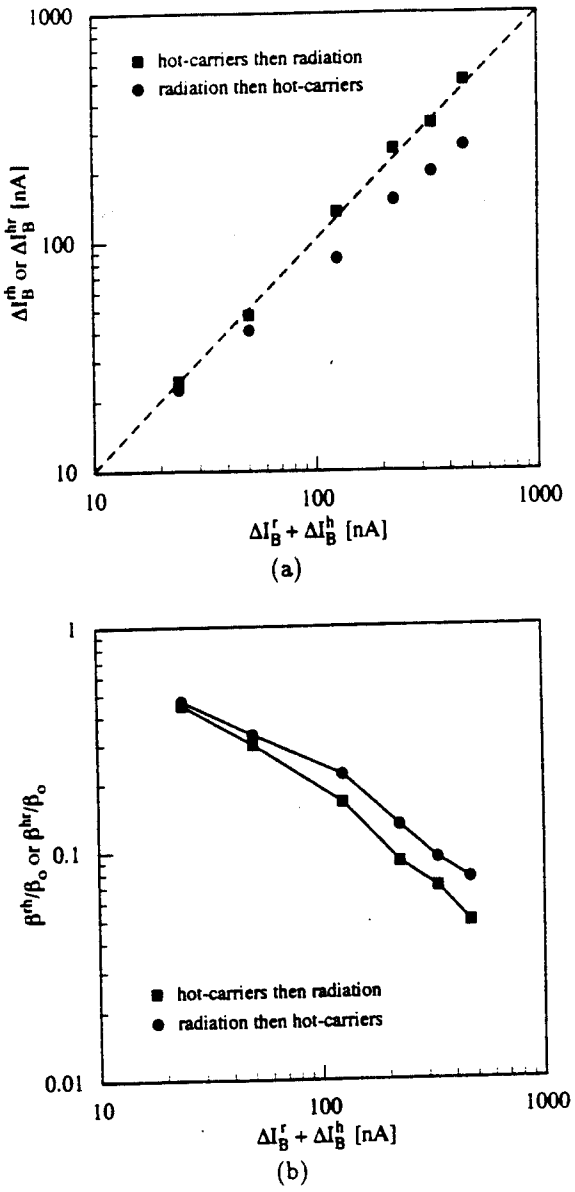


Fig. 2. The effect of interchanging the order of radiation stress and hot-carrier stress on (a) excess base current and (b) current gain. Device degradation is less severe when radiation stress precedes hot-carrier stress than it is when the sequence of stress types is reversed. All data were measured at $V_{BE} = 0.7$ V.

C. Effect of Radiation Stress on Subsequent Hot-Carrier Stress

An additional experiment was conducted in order to examine more closely the effect of radiation damage on subsequent hot-carrier stress in an npn BJT. Three BJTs identical to those used in the previous experiment were irradiated to total doses of 150, 450, and 1,000 krad(SiO_2), respectively. Each device subsequently was hot-carrier stressed for various increments of time up to a total of 100,000 s. Both the irradiation and hot-carrier stress were

performed under the conditions described previously. Gummel measurements were taken before irradiation, immediately following irradiation, and after each time increment of hot-carrier stress. In order to minimize the effects of forward-biased current soak[24] on the measurement results, Gummel sweeps included only five base-to-emitter voltages between 0.4 and 0.8 V and lasted only a few seconds. Each Gummel measurement was repeated, from which annealing of damage due to the measurement itself was verified to be negligibly small. Annealing of radiation damage was avoided by performing the hot-carrier stress immediately following irradiation.

The progression of the base current with hot-carrier stress time for the device which received a total dose of 1,000 krad(SiO_2) is illustrated in Fig. 3. The base current is plotted as a function of base-to-emitter voltage. As expected, the high total dose resulted in a large increase in base current in the virgin device. Subsequent hot-carrier stress, however, revealed some very interesting and rather unexpected results. As indicated in the figure, hot-carrier stressing the irradiated device acted initially to *decrease* base current. This reduction in the radiation-induced excess base current continued for stress times totaling several hundred seconds, at which time it reversed, and the base current began to increase again. Thereafter, the base current increased monotonically for as long as the stress continued.

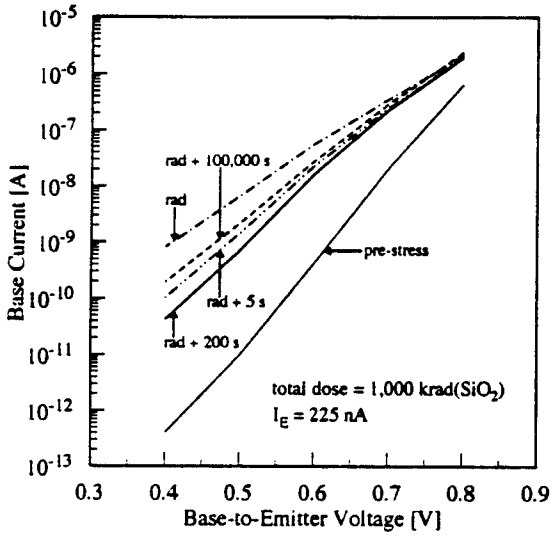


Fig. 3. The temporal progression of base current in an irradiated npn BJT as it is subjected to hot-carrier stress. Hot-carrier stress decreases base current substantially before eventually increasing it.

This hot-carrier response of the irradiated device is depicted in another form in Fig. 4 along with the responses of the other BJTs irradiated. In this figure, the current gain following the combined stresses of radiation and hot-carriers, normalized by the current gain following irradiation only, is plotted for each device as a function of hot-carrier stress time. The gain was measured at a base-to-emitter voltage of 0.7 V. The dashed line at $\beta_{rh}/\beta_r = 1$ divides the figure into two distinct regions. Any data points located above this line indicate that hot-carrier stress *increased* the current gain in the irradiated device, whereas those data points located below the line indicate that hot-carrier stressing the irradiated device decreased the current gain. The figure indicates that the degree to which hot-carrier stress increases current gain in an irradiated npn BJT grows with increasing total dose. In addition, the hot-carrier stress time at which the current gain stops increasing and the duration of stress time over which the current gain remains greater than it was immediately following irradiation are strongly dependent on total dose.

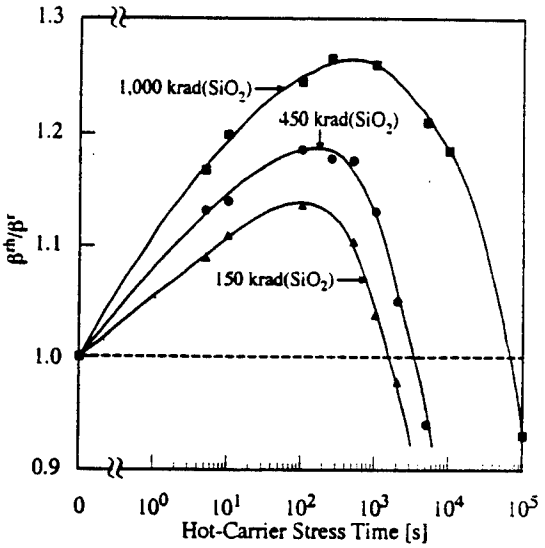


Fig. 4. The effect of hot-carrier stress on the current gain of irradiated npn BJTs measured at $V_{BE} = 0.7$ V. The extent to which hot-carrier stress recovers current gain previously degraded by radiation depends strongly on the total dose.

D. Effect of Hot-Carrier Stress on Subsequent Radiation Stress

In order to gain additional insight into the problem of irradiating hot-carrier damaged BJTs, a final experiment complementary to the one described in the previous section was performed. Another group of three identical virgin test devices were hot-carrier stressed for times of 100, 4,000, and 100,000 s, respectively, after which they were irradiated to a total dose of about 6 Mrad(SiO_2). The conditions under which the hot-carrier and radiation stresses were administered were consistent with the previous experiments described. Gummel measurements were taken before hot-carrier stress, immediately following hot-carrier stress, and after periodic interruptions of subsequent radiation stress so that the excess base currents resulting from stress could be quantified.

In Fig. 5, the excess base currents in the three devices are compared as a function of total dose at a base-to-emitter voltage of 0.7 V. The variation in excess base

currents for zero total dose reflects the wide range of hot-carrier stress times used and gives some indication of how stress time determines the level of damage created in these devices. In contrast to the case in which irradiation precedes hot-carrier stress, the excess base currents always increase here as a result of applying the second stress type. Although the initial excess base currents vary widely, there is little difference among the devices in the rates at which the excess base currents are increased by radiation. The excess base currents saturate at different levels commensurate to their initial values. The differences in the saturation levels are comparable in magnitude to the differences that existed in the initial excess base currents. These results further substantiate the observation made earlier that radiation effects in npn BJTs are influenced little by damage created initially by hot-carriers.

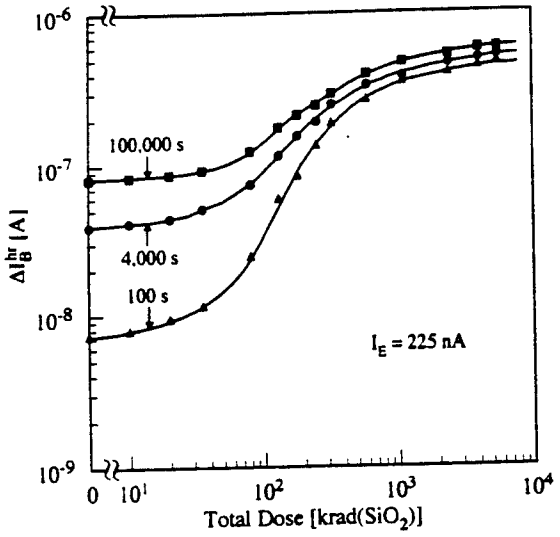


Fig. 5. The effect of ionizing radiation on the excess base currents of hot-carrier stressed npn BJTs. The rate at which radiation increases base current is influenced little by damage created initially by hot-carriers. All data were measured at V_{BE} = 0.7 V.

III. PISCES SIMULATION

To aid in understanding the physical mechanisms underlying the experimental results, PISCES simulations[25] were carried out in a way which closely mimicked the hot-carrier stressing of an irradiated BJT. The device geometries and materials defined in the simulations replicated those of the actual experimental test devices. The appropriate doping profiles were generated by SUPREM process modeling and were verified with spreading resistance measurements of control wafers processed along with the test devices. The carrier recombination times used in the simulation were obtained by matching simulated Gummel plots to those actually measured in the pre-stressed devices. Operation of the BJT was simulated for a constant emitter current in the emitter-base avalanche breakdown region using various densities of positive oxide trapped charge. The appropriate oxide charge densities were calculated from measured parallel shifts in the C-V characteristics of an irradiated metal-oxide-silicon capacitor that was fabricated in the same process as the BJTs. PISCES was used to solve Poisson's equation and the continuity equations for electrons and holes simultaneously in two dimensions at discrete points in the base, emitter, and overlying oxide under the simulation conditions described.

Fig. 6 summarizes the simulation results for the electric-field along the Si surface in the emitter-base depletion region with oxide trapped charge density as a parameter. The ordinate axis represents the magnitude of the electric-field normalized by the pre-stressed peak electric-field magnitude. Negative abcissa values correspond to locations within the emitter, whereas positive values are located within the base. The condition $N_{ox} = 0$ is used to approximate the state of the oxide prior to irradiation, while the densities $N_{ox} = 1 \times 10^{12}$ cm^{-2} and $N_{ox} = 3 \times 10^{12}$ cm^{-2} correspond to total doses of approximately 100 and 1,000 krad(SiO_2), respectively. The figure clearly reflects the spreading of the emitter-base depletion region due to the addition of positive charge in the oxide. Whereas the electric-field is significant in magnitude over a distance of only about 0.15 μm near the emitter-base junction when there is no oxide charge present, it increases dramatically far from the junction with the addition of positive oxide charge. In addition, increasing the density of positive oxide charge reduces the peak electric-field in the depletion region near the emitter-base junction. The peak electric-field along the Si surface is of utmost importance in this simulation, as it plays a very strong role in determining the extent to which hot-carrier injection occurs in the oxide.

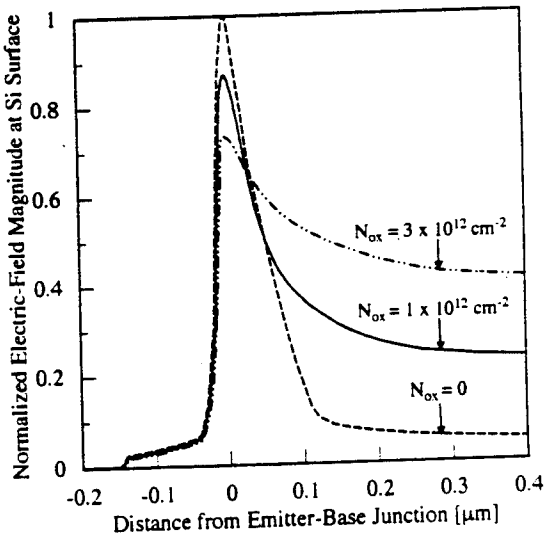


Fig. 6. The effect of radiation-induced positive oxide charge on the electric-field in the emitter-base depletion region of an npn BJT which is subjected to hot-carrier stress. Positive oxide charge significantly reduces the peak electric-field magnitude while spreading the depletion region.

IV. DISCUSSION

The results of this study demonstrate that the effects of radiation stress and hot-carrier stress on the current gain of npn BJTs are not simply additive. When these two stress types are applied to a BJT, the physical mechanisms by which they degrade device performance are considerably interactive. Although their interaction appears to be quite complex, the results presented suggest a simple model, which is consistent with accepted theory of the individual stress types, by which the combined effects of radiation stress and hot-carrier stress on current gain can be explained. Because the interaction is decidedly stronger when irradiation precedes hot-carrier stress, such a model is best developed by focusing on how radiation damage influences the way in which hot-carrier stress affects recombination current in the emitter-base depletion region.

The PISCES simulation results which relate oxide trapped charge to the electric-field in the emitter-base depletion region are of considerable importance in understanding the hot-carrier response of an irradiated npn BJT. Of particular relevance is the result that positive oxide charge acts to decrease the peak electric-field near the emitter-base junction. Physically this can be interpreted as a consequence of dropping a given base-to-emitter reverse bias, induced by hot-carrier stress, over a depletion region that increases in size with the addition of positive oxide charge. A decrease in the peak electric-field along the Si surface, E_p, corresponds to a decrease in the probability of hot-carrier injection, P_{ϕ_b}, according to the relation[26]

$$P_{\phi_b} \propto \frac{E_p}{\phi_b} \exp(-\frac{\phi_b}{\lambda E_p}), \qquad (3)$$

where λ represents the mean free path of the carriers, and ϕ_b represents the potential barrier presented by the oxide. Since a consequence of radiation stress is the creation of positive oxide trapped charge, it follows that the effect of radiation is to decrease the probability of subsequent hot-carier injection near the emitter-base junction. This realization accounts, in part, for the improvement in the hot-carrier response observed in the irradiated npn BJTs.

It should be noted that the increase in the electric-field far from the emitter-base junction which accompanies the spreading of the emitter-base depletion region could complicate the process of hot-carrier injection in modern bipolar structures having oxides much thinner than the 545 nm oxide used in the experimental test device. Even in the absence of oxide charge, a poly-Si emitter overlying an especially thin oxide can act as a field plate which creates a non-negligible electric-field in the extrinsic base beneath it[27]. The addition of radiation-induced positive oxide charge might be expected to increase the electric-field in such structures to magnitudes sufficient to create hot-carriers far from the emitter-base junction, thereby shifting localization of hot-carrier injection to a relatively large region of the emitter-base depletion region covering much of the extrinsic base.

In addition to altering the probability of hot-carrier injection throughout the emitter-base depletion region, radiation damage has a pronounced effect on the way in which injected carriers affect recombination current in the base. As evidenced by the reversal of current gain degradation demonstrated in this study, a significant amount of radiation-induced damage can be negated by the subsequent application of hot-carrier stress. Two defects widely studied in the radiation effects of Si-SiO_2 structures which are relevant to this transpiration are: (i) trapped holes in the bulk of the oxide[28-30], which are commonly associated with E' centers[31-34], a term used to describe unpaired electrons trapped on Si sp^3 orbitals projecting into O vacancies, and (ii) neutral electron trapping sites[35-38], also located in the oxide bulk, which are thought to be formed principally through the rupture of strained bonds in the creation of electron-hole pairs.

The process whereby current gain degraded by radiation is partially recovered most likely is due to a combination of two events occuring in the oxide overlying the emitter-base junction. In one event, some of the electrons injected into the oxide during hot-carrier stress recombine with trapped holes created by radiation, in which case the result is to neutralize those radiation-induced defects. In the second event, other injected electrons become captured by the neutral electron traps, thereby charging the traps negative and compensating remaining positive charges trapped in the oxide. In either case, the result of these electron capture processes is to decrease the electrostatic potential within the emitter-base depletion region and thereby decrease the recombination current measured at the base terminal. This reduction of excess base current and corresponding increase in current gain is a remarkable observation in that, until now, hot-carrier stress has been associated only with the degradation of BJT performance.

The reduction of excess base current does not continue indefinitely, however. As radiation damage is being neutralized and compensated by injected electrons, G-R centers are created continuously at the oxide interface. Since the G-R centers act to increase excess base current by increasing the surface recombination velocity, there exist competing mechanisms by which current gain is affected. An expression formalized elsewhere[39] which allows the assessment of the relative contributions of these mechanisms to the excess base current which flows at the surface of the base is

$$\Delta I_B \propto N_T [L_{R_p} + K_1 \exp(\frac{N_{ox}^2}{K_2})], \qquad (4)$$

where N_T and N_{ox} represent the densities of G-R centers and oxide charge, respectively, L_{R_p} refers to the location of the peak in surface recombination velocity, and K_1 and K_2 are constants unrelated to stress. Both terms in this expression contribute to the excess base current in an irradiated BJT, whereas, for hot-carrier stress, primarily the first term contributes. Because of the keen sensitivity of excess base current to changes in the oxide charge density,

the reduction in the density of radiation-induced positive oxide charge by hot-carrier stress initially drives the excess base current down, even as G-R centers are being created. After positive charge in the oxide has been reduced sufficiently, its contribution to excess base current becomes dominated by that of the G-R centers, and the excess base current begins to increase again. The excess base current never returns to zero, because the process of positive oxide charge reduction itself creates G-R centers, and because the injection of electrons which precipitates the reduction is localized near the emitter-base junction.

Since the effects of radiation damage on subsequent hot-carrier stress generally are to hamper the increase in excess base current, while hot-carrier damage has little effect on subsequent radiation stress, current gain degradation in npn BJTs due to a combination of the two stress types is least severe when radiation stress precedes hot-carrier stress. Alternatively, a bound on current gain degradation is achieved when hot-carrier stress is performed before irradiation. These results should be taken into account in the design and reliability testing of npn BJTs to be used in environments in which they will be subjected to both ionizing radiation and hot-carrier stress.

V. SUMMARY

Identical npn BJTs were characterized experimentally after subjecting them to various combinations of ionizing radiation and hot-carrier stress. The experiments emphasized assessment of the importance of the stress type sequence in determining the magnitude of current gain degradation. The results indicate that the effects of the two stress types on current gain are not simply additive. Degradation of current gain is less severe when irradiation precedes hot-carrier stress than it is when the order of the stress types is reversed. The importance of the stress type sequence is attributed primarily to an improvement in the hot-carrier response of the BJT due to radiation damage. It has been demonstrated that hot-carrier stress initially reduces excess base current and improves current gain in irradiated BJTs. PISCES simulations, which mimicked the hot-carrier stressing of an irradiated npn BJT, revealed that net positive oxide charge induced by radiation significantly reduces the peak electric-field in the emitter-base depletion region. A qualitative model based on the probability of hot-carrier injection determined by radiation damage and on the neutralization and compensation of radiation-induced positive oxide charge by injected electrons has been proposed to explain the interaction of ionizing radiation and hot-carrier stress in npn BJTs. The results are useful in bounding the damage expected from the combined stresses of ionizing radiation and hot-carriers and should be taken into account when designing and testing npn BJTs for use in mixed environments.

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V.N. Simple Technique for Improving the Hot-Carrier Reliability of Single-Poly Bipolar Transistors

Simple Technique for Improving the Hot-Carrier Reliability of Single-Poly Bipolar Transistors

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Abstract – It is shown experimentally and through simulation that reduced screen oxide thickness leads to increased breakdown voltage of the emitter-base junction (BV_{ebo}) and reduced peak electric field at breakdown, which translates into improved hot-carrier reliability. The effect of reduced screen oxide thickness on the peak cutoff frequency is minimal. For these devices, thinning the screen oxide from 55 to 35 *nm* increases BV_{ebo} by 0.2 *V*, improves the hot-carrier-induced excess base current by more than an order of magnitude at a base-emitter voltage of 0.6 *V*, and degrades the peak cutoff frequency by only 3 percent.

I. INTRODUCTION

The current gain I_C/I_B of bipolar transistors is degraded when the emitter-base junction is reverse biased [1], as it is in normal BiCMOS circuit operation [2]. The stress leads to excess base current in the device and no change in the collector current. The excess base current is caused by increased surface recombination velocity due to surface damage created during the stress [3, 4]. The surface damage is proportional to the injected hot electron current [3, 5].

The injected electron current into the oxide depends on the strength of the electric field at the oxide-silicon interface near the emitter base junction [6, 7]. By reducing the electric fields in this region through tailoring the impurity profile, improved hot-carrier and breakdown performance of bipolar devices has been reported [8].

In this work, we show that similar improvements in bipolar hot-carrier and breakdown performance can be obtained by reducing the screen oxide thickness over the extrinsic base. The emitter polysilicon that is extended over the oxide to account for mask alignment design rules can reduce the surface electric fields during reverse-bias stress, and thus increase the breakdown voltage and suppress hot-carrier effects. The action of the polysilicon overlap is identical to that of the field-plate technique that is commonly used for high-voltage junction termination [9]. The field plate technique is extremely simple to implement, unlike profile tailoring methods, which require precise control of the impurity distribution to be effective [8].

We also investigate the effect of screen oxide thickness on cutoff frequency, f_T. It is shown that at high current levels where the peak cutoff frequency occurs, the cutoff frequency is limited by the transit time and not by capacitive terms. The increased capacitance due to the reduced screen oxide thickness becomes more important at lower current levels, but the effect is still relatively small.

II. EXPERIMENTAL DETAILS

A cross-section of the devices studied in this work is shown in figure 1. These devices are NPN polysilicon emitter bipolar transistors fabricated in a BiCMOS process closely related to that described in [10]. The surface doping of the extrinsic base is $7.8 \times 10^{17}\ cm^{-3}$, and the emitter size is $2 \times 15\ \mu m$.

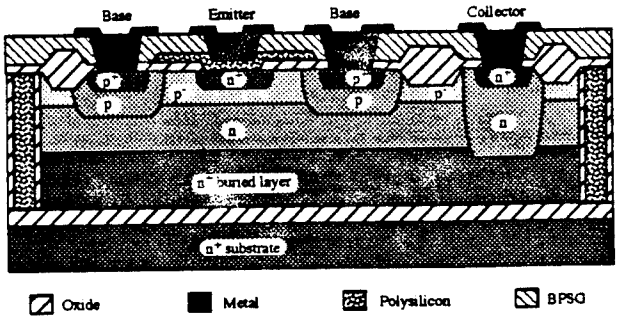


Figure 1. Representative cross-section of the devices studied in this work.

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Different screen oxide thicknesses were obtained by varying the HF dip time of the devices after the base implant through the screen oxide. The final screen oxide thicknesses were determined by capacitance measurements on MOS test structures. Except for the different HF dip times, all devices received the same processing. All the devices had nominally identical measured dc current gain.

III. Experimental Results

The reverse characteristics of the emitter-base junction for three of the devices with different screen oxide thicknesses are shown in figure 2. It is seen that reduced screen oxide thickness leads to higher breakdown voltage. This indicates that the surface electric fields have been reduced by the influence of the emitter polysilicon on the surface potential in the extrinsic base.

The devices were stressed with a constant reverse current of 900 *nA* for a total of 10,000 seconds. This current places the emitter-base junction well into avalanche breakdown, as seen in figure 2. Constant current stress ensures that the same amount of avalanching is occurring in each device, although the voltage that develops across the junction during the stress is different.

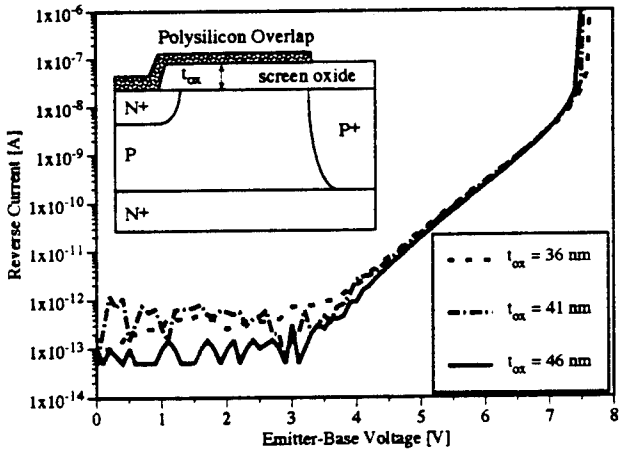


Figure 2. Measured reverse characteristics of the emitter-base junction for three different screen oxide thicknesses.

The base current is written as the sum of pre-stress and excess current as $I_B = I_{B,pre} + \Delta I_B$. The excess base current, ΔI_B, measured at a base-emitter voltage of 0.6 *V* is plotted versus increasing hot-carrier stress time in figure 3. It is seen that thinner oxides lead to improved hot-carrier performance. Interestingly, although the breakdown voltage of the junction has only been increased by about 0.2 V as the oxide thickness decreases from 46 to 30 nm, as seen in figure 2, the hot-carrier performance improves by nearly an order of magnitude, as seen in figure 3.

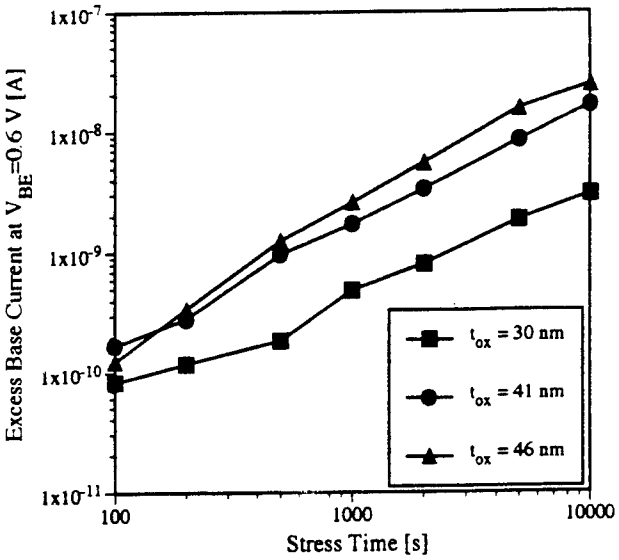


Figure 3. Excess base current at a base-emitter voltage of 0.6 V versus stress time for three different screen oxide thicknesses.

IV. Modeling

Interface trap creation in BJTs due to hot carrier stress is proportional to the hot-electron current, J_{hot}, injected into the oxide during the stress [3, 5]. The increase in interface trap density, N_T, causes an increase in surface recombination velocity, v_{surf}, where $v_{surf} = \sigma\, v_{th}\, N_T$, σ is the capture cross-section, and v_{th} is the thermal carrier velocity. This causes increased recombination in the emitter-base depletion region and reduces the current gain [3 – 5].

In figure 4, PISCES-simulated [11] breakdown voltage and peak electric field at breakdown of the emitter-base junction is plotted versus the screen oxide thickness. The doping profiles were obtained using SUPREM simulations and were verified using spreading resistance measurements. Good agreement with experimental breakdown voltage data, indicated with error bars, is evident. It is seen that as oxide thickness is decreased, the peak surface electric field at breakdown decreases. Physically, the reduced surface electric fields mean that more avalanching is occurring away from the oxide-silicon interface, which translates into a reduced probability of hot-electron injection [6, 7]. Since J_{hot} decreases, v_{surf} and thus ΔI_B decreases for a given stress time. This explains the experimentally-observed trend in figure 3 that reduced screen oxide thickness leads to improved hot-carrier reliability.

In figure 5, PISCES-simulated cutoff frequency is plotted versus collector current for a wide range of oxide thicknesses. It is seen that oxide thickness affects the cutoff frequency at low current levels, and has a negligible effect at the higher current levels.

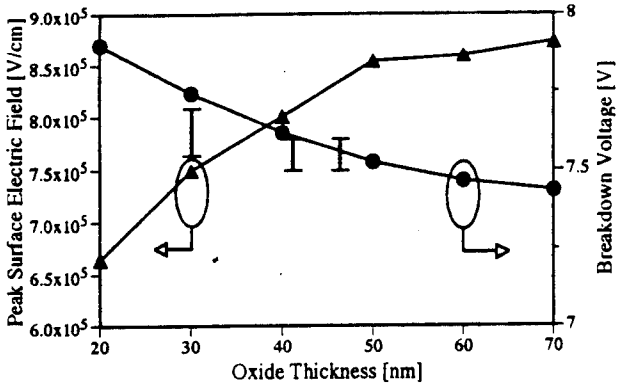


Figure 4. PISCES-simulated peak surface electric field at breakdown and junction breakdown voltage versus screen oxide thickness. The range of experimental breakdown voltage data is indicated with error bars.

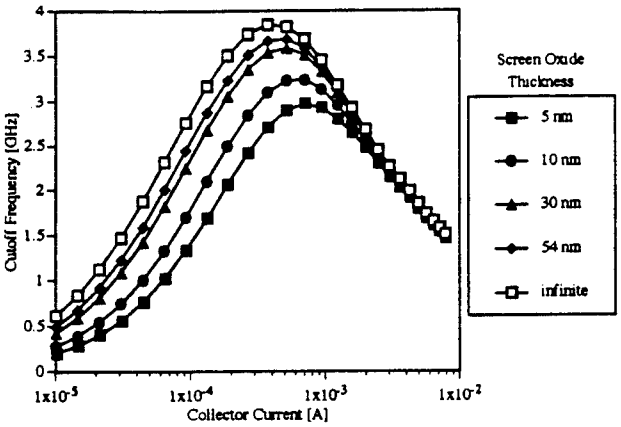


Figure 5. PISCES-simulated cutoff frequency at $V_{CE} = 2\ V$ versus collector current for several screen oxide thicknesses.

The cutoff frequency in a BJT may be expressed as

$$\frac{1}{2\pi f_T} = \frac{1}{I_C}\left[\frac{kT}{q}\left(C_{je} + C_{jc}\right)\right] + \tau_t + R_C C_{jc} \qquad (1)$$

where I_C is the collector current, τ_t is the transit time for electrons, kT/q is the thermal voltage, C_{je} is the emitter junction capacitance, C_{jc} is the collector junction capacitance, and R_C is the collector resistance. When I_C is large, τ_t dominates the cutoff frequency, and the increase in C_{je} due to the reduced screen oxide thickness has little effect. As I_C is reduced, C_{je} has more of an effect on the cutoff frequency, as seen in figure 5. The maximum cutoff frequency, $f_{T,max}$, is plotted versus oxide thickness in figure 6. It is seen experimentally that, for the oxide thicknesses in the 35 to 55 nm range, the effect on $f_{T,max}$ is indeed minimal.

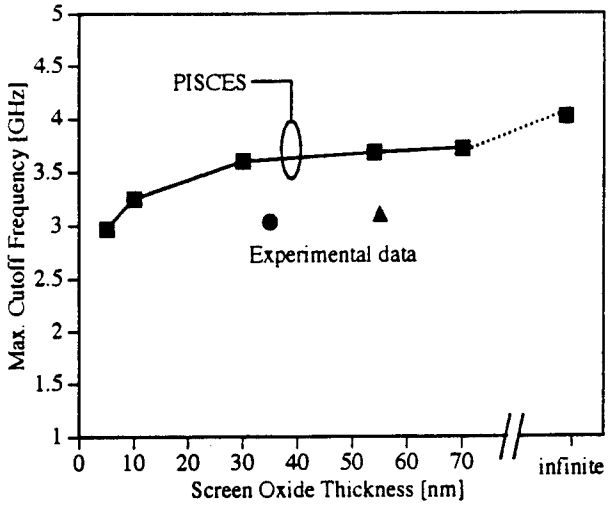


Figure 6. Experimental and PISCES-simulated maximum cutoff frequency at $V_{CE} = 2\ V$ versus screen oxide thickness.

SUMMARY

Improved hot-carrier performance in BJTs through the use of a field-plate junction termination technique was reported. By reducing the screen oxide thickness over the extrinsic base, higher junction breakdown voltage and less current-gain degradation during constant current stressing was observed. The effect on cutoff frequency was shown to be minimal at high current levels and more important at lower current levels.

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V.O. Visualization of Ionizing-Radiation and Hot-Carrier Stress Response of Polysilicon Emitter BJTs

VISUALIZATION OF IONIZING-RADIATION AND HOT-CARRIER STRESS RESPONSE OF POLYSILICON EMITTER BJTs

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ABSTRACT

Process and device simulation software tools are used to produce an animated visualization of the mechanisms involved in the ionizing-radiation and hot-carrier stress responses of BJTs. A physically-based model is presented, which compares ionizing-radiation response with hot-carrier response in polysilicon-emitter BJTs. During ionizing radiation, positive charge accumulates along the oxide-silicon interface. The accumulated charge causes excess base current to flow, characterized by an ideality factor between one and two for low total doses of ionizing radiation, and an ideality factor of two for high total doses of ionizing radiation. During hot-carrier stress, the oxide damage is localized near the emitter-base junction, and the excess base current has an ideality factor of two.

INTRODUCTION

The current gain, I_C/I_B, for BJTs is reduced after exposure to ionizing radiation [1-4], or after the emitter-base junction is strongly reverse-biased [5]. The gain decreases in both cases, as damage to the oxide over the emitter-base junction causes the base current to increase, while the collector current remains approximately constant. The excess base current, ΔI_B, is caused by recombination in the emitter-base depletion region, as a result of the introduction of positive oxide charge and interface states at the oxide-silicon interface [3-4]. Trapped positive charge along the interface increases the surface potential in the extrinsic base. This increase in potential depletes the extrinsic base and causes excess base current to flow [3-4]. For hot-carrier stress, ΔI_B is caused primarily by interface states concentrated in the oxide over the emitter-base junction during reverse-bias stress [6-10]. For ionizing radiation, ΔI_B is caused by an interactive combination of interface states and trapped oxide charge [3-4].

A physical model, based on the mechanisms described above, has been proposed for the recombination current in the extrinsic base [11]. As the surface potential increases due to trapped positive charge, the region of high recombination broadens and moves into the extrinsic base. When sufficient charge has been accumulated to bring the surface of the extrinsic base to the crossover condition (n = p), further increases in charge move the recombination peak away from the surface and into the bulk [3]. The movement of the recombination peak is a complex phenomenon that varies in two dimensions and also with time, making it very difficult to represent in static form. An intuitive understanding of the movement of recombination current from the surface to the subsurface of the extrinsic base is significantly enhanced with the aid of computer simulation.* In this work, a series of graphic solution plots were time-sequenced to form an animated two-dimensional representation of recombination rate versus position in the device, as different amounts of positive charge were introduced into the emitter-base junction oxide. This paper describes the mechanisms responsible for the gain degradation and explains how the simulation tools can be used to understand the effects.

EXPERIMENT

The devices studied are NPN polysilicon emitter bipolar transistors fabricated in a BiCMOS process [12]. Emitter geometry ranges from 1.5 μm x 1.5 μm to 14 μm x 14 μm, and includes 2 μm x 50μm and 2 μm x 15 μm devices. A representative cross-section of a device is shown in Fig. 1.

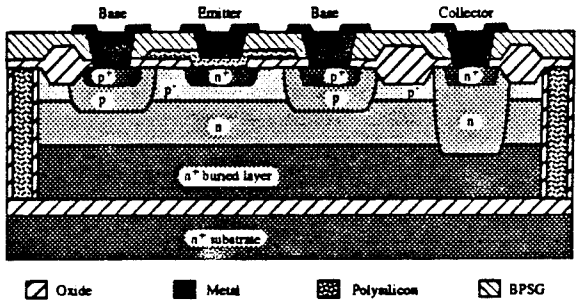


Figure 1. NPN Polysilicon Emitter BJT: Cross section view.

Some of the devices were irradiated with 10 keV X-rays at a dose rate 1.7 krad(SiO_2)/s up to a total dose of 1 Mrad(SiO_2). All pins were grounded during irradiation. Other devices were subjected to a constant reverse current of 2 μA through the base-emitter junction with the collector open for a total of 2,048 seconds. This value of constant current places the base-emitter junction well into avalanche breakdown.

The normalized current gains versus base-emitter voltage for irradiation and hot-carrier stress are plotted in Fig. 2 and Fig. 3, respectively. Notice that the current gain decreases as the total dose increases and also as the hot-carrier stress time increases. Also note that the graphs of both stress types appear to be qualitatively similar.

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* Simulation tools provided by SILVACO International

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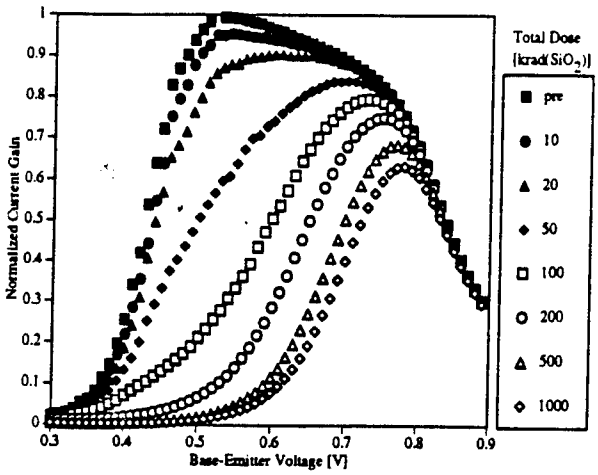


Figure 2. Normalized current gain versus base-emitter voltage for various values of total ionizing dose.

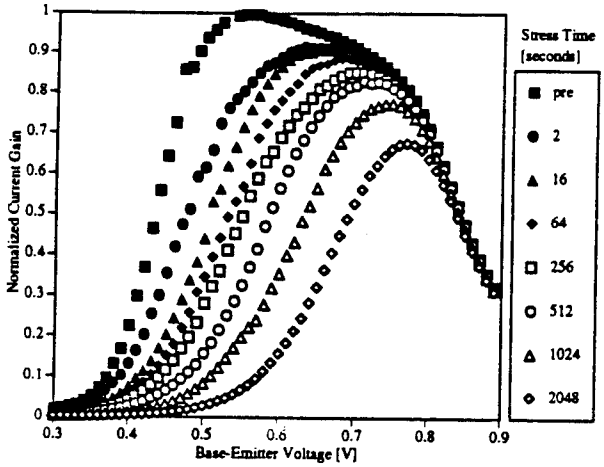


Figure 3. Normalized current gain versus base-emitter voltage for various values of hot-carrier stress time.

The net base current I_B, defined as

$$I_B = I_{B,pre} + \Delta I_B$$

where $I_{B,pre}$ is the device base current before stress, and ΔI_B is the recombination current in the emitter-base depletion region due to irradiation or hot-carrier stress.

Recombination current, ΔI_B, in P-N junctions varies as

$$\Delta I_B = \Delta I_{BO} \exp\left[V/(nV_T)\right]$$

where V_T is the thermal voltage (kT/q), ΔI_{BO} is a device-dependent constant, and n, the ideality factor, depends on the oxide charge and forward voltage, V. Figure 4 and Figure 5 show plots of excess base current, ΔI_B, versus base emitter voltage, V_{BE}, for irradiation and hot-carrier stress, respectively. From Fig. 4, for low total dose, the curves have a slope corresponding to an ideality factor of n = 2 for large V_{BE} and a slope corresponding to $1 < n < 2$ for small V_{BE}. For relatively high total doses, the excess base current exhibits n = 2 for nearly the entire voltage range. The curves in Fig. 5 exhibit an ideality factor of n = 2 for all stress times. An ideality factor of n = 2 denotes predominantly bulk recombination, while $1 < n < 2$ denotes predominantly surface recombination [3].

The movement of recombination current from surface to subsurface is an inherently two-dimensional effect, which does not lend itself to visualization in static media. A useful way to demonstrate the effect is to have it visually represented by animating two-dimensional representations of the recombination rates throughout the device structure for different stress levels.

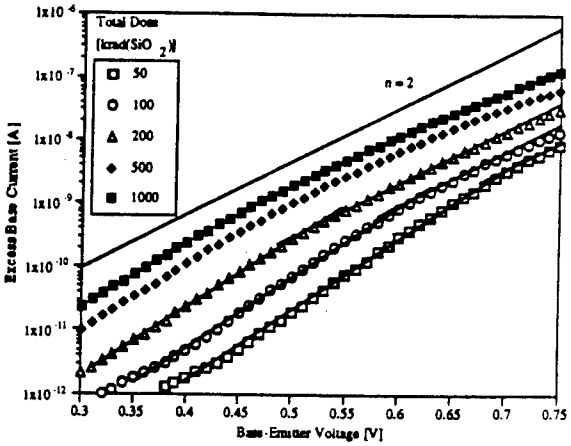


Figure 4. Excess base current versus base-emitter voltages for different values of total ionizing dose.

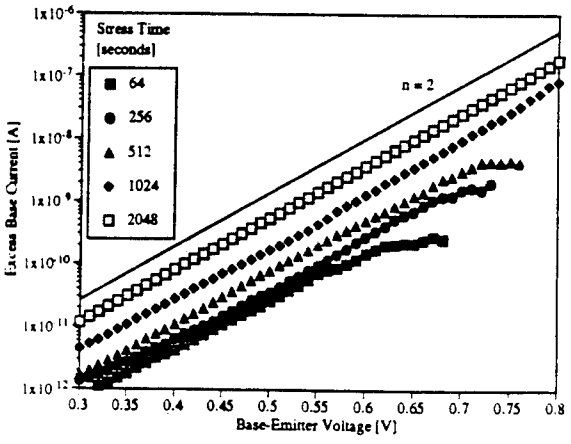


Figure 5. Excess base current versus base-emitter voltage for increasing levels of hot-carrier stress time.

SIMULATIONS

The devices were simulated using the two-dimensional SPISCES code [13]. The doping profiles were obtained from SSUPREM4 [14] and verified with spreading resistance measurements. The electrical characteristics of the simulated device were chosen to match the parameters of the real device as closely as possible.

The effects of ionizing radiation were simulated by introducing positive charge at the oxide interface along the base and emitter. Hot-carrier stress was modeled by increasing the surface recombination velocity near the emitter-base junction. This simulation approach is consistent with results obtained using charge-separation techniques and test structures [3,11,15]. The movement of recombination current from surface to subsurface may be visualized by examining Figs. 6 through 9.

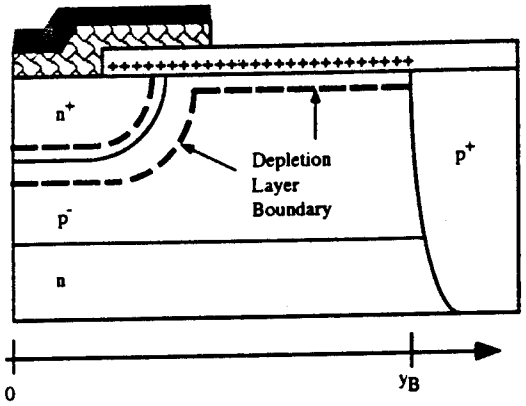


Figure 6. Schematic cross-section of the base-emitter junction showing the effect of oxide charge on the depletion layer.

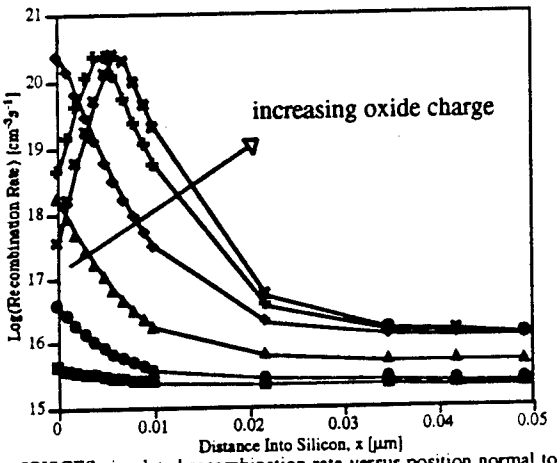


Figure 7. SPISCES simulated recombination rate versus position normal to the interface for V_{BE} = 0.5 V and various amounts of positive oxide charge.

Figures 7 through 9 are obtained from SPISCES simulations, and they demonstrate the movement of the recombination current into the substrate, as positive charge is added along the oxide interface.

Sequenced solution plots are cascaded, as discrete amounts of positive charge are added to the oxide interface. These static individual solutions can be animated and visualized. This technique presents an intuitive and dynamic view of recombination mechanism information, such as the recombination rates shown in Figs. 7 and 8, and the excess base currents shown in Fig. 9.

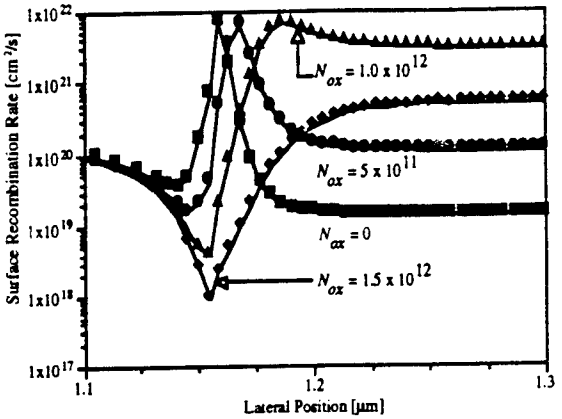


Figure 8. SPISCES-simulated surface potential and surface recombination rate versus lateral position near the emitter-base junction. The base-emitter voltage is 0.5 V with various amounts of oxide charge, N_{ox}, in units of cm^{-2}.

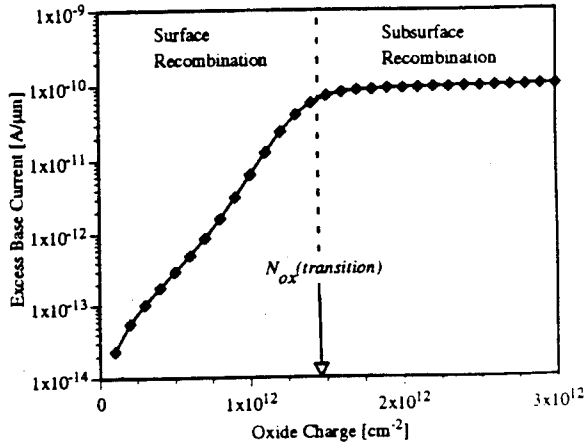


Figure 9. SPISCES-simulated excess base current versus oxide charge.

Note that as the oxide charge is increased, the recombination peak moves subsurface. When there is sufficient oxide charge to bring the surface of the extrinsic base to the crossover condition (n = p), further increases in charge move the recombination peak away from the surface and into the bulk, as seen in Fig. 8. This effect is further illustrated in Fig. 9, showing excess base current versus oxide charge. Note from Fig. 9 that after a critical value of oxide charge has been introduced, the excess base current stops increasing and appears to saturate due to the recombination movement below the surface of the extrinsic base. Any oxide charge added, in excess of the critical value of oxide charge, does not affect the recombination rate due to the subsurface movement of recombination, and so does not affect the excess base current [15-16].

The damage due to ionizing radiation is limited, because for N_{ox} greater than some critical value, recombination current flows primarily below the oxide-silicon interface. The device then becomes insensitive to further increases in surface damage [15-16]. The damage due to hot-carrier stress, however, is proportional to the amount of charge passed through the emitter-base junction [8,17].

CONCLUSION

A physically-based model for current gain degradation caused by irradiation and hot-carrier stress in BJTs has been presented. The validity of the model is demonstrated by physically-based device simulation using SPISCES device simulation software. Visualization of the degradation dynamics, using device simulation tools is an effective method to represent the process of change in recombination current due to stress, resulting in current gain degradation.

ACKNOWLEDGEMENTS

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V.P. Relaxation of Si-SiO_2 Interfacial Stress in Bipolar Screen Oxides due to Ionizing Radiation

RELAXATION OF Si-SiO_2 INTERFACIAL STRESS IN BIPOLAR SCREEN OXIDES DUE TO IONIZING RADIATION†

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Abstract

Current gain degradation due to ionizing radiation in complementary single-crystalline emitter bipolar transistors was found to grow progressively worse upon subjecting the transistors to repeated cycles of radiation exposure and high-temperature anneal. The increase in radiation sensitivity is independent of the emitter polarity or geometry and is most dramatic between the first and second radiation and anneal cycles. In parallel with the current gain measurements, samples from a monitor wafer simulating the screen oxide region above the extrinsic base in the npn transistors were measured for mechanical stress while undergoing similar cycles of irradiation and anneal. The oxide on the monitor wafer consisted of a 45 nm thermal layer and a 640 nm deposited layer. The results indicate that ionizing radiation helped relieve compressive stress at the Si surface. The magnitude of the stress change due to radiation is smaller than the stress induced by the emitter contact metallization followed by a post-metallization anneal. Correlation of radiation sensitivity in the bipolar transistors and mechanical stress in the monitor wafer suggests that mechanical stress may be influential in determining the radiation hardness of bipolar transistors and lends validation to previously reported observations that Si-SiO_2 interfaces are increasingly more susceptible to radiation damage with decreasing Si compressive stress. Possible mechanisms for the observed changes in stress and their effect on the radiation sensitivity of the bipolar transistors are discussed.

I. INTRODUCTION

It has been reported in a number of related studies that mechanical stress is strongly linked to the radiation hardness of Si-SiO_2 structures. In Al-gate metal-oxide-silicon capacitors (MOS-Cs), stress distributions modified by systematic variations in gate geometry[1], gate thickness[2] and time lapse following post-metallization anneal (PMA)[3] have been correlated with radiation sensitivity. Similar dependences on gate-induced stress of the radiation hardness of silicide-gate MOS-Cs[4] and the annealing of radiation-induced interface traps in Al-gate MOS-Cs[5] have been reported. In related work, x-ray photoelectron spectroscopy (XPS) studies have revealed a link between the radiation hardness of thermal oxides and the concentration of strained bonds near the Si-SiO_2 interface[6,7]. Since disclosure of these results, numerous improvements in the radiation hardness of metal-insulator-semiconductor (MIS) devices have been attributed to modifications in Si-SiO_2 interfacial stress. Notable examples include the reduction in radiation sensitivity of MOS-Cs due to the incorporation of Cl[8], F[9] or N[10] into the oxide layer and improvements in the radiation tolerance of thermal oxides prepared by rapid thermal oxidation at increased oxidation temperatures[11].

One particular collection of work relating mechanical stress to the radiation sensitivity of MIS devices has drawn considerable attention due to its potential significance for device hardening. This work reports dramatic improvements in the radiation hardness of MOS-Cs[12], metal-oxide-nitride-oxide-silicon capacitors (MONOS-Cs)[13] and metal-oxide-silicon field effect transistors (MOSFETs)[14] due to repeated cycles of ionizing radiation and high-temperature anneal. The authors suggest that radiation itself is an impetus for improving the radiation hardness of MIS devices through a change in Si-SiO_2 interfacial stress, although they make no measurements to quantify any effects of radiation on stress. Whereas radiation-induced changes in the mechanical stress of metal-oxide-silicon (MOS) device materials have been observed[15], very little is actually known about the direction in which ionizing radiation may change stress in Si-SiO_2 structures, the magnitude of any such changes, or the physical mechanisms by which these changes may occur.

In integrated bipolar junction transistors (BJTs), the Si-SiO_2 interface immediately above the emitter-base junction plays a very important role in the device's radiation response. The oxide at this interface typically is used as a screen for base implants and may include a deposited layer. Ionizing radiation degrades current gain in BJTs by introducing trapped net positive charge and interface traps into the oxide[16,17]. The positive oxide trapped charge spreads the emitter-base depletion region, which results in increased recombination current in the base under forward-biased operation of the junction[18,19]. Radiation-induced interface traps, especially those near midgap, serve as generation-recombination (G-R) centers through which recombination current in the base is further increased due to

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enhanced surface recombination velocity[20]. The defects generated by radiation degrade current gain, since they increase base current while affecting the collector current negligibly. Given the relationship of radiation damage and mechanical stress observed in MIS devices, stress might also be expected to play a role in the radiation response of BJTs. Furthermore, because of the implications for hardening BJTs to radiation, it is of considerable interest to examine the effect of radiation and anneal cycles on the radiation hardness of BJTs as has been done with MIS devices.

In this study, complementary single-crystalline emitter BJTs with oxides consisting of a thermal layer and a thick deposited layer were characterized for radiation-induced current gain degradation while receiving repeated cycles of ionizing radiation and high-temperature anneal. In parallel, monitor wafers processed with the same two-layer oxide were measured for mechanical stress while undergoing similar cycles of irradiation and anneal. It is shown that compressive stress existing in the Si prior to irradiation is relieved slightly by the radiation process. In contrast with claims made for MIS devices, radiation and anneal treatments degrade the radiation hardness of the BJTs. Correlation of radiation sensitivity in the BJTs and stress in the monitor wafers is consistent with previously reported observations of MOS structures that decreasing compressive Si stress leads to increased radiation sensitivity, suggesting that the changes in device radiation hardness due to repeated cycles of irradiation and anneal may be explained, at least in part, by radiation-induced changes in stress.

II. EXPERIMENT

A. Description of BJT Technology

The bipolar transistors investigated in this work were fabricated on bonded (100) silicon-on-insulator wafers in a complementary bipolar process[21] and mounted in ceramic dual-in-line packages. The devices are dielectrically isolated by a trench etch and refill process and have standard single-crystalline emitters with emitter geometries of either a single 1.5 x 1.5 μm^2 square or three 1.5 x 10 μm^2 rectangular stripes. The oxide above the emitter-base junction consists of a 640 nm layer deposited by low-pressure chemical vapor deposition (LPCVD) on a 45 nm thermal layer grown in dry O_2. The thermal oxide is used as a screen for base implants in both the npn and pnp devices. Relevant device parameters are listed in Table I, while a cross-section of the npn device is shown in Fig. 1(a). The cross-section is useful for visualizing the physical mechanisms by which ionizing radiation degrades current gain in the device.

The Si-SiO_2 interface above the extrinsic base is where mechanical stress is most relevant to the device's radiation response, since it is this oxide where radiation damage has the greatest effect on current gain. However, because the small target area and the complexity of overlying materials preclude meaningful strain measurements at this interface by x-ray diffraction, a monitor wafer from the same bipolar process was specially fabricated for the purpose of strain characterization. The monitor wafer was processed with the same two-layer oxide and p-type base over its entire surface as exist in the fully-processed npn BJT. On half of the wafer, the emitter contact metallization was simulated by sputtering a 75 nm Ti barrier layer and a 750 nm Al layer over the oxide. Following metallization, the wafer was annealed at 450 °C for 30 min in N_2. Finally the wafer was cut into 1.5 cm x 3 cm pieces suitable for mounting in the x-ray diffractometer. A cross-section of the monitor wafer is provided in Fig. 1(b), and the region in the BJT simulated by the monitor wafer is emphasized in Fig. 1(a) for clarity. As stress in the fully-processed BJT may be exacerbated by additional material layers and geometry constraints, it should be made clear that the monitor wafer is intended only to provide a fair qualitative understanding of the effects of radiation on mechanical stress in the base of the BJT and not an exact assessment of stress in the base at any point in the experiment.

Table I. Relevant Device Parameters

Parameter	npn	pnp
oxide thickness [nm]	685	685
emitter-base junction depth [nm]	300	300
active base width [nm]	800	800
peak extrinsic base doping [10^{18} cm^{-3}]	1.1	3.2
peak current gain	65	40
V_{BE} at peak current gain [V]	0.65	-0.58

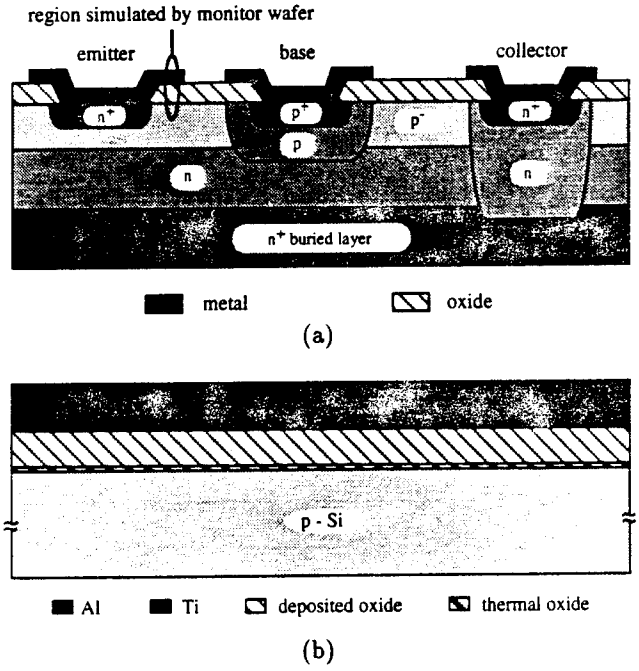


Fig. 1. (a) A cross-section of the npn bipolar transistor investigated in this work emphasizing the region simulated by the monitor wafer. (b) A cross-section of the monitor wafer used for the mechanical stress measurements.

B. Effect of Radiation and Anneal Cycles on BJT Radiation Hardness

Six groups of BJTs were investigated individually for radiation-induced current gain degradation while undergoing a total of four cycles of ionizing radiation exposure and high-temperature anneal. Each group consisted of two npn devices and two pnp devices, where the two devices of either polarity had different emitter geometries. Any given group received the same total dose from cycle to cycle, but the total doses administered to the six groups varied from 250 to 4,000 Gy(SiO_2) per cycle. The irradiations were performed with a ^{60}Co γ-source at a dose rate of 40 Gy(SiO_2) hr^{-1}, during which the devices were situated in a box made of Pb and Al designed to filter low-energy photons. Annealing of radiation damage was performed at 275 °C in N_2 until current gains were restored to their pre-radiation values. The required anneal times varied between 10 and 50 hr depending on the level of radiation damage. All device terminals were grounded during both the irradiation and anneal steps. The temperature at which the current gains were measured varied less than 2 °C over the course of the experiment.

Current gain characteristics prior to any radiation exposure and following the first, second and third exposures to radiation are shown for a representative device in Fig. 2. These particular characteristics were measured for a 45 μm^2 npn device that received a total dose of 700 Gy(SiO_2) per cycle. All current gains are normalized by the pre-radiation peak current gain and are shown as a function of base-to-emitter voltage. Gain characteristics following each complete radiation and anneal cycle were indistinguishable from the pre-radiation characteristics. Over a wide range of base-to-emitter voltages, it is clear that radiation-induced current gain degradation grows more severe with an increasing number of radiation and anneal cycles. The increase in radiation sensitivity is most severe following the first cycle and diminishes with subsequent cycles. Virtually no change in the radiation response was observed between the third and fourth exposures to radiation. Similar differences in the post-radiation current gain characteristics due to repeated cycles of radiation exposure and anneal were observed for all other devices characterized.

These trends are illustrated in another form in Fig. 3 along with data from the other devices subjected to identical cycles of radiation exposure and anneal. Here normalized current gain following irradiation to a total dose of 700 Gy(SiO_2) is plotted as a function of the number of radiation and anneal cycles given to each device prior to irradiation. The current gains were measured at a base-to-emitter voltage magnitude of 0.6 V. The differences in the amount of current gain degradation sustained by the various devices reflect emitter geometry and polarity dependences reported elsewhere[22]. The ascertainment that device radiation sensitivity is increased following repeated cycles of radiation and anneal, especially following the first cycle, is seen here to be independent of the emitter polarity or geometry.

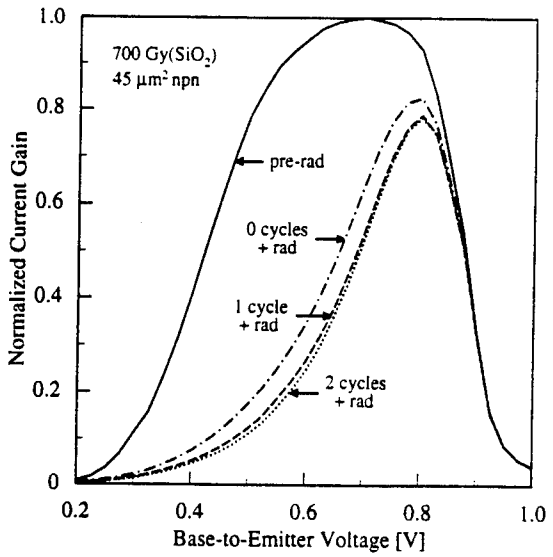


Fig. 2. Effect of radiation and anneal cycles on radiation-induced current gain degradation in a representative device. Gain degradation increases with an increasing number of cycles over a wide range of base-to-emitter voltages.

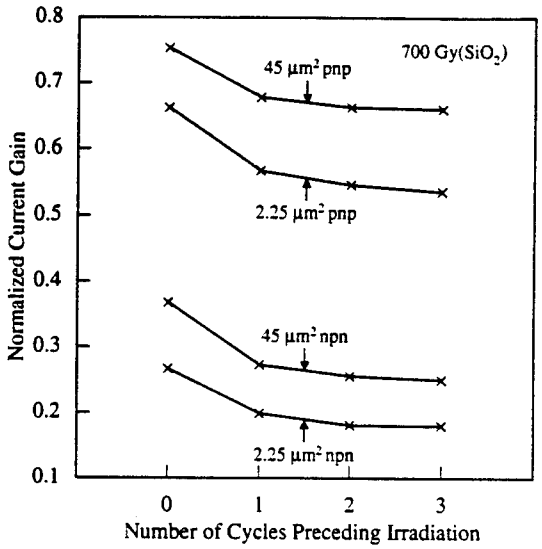
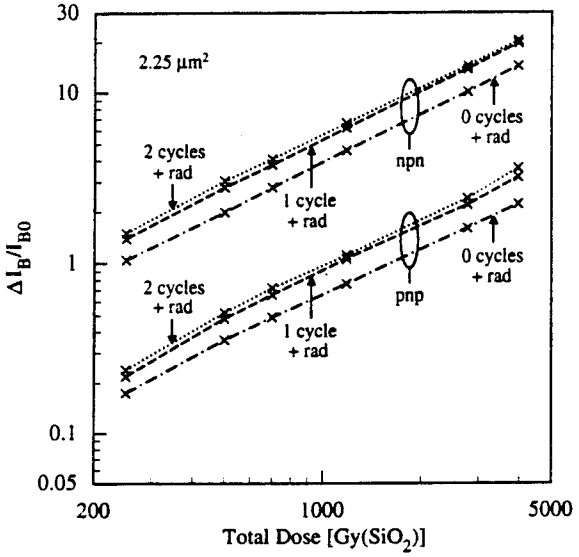


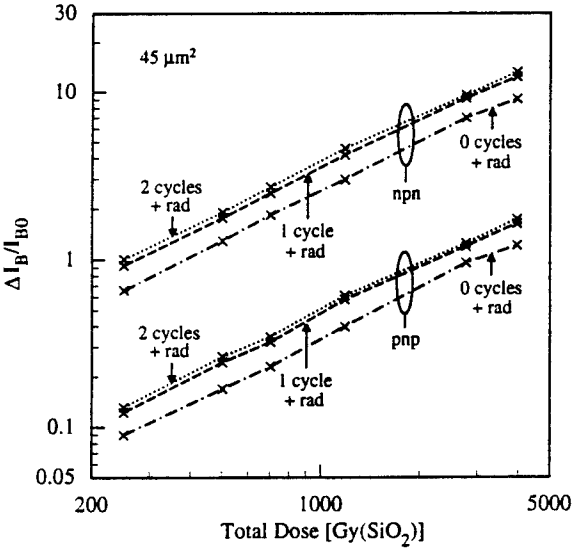
Fig. 3. Effect of radiation and anneal cycles on radiation-induced current gain degradation in a representative group of devices. Gain degradation increases with an increasing number of cycles independent of emitter polarity or geometry. All data were measured at $|V_{BE}| = 0.6$ V.

Fig. 4 shows the changes in radiation-induced current gain degradation to be manifested in the excess base current, ΔI_B, where excess base current is defined as the increase in base current due to radiation exposure. Excess base currents following the first, second and third irradiations are plotted in Figs. 4(a) and 4(b) for all of the 2.25 μm^2 and 45 μm^2 test devices, respectively, as a function of the total dose delivered per cycle. The excess base currents were measured at a base-to-emitter voltage mag-

nitude of 0.6 V and are normalized by the pre-radiation values of base current in order to account for part-to-part variations. These results establish that the trends in increased radiation sensitivity due to repeated cycles of radiation and anneal for devices of any emitter polarity and geometry combination are apparent over a wide range of total doses. Although the data are not presented in this work, similar changes in the radiation sensitivity of polycrystalline emitter BJTs due to repeated cycles of radiation and anneal were observed, indicating this to be a common response in BJTs.



(a)



(b)

Fig. 4. Effect of radiation and anneal cycles on radiation-induced excess base current for (a) the 2.25 μm^2 devices and (b) the 45 μm^2 devices. Excess base current increases with an increasing number of cycles over a wide range of total doses. All data were measured at $|V_{BE}| = 0.6$ V.

C. Effect of Radiation and Anneal Cycles on Si-SiO₂ Interfacial Stress

Monitor wafer samples simulating the Si-SiO_2 interface above the base of the npn BJTs were measured for mechanical stress while undergoing two cycles of radiation and anneal similar to those applied to the fully-processed BJTs. Two samples with metallization and two samples without metallization were characterized. Before beginning the experiment, stresses in the samples were allowed 100 hr following the PMA to reach equilibrium. Irradiation of the samples was performed with a ^{60}Co γ-source at a dose rate of 40 Gy(SiO_2) hr^{-1}. One metallized sample and one unmetallized sample were given a total dose of 500 Gy(SiO_2) per cycle, while the remaining two samples received a total dose of 4,000 Gy(SiO_2) per cycle. The anneal steps were performed at 275 °C in N_2 for 10 hr. No bias was applied to the samples during the course of the experiment. The stress measurements were performed 24 hr following the completion of each irradiation or anneal step.

Values for mechanical stress at the Si surface were computed from x-ray diffraction measurements[23] taken at room temperature with a powder theta-theta diffractometer. X-rays emitted from a Cu source were directed through the amorphous SiO_2 layer onto the Si surface of the sample under test. The angle of x-ray incidence relative to the Si surface was varied until a peak in the intensity of the radiation reflected from the {400} planes was achieved for each of the k_{α_1} and k_{α_2} wavelengths. The reflection of the x-rays is illustrated in Fig. 5, where the relevant geometry in the Si is emphasized. The strained lattice constant was calculated in each case according to Bragg's law

$$d = \frac{2\lambda}{\sin\theta_B}, \tag{1}$$

where λ is the wavelength of the radiation, and the Bragg angle, θ_B, is the angle of incidence required for a peak in the reflected intensity.

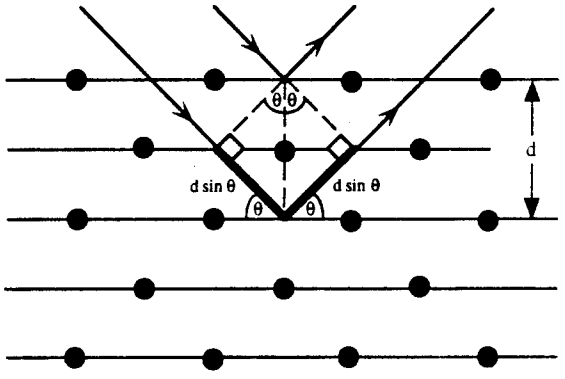


Fig. 5. The measurement of Si strain by x-ray diffraction. Waves reflected from different planes of atoms interfere constructively when the difference in their path lengths, $2d \sin\theta$, equals an integral number of wavelengths.

The strain of the Si lattice in the direction perpendicular to the surface was calculated from

$$\epsilon = \frac{\overline{d} - d_0}{d_0}, \tag{2}$$

where $d_0 = 0.543072$ nm[24] represents the unstrained Si lattice constant, and $\overline{d}$ represents the average of the strained lattice constants determined from measurements with the two wavelengths. Finally the stress induced at the Si surface within the interfacial plane was related to the strain by[25]

$$\sigma = \frac{E}{1-\nu}\epsilon, \tag{3}$$

where, for this problem, Young's modulus, E, is defined as the ratio of uniaxial tension to strain in an arbitrary direction $\hat{x}$ within the (100) Si plane, and Poisson's ratio, ν, is defined as the ratio of compression in the [100] direction to extension in the direction $\hat{x}$ when stressed under tension in the direction $\hat{x}$. Although the individual elastic constants associated with {100} Si planes vary with direction, the quantity $\frac{E}{1-\nu} = 1.805 \times 10^{11}$ Pa[26] is invariant with direction.

The major sources of error in the x-ray diffraction measurements are misalignment of the mounted samples with the x-ray source and the estimation of the peak positions in the measured diffraction patterns. The position of each of the k_{α_1} and k_{α_2} peaks was determined by fitting a Lorentzian distribution to the discrete measurement points. Before beginning the experiment, it was determined from repetitive measurements on a test sample that the combined measurement errors resulted in a standard deviation of approximately 0.6 arcsec in the measurement of a given Bragg angle, where an error of 1 arcsec in the Bragg angle corresponds to an error of approximately 1.3×10^6 Pa in stress.

Because the resolution in a single stress measurement was comparable in magnitude to the small stresses inherent in the samples, a statistical approach based on large numbers of measurements was taken. Four replicates per sample were included in the analysis, where each replicate was measured for stress a minimum of eight times per data point. The measurement results were used to compute 80% confidence intervals for stress based on the t-distribution and the standard deviations in the results[27]. Between successive measurements, each sample was removed from the diffractometer and remounted. No references internal to the samples were used for alignment. For each data point taken, a separate set of at least 16 diffraction measurements was made on a sample from an unirradiated bare Si wafer, where, like the test specimens, the sample was remounted between successive measurements. The mean Bragg angle computed from the bare Si measurements was used as a reference against which to calibrate the measurement results of the test sample replicates.

The measurement results are summarized in Fig. 6, where stress at the Si surface is plotted prior to irradiation and following each radiation or anneal step. The error bars represent the 80% confidence limits described above. A negative stress value indicates a tensile stress, while a positive stress value indicates a compressive stress. When the Si is in compression, the Si lattice is expanded in the direction normal to the Si-SiO_2 interface. Conversely, the Si lattice is contracted normal to the interface when the Si is in tension. The initial stress measured in the unmetallized samples is comparable in orientation and magnitude to stresses measured in other Si samples with deposited oxides[28]. The difference in the initial stresses for the metallized and unmetallized samples results from thermal contraction of the Al layer following the PMA[29]. The results indicate that each radiation and anneal cycle helps relieve compressive stress existing at the Si surface. The change in stress due to radiation is smaller in magnitude than the stress induced by the metallization. Relaxation of the stress is more pronounced for the samples receiving the larger total dose. The small increase in stress following the anneal steps in the unmetallized samples is likely due to a larger thermal expansion coefficient for the deposited oxide as compared with that of Si[28].

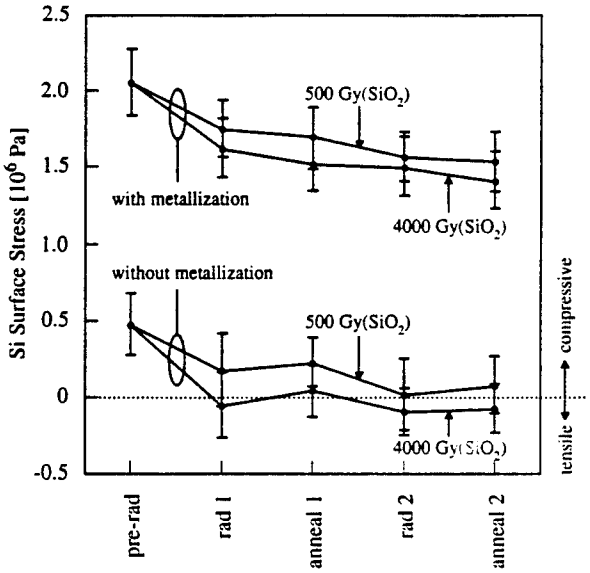


Fig. 6. Effect of radiation and anneal cycles on Si surface stress in the monitor wafer. Relaxation of compressive stress is smaller than the stress induced by the metallization.

D. Correlation of BJT Radiation Hardness and Si-SiO_2 Interfacial Stress

In Fig. 7, radiation-induced excess base current in the npn BJTs is correlated with Si surface stress in the monitor wafer. The abscissas for Si surface stress are taken from Fig. 6, whereas the ordinates for normalized excess base current come from Fig. 4. Each ordered pair maps BJT radiation-induced excess base current in a given radiation and anneal cycle to Si surface stress in the metallized portion of the monitor wafer at the start of the cycle. Excess base currents for BJTs with both emitter geome-

tries are included and correspond to total doses of 500 and 4,000 Gy(SiO_2) per cycle to match the total doses delivered to the monitor wafer samples. Progression of the measurement results through three cycles of radiation and anneal is from right to left along any one of the curves in the figure. Correlation of the results is such that, as Si surface stress in the monitor wafer is made less compressive by repeated cycles of radiation and anneal, radiation-induced excess base current in the BJTs increases regardless of emitter geometry. Because of the likeness of the monitor wafer to the region above the extrinsic base in the BJTs, the relationship suggests that the radiation hardness of the BJTs degrades with decreasing compressive stress along the surface of the extrinsic base. This inference is supported by conclusions from studies of MOS-Cs asserting that the radiation hardness of Si-SiO_2 interfaces degrades with decreasing compressive (increasing tensile) stress at the Si surface[1-4] and implies that radiation-induced changes in stress are influential in effecting the observed changes in BJT radiation hardness due to repeated cycles of radiation and anneal.

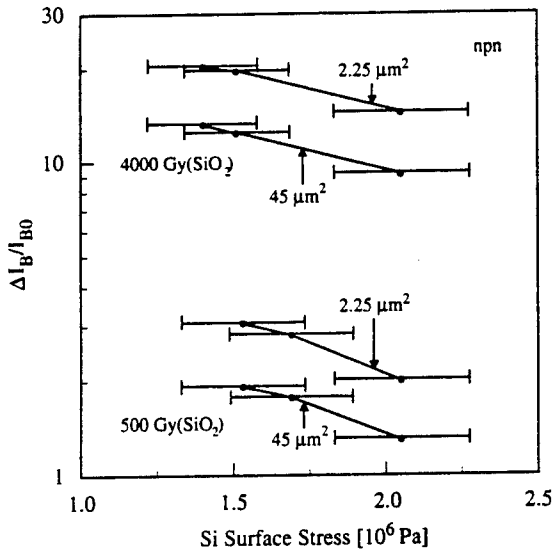


Fig. 7. Correlation of radiation-induced excess base current in the npn BJTs and Si surface stress in the monitor wafer. The trend suggests that the radiation hardness of the BJTs degrades with decreasing compressive stress in the base. The excess base currents were measured at V_{BE} = 0.6 V.

E. Effect of Total Dose on Si-SiO_2 Interfacial Stress

An additional pair of monitor wafer samples with and without metallization were investigated for the effect of total dose on Si surface stress using the statistical approach described in the previous experiment. Pre-radiation values of stress in the samples were measured 100 hr following the PMA. The samples were irradiated without bias by a ^{60}Co γ-source at a dose rate of 200 Gy(SiO_2) hr^{-1}. A total dose of 25 kGy(SiO_2) was delivered to the samples, during which time the irradiation was interrupted periodically for additional stress measurements.

The measurement results are shown in Fig. 8, where the error bars represent the 80% confidence limits for stress. The initial stresses reflect the effects of processing mentioned earlier. Compressive stress existing at the Si surface prior to irradiation is decreased by the ionizing radiation in each of the metallized and unmetallized samples. The amounts of stress reduction in the two samples are similar. The changes in stress are comparable in magnitude to those resulting from the repeated cycles of radiation and anneal described previously, indicating that stress relaxation in these samples is associated largely with irradiation and not with annealing. The relaxation of stress appears to persist for approximately 10 kGy(SiO_2), although the resolution of such small changes in stress is inhibited by the precision of the stress measurements. The change in Si surface stress due to radiation clearly is smaller than the stress induced by the metallization. Although radiation exposure modifies stresses in these samples, the results demonstrate that radiation-induced stresses in Si-SiO_2 structures can be dominated by processing effects.

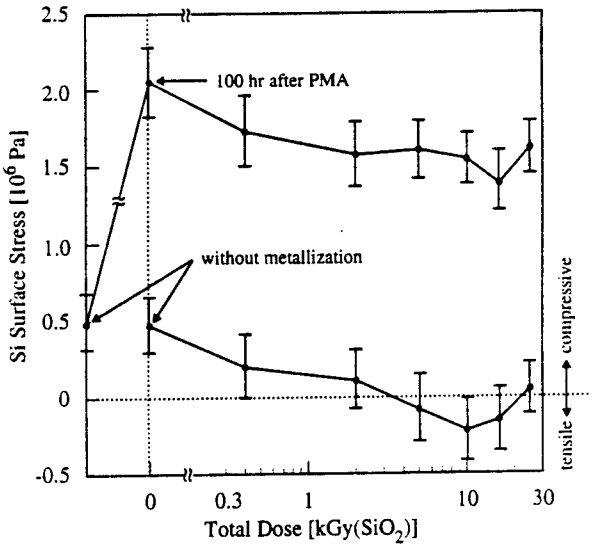


Fig. 8. Effect of total dose on Si surface stress in the monitor wafer. Relaxation of compressive stress is smaller than the stress induced by the metallization.

III. DISCUSSION

It is likely that a change in oxide density contributed to the radiation-induced stress changes observed in the monitor wafer. Thermally grown SiO_2 films on Si have been reported both to expand[30,31] and to shrink[32,33] in volume upon irradiation with energetic ions and electrons. Bulk vitreous silica, which is very similar in structure to oxides deposited by chemical vapor deposition (CVD) techniques[34], also can sustain varied changes in volume due to radiation. Increases in density due to neutron radia-

tion[35] and to various forms of ionizing radiation[36] have been reported, while vitreous silica compacted by external pressure has been shown to decrease in density following exposure to x-rays and fuel elements of a nuclear reactor[37,38].

The current understanding of radiation-induced density changes in SiO_2 is that such changes are dictated by the structural order of the particular silica form and by the material's initial density. Specifically, there exists some equilibrium density, such that dense films of high purity will incur a decrease in density due to radiation, while more porous films will undergo a density increase. Since a decrease in SiO_2 density would be accompanied by a decrease in compressive stress (increase in tensile stress) in any underlying Si, the measurement results for stress in the monitor wafer are consistent with the notion that radiation exposure reduced the wafer's oxide density. Such consideration, however, is complicated by the fact that two oxide layers are present. In this regard, it is interesting to note that the processing of the monitor wafer included an 800 °C anneal in an ambient of N_2 and O_2 for oxide densification.

The correlation of radiation sensitivity in the BJTs and mechanical stress in the monitor wafer is consistent with at least two well-known models for stress-related radiation effects in Si-SiO_2 structures. The Si surface stress model is one such example based on the probability of bond reformation[2-4]. It is maintained that the rupture of strained Si-SiO_2 interfacial bonds by radiation is accompanied by a relaxation of the ionized atoms to new positions of equilibrium[39]. The model asserts that, since a tensile stress corresponds to a stretching of the lattice, adjacent Si surface atoms under tension will tend to move farther apart upon ionization, thereby reducing the probability of bond reformation. The probability of bond reformation associated with radiation damage, therefore, is thought to grow less favorable with increasing tensile (decreasing compressive) stress at the Si surface. Reformation of fewer interfacial bonds, in turn, results in greater interface trap densities.

An alternative interpretation of the noted correlation can be made with an extension of the oxide bond strain gradient model[40]. Strained bonds are known to exist on the insulator side of the Si-SiO_2 interface owing to the lattice mismatch of the dissimilar materials[6]. It is thought that a gradient in the oxide bond strain directed toward the Si can elicit the propagation of certain radiation-induced oxide defects to the Si-SiO_2 interface, where they can readily create interface traps[7]. The density of interface traps induced by the defects is believed to depend on the magnitude of the bond strain gradient, such that a larger gradient results in the formation of more interface traps.

Due to the combined effects of a large thermal expansion coefficient[28] and an increase in density, the deposited oxide layer in the monitor wafer would be expected to compress the underlying thermal oxide and Si following the previously mentioned high-temperature densification anneal. As described earlier, the subsequent metallization and PMA of the wafer induce an even larger compressive stress in the Si. In accord with arguments made elsewhere[40], the combined compressive effects of the deposited oxide and Al layers reduce the bond strain gradient in the thermal oxide near the Si-SiO_2 interface. Any subsequent decrease in compressive (increase in tensile) stress at the Si surface due to, for example, a radiation-induced decrease in oxide density, would be accompanied by a relaxation of the oxide bond strain gradient to a larger value and, therefore, a greater propensity for interface trap formation.

In an npn BJT, the radiation-induced excess base current that flows at the surface of the base can be expressed as[41]

$$\Delta I_B \propto N_T \left[L_{R_p} + K_1 \exp\left(\frac{N_{ox}^2}{K_2}\right)\right], \qquad (4)$$

where N_T and N_{ox}, respectively, represent the densities of G-R centers and oxide charge above the extrinsic base, L_{R_p} refers to the location of the peak in surface recombination velocity, and K_1 and K_2 are constants unrelated to radiation. Since the G-R centers represented by N_T are, in fact, interface traps close enough in energy to midgap to facilitate surface recombination, an increase in radiation-induced interface trap densities generally leads to greater excess base current through an increase in N_T. Although the dependence on N_{ox} differs, a similar relationship between excess base current and N_T exists for vertical pnp BJTs[42].

Because of the considerable evidence relating hydrogen to the formation of radiation-induced interface traps[43,44], the role of hydrogen must also be considered in trying to account for the change in BJT radiation sensitivity due to repeated cycles of irradiation and anneal. According to the hydrogen model[45,46], H^+ ions liberated by radiation-induced holes in the oxide bulk can create Si-SiO_2 interface traps in the form of dangling Si bonds by reacting with Si-H trap precursors and substrate electrons near the interface. Assuming that the hydrogen model is applicable, the current gains measured in the BJTs imply that repeated cycles of radiation exposure and anneal lead to either an increase in the amount of hydrogen at or near the Si-SiO_2 interface in the screen oxide or an improvement in the efficiency with which hydrogen generates the interface traps. At present, there is insufficient evidence to speculate further.

IV. SUMMARY

Complementary single-crystalline emitter BJTs of two emitter geometries were investigated for radiation-induced current gain degradation while undergoing repeated cycles of ionizing radiation exposure and high-temperature anneal. Current gain degradation was found to grow progressively worse with an increasing number of cycles regardless of emitter polarity or geometry. The change in device radiation sensitivity was largest following the first radiation

and anneal cycle and diminished with subsequent cycles. The degradation in BJT radiation hardness sharply contrasts with the dramatic improvements in radiation hardness reported by others for MIS devices that received similar radiation and anneal treatments. It is concluded that the treatment of single-crystalline emitter BJTs with multiple cycles of radiation exposure and anneal does not make a promising technique for improving device tolerance to ionizing radiation.

In conjunction with the current gain measurements, samples from a monitor wafer processed to resemble the screen oxide region in the npn BJTs were characterized for mechanical stress while undergoing cycles of irradiation and anneal similar to those received by the BJTs. The oxide on the monitor wafer consisted of a 640 nm layer deposited on top of a 45 nm thermal layer. Values for Si stress in the Si-SiO_2 interfacial plane were obtained from the spacing of Si atomic planes by x-ray diffraction. The results indicate that compressive stress existing in the Si prior to irradiation is relieved somewhat by the repeated cycles of radiation exposure and anneal. A separate measurement of Si surface stress as a function of total dose absorbed by the samples revealed a comparable relaxation of stress, indicating that stress relaxation in the samples is elicited largely by irradiation and not by annealing. The change in stress due to radiation exposure was smaller than the stress induced by the emitter contact metallization.

Correlation of radiation sensitivity in the BJTs and mechanical stress in the monitor wafer is consistent with previously reported conclusions from studies of MOS-Cs that Si-SiO_2 interfaces are increasingly more susceptible to radiation damage with decreasing compressive (increasing tensile) stress in the Si. This result suggests that mechanical stress may play an important role in determining the radiation hardness of BJTs and that the observed changes in device radiation sensitivity following repeated cycles of radiation exposure and anneal may be explained, at least in part, by radiation-induced changes in mechanical stress.

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V.Q. Physically Based Comparison of Hot-Carrier-Induced and Ionizing-Radiation-Induced Degradation in BJTs

Physically Based Comparison of Hot-Carrier-Induced and Ionizing-Radiation-Induced Degradation in BJT's

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Abstract—**A physically based comparison between hot-carrier and ionizing radiation stress in BJT's is presented. Although both types of stress lead to qualitatively similar changes in the current gain of the device, the physical mechanisms responsible for the degradation are quite different. In the case of hot-carrier stress the damage is localized near the emitter-base junction, which causes the excess base current to have an ideality factor of two. For ionizing radiation stress, the damage occurs along all oxide-silicon interfaces, which causes the excess base current to have an ideality factor between one and two for low total doses of ionizing radiation, but an ideality factor of two for large total doses. The different physical mechanisms that apply for each type of stress imply that improvement in resistance to one type of stress does not necessarily imply improvement in resistance to the other type of stress. Based on the physical model, implications for correlating and comparing hot-carrier-induced and ionizing-radiation-induced damage are discussed.**

I. Introduction

THE current gain I_C/I_B of bipolar transistors is degraded when the oxide over the emitter-base junction is damaged. This can occur when the emitter-base junction is reverse-biased [1], as it is in normal BiCMOS circuit operation [2], or when the device is exposed to ionizing radiation [3]–[6]. Both hot-carrier damage and ionizing radiation typically lead to excess base current in the device ΔI_B, and no change in the collector current. The effects on device performance are qualitatively similar for both types of stress [6], [7].

For hot-carrier stress, many authors have assumed that ΔI_B is caused primarily by interface states created in the oxide over the emitter-base junction during the stress [7]–[11]. The effects of trapped charge created during the hot-carrier stress have received less attention, as the presence of the trapped charge near the emitter–base junction is difficult to detect from the current-voltage characteristics of the device [6].

Ionizing radiation occurs naturally in space and during electron-beam lithography [12]. For ionizing radiation stress, it has been shown that ΔI_B is caused by an interactive combination of interface states and trapped positive oxide charge [5], [6]. It has been shown that trapped positive charge far from the junction can substantially influence the excess base current by increasing the surface potential in the intrinsic base [5], [6]. The presence of the oxide charge is easily detected from a plot of excess base current versus base-emitter voltage [5].

Ionizing radiation has been used to mimic hot-carrier stress by selectively degrading individual transistors in an ECL circuit [7]. This approach has obvious advantages for studying circuit-level performance and degradation issues. It would also be useful if hot-carrier stress data could be used to predict ionizing radiation response, as radiation testing is generally more costly than hot-carrier sressing. The two types of stress can be correlated to one another for a specific set of test conditions [7]. The generality of the correlation is uncertain, however, as no physical basis exists for the comparison of hot carrier-induced and ionizing-radiation-induced degradation in bipolar transistors.

This work presents a physically based model for excess base current in BJT's that is applicable to both hot carrier-damage and ionizing radiation-induced damage. The general expression for excess base current is verified experimentally and with S-PISCES 2B [13] simulations. The salient features of both ionizing-radiation-induced and hot-carrier-induced degradation are explained in terms of the general model. The analysis indicates that improvements in resistance to one type of sress do not necessarily imply an improvement in resistance to the other type of stress. These results demonstrate that care must be taken when using the results of one type of stress to predict or mimic the results of the other type of stress.

II. Device and Experimental Details

The devices studied in this work are n-p-n polysilicon emitter bipolar transistors fabricated in a BiCMOS process closely related to that described in [14]. A representative cross-section of the devices is shown in Fig. 1. Relevant structural

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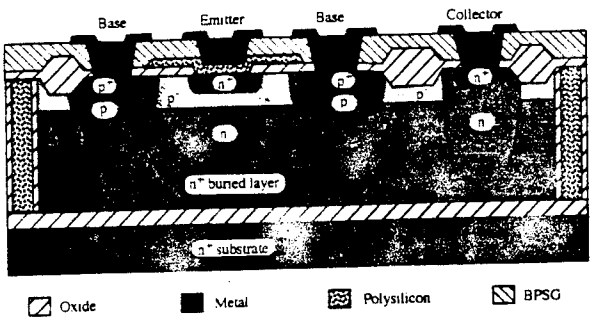
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ig. 1. Representative cross-section of the devices studied in this work.

TABLE I
RELEVANT DEVICE PARAMETERS

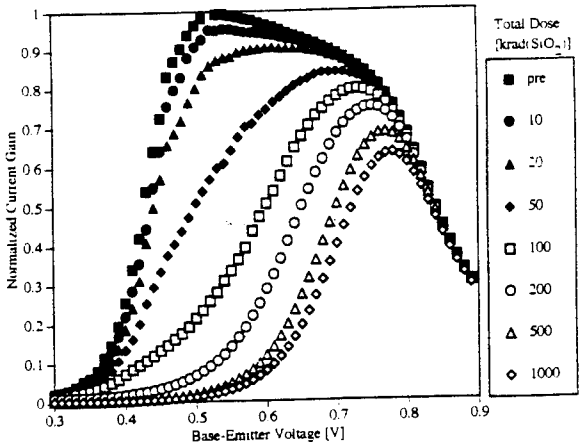
Parameter	Symbol	Value
Int. Base Surf. Doping	N_s	7.8×10^{17} cm^{-3}
Int. Base Length	L_{IB}	1 μm
Oxide Thickness	t_{ox}	550 Å
Emitter Size	$L_{E1} \times L_{E2}$	3 x 3 μm
Nominal Current Gain	N/A	200

and experimental information is summarized in Table I. For the irradiation study, the devices were irradiated with 10 keV x-rays at a dose rate of 1.7 krad(SiO_2)/s up to a total dose of 1 Mrad(SiO_2). All pins were grounded during irradiation. For the hot electron stress, a constant reverse current of 2 μA was applied through the emitter-base junction with the collector open for a total of 2.048 seconds. This stress current places the emitter-base junction well into avalanche breakdown. A Hewlett-Packard 4145B Semi-Conductor Parameter Analyzer was used for device characterization.

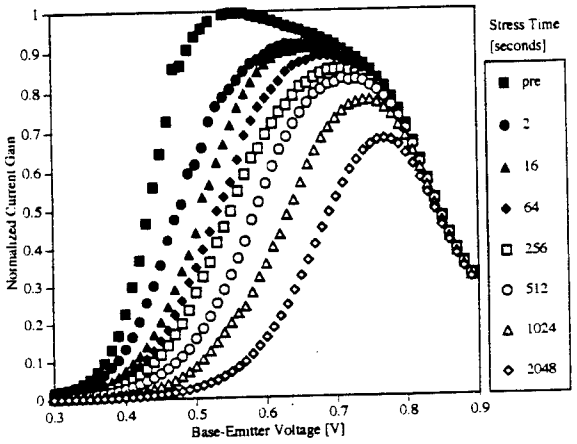
III. EXPERIMENTAL RESULTS

The normalized common-emitter current gain I_C/I_B, is plotted versus base-emitter voltage V_{BE}, in Fig. 2 for increasing values of each type of stress. Fig. 2(a) shows the normalized current gain for increasing values of total ionizing dose, while Fig. 2(b) shows the normalized current gain for increasing values of hot-carrier stress time. The current gain degrades substantially for both types of stress, and the degradation is most severe at lower values of V_{BE}. Note that the current gain degradation tends to saturate for large values of total ionizing dose, but shows no tendency to saturate for the stress times shown here. The trend, however, is qualitatively similar for both types of stress.

The collector current remains approximately constant throughout both radiation and hot electron stressing. The current gain degrades because the base current increases. The base current is written as $I_B = I_{B,\text{pre}} + \Delta I_B$, where the excess base current ΔI_B, is a recombination current in the emitter-base depletion region.



(a)



(b)

Fig. 2. (a) Normalized current gain versus base-emitter voltage for increasing levels of total ionizing dose. (b). Normalized current gain versus base-emitter voltage for increasing levels of hot-carrier stress time.

Recombination current in p-n junctions varies as $\Delta I_B = \Delta I_{Bo} \exp[\beta V/n]$ where n, the ideality factor, depends upon oxide charge and forward voltage. It will be shown in the next section that the relative contribution of the oxide charge far from the emitter-base junction is what determines the ideality factor in the diode equation. In [5] it is shown that the value of oxide charge can be determined by plotting the excess base current versus base emitter voltage, as in Fig. 3. Three transition voltages, V_{tr}, are also identified. The transition voltages mark the transition between predominantly surface and predominantly subsurface recombination. These transition voltages are readily related to net positive oxide charge, N_{ox}, by the simple relationship [5]

$$N_{ox} = \sqrt{\frac{2\epsilon_{Si} N_s}{q}\left(\frac{1}{\beta}\ln\left(\frac{N_s}{n_i}\right) - \frac{V_{tr}}{2}\right)} \qquad (1)$$

where n_i is the intrinsic carrier concentration, $\beta = q/kT$ is the inverse thermal voltage, N_s is the surface concentration in the intrinsic base, ϵ_{Si} is the permittivity of silicon, and q is the magnitude of the electronic charge. In general, N_{ox} includes the contributions of both oxide-trapped charge, N_{ot},

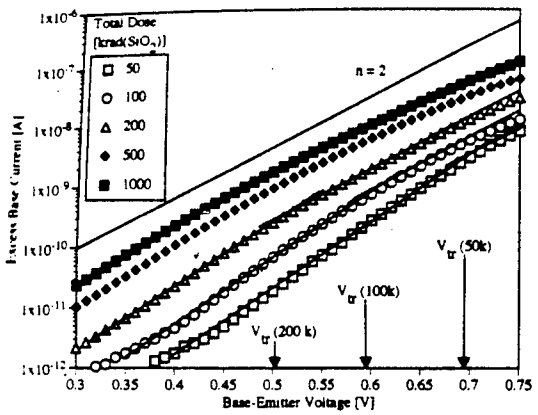


Fig. 3. Excess base current versus base-emitter voltage for various levels of total ionizing dose.

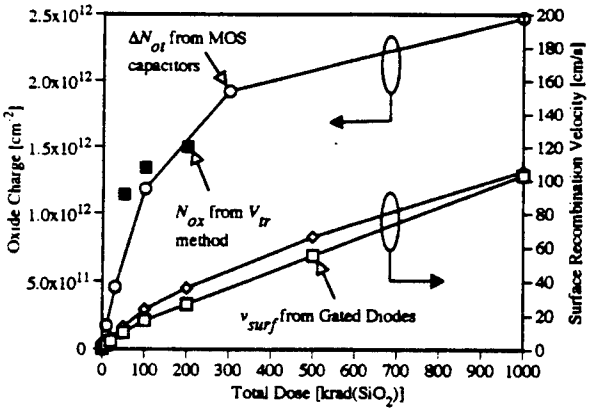


Fig. 4. Oxide charge and surface recombination velocity from two gated diodes versus total dose.

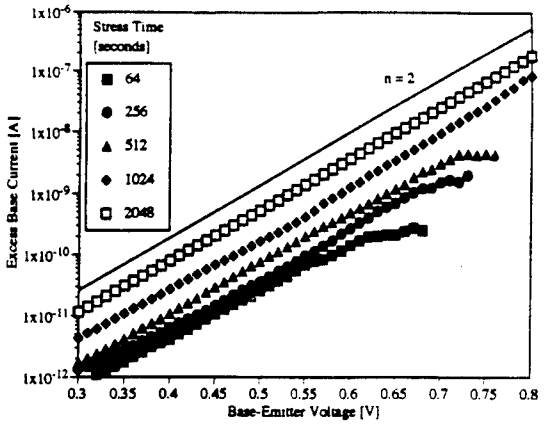


Fig. 5. Excess base current versus base-emitter voltage for increasing levels of hot-carrier stress time.

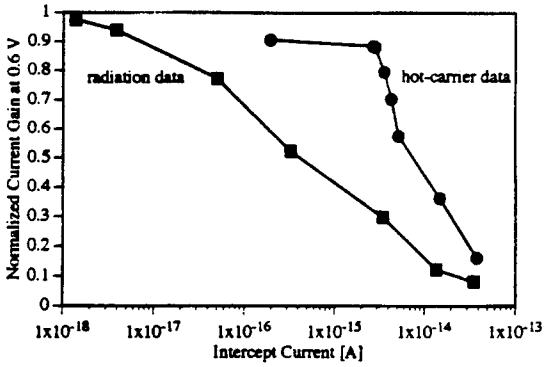


Fig. 6. Normalized current gain at 0.6 V versus intercept current.

and charged interface traps, as discussed in [5]. In Fig. 4, N_{ox} calculated from the transition voltages is plotted versus total ionizing dose. Oxide-trapped charge, N_{ot}, measured from MOS capacitors and surface recombination velocity v_{surf}, measured from gated diodes from the same process, is also plotted for comparison. It is seen from Fig. 4 that N_{ox} is similar to N_{ot} for these devices, and that both v_{surf} and N_{ox} increase with increasing total ionizing dose. The degradation due to ionizing radiation is caused by increases in both positive oxide charge and surface recombination velocity [5], [6], but is primarily due to increases in oxide charge [15].

Note also from Fig. 3 that, for large values of total ionizing dose, the ideality factor is approximately two for the entire range of V_{BE}. Further increases in total ionizing dose do not cause the excess base current to increase substantially once $n = 2$ for all V_{BE}. This saturation behavior and corresponding ideality factor for ionizing radiation is explained the next section.

In Fig. 5, ΔI_B is plotted versus V_{BE} for several values of increasing hot-carrier stress time. The ideality factor is roughly two for all stress times, and no transition voltage can be determined for any stress level. This is because the recombination current is localized near the emitter-base junction for all values of V_{BE}. Thus, even if trapped charge is present near the emitter-base junction, it cannot be detected from this plot. In other studies, it has been reported that $n > 2$ for hot-carrier stress, which is attributed to trap-assisted tunneling [16]. Evidently, this does not occur for these devices, indicating that the excess base current is entirely recombination current near the emitter-base junction.

In Fig. 6, normalized current gain at V_{BE} =0.6 V is plotted versus intercept current ΔI_{Bo} for each type of stress. Since $n < 2$ for the radiation sress data at lower total doses, the intercept current for a given current gain degradation is much less than for hot-carrier stress. The curves approach one another for large intercept currents because for radiation stress, $n \rightarrow 2$ for large values of N_{ox}.

A simple model for the observed trends in the excess base current for both hot-carrier and ionizing radiation stress is presented and verified in the next section. The model provides insight into the similarities and differences between the types of damage caused by each type of stress. It also serves as a basis for comparing the two types of stress.

IV. Model

The recombination current in the emitter-base space charge region can be obtained analytically from Shockley-Read-Hall (SRH) recombination theory [17], [18]. The electron concentration at the surface can be written as

$$n_s = n_i \exp\left[\beta(\psi_s - \varphi_{nf})\right] \tag{2}$$

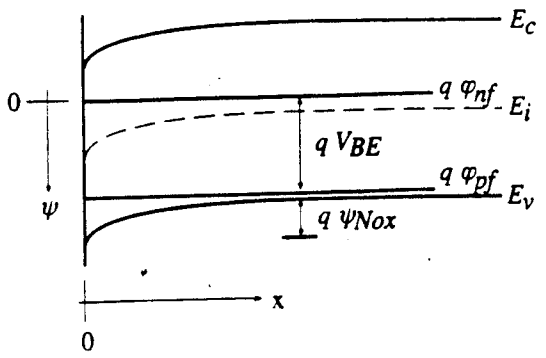


Fig. 7. Energy band diagram perpendicular to the oxide-silicon interface.

and the hole concentration at the surface is written as

$$p_s = n_i \exp\left[\beta(\varphi_{pf} - \psi_s)\right]. \tag{3}$$

In these equations φ_{nf} is the quasi-Fermi level for electrons, and φ_{pf} is the quasi-Fermi level for holes. The potential ψ is always the intrinsic potential ψ_i. The reference for potential is φ_{nf}, which we define to be zero. The applied voltage appears as a splitting of the quasi-Fermi levels; $V_{BE} = \varphi_{pf} - \varphi_{nf}$. These conventions are illustrated in Fig. 7.

Assuming equal electron and hole capture cross sections, a single trap level at midgap in equilibrium with the bulk semiconductor and moderate forward bias, the recombination rate at the surface can be written as a function of lateral position as [5]

$$R_s(y) = \frac{n_i v_{surf} \exp\left(\frac{\beta V_{BE}}{2}\right)}{2\cosh\left[\beta\left(\psi_s(y) - \frac{V_{BE}}{2}\right)\right]}. \tag{4}$$

The surface recombination velocity is given by $v_{surf} = \sigma v_{th} N_T$, where σ is the capture cross section, v_{th} is the thermal carrier velocity, and N_T is the trap density.

The peak recombination rate, $R_{s,pk}$, occurs when $\psi_s = V_{BE}/2$ and is given by

$$R_{s,pk} = \frac{1}{2} n_i v_{surf} \exp\left(\frac{\beta V_{BE}}{2}\right). \tag{5}$$

The recombination rate versus lateral position curve is a peaked function. The peak occurs near the emitter-base metallurgical junction, with a plateau region over the intrinsic base. This trend is illustrated in Fig. 8(a) and 8(b), where PISCES-simulated surface potential and surface recombination rate are plotted versus lateral position for a fixed forward voltage of $V_{BE} = 0.5$ V and varying amounts of positive oxide charge. For large amounts of oxide charge, the surface recombination rate decreases in the intrinsic base. In this case, the recombination peak has moved below the oxide/silicon interface. When this happens, the excess base current saturates, as discussed later.

When the surface recombination rate has a peak near the emitter-base junction, the surface potential in the intrinsic base is less than half the applied voltage, $\psi_s < V_{BE}/2$, allowing

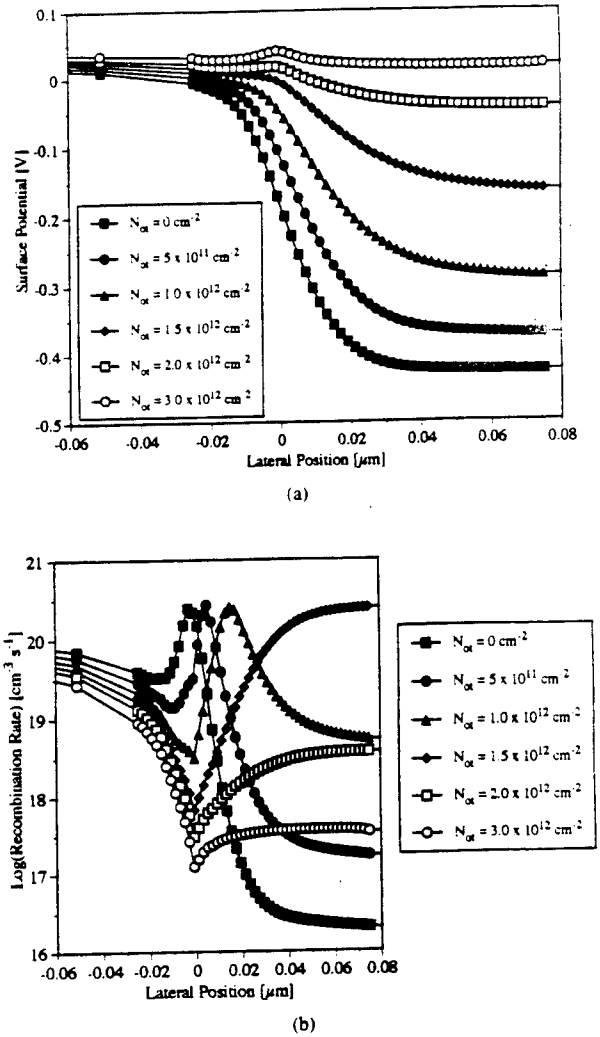


Fig. 8. PISCES-simulated (a) surface potential, and (b) surface recombination rate versus lateral position near the emitter-base junction. The metallurgical junction is at the origin, and the base-emitter voltage is 0.5 V with varying amounts of oxide charge.

the cosh term to be approximated by neglecting one of the exponentials. This approximation allows the recombination rate in the intrinsic base to be written as

$$R_{s,IB} = n_i v_{surf} \exp\left(\beta \psi_{s,IB}\right) \tag{6}$$

where $\psi_{s,IB}$ is the surface potential in the intrinsic base and is given by

$$\psi_{s,IB} = -\frac{1}{\beta} \ln\left(\frac{N_s}{n_i}\right) + \psi_{N_{ox}} + V_{BE}. \tag{7}$$

$\psi_{N_{ox}}$ is the band-bending due to the oxide charge which may be written in the depletion approximation as

$$\psi_{N_{ox}} = \frac{q N_{ox}^2}{2\epsilon_{Si} N_s}. \tag{8}$$

A qualitative sketch of the recombination rate and corresponding surface potential showing important definitions is shown in Fig. 9.

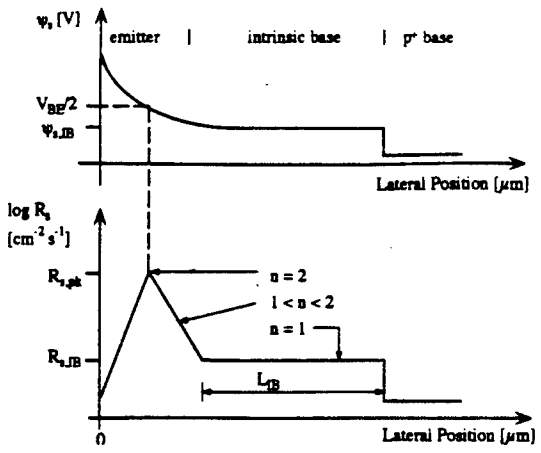


Fig. 9. Schematic representation of the surface potential and surface recombination rate versus lateral position.

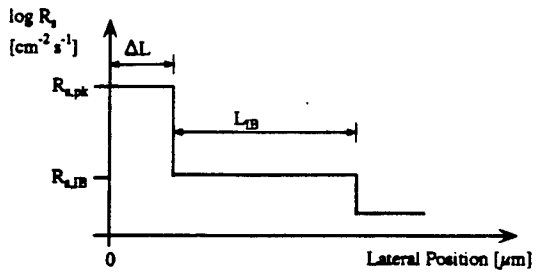


Fig. 10. Idealized recombination rate versus lateral position.

Combining (6)–(8) and using the definition of the extrinsic Debye length, L_D

$$L_D^2 = \frac{kT\epsilon_{Si}}{q^2 N_s} \tag{9}$$

allows $R_{s,IB}$ to be written as

$$R_{s,IB} = \frac{n_i^2}{N_s} v_{surf} \exp(\beta V_{BE}) \exp\left[\frac{N_{ox}}{\sqrt{2}L_D N_s}\right]^2. \tag{10}$$

Now, consider the approximation to the $R_s(y)$ profile shown in Fig. 10. This approximation removes the dependence of the recombination rate on the details of the surface potential near the junction. Instead, a new parameter ΔL has been introduced. The physical interpretation of ΔL is the effective width over which recombination proceeds with an ideality factor of 2. Mathematically, $R_s(y)$ is approximated by the double-step function

$$R_s(y) = \begin{cases} 0, & y < 0 \\ R_{s,pk}, & 0 \le y \le \Delta L \\ R_{s,IB}, & \Delta L \le y \le \Delta L + L_{IB} \end{cases} \tag{11}$$

where the origin is on the emitter side of the emitter-base junction at a point where $R_s \ll R_{s,pk}$.

In general, the excess base current that flows at the surface of the intrinsic base $\Delta I_B(surface)$, is given by

$$\Delta I_B(surface) = q \int_{intrinsic\ base} R_s(y, z)\, dydz. \tag{12}$$

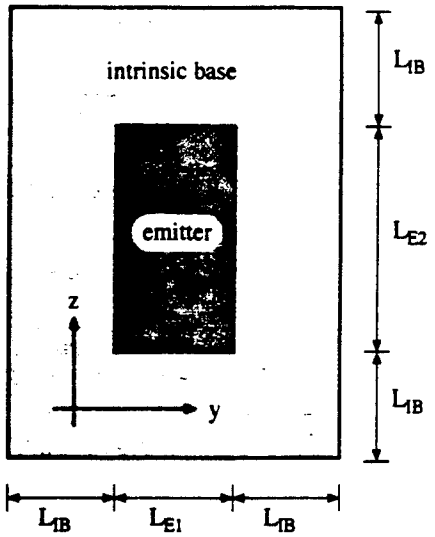


Fig. 11. Schematic top view of the BJT.

A top view of the BJT showing the emitter-base region is shown in Fig. 11. A rectangular emitter is considered for generality.

A rigorous solution of (12) would require that R_s be inserted into (12), and the integral performed numerically. The integral must be performed over the entire area of the intrinsic base. If, however, the approximate $R_s(y)$ profile as given by (11) is used, a particularly transparent and simple form for $\Delta I_B(surface)$ results:

$$\Delta I_B(surface) = qn_i v_{surf}(L_{E1} + L_{E2}) \exp\left[\frac{\beta V_{BE}}{2}\right] \cdot \left\{\Delta L + \frac{2n_i L_{IB}}{N_s}\left(1 + \frac{2L_{IB}}{L_{E1} + L_{E2}}\right) \cdot \exp\left[\frac{N_{ox}}{\sqrt{2}L_D N_s}\right]^2 \exp\left[\frac{\beta V_{BE}}{2}\right]\right\}. \tag{13}$$

This form for $\Delta I_B(surface)$ elucidates many of the features of stress-induced damage in BJT's. It expresses the excess base current due to surface recombination as the sum of a term proportional to the perimeter of the emitter and a term proportional to the area of the intrinsic base. These two terms have different voltage dependencies; the perimeter term has an ideality factor of 2, and the area term has an ideality factor of 1. When both terms contribute, the ideality factor is between 1 and 2. This is the situation that exists for irradiated BJT's when $V_{BE} < V_{tr}$, as illustrated in Fig. 3. For hot-carrier stress, primarily the first term contributes to the excess base current. The hot-carrier stress may increase v_{surf} or ΔL or both, but the ideality factor of the excess base current is always 2 as illustrated in Fig. 5.

When the recombination peak moves below the surface of the intrinsic base, the recombination current becomes relatively insensitive to increases in surface damage [5], [19]. This is because the point of maximum recombination now lies below the surface, as seen in Fig. 12. Here, PISCES-simulated

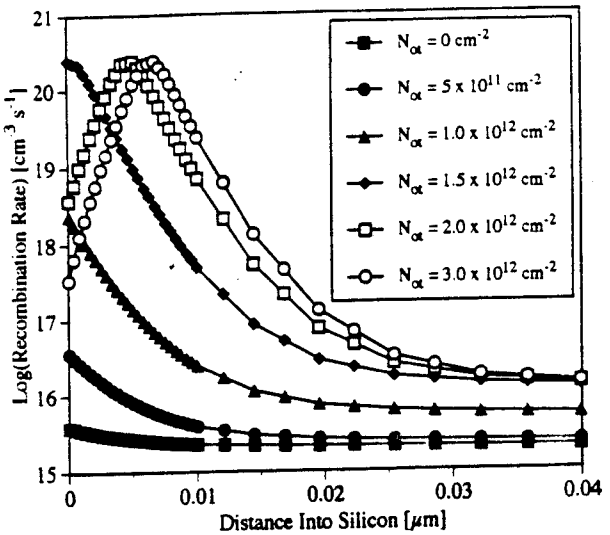


Fig. 12. PISCES-simulated recombination rate versus distance into the silicon in the intrinsic base. The base-emitter voltage is 0.5 V with varying amounts of oxide charge.

recombination rates normal to the oxide-silicon interface are plotted for a fixed forward voltage of 0.5 V and varying amounts of oxide charge. The transition between surface and subsurface recombination occurs at the transition charge as given by (1) using $V_{tr} = 0.5$ V, which gives a transition charge of 1.5×10^{12} cm^{-2}. This prediction is confirmed in Fig. 12. The excess base current that flows when the peak lies below the surface depends on the bulk recombination lifetime according to

$$\Delta I_B(subsurface) = \frac{qn_i}{2\tau}\Delta x 4L_{IB}^2\left(1+\frac{L_{E1}+L_{E2}}{2L_{IB}}\right)\exp\left[\frac{\beta V_{BE}}{2}\right] \quad (14)$$

where Δx is the effective recombination width and τ is the bulk recombination lifetime. An estimate for Δx is the depletion-layer width induced by the positive oxide charge in the depletion approximation, $\Delta x < N_{ox}/N_s$. Note that the ideality factor n for $\Delta I_B(surface)$ is 2 because the recombination rate below the surface is dominated by the recombination peak, in contrast to $\Delta I_B(surface)$, as can be readily verified by comparing Figs. 8(b) and (12).

The validity of the piecewise-continuous model for ΔI_B, derived above, is confirmed by the PISCES simulation results in Fig. 13. For convenience, in the PISCES simulations the recombination time constants at the surface were the same as those in the bulk. Doping profiles were taken from SUPREM simulations and verified with spreading-resistance and capacitance measurements. Note in particular from Fig. 13 that further increases in N_{ox} beyond $N_{ox}(transition)$ do not cause an increase in ΔI_B for the reasons cited above. This explains the experimentally observed result on many different device technologies that increases in base current due to ionizing radiation tends to saturate for large total doses [5], [6], [10], [19]. Also note from Fig. 12 that the excess base current increases exponentially for $N_{ox} < N_{ox}(transition)$, as predicted by (13).

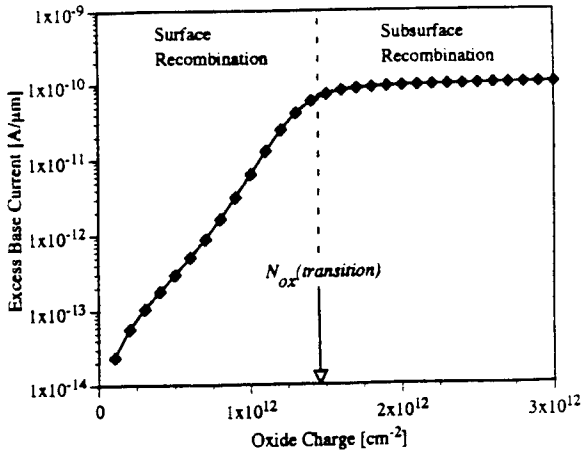


Fig. 13. Excess base current versus positive oxide charge.

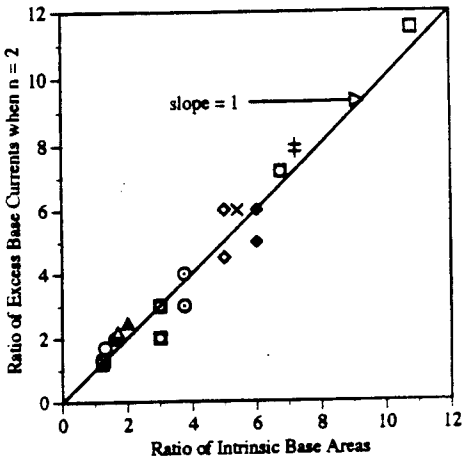


Fig. 14. Ratio of excess base currents for subsurface recombination versus ratio of intrinsic base areas for several device geometries.

Equation (14) is also verified in Fig. 14, where the ratio of excess base currents for large total doses is plotted versus the ratio of intrinsic base areas for several device geometries. The devices were fabricated on the same test chip as the devices in Table I. Emitter size and shape ranged from 1.5 × 1.5 to 14 × 14 μm^2, along with 2 × 50 and 2 × 15 μm^2 devices. The excess base currents clearly stand in the ratio of the intrinsic base areas, as predicted by (14).

V. Discussion

A mapping can be made between the hot-carrier stress data and the ionizing radiation stress data by equating the normalized current gains at a fixed base-emitter voltage. This map can be used as a guide for determining how much of each type of stress will cause a given amount of device degradation. This approach has been used to study circuit-level hot-carrier degradation issues by using a scanning electron microscope to selectively degrade individual transistors in the circuit [7].

The correlation between radiation-induced degradation and hot-carrier-induced degradation is extremely sensitive to the test conditions used. For example, ionizing-radiation-induced degradation is dose-rate dependent, with lower dose rates

causing more damage than higher dose rates [20]. For hot-carrier stress, the amount of degradation in a given device depends on the stress current or voltage used [9], and the ambient temperature [11], [21]. Changing any of these variables would require a new mapping between hot-carrier and radiation damage.

Correlating and interpreting results from devices with different geometries is conceptually understood in the context of (13) and (14). It is seen from (13) and (14) and Figs. 12 and 13 that the excess base current due to ionizing radiation is proportional to the area of the intrinsic base. The excess base current for hot-carrier stress, however, is proportional to the perimeter of the emitter. Finally, the effect the excess base current will have on the current gain of the device depends on the ratio of the emitter perimeter to the emitter area [7], [3].

Equation (14) shows that the amount of damage that can be done by radiation is limited, a result that has been observed experimentally [5], [10], [19]. Physically, the damage due to ionizing radiation is limited because for $N_{ox} > N_{ox}(transition)$, the recombination current flows primarily below the oxide-silicon interface, and is thus insensitive to further increases in surface damage [15], [19]. For constant-current hot-carrier stressing in the avalanche breakdown regime of the emitter-base junction, the amount of damage is proportional to the amount of charge passed through the junction [2], [9]. Thus, the amount of damage that can be done by hot-carrier stressing could easily be much larger than the amount of damage done by radiation, as has been observed experimentally [6].

Improvement in the radiation hardness of a BJT does not necessarily imply that the device will also be less susceptible to hot-carrier damage. Equation (13) shows that substantial improvement in the radiation hardness of BJT's for surface recombination can be expected by increasing the surface doping of the intrinsic base. Once sufficient charge has accumulated to force the recombination peak below the surface, however, (14) shows that increased doping will have an adverse affect on the radiation hardness of the device due to the inverse relationship between doping and lifetime.

For hot-carrier stress, the performance of the device depends on the details of the stress conditions [22]. Increasing the doping in the intrinsic base leads to larger surface electric fields for a given reverse-bias voltage, which leads to worse performance for constant-voltage stress and constant-current stress in the avalanche regime, but may not lead to worse performance under constant current stress at sub-avalanche currents [22]. The ambiguity arises because of the additional junction leakage components present in heavily doped junctions, such as band-to-band and trap-assisted tunneling [16].

Device geometry also affects the radiation hardness and hot-carrier performance differently. Reducing the area of the intrinsic base improves radiation hardness, as shown in Fig. 13. Changing the area of the intrinsic base, however, has no direct effect on the hot-carrier resistance of the device.

Finally, the goals of oxide engineering for hot-carrier resistance and radiation hardness in BJT's are not identical. From (13), it is seen that suppression of radiation-induced oxide charge in the oxide overlying the intrinsic base will lead to substantial improvement in the radiation hardness of the device. To improve the hot-carrier resistance of the device, (13) suggests that attention should be paid to suppressing interface state build up, as well as oxide charge build up.

VI. Conclusions

A physically-based model for radiation-induced and hot-carrier-induced degradation in BJT's has been presented. The origins of the excess base current for the two types of stress were found to be very different. Positive oxide charge was identified as the primary driving force behind ionizing-radiation-induced degradation, in constrast to the situation for hot-carrier stressing. The different dependencies on device geometry and doping of hot-carrier-induced and ionizing-radiation-induced degradation mean that improvement in resistance to one type of stress does not necessarily imply improvement in resistance to the other type of stress. Implications for correlating hot-carrier induced and ionizing–radiation induced degradation were discussed. The analysis provides insight into the issues that must be taken into account when comparing hot-carrier and radiation stress results, especially when one type of stress is used to mimic the other type of stress.

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VI. Summary

This report has covered work on modeling of single-event burnout of power MOSFETs, single-event gate rupture of power MOSFETs, total-dose effects on power MOSFETs, 1/f noise in power MOSFETs, total-dose gain degradation in bipolar junction transistors, and mechanical and hot-carrier-induced stress effects in bipolar junction transistors. Each technical section of this report is self-contained.

Each technical section describes work that has contributed to the technical base necessary to provide radiation-hardened power MOSFETs and bipolar junction transistors for DNA-supported systems. Much of the work has yielded design guidelines that can be used in the development of radiation-hardened electronics. This work has been widely disseminated through technical talks and technical papers, and through direct consultation with government laboratory personnel and personnel from the electronics industry.

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