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Monterey, California



THESIS

**VLSI IMPLEMENTATION OF A DIGITALLY
PROGRAMMABLE THREE STAGE GIC FILTER**

by

Steven L. Pettit

June 1995

Thesis Advisor:

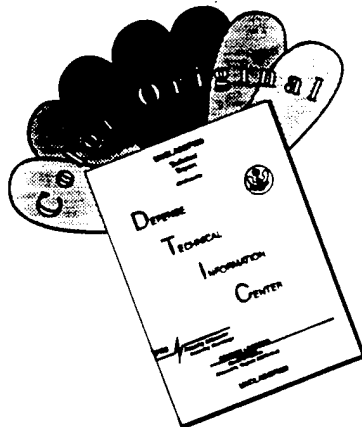
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In this research, a multiple stage analog active filter is analyzed and designed using periodic sampling techniques. A General Immitance Converter (GIC) is the basic building block used to realize VLSI implementation of a three stage, bi-quadratic, digitally programmable filter. The manufacture of this microchip is the initial step in development of a stray insensitive CMOS GIC filter. Switched capacitor networks are used to facilitate component layout accuracies, further reducing the filters sensitivity to component tolerances. Simulations of extracted CMOS filter circuits are compared to simulations using PSPICE models. The final goal of this thesis is a manufactured CMOS microchip suitable for further development and testing.

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THREE STAGE GIC FILTER**

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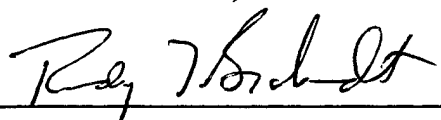
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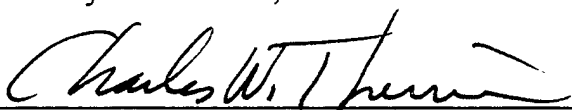
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ABSTRACT

In this research, a multiple stage analog active filter is analyzed and designed using periodic sampling techniques. A General Immitance Converter (GIC) is the basic building block used to realize VLSI implementation of a three stage, bi-quadratic, digitally programmable filter. The manufacture of this microchip is the initial step in development of a stray insensitive CMOS GIC filter. Switched capacitor networks are used to facilitate component layout accuracies, further reducing the filters sensitivity to component tolerances. Simulations of extracted CMOS filter circuits are compared to simulations using PSPICE models. The final goal of this thesis is a manufactured CMOS microchip suitable for further development and testing.

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I. INTRODUCTION

A. BACKGROUND

Integrated circuit technology has seen a great deal of change in the past 30 years. Most of the advances have been made with digital circuits, and it was neither practical nor desirable to integrate analog components. Digital circuitry of the 1990's is capable of performing very complex computational functions; but as good as the digital networks become, they must still interface with the analog world. This relationship is vital in A/D converters, robotics, communications equipment, spacecraft control, and remote sensing, just to name a few. The analog interface with digital systems is normally accomplished by separate components, necessitating large circuit boards and correspondingly large power supplies. By integrating the analog interface, circuit size and power consumption can be minimized. Modern Very Large Scale Integration (VLSI) techniques enable the combination of analog and digital circuits on a single microchip. In some cases, such as filtering, integrated analog circuits can accomplish functions much more economically than the digital counterpart. At a minimum, analog integrated circuits must be studied because the very problems that challenge the leading technological edge of the digital world are analog in nature.

This research focuses on the integration of a digitally programmable analog filter. Digitally programmable filters find many uses in the area of communications, speech processing, neural networks, control, etc. The programmable nature of the filter increases the versatility of the filter such that mass production becomes economical. The final product of these efforts will be four microchips manufactured through the MOSIS foundry using a two micron CMOS process. The funding for the chip manufacturing was provided by the National Science Foundation.

B. FILTERS

The purpose of a filter in an electrical sense is to modify the amplitude response of a signal such that selected frequencies are attenuated, while others pass through the filter unmodified or are amplified. Filters are generally grouped into categories based on the ranges of frequencies that are attenuated or passed. The common groups are highpass, lowpass, bandpass and notch or bandreject, and they generally represent the frequencies that will be passed by the filter. Figure 1.1 illustrates an example amplitude response for each class of filters. The design of a filter involves an attempt to achieve an ideal

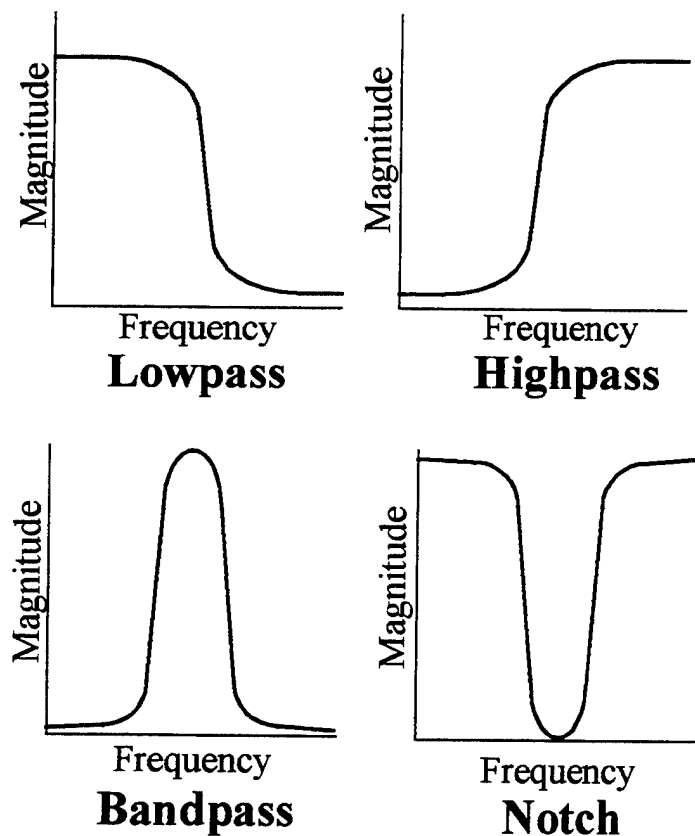


Figure 1.1: Amplitude Responses of Four Basic Filter Types

amplitude response. This goal is unattainable given the natural limits of circuit construction [Ref. 1]. The ideal filter's amplitude response would fully pass and fully attenuate only the exact frequencies desired. Figure 1.2 shows the amplitude response of an ideal

bandpass filter. The transfer function of an ideal filter would have an order of infinity. Actual filters approach the ideal case in one of three ways. Some filters will emphasize the flatness of the passband, while others concentrate on the steepness of the attenuation slope. Phase response, which is another non-ideal property of a filter, can be optimized at the expense of other characteristics. Generally, higher order filters will have steep attenuation slopes, and ripple in the passband. Higher order filters are also more expensive in terms of number of components and complexity. This research deals with second order filters, which have the general transfer function shown in Equation 1.1.

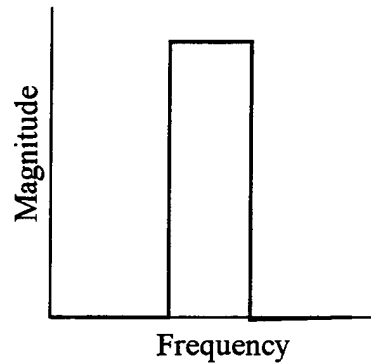


Figure 1.2: The Ideal Magnitude Response for a Bandpass Filter

$$H(s) = \frac{k \left[s^2 \pm \frac{\omega_n}{Q_z} s + \omega_n^2 \right]}{s^2 \pm \frac{\omega_0}{Q_p} s + \omega_0^2} \quad (\text{Eq 1.1})$$

In the equation above, the parameters ω_n , ω_0 , Q_z and Q_p are the null frequency, resonant frequency, zero quality factor and pole quality factor. The quality factors are a measure of the sharpness of the amplitude response curve at the respective frequencies. Q_z is nearly always infinity [Ref. 2]. A description of quality factor is illustrated in Figure 1.3 and its governing equation is Eq. 1.2.

$$Q = \frac{f_0}{f_1 - f_2} \quad (\text{Eq 1.2})$$

The transfer functions associated with each type of filter are listed in Table 1.1. These functions are called Bi-Quadratic functions and are typically referred to as biquads. All four biquad transfer functions are realized by the programmable filter developed in this research .

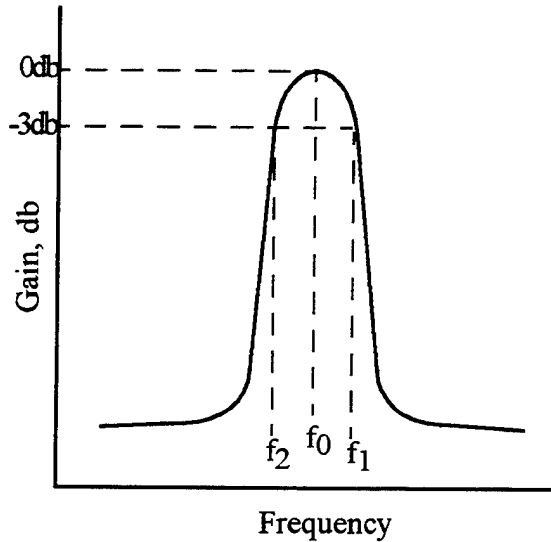


Figure 1.3: Quality Factor for a Bandpass Filter

C. THESIS ORGANIZATION

The goal of this thesis is the design and manufacture of a digitally programmable integrated active filter. Chapter II outlines the necessity of active filters and presents the selection of the General Immittance Converter filter for chip integration. The properties of the ideal General Immittance Converter filter are presented in detail. The advantageous use of switched capacitor networks to realize resistances on a microchip is explored in the third chapter. Chapter III also covers the theoretical basis for sampled data networks and the development of the bilinear switched capacitor resistor for use in the programmable filter. Chapter IV discusses, programmability of the General Immittance Converter filter. Logic is designed to enable selection of four topologies, eight center or corner frequencies and six

pole quality factors. Minimal layout area is considered as one of the primary design constraints. Chapter V introduces the physics of semiconductors and the theory of operation for basic integrated devices. The overall layout of the programmable filter chip is presented, along with detailed design considerations for component devices such as operational amplifiers and capacitors. The chapter finishes by comparing ideal filter simulations with simulations performed by extracting network data from the programmable GIC filter integrated circuit.

Filter Topology	Transfer Function
Lowpass	$H(s) = \frac{2\omega_p^2}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}$
Highpass	$H(s) = \frac{2s^2}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}$
Bandpass	$H(s) = \frac{\frac{2\omega_p}{Q_p}s}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}$
Notch	$H(s) = \frac{s^2 + \omega_n^2}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}$

Table 1.1. Transfer Functions for Four Topologies of the Bi-Quadratic Filter

II. INTRODUCTION TO THE GENERALIZED IMMITANCE CONVERTER FILTER

A. ACTIVE VERSUS PASSIVE FILTERS

Passive filters use networks of inductors and capacitors to realize some form of wave shaping and do not require external power sources to operate. These components are effective for constructing simple lowpass, highpass, bandpass, notch and allpass filters, but the use of an inductor can cause sometimes insurmountable problems in system design. Aside from having poor performance in low frequency applications, inductors are rather large and electrically lossy devices. In addition, desirable integration of inductors on a silicon microchip is nearly impossible when the physics of the problem are presented. The inductor dilemma motivates the realization of inductorless filter circuits.

Active elements such as operational amplifiers, are defined by their power source requirement and can be used to construct inductorless filter circuits. The basic premise of this concept is to realize inductive impedance properties without using an inductor. Several inductor simulation networks that use the operational amplifier as a building block have been proposed in Schaumann [Ref. 3].

B. INDUCTOR SYNTHESIS WITH ACTIVE DEVICES

Many networks designed to synthesize inductance have been proposed and studied. Simulation circuits include the Negative Impedance Converter (NIC), the Gyrator and the Generalized Impedance Converter (GIC).

The Generalized Impedance Converter (GIC) is depicted in Figure 2.1. This simulation circuit is considered to be the most tolerant to the non-ideal operational amplifier qualities of finite gain and bandwidth [Ref. 4].

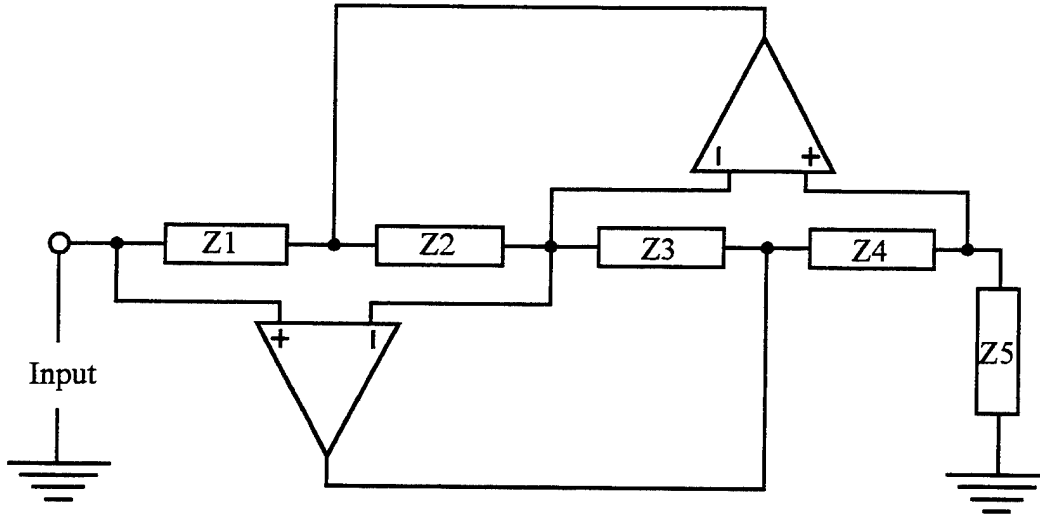


Figure 2.1: Antoniou's Generalized Impedance Converter

The impedance at the input of the GIC depicted in Figure 1 is given by

$$Z_{in} = \frac{Z_1 Z_3 Z_5}{Z_4 Z_2} \quad (\text{Eq 2.1})$$

If a capacitance is substituted for Z_4 or Z_2 and resistances are substituted for the remaining impedances, the input impedance Z_{in} is characterized by

$$Z_{in} = sCk \quad (\text{Eq 2.2})$$

where Ck is equivalent to an inductance L . Other impedance conversions can be shown, but the use of converting a capacitance to an inductance is probably the most useful for filter construction.

C. THE GIC FILTER

The Generalized Immittance Converter is a generic filter design based on the properties of Antoniou's Generalized Impedance Converter. This filter design was introduced by Bhattacharyya [Ref. 5] and was found to have very low sensitivities to both passive component tolerances and non-ideal operational amplifier properties. The GIC filter is depicted in Figure 2.2. By using admittance values listed in Table 2.1, the various

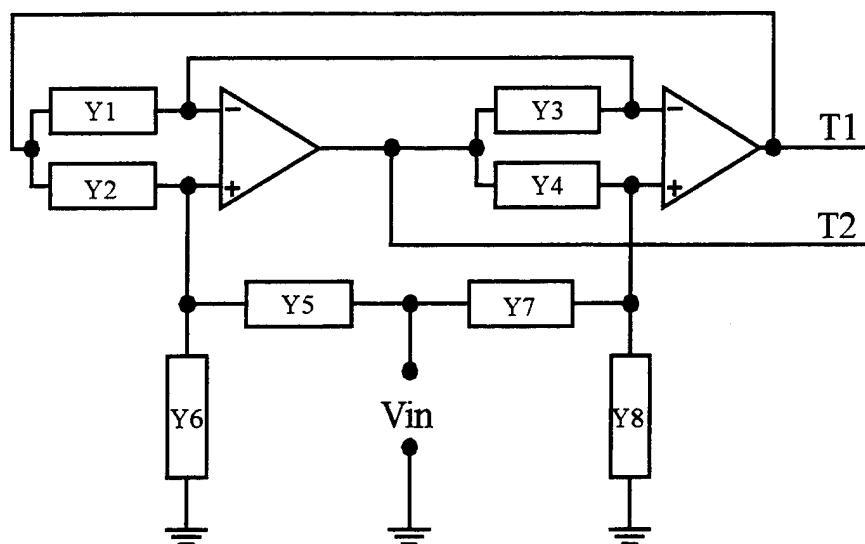


Figure 2.2: The General Immittance Converter Filter

Filter Topology	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8
Lowpass	G	C	$C + \frac{G}{Q_p}$	G	G	0	0	G
Highpass	G	G	C	G	0	G	C	$\frac{G}{Q_p}$
Bandpass	G	G	C	G	0	G	$\frac{G}{Q_p}$	C
Notch	G	G	C	G	G	0	C	$\frac{G}{Q_p}$

Table 2.1. Admittance Values for Realizing Four Topologies of the GIC Filter

filter topologies depicted in Figure 1.3 are realized. The output for the lowpass and notch topologies are taken from terminal one, while the remaining topologies use terminal two as an output. The transfer functions, when outputs are taken at nodes one and two, can be calculated by nodal analysis. If the operational amplifiers are considered to be ideal and the output is taken at node one, the transfer function in terms of the admittances is described as Eq. 1.3. Equation 1.4 describes the transfer function if the output is taken from node two. An admittance analysis rather than an impedance analysis is used for the GIC filter because it greatly simplifies the mathematics. The transfer functions associated with the different topologies are listed in Table 2.2. Note that the denominators of the transfer functions in Eq. 2.3 and 2.4 are equal. Substituting the impedance values listed in Table 2.1 into the appropriate transfer function T_1 or T_2 results in the discrete value transfer functions listed in Table 2.2.

$$T_1 = \frac{v_1}{v_i} = \frac{Y_1 Y_4 Y_5 + Y_3 Y_7 (Y_2 + Y_6) - Y_3 Y_5 Y_8}{Y_1 Y_4 (Y_5 + Y_6) + Y_2 Y_3 (Y_7 + Y_8)} \quad (\text{Eq 2.3})$$

$$T_2 = \frac{v_2}{v_i} = \frac{Y_1 Y_4 Y_5 + Y_1 Y_5 Y_8 + Y_2 Y_3 Y_7 - Y_1 Y_6 Y_7}{Y_1 Y_4 (Y_5 + Y_6) + Y_2 Y_3 (Y_7 + Y_8)} \quad (\text{Eq 2.4})$$

By correlating the discrete values with the generic biquadratic transfer functions listed in Table 2.2, relations for the following two filter characteristics can be made.

- Center or Corner Frequency (depending on the filter topology)
- Pole Quality Factor

By setting the last term in each denominator equal,

$$\omega_p^2 = \frac{G^2}{C^2} \rightarrow \omega_p = \frac{G}{C} \quad (\text{Eq 2.5})$$

The center or corner frequency is only dependant on the ratio of the admittances of the resistors and the admittances of the capacitors.

Filter Topology	Transfer Function (with discrete values)	Transfer Function
Lowpass	$T_2 = \frac{2\frac{G^2}{C^2}}{s^2 + \frac{Gs}{CQ_p} + \frac{G^2}{C^2}}$	$T_2 = \frac{2\omega_p^2}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}$
Highpass	$T_2 = \frac{2s^2}{s^2 + \frac{Gs}{CQ_p} + \frac{G^2}{C^2}}$	$T_1 = \frac{2s^2}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}$
Bandpass	$T_2 = \frac{\frac{sG^2}{CQ_p}}{s^2 + \frac{Gs}{CQ_p} + \frac{G^2}{C^2}}$	$T_1 = \frac{\frac{2\omega_p s}{Q_p}}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}$
Notch	$T_2 = \frac{s^2 + \left(\frac{G^2}{C^2} + \frac{G^2}{C^2 Q_p}\right)}{s^2 + \frac{Gs}{CQ_p} + \frac{G^2}{C^2}}$	$T_2 = \frac{s^2 + \omega_n^2}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}$

Table 2.2. Transfer Functions Realized by GIC Filter

The pole quality factor can be analyzed by correlating the second denominator terms of the generic and discrete valued transfer functions, the following relation is written

$$\frac{G}{CQ_p} = \frac{\omega_p}{Q_p} \quad (\text{Eq 2.6})$$

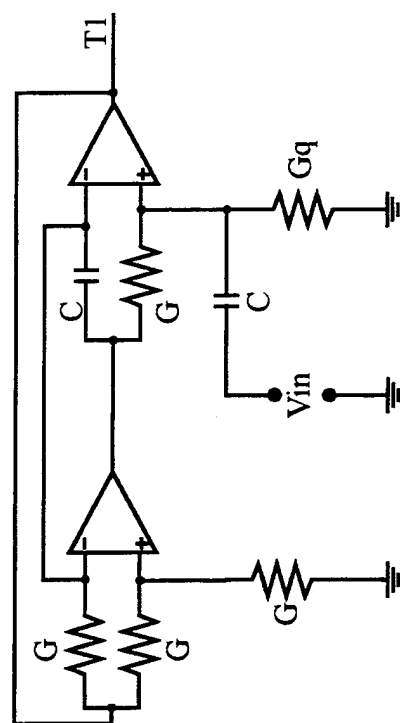
If the admittance value of the resistor represented in the second term of the transfer function denominator is scaled by Q_p such that

$$G_q = \frac{G}{Q_p} \quad (\text{Eq 2.7})$$

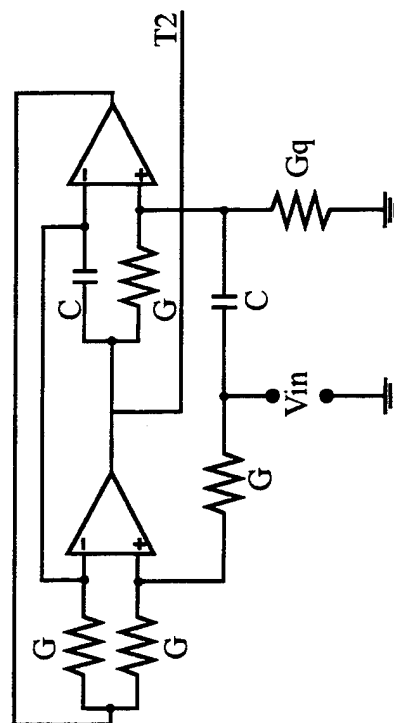
The ratio of the resistive component admittance G_q to the common resistor admittance G is solely responsible for determining the quality factor of the filter. This relationship shown in Eq. 2.8 is merely a rearrangement of Eq. 2.7

$$Q_p = \frac{G}{G_q} \quad (\text{Eq 2.8})$$

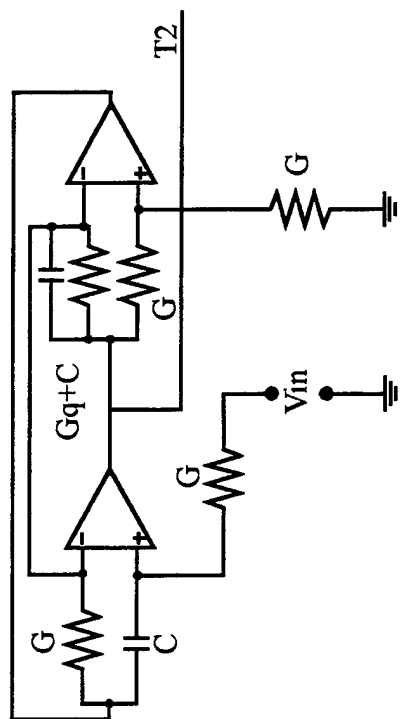
The relationships described in equations 2.5 and 2.8 can be used to adjust the principle operating parameters of any configuration of a GIC filter. If the admittance G is assigned a constant value, then the center or corner frequency and the pole quality factor of the filter can be adjusted independently by changing C and G_q respectively. This independent adjustment scheme allows the GIC to be inherently programmable.



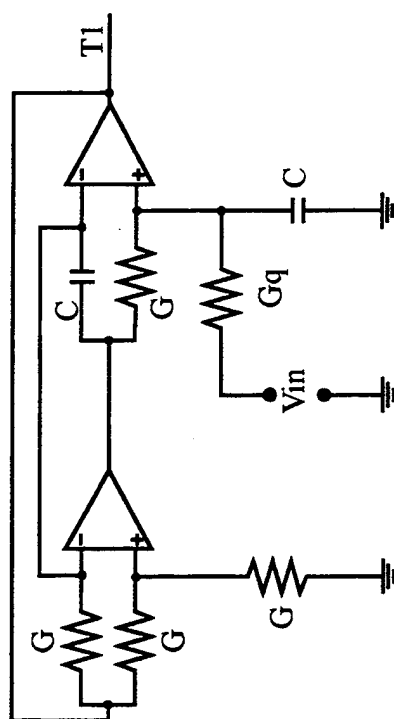
Highpass



Notch



Lowpass



Bandpass

Figure 2.3: The Four Topologies of the GIC Filter

III. SWITCHED CAPACITOR NETWORKS

A. THE NEED FOR SWITCHED CAPACITOR NETWORKS

The problems associated with the integrated circuit (IC) implementation of an inductor have been addressed, but there is yet another stumbling block to the IC development of analog circuits. Resistances can be made to exacting tolerances as discrete non-integrated components, but the VLSI design of a resistor is "sloppy" and component tolerances can be as high as 50 percent. Resistors can be constructed on an integrated circuit by snaking narrow channels of highly doped diffusion, polysilicon or metal until the proper length over width ratios corresponding to the equivalent resistance is met. Resistor tolerances can be improved by laser trimming the edges of the resistive polysilicon and metal materials, but this process is very costly. Integrated circuit resistors require a relatively large layout area, and if multiple resistors are to be implemented, the amount of area required can be prohibitive. An additional problem with integrated circuit resistors is their poor linearity and low tolerance to the large temperature deviations that occur in integrated circuits. To fully appreciate the value of implementing resistances by using switched capacitor networks, the analog use of resistances must be studied.

Analog systems use a combination of resistors, capacitors and active devices to construct circuits that implement specific functions. The performance of these circuits is directly dependent on the accuracies of the resistors and capacitors. Filters are specifically dependent on the time constant or resistor-capacitor product. The time constant (τ) of the filter is assumed as follows:

$$\tau = R_1 \cdot C_2 \quad (\text{Eq 3.1})$$

The dependency of τ on R_1 and C_2 is illustrated by the following expression:

$$\frac{d\tau}{\tau} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} \quad (\text{Eq 3.2})$$

In Eq. 3.2, dX/X is interpreted as the accuracy of X . Given a CMOS process in which

large deviations in absolute values for R_1 and C_2 are standard, large inaccuracies in τ can be expected.

The representation of a switched capacitor network implemented as a resistor will be developed at a later point in this chapter, but to help illustrate the benefits of switched capacitor, the resistive value of a series or parallel switched capacitor network is correctly assumed as

$$R = \frac{T_c}{2C_r} \quad (\text{Eq 3.3})$$

where T_c is clock period and C_r is the capacitive value in the switched capacitor network. The combination of Eq. 3.1 and Eq. 3.3 yields

$$\tau = \frac{T_c}{2C_r} \cdot C_2 = \frac{T_c C_2}{2C_r} \quad (\text{Eq 3.4})$$

The accuracy of τ is then stated as

$$\frac{d\tau}{\tau} = \frac{dT_c}{T_c} + \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \quad (\text{Eq 3.5})$$

If the clock is assumed to be very accurate, then the accuracy of τ is expressed as

$$\frac{d\tau}{\tau} = \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \quad (\text{Eq 3.6})$$

CMOS capacitors can be constructed such that their relative values are within 0.1% of each other. With this close tolerance, the time constant of Eq. 3.4 is much more accurate than that of Eq. 3.1. Since the resistive characteristics of a switched capacitor network are realized with a ratio of capacitors, and the capacitors undergo identical manufacturing processes, as well as identical operational temperature deviations, the sensitivity of the resultant device to these deviations can be shown to be very small. Another advantage of switched capacitor networks is in the practical realization of large time constants without the need for physically large components. Equation 3.4 shows that the relative size of capacitor values determines the time constant for a given clock frequency. If the capacitor

used in the switched capacitor resistive network is small relative to the value of C_2 and the frequency of the clock is low, the time constant will be large.

B. SWITCHED CAPACITOR OPERATION

Switched capacitor networks generally consist of capacitors connected with switches which are driven by a clock. Figure 3.1 is an example of a switched capacitor network. The switches depicted in the circuits throughout this thesis are always shown in the open position. The phase of the clock signal driving the switch is indicated by ϕ_n , where n

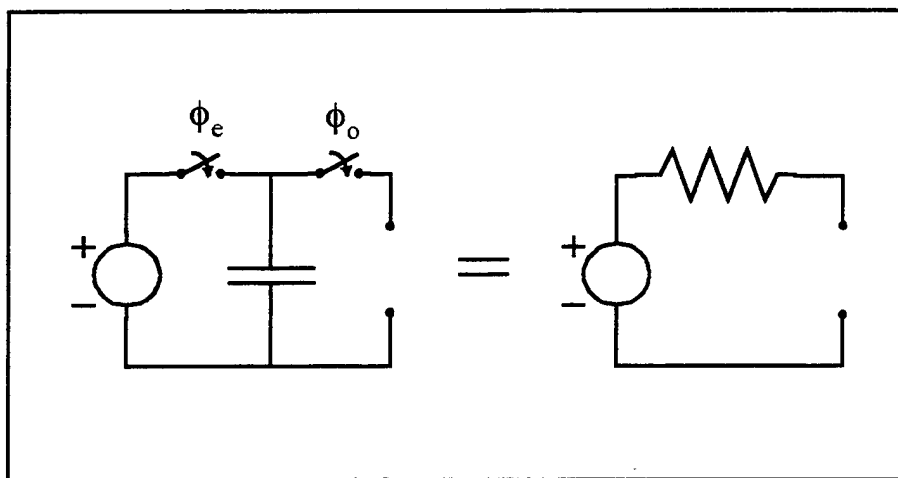


Figure 3.1: Basic Switched Capacitor Network

indicates the specific phase of the signal driving the switch. All switch signals are driven by one clock. The output of a two phase non-overlapping clock is shown in Figure 3.2. The two phases are labeled even and odd to distinguish the master clock phase in which the driven switch is closed. Note that the phases are delayed such that only one phase is “on” at any instance. This non-overlapping characteristic is required to prevent a virtual short circuit which would occur if the two switches in Figure 3.1 were closed simultaneously. A side effect of the non-overlapping characteristic is a duty cycle of less than 50 percent. A clock with more than two phases can be used for more complex circuits, but throughout this report, the phases will be limited to two. Another assumption made for the

scope of this report is that each switch is closed only once during a clock period and that the switches are closed when the clock equals 5 volts and open when the clock signal level equals -5 volts. A switched capacitor network that uses a two phase clock is called a bi-phase network.

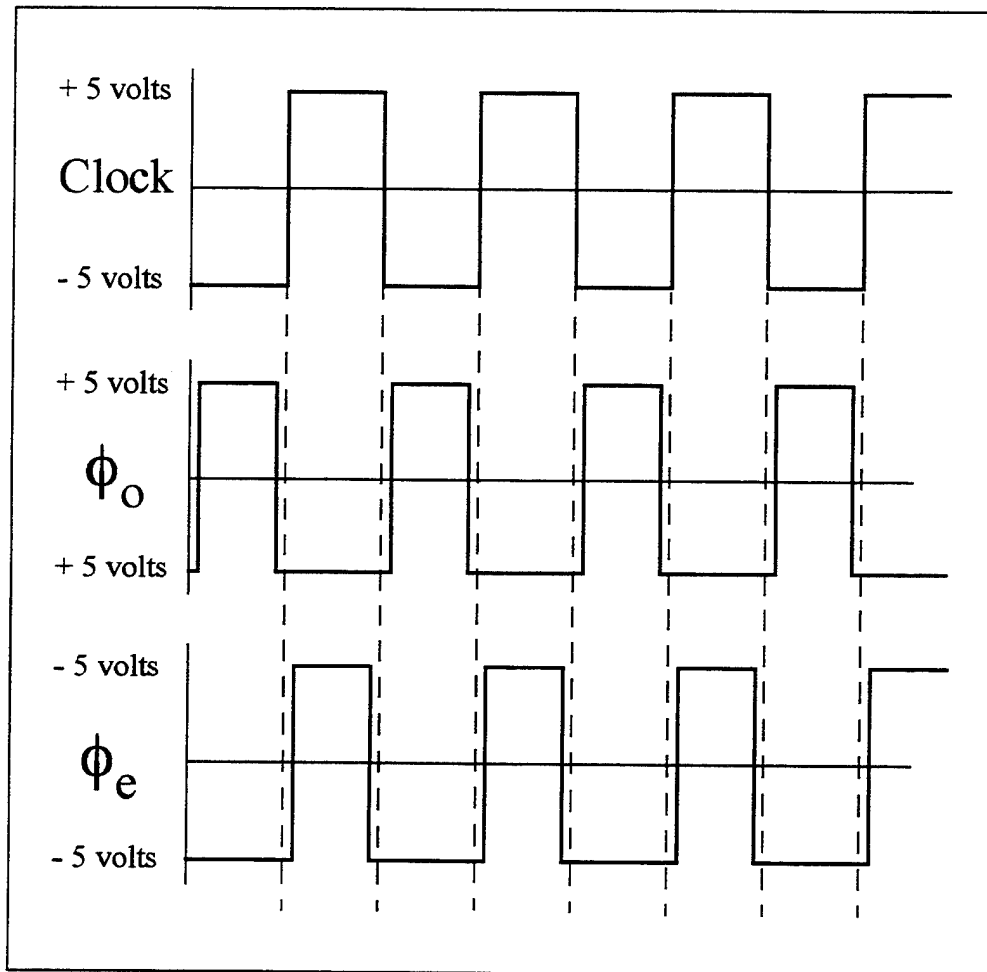


Figure 3.2: Two Phase Non-overlapping Clock

C. BI-PHASE SWITCHED CAPACITOR NETWORKS

A typical biphas switched capacitor network can be considered as two separate topologies. As the even phase is asserted, one topology is realized; when the odd phase is asserted, the other topology is realized. The output of the even topology after one cycle is used to determine the initial condition for the input of the odd topology, and the odd output

is used to initialize the next step of the even input. The combination of the sampled waveforms from the two topologies constitute the output of the total network. This iterative analysis is particularly useful with computer aided design tools. A second method of switched capacitor network analysis is to keep the even and odd topologies combined into a single z-domain equivalent circuit.

D. CONTINUOUS AND DISCRETE DOMAINS

It is convenient to design and discuss filter operations in the s-domain but since switched capacitor networks use sampled data techniques, similar to that of a digital filter, z-domain analysis must also be used. The z-domain analysis must not, however disregard the impedance and loading characteristics of the equivalent s-domain analog network.

The continuous time filter has a system response determined by the following system of first order differential equations.

$$\frac{dx_i(t)}{dt} = g_i(t), \quad i = 1, 2, \dots, N. \quad (\text{Eq 3.7})$$

Here, the x_i are the state variables of the filter and the variations of Eq 3.7 are the state equations. The $g_i(t)$ are linear functions of the state variables and the input signal. By using the Laplace transformation, Eq. 3.7 becomes

$$s_a X_i(s_a) = G_i(s_a), \quad i = 1, 2, \dots, N. \quad (\text{Eq 3.8})$$

where $x_i(t) = 0$ for $t \leq 0$ is assumed, and the subscript 'a' is used to indicate that the expression refers to an analog model. [Ref. 7]

The state equations of a sampled data system, which has approximately the same properties of a continuous time filter, are related by the first order difference equations extracted by integrating Eq. 3.8 between $(n-1)T$ and nT . The integration yields Eq. 3.9 which is then simplified in Eq. 3.10. As shown, the integration of the left hand side of Eq. 3.9 simplifies into the proper difference form. The integration of the right hand side of Eq. 3.10 requires the use of a numerical integrator. The four possible numerical integration techniques are the Euler forward integration, Euler backward integration, the bilinear or

trapezoidal integration and the midpoint integration. A graphical depiction of the four integration techniques is shown in Figure 3.3.

$$\int_{nT-T}^{nT} \frac{dx_i(t)}{dt} dt = \int_{nT-T}^{nT} g_i(t) dt, \quad i = 1, 2, \dots, N \quad (\text{Eq 3.9})$$

$$x_i(nT) - x_i(nT-T) = \int_{nT-T}^{nT} g_i(t) dt, \quad i = 1, 2, \dots, N \quad (\text{Eq 3.10})$$

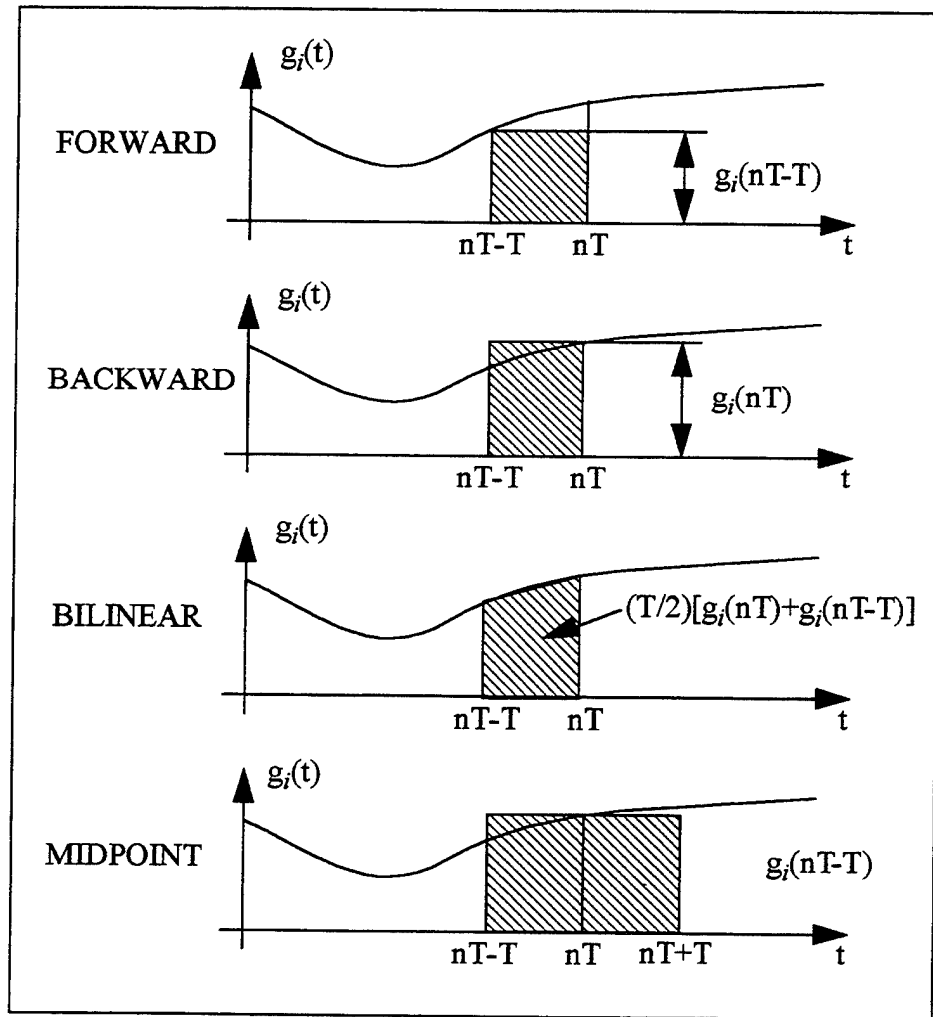


Figure 3.3: Numerical Integration Techniques after [Ref. 7]

A relationship between the variable s in the s -domain and the variable z in the z -domain can be developed by investigating the result of equation 3.10 using the four numerical integration techniques and relating these results to the corresponding s -domain functions. The results of the s to z relationship for each integration technique is presented below in Equations 3.11 through 3.14.

Forward difference:

$$z = 1 + Ts \quad (\text{Eq 3.11})$$

Backward difference:

$$z = \frac{1}{1 - Ts} \quad (\text{Eq 3.12})$$

Bilinear difference:

$$z = \frac{1 + \left(\frac{T}{2}\right)s}{1 - \left(\frac{T}{2}\right)s} \quad (\text{Eq 3.13})$$

Midpoint difference:

$$z = s_a T \pm \sqrt{(s_a T)^2 + 1} \quad (\text{Eq 3.14})$$

Two characteristics that are required of a transformation method are the ability to map stable s -domain functions into stable z -domain functions and the ability to map the $j\omega$ -axis in the s -plane to the unit circle in the z -domain. The former of these criteria ensures the networks stability, while the latter ensures the preservation of gain response. The ability of the four transformation techniques to meet these required characteristics can be tested by setting $s = -\sigma + j\omega$ and evaluating z for different stable values of s .

The backwards difference transformation maps stable s -poles into stable z -poles but does not map the $j\omega$ -axis to the unit circle of the z -plane. The forward difference transformation does not map stable s -poles to stable z -poles in the z -domain or map the $j\omega$ -axis onto the z -domain unit circle. The bilinear transformation does map stable s -plane

poles into stable z-plane poles, and it also maps the s-plane $j\omega$ -axis to the unit circle in the z-plane. The results of the forward difference transformation, the backward difference transformation and the bilinear transformation are shown in Figure 4.[Ref. 8]

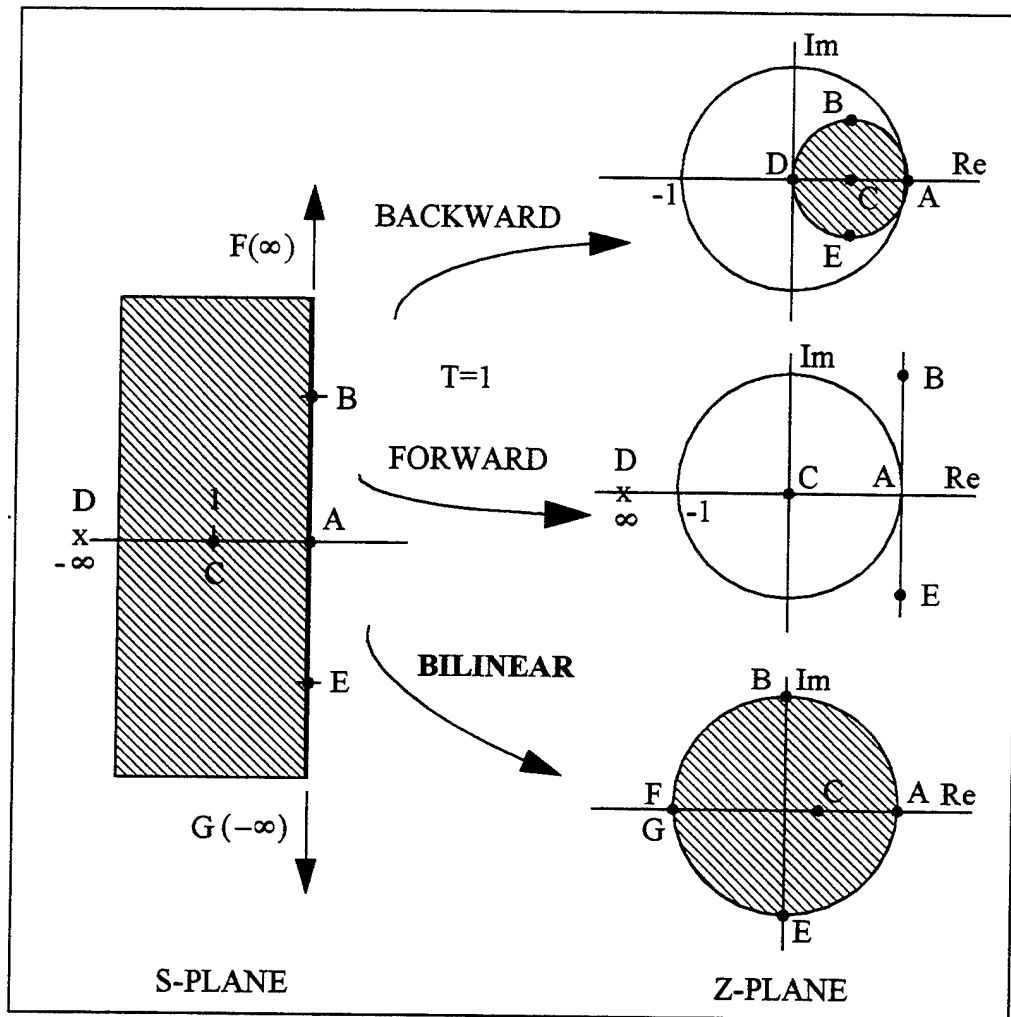


Figure 3.4: Backward and Forward transformations after [Ref. 8]

The midpoint transformation maps the $j\omega$ -axis to the unit circle in the z-plane, and the stable s-plane poles are mapped as stable z-plane poles but not in an algebraic one-to-one fashion. A stable s-plane pole maps as one stable and one unstable z-plane pole. This unwelcome destabilizing effect eliminates the midpoint transformation as an s to z mapping

technique. The obvious choice for performing this mapping function is the bilinear transformation.

E. FREQUENCY WARPING

The bilinear transformation meets all of the requirements specified to map s-plane poles to z-plane poles, but it does have some side effects that cannot be ignored. If Eq. 3.13 is solved for the variable s,

$$s_a = \frac{2}{T} \times \frac{z-1}{z+1} \quad (\text{Eq 3.15})$$

if $e^{j\omega T}$ is substituted for z and the numerator and denominator are divided by $2e^{j\omega T/2}$, then

$$\frac{\omega_a T}{2} = \tan \frac{\omega T}{2} \quad (\text{Eq 3.16})$$

Eq. 3.16 can be rearranged to produce

$$\omega = \frac{2}{T} \tan^{-1} \left[\frac{\omega_a T}{2} \right] \quad (\text{Eq 3.17})$$

Equation 3.17 describes the relation between a given frequency in an analog network and its corresponding frequency in a switched capacitor filter. This effect, known as warping, is the result of mapping a straight line $j\omega$ in the s-domain to a unit circle in the z-domain, and must be considered when designing a switched capacitor network.

As the clock frequency increases relative to the design frequency of the analog network, the effects of warping are minimized. For this analysis, the clock period T is defined as

$$T = \frac{2\pi}{X\omega_a} \quad (\text{Eq 3.18})$$

where X is defined as the relation

$$X = \frac{\omega_{\text{clock}}}{\omega_a} \quad (\text{Eq 3.19})$$

When Eq. 3.19 is substituted into Eq. 3.18 the result is

$$\omega = \frac{\omega_a X}{2\pi} \tan^{-1} \left[\frac{\omega_a 2\pi}{2X\omega_a} \right] \quad (\text{Eq 3.20})$$

Eq. 3.20 can be simplified and the result shown as Eq. 3.15 can be studied for varying values of X .

$$\omega = \frac{\omega_a X}{\pi} \tan^{-1} \left[\frac{\pi}{X} \right] \quad (\text{Eq 3.21})$$

As the value of X increases and π/X decreases the $\tan^{-1}(\pi/X)$ approaches π/X , and ω approaches ω_a . In general, the clock frequency should be approximately 10 times greater than the highest analog frequency to minimize warping effects [Ref. 9]. Figure 3.5 shows the ratio of ω to ω_a versus the ratio of ω_{clock} to ω_a .

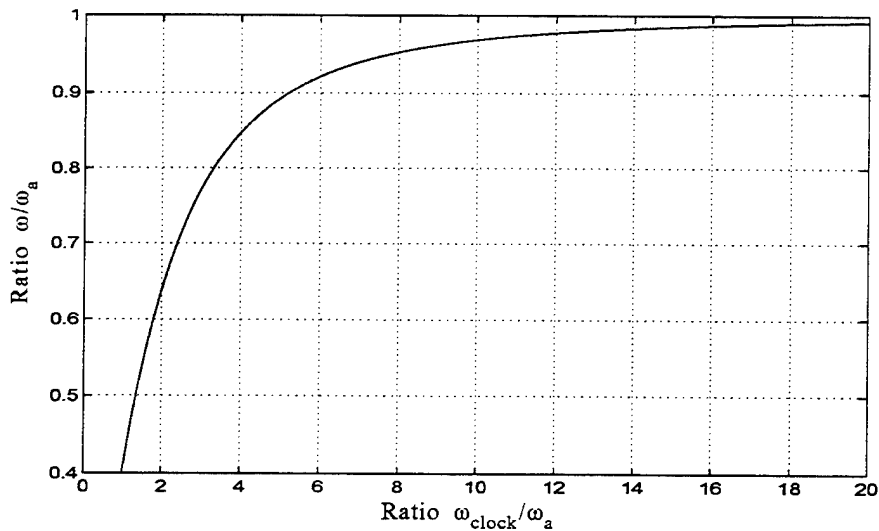


Figure 3.5: The Effects of Frequency Warping

F. ELEMENT TRANSFORMATIONS

It is sometimes useful to take an element by element replacement approach to switched capacitor network design rather than transform an entire analog network all at once. This approach is particularly useful when the analog network to be converted is complex enough to make the transformation to the z -domain cumbersome. In the element by element

approach, resistors, capacitors and inductors are substituted with their equivalent switched capacitor networks. This one-for-one replacement requires the generic z-domain conversion of resistors and capacitors using the four previously mentioned transformation methods. The equivalent device admittances are used to facilitate the transformation. The sampling nature of switched capacitors make the network admittances time dependant. This time dependance can be best qualified by charge analysis. Because of this affect, admittances take the form of $\Delta Q/V$ in lieu of the traditional I/V approach.

1. Resistor

The relationship between voltage and current across a resistor can be described as Eq. 3.22.

$$i(t) = Gv(t) \quad (\text{Eq 3.22})$$

where $G=1/R$. If charge q is introduced,

$$\frac{dq(t)}{dt} = Gv(t) \quad (\text{Eq 3.23})$$

and the Laplace transform is applied, then

$$sQ(s) - q(0) = GV(s) \quad (\text{Eq 3.24})$$

With the initial condition $q(0) = 0$,

$$\frac{Q(s)}{V(s)} = \frac{G}{s} \quad (\text{Eq 3.25})$$

2. Capacitor

The relationship for current and voltage across a capacitor is

$$i(t) = c \frac{dv(t)}{dt} \quad (\text{Eq 3.26})$$

When charge q relationship is used, we have

$$\frac{dq(t)}{dt} = c \frac{dv(t)}{dt} \quad (\text{Eq 3.27})$$

Then by applying the Laplace transform, the equation becomes

$$sQ(s) - q(0) = c(sV(s) - v(0)) \quad (\text{Eq 3.28})$$

With the initial conditions, $q(0) = v(0) = 0$, the result simplifies to

$$\frac{Q(s)}{V(s)} = C \quad (\text{Eq 3.29})$$

3. Inductor

The voltage-current relationship for an inductor is

$$v(t) = L \frac{di(t)}{dt} \quad (\text{Eq 3.30})$$

When charge q relationship is used, the relationship becomes

$$v(t) = L \frac{d^2 q(t)}{dt^2} \quad (\text{Eq 3.31})$$

Applying the Laplace transformation to Eq. 1.31, results in

$$V(s) = L \left(s^2 Q(s) - sq(0) - \frac{dq(0)}{dt} \right) \quad (\text{Eq 3.32})$$

With the initial conditions $\frac{dq(0)}{dt}$ and $(q(0))$ set to 0, Eq 3.32 simplifies to

$$\frac{Q(s)}{V(s)} = \frac{1}{Ls^2} \quad (\text{Eq 3.33})$$

The forward, backward and bilinear s to z transformations are applied to the s domain models for the resistor, capacitor and inductor. The results of these transformations are listed in Table 3.1.

To facilitate the realization of switched capacitor networks, the admittances of Table 3.1 are scaled by a factor of $1 - z^{-1}$. This scaling forces the capacitor admittance for each transformation to be

$$C(1 - z^{-1}) \quad (\text{Eq 3.34})$$

which is easily realizable with hardware [Ref. 8]. Since voltage transfer functions are dimensionless, they are unaffected by the change in admittance definition or the scaling [Ref. 8]. The results of the scaled admittances are listed in Table 3.2.

Transformation	s	C	$\frac{G}{s}$	$\frac{1}{Ls^2}$
Forward	$\frac{1-z^{-1}}{\tau z^{-1}}$	C	$\frac{G\tau z^{-1}}{1-z^{-1}}$	$\frac{\tau^2 z^{-2}}{L(1-z^{-1})^2}$
Backward	$\frac{1-z^{-1}}{\tau}$	C	$\frac{G\tau}{1-z^{-1}}$	$\frac{\tau^2}{L(1-z^{-1})^2}$
Bilinear	$\frac{2(1-z^{-1})}{\tau(1+z^{-1})}$	C	$\frac{G\tau(1+z^{-1})}{2(1-z^{-1})}$	$\frac{\tau^2(1+z^{-1})^2}{4L(1-z^{-1})^2}$

Table 3.1. Z-domain Admittances (unscaled).

Transformation	C	$\frac{G}{s}$	$\frac{1}{Ls^2}$
Forward	$C(1-z^{-1})$	$G\tau z^{-1}$	$\frac{\tau^2 z^{-2}}{L(1-z^{-1})}$
Backward	$C(1-z^{-1})$	$G\tau$	$\frac{\tau^2}{L(1-z^{-1})}$
Bilinear	$C(1-z^{-1})$	$\frac{G\tau(1+z^{-1})}{2}$	$\frac{\tau^2(1+z^{-1})^2}{4L(1-z^{-1})}$

Table 3.2. Z-domain Admittances (scaled).

G. THE BILINEAR RESISTOR

The governing equations for a floating bilinear switched capacitor resistor used in the construction of the GIC filter must be developed next. The switched capacitor network depicted in Figure 3.6 will be analyzed using nodal charge conservation techniques.

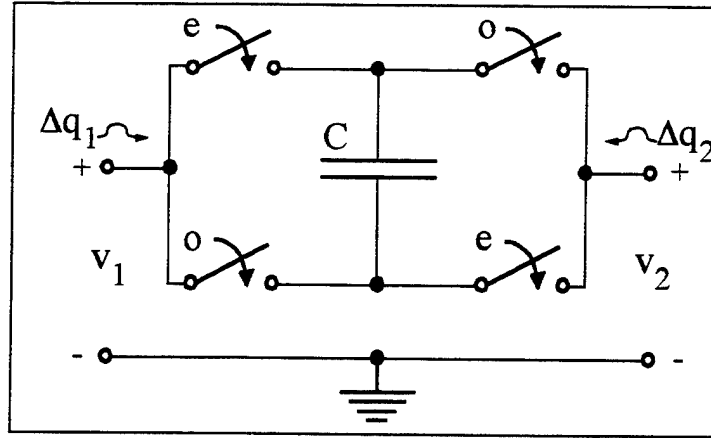


Figure 3.6: Floating Bilinear Resistor

Using the concept of separate topologies for the even and odd phases of the biphase network forces the requirement for two distinct but coupled charge equations for each node. The master clock period depicted in Figure 3.2 is denoted as τ with $T = \tau/2$, the sampling instant kT represents the instantaneous redistribution of charge at the specific nodes for the even and odd sampling periods. The general equations 3.35 and 3.36 from Laker [Ref. 8] represent the charge in the i th capacitor connected at a specific node p in the time domain for the even and odd sampling instances. The variable M denotes the total number of capacitors connected to node p .

$$\Delta q_p^e(kT) = \sum_{i=1}^{M_{ep}} q_{pi}^e(kT) - \sum_{i=1}^{M_{ep}} q_{pi}^o[(k-1)T] \quad \text{for } k \text{ an even integer} \quad (\text{Eq 3.35})$$

$$\Delta q_p^o(kT) = \sum_{i=1}^{M_{op}} q_{pi}^o(kT) - \sum_{i=1}^{M_{op}} q_{pi}^e[(k-1)T] \quad \text{for } k \text{ an odd integer} \quad (\text{Eq 3.36})$$

In the z domain, the even and odd sampling instances are represented in Eq. 3.37 and Eq. 3.38.

$$\Delta Q_p^e(z) = \sum_{i=1}^{M_{ep}} Q_{pi}^e(z) - z^{-1/2} \sum_{i=1}^{M_{ep}} Q_{pi}^o(z) \quad \text{for } k \text{ an even integer} \quad (\text{Eq 3.37})$$

$$\Delta Q_p^o(z) = \sum_{i=1}^{M_{op}} Q_{pi}^o(z) - z^{-1/2} \sum_{i=1}^{M_{op}} Q_{pi}^e(z) \quad \text{for } k \text{ an odd integer} \quad (\text{Eq 3.38})$$

The second terms on the right hand side of Equations 3.35, 3.36, 3.37 and 3.38 represent the initial conditions of the node for the kT sampling instance.

Using the relationship $Q = CV$, the charge conservation equations for the network in Figure 3.5 can be written as

$$\Delta Q_1^e(z) = CV_1^e(z) + Cz^{-1/2}V_1^o(z) - \left(CV_2^e(z) + Cz^{-1/2}V_2^o(z) \right) \quad (\text{Eq 3.39})$$

$$\Delta Q_1^o(z) = CV_1^o(z) + Cz^{-1/2}V_1^e(z) - \left(CV_2^o(z) + Cz^{-1/2}V_2^e(z) \right) \quad (\text{Eq 3.40})$$

$$\Delta Q_2^e(z) = CV_2^e(z) + Cz^{-1/2}V_2^o(z) - \left(CV_1^e(z) + Cz^{-1/2}V_1^o(z) \right) \quad (\text{Eq 3.41})$$

$$\Delta Q_2^o(z) = CV_2^o(z) + Cz^{-1/2}V_2^e(z) - \left(CV_1^o(z) + Cz^{-1/2}V_1^e(z) \right) \quad (\text{Eq 3.42})$$

The charge equations for node one and node two are added to obtain

$$\Delta Q_1(z) = C \left(1 + z^{-1/2} \right) V_1(z) - C \left(1 + z^{-1/2} \right) V_2(z) \quad (\text{Eq 3.43})$$

$$\Delta Q_2(z) = C \left(1 + z^{-1/2} \right) V_2(z) - C \left(1 + z^{-1/2} \right) V_1(z) \quad (\text{Eq 3.44})$$

The forms of Equations 3.43 and 3.44 can be rewritten as

$$\Delta Q = Y_R V_x - Y_R V_y \quad (\text{Eq 3.45})$$

The impedance Y_R is represented by

$$Y_R = C \left(1 + z^{-1/2} \right) \quad (\text{Eq 3.46})$$

If the dummy variable $z' = e^{s\tau/2}$ is substituted for $z = e^{s\tau}$ in Eq. 3.46, then

$$Y_R = C \left(1 + z'^{-1} \right). \quad (\text{Eq 3.47})$$

The admittance identified by equation 3.47 exactly matches the admittance calculated for a bilinear resistor in Table 3.2. The admittance of a theoretical bilinear resistor from Table 3.2 and the calculated admittance of the network in Figure 3.5 (Eq. 3.47) are equated in Eq. 3.48.

$$C \left(1 + z'^{-1} \right) = \frac{G\tau \left(1 + z^{-1} \right)}{2} \quad (\text{Eq 3.48})$$

Simplifying Eq. 3.48 and rearranging, yields the admittance

$$G = \frac{2C}{\tau} \quad (\text{Eq 3.49})$$

The substitution of z with z' must now be accounted for. The substitution of the dummy variable can be viewed as dividing the clock rate or sampling period by two. The actual higher sampling rate is restored by multiplying Eq. 3.49 by 2, resulting in the actual admittance of the bilinear resistor of Figure 3.5

$$G = \frac{4C}{\tau} \quad (\text{Eq 3.50})$$

H. CONCLUSION

Equation 3.5 can be used to determine the appropriate ratio of clock frequency to capacitor value to obtain a desired equivalent admittance. The effects of frequency warping cannot be forgotten. To incorporate both the warping effects and the admittance requirements for the switched capacitor networks in this design, the clock frequency is first

determined to significantly reduce the warping effects for the highest analog frequency expected by the GIC filter. The equivalent resistance is then achieved by choosing an appropriately sized capacitor.

IV. THE INTEGRATED PROGRAMMABLE GENERALIZED IMMITTANCE CONVERTER FILTER

A. INTRODUCTION

The goal of this research is the integration of a programmable three stage Generalized Immittance Converter filter. This chapter combines the GIC filter of chapter two, the switched capacitors of chapter three, networks to make the GIC programmable, and design limitations of Very Large Scale Integration (VLSI). The latter two subjects can not be considered separately because VLSI causes a trade-off in programmability and vice versa. Only design constraints caused by VLSI are addressed in this chapter and further details of the integration are left to chapter five. The integrated design will be manufactured through MOSIS, an organization who acts as a clearing house for low volume manufacturing of custom microchips.

B. OPTIONS AND LIMITATIONS

The depth of programmability for this design is mainly limited by layout area and the maximum number of pins on the chip package. The package size used in this design is limited by available funding to 40 pins and a 2.25 by 2.20 millimeter layout area. Nine of the 40 pins are required for analog and digital power supplies, ground and a clock input. The assignments for the 10 overhead pins are shown in Figure 5.6. The remaining 30 pins are divided equally among the three GIC stages specified as a design goal. A larger package with additional pins would allow greater frequency control through separate clock inputs to each GIC section. It would also provide for the capability of programming the order of the filter by controlling the cascading of the three independent GIC sections. Table 4.1 lists the pin assignments for a single GIC stage.

Following the selection of pin assignments, layout area becomes the primary design constraint. The "tiny" chip design specified by the MOSIS manufacturing process has an allowable area or die size of 2,200 by 2,250 microns using the two micron silicon technology. Unfortunately, predetermining the layout area would require in depth

parametric models, and the design limits are best tested by physically constructing devices while keeping the permitted overall layout area in mind.

Function	# of Pins
Input	1
Output	1
Topology	2
Frequency	3
Quality	3
Total	10

Table 4.1. Number of Pins Required for a Single Stage Programmable GIC Filter

C. PROGRAMMING TOPOLOGY

The four filter types realized by this design are highpass, lowpass, bandpass and notch filters. An all pass filter can easily be constructed using the GIC design, but programming of five filter types would require a three bit control signal rather than the two bit signal, which is shown later, required to program four types. The extra bit would be needed for each filter section, and would add the requirement of three more pins for the entire chip.

The four topologies of the GIC filter are realized by replacing the admittances indicated in the circuit of Figure 2.2 with the appropriate discrete values found in Table 2.2. Admittance values for Y1 and Y4 are G for all four topologies. Similarly, the admittance value for Y2 is C for three topologies and C plus a parallel resistance for the special case of the Lowpass filter. The consistent discrete values of these three admittances allows the corresponding components to be connected directly to the appropriate nodes of the GIC filter. The remaining admittances are represented in each topology by one of four discrete components or an open circuit. The four components consist of three resistors, two with admittance G and one with admittance G_q , and a capacitor with admittance C. Figure 4.1

shows the GIC filter with discrete components and the required switches needed to relocate the above four components in order to realize the four filter configurations. Figure 4.2 from Michael [Ref. 10] separates the discrete components with their appropriate switches, connecting nodes and admittances realized for each topology and is used to generate the logic required to control the 18 switches. The position of each switch in Figures 4.1 and 4.2 is shown for each filter configuration in truth table one of Figure 4.3. Truth table one entries are combined where the logic is identical in truth table two of Figure 4.3. By observation, it is noted that columns one, three and seven are the inverse of columns two, four and eight respectively. Additionally, it is noted that column five, which represents switches S_6 and S_{10} , corresponds to the inverse of the input bit "fa". Truth Table 3 of Figure 4.3 summarizes the logic required to control topology switching. The logic circuit that performs switching control for the different topologies is depicted in Figure 4.4.

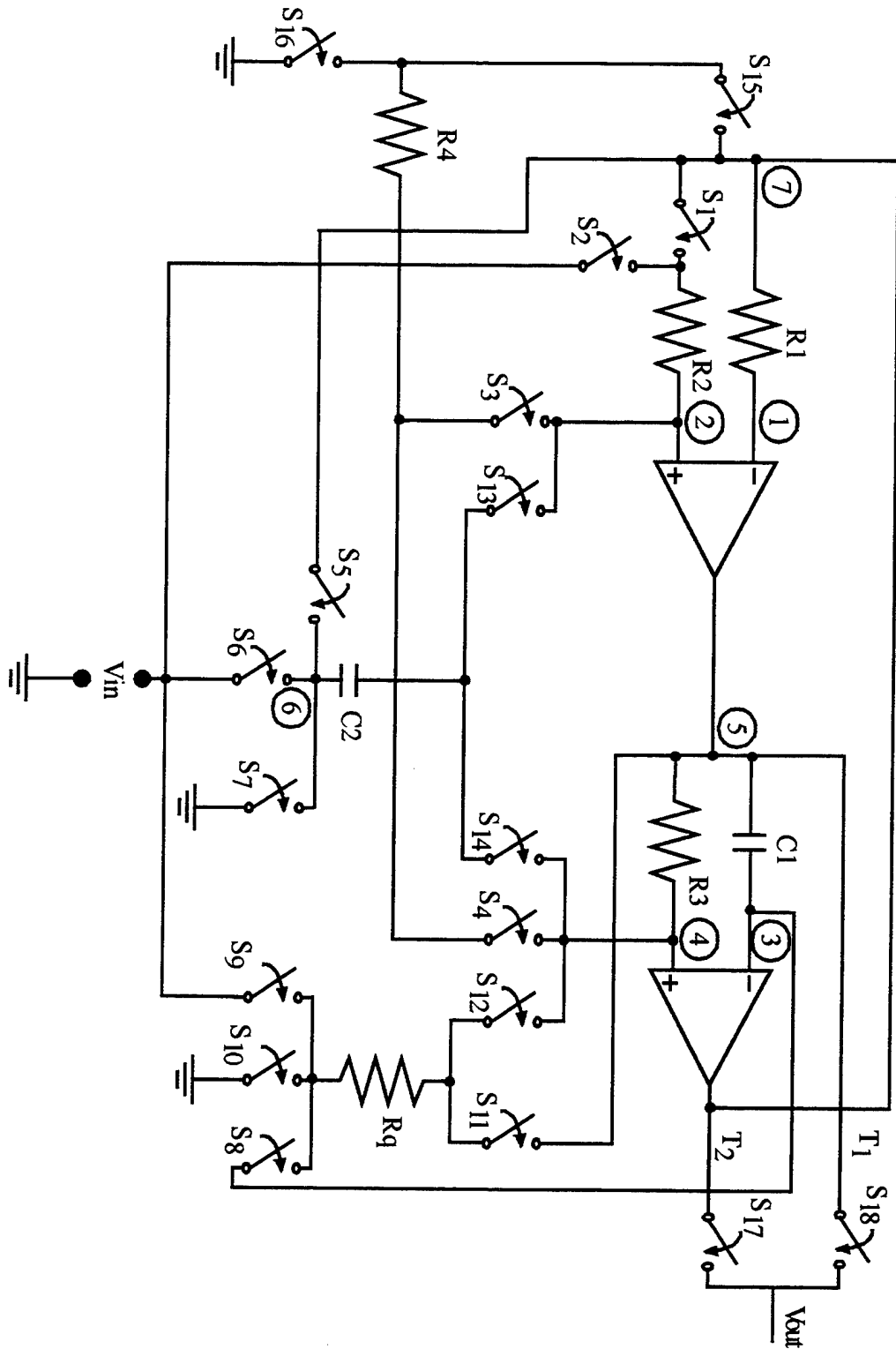


Figure 4.1: The GIC Filter with Programmable Topology

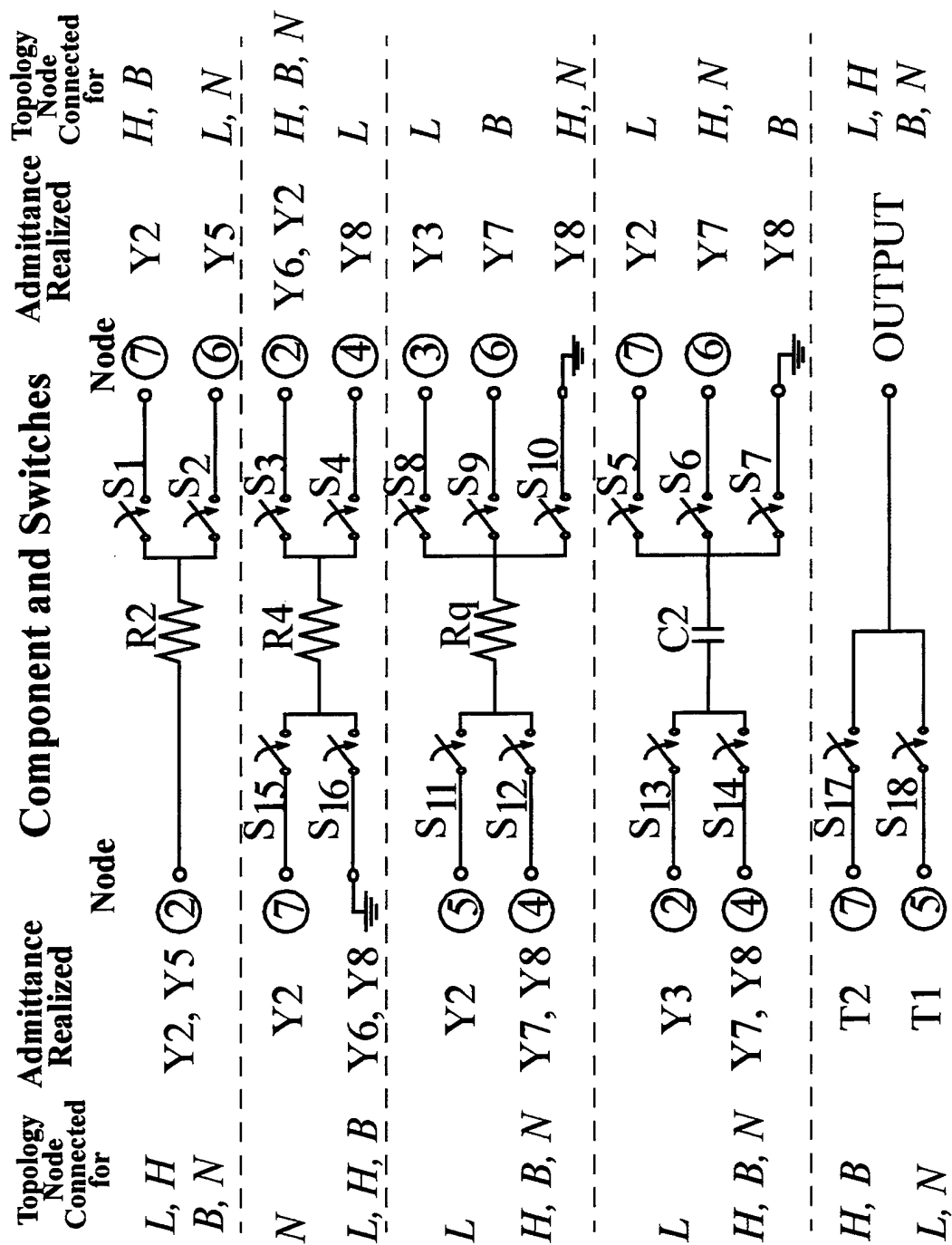


Figure 4.2: Discrete Components, Switches and Affected Nodes for Topology Programming of the GIC Filter

Truth Table 1																			
Input	Filter Type	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁	S ₁₂	S ₁₃	S ₁₄	S ₁₅	S ₁₆	S ₁₇	S ₁₈
11	Lowpass	0	1	0	1	1	0	0	1	0	0	1	0	1	0	0	1	0	1
01	Highpass	1	0	1	0	0	1	0	0	0	1	0	1	0	1	0	1	1	0
10	Bandpass	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	1	0
00	Notch	0	1	1	0	0	1	0	0	0	1	0	1	0	1	1	0	0	1



Input	Filter Type	S ₁ S ₁₇	S ₂ S ₁₈	S ₃ S ₁₂ S ₁₄	S ₄ S ₅ S ₈ S ₁₁ S ₁₃	S ₆ S ₁₀	S ₇ S ₉	S ₁₅	S ₁₆
11	Lowpass	0	1	0	1	0	0	0	1
01	Highpass	1	0	1	0	1	0	0	1
10	Bandpass	1	0	1	0	0	1	0	1
00	Notch	0	1	1	0	1	0	1	0



Input (fa,fb)	Filter Type	S ₂ S ₁₈	S ₃ S ₁₂ S ₁₄	S ₇ S ₉	S ₁₆
11	Lowpass	1	0	0	1
01	Highpass	0	1	0	1
10	Bandpass	0	1	1	1
00	Notch	1	1	0	0

Truth Table 2

Truth Table 3

Figure 4.3: Truth Tables for Topology Programming Logic

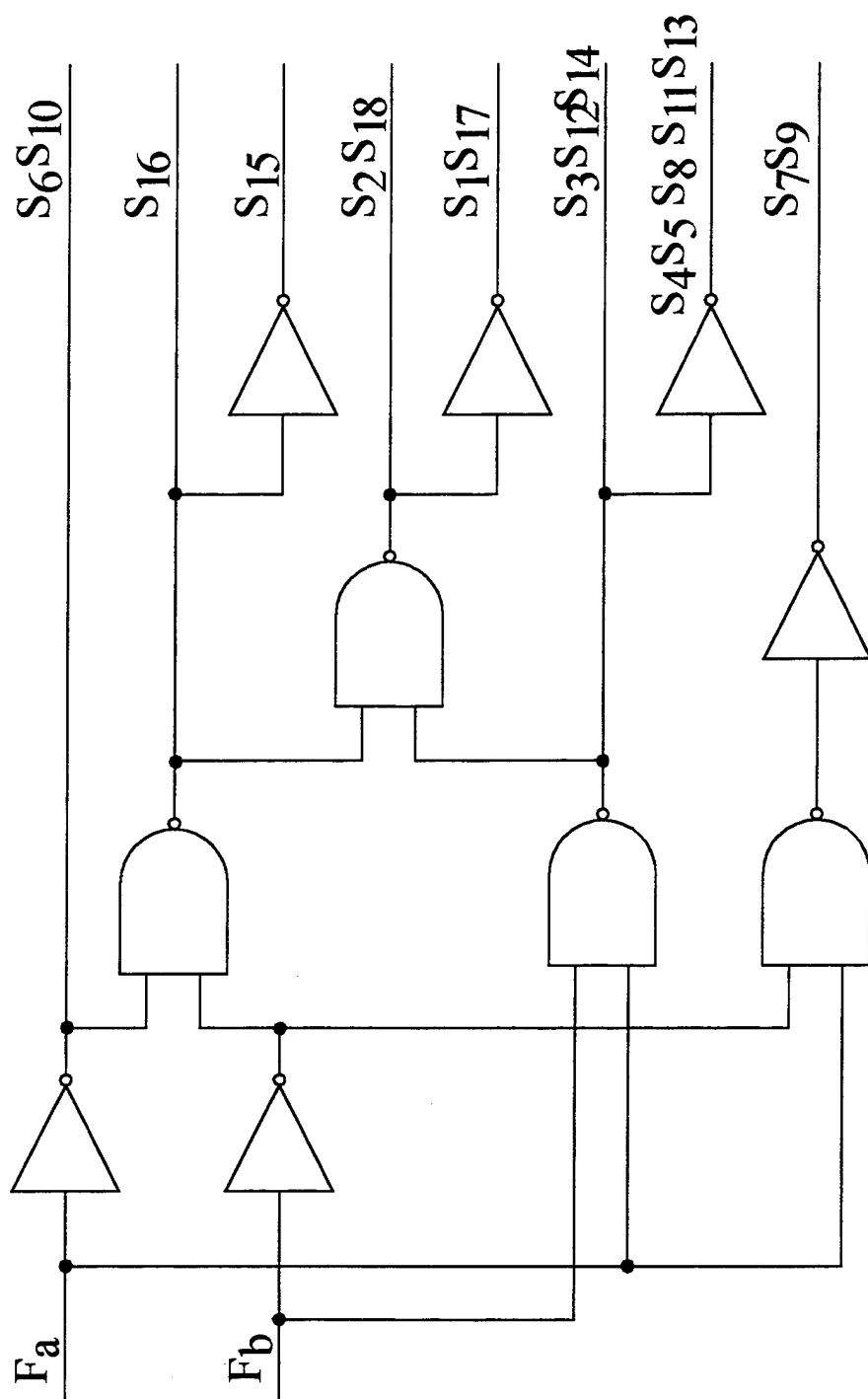


Figure 4.4: Logic Circuit to Control Topology Switching

D. SWITCHED CAPACITORS AND PROGRAMMABILITY

The use of switched capacitors to realize resistances has a very positive effect on programmability. Equations 2.5 and 2.8 describe the determination of corner or center frequency and quality factor for a GIC filter respectively and are reiterated in the following Equations 4.1 and 4.2.

$$\omega_p = \frac{G}{C} \quad (\text{Eq 4.1})$$

$$Q_p = \frac{G}{G_q} \quad (\text{Eq 4.2})$$

If the equivalent admittance for a switched capacitor realization as given by Eq. 2.51, and reiterated in Eq. 4.3, is combined with equations 4.1 and 4.2, the results are the frequency and quality factor selectivity for a switched capacitor GIC filter. These results are given as Equations 4.4 and 4.5. Equation 4.4 can be further simplified by converting the units of all frequencies into cycles per second (Hz). The result is shown as Eq. 4.6.

$$G = \frac{4C_r}{T_{\text{clock}}} \quad (\text{Eq 4.3})$$

$$\omega_p = \frac{4C_r}{CT_{\text{clock}}} \quad (\text{Eq 4.4})$$

$$Q_p = \frac{4C_r T}{4C_{qr} T} = \frac{C_r}{C_{qr}} \quad (\text{Eq 4.5})$$

$$f_p = \frac{0.6366C_r}{C} f_{\text{clock}} \quad (\text{Eq 4.6})$$

For notation purposes, the capacitors in the bilinear switched capacitor networks representing G and G_q will be referred to as resistor capacitance and quality capacitance respectively. The remaining two capacitances in the GIC filter network will be referred to as frequency capacitors.

Equation 4.5 shows that by simply adjusting the ratio of resistor capacitance to quality capacitance, quality factor can be controlled. By adjusting the ratio of frequency capacitors to resistor capacitance, frequency is adjusted relative to a common clock frequency. The operating parameters for any topology of the GIC filter are therefore determined by the relative sizes of three sets of capacitors. When the size of the resistor capacitor, and hence the resistance of the bilinear network for the common resistance, is fixed, quality capacitance and frequency capacitance can be adjusted separately to independently control the corner frequency and quality factor of the filter.

E. CAPACITOR SIZING

The size of the resistor capacitor must be properly chosen so that the programmable range of the filter is acceptable. Small parasitic capacitances exist between layers in a silicon chip. The operating value of the resistance, quality and frequency capacitances must not approach that of the parasitic capacitances. As the operating capacitors get smaller, the parasitic capacitances provide a larger percentage of the network capacitance and their affect becomes more debilitating. Excessively large capacitances, on the other hand, are precluded by layout area. The largest parasitic capacitance seen by an operating capacitor in the GIC layout is approximately 15 femptofarads. The smallest value for a discrete capacitor used in the circuit is chosen as 100 femptofarads. This value is almost an order of magnitude larger than the parasitic capacitance, with which it is associated.

Recalling that pole quality factor is determined by the ratio of resistor capacitance to quality capacitance, develops the relationship of capacitor sizes for high and low pole qualities. For much desired high quality factors, the quality capacitance must be lower than the resistor capacitance. A reversed relationship exists between the resistor capacitance and the frequency capacitance. Because of the warping effect described in Chapter Two the clock frequency must be approximately 10 times the pole corner frequency. To determine the minimum size frequency capacitor relative to the resistor capacitor, $10f_p$ is substituted for f_{clock} in Eq. 4.6 and the results are written in Eq. 4.7

$$C_f = 6C_r \quad (\text{Eq 4.7})$$

The minimum size frequency capacitor must be at least 6 times the size of the resistor capacitor. The spread of capacitor sizes ranges from the smallest valued quality capacitors to the largest valued frequency capacitors, with the resistor capacitor falling in between these two.

The quality capacitors represent the smallest valued discrete capacitors, and they are, therefore, assigned the smallest allowable capacitance value of 100 femptofarads. Given the relationship of Eq. 4.7, the relative sizes of the smallest value quality capacitors to the smallest value frequency capacitors is given by Eq. 4.8.

$$C_f = 6Q_{p(\text{highest})} C_q \quad (\text{Eq 4.8})$$

For a pole quality of ten, the frequency capacitor will have to be 60 times the size of the quality capacitor. High pole quality factors would consume a great deal of layout area in this programmable circuit.

F. PROGRAMMING POLE FREQUENCY AND QUALITY FACTOR

A maximum pole quality factor of five is chosen as a trade-off between high quality factors and layout area. The smallest value of frequency capacitance is 30 times 100 femptofarads or 3 picofarads. The resistor capacitance value is 500 femptofarads and will be implemented on the chip as a single capacitor. Further details of layout design are covered in Chapter V.

The range of values for the pole quality factor is varied from the maximally flat characteristic at $Q_p = 0.707$ to the maximum value $Q_p = 5$. The integer values of $Q_p = 1, 2, 3$ and 4 cover the range of the selectable pole quality factors. A three bit control signal can allow for the selection of up to eight different values of the quality factor, but the current design uses only six different values. Because of the VLSI design concerns, all capacitors are implemented using multiple copies of the same unit sized capacitor. The unit capacitor chosen for this design is the resistor capacitor which has a value of 500 femptofarads. The

quality capacitor which must range in size from 100 to 707 femptofarads is made up of a combination of unit capacitors connected in both series and parallel fashion. Four unit capacitors, a network of switches and simple control logic are used to implement the quality capacitor. The network diagram is shown in Figure 4.5. Increasing the levels of selectivity of this network by two adds a significant amount of control logic with only a small increase in the fidelity of the quality factor selection. It is important to note that adding levels of selectivity to the design does not increase the maximum value of the available pole quality factor. The selectable levels of pole quality factor and their respective digital control signals are listed in Table 4.2. The control signals are carefully ordered to provide minimized control logic. Table 4.2 also describes the required state of the switches for the case of each control signal or pole quality factor. The circuit which implements the logic described in Table 1.2 is shown in Figure 4.6.

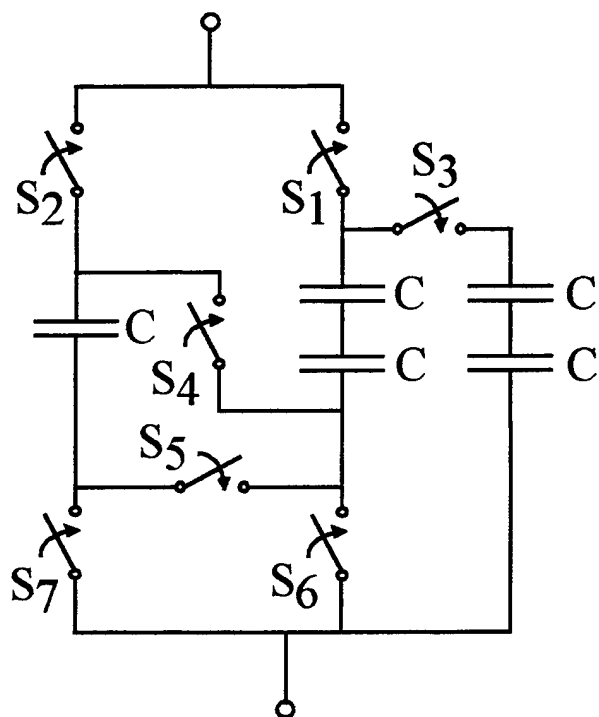


Figure 4.5: Network for Programming Pole Quality Factor

Pole Quality Factor	Control Signal (Q2,Q1,Q0)	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇
0.707	0 1 1	0	1	1	1	0	0	1
1	0 1 0	0	1	X	X	X	0	1
2	1 0 0	1	0	0	X	X	1	0
3	1 1 1	1	0	0	1	0	0	1
4	0 0 1	0	1	1	1	X	0	0
5	0 0 0	0	1	1	0	1	0	0

Table 4.2. Pole Quality Factor Truth Table

The presence of signals which are inversions of each other is particularly useful when implementing a CMOS pass gate or switch. When controlling a pass, gate both the control signal and the inverted control signal are required to ensure that the gate is either fully cut off or fully turned on. This is described in further detail in Chapter V. Figure 4.6 shows that this logic circuit takes advantage of the aforementioned inversion benefit.

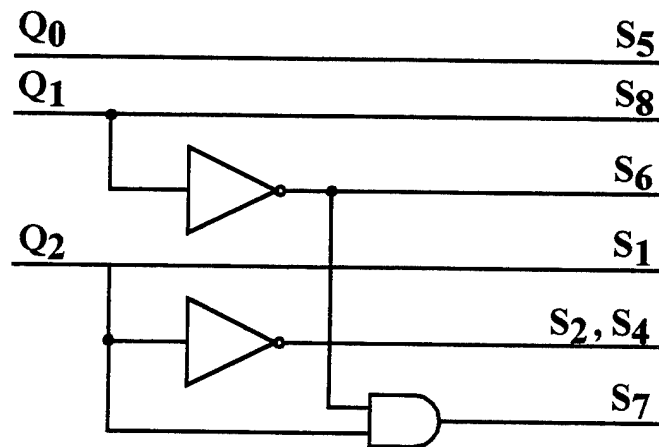


Figure 4.6: Logic Circuit to Control Pole Quality Factor Switching

To program the pole resonant frequency, the circuit of Figure 4.7 is used. The capacitor banks described are made up of multiple copies of the unit capacitor connected in parallel. The value C represents six unit capacitors or a total capacitance of three picofarads. The values $2C$ and $4C$ represent six picofarads and eight picofarads respectively. By controlling which capacitors are connected with a three bit control signal, eight levels of selectivity are achieved. The switches in the circuit of Figure 4.7 are driven directly by the control signals F_2 , F_1 and F_0 . The control signals and their resultant pole resonant frequencies are listed in Table 4.3. It is important to note that the frequencies listed are scaled values of the clock frequency, which must be given before exact corner frequencies can be determined. Regardless of the clock frequency or control signal, the corner frequency is always less than one tenth that of the clock, practically eliminating any frequency warping that might otherwise occur. Adjustment or programmability of the clock frequency would greatly increase the robustness of this filter and should be investigated in follow-on designs. The clock could be scaled down and programmed through a series of flip flops but the control would require a larger chip package.

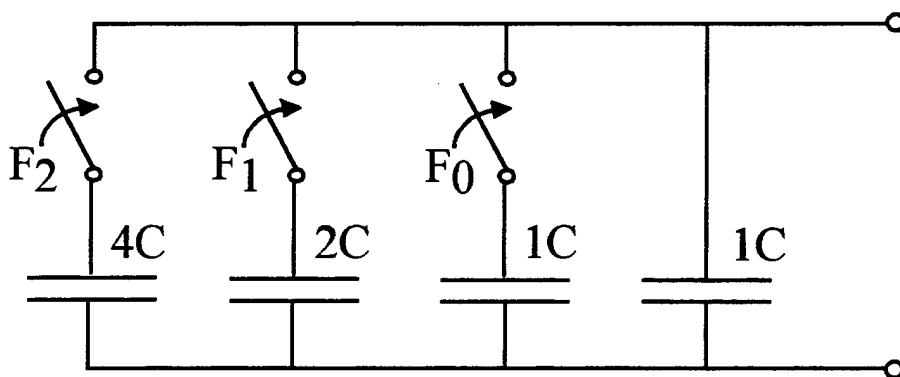


Figure 4.7: Switching Network to Realize Pole Resonant Frequency Programmability

Control Signal (F2,F1,F0)	Capacitance Realized	Corner Frequency (as function of f_{clock})	Corner Frequency ($f_{\text{clock}}=1\text{MHz}$)
0 0 0	1C	$0.1061(f_{\text{clock}})$	106 kHz
0 0 1	2C	$0.0531(f_{\text{clock}})$	53.1 kHz
0 1 0	3C	$0.0354(f_{\text{clock}})$	35.4 kHz
0 1 1	4C	$0.0265(f_{\text{clock}})$	26.5 kHz
1 0 0	5C	$0.0212(f_{\text{clock}})$	21.2 kHz
1 0 1	6C	$0.0177(f_{\text{clock}})$	17.7 kHz
1 1 0	7C	$0.0152(f_{\text{clock}})$	15.2 kHz
1 1 1	8C	$0.0133(f_{\text{clock}})$	13.3kHz

Table 4.3. Programmable Control of Pole Resonant Frequency

V. VLSI LAYOUT OF THE PROGRAMMABLE GIC FILTER

A. SEMICONDUCTORS

Silicon which is a semiconductor is the primary constituent of a metal oxide silicon process (MOS). Pure silicon, which is allowed to crystallize into a stable lattice form, has current carrying properties that fall between that of a conductor and an insulator. The silicon atom has four electrons in its outermost shell, but the desirable number of electrons for this shell to reach a low energy state is eight. To compensate for the lack of four electrons, the atoms form a lattice in which they share a single electron with each of their four neighboring atoms. The bonds formed by the electrons that hold the lattice together are called covalent bonds. If sufficient energy is introduced into the lattice, some of the covalent bonds will be broken and an electron will be allowed to go free, leaving the parent atom positively charged. This positively charged atom is called a hole because it will very strongly attract other free electrons. The recombination of a hole and an electron will return that portion of the lattice to molecular equilibrium, allowing the next bit of excess energy to free another electron. This process continues repetitively and the conductive nature of silicon arises from the propagation, in opposite directions, of holes and electrons. The holes and electrons in a semiconductor are referred to as charge carriers.

By adding impurities into the lattice, the conductive properties of silicon can be changed. The impurities or dopant material added have either three or five electrons in their outer shell depending on whether a p-type or n-type material is desired. Adding a p-type dopant to the silicon lattice causes an imbalance in the outer shells of the impurity's neighboring silicon atoms because the impurity only contributes three electrons. The result is a silicon lattice where there are an excess number of holes. The holes in a p-type material are called the majority carrier. An imbalance in the crystal structure is also created if an n-type dopant is added to the crystal lattice. The impurity will share an electron with each one of its four silicon neighbors but since it has five electrons in its outer shell, one of the electrons will not be covalently bonded in the lattice. The majority carrier in this n-type

material is the electron. The n-type and p-type silicon have much greater conductivity than pure silicon.

B. METAL OXIDE SILICON TRANSISTORS

The MOS structure is created by forming layers of p-type silicon, n-type silicon, silicon dioxide (an insulator), polysilicon (a conductor) and metal. The n-type or p-type silicon in the form of a circular wafer constitutes the base of the structure called the substrate or bulk. Polysilicon is a silicon crystal structure which is not permitted to form in the previously mentioned uniform lattice. Because the polysilicon is composed of the same atoms as the substrate, it can be grown in very thin, smooth layers while still maintaining its structural integrity. The non-uniform polysilicon crystal is commonly used as a conductor to construct transistor gates and capacitor plates. Polysilicon has high resistivity, but these properties can be reduced by lacing the polysilicon with metal.

An n-type metal oxide silicon (NMOS) transistor is illustrated in Figure 5.1. Visualizing the transistor as a valve associates the source and drain of the transistor as the input and output and the gate as the control handle. The source and drain of the NMOS transistor are constructed from n-type material, and they are separated by a channel of p-type silicon. Electrons are the majority carrier in the source and drain, but the channel separating them has a majority carrier of holes and therefore relatively few free electrons. In this case, the source and drain separated by a high impedance. The gate, made of a conductor such as metal or polysilicon, is insulated from the p-type channel by a layer of silicon dioxide (glass). If a positive charge is placed on the gate, an electric field is established between the gate and the grounded substrate. This electric field repels the holes in the channel down and attracts the small number of free electrons in the substrate, creating a layer of free electrons, or n-type material, locally under the gate. The channel has the same majority carriers as the source and drain so that if a voltage is applied across them, current will flow.

A p-type metal oxide silicon (PMOS) transistor operates by the same principle as the NMOS. The PMOS transistor is shown in Figure 5.2. The source and drain are p-type material abundant with holes which are the charge carriers for this device. The substrate is n-type material and is connected to a positive voltage rather than ground. A p-channel (transistor is on) will be formed if the gate is grounded, and if a positive voltage is applied, minority carriers will populate the channel region causing the transistor to be turned off. Complementary metal oxide silicon (CMOS) combines NMOS and PMOS on the same wafer. A cross section of a CMOS process is shown in Figure 5.3. By placing either an n-type tub, known as an n-well, in p-type silicon or a p-well in n-type silicon, CMOS can be realized. There are some special problems associated with CMOS that will be addressed in Section C. The advantages of CMOS that will be discussed later far outweigh both the expense and problems associated with the process.

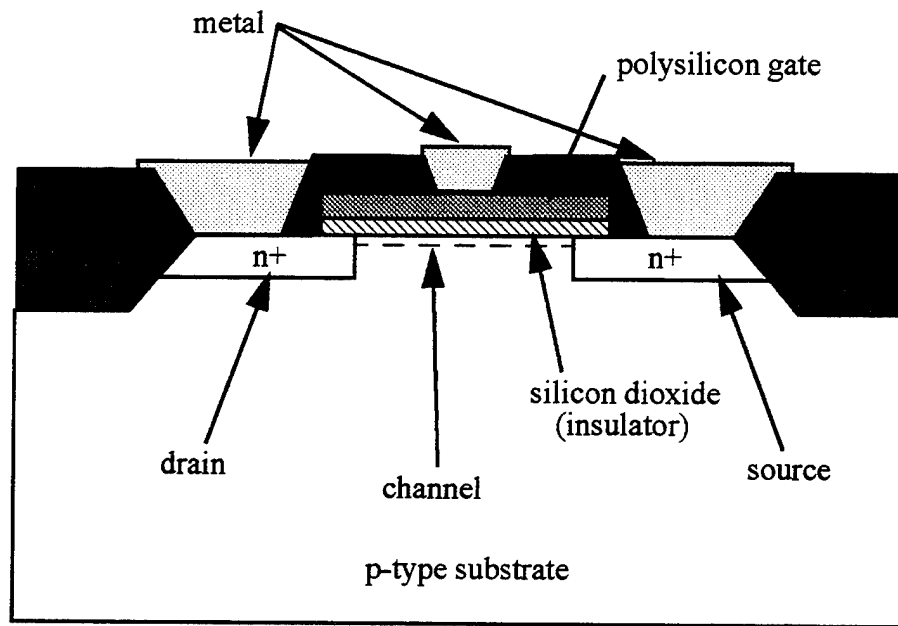


Figure 5.1: N-type Metal Oxide Silicon Transistor

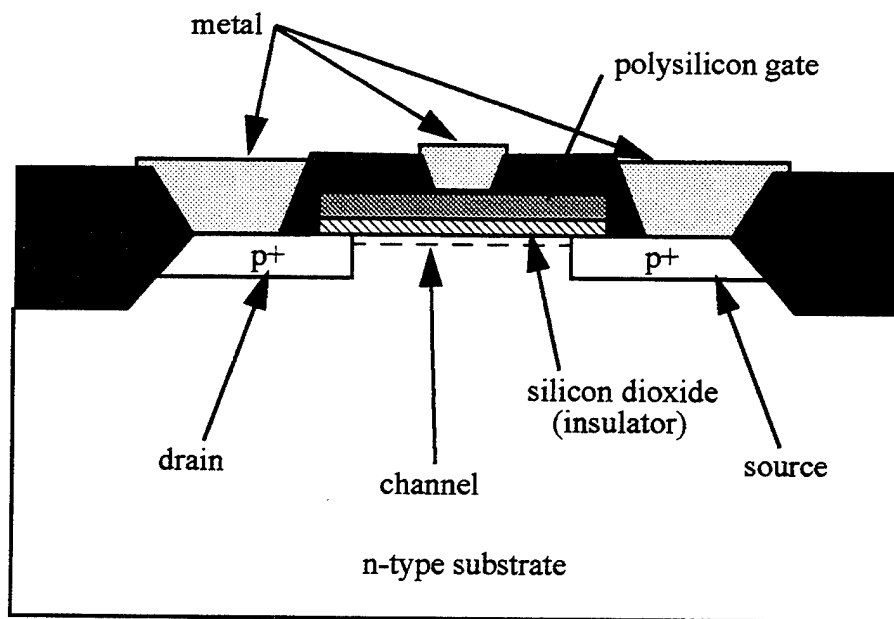


Figure 5.2: P-type Metal Oxide Silicon Transistor

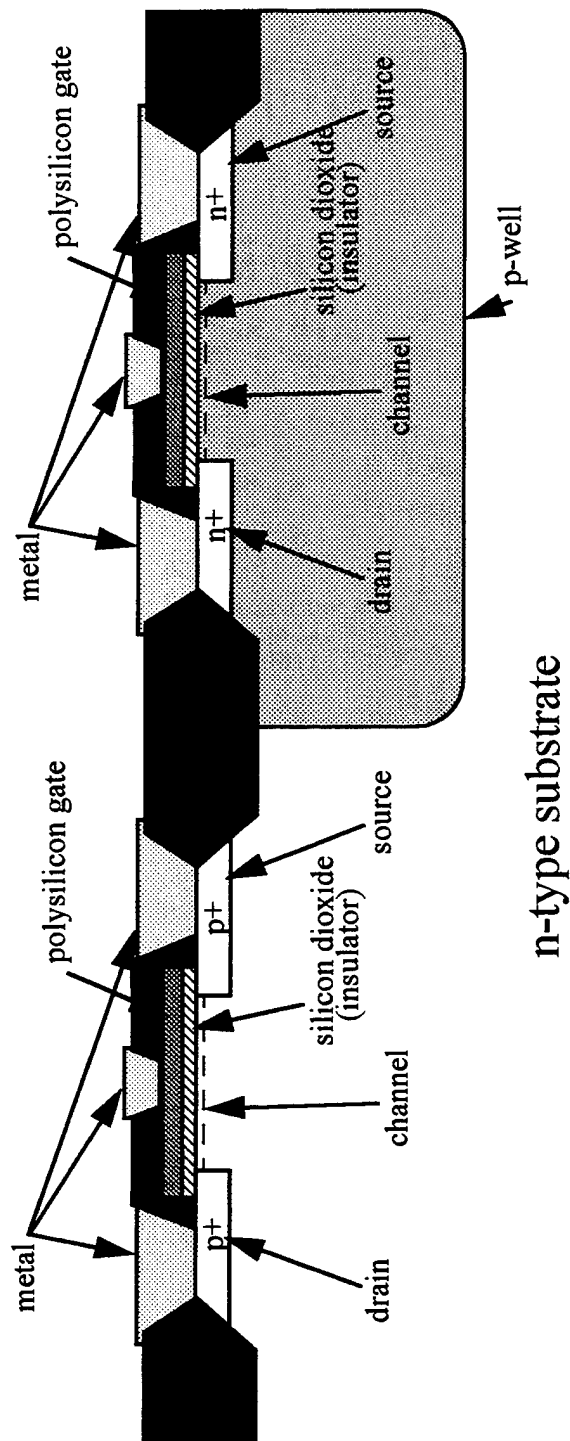


Figure 5.3: Complementary Metal Oxide Silicon Transistors

In practice, the operation of MOS transistors is not so black and white. MOS transistors have three regions of operation. The regions are depicted in Figure 5.4. The Y-axis is the drain-source current and the X-axis is the drain-source voltage. The three curves represent three different gate-source voltages.

The “cutoff” region is designated as such because the gate-source voltage is less than the threshold voltage and regardless of the drain-source voltage, current does not flow. In the “triode” region, the gate-source voltage is higher than the threshold voltage, but drain - source voltage is not significantly high. The following equation describes the voltage condition for the triode region.

$$v_{ds} \leq v_{gs} - v_t \quad (\text{Eq 5.1})$$

The saturation region occurs when the drain-source voltage becomes high relative to the gate-source voltage. This region is described by the following equation.

$$v_{ds} \geq v_{gs} - v_t \quad (\text{Eq 5.2})$$

In the saturation region, the channel is “pinched off” and the drain-source current is primarily dependant on gate-source voltage. Analog circuits most often operate in the pinch-off region.

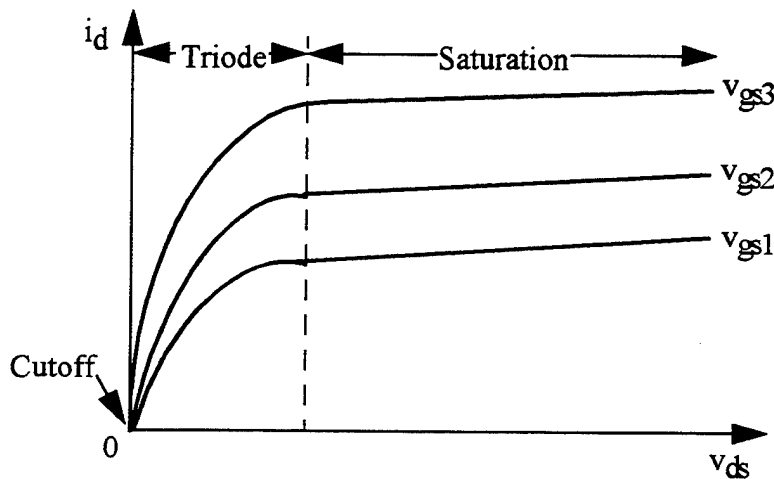


Figure 5.4: Operating Regions of a Field Effect Transistor

C. PROBLEMS ENCOUNTERED WITH VLSI LAYOUT

There are several design difficulties that must be addressed when constructing VLSI circuits. Some of the problems are specific to VLSI networks and some are consistent with the discrete counterparts of the integrated network. The ability of a gate or switch to fully cutoff or pass a signal is of great concern to the circuit designer. An NMOS transistor will pass a low voltage well, but a high voltage will be altered by the magnitude of the transistor threshold voltage. A PMOS transistor has the opposite effect. If an NMOS and PMOS transistor are used in conjunction, both high and low voltages will be acceptably passed. This configuration known as a pass gate connects the two types of transistors in parallel with the gates controlled by opposite signals. The layout of a pass gate is depicted in Appendix B.

Another problem associated with silicon transistor operation is the varying of the transistor threshold and substrate voltages. By ensuring that the substrate is locally connected to V_{dd} for a PFET and V_{ss} for an NFET, the transistor threshold voltages are stabilized across the chip. These contacts are called plugs. In a digital circuit, where the goal is to mainly pass "ones" equivalent to V_{dd} or "zeros" equivalent V_{ss} , the plugs can be connected directly to the sources of the transistors. In an analog circuit, the sources of the transistors are not necessarily connected to V_{dd} or V_{ss} , resulting in a mandatory separation distance between the sources, drains and plugs. An analog chip has an inherently smaller density of devices than a digital chip due to the required plug spacing.

There is another advantage to plugging the wells of a microchip. By keeping the p-type substrate at a low voltage and the n-type substrate at a high voltage, the natural p-n junction is reverse biased and current will not flow. Forward biasing of this junction is in effect a physical connection between V_{dd} and V_{ss} . This destructive phenomenon is known as latchup. Latchup is a primary concern when a chip is initially tested and current flow should be carefully monitored during power up.

Parasitic capacitances plague the operation of microchips just as they do for discrete networks. The problem with parasitic capacitances in analog VLSI layouts is that they can

easily approach the values of the component capacitors in the network. The speed of digital networks is primarily inhibited by parasitic capacitance. The majority of the parasitic capacitance arises from the active area of the transistor which can be rather large in analog networks where transistors with high betas are required. Parasitic capacitance in the GIC VLSI layout is on the order of 20 femptofarads. The smallest component capacitance in the network was chosen to be 100 femptofarads, and the majority of component capacitances are two orders of magnitude greater than the parasitic capacitances.

The combination of digital and analog networks on the same silicon substrate poses a problem with noise injection. The high frequency digital signals can inject noise through the substrate, power lines and capacitive coupling between components. The addition of high frequency noise to an analog circuit can at a minimum distort the output signal and at a maximum cause the network to go unstable. The transfer of noise is minimized by physically separating the digital and analog devices. This separation is the primary design consideration when planning the chip layout or floorplan, and it is the only method to disrupt capacitive coupling of digital noise. Another procedure that prevents noise distribution is the addition of guard rings around critical nodes. Guard rings are similar to plugs in that they are a connections from Vdd and Vss to the substrate. The local connections are made through a highly doped region, and they stabilize the substrate voltage in the area of the connection. The guard ring can be viewed as a trench that a noise spike must propagate through. If the spike is a high voltage, it will be absorbed by the Vss connection, and if it is a low voltage, it will be absorbed by the Vdd connection. Both guard rings and a smart floorplan are used to reduce propagation of digital noise into the analog section of the GIC filter on this chip.

D. COMPONENT LAYOUT

1. Capacitors

The very principals that make parasitic capacitance a problem in microchip design make the layout of the capacitor as a component a natural process. Capacitors are

constructed in the form of dielectrically insulated, parallel plates. The materials used for the plates and the dielectric can vary but some make more efficient capacitors than others. The basic governing equation for a parallel plate capacitor is

$$C = k\epsilon_0 \frac{A}{d} \quad (\text{Eq 5.3})$$

where ϵ_0 is the permittivity constant, k is the dielectric constant of the material between plates, A is the area of plate overlap, and d is the distance between plates. For a capacitor of a given physical size, the variables controlling the capacitance are k and d . Silicon dioxide or glass has the highest dielectric constant of any VLSI materials available so it is only natural to choose it as the dielectric. Metal to metal capacitors can be constructed, but the distance between the plates is relatively large due to the roughness of the metal. Polysilicon, however, has a smooth flat surface as well as good conductive properties so the plates can be placed very close together with a small layer of silicon dioxide as the dielectric. In an analog CMOS process, two layers of polysilicon are available and the construction of a capacitor is straight forward. The cross section of a poly-poly capacitor is shown in Figure 5.5.

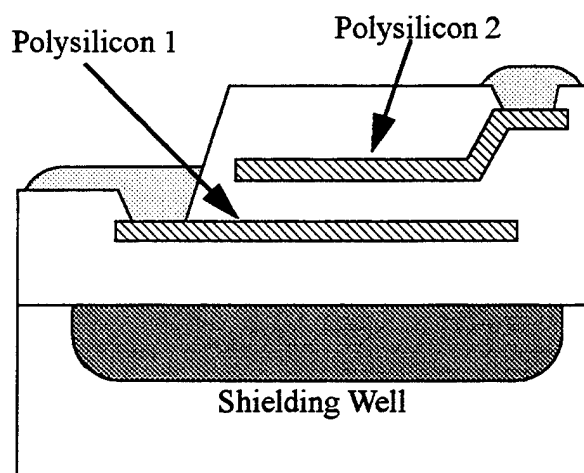


Figure 5.5: Capacitor Constructed with Two Layers of Polysilicon

2. Operational Amplifier

The operational amplifier used in this GIC network was initially developed in silicon by Silvernagle [Ref. 11]. The use of a commercial opamp, such as the TLC2201 manufactured by Texas Instruments, would improve the performance of the GIC filter, but the monolithic integration of such an opamp with this network would require detailed VLSI layout plans which are considered proprietary. This unfortunate circumstance requires the use of amplifier circuits for which detailed designs are available. The schematic of the opamp used in this design is shown in Figure 5.6, and the VLSI layout is depicted in Appendix B. This operational amplifier will be referred to as the Silvernagle opamp. The thesis research which led to the integration and manufacture of this opamp is detailed in Silvernagle [Ref. 11]. The Silvernagle opamp was simulated and experimentally tested before integration into the GIC filter.

The sensitivity of the GIC filter to the non-ideal properties of the operational amplifier are detailed in Michael [Ref. 9]. The GIC filter has very good sensitivity properties compared to other biquad filters, but to ensure good performance, the Silvernagle opamp was tested for gain-bandwidth product and slew rate. The results are compared with the TLC2201 CMOS opamp in Table 5.1. The gain bandwidth product and the slew rate of the Silvernagle opamp compare favorably with the commercial opamp and the measured values are close to the simulated parameters. The results of this testing qualified the Silvernagle operational amplifier for integration into the GIC filter.

Parameter	Silvernagle Opamp (measured)	Silvernagle Opamp (simulated)	TLC2201 Texas Instruments Opamp
Gain Bandwidth product (MHz)	1.7	1.6	1.8
Slew Rate (Volt/ μ sec)	4.2	5.5	2.5

Table 5.1. Operational Amplifier Performance Summary

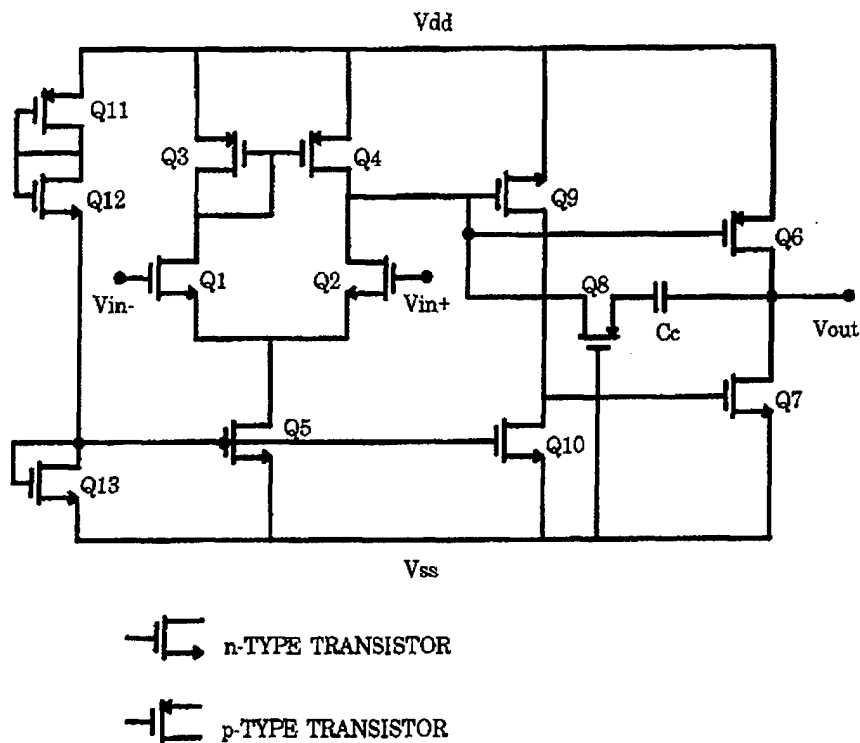


Figure 5.6: CMOS Operational Amplifier After Ref. [11]

3. Input and Output Pads

The input and output pads used to connect chip nodes to package pins via bond wires are taken from a VLSI library supplied by MOSIS. The analog input/output pads have integral guard rings to protect the internal chip from outside voltage spikes. The digital input and output devices offer high impedance opposite the direction of signal flow and a buffer to provide a low impedance input to either the internal chip or an off chip device. These pads form a ring around the entire layout, and they require their own power supply. Four of the package pins are used to supply the pad ring with Vdd and Vss.

E. FLOORPLAN FOR THE GIC FILTER

The floorplan and pad assignment for the three stage programmable GIC filter and the matching VLSI layout are shown in Figure 5.7. The matching VLSI layout of the filter is shown in Figure 5.8. Three GIC filter sections which are all oriented in the same direction are spaced evenly on the inside of the pad ring. The layout for a specific filter section is also displayed in Figure 5.7. The operational amplifiers and frequency capacitors are located at the top of the chip and the high frequency digital components, such as the two phase non-overlapping clock, are located at the bottom. The switched capacitor bilinear resistors are located adjacent to the clock. The logic and switching for selecting topology divides the purely analog and purely digital components. Some digital logic circuitry is located near the analog portion of the chip, but the switching is user selected by wiring the pins of the chip high or low, and therefore does not provide high frequency noise.

The following layout diagrams are located in Appendix B:

- Entire chip with the padding.
- Single stage programmable GIC filter.
- Operational amplifier.
- Frequency capacitor.
- Frequency selection logic.
- Topology control logic.
- Quality capacitor and control logic.
- Two phase non overlapping clock.
- Bilinear switched capacitor resistor.
- Pass Gate.

The layout was accomplished with a CAD tool called MAGIC, developed by The University of California, Berkeley.

F. SIMULATION

The GIC filter was first simulated using PSPICE. The first simulation was setup using ideal discrete components and the commercial TLC2201 MOSFET operational amplifier manufactured by Texas Instruments. Simulations were run for each topology. Frequency

was varied while keeping quality factor at 5, and then quality factor was varied while holding the frequency at 15 kHz. The filter performed as expected in each configuration.

The SPICE parameters for the VLSI layout were extracted using tools supplied with MAGIC. Most parasitic capacitances are accounted for with this extraction but, some are not. Specifically unaccounted for are parasitic capacitances for long poly or metal runs, and large source or drain areas. The largest capacitance per area exists where poly crosses p-diffusion or n-diffusion. This is known as the active area and the extraction will detail its dimensions. The simulation program is responsible for computing capacitance and beta of a transistor based on its device models and the extracted size of the active area. All nodes, including those for the switched capacitor networks, are extracted. PSPICE does not have the capabilities to converge on a solution when given mixed digital and analog signals. Because of this simulation shortfall, the extracted spice deck must be modified by replacing the sampled data networks with discrete components. Simulation software such as SWITCAP2 is designed to handle switched capacitors but is currently unavailable at the Naval Postgraduate School.

The results of the extracted simulations are shown along with the corresponding "ideal" simulations in Figures 5.9 through 5.24. The extracted simulations for each topology is nearly identical to the simulations done with the commercial operational amplifier. The simulations for the notch filter show the dependency of both quality factor and f_0 on the filters center frequency. Exact performance data can only be obtained through testing of the actual microchip but with better tools, such as an operating version of CADENCE and SWITCAP2, better simulations could be performed.

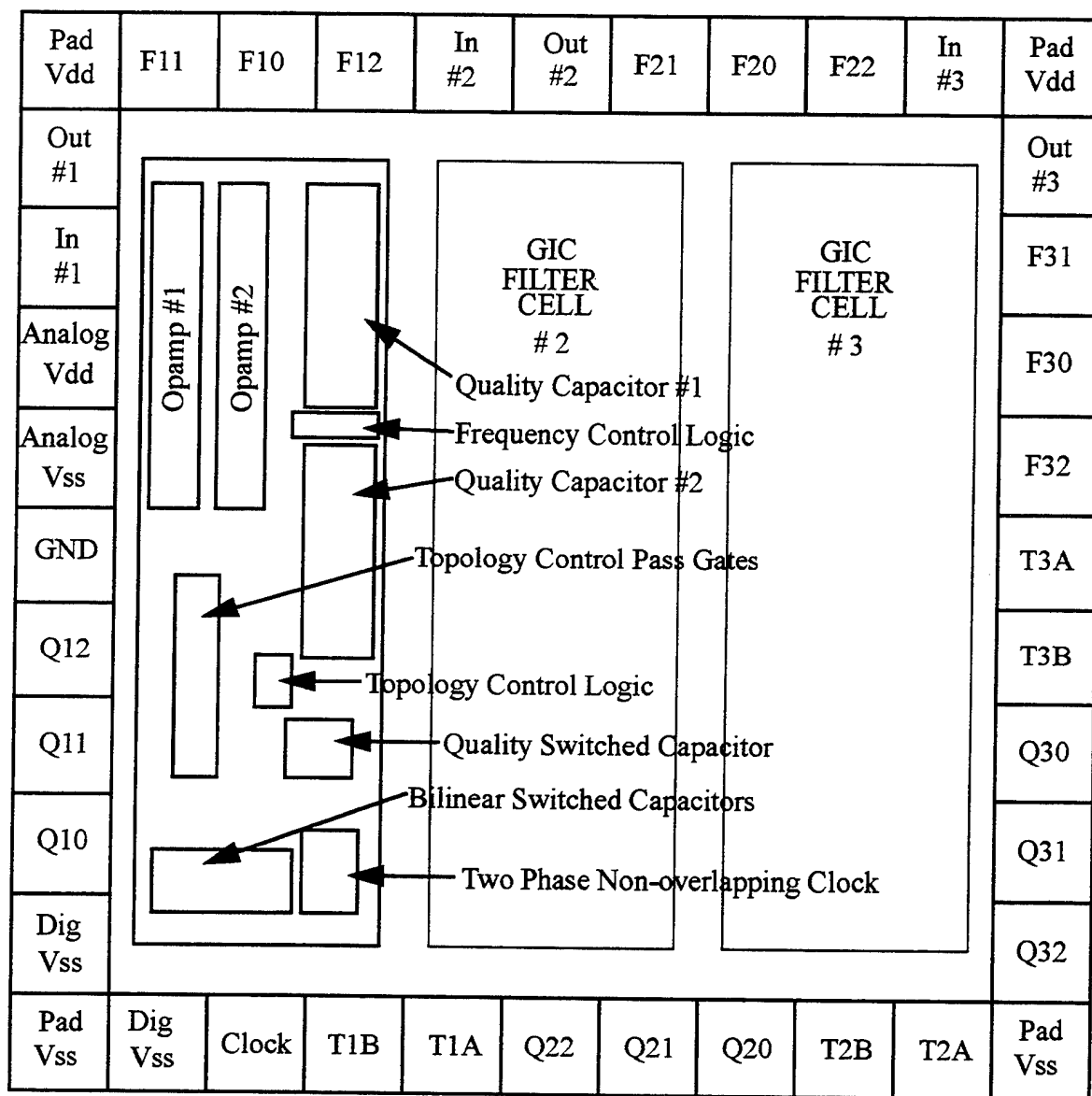


Figure 5.7: Floor Plan of a Three Stage Programmable GIC Filter

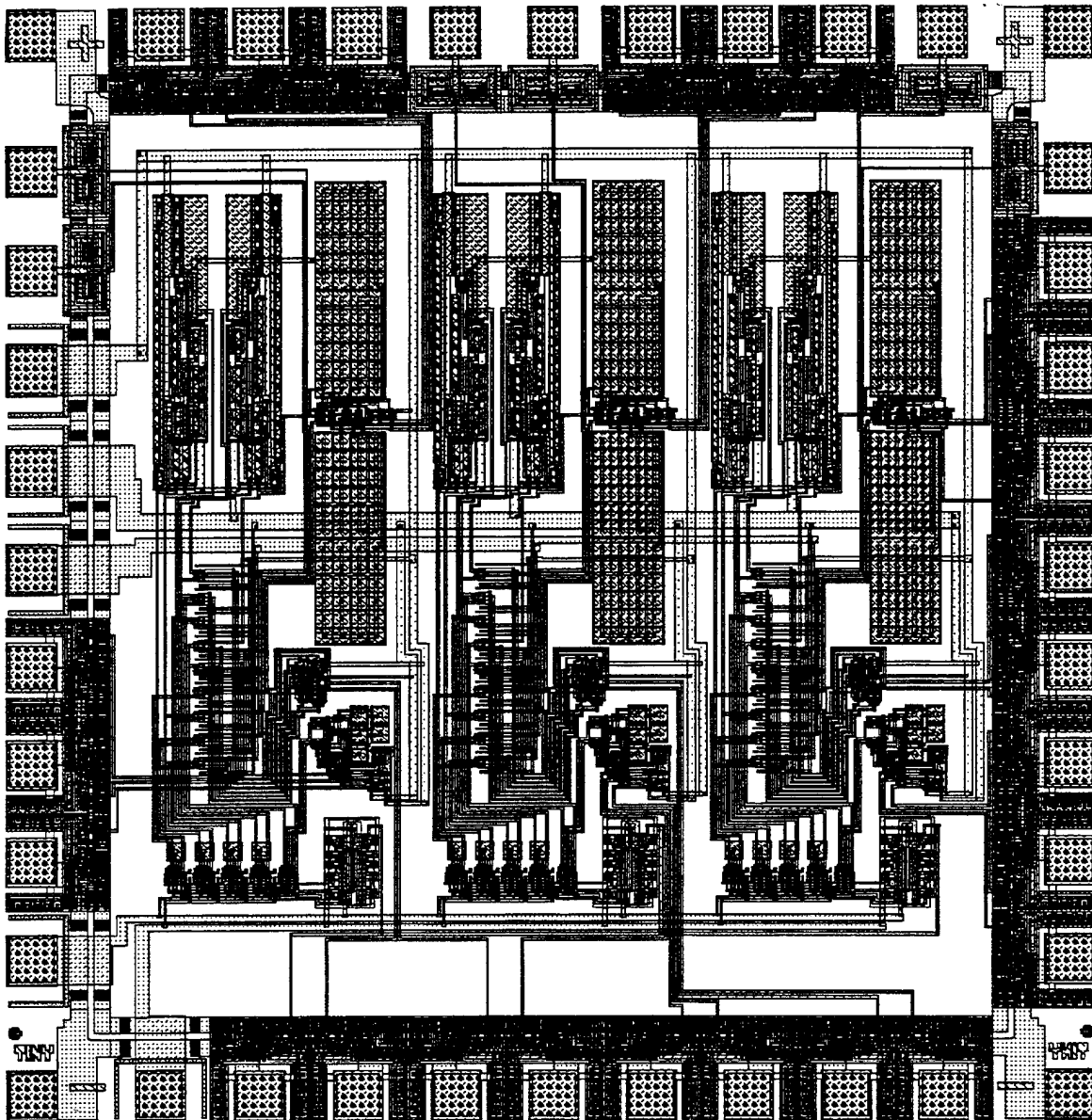


Figure 5.8: VLSI Layout of Three Stage Programmable GIC Filter

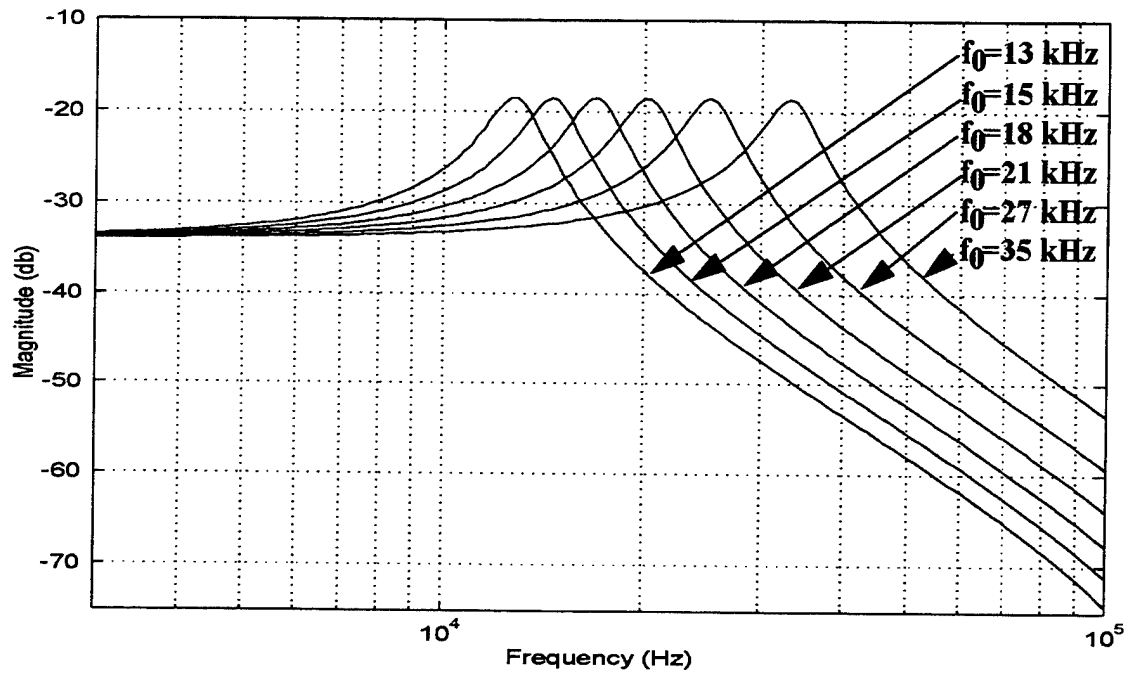


Figure 5.9: The Ideal Lowpass Filter Simulation for Varying f_0

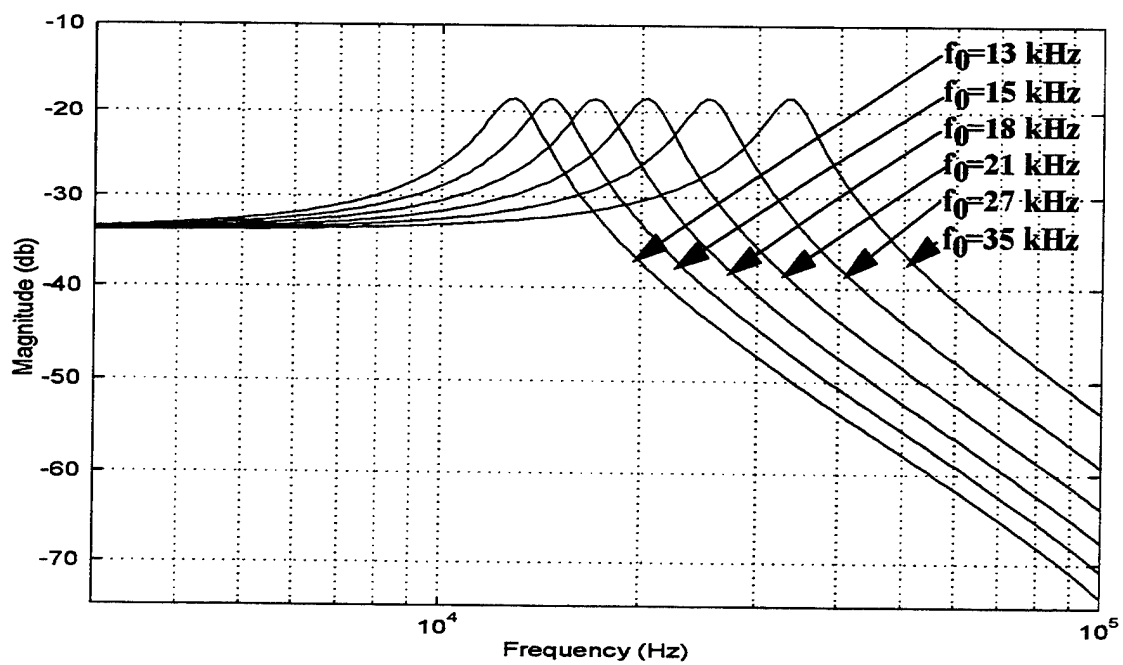


Figure 5.10: The Extracted Lowpass Filter Simulation for Varying f_0

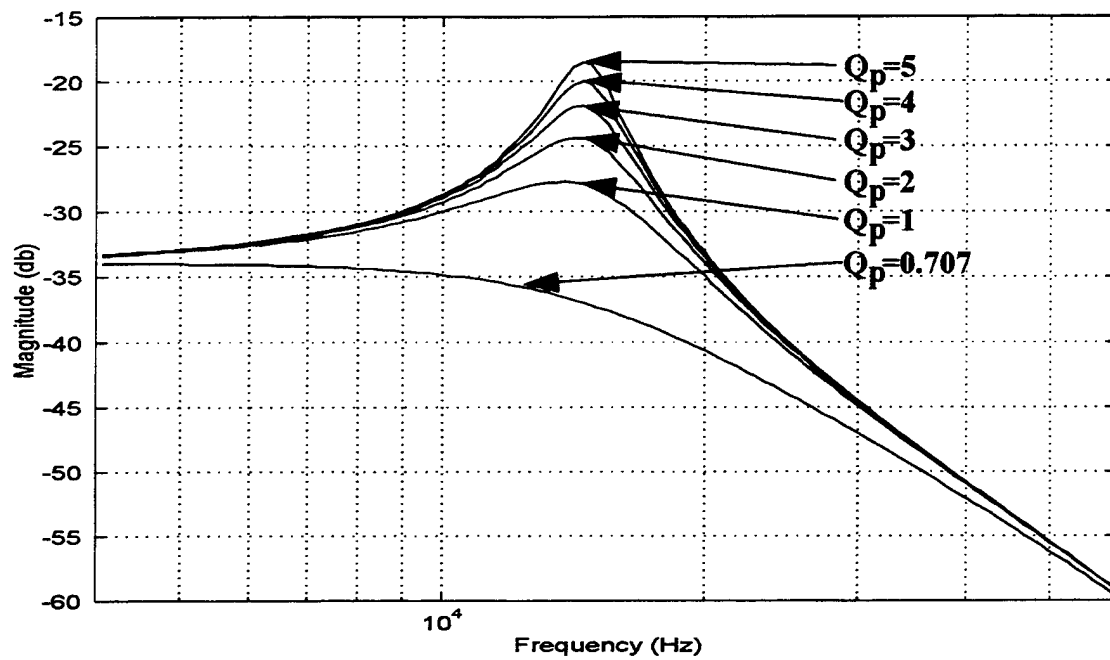


Figure 5.11: The Ideal Lowpass Filter Simulation for Varying Q_p

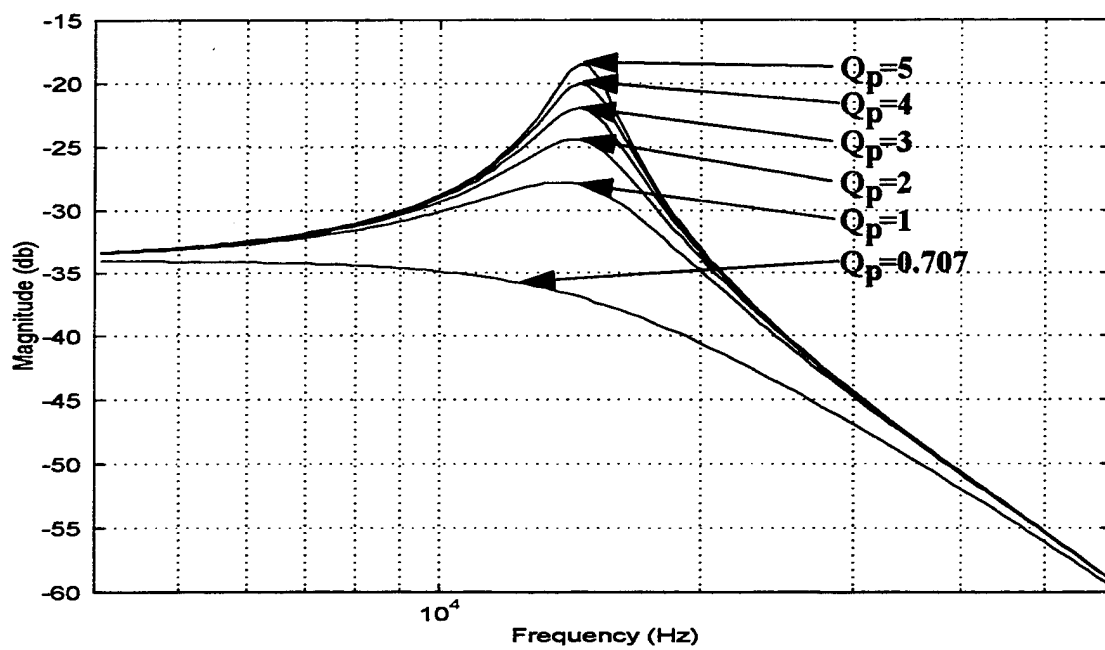


Figure 5.12: The Extracted Lowpass Filter Simulation for Varying Q_p

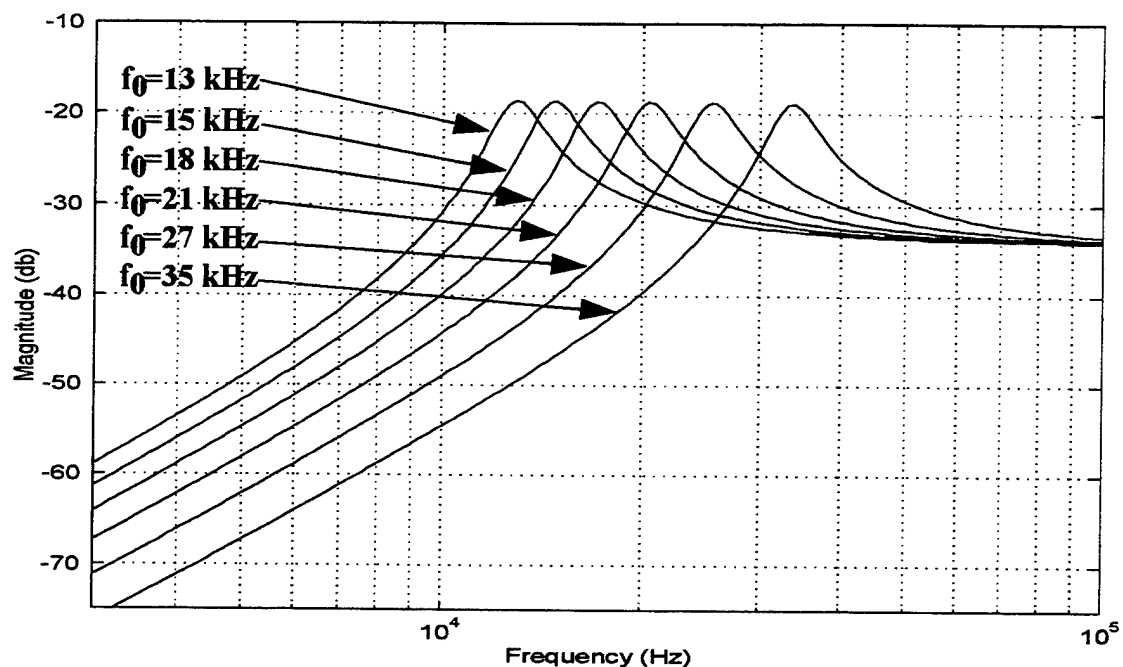


Figure 5.13: The Ideal Highpass Filter Simulation for Varying f_0

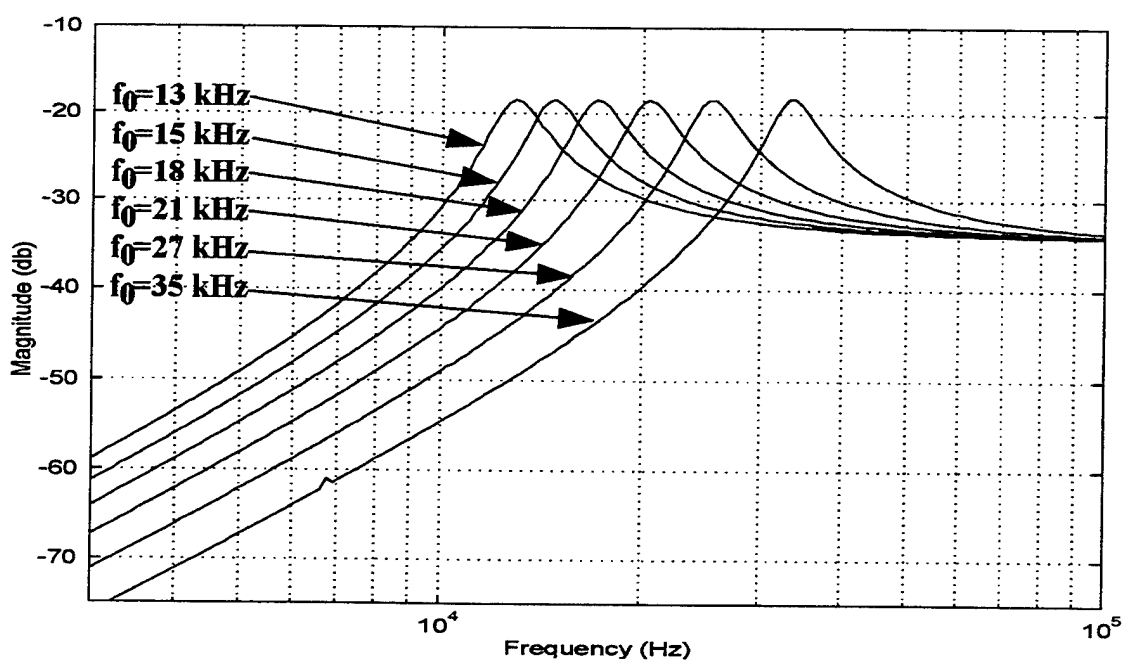


Figure 5.14: The Extracted Highpass Filter Simulation for Varying f_0

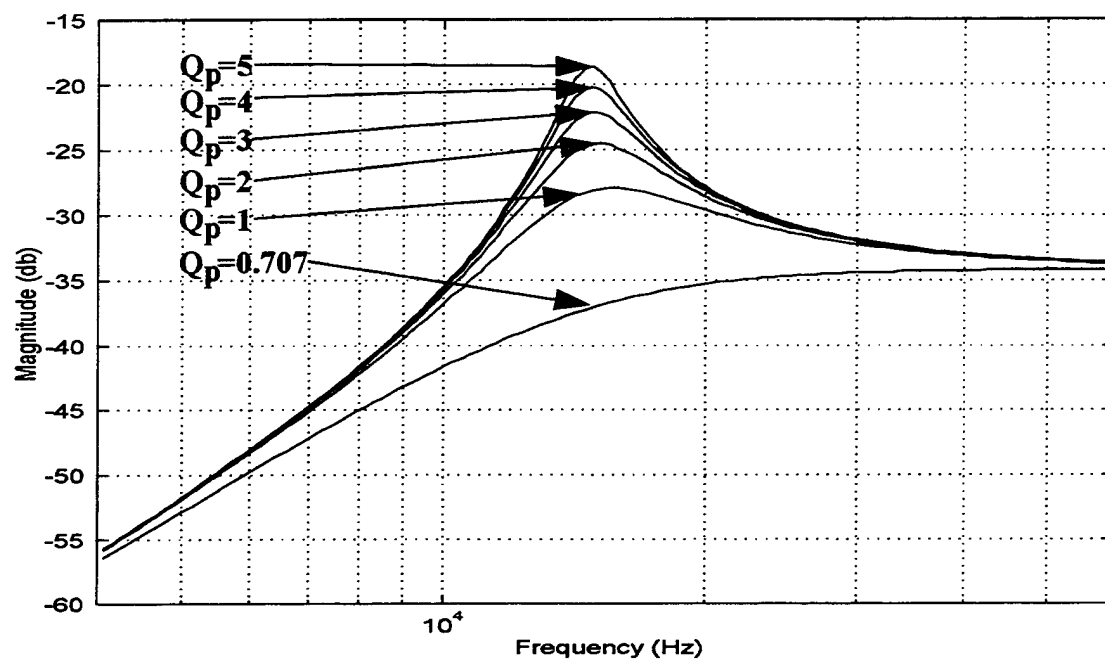


Figure 5.15: The Ideal Highpass Filter Simulation for Varying Q_p

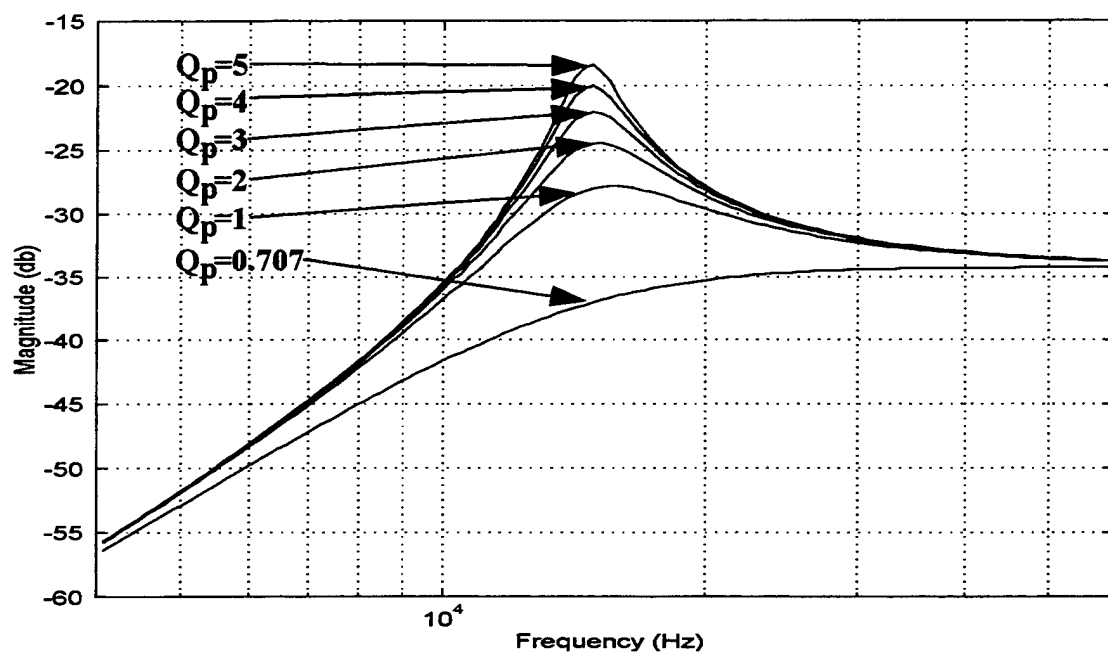


Figure 5.16: The Extracted Highpass Filter Simulation for Varying Q_p

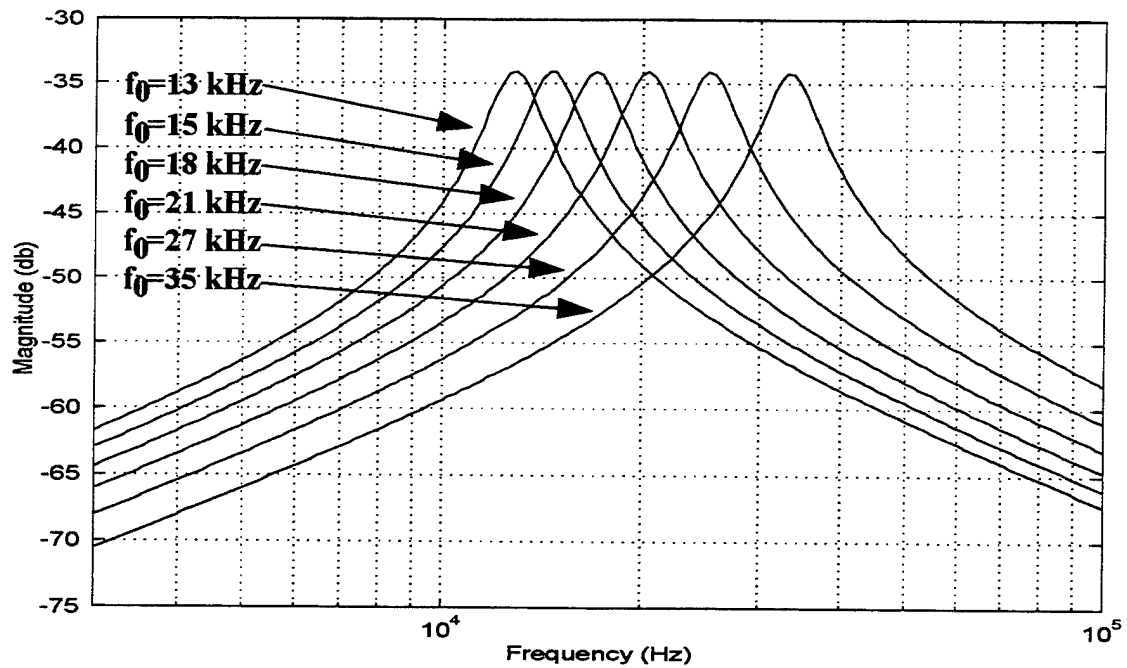


Figure 5.17: The Ideal Bandpass Filter Simulation for Varying f_0

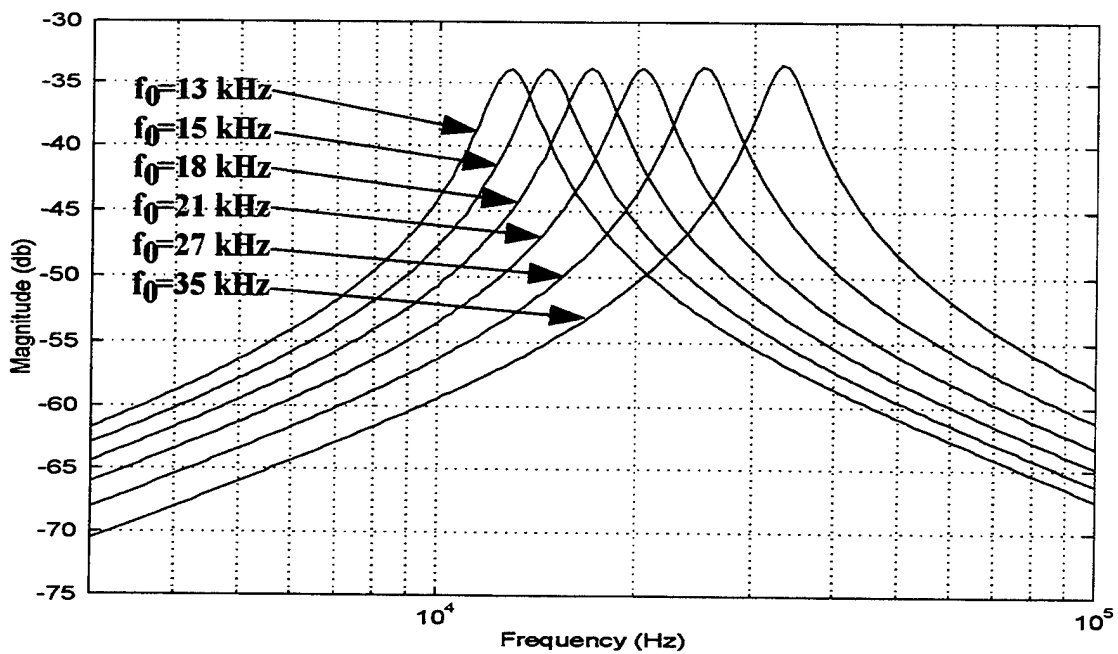


Figure 5.18: The Extracted Bandpass Filter Simulation for Varying f_0

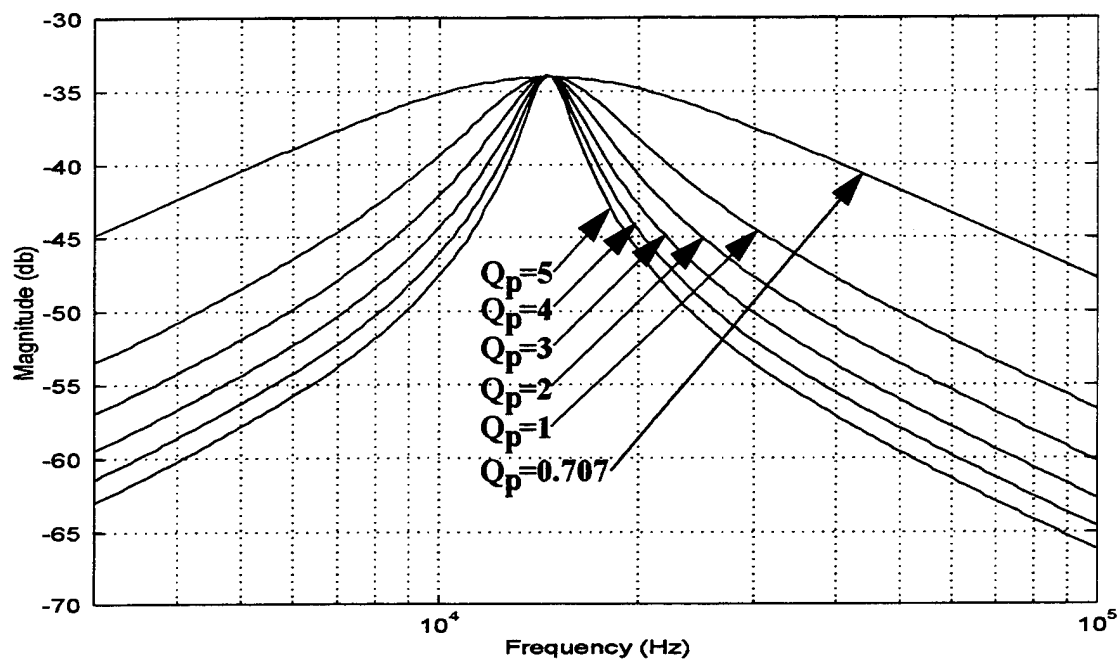


Figure 5.19: The Ideal Bandpass Filter Simulation for Varying Q_p

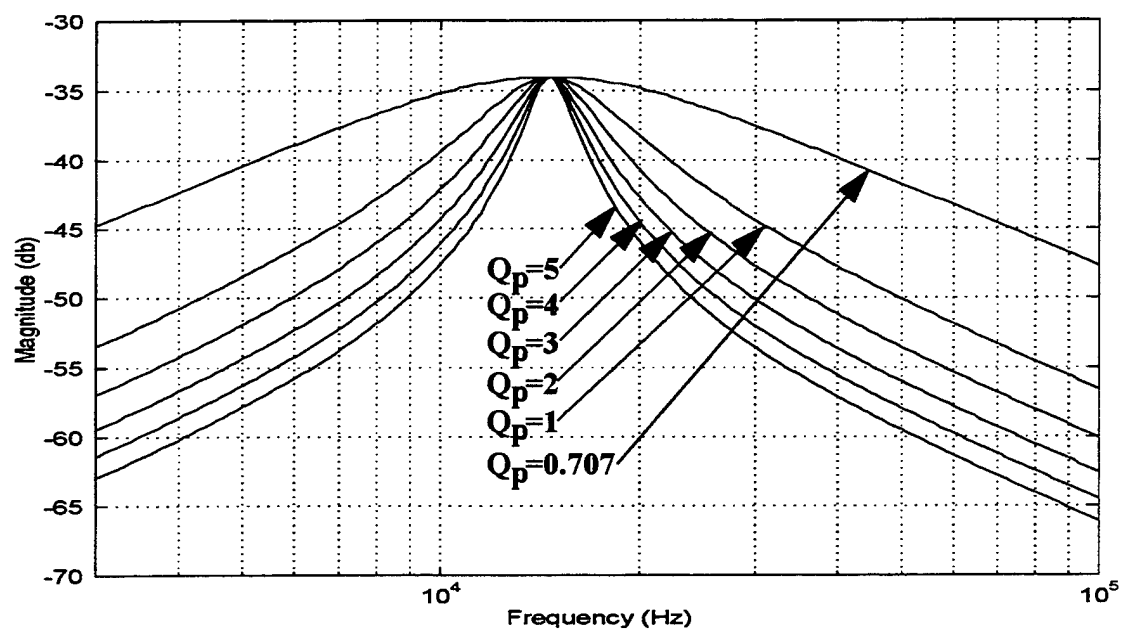


Figure 5.20: The Extracted Bandpass Filter Simulation for Varying Q_p

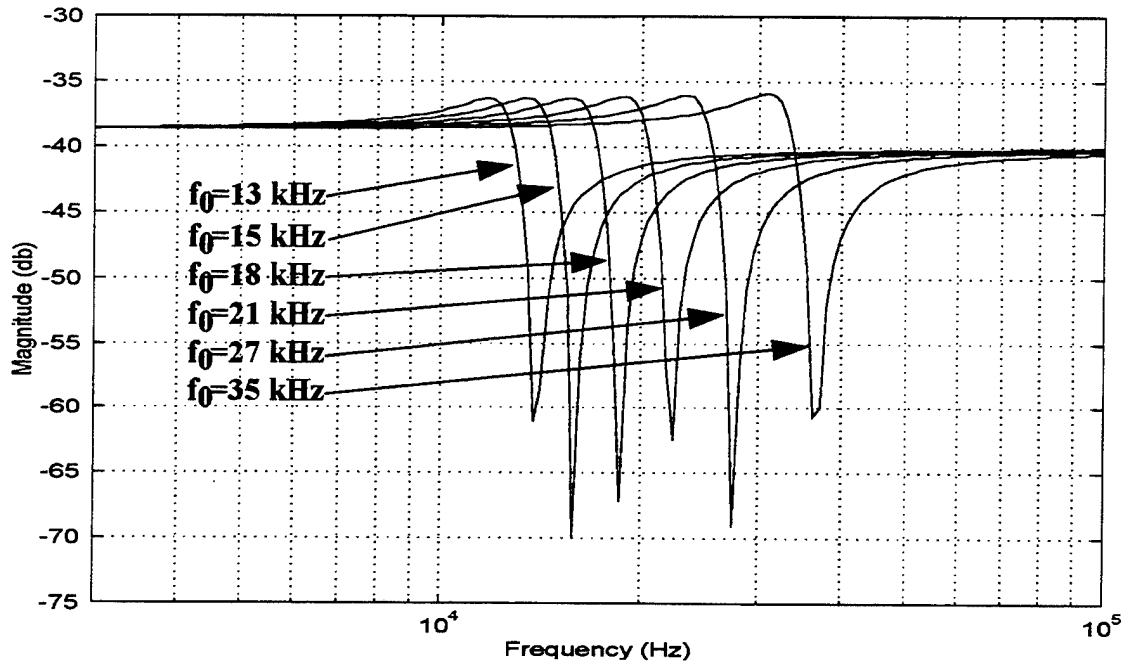


Figure 5.21: The Ideal Notch Filter Simulation for Varying f_0

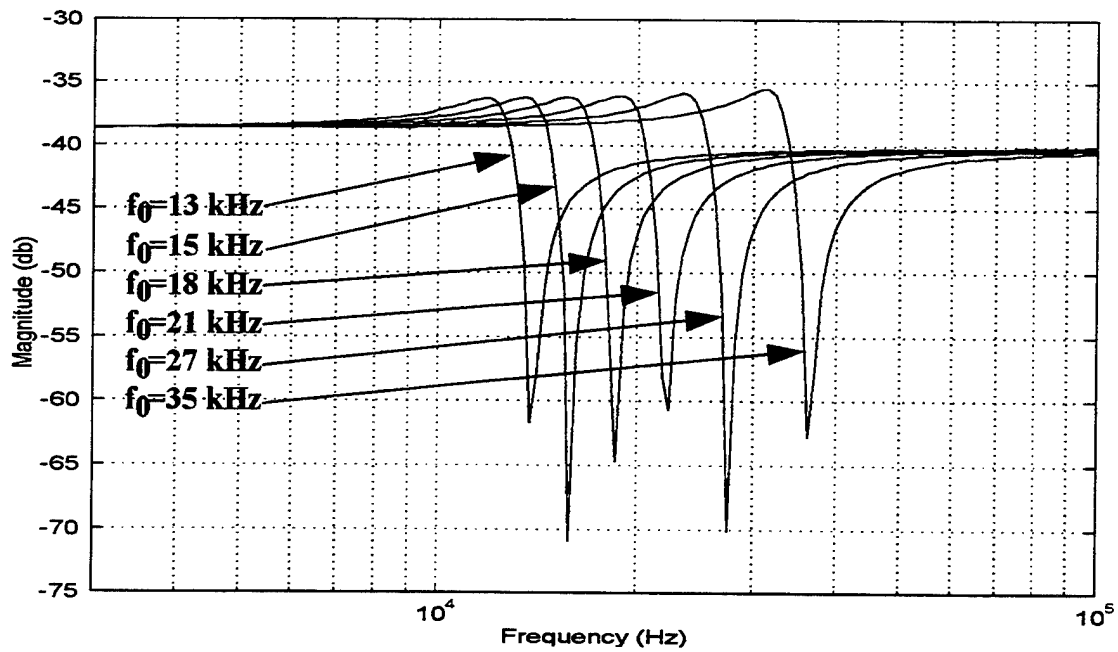


Figure 5.22: The Extracted Notch Filter Simulation for Varying f_0

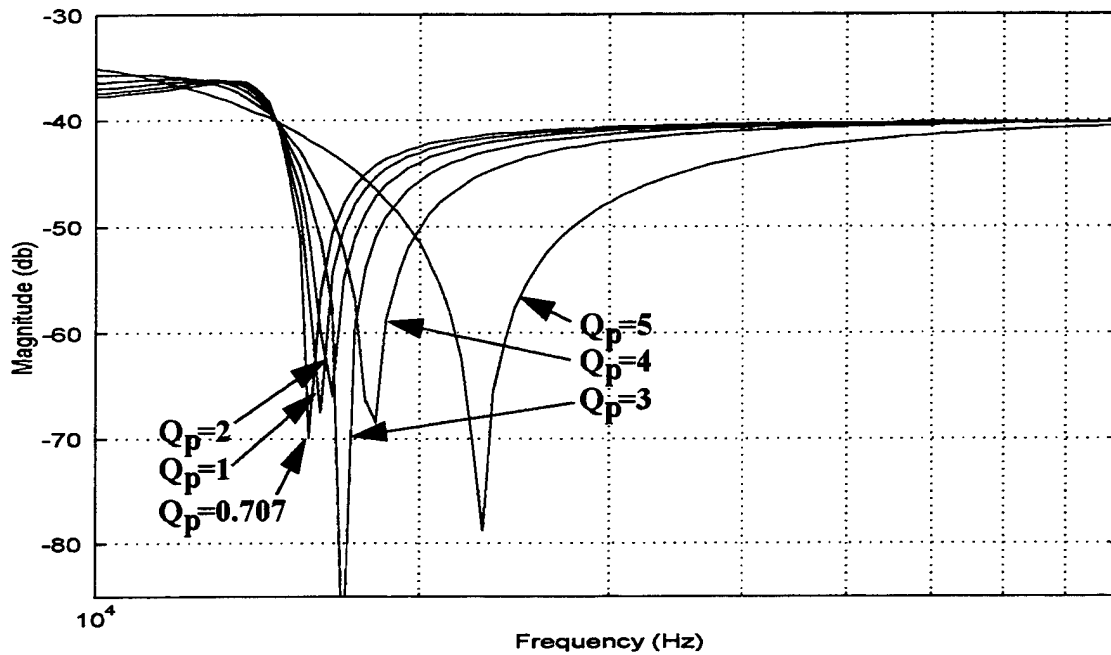


Figure 5.23: The Ideal Notch Filter Simulation for Varying Q_p

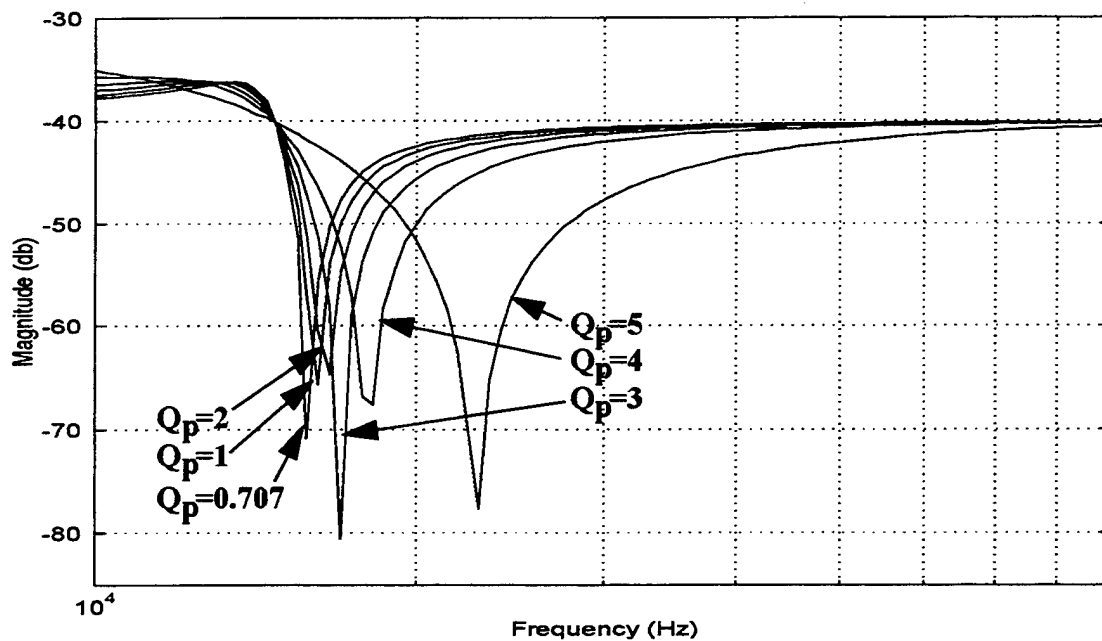


Figure 5.24: The Extracted Notch Filter Simulation for Varying Q_p

VI. RECOMENDATIONS AND CONCLUSION

The goal of this research is the very large scale integration of a digitally programmable, three stage Generalized Immittance Converter filter. The application of this device would be beneficial in areas such as signal processing, neural networks, controls and communications. Stray capacitance is one of the primary parasitic design considerations facing the analog integrated circuit designer. The testing of these GIC filters will help gain insight into the use of bilinear switched capacitors, and their response to stray capacitance in filter integration. The problem of bandwidth limitations of GIC filters, caused by sensitivity to non-ideal components, will also be enlightened by the testing of these microchips.

Four identical microchips will be manufactured in July of 1995 through MOSIS. The testing of these chips should first check for proper operation of the power and ground pins. The chip should not initially be powered by a voltage higher than plus or minus five volts. On initial testing, the power supply voltage should be gradually increased in small increments while observing current flow. If there is a rapid increase in current flow, latchup could be occurring and the voltages must be decreased to prevent chip destruction. The switched capacitor filters should be driven with a clock frequency no higher than one megahertz. The primary testing points for the filters are the proper operation of the bilinear switched capacitor networks, the proper amplitude response, the proper frequency tunability and the proper pole quality selectability. Poor amplitude response or frequency tunability could be an indication of large parasitic poles and an increase in the component capacitances would be necessitated in a follow on chip.

The use of CAD tools such as Cadence would provide better extracted simulation data than MAGIC. MAGIC CAD tool was initially designed to construct digital circuits and the capacitances associated with large analog devices are not properly addressed in the translation. Cadence also has SWITCAP2, a switched capacitor simulation package. SPICE will not converge when presented with the high, square wave frequencies present in

a switched capacitor network, so extracted switched capacitors must be replaced with resistors unless a specific switched capacitor simulation tool such as SWITCAP2 is used.

The operational amplifier used provided sufficient bandwidth and offset voltage performance to test the concept of this design, but the network performance could be drastically increased with a higher quality device. Local work in pseudo-BiCMOS and composites should yield some good performing operational amplifiers.

The use of Gallium Arsenide to implement a switched capacitor network has many advantages. Gallium arsenide has higher electron mobility than silicon and can therefore operate at much higher clock speeds. Higher clock speeds would allow this filter design to have much wider bandwidth. Gallium arsenide also has radiation tolerance which is essential for spaceborne applications.

The design of this device is the initial step in the development of a monolithic analog device capable of handling a wide range of frequencies with minimal unwanted signal distortion. The GIC filter is a good basis for this design and with improvements in parasitic capacitance and operational amplifier qualities, the development of a design for cost effective mass production is not beyond reach.

APPENDIX A. PSPICE CODE FOR CIRCUIT SIMULATIONS

A. PSPICE SIMULATION FILE FOR SILVERNAGLE OPERATIONAL AMPLIFIER

```
** Opamp sub-circuit extracted from cmosopamp2
** Technology: scmos
** .MODEL ecap CAP CJ=4.59E-4 CJSW=2E-10
```

```
.SUBCKT OPAMPEXT 110 111 101
```

```
.MODEL nfet NMOS LEVEL=2 PHI=0.600000 TOX=4.2000E-08 XJ=0.200000U
TPG=1
```

```
+ VTO=0.8410 DELTA=6.0220E+00 LD=7.3030E-08 KP=4.6856E-05
+ UO=569.9 UEXP=2.2470E-01 UCRIT=8.3850E+04 RSH=2.0000E+01
+ GAMMA=0.4977 NSUB=5.0450E+15 NFS=1.980E+11 VMAX=6.6330E+04
+ LAMBDA=3.1750E-02 CGDO=9.0065E-11 CGSO=9.0065E-11
+ CGBO=4.8051E-10 CJ=9.1203E-05 MJ=0.7451 CJSW=2.4684E-10
+ MJSW=0.068631 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -8.4220E-07
```

```
.MODEL pfet PMOS LEVEL=2 PHI=0.600000 TOX=4.2000E-08 XJ=0.200000U
TPG=-1
```

```
+ VTO=-0.9297 DELTA=3.8240E00 LD=3.3390E-07 KP=1.6994E-05
+ UO=206.7 UEXP=2.6190E-01 UCRIT=8.6610E+04 RSH=5.7120E+01
+ GAMMA=0.7262 NSUB=1.0740E+16 NFS=3.270E+11 VMAX=9.9990E+05
+ LAMBDA=4.4380E-02 CGDO=4.1179E-10 CGSO=4.1179E-10
+ CGBO=3.6700E-10 CJ=3.1278E-04 MJ=0.5709 CJSW=3.4621E-10
+ MJSW=0.294506 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -1.3512E-07
```

```
** M0 100 101 100 0 ecap L=29.0U W=392.0U
CCOMP 100 101 6.89P
M1 101 103 102 102 pfet L=10.0U W=164.0U
M2 104 104 102 102 pfet L=10.0U W=60.0U
M3 103 105 100 102 pfet L=10.0U W=10.0U
M4 101 106 105 105 nfet L=9.0U W=50.0U
M5 106 107 105 105 nfet L=10.0U W=71.0U
M6 106 103 102 106 nfet L=176.0U W=10.0U
M7 108 107 105 105 nfet L=10.0U W=53.0U
M8 103 109 102 102 pfet L=10.0U W=60.0U
```

```

M9 109 109 102 102 pfet L=10.0U W=60.0U
M10 103 110 108 108 nfet L=10.0U W=66.0U
M11 109 111 108 108 nfet L=10.0U W=66.0U
M12 104 104 107 107 nfet L=460.0U W=10.0U
M13 107 107 105 105 nfet L=10.0U W=27.0U

```

```

C0 101 105 12F
C1 105 0 375F
** NODE: 105 = Vss
** NODE: 111 = Vin-
** NODE: 110 = Vin+
C2 109 0 259F
** NODE: 109 = 8_10_24#
C3 108 0 235F
** NODE: 108 = 8_45_30#
C4 107 0 118F
** NODE: 107 = 8_65_26#
C5 106 0 192F
** NODE: 106 = 8_63_340#
C6 102 0 657F
** NODE: 102 = Vdd
C7 101 0 954F
** NODE: 101 = 8_99_492#
C8 100 0 119F
** NODE: 100 = 8_103_488#
C9 104 0 436F
** NODE: 104 = 8_80_83#
C10 103 0 381F
** NODE: 103 = 8_33_141#
** NODE: 0 = GND!

```

```

Vplus 102 0 DC 5
Vminus 0 105 DC 5

```

```

.ENDS OPAMPEXT

```

```

XOP 1000 1001 1001 OPAMPEXT
VAC 1000 0 SIN(0 500MV 10KHZ)

```

```

.TRAN .001US 0.5MS 0 1US
.PROBE
.END

```

B. PSPICE FILE FOR LOWPASS GIC FILTER

***High pass GIC filter using extracted operational amplifier subcircuit

**#1

XOP01 05 04 02 OPAMPEXT

XOP02 03 04 01 OPAMPEXT

RY01 01 04 3061K

RY02 01 05 3061K

CY03 02 04 4p

RY04 02 03 3061K

RY06 05 0 3061K

RY07 0 03 18366K

CY08 03 06 4p

**#2

XOP11 15 14 12 OPAMPEXT

XOP12 13 14 11 OPAMPEXT

RY11 11 14 3061K

RY12 11 15 3061K

CY13 12 14 3.5p

RY14 12 13 3061K

RY16 15 0 3061K

RY17 0 13 18366K

CY18 13 16 3.5p

**#3

XOP21 25 24 22 OPAMPEXT

XOP22 23 24 21 OPAMPEXT

RY21 21 24 3061K

RY22 21 25 3061K

CY23 22 24 3p

RY24 22 23 3061K

RY26 25 0 3061K

RY27 0 23 18366K

CY28 23 26 3p

**#4

XOP31 35 34 32 OPAMPEXT

XOP32 33 34 31 OPAMPEXT

RY31 31 34 3061K

RY32 31 35 3061K

CY33 32 34 2.5p

RY34 32 33 3061K

RY36 35 0 3061K

RY37 0 33 18366K

CY38 33 36 2.5p

**#5

XOP41 45 44 42 OPAMPEXT

XOP42 43 44 41 OPAMPEXT

RY41 41 44 3061K

RY42 41 45 3061K

CY43 42 44 2p

RY44 42 43 3061K

RY46 45 0 3061k

RY47 0 43 18366K

CY48 43 46 2p

**#6

XOP51 55 54 52 OPAMPEXT

XOP52 53 54 51 OPAMPEXT

RY51 51 54 3061K

RY52 51 55 3061K

CY53 52 54 1.5p

RY54 52 53 3061K

RY56 55 0 3061K

RY57 0 53 18366K

CY58 53 56 1.5p

VAC0 06 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC1 16 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC2 26 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC3 36 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC4 46 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC5 56 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

** .TRAN .001US 0.5MS 0 1US

.AC DEC 100 1000 500K

.OPTIONS NUMDGT=3 WIDTH=132

.PROBE

.print ac vdb(01) vdb(11) vdb(21) vdb(31) vdb(41) vdb(51)

.END

C. PSPICE FILE FOR BANDPASS GIC FILTER

*** Band pass GIC filter using extracted operational amplifier subcircuit

***#1

XOP01 05 04 02 OPAMPEXT

XOP02 03 04 01 OPAMPEXT

RY01 01 04 3061K

RY02 01 05 3061K

CY03 02 04 4p

RY04 02 03 3061K

RY06 05 0 3061K

RY07 06 03 18366K

CY08 03 0 4p

***#2

XOP11 15 14 12 OPAMPEXT

XOP12 13 14 11 OPAMPEXT

RY11 11 14 3061K

RY12 11 15 3061K

CY13 12 14 3.5p

RY14 12 13 3061K

RY16 15 0 3061K

RY17 16 13 18366K

CY18 13 0 3.5p

***#3

XOP21 25 24 22 OPAMPEXT

XOP22 23 24 21 OPAMPEXT

RY21 21 24 3061K

RY22 21 25 3061K

CY23 22 24 3p

RY24 22 23 3061K

RY26 25 0 3061K

RY27 26 23 18366K

CY28 23 0 3p

***#4

XOP31 35 34 32 OPAMPEXT

XOP32 33 34 31 OPAMPEXT

RY31 31 34 3061K

RY32 31 35 3061K

CY33 32 34 2.5p

RY34 32 33 3061K

RY36 35 0 3061K

RY37 36 33 18366K

CY38 33 0 2.5p

```

**#5
XOP41 45 44 42 OPAMPEXT
XOP42 43 44 41 OPAMPEXT
RY41 41 44 3061K
RY42 41 45 3061K
CY43 42 44 2p
RY44 42 43 3061K
RY46 45 0 3061k
RY47 46 43 18366K
CY48 43 0 2p
**#6
XOP51 55 54 52 OPAMPEXT
XOP52 53 54 51 OPAMPEXT
RY51 51 54 3061K
RY52 51 55 3061K
CY53 52 54 1.5p
RY54 52 53 3061K
RY56 55 0 3061K
RY57 56 53 18366K
CY58 53 0 1.5p

VAC0 06 0 DC 0 AC 10MV
+SIN 0 1M 1K 0 0 0
VAC1 16 0 DC 0 AC 10MV
+SIN 0 1M 1K 0 0 0
VAC2 26 0 DC 0 AC 10MV
+SIN 0 1M 1K 0 0 0
VAC3 36 0 DC 0 AC 10MV
+SIN 0 1M 1K 0 0 0
VAC4 46 0 DC 0 AC 10MV
+SIN 0 1M 1K 0 0 0
VAC5 56 0 DC 0 AC 10MV
+SIN 0 1M 1K 0 0 0

** .TRAN .001US 0.5MS 0 1US

.AC DEC 100 1000 500K
.OPTIONS NUMDGT=3 WIDTH=132
.PROBE
.print ac vdb(01) vdb(11) vdb(21) vdb(31) vdb(41) vdb(51)

.END

```


D. PSPICE FILE FOR NOTCH GIC FILTER

*** Notch GIC filter using extracted operational amplifier subcircuit

**#1

XOP01 05 04 02 OPAMPEXT
XOP02 03 04 01 OPAMPEXT
RY01 01 04 3061K
RY02 01 05 3061K
CY03 02 04 4p
RY04 02 03 3061K
RY06 05 06 3061K
RY07 0 03 18366K
CY08 03 06 4p

**#2

XOP11 15 14 12 OPAMPEXT
XOP12 13 14 11 OPAMPEXT
RY11 11 14 3061K
RY12 11 15 3061K
CY13 12 14 3.5p
RY14 12 13 3061K
RY16 15 16 3061K
RY17 0 13 18366K
CY18 13 16 3.5p

**#3

XOP21 25 24 22 OPAMPEXT
XOP22 23 24 21 OPAMPEXT
RY21 21 24 3061K
RY22 21 25 3061K
CY23 22 24 3p
RY24 22 23 3061K
RY26 25 26 3061K
RY27 0 23 18366K
CY28 23 26 3p

**#4

XOP31 35 34 32 OPAMPEXT
XOP32 33 34 31 OPAMPEXT
RY31 31 34 3061K
RY32 31 35 3061K
CY33 32 34 2.5p
RY34 32 33 3061K
RY36 35 36 3061K
RY37 0 33 18366K
CY38 33 36 2.5p

**#5

XOP41 45 44 42 OPAMPEXT

XOP42 43 44 41 OPAMPEXT

RY41 41 44 3061K

RY42 41 45 3061K

CY43 42 44 2p

RY44 42 43 3061K

RY46 45 46 3061k

RY47 0 43 18366K

CY48 43 46 2p

**#6

XOP51 55 54 52 OPAMPEXT

XOP52 53 54 51 OPAMPEXT

RY51 51 54 3061K

RY52 51 55 3061K

CY53 52 54 1.5p

RY54 52 53 3061K

RY56 55 56 3061K

RY57 0 53 18366K

CY58 53 56 1.5p

VAC0 06 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC1 16 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC2 26 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC3 36 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC4 46 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

VAC5 56 0 DC 0 AC 10MV

+SIN 0 1M 1K 0 0 0

** .TRAN .001US 0.5MS 0 1US

.AC DEC 100 1000 500K

.OPTIONS NUMDGT=3 WIDTH=132

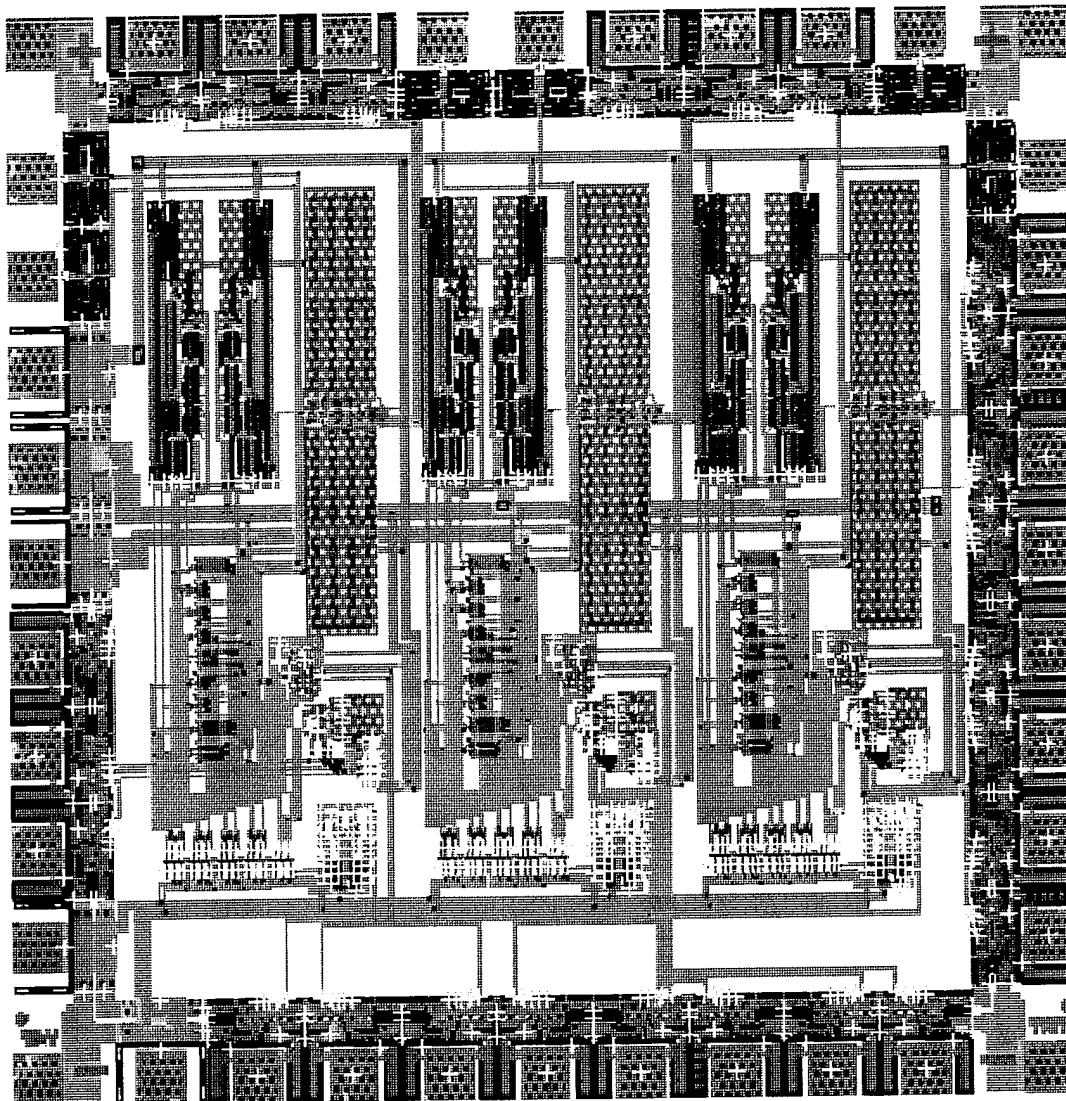
.PROBE

.print ac vdb(02) vdb(12) vdb(22) vdb(32) vdb(42) vdb(52)

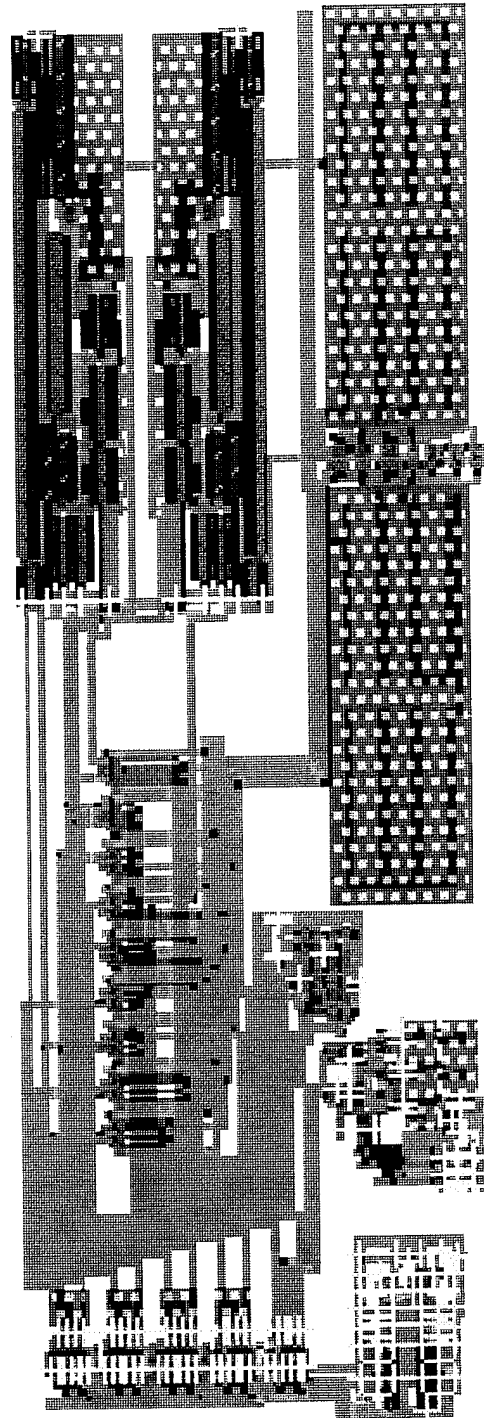
.END

APPENDIX B. VLSI LAYOUTS OF FILTER COMPONENTS

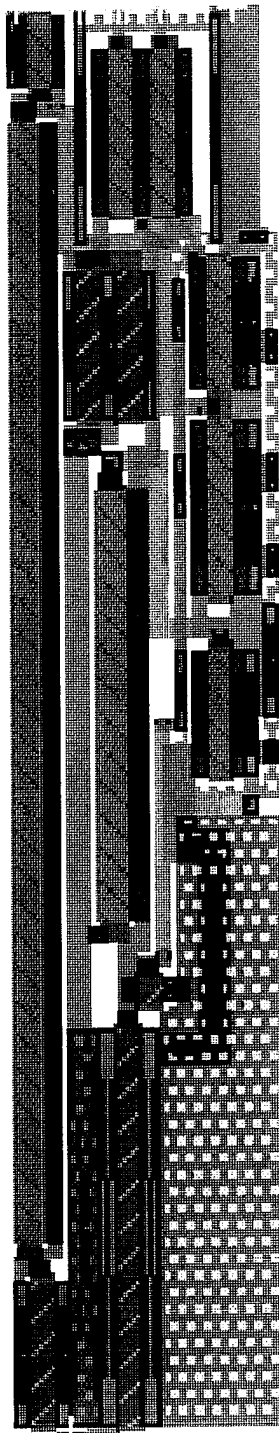
A. INTEGRATED THREE STAGE PROGRAMMABLE GIC FILTER



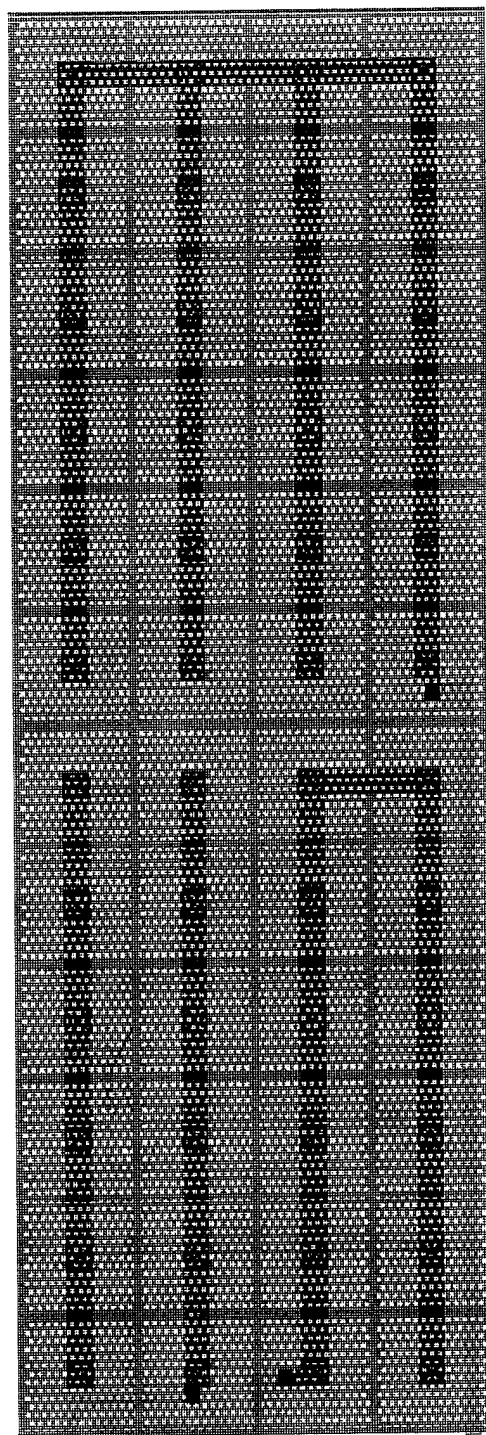
B. SINGLE STAGE GIC FILTER CELL



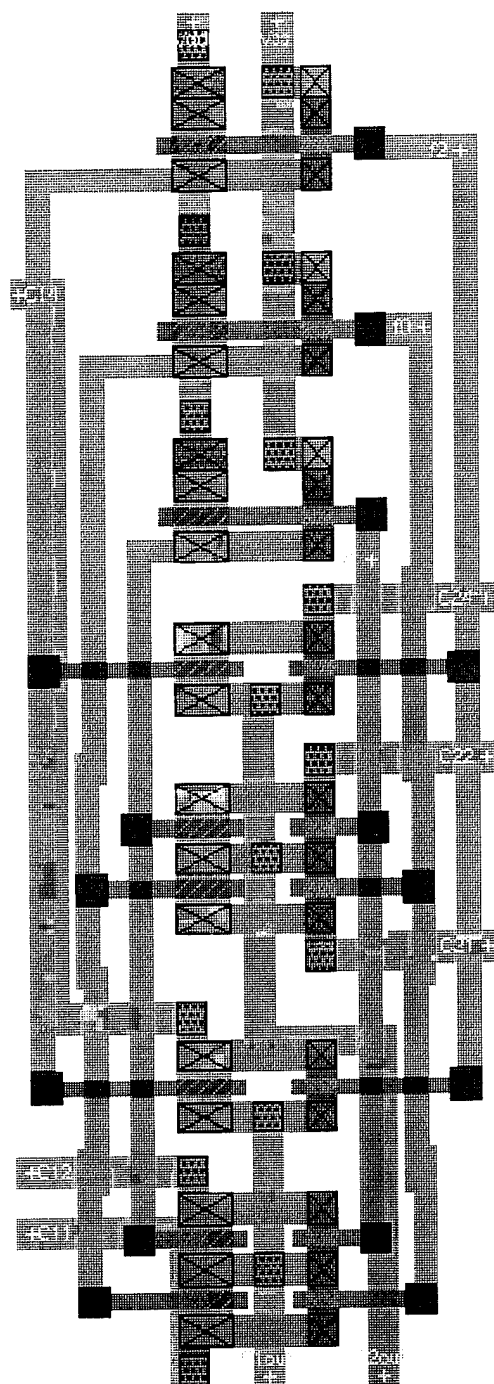
C. SILVERNAGLE OPERATIONAL AMPLIFIER



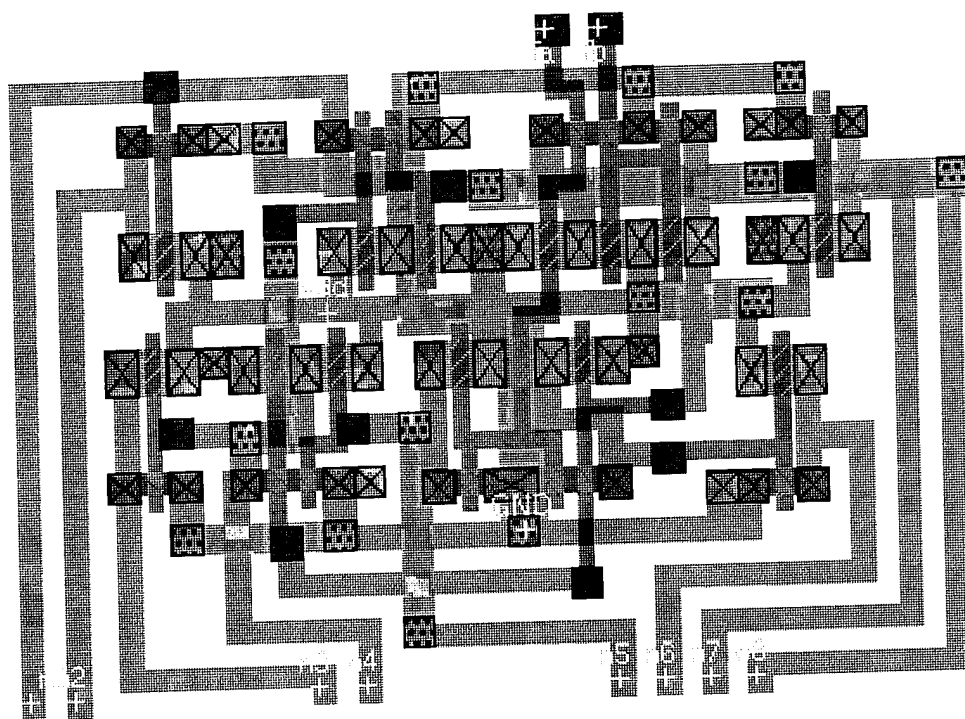
D. FREQUENCY CAPACITOR



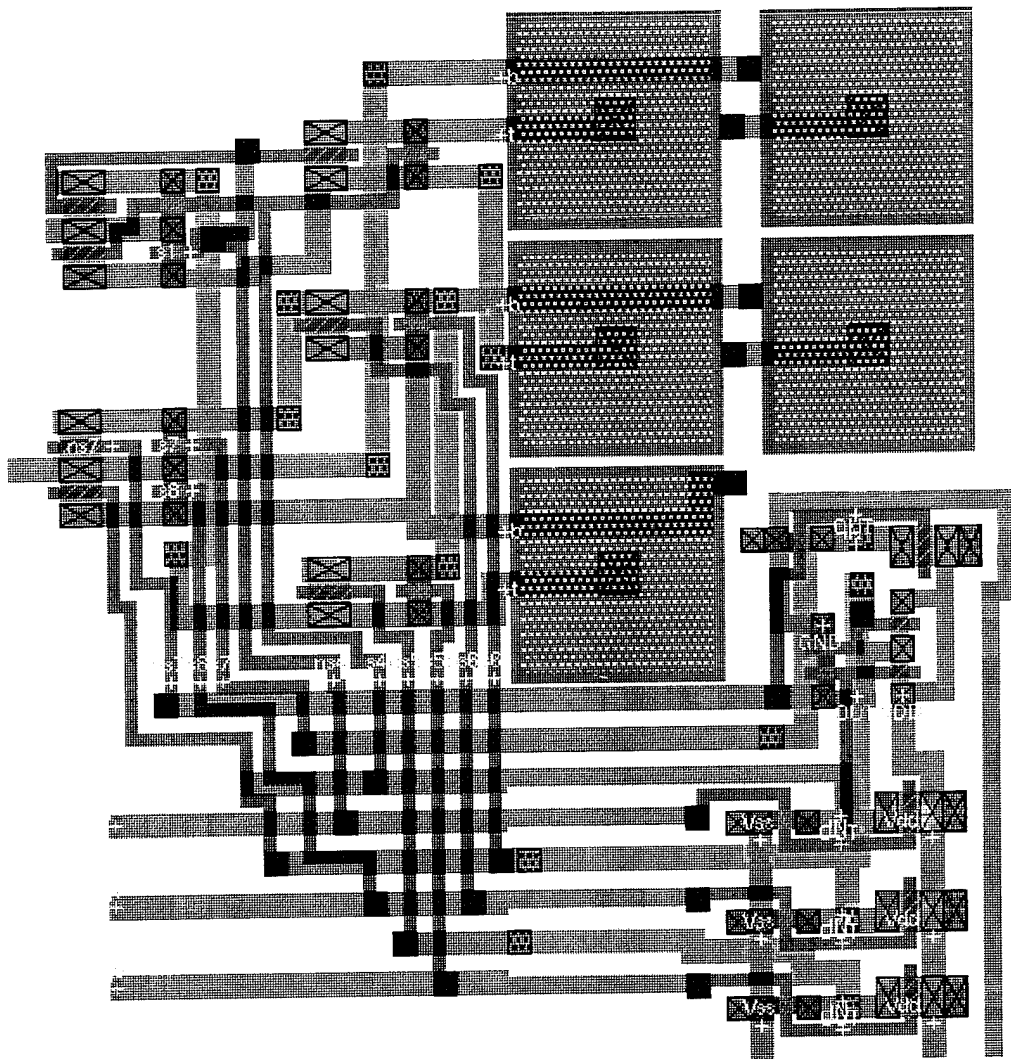
E. FREQUENCY SELECTION LOGIC



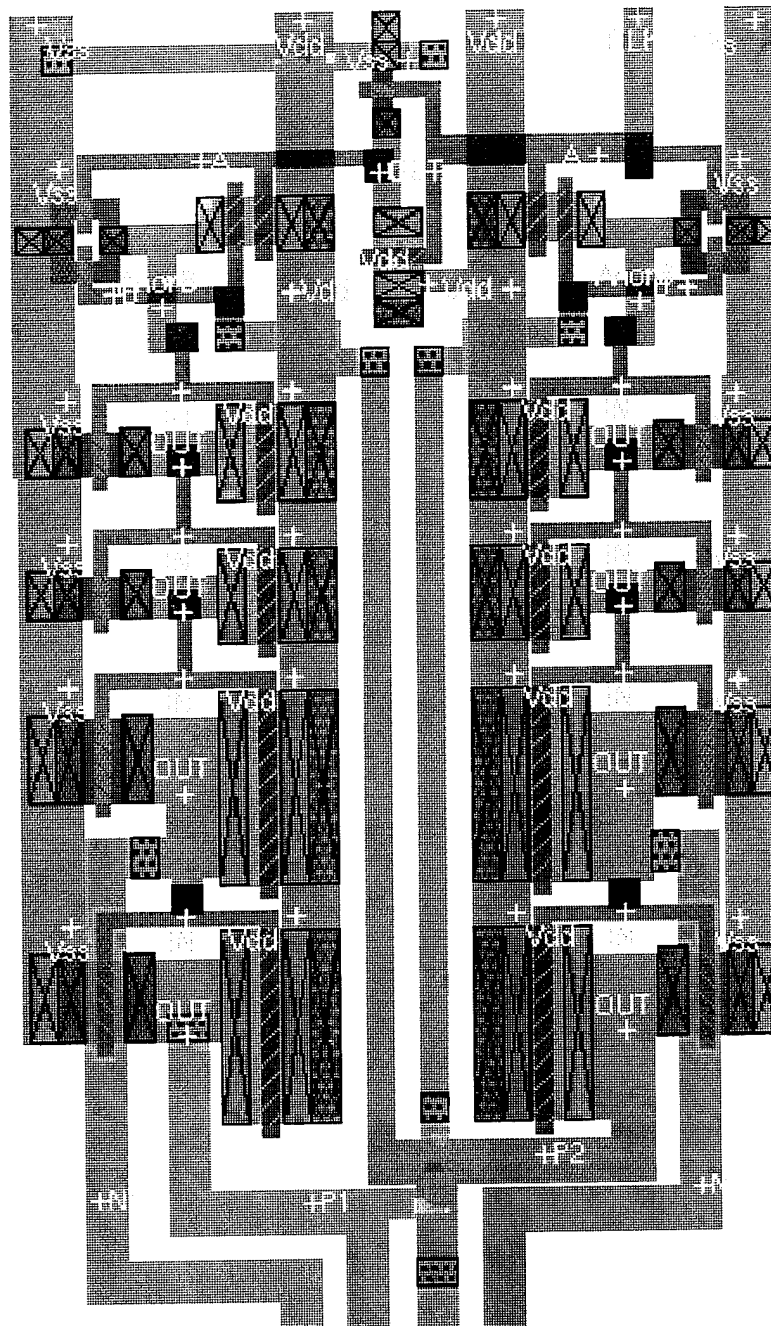
F. TOPOLOGY CONTROL LOGIC



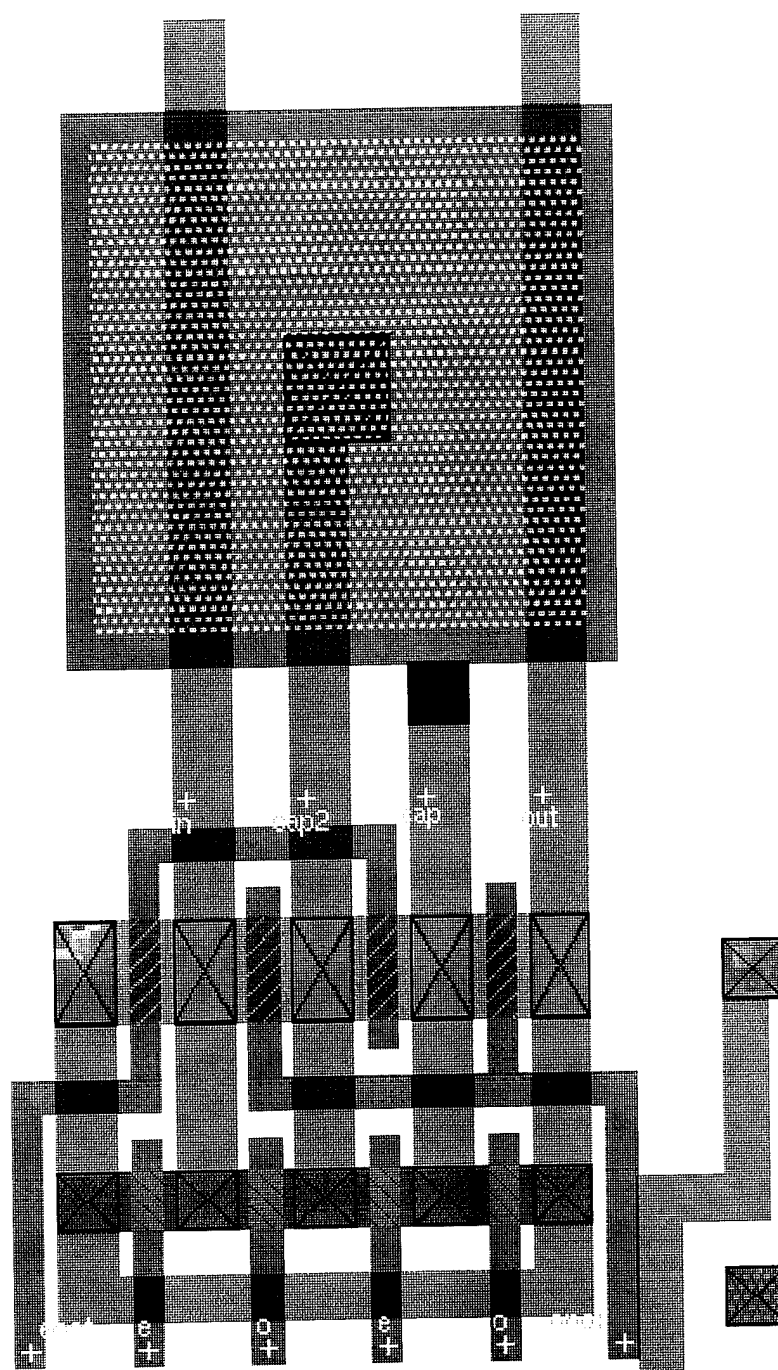
G. QUALITY CAPACITOR AND CONTROL LOGIC



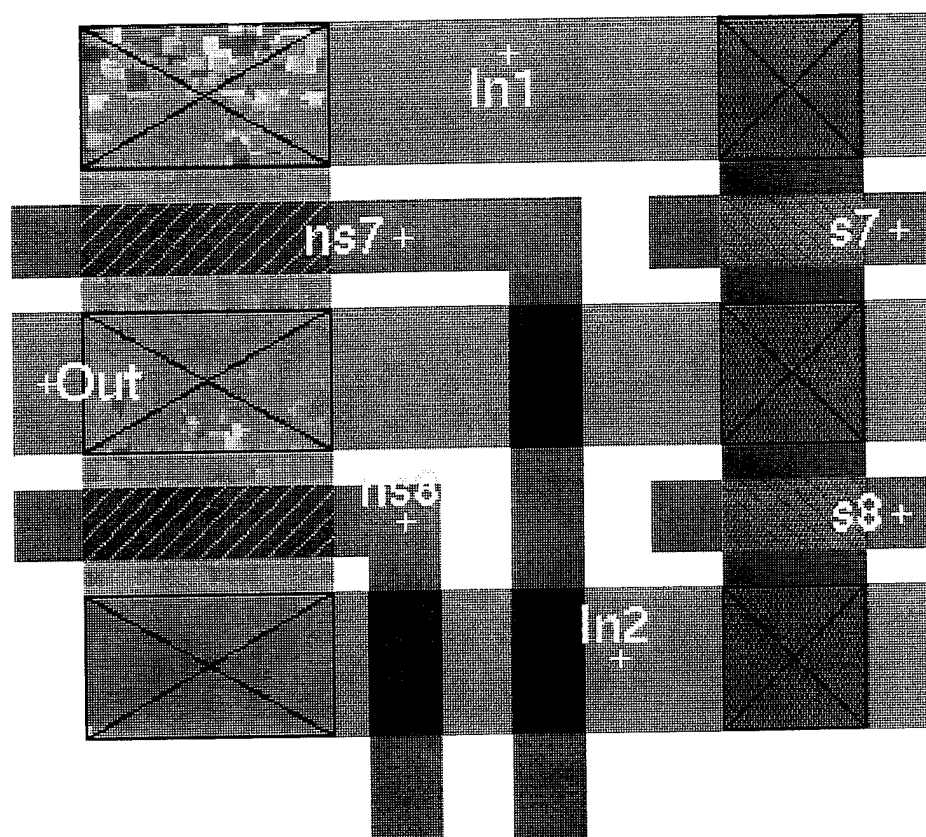
H. TWO PHASE NON-OVERLAPPING CLOCK



I. BILINEAR SWITCHED CAPACITOR RESISTOR



J. PASS GATE



LIST OF REFERENCES

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