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PLASTIC PACKAGE AVAILABILITY (PPA) PROGRAM

National Semiconductor Corp.

Dow Corning Corp.
Honeywell
Naval Surface Warfare Center - Crane
Plaskon Electronic Materials Inc.
Rome Laboratory
Sandia National Laboratories

Final Technical Report for Period October 1992 - November 1995

November 1995

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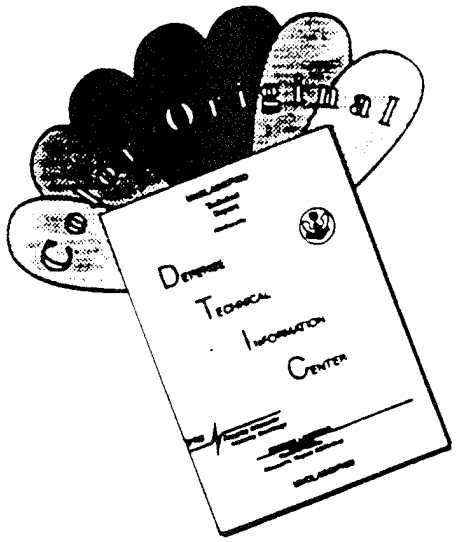
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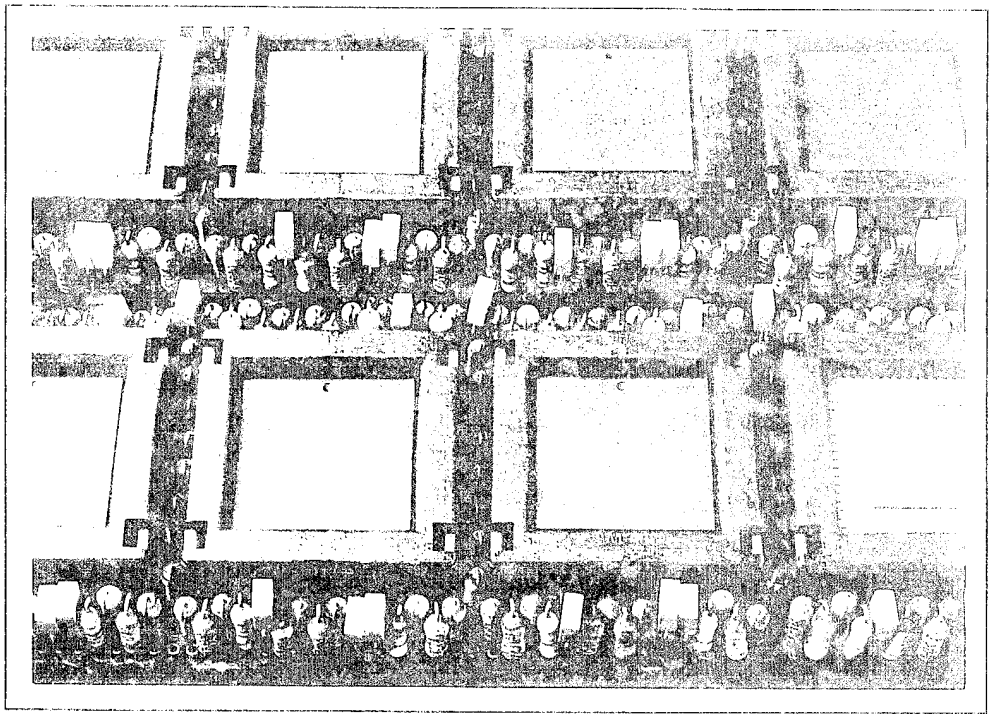
PLASTIC PACKAGE AVAILABILITY PROGRAM

FINAL REPORT

Contract No DLA900-92-C-1647

Objective:

Investigate contemporary technology and provide recommendations which are critical to the selection of plastic-encapsulated microcircuits in harsh military environments.



HAST Board loaded with 68L-PLCC devices *ready for insertion into the high temp, high humidity environmental test chamber at Dow Corning, in Auburn, Mich. Note the high density of surrounding circuit board components required for powering and biasing this high lead-count device. Also note the golden ceramic CQJB control unit to the right and the test compound marking on the plastic units. B24 & UL512HX*

PREFACE

The use of PEM in military systems offers several advantages over ceramic parts, such as weight, size, cost, and increasingly, availability; however, historically PEM have not met the most stringent reliability requirements of mil-standard specifications. This final report for the Plastic Package Availability (PPA) Program, a Tri-Service sponsored effort funded through the Defense Logistics Agency (DLA), describes the results obtained from the investigation of this dilemma. ***The program's objective was to investigate contemporary technology and provide a better understanding for the potential use of plastic-encapsulated microcircuits (PEM) in military systems.***

This program investigated and tested a variety of PEM components and attendant issues in order to better understand and guide the military and its suppliers in the use of PEM in military systems. The program goal was to baseline PEM package performance capability in harsh environments as well as investigate potential material improvements which might be achievable in the near term. John Christensen of the Manufacturing Engineering/Research Office was the DLA program manager for the PPA program. The DLA program office was supported by a government steering committee comprised of: Dr. Noel Donlin, Army-MICOM; Leon Lantz II, DoD; Greg Pitz and Robert Tonar (interim program mgr.), DESC; Dan Quearry, NSWC-Crane; James Reilly, USAF-Rome Labs and Robert Savage, NASA-Goddard.

National Semiconductor Corporation (NSC) was the prime contractor for this program under Contract No. DLA900-92-C-1647. Ron Kovacs was the program manager for NSC, in the Packaging Corporate Technology Group. Comprising the PPA performing team were NSWC-Crane Labs, Dow Corning, Honeywell Technology Center and Commercial Flight Systems, Plaskon Electronic Materials/Amoco, USAF-Rome Labs and Sandia National Laboratories. This team covered PEM manufacture, test, environmental stress, die coatings, mold materials, sensor test chip development and failure analysis.

The subcontracting program managers were: Crane, Dan Quearry; Dow Corning, Robert Camilletti; Honeywell, Fred Malver; Plaskon, Dr. Nicholas Rounds; Sandia, David Peterson. Unfunded additional study was managed by James Reilly, Rome Labs. Additional credits for these organizations are included in their final reports which are contained in the "Sections" portion later in this report.

This report is organized into five main parts; Executive Summary, Task Discussion, Results, Conclusions (with recommendations and suggested areas for future work) and Sections. "Sections" includes a Materials of Construction tutorial, each of the individual performing team's Final Reports, the Failure Analysis Final Report, and Documentation, containing the NSC HLC Final Test Report and various program supporting materials.

The program tasks and the organizations performing work for those tasks are:

TASK	DESCRIPTION	PERFORMER
Task 1.0	Mil IC Pkg. Criteria Definition & System Selection	All & Honeywell
Task 2.0	Plastic Package Criteria Definition	Plaskon
Task 3.0	Mold Compound Formulation and Optimization	Plaskon
Task 4.0	Moisture & Corrosion Test Chip Development	Sandia
Task 5.0	Assembly of Test Devices	National
Task 6.0	RWOH Coating of Test Devices	Dow Corning
Task 7.0	Device Reliability Testing	Crane, DC, NSC
Task 8.0	Device Reliability Analysis	NSC, Rome
Task 9.0	Plastic Usage Specification	Plaskon
Task 10.0	Technology Transfer	All
Task 11.0	Program Management	National
Task 12.0	Data Items	National

The PPA technical supporting team at National Semiconductor consisted of: Dr. Randy Lo, Manager of Packaging Materials, Andrea Chen, Mold Engineer, and Dr. Luu Nguyen, Sr. Staff Program Manager, all of the Packaging Technology Group; Jeffrey Weintraub, Staff Statistician, Corporate QA; Thomas Pak, Test Engineer and Dr. Robert Byrne, Sr. Engineering Program Manager, both of the Government Technology Business Unit; Rebecca Simmons, Associate Engineer and Joseph Bendik, Assistant Program Manager, both of National's Research Lab.

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GLOSSARY OF TERMS

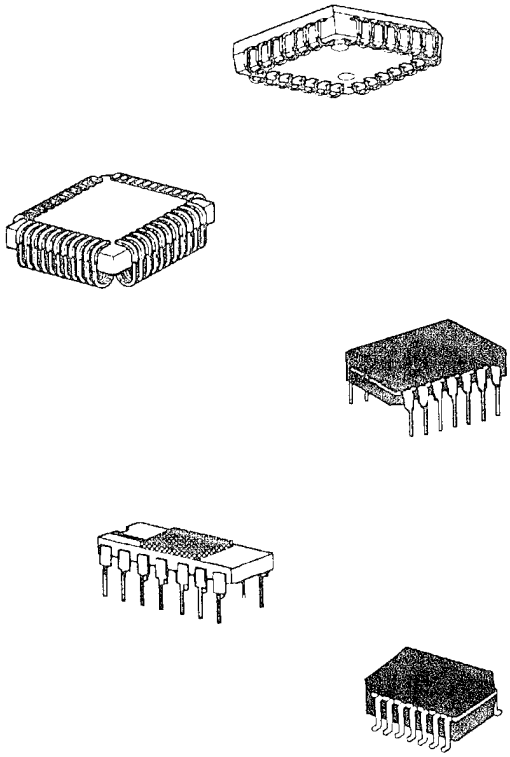
Å	Angstrom (10k Å = 1 micrometer)
ATC04	Stress sensor Assembly Test Chip developed by Sandia National Labs
AES	Auger Electron Spectroscopy
ARPA	Advanced Research Program Office
B_	B8, B14, B24 (National Standard Molding Compound)
CERDIP	(CDIP) Ceramic Dual In-line Package
CMOS	Complementary Metal Oxide Semiconductor
C-SAM	C-Mode Scanning Acoustic Microscope
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
DoD	Department of Defense
DI	Deionized Water
DIP	Dual In-line Package
DLA	Defense Logistics Agency
DOE	Design of Experiment
EDS	Energy Dispersion Spectroscopy
FOx®	Flowable Oxide, Product of Dow Corning
FTIR	Fourier Transform Infared Spectroscopy
GaAs	Gallium Arsenide
HAST	Highly Accelerated Stress Test
HLC	High Lead-Count Package
HTS	High Temperature Storage
IC	Integrated Circuit
I/O	Input and Output
JEDEC	Joint Electronic Device Engineering Council
LCC	Leaded Chip Carrier
LM124	Generic industry part number for a 14 pin Quad-op-amp
LRU	Line Replaceable Unit
MC	Molding Compound
MCM	Multi-Chip Module
MDIP	Molded Dual In-line Package
MOS	Metal Oxide Semiconductor
MTBF	Mean Time Between Failures
MTTF	Mean Time To Failure
NASA	National Aeronautical Space Administration
NAT-01	National Semiconductor -01 Moisture Corrosion Sensor Test Chip
Ni	Nickel
OPL	Operating Life (Test)
PDIP	Plastic Dual In-line Package
PECVD	Plasma Enhanced Chemical Vapor Deposition

GLOSSARY (continued)

PEM	Plastic Encapsulated Microcircuit
PLCC	Plastic Leaded Chip Carrier
PQFP	Plastic Quad Flat Pack
PPA	Plastic Packaging Availability
Precondition	Board Assembly Simulation
RH	Relative Humidity
RIE	Reactive Ion Etch
RT	Room Temperature
RWOH	Reliability Without Hermeticity
SAM	Scanning Acoustic Microscopy
SCX6244	Internal National Semiconductor part number for 4.4k CMOS gate array
SEM	Scanning Electron Microscope
SLAM	Scanning Laser Acoustic Microscope
Si	Silicon
SiC	Silicon Carbibe
SMT	Surface Mount Technology
SOIC	Small Outline Integrated Circuit
SPEC	Surface Protected Electronic Circuit
TC	Temperature Cycle
TEM	Transmission Electronic Microscope
TSOP	Thin Small Outline Package
ULS12HX	Plaskon low stress mold compound
VLSI	Very Large Scale Integration
WDX	Wavelength Dispersion X-ray
WL	Wright Laboratory
WVTR	Water Vapor Transmission Rate
XM	X-ray Microscopy
X9074	X9074.07, Plaskon experimental anti-popcorn mold compound
34, 34X	3400, 3400X Plaskon molding compounds
68L-CQJB	68 lead ceramic quad J-bend package outline; also referred to as CQCC-J68 in MIL-STD-1835

PLASTIC PACKAGE AVAILABILITY PROGRAM

EXECUTIVE SUMMARY



EXECUTIVE SUMMARY

Background: The PPA program was a 3 year effort, which included a 9 month delay for loss of funding after the first year, concluding in November of 1995 with a final full-day review at the SHARP conference in Indianapolis, IN. In addition to the performing partners Navy-Crane, Dow Corning, Honeywell, Plaskon, AF-Rome, and Sandia National Laboratory, an effective government steering committee comprised of USAF-Rome, NSWC-Crane, NASA-Goddard, Army-MICOM, Huntsville, DESC-Dayton, DoD-Ft. Meade and the funding agency, DLA-Arlington, gave guidance and support to the effort.

In the course of the program execution, a detailed plan was devised, industry surveys were made, field data was collected and analyzed, sensor test-chips were developed and evaluated, an extensive PEM experiment was conducted, and frequent technology transfer activities were undertaken; including; industry updates at JC13 meetings, mailings to interested parties, workshops with the government steering committee, and technical papers presented, as well as, comprehensive 6 month and final reviews.

Task Discussion: This report documents the successful completion of the tasks and deliverables, contained in the original and revised "re-start" Statements of Work, for contract No. DLA900-92-C-1647 resulting from BAA 92-02-MLK, Subarea E2, Plastic Availability, awarded to National Semiconductor Corporation. The main reliability task of the PPA program benchmarked present day PEM capability in harsh, military-like environments. The program also documented an OEM users experience in the use of PEM in systems aboard commercial aircraft. Other significant accomplishments and efforts include the development of a unique moisture/corrosion sensor test chip, evaluation of a wafer-level chip hermetic coating technology, characterization and test of enhanced-performance molding compounds, and C-SAM/dye-penetrant studies.

Results: The following are the key results from the program tasks.

1. *Extended accelerated life-testing*, at Crane, Dow Corning, and National on PEM produced a total of 285/1555 failures for study (some tests were run purposely beyond the device ratings). Most failures (94%), were in the **moisture related HAST** tests. The major failure mode was metal corrosion initiating at the bond pad. In these HAST tests the following variables significantly affected failure rates:

- board assembly "preconditioning" stress simulation
- operating voltage
- mold compound formulations

Two temperatures (130 °C & 159 °C) were run on the HAST tests, and both produced similar failure modes, thus allowing the calculation of activation energies and prediction failure-rate curves for times vs. temperature and voltage.

Temperature cycle caused 12/36 of the high lead-count units from one mold compound type to fail because of package-stress caused cracked chip dielectric.

High Temperature Storage did not produce any room temperature electrical failures, however, due to intermetallic formation between the gold ball-aluminum bondpad structure, bond strengths were degraded below minimum bond-pull values. Electrical tests at 125 °C showed a high gross-functional failure rate on these same devices, whereas only minimal bond strength degradation and no electrical failures occured on the ceramic control parts at 125 °C. The ceramic controls use an aluminum-aluminum bond structure.

Ceramic-hermetic parts made effective control units with only 2/300 failures for all life-tests combined.

2. *System user experience,* by an OEM (Honeywell), in using careful vendor selection, qualification and parts screening reports on a successfully implemented program using PEM in commercial avionics guidance systems. Linear technology parts required special attention. In the relatively benign environment of the cooled aircraft equipment bay, acceptable field failure rates were obtained, approaching and in some cases exceeding, those failure rates observed for ceramics. Component failure rates varied significantly between systems. Dry storage and bakeout procedures were adhered to before board assembly.

3. *The Nat-01 moisture/corrosion test chip*, developed by Sandia National Laboratories, proved to be effective in sensing moisture and corrosion inside the PEM package. In most cases the sensor data correlated well with the product-mold compound test results. Another sensor, the Assembly Test Chip (ATC04), previously developed by Sandia, also measured package stress and differentiated between the test mold compounds. The NAT-01 will be offered commercially by Sandia as is presently done with the ATC04.

4. *The wafer level coating process,* developed jointly by Dow Corning and National, with shared funding from another DoD program, on a best-effort basis, did not prove successful on the first attempt to passivate product wafers. This effort is being continued by Dow Corning, Sarnoff Labs, and Microelectronics Center of North Carolina under a USAF-WRDL funded program called "Chip Seal". An update of this program was given at the final review and is included in Dow Corning's Section in this report.

5. *Plaskon characterized and provided enhanced versions of several of their commercially available mold compounds* for the DOE component build. HAST results from product and

NAT-01 devices, in most cases, favored the use of "ionic getter" additives. TC results from product did not conclusively favor low-stress formulations.

6. *Work by USAF-Rome Labs* on product from the life test experiment showed no correlation between initial C-SAM measurements and future fails. Dye-penetrant studies showed a leakage path from the external lead to the bond pad on a preconditioned SOIC device. The mold release waxes in the compound formulations are known to accumulate at the internal package material interfaces, and thus could offer an enhanced path for the dye chemicals, which would not necessarily hold for moisture, per Jim Peterson of Plaskon.

Key conclusions: With proper vendor selection, qualification and application, PEM can give reliable performance when used with-in manufacturer's maximum specified conditions, in relatively benign environments. Concern continues to exist for operating PEM in harsh military like environments thus precautions should be taken to isolate PEM from harsh environments and to derate operating conditions when possible, to gain extended, longer-term reliability. This concern is a result of the three main failure modes experienced in the accelerated life-test study. The three in order of importance (occurance), are:

1) Moisture remains a concern for all PEM, especially when conditions of aggressive board assembly processing is used, and the accelerating forces of higher voltages and/or temperatures exist. Absorbed moisture can cause immediate package integrity to be compromised during board assembly solder operations (popcorning, although not observed in this study, is an industry concern), or corrosion of chip metallizations can occur, resulting in longer-term device failure. The use of compound getter additives did not show an advantage in all cases.

2) Package stresses can be a concern, especially for larger die/package combinations, in that the die can crack from extreme cycling of temperature; however the temperature cycle DOE results did not confirm the value of using low-stress compounds.

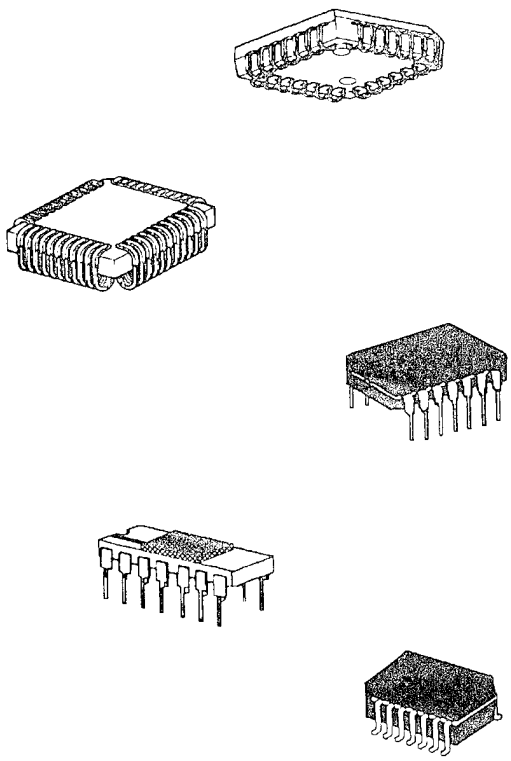
3) Intermetallic formation in the gold-aluminum wire bond structure (unique to most PEM), resulting from prolonged exposure to high temperatures, and in the presence of other contaminants, results in severe bond-strength degradation and eventual electrical failure.

Recommendations: A list of recommended DO's and DON'Ts has resulted from the PPA program, for example; "do use board assembly "preconditioning" prior to qualification, which simulates worse-case board assembly/repair conditions" and "don't use aggressive, halide-based fluxes, during PEM board-solder assembly/repair".

Finally, several areas for future work are recommended, such as "determine the 'culprit' process step(s) in the preconditioning flow", and the development of a chamber and test for determining the long-term reliability for storage and intermittent operation of PEM in realistic corrosive environments.

PLASTIC PACKAGE AVAILABILITY PROGRAM

TASK DISCUSSION



TASK DISCUSSION

Background: The original PPA program award was made in mid-'92 and designed for a 2 1/2 year effort, but then was put on hold by the DLA for lack of funding less than a year later. In the spring of '94 funding was again secured (although reduced), and in May a "re-start" announcement and review was held at the Joint Electron Device Engineering Packaging Council (JC13) meeting in San Diego (See *Figure* 1, Plastic Package Availability Program Schedule).

The original charge of the program was to evaluate standard commercial PEM under military environmental conditions resulting in recommendations for PEM "Mil-Specifications and Standards". Only commercially available, non-research type, plastic molding compounds were to be evaluated. Minor modifications were to be allowed to evaluate possible "easy" enhancements which could be made to improve PEM reliability under harsh environmental conditions.

Tasks: Please refer to *Figure* 1, Plastic Package Availability Program Schedule, throughout the Task Discussion for task organization, schedules and subtask detail.

Task 1.0 Mil IC Package Criteria Definition and System Selection.

Subtask 1.1 Preliminary Review (all)

A preliminary review of all proposed tasks was held on November 2nd, 1992, the program subcontractors, and a meeting the following day, was held with members of the government steering committee to agree on final approaches and time schedules. This meeting was held at NSWC-Crane. All tasks and schedules were agreed on.

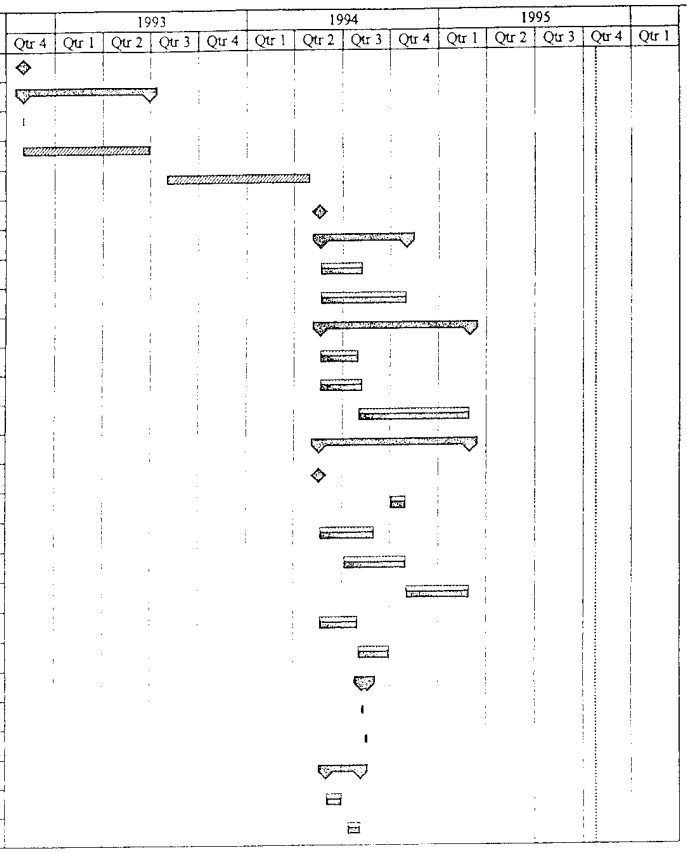
A "Materials of Construction" tutorial was included as a deliverable in this subtask and is included in this report as Section 1.

Subtask 1.2 System Selection and Baseline Description (Honeywell)

Honeywell provided the system user perspective to the PPA program. Honeywell's Commercial Flight System business had an experience base using both ceramic and plastic devices in their LRU's (line-replaceable units). This subtask involved system selection for the study, identification and listing of all integrated circuit (ICs) components, vendor selection and procurement process as well as subsequent part processing, production and repair flow. This subtask was completed and documented in an interim report, and is included in Honeywell's Final Report, (see Section 8) as Appendix B.

PLASTIC PACKAGE AVAILABILITY PROGRAM RESTART SCHEDULE

ID	Name
1	PROGRAM START November, 1992
2	**Task 1.0 Mil IC Pkg Criteria Def. & System Selection**
3	Subtask 1.1 Preliminary Review
4	Subtask 1.2 System Selection & Baseline Description
5	Note: Program on Hold Aug '93 to May '94
6	Restart Kickoff Mtg @ JC13 in San Diego 5/22
7	**Task 2.0 Plastic Pkg Criteria Def.**
8	Subtask 2.1 Select & Supply Formulations
9	Subtask 2.2 Select General Specification
10	**Task 3.0 Mold Compound Formulation and Optimization**
11	Subtask 3.1 Compound Formulation
12	Subtask 3.2 Anti-popcorn Formulation
13	Subtask 3.3 Compound Characterization
14	**Task 4.0 Moisture & Corrosion Test Chip Development**
15	Subtask 4.1 Test Chip Design (complete)
16	Subtask 4.2 Develop test Chamber (documentation)
17	Subtask 4.3 Develop Test Procedures
18	Subtask 4.4 Test Chip Calibration
19	Subtask 4.5 Moisture Specification
20	4.5a Deliver Nat 01 Sensor Chips
21	4.5b Chip Process Specs & GDSII file
22	**Task 5.0 Assembly of Test Devices**
23	Subtask 5.1 High Lead-Count Devices
24	Subtask 5.2 Low Lead-Count Devices
25	**Task 6.0 RWOH Coating of Test Devices (best effort)**
26	Subtask 6.1 Mask design
27	Subtask 6.2 Coating of Test Devices



PLASTIC PACKAGE AVAILABILITY PROGRAM RESTART SCHEDULE

ID	Name
28	**Task 7.0 Device Reliability Testing**
29	Subtask 7.1 Test Plan Definition
30	Subtask 7.2 Benchmark & Rel Test
31	Subtask 7.3 Moisture Correlation Tests
32	**Task 8.0 Device Reliability Analysis**
33	Subtask 8.1 Reliability Prediction Methodology
34	Subtask 8.2 Assessment of Fielded Systems
35	**Task 9.0 Plastic Usage Specification**
36	Subtask 9.1 Materials & Testing Specifications
37	**Task 10.0 Technology Transfer**
38	Subtask 10.1 Information Dissemination Reviews
39	Subtask 10.2 Information Dissemination Conferences
40	Restart Review @ JC 13 Meeting (San Diego, CA
41	Status Review @ JC.13 Meeting (Dayton, OH)
42	6 Month Review @ SHARP Conference (Indianapolis, IN)
43	Status Review @ JC 13 Meeting (Chandler, AZ)
44	Status Review @ JC 13 Meeting (Providence, RI.)
45	Pgm Review @ Adv Tech A, Q, & R Wkshp (Newport Bch, CA)
46	Status Review @ JC 13 & internal final @ DESC (Dayton, OH)
47	Pgm Final Review @ SHARP Conf (Indianapolis, IN.), 11/15/95
48	**Task 11.0 Program Management**
49	Subtask 11.1 Program Management
50	Subtask 11.2 Key Personnel
51	**Task 12.0 Data Items**
52	Subtask 12.1 Monthly Financial Reports
53	Subtask 12.2 Monthly R&D Reports

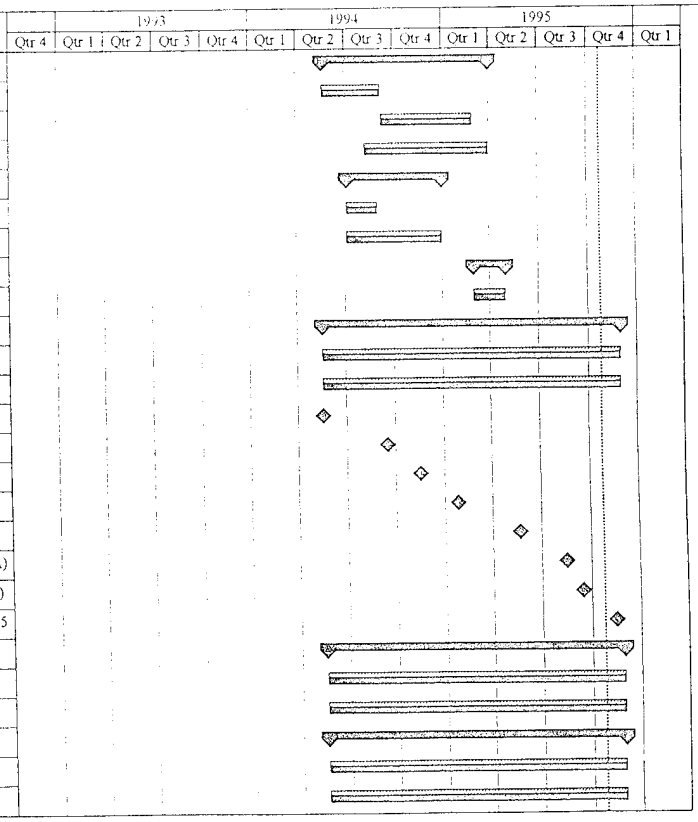


Figure 1

Task 2.0 Plastic Package Criteria Definition (Plaskon)

This task primarily was to select epoxy mold compound (EMC) formulations for the building of plastic encapsulated microcircuits to be assembled in task 5.0. It was broken into two subtasks, one for selection of baseline formulations and the other for review of commercial specifications for EMCs.

Subtask 2.1 Select and Supply Formulations

Plaskon selected two standard commercially available EMC's as the baseline compounds, to be used in the design of experiment (DOE) designed for the PPA program in Task 7.1. (See *Figure* 2, PPA DOE). Their 3400 standard compound for low to moderate lead-count packages and ULS12H formulation for high lead-count packages requiring low stress were chosen for the 14L and 68L packages, respectively. Please refer to Plaskon's Final Report, Section 2, Table 2, for typical material properties of these two compounds.

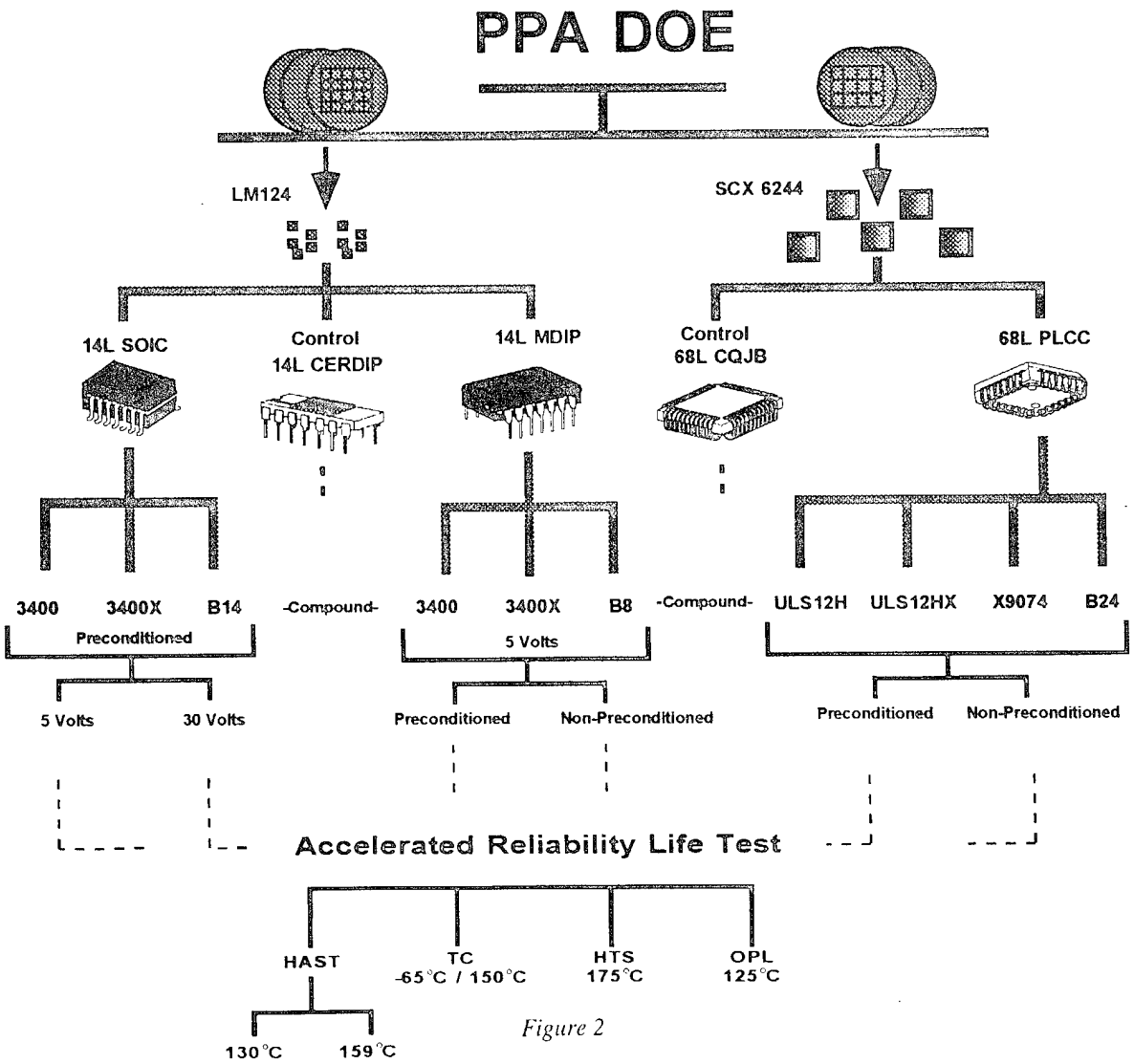


Figure 2

Subtask 2.2 Select General Specification

Plaskon surveyed the commercial supplier industry for EMC's and found very good agreement for the established properties that were measured. Also the semiconductor user industry was surveyed and these key points and typical qualification tests were noted concerning EMCs:

- Ionic purity was considered important for device reliability
- Flame retardant levels (bromine) are minimized for optimum HTS reliability
- None of the respondents knew of any device field failures directly traceable to plastic encapsulants
- Extensive functional reliability testing is required for qualification of plastic encapsulants but device reliability tests are not usually included in mold compound specifications

Typical EMC User Qualification Tests

Package Assembly Related	Device Performance Related
Moldability (flow & release)	Pressure Pot, 15 psi/126 °C
Wire Sweep	Thermal Shock, -65 °C to +150 °C
Void Level	HAST, 130 °C / 85% RH
Mark Permanency	HTS, 175 °C / 200 °C
Wire Bond Pull Strength	Package Crack & Delimitation after:
Line Movement (chip metal traces)	preconditioning, 85% RH / 85 °C and
Board Adhesion	solder reflow, 212-235 °C

Refer to Plaskon's Final Report, Section 2, Tables 3 and 4, for a typical EMC procurement specification and a recommended specification template.

Task 3.0 Mold Compound Formulation and Optimization (Plaskon)

Task 3.0 is comprised of three subtasks: 3.1, Compound Formulation; 3.2, Anti-popcorn Formulation and 3.3, Compound Characterization.

Subtask 3.1 Compound Formulation

The approach elected by Plaskon was to use ultra-pure epoxy cresol base resins to reduce the amount of total hydrolyzable chloride content in the EMC, thus reducing the available ionic contamination available to cause bond pad corrosion. Also ion scavengers (getters) were added to produce the these higher reliability formulations. Testing at Plaskon showed improved performance with these enhanced compounds in HAST at 145 °C and HTS at 200 °C. Elimination of the flame retardant additive (Bromine) to Plaskon's EMC 3400 also showed improvement on 200 °C HTS, but this was not considered a practicable enhancement at this time. See Plaskon's discussion of task 3.1 (Plaskon Final Report, Section 2), for added detail and data (testing at Plaskon should not be confused with the PPA DOE).

Subtask 3.2 Anti-popcorn Formulation (9074.07 compound)

This task was added at the time of the program restart due to an industry trend and desire to use thinner surface mount packages and concern for the cracking (popcorning) of these devices during solder reflow. Elaborate dry-bagging procedures (see *Figure* 3, Photocopy of dry bag used for shipping and storing surface mount devices, with labeled moisture/baking instructions, National Semiconductor) are required for many surface mount device types to preclude this cracking during board assembly. The plastic molding compound has a proclivity to absorb moisture and when quickly heated, such as in a solder reflow IR or vapor-phase furnace, will crack with an audible noise if the plastic is not strong enough to withstand the steam pressure. The dry bag in *Figure* 3 stipulates that after opening the bag the units must be mounted within 72 hours, or stored at less than 20% RH or baked... and several bake options are given, before board mounting. The reason for this is shown in *Figure* 4, which shows moisture take-up for the 4 HLC mold compounds selected in the following subtask 3.3, and used in the PPA DOE. The graphs show that in less than a day, the compounds have reached approximately 50% saturation by weight percent at the accelerated conditions of 159 °C/ 85% RH.

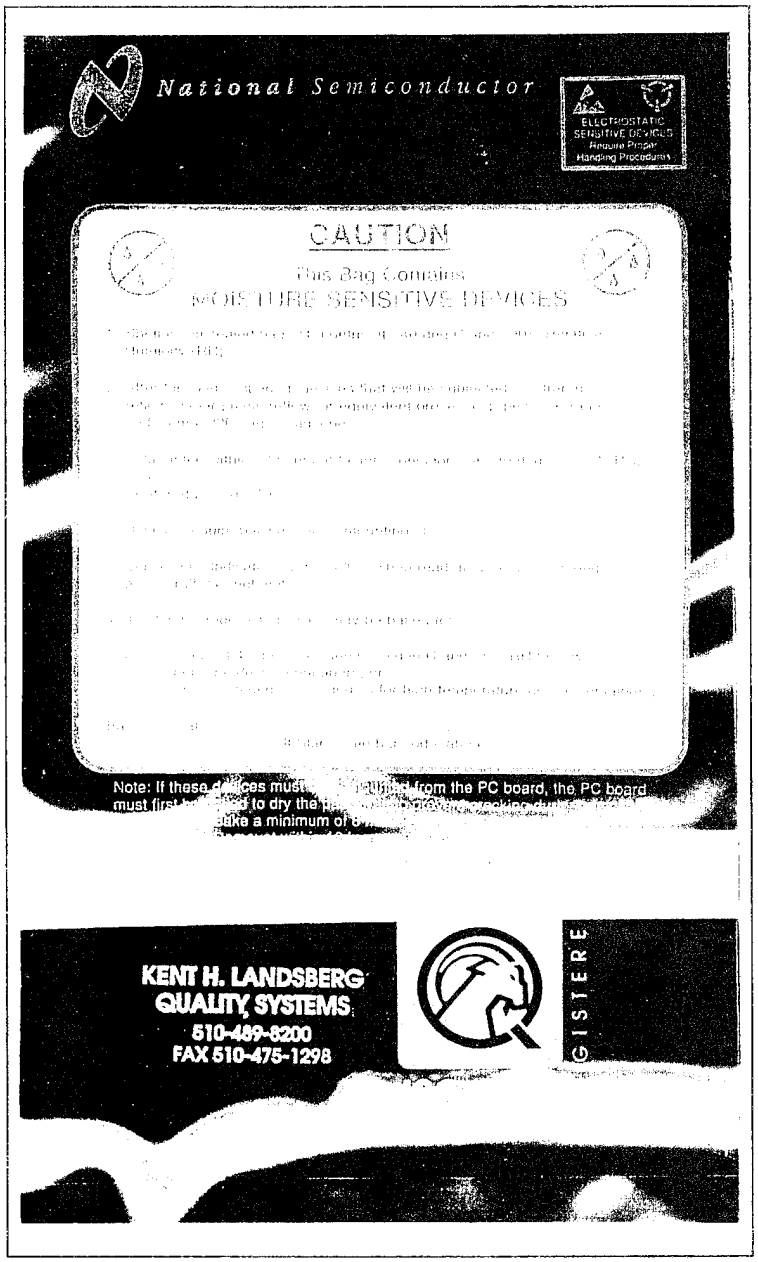


Figure 3 Dry Bag for shipping SMT

Subtask 3.3 Compound Characterization

Plaskon characterized the five resulting compound formulations, three for a high lead-count (HLC) plastic package and two for a low lead-count (LLC) package. These selections included the standard EMC 3400 for the LLC package , and low stress EMC ULS12H, for the HLC

package, higher reliability versions of both, using ultra pure resins and additive getter compounds, (to remove mobile ionics), as well as a high strength "anti-popcorn" EMC for the HLC package; X9074.07. These compounds all fall into the class of thermosetting epoxy polymers. Please refer to Plaskon's Final Report, (Section 2) for a detailed discussion of the selection rationale.

Plaskon prepared the 5 test compounds in their Singapore manufacturing facility, using raw materials from the same lots. Over 5 Kgm of each was shipped under refrigeration to National's production facilities in Malacca, Maylasia (3400 / 3400X for LLC) and National's Singapore facility (ULS12H / ULS12HX and X9074.07 for HLC). Samples of the Plaskon test EMCs plus samples from the National standard production mold lots (B8/14/24) were sent to Plaskon's research labs in Springhouse, PA for testing and characterization. Both lower chlorine and bromine were measured on the high reliability "X" versions. It was felt that the lower chlorine could have resulted simply from using lower chloride epoxy for these formulations, but the lower bromine has to be due to the action of the scavenger additive. Refer to Plaskon Final Report (Section 2) to table 10 for the characterization of the five selected test compounds, and table 14 for the three NSC standard production compounds.

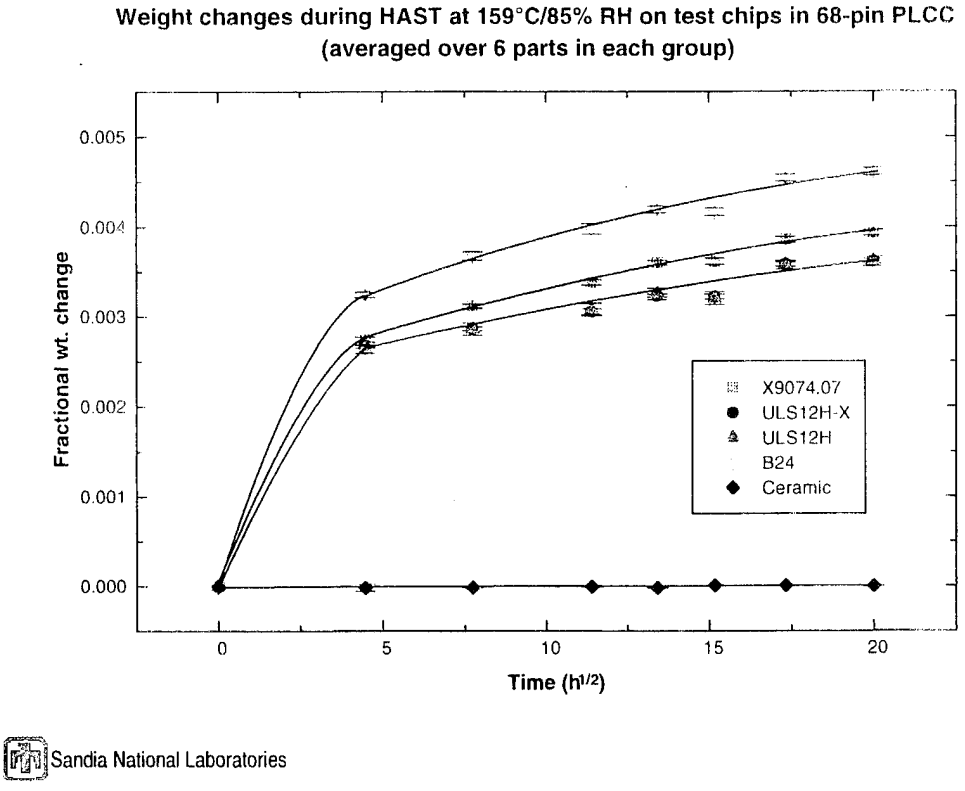


Figure 4

Task 4.0 Moisture and Corrosion Test Chip Development (Sandia)

This task was divided into five subtasks, and then a best effort task was added to study the HLC device using the Sandia ATC04 (Assembly Test Chip) stress sensor. The subtasks were 4.1, Test Chip Design; 4.2, Develop Test Chamber; 4.3, Develop Test Procedures; 4.4, Test Chip Calibration; 4.5, Moisture Specification, which included, 4.5a, Delivery of Test Chips to National for use in the DOE and 4.5b, Chip Process Specifications and GDSII (design) file. Refer to Sandia Final Report (Section 3) for a complete discussion of these tasks; however, please note that Subtask 4.2, Develop Test Chamber, was included in the Test Chip Calibration subtask in the Sandia report, so the subtask numbering sequence is one off when compared to the Gantt Schedule in *Figure* 1, and with the discussion that follows.

Subtask 4.1 Test Chip Design

A moisture and corrosion sensor chip (NAT-01) of 100 mils on a side was designed to accommodate the LLC package types to be used in the DOE. The design is shown in Sandia's *Figure* 6 (Section 3). A triple track metal trace structure is shown in four quadrants, two passivated and two unpassivated. The moisture sensor tracks are over porous silicon, which change capacitance as moisture is absorbed. The corrosion sensor tracks are over silicon dioxide.

Subtask 4.2 Develop Test Chamber

A test chamber was developed and documented to calibrate the NAT-01 test chip designed in Subtask 4.1. See *Figure* 11, Precision humidity generator functional layout, in Sandia's report (Section 3), for a schematic of the test chamber.

Subtask 4.3 Develop Test Procedures

Possible test set-ups with biasing arrangements are shown in *Figures* 8 & 9 in Sandia's report (Section 3) for the moisture and corrosion sensor elements. *Figure* 10 shows a typical electrical measurement set-up for the NAT-01. These procedures were used to characterize the NAT-01 in Subtask 4.4.

Subtask 4.4 Test Chip Calibration

The procedures developed in Subtask 4.3 were used to calibrate the NAT-01 test chip and show robustness of the chip design and process. The NAT-01 die that were to be supplied to National for inclusion in the DOE were characterized, and identification maintained by wafer area, so that Sandia could determine the effects of package assembly processing on the sensor chip electrical characteristics. A number of "best effort" tasks involving in situ moisture tests were outlined to further investigate the potential applications of the NAT-01. Sandia further broke this subtask into characterizing the moisture monitor and characterizing the corrosion

monitor in their final report, (Section 3). Sensor chip data is given for the various mold compounds used in the PPA DOE in Sandia's Table III for passivated NAT-01 elements, from life-tests run at both Crane and Dow Corning. Sandia's *Figure* 22 shows exposed bond pad voiding failure from Crane HAST tests, while the silicon nitride passivated triple track sensor structure remains unaffected.

Subtask 4.5 Moisture Specification

This task was designed to produce a test specification for the NAT-01 similar to JEDEC Test Method A110 for HAST. It was expected that the hermetic chip coating process to be developed in Task 6 would be available in time to allow completion of this task, unfortunately, it was not. The procedures and methods that have been developed and tested in a laboratory setting for the NAT-01 should be adequate to continue this work at such time that a chip seal process becomes available.

In excess of 500 NAT-01 separated chips were characterized and delivered to fulfill Subtask 4.5a requirements shown in the PPA Gantt schedule, *Figure* 1. A NAT-01 unit process (wafer fabrication) flow specification and a GDS II design file tape were delivered to National to meet the documentation requirements of Subtask 4.5b.

Subtask 4.6 Stress Measurement using ATC04 (a "best effort task" included mid-way in the program at the suggestion of industry observers- not shown on PPA Schedule)

The ATC04 is a Sandia developed stress sensor chip which is offered commercially. It is designed with an array of diffused silicon resistors which have been calibrated to measure stress imposed on the chip from the package materials, through the piezoelectric effect. Temperature compensation is accomplished with a diode thermometer. This chip was used in a side experiment to the main PPA DOE to monitor stress after the assembly operation (die attach and molding) using the different test compounds for the 68L-PLCC package, i.e., ULS12H, -12HX, X9074.07 and the B24 standard. The ULS12HX low stress and low ionics compound had the lowest stress after assembly, whereas the X9074.07 anti-popcorn and B24 had the highest, as shown in *Figure* 27 of the Sandia report, Section 3. This is followed by *Figure* 28 which shows the stress relaxation measured on these parts after interim steps in the preconditioning flow sequence (temperature cycle and solder reflow).

Task 5.0 Assembly of Test Devices

In this task both low lead-count LM124 linear quad op-amps and high lead-count SCX6244 CMOS 4.4K gate array custom digital avionics circuits were built in National's off-shore volume production facilities to fill the requirements of the PPA DOE shown in *Figure* 2. The ceramic control units for each chip type were assembled in National's Santa Clara, CA packaging pilot production facility. NAT-01 test sensor devices were also assembled in each package type, although these are not shown in *Figure* 2. Jim Reilly of Rome Labs accompanied

National packaging engineers from Santa Clara, to direct the assembly builds in Southeast Asia. They were assisted by local National assembly engineering and production personnel. In addition, for the set-up of the mold processes involving the Plaskon compounds, engineers assisted from Plaskon's Singapore production facilities, which manufactured all the Plaskon supplied compounds.

The challenge was to keep the builds as near to standard production as was possible, but yet maintain sub-lot identity and retrieve sub-lot assembly monitor data. Special treatment was avoided, but yet at the same time enough attention was given to insure that when the builds were done and in test, enough good units would result to meet the DOE quantity requirements. This was accomplished by both over-building and by assigning sub-lot identity at the die attach process step, which immediately follows die saw (separation from the wafer), see assembly process flow, *Figure* 5. These sub-lots were identified as to the special marking each would get just prior to singulation, identifying mold compound used and whether the chip was a NAT-01 sensor chip or a product chip.

Subtask 5.1 Assembly of LLC Test Devices

The LLC plastic devices were assembled in National's Malacca, Malaysia plant in the month of August, 1994. Four linear LM124 wafers were used. The ceramic control units were assembled in National's Santa Clara, CA facility, in 14L CERDIP packages. One wafer was partially used. (See *Figure* 5, PPA Low Lead-Count Plastic Assembly Process Flow).

PPA Low Lead-Count Plastic
Assembly Process Flow

1. Die Saw
2. 2nd Optical (sample)
3. Die Attach (Lot formation)
4. Poly Cure
5. Wire Bond
6. 3rd Optical 100%
7. Mold
8. X-ray sample
9. Post Mold Cure
10. Die Set Deflash
11. Media Deflash
12. Mark (include EMC type)
13. Solder Plate
14. Open / Short test

Figure 5

The LLC plastic build was split into 14L-SOIC Wide Body (surface mount) and 14L-MDIP (through-hole mount) standard production packages. Both packages use a copper lead-frame with silver coated lead tips and die attach paddle, to facilitate bonding (often "down-bonding" is used from the chip to the paddle to make a ground connection, but is not required on the

LM124). One hundred each of the NAT-01 moisture/corrosion sensor test chip were also assembled in the two 14L packages. The NAT-01 die attach required manual "hand" die attach because the die had been separated from the wafer at Sandia and put in die waffle packs for shipment, thus losing the close tolerance orientation required for automatic die attach. The LM124 electrically probed product wafers however, were affixed to sticky, stretch- membrane and wafer-sawed per standard volume production "automatic" die attach. Several frames of reject die were also assembled with each sub-lot, to be later used for mold set-up, (see *Figures*, 1, 2, and 3, Section 4, Documentation).

All product builds (with sub-lot identity at die attach), were assembled on the same piece of equipment at each assembly step, at the same time, i.e., as one large lot. No problems were encountered in the build, all yields ran the typical 98+%. At mold, each compound to be used (3400, 3400X, B8 -MDIPs, & 3400, 3400X, B14-SOICs) was purged through the gang-pot mold press and then several test "shots" run, using the lead-frames assembled with reject die. Visual inspection for flashing run-out, mold fill, surface pitting, and X-Ray inspection for mold wire-wash was performed (see *Figure* 4 in Section 4, Documentation). Only minor adjustments to in-mold cure times had to be made from those used for the standard B8 and B14 compounds, to accommodate the 3400 and 3400X Plaskon supplied compounds.

In addition to the standard product and date code marking, the mold compound used was also stamped on each part. Prior to shipping back to Santa Clara, the parts were 100% tested at room temperature, pass-fail, to the LM124 test program. Again, test yields were typical for this product at 95+%, and there was negligible difference between the sub-lots. The assembly was accomplished in a weeks time, utilizing 1st and 2nd shifts only, so that engineering monitoring could prevail to preclude part mixing. The electrical testing and shipment to Santa Clara, CA was accomplished the following week.

In Santa Clara, the parts were preconditioned (parts ship/storage/board assembly simulation), per the flows for each package type shown in *Figure* 6, Precondition Flow Sequence. Per the DOE plan shown in *Figure 2*, a sufficient number of parts to populate the "No Precondition" branch were withheld from preconditioning. The parts were then shipped to NSWC-Crane Labs for 100% post preconditioning electrical screen and "zero-hour" base-line testing.

Subtask 5.2 Assembly of HLC Test Devices

In August of 1994, during the week following the LLC build in Malacca, in Subtask 5.1 above, the States-side engineering team accomplished the build of the HLC 68L-PLCC SCX6244 parts in a similar manner to the LLC build. Again they were assisted by local National and Plaskon engineering. While in Singapore, both Sumitomo and Plaskon mold compound production facilities were toured by the visiting engineering PPA team, including Jim Reilly of Rome Labs. The ceramic quad J-bend (CQJB) parts were assembled in Santa Clara, California.
The SCX 6244 chip is about 15X larger in area than the LM124 chip. It is made with a more dense, 2 micrometer CMOS wafer fabrication technology, on 6 inch (150 millimeters) wafers, as

compared to the more mature, LM124 product, which uses linear wafer fabrication technology equivalent to 5 micron technology, on four inch (100 millimeter) wafers. The SCX6244 wafers also have an organic stress relief coating applied in wafer fabrication for those wafers intended for plastic packaging. Those wafers intended for ceramic-hermetic assembly do not require the stress relief coating, nor does the much smaller LM124 die.

As with the LLC assembly, lots were formed at die attach, identifying the four mold compounds to be used, ULS12H, ULS12HX, X9074.07 from Plaskon and the standard production compound used by National, B24. Each device was marked with the mold compound used for its lot, and this identification remained visible throughout the DOE testing. The parts were pass-fail tested at room temperature in Singapore and then shipped to National in Santa Clara for preconditioning (see *Figure* 6, Precondition Flow Sequence for 68L-PLCC) and base-line, zero-hour electrical testing. Refer to the National Semiconductor Final Report for High Lead-Count Stress and Electrical Testing in Documentation, Section 7.

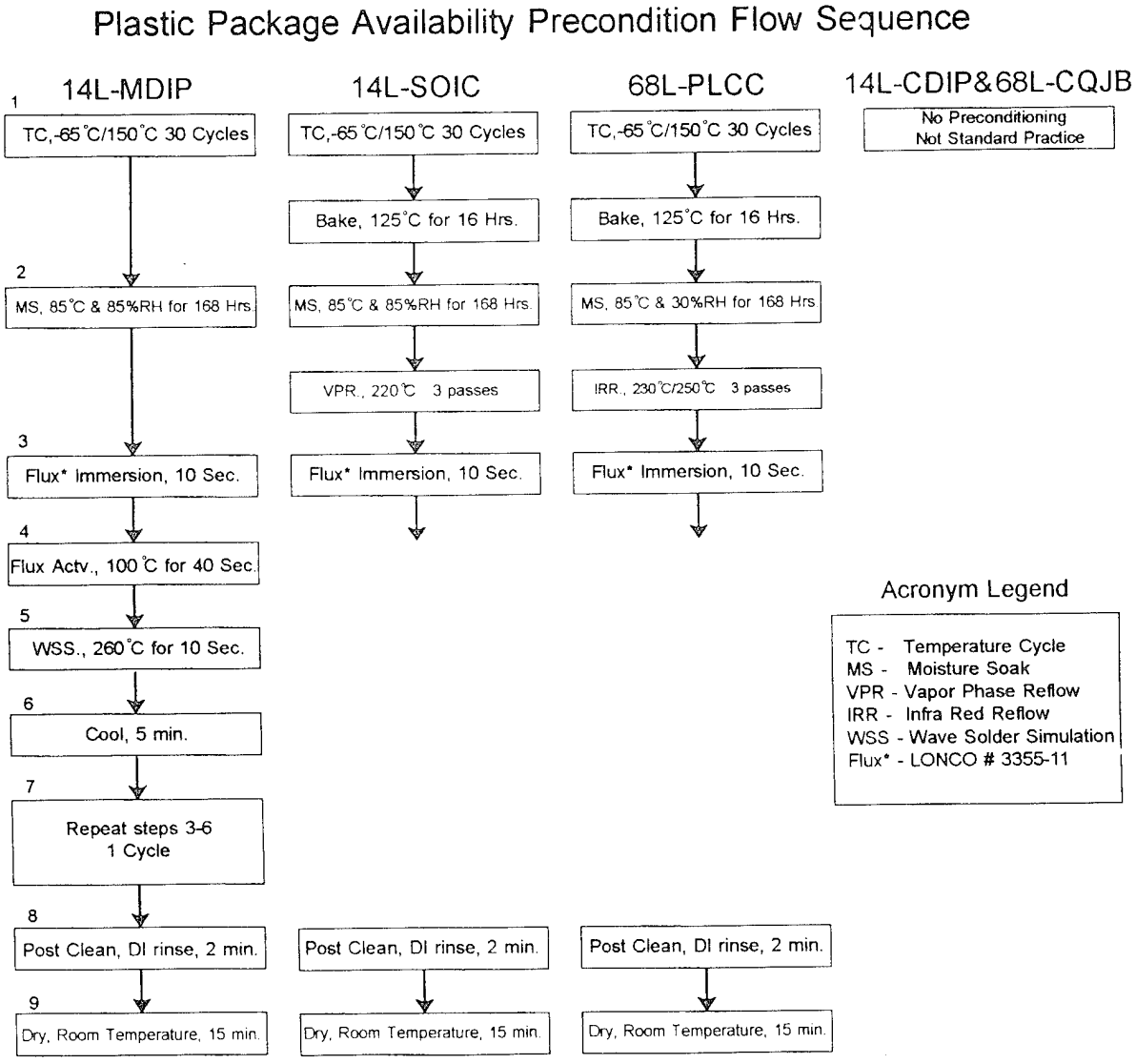


Figure 6

Task 6.0 RWOH Coating of Test Devices (best-effort, National & Honeywell)

This task was officially dropped for budgetary reasons when the PPA program was re-started with reduced funding. Since National, Dow Corning and the DoD had an interest in chip coating technologies to improve plastic device reliability, and had demonstrated a successful assembly level coating in the RWOH (Reliability With-Out Hermeticity) program, funded by the USAF- Wright Development Laboratory, work was continued on a best-effort basis.

Subtask 6.1 Mask Design (National)

National designed and fabricated several pad definition and pad opening masks for the SCX6244 wafers. These were used to define gold pads on top of the aluminum pads of finished wafers, and openings in the Dow Corning coatings which were applied after the gold pads were formed.

Subtask 6.2 Coating of Test Devices (National & Dow Corning)

SCX6244 wafers (150 millimeters diameter, intended for ceramic-hermetic packaging, sans the organic stress relief coating normally applied to wafers intended for plastic encapsulation) were processed to the flow in Table 1.

RWOH Wafer Level Coating Process Flow

1.	Noble Metal Deposition	NiV / Au 1kÅ / 2kÅ	National
2.	Pattern Bond pad	Mask & Etch (wet)	National
3.	Hermetic Coat Deposition	FOx / SiC 10kÅ / 5kÅ	Dow Corning
4.	Open Bond pad	Mask & Etch (dry)	National

Table 1

Preliminary salt spray tests run on the coated die from sawed wafers were negative. In several minutes considerable bond pad corrosion had initiated. Also, many of the bond pads appeared to have contamination on them. Further processing was terminated at this point. Analysis showed possible incomplete pad etch in step 4 above. Also, it was determined that the 2000 angstroms of evaporated gold was insufficient for adequate corrosion protection, and auger analysis did show discontinuous gold regions. It is thought that 5000 angstroms would be a better thickness for future efforts. Please see the Dow Corning Final Report (Section 5), subsection 1.0, RWOH Coating of Test Devices for further detail.

Task 7.0 Device Reliability Testing

In planning the DOE shown in *Figure* 2, there was concern on how to meet the time and budget allocation for the task, yet cover the major issues at hand... i.e., how do PEM perform in harsh military-like environments? It was desirous to study both a large and small chip, since stress issues are usually only a concern on larger chips. Also, since the original program proposal in 1992, the interest in surface-mount technology (SMT) had increased significantly, so a small SOIC SMT device was added for comparison, to the already planned, small, 14L through-hole-mount device, and 68L-PLCC SMT.

In addition it was commonly believed among the PPA team that preconditioning (board assembly simulation), was necessary for rating and grading SMT devices and should be done prior to any qualification life-testing; however, there was not agreement on the need to precondition through-hole devices, since the plastic body of the device is shielded from the heat of the solder bath by the printed circuit board during solder reflow. Further, it was suggested by Peter Brooks of Harris, that voltage was also a significant accelerating factor in PEM HAST performance, and should be looked at. Finally, it was desirous to evaluate several mold compound variables also, such as ionic getters and the use of ultra-clean starting resins.

So the "demand" side of the DOE, determining resources needed, contained questions about chip size, board-mount technology, preconditioning, bias-voltage, and mold compound variables in addition to the various accelerated environmental tests that would be used to differentiate between these variables. On the resources available "supply side", there were concerns about the number of devices needed to populate the test-cells, the expense of HAST and burn-in boards, the availability of test chambers for long periods of time (up to 1 yr.), how many devices (sockets and boards) could be put in the HAST and burn-in chambers, time-to-test each device, tester availability and engineering test-program support. In addition, logistics between environmental test location and electrical read-out tester location needed to be comprehended in the schedule, i.e., it had been planned to perform environmental test at Dow Corning on the HLC devices and electrical read-out test at National, to take advantage of available facilities at each.

Subtask 7.1 Test Plan Definition (All)

The PPA DOE is shown in *Figure* 2. The "Accelerated Reliability Life Test" plan is shown at the bottom of the *Figure*. LM124 linear quad op-amps were used for the LLC leg of the DOE whereas a digital circuit using the SCX6244 gate array chip was used for the HLC leg. The LM124 is a 62X60 mil sqr. chip and the SCX6244 is a 259X262 mil sqr. chip.

The LM124 chip is small enough that the stress relief coating often applied to wafers of larger chips is not required. The SCX6244 wafers intended for plastic do have the stress relief coating. The HLC ceramic control units came from wafers without the polyimide organic stress-relief

coating, so to be rigorously correct, *Figure* 2 should show different wafers (same product chip) above the HLC control leg.

The B_ compounds are National's standard production plastic, while the 3400 & ULS12H are Plaskon's standard plastic for these type packages, and the X compounds represent hi-rel versions using ultra-pure resins and ionic-getter additives. All of the SOICs were preconditioned prior to life-testing, whereas splits were made for the MDIP and PLCC packages. The SOIC HAST legs contain the voltage split, with 5 and 30 volts representing the specification sheet extremes for operating bias of the linear quad op-amp.

The choice of using two HAST temperatures was driven by several considerations. The first was that the RWOH coated devices were not expected to have appreciable failures at reasonable test duration times and normally used HAST temperatures, based on results from the RWOH program; accordingly, it was decided to use the maximum nominal chamber operating temperature of 159 °C. The second was that it was desired to run two different HAST temperatures so that activation energies could be calculated (with the condition that the failure mode/mechanism be the same). Since there was controversy over the use of a temperature in the range of the glass transition temperatures of the mold compounds being used, it was decided a second temperature should be run as a backup, and at a value more accepted and used by industry, thus 130 °C was also chosen.

Please see Crane's Final Report, Section 6, for LLC Stress and Electrical Testing, and National's Final Report for HLC Stress and Electrical Testing, Documentation, Section 4, for detail on the test quantities and readout points.

Subtask 7.2 Benchmark and Reliability Testing (Crane, Dow Corning & National)

Numerous problems were encountered in conducting the "Accelerated Reliability Life Testing" shown in the PPA DOE of *Figure* 2. Dow Corning's initial receipt of HAST test boards had incorrect "low-temp" passive components which failed during the first week of 159 °C testing, so the boards had to be retrofitted with properly rated components, thus delaying the program about a month. Devices tested at 159 °C on HAST required extra cleaning and scraping prior to electrical testing to remove lead contamination build-up. Eventually this caused several external leads to fall off during testing or handling on both the surface-mount LLC and HLC devices.

Scheduling the tester at National and achieving fast turn-around times for the HAST and Temp Cycle (TC) HLC devices sent from Dow Corning for test and return, often took as much as two weeks against a plan target of 1 wk. Crane miscalculated the amount of test time per device that it would take their tester to test the large number of LLC linear devices (several minutes per device). Tests other than HAST produced no, or very few, failures for the life-test time that was available in the program schedule.

Subtask 7.3 Moisture Correlation Tests (Crane, Dow Corning & Sandia)

Several units each of the NAT-01 sensor chip, assembled in the same package outline and with the same mold compounds as the product test units were included in the HAST tests for both the LLC and HLC devices. These devices were baseline tested at Sandia prior to being sent to Crane and Dow Corning for the LLC and HLC HAST testing respectively. Both Sandia in Section 3 and Dow Corning in Section 5 report on the NAT-01 sensor testing.

Task 8.0 Device Reliability Analysis (Honeywell)

Subtask 8.1 Reliability Prediction Methodology

Honeywell reports on and documents their reliability prediction methodology for both PEM and ceramic-hermetic devices used in their avionics guidance business. This is covered in Honeywell's Final Report (Section 8), in their Appendix C.

Subtask 8.2 Assessment of Fielded Systems

This task was to assess and compare PEM and hermetic failure data from Honeywell avionics fielded systems by collecting and analyzing this data. Honeywell's Final Report (Section 8) focuses mainly on this task, i.e., documenting field reliability experience. Honeywell compares resulting field failure rates between plastic and hermetic devices as well as comparing the results against predicted failure rates. Factors influencing the failure rates such as derating and thermal environment are also discussed. The equipment studied operated in a commercial airborne equipment bay environment where:

1. normal ambient temperature was 18°C to 38°C
2. average part ambient temperatures are on the order of 50 °C
3. semiconductor junction temperatures under normal conditions are < 85 °C
4. " " " maximum " " < 110 °C

Seven LRUs are included in the study and the data includes a breakout of part type categories for digital , linear, memory, and microprocessor. The time period covered was 1989 through 1994. Total equipment operating hours ranged from 668,000 hours for LRU 3 to almost 10 million hours for LRU 7, reference Table 4.1.1, Total LRU Equipment Operating Hours, in Section 8.

Task 9.0 Plastic Usage Specification (Plaskon)

The original goal of this task was to develop a set of military specifications by selecting and testing a number of commercially available epoxy mold compounds (EMC's), or near commercially available, with only minor modifications allowed. This was later amended in the restart program to "a set of specification guidelines".

Subtask 9.1 Materials and Testing Specification

In fulfilling this task, Plaskon recommends specifications for the three general types of mold compounds studied in this program, i.e., standard, low stress and anti-popcorn. These in-turn are each divided into two sub-types: Type 1 with several special requirements for conventional molding using large (many units) cavity dies requiring long injection feeder runs and Type 2, for automated gangpot (small dies) with short feeder runs. These are shown in Table 2, "ECM Specifications".

Task 10.0 Technology Transfer (All)

Subtask 10.1 Information Dissemination Reviews

Five successive reviews at JC13 packaging technology meetings were given at various locations as shown in *Figure* 1, PPA Program Schedule (under line item no. 37, Task 10), with published handout material furnished and also mailed to various interested parties as documented in the monthly R&D reports, "Trip Report" section. Typical attendance at these reviews was 35-75 technologists, mostly from the Mil/Aero industry. National typically had 2-4 technologists representing the PPA program at these reviews. Three (3) government steering committee workshops were also held, one at National, Santa Clara, CA, one at Plaskon, Springhouse, PA and one at DESC, Dayton, OH.

Subtask 10.2 Information Dissemination Conferences

Information was disseminated at three conferences including the Advanced Technology Acquisition, Quality and Reliability Workshop (5 papers presented), in Newport Beach, CA, (8/95), and the Standard Hardware Acquisition and Reliability Program (SHARP), in Indianapolis, OH, for the 6 month re-start review, (11/94), and the program final review, (11/95). Also, reviews given (or planned) but not shown in *Figure* 1, were at NEPCON SE, '95 in Orlando, FL, (11/95) and Defense Manufacturing Conference (DMC), in Dallas, TX, (11/95) and tentatively NEPCON West '96, in Anaheim, CA, (3/96)

EMC Specifications

				Standard		Low Stress		Anti-popcorn	
Property	**Method**	**Conditions**	**Units**	**Type 1**	**Type 2**	**Type 1**	**Type 2**	**Type 1**	**Type 2**
				Limits	**Limits**	**Limits**	**Limits**	**Limits**	**Limits**
Moldability									
Spiral flow.	SEMI G11	175C/1000 psi	cm	35-75	60-125	35-75	60-125	35-75	60-125
Ram Follower Gel Time	SEMI G11	175°C/1000 psi	seconds	8-12	10-25	8-12	10-25	8-12	10-25
Hot Hardness	Shore D	175°C (90 sec.)		≥ 60	≥ 60	≥ 60	≥ 60	≥ 60	≥ 60
Flash & Bleed	SEMI G45	175°C/1000 psi							
2 mil Channel			mm	≤ 20	≤ 20	≤ 20	≤ 20	≤ 20	≤ 20
0.25 mil Channel			mm	≤ 5	≤ 5	≤ 5	≤ 5	≤ 5	≤ 5
Thermal Properties									
CTE	SEMI G13	Post cure							
Alpha 1		4 hrs/ 175°C	ppm/°C	≤ 26	≤26	≤ 18	≤ 18	≤ 18	≤ 18
Alpha 2			ppm/°C	≤ 80	≤ 80	≤ 65	< 65	≤ 65	< 65
Glass Transition Temp. (Tg)			°C	≥ 140	≥ 140	≥140	≥ 140	≥130	≥ 130
Stress Index						≤ 35	≤ 35	≤ 50	≤ 50
Flammability	UL-94	1/8" thickness		V0	V0	V0	V0	V0	V0
Physical Properties									
Flexural Strength	D790	Room temp.	Kpsi	≥ 16	≥ 16	≥14	≥14	≥18	≥18
Flexural Modulus	D790	Room temp.	Mpsi	≤ 3.5	≤ 3.5	≤ 2.0	≤2.0	≤ 4.0	≤4.0
Flexural Strength	D790	215°C	Kpsi					≥1.0	≥1.0
Flexural Modulus	D790	215°C	Mpsi					≤ 150	≤150
Specific Gravity	D792			1.5-3.0	1.5-3.0	1.5-3.0	1.5-3.0	1.5-3.0	1.5-3.0
Ash content		650°C	%	65-85	65-85	65-85	65-85	75-90	75-90
Viscosity		175°C/1000 psi	poise	≤ 300	≤ 300	≤ 100	≤ 100	≤ 200	≤ 150
Electrical									
Dielectric Constant	D149	1 KHz/room temp		≤ 5.0	≤ 5.0	≤ 5.0	≤ 5.0	≤ 5.0	≤ 5.0
Dissipation Factor	D149	1 Khz/ room temp		≤ 0.010	≤ 0.010	≤0.010	≤ 0.010	≤0.01	≤ 0.010
Volume Resistivity	D257	Room temp.	W-cm	$\geq 10^{14}$	$\geq 10^{14}$	$\geq 10^{14}$	$\geq 10^{14}$	$\geq 10^{14}$	$\geq 10^{14}$
Analytical									
Moisture absorption		85°C/85RH/168 hr	%	≤0.60	≤ 0.60	≤0.60	≤ 0.60	≤0.30	≤ 0.30
Water Extract Conductivity	SEMI G29	48 hrs/121°C	μ mhos/cm	≤ 150	≤ 150	≤ 150	≤ 150	≤ 150	≤ 150
pH of Extract				3.5-7.5	3.5-7.5	3.5-7.5	3.5-7.5	3.5-7.5	3.5-7.5
Extractable Sodium			ppm	≤ 50	≤ 50	≤ 50	≤50	≤ 50	≤50
Potassium			ppm	≤ 50	≤ 50	≤ 50	≤ 50	≤ 50	≤ 50
Chlorine			ppm	≤ 25	≤ 25	≤25	≤25	≤25	≤25
Bromine			ppm	≤ 25	≤ 25	≤ 25	≤25	≤ 25	≤25
Iron			ppm	≤50	≤ 50	≤ 50	≤50	≤ 50	≤50
Total Antimony	Xray Fluorescence		%	≤ 2.5	≤ 2.5	≤ 1..0	≤ 1..0	≤ 1..0	≤ 1.0
Total Bromine	Xray Fluorescence		%	≤ 1..0	≤ 1..0	≤ 2.5	≤ 2.5	≤ 2.5	≤ 2.5

Table 2

Task 11.0 Program Management

Subtask 11.1 Program Management

A revised Contract Management Plan, CDRL item A014, was submitted to the DLA contracting program office. All provisions of that plan have been complied to in that National Semiconductor has managed and coordinated the efforts of the PPA program, and has assured compliance with government regulations and procedures through requirements set forth in National's internal Standard Operating Procedure (SOP) 1-472, Procedures for Government Technology Business Unit Contracts. The remaining items of this subtask, i.e., timely submission of reports, dissemination of information gained, and assignment of a single program manager reporting directly to the DLA program Contracting Officer's technical representative (COTR) on technical matters and Contracting Officer for contract matters have been met as reported on in Task 12.0, Subtask 11.2, and Task 10.0 of this final report.

Subtask 11.2 Key Personnel

Key personnel were constant for the duration of this program with the exception of the program manager position, which was revised with due notification and authorization, at the time of re-start. This change was necessary due to re-assignment of John Jackson, the original program manager, during the hold status mid-way in the program. Ron Kovacs of National's Package Technology Group managed the program from the time of re-start in May of '94 with support from Dr. Bob Byrne of the Government Technology Business Unit (GTBU). Drs. Randy Lo and Luu Nguyen, also of the Package Technology Group, acted as program technical advisers for the duration of the program. Dennis Ralston of GTBU was the contracting officer and administrative point of contact for the program.

Task 12.0 Data Items

This task was divided into 13 subtasks in the contract management plan, technically 12.1.1 through 12.1.13. For brevity, only the ongoing activity of preparing monthly financial and technical reports are expanded on below, and are shown in the PPA Program Schedule (*Figure* 1), as subtasks 12.1 and 12.2. For completeness; however, the 13 subtasks have been delivered (this final report and it's presentation at the November SHARP conference in Indianapolis complete the list), and include: 12.1.1, Program Plan; 12.1.2, Functional Test Plan; 12.1.3, Functional Test Report; 12.1.4, Material Specification; 12.1.5, Process Specifications; 12.1.6, Reliability Test Plan; 12.1.7, Reliability Test Report; 12.1.8, Technology Transfer Plan; 12.1.9, Funds and Man-hour expenditure Report (monthly); 12.1.10, R&D Status Report (monthly); 12.1.11, Contract Funds Status Report (quarterly); 12.1.12, Scientific and Technical Report (final); and 12.1.13, Presentation Material.

Task 12.1 Monthly Financial Reports (National)

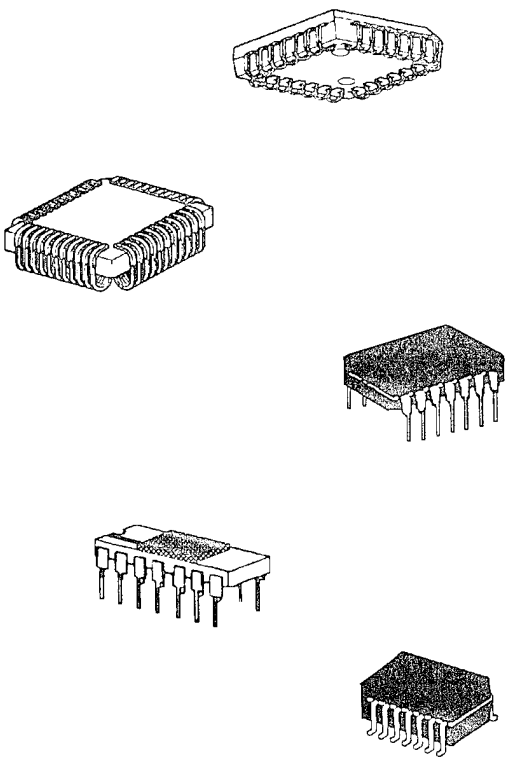
Monthly financial reports have been submitted by National's Government Technology Business Unit detailing expenditures for labor, materials, outside services, subcontractor payments and overhead, in a timely manner to the DLA contracting program office, throughout the performance of the PPA contract.

Task 12.2 Monthly R&D Reports (National)

A total of 25 monthly R&D reports have been submitted to the DLA program office as well as the PPA government steering committee and other designated government persons, in a timely fashion, during the active duration of the PPA contract.

PLASTIC PACKAGE AVAILABILITY PROGRAM

RESULTS



RESULTS

Task 4.0 Moisture and Corrosion Test Chip Development (Sandia)

The NAT-01 moisture sensor with the porous silicon technology did react to moisture, and gave readings to suggest that it may be effective as a pin-hole detector on passivated die. It also was capable of surviving 300 °C for 4 hours in three different ambients, air, N2 and vacuum and remained functional, which indicates that it could withstand most assembly high temperature processing.

The corrosion sensor , which is not new technology, but is desirable to have on the same chip with the moisture sensor, was quite effective in predicting early fails; however, correlation with product failures by mold compound, was mixed between tests run at Sandia, Crane and Dow Corning. This could be due in part to the small sample sizes used for the sensor. See Sandia's final report (Section 3), for a full discussion and data on the NAT-01. Also, it should be noted, that the 100mil X 100mil square chip when put in the relatively large PLCC and CQJB package outlines, results in long wire lengths which violate the construction design rules (wire sag and mold sweep). This was waived (and did not appear to cause a problem), in order to get sensor data in these package types. Sandia intends to make this chip available commercially.

The ATC04 was effective in distinguishing between stress levels for the various mold compounds on finished devices as well as stress changes from assembly processing steps and post assembly preconditioning steps. *Figures* 27 and 28 in Sandia's Final Report (Section 3), displays this data. The ATC04 has proven to be an excellent stress monitor for PEM. Sandia offers this sensor chip commercially.

Task 7.0 Device Reliability Testing (Crane, Dow Corning and National)

Radiation Testing : As part of the reliability testing program, 14L-MDIP LM124s were submitted for radiation testing. The results were similar to those previously obtained for ceramic LM124s. There were no parametric electrical failures up to 100K Rads total dose level. Parametric failures occurred between 100K and 150K Rads. Functional failures occurred above 200K Rads.

Accelerated, Harsh Environment Life-Testing: The results from over 6 months of accelerated environmental stress testing generated a total of 287 failures for 1855 total devices tested, including the ceramic control units. The breakout for ceramic and plastic results, between the various stress tests, are given in Table 3. The tests were designed to generate failures and make distinction between the variables included in DOE, i.e.,

voltage, mold compounds, and HAST temperatures, in a time period consistent with the program schedule and budget. To accomplish this some of the test conditions were beyond the recommended operating ranges of the plastic devices (see *Figure* 10 in Documentation, Section

4), and this strategy worked quite well for HAST, but to a much lesser degree for the other tests, as can be seen in Table 3, with relatively few failures in the non-HAST tests. As can be seen with only 2/300 total failures for all tests combined, the hermetic-ceramic units provided effective control vehicles, verifying good silicon starting chips, and providing a baseline for the test methods, procedures and handling. The numbers that were summed to make Table 3 came from the Master Failure Analysis Chart, *Figure* 12.

DOE RESULTS (fails/total tested)

	Totals		HAST 130 °C	HAST 159 °C	TC -65 °C / 150 °C	HTS 175 °C	OPL 125 °C
CERAMIC	2/300	0.7%	1/52	0/54	1/75	0/95	0/24
PLASTIC	285/1555	18%	79/280	190/285	12/444	4/426	0/120

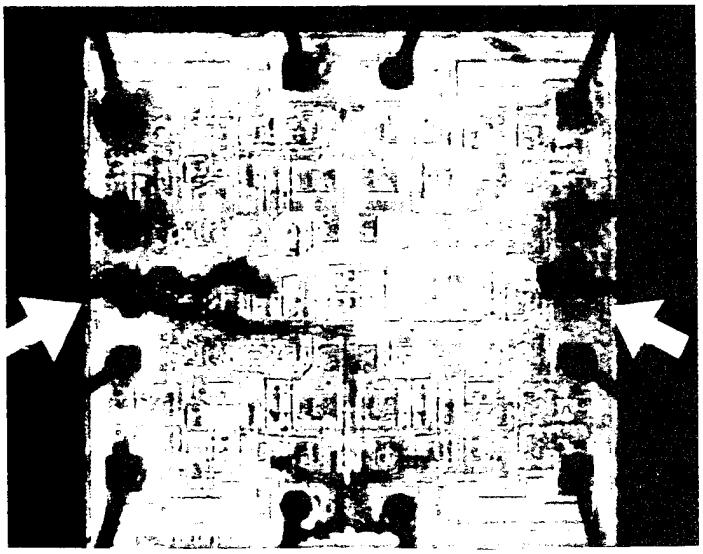
Table 3

The analysis of the DOE results are given in graphical representation, *Figures* 17-37. Key excerpts from the Failure Analysis Report (Section 9), are given in *Figures* 7-11. These analysis and excerpts form the supporting basis for the conclusions and recommendations derived from the Device Reliability Testing task of the PPA program.

Figure 7 shows gross corrosion on the bondpads and circuit metalization of a failed LLC plastic unit after 216 hrs. of HAST. This corrosion is typical of the most prevalent failure mode experienced on the LLC devices and is related to moisture, further accelerated by: temperature as shown in the graphs of *Figures* 17, 18 and 20 (for DIPs & SOICs @ 130 °C vs. 159 °C), preconditioning as shown in *Figure* 19 (for DIPs w/precon vs. no-precon) and voltage as shown in *Figure* 21 and 22 (SOICs @ 5V vs. 30V). This corrosion on the LLC LM124 devices was most advanced on the power and ground leads (pins #4 & #11), but occurred on other pads also. The shorter lead-length paths from the package sides (pin #s 3-5 and 10-12) typically had more corrosion (started earlier) than the end pins of both 14-lead SOIC and DIP packages. This suggested that the interface between the lead-bondwire-bondpad and mold compound was the primary moisture ingress pathway. This was further supported by Dye-Penitrant analysis performed by Rome Labs on one of the SOIC devices, shown in *Figure* 13, (also reference Rome Final Report, Section 7).

Figure 8 shows bondpad corrosion of a failed HLC plastic device after 216 hrs. of HAST. The bondpad metalization on the SCX6244 die is aluminum-silicon-copper, compared to pure aluminum for the LLC (this might account for the different appearing corrosion between the LLC and HLC devices; also the LLC corrosion appears more severe). This corrosion was the most prevalent failure mode identified in the HLC failures and again is related to moisture, accelerated by temperature, as shown in *Figure* 30 (PLCCs @ 130 °C vs. 159 °C), and preconditioning as shown by comparing *Figures* 30 & 31 (PLCCs w/o & w/preconditioning).

Corrosion
HAST 159°C @ 216 hrs
14 L SOIC DLA-05
3400 # 19 30 Volts



SEM & EDS Data
Corrosion
HAST 159°C @ 216 hrs
14 L SOIC DLA-05
3400 # 19 30 Volts

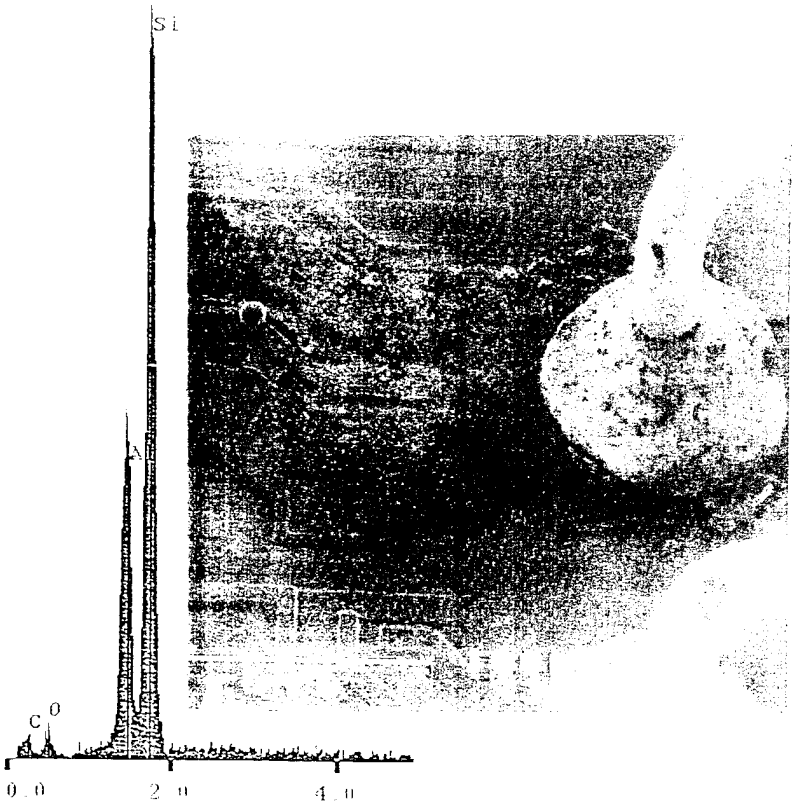
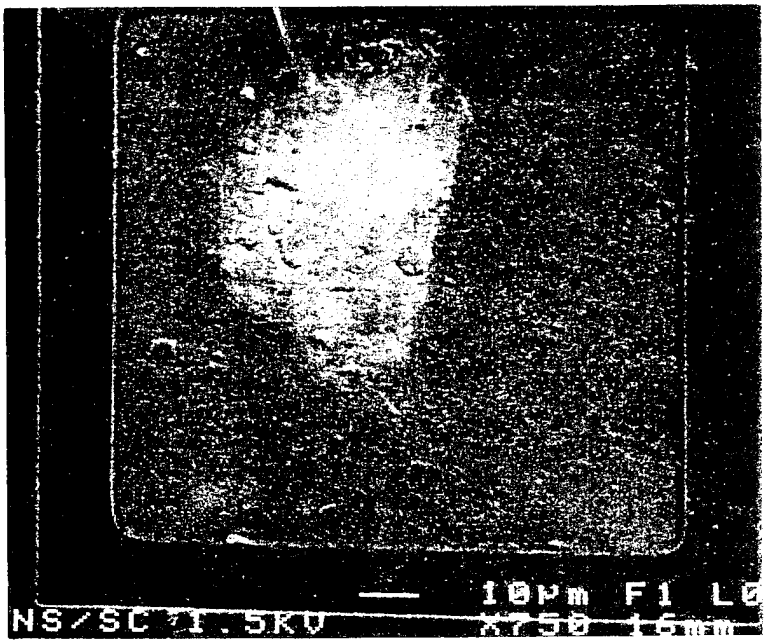
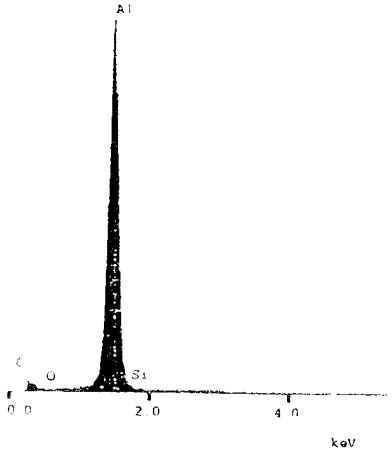


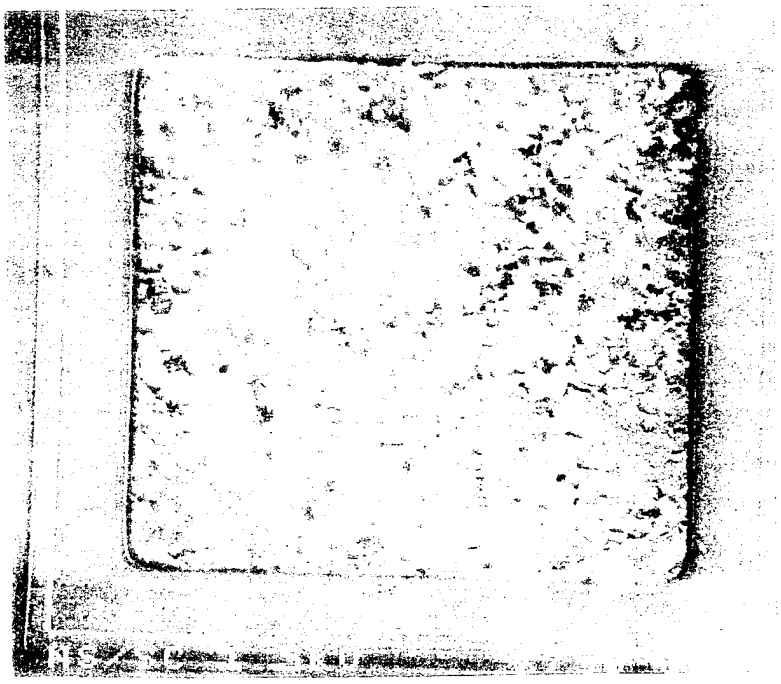
Figure 7

Taken from F/A report, Section 9. Shows gross corrosion on bond pads and circuit metallization after 216 hrs. of HAST at 159°C.



SEM & EDS Data
"Normal"
aluminum bond pad
unstressed device
(Non-Bonded Pad)





SEM & EDS Data
"Oxidized"
aluminum bond pad
HAST 130°C @ 216 hrs
ULSI2HX preconditioned
(Non-Bonded Pad)

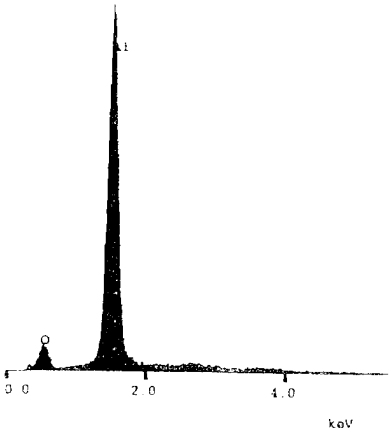


Figure 8

Taken from F/A report, Section 9. Shows corrosion after 216 hrs. of HAST at 130°C.

Also, *Figure* 14 shows a C-SAM photo of a 68L-PLCC before and after preconditioning, from both the top and bottom with delamination observable only on the backside of die paddle (between the mold compound and leadframe). Moisture can accumulate in these delamination-caused gaps and provide a potential source for corrosion.

The second bonds (wire-to-leadframe as opposed to first bond, wire-to-die), typically showed no corrosion. The second bond for the plastic packages involves gold wire-to-silver spot-plated copper and this is a much more inert system, than the gold-aluminum system of the first bond. Corrosion was the most prevalent PEM failure mode for the total DOE.

Figure 9 (top photo), shows evidence of dielectric stress cracking on a HLC plastic device after 2000 temperature cycles. One group only, of compound ULS12H, had any failures, 12/36, as shown in the graph of *Figure* 29, Temperature Cycle of PLCC vs. CQJB (for detail see Master HLC Failure Analysis Chart in Section 9). The LLC plastic had no failures, as shown graphically in *Figure* 24 for Temperature Cycle Performance of LM124 Plastic DIPs vs. SOICs, out to 1512 temperature cycles at which point the test was terminated for time constraints (for detail see Master LLC Failure Analysis Chart in Section 9). Cracks in the corners of the failed large dice topside dielectric passivation were evident when decorated w/KOH etching solution (underlying aluminum circuit traces etched away). Evidence of cracks did not exist for non-failed die from the other HLC TC test compounds, such as the X9074 compound (bottom photo in *Figure* 9). Dielectric stress cracking was 2nd most prevalent failure mode for the total DOE, although only affecting the HLC devices.

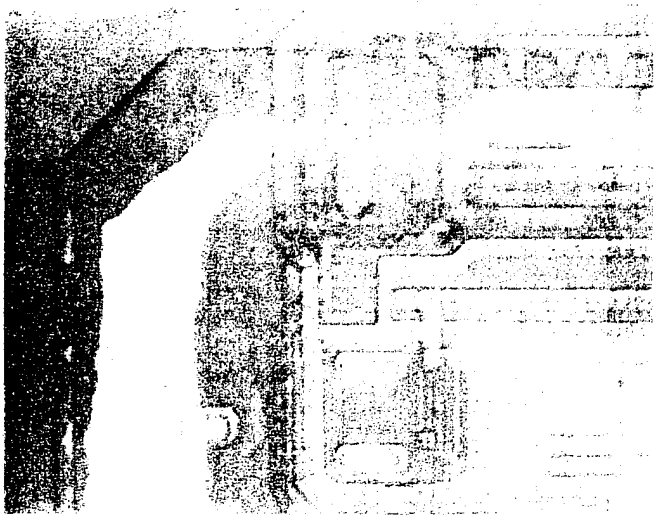
Figure 10 shows the formation of gold-aluminum intermetallic at the gold ball-aluminum bondpad interface of a non-failed HLC device after 4125 hrs. of high temperature storage. No failures were generated by HTS as shown by the graph in *Figure* 25, High Temperature Storage @ 175 °C for PLCC vs. CQJB, for the standard room-temperature electrical readouts; however, when the same devices were tested at 125 °C, 26/47 showed gross-functional failure. The results of the 125 °C test by mold compound showed the X9074 anti-popcorn to be far superior to the other compounds for passing gross functional: (see *Table 4*)

Mold Compound (pass/total): X9074 (16/17); B24 (5/16); ULS12H (0/14); CQJB (42/42) note: these units had no initial baseline testing at hot temperature, but hot testing of the ceramic control units after the 4125 hrs showed no fails, which validates the plastic hot test results.

Table 4

The intermetallic of the gold-aluminum system is known to be brittle, can be accelerated by other contaminants, and grows w/temperature, weakening the bond strengths, as shown in the plots of *Figure* 27, Affect of HTS on Wire Bond Strength in PLCC: PRE HTS vs. Post HTS. A majority of the bond strengths have degraded to, or below the minimum strengths, specified for the gold wire used.

KOH Etch
Passivation Cracks
@ 2000 Temperature Cycles
ULS12H Vss Pin 45



KOH Etch
No Passivation Cracks
@ 2000 Temperature Cycles
X9074 Vss Pin 45

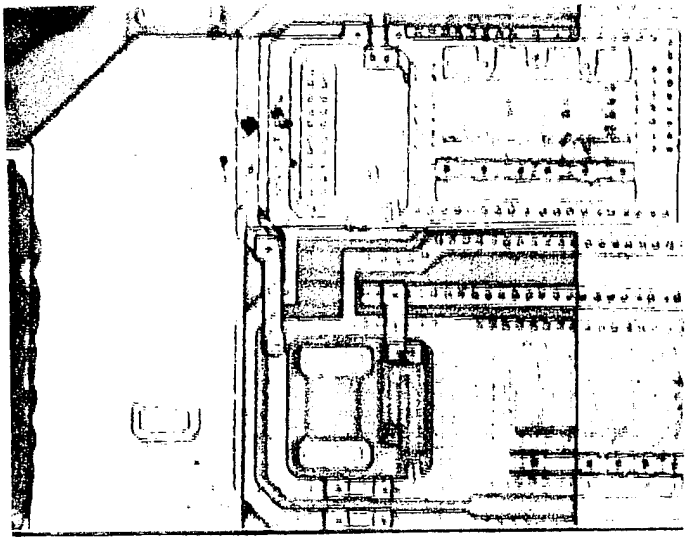


Figure 9

Taken from F/A report, Section 9. Shows evidence of dielectric stress cracking.

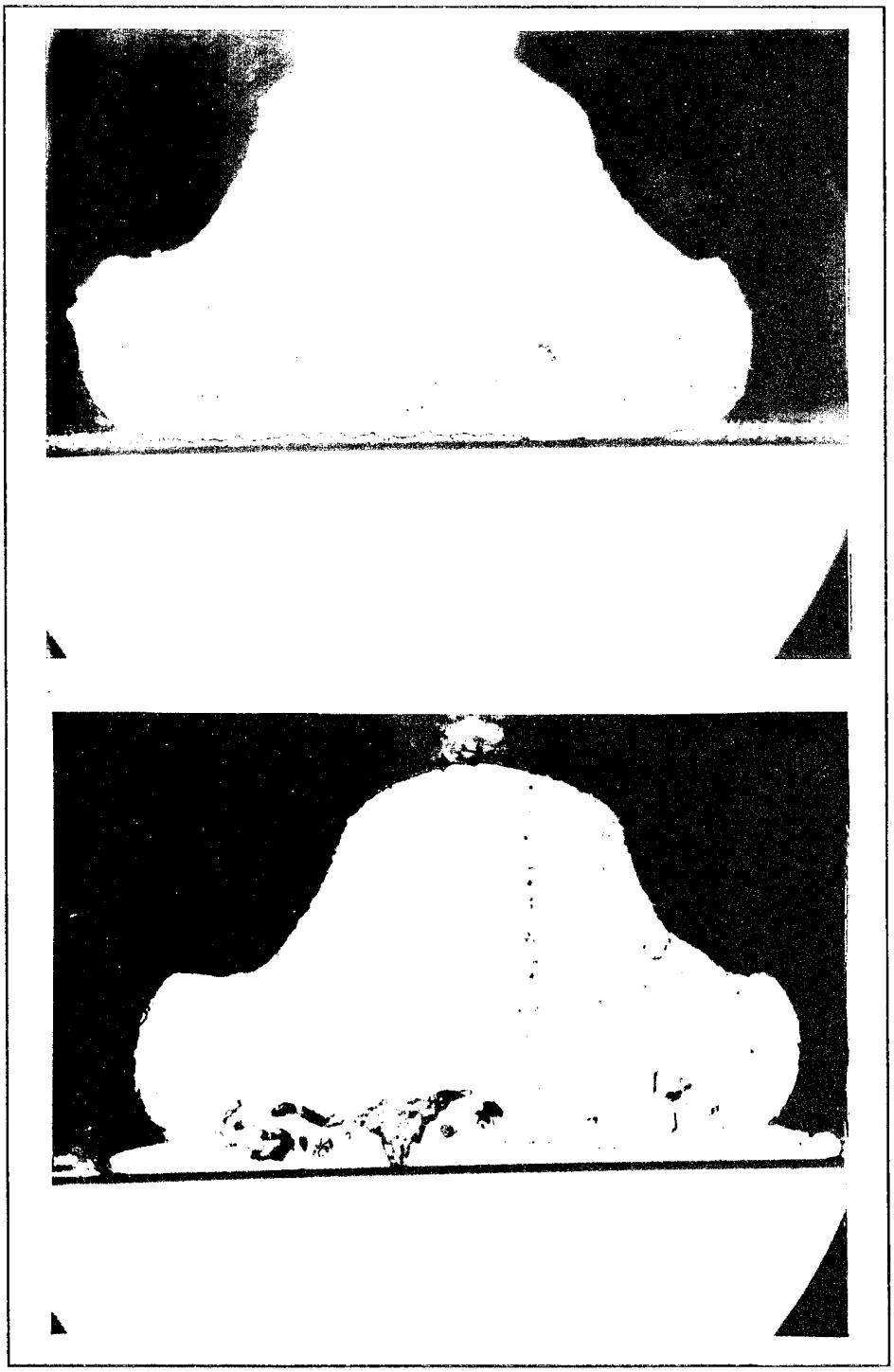


Figure 10

Cross section at 1000X to better show intermetallic (AuxAly) region formed between the gold ball-aluminum bondpad. Top, 0 hr. and bottom, 4125 hr.

Figure 26, Affects of Wire Bond Strength in CQJB: PRE HTS vs. Post HTS, shows plots for the aluminum-aluminum bond strengths of the hermetic-ceramic control CQJB from the HTS test. Although the CQJB bond strengths have somewhat degraded they are still well above the minimum for the aluminum wire used. *Figure* 11 shows a cross-section through this aluminum-aluminum bond system, which is used in most hermetic-ceramic packages, for comparison to the gold-aluminum system of *Figure*10, which is used in most plastic devices. As expected, no signs of an intermetallic are observable in the aluminum-aluminum bond cross-section of *Figure* 10.

Figure 15 shows the "wedge" second-bonds of both the hermetic-ceramic CQJB (aluminum wire-to-gold/nickel/tungsten metallized ceramic) and PLCC (gold wire-to-silver, spot-plated copper leadframe) after 4125 hrs of HTS. Typically no corrosion or bond strength degradation was found on the second-bond structures.

Figure 23, High Temperature Storage Performance of LM124 Plastic ICs: DIP vs. SOIC, shows the few failures (for the room temperature readout testing used, 4/150), that were generated for the HTS for all of the LLC plastic. It was assumed the same intermetallic mechanism existed in these LLC devices and due to time limitations, no 125 °C testing nor further failure analysis was performed.

Figure 28, Operating Life Performance @ 125 °C for PLCC vs. CQJB graphically shows no failures for all HLC tested out to 4000 hrs. This test produced no failures, and thus no distinction between variables, and resulted in learning only that within a warm, dry environment, the large plastic PLCCs did exceptionally well.

Figures 32 and 33, Moisture Performance of Surface Mount Packages at 130 °C and 159 °C respectively, for PLCC vs. SOIC, give additional information for comparing the LLC and HLC devices. Since the 68L-PLCC devices uses a very large, complex chip (SCX6244-4.4K gate array) vs. the relatively small, looser geometry, LM124 in the 14L-SOIC the results are what might be expected with the SOIC outperforming the PLCC on HAST at both temperatures.

Task 8.0 Device Reliability Analysis (Honeywell)

Honeywell's full report with accompanying results, data and statistical treatment of that data is contained in Section 8, Honeywell Final Report. Honeywell includes Appendices A (Component Derating Criteria), B (Practices and Procedures for Using PEM) and C (Reliability Prediction Methodology) to support this main field reliability analysis task. Honeywell concluded that *"The results of (their) study confirm that the approach Honeywell has taken in the use of (PEM) for the commercial avionics environment has maintained product reliability; i.e., the use of (PEM) has not been observed to degrade product reliability in commercial air transport applications."*

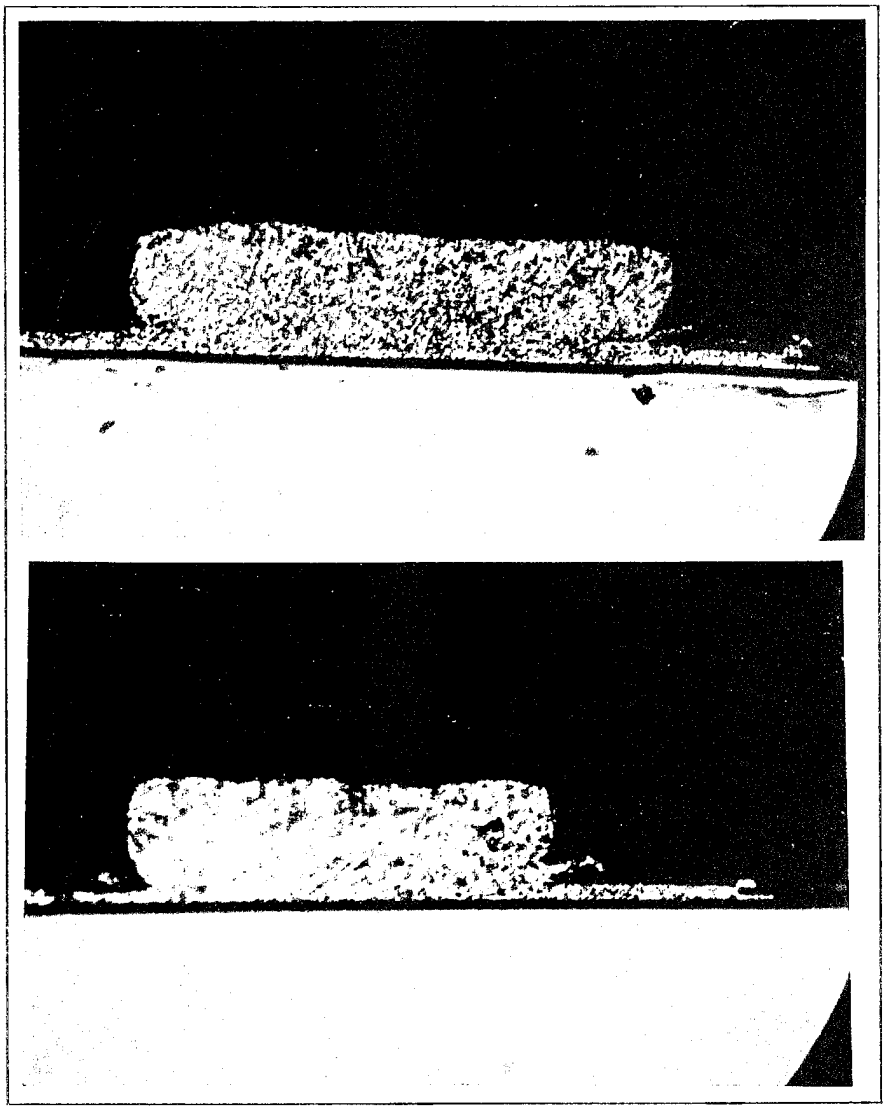


Figure 11

Shows cross-section of aluminum wire bond to aluminum bondpad (for a comparison to Gold Ball-Aluminum Bond Pad cross-section in figure 10) on SCX6244 68L - CQJB, after 0 hr. (top) and 4125 hrs. (bottom) of HTS at 175°C, and lack of intermetallic as expected.

MASTER FAILURE ANALYSIS CHART

= ET failures found in cell

Package	130°C HAST	159°C HAST	TC-65°C/150°C	HTS 175°C	OPL 125°C
 Control 68L CQJB	0/22 @ 1296 Hrs	0/24 @ 648 Hrs	0/25 @ 2000 Cycles	0/45 @ 4125 Hrs	0/24 @ 4000 Hrs
 Preconditioned	22/40 @ 1296 Hrs	44/63 @ 216 Hrs	12/144 @ 2000 Cycles	0/72 @ 4125 Hrs	0/60 @ 4000 Hrs
Non-Preconditioned 68L PLCC	0/60 @ 1296 Hrs	9/42 @ 648 Hrs		0/54 @ 4125 Hrs	0/60 @ 4000 Hrs
 5 Volts	1/45 @ 1080 Hrs	29/45 @ 648 Hrs	0/150 @ 1512 Cycles	0/150 @ 1512 Hrs	Not Performed
30 Volts 14L SOIC	30/45 @ 1080 Hrs	39/45 @ 216 Hrs			
 Preconditioned	25/45 @ 1080 Hrs	39/45 @ 216 Hrs	0/150 @ 1512 Cycles	4/150 @ 1512 Hrs	Not Performed
Non-Preconditioned 14L DIP	1/45 @ 1080 Hrs	30/45 @ 648 Hrs			
 5 Volts	0/15 @ 1080 Hrs	0/15 @ 648 Hrs	1/50 @ 1512 Cycles	0/50 @ 1512 Hrs	Not Performed
Control 30 Volts 14L CERDIP	1/15 @ 1080 Hrs	0/15 @ 648 Hrs			

Cum Failures / Total Sample Size @ Cum Hours

Corrosion | Cracks | Intermetallic

Major Failure Mode Distribution

Figure 12

The color shows the degree of concern (severity) for the 3 types of PEM degradation failure mechanisms generated in the DOE.

Moisture Paths and Contamination Sources In PEM Structure

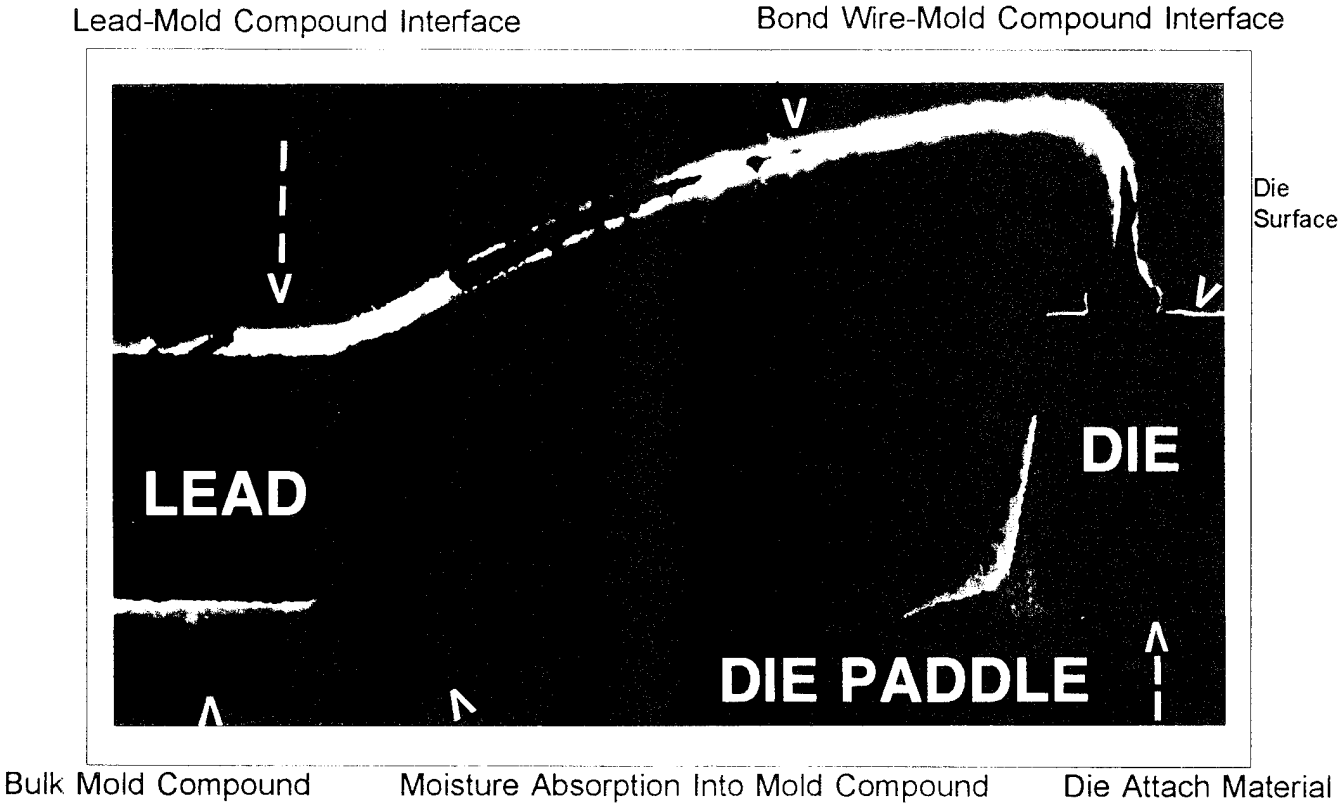


Figure 13

Shows complex materials and interfaces, comprising the structure of the LM124 14L - SOIC. These interfaces and materials can provide paths and sources for moisture and contamination during the life of the device.

National Semiconductor

Joint Directors of Laboratories

PLASTIC PACKAGE AVAILABILITY

C-SAM Photo of 68L-PLCC: SCX6244

Preconditioned vs. No-Preconditioned

X9074 Mold Compound

TOP View — NO-PRECONDITIONING — Bottom View

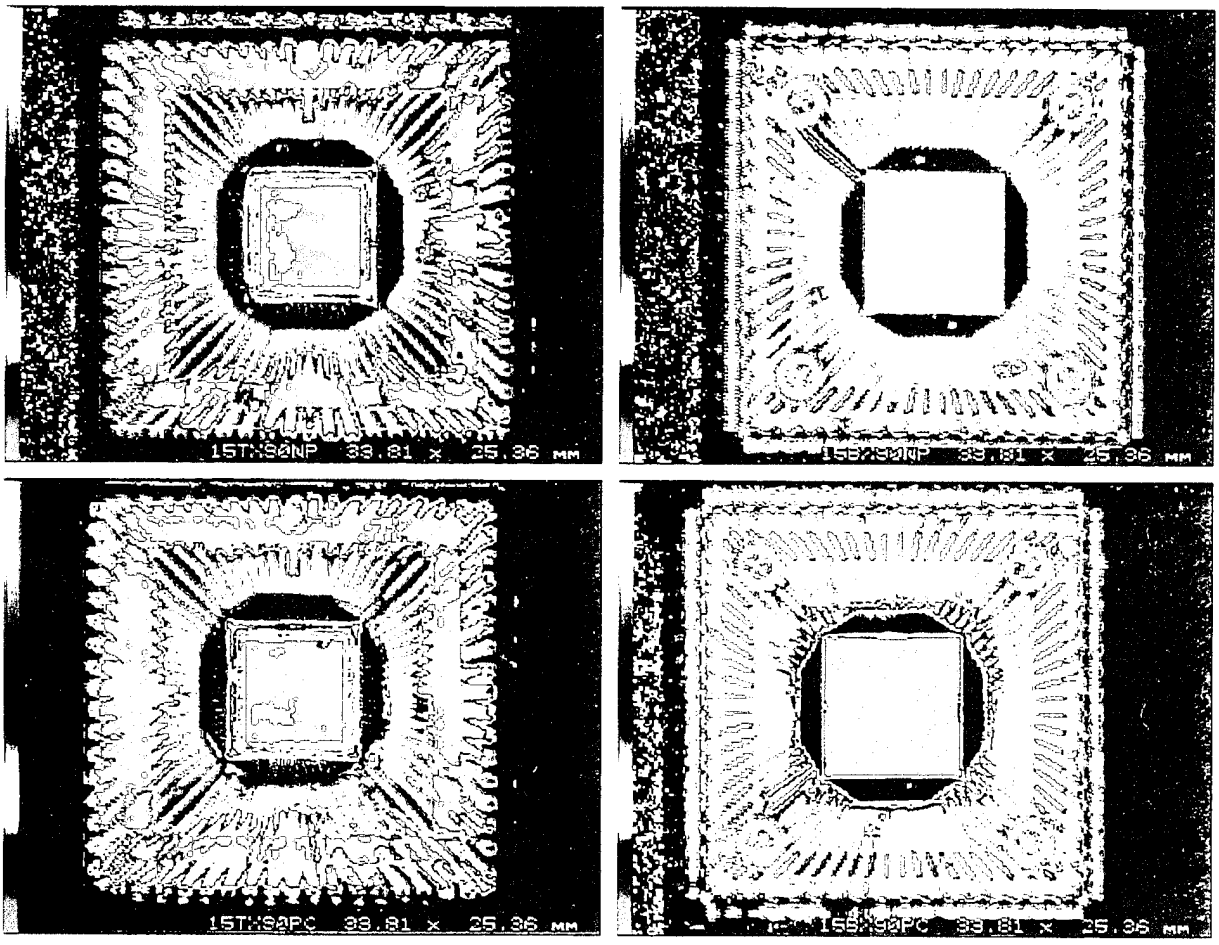


Figure 14

PRECONDITIONED

Shows delamination on the underside of the paddle on preconditioned 68L - PLCC. The Topside appears to be only marginally affected, if at all.



Figure 15

Shows typical 2nd bonds for 68L - CQJB (left) and 68L - PLCC (right) after 4125 hrs. of HTS at 175°C. The Aluminum wire to Au/Ni/W finger in the ceramic CQJB (left) and Au wire to Ag/Cu lead in the plastic PLCC (right) typically showed no corrosion, or bond strength degradation.

A National Semiconductor consideration of the data from a "FITs" (failures in time), perspective and with comments on the system/component failure-rate variability, follows.

Summary and Analysis of the Honeywell Field Reliability Data by National Semiconductor:

This report is a compilation of three separate studies totaling nearly 6.3 billion device operating hours, performed by Honeywell as part of the Plastic Package Availability Program. In this report National summarizes the data compiled by Honeywell and documents the field experience of plastic and hermetic ICs installed in Line Replaceable Units (LRU) manufactured by Honeywell Commercial Avionics Systems. These systems were installed in the equipment bays or cockpits of commercial aircraft, with a normal ambient temperature of 18°C to 38°C, and a high percentage of power-on time. This study compiled the data obtained from over 6.29 billion operating hours.

The First Study consisted of determining the failure rate on LRU 1, 2 and 3. The ICs installed in these LRUs were thru-hole hermetic devices which received burn-in and extended-temperature testing. Most the IC were Mil-Std.-883 compliant.

The Second Study focused on determining the reliability of ICs installed on LRU 4. All the hermetic ICs in this LRU were of thru-hole design. They were 100% screened with burn-in and extended-temperature testing; some of the ICs were Mil-Std -883 compliant. Of the plastic ICs, all were surface mount type; 47% were lot sample screened using burn-in and extended-temperature testing by the manufacturer; 35% received 100% screening by the manufacturer and 18% were not screened.

In the Third Study, the failure rate of LRUs 5, 6 and 7 was determined. All the ICs in these LRUs were in plastic surface mount packages and were 100% screened using burn-in and extended-temperature testing.

The failure rate for three categories of ICs, Digital SSI/MSI, Memory LSI and Linear ICs assembled in the two package types, thru-hole hermetic and surface mount plastic, is shown in Studies 1, 2 and 3. The operating hours and number of failures was reported by Honeywell and the FITs rates were calculated by National.

Results:

In the Digital SSI/MSI device category, see Table 5, the overall failure rate for plastic surface mount ICs screened by burn-in and extended-temperature testing was 60% less than the failure rate for hermetic thru-hole ICs that were screened. However, there was significant variation in the failure rates among the LRUs. Also, the performance of the best hermetic IC was, twice that of the best plastic ICs.

Operating Hours and FITS for Burned-in and Temperature Tested Digital ICs Assembled in Hermetic and Plastic Packages

LRU Number	Device Type	Reported IC Failures	Reported IC Operating Hours	Observed FITS	FITS Ratio for Package & IC Type
1	Digital SSI/MSI Hermetic	3	834,852,000	4	1 X
2	Digital SSI/MSI Hermetic	25	1,098,816,000	23	6 X
3	Digital SSI/MSI Hermetic	6	138,276,000	43	11 X
4	Digital SSI/MSI Hermetic	0	892,000	0	0 X
4	Digital SSI/MSI Plastic	3	53,520,000	56	14 X
5, 6 & 7	Digital SSI/MSI Plastic	9	1,104,549,000	8	2 X
Total	Digital Hermetic	34	2,072,836,000	16	2 X
	Digital Plastic	12	1,158,069,000	10	1 X

Table 5

For the Memory/LSI devices, see Table 6, the overall failure rate for plastic surface mount ICs screened by burn-in and extended-temperature testing was about 30% less than the failure rate for similarly screened hermetic thru-hole ICs. However, there was significant variation in the failure rate among the LRUs. Also, the performance of the best hermetic IC was twice that of the performance of the best plastic ICs.

Operating Hours and FITs for Burned-in and Temperature Tested Memory/LSI Assembled in Hermetic and Plastic Packages

LRU Number	Device Type	Reported IC Failures	Reported IC Operating Hours	Observed FITS	FITS Ratio for Package & IC Type
1	Memory/LSI Hermetic	2	64,773,000	31	1 X
2	Memory/LSI Hermetic	67	257,535,000	260	8 X
3	Memory/LSI Hermetic	6	40,748,000	147	5 X
4	Memory/LSI Hermetic	1	16,948,000	59	2 X
4	Memory/LSI Plastic	1	16,948,000	59	2 X
5, 6 & 7	Memory/LSI Plastic	47	315,864,500	149	5 X
Total	Memory/LSI Hermetic	76	380,004,000	200	1 X
	Memory/LSI Plastic	48	332,812,500	144	1 X

Table 6

For the Linear devices, see Table 7, the overall failure rate for hermetic thru-hole ICs screened by burn-in and extended-temperature testing was nearly four times better than the failure rate for similarly plastic surface mount ICs. There was significant variation in the failure rate among the LRUs.

Operating Hours and FITS for Burned-in and Temperature Tested Linear ICs Assembled in Hermetic and Plastic Packages

LRU Number	Device	Type	Reported IC Failures	Reported IC Operating Hours	Observed FITS	FITS Ratio for Package & IC Type
1	Linear	Hermetic	3	392,236,500	8	1 X
2	Linear	Hermetic	17	1,090,231,500	16	2 X
3	Linear	Hermetic	2	93,520,000	21	3 X
4	Linear	Hermetic	3	69,576,000	43	5 X
4	Linear	Plastic	7	37,464,000	187	23 X
5, 6 & 7	Linear	Plastic	31	663,288,000	47	6 X
Total	Linear	Hermetic	25	1,645,564,000	15	1 X
	Linear	Plastic	38	700,752,000	54	4 X

Table 7

Delimitations:

- The hermetic ICs were installed in older design LRUs which may have impacted the results. The devices in the older LRUs (which used hermetic ICs may be experiencing wear-out, while the plastic ICs in the newer LRUs could be experiencing infant mortality.

- The significant variation in IC reliability performance could account for a major portion of the variation between the plastic and hermetic ICs. Several factors could account for this variability including: The selection of parts and suppliers, the equipment design and location of the equipment.

- It should be noted that all the LRUs in this study were installed in the equipment bays and cockpits of commercial aircraft with a normal ambient temperature of 18°C to 38°C, with a high percentage of power-on time. These environmental conditions may not be equivalent to other operating conditions.

Conclusions:

- The data suggests that burned-in and temperature screened plastic ICs can be used reliably in controlled temperature (18°C to 38°C), protected environments which have a high operating duty cycle.

- There was a significant difference in the performance among various categories of ICs, Digital SSI/MSI, Memory LSI and Linear, and these differences can be exacerbated by package type.

- The reliability of Digital SSI/MSI devices, burn-in and extended temperature screened plastic surface mount ICs was slightly better (60%) than the reliability of similarly screened thru hole hermetic ICs.

- In the Memory LSI device category, the reliability of burn-in and extended temperature screened plastic surface mount ICs was about equal that of similarly screened thru hole hermetic ICs.

- The performance of the Linear devices was another matter. For the Linear IC group, the reliability of burn-in and extended temperature screened hermetic ICs was four times better than similarly screened plastic ICs.

- Looking at the performance among the LRUs, the best hermetic devices out performed the best plastic ICs by two to one in every device category. It should be noted that there was more variation in reliability among LRUs than there was between package types.

Task 9.0 Plastic Usage Specification (Plaskon)

The recommended specification for various types of Epoxy Mold Compounds (EMCs), is given in Table 2. *Figure* 16 shows the three accelerated environmental tests performed. The performance of the various Plaskon test compounds, 3400 and 3400X, for the LLC devices and ULSH12, ULSH12X and the anti-popcorn X9074 is contained in the graphs of *Figures* 17-25 and 28-33. In general, getters and clean starting resins (the 3400X and ULSH12X), performed better for both product and NAT-01 sensor test chips, with the exception of : DIPs at 159 °C HAST, see *Figure* 17, the #34 compound outperformed the #34X, and as shown in *Figure* 21 for 130 °C HAST @ 30 Volts, #34 again significantly outperformed the #34X. These results could not be reconciled, and analysis of the molding compound on failed units did confirm that the mold compound type did match the unit marking. The only other explanation, (other than that the results are valid and the data is identifying a problem source with the "X" compounds), is that the data was mixed in the test lab. This is perplexing, because such a mix-up was discovered and corrected, but it is this "correction" that caused the present unexplainable findings. The tests should be re-run, at least to the first data, point to confirm the results. Please see Plaskon's Final Report, Section 2, for additional test and material analysis results performed at Plaskon.

Summary of Plastic Package Reliability Testing Program

Tests Performed by :

Naval Surface Warfare Center, Crane

DOW CORNING Dow Corning Corporation

National Semiconductor

Figure 16

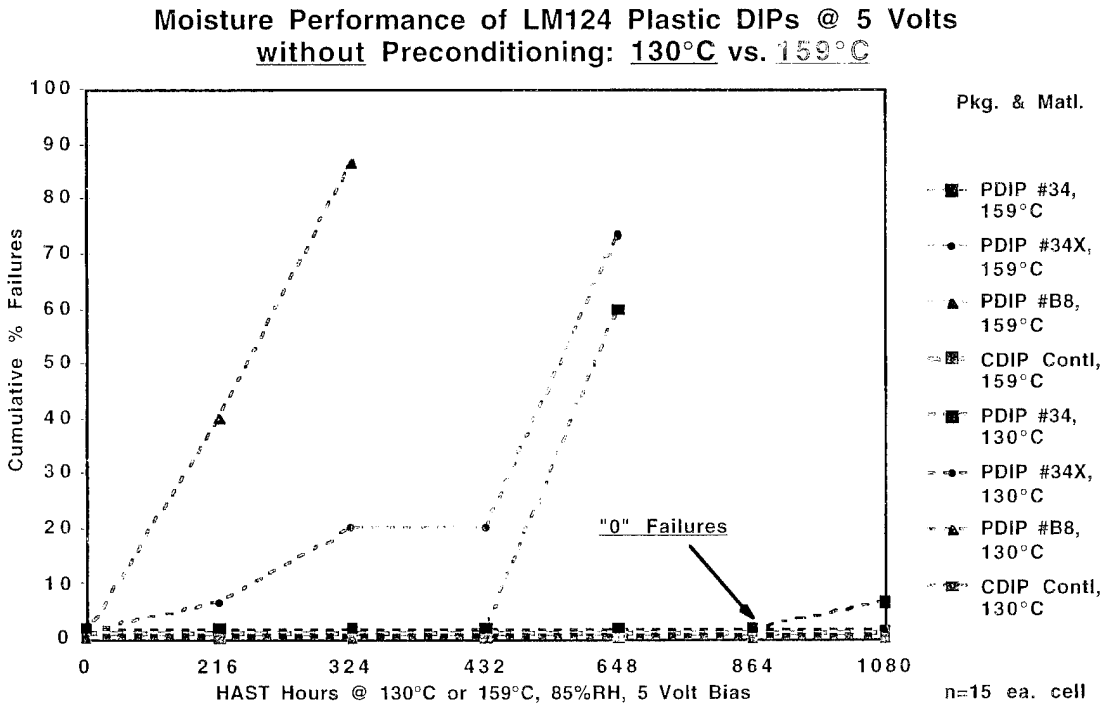


Figure 17

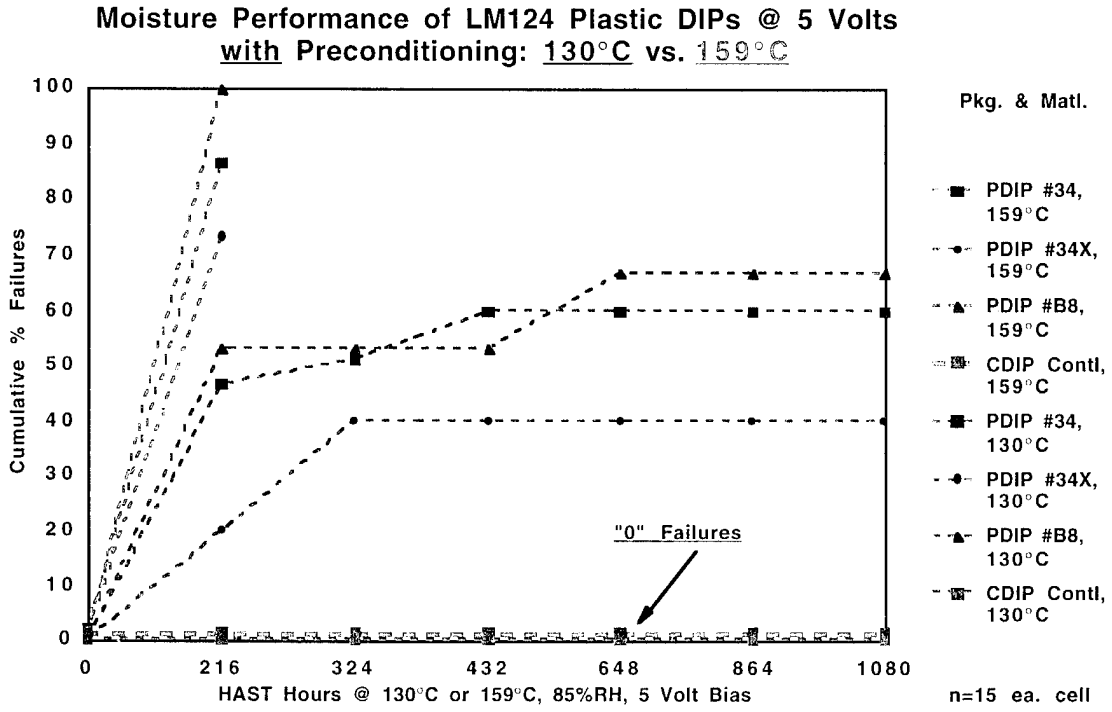


Figure 18

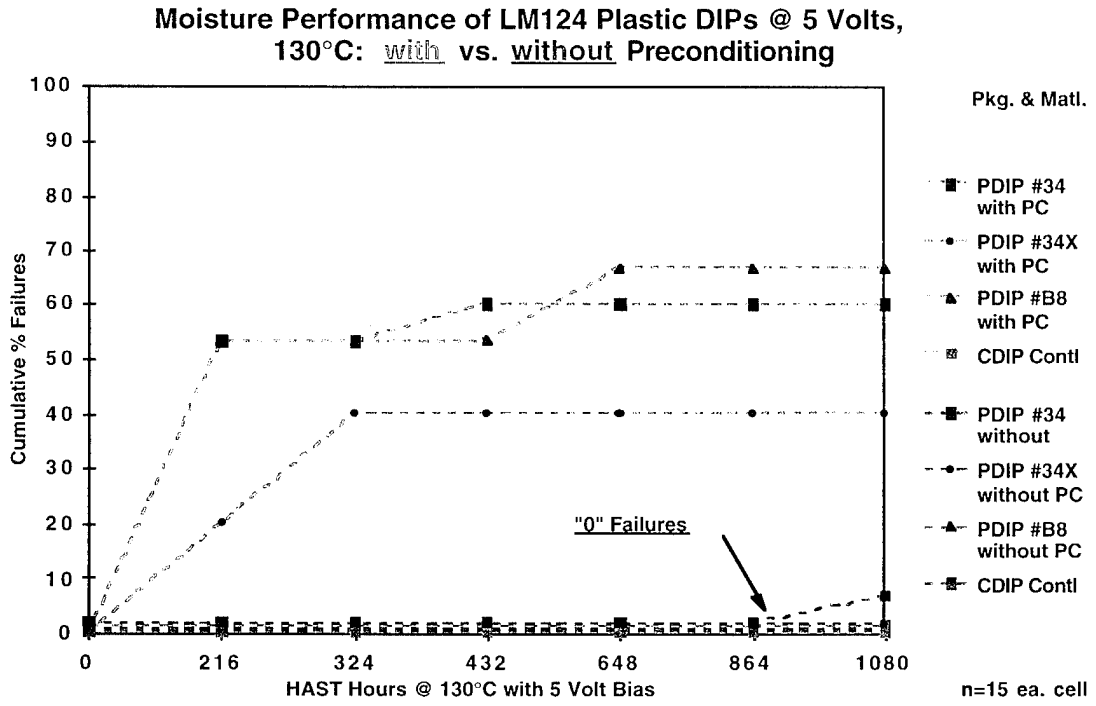


Figure 19

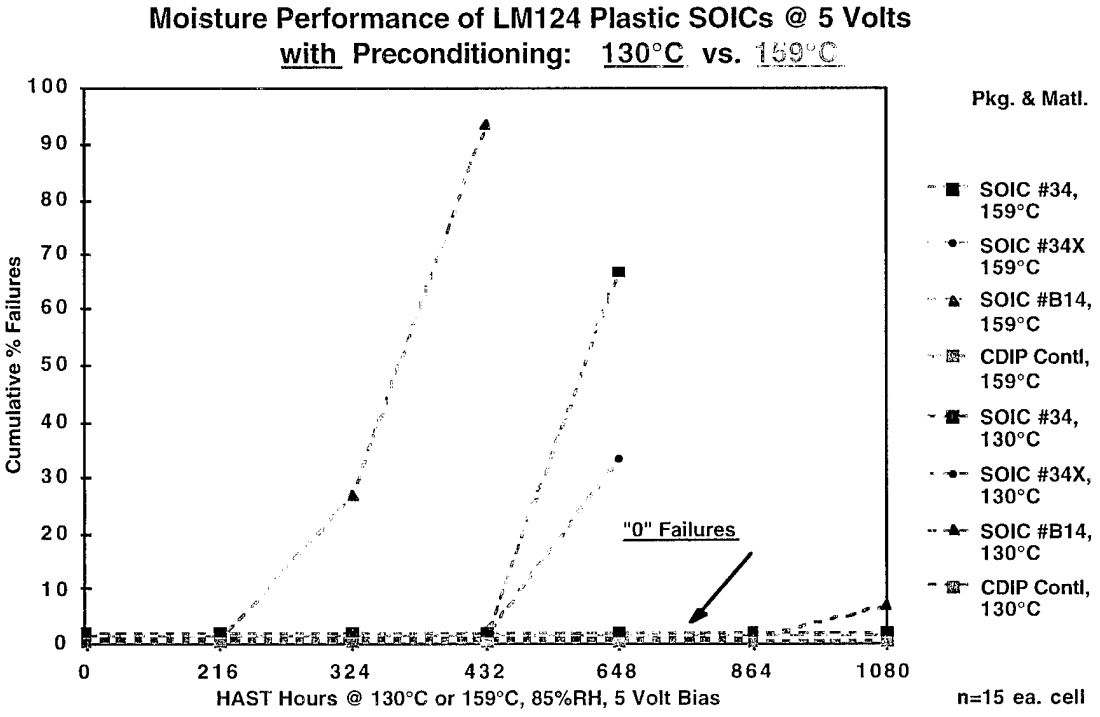


Figure 20

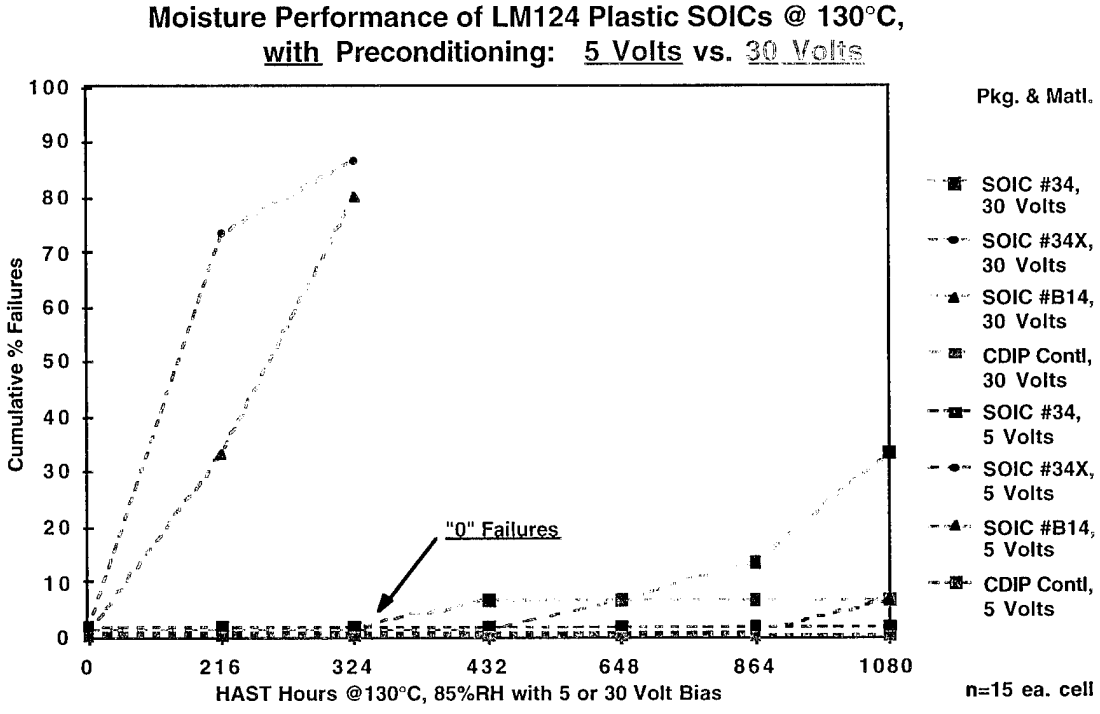


Figure 21

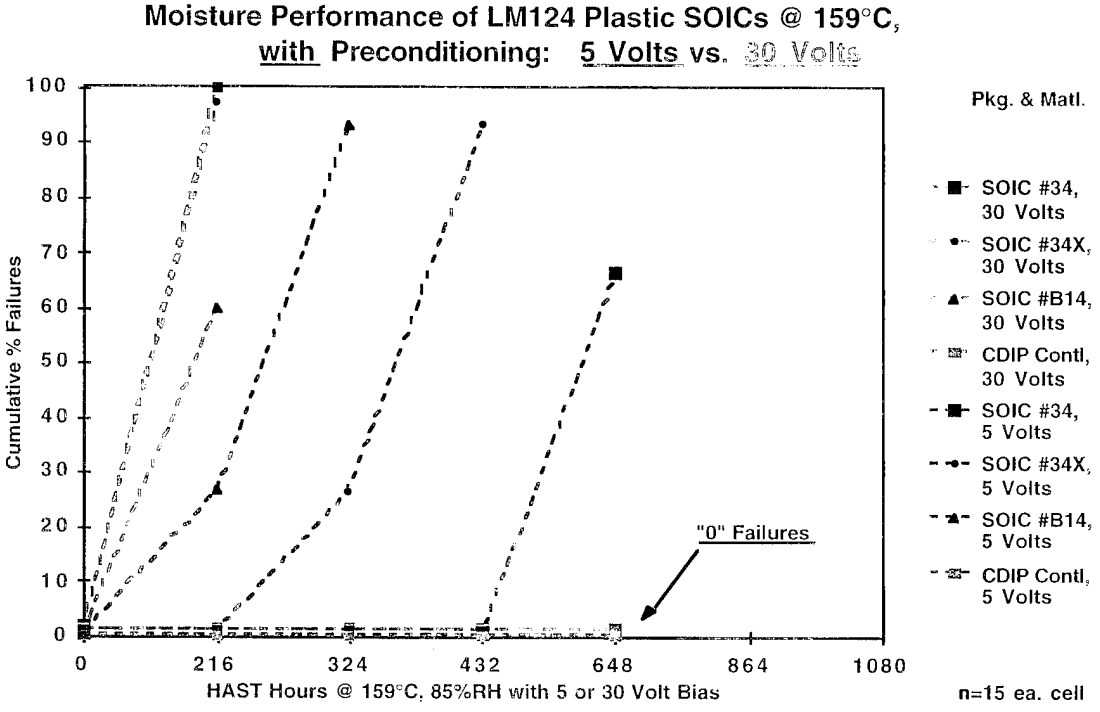


Figure 22

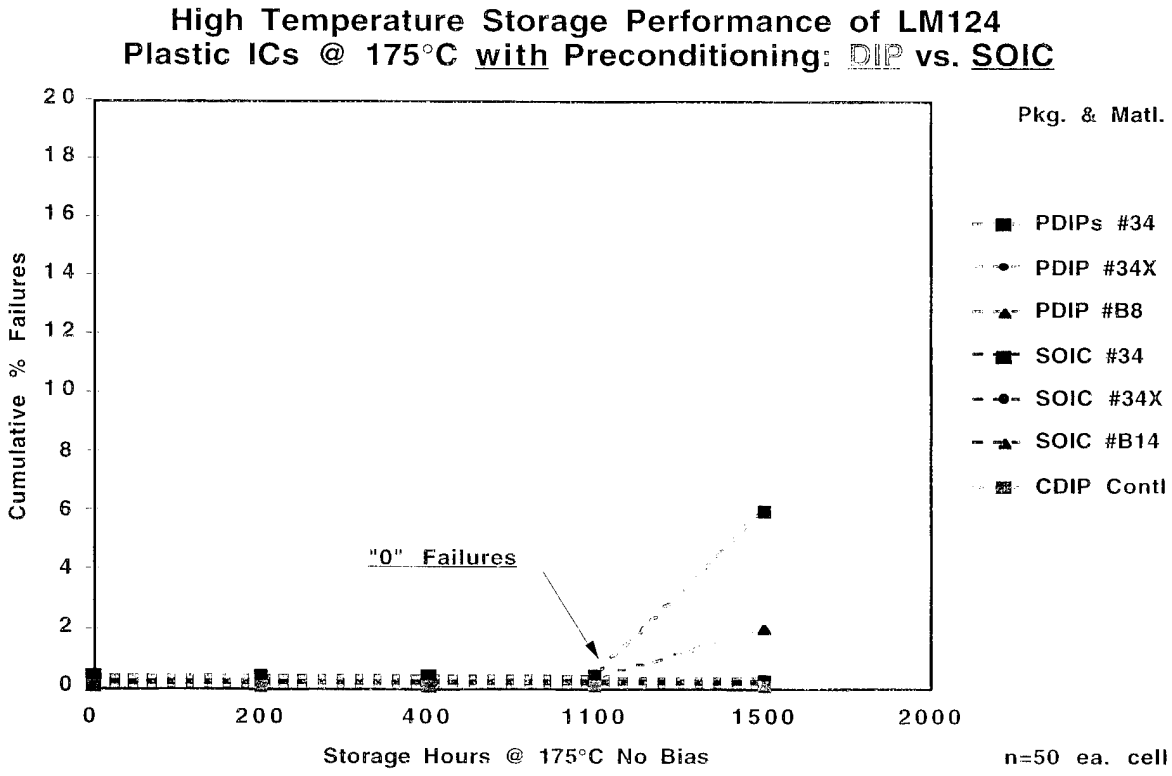


Figure 23

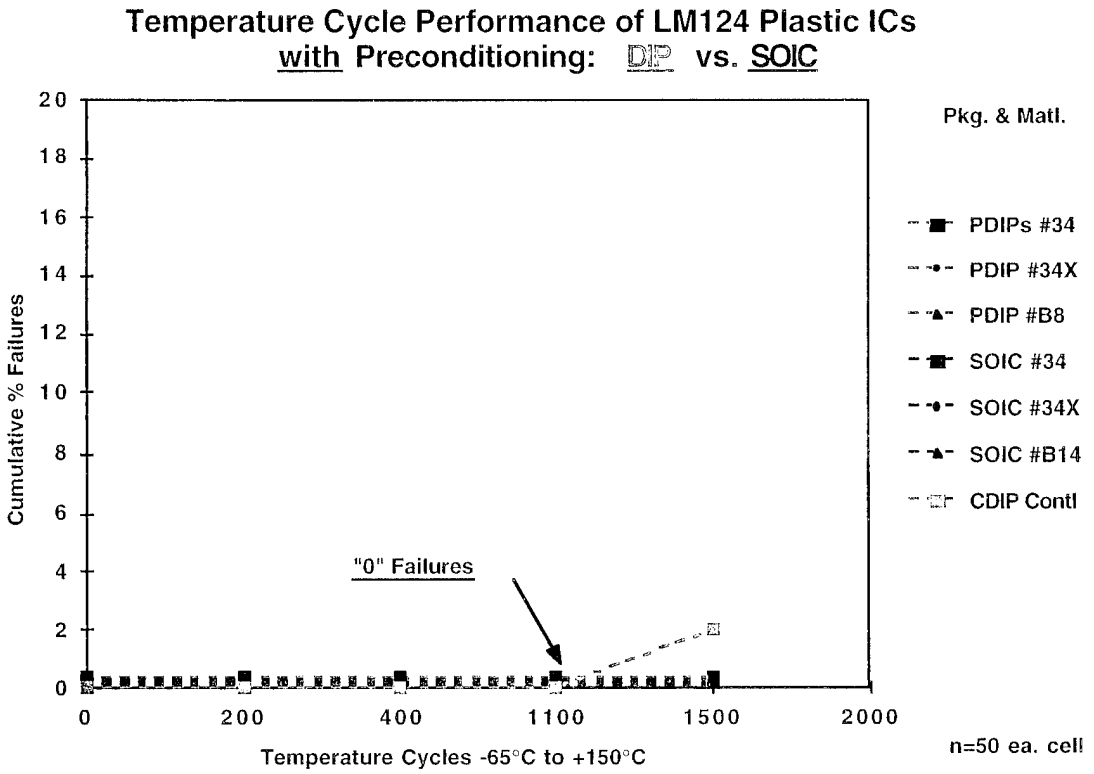


Figure 24

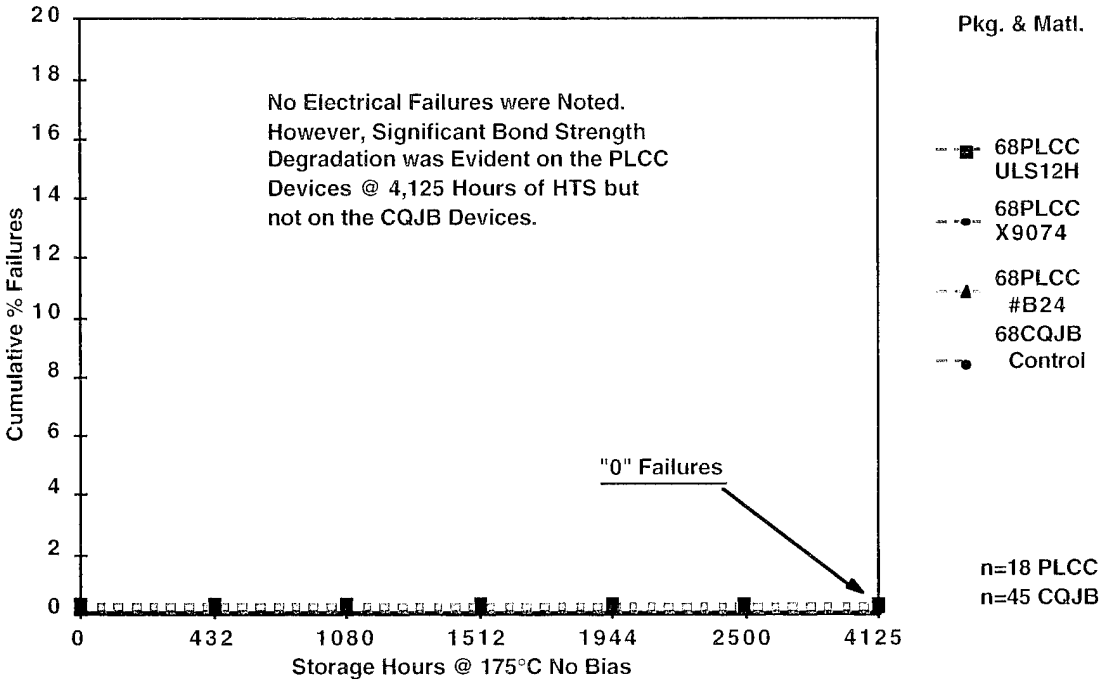


Figure 25

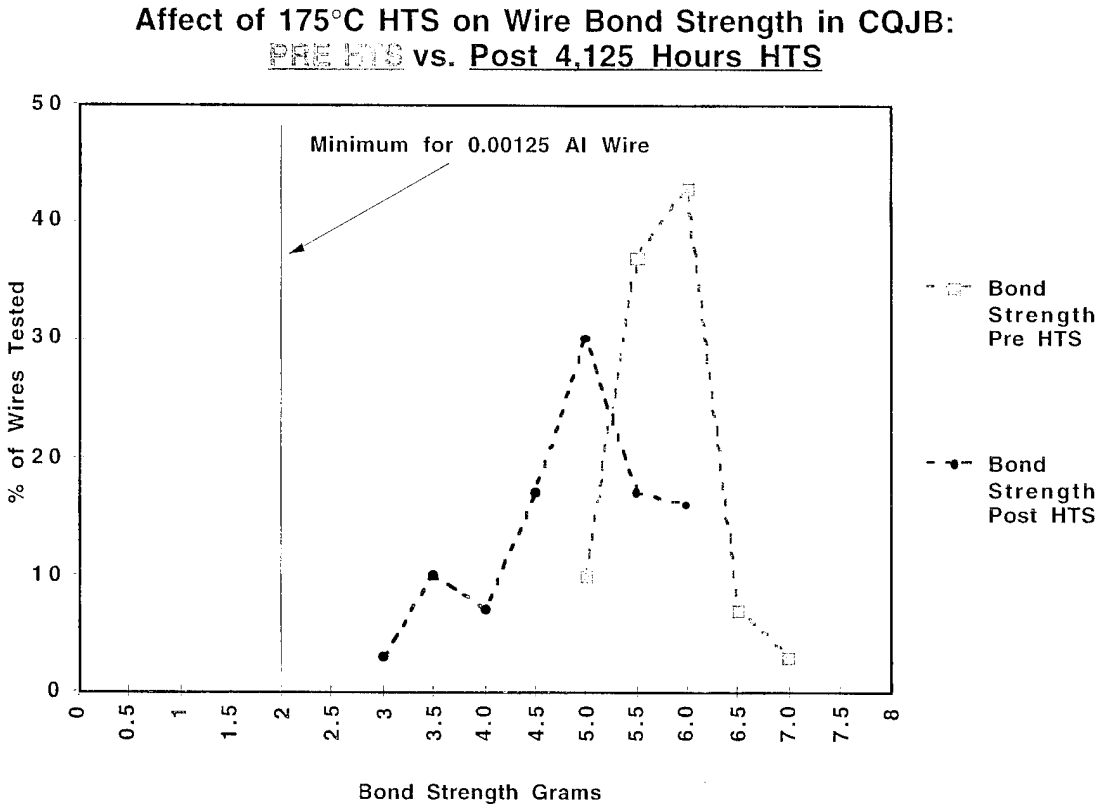


Figure 26

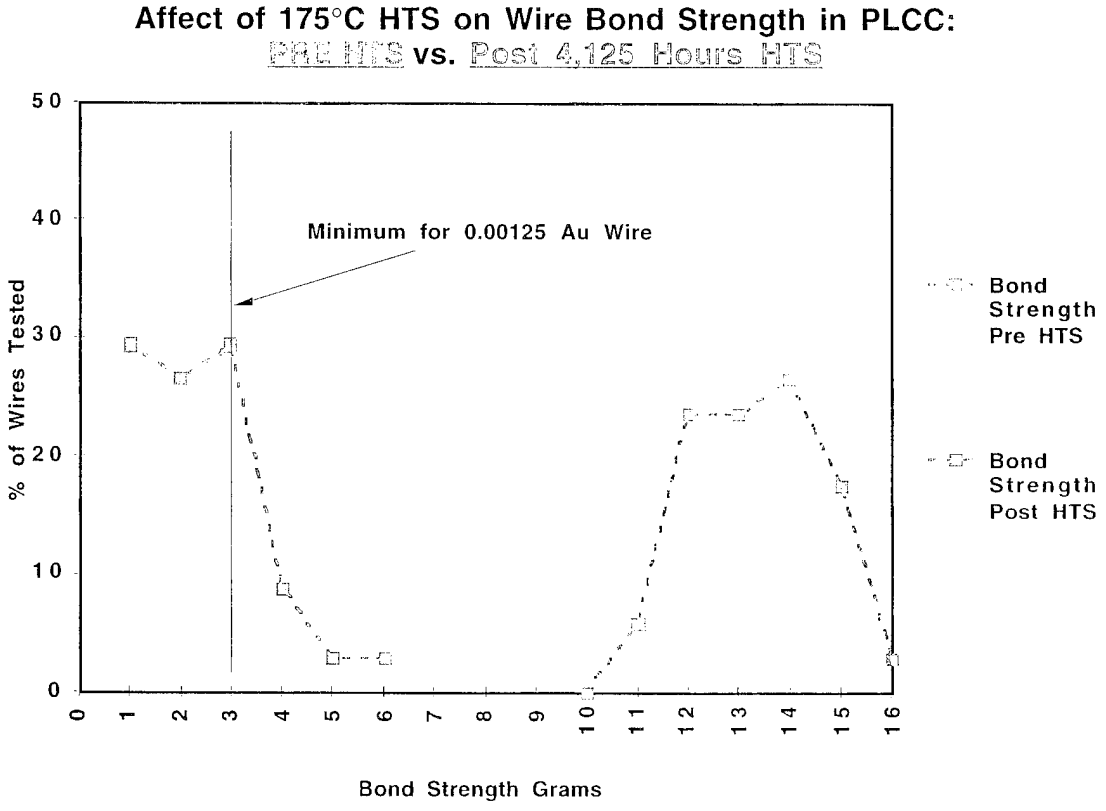


Figure 27

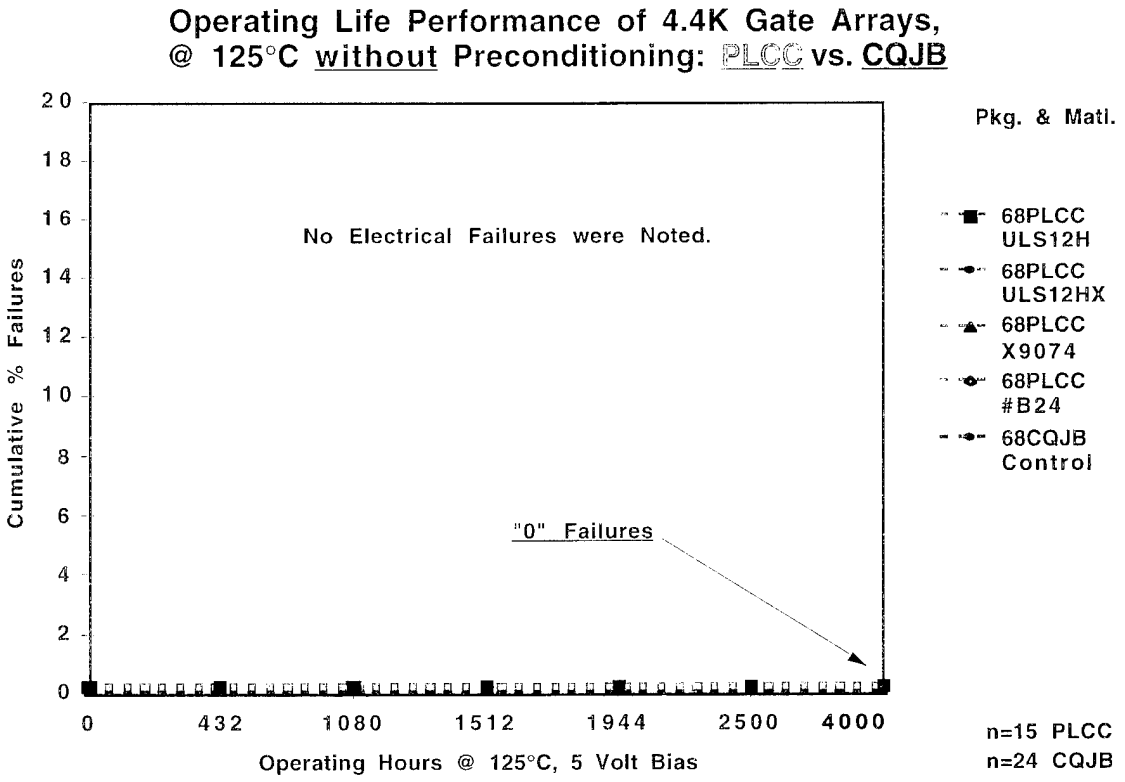


Figure 28

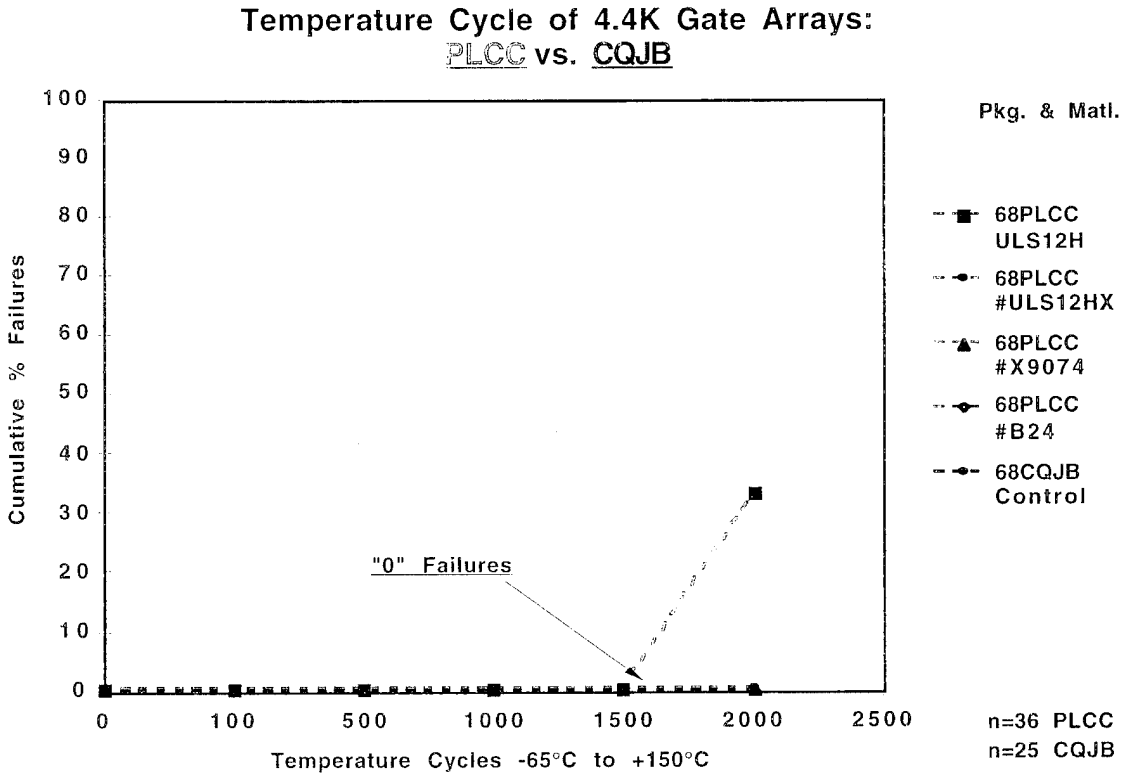
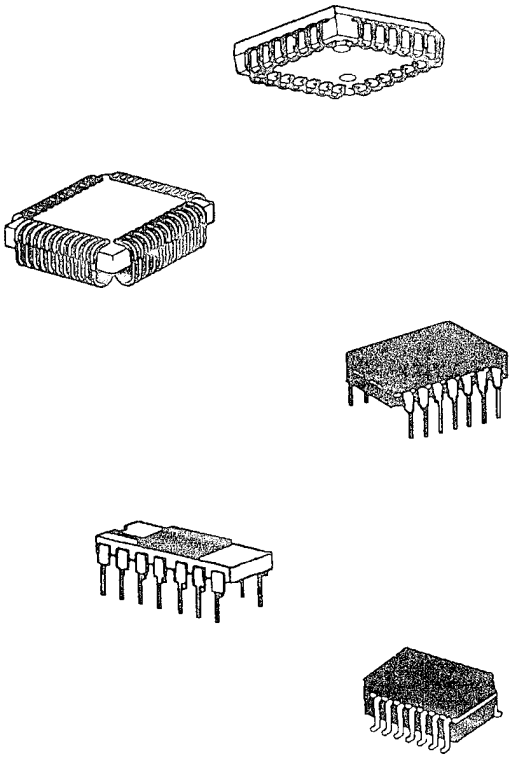


Figure 29

PLASTIC PACKAGE AVAILABILITY PROGRAM

CONCLUSIONS



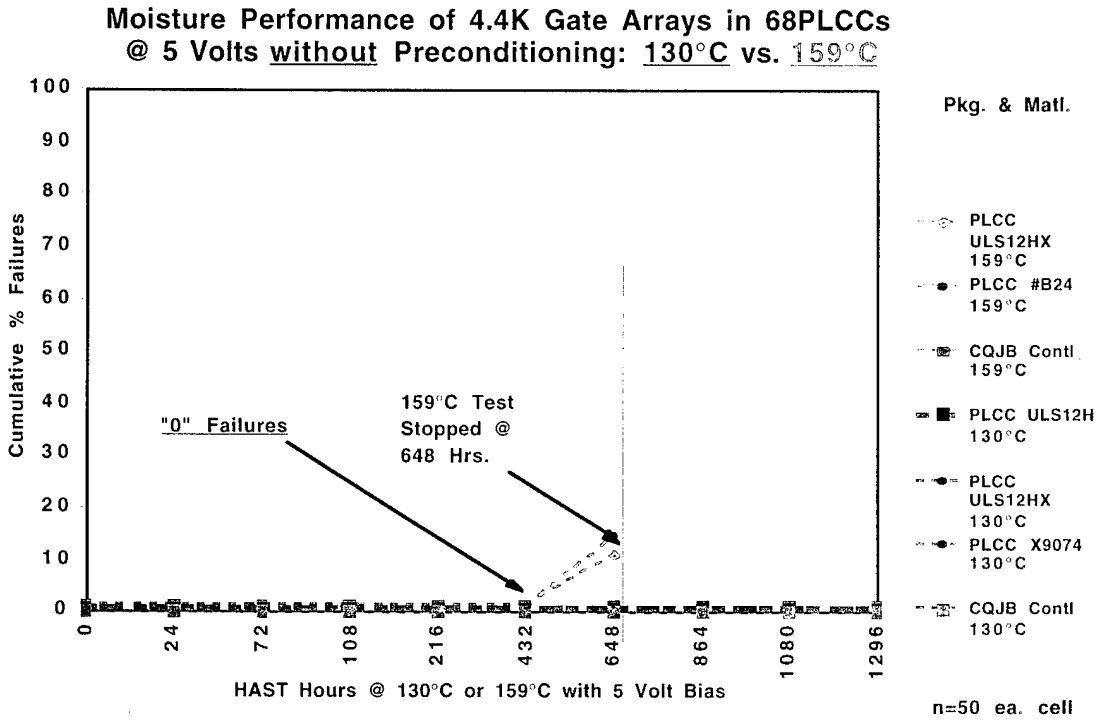


Figure 30

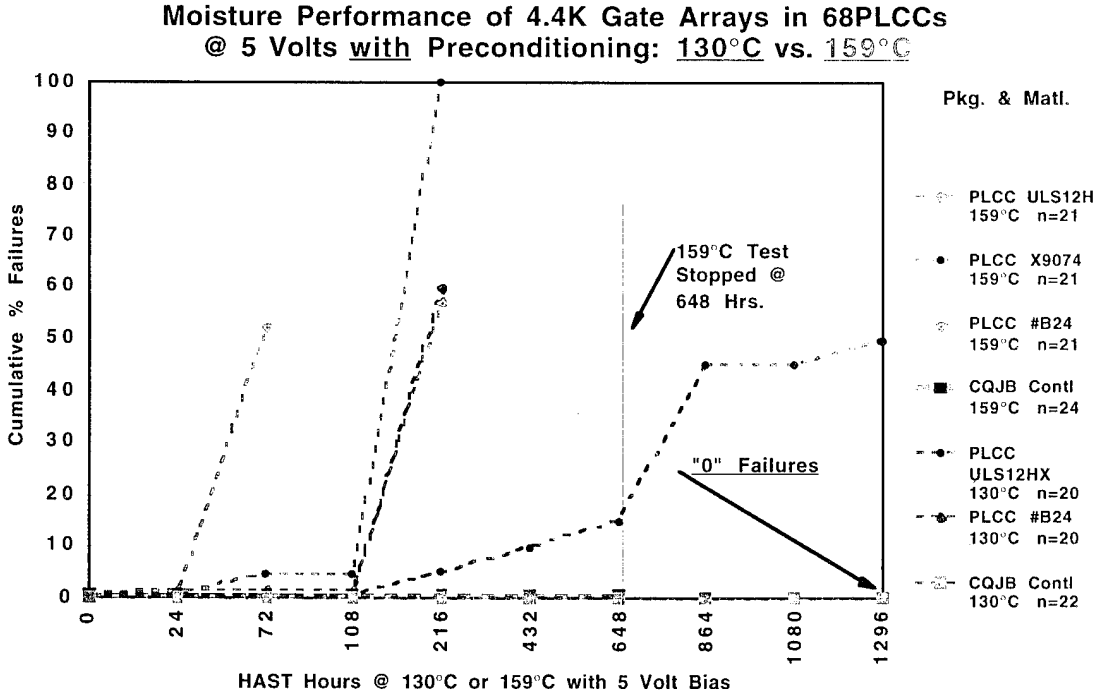


Figure 31

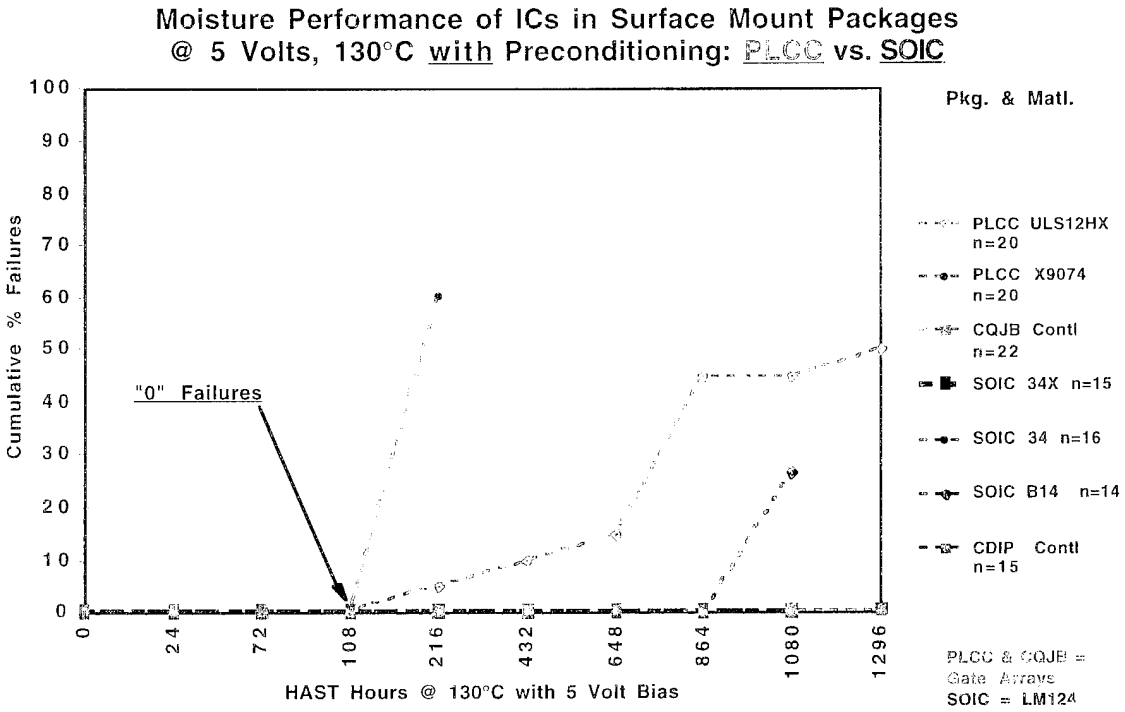


Figure 32

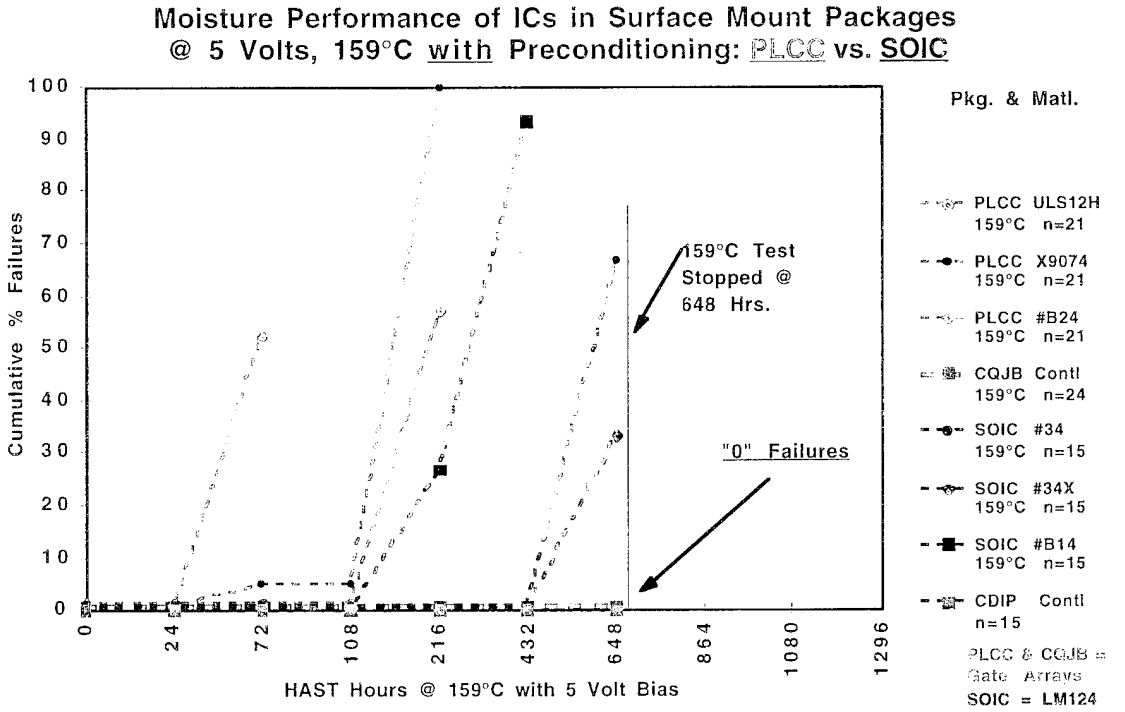
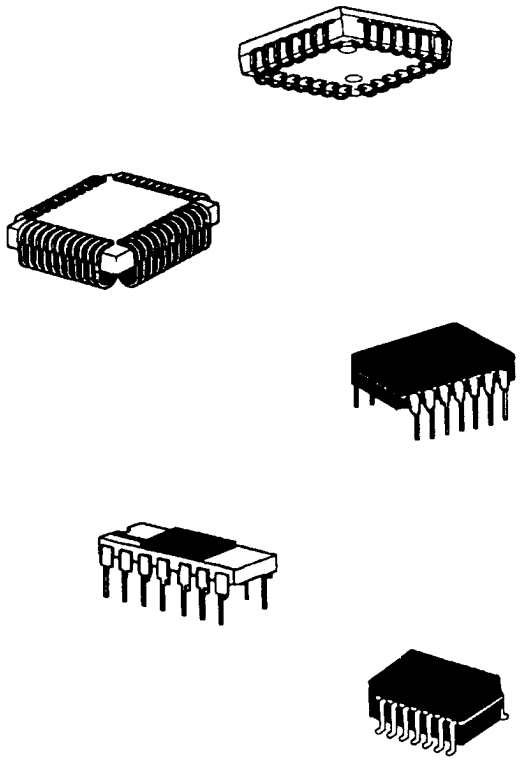


Figure 33

PLASTIC PACKAGE AVAILABILITY PROGRAM

CONCLUSIONS



CONCLUSIONS:

Task 4.0 Moisture and Corrosion Test Chip Development

The development of the NAT-01 proved to be successful and aided in the understanding of the moisture take-up in PEM, correlated corrosion failure modes on HAST and appeared to be able to identify pin-holes in the chip passivation. The evaluation of the ATC04 showed it could distinguish between different mold compounds and measure stresses as a function of the assembly and preconditioning processing steps.

Task 7.0 Device Reliability Testing

Radiation Tolerance: Plastic performs similar to ceramic on LM124s for radiation tolerance where both package types experience parametric failures after 100K Rads and gross functional failures after 200K Rads total dosage.

Accelerated, Harsh Environment Life-testing: Figure 12 highlights the conclusions from the DOE life-test PEM results, with color applied to the Master F/A Chart. The red signifies "***corrosion***" as the most serious, highest occurring failure mode, all resulting from HAST. Preconditioning and bias voltage were significant accelerating factors to the moisture related corrosion mechanism. The orange signifies a much lower incident failure mode, but one that becomes important as chip size increases, "***cracking***" of the chip surface passivation coating. The cracking occurred in the corner areas of the SCX6244 chips where it is known that the highest stresses, imposed by the package materials, occur. The yellow represents a caution in that no failures were experienced in HTS when monitored with room-temperature electrical testing, but F/A documented an inherent, known, degradation mechanism, "***intermetallic growth***", caused by the gold ball-aluminum pad bonding process/structure. Bond pull strength is significantly weakened by this growth. Significant failures did occur after 4125 hrs of HST when the devices were electrically tested at 125°C. This intermetallic and bond strength degradation did not occur in the all aluminum bond-to-die system that was used in the ceramic control units.

Failure Rate Extrapolation: As a result of the failure mode similarity for the two temperatures and two voltages used on the HAST testing, activation energies could be calculated, and Weibull failure rate prediction curves vs. time thus determined for extended life at various temperatures and voltages. See figures 34-37 for these curves. Examples:

- Figure 34: >30 yr. life @ 55 °C degrades to < 1 yr. @ 130°C, HAST @ 5v / 55% RH
- Figure 36: >10 yr. life @ 5v degrades to < 1 yr. @ 20v, HAST @ 55 °C @55% RH

Weibull Estimates for Moisture Performance of LM124 in Plastic SOIC (Epoxy #B14), with Preconditioning, @ 85%RH and 5 Volt Bias

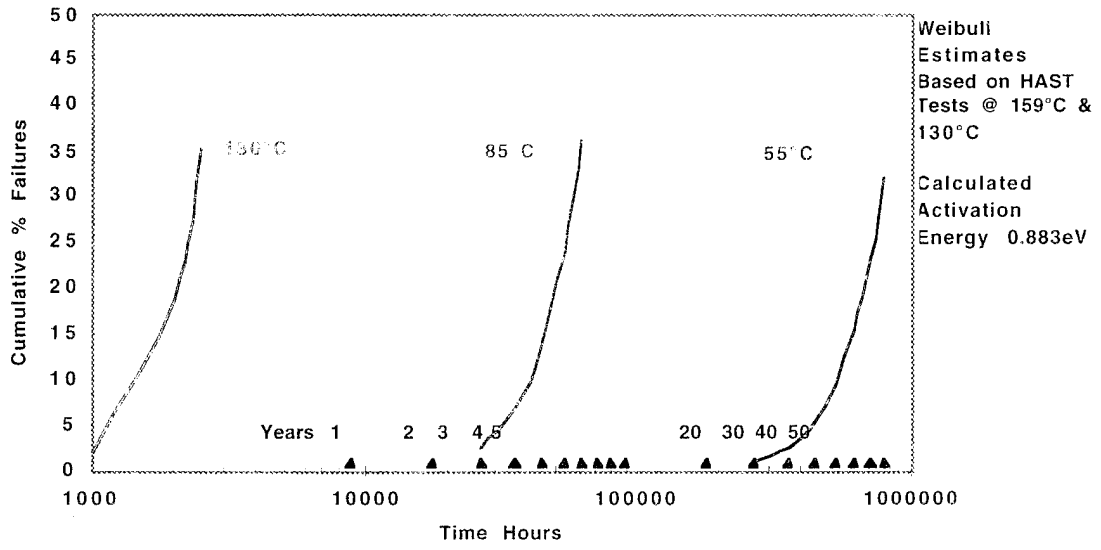


Figure 34

Weibull Estimates for Moisture Performance of 4.4K Gate Arrays in 68PLCC (Epoxy #B24), with Preconditioning, @ 85%RH and 5 Volt Bias

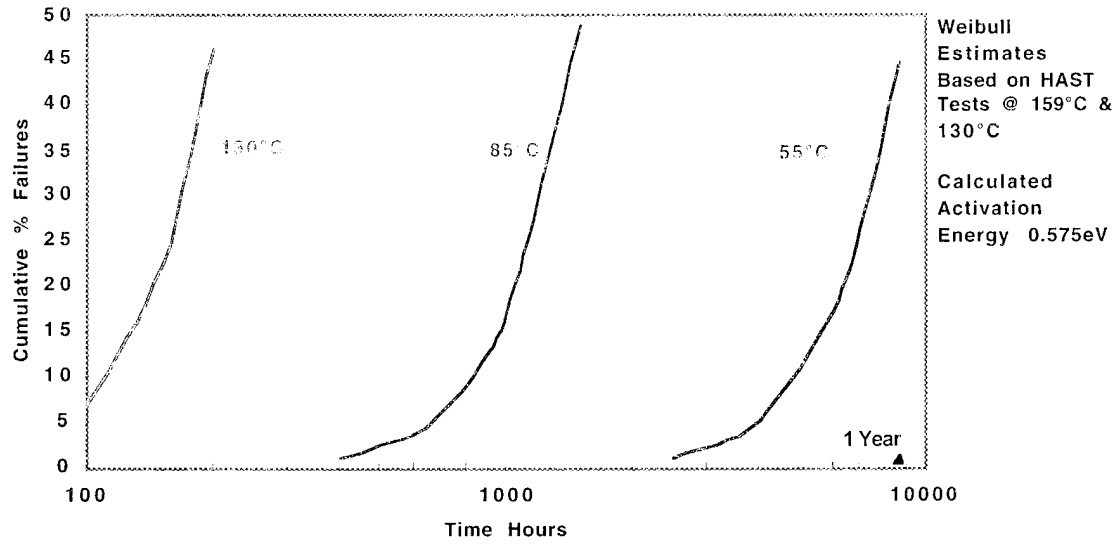


Figure 35

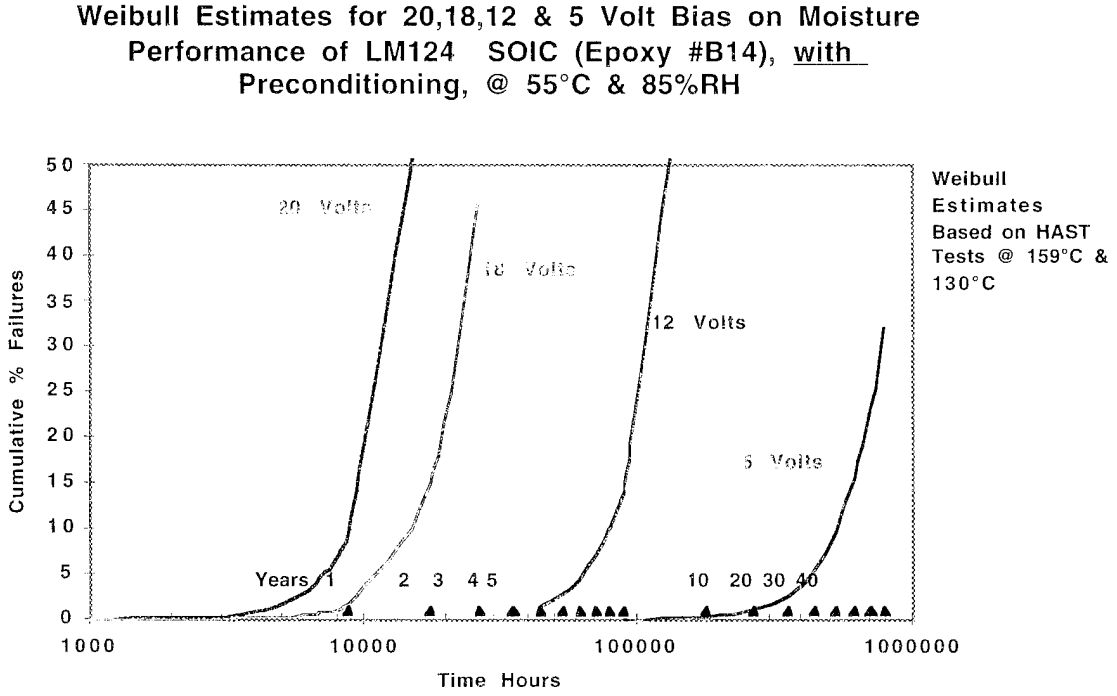


Figure 36

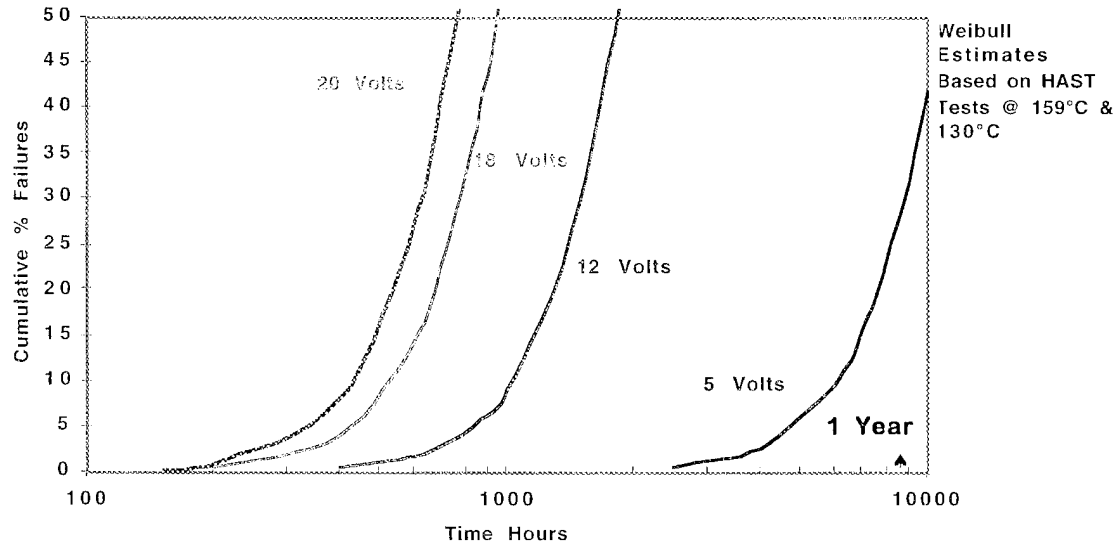


Figure 37

Task 8.0 Device Reliability Analysis

Honeywell has shown that with a careful program including vendor qualification, burn-in and temperature testing, and proper component-system design-in, as well as a relatively benign, controlled environment (commercial aircraft equipment bays), PEM can achieve acceptable failure rates.

DO's and DON'Ts: The following DO's and DON'Ts highlight the findings and recommendations of the PPA program for the use of PEM in harsh, military like environments:

Recommended DO's:

- do continue to use rigorous vendor qualification, extended-temp screening and burn-in as required, for PEM high-Rel applications, similar to ceramic-hermetic, with the addition of HAST testing
- do qualify mold compound changes
- do design for lowest practicable operating voltage and temperature
- do use board assembly "preconditioning" prior to qualification, which simulates worse case board assembly/repair conditions
- do use non-aggressive, no-clean, fluxes in board assembly, and rigorously follow the dry-bag procedures specified by the component manufacturer
- do include temperature cycle for qualification of larger chips (>250 mils / side)
- do maintain low-humidity environment
- do include the NAT-01 and ATC04 test chips for plastic package studies
- do consider the use of hermetic-ceramic for use in long-term, harsh environments, as the use of PEM continue to be a concern for these applications

Recommended DON'Ts:

- don't use PEM for long-term high humidity operation, especially where higher voltages or higher temperatures are required
- don't use aggressive, halide-based fluxes during PEM board solder assembly/repair
- don't use high stress mold compounds with large chips (>250 mils/side)
- don't use PEM beyond manufactures ratings
- don't run environmental life-test qualification w/o first preconditioning with worse-case board assembly/repair simulated pre-stressing

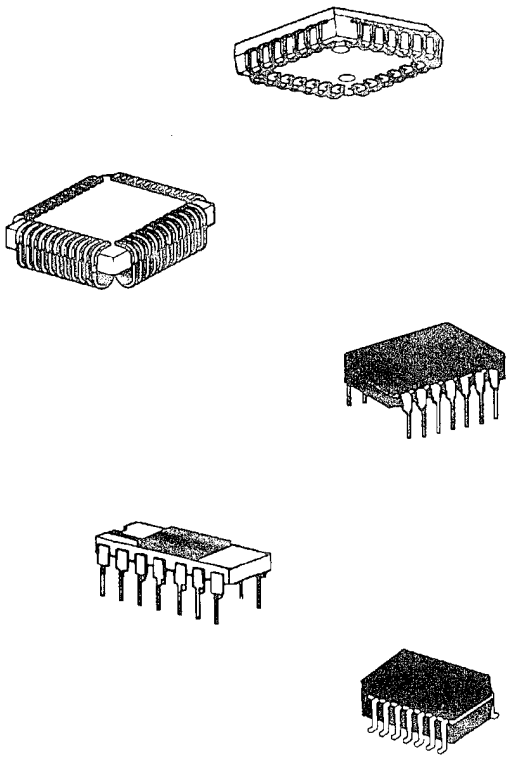
Key Suggested Areas for Future Work:

- re-visit low-stress mold compound TC performance on large PEM
- confirm the advantages of using getter additives on HAST performance
- develop a dynamic, corrosive atmosphere HAST chamber for determining long-term storage, and intermittent operation long-term storage, PEM reliability
- determine the "culprit" process step(s) in the preconditioning flow
- develop improved materials for increased PEM moisture tolerance
- develop economically effective non-corroding bondwire-bondpad structure
- develop PEM package qualification standard using sensor test chip(s)
- continue industry field reliability data collection/analysis, under auspices of academic or industry association

PLASTIC PACKAGE AVAILABILITY PROGRAM

MATERIALS OF CONSTRUCTION SECTION 1

Task 1.0 Mil IC Pkg Criteria Def. & System Selection



MATERIALS OF CONSTRUCTION

Sub-Section: **Pages**

	Executive Summary	2
1.0	Introduction	3
2.0	Leadframe	5
3.0	Die Attach	22
4.0	Wire Bonding	30
5.0	Die Coating	37
6.0	Pack and Ship	42
7.0	References	46
8.0	Recommendations for Plastic Package Materials of Construction Given Certain Reliability Issues	48

The Materials of Construction Team: Eric Huang, Mark Baker, Andrea Chen, Joseph Bendik, and Luu Nguyen.

EXECUTIVE SUMMARY

BACKGROUND

Part of the Plastic Package Availability Program, DLA 900-92-C-1647, involves a review of the materials of construction of molded plastic packages. In this phase of the work, the technology will be overviewed without recommendation as to what should or should not be used for military environments. This work is broken down into sub-sections each of which describes one significant part of the plastic package in detail.

Plastic-encapsulated integrated circuits have proliferated throughout the electronics industry and currently make up over 90% of all integrated-circuit (IC) packages built today. The first plastic packages which came out in the 1960's had reliability and functionality problems particularly at elevated temperatures. In the early days, 85°C/85% RH tests generally gave 25% failures at 1000 hours compared to less than 0.1% today (1). Much of this improvement has come out of extensive research into the failure mechanisms and the material interactions within plastic-encapsulated packages. The physical characteristics of the leadframe material, mold compound, die attach material, bond wire, or other interconnect material, and the IC chip must be taken into account when developing a package. The selection of these materials play a large role in the reliability of the device.

SYNOPSIS

The purpose of the Plastic Packaging Availability Program is to complement and extend current knowledge in the materials, design, assembly, testing and reliability associated with plastic packages. This materials-of-construction report is a deliverable of **Task 2**, *Plastic Package Criteria Definition*, as outlined in the contract between National Semiconductor Corporation (NSC) and the Department of Defense (DoD).

In this report, the effect of various materials of construction of plastic-encapsulated packages on reliability issues is discussed with the appropriate background. It is not the intent of the authors to compile a "complete" report on materials of construction in plastic packages. Only five major components of the plastic-encapsulated package are discussed: Leadframe (Sub-Section 2.0); Die Attach (Sub-Section 3.0); Wire Bonding (Sub-Section 4.0); Die Coating (Sub-Section 5.0); and, Pack and Ship (Sub-Section 6.0). The mold compound is another important integral component of the package. However, this aspect is covered in detail by Plaskon's report.

The information is presented to cover the issues that would be of interest to DoD end users. The report is separated into four categories:

- Introduction
- Materials & Properties
- Manufacturing Processes
- Vendors/Manufacturers

This report was compiled using literature searches, specification reviews, interviews, and past experience to present the most relevant information possible using National Semiconductor's extensive plastic packaging background. Among the package-related issues covered in this report are:

- Delamination/Package Cracking/Moisture Penetration
- Stress/Die Cracking
- Corrosion
- Thermal Management

Given certain reliability problems common known to plastic-encapsulated packages, recommendations for enhancing the performance of the packages are summarized in Sub-Section 8.0.

1.0 INTRODUCTION

The selection of leadframe material greatly influences the stress in molded plastic packages. Mismatched coefficients of thermal expansion (CTEs) result in decreased reliability. Leadframe to mold compound mismatch can result in poor adhesion, thereby, inducing package cracking and reducing moisture resistance. Mismatch of die to mold compound CTEs can result in passivation cracking and die metal damage. Leadframe to die mismatch increases the stress on the die.

As part of the plastic package, the leadframe performs the following specific critical functions (2):

- provide an electrical and thermal conductor between the device and the board or the outside environment,
- provide stability and indexing capability for the package as it proceeds through the manufacturing process,
- provide a support matrix for the epoxy molding compound,
- serve as a substrate for chip attach, and
- act as a dam which prevents the epoxy molding compound (EMC) from escaping through the lead spacing.

Most often the package, and therefore the IC, is accessed through a printed wiring board, PWB. The PWB is a larger circuit consisting of interconnected traces which terminate at lead insertion points where ICs or other devices fit to make their contribution on the given signal. The insertion points may be through-hole vias, or surface mount pads. Usually molded DIPs have through-hole leads. Surface mount devices, SMDs, use surface mount pads for the gull wing or J-leads of the SMD package. Sockets can form the first interconnect on the PWB, so that IC packages may be easily inserted into the sockets and removed as needed. IC test boards use sockets.

All factors must be considered when developing a molded plastic package for an IC. High power linear devices require different materials selection than does a low power digital processor on a large Si chip. A small "jellybean" linear chip has tighter package cost constraints than does the microprocessor device. A more elaborate leadframe could be considered in the latter case.

In this report, the leadframe will be described with respect to the following areas:

- Materials & properties,
- Design & structure,
- Manufacturing,
- Vendors/Manufacturers

Since general reliability of plastic-encapsulated devices is the main focus of the Plastic Packaging Availability Program, the information will be summarized within such context. The three issues that are important to making decisions on the materials selection, processing, etc., of plastic packages are cost, availability, and reliability.

1.1 Cost and Availability

In the past, cost considerations were not always readily associated with government military spending. Many feel that the cost of military microelectronic parts far outweigh the high reliability that was offered. However, with the changing global political scene and tightening military budget, cost has moved to the forefront of issues confronting procurement of military electronics (3). Plastic packages, which in the past were seen as high risk as far as reliability was concerned, have become desirable for their cost and weight savings. Availability of many devices for use in military systems is also an issue. With many semiconductor companies feeling the same economic constraints, some of the desired devices may only be offered in a plastic configuration.

Another example of availability problems arises when considering the vendor base for epoxy molding compounds. Almost all the major suppliers of EMCs are foreign. This can pose a problem when facing the DoD's restrictions regarding domestic/foreign materials suppliers.

1.2 Reliability

The reliability of plastic packages depends on many factors. There are many mechanisms of failure that can occur . The following is a brief list of possible failure mechanisms and reliability concerns. Electrical failure due to electromagnetic effects are not covered.

- Electrochemical mechanisms:
  - Solderability
  - Bondability
  - Delamination/Adhesion
  - Corrosion
  - Ionic contamination
  - Electromigration
- Thermomechanical mechanisms:
  - Thermal conductivity
  - Thermal stress due to CTE mismatch
  - Delamination / "Popcorning"
  - Lead bend fatigue
  - Lead break
  - Stress/Die attach pad (DAP) shift

Many of these effects contribute to package cracking. This can be a potentially costly problem due to the lack of environmental protection afforded to the device by a cracked package. These failure mechanisms are not at all independent of each other. For example, delamination of the EMC from the DAP can occur because of excess stresses caused by the mismatch in the thermal expansion coefficients of the leadframe material and EMC. The delamination can also occur because of expansion of gasified moisture at the DAP/EMC interface during heat excursions such as seen during solder reflow.

Ensuring the reliability of plastic packages involves accounting for very complex interaction of failure mechanisms. In deciding upon various materials of construction, consideration of all the above mechanisms is crucial.

1.3 Brief Description of Some Failure Issues

1.3.1 Fatigue

In plastic packaging, fatigue failure occurs mainly due to the thermomechanical effect of temperature cycling. One of the most prevalent fatigue failure areas is the outer lead-solder interface of surface mounted devices. Differing CTEs between leadframe material, solder, and the PWB create stresses during temperature excursions. These stresses are cycled when the temperature is cycled. Thus, in many rugged applications, such as automobile components, the opportunity for failure is high because of temperature cycling. Fatigue can also occur because of lead bending. Often, a device lead is bent due to improper insertion. Sometimes, the lead needs to be straightened to allow for another insertion attempt. A fatigue failure could occur and render the IC useless.

1.3.2 Delamination/Package Cracking

Delamination is the physical separation of two adjoining layers. It can be considered as an internal crack within the package. It can occur in a number of areas in the package, including the DAP/EMC interface, DAP/die attach/Si interface, and the EMC/Si interface. Delamination can occur due to either the effect of CTE mismatch between materials during thermal cycling, or the collection and subsequent vaporization of moisture at an interface. In the latter case, package cracking is almost inevitable. This type of delamination commonly occurs during the surface mounting of components to PWB, where the components are rapidly heated. In both cases, adhesion is the key to solving these problems.

1.3.3 Corrosion

In both hermetic and non-hermetic packaging, corrosion of the outer leads and internal areas is a major concern. It plays a major role in the reliability of the electronic device. The most prevalent areas for corrosion are the outer leads, bond wires, device metallization (including bond pads), and inner leads. The exposure of these areas to both moisture and dissolved ionics is needed to cause corrosion problems.

In plastic packaging, the problem becomes much more complex because of the porosity of the EMC and the higher probability of impurities in the EMC. Many solutions can be implemented to correct or alleviate the corrosion problem. For example, special coatings deposited on assembled parts can help to provide some protection to the device and bond wires. Delamination and package cracking contribute to corrosion by allowing a faster path for ion-laden moisture to penetrate.

1.4 Package Types

It is helpful to understand the scope of this report. The main concern of the report is plastic-encapsulated packages. These include any epoxy molding compound packages used for microelectronics. A brief list of the various package types and other information is given in Reference 2. Note that the various package designations can vary throughout the industry.

The various package types can be separated into two categories, through-hole or surface mountable. These terms refer to the method by which the package is connected to the PWB. The through-hole packages include molded dual-in-line packages (MDIP), single-in-line packages (SIP), zigzag-in-line packages (ZIP), and transistor outline packages (TO). The surface mount packages include small outline packages (SO), plastic quad flat packages (PQFP), and plastic leaded chip carriers (PLCC). A list of packages also appears in Table 2-6, which also shows applications that use those package configurations. Please note that the package designations vary slightly from company to company.

2.0 LEADFRAMES

2.1 Introduction

Many demands are placed upon the leadframe in an integrated circuit plastic package. From leadframe manufacture to package assembly to operating life of the IC device, the plastic package leadframe has many challenges to overcome. The leadframe material to use is selected considering these obstacles along with other specifics, e.g., IC chip size, the number of leads, the geometries of the part (lead bend angles and pitch), volume of product to be built, and thermal requirements.

Many leadframe materials will be discussed and compared with respect to their properties and the effect of those properties on the general reliability and overall cost of plastic packages. The previous section briefly describes some of the reliability and cost issues that arise when considering plastic packages.

Table 2-1: Reliability effect and relevant properties

Reliability Effect	Material Property
1. Fatigue	Yield strength Hardness Thermal coefficient of expansion % elongation Young's modulus of elasticity
2. Delamination/Package Cracking	Surface roughness Thermal coefficient of expansion
3. Corrosion	Reactivity Cleanliness
4. Lead break/DAP shift	Yield strength Young's modulus of elasticity
5. Electrical/Thermal Performance	Electrical conductivity Thermal conductivity

There are basically three classes of leadframe materials used in industry. They are:

- Ni-Fe alloys (i.e. Alloy-42),

- Cu alloys, and
- Clad materials (layered composite strips).

Because of the various stresses that the leadframe sees during its manufacture, use, and operating life, there are certain critical properties that need to be addressed when selecting the leadframe material. Table 2-1 is a brief list of some of these properties and the reliability effect. In this section, a brief description of the stresses that leadframes see in their lifetime and a relation between the reliability problems and materials properties that alleviate these problems will be discussed. The relative cost of materials and the role this plays will also be presented.

2.2 Sources of Stresses for Leadframes

Requirements are placed upon leadframes during manufacture and over the package functional lifetime. Materials chosen for the leadframe construction must have properties which allow the leadframe to withstand manufacturing and operating conditions without failing. Table 2-2 is a list of sources of these requirements and the stresses or reliability problems that might be incurred.

Table 2-2: Sources of stresses on leadframes

Source	Effect	Optimized Property
Manufacturing (Stamping)	Fracture Plastic deformation Lead deflection Springboard Burrs Planarity	Toughness Yield strength Modulus of elasticity Modulus of elasticity Ductility Modulus of elasticity
Manufacturing (Etching)	Non-uniform etch rate	Material purity
Assembly	Bondability Planarity Softening Fracture Deformation	Surface cleanliness Modulus of elasticity Recrystallization temperature Toughness Yield strength
Operating life	Corrosion Electromigration Moisture penetration Package cracking	Resistance to corrosion Electrolytic potential Adhesion CTE

2.2.1 Leadframe Manufacturing

Before a leadframe can be manufactured, the material must be rolled into sheets of the appropriate thickness. The ingot is processed through a series of rolling and heat treatments to achieve the desired thickness and % reduction in area. The rolled material is then slit to the proper handling width for leadframe processing. The material is then either stamped, where individual punches remove sections of material leaving the leadframe features behind, or etched where the leadframe pattern is photochemically removed from the matrix. Specifications of flatness and dimensional accuracy must be met, as well as elimination of slivers or dents induced during processing. See Sub-section 2.4 for more manufacturing information.

During this process, the material undergoes a myriad of stresses and changes. The deformation and heat treatment cycles greatly affect the final material properties, such as hardness, toughness, etc. The stamping process can be the most rigorous. The material can easily fracture or deform during this process.

The etching process can impart deformations due to temperature and handling as well, since the material thicknesses involved are smaller than for stamping. Because etching is a chemical process, reaction rates are a concern over the area of the leadframe. Additional processing such as coining and downsetting again depend upon the inherent material characteristics for success.

2.2.2 Package Assembly

During package assembly, more demands are placed on the leadframe material. The leadframe serves as the chip carrier during assembly operations providing mechanical support prior to molding. During die attach cure, the leadframe is exposed to temperatures of 150 to 250°C for 2 to 4 hours, typically. Bondability must be insured during the wire bonding operation; a clean non-oxidized leadframe surface is required. Leadframe planarity is an issue. If the internal leads are out of planarity by as little as 0.004", depending on the material and thickness, the leadframe is not bondable. The material must be resistant to scratches and handling defects. Scratched, slivered, or dented leadframes during molding can lead to resin bleed.

Trim and form operations involve bending of the leadframe material to the final lead position. Subsequent handling during testing, packing, or installation can cause lead bending. These leads must be straightened out, often more than once. The material must be ductile enough to resist cracking during bending and strong enough to maintain lead position during assembly and handling.

2.2.3 Product Operating Life

The overall reliability of the integrated circuit is often directly related to the package. The leadframe is a key component in this relationship. While the IC, bonds, and wires are within the encapsulant, the external leads of the leadframe are directly submitted to atmospheric conditions. Corrosion of the leadframe material can lead to early opens or shorts. This corrosion can occur on the external leads, or on internal leads, pads, and wire, through migration of ions to the interior of the package. The compatibility of the leadframe material to other material in the package has been shown to influence package cracking during temperature cycling (4).

2.3 Properties of Common Leadframe Materials

Given the requirements dictated by the various stresses seen by the leadframe, consideration must be given to the various properties of the leadframe material desired. This Sub-section describes the various materials available for use in industry and their characteristics. A comparison of these properties among leadframe materials and other materials is given in Table 2-3.

2.3.1 Leadframe Materials

As mentioned above, there are basically three types of leadframe materials: Ni-Fe alloys, Cu alloys, and clad materials. Clad materials are not in use as prominently today as the other two materials.

Ni-Fe alloys: The Ni-Fe alloys, commonly known as Alloy-42, contain approximately 42% nickel and 57% Fe with trace elements. It is a desirable material because its CTE closely matches that of silicon (4.5 ppm/°C vs. 2.6 ppm/°C). It possesses excellent elastic properties and can be heat treated to provide a wide range of tensile properties. There is no need for barrier metal plating when solder plating onto Alloy-42. In comparison to the Cu alloys, Alloy-42 does have some drawbacks. It possesses very low thermal and electrical conductivity, which are two properties crucial to IC performance. Thus, it has limited use in applications where power and heat dissipation are critical.

Cu alloys: Cu alloys have generally lower strength than Alloy-42. Table 2-3 lists a variety of Cu alloys and Alloy-42 with their respective properties. The conductivity of Cu alloys exceeds that of Alloy-42. Additives such as Fe, Zr, Zn, Sn and P can help to improve the mechanical properties of the Cu alloys. Pure copper is inadequate for the needs of plastic package leadframes. Heat treatments also help to refine the mechanical properties of Cu alloys. The Cu alloys seem to exhibit better adhesion with most EMCs than Alloy-42. This is because of the relatively good match of CTEs between Cu alloys and EMCs (17 ppm/°C vs. 20 ppm/°C). CTE mismatch between the Cu and the silicon die is usually compensated for by the die attach material used, generally with an intermediate CTE value.

Clad materials: These materials attempt to get the best of both worlds by creating a layered composite of copper on a steel matrix. The premise is to obtain the strength of the steel matrix material while getting the conductivity of the copper layer. High pressure rolling is used to create these materials.

2.3.2 Material Properties

Table 2-3 lists properties of many leadframe materials. The modulus of elasticity, Young's modulus, is a measure of the resilience of the material; it is the ratio of the stress and the reversible strain. Ductility identifies the amount of strain at failure. It is the total plastic strain prior to fracture and may be expressed as % elongation. Strength is a measure of the level of stress required to make a material fail.

Table 2-3: Leadframe materials and properties (5)

Alloy	Chemical Composition %	Young's Modulus (GPa)	CTE (ppm/°C)	% Elongation	Thermal Conductivity (W/°C.mm)	Electrical Conductivity (% IACS)
Alloy-42	42 Ni, other Fe	145	4.5	10 to 15	0.015	3
C151	99.9 Cu, 0.1 Zr	117	17.7	4 to 8	0.36	90
C155	0.11 Mg, 0.07 Ag, 0.06 P	117	16.3	2	0.347	78
C194	2.35 Fe, 0.12 Zn, 0.03 P	120	16.3	7	0.263	65
C195	1.4 Fe, 0.1 P, 0.8 Co, 0.6 Sn	119	16.9	2	0.197	50
C197	0.6 Fe, 0.05 Mg, 0.2 P	118	16.8	7	0.32	80
C19750	0.6 Fe, 0.05 Mg, 0.2 P, 0.23 Sn	120	16.9	7	0.262	65
C505	1.25 Sn, 0.1 P	117	17.3	8	0.21	48
C70250	3 Ni, 0.65 Si, 0.15 Mg	131	17	2	0.172	40
C50710 (MF202)	2 Sn, 0.2 Ni, 0.15 P	113	17	11	0.15	30
PBR-2	6 Sn, 0.2 P	108	18	10	---	---
OFC	99.9 Cu	117	17.6	5	0.398	100
Silicon	Si	188	2.6	---	0.084	---
EMC	Low Stress Epoxy	14.7	20 to 24	---	---	---

The thermal coefficient of expansion is the fraction of the initial length a material will expand per degree. Thermal conductivity is the relation of thermal flux to thermal gradient and is a measure of thermal energy which can be dissipated for each degree difference in temperature. Electrical conductivity, the reciprocal of resistivity is a measure of the ease of passing electrical current through a material and is given in % IACS, the percent of the electrical conductivity of the International Annealed Copper Standard (100% IACS).

Strength and Formability: High strength leadframes are desirable but attempts to increase the strength of a material usually results in a loss of ductility and lower electrical and thermal conductivity. Optimum elongation of ≥ 4% is generally desired for good formability and resistance to lead bend failure (6). Of the methods available to increase strength, only grain size reduction increases strength with an acceptable decrease in percent elongation. Deformation of the leadframe alloy below the recrystallization temperature generally produces a reduction in grain size. This is accomplished through the reduction in the thickness of the alloy strip by cold work/annealing cycles.

Temper designations are arbitrarily assigned to different tensile strength ranges produced by different percent reductions in thickness. 1/4 hard, 1/2 hard, 3/4 hard, hard, extra hard and spring hard are typical temper designations. Hard tempers are most often used for leadframe manufacturing. A 0.02" annealed metal rolled down to 0.01" would represent 50% reduction (7). The leadframe material behaves anisotropically subsequent to cold working. When bending the material, the bend axis perpendicular to the direction of the rolling displays an increase in formability over the axis parallel to the direction of rolling. The perpendicular axis is referred to as "good way" bending and the parallel axis is referred to as "bad way."

Lead Bend Fatigue: Metal fatigue resistance is an important quality in leadframe material. Bending occurs in trim and form operations as well as inadvertent bending in handling, which requires further bending to straighten out. Any cracks in the leads during this bending compromises the reliability of the device and must be rejected. This is known as lead bend fatigue, LBF.

Mil-Std-883, test method 2004-B2, describes the test used to monitor LBF; the material must complete three full 90° bending cycles without cracking. The quality of the cut edges of the material should be taken into account as nicks, slivers and other defects can be sites for crack propagation and affect the test results. Alloy-42 is the most resistant to LBF, but is twice the cost of Cu alloy materials, and has poor thermal and electrical conductivities. The Cu alloys are typically adequate in LBF resistance and increased LBF resistance is seen with cold working.

Softening Resistance: One challenge in developing alloys for leadframe material is to increase the softening resistance. Softening occurs at some annealing temperature where recrystallization occurs. The result is a large drop in strength. 99.9% Cu softens below 200°C, an unacceptably low temperature, within the die attach cure temperature of many die attach compounds. Small additions of other elements to copper has a marked effect on the softening resistance. Adding just 0.06% Ag to Cu increases the softening temperature to over 320°C. In all copper alloys the higher the temper, the lower the softening temperature for a given alloy. Alloy-42, the only widely used non-Cu leadframe material, is the most resistant to softening followed by C195, C194, C151, C155 and finally C110, 99.9 % Cu. The relationship between hardness and temperature is well known for a variety of leadframe materials (8).

Besides Ag, elements commonly added to copper to increase the strength and softening resistance include Co, Ni, Fe and Sn. Alloying elements present in the alloy as solid solutions will greatly decrease both the thermal and electrical conductivity. Alloying elements present within finely dispersed precipitates add strength to the material without deterioration of the thermal or electrical conduction. This can be accomplished by heat treatment of certain alloys to bring about the controlled precipitation of a second phase.

2.4 Leadframe Design and Structure

2.4.1 Introduction

The design of a leadframe contains many general features that are found in most leadframes, regardless of the application or package. It also contains features that are specific to package configuration, size, and end use. The features also relate to the actual manufacture of the leadframe and package. For instance, most leadframes are available in either strip or reel form, with each site connected by the rails. These rails provide stability during processing, electrical continuity for pre-plating, and allow the leadframes to be handled automatically by the processing equipment.

In considering the design of leadframes, it is helpful to review the exact purpose of the leadframe in the manufacture and end use of the packaged device. Throughout the entire assembly process, the leadframe plays a major role in the reliability and manufacturability of the final product. In a sense, it is the basic structure around which the entire package is built around. Some of the reliability and manufacturing issues that are influenced by the leadframe design are:

- delamination,
- moisture penetration/corrosion,
- stress,
- outer lead beam strength, and
- thermal conductivity.

As the various general and special features of leadframes for plastic packages are described, their relation to the above mentioned reliability and manufacturing issues will be emphasized, as well as function and other information. Other issues, such as design differences due to stamping vs. etching and fine vs. coarse pitch will also be related.

2.4.2 Basic Features

The basic features of leadframes are listed below. Each has a function that is critical to all leadframes used in plastic packages. There are some instances where one of these basic features may be either absent or drastically redesigned in some special packaging configurations.

Rails/Strip: The purpose of the leadframe strip is to hold a specified number of frames together for processing. This is primarily accomplished by manufacturing the leadframes attached together by rails on either side of the strip.

The strip rigidity depends heavily on the width of the rails; in general between 80 and 300 mils wide. This is especially critical for fine pitch applications where leadframe thickness is typically thinner than coarse pitch leadframes, 6 mils vs. 10-15 mils. Interdigitated frames (IDF) are a type of leadframe design, typically used for DIPs, which maximizes the area on the strip by meshing the outer leads of each unit with its adjacent units on the strip.

Outer Leads: The purpose of the leadframe outer leads is to provide a terminal connection to the printed circuit board from the IC. The leadframe outer lead pitch and configuration are set by the type of package and end use. For example, molded DIPs, which are typically inserted into PCB through holes, require only one bend, whereas a surface mounted package, such as a PLCC or QFP, may require more complex bending. Table 2-4 lists the various package types and their type of lead deformation.

Table 2-4: Lead deformation

Package Type	Lead Deformation	Number of Bends
SOT	Gull wing	2
SIP	Straight	0
MDIP/PDIP	90°	1
ZIP	Zigzag	2
SOP	Gull wing	2
PLCC	J-bend	2
SOJ	J-bend	2
PQFP	Gull wing	2
TO	Straight/Bent	0-2

The outer leads need to be designed with the appropriate thickness as well as material and metallurgy, to withstand the various processing and assembly stresses.

Dambar: The purpose of the dambar is to stop plastic flow, prevent mold flash and hold the leads together until the trimming operation. This is accomplished by designing a bar into the leadframe that extends around the perimeter of the desired packaged outline. In general, the dambar width should be approximately twice the leadframe thickness. In the special case of fine pitch applications, dambar width should be kept larger than 15 mils. The dambar should be located close enough to minimize flash, but far enough from the package outline to allow for deflash during trimming.

Inner Leads: The purpose of the inner leads is to provide bonding targets and an electrical path to the outside environment from the chip. In designing the inner lead configuration, considerations must be given to lead pitch and spacing based on material thickness, manufacturing method, coining, and optimum Beam Strength Ratio (BSR). The BSR is a function of the lead dimensions as given in the following equation:

$$BSR = [thickness/width] \times length$$

The BSR is a measure of a lead's resistance to lateral deflection. In general, a low BSR (< 1) is better than a high BSR. It is also used in determining the need for taping of the leads for stability. Allowing for the largest (widest) possible cross section for a feature helps keep the BSR low. In most conventional packages, the leads are radially aligned such that they are divergent away from the die attach pad. For stamped frames, the minimum spacing and width are approximately the material thickness. Table 2-5 lists the general design rules for lead spacing and width for etched leadframes.

The lead tips should be fabricated to have sharp corners for a clearly defined bonding area. The design of the inner leads should always account for metal deformation or lead growth effects on metal-to-metal spacing. These effects arise from the coining operation. Jahsman (9) discusses the limitations on bond densification and die size imposed by leadframe design. The result is a variable center, variable radius inner lead layout, sometimes noted as fanout, which helps keep constant bond pad pitch on the die and lowers the angle of attack between the wire and the lead tip orientations of the second bond. This is currently used in most fine pitch QFP, PLCC, and other quad designs.

Table 2-5: Lead spacing and width for etched leadframes

Material Thickness (mils)	Lead Spacing (mils)	Lead Width (mils)
10	6	5
8	5	5
6	4.1	4
5	3.7	4
4	3.3	4

It should be noted that deflection of the inner leads can occur vertically during the molding operation. This arises from the different flow rates of EMC between the two halves of the mold cavity. In most coarse pitch low lead count packages, this is not a problem. However, with decreasing package size and increasing I/O, this becomes a problem. Suhir and Manzione (10) evaluated the maximum stresses and deflections, and found that lead deflection is proportional to the fifth power of lead length and the inverse third power of lead thickness. Equations for determining maximum stresses and deflections given material and process parameters are also given.

Die Attach Pad/Flag: The purpose of the die attach pad (DAP), or flag, is to provide an area of support for the chip in the package. Typically, an epoxy is used to attach the chip on the pad. It also serves secondary purposes of promoting heat transfer from the chip to the leadframe and providing overall stability. In most cases, the DAP is part of the leadframe itself, stamped or etched out during the manufacture of the leadframe. There are special cases where a DAP is not used. Suzumura, Kawamura, and Tubosaki (11) describe the development of a special leadframe for the Chip-On-Lead package technology. Using the special leadframe, the chip is directly attached to the inner leads via a non-conductive polyimide film. The chip is wirebonded on two sides of the chip. This leadframe allows for the use of a few standard widths with varying lengths for packaged DRAMs of increasing memory size.

In many plastic packages, the DAP is "downset" from the plane of the outer leads. This is accomplished using tooling specially designed to lower the DAP by forming the tie bars. The purpose of downsetting the DAP is to bring the top of the die to the same plane as the top of the inner lead tips. This provides easier more reliable wire bonding to be performed and minimizes wire sweep.

Tie Bars: The purpose of tie bars are to provide stability for the DAP. They are usually the only link between the DAP and the rest of the leadframe. They usually extend beyond the package outline. A general guideline for tie bar width is no smaller than 150% of the material thickness. Notches and fishtail are incorporated to facilitate trimming. As mentioned above, the tie bars are formed to lower the DAP when downsetting is required. The downset angle is typically 30°.

Indexing Holes: The purpose of indexing holes on the rails of the leadframe is to provide a reference point and facilitate automatic handling of the frames. In such cases where automated machinery and reel supply is used, they allow the frame to be indexed to the next site when processing, such as wire bonding, is complete on a site. In most cases, location of indexing holes is specified for the particular package configuration by international standards organizations such as JEDEC and EIAJ.

2.4.3 Special Features

This is a list of special features that may be found in most leadframes. In most of these cases, the features serve a secondary purpose above and beyond the basic purpose of the leadframe. For example, reducing distortion in the leadframe is considered a secondary purpose to the basic purpose of providing electrical connection. These special features, although not considered basic in this report, are in most cases critical to the packages that use them.

Expansion Slots: The purpose of expansion slots is to reduce leadframe distortion due to thermal stresses during the molding process. They are used in cases where there is wide metal and relatively low material thickness. Slots also help in reducing oil canning problems with stamped frames when wide metal areas occur larger than about 0.040". There is no set rule for the number of expansion slots except to say that there can never be too many. Minimum width is generally between 100 to 150% of the material thickness. The slots are usually symmetric along the long and short axis of the leadframe strip. Sometimes, square holes are also used in addition to slots.

Locking Features: The purpose of the various locking features found on leadframes is to provide improved physical adhesion between the epoxy molding compound and the leadframe. A by-product of the improved adhesion is a higher resistance to moisture ingress via the EMC/leadframe interface. These features are usually present in the following leadframe features:

- locking holes on inner leads,
- locking holes on the tie bars,
- locking holes on the DAP,
- anchors/hooks,
- dimples,
- scallops, and
- fishtail.

In general, locking holes on inner leads are rectangular-shaped. They seem to be used as the primary locking mechanism in most frames, due to the relatively short path for moisture ingress through the leads. They should be kept at a minimum of 0.008" from the package outline and are size-limited to the location on the leadframe and the manufacturing process. Locking holes on the tie bars work in much the same way as those on the inner leads. They are often combined with what is known as "fishtail." Fishtail located at the end of the tie bar farthest from the DAP. It allows for the expansion of the leadframe without bending when the leadframe is first placed into the mold. The temperature difference between the leadframe and the mold is great initially and accounts for DAP shift due to thermal stresses. Fishtail and other designs are supposed to absorb deformation and keep the DAP level. Most leadframe manufacturers prefer anchors over locking holes, especially for stamped frames. Square holes are usually preferred over round holes in those cases. In general, the locking hole diameter should be approximately 150% of the material thickness.

Dimples/Scallops: Dimples and scallops are listed above as alternative locking features to locking holes on inner leads. They help anchor the DAP to the EMC. The minimum size and spacing of dimples on the DAP depend upon the method of manufacture. Dimples on stamped frames are approximately 0.004" across and are roughly 1/10 the thickness of the material depth. For etched frames, the dimple depth is approximately half the material thickness. The diameter is 100% of the material thickness.

A scallop is an intentional regular protrusion of metal from the DAP. It is an alternative locking feature that solely aids in mechanical adhesion between the leadframe, via the DAP, and the EMC.

V-Notches: V-notches allow for easier separation of the package from the rails. It is usually only used in stamped leadframes for coarse pitch applications. This is because stamped, coarse-pitch leadframes use the thickest material. The notch is generally located on the tie bar near the package outline. No V-notches are used in fine pitch stamped frames or etched frames.

V-Grooves: The purpose of the V-grooves is to improve adhesion between the inner leads and the EMC. The grooves run perpendicular to the leads in the plane of the frame. They must be located no closer than 0.005" from the coined surface of the inner lead and no closer than 0.003" from the package outline.

Tape: The purpose of taping the inner leads is to maintain lead position during processing and assembly. Determining whether and how a frame needs to be taped is based on the BSR and customer specifications. Typically, tape is used in certain high lead count, fine pitch applications where long inner leads are needed. The standard size of tape width ranges from 0.040" to 0.060" wide. Most tape is on the order of 0.002" thick with less than 0.001" of adhesive. It is usually applied on the plated side of the frame. The tape material should be able to withstand the thermal processing that most leadframes see during assembly and end use. Polyimide tape is used widely.

2.4.4 Effect on Reliability

Delamination: Delamination or package cracking can be avoided by utilizing a number of the features above in the leadframe design. One cause of delamination is poor adhesion between the leadframe and the EMC or die attach material. This can be alleviated by utilizing some of the locking features, such as inner lead locking holes, dimples or scallops on the DAP, anchors on the leads or tie bars, and fishtail. Additionally, accounting for other areas of

stress concentration in the plastic package that arise from leadframe desig:. can greatly improve package cracking resistance. The locking configurations basically reduce the mean leadframe/EMC interface area by placing "pillars" of EMC through the leadframe, which provide crack propagation barriers.

Moisture Penetration/Corrosion: A related issue to delamination is moisture/ion penetration into the package. The rapid heating that the package sees during surface mounting can lead to delamination and package cracking via expansion of vaporized moisture that collect at the surface. The same moisture can dissolve ions from the EMC which help corrode parts of the interior of the package. The locking holes placed on the inner leads and the tie bars help improve adhesion and reduce the available area of interface, thereby reducing the amount of ingress of moisture due to capillary action.

Stress: Stress is always present in the manufacture and use of a plastic package. The leadframe is under a myriad of stresses when it goes through the manufacturing and assembly processes. For this reason, features such as expansion slots are incorporated into the leadframe. Excess stress becomes a problem in many fine pitch, high I/O designs. To avoid the buckling that can occur in leadframes made with thinner material, i.e. fine pitch, expansion slots are placed in the wide metal areas, i.e. rails. During heating, these slots help reduce the buckling associated with expansion stresses in the leadframe. These slots also help reduce the buckling that can occur after molding during cooling.

Another design solution for stress-related problems is to strengthen the leadframe by design. Optimizing the BSR can help alleviate lateral stress problems by strengthening the lead. Taping the leads can also help by making the movement of one lead dependent on the others, thereby increasing the stress required for deflection.

Outer Lead Beam Strength: Outer lead problems such as lead bend fatigue and lead break are generally material issues, but design can also help to correct them. Designing thicker, wider outer leads with larger bend radii can help eliminate lead break problems by decreasing the stress imposed on the lead.

Thermal Conductivity: The thermal characteristics of a plastic package depend on many factors. Leadframe design plays a prominent role in the thermal characteristics of the package. The use of wide leads (large cross-sectional area), heat spreaders, and redundant leads helps in the transmittal of thermal energy away from the interior of the package. Wide leads lower the resistance of the leads. Heat spreaders attached to die attach pads help provide maximum external surface area for radiation and convection cooling. The redundant leads provide more cross-sectional area for maximum heat transfer. Sub-section 2.4.5 contains an example of the use of an expanded DAP, redundant leads, and a heat spreader in a medium to high power application.

2.4.5 Application/Package Specific

Lead counts for specific packages: Table 2-6 is a list of plastic package types, lead count range, lead pitch, and applications.

Medium to high power: In these applications, the important issue is thermal dissipation. The thermal resistance of a package from junction to ambient, θ_{ja}, is used as a general indicator of the thermal dissipation capabilities of packages. Packages with good thermal capabilities, i.e. lower θ_{ja}, are generally used for these applications, such as SIPs, DIPs, TOs, etc. In general, high power packages are characterized by thick leads made of materials with good thermal conductivity, such as copper alloys. The larger cross sectional area of the leads lowers the thermal resistance of the leads and the package overall. In many cases, heat spreaders are preferred to enhance the removal of thermal energy from the interior of the package. The heat spreaders are generally made of copper or some other low thermal resistance alloy and plated to improve environmental resistance. They are usually attached to either the back side of the die, some or all of the leads, or both. Kasem and Feinstein (12) describe a non-conventional molded DIP for medium to high power applications. It exhibits improved θ_{ja} through leadframe modification by integrating the DAP with some leads and creating a web to which an external heat spreader may be applied.

Multi-Chip Packages (MCP): The trend toward higher clock speeds, increasing memory sizes, and decreasing PCB landscape has driven the need for integrated multiple chip packaging as one solution. The question of how to make a MCP economically is one that is the subject of much debate and research. Many agree that plastic packaging will play a major role in future MCP solutions. Currently, many companies select the QFP as the package of choice for their integration.

This brings up the issue of how to efficiently package multiple die. One of the approaches that can be used is altering the leadframe to fully utilize the space available within the package. By integrating the leadframe and substrate both mechanically and electrically, thereby eliminating the DAP, the process can be simplified and more package real estate can be gained. There are two approaches to doing this. The simpler method involves physically and electrically bonding the lead tips to pads on the outer edge of the substrate. This creates an electrical connection as well as providing a die attach substrate. The other method involves the integration of the leadframe as the center layer of a multiple layer substrate. This method uses through-hole plating and other PCB techniques to accomplish the same goal.

Table 2-6: Plastic packages

Package Type	Lead Count	Lead Pitch (mm)	Application
SOT	3	3.0	Diodes, transistors
SIP	3-12	2.5	Power transistors, Darlingtons plus control logic
MDIP/PDIP	8-64	2.5	Linear, logic, DRAMs, SRAMs, microprocessors, ROMs, PROMs, gate arrays
ZIP	16-24	1.3	DRAMs, SRAMs
SO	8-28	1.3	Linear, logic, SRAMs
PLCC	18-24	1.3	DRAMs, logic, PROMs, microprocessors, gate arrays, standard cell
SOJ	20-26	1.3	DRAMs
PQFP	88-200	0.6	Gate arrays, standard cell logic
VSOP	16-30	0.6	DRAMs
VSQF	32-100	0.5	Gate arrays

2.5 Leadframe Manufacturing

2.5.1 Introduction

In this section leadframe manufacturing methods are described. Advantages and disadvantages of the different techniques are compared for various leadframe requirements. Reliability issues related to manufacturing are discussed at the end of the Sub-section.

The basic leadframe manufacturing sequence is as follows:

- Pattern leadframe geometry out of alloy sheet or strip
  - Stamped leadframes
  - Etched leadframes
- Plate leadframes
  - internal leads, enhance bondability
  - external leads (before or after IC assembly)
- Tape internal leads (optional)
- Downsetting (optional)

There are two main methods of producing leadframes; they are either stamped out of the base material or photochemically etched out of this material. Stamping is a high initial cost process which is low cost per part for high volumes, in the millions of parts. Leadframe production targeted for high speed, high volume is best suited for stamping. On the other hand, designs requiring fine pitch and thin leads are better suited for etch manufacturing. Distortion of the material is more likely when stamping thin, fine geometry material. High lead count leadframes, with many features, require multiple passes through stamping presses which can lead to registration problems. Etching is more easily performed on these higher pin count leadframes. Low volume builds lend themselves to etching because the hardware set up is less expensive.

2.5.2 Stamping Leadframes

Advantages and disadvantages of stamping leadframes, process description, and problems arising from stamping will be discussed in this Sub-section. High volume production of leadframes is suitable for stamping if the design is not too complicated. High pin count leadframes will require more process characterization to stamp. Stamping is most appropriate for gross to moderate geometries and moderate to thick leadframes. The stamping press is set up in a reel to reel format where material is removed from the alloy sheet using punches and dies. Inspection of stamped leadframes is critical. Such defects as burrs, slug marks, toll marks, and others, can result from improper tool care or adjustment.

Table 2-7: Stamping leadframes

Advantages	Disadvantages
Low cost for large volume production	High initial cost, not for small builds
Requires a small equipment footprint	Induces stress in the leadframe
Reduces process steps; no masking	Difficult to stamp thin material without distortion
Automated process	Long leads of fine pitch are likely to be distorted

Benefits of Stamping: Table 2-7 gives a breakdown of the advantages and disadvantages of stamping leadframes. Stamping is the manufacturing process of choice for high volume production. It is less expensive per part and is much faster than etching for square foot of process area. Stamping becomes inappropriate at high lead count leadframes of fine pitch. These leadframes are necessarily thin and generally cannot stand up to the stamping while maintaining planarity.

Process Description: To maintain planarity, the strip first passes through a flattening tool or straightener. The straightener is usually a high force roller which flattens the material. The section of the strip to be stamped moves to the stripper plate where it enters a series of tungsten carbide punches and dies called the progressive die. First, the guide holes on both edges of the strip are punched out giving the material a reference point to each leadframe site. Pins entering the guide holes hold the strip in the proper location throughout the stamping process.

The material removed, or slugs, fall into the dies which are wider beyond the initial orifice such that the slugs pass through to a scrap bucket below. The strip is indexed to successive stations where punches and dies remove material until the final leadframe configuration remains. Often to maintain planarity, 30 to 75 mils of edge material is removed during the stamping. This edge region is the area with the greatest residual stress. Stamping presses are typically 20 to 40 inches long and hold from 40 to over 350 punches. The stamping press is set up in a reel to reel format. Presses are generally rated between 20 and 200 tons and run at speeds of up to a maximum of 1000 strokes per minute. Typical running speeds are between 250 strokes per minute, for higher lead count leadframes, to 800 strokes per minute for more simple structures.

Stamping Problems: Stress introduced during stamping is a major concern when using the technology. Quality of the punches and dies can sharply affect the product and maintenance of these parts, sharpening and replacement, is0 critical. Table 2-8 lists many defects resulting from stamping.

Table 2-8: Stamping-induced defects

Defect	Cause
Oversize inner lead pad	Excessive coining force
Cross bow	Stress in leadframe material
Edge burrs	Dull/worn punching tool
Tool marks	Broken/worn punch tool
Twisted leadframe	Low die to tool clearance

Stamped leadframes can generally be manufactured down to a lead position tolerance of ± 0.002". Stiffer material is easier to punch without distortion. Worn, chipped or rounded punches can cause burrs in the leadframes. A table of typical defect limits for the internal leads of a 40 pin leadframe are given in Table 2-9.

Table 2-9: Defect limits for 40 pin leadframe (13)

Defect	Permissible Limit
Lead twist	≤ 5.5°
Vertical deflection	+ 4 to - 6 mils
Lateral deflection	± 2 mils
Vertical burr	≤ 20 microns
Lateral burr	≤ 30 microns

2.5.3 Etching Leadframes

Leadframe etching is considered in this Sub-section. The advantages relate to complicated geometrical capabilities whereas the disadvantage mainly lies in the throughput as compared to stamping. The processing may either be reel to reel or sheet format. The stress-induced defects of stamping are not as prevalent in etching but the leadframes are bound by the same planarity and geometry issues. Photomask transfer can be a large source of defects.

Advantages of Etching Leadframes: The process of etching alloys into leadframes does not require the large initial cost for tooling which stamping needs. Listed in Table 2-10 are some advantages and disadvantages in etching leadframes.

Table 2-10: Etching leadframes

Advantages	Disadvantages
Quick turn for new design, fast set up	Complicated process, many steps
Easily define complicated/fine pitch patterns	Consumes much area/floor space
Easily handles thin material	More easily oxidized than stamping (wet processing)
Inexpensive for small lots (few 10,000s)	---

To change from one leadframe design to another requires a few $K for phototool design and a few hours to a few days for set up. The same change can cost hundreds of $K for the stamping set up. It takes months to have a new stamping tool made. The photochemical process allows for tight geometries to be etched without large amount of stress imparted to the leadframe. The material passes through many processes to clean, mask, etch, rinse, and dry. This processing takes a large footprint compared to stamping. With the wet processing the chance of oxidizing the leadframes is increased.

Process Description: Etched leadframes are processed in either reel to reel coils or sheet form. Subsequent processing is basically the same regardless of the starting shape. The incoming strip goes through pre-clean and activation steps, in chemical baths, removing any contamination and oxide. The material is covered with photoresist on both sides in either laminated sheet or liquid form. The strip is then brought into contact with a photomask which allows ultraviolet light to pass through those areas in which the resist, and hence, the metal is to be retained (negative photoresist). The patterned material then goes through jet etching. Corrosive chemicals flow through nozzles directed at both sides of the strip. The etched leadframes are etched from two sides. The etch is anisotropic, roughly 2:1 "etch factor". The 2:1 etch factor means that the system etches twice as fast in the Z direction as in the X or Y directions. Etching in the X and Y directions usually undercut the photoresist, so it is desirable to have an etch factor greater than 1:1 in the Z direction.

Etch process problems: Those same planarity and surface finish criteria given for stamping in Sub-section 2.5.2 hold for etched leadframes as well. The process itself tends to be more sensitive to uniformity of etching, where metal to metal clearance can be a problem, and mask transfer, where mask defects transfer onto the alloy.

Leadframe etching capabilities are listed in Table 2-11 for different material thicknesses. The numbers are typical and will vary among manufacturers. The minimum spacing is the space between surfaces of the leads. The metal clearance is the space between the closest points on the sidewalls of the leads.

Table 2-11: Etched leadframe capabilities

Material Thickness (mils)	Min. Lead Pitch (mils)	Min. Nominal Spacing (mils)	Min. Metal-Metal Clearance (mils)
4	7.0	3.0	2
5	7.4	3.4	2
6	7.9	3.9	2
8	8.7	4.7	2

After etching and rinsing, the alloy strip goes through resist removal. The resist is removed by running the strip through more nozzles, this time spraying resist removal chemicals. After rinsing and drying the etched leadframe is ready for final inspection.

2.5.4 Leadframe Backend Manufacturing

The back end processes which include plating, taping, and downsetting are crucial to the manufacturing of leadframes. These topics together with attributed problems will be briefly described.

Plating of Leadframes: There are two reasons that one might plate the leadframe. Plating of the inner leads with a pure metallic film enhances the wire bondability of the lead by providing a clean, fresh surface for bonding. Plating of the outer leads with a solder or other layer enhances the environmental protection of the lead and the solderability of the lead by completely coating the exposed leads. Usually, a leadframe will undergo both platings but not at the same time. For more description on plating and related issues, see Sub-section 2.6, Leadframe Plating.

Taping of Leadframes: Before shipping the leadframes, an adhesive which is typically a high temperature, polyimide tape is usually placed over the internal leads of the leadframe to hold them in place. This is most desirable in frames with small, long leads, or thin material as in high lead count or fine pitch applications. In practice, it is applied to the majority of leadframes over 20 leads.

DAP downset: The DAP is often downset to put the chip in the center of the package. This allows for equal mold compound on either side of the die. This way the rate of mold cavity filling is equal on either side of the die during molding. Forces due to molding acting on either side of the die tend to be equal and die shift is prevented. Also, because the surface of the IC is now lowered, there is less of a chance of edge shorts occurring. After processing, the leadframes are packed in coils (reels) or cut into strips, approximately 6 to 10 inches long, for shipping in cartridge form. A paper or plastic of width similar to the leadframe strip is interwoven between the strips for protection.

2.5.5 Reliability Issues

Table 2-12: Manufacturing processes and reliability

Failure Mode	Defect	Process Step
Bond or wire break	Lead twist	Stamping
	Lead tip non-planarity	Stamping
	Inner lead corrosion	Etching
	Blistering	Plating
	Bleed out	Plating
Lead shorting	Edge burr	Stamping
	Slug/tool marks	Stamping
	Oversize bonding pads	Stamping
	Insufficient clearance	Etching
Die lift	Blistering	Plating
	Peeling	Plating
	Contamination	Plating
	Nodularity	Plating

Each step of the leadframe manufacturing presents its own reliability problems. In this Sub-section each manufacturing step will be considered with reliability in mind. Table 2-12 presents a list of the reliability concerns associated with each step in manufacturing.

Reliability Concerns with Stamping: The lead tips will sometimes twist or bend, providing a distorted, non-planar, bonding surface. Bonding can still be performed due to the clamping which accompanies bonding. When the clamping is removed, however, stress will be placed on the ball bond and wire as the frame distorts once again. This can lead to broken wires and lifting ball bonds.

The tool-induced defects occur most often from worn or faulty tools. These defects can lead to shorting as pieces of metal are torn out of the desired position. Coining defects tend to enlarge the pad area of the inner leads increasing chances for contact with adjacent leads.

Reliability Concerns with Etching: The chemical nature of the etch process lends itself more prone to oxidation of the leadframes. The oxidation will not form as strong a bond to the wire as clean alloy, and the bond may fail. The photomasking of the leadframes in the etch process gives opportunity for mask transfer. Mask transfer opens holes in the photoresist where they should not be. Subsequent exposure to the etchant removes metal in these areas. The failures due to these holes could be numerous. Weakened leads could short, and holes in leads could cause opens.

Non-uniform etching can lead to metal clearance problems. Areas etching faster may have the correct clearance, while the slower etched area has leads which are too wide. Shorting can result from metal clearance problems.

Reliability Concerns with Plating: Blistering, peeling, nodularity, and contamination all have the end result of inducing poor adhesion of the wire bonds and/or the die attach. In both cases the wire bond is in jeopardy and opens can result. Contamination may also lead to corrosion and/or current leakage if the contamination is ionic in nature.

Bleed out occurs when the plating solution plates further up the leads than intended. The current is dispersed over a greater area and the deposit will be thinner. This could lead to poor bondability since a thinner metal deposit was made.

Reliability Concerns with Taping/Downsetting: Taping and downsetting tend to improve the reliability of the package. Taping holds the leads in the same plane resulting in less stress on the bonds. Downsetting results in reduced mold forces differential improving post-mold die positioning. Downsetting also reduces edge short by lowering the die surface with respect to the inner lead fingers.

2.6 Leadframe Lead Finish

2.6.1 Introduction

Plating of IC leadframes is discussed in this Sub-section. The purpose of plating the leadframes is followed by a description of plating methods. Reliability and cost related to leadframe plating is reviewed at the end of the section. There are three reasons for surface finishing of the leadframes:

- Enhance wire bonding to internal leads
- Enhance solderability of external leads
- Environmental protection of external leads

Internal leads are plated to enhance wire bonding in package assembly. Precious metal can be plated to the entire leadframe to accomplish this, but most often selective plating of the bonding area is used. Reduced metal consumption keeps costs down in this case.

External leads are usually plated, with tin/lead solder, after package assembly. Two variations from this are leadframes pre-plated by the manufacturer and assembled parts which get solder dipped or plated. The solder finishing of external leads not only improves solderability for mounting the chips on PWBs, but this same solder helps protect the leads from corrosive environments.

2.6.2 Leadframe Spot Plating

Internal lead plating with precious metal is most often accomplished by selectively plating the lead tips and DAP of the leadframe. Known as spot plating, the process represents a large cost savings over flood plating used in the past. Flood plating coats the entire leadframe with metal.

Process Description: Spot plating of leadframes is carried out on a reel to reel automated strip plating machine. Feed and uptake spools are set up at their respective ends of the equipment. Unplated leadframes are fed in and the plated leadframes are taken up on the exit reel. The strip is indexed from one station to the next until the entire reel has been processed. A new reel is attached to the last frames of the previous reel and the process continues without stopping. In a similar manner the take up reel is changed.

The distance indexed represents the physical length of the plating process and this is the length of the strip section which is plated at a given time. This is accurately measured to insure that every frame gets completely plated once. Pre-clean, activation, rinsing, and plating are carried out in series. Cleaning of the strip, prior to plating, often incorporates a chemical clean or degrease and/or an electroclean. In the electroclean, current is passed through the strip, across a chemical bath, dislodging any oxidation which may be present on the material. The strip is next indexed to a rinse bath removing any residual cleaning chemicals.

In masking off the area not plated, a hard mask is used. Made of plastic or other chemically resistant material, the mask is automatically clamped to the leadframe strip such that only the internal leads are exposed to the plating solution. Typical plating time is a few seconds at over 1000 $Å/ft^2$. After the high current plating, the mask plate releases the strip, which is then indexed for the next section to be plated.

The plated section next goes through a rinse station. Rinsing at this stage is a recirculating drag out rinse so that the precious metal in solution on the strip may be reclaimed. After rinse, the strip receives a hot air dry to remove residual water immediately; slower drying can cause oxidation of the non-plated material. The strip is taken up on the exit reel and is interwoven with a protecting paper strip. Some manufacturers will plate a pure copper layer over the alloy prior to spot plating. In this way, the material being plated on is uniform and consistent.

Materials Used in Spot Plating: Gold, silver and copper have all been used in spot plating but silver is most commonly used. Silver does the best job for the cost and reliability, and has been proven many times over. Gold works well and is commonly used, but the cost has become prohibitive, particularly in the present day IC competitive market.

Copper has been effectively spot plated for bonding enhancement, but with copper oxidation is always an issue. Handling and storage of leadframes has to be done in a manner to insure the frames don't oxidize (14). For these reasons, assembly houses prefer to use silver spot plated leadframes.

Costs: Part of the reason that spot plating today uses silver is for costs purposes. Silver is relatively cheap when compared to gold, yet reliability testing is good with silver. No increased constraints on storage are needed with silver and therefore cost is the main difference. At 1/100 the price of gold, silver can be spot plated to leadframes for material costs of less than $0.01 per frame.

Reliability: Gold wire bonding to unplated leads can result in low bond pulls when testing the wire bond pull strength. The level of bond pull degradation largely depends on the history of the leadframe prior to bonding and the bonding stage temperature. These factors affect the rate of oxidation growth. Copper and copper alloys readily oxidize and this oxidation can form a scaly surface with easily breaks free and lifts. Precious metal plating over the alloys prevent oxidation formation. Bonding to this surface is consistently strong and reliable.

The plated leadframe must be inspected for defects. Peeling, blistering, or contaminated plate deposits can give poor bonding strength and field failures. Overly rough or nodular plating can give poor bonding and lead to reliability problems.

2.6.3 External Lead Plating

External lead plating will be discussed in this Sub-section. This plating enhances the solderability of the IC package when mounting to a PWB and also acts as an environmental barrier protecting the leads. Description of processing and materials will be followed by discussion of reliability and costs.

Process Description: Solder is applied to the external leads of the leadframe in one of the following three ways:

- Plating of the leads after package molding (traditional)
- Molten solder dipping of the package
- Pre-plating of the leadframes prior to assembly

Traditionally solder plating occurs after package molding. The leadframe strip, with external leads still shorted together, is plated in a large plating bath. Large plating racks are loaded with strips, and the rack is automatically moved through the solution. The plating rate is set so that when the rack reaches the end of the plating tank, the plating is completed. Many racks are plated at a time.

Some older processes do not use electroplating but dip the molded and singulated parts into a molten solder bath. The parts are automatically loaded into a solder resistant basket which carries the packages through the solder. The solder only adheres to the external leads.

A new pre-plated frame process is being used by many companies, where the leadframes are reel to reel plated prior to assembly. Plating of solder on leadframes is carried out in a reel to reel plating station. It is done in a manner similar to precious metal spot plating except the mask is reversed. The internal leads should remain solder free and the external leads get plated. The mask encloses the internal leads and has openings for the external leads.

Materials Used in External Lead Plating: The protective coatings applied to the external leads are generally a solder material that helps in achieving good solderability. The material used in strip plating and pre-plating frames is usually a SnPb alloy with 85% Sn and 15% Pb nominal composition. Solder dipping uses a eutectic composition SnPb alloy with 63% Sn and 37% Pb.

Reliability in External Lead Plating: Many reliability issues arise with solder finishing of the external leads. The main concerns are by process:

- Strip Plate
  - Exposed alloy due to handling scratches
  - Solder whiskering
  - Solder peeling

- Molten Solder Dip
  - Delamination of mold compound from leadframe
  - Solder peeling
  - Solder bridging
  - Solder voids

- Pre-Plated Leadframes
  - Solder cracking
  - Solder peeling
  - Solder whiskering

Due to the excessive handling in strip plating, the solder can often be dislodged and result in shorting and alloy corrosion. The plated solder can sometime form whiskers which, in severe cases, can also cause shorting.

The temperature excursions seen in solder dipping can cause delamination of mold compound to the leadframe. This is caused by CTE differences and can allow moisture to enter the package which may start corrosion. The solder on the leads can also peel and short, or improper wetting may lead to voids in the coating or bridge across leads.

Pre-plated leadframes are particularly susceptible to solder cracking. Since the solder goes on while the leadframe is unformed, the trim and form operations place a great strain on the solder coating. These frames will also be susceptible to the peeling and whiskering of the strip plating process.

Cost Comparison: The most economic process is to use the pre-plated leadframes. This simplifies the assembly a great deal, plus reduces assembly time. Payback is seen in process reduction as well as cycle time improvement. Not all leadframes lend themselves to pre-plating and many qualified assembly processes cannot use pre-plated leadframes. While the cost of molten solder dipping is comparable to strip plating, the temperature excursion is great and can damage some devices.

2.6.4 Lead Plating and Reliability Issues

Lead plating is largely done to improve reliability. The processes involved can often induce reliability problems of their own. This Sub-section will present a discussion of each method of lead plating and the reliability issues associated with each.

Plating of Internal Leads: Precious metal plating over alloys prevents oxidation formation. Bonding to this surface is consistently strong and reliable. Defects in the plating can lead to reliability problems. Some plating defects are:

- Blistering
- Peeling
- Contaminated
- Incorrect metal thickness
- Rough or nodular deposit

These defects can lead to failures which include die delamination, wire bond lifting, and lead tip oxidation. Inspection of the finished leadframe can keep these defects out of the IC package.

External Lead Plating - Solder: The external lead plating of IC leadframes tend to be more of a reliability problem than is the internal lead plating. The exposure to the environment increases the likelihood of the plated solder getting scraped off. The severe bending of the leads after plating causes large strain in the solder deposit which can lead to cracking of the solder. Also solder is susceptible to whiskering where metallic whiskers extend from the deposit. The following failures summarized in Table 2-13 are associated with solder finishing of the external leads:

Table 2-13: Solder deposition and failure modes

Process	Defect	Failure Mode
Strip Plate	Handling scratches	Corrosion
	Solder whiskering	Lead shorting
	Solder peeling	Lead shorting
Molten Solder Dip	Delamination (EMC/leadframe)	Wire breakage and package cracking
	Solder peeling	Corrosion/shorting
	Solder bridging	Lead shorts
	Solder voids	Corrosion
Pre-Plated Leadframes	Solder cracking	Corrosion/shorting
	Solder peeling	Corrosion/shorting
	Solder whiskering	Lead shorting

The defects where the underlying alloy is exposed, e.g., peeling, scratches, cracking and voids in the solder finish, become susceptible to corrosion. Defects where solder can lift and cause flakes, which can then redeposit, increase the chances of lead shorting.

2.7 Leadframe Manufacturers

2.7.1 Domestic Manufacturers

When trying to separate between domestic and foreign leadframe manufacturers, one should note that a clear distinction cannot be easily made. Like many other industries, many so called "domestic" corporations use overseas

or foreign-based subsidiaries to perform some or all the manufacturing processes. In this report, we will treat domestic suppliers as those companies that are headquartered within the United States. Table 2-14 lists domestic leadframe suppliers.

Table 2-14: Domestic leadframe suppliers

Company	Manufacturing Type	Location
DynaCraft	Stamped, etched	Santa Clara, CA
Leading Technologies	Stamped, etched	Leechburg, PA
Texas Instruments	Stamped, etched	Attleboro, TX
Contact International	Etched	Santa Clara, CA

2.7.2 Foreign Manufacturers

Table 2-15 lists foreign or overseas leadframe suppliers.

Table 2-15: Foreign leadframe suppliers

Company	Manufacturing Type	Location
Quality Platers (QPL)	Etched	Hong Kong
Sumitomo	Etched	Japan
Toppan	Etched	Japan
Gotoh	Stamped	Japan
Shinko	Stamped	Japan
Dai Nippon	Etched	Japan

3.0 DIE ATTACH

3.1 Die Attach Materials

In this Sub-section, die attach materials will be discussed, with emphasis on those used in plastic packages. A critical part of the manufacture and reliability of a plastic-encapsulated IC is the attachment of the device (die) to the leadframe. In most cases, a die attach material (D/A) is applied to either the die or the die attach pad (DAP) to help glue the die to the DAP. The die attach material helps to hold the die in place for subsequent wire bonding and end-of-line processing. It also provides a critical interface between the die and the leadframe, across which both thermal and electrical energy can be transferred. Depending upon the application, the D/A needs to possess certain properties to help perform its functions within the plastic-encapsulated device. Additionally, the type of processing necessary to deposit such material is important in determining its reliability and applicability in certain situations.

In choosing a die attach material, consideration must be given to the application and environment in which the package will be used. For example, if the die is to be enclosed in a ceramic package with sealed lid, the die attach material should be able to withstand the higher temperatures, i.e. 350 - 450°C, associated with the lid sealing operation in hermetic packaging. In such a case, hard solders would be used because of their high temperature stability. The following is a list of possible considerations for choosing die attach material:

- electrical conductivity,
- thermal conductivity,
- cure temperature,
- ionic impurities content,
- reworkability,
- viscosity,
- long term aging.

Electrical Conductivity: In some cases, due to device electrical reliability or functionality, it is desirable to have electrical conduction through the backside of the die to the DAP. This helps to decrease the inductance of packages, which is dependent on lead length to the ground plane. Some discrete devices utilize the backside as a primary connection for one of the device terminals, thereby making it absolutely necessary to have conduction through the backside. Electrical conductivity is a problem with organic and glass adhesives because of their inherent non-conductivity, but can be achieved by using conductive metal filler in the material.

Thermal Conductivity: Since one of the primary paths of heat conduction in ICs is through the backside of the die to the leadframe in a plastic package, it is important that the die attach material possesses the appropriate thermal conductivity. This factor is interrelated with electrical conductivity. Thermally conductive fillers can be either metal or inorganic, depending on the requirement for electrical conductivity as well.

Cure Temperature: The cure, or alloying, temperature determines the maximum temperature that the device can be subjected to after the die attach process. However, in the case of organic materials, the breakdown temperature is often higher than the cure temperature. The curing schedule will also determine the material properties after cure (15). This is a concern that is especially critical in organic and glass adhesives. Corrosion is always a concern with respect to ICs. Ionic impurities that are extractable by water contribute to rapid corrosion of aluminum, which is the primary metal used in devices. Thus, reducing the amount of ionics present in the package will greatly reduce the risk of corrosion. A common measurement method is using water extract conductivity measurements, such as an ion chromatograph (16). With the advent of multi-chip packaging, a reworkable die attach material has become a very desirable commodity. Reworkability will reduce scrap costs related to substrates and die. Viscosity is a processing concern with organic adhesives that would be automatically dispensed, such as from a syringe. A relatively low viscosity is desirable to help avoid void formation during the dispensing process. These voids can become sources of delamination, debonding, and package cracking.

3.2 Cost and Availability

Supplier issues facing die attach materials are less critical than with molding compounds since there are several domestic manufacturers providing a number of products in the world market.

Table 3-1: Reliability issues related to die attach materials

Reliability Issue	Related D/A Material Issue
Delamination/Package Cracking/Moisture Penetration	CTE Hardness Fracture toughness Oxidation/degradation of D/A Voiding Resin bleed
Stress/Die Cracking	CTE Hardness Compliance Die shear strength Fatigue
Corrosion	Outgassing Ionic content
Thermal Management	Thermal conductivity Voiding

3.3 Reliability

The die attach material can affect the reliability of plastic-encapsulated devices. Table 3-1 lists some of the reliability issues that are affected by die attach material properties. Many of these issues are related to the effects of thermal processing during and after assembly. For example, die cracking typically arises due to thermal expansion stresses resulting from the mismatch in coefficient of thermal expansion (CTE) between the Si and the D/A or leadframe during temperature cycling.

3.4 Brief Description of Some Failure Issues

Delamination/Package Cracking: Delamination is the physical separation of two adjoining layers. It can be considered as an internal crack within the package. It can occur in a number of areas in the package, including the DAP/EMC interface, DAP/die attach/Si interface, and the EMC/Si interface. Delamination can occur due to either the effect of CTE mismatch between materials during thermal cycling, or the collection and subsequent vaporization of moisture at an interface. In the latter case, package cracking is almost inevitable. This type of delamination commonly occurs during the surface mounting of components to printed circuit boards (PCB), where the components are rapidly heated. In both cases, adhesion is the key to solving these problems.

Corrosion: In both hermetic and non-hermetic packaging, corrosion of the outer leads and internal areas is a major concern. It plays a major role in the reliability of the electronic device. The most prevalent areas for corrosion are the outer leads, bond wires, device metallization (including bond pads), and inner leads. The exposure of these areas to both moisture and dissolved ionics is needed to cause corrosion problems. With respect to D/A, especially organic materials, outgassing during curing can deposit volatile species on the device. These species may contain ionics and other constituents, which can induce or exacerbate conditions for corrosion. Thus, the need for very low ionics content, and low solvent and volatiles levels in the polymers. In plastic packaging, the problem becomes much more complex because of the porosity of the EMC and the higher probability of impurities in the EMC. Many solutions can be implemented to correct or alleviate the corrosion problem. For example, special coatings deposited on assembled parts can help to provide some protection to the device and bond wires. Delamination and package cracking contribute to corrosion by allowing a faster path for ion-laden moisture to penetrate.

Thermal Management: Heat dissipation can be a critical issue, especially with power devices. Above a given operating temperature, a device will not run optimally and eventually breakdown prematurely, caused by uncontrolled migration of the dopants within the device. In addition, the bond from the pads to the bond wires will become weak, and lost due to intermetallic growth at elevated temperatures. This phenomenon is accelerated in plastic packages because of the presence of bromine (Br) and antimony (Sb) as flame retardants in the molding compound.

3.5 Requirements and Specifications

This Sub-section will cover some of the testing and requirements currently specified in industry. Mil-Std-883D, method 5011.2, addresses the supplier requirements related to organic die attach adhesives for use in military parts (17). It outlines the relevant inspection and acceptance criteria for organic or polymeric adhesives used on microelectronic devices. The following list outlines the properties to be tested, both for cured and uncured adhesives, as outlined by Mil-Std-883D, method 5011.2.

Uncured adhesive properties:
- Materials
- Viscosity
- Pot Life
- Shelf Life
- Infrared Spectrum

while for

Cured adhesive properties:
- Adhesive Cure
- Thermal Stability
- Filler Content
- Outgassed Materials
- Ionic Impurities
- CTE
- Thermal Conductivity
- Volume Resistivity
- Dielectric Constant
- Dissipation Factor
- Sequential Test Environment.

3.6 Materials and Properties

There are four categories of die attach material used in microelectronics packaging. They are:

- Hard solders (Gold-Silicon eutectic, Gold-Tin, Gold-Germanium)
- Soft solders (Combinations of Lead, Tin, Silver, Indium and/or Antimony)
- Glass (Silver glass)
- Organic adhesives (polyimide, epoxy, thermoplastics)

In general, hard solders and glasses are primarily used in hermetic packages, soft solders are found in both hermetic and plastic packages, and organic adhesives are primarily used in plastic encapsulated packages. Each has its advantages and disadvantages, listed in Table 3-2.

Table 3-2: Adhesive materials (18)

Die Attach Material	Advantages	Disadvantages
Hard Solders	No thermal fatigue; High strength	No stress relief; High cost
Soft Solders	Stress relief; Low cost	Thermal fatigue; Creep movement; Low strength
Glass	Good thermal stability; Low cost	High processing temperature; Poor thermal conductivity; No stress relief
Organic	Low processing temperature	Fair thermal stability; Low thermal conductivity

3.6.1 Hard Solders

Table 3-3: Properties of hard solders

Property	Au-Si eutectic	Au-Ge	Au-Sn
Composition (wt%)	96.5Au - 3.5Si	78Au - 12Ge	80Au - 20Sn
Eutectic temperature (°C)	363	356	280
Bonding temperature (°C)	425	N/A	350
CTE (10^{-6} ppm/°C)	12.3	13.3	15.9
Thermal conductivity (W/m°C)	27.2	44.4	57.3

Gold-Silicon (Au-Si) eutectic, Gold-Tin (Au-Sn), and Gold-Germanium (Au-Ge) are typically used in hermetic packaging where lid sealing temperatures are high (>400°C), and good reliability at high temperatures are necessary (19). They possess very high tensile strength, good for fatigue and creep resistance, but minimal ductility, making devices attached with hard solder susceptible to high stresses and die cracking (20). Usually, packages using hard solders have closely matched CTEs between the Si, D/A, and leadframe/substrate to avoid high stress conditions, e.g., a ceramic dual in-line package (CERDIP) with Alloy-42 leadframe, Au-Si eutectic D/A, and Si chip.

The hard solders used in industry, eutectic compositions of Au-Si, involves creating a molecular bond line between the device chip (Si) and the substrate (Cu or Alloy-42 or others). This is accomplished by combining die back metallization with a preform, either of some Au-Si composition, or of pure Au. Au is usually plated on the substrate. Upon application of heat energy and pressure, the Au and Si interdiffuse to form an alloy of eutectic composition (Au-3.5 wt% Si). In this process, it is very important to avoid oxidation or adsorption of oxygen on the surface of the Si. This tends to interfere with good bonding. The bonding process is often performed under a nitrogen gas blanket to avoid any oxidation. Table 3-3 contains some pertinent information regarding hard solders used for die attach.

3.6.2 Soft Solders

Combinations of Lead (Pb), Tin (Sn), Silver (Ag), and/or Antimony (Sb) are used in both hermetic and plastic packaging. Their advantage is in the excellent thermal conductivity and mechanical properties. Often, they are processed in a similar fashion as the hard eutectic solders. Soft solders, such as 95Pb-5Sn, exhibit better thermal conductivity than organic die attach adhesives while providing for better compliance to stresses than the Au-eutectic hard solders. An additional advantage over Au-eutectic formulations is the lower processing temperature involved with soft solders, which ranges from 200 to 300°C. Soft solders are available in paste form and as preforms.

One of the drawbacks for using soft solder is its susceptibility to thermal fatigue at the bond line. Flux can be used to obtain good wetting of the die and pad, but the bond is then susceptible to voiding. Voiding can lead to "hot spots" within the die attach material when dissipating high power, which can degrade the performance of the solder

and, ultimately, the device. This can be avoided by performing the bonding under a nitrogen gas blanket after cleaning, which achieves the same result as flux, keeping the surfaces free from native oxide layers which can degrade the wetting of the solder to the surfaces.

Processing of soft solder die attach typically involves both a die backside and leadframe metallization layer for better adhesion. Both Ag and Cu are excellent for adhering to solder. These are typical metallizations found on the die attach pad and lead tips of leadframes for plastic packaging. The die back is typically metallized with a combination of Ti, Ni, and Ag to form an excellent intermediary for good bonding between the solder and Si. Typically, 95Pb-5Sn and 65Sn-25Ag-10Sb (J-alloy) solders can be used with the above described process.

As mentioned above, the soft solders are used in both hermetic and plastic packages, primarily in high power applications. Examples of hermetic packages used for high power are metal cans. Examples of plastic packages used for high power are SIP and TO packages. The high power applications are typically low lead count (3-23 leads). In these applications, a critical package parameter is the thermal resistance between junction and case, known as the θ_{JC}, which is given in °C/W. For high power applications, this parameter should be as low as possible. The die attach material used contributes greatly to this parameter. Soft solder die attach possesses excellent thermal conductivity, which reduces θ_{JC} significantly over other die attach types (21).

3.6.3 Silver-Glass Adhesives

Silver-glass materials used as die attach adhesive are a low cost alternative to Au-eutectic hard solders. Silver-glass material is essentially an inorganic adhesive that results from the firing of an organic-inorganic combination of materials at a high temperature (>400°C), although there have been lower temperature versions developed recently. The firing step drives off the organic component to leave an essentially void-free bond. They are used primarily in hermetic and power packages. In general, these adhesives exhibit better mechanical properties than hard solders. They are more compliant because of the lower elastic modulus as compared to hard solders. Due to the lack of voids, they resist cracking of the die bond interface better than Au-eutectics and other die attach materials.

Table 3-4: Properties of silver glass

Property	Ag-glass
Viscosity (cps)	45,000
Bonding temperature (°C)	410
CTE (10^{-6} ppm/°C)	15
Thermal conductivity (W/m°C)	32.4

The material properties, as shown in Table 3-4, are heavily dependent upon the solids and silver flake contents present in the silver-glass die attach material. The silver flakes provide the electrical and thermal conductivity necessary for good die attachment. Flakes are used because of their large surface area, which help in providing maximum conductivity. Both the silver and its oxide exhibit exceptional conductivity, which makes it a more logical choice than copper or aluminum for use in this application, where oxidation is highly probable. The particle size distribution and shape of the silver flake is very important in the rheology and adhesion of the adhesive. The silver content of these adhesives is approximately 80% after die attachment. Solids content in the pre-fired Ag-glass material usually ranges between 85 - 90%. Electrical conductivity is critical in many cases where Ag-glass die attach is used.

3.6.4 Organic Adhesives

Organic adhesives, such as epoxies and polyimides, have been used for die attachment in both hermetic and plastic packaging. They possess significant cost and processing advantages over the aforementioned materials, mostly due to the elimination of expensive metallurgy. Although organic adhesives are primarily used in plastic packaging, there has been some usage in the high reliability, military-qualified, hermetic packages. These requirements will be discussed later. The use of organic adhesives for die attach extends back to the 1970's, where they were used for hermetic devices by NASA. Organic adhesives, whether in dispensable or film form, possess lower elastic moduli, which help provide a better stress intermediary between the Si and leadframe material. The following types will be discussed here.

- Polyimides
- Epoxies
- Reworkable (thermoplastics)
- Films (solid or tape form)

In general, organic adhesives require lower temperature processing than either hard or soft solders, and Ag-glasses. For polyimides, cure temperatures as low as 275°C can be used. For epoxies, even lower cure temperatures, like 150°C, are used. Processing of these materials for die attach can be automated relatively easily for increased throughputs. These materials are available in either solution, paste or film form. Table 3-5 lists some commercial organic die attach adhesives and their relevant properties.

Table 3-5: Commercially available organic die attach adhesives

Property	Ablebond 84-1LMISR4	Hitachi EN-4110
Material type	Epoxy	Polyimide
Bonding temperature (°C)	150°C	275°C
T_g (°C)	120	240
CTE (10^{-6} ppm/°C)	41	37
Thermal conductivity (W/m°C)	2.5	N/A

The typical organic adhesive comprises basically of the organic resin as the matrix material, and either an electrically conductive, such as Ag flake, or non-conductive filler. Solvents, catalysts, hardeners, and additives for adhesion and for low stress are also integral parts of the material design, in addition to the main components.

Polyimides: These materials have been used widely in industry as die attach adhesives. Polyimides were developed as high thermal resistance and reduced impurity alternatives to early forms of epoxy die attach. Polyimides are similar to thermoplastic polymers in that they can be reworked or remelted and cured infinitely. They provide a distinct thermal stress advantage over eutectic and soft solder die attach materials (22). Polyimides are cyclic-chain polymers. These polymers are used widely for many industrial applications needing high thermal stability, such as wafer die coats and die attachment. Silver flake is added, similar to the Ag-glass adhesives, to impart electrical conductivity to the polyimide. The application of the polyimide is usually in the form of polyamic acid, which, upon curing at temperatures above 250°C, imidize to form polyimide with water vapor as a by-product. Once cured, the polyimide is virtually insoluble in most common solvents.

One of the primary disadvantages of polyimide die attach materials is the requirement of long and high temperature exposures to fully cure or imidize the polyamic acid into polyimide. Temperatures range from 250°C to 425°C for anywhere from 1 to 2 hours. This can cause problems regarding residual thermal stress after cooling (23). The resultant stresses can lead to problems such as die cracking or delamination. This can also be attributed to the high elastic modulus of the resultant cured material. As with any laminated or layered structure, thermal stresses are proportional to the change in temperature. This is where epoxies hold an advantage over polyimides.

Another disadvantage is the tendency of the cured polyimide to absorb moisture. The absorbed moisture can lead to corrosion and delamination in large dies. Surface mount operations usually involve high heat which can cause moisture to vaporize in the polyimide and delaminate the die bond. Corrosion of the backside can seriously inhibit the electrical performance of the device.

Epoxies: Epoxy die attach adhesives have captured most of the die attach market primarily because of the versatility they provide for a wide range of applications. Currently, high purity, low stress, fast cure, and reworkable epoxy die attach adhesives are available. Epoxy adhesives provide a low temperature, simple process, high reliability alternative to the other materials mentioned above in plastic-encapsulated devices. Early versions of epoxy were not able to compete with polyimide with regard to cleanliness and freedom from ionic impurities. However, newer epoxies are available with high levels of purity, down to 10 ppm or less. Epoxies also do not require high temperatures for cure. Typical cure profiles reach maximums of 150°C to 250°C for around 1 to 2 hours. Recent advances in epoxy die attach adhesives have produced fast or "snap" cure adhesives that only require seconds or a few minutes for cure instead of an hour (24). As with the polyimides, epoxy adhesives typically contain electrically conductive or non-conductive fillers, depending on the application. Again, the most common filler is silver flake.

One advantage of epoxy adhesives is their relatively low solvent/volatiles content as compared to polyimide adhesives. Typically, epoxies contain between 5 and 10 percent solvents/volatiles, whereas polyimides contain between 18 and 30 percent. These numbers can be calculated through weight loss. Since voids are directly related to the outgassing or trapping of outgassed solvents and other volatiles, it follows that epoxies are less susceptible to voiding at the bond line.

Reworkable (Thermoplastics): Reworkable die attach materials, an attractive feature for the multi-chip package assembly, are primarily thermoplastics, although most of the other materials (polyimides, Ag-glass, epoxies) can be reworked, to some extent. With thermoplastics, the die can be removed, with heating of the material, without leaving a residue on the device backside, ideally. Thermoplastics can be reworked repeatedly, since it does not undergo cross-linking. These materials have already been qualified to MIL-Std-883C for use in hybrid packages, but not for single IC packages for military applications, and have been targeted for the Ag-glass market. Its advantages are lower cost, longer pot life, ease of processing, shorter processing time, and no die backside metallization requirement. One major drawback is its lack of historic use, and reliability concerns, especially with respect to military uses.

Films: Film die attach materials are primarily used for chip-on-lead (COL) or lead-on-chip (LOC) applications. The COL/LOC configuration is primarily used to facilitate the insertion of large DRAM memory devices into a relatively small package (11). Like their dispensable counterparts, organic film adhesives can be made either conductive or non-conductive. They are available in either thermoset or thermoplastic configurations. Thermoset configurations include epoxies and modified polyimides. Thermoplastic configurations include aromatic polyester, acrylic, and fully imidized polyimides. Typically, processing involves application of the film adhesive in tape form combined with heat and pressure. These materials currently have limited use in industry and will not be covered in detail here.

3.7 Die Attach Materials Processing

3.7.1 Inorganic Die Attach Processing

Die Backside Preparation: The Si wafer must often receive a backside coating to insure good die bonding, especially in the case of inorganic attach materials. This is due to the bonding mechanism being a metallurgical bond between the surfaces, through interdiffusion. For adhesion by organic (polyimides, epoxies, thermoplastics) no special preparation on the die backside is required to insure good bonding.

Hard Solders: For Au-eutectic bonding, the state of the die backside is very important. Si, though, easily forms a thick oxide (SiO_2) layer, up to 5 nm thick. To achieve the eutectic bond, a scrubbing action must be performed during bonding to break open the oxide and allow the silicon to bond with the gold. Often, to insure no oxide will interfere with the bonding process, the Si wafer will have its backside coated with 100 to 150 nm of Au.

Soft Solders: Si or SiO_2 is not amenable to wetting by soft solders, but Ag or Cu is. Typically, Ag is coated on the backside, along a Ni (diffusion barrier) and Ti (for bonding between the Si and Ni) underlayers.

Silver Glass: Here, the case is reversed of that for hard solders. Ag-glass bonds very well to SiO_2 or alumina, but not to Au. However, some Au is necessary to lower the volume resistivity, so the thickness of the Au backside coating must be carefully determined. However, the Au thickness cannot be so thin that the Au-Si eutectic is created preferentially over the Ag-glass-Si bond, because the Au-Si eutectic layer will prevent good adhesion with the glass (25).

Preforms: To aid ease of use in assembly, preforms are often used with hard and soft solder processes.

Hard Solders: For Au-eutectic bonding, a Au-2%Si alloy is used, to insure good wettability and bond strength. At higher levels of Si, closer to the actual eutectic, the bond is degraded because of the high volume content of Si (close to 20%), which reduces wetting, and large amounts of SiO_2 produced during processing.

Soft Solders: In the case of soft solders, preforms are of the same composition as the paste form. Preforms are used when flux is not desired. The preforms can either be conventionally cast or rapidly solidified. The latter

has the advantage of an uniform microstructure, which improves wettability, reduces impurity levels, and retardation of fatigue cracking due to very fine grain structure.

3.7.2 Organic Adhesive Die Attach Processing

In full-scale production of plastic packages, the adhesive application and attachment of the die onto the lead frame are all done on an automated die bonder. The frames are then loaded into magazines, which are then transported to an oven for curing. For the newly developed snap-cure epoxies, the frames can travel directly into a connected in-line cure oven. Some equipment manufacturers (e.g., K&S, ESEC) sell automated assembly modules, which allow the die-attached frames to go directly to wire bonders (26).

Dispensing: For automated die bonders, the adhesive is dispensed either through a needle or stamped using a star-pattern nozzle. With automatic dispensing, the adhesive must have the proper rheology for problem-free, high-speed dispensing. It should flow smoothly out during application, and must not exhibit "tailing" or "stringing" (a thread of material still connected from the dispensed portion to the needle or nozzle head) (27). If the viscosity is too low, then dripping will be observed. Neither is desirable for a manufacturing process. Equipment adjustment is required to insure the right thickness and fillet. The fillet provides most of the bond strength, but cannot be allowed on the die surface, due to shorting or Ag migration. Also, the material should have a long working life, to minimize the batch changes, which would slow the throughput of a production line.

Curing: The cured material properties of organic adhesives is very much dependent on the time-temperature curing schedule. Often, even if a material is fully cured, but at lower temperature, it will not have the best properties possible, had it been cured at its higher optimal temperature. The adhesives should have minimal voiding during cure, to insure good bond strength. These organic adhesives should also exhibit low outgassing to minimize the release of solvents, water, and other by-products through cure. The by-products will then redeposit less often on the die surface, lead frame, DAP, and oven interior. When redeposited on the pads, wire bonding can be affected causing weaker bond strengths. Naturally, there are reliability concerns with outgassing such as with corrosion and adhesion. The latter could affect the thermal cycling (stress) behavior, by reducing adhesion with the die surface and molding compound, which during cycling could smear, and potentially crack, the top metallization and passivation (28).

Table 3-6: Domestic die attach material manufacturers

Company	Material Type	Location
Ablestik	Polyimide, Epoxies, Film, Silver-Glass, Reworkable	Rancho Dominguez, CA
AI Technology, Inc.	Reworkable	Princeton, NJ
Alpha Metals (Staystik)	Reworkable, Silver-Glass	Jersey City, NJ
Dexter Electronic	Epoxies	Olean, NY
Epoxy Technology	Polyimides, Epoxies	Billerica, MA
Emerson & Cuming	Silver-Glass	Lexington, MA
Indium Corp.	Hard and Soft Solders	Utica, NY
Olin Hunt	Epoxies	Ontario, CA
Quantum Materials, Inc. (QMI)	Silver-Glass	San Diego, CA
Williams Precious Metals	Hard and Soft Solders	Buffalo, NY

3.8 Die Attach Manufacturers

3.8.1 Domestic Manufacturers

Several manufactures, both domestic and foreign, produce adhesives for IC attachment. The range of products they offer are varied, encompassing a number of applications from hermetics to hybrids to multi-chip packages. Once again, "domestic" refers to corporations with headquarters located in the United States. Table 3-6 lists domestic die attach material suppliers.

3.8.2 Foreign Manufacturers

Table 3-7 lists foreign or overseas manufacturers of die attach adhesives.

Table 3-7: Foreign die attach material manufacturers

Company	Material Type	Location
Hitachi Chemical Co.	Polyimide, Epoxies	Japan
Johnson Matthey	Hard Solders, Ag-glass	Great Britain
Sumitomo Plastics	Epoxies	Japan

4.0 WIRE BONDING

4.1 Introduction

The electrical interconnect between the silicon die and the leadframe is perhaps the most important part of the device. Without a reliable interconnect, continuity and signal integrity could be degraded or even lost. The wire bond is the most common interconnect method, as opposed to tape automated bonding, because of its cost benefit and its versatility. Since the very first "flying wire" interconnect was envisioned in the first integrated circuit patent, the wire bond has amassed an enormous reputation as the most reliable interconnect process.

4.1.1 Wire bond Structure

The wire bond consists of three basic parts, depending on the type of bonding process: first bond (ball or wedge), the loop, second bond (crescent or wedge).

4.1.2 Wire bond Materials

Wire bond reliability, from both an electrical and environmental standpoint, is dependent on appropriate materials selection and manufacture. Depending on the type of package and the target application, a number of material properties may be important, such as conductivity, stiffness/workability, hardness, high temperature tensile strength, and corrosion resistance. In a hermetic package, the corrosion resistance of a wire material is not as important as the stiffness of the wire, thus resulting in the use of aluminum wire instead of gold. The manufacturing process chosen is often a result of the type of material to be used. For example, a high speed ball bonding process is more likely to be used for a gold wire process than an aluminum wire process.

Additionally, because the wire bond provides a conductivity bridge between the die and the leadframe, it is of utmost importance that the bond on either end of a wire bond be reliable. Thus, another factor in choosing a reliable material is whether the metallic alloy systems, represented by a phase diagram, are ideal for forming a sturdy, reliable bond. In order to do this, the bonding surface metallurgy and condition are very important.

Some technical considerations for selecting a wire bond material include:

- tensile strength,
- flexural strength (stiffness),
- workability/ductility,
- bond pull strength (adhesion),
- processing temperature (maximum bonding temperature),
- compatibility with bond pad/lead metallurgy, and
- surface contamination.

These considerations are not necessarily properties, but represent the general areas of concern regarding reliability of plastic packages.

Tensile Strength: The ultimate tensile strength ("UTS") of a wire is a measure of the maximum load a material will support without complete failure. It is important as an overall indicator of susceptibility of wires to stresses during the assembly process. It is desirable to have a material with high ultimate tensile strength, but not at the expense of workability. However, it is important to note that although the UTS is helpful in evaluating relative

strengths of such materials, it is still not an indicator of how wires made from such materials will hold up in the assembly process.

Flexural Strength: The flexural strength or stiffness is a measure of elasticity of a material. It is most important in preventing wire sweep, which is the movement of bond wires perpendicular to their length during molding. It is desirable to have a material with a relatively high flexural strength without sacrificing workability. The stiffness is sometimes measured as the Young's elastic modulus and can be obtained with the same measurement used to determine tensile strength.

Workability: Workability or ductility affects the manufacturability of a wire bond. The ductility can be represented as an inherent property of the material as percent elongation. However, workability goes beyond just percent elongation; it also includes any age hardening or work hardening characteristics that might be present. One example is the age hardening of copper wire. If it is stored at elevated temperature for extended periods, it is possible for a wire to go "stale" and become brittle.

Bond Pull Strength: Bond pull strength is a measure of the adhesion and strength of a wire bond. Unlike tensile strength and flexural strength, it is not an inherent material property, but rather an indicator of the strength of both the wire-pad interface adhesion and the wire itself. It is measured on the wire as-bonded and is strongly dependent on the shape and quality of the wire bond.

Processing Temperature: The processing temperature is not an inherent material property. The processing temperature is dependent on both the temperature properties of the material and the manufacturing process. For example, a gold thermosonic bond would require a higher bonding temperature than an aluminum ultrasonic bond, but a lower temperature than a gold thermocompression bond. It is important because a variety of other materials, such as die attach and the chip itself may be sensitive to extreme temperatures.

Metallurgical Compatibility: The metallurgical compatibility or intermetallic formation is a major reliability concern. The formation of brittle intermetallic compounds can cause the bond to degrade such that the possibility of lifted bonds is high. Certain systems are highly susceptible to formation of such compounds in certain temperature ranges and over time. These can be identified by analyzing the phase diagram for the metal system. Nevertheless, intermetallic formation is not all bad. A certain level of intermetallic formation is required to create a strong bond. Typically, the use of the word "intermetallic" in industry connotes the less desirable meaning.

Surface Contamination: Surface contamination, including oxide layers, impacts the reliability of the bond during manufacture. The presence of surface films requires additional force or energy to break, resulting in other reliability problems, such as cratering or die cracking. It is important to understand where a surface contamination issue might arise, such as in copper bonding, where a thick surface oxide may be formed, especially at high temperature.

4.1.3 Cost and Availability; Alternatives

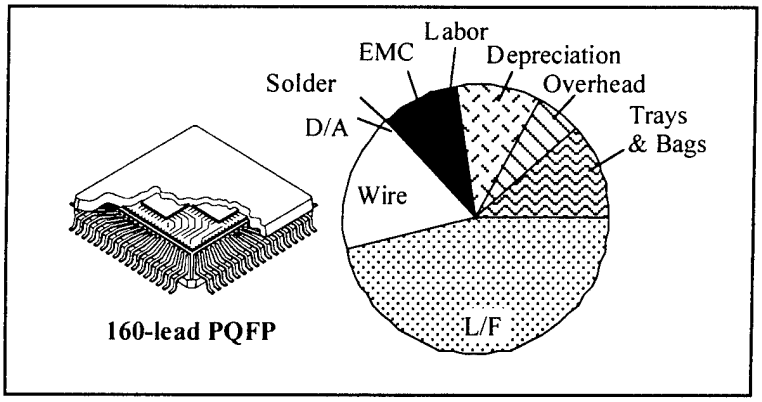
Cost and Availability: The relative costs of various materials of construction of a plastic package (160-lead Plastic Quad Flat Package, in this case) are depicted in Figure 4-1. Using the typical design rules of keeping wire lengths under 200 mils to minimize wire sweep, the maximum amount of gold wire for the 160-lead PQFP is about 32 in. This translates to almost 1/5 of the total package cost, which is about the same level as the item "Trays & Bags". The latter includes not only the actual cost of the plastic trays, bags, or tubes (See Sub-Section 6.0) but also the inherent cost of dry bagging. It should be pointed out that the relative costs will vary with different package types and sizes, and will depend on whether dry bagging or any other special handling precaution is required.

The total worldwide 1995 market for wire bond materials is around $US 400M. It is a relatively small market with even smaller profit margins, and pricing fluctuating with that of precious metals.

Alternatives: Although wire bonding is the predominant interconnect method in plastic packaging, there are two alternatives worth noting. The first is Tape Automated Bonding ("TAB"). It involves using thinner leadframes that are "bumped" (29) and thermocompression bonded directly to the die. Typically, the die is also bumped with either gold or copper in a post-fab assembly process. The advantages of TAB are the relatively high throughput through the bonding process and the relative strength of such bonds. The disadvantage is the high cost associated with tooling and design of leadframes.

The second alternative is flip-chip bonding, which essentially involves bonding of solder bumped die to a substrate or even a printed circuit board (in the case of chip-on-board). This process has advantages in low manufacturing cost and reworkability. However, due to the high cost of repatterning bond pad locations and the solder bumping process itself, the process is not commonly found in plastic packaging at a high volume level.

Figure 4-1: Relative materials costs for a 160-lead plastic quad flat package (41)



4.1.4 Reliability Issues

Wire bond materials and processing can affect the reliability of plastic-encapsulated devices in a number of ways. Primarily, wire bond problems can result in functional failures and parametric shifts. However, there are also some impact on the long term reliability.

Bond Pad Cratering: One of the main reliability concerns with wire bonds is cratering of the bond pad. This phenomenon is caused by mis-application of ultrasonic energy to the bond pad during the bonding process. The energy necessary to create a strong bond can also induce cracks either through the underlying bond pad metallization or in the silicon itself. The most common source of cratering problems is contaminated bond pads, where more ultrasonic energy may be necessary to break through the surface films. This results in excessive amounts of ultrasonic energy that cause cratering. The end result is lifting of the bond and pad, thereby creating an open circuit.

Cratering problems can be minimized through process optimization (30). Generally, they are typical of ultrasonic bonding and not thermocompression bonding. This is primarily because of the directional nature of the ultrasonic energy which creates paths for crack propagation. Cratering can be resolved by using thicker and softer bond pad metallization to help absorb the ultrasonic energy (31).

Delamination/ Package Cracking: Wire bonds generally do not have a great effect on delamination or package cracking. On the other hand, delamination can expose wire bond reliability problems. For example, a package that may have low to medium delamination may cause lifting of weak bonds or even breaking of wires, thereby causing opens. Wires that are swept close together can cause shorts or leakage in moist conditions.

Die Cracking/Temperature Cycling: Both die cracking and bond pad cratering can result where formation of a strong wire bond requires excessive force and energy. A wire material that is too hard or has a thick surface layer that must be broken will require more energy to overcome either the surface layer or to deform the wire. This can translate into stresses high enough to create microcracks that would propagate in subsequent temperature cycling. In addition, temperature cycling can cause fatigue failures on wires at their weakest point, such as at the top of the ball, where cracks in the wire can form if improperly processed.

Corrosion/Intermetallics: Material type plays an important role in corrosion-related failures. First, a wire material, such as aluminum, may be generally susceptible to moisture corrosion by virtue of its natural affinity to react with water, especially in the presence of chlorine. This would be a traditional corrosion problem. The result would be substantially degraded electrical performance and opens. Another consideration is where the wire material does not actually corrode, but rather reacts with another material to which it is bonded, such as where gold wire is

bonded to aluminum bond pads or leadframes. In that case, the diffusion rate of aluminum through gold is greater than that of gold through aluminum, especially at elevated temperatures, creating a problem known as Kirkendall voiding on the die. Bond resistance increases gradually until electrical opens register.

Another corrosion concern is at the bond pad-wire bond interface. Bond pads are usually square. A typical wire bond will not cover the entire bond pad area, leaving the corners exposed. This can lead to corrosion problems with the exposed aluminum in a plastic package. One solution is to use round or octagonal bond pad openings to help minimize the exposed aluminum area.

4.1.5 Current Military Specification Requirements

Currently, the military specifications for wire bonds for integrated circuits only cover aluminum wire bond materials. The main reason is that, thus far, packages used for military integrated circuits are predominantly ceramic/hermetic, except for certain ordnance applications (e.g., fuses) requiring resistance to large acceleration. There is currently no specification for materials in plastic-encapsulated packages.

4.1.6 Types of Plastic Packages

There are numerous package types or outlines in industry today. These can be classified by their lead counts, end application, overall package size, or other physical characteristics. For the purposes of this Sub-section, plastic packages will be classified into the following categories:

- Low lead count
- Medium lead count
- High lead count
- Fine pitch
- Low profile

4.2. Wire Materials and Properties

The following Sub-section outlines the various types of wire materials and their properties as related to package reliability. Table 4-1 compares the different materials.

Table 4-1: Wire bonding materials (32)

Wire Material	Advantages	Disadvantages
Gold	Resistant to corrosion; Amenable to high volume processing	Expensive; Require high temp. bonding to Ag; Intermetallics
Aluminum	Inexpensive; Compatible with Al bond pad materials; Excellent for low profile bonding	Susceptible to corrosion; Difficult to process other than wedge bonding
Copper	Resistant to wire sweep; Inexpensive	Can be too hard (cratering); May require special processing

4.2.1 Gold

Gold is the preferred wire material in use for plastic-encapsulated packages. Gold wire is highly resistant to corrosion, thus requiring little, if any, special treatment to avoid corrosion-related reliability problems in the non-hermetic environment of plastic packages. Additionally, gold wire, when doped with the appropriate elements, possesses excellent mechanical properties that make high volume manufacturing possible. Gold wire is relatively soft and does not harden as a result of deformation to the extent that other materials harden. Less energy is required to ensure a good bond, resulting in lower likelihood of cratering. Gold is soft in its pure state. Like most wires, dopants are used to improve wire properties. Gold wire are typically doped with beryllium or copper to provide workability. Beryllium is typically doped at 5-10 ppm by weight. Copper is doped at 30-100 ppm by weight.

The primary downside of gold wire is the material cost. The average cost of gold is one hundred times that of silver and one thousand times that of copper (33). Although cost consideration is crucial when it comes to high volume production, gold has retained its dominance in plastic packaging. This is a result of the relatively high cost of ownership, i.e. total cost, associated with alternative materials. In comparison, aluminum offers excellent

compatibility with bond pad metal and good conductivity and workability. However, aluminum is highly susceptible to corrosion. Yield fallout from corrosion increases the cost of using aluminum wire. Likewise, copper, which has tremendous cost advantages from a raw material standpoint, requires specialized handling, and suffers from increased likelihood for cratering which drive up the total cost. Thus, gold remains the preferred wire material for plastic packaging.

Because gold is highly resistant to oxidation, it is ideal for both thermocompression and thermosonic bonding, where elevated temperatures that ensure good bonding are not detrimental to surface. These bonding techniques also allow for higher volume manufacturing with good yield.

The predominant bond pad metallurgy on silicon is aluminum, possibly with nickel-based or titanium-based barrier layers. This presents a compatibility problem at elevated temperatures for extended periods of time when using gold wire. The gold-aluminum system contains brittle intermetallics, such as Au_5Al_2, Au_2Al, $AuAl_2$, AuAl, and Au_4Al, that can form over time. This is accelerated at elevated temperatures, e.g. greater than 175°C. This begins with the initial bonding process, where wire and pad are mated together at elevated temperatures and achieve a "good" bond. As time progresses and at elevated temperatures, intermetallics form naturally. Intermetallic formation may result in Kirkendall voiding because of disparate diffusion rates.

Copper, which is typically used for leadframes, can also have some compatibility issues with gold wire. Copper and gold form ductile intermetallics at temperatures in excess of 200°C. Bond strength is usually affected as a result of void formation. However, there is evidence of high bond reliability for elevated temperatures and extended times in gold-copper systems (34).

Silver is used as a plating on leadframe bond sites for a number of reasons, such as for pattern recognition on high volume wire bonders. It typically does not pose any compatibility issues. However, cleanliness of the bonding surface is important in ensuring a good bond.

The presence of these problems can result in degradation in signal integrity. Voids or partially lifted bonds may also result in crack sources for package cracks in molding compounds.

4.2.2 Aluminum

Aluminum wire is commonly found in ceramic packaging. It has found limited use in plastic packaging. The primary concern is susceptibility to corrosion within the non-hermetic environment of plastic packaging. Aluminum oxidizes readily in the presence of moisture. This process is exacerbated when chlorine ion contamination is present, resulting in the formation of an aluminum hydroxide. Thus, aluminum is not ideal for use in plastic packaging where moisture is almost always present at some concentration. Like gold, aluminum is typically alloyed with certain elements for improved properties. These may include silicon or magnesium.

There is some application in plastic-packaged devices where low profiles and fine pitch are necessary. The ideal processing for aluminum wires is wedge bonding. This process produces very low bond heights. It allows for fine pitch because of the absence of a capillary. There are no real compatibility problems with bond pads, since the materials are essentially the same. However, aluminum and silver do not bond well. The system contains many intermetallic phases which provide poor bonds. They also oxidize readily in humid environments. There is also the problem of Kirkendall voiding.

Generally, wedge bonding is the preferred method of bonding aluminum wire. However, wedge bonding is slow in comparison to ball bonding. It does not lend itself well to ball bonding, either ultrasonically or by thermocompression. Ball bonding would require use of an inert gas blanket during bonding to avoid high oxygen contents in the wire which result in brittle wire and undesirable properties (35).

4.2.3 Copper

Copper wire presents distinct advantages with regard to cost and wire stiffness over gold. However, processing difficulty offsets most advantages that are gained with regard to cost. As mentioned above, gold is the most prevalent wire material in use in plastic packages. Copper has found limited use in power applications, where thick, stiff wires are necessary to handle high current and thick molding compound. The high stiffness of copper

makes it ideal for avoiding wire sweep problems, where wires are deflected perpendicular to the direction of bonding during the molding process, sometimes resulting in shorted wires.

The predominant problem with using copper wire is its relatively high hardness when compared with gold. This can create problems with cratering under die pads as a result of the bonding process. Additionally, harder bond pad metallizations are required to avoid excessive deformation of the bond pad. This problem is closely linked with the method of processing used to create the copper wire bond. Copper ball bonding must be carried out in an inert atmosphere, such as argon, to avoid heavy oxide formation on the ball. This oxide contributes the increased hardness of a copper ball and requires more force and energy to create a bond, thereby making it extremely difficult to bond without cratering (39). There is some evidence that dopants can improve the bondability of copper wire in an automated setting (37). More recent results with copper wire bonding indicate that good reliability in integrated circuits can be obtained provided that the proper bond pad metallization has been used to avoid cratering (38).

Copper does not have compatibility problems with copper leadframes. Generally, copper-aluminum bonds are stronger and avoid Kirkendall voiding as compared with gold-aluminum bonds. The high temperature storage life is almost double that of gold-aluminum bonds at 200°C (39). The strength of copper-aluminum bonds does decrease at elevated temperatures due to formation of a brittle $CuAl_2$ intermetallic (40).

4.3 Wire Bonding Processing

4.3.1 Introduction

Reliable wire bonds are as much a function of manufacturing process as they are of materials. Reliability can be compromised when either inappropriate or poorly controlled processing is used. As mentioned in the previous Sub-section, the various materials used in wire bonding are sometimes "typecast" with a particular type of bonder. For example, gold wire is typically bonded using a thermosonic ball bonder. Aluminum is typically bonded using an ultrasonic wedge bonder. The choice of process depends on both the material and the end application.

4.3.2 Types of Wire bonding Processes

There are basically three types of wire bonding processes used for production of plastic packages: thermocompression, ultrasonic, and thermosonic. Of these three, the most prevalent is thermosonic wire bonding, which is the preferred method for bonding gold wire.

Thermocompression: Thermocompression bonding uses a heated capillary which compresses the wire against the bond pad with such force at a certain temperature that interdiffusion occurs at the interface and a bond is formed. A ball is initially formed at the end of a wire that is fed through the capillary. A "flame" melts the end of the wire to form the ball, which is generally polarized in relation to the bond pad. When a ball is formed, the capillary strikes the bond pad and applies the specified force for a few milliseconds. The capillary then moves in such a manner as to draw the wire through the capillary and moves to the second location of the bond. It then strikes the second location with another specified force and pinches off the wire. Bonding temperatures tend to be high, approximately 300 to 400°C to ensure good bonds. Forces necessary to create a good bond are highly dependent on the metallurgy and size of the wire and the cleanliness of the wire and bond pad.

Ultrasonic: Ultrasonic bonding uses ultrasonic energy to create a bond. The process involves much lower temperatures than thermocompression, and is thus better suited for materials where oxidation or high temperature is a problem. It is the most common method of bonding aluminum wires. Typically, a bonding wedge with a guide cut is used where the wire is fed under a flat tool that holds the wire to the pad and transmits the energy to break through surface films and create the bond. The process is a slower process than thermocompression because the bonding tool is asymmetrical and requires constant alignment of the device to be bonded to the tool. Typical throughput for ultrasonic wedge bonders is three wires per second.

Thermosonic: Thermosonic bonding is essentially a thermocompression process with an ultrasonic element. It uses the same type of capillary as thermocompression, but the capillary is not heated. The set-up is the same as thermocompression, except that the capillary is tied into the transducer and delivers the ultrasonic energy. This allows for bonding at lower temperatures than with thermocompression.

The bonding temperature is usually 200°C lower than thermocompression. This process is used for small (< 3 mils) wire diameters. The process is typically used for gold wire, although applications for aluminum and copper wire have been explored and used in limited circumstances. Thermosonic bonding is desirable because of its ability to produce highly consistent and reliable bonds at high throughputs, approximately ten wires per second.

4.3.3 Concerns/Special Manufacturing

Concerns: One of the main reliability concerns with wire bonds is cratering of the bond pad. This phenomenon is caused by application of ultrasonic energy to the bond pad during the bonding process. The energy necessary to create a strong bond can potentially induce cracks either through the underlying bond pad metallization or in the silicon itself. The most common source of cratering problems is contaminated bond pads, where more ultrasonic energy may be necessary to break through the surface films. Other causes for pad cratering are unoptimized bonding conditions (e.g., high velocity approach of the capillary, high force, long bond time, ...) or peculiar pad metallization (e.g., Cu nodules distributed unevenly though the thickness of the in AlCu pad). This results in excessive amounts of ultrasonic energy that can cause cratering. The result is the lifting of the bond and pad, thereby creating an open circuit.

Cratering problems can be minimized through process optimization (30,38). Generally, they are typical of ultrasonic bonding and not thermocompression bonding. This is primarily because of the directional nature of the ultrasonic energy which creates paths for crack propagation. Cratering can be resolved by using thicker and softer bond pad metallization to help absorb the ultrasonic energy (31).

Another concern is corrosion or oxidation. For wire materials, such as aluminum or copper, high temperature bonding processes are not desirable because of the susceptibility of those materials to oxidization. For this reason, ultrasonic bonding is typically used for aluminum. Thermosonic bonding can be used for aluminum and copper with an inert gas blanket during bonding to help reduce the level of oxygen present during bonding.

Special Considerations: The advent of portable personal electronics has driven the semiconductor industry to produce smaller, thinner, and lighter packages. As a result, the demand for low profile and fine pitch wire bond capability has increased. Among the modifications in wire bonders to accommodate this demand are improved bond head movement programs to create low loop heights and redesigned capillary shapes. Improved wire looping is accomplished by bond head movements that actually work the entire wire to create a worked loop instead of a curved loop. Fine pitch wire bonding is addressed through various design and process improvements such as staggered bond pads or altered capillaries. Another fine pitch process improvement is nail head bonding, where a bond with a very small ball is produced to improve spacing. These special bonding considerations involve special material selection decisions which are beyond the scope of this Sub-section.

4.4 Wire Bond Suppliers

4.4.1 Domestic Suppliers

Table 4-2: Domestic suppliers of wire bond materials

Company	Manufacturing Type	Location
American Fine Wire (recently acquired by Kulicke & Soffa Ind.)	Aluminum, Gold	Selma, AL

4.4.2 Foreign Suppliers

Table 4-3: Foreign suppliers of wire bond materials

Company	Manufacturing Type	Location
Tanaka	Aluminum, Gold, Copper, Solder	Tokyo, Japan
Sumitomo Metals & Mining	Aluminum, Gold, Copper	Tokyo, Japan
Mitsubishi	Aluminum, Gold	Tokyo, Japan
Nippon Micro Metal	Aluminum, Gold	Tokyo, Japan
Furukawa	Gold, Copper	Tokyo, Japan

5.0 DIE COATING

5.1 Introduction

Coatings used for semiconductor devices can include a variety of organic and inorganic materials. Their purposes are varied, from stress relief due to encapsulation, to alpha particle protection, to simple chip passivation. In addition, the category may include conformal coatings used for protection of the silicon die and wires, such as in chip-on-board applications (42). In this Sub-section, die coatings are discussed only within the context of plastic-encapsulated packages.

The typical commercial plastic-packaged device has a surface coating, usually a top-layer passivation, applied at the end of wafer fabrication. The passivation protects against alpha particles and gives stress relief imparted by the encapsulation process, which may affect device characteristics. The die would then be mounted, wire bonded and molded with no additional surface processing. Coatings may be viewed as an intermediate packaging step between device assembly and encapsulation. It is important to recognize that, unlike other categories mentioned in the Materials of Construction, such as leadframes or bonding wires, different coating materials can perform the same, as well as varied, purposes. So, it is important to first identify the desired benefit or end-application before evaluating the material to be used.

5.2 Applications

As mentioned previously, there are a number of different applications for die coatings. They can be grouped into the following categories:

- Stress relief,
- Alpha particle protection,
- Environmental protection,
- Passivation, and
- Mechanical protection

Mechanical protection in the context of chip-on-board, where no further encapsulation is performed, will not be addressed here. However, there is some application for using those encapsulants for mechanical protection against wire sweep during the encapsulation process. Inorganic materials, like silicon nitride or oxy-nitride, used as passivation, will also not be addressed.

Stress Relief: Stress relief is critical in applications where stress-sensitive devices are packaged in plastics. As silicon die sizes increase, the stresses from both transfer molding and thermal expansion coefficients mismatch can result in delamination, package cracking, or die cracking. In such cases, die coatings relieve stress by providing a barrier or cushion between the silicon and the encapsulant. Both silicones and polyimides can be used as stress relief coatings in plastic packages.

Alpha Particle Protection: Memory devices are extremely sensitive to bombardment by alpha particles associated with radioactive impurities in the fillers of mold compounds. These particles can cause soft errors in memory devices. Extensive purification of mold compound combined with good surface barrier on the die (usually polyimide) helps to minimize the effect of alpha particles.

Environmental Protection: Unlike traditional ceramic packaging, plastic-encapsulated packaging does not create a hermetic environment. Even though molding compounds are relatively porous to moisture, epoxy-encapsulated devices have excellent reliability for most commercial applications. However, in applications where there is a low margin for error or harsh environments are present, additional protection beyond that offered by a standard plastic package may be required. Die coatings are an inexpensive way to achieve such added protection. Such materials can serve as an additional barrier to ion-laden moisture that may threaten exposed areas of aluminum on the die. Performance of die coatings can be evaluated by accelerated life tests such as THBT and HAST (43).

5.3 Cost and Availability

Any process and material which is not part of a standard process will obviously add cost and affect throughput. However, many of these are also fairly common and readily available. Naturally, it is a question whether the additional cost is offset by the increase in yield and performance.

5.4 Reliability and Failure Issues

The sole purpose of using die coatings is to improve the overall reliability of the device. Thus, the thrust of this Sub-section will focus on the advantages that die coatings convey to the end product.

Temperature/Stress: Materials chosen for die coatings must be able to withstand the rigors associated with semiconductor manufacturing, processing, and testing. For example, a die coat at the wafer level must be able to retain adhesion through the wafer sawing process and withstand the temperatures associated with die attach cure and wire bonding, followed by the stresses of the molding process and the post-mold cure temperature. Epoxies begin to break down beyond 200°C of continuous heat. In contrast, polyimides can withstand exposure temperature above 250°C.

Moisture: Another concern with die coatings is the moisture absorption and desorption that may be associated with both manufacture and use. For example, polyimides desorb moisture during the polyimide curing process. During cure, a typical polyimide film can lose up to 10 weight % of moisture. An incomplete cure could result in release of moisture later in the assembly process or during field use. Silicone materials are highly permeable to moisture. However, certain silicone gels bind to the surface and occupy all the active surface sites, thereby, inhibit potential corrosion.

Adhesion/Delamination: Die coatings are only effective if they stay on the die. Delamination defeats the purpose of using most die coatings, as protection/barrier of the underlying device. Adhesion is also an important factor in avoiding package delamination as well as corrosion.

5.5 Die Coating Materials and Properties

There are three types of materials in wide use as die coatings. They are polyimides, silicones, and epoxies. These materials can be used for a variety of the applications noted above. Table 5-1 shows the relative characteristics of various coating materials.

Table 5-1: Relative characteristics of various coating materials (44)

Material	Thermal conductivity (W/m°C)	Thermal expansion (10^{-5}/°C)	Continuous heat resistance (°C)	Effects of weak acids
Polyimides	---	4.0 - 5.0	260	Resistant
Silicones	3.5 - 7.5	6 - 9	204	Little or none
Epoxies	4 - 5	4.5 - 6.5	121	None
BCBs	---	3.4	300	None

5.5.1 Polyimides

Polyimides are organic polymers that possess extremely high heat resistance (45). The class of polyimides is quite large and encompasses a number of different materials in use throughout the electronics industry. For this report, the discussion is restricted to condensation polyimides, named for the water produced as part of the imidization process. They have wide application throughout the semiconductor industry from dielectric layers to conformal coating. Within this category, names used by various vendors include Pyralin™, PIQ, and PI (46). Some of the desired properties that polyimides possess are:

- High temperature resistance,
- Low thermal expansion,
- Desirable dielectric constant (3.4 @ 1 kHz),
- Planarization capability,
- Ease of processing, and
- High purity

Polyimides can be used as a buffer coat for stress relief, passivation, alpha particle barrier, and moisture barrier. These applications can be met by using polyimides applied as a thin film. There are two basic types of polyimides: photosensitive and non-photosensitive. The photosensitive polyimides do not require an additional masking step to pattern the bond pad openings as with non-photosensitive polyimides. However, photosensitive polyimides usually require dry (plasma) processing, while non-photosensitive material requires all wet (chemical) processing. Functionally, the two types are identical. Polyimides are formed by a process known as imidization. This involves the curing of polyamic acid, a precursor to polyimide. A high temperature cure of about 300°C for one hour will cause the polyamic acid to react forming a polyimide film (47). Polyamic acid allows for a convenient delivery vehicle for achieving planarization and coverage before conversion to polyimide.

One of the problems posed by polyimide films is voiding. The spin-on process combined with the presence of water as a by-product of curing can cause voiding to occur in the cured film. In this case, the resilience of polyimide becomes a disadvantage, as voids are often baked in. The solution is careful process control. Polyimides, available commercially as polyamic acid, can also be obtained pre-imidized to avoid exposure to water by-products, known as siloxane polyimides. These products do not have water as a by-product of the curing process.

5.5.2 Silicones

Silicones have been widely used in the electronics industry since the 1940s (48). They are predominantly used as moisture barriers in board level products, e.g., as a conformal coating. Historically, silicone-based materials were also used as encapsulants, before the advent of high-purity molding compounds. As a die coating material, they would be drop-dispensed or globbed on. There are two basic types of silicones used for electronic applications: room-temperature vulcanized (RTV) and heat-curable hydrosilation silicones. Silicones belong to the category of polymers known as elastomers.

RTV silicones do not require any heat processing and cure at room temperature through a condensation process that involves a volatile byproducts such as alcohol. They can also be produced by a non-volatile addition process using platinum catalysts. Silica fillers are used to provide improved dimensional stability, while solvents, such as xylene, are used to help control viscosity for encapsulants. Pigment can be used to help protect light sensitive devices.

Heat-curable hydrosilation silicones are available in gel form for easy application. Because it is heat assisted, the cure times are much lower than that of RTV silicone. It is also easier to control the cure process by controlling the heat. The process involves crosslinking, by application of heat in the presence of a platinum catalyst, of low viscosity linear hydride resin with higher viscosity vinyl resins.

The main benefit of using silicones is the non-corrosive by-products that are generated during processing. The result is a pure silicone resin that contains low levels of ionic contaminants. Silicones offer excellent alpha particle shielding (49). As mentioned, they also possess desirable mechanical properties for processing. However, the drawbacks include poor solvent resistance and weak mechanical properties, e.g., hardness and strength.

5.5.3 Epoxies

Epoxies are widely used in electronics, predominately as an encapsulation material. Epoxy-based molding compounds are almost the sole material used in plastic encapsulation at the high volume commercial level. In addition, epoxy-based encapsulants are also used in many "glob-top" applications such as chip-on-board. Epoxy-based materials are also used as the matrix material for printed circuit boards (PCB) (50).

Epoxy-based die coats are typically used in production for protecting chips mounted directly onto a PCB. Unlike polyimides, they are rarely applied as thin films in production processing. These "glob-top" epoxies are typically based on a liquid bisphenol A-type epoxy resin and an anhydride. Like silicones, fillers and other additives are used to improve mechanical properties, provide alpha particle protection, and provide other benefits. Anhydrides are added as epoxy curing agents because they improve processing characteristics such as pot life and cure profiles. Pot life represents the amount of time a liquid polymer remains "workable" at room temperature, with the addition of catalysts and other additives. Chemical resistance of the resultant epoxy is generally poor. A typical epoxy glob-top die coating would consist of 20 parts resin, 9 parts anhydride, 70 parts fused silica filler, and 1 part other additives by weight. Epoxy-based die coatings can be used to provide mechanical protection for wires during

the molding process. They are an aid to preventing wire sweep. They also can provide some measure of environmental protection. The moisture absorption of epoxy die coats is relatively low compared to other polymers. For example, over 24 hours in boiling water, a typical glass-filled epoxy resin will absorb about 0.2% water by weight. In contrast, polyimide materials absorb about 3% water by weight over 24 hours.

5.5.4 Other Materials

Benzocyclobutene (BCB): A high performance polymer developed by Dow Chemical Company is a versatile coating material that can be applied by thin-film processing. It has a low dielectric constant, low moisture absorption, and excellent adhesion. Thermal stability without antioxidant additives is poor. It has yet to see widespread commercial use (51).

5.5 Die Coating Processing

Die coatings, whether dropped-on or spun-on, are generally delivered in liquid form, spread over the desired area, and cured. The process used is highly dependent on the material and the nature of the device being covered. For example, a wafer is most efficiently covered by spin coating because thin-film patterning can be used to expose the bond pads through the die coating. An assembled device is not amenable to spin coating (at least not at thin-film process levels) because of the fragility and topographical non-uniformity of the assembled structure.

5.5.1 Thin Film (Spin-On)

Polyimides and some silicones are applied through thin film spin coating. This involves cleaning the wafer, dispensing the die coating, spinning the wafer at various speeds to spread the resin over the wafer, and soft baking (e.g., partial cure). The coating is dispensed from a reservoir using a special pump to control the amount dispensed. Thicknesses of the coating can range from 1 micron to 50-100 microns, but the typical thickness is 1.5 to 3 microns. Much thicker coatings may require multiple coat and soft bake steps. After the coating is applied, it must be patterned to open up the bond pads for wire bonding. This is done using standard photolithography processing. Photosensitive polyimides do not require photoresists to create the pattern. Solvents are used to open the bond pads through the resist pattern.

The principal problem with spin coating is ensuring a void-free coating with uniform thickness. The presence of voids or pinholes can greatly decrease the reliability of the device. Contamination under the coating layer also undermines the reliability of the device. Contamination, such as dust particles and other extraneous material, can lead to voids during cure and may contribute ions to accelerate corrosion under the die coating.

Proper process characterization is critical in ensuring maximum effectiveness of polyimide and other thin film die coating. Spin speeds should be optimized to maximize coverage. Sometimes, a two-stage spin process can be used to help decrease void concentration and increase uniformity. In addition, the dispensing set-up needs to be such that air bubbles are minimized in the line from the coating reservoir. Proper cleaning procedures are critical for both thin film and globbing applications. Wafers can be cleaned using solvents combined with spin scrubbers, which use high pressure DI water while spinning the wafer. Plasma cleaning can help eliminate residual organic materials.

5.5.2 Globbing or Drop Dispensing

Epoxy-based and silicone coatings, as well as some polyimide coatings, are applied by "globbing" the material over the die. This entails a simple process of dispensing material over the die and allowing the material to wet the surface. A pneumatically controlled syringe is used to control the amount of material dispensed. For more complex coverage areas, a syringe mounted on an X-Y table can be used to allow "drawing" of patterns similar to the die attach dispensing process. Special dispensing heads can be used to distribute material over a wider die area. Globbing is generally used to die coat devices that have already been partially assembled.

The problem with globbing is void formation and even coverage, because the spread of the material is not controlled by spinning. These inconsistencies can lead to voids later in processing or unpredictable reliability results. This can be avoided choosing a die coating material that has a relatively low viscosity to aid flow. On the other hand, there will be cases where the coating is required to only cover certain features, in which case, a thixotropic material will be needed to preventing spreading. Proper cleaning procedures also will aid wetting and

coverage as well as minimizing contamination. Plasma cleaning is commonly used to clean assembled devices and enhance adhesion of die coatings to device surfaces.

5.5.3 Cure

Once the die coating has been applied to the device, it is generally necessary to cure the layer prior to molding. Polyimides which produce water as a by-product are typically cured between 200 - 400°C, through a step cure process. Epoxies are generally cured at approximately 200°C, depending on the base catalyst; again, often using a step cure also.

5.5.4 Other Techniques

An ultrasonic spray coater can be used to apply die coating precursors such as polyamic acid over devices, assembled or unassembled. This method uses ultrasonic energy to atomize a solution into 10-20μm particles over the device. This process is not widely used.

Screen printing coating materials is another technique. It allows for precise placement of material over defined areas. The difficulty is having a coating material with the proper thixotropic index, and coating tends to be fairly thick. This technique is also not widely used, although some products are available on the market.

5.6 Die Coating Manufacturers

5.6.1 Polyimides

Table 5-2: Suppliers of polyimides

Company	Location
DuPont	Wilmington, DE
Micro-Si	Phoenix, AZ
Epoxy Technology	Billerica, MA
OCG	West Patterson, NJ
Amoco Chemical Co.	Naperville, IL

5.6.2 Silicones

Table 5-3: Suppliers of silicones

Company	Location
Dow Corning	Midland, MI
GE Silicone	Waterford, NY
Loctite	Troy, NY

5.6.3 Epoxies

Table 5-4: Suppliers of epoxies

Company	Location
Dow Chemical	Midland, MI
Ablestik	Rancho Dominguez, CA
Loctite	Troy, NY
Dexter Electronic Materials	City of Industry, CA
Hitachi Chemical	Tokyo, Japan
Sumitomo Chemical	Tokyo, Japan

5.6.4 BCB

Table 5-5: Supplier of BCB

Company	Location
Dow Chemical	Midland, MI

6.0 PACK AND SHIP

6.1 Introduction

Packing systems are very important in the semiconductor business. Shipping exposes the parts to moisture, temperature changes, and rough handling. The packing system must address all these issues to guarantee that the customers receive parts in good working condition.

Population of printed circuit boards (PCBs) is often done with automated equipment. Tape-and-reel, tube, and tray shipping materials provide a format of presentation to this equipment which allows standardization, repeatability and efficiency of operation. These same carriers can be used at the manufacturer's assembly and test floor giving a means of handling the singulated parts.

There are three basic levels of packing for semiconductors. The first level is where individual parts are loaded into tubes, trays, tapes, and carriers. The second level involves the boxes and bags storing those tubes, trays, tapes, and carriers. Finally, the third level represents the shipping container. The most intricate and varied of the three levels is the first level. First level packing components also double as carriers for the parts, and many meet automated handling requirements.

6.2 Immediate Containers

Many factors influence the choice of which format of first level packing to use. Trays, tubes, tape-and-reel, and individual packs are among those available. The sensitivity to lead bending, the temperatures to be experienced, and the end use of the parts all need to be considered when choosing a packing system. The Joint Electronic Device Engineering Council (JEDEC), the Electronic Industries Association (EIA), and the Electronic Industries Association of Japan (EIAJ) have standards that apply to these first level packing formats. Each type of first level packing vessel will now be described.

6.2.1 Tubes

As with most first level packing systems for semiconductors, tubes are made of anti-static material, or are coated with such material, to resist ESD damage. The tube material is low temperature plastic which melts at approximately 60°C and must be handled and stored accordingly. Flat tubes and coin stack tubes are commonly used for surface mount, SMT, devices and packages requiring unit carriers. Rail tubes are used for dual-in-line packages.

Pin #1 of the devices loaded into tubes have known orientation which is beneficial for automated PCB loading. The tube ends and stopper pins are fit such that very little movement of parts is possible in the tube minimizing damage. Often extra devices are shipped with the order to fill all the tubes.

6.2.2 Trays

More delicate, often high lead count, packages are loaded into trays. Each part has its own cavity and no interference from neighboring parts can inflict damage on each other. Thin quad flat packs (TQFPs), thin standard outline packages (TSOPs), and high lead count plastic leaded chip carriers (PLCCs), are most often shipped in trays. Other devices are loaded in trays as needed by the customer.

Trays are made of anti-static material or are coated to resist ESD damage. Trays conform to JEDEC standards which make them interchangeable from different suppliers. The trays are stackable conserving on space. A stack of loaded trays will have an empty tray on the top to act as a cover. Trays are suitable for presentation to many automatic PCB loading machines. Trays are available in two temperature ranges. Lower temperature trays

are less expensive but melt over 70°C. High temperature trays are good to approximately 150°C. High temperature trays may be used for parts which need baking to dry as part of the pack and ship process. Bake temperatures are approximately 120°C. If a low temperature tray is baked, it will melt resulting in all parts lost. Alternately parts may be transferred to metal carriers for bake and transferred back to the low temperature tray, tube, etc. Pin #1 of the devices are located at some known corner or side of the tray site.

6.2.3 Tape-and Reel

Devices are packed in tape-and-reel format to accommodate the PCB loading equipment which handles tape-and-reel. This format provides the densest loading for automated PCB loading equipment. Some machines can handle up to 150 different reels. Standards apply to tape-and-reel format.

Devices are loaded into cavities in the carrier tape which is then sealed with a clear plastic protective cover enabling device verification. The loaded tape is wound onto plastic reels for labeling and packing. All materials are anti-static to protect against ESD damage. Tape-and-reel packs are generally made of low temperature material. Tape-and-reel holds more parts per pack than any of the other first level packing systems and is the most expensive. Only surface mount devices (SMT) are loaded in tape-and-reel format as these devices are the only ones used with that type of automated PCB loading equipment.

6.2.4 Individual Packs

Also known as "blister packs", individual packs are usually used for filling smaller orders. Individual packs hold 10 to 15 devices per strip depending on the parts. Made of clear anti-static plastic, separate cavities are linked together in a strip. Often anti-static pads are packed with the devices for added protection.

Table 6-1 lists the different types of first level packing available in the industry.

Table 6-1: Comparison of the various types of packing options

	Tubes	Trays	Tape-and-Reel	Individual Packs
Package Type	DIP*, PLCC, SO**, PQFP	PQFP, PPGA*** PLCC	PLCC, SO	PLCC, PQFP
High Temperature Option?	No	Yes	No	Yes
ESD Protection?	Yes	Yes	Yes	Yes
Compatible with Automatic Equipment?	No	Yes	Yes	No
Material	PVC, (Polyvinyl-chloride)	PVC, High temperature plastic	PVC	Polystyrene & Polyester

** DIP: Dual-in-line package; ** SO: Standard Outline; *** PPGA: Plastic Pin Grid Array*

6.3 Intermediate Containers

The packing containers, tubes, tape-and-reel, trays, and carriers described previously go into intermediate containers for shipping. Intermediate, or second level, packing includes bags and boxes. A specified number of immediate containers may be packed into these bags or boxes. The main concerns of second level packing are: 1. keeping moisture out; 2. ESD protection; 3. labeling and identification; and, 4. space efficiency and stackability.

6.3.1 Bag Packing

Moisture absorbed in a plastic package can cause cracking if the device is exposed to high temperature gradients and the ratio of die size to package size is relatively high. This phenomenon is commonly referred to as "popcorning" or the "popcorn effect." These high temperature gradients are common to the board loading processes of surface mount technology devices. Vapor phase reflow and infrared reflow of parts mounted on the boards expose the parts to high temperature gradients. Many PQFPs, PLCCs, TSOPs, and some SSOPs (Shrink Small Outline Packages), especially in high lead counts, are susceptible to this cracking. All packages should be evaluated for sensitivity to this costly mode of yield loss.

Dry packing of parts, after a dehydration bake, insures that parts reach customers with a very low moisture content. Measured in % relative humidity (RH), moisture content never gets above 30% RH and usually is closer to 1%, when standard dry packing procedures are followed. Dry packing incorporates the moisture barrier bags to keep moisture out, desiccant packets to absorb moisture, and moisture indicator cards to give the level of moisture, in % humidity, by changing color relative to a color code.

Parts are usually guaranteed to be below some manufacturer specified relative humidity, e.g. 30%, for some specified period of time such as one year based on specified ambient storage conditions, e.g. $\leq$ 90% RH at $\leq$ 40°C. After this period of time has passed, parts need to be baked if the humidity indicator card reveals that a specified RH has been exceeded. The parts should be mounted within some specified time, again given by the manufacturer, or dry packed for continued storage.

In compliance with MIL-Std 81705B, type 2, the moisture barrier bag usually consists of four layers. Layer 1 is an inner layer of anti-static plastic, layer 2 is an aluminum foil, layer 3 is made of low density polyethylene, and layer 4 is an outer sheet of anti-static plastic. Different bag sizes are made for tubes, trays, carriers, and reels. The bags are sealed with impulse heat bag sealers at some specified temperature and time. Specifications and standards which apply to dry bagging include:

- MIL-Std-81705B, type 2, bag construction.
- Federal standard 101, method 2017, specifies the water vapor transmission rate of the composite bag.
- Federal standard 101, method 2065, specifies puncture resistance.
- MIL-Std-3464D, type 2, desiccant material.

Other concerns with the bags include:

- ESD protection - this is afforded by the bag anti-static layers.
- Bursting strength should be tested and specified.
- Tensile strength of the bags should be tested and specified.
- Temperature range of the bag material should be tested and specified.

Non dry pack bags are also available. These bags give an added layer of protection from the environment without the added cost of the composite moisture barrier bags. These bags are generally made of an anti-static material such as carbon-impregnated polyvinyl chloride to give added ESD protection.

6.3.2 Boxes

Dry packed and non dry packed tubes, trays reels, and carriers are packed into boxes to add protection, provide more efficient handling and storage, order grouping, and enhanced labeling efficiency. Different box sizes are used depending on the immediate packing system, tubes or trays etc., and the size of the order. The following boxing strategies are listed by the immediate packing device:

- Tubes - Loaded into long, top loading boxes, the tubes may be boxed as is or in dry packed bags. Many long top loading boxes will fit into one larger end loading box. Pin #1 of devices in these boxes will be situated towards the labeled end of the box. Anti-static bubble pack, which is clean and environmentally sound, is used to fill voids in boxes left from incomplete filling, etc.

- Trays - As with tubes, both dry packed and non dry packed trays are boxed for shipping. Trays are stacked with an empty tray acting as a cover, wrapped in anti-static bubble pack, and inserted into the box. Pin #1 is situated towards the labeled end of the box.

- Tape-and-Reel - Dry packed and non dry packed tape-and reel systems are boxed for shipping. Within a large box of tape-and-reels, independently boxed reels are separated by corrugated cardboard sheets.

6.4 Labeling

Labels are both machine and human friendly. Information such as lot number, device number, quantity, etc., are written in English and on bar codes. EIA standard 556 applies to the proper use of bar codes. The label also helps to designate where pin #1 is located for tube and tray boxes. ESD and moisture warnings may also be attached to boxes as appropriate.

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8.0 Recommendations for Plastic Package Materials of Construction Given Certain Reliability Issues

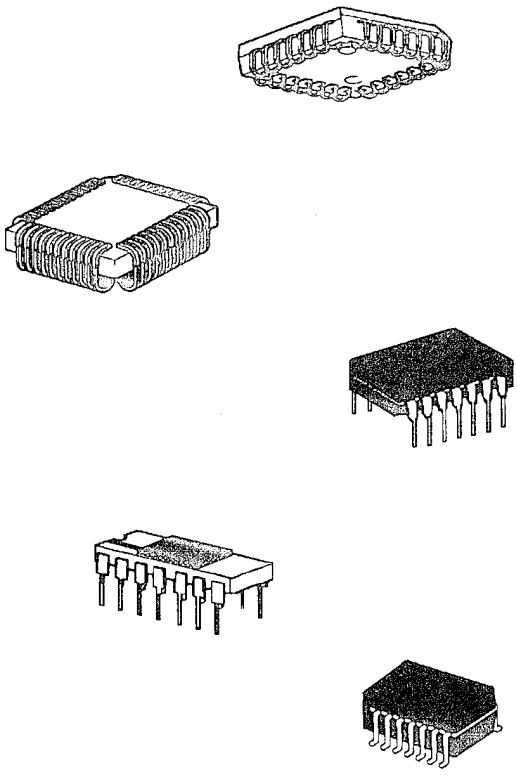
	Mechanical Stress	*Dry Corrosion (Intermetallics)*	*Wet Corrosion*	*Delamination/Package Cracking/ Moisture Penetration/ Popcorning*
Molding Compound	- Use low stress formulations for high pin count, large die, etc. - Optimize EMC fracture toughness - Optimize package thickness	- Control [Br^-] & [SbO_2] concentration in flame retardants	- Control purity and optimize composition - Minimize water permeability of compound - Control void concentration - Solubility of water in EMC	- Maximize adhesion to leadframe - Minimize water permeability of compound - Control void concentration - Solubility of water in EMC - Be aware of reflow conditions - Adhesion promoters? - Optimize EMC fracture toughness
Leadframe	- Use stress relief features (e.g., slots) at high stress areas (e.g., rails) - Optimize aspect ratio/dimensions to resist lead deflection - Maximize modulus of elasticity - Optimize CTE to closely match Si, EMC, D/A - Control burrs & sharp edges	- Control leadframe and wire bond metallurgy	- Maximize cleanliness - Employ locking features to help impede moisture penetration - Optimize CTE - Optimize plating cleanliness	- Employ locking features to help impede moisture penetration - Optimize CTE - Optimize plating cleanliness and minimize leadframe surface contamination - Use Cu for better adhesion with EMC - Adhesion promoters? - Control burrs and sharp edges (stamped vs. etched leadframe)
Die Attach	- Optimize modulus and CTE - Reduce void concentration - Optimize thickness of bond line - Optimize filler content for high thermal conductivity and better flow properties - Optimize D/A fracture toughness	**** No failure mechanisms identified and traced back to D/A ****	- Reduce outgassing of D/A - Control ionic and water impurity content	- Optimize CTE and modulus - Control void concentration
Interconnect	- TAB vs. wire bond? - Optimize wire mechanical properties for wire sweep resistance	- Control wire, leadframe, and bond pad metallurgy	- Use Au wire	**** No failure mechanisms identified and traced back to Interconnect ****
Die Coating	- Optimize modulus and CTE - Optimize thickness & uniformity - Optimize dispense method (spin coat vs. glob top)	- Ensure good pad coverage - Use unreactive bond pad metallurgies where possible (e.g., barrier layers) - Control impurity levels in die coating	- Ensure good pad coverage - Use nitride or equivalent passivation as getter for O_2 - Use non-reactive bond pad metallurgy - Control impurity levels in die coating	- Optimize adhesion with EMC - Minimize water absorption - Control outgassing - Beware of surface contamination
Packing/ Storage	- Use trays instead of tubes where feasible - Avoid handling damage	**** No failure mechanisms identified and traced back to Packing/Storage ****	- Control storage conditions - Use dry bags with desiccant - Use within recommended period after bags are open	- Control storage conditions - Use dry bags with desiccant - Implement dry bake prior to mounting

PLASTIC PACKAGE AVAILABILITY PROGRAM

PLASKON FINAL REPORT

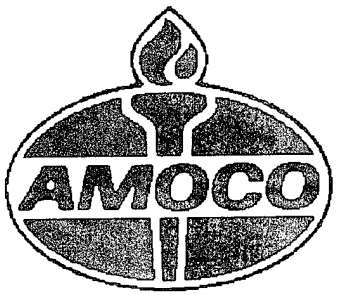
SECTION 2

Task 2.0 Plastic Pkg Criteria Def.
Task 3.0 Mold Compound Formulation & Optimization
Task 9.0 Plastic Usage Specification



PLASTIC PACKAGING AVAILABILITY

BAA 92-02 SUB AREA E2
TRI-SERVICE INITIATIVE



AMOCO CHEMICAL COMPANY
PLASKON ELECTRONIC MATERIALS, INC.
Sub Contractor

FINAL REPORT

November, 1995

William F. Bates

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Scope of Program

The goal of this program is to develop a set of Military specifications for commercially available epoxy molding compounds (EMC). These specifications are to be applicable to state-of-the-art EMCs currently being offered by leading EMC manufacturers for encapsulation of semiconductor devices by the transfer molding process. Representative EMCs conforming to these specifications will be provided to demonstrate their suitability for use by the Military. However, it is not within the scope of this program to develop new or exotic EMCs specifically for Military use or to provide detailed EMC formulations.

SUMMARY

Five Plaskon EMCs representative of state-of-the-art commercially available epoxy encapsulants for semiconductor devices were selected for this program. These consisted of a standard EMC, an ultra low stress version, higher reliability versions of these two and an antipopcorn[1] compound. The two high reliability analogs were formulated using low chloride resins and specific ion scavengers. The improved reliability of these analogs was confirmed by High Temperature Storage (HTS) and Highly Accelerated Storage Test (HAST) studies.

Production quantities of the five chosen EMCs were submitted to National Semiconductor for molding and reliability testing on select devices. Concurrently, Plaskon characterized each of these EMCs for chemical, electrical and mechanical properties. The characterization data were then compared to NSC reliability test data for correlation. The comparison of data confirmed correlation between reduced low levels of halogens in the EMCs and device reliability.

Proposed specifications were written for each of the EMC use categories and are included with this report.

EMC GENERIC FORMULATION

EMCs described in this report and covered by the proposed Military specifications are thermosetting epoxy polymers of the following generic composition:

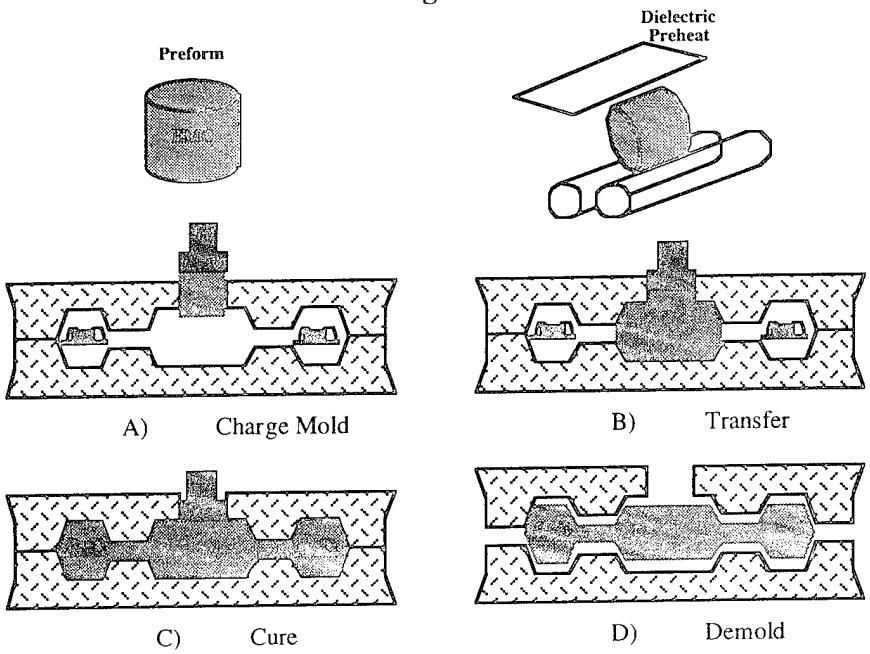
Table 1

Ingredient	Percentage By weight
Epoxy resin	10-20
Phenol novolac hardener	5-15
Accelerator	< 1.0
Silica filler	60-80
Brominated Flame retardant	0.50-2.0
Antimony oxide	0.50-3.0
Carbon black	< 1.0
Synthetic wax	< 2.0
Coupling agent	< 1.0
Stress absorber (optional)	0 - 5.0

The transfer molding process by which these EMCs are used to encapsulate semiconductor devices is shown in Fig 1. Basically, the process consists of preheating a preform or pellet of EMC, transferring it under pressure into a heated mold, allowing it to cure for 0.5 - 3.0 minutes and demolding the finished part.

Fig .1

EMC Molding Process



SELECTION OF BASELINE FORMULATIONS (Task 2.1)

Two EMCs were selected from Plaskon's list of commercially available molding compounds to be baseline formulations. The main criterion used in selection of baseline formulations was the use and acceptance of these EMCs for their intended applications by leading semiconductor manufacturers.

Plaskon 3400 was selected as being representative of typical EMCs used to encapsulate low to moderate lead count semiconductor devices and discrete electronic components. Typical applications include 14/16, 24 & 64 lead DIPs, SIPs, resistor networks, thermistors, transistors and diodes. Plaskon 3400 and other compounds of this type are known for having excellent moldability over a wide range of processing conditions together with excellent electrical, chemical and physical properties. The reliability performance of 3400 on devices for which it is intended is excellent.

Plaskon ULS-12H was selected as being typical of very low stress EMCs used to encapsulate stress sensitive devices such as large die, fine pitch TSOPs, PLCCs and QFPs. The low stress of ULS-12H is the result of a combination of low coefficient of thermal expansion (CTE) and low flexural modulus. The low thermal expansion reduces stress by minimizing the difference in CTE between the mold compound and the silicon die of the device. The low modulus allows some yield, thereby absorbing some of the stress.

The industry accepted estimation of stress characteristics of an EMC is Stress Index. Stress Index is the mathematical product of alpha 1 in ppm/°C (CTE below glass transition temperature, Tg) of the EMC and its flexural modulus in Mpsi.

$$\text{Stress Index} = \text{CTE (alpha 1) (ppm/°C)} \times \text{Flexural modulus (Mpsi)}$$

By today's standards, an EMC can be classified as low stress when its Stress Index is below 35.

Table 2 lists typical properties of the two baseline compounds selected for this program.

Table 2

	Plaskon 3400	Plaskon ULS-12H
Physical Properties		
Spiral flow, in	35	32
Ram follower gel, sec	18	15
Viscosity (orifice), PaS	10	5.5
Specific Gravity	1.83	1.88
Ash content, %	71.8	78
Hydrolyzable chlorine, ppm	< 10	< 1
Flammability, UL 94V0, in.	1/8	1/8
Thermal properties		
Glass transition temperature(Tg)°C	155	168
Linear thermal expansion		
Alpha 1, ppm/°C	20	12.5
Alpha 2, ppm/°C	62	65
Thermal conductivity		
cal/cm-sec-°C x 10E-4	16	17
Mechanical Properties		
Flexural strength, Kpsi	18	15.5
Flexural modulus, Mpsi	2.2	2.05
Shore D Hardness @ 177°C, min.	70	80
Stress Index	44	26
Electrical Properties		
Dielectric constant, 1 KHz	3.8	3.8
Dissipation factor, 1 KHz	0.002	0.002
Arc resistance, seconds	180	180

REVIEW OF COMMERCIAL SPECIFICATIONS FOR EMCs (Task 2.2)

Plaskon internal EMC specifications, specifications from other key EMC suppliers and available procurement specs from semiconductor manufacturers were reviewed with an aim toward identifying important properties characterizing various grades of epoxy molding compound. In general, EMC properties for which limits were established were essentially the same for like grades of epoxy regardless of the supplier.

Engineers from five US Semiconductor manufacturers were surveyed by telephone to determine how suppliers to the Military of ceramic and/or plastic electronic parts handle EMC qualifications and specifications. Here are a few key responses from that survey:

- **Ionic purity as determined by water extract conductivity and ion chromatography is an important indicator of device reliability performance.**
- **Flame retardant levels (bromine) are minimized for optimum HTS reliability.**
- **None of the respondents knew of any device field failures directly traceable to plastic encapsulants.**

- **Extensive functional reliability testing is required for qualification of plastic encapsulants but device reliability tests are not usually included in mold compound specifications.**

Typical EMC User Qualification Tests

Moldability	Pressure pot , 15 psi/126°C
Wire sweep	Thermal shock, -65°C to + 150°C
Void level	HAST, 130°C / 85% RH
Mark permanency	HTS, 175°C / 200 hrs
Wire bond pull strength	Package crack & delamination after
Line movement	Preconditioning, 85% RH / 85°C and
Board adhesion	Solder reflow, 215-235°C

An example of typical EMC properties and limits specified in a semiconductor manufacturer's procurement specification for a standard grade epoxy encapsulant is shown in Table 3.

Table 3

Typical EMC Procurement Specification

Property	Limits
Spiral flow, cm	60 - 90
Ram follower gel time, sec	15 - 25
Thermal expansion	
alpha 1, ppm/°C max.	25
alpha 2, ppm/°C max.	75
Glass transition temperature, °C min.	150
Ash content, %	70 - 72
Nitrogen content, ppm	400 - 455
Water extract conductivity, μmhos/cm, max.	20
Extractable Cl, ppm, max.	25
Extractable Na, ppm, max.	25
Extractable K, ppm, max.	10
Hydrolyzable halides, ppm, max.	50
Total bromine, %	0.60 - 0.90
Total antimony, %	1.0 - 1.5
Flammability (UL 94 VO), 1/8"	pass

EMC suppliers are usually required to furnish a certificate of analysis for all or most of the properties listed in the procurement specification for each lot shipped.

Based on all the information gathered on EMC specification requirements, the following template is recommended as a guideline in writing EMC specifications.

Table 4

EMC Specification Template

Property	Method	Conditions	Units	limits
Moldability				
Spiral flow	SEMI G11	175°C/1000 psi	inches	
Ram Follower Gel Time	SEMI G11	175°C/1000 psi	seconds	
Hot Hardness	Shore D	175°C (90 seconds)		
Flash & Bleed	SEMI G45	175°C/1000 psi		
2 mil Channel			millimeters	
0.25 mil Channel			millimeters	
Thermal Properties				
Coefficient of Thermal Expansion	SEMI G13	Post cure		
Alpha 1		4 hrs/ 175 °C	ppm/°C	
Alpha 2			ppm/°C	
Glass Transition Temp. (Tg)			Degree C	
Flammability	UL-94	1/8" thickness		
Physical Properties				
Flexural Strength	ASTM D790	Room Temp.	Kpsi	
Flexural Modulus	ASTMD790	Room temp.	Mpsi	
Specific Gravity	ASTM D792			
Moisture Absorption	IPC-SM-786A	Level 1	Percent	
Ash content	ASTM D2584	650°C	Percent	
Viscosity	ASTM D3835	175°C/1000 psi	Poise	
Electrical				
Dielectric Constant	ASTM D149	1 KHz/room temp		
Dissipation Factor	ASTM D149	1 Khz/ room temp		
Volume Resistivity	ASTM D257	Room temp.	Ohm-cm	
Analytical				
Water Extract Conductivity	SEMI G29	48 hrs/121°C	μ mhos/cm	
pH of Extract				
Extractable Sodium			ppm	
Potassium			ppm	
Chlorine			ppm	
Bromine			ppm	
Iron			ppm	
Total Antimony	X-ray fluorescence		Percent	
Total Bromine	X-ray Fluorescence		Percent	

RATIONALE FOR SPECIFICATION ITEMS (Task 2.2)

The rationale for selection of the EMC properties listed in the Template (Table 4) involves consideration of moldability, reliability and lot to lot consistency.

Properties important to overall moldability include spiral flow , gel time, hot hardness , flash & bleed and viscosity. Spiral flow, gel time and viscosity dictate the process window for mold fill and cycle time. Hot hardness development is essential to assuring molded runner & part integrity during demolding and ejection. Low to moderate viscosity of the molten EMC is needed for proper cavity fill and minimal movement of bonding wires . Flash & bleed deposits on leadframes or mold land surfaces are difficult to remove and must be controlled.

Reliability of EMCs is assured by control of properties affecting stress, metal movement (wire sweep & line movement) , generic leakage, intermetallic formations and corrosion. Thermal expansion of EMC is designed to be as close as possible to the metal components of the encapsulated device to prevent cracking due to mismatches in expansion. Flexural strength and modulus give a good indication of toughness and the ability to yield under stress without cracking. Water extract conductivity and determination of specific ions gives a good indication of the potential for liberation of free ions which can corrode the metal circuitry or cause intermetallic formation and ball bond failure. Dielectric constant, dissipation factor and volume resistivity are standard electrical properties which are used to characterize the electrical insulating properties of EMC and can also give an indication of generic leakage potential.

Moisture absorption is another important EMC property which must be included in any EMC specification. High moisture levels are associated with voids in molded parts, increased mold staining and popcorn cracking. Flammability is also a property which must be controlled along with the amount of the bromine flame retardant. Excessive bromine is known to cause wire bond failure at high temperature.[2]

EMC OPTIMIZATION FOR RELIABILITY (Task 3.1)

One potential reliability problem with devices encapsulated in plastic is corrosion of the metallization due to attack by ionic halogens in the epoxy molding compound. The main source of potentially mobile chloride ions is the base epoxy resin. The synthesis of epoxy cresol novolac resin (ECN) involves the epoxidation of cresol novolac resin with epichlorohydrin followed by a dehydrohalogenation step. Incomplete dehydrohalogenation results in the formation of chlorohydrin species which can hydrolyze to release corrosive chloride ions. Today's ECN resin typically will contain 600-850 ppm total chlorine, less than 1/2 of which is considered hydrolyzable.

Device failure under extreme moisture stress such as HAST is usually the result of bond pad corrosion . This is a self-sustaining reaction as follows:

$$Al + 4Cl^- \quad \text{-----}> \quad ALCl_4^- + 3e$$

$$2\,ALCl_4^- + 6H_2O \quad \text{-----}> \quad 2Al(OH)_3 + 6H^+ + 8Cl^-$$

Obviously, one method of improving reliability is by simply using lower chloride epoxy resins. The beneficial effects of lower chloride to device performance in HAST & HTS is shown in the following graphs (fig 2 & 3).

Fig 2

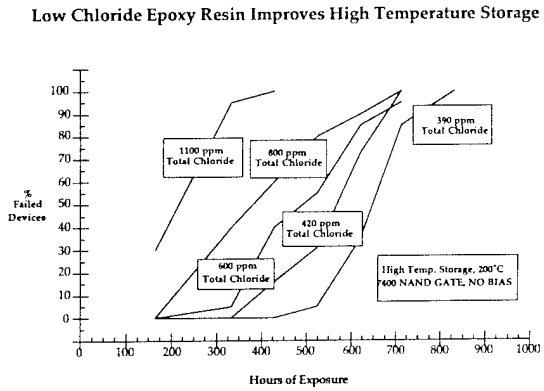
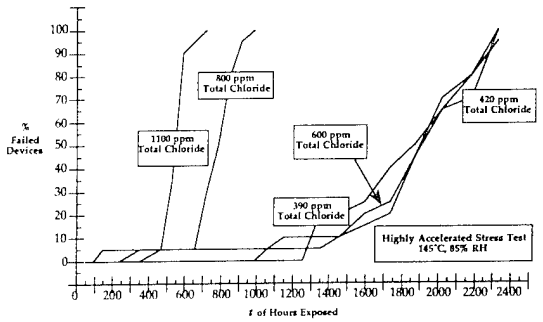


Fig 3



Another method of enhancing reliability is the use of ion scavengers. This technology is well known to epoxy formulators and has been reported in numerous publications.[3] Basically, a scavenger, getter or ion exchanger is a substance used to capture and inactivate free ions. There are a variety of scavengers available, each with unique anion or cation capturing ability.

Ion Scavenging Example

$$M(OH)_3 + HX \text{ ----------> } M(OH)_2X + H_2O$$

M = Metal X = Halogen

Figures 4 & 5 show HAST & HTS improvement as the result of incorporating ion scavengers in standard EMC.

Fig 4

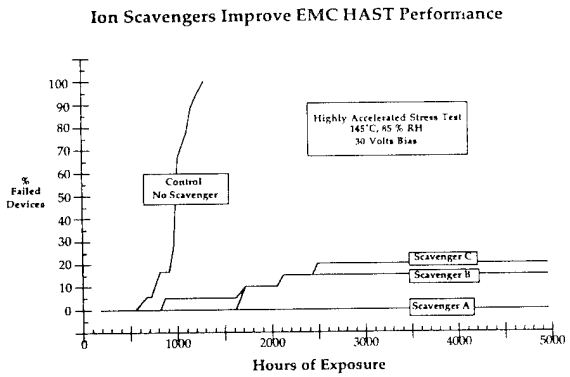
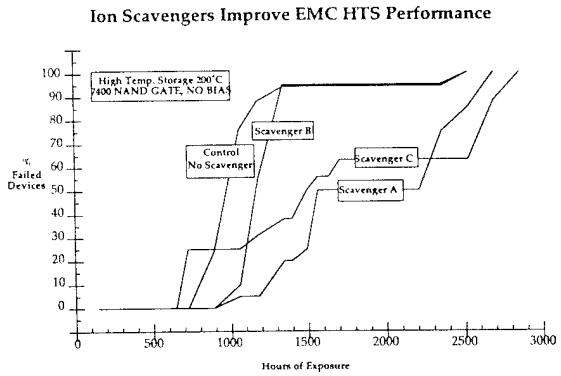


Fig 5



The review of pertinent literature and Plaskon's data base confirms that the best method of improving EMC reliability performance, without resorting to expensive or exotic approaches, is to formulate with low chloride ECN resins together with the appropriate ion scavengers.

Verification of Reliability Improvement.

New laboratory studies verified the anticipated improvement in reliability resulting from the use of high purity ECN and scavengers. In addition, work was done to evaluate the effects on reliability of different calalyst and bromine types. Another study compared 3400 with and without flame retardant.

Table 5 shows the design and all characterization data for an experiment comparing Plaskon 3400 with analogs containing high purity resins, getters, different bromine sources and different catalysts. These data show very little difference between the five formulations except for a lower glass transition temperature for compounds D and E which contain an alternate catalyst. Suprisingly, there is very little difference in water extract conductivity and extractable chlorine between those with and without low chloride resins and ion scavengers. However, HAST & HTS results shown in figures 6 & 7 clearly show definite improvement in reliability for the analogs containing low chloride resin and scavengers.

Table 6 is an experiment designed to compare ULS-12H with analogs containing low chloride epoxy and ion scavengers. The data indicate no difference between these except for longer flow & gel for compounds C & D which contain ion scavengers. Figures 8 & 9 again clearly show improvements in both HAST & HTS for those formulations containing low chloride resins and ion scavengers.

Table 7 shows the design & data for an added experiment to study the effects of bromine/antimony flame retardants on reliability. Graphs of reliability data, Figs 10 & 11, show little difference in HAST performance between the flame retarded and non flame retarded formulations but a tremendous difference in 200°C HTS. This experiment clearly demonstrates the negative effects of flame retardants on HTS . Indeed, M. Nakao et al. [4] describe the phenomenon of free bromide ions causing wire bond failure at high temperatures due to intermetallic alloy formation. It is obvious that if bromine/antimony flame retardants are used, the amount of each should be minimized and controlled by specification .

Table 5

PLASKON 3400 & ANALOGS CHARACTERIZATION DATA

	A	B	C	D	E
Epoxy Purity	Norm	High	High	High	High
Ion Scavenger	No	Yes	Yes	Yes	Yes
Bromine Type	A	A	B	A	B
Catalyst Type	X	X	X	Y	Y
Spiral Flow, in.	29	35	33	38	36
RFGT, sec	19	25	26	25	24
Hot Hardness @ 90 sec	84	70	73	70	69
Flash & Bleed					
3 mil, mm	9	8	10	9	9
2 mil, mm	3	3	3	4	3
1 mil, mm	2	2	2	3	2
0.5 mil, mm	2	2	2	3	2
0.25 mil, mm	2	3	2	3	3
Thermal Expansion					
CTE Alpha 1, ppm	21	23	22	21	21
CTE Alpha 2, ppm	63	65	62	65	62
Tg, °C	159	153	158	137	136
UL 94 VO, 1/8 in.					
Flame out Time, sec	14	11	14	17	18
Flex Strength, Kpsi	17	17	17	18	17
Flex Modulus, Mpsi	2.1	2.1	2.2	2.2	2.3
Specific Gravity (g/cc)	1.8	1.8	1.8	1.8	1.8
Filler Content, %	71.9	71.9	71.9	71.9	71.9
Viscosity, PaS (175°C)	12	10	12	9	13
Flow Rate, mls/sec(175°C)	1.0	1.0	0.9	1.2	0.9
Dielectric Constant	3.52	3.47	3.41	3.67	3.54
Dissipation Factor	0.003	0.004	0.003	0.004	0.003
Volume Resistivity (ohm-cm x 10^{+15})	3.3	1.8	1.2	1.7	2.1
Water Extract (1.5 hr @ 100°C)					
Conductivity, μmhos-cm	34	35	44	20	59
Extractable Na, ppm	20	27	23	29	37
K, ppm	17	1	1	2	8
Cl, ppm	3	< 1	<1	< 1	3
Br, ppm	4	2	3	2	3

Fig. 6

Low Chloride Epoxy & Ion Scavengers Improve Plaskon 3400 HTS Performance

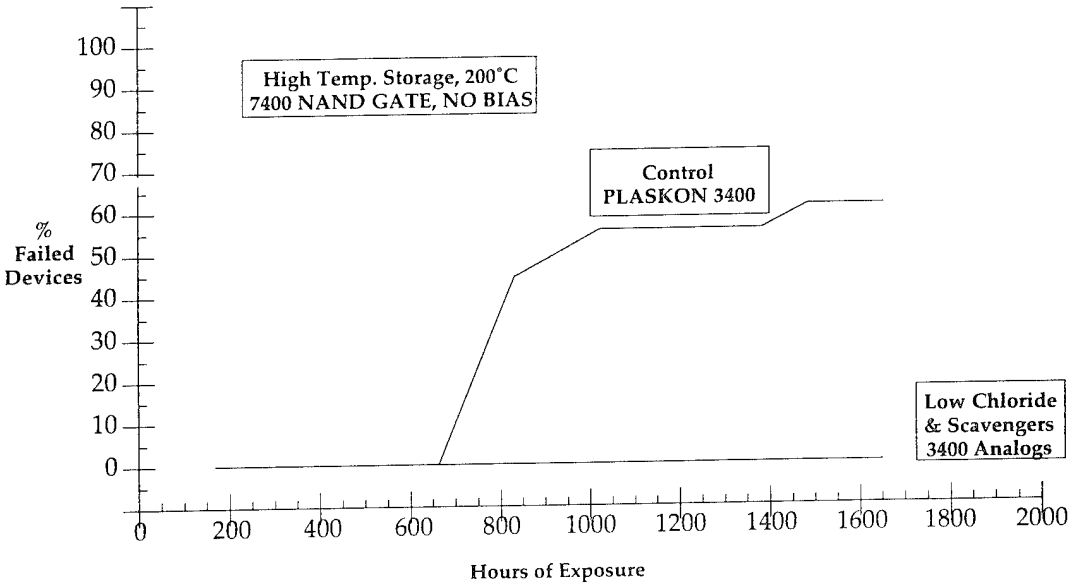


Fig. 7

Low Chloride Epoxy & Ion Scavenger Improve Plaskon 3400 HAST Performance

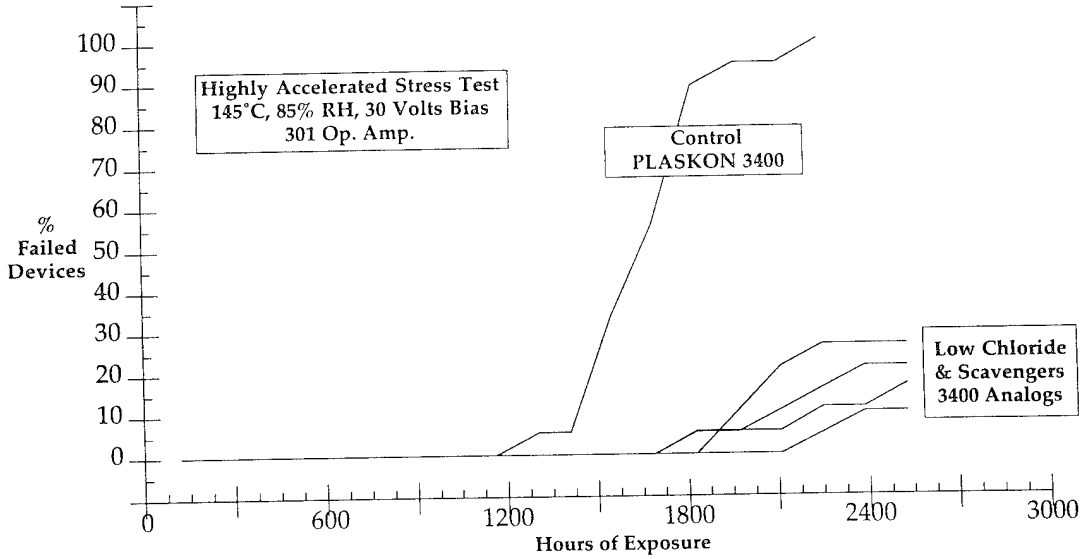


Table 6

ULS 12H & Analogs
CHARACTERIZATION DATA

	A	B	C	D
Resin Purity	Norm	High	Norm	High
Ion Scavenger	No	No	Yes	Yes
Spiral flow, in	33	35	42	41
Gel Time, sec	15	22	30	30
Flash & Bleed				
3 mil, mm	18	16	19	20
2 mil, mm	3	3	3	3
1 mil, mm	2	3	3	3
0.5 mil, mm	2	3	3	3
0.25 mil, mm	3	4	5	4
Thermal Expansion				
CTE Alpha 1, ppm	13	14	15	14
CTE Alpha 2, ppm	62	62	65	64
Tg, °C	162	165	157	160
UL 94 V0 (1/8"), sec	16	11	15	12
Flex Strength, Kpsi	17	16	16	15
Flex Modulus, Mpsi	2.1	2.1	2.1	2.1
Volume Resistivity				
(ohm-cm x 10^{+15})	2.4	2.3	2.3	2.2
Filler content, %	77.4	77.4	77.4	77.4
Viscosity @ 175°C, PaS	5.8	4.6	4.1	4.3
Flow rate, mls/sec	1.9	2.3	2.6	2.4
Specific Gravity, g/cc	1.85	1.83	1.86	1.85
Dielectric Constant	3.61	3.56	3.53	3.57
Dissipation Factor	0.003	0.003	0.004	0.004

Fig 8

Low Chloride Epoxy & Ion Scavengers Improve PLASKON ULS-12 HTS Performance

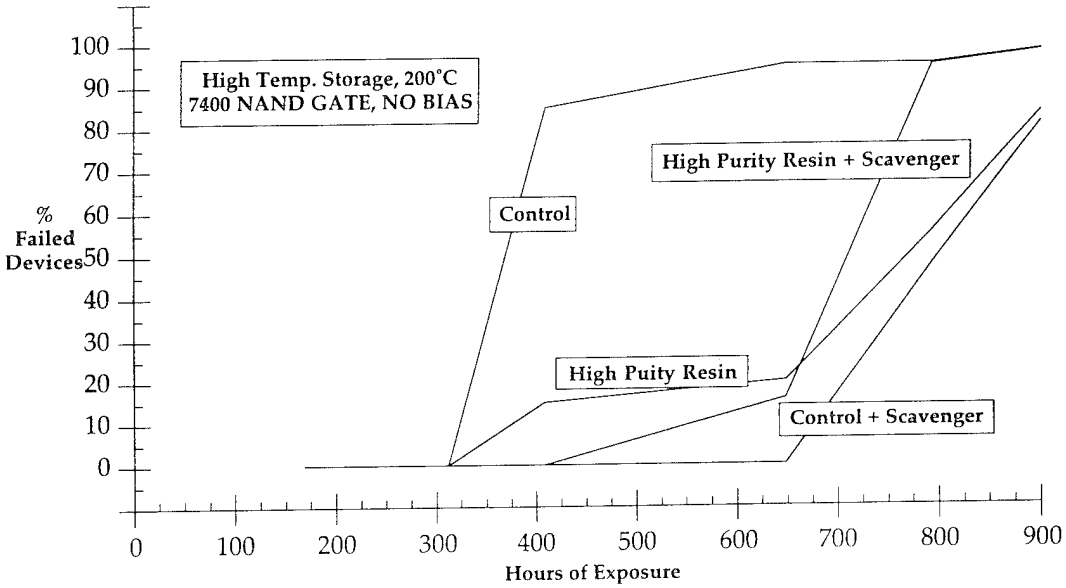


Fig 9

Low Chloride Epoxy & Ion Scavengers Improve PLASKON ULS-12 HAST Performance

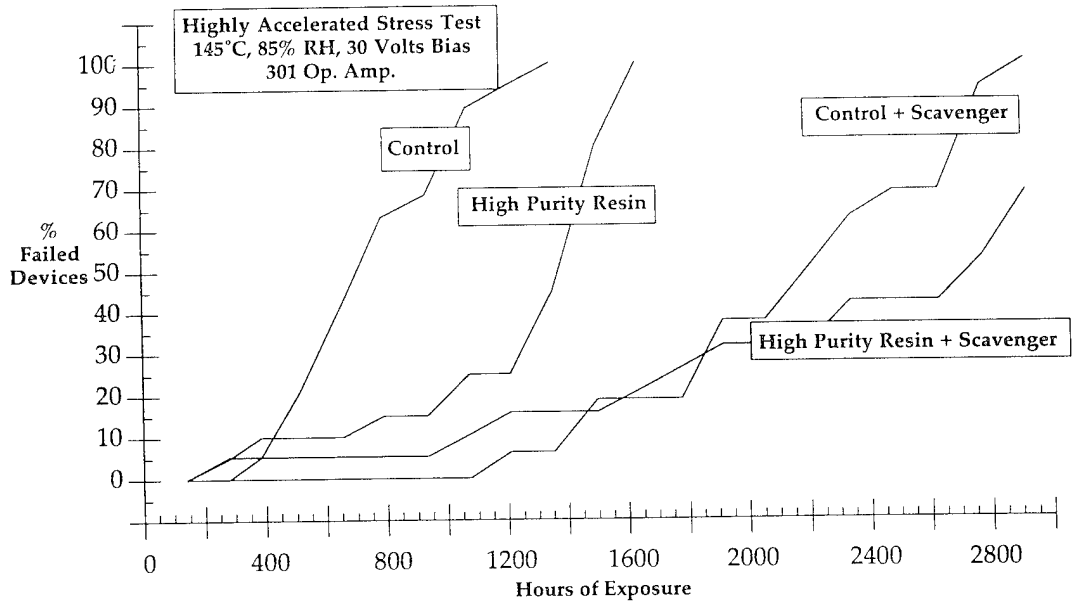


Table 7

Standard EMC
No Flame Retardant

	A	B	C	D
Flame Retardant	Yes	No	No	No
Resin Purity	Norm	Norm	High	High
Ion Scavenger	No	No	No	Yes
Properties				
Spiral flow, in.	31	30	32	33
Ram Follower Gel Time, sec	19	17	17	17
Hot Hardness @ 90 sec	86	84	81	84
Flash & Bleed				
3 mil, mm	4	5	5	5
2 mil, mm	2	2	2	2
1 mil, mm	2	2	1	1
0.5 mil, mm	1	1	2	2
0.25 mil, mm	2	2	2	2
Thermal Expansion				
Alpha 1, ppm / °C	22	23	21	22
Alpha 2, ppm / °C	63	67	61	61
Tg, °C	162	164	167	167
UL 94 VO, sec (1/8"), sec	20	F	F	F
Flexural Strength, Kpsi	18	17	17	17
Flexural Modulus, Mpsi	2.3	2.3	2.3	2.3
Specific Gravity(g/cc)	1.81	1.78	1.79	1.79
Filler Content %	72	72	72	72
Viscosity, poise @ 175 °C	138	130	136	120
Flow Rate, mls/sec	0.80	0.81	0.77	0.88
% Ash	73	73	73	73
Dielectric Constant	3.60	3.65	3.45	3.61
Dissipation factor	.003	.004	.003	.003
Vol. Resistivity, ohm-cm X 10^{+15}	3.7	3.9	4.1	3.7
Water Extract ,(1.5 hr @ 100°C)				
Conductivity, µmhos/cm	19	24	20	31
Extractable Na, ppm	26	26	24	31
K, ppm	3	3	3	6
Cl, ppm	<1	<1	<1	4
Br, ppm	1	<1	<1	<1
Ca, ppm	<1	4	7	9
pH of extract	3.8	4.2	4.5	4.5

Fig 10

Eliminating Flame Retardant Greatly Improves HTS Performance of PLASKON 3400

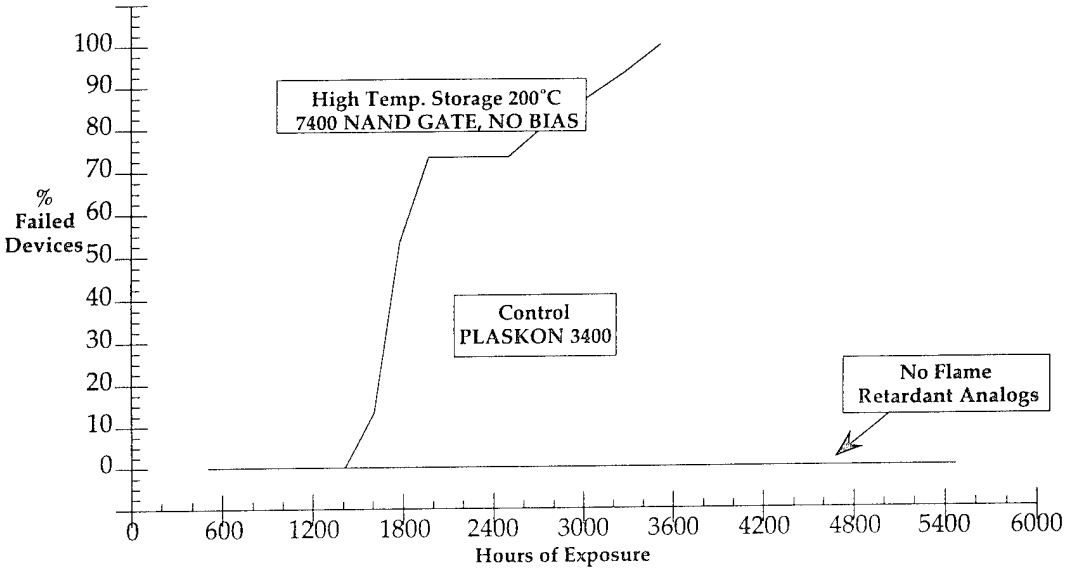
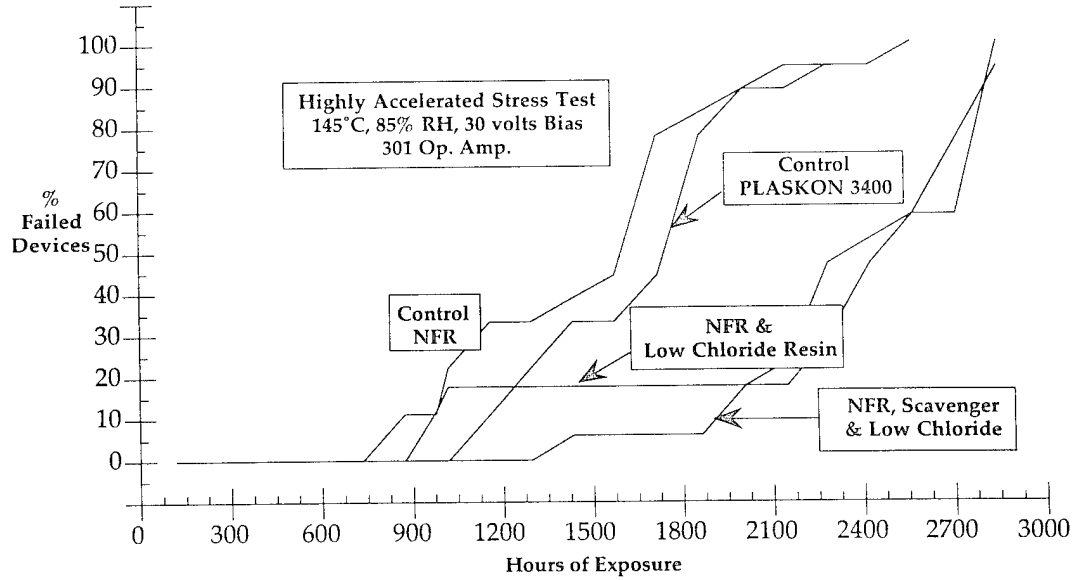


Fig 11

Flame Retardants Do Not Effect HAST Performance



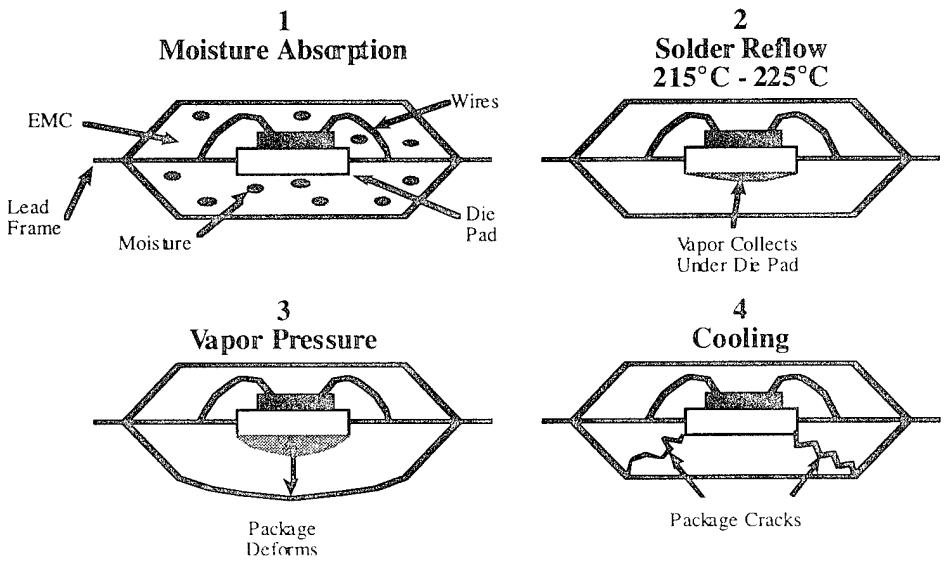
SELECTION OF AN ANTIPOPCORN EMC (Task 3.2)

A fifth EMC type chosen for inclusion in this program was an antipopcorn compound, Plaskon X 9074.07. Popcorning is a term used to describe packaging cracking of electronic devices during solder reflow or dip . This type of package cracking is the result of pressure exerted by moisture absorbed by the EMC quickly converting to steam at solder temperatures of 210-260°C.

Popcorn cracking is a problem affecting QFPs ,TSOPs, SOICs and other surface mount devices. At the time of this report, there was no EMC available which would completely eliminate popcorn cracking on all devices. In many cases, semiconductor manufacturers have to bake popcorn-susceptible plastic encapsulated surface mount components at 125°C to drive out moisture and then package the parts in sealed bags with desiccant for delivery to the assemblers.

The mechanism of popcorn cracking is shown in Fig 12. A standard epoxy molding compound will typically absorb moisture up to its saturation point of 0.4-0.6%. During solder reflow, the moisture turns to steam thereby exerting pressure on the bottom of the die pad and plastic. This pressure causes bulging of the plastic which leads to package cracking.

Fig 12



The following three characteristics of Plaskon X9074.07 contribute to reduced potential for popcorn package cracking .

- **Low moisture content - 0.28% at saturation as compared to 0.4-0.6% for standard EMCs.**
- **Low alpha 1 CTE - 13.5 ppm /°C as compared to >20 ppm /°C for standard EMC**
- **High flexural strength at solder reflow temperatures of 1.4 Kpsi at 215 °C as compared to < 1.0 Kpsi for standard EMC.**

Table 8

X 9074 .07 Typical Properties

Spiral flow, @ 177°C/1000 psi, cm	30
Ram follower gel time @ 177°C, sec	20
Viscosity @ 175°C, poise	60
Mold shrinkage, in/in	0.0025
Flammability, UL-94, 1/8"	VO
Moisture absorption 85C/85%RH, 168 hr, %	0.28
CTE, alpha 1, ppm/°C	13.5
CTE, alpha 2, ppm/°C	45
Glass transition temperature (Tg),°C	135
Thermal conductivity, cal/cm-sec-°C x 10^{-4}	17
Flexural strength @ 21°C, Kpsi	20
Flexural strength @ 215°C, Kpsi	1.4
Flexural modulus @ 21°C, Mpsi	3.0
Flexural modulus @ 215°C, Kpsi	100

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) classifies the moisture sensitivity of surface mount components as follows:

Table 9

IPC-SM-786A

Level	Moisture Sensitivity	Storage	Floor life	Preconditioning Moisture
1	None	No bag	No limit @ 30°C/85% RH	85°C/85%RH/ 168 hrs
2	Limited	Bag + Desiccant	1 Year @ 30°C/60% RH	85°C/60%RH/ 168hrs
3	Sensitive	Bag + Desiccant	1 Week @ 30°C/60% RH	30°C/60%RH/ 168hrs + MTL*
4	Highly Sensitive	Bag+ Desiccant	72 hrs @ 30°C/60%RH	30°C/60%RH/72 hrs + MTL
5	Highly Sensitive	Bag+ Desiccant	24 hrs @ 30°C/60% RH	30°C/60%RH/24 hrs + MTL

* MTL = manufacturer's life test, typically 7-14 days

Level 1 and level 2 preconditioning will typically result in moisture saturation of EMC encapsulated parts. At level 3 and below, EMC will become only partially saturated. The chemistry of X9074.07 is designed to give slow moisture diffusion and low total moisture absorption to meet the requirements of level 2 above and possibly level 1.

SUPPLY OF EMCS FOR NSC RELIABILITY TESTS (Task 3.3)

The five EMCs selected for inclusion in this program, were prepared in Plaskon's Singapore manufacturing facility under close supervision of Plant engineers and the Quality Department. Common raw materials used in the five compounds came from the same lots. The method of production and processing conditions were the same for the baseline compounds 3400 and ULS-12H and their high reliability analogs, 3400X and ULS-12HX. Large samples of the five compounds were shipped under refrigeration to National Semiconductor for device testing and to Plaskon Research for material characterization.

TESTING OF EMC PRODUCTION COMPOUNDS

Each of the five compounds was tested for those properties listed in the proposed specification template, Table 4. Test results for all items except water extract conductivity are listed in Table 10. All results for the baseline compounds and X9074.07 were within manufacturing specifications. The two high reliability analogs of the baseline compounds gave "as expected" results of longer flow, longer gel time, lower hot hardness and lower Tg than the baseline compounds. These differences are the result of cure interference by the scavengers used in the formulations.

Water extract conductivity test results are shown in Table 11. The test method used was SEMI Standard G-29 with extraction times of 24 to 240 hours. The EMC was prepared by post curing spiral flow specimens for 4 hours at 175°C, and then grinding these to a -40/+80 mesh powder. Parr Bombs were used for the extraction with 1.5 grams of powdered EMC and 15 milliliters of conductivity water. The bombs were sealed, placed in an oven at 121°C (15 psi) and then removed for testing at each of the testing intervals. Separate bombs were used for the five testing times, 24 , 48, 96, 120 & 240 hrs. A Dionex 2020i Ion Chromatograph was used to determine specific conductance, pH and concentrations of specific ions and cations.

It was anticipated, based on Plaskon internal historical data and input from semiconductor engineers, that the water extract conductivity test would be capable of differentiating between standard and high reliability EMC. Furthermore, data from Plaskon failure analysis and voluminous literature on this subject points to extractable halogens as prime culprits in device reliability failure. Also, as expected , the extraction tests show much lower extractable chlorine and bromine for the 3400X and ULS-12HX analogs as compared to the baseline compounds 3400 and ULS-12H. The lower chlorine could simply be the result of using lower chloride epoxy but the lower bromine has to be due to the action of the scavenger. The lower chloride and bromide of the "X" high reliability versions correlates with good HAST and HTS results shown in Figs 13 & 14.

The specific conductance values from the WEC test do not seem to correlate well with reliability. In fact, the higher reliability analogs have higher specific conductance indicating more mobile ions. The explanation for this is that the ion scavenger is a metal salt which partially ionizes in water to form two ionic species, one of which reacts with halogens while the other remains mobile. The free complex ion from the scavenger apparently has little or no effect on device reliability.

Table 10

Characterization of EMCs

Property	**3400**	**3400X**	**ULS-12H**	**ULS-12HX**	**X9074.07**
Lot Number	4G402	4G401	4G425	4G424	4G410
Spiral flow, in.	31	36	42	44	37
Ram Follower Gel Time, sec	19	23	24	31	21
Hot Hardness, Shore D	75	70	80	50	68
Flash & bleed					
3 mil, mm	5.2	5.3	7.9	7.6	12.6
2 mil, mm	2.7	2.9	2.3	2.3	2.6
1 mil, mm	3.5	4.1	2.6	2.6	2.2
Thermal Mechanical Analysis					
Alpha 1 , ppm/°C	22	22	14	14	14
Alpha 2 , ppm/°C	59	56	59	59	45
Glass Transition (Tg),°C	161	151	161	152	127
Flammability, UL-94 VO. 1/8"	Pass	Pass	Pass	Pass	Pass
Flexural Strength, Kpsi	18.0	18.7	18.6	16.1	22.9
Flexural Modulus, Mpsi	2.2	2.3	2.1	1.9	3.2
Energy to Break, in-lb	4.6	4.8	6.4	5.2	5.4
Strain at break, %	0.88	0.89	1.10	1.04	0.80
Specific Gravity	1.82	1.82	1.88	1.88	1.96
Ash content, %	72.7	72.2	78.2	79.7	81.7
Viscosity, poise (175°C)	68	75	74	41	79
Flow rate, mls/sec	1.6	1.4	1.4	2.6	1.3
Dielectric Constant	3.49	3.59	3.80	3.71	3.76
Dissipation Factor	0.003	0.003	0.002	0.004	0.003

A special low chloride ECN resin was used in 3400X and ULS-12HX, the higher reliability versions of the baseline compounds 3400 and ULS-12H.
Here is a comparison of the properties of the two epoxy cresol novolacs used in these compounds.

	Standard ECN	Low Chloride ECN
Epoxy equivalent weight	194	198
Total Chloride, ppm	760	400
Hydrolyzable chloride, ppm	390	170

Table 11

Water Extract Conductivity
(-40 /+ 80 mesh powder)

Hours	Conductivity	pH	Cations, ppm			Anions, ppm		
3400	µmhos/cm		Na	K	Mg	Ca	Cl	Br
24	39.5	5.0	19.0	4.6	<1.0	27.1	18.5	8.2
48	39.9	4.9	22.5	4.6	<1.0	17.1	19.2	9.5
96	86.0	4.2	26.3	10.6	<1.0	14.5	58.2	22.3
120	42.5	4.9	40.0	14.9	<1.0	15.6	51.3	27.7
240	47.9	4.2	29.8	27.8	<1.0	18.1	34.2	31.9
3400X								
24	110.6	4.3	27.2	4.6	1.1	24.0	5.0	2.4
48	161.5	4.1	19.8	4.6	1.3	37.2	11.8	5.4
96	149.7	4.0	32.8	8.6	2.1	37.1	10.6	5.0
120	157.1	4.0	34.7	13.7	<1.0	28.6	14.4	6.0
240	170.1	3.6	26.5	20.1	2.3	37.2	28.8	46.3
ULS -12H								
24	116.6	3.7	6.8	<1.0	<1.0	19.0	5.6	4.5
48	156.2	3.7	27.0	5.7	<1.0	21.2	20.1	13.2
96	169.8	3.8	21.8	9.7	<1.0	9.7	36.0	31.3
120	142.2	3.7	36.9	11.8	<1.0	16.7	28.0	23.5
240	170.1	3.6	30.4	22.6	<1.0	10.6	32.5	28.3
ULS-12HX								
24	199.3	3.9	27.2	8.3	1.1	21.1	8.2	1.7
48	187.9	3.7	23.3	9.5	1.3	37.2	7.3	1.4
96	189.2	3.7	32.0	13.2	7.1	24.2	22.4	3.2
120	196.7	3.7	37.7	18.3	<1	16.9	14.4	1.8
240	220.5	3.7	30.6	18.1	<1	15.7	15.3	3.9
X9074.07								
24	81.6	3.9	9.2	<1.0	<1.0	<1.0	21.9	12.0
48	104.1	3.8	29.8	<1.0	<1.0	<1.0	38.9	30.5
96	203.3	3.4	20.6	3.3	<1.0	<1.0	65.3	41.7
120	133.5	3.9	41.8	1.2	<1.0	<1.0	51.9	21.4
240	220.2	3.5	32.0	3.5	<1.0	<1.0	89.2	60.7

Extraction Conditions: 121°C in a pressure vessel
1.5 grams EMC in 15 mls high purity water

Sample Preparation: Post cured 4 hours @ 175°C

Table 12

Water Extract Conductivity
Retest (-100 mesh powder)

Hours	Conductivity	pH	Cations, ppm				Anions, ppm	
3400	µmhos/cm		Na	K	Mg	Ca	Cl	Br
24	30.2	5.0	15.5	2.6	<1.0	<1	1	<1.0
48	38.6	4.9	19.8	15.5	<1.0	26.2	12.4	2.8
96	68.5	5.0	18.8	18.1	<1.0	13.2	41.5	20.2
120								
240								
3400X								
24	52	4.6	34.2	8.9	<1.0	7.6	<1.0	<1.0
48	173	5.0	24.2	8.1	<1.0	20.6	4.4	1.0
96	204	4.4	28.4	15.5	<1.0	35.1	16.7	<1.0
120	167	4.3	58.0	41.0	<1.0	32.5	11.5	7.4
240	214	4.2	31.0	47.3	<1.0	53.3	43.7	67.4
ULS -12H								
24	137.4	4.2	25.4	11.4	<1.0	<1.0	15.8	25.8
48	130.4	4.3	24.9	7.0	<1.0	<1.0	12.8	17.9
96	192.0	4.3	36.0	21.0	<1.0	<1.0	13.3	19.1
120	165.6	4.2	35.8	8.9	<1.0	3.2	19.6	22.9
240	186.4	3.5	31.4	10.0	<1.0	3.8	24.7	12.7
ULS-12HX								
24	135.9	4.3	33.3	16.3	<1.0	<1.0	2.7	1.0
48	199.2	4.2	30.0	20.7	<1.0	4.7	8.5	2.2
96	216.7	4.3	30.0	13.7	<1.0	10.1	10.7	6.8
120	203.0	4.1	39.0	97.0	<1.0	5.7	22.5	15.6
240	203.0	3.7	35.0	41.7	<1.0	16.2	41.3	19.6
X9074.07								
24	136.1	4.3	44.3	<1.0	<1.0	<1.0	41.1	25.5
48	62.5	4.7	25.1	<1.0	<1.0	<1.0	8.9	6.2
96	88.7	4.5	27.5	<1.0	<1.0	<1.0	9.4	2.8
120	158.5	4.1	26.6	<1.0	<1.0	<1.0	63.8	40.0
240	163.8	3.6	32.0	<1.0	<1.0	<1.0	53.0	24.9

Figure 13

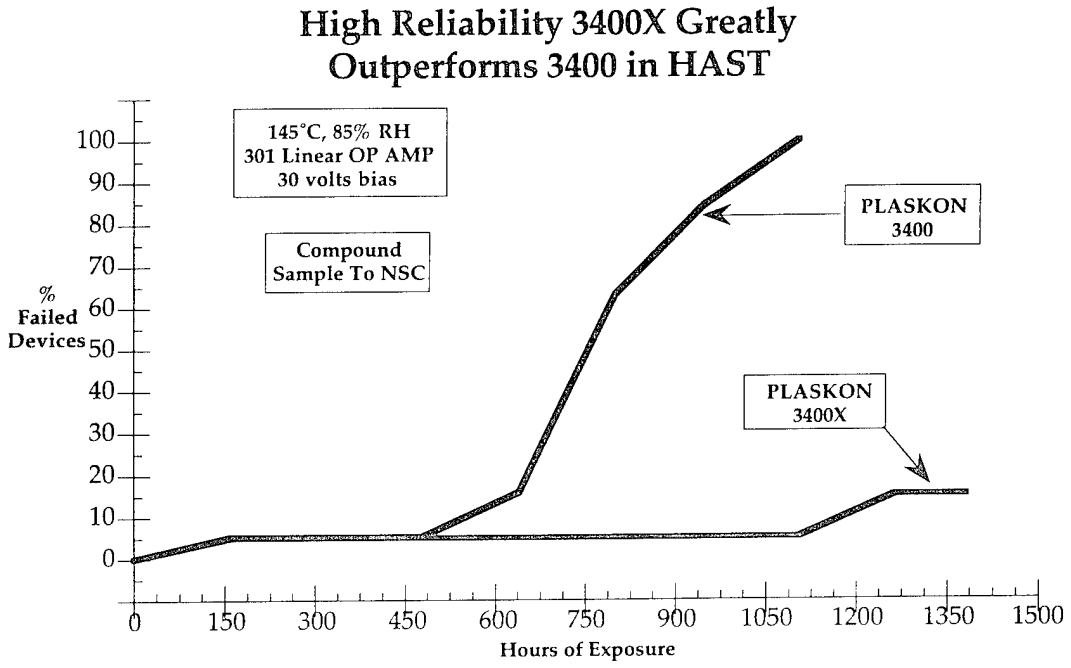


Figure 14

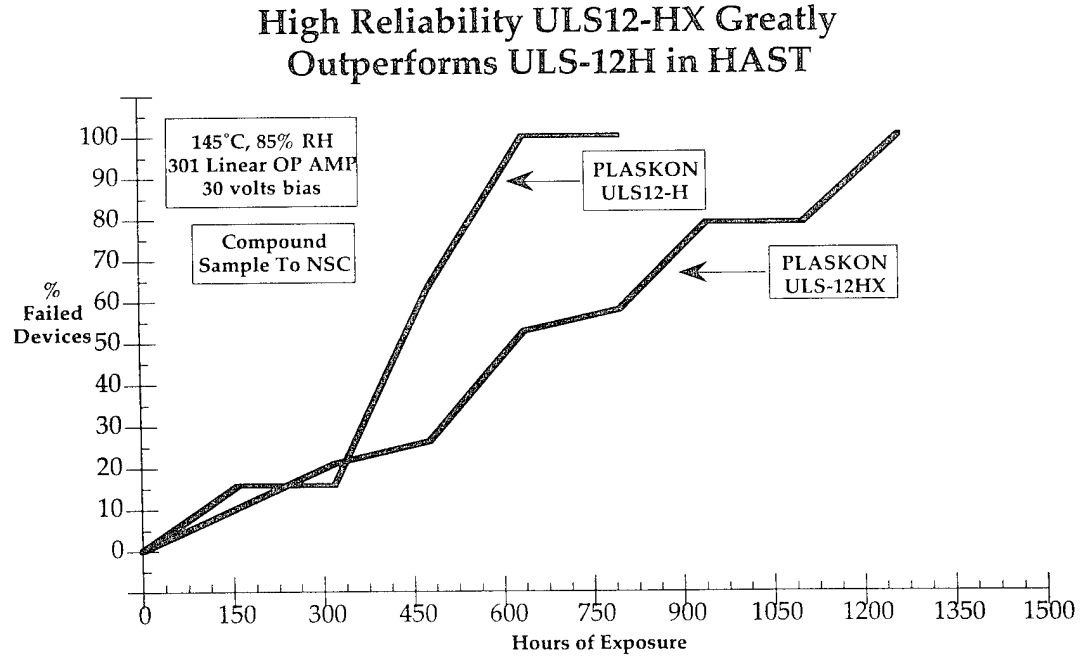


Table 12 is a repeat of WEC on the EMC production samples using minus 100 mesh powder instead of -40/ + 80 mesh. The expected results was more extracted ions. However, the data for the -100 mesh did not show an increase in ionic content but did show greater variability. Based on these results, a decision was made to use -40/ + 80 mesh powder for additional testing and in the final specifications.

Table 13 is WEC results for the three control compounds used by NSC, standard EMCs B8, B14 and B-24 a low stress EMC. Other characterization data for the controls are listed in Table 14. These data were used in the correlation of EMC properties to NSC and Crane reliability results.

Table 13

Characterization of NSC Control EMC's

Water Extract Conductivity

B-8								
Hours	Conductivity	pH	Cations,ppm				Anions,ppm	
	Micro mhos/cm		Na	K	Mg	Ca	Cl	Br
24	87.0	4.5	32.2	2.6	<1.0	54.4	32.0	27.9
48	91.2	5.7	33.7	2.2	<1.0	56.6	45.0	6.2
96	134.6	4.4	35.2	17.7	<1.0	116.8	60.5	17.3
120	132.5	4.6	68.0	46.0	<1.0	149.5	34.6	14.4
240	94.2	4.0	36.8	4.8	<1.0	72.1	13.3	15.9
B-14								
24	44.7	5.0	23.7	<1.0	<1.0	<1.0	10.2	15.9
48	56.2	4.9	26.9	<1.0	<1.0	<1.0	12.4	17.9
96	93.5	4.6	24.4	<1.0	<1.0	<1.0	23.4	30.7
120	97.5	4.9	73.0	50.0	<1.0	1.2	56.6	80.2
240	81.3	4.1	25.6	32.5	<1.0	<1.0	61.4	33.6
B-24								
24	51.8	5.0	19.3	<1.0	<1.0	<1.0	8.9	3.9
48	68.2	4.7	23.4	<1.0	<1.0	<1.0	7.0	17.9
96	137.7	4.4	25.6	<1.0	<1.0	<1.0	32.0	12.7
120	96.4	4.4	52.0	24	<1.0	<1.0	25.3	16.7
240	116.2	4.0	21.3	2.6	<1.0	<1.0	48.4	25.5

Table 14

Characterization of NSC Control EMCs

Property	B8	B14	B24
Lot Number			
Spiral flow, in.	22	22	32
Ram Follower Gel Time, sec	14	13	17
Hot Hardness, Shore D	87	90	75
Flash & bleed			
3 mil, mm	10	4	4
2 mil, mm	1	1	2
1 mil, mm	1	1	1
Thermal Mechanical Analysis			
Alpha 1 , ppm/°C	26	19	18
Alpha 2 , ppm/°C	61	55	76
Glass Transition (Tg),°C	173	157	179
Flammability, UL-94 VO. 1/8"	Pass	Pass	Pass
Flexural Strength, Kpsi	19	18	14.2
Flexural Modulus, Mpsi	2.3	2.4	1.8
Specific Gravity	2.1	2.2	1.88
Ash content, %			74.5
Viscosity, poise (175°C)	261	92	75
Dielectric Constant	3.5	3.8	3.8
Dissipation Factor	0.004	0.005	0.005

COMPARISON OF EMC PROPERTY DATA TO RELIABILITY DATA (Task 9.1)

Sandia National Laboratories compared standard molding compound to the high reliability analogs on NAT-01 triple track test chips in 159°C / 85% RH HAST at 5 volts bias. The failure mode is, of course, corrosion caused by EMC contaminates. Table 15 compares Sandia's time to 50% failure (t_{50}) to 48 hour extractable halogens for standard and low stress EMC and their analogs containing ion scavengers and low chloride resin.

Table 15

Unpassivated Triple Track Failure versus Extractable Halogens
68 ld PLCC 159C/85% RH / 5v

	Standard EMC	"X" Version
Triple Track Failures (t_{50}), hrs	40	200
	3400	3400X
Extractable Cl, ppm	19.2	11.8
Extractable Br, ppm	9.5	5.4
	ULS-12H	ULS-12HX
Extractable Cl, ppm	20.1	7.3
Extractable Br, ppm	13.2	1.4

These data show a definite relationship between low levels of extractable halogens and time to 50% failure in the Sandia Triple Track study.

A second study conducted by Sandia compares in plane compressive stress of the low stress EMCs using their ATCO4 die in a 68 ld PQFP. Data in Table 16 compares Sandia's results to the calculated stress index for each compound. The higher negative numbers reported by Sandia indicate higher stress.

Table 16

Sandia Stress Data Compared to Calculated Stress Index

	X9074.07	B24	ULS12H	ULS12HX
Stress, Mpa approx.	-111	-108	-93	-75
Stress Index	44.8	32.4	29.4	26.6

The coefficient of correlation for this set of values is 0.7908 which is less than ideal but there is a definite trend of EMC with lower stress index numbers giving lower stress on the Sandia die.

This comparison of the data from the Sandia studies to extractable halogens and stress index suggests that these two EMC material properties are good indicators of corrosion and stress potential .

Review of NSC and Crane Reliability Data

Table 17 shows National Semiconductor HTS and operational life test results on 68 ld PLCCs in which there were no device failures. The compounds studied in these tests were the two Plaskon low stress EMCs, the antipopcorn compound, the low stress control and ceramic.

Table 17

NSC 68 ld PLCC Test Results

EMC	Test	Conditions	Hours	% Fail
ULS-12H	HTS	175°C	4125	0
ULS-12HX	HTS	175°C	4125	0
X 9074.07	HTS	175°C	4125	0
B24 HTS	175°C	4125	0	
Ceramic	HTS	175°C	4125	0
ULS-12H	Op Life	125°C	4000	0
ULS-12HX	Op Life	125°C	4000	0
X 9074.07	Op Life	125°C	4000	0
B-24	Op Life	125°C	4000	0
Ceramic	Op Life	125°C	4000	0

On this device and under these conditions, each of the EMC encapsulant is equivalent to ceramic.

Table 18 shows NSC electrical test results after temperature cycling at -65°C to + 150°C for the low stress compounds, the antipopcorn EMC and ceramic.

Table 18

Compound	Electrical Failures	
	1500 cycles	2000 cycles
ULS-12H	0/36	12/36
ULS-12HX	0/36	0/36
X 9074.07	0/36	0/36
B-24	0/36	0/36
Ceramic	0/25	0/25

The massive failures of ULS-12H at 2000 cycles as compared to 0 for ULS-12HX are most likely caused by "dry corrosion" due to free bromide and chloride as described by Tom Raymond [4] from AMD. ULS-12HX and X9074.07 both contain anionic scavengers to capture free bromide which is known to contribute to ball bond degradation and chloride which can corrode the ball bond pad. This writer does not know the exact composition of B-24 (different supplier) and therefore cannot comment on whether or not it contains an anionic scavenger.

Tables 19 & 20 show NSC HAST results at 130°C and 159°C with and without preconditioning. None of the ceramic devices used in NSC or Crane studies were preconditioned.

Table 19

NSC 68ld PLCC HAST (fail/total devices)
130°C

	216 hrs		432 hrs		648 hrs		864 hrs		1080 hrs	
Compound	P	NP	P	NP	P	NP	P	NP	P	NP
ULS-12H		0/20		0/20		0/20		0/20		0/20
ULS-12HX	1/20	0/20	1/19	0/20	1/18	0/20	6/17	0/20	0/11	0/20
X 9074.07		0/20		0/20		0/20		0/20		0/20
B-24	12/20									
Ceramic	0/24		0/24		0/24		0/24		0/24	

P= Preconditioned
NP = Not preconditioned

Table 20

NSC 68ld PLCC HAST (fail/ total devices)
159°C/85%RH

	72 hrs		108 hrs		216 hrs		432 hrs		648 hrs	
Compound	P	NP	P	NP	P	NP	P	NP	P	NP
ULS-12H	0/21		0/21		0/21		12/21			
ULS-12HX		0/21		0/21		0/21		0/21		5/21
X 9074	1/21		0/20		20/20					
B-24	11/21	0/21		0/21		0/21		0/21		4/21
Ceramic	0/24		0/24		0/24		0/24		0/24	

With regards to the EMC used in these HAST tests, only the following conclusions can be drawn :

1. **Preconditioning accelerates device failure in HAST.**
2. **Ceramic is superior to EMC in HAST**
3. **B-24 is worse in preconditioned HAST than the other EMCs.**

Review of Crane HAST Results

At Crane Naval base, 130°C and 159°C HAST tests were conducted on DIPs and SOICs encapsulated in standard EMC (3400), its high reliability analog, B8 and B14 controls and ceramic. Tables 21 & 22 compare 130°C HAST results with 48 hour extractable halogens.

Table 21

Crane HAST @ 130°C
Extractable Halogens versus Failures

Compound	**Failure, %** DIPs no precon		SOICs 5V		**Extractable** 48 hr @ 121°C	
	216 hrs	648hrs	216 hrs	648hrs	Cl	Br
3400	0	0	0	0	19	10
3400X	0	0	0	0	12	5
B8	0	0			16	28
B14			0	0	12	18
Ceramic	0	0	0	0		

Table 22

Crane HAST @ 130°C

Compound	Failure, % DIPs precon		SOICs 30V		Extractable 48 hr @ 121°C	
	216 hrs	648 hrs	216 hrs	648 hrs	Cl	Br
3400	53	60	0	7	19	10
3400X	20	40	73	100	12	5
B8	53	67			16	28
B14			33	100	12	18
Ceramic	0	0	0	0		

Preconditioning and higher bias voltage resulted in an unexpected and inconsistent high rate of failure. One anomaly is that 3400X with lower extractables had fewer failures on DIPs than 3400 but the reverse was true for the 30 volt SOICs. One theory as to the cause of the high level of failures is that the chloride containing organic solder flux used in preconditioning somehow contaminated the devices.

Table 23

Crane HAST @ 159°C
Extractable Halogens versus Failures

Compound	Failure, % DIPs		SOICs 5V		Extractable 48 hr @ 121°C	
	216 hrs	648 hrs	324 hrs	648 hrs	Cl	Br
3400	0	60	0	67	19	10
3400X	7	62	0	33	12	5
B8	40	100			16	28
B14			27	100	12	18
Ceramic	0	0				

Table 24

Crane HAST @ 159°C

Compound	Failure, % DIPs precon		SOICs 30V		Extractable 48 hr @ 121°C	
	216 hrs	432 hrs	216 hrs	324 hrs	Cl	Br
3400	87	100	100	100	19	10
3400X	73	100	100	100	12	5
B8	100	100			16	28
B14			60	100	12	18
Ceramic	0	0				

The 159°C HAST study by Crane again shows that preconditioning and high voltage cause very early massive HAST failures. The results of these tests suggest that HAST at 159°C with 30 volts bias may be too harsh and therefore incapable of differentiating between standard EMC and the "X" versions

Water extract conductivity tests were run on 3400 failed devices to determine why 30 volt SOICs devices failed faster than the 5 volt SOICs. In this experiment, chips from a 3400 SOIC control and two failed 3400 SOICs were ground to a fine powder, placed in conductivity water at room temperature (23°C) for one week and then tested for extractable ionics. Results detailed in Table 25 show higher levels of extractables for EMC from devices subjected to 30 volts bias. It is reasonable to conclude that the early failures of the 30 volt devices could be due to increased free ionics as the result of aggressive electro- chemical reactions.

Table 25

Plaskon 3400 SOICs
Water Extract of Failed Devices 159C HAST

	Control		
Time in HAST, hrs	0	216	648
Test voltage	30	5	
Extractable ionics, ppm			
Na	2	33	3
NH4	<1	<1	<1
K	<1	16	<1
Cl	3	15	1
Br	<1	1	<1
SO4	<1	8	2

RECOMMENDED MILITARY EMC SPECIFICATIONS (Task 9.1)

Plaskon's recommendations for specifications covering the three types of Epoxy Molding Compounds studied in this program, standard grade, low stress and antipopcorn are detailed in the next three pages of this report.

Each of these specifications lists properties necessary to characterize basic moldability, thermal mechanical , electrical and chemical properties of EMC. Limits are set for each EMC to control extractable ionics, especially chloride and bromide which are known to cause corrosion and ball bond failure under moisture and/or heat stress. Stress Index, the mathematical product of alpha 1 CTE and flexural modulus, has been added to differentiate the low stress EMC from the standard grade. Limits of CTE and flexural modulus for low stress EMC are necessarily lower than those of standard grade.

Moisture content and high temperature flexural strength, have been added to the antipopcorn EMC specification to differentiate it from the other two grades in this program . Moisture absorption is to be determined by ICP's most stringent moisture conditioning protocol of 168 hours at 85°C/85% RH.

The three specifications should include a general description of the EMC, i.e silica filled epoxy resin with a novolac hardener and one or more ion scavengers to capture trace amounts of free halogens and alkali metals. The specific chemical structure and amount of scavenger used are generally EMC manufacturer's trade secrets and therefore are not included in the list of EMC properties .

Each of the three specifications is divided into two types for use in the two most common types of molding operations. Type 1 is for conventional molding, type 2 for automated gangpot.

The test methods listed in these specifications are accepted Industry standards
Test apparatus and sample descriptions are included in appendix B.

Standard EMC Specification

Property	Method	Conditions	Units	Type 1 Limits	Type 2 Limits
Moldability					
Spiral flow	SEMI G11	175°C/1000 psi	cm	35-75	60-125
Ram Follower Gel Time	SEMI G11	175°C/1000 psi	seconds	8-12	10-25
Hot Hardness	Shore D	175°C (90 seconds)		≥ 60	≥ 60
Flash & Bleed	SEMI G45	175°C/1000 psi			
2 mil Channel			millimeters	≤ 20	≤ 20
0.25 mil Channel			millimeters	≤ 5	≤ 5
Thermal Properties					
Coefficient of Thermal Expansion	SEMI G13	Post cure			
Alpha 1		4 hrs/ 175°C	ppm/°C	≤ 26	≤26
Alpha 2			ppm/°C	≤ 80	≤ 80
Glass Transition Temp. (Tg)			Degree C	≥ 140	≥ 140
Flammability	UL-94	1/8" thickness		V0	V0
Physical Properties					
Flexural Strength	D790	Room Temp.	Kpsi	≥ 16	≥ 16
Flexural Modulus	D790	Room temp.	Mpsi	≤ 3.5	≤ 3.5
Specific Gravity	D792			1.5-3.0	1.5-3.0
Ash content	D2584	650°C	Percent	65-85	65-85
Viscosity	D3835	175°C/1000 psi	poise	≤ 300	≤ 300
Electrical					
Dielectric Constant	D149	1 KHz/room temp		≤ 5.0	≤ 5.0
Dissipation Factor	D149	1 KHz/ room temp		≤ 0.010	≤ 0.010
Volume Resistivity	D257	Room temp.	Ohm-cm	≥ 10^{14}	≥ 10^{14}
Analytical					
Water absorption		85°C/85RH/168 hr	Percent	≤0.60	≤ 0.60
Water Extract Conductivity	SEMI G29	48 hrs/121°C	μ mhos/cm	≤ 150	≤ 150
pH of Extract				3.5-7.5	3.5-7.5
Extractable Sodium			ppm	≤ 50	≤ 50
Potassium			ppm	≤ 50	≤ 50
Chlorine			ppm	≤ 25	≤ 25
Bromine			ppm	≤ 25	≤ 25
Iron			ppm	≤50	≤ 50
Total Antimony	Xray Fluorescence		Percent	≤ 2.5	≤ 2.5
Total Bromine	Xray Fluorescence		Percent	≤ 1..0	≤ 1..0

Low Stress EMC Specification

Property	Method	Conditions	Units	Type 1 Limits	Type 2 Limits
Moldability					
Spiral flow	SEMI G11	175°C/1000 psi	cm	35-75	60-125
Ram Follower Gel Time	SEMI G11	175°C/1000 psi	seconds	8-12	10-25
Hot Hardness	Shore D	175°C (90 seconds)		≥ 60	≥ 60
Flash & Bleed	SEMI G45	175°C/1000 psi			
2 mil Channel			millimeters	≤ 20	≤ 20
0.25 mil Channel			millimeters	≤ 5	≤ 5
Thermal Properties					
Coefficient of Thermal Expansion	SEMI G13	Post cure			
Alpha 1		4 hrs/ 175°C	ppm/°C	≤ 18	≤ 18
Alpha 2			ppm/°C	≤ 65	< 65
Glass Transition Temp. (Tg)			Degree C	≥140	≥ 140
Stress Index				≤ 35	≤ 35
Flammability	UL-94	1/8" thickness		V0	V0
Physical Properties					
Flexural Strength	D790	Room Temp.	Kpsi	≥14	≥14
Flexural Modulus	D790	Room temp.	Mpsi	≤ 2.0	≤2.0
Specific Gravity	D792			1.5-3.0	1.5-3.0
Ash content	D2584	650°C	Percent	65-85	65-85
Viscosity	D3835	175°C/1000 psi	poise	≤ 100	≤ 100
Electrical					
Dielectric Constant	D149	1 KHz/room temp		≤ 5.0	≤ 5.0
Dissipation Factor	D149	1 KHz/ room temp		≤0.010	≤ 0.010
Volume Resistivity	D257	Room temp.	Ohm-cm	$\geq 10^{14}$	$\geq 10^{14}$
Analytical					
Moisture absorption		85°C/85%RH/168 hr	Percent	≤0.60	≤ 0.60
Water Extract Conductivity	SEMI G29	48 hrs/121°C	μ mhos/cm	≤ 150	≤ 150
pH of Extract				3.5-7.5	3.5-7.5
Extractable Sodium			ppm	≤ 50	≤50
Potassium			ppm	≤ 50	≤ 50
Chlorine			ppm	≤25	≤25
Bromine			ppm	≤ 25	≤25
Iron			ppm	≤ 50	≤50
Total Bromine	Xray Fluorescence		Percent	≤ 1..0	≤ 1..0
Total antimony	Xray fluorescence		Percent	≤ 2.5	≤ 2.5

Antipopcorn EMC Specification

Property	Method	Conditions	Units	Type 1 Limits	Type 2 Limits
Moldability					
Spiral flow	SEMI G11	175°C/1000 psi	cm	35-75	60-125
Ram Follower Gel Time	SEMI G11	175°C/1000 psi	seconds	8-12	10-25
Hot Hardness	Shore D	175°C (90 seconds)		≥ 60	≥ 60
Flash & Bleed	SEMI G45	175°C/1000 psi			
2 mil Channel			millimeters	≤ 20	≤ 20
0.25 mil Channel			millimeters	≤ 5	≤ 5
Thermal Properties					
Coefficient of Thermal Expansion	SEMI G13	Post cure			
Alpha 1		4 hrs/ 175°C	ppm/°C	≤ 18	≤ 18
Alpha 2			ppm/°C	≤ 65	< 65
Glass Transition Temp. (Tg)			Degree C	≥130	≥ 130
Stress Index				≤ 50	≤ 50
Flammability	UL-94	1/8" thickness		V0	V0
Physical Properties					
Flexural Strength	D790	Room Temp.	Kpsi	≥18	≥18
Flexural Modulus	D790	Room temp.	Mpsi	≤ 4.0	≤4.0
Flexural Strength	D790	215 °C	Kpsi	≥1.0	≥1.0
Flexural Modulus	D790	215 °C	Kpsi	≤ 150	≤1 50
Specific Gravity	D792			1.5-3.0	1.5-3.0
Ash content	D2584	650°C	Percent	75-90	75-90
Viscosity	D3835	175°C/1000 psi	poise	≤ 200	≤ 150
Electrical					
Dielectric Constant	D149	1 KHz/room temp		≤ 5.0	≤ 5.0
Dissipation Factor	D149	1 KHz/ room temp		≤0.01	≤ 0.010
Volume Resistivity	D257	Room temp.	Ohm-cm	$\geq 10^{14}$	$\geq 10^{14}$
Analytical					
Moisture absorption		85°C/85%RH/168 hr	Percent	≤0.30	≤ 0.30
Water Extract Conductivity	SEMI G29	48 hrs/121°C	μ mhos/cm	≤ 150	≤ 150
pH of Extract				3.5-7.5	3.5-7.5
Extractable Sodium			ppm	≤ 50	≤50
Potassium			ppm	≤ 50	≤ 50
Chlorine			ppm	≤25	≤25
Bromine			ppm	≤ 25	≤25
Iron			ppm	≤ 50	≤50
Total Bromine	Xray Fluorescence		Percent	≤ 1..0	≤ 1.0
Total antimony	Xray fluorescence		Percent	≤ 2.5	≤ 2.5

Appendix A

Abbreviations

ASTM	American Society for Testing & Materials
Br	Bromine
C	Centigrade
Cl	Chlorine
cps	Centipoise
CTE	Coefficient of Thermal Expansion
DIP	Dual inline package
EMC	Epoxy molding compound
EOCN	Epoxy Ortho Cresol Novolac resin
Fe	Iron
g	gram
g/cc	grams per cubic centimeter
HAST	Highly accelerated stress test
Hr	Hour
HTS	High Temperature Storage
ICP	Institute for Interconnecting and Packaging Electronic Circuits
in	inch
K	Potassium
Kg	Kilogram
mm	millimeter
Na	Sodium
PaS	Pascal seconds
PLCC	Plastic leaded chip carrier
PN	Phenolic Novolac resin
ppm	Parts per million
psi	pounds per square inch
QFP	Quad flat pack
RH	Relative humidity
RFGT	Ram Follower Gel Time
s	Second
SEMI	Semiconductor Equipment & Materials International
SOIC	Small outline integrated circuit
TSOP	Thin small outline package
Tg	Glass transition temperature
UL	Underwriters Laboratories
WEC	Water extract conductivity

Appendix B

Test Equipment and Samples

Spiral Flow & Ram Follower Gel Time

15 Ton Transfer Molding press with displacement transducer
486 Computer interface for data reduction
EMMI Spiral Flow Mold, Kras Corp., Fairless Hills, PA
Test sample : 15 to 25 grams of granular EMC

Hot Hardness

Shore Durometer D (ASTM D2240)
Measured on hot molded cull during the spiral flow test

Flash and Bleed

15 Ton Transfer Molding press
Flash Mold, Kras Corp., Fairless Hills, PA
Test sample : 15 to 25 grams of granular EMC

Thermal Mechanical Analysis (TMA)

Dupont 2000 Analyzer with model 943 TMA module
Sample: molded cylinder 5 mm diameter x 5 mm

Flammability - UL-94

Laboratory burner , 4" tube with inside diameter of 0.370"
Test Specimen: Molded bars, 5" x 0.5" x Test thickness)

Flexural Strength and Modulus

Instron model 1122, or equivalent
S.E.S. temperature chamber model UTB 1.2I
Test specimens: Molded bars 5"x 0.5" x 0.25"

Specific Gravity

Pycnometer, 750 ml
Test specimen: Molded bars, 5" x 0.5" x 0.0625"

Ash Content

Muffle Furnace capable of heating to 700°C
Sample size: One gram of granular material

Viscosity

Shimadzu CFT-500 Automatic Rheometer
Test sample: EMC pellet, 3.50 gram by 11 mm diameter

Appendix B (cont.)

Dielectric Constant and Dissipation Factor

Gen Rad 1688 Precision LC Digibridge
Specimen holder (Rhode & Schwartz Type KMT Variable capacitor)
Test Specimen: Molded EMC disk 4" in diameter by 0.125" in thickness

Volume and Surface Resistivity

Hewlett-Packard 4329A High Resistivity Meter
HP model 1608A Resistivity Cell
Test specimen: Molded disk 4" in diameter by 0.125" in thickness

Water absorption

ESPEC F Series Humidity Chamber, Model PR-2F
Test specimen: Molded EMC disk, 2" diameter by 0.125" thick

Water Extract Conductivity

Ion Chromatograph, Dionex 2020i
ESPEC F Series Humidity Chamber, Model PR-2F
Parr 4749
Spex grinding mill
pH meter with standard combination pH and reference electrode
Conductivity meter, YSI Model 34 with 1.0/cm conductivity cell
Test sample: 1.5 of -40/+80 mesh EMC/15 mls of conductivity water

Highly Accelerated Stress Test (HAST)

Espec humidity chamber, Model TPC 410
Variable power supply, capable of supplying 30 volts/2 amps
Circuit test boards - South Bay Electronics design, Type 1A, Rev A, coated with Dow Corning conformal coating 1-2577
Tektronics curve tracer Model 576
High purity water, >17 megohm or better
Test device: National Semiconductor LM301 operational amplifier

High Temperature Storage

HotPak oven capable of heating to 200° C
Genrad Model 1732M Digital IC Test System
Test device: Texas Instruments 7400 Quad Nand Gate

Total Antimony and Bromine

X-ray Fluorescence, ASOMA model 8620
Test sample -40/+100 mesh powder.

End Notes

1 Popcorn refers to the phenomenon of plastic package cracking during solder reflow due to pressure caused by absorbed water rapidly converting to steam.

2 M. Nakoa, T. Nishiokam, M Shimizu, H Tabatam, and K Ito , "Degradation of Brominated Epoxy Resin and Effects on Integrated Circuits Device Wirebonds," Polymers for Electronics Packaging and Interconnects, ACS Symposium Series 407, pp 375-443, 1989.

3 Mizugshira, H. Higuchi, and T. Ajiki, "Improvement of Moisture Resistance by Ion Exchange Process, :IEEE, International Reliability Physics Symposium, 1987

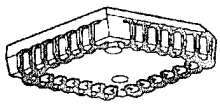
4 Avoid Bond Pad Failure Mechanisms in Au-Al Systems, Tom Raymond, Semiconductor International, Sept 1989, pp 152-158.

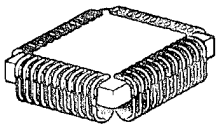
PLASTIC PACKAGE AVAILABILITY PROGRAM

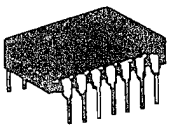
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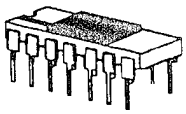
SECTION 3

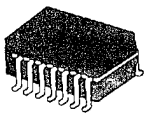
Task 4.0 Moisture & Corrosion Test Chip Development











PLASTIC PACKAGE AVAILABILITY PROGRAM

"Sensor Chip Development"

SANDIA NATIONAL LABORATORIES
ADVANCED PACKAGING DEPARTMENT
ALBUQUERQUE, NM 87185-1082



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INTRODUCTION

The objective of the Plastic Package Availability (PPA) program is to provide the data necessary for the DoD to revise its specification concerning the use of plastic ICs in military systems. To achieve this objective National Semiconductor assembled a team consisting of Dow Corning, Honeywell, Plaskon Electronic Materials and Sandia National Laboratory. Each member of the team will make contributions based on their own area of unique expertise. Honeywell is to report on system considerations for the replacement of hermetic with plastic ICs based on field experience with commercial products. Plaskon will review current commercial state-of-the-art materials and processes and develop a preliminary specification for military grade epoxy molding compounds. Dow Corning is to demonstrate improvements in reliability of plastic packaged ICs through the use ceramic moisture barrier die coat technology. The role of Sandia National Laboratory in the PPA program is development of a moisture and corrosion test chip that can be used to validate and possibly even qualify the materials and processes generated by the other team members.

TASK DESCRIPTION

The moisture/corrosion test chip development task is broken down into the following sub-tasks:

4.1 Test Chip Design - Sandia shall design and develop a silicon test chip for measuring the susceptibility to moisture activated corrosion of a molded part at the die surface. This task will include design, mask making, and process development.

The test chip shall have moisture sensors and corrosion detection features. The sensor should be able to withstand 300°C for a minimum of 4 hours without degradation of performance.

The moisture sensors shall consist of at least one set of two sensors, one uncovered and one covered with standard SNL chip passivation. The uncovered sensor shall allow detection of moisture absorption into the plastic, while the protected sensor shall measure the breaching of the passivation, (e.g., presence of pinholes). The moisture sensor shall use Sandia's CMOS technology: the detector shall be made up of a microplate capacitor with the silicon substrate/wafer as one plate and a fine grid structure of IC metalization as the other; the dielectric shall be an anodized silicon surface layer.

The corrosion detector shall consist of two sets of triple track structures, one uncovered and one covered with chip passivation. The covered detector shall be used to evaluate the protective properties of the passivation layer against moisture activated corrosion. The uncovered detector shall be used to evaluate the susceptibility to corrosion of the Al IC conductors adjacent to molding compound and to provide secondary measurement of bulk moisture content in the molding compound.

The test chip shall be produced in a 100 mil square modular unit, which can be used as a single die, or a quad, or an array of multiple dies.

4.2 Develop Test Procedures - Test procedures shall be developed for use of the moisture sensor for detection of defects or pinholes in chip passivation. Procedures shall be developed for use of the corrosion detector in HAST on test chips in open and molded packages.

4.3 Test Chip Calibration - Calibration graphs and measurement data, including mean and standard deviation of a representative sample population from the wafers of the deliverable group of test chips, shall be provided for moisture levels in the range of 500 to 6,000 ppm_v. In addition, measurement data shall be provided from a sample population calibrated before and after bake-out at 300°C for a minimum of 4 hours to demonstrate minimal performance degradation after exposure to elevated temperature.

Results of the following "best effort" experiments to be undertaken at the discretion of SNL shall be shared with NSC:

- In situ HAST performance of open package moisture sensor.
- In situ HAST performance of moisture sensor in molded or liquid encapsulated (globbed) package.
- Capacitive response of unpassivated corrosion detector in molded package to various humidity level, possibly including HAST conditions.

- Determination of diffusion rate through molding materials using the unpassivated moisture sensor.
- Moisture concentration at the chip surface using the unpassivated moisture sensor or triple track corrosion detector.

4.4 Moisture Test Specification - SNL shall provide suggested elements to a possible Plastic Qualification specification. These elements will describe how SNL feels that the moisture and corrosion test chip should be used to aid in qualification of a non-hermetic IC assembly process. Five hundred die will be delivered which have been visually inspected for shorts. The GDS II mask design file will be delivered. An informal document shall be delivered containing descriptions of the manufacturing process, chip cross-sections at intermediate processing steps, anodization procedure, final chip layout, and additional data deemed pertinent.

During the Open Program Review on 5/19/94 in San Diego, it was suggested by industry observers that the Sandia ATC04 Stress Test Chip be used to evaluate the various epoxy molding compounds formulated by Plaskon for the program. A follow-on task was agreed to:

4.5 Stress Measurement using ATC04 - Measure and compare stress properties of the molding compounds developed by Plaskon for the PPA program. In addition, evaluate the effect of preconditioning on the stress profile in the molded package.

A second part to this task involving evaluation of the effect of curing time on the stress profile of 68-lead PLCCs was beyond the scope of current PPA funding and will be added to a separate extension proposal.

TASK 4.1 – TEST CHIP DESIGN

The test chip is comprised of a moisture sensor and a corrosion detector. The corrosion detector is a conventional triple track corrosion structure similar to that used in previous ATCs (Assembly Test Chips) designed and built by Sandia. Design particulars will be covered at the end of this section. The moisture sensor is required to detect pinholes or defects in a moisture barrier coating and withstand processing temperatures of 300°C for at least 4 hours. These requirements are especially challenging and experimentation was necessary to validate the best design approach.

Moisture Sensor Options: The need for a sensor that is compatible with standard microelectronics fabrication processes and able to withstand processing temperatures typical of the application of plasma enhanced chemical vapor deposited (PECVD) coatings, pointed to volume effect capacitors. Volume effect sensors measure changes in impedance, capacitance, or resistivity due to moisture adsorption in a porous region contained between two electrodes. Within this group of sensors, several porous media have been previously investigated, including Al_2O_3[1,2] (aluminum oxide), polyimide[2], and porous silicon[3]. The most common of these is the Al_2O_3 moisture sensor, a passive device made by forming a thin porous film of non-conductive Al oxide on an Al conductor using a sulfuric acid anodic etch process. The bottom electrode of the capacitor is the unanodized portion of the Al conductor and the top electrode is generally formed by depositing a thin, permeable film of Au or Pd on the oxide. The oxide region contains columnar pores with diameters 100–150 Å. Vapor phase moisture is transported into the pores by the process of ordinary diffusion. As the partial pressure of water vapor increases, water molecules will adhere to the pore walls creating monolayers of water distributed throughout the surface area of the porous film. At a certain critical partial pressure, liquid water will begin to fill the pores through the process of microcapillary condensation. The presence of vapor and liquid phase water in the porous dielectric region of the capacitor causes a change in the effective dielectric constant and a corresponding change in capacitance. The sensitivity of the capacitor to moisture is enhanced by the polar nature of the water molecule, which has a relative dielectric constant of ~ 80. Unfortunately, the Al_2O_3 moisture sensor appears to desensitize after exposure to temperatures above ~ 150°C[2], and is not intrinsically compatible with standard IC processing.

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[1] R. F. Macko, in *Proceedings of the NBS/RADC Workshop on Moisture Measurement Technology for Hermetic Semiconductor Devices, II*, edited by E. C. Cohen and S.Ruthberg, NBS Special Publication 400-72, 110-112 (1982).

[2] J. N. Sweet, M. R. Tuck, D. W. Peterson, and S. W. Palmer in *Proceedings of the Ninth IEEE International Electronics Manufacturing Technology Symposium*, edited by W. M. Beckenbaugh, 229-235 (1990).

[3] R. C. Anderson, R. S. Muller, and C. W. Tobias, *Sensors and Actuators* A21-A23, 835 (1990).

A capacitive moisture sensor can also be fabricated from porous Si (PS). PS is formed during the anodization of doped Si in a bath of hydrofluoric acid (HF). The density of PS can vary from 20–80% that of bulk Si. PS retains the crystalline structure of the starting material and has specific surface areas that can range between 40 and 400 m^2/g[4]. The porous microstructure depends largely on the dopant type and concentration of the starting wafer. PS formed from *n*-type Si have columnar, non-connected pores similar in structure to Al_2O_3 porous films. PS from *p*-type Si substrates contain finer pores with diameters in the 100 Å range. Lightly doped *p*-type Si substrates (< 1 Ω-cm), in particular, develop *interconnected* pores in a sponge-like matrix.

Anodization Process: The formation of PS through anodic etching of Si is illustrated in Fig. 1. The Beale[5] theory assumes the Fermi level is pinned at mid-gap, much like a Schottky barrier diode. Charge flows across the Schottky barrier by thermionic emission in lightly doped *p*-type Si substrates. The current flows preferentially down the electrolyte path of least resistance, dissolving Si at the pore tips due to local field enhancement. Local field enhancement is greatest during the onset of pore growth when the radius is smallest and decreases with time. The orientation of a given pore tip and its subsequent growth direction can vary from normal to the surface to perpendicular to the surface. The "off normal" pores eventually intercept other pores creating the interconnected pore morphology common to lightly doped *p*-type PS.

The anodization process is carried out in a double-tank electrochemical cell, where both sides of the wafer are in contact with HF electrolytes[6]. The cell is constructed of high density polyethylene with sapphire windows at each end to facilitate front and backside illumination with external light sources for carrier generation. A liquid-tight seal is obtained with a cam-type lever which compresses O-rings fitted in each half-cell against the wafer. The half-cells are cylindrical cavities; thus, the electrolyte volumes between the wafer and the two platinum mesh electrodes have the same cross-section as the exposed region of the wafer. This geometry minimizes current crowding at the wafer edge and optimizes the primary current distribution. Anodization parameters used for the NAT-01 sensors are 5 mA/cm^2 for 252 seconds in 5% HF by weight on 0.14 – 0.3 Ω-cm *p*-type 152 mm (six inch) Si wafers. This process nominally results in a 0.9 μm film of 80% porosity.

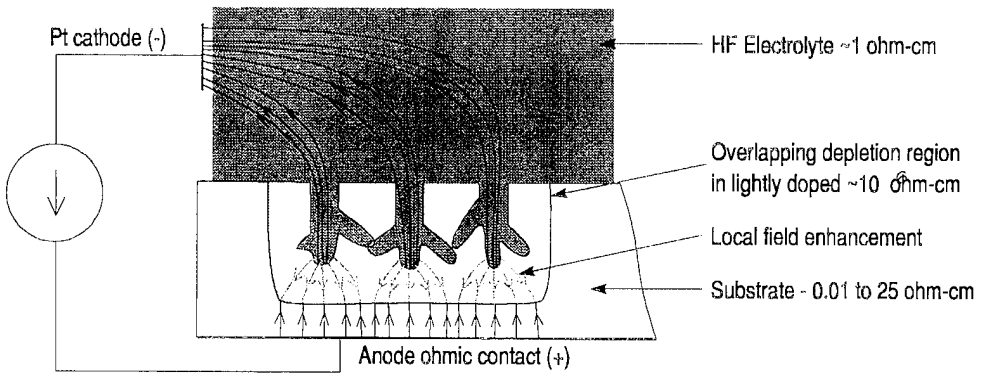


Fig. 1. Beale model for porous film formation in Si. The backside ohmic contact is normally achieved with a platinum electrode in a wet chemical cell using ~ 49% HF electrolyte solution.

Diffusion experiments: One of the key requirements for the moisture sensor is response to a point moisture source characteristic of a defect or pinhole in a moisture barrier coating passivation system. Two experiments were carried out to demonstrate lateral diffusion through a PS film made from lightly doped *p*-type Si. In the first experiment, dot capacitors were made with 0.050 inch diameter 300 Å thick Au dots and 1 μm thick Al dots. Au

[4] T. R. Guilinger, M. J. Kelly, and S. S. Tsao in *Silicon-on-Insulator and Buried Metals in Semiconductors*, edited by J. C. Sturm, C. K. Chen, L. Pfeiffer, and P. L. F. Hemment, Material Research Society Proceedings **107**, 455-458 (1988).

[5] M. I. Beale, J. D. Benjamin, M. J. Uren, N. G. Chew, A. G. Cullis, "An Experimental and Theoretical Study of the Formation and Microstructure of Porous Silicon," *J. Crystal Growth*, **73**, 622 (1985).

[6] M. J. Kelly, R. R. Guilinger, V. E. Granstaff, D. W. Peterson, J. N. Sweet, and M. R. Tuck in *Proceedings of the Symposium on Electrochemical Microfabrication*, 180th Meeting of Electrochemical Society, edited by M. Datta, K. Sheppard, and D. Snyder, Phoenix, AZ, (1991).

dots of this thickness are well known to be transparent to vapor phase moisture. Fig. 2 shows the results of this experiment. Lateral diffusion is clearly evident in the case of the Al dot capacitor, although the final concentration within the dielectric volume is less than for the case of the Au dot, as indicated by the difference in final response. This would suggest a radial concentration gradient underneath the Al dot at equilibrium. The curious difference in ingress vs. egress diffusion times for the Al dot capacitor is always observed in these lateral diffusion experiments with porous Si and remains unexplained at this time.

A second experiment was carried out to further demonstrate the responsiveness of lightly doped porous Si to a pinhole moisture source. In this experiment a number of Al dot sensors were passivated with a 7 KÅ SiN moisture barrier coating. A small nick in the passivation at the center of each dot provided a bonding site for an Al bondwire. Fig. 3 shows typical capacitive response of one sensor to a drop of water before and after a 2 μm pinhole was formed using a YAG laser. In the latter case, the moisture front underneath the SiN layer could be seen with the naked eye progressing outward in a spherical front from the pinhole even after the original drop had evaporated (~ 3 minutes). When the moisture front reached the edge of the Al dot (also ~ 3 minutes), the capacitance was observed to increase exponentially, as seen in Fig. 3.

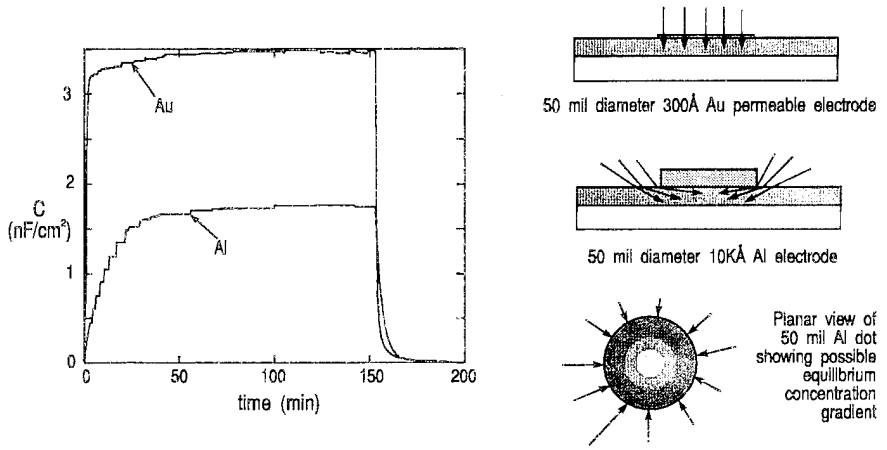


Fig. 2. Lateral diffusion experiment using 0.050 inch diameter Al and Au dot capacitors made from 0.1-0.3 Ω-cm *p*-type porous Si. Probable diffusion paths for moisture are shown at right. Graph on left shows capacitive response of two sensors to a step change in moisture concentration from 300 to 6000 ppm_v.

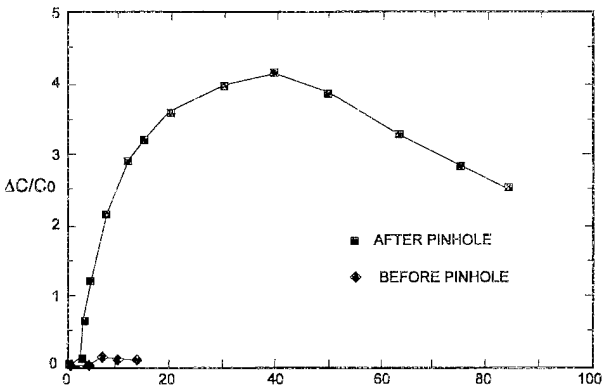


Fig. 3. Capacitive response to a point moisture source of 0.050 inch diameter Al dot capacitor moisture sensor made from 8-16 Ω-cm *p*-type porous Si. The sensor was capped with a 7 KÅ SiN moisture barrier coating and exposed to a drop of water before and after a ~ 2 μm pinhole was formed with a laser ~ 0.050 inch from the edge of the Al dot.

Process optimization: Successful demonstration of lateral diffusion and pinhole detection in lightly doped porous Si films led to the design and fabrication of a simple Al grid test chip to be used in process development. The test chip, shown in Fig. 4, contains four Al grid porous Si capacitors of varying surface area, with 5μm lines

and spaces. The chip was used to optimize the interlevel dielectic and passivation etch steps over porous Si. After some trial and error, it was determined that a 1200 Å film of PETEOS (Plasma Enhanced Tetraethylorthosilicate – a low temperature decomposition resulting in SiO_2) could be used to protect the porous Si layer during subsequent processing steps and would as an etch stop during the final passivation plasma etch. The film also corrected a problem with delamination of Al conductors during DI (deionized) water rinse cycles by forming an adhesive bonding layer between the porous Si and the Al. One issue remained: Minimum line widths that would still adhere to the PETEOS over porous Si film. A small lot of ATC01 test chips was fabricated using lightly doped *p*-type substrates which were completely anodized and coated with PETEOS prior to processing. The ATC01 contains Al triple track structures with line widths ranging from 1.25 μm to 6 μm. At the end of processing, the SiN passivation and the PETEOS protecting the porous Si was removed using the etch process previously developed. All of the triple tracks maintained adhesion, however many of the 1.25 μm triple tracks were discontinuous, having gaps apparently caused by the etch process. All of the 2 μm and greater tracks were electrically and mechanically good.

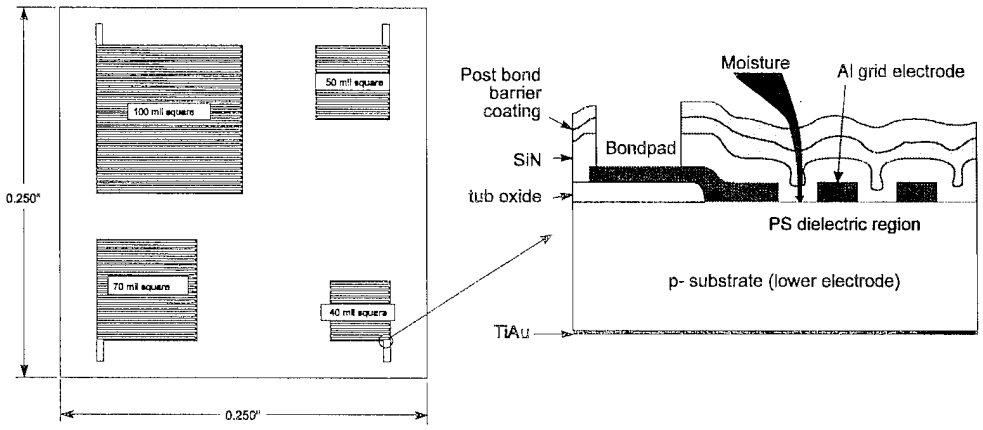


Fig. 4. Porous Si technology demonstration test chip. This chip was used in a number of experiments to demonstrate pinhole or defect detection using an Al gridded device fully compatible with standard CMOS processing.

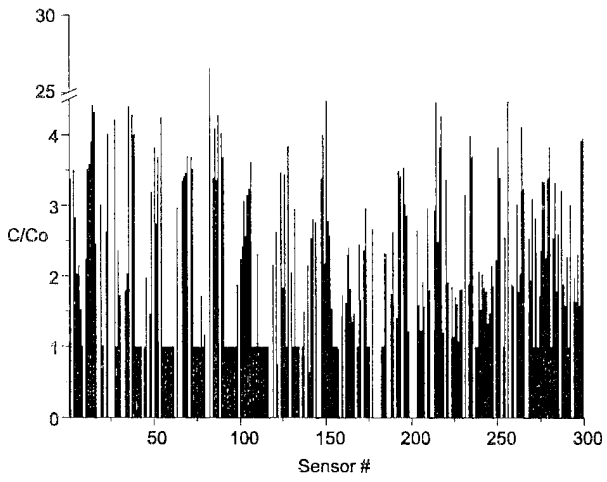


Fig. 5. Wafer level pinhole detection experiment using the test chip shown in Fig. 4 coated with 7 KÅ of PECVD Si_3N_4 at the wafer level. Capacitance readings of the 0.100 inch square sensors were taken before (C_0) and after (C) a 12 hour soak in deionized water. The total surface area represented by the 300 sensors is 3.20/28.27 in^2, or ~ 11%. Measurements greater than 1 indicate leakers.

Besides process optimization, the Al grid test chip was used to demonstrate pinhole detection in a second round of experiments. Wafers were passivated with a number of inorganic barrier coatings including 7 KÅ of Si_3N_4

(NH_3 - based SiN typically used for chip passivation). The results of a wafer level diffusion experiment are shown in Fig. 5, where all 300 of the 0.100 inch square porous Si sensors on a SiN passivated wafer were measured with an LCR meter before and after a 12 hour soak in DI water. The graph shows the ratio of $C_{final}/C_{initial}$ as a function of sensor location. A ratio of 1 signifies a "non-leaker" and ratios of greater than 1 represent "leakers" with the magnitude of the ratio functionally dependent on the diffusion rate and therefore related to the defect cross-section. The sensors are sealed during the SiN deposition process in a vacuum devoid of moisture, so the capacitance measurements of the non-leakers represent a "dry" capacitance. Leakers respond not only to the highly concentrated moisture source presented during DI water immersion, but also to the partial pressure of water vapor in the room ambient, ~ 35% RH in our facility. In other words, a leaker will eventually reveal itself during storage in ambient conditions. The wafer in Fig. 5 was remeasured periodically and the non-leakers remained unchanged after 3 months of storage in the room ambient. The leakers were still evident, but with different magnitudes reflecting equilibration to a reduced moisture source.

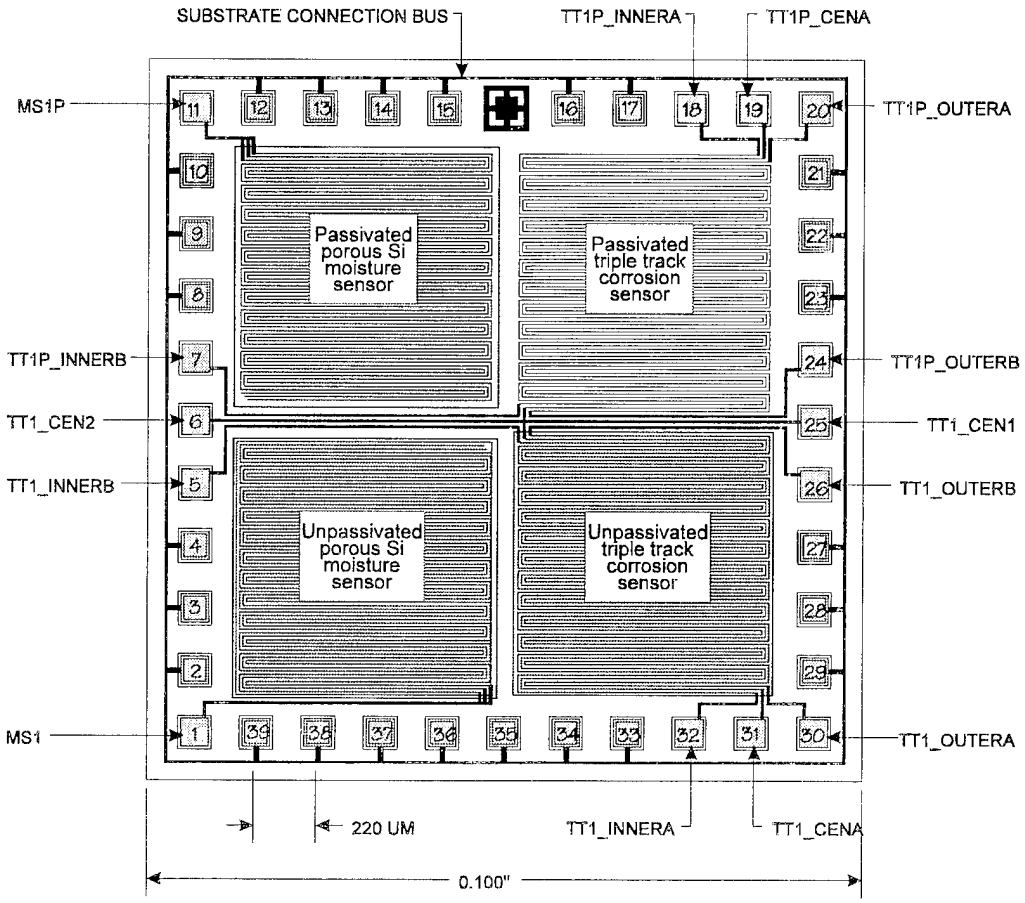


Fig. 6. Layout for the NAT-01 moisture and corrosion test chip. Al triple tracks are 2 μm lines and spaces and each of the four sensing regions are ~ 915 μm square.

Test chip layout: Based on the previous experimental work, a 2 μm minimum feature size was chosen for the Al grid electrode covering the porous Si sensors. The corrosion triple tracks were laid out using the same design rules. The layout maximizes the surface area of four sensing regions within the space available after allowing for a perimeter string of 120 μm bondpads on a 0.100 inch design area. Two of the sensors are Al triple track corrosion structures, one passivated with standard SiN and the other unpassivated. The other two sensors have the same layout except that the triple tracks are tied together at the end to form the upper electrode of a porous Si capacitor. Bondpads not used for signal I/O are used as ohmic contacts to the substrate which serves as the lower electrode of the moisture sensor capacitors. The layout is shown in Fig. 6, and bondpad position data is contained in Table I.

TABLE I. NAT-01 bondpad position data.

Signal	*x*-position (μm)	*y*-position (μm)	Pad Nr.	Signal	*x*-position (μm)	*y*-position (μm)	Pad Nr.
MS1	-1100	-1100	1	TT1P_CENA	880	1100	19
SUB1	-1100	-880	2	TT1P_OUTERA	1100	1100	20
TT1_INNERB	-1100	-220	5	TT1P_OUTERB	1100	220	24
TT_CEN2	-1100	0	6	TT_CEN1	1100	0	25
TT1P_INNERB	-1100	220	7	TT1_OUTERB	1100	-220	26
SUB2	-1100	880	10	TT1_OUTERA	1100	-1100	30
MS1P	-1100	1100	11	TT1_CENA	880	-1100	31
TT1P_INNERA	660	1100	18	TT1_INNERA	660	-1100	32

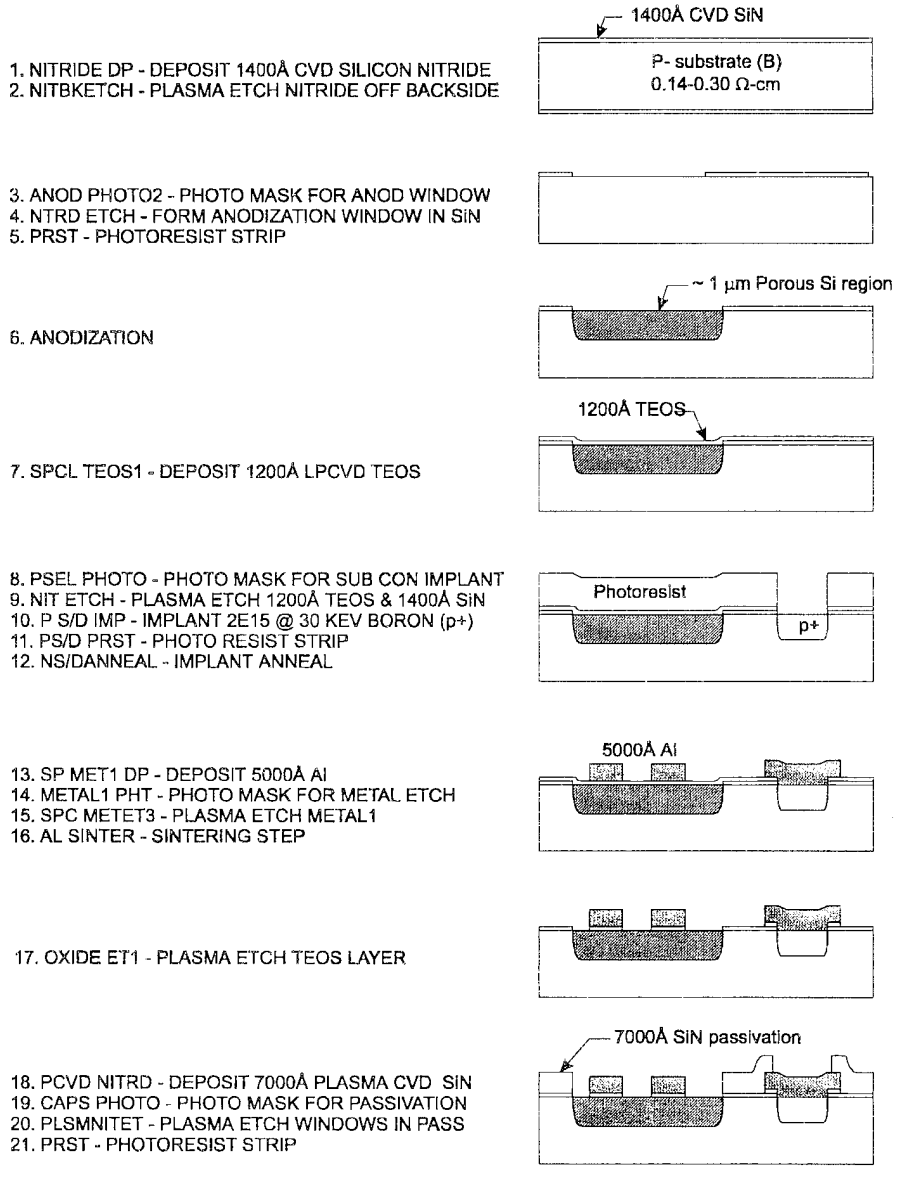


Fig. 7. Processing flow for NAT-01 test chip.

Process Steps: The fabrication flow of NAT-01 is shown in Fig. 7. Starting material is 0.14–0.30 Ω-cm *p*-type [100] Si wafers. A 1400Å SiN layer is deposited and patterned photolithographically to form the anodization mask. SiN has a relatively slow etch rate in the HF anodization bath. The anodization process is carried out in a two-sided electrochemical cell, as described earlier. After anodization, the porous Si layer is protected during subsequent processing with a 1200Å oxide layer (LPCVD TEOS), which also acts to prevent backetching and delamination of the Al metal grid during later processing. Next, the *p*+ substrate contacts are implanted and annealed. Al is deposited and plasma etched. The TEOS layer protecting the porous Si acts as an etch stop during this step. The remaining TEOS between the Al grid lines is removed next. The final step is deposition and etch of 7000Å PCVD SiN for passivation.

TASK 4.2 – DEVELOP TEST PROCEDURES

This section describes possible methods for characterizing IC moisture barrier coatings and epoxy molding compounds or liquid encapsulants using the NAT-01 test chip. These are general guidelines that can be tailored to specific situations by the user.

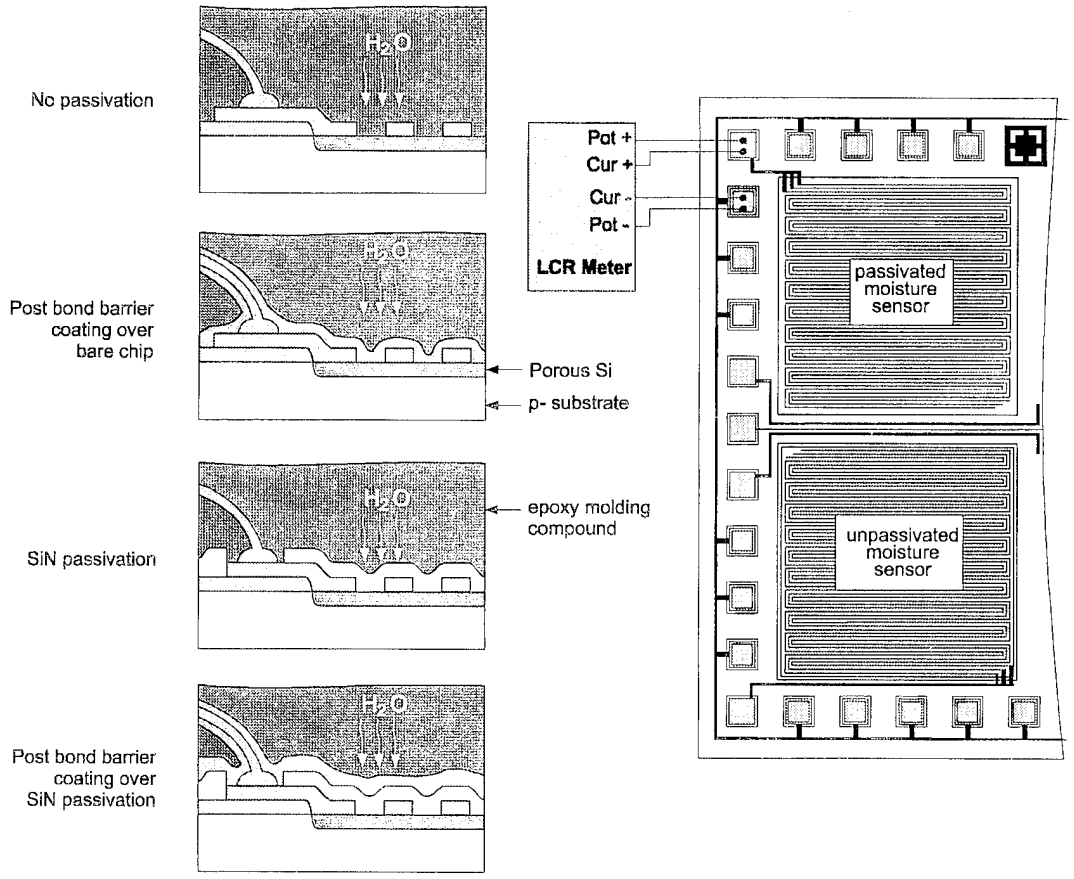


Fig. 8. Test set-up and possible experimental conditions for the NAT-01 porous Si MS.

Moisture Sensor Procedures: The moisture sensor (MS) is used to detect changes in the concentration of vapor phase moisture at the chip surface. This is done by measuring the change of capacitance across the moisture sensitive porous Si dielectric before and after exposure to a moisture source using a common LCR or capacitance meter. Typical "dry" capacitance readings for either NAT-01 MS are ~ 25 pF at 1 kHz using a 1 V source. Readings are often normalized to facilitate comparison by calculating fractional changes in capacitance, $(C-C_0)/C_0$. The passivated MS should not exhibit measurable changes in capacitance at room temperature from the initial post-fabrication readings as long as the SiN film remains intact. Since the passivated MS is protected during and after

the fabrication process from exposure to organic contaminates that can affect the hydrophilicity of the pore walls, its intrinsic sensitivity is significantly greater than the unpassivated MS. Experimental measurements discussed later in this document show order of magnitude differences in sensitivity.

Fig. 8 illustrates four possible experimental conditions for use of the two moisture sensors. The first case is for the unpassivated MS. Here, the permeability of the epoxy molding compound (or liquid encapsulant) to vapor phase moisture is estimated by measuring the change in capacitance as a function of time during exposure of a previously dried out part to a known moisture concentration at a controlled temperature. Changes in weight corrected for non-absorptive package components (lead frames, die) are also recorded. This process is carried out until both measurements indicate the package has reached equilibrium conditions with the external moisture source. Using the gravimetric data, a diffusion coefficient can be obtained from the linear part of a plot of mass uptake, M_t, against root time using Eq. (1)[7].

$$\frac{M_t}{M_\infty} = \frac{4}{l}\left(\frac{Dt}{\pi}\right)^{1/2} \tag{1}$$

Solving Eq.(1) for the diffusion constant in terms of the slope, the diffusion coefficient is calculated by,

$$D = \pi\left(\frac{kl}{4M_\infty}\right)^2 \tag{2}$$

where k is the slope of the linear portion of the plot of M_t vs. $t^{1/2}$.

It should be noted that Eqs. (1) and (2) assume Case I or "Fickian" diffusion in the polymer. Fickian diffusion is characterized by sorption and desorption curves as functions of the square root of time that are linear in the initial stage. This is generally the case with epoxy molding compounds, but estimates of the diffusion coefficient based on experimental weight gain measurements assume one-dimensional penetration along two surfaces, and thus are done on thin strips of material. A molded part will have edge effects that can possibly skew the M_t vs. $t^{1/2}$ curve to the extent that it is not linear in the initial stage.

The fractional change in capacitance of the unpassivated MS will reflect the moisture flux at the chip surface during the diffusion process. In order to make quantitative measurements of surface flux, it would be necessary to calibrate the packaged sensors at various known moisture concentrations. The capacitance response would be recorded after the readings ceased to change, indicating equilibrium between the inside and outside of the package.

The second experimental condition is the unpassivated MS coated with a postbond moisture barrier coating as shown in Fig. 8. These coatings are normally applied in a vacuum using a plasma CVD or sputtering process, and therefore a sensor protected with a defect free coating would be expected to exhibit "dry" capacitance readings of ~ 25 pF at all times. If there is variation from this measurement, particularly as a function of time, it could be concluded that a defect exists in the coating. The rate of change in capacitance of an unpackaged sensor during exposure to a step change in ambient moisture concentration is functionally related in to defect characteristics, such as cross-section, crack vs. pinhole, etc. Assuming that "non-leakers" were packaged with epoxy molding compound or liquid encapsulant, subsequent changes in capacitance from the baseline would indicate packaging-related damage to the postbond barrier coating. Exposure of packaged parts to extremely high moisture concentrations in a HAST or pressure cooker system would accelerate the detection of small defects with low effective diffusion rates.

The third and forth experimental conditions illustrated in Fig. 9 involve the passivated MS with and without a postbond barrier coating. The former is a measure of the protective properties of the SiN passivation film applied during fabrication of the sensor, and the latter reflects the combined protection offered by both coatings. HAST or pressure cooker tests would aid in rapid isolation of leakers.

Corrosion Detector Procedures: The Corrosion Detector (CD) triple track structures are used to characterize the susceptibility of a molded or liquid encapsulated part to electrochemical corrosion in the presence of moisture and ionic contaminants that originate in the molding compound or molding process. An electric field present between alternate tracks will sweep these ionics toward an anodic or cathodic Al electrode and initiate an electrochemical corrosion process in the presence of moisture. A failure is considered to be an electrically open

[7] M. T. Goosey, "Permeability of Coatings and Encapsulants for Electronic and Optoelectronic Devices," in *Polymer Permeability*, edited by J. Comyn, Elsevier Applied Science Publishers, New York, (1985).

track. Track resistance measurements are normally made "off-line" and the parts are then reintroduced into the testing environment. Testing proceeds until sufficient failures are observed so that an estimate can be made of the failure distribution function, at a minimum t_{50}, or time until 50% of the population fails. Failure statistics for molded parts generally follow an Eyring relationship.[8] One Eyring model often cited is the Peck relationship,[9]

$$\tau = A(RH)^{-n} \exp\left[\frac{E}{kT}\right], \tag{3}$$

where n=2.7 and E=0.79 eV are estimates based on an extensive literature survey of product failures during accelerated temperature and humidity testing. One criticism of this model is its lack of a voltage acceleration factor. Data are commonly plotted on lognormal charts to aid in visual identification of failure regimes. A failure distribution reflecting a single failure mechanism will appear as a straight line on a lognormal chart.

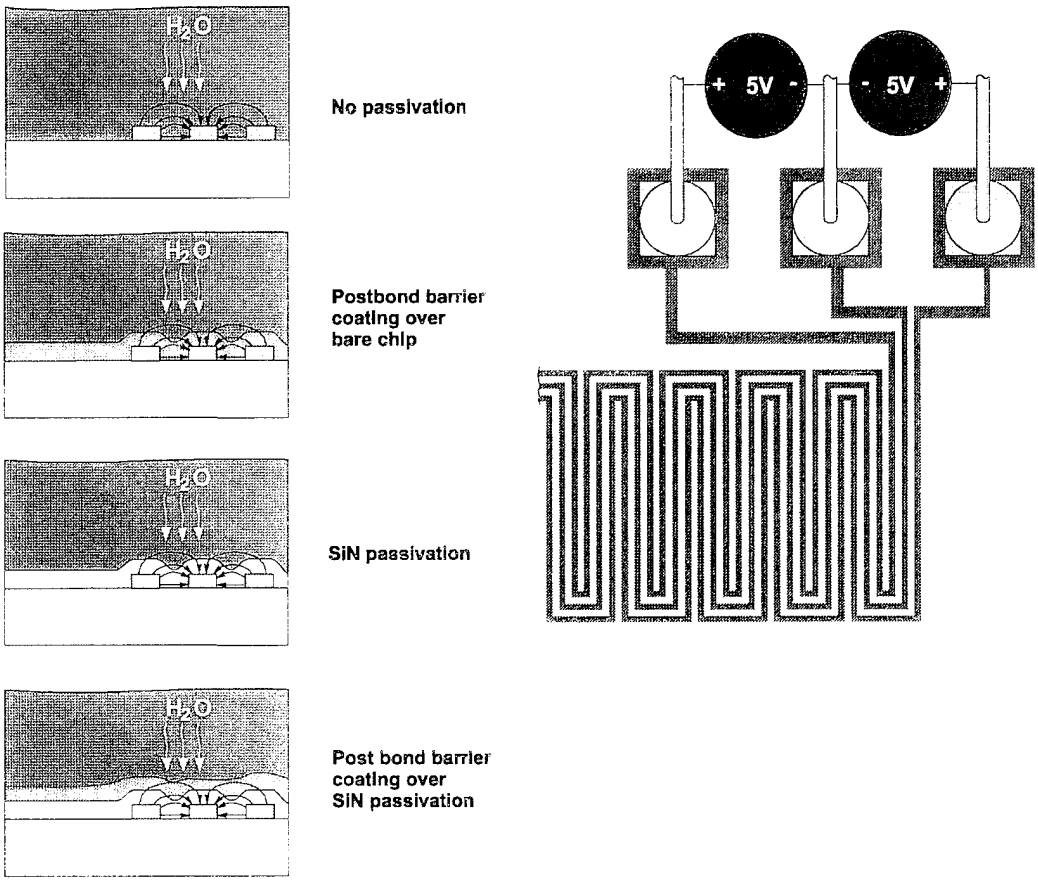


Fig. 9. Test set-up and possible experimental conditions for the NAT-01 CD.

Fig. 9 illustrates four possible experimental conditions in which the passivated and unpassivated CD can be used during accelerated stress testing. The unpassivated CD is very sensitive to the presence of ionic contaminates and will corrode quickly under biased temperature and humidity testing. The unpassivated CD protected with a postbond moisture barrier coating would measure the protective properties of the coating during accelerated testing. The passivated CD, both with and without postbond coating, would also test moisture barrier properties. Electrochemical corrosion of the biased tracks can only occur where there is a breach in the barrier coating. In

[8] W. Nelson in *Accelerated Testing - Statistical Models, Test Plans, and Data Analyses*, John Wiley, New York, (1990).

[9] D. S. Peck, "Comprehensive Model for Humidity Testing Correlation," *Proceedings of the International Reliability Physics Symposium*, **24**, 44-50 (1986).

practice, reasonably good SiN passivation coatings will protect the high field region of biased triple tracks beyond the point at which other failure mechanisms appear, for instance, corrosion of the Au/Al bondwire to bondpad interface. It is important to perform failure analysis in these cases so that the actual failure mode can be identified.

Fig. 10 contains a functional diagram of the NAT-01 test chip showing typical measurement equipment connection for electrical testing. The chip bondpads only are shown for simplicity, but a package part would include a die-to-device pin diagram.

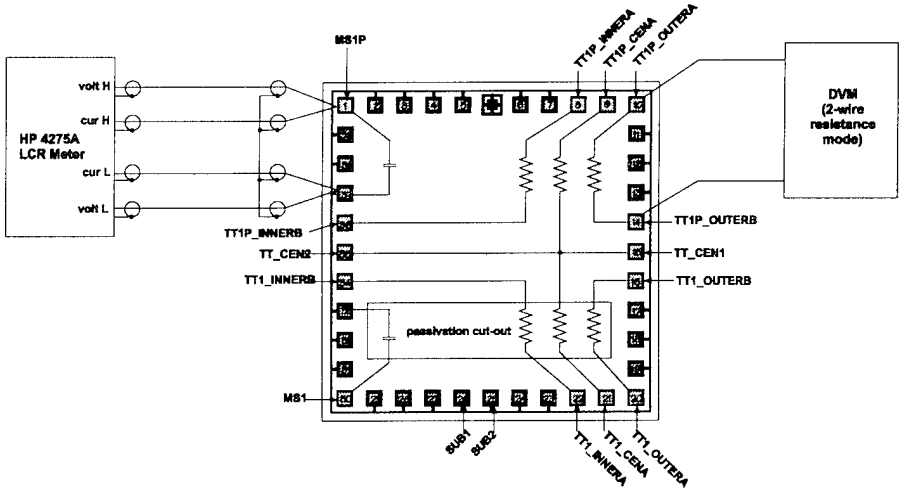


Fig. 10. Typical electrical measurement set-up for NAT-01. Capacitance measurements should be ~25 pF for the (non-leaking) passivated MS and >25 pF for the unpassivated MS. The CD triple tracks should read ~ 2200Ω.

TASK 4.3.1 – MOISTURE SENSOR (MS) CHARACTERIZATION

All MS calibrations were done with a locally fabricated precision humidity generator. This source is capable of producing a 1 liter per minute constant flow of N_2 carrier gas containing moisture concentrations from < 50 ppm_v to >10,000 ppm_v at room temperature. The gas is passed over the devices under test that are contained within a test fixture and then enters the measurement head of an optical dewpoint hygrometer. A functional layout of the humidity generator is shown in Fig. 11. A data acquisition system was developed for controlling settings of the mass flow controllers, making capacitance measurements on the devices under test, and interrogating the optical dewpoint hygrometer.

High Temperature Performance: A series of experiments were performed to characterize the sensitivity of the NAT-01 MS to elevated temperature cycles in various ambients. The original requirement for this capability was the need for the MS to survive application of the Dow Corning postbond moisture barrier coating, which originally had a cure schedule that reached 275°C. Since it was not clear exactly what gaseous environment the MS would see during this process, the high temperature characterization encompassed air, N_2, and vacuum. Results from these tests are shown in the following Figs. 12-14.

Results show that the unpassivated MS sensitivity to moisture decayed approximately 35% for air, 30% for N_2, and 28% for vacuum ambients, respectively, after temperature exposure and ambient storage. This is clearly a concern for applications in which the absolute sensitivity must be invariant after temperature excursions, but for pinhole or defect detection in moisture barrier coatings, it is probably not an issue. The experiment does demonstrate that the MS can survive high temperature exposures for extended periods of time without losing functionality.

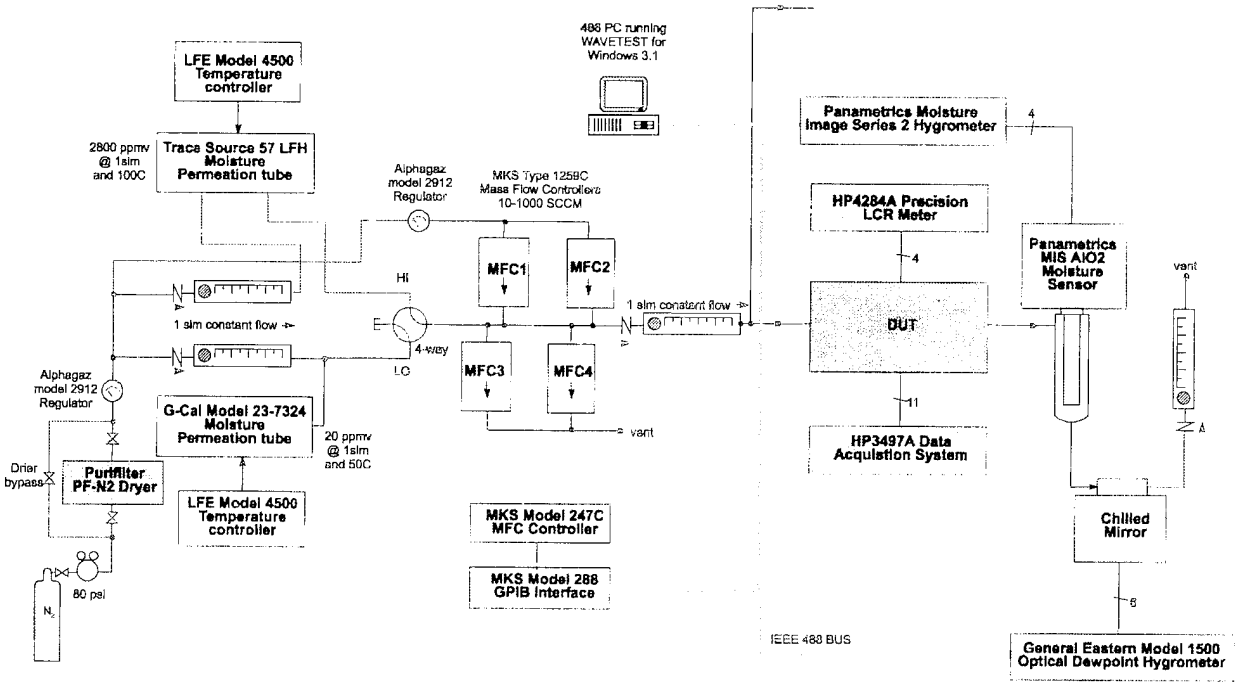


Fig. 11. Precision humidity generator functional layout

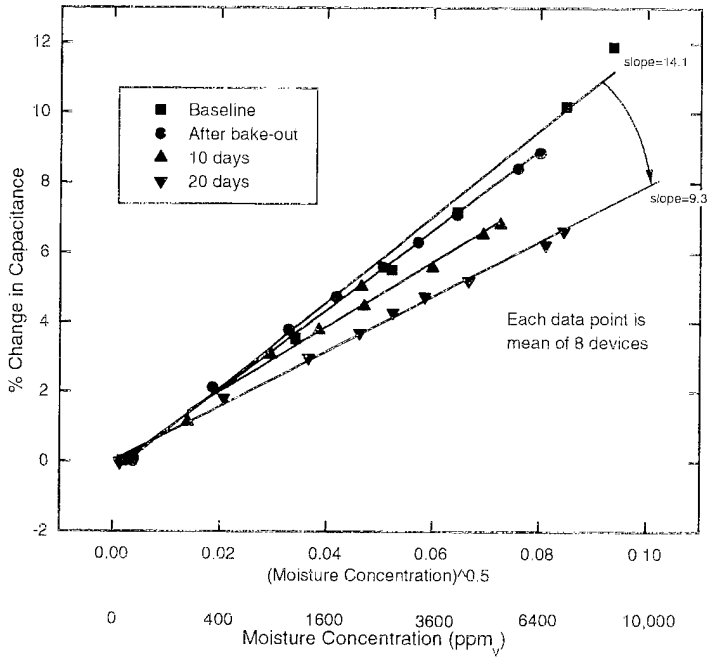


Fig. 12. NAT-01 MS calibration measurements after exposure to air at 300°C for 4 hours. Measurements were made immediately after exposure, and then after 10 and 20 days, respectively, of ambient storage. Plot is in % change of capacitance vs. square root of moisture concentration. Lower legend is in ppm$_v$ for reference.

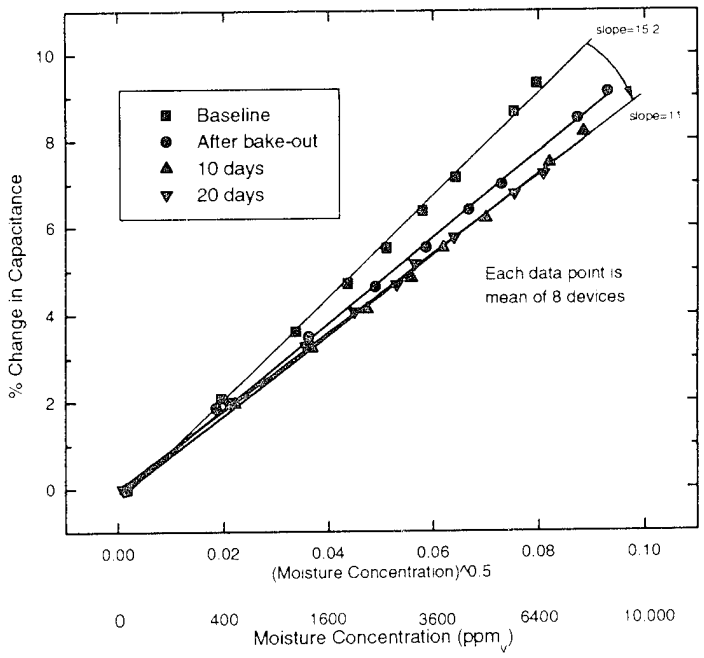


Fig. 13. NAT-01 MS calibration measurements after exposure to vacuum at 300°C for 4 hours. Measurements were made immediately after exposure, and then after 10 and 20 days, respectively, of ambient storage. Plot is in % change of capacitance vs. square root of moisture concentration. Lower legend is in ppm$_v$ for reference.

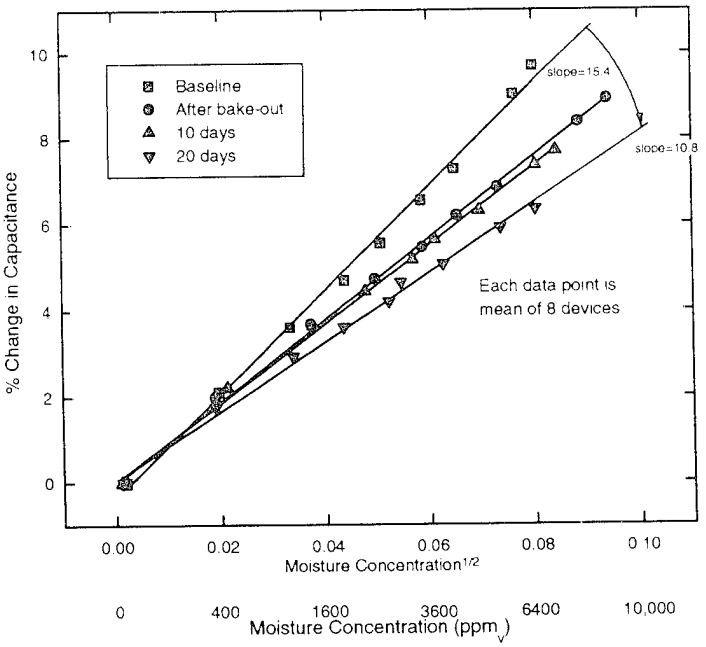


Fig. 14. NAT-01 MS calibration measurements after exposure to N_2 at 300°C for 4 hours. Measurements were made immediately after exposure, and then after 10 and 20 days, respectively, of ambient storage. Plot is in % change of capacitance vs. square root of moisture concentration. Lower legend is in ppm$_v$ for reference.

Moisture Diffusion Experiments: The purpose of this work was to d monstrate the use of the passivated and unpassivated MS during conditions of package dry-out and moisture ingress. The dry-out condition was 100°C at

10^{-4} Torr. The moisture ingress experiments were initially performed using a Thunder Scientific Humidity Generator at 50°C and 85% RH, which is a moisture concentration of approximately 118,000 ppm_v. Later, diffusion experiments were carried out in parallel with ongoing HAST experiments on the CD at 159°C and 85% RH.

Fig. 15 shows some results from a diffusion experiment using a vacuum oven for dry-out and the Thunder Scientific unit for wet-up. These data are for a group of NAT-01 test chips molded in 14-lead DIPs using Plaskon 3400-2 (preconditioned) epoxy molding compound, and are representative of data from the other material splits in the overall experiment. The unpassivated MS data track the ambient moisture concentration, and the passivated MS data split into two apparent groups. One group roughly tracks the external humidity, suggesting defects or pinholes in the passivation, while the other group is essentially straight line with a gradual trend toward increasing readings. The latter could be due to increases in fringe field capacitance due to moisture build-up on the molding compound side of the passivation.

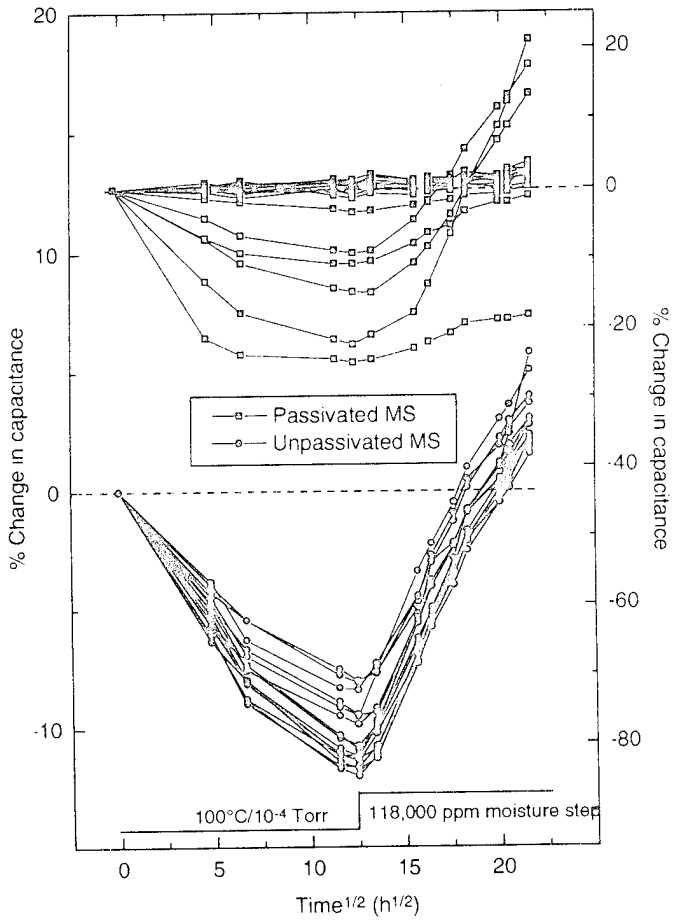


Fig. 15. NAT-01 MS response as a function of time during dry/wet cycle using a Thunder Scientific moisture source. Passivated sensors (▣) show two trends: "leakers" that appear to follow the swing in ambient moisture concentration, and "non-leakers" that are relatively unresponsive. Unpassivated sensors (○) track the swing in ambient moisture concentration.

A second moisture ingress experiment was run in conjunction with HAST testing of the CD. In this experiment, NAT-01 test chips molded in 68-lead PLCCs using Plaskon ULS12H and ULS12H-X ultra-low stress molding compounds (-X material containing ionic scavengers). A control group of hermetically sealed ceramic parts were also present. The unpassivated MSs were measured before and at predetermined off-line intervals during HAST at 159°C and 85% RH. These data are shown in Fig. 16 plotted as fractional changes in capacitance vs. time.

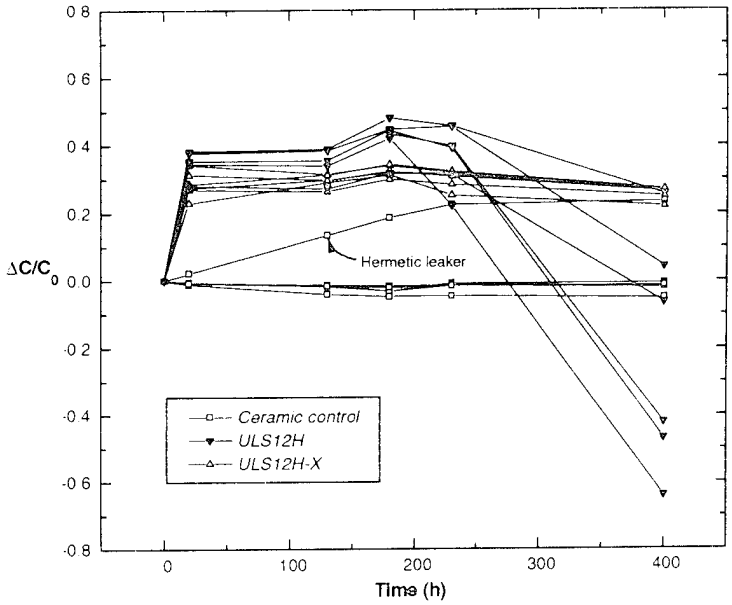


Fig. 16. NAT-01 *unpassivated* MS response during HAST at 159°C and 85% RH. Two groups were molded in 68-lead PLCCs using Plaskon ultra-low stress compounds ULS12H (▼) and ULS12H-X (△), and a ceramic control group (□). Plot is fractional change in capacitance as a function of time. One "leaker" is evident in the control group. The drop-off in response of some of the molded parts is due to corrosion of the Al electrode.

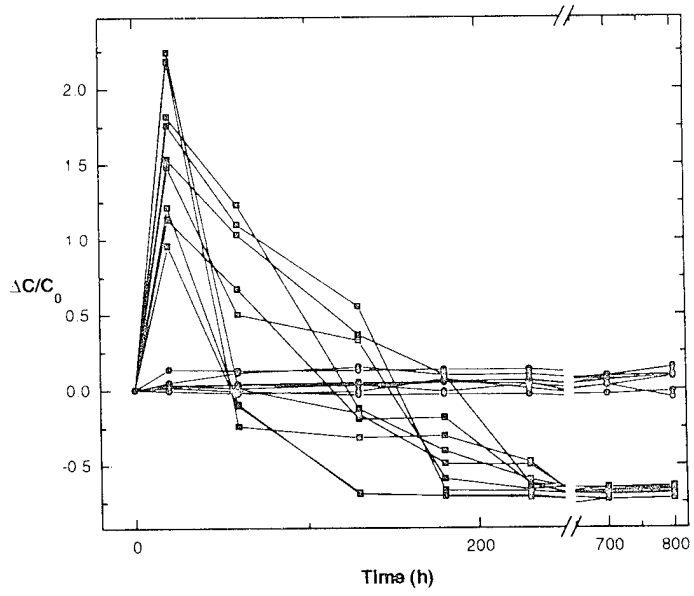


Fig. 17. NAT-01 *passivated* MS response during HAST at 159°C and 85% RH. Devices were molded in 14-lead DIPs using different Plaskon molding compounds. Plot is fractional change in capacitance as a function of time. Data are grouped by devices showing leaks (▣) and devices showing no leaks (●) irrespective of molding compound. First measurement is at 20 hours. (Note break in time axis.)

The first off-line measurement interval was at 20 hours, and it can be seen that the unpassivated MS responses indicate equilibrium moisture concentration at the chip surface at this point in time. The ceramic control parts were non-responsive with the exception of one leaker. At approximately 200 hours, the response of some of the devices dropped off toward negative fractional changes. Failure analysis results showed that the Al electrodes in these devices had decomposed due to corrosion resulting in open circuit capacitance readings of 7 – 15 pF. Of particular interest is the fact that corrosion of Al grids occurred only with ULS12H parts. The low ionics group (ULS12H-X) appeared unaffected during the course of the experiment, suggesting lower susceptibility to electrochemical corrosion. HAST failure data described in the next section, also discriminated between materials with and without ionic scavengers.

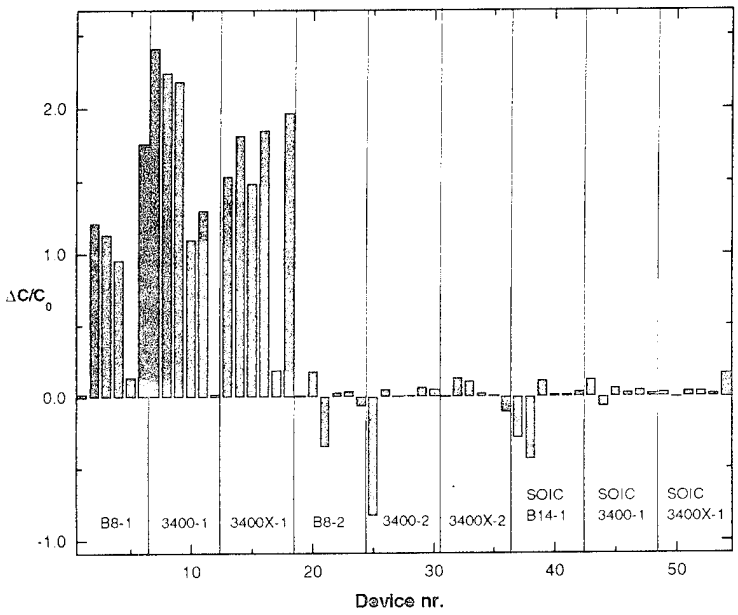


Fig. 18. NAT-01 MS response of *passivated* MSs at first (20 hour) off-line measurement point during HAST at 159°C and 85% RH. Each bar represents fractional change in capacitance of an individual part molded in 14-lead DIPS, unless specified as SOIC, using the Plaskon molding compound shown at the bottom. The parts are further divided into "not preconditioned" (-1), and "preconditioned" (-2).

Moisture Penetration Though Passivation Experiments: The capacitive responses of the passivated MS in HAST fall into two groups: non-leakers with essentially straight line response, and leakers with very high readings at the first off-line measurement interval followed by a drop off to open circuit readings at 100-200 hours. (Refer to Fig. 17) As with the Thunder Scientific experiment, failure analysis indicated the drop off was associated with corrosion of the Al grid. HAST conditions were 159°C and 85% RH.

Fig. 18 shows the passivated MS response across all of the molding compounds at the first measurement interval (20 hours). Groups annotated with a -2 were preconditioned by National Semiconductor prior to shipping to Sandia for further testing. The National Semiconductor preconditioning procedure consists of 30 temperature cycles -65 to +150°C, bake at 125°C for 16 hours, moisture soak at 85°C/30% RH for 168 hours, 3 IR reflow cycles at 230–250°C, followed by flux immersion and activation. In this plot, small bars mean passivation layer with little or no moisture leak rate. Negative responses could possibly be due to Al grid corrosion, suggesting leaks through the passivation layer. The preconditioned group underwent thermal cycles and thermal shock that could potentially damage the passivation layer, and it would be logical to assume that they would exhibit more leaks of greater defect size than the non-preconditioned parts. However, the data in Fig. 18 show the opposite trend, a result that is unexplained at this time.

TASK 4.3.2 – CORROSION DETECTOR (CD) CHARACTERIZATION

Characterization of the CD was done using a HAST-1000 system from Express Test operated at 159°C/85% RH and 5 VDC bias. There were two objectives to this work. First, to demonstrate the operation and utility of the passivated and unpassivated triple track corrosion structures under experimental conditions. Second, to accumulate experimental data on molded test chips that could be compared to HAST data from Crane and Dow Corning on similar parts that were being tested in parallel. As typical failure rates were not known at the onset, relatively short off-line measurement intervals were used to insure that early failures were trapped. The measurement interval started at 20 hours and increased in steps to 100 hours where it remained until the end of the experiment.

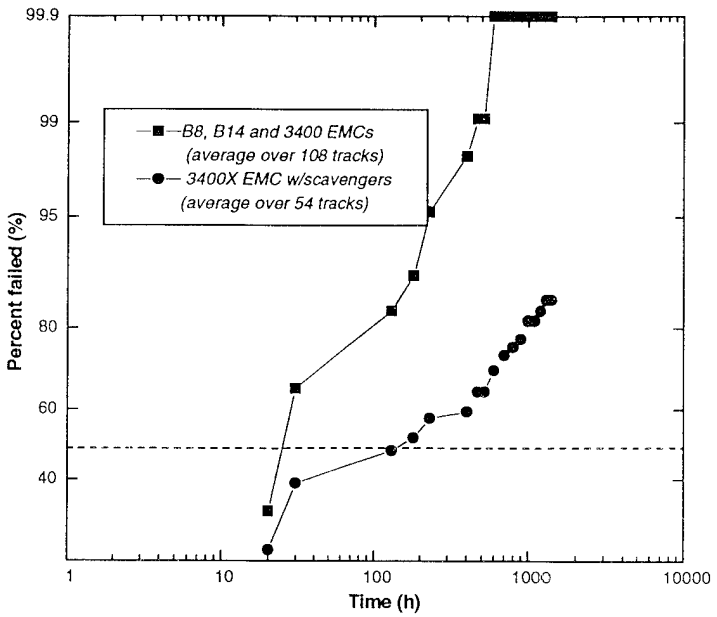


Fig. 19. NAT-01 *unpassivated* CD triple track failure distribution during HAST at 159°C/85% RH and 5 VDC bias on 14-lead DIPs and SOICs molded in Plaskon molding compounds. Plot is log-normal showing failures observed during off-line measurement intervals in a normal probability distribution as a function of log time. Failure data for parts molded in B8, B14 and 3400 compounds without scavengers are grouped and shown as filled squares (■), and data for parts molded in 3400X with scavengers are shown as filled circles (●). The 3400X parts have a t_{50} of 5-10X greater than the parts without scavengers.

The *unpassivated* CD was expected to be very sensitive to the state of ionic contamination at the chip surface and within the molding compound. Biased HAST was performed on 14-lead DIPs and SOICs that were molded in 4 different Plaskon molding compounds, 6 parts to a material. One of the compounds, 3400X, had a special ionic scavenger present to reduce ionic contamination. Fig. 19 shows data from this experiment, grouped by -X and non-X compounds to see the effect of ionic scavengers. As can be seen in the chart, the t_{50} (time at which 50% of the parts in a distribution have failed) increased roughly 5–10X for parts molded with the -X compound. Failure analysis showed that electrical failures were due to corrosion of the Al triple tracks in the high electric field region. It should be noted that the data in Fig. 19 are averaged over all triple tracks, both anodic and cathodic.

NAT-01 parts from the same groups were forwarded to both Dow Corning and Naval Surface Warfare Center Crane for parallel testing using the same 159°C and 85% RH HAST conditions. Cumulative failure data for the unpassivated CDs are shown in Table II. Although the data do not fit the distribution suggested by Fig. 19, there is a similar trend evident in the Dow Corning -X parts in terms of reduced failure rate. These data illustrate the difficulty in making generalizations based on failures out of very small populations sampled at wide intervals. A more statistically valid approach shedding more light on failure mechanisms would involve more parts per molding compound sampled at shorter intervals and would separately analyze anodic and cathodic failure data. A SEM micrograph of a typical unpassivated triple track failure for a decapsulated part tested at Crane is shown in Fig. 20.

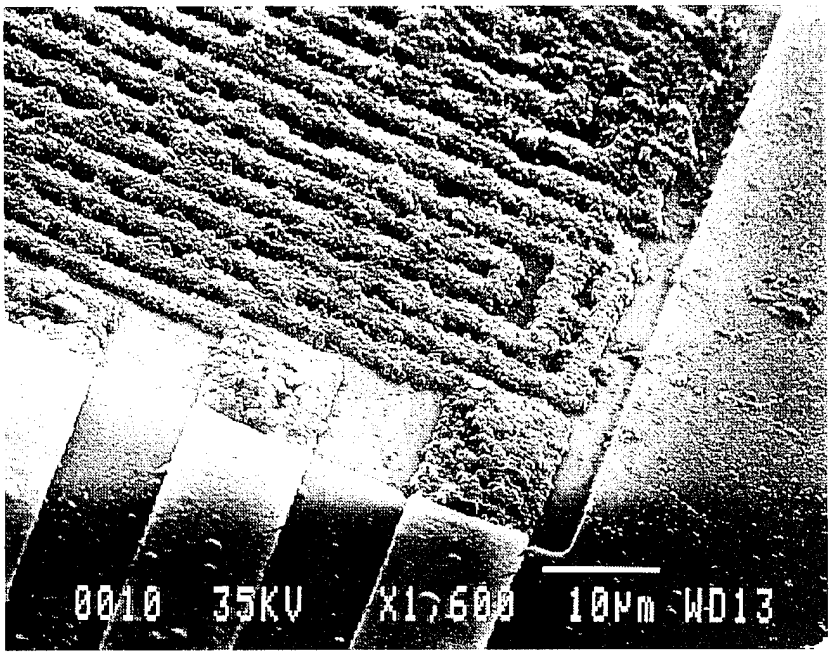


Fig. 20. SEM micrograph of decapsulated NAT-01 *unpassivated* CD that failed during HAST at 159°C/85% RH with 5 VDC bias between tracks. This part was molded in a 14-lead DIP using Plaskon 3400 molding compound.

TABLE II. NAT-01 *unpassivated* CD cumulative failure data from Dow Corning (DC) and Crane during HAST at 159°C/85% RH and 5 VDC bias. Data are shown as number failed out of total population. Blanks are where no data were taken. The Crane data for DIPs includes both preconditioned and non-preconditioned sub-groups.

EMC	Site/Package	24h	72h	108h	216h	312h	432h	648h
B24	DC/68L PLCC	7/9	9/9	9/9	9/9		9/9	9/9
X9074.07	DC/68L PLCC	9/9	9/9	9/9	9/9		9/9	9/9
ULS12H	DC/68L PLCC	9/9	9/9	9/9	9/9		9/9	9/9
ULS12H-X	DC/68L PLCC	4/9	7/9	7/9	7/9		9/9	9/9
B8	Crane/14L DIP				17/17	17/17	17/17	
3400	Crane/14L DIP				16/16	16/16	16/16	
3400X	Crane/14L DIP				13/17	13/17	13/17	
B14	Crane/14L SOIC*				5/7	6/7	6/7	
3400	Crane/14L SOIC*				5/5	5/5	5/5	
3400X	Crane/14L SOIC*				8/8	8/8	8/8	

* The 30 VDC bias group was excluded.

It would be expected that the *passivated* CD would be less sensitive to ionic contamination originating within the molding compound and more sensitive to defects or pinholes in the SiN passivation (or other barrier coating). This is true up to the point at which bondpad corrosion develops and becomes the dominant failure mechanism, which appears to be the case for most of the passivated CD failures. Data from the same HAST experiment described above can be grouped according to preconditioned and non-preconditioned parts, showing the effect of preconditioning on failure rate. This is shown in Fig. 21 for 14-lead DIPs and SOICs, where it can be seen that the preconditioned parts show a reduction in t_{50} of ~50%. One must be careful in ascribing too much to these data, however, as the difference in standard deviations (slopes) of the two series suggest convolution with one or more other failure mechanisms. Failure analysis of these parts showed that the principle failure mechanism was a combination of Au_xAl_y intermetallic formation, associated Kirkendall voiding of interface, and some corrosion

activity due to the presence of moisture and ionic contaminates. Fig. 22 contains a SEM micrograph of a typical decapsulated NAT-01 part that exhibited an electrical failure of the passivated CD during HAST.

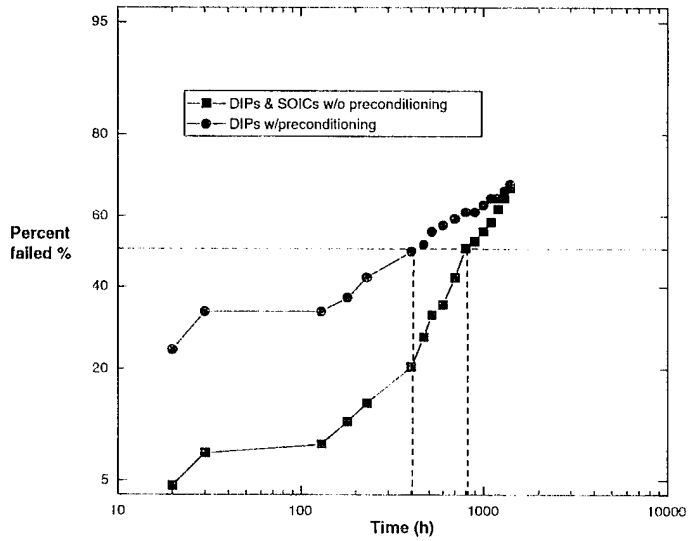


Fig. 21. NAT-01 *passivated* CD triple track failure distribution during HAST at 159°C/85% RH and 5 VDC bias on 14-lead DIPs and SOICs molded in Plaskon molding compounds. Plot is log-normal showing failures observed during off-line measurement intervals in a normal probability distribution as a function of log time. Non-preconditioned parts are shown as filled squares (■), and preconditioned parts are shown as filled circles (●). The preconditioned parts show a reduction in t_{50} of ~50%.

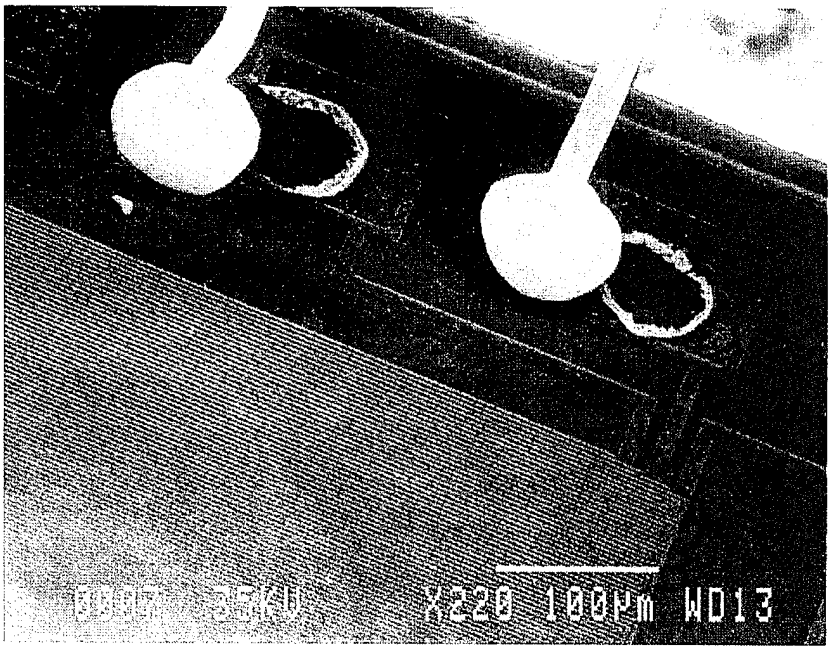


Fig. 22. Decapsulated NAT-01 test chip after 432 hours of HAST by Crane at 159°C/85% RH and 5 VDC bias, showing bondwire/bondpad voiding failure of the passivated CD. Bondwires were moved to the side for clarity. Note voiding in center of bondpads and lack of any signs of corrosion in the high field region of the triple track structure.

It has been noted in the literature that voiding in the bondpad interface of Au ballbonded Al pads can be accelerated in the presence of ionic contamination.[10] This means that triple track corrosion structures protected with reasonably good passivation coatings may not fail in the high electric field region between the tracks, as intended, but can fail elsewhere, particularly in the bondwire/bondpad region. Although the relatively weak electric field present between the bondpads of a biased triple track probably influence the onset of electrochemical corrosion in this region, it is not uncommon to observe corrosion of unbiased Au bonded Al pads and unbonded Al pads during failure analysis of molded parts taken from HAST.

Table III contains cumulative failure data for the *passivated* CDs during HAST at Dow Corning and Crane. Table IV contains additional HAST failure data from Dow Corning on NAT-01 parts run at 130°C/85% RH and 5 VDC bias. The Dow Corning data for 159°C HAST shows a clear improvement in time-to-fail for the -X group over the other materials except for the B24, which has a similar failure trend. There is no reason based on known material properties that explains why the B24 material should have better HAST performance than the other non-scavenger materials, so it is possible we are seeing normal statistical variance in a small sample size. On the other hand, the increased time-to-fail is also borne out by the 130°C HAST data from Dow Corning in Table IV. The Crane data shows essentially no difference in the materials with and without ionic scavengers.

TABLE III. NAT-01 *passivated* CD cumulative failure data from Dow Corning (DC) and Crane during HAST at 159°C/85% RH and 5 VDC bias. Data are shown as number failed out of total population. Blanks are where no data were taken. The Crane data for DIPs includes both preconditioned and non-preconditioned sub-groups.

EMC	Site/Package	24h	72h	108h	216h	312h	432h	648h
B24	DC/68L PLCC	0/8	0/8	1/8	2/8		2/8	3/8
X9074.07	DC/68L PLCC	0/9	2/9	3/9	8/9		8/9	9/9
ULS12H	DC/68L PLCC	0/9	0/9	0/9	2/9		4/9	7/9
ULS12H-X	DC/68L PLCC	1/9	1/9	1/9	1/9		2/9	2/9
B8	Crane/14L DIP				12/16	14/16	14/16	
3400	Crane/14L DIP				9/15	9/15	9/15	
3400X	Crane/14L DIP				10/17	11/17	11/17	
B14	Crane/14L SOIC*				2/8	4/8	5/8	
3400	Crane/14L SOIC*				4/9	8/9	8/9	
3400X	Crane/14L SOIC*				2/9	5/9	5/9	

* The 30 VDC bias group was excluded.

TABLE IV. NAT-01 *passivated* and *unpassivated* CD cumulative failure data from Dow Corning (DC) during HAST at 130°C/85% RH and 5 VDC bias. Data are shown as number failed out of total population.

	Passivated CD					Unpassivated CD				
EMC	216h	432h	648h	864h	1080h	216h	432h	648h	864h	1080h
B24	0/9	1/9	1/9	1/9	1/9	9/9	9/9	9/9	9/9	9/9
X9074.07	0/9	0/9	1/9	3/9	4/9	9/9	9/9	9/9	9/9	9/9
ULS12H	0/9	0/9	0/9	0/9	1/9	7/8	8/8	8/8	8/8	8/8
ULS12H-X	1/9	2/9	2/9	2/9	2/9	7/8	7/8	7/8	7/8	7/8

[10] G. G. Harman, in *Reliability and Yield Problems of Wire Bonding in Microelectronics*, International Society for Hybrid Microelectronics, (1989).

TASK 4.4 – MOISTURE TEST SPECIFICATION

At the inception of this program in 1992, it was envisioned that Sandia would develop a test specification similar to JEDEC Test Method A110 for HAST that would specify how to test quasi-hermetic packages for moisture intrusion. The term "quasi-hermetic" is intended to mean some degree of hermeticity afforded to a non-hermetic plastic encapsulated microelectronic (PEM) part by a combination of moisture barrier coatings and low diffusion, low moisture solubility epoxy molding compounds. The NAT-01 test chip was designed around this concept and, based on experimental results described in this document, it appears to perform this function. However, a moisture barrier coating technology has not evolved that can protect both the chip Al metalization and, more importantly, the Au/Al bondwire/bondpad interface from electrochemical corrosion.

On the other hand, experimental evidence continues to accumulate suggesting that a combination of a good SiN passivation coating and a low-ionics molding compound can result in long times-to-fail in the most aggressive HAST environments – environments so severe that some wonder if failure mechanisms are being generated that are not representative of real life conditions. This not to say that the Au/Al intermetallic/voiding/corrosion process observed at the bondpads in this and other work is not a general reliability concern, but it is to say that it may not be a reliability concern for many, if not most, application environments.

The NAT-01 test chip does provide a means of evaluating important physical properties of organic and inorganic materials used in plastic encapsulated microelectronic parts in a laboratory setting, and will be valuable in the development and characterization of potential wafer-level or post-bond moisture barrier coatings as well as new molding compounds with enhanced corrosion prevention. The procedures and guidelines contained in this document should be sufficient for most users to perform these experiments. But it would appear premature to suggest revisions or additions to a reliability testing specification that would prescribe detection or measurement of moisture diffusion through barrier coatings that do not yet or may never exist.

TASK 4.5 – STRESS MEASUREMENT USING ATC04

As mentioned in the Task Description section, this task was added on mid way through the program based on input from industry observers. The purpose was to measure and compare the stress properties of the molding compounds developed for the PPA program, including the new ultra-low stress formulations. A secondary objective was to monitor the changes in stress brought about by the process of preconditioning. In this section, the ATC04 test chip will be described, followed by the experimental plan, and experimental results.

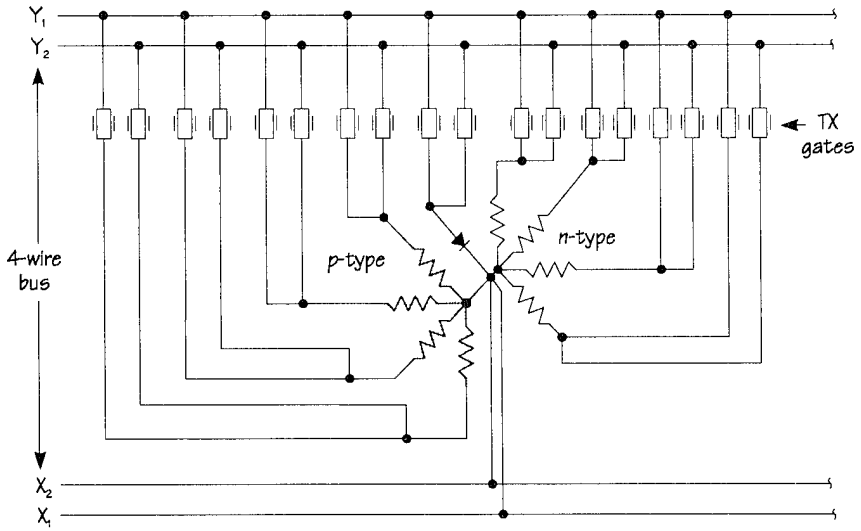


Fig. 23. Schematic of 1 of 25 piezoresistive stress sensing and temperature measurement cells. The address circuitry is not shown. A current is applied to terminals X_1 and Y_1 and the resultant voltage is measured across X_2 and Y_2.

ATC04 Test Chip: The ATC04 chip is fabricated in a 2 μm twin-tub CMOS process and operates at 5 V. The chip is square, ≈ 0.25 in. on a side, and all required bondpads are replicated on each side of the die. The test chip contains an array of 25 stress sensing cells, each approximately 200 μm on a side, with a diode thermometer in the center of each cell. A cell contains four *n*-type and four *p*-type piezoresistors for mechanical stress measurement and a diode for temperature measurement. Each cell is addressable, either by sending it a 9-bit address word or by sequentially addressing with a clock toggle. Measurements are then made using a four terminal or Kelvin technique, with two connections for a current source and two for a voltage measurement device. A single cell is shown schematically in Fig. 23.

The use of four resistors of each doping type, two parallel to the chip edges ([11$\bar{0}$], [110] directions) and two on 45° diagonals ([100], [010] directions), facilitates obtaining the maximum amount of information possible from planar stress sensors on <100> Si. In particular, the in-plane shearing stress, σ_{xy}, and the in-plane normal stress difference, σ_{xx} - σ_{yy}, can be measured to high accuracy, while the individual diagonal stress tensor components, σ_{xx}, σ_{yy}, and σ_{zz}, can be measured at reduced accuracy. The basic ATC04 layout is shown in Fig. 24. With the exception of the polysilicon heaters, all bondpads are replicated on each side of the die to facilitate perimeter access to the piezoresistor cells when using arrays of ATC04 to simulate large die.

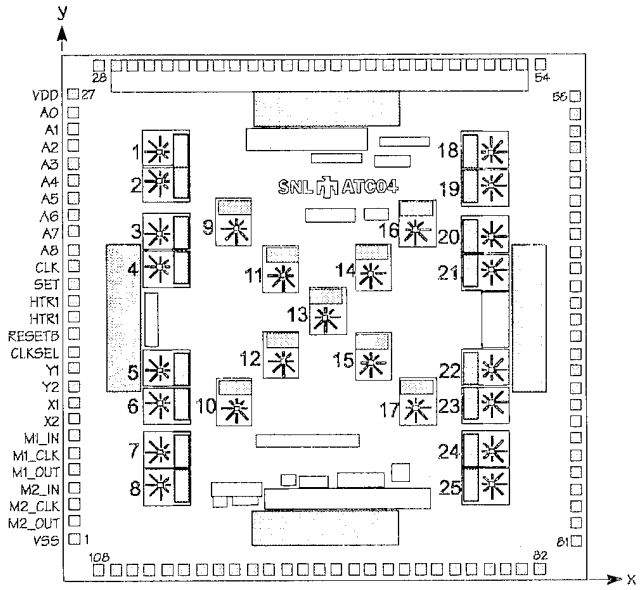


Fig 24. Basic ATC04 layout showing locations of stress sensor cells. The first 27 bondpads are replicated around the die except for the heaters, which are unique to each side. Stress cells are numbered 1 through 25, as shown.

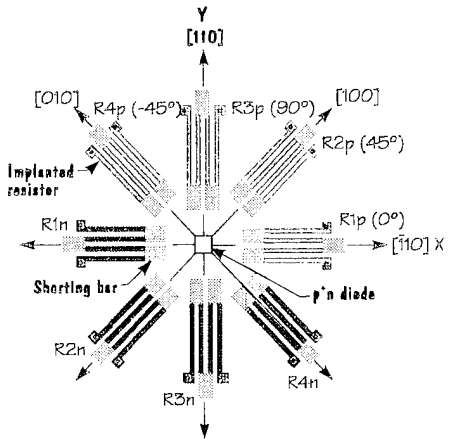


Fig. 25. One of 25 stress cell piezoresistor rosettes with center diode for temperature compensation. Each rosette contains 4 p-type and 4 n-type piezoresistors aligned at 0°, 45°, 90°, and 135° to the wafer flat [110].

Each ATC04 stress sensor cell has four *n*-type and four *p*-type resistors oriented at 0°, +45°, 90°, and 135° with respect to the bottom of the die. The crystal axis associated with the bottom of the die is the [110] axis and this is defined as the *x*-axis direction. Fig. 25 shows the layout of a single stress cell piezoresistor rosette, 1 of 25 on the ATC04 chip. ATC04 can measure the three diagonal components of the stress tensor, σ_{xx}, σ_{yy}, and σ_{zz}, together with the in-plane shearing stress, σ_{xy}. The fundamental equation relating resistance change to stress tensor components for resistors on <100> Si have been given by Sweet.[11]The derivation of these equations is also discussed in detail by Bittle, Suhling, Beaty, Jaeger, and Johnson.[12] It should be noted that the resistor numbering scheme used by Bittle *et al* is different from ours. The change in resistance ΔR_i of the *i*th resistor produced by the stress tensor components is given by,

$$\begin{aligned}
\frac{\Delta R_1}{R_{10}} &= \frac{(\pi_S + \pi_{44})}{2}\sigma_{xx} + \frac{(\pi_S - \pi_{44})}{2}\sigma_{yy} + \pi_{12}\sigma_{zz} \\
\frac{\Delta R_2}{R_{20}} &= \frac{\pi_S}{2}(\sigma_{xx} + \sigma_{yy}) + \pi_{12}\sigma_{zz} + \pi_D\sigma_{xy} \\
\frac{\Delta R_3}{R_{30}} &= \frac{(\pi_S - \pi_{44})}{2}\sigma_{xx} + \frac{(\pi_S + \pi_{44})}{2}\sigma_{yy} + \pi_{12}\sigma_{zz} \\
\frac{\Delta R_4}{R_{40}} &= \frac{\pi_S}{2}(\sigma_{xx} + \sigma_{yy}) + \pi_{12}\sigma_{zz} - \pi_D\sigma_{xy}.
\end{aligned} \tag{4}$$

In Eqs. (4), $\pi_S = \pi_{11} + \pi_{12}$ and $\pi_D = \pi_{11} - \pi_{12}$, where π_{11}, π_{12}, and π_{44} are the fundamental coupling constants or "pi" coefficients which relate stress changes to resistance shifts. R_{0i} is the initial resistance of the *i*th resistor before the stress is applied and the stress tensor $[\sigma_{ij}]$ is defined relative to the chip coordinate system.

There are two measurable stress quantities which do not require a correction for the inevitable temperature shift which occurs between the initial and final measurements. If the fourth of Eqs. (4) is subtracted from the second of Eqs. (4), the quantity σ_{xy} may be found as,

$$\sigma_{xy} = \frac{\delta R_{24}^D}{2\pi_D} \tag{5}$$

Subtracting the third of Eqs. (4) from the first of Eqs. (3) yields,

$$\sigma_{xx} - \sigma_{yy} = \frac{\delta R_{13}^D}{\pi_{44}} \tag{6}$$

If the second and fourth of Eqs (5), or the first and third of Eqs (4) are summed the result is,

$$\begin{aligned}
\delta R_{13}^S &= \delta R_{24}^S \\
&= \pi_S(\sigma_{xx} + \sigma_{yy}) + 2\pi_{12}\sigma_{zz}
\end{aligned} \tag{7}$$

Solving Eq. (6) for σ_{yy} and substituting the result in Eq. (7) yields, after some manipulation,

$$\sigma_{xx} + (\pi_{12}/\pi_S)\sigma_{zz} = \frac{(\delta R_{24}^S - 2\alpha\Delta T)}{2\pi_S} + \frac{\delta R_{13}^D}{\pi_{44}} \tag{8}$$

In the case of Eq. (8), we use *n*-type data for $\delta R_{24}{}^S$ because $|\pi_S|$ is very small for *p*-type resistors. In addition, there is a theoretical result[11] for *n*-type resistors $\pi_S{}^n \approx -\pi_{12}{}^n$ which can be used in Eq. (8) to yield the result we have used for data analysis,

$$\sigma_{xx} - \sigma_{zz} = \frac{(\delta R_{24n}^S - 2\alpha_n\Delta T)}{2\pi_S^n} + \frac{\delta R_{13p}^D}{\pi_{44}^p} \tag{9}$$

---

[11] J. N. Sweet, "Die Stress Measurement Using Piezoresistive Stress Sensor," in J. H. Lau, Thermal Stress and Strain in Microelectronics Packaging, Van Nostrand Reinhold (1993).

[12] D. A. Bittle, J. C. Suhling, R. E. Beaty, R. C. Jaeger, and R. W. Johnson, "Piezoresistive Stress Sensors for Structural Analysis of Electronic Packages," J. of Electronic Packaging, **113**, 203 (1991).

In the case of plastic encapsulated microelectronic packages with relatively large x and y dimensions compared to z thickness, $|\sigma_{zz}|$ is very small relative to $|\sigma_{xx}|$, so Eq. (9) is essentially a measure of the in-plane compressive stress, σ_{xx}.

Experimental Plan: The test sequence for measurement of packaging stresses is shown in Fig. 26. ATC04 die were premeasured (initial measurements) at the die level in waffle packs and shipped to National Semiconductor where they were packaged in 68-lead PLCCs at the Singapore assembly site using four of the epoxy molding compounds developed by Plaskon for the PPA program (B24, X9074.07, ULS12H, and ULS12H-X). At each stage in the experiment, C-mode SAM was used to look for delaminations between the molding compound and the die or die paddle, followed by measurement of the ATC04 stress cells. The bake, moisture soak, and IR reflow steps are out of National's preconditioning specification which simulates the worst case surface mount situation in terms of moisture sensitivity (class 1 qualification).

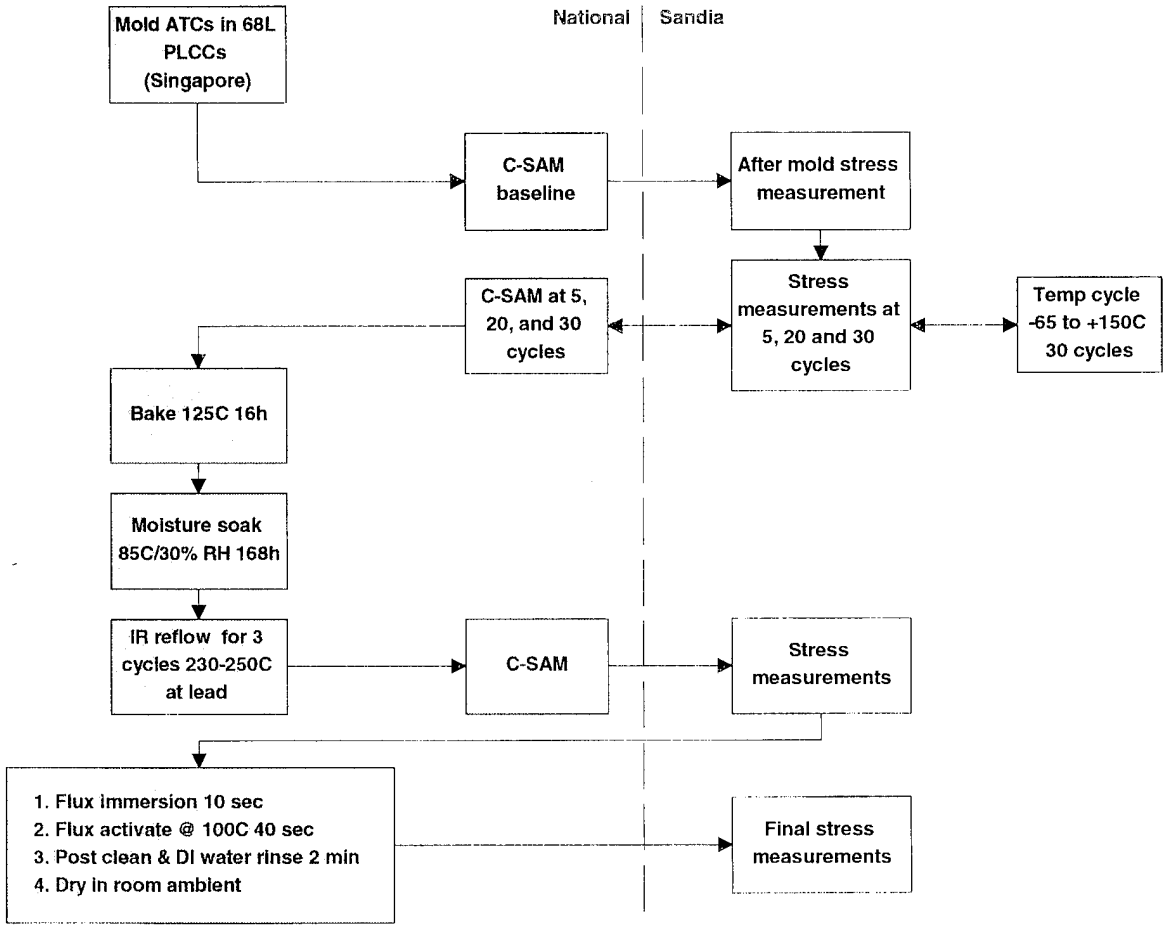


Fig. 26. Test plan for measurement of epoxy molding compound stresses using ATC04 Assembly Test Chips.

Experimental Results: The B24 material is considered a baseline "standard" epoxy molding compound. The X9074.07 is essentially the same material with anti-popcorn additives proprietary to National Semiconductor. The ULS12H is a ultra-low stress material developed expressly for the PPA program, along with a low ionics version, ULS12H-X, containing ionic scavengers. It was assumed at the beginning of the experiment that the latter two would exhibit essentially the same stress behavior. Both in-plane compressive stresses (Eq. 8) and in-plane shear stresses (Eq. 4) where calculated for each of the 25 cells per die. The compressive stress calculations were averaged across each die and the shearing stresses were sorted to provide the peak absolute stress. Only the compressive stress data will be discussed here, as the shearing stress data did not appear to be informative for the purposes of this experiment. This is partly due to the relatively benign shearing stress state present in die smaller than 0.300

inch, such as the ATC04. The ATC04 is often used in the QUAD form, 0.456 inch on a side, to simulate larger die where shearing stress is critical reliability issue. In these larger formats, it is common to apply a polyimide coating over the chip SiN passivation to relieve the high shearing stresses present at the chip edges and corners.

Average compressive stresses, σ_{xx}, after the molding operation are plotted in Fig. 27 as probability vs. stress. In this format, data fitting a straight line would be normal with the slope representing the standard deviation.

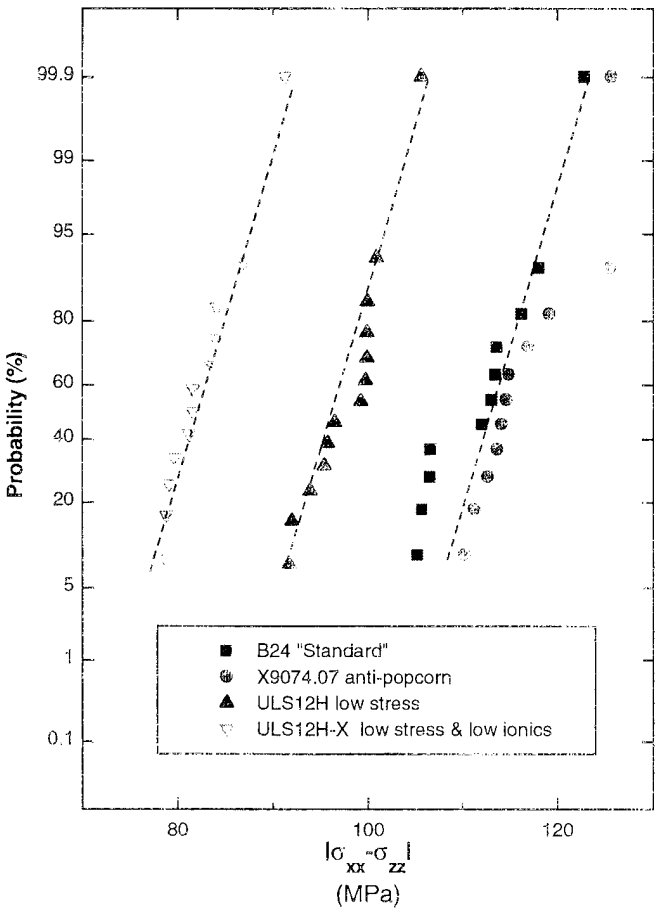


Fig. 27. Average in-plane compressive stress measured with ATC04 test chips molded in 68-lead PLCCs with Plaskon epoxy molding compounds. These data represent changes in stress state due to the die attach and molding operations.

The data in Fig. 27 show a clear trend toward decreasing compressive stress for the low stress formulations, but it was not immediately clear why the ULS12H-X material was so much lower than the ULS12H material. It is informative to predict the stress rankings for these materials using a "stress index" expression, $E\alpha(T_G-T_A)$, where E is the elastic modulus, α is the coefficient of thermal expansion, T_G is the glass transition temperature, and T_A is the ambient temperature. For the materials used in this experiment we get:

B24=33.4 MPa
X9074.07=31.5 MPa
ULS12H=27.6 MPa
ULS12H-X=23.3 MPa

Using this stress ranking, we see that the distributions in Fig. 27 basically follow the same trend and, therefore, are in general agreement with expectations based on material properties. No delaminations were evident from C-SAM at this point or after subsequent thermal cycling.

Fig. 28 contains plots of all the stress data recorded during the experiment. Each chart contains data for one of the four molding compounds, plotted as absolute compressive stress as a function of part serial number. Stress measurements underwent a shift in magnitude toward decreasing compressive stress after the first temperature cycle, but maintained the new stress reading through subsequent temperature cycling and IR reflow with the exception of one part –L11. This part, molded with the ULS12H material, had indications of die attach delamination after IR reflow in C-SAM and also a significant jump in average compressive stress reading.

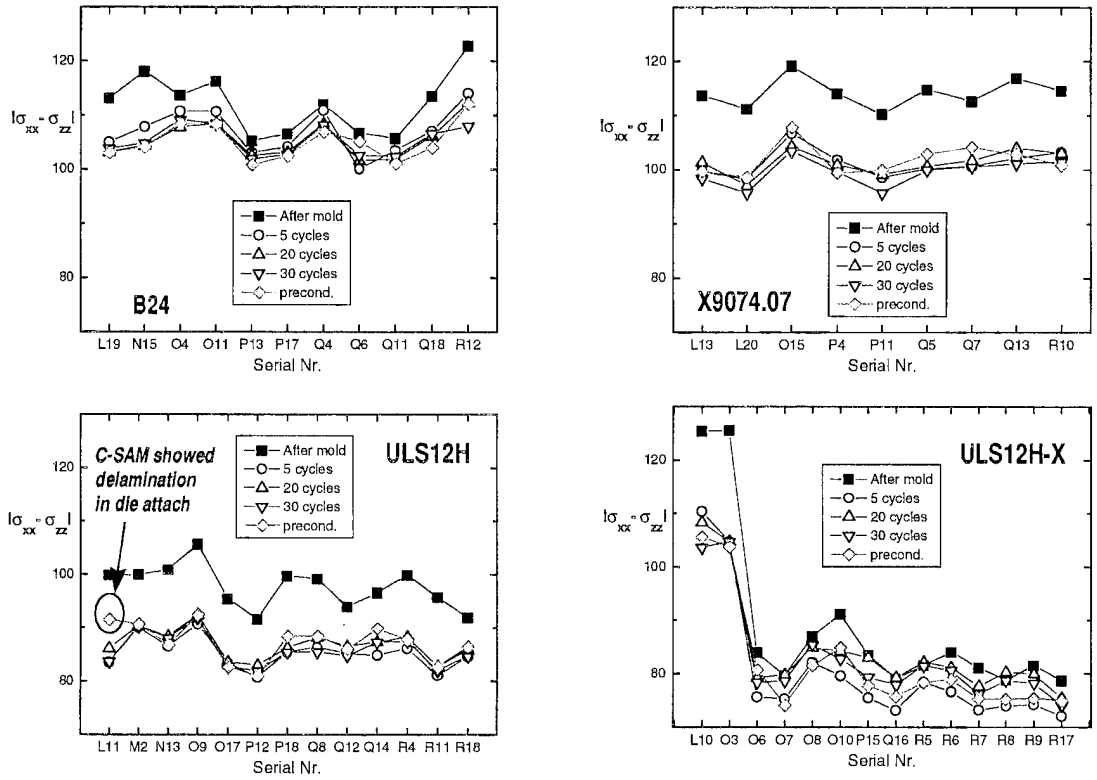


Fig. 28. Average in-plane compressive stress measured by ATC04 test chips molded in 68-lead PLCCs during -65° to +150°C temperature cycle and ~240°C IR reflow simulation. Each data point represents the average of 25 stress cell readings on a single die. Plots are absolute compressive stress vs. part serial number. Symbols in all plots: after mold (■), after 5 temp cycles (O), after 20 temp cycles (△), after 30 temp cycles (▽), and after IR reflow (◇). Note general relaxation of stress after first temperature cycle across all molding compounds. The two outliers in the ULS12H-X chart are thought to be X9074.07 parts that were mismarked. Part L11 showed delamination of the die attach from C-SAM that correlated with an increase in compressive stress after IR reflow.

A plot of the compressive stress readings by sensor cell of part L11 is contained in Fig. 29. Each data point represents the calculated stress at the location of the sensor listed at the bottom. (See Fig. 24 for sensor location reference) For simplicity, only the final temperature cycle data are shown. The stress relaxation after temperature cycling apparent in the averaged data in Fig. 29 is evident cell by cell. However, after IR reflow the data show that cells numbered 9 through 17 see an increase in stress of ~10 MPa over what would be expected based on the response of the remaining cells. C-SAM of this part showed a complete delamination of the die attach interface. Linear elastic theory would predict that a delamination of either the die attach interface or the die surface to mold compound interface would cause the die to bow in a direction opposite the delamination. Fig. 30 illustrates this effect for the case of die attach delamination. An upwardly bowing die would cause an increase in compressive stress proportional to the local radius of curvature. The data in Fig. 29 suggest that the curvature is minimal at the outer edges of the die, something that seems intuitively correct, but has not been confirmed analytically or through finite element modeling.

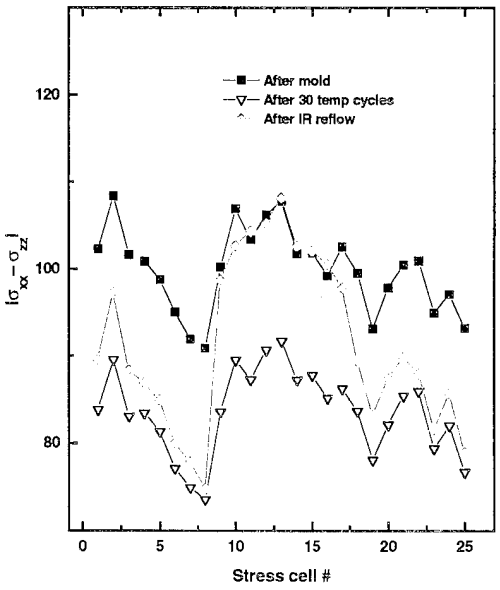


Fig. 29. Compressive stress measurements on part L11 as a function of cell number. Symbols are after mold (■), after 30 temperature cycles (▽) and after IR reflow (^). Stress peaking in center cells after IR reflow are associated with die attach delamination.

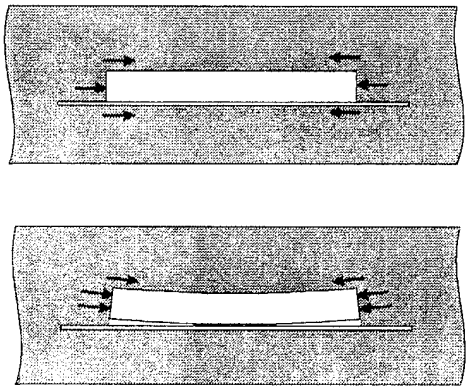


Fig. 30. Conceptual cross-section of a die bonded to Cu lead frame paddle in a molded package (top) illustrating die bending (bottom) due to delamination of the die attach interface. The die would bow away from the paddle causing an increase in compressive stress at the die surface.

SUMMARY

The design and characterization of the NAT-01 moisture and corrosion sensing test chip has been completed. Temperature sensitivity experiments indicate that the moisture sensor sensitivity drift during long term exposure to 300°C in air, N_2, and vacuum environments is excessive for experimental applications requiring absolute measurement accuracy. However, the ability of the sensor to withstand these conditions without loss of functionality and only moderate changes in sensitivity demonstrates its utility for a number of experimental purposes including pinhole detection in moisture barrier coatings and measurement of moisture diffusion through

epoxy molding compounds. In particular, the moisture sensor provides a means of quickly judging the efficacy of a barrier coating without undergoing lengthy HAST testing using triple track corrosion sensors or product die.

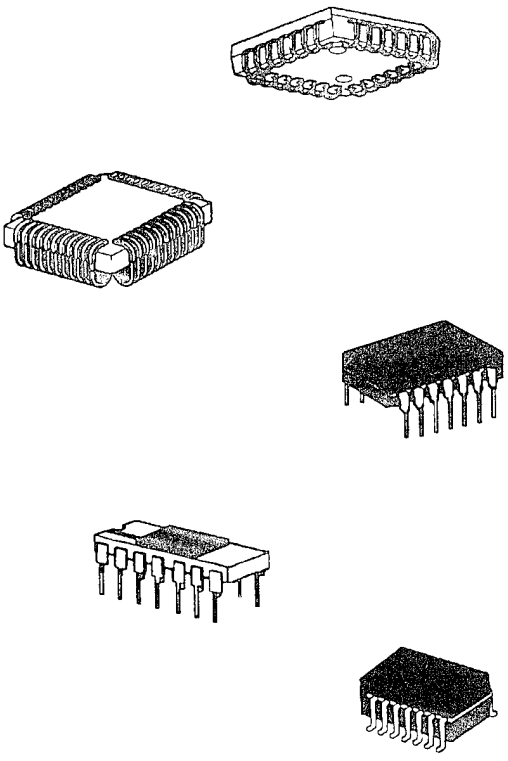
The corrosion sensor triple track is not a unique design to the NAT-01, but inclusion of both passivated and unpassivated structures allows sensitive detection of ionic contamination in molding compound materials and discrimination of electrochemical corrosion failure mechanisms. Parallel HAST experiments with Dow Corning and Naval Surface Warfare Center Crane using the NAT-01 yielded failure data that were not completely consistent with HAST sensor characterization experiments done at Sandia. It is not obvious why this is so, but the relatively small sample sizes that resulted in each leg of their experiments can contribute to misdiagnosis of failure data.

HAST failure data from unpassivated NAT-01 corrosion sensors packaged in 14-lead DIPs and SOICs suggest improved reliability in moisture environments using Plaskon low ionics materials. This was supported by Dow Corning HAST failure data on NAT-01 unpassivated corrosion sensors packaged in 68-lead PLCCs, but not by HAST failure data from Crane.

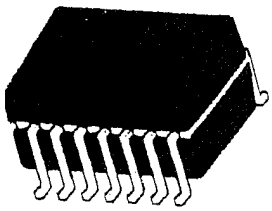
Stress measurements using the ATC04 stress measurement test chip were able to discriminate between standard and low stress molding compounds, showing a clear reduction in room temperature compressive stress on die molded in 68-lead PLCCs using the Plaskon ULS12H and ULS12H-X materials. These measurements were able to detect, in at least one case, delamination of the die attach interface after IR reflow.

PLASTIC PACKAGE AVAILABILITY PROGRAM

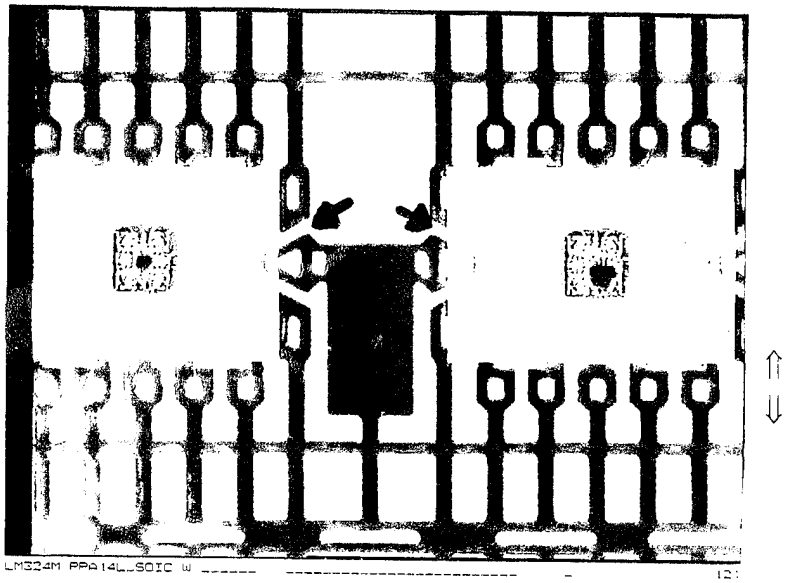
DOCUMENTATION SECTION 4



PPA ASSEMBLY DOCUMENTATION



14L - SOIC



A pair of bonded reject (note the ink dots)
LM1902 die

Lead Frame strip is 14 pairs long for a total of 28 units / strip

Arrows in picture denote EMC inject paths.

Figure 1

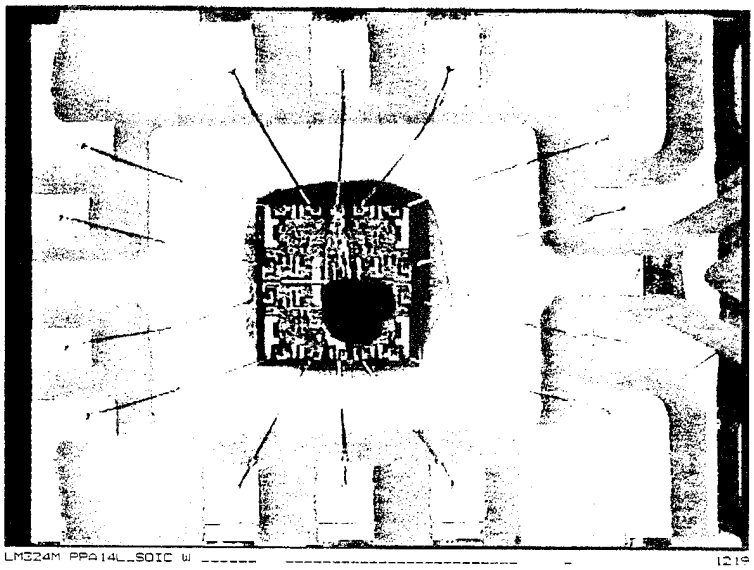


Figure 2

Enlargement shows die attach material run-out around die perimeter, detail of automatic gold ball-bond placement, and silverplated die paddle, and lead tips. Note longer wire path lengths required for (8) end lead bonds vs. (6) top & bottom lead bonds

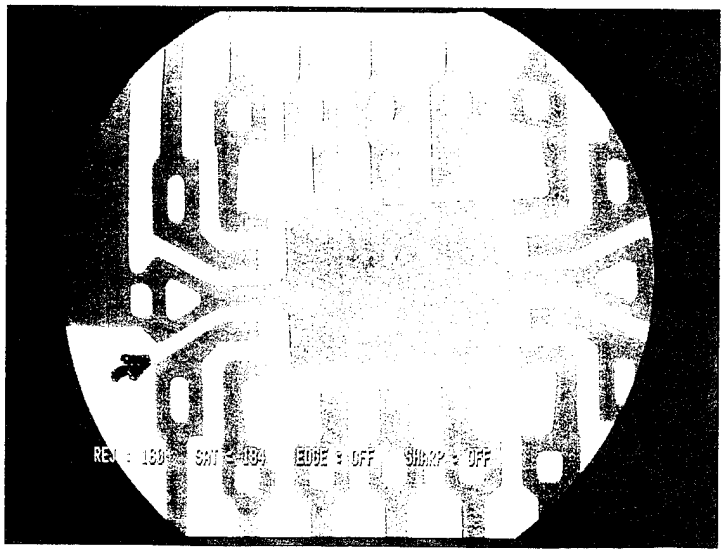


Figure 3

X-ray photograph after mold. Showing acceptable wire sweep. Routinely performed each work shift or mold set-up.

Arrow on photo shows EMC inject path

PPA ASSEMBLY DOCUMENTATION - 14L - DIP

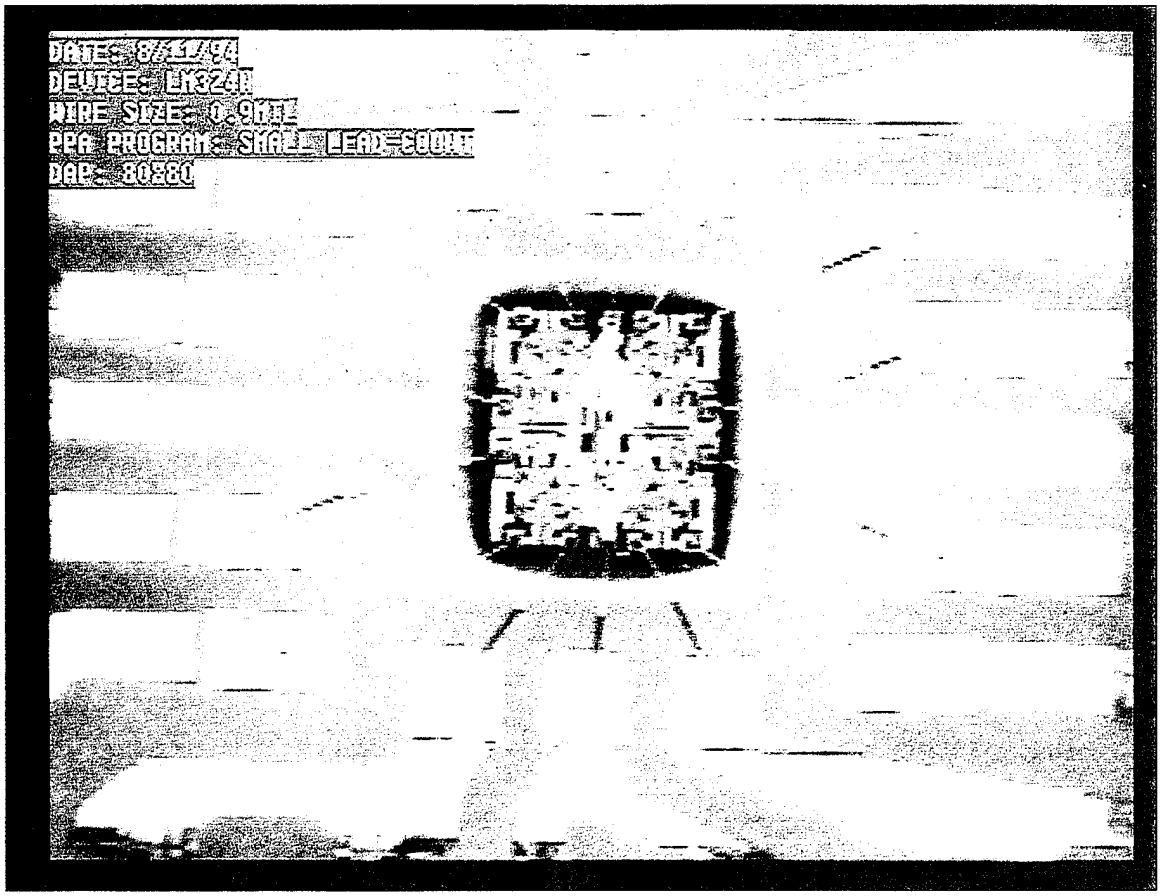
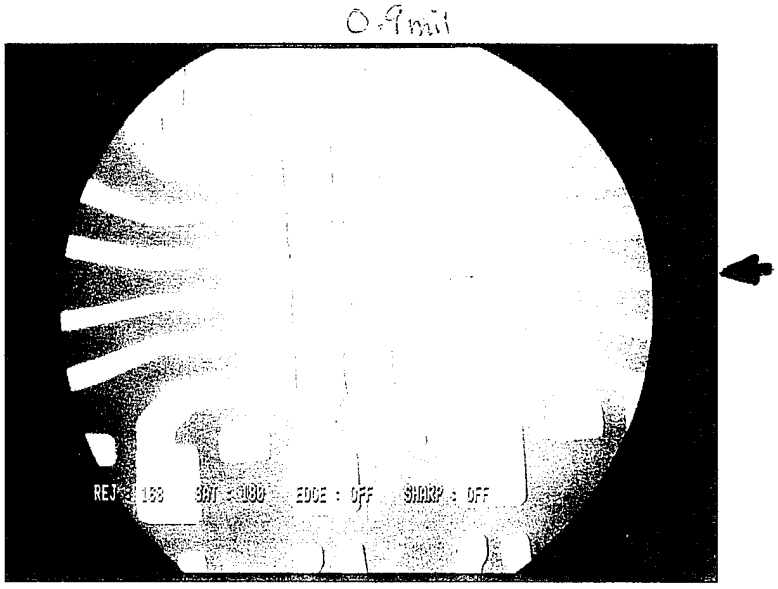


Figure 4a Enlargement shows die attach material run-out around die perimeter, detail of automatic gold ball-bond placement, and silver-plated die paddle and lead tips. Note longer wire path lengths required for (8) end lead bonds vs. (6) top & bottom lead-bonds.



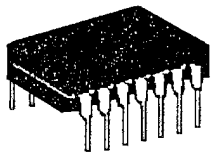


Figure 4b 14L- DIP

X-ray photograph after mold. Showing acceptable wire sweep. Routinely performed each work shift or mold set-up.

Arrow on photo shows EMC inject path.

National Semiconductor

May 1989

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

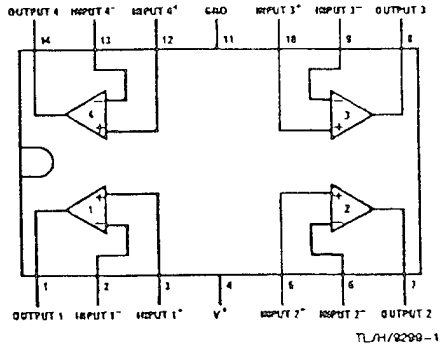
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3 V_{DC} to 32 V_{DC}
  - or dual supplies ±1.5 V_{DC} to ±16 V_{DC}
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC} and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagram

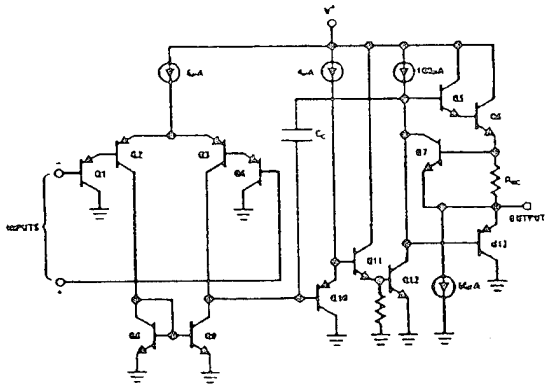
Dual-In-Line Package



Top View

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ, LM324M, LM324AM, LM2902M, LM324N, LM324AN or LM2902N
See NS Package Number J14A, M14A or N14A

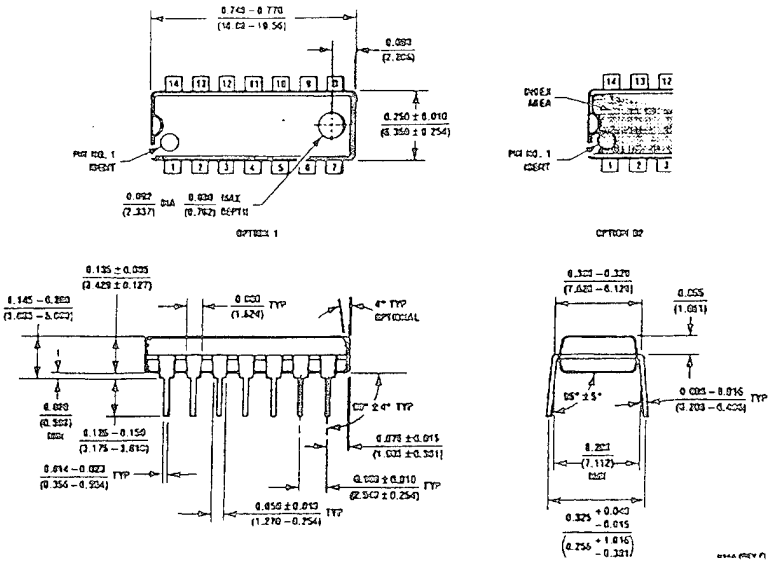
Schematic Diagram (Each Amplifier)



©1988 National Semiconductor Corporation TL/H/9299

Figure 5

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LM324N, LM324AN or LM2902N
NS Package Number N14A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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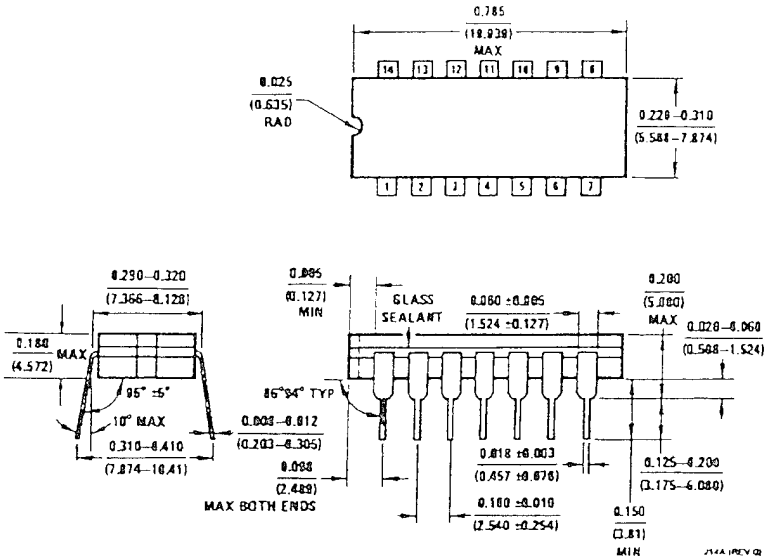
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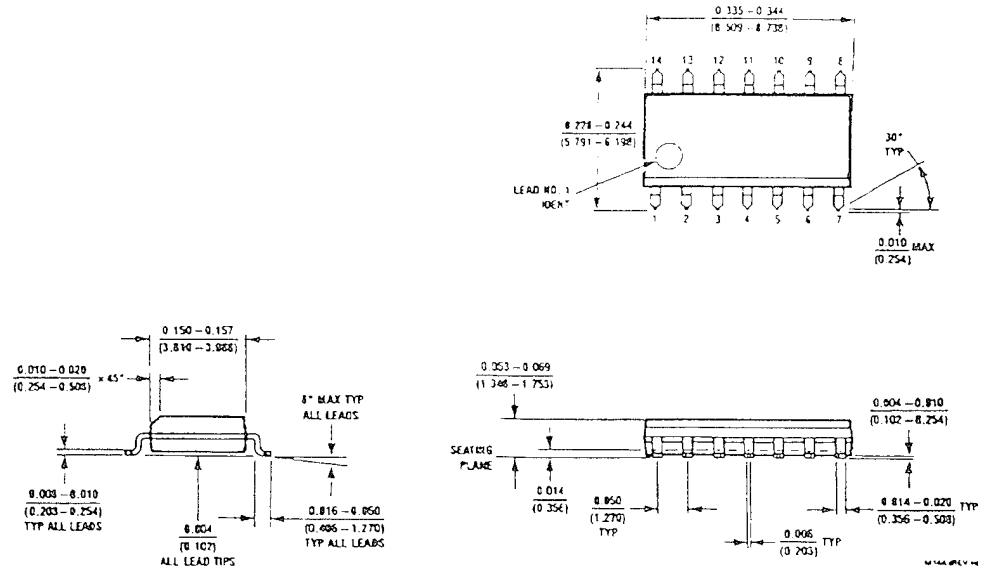
National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.
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Figure 6

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J or LM324AJ
NS Package Number J14A



S.O. Package (M)
Order Number LM324M, LM324AM or LM2902M
NS Package Number M14A

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Figure 7

Figure 8

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 9)

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Input Current (V_{IN} < −0.3 V_{DC}) (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0\ V_{DC}$, (Note 4), unless otherwise stated

Parameter	Conditions	LM124A		LM224A		LM324A		LM124/LM224		LM324		LM2902		Units
		Min	Typ Max	Min	Typ Max	Min	Typ Max	Min	Typ Max	Min	Typ Max	Min	Typ Max	
Input Offset Voltage	(Note 5) $T_A = 25°C$		±1 ±2		±1 ±3		±2 ±3		±2 ±5		±2 ±7		±2 ±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		20 50		40 80		45 100		45 150		45 250		45 250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		±2 ±10		±2 ±15		±5 ±30		±3 ±30		±5 ±50		±5 ±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$, (LM2902, $V^+ = 26\ V_{DC}$), $T_A = 25°C$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	V_{DC}
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps													
	$V^+ = 30V$ (LM2902 $V^+ = 26V$)		1.5 3		1.5 3		1.5 3		1.5 3		1.5 3		1.5 3	mA_{DC}
	$V^+ = 5V$		0.7 1.2		0.7 1.2		0.7 1.2		0.7 1.2		0.7 1.2		0.7 1.2	
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$, $R_L \geq 2\ k\Omega$, ($V_O = 1\ V_{DC}$ to $11\ V_{DC}$), $T_A = 25°C$	50	100	50	100	25	100	50	100	25	100	25	100	V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5\ V_{DC}$, $T_A = 25°C$	70	85	70	85	65	85	70	85	65	85	50	70	dB
Power Supply Rejection Ratio	DC, $V^+ = 5\ V_{DC}$ to $30\ V_{DC}$ (LM2902, $V^+ = 5\ V_{DC}$ to $26\ V_{DC}$), $T_A = 25°C$	65	100	65	100	65	100	65	100	65	100	50	100	dB

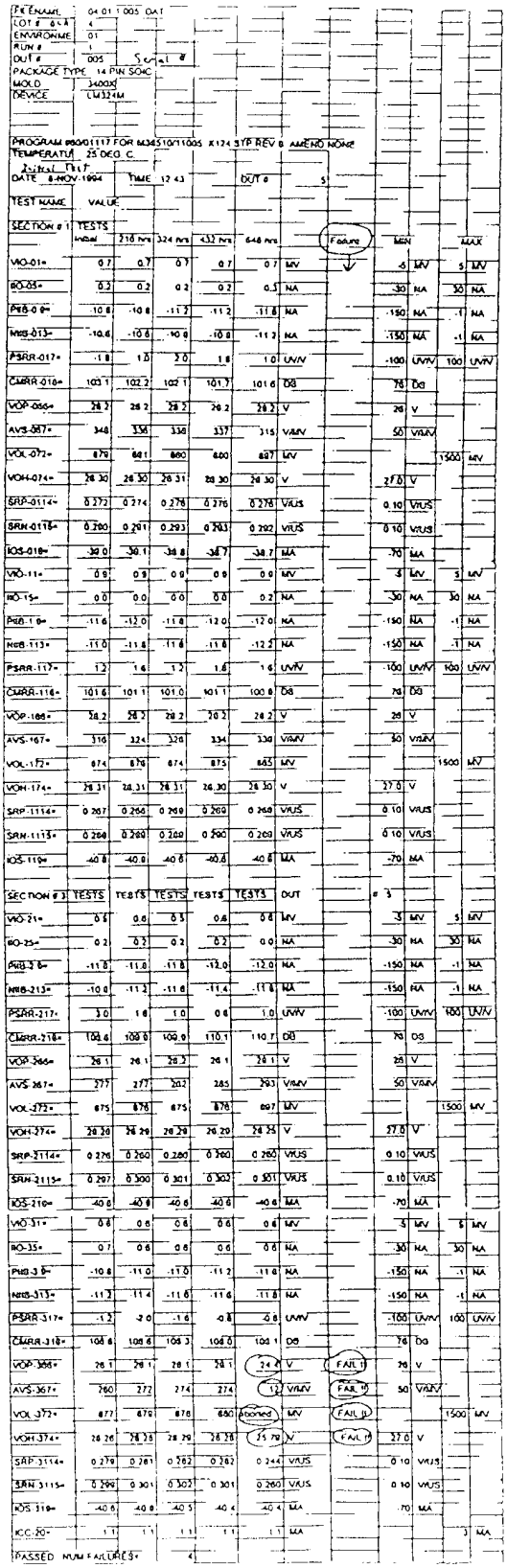


Figure 9a

Parametric readouts for a 14L - SOIC on 159°C HAST. Drifts were negligible up to 648 hrs. at which point, 3 voltage out and a voltage gain parameter failed on quad section 4.

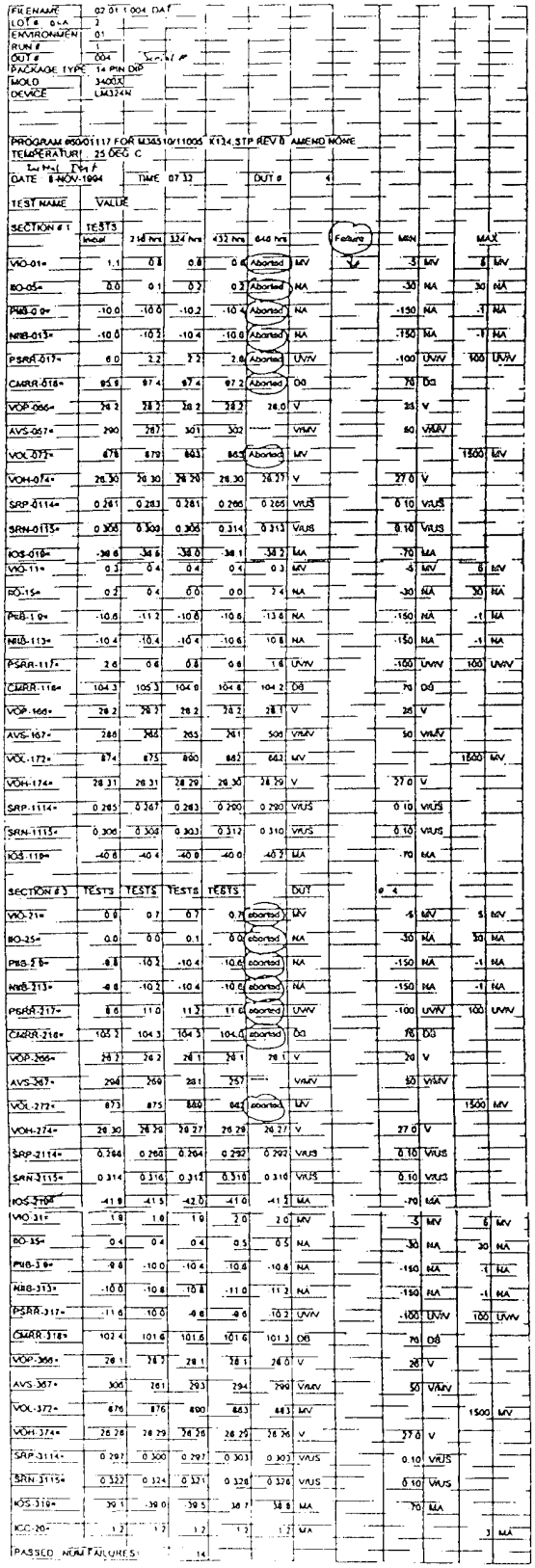


Figure 9b

Parametric readouts for a 14L - MDIP on 159°C HAST. Drifts were negligible until 648 hrs., when 7 parameters each failed on quad sections 1 and 3.

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National Semiconductor

Oct. 27, 1995

Ron Kovacs
National Semiconductor Corporation
3707 Tahoe Way
Mail Stop 19-100
Santa Clara, CA 95051

Subject: Maximum Recommended Operating Conditions vs. Plastic Package Availability Test Conditions

Dear Ron,

You asked for a comparison of Maximum Recommended Operating Conditions for LM124s in 14 lead SOICs, 14 lead plastic molded DIPs, and 14 lead Cerdip. The test conditions that you listed in your memo were: HAST(Highly Accelerated Stress Testing) @ 130°C & 159°C, Temperature Cycling from -65°C to 150°C, HTS (High Temperature Storage) @ 175°C and OPL (Operating Life Testing) @ 125°C.

HAST (Highly Accelerated Stress Testing) @ 130°C & 159°C:
There is no listed operating condition for HAST testing, as it is a destructive environment outside the expected operating conditions. As it's name implies, it is a highly accelerated test, normally used to predict and to qualify the reliability of commercial plastic integrated circuits for commercial applications. It is intended to exacerbate the weaknesses inherent to plastic packaging systems. Normally, it is not applied to hermetic devices due to their inherent strengths at resisting moisture ingress. The basic assumption is that neither hermetic nor plastic parts are actually operated in any application in an environment of high pressure/high temperature steam with or without bias applied. 159°C is beyond the maximum storage temperature listed for LM124 devices in any plastic package of 150°C(1). Hermetic package absolute maximum storage temperature is 165°C(2). Neither package system stores well at these elevated temperatures from a solderability standpoint, and the plastic package system may be above it's glass transition point. 130°C(1) (2) is above the absolute maximum operating condition for LM124 devices in either hermetic or plastic packages.

	LM124	LM124	LM324 (most commonly used commercial "LM124" device)
	Plastic	Hermetic	Plastic
Max Storage	150°C(1)	165°C(2)	150°C(1)
Max Operating	125°C(1)	125°C(2)	70°C(1)
Max Tj	150°C(1)	200°C(2)	150°C(1)

HAST testing is not required(3) (4) for qualification of commercial IC's at National, but is sometimes performed to meet specific customer requirements. Normally the test temperature is 130°C for 96 hours.

National normally performs the of 85°C/85%RH Biased Humidity Life and Storage Autoclave 121°C/100%RH/1atm(gage) as moisture related qualification tests(3) (4). Both test conditions are considered destructive tests.

Commercial NSC qualification requirements(3):
85°C/85%RH Biased Humidity Life:
Category 1 plastic devices are tested for 500 hours (ss=100 acc=0)
Category 2 plastic devices are tested for 1000 hours (ss=100 acc=0)
Category 3 plastic devices are tested for 1000 hours minimum with ss=116

Figure 10

Storage Autoclave 121°C/100%RH/1atm(gage) (3):

Category 1 plastic devices are tested for 96 hours (ss=50 acc=0)
Category 2 plastic devices are tested for 168 hours (ss=50 acc=0)
Category 3 plastic devices are tested for 500 hours (ss=50 acc=0)

Explanation of "Category" (3):
Category 1 devices are basic commercial devices, Category 2 devices are essentially telecom type requirements, and Category 3 devices are automotive safety applications (like antilock braking, engine controls etc.). Mil/Aero Division products are also defined in the Category 3 section.

Temperature Cycling from -65°C to 150°C:
Both Hermetic and Plastic devices are often qualified by temperature cycling across this range.

	LM124 Plastic	LM124 Hermetic	LM324 (most commonly used commercial "LM124" device) Plastic
Max Storage	150°C(1)	165°C(2)	150°C(1)
Min Storage	-65°C(1)	-65°C(2)	-65°C(1)
Max Operating	125°C(1)	125°C(2)	70°C(1)
Min Operating	-55°C(1)	-55°C(2)	0°C(1)
Max Tj	150°C(1)	200°C(2)	150°C(1)

Commercial NSC qualification requirements(3):
Category 1 plastic devices are tested 0°C to 125°C 1000 cycles (ss=100 acc=0)
Category 2 plastic devices are tested 0°C to 125°C 2000 cycles (ss=100 acc=0)
Category 3 plastic devices are tested -65°C to 150°C 2000 cycles (ss=153 acc=0)

HTS (High Temperature Storage) @ 175°C:
This test is considered destructive because it exceeds the glass transition point of most molding compounds used by NSC. It also exceeds the absolute maximum ratings for both hermetic and plastic packages for this device type. While the hermetic package is capable of extended storage at this temperature, the solderability would be negatively impacted. The gold/aluminum interfaces in plastic package systems can be permanently degraded by this exposure. National has published an absolute maximum of 167°C(6) for gold/aluminum interface devices (most plastic and a very few hermetic packages) to prevent the onset of Kirkendall voiding. National normally tests HTS(4) at 150°C for 1000 hours when qualifying a new plastic package system.

	LM124 Plastic	LM124 Hermetic	LM324 (most commonly used commercial "LM124" device) Plastic
Max Storage	150°C(1)	165°C(2)	150°C(1)
Max Operating	125°C(1)	125°C(2)	70°C(1)
Max Tj	150°C(1)	200°C(2)	150°C(1)

OPL (Operating Life Testing) @ 125°C:
168 hour exposures are not considered destructive, but solderability is negatively impacted. Significant degradation of solderability occurs for 1000 hour exposures.

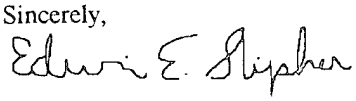
	LM124	LM124	LM324 (most commonly used commercial "LM124"

	Plastic	Hermetic	device) Plastic
Max OPL	125°C(1)	175°C(2)	125°C(1)
		Normal 150°C	
Max Operating	125°C(1)	125°C(2)	70°C(1)
Max Tj	150°C(1)	200°C(2)	150°C(1)

Commercial NSC qualification requirements(3):
Category 1 plastic devices are tested 500 hours @ 125°C (ss=100 acc=0)
Category 2 plastic devices are tested 1000 hours @ 125°C (ss=100 acc=0)
Category 3 plastic devices are tested 1000 hours @ 150°C (ss=116 acc=0)

Sources:
1. LM124,224,324 datasheet (Absolute Maximum Ratings)
2. Mil-Prf-38535
3. SOP-5-284 - Graded Product Qualification for New Products
4. NSC Packaging Databook
5. The evaluation of Reliability Data - National Semiconductor Corporation
6. Reliability Handbook - National Semiconductor Corporation

Sincerely,



Quality Assurance Manager, Military Aerospace Division
Telephone: (408) 721-2664 Pager: (408) 447-9588

cc: Bob Bryne

1.0 :DIE SHEAR DATA OF SO14W

device	: lm324m	nat01m
die size	: 60x66	100x100
s/size	: 5 units	4 units
MIN	: 3.59	2.60
MAX	: 4.35	5.24
AVER	: 3.944	7.55
STD DEV	: 0.356	1.15

ALL READING ARE IN (KG)

b/mode	: > 50% sil rem. (100%)	50% of clean shear and 50% of tie bar break
SPEC REQ	: 1.5	2.5

1.1 :DIE SHEAR DATA OF MDIP

dev	: lm2902n	nat01n
die size	: 60x66	100x100
s/size	: 5 units	1 unit
MIN	: 4.95	5.24
MAX	: 5.24	5.24
AVER	: 5.112	27.5
STD DEV	: 0.11	13.0
b/mode	: >50% sil.rem.(100%)	<50% sil rem.
SPEC LIMIT	: 1.5	2.5

2.0 :PULL TEST DATA OF SO14W

MIN	: 4.5	4.7
MAX	: 10.4	10.0
AVER	: 7.13	7.76
STD DEV	: 1.28	1.39
S/SIZE	: 50	50
BREAK MD	: B MODE	B MODE

B STAND FOR WIRE BREAK BETWEEN HEEL OF THE BALL
ALL THE READING WERE IN (GM)

2.1 : PULL TEST DATA OF MDIP

MIN	: 4.5	4.7
MAX	: 8.0	8.2
AVER	: 6.02	6.66
STD DEV	: 0.82	1.17
S/SIZE	: 50	14
BREAK MD	: B MODE	B MODE

3.0 : BALL SHEAR DATA ON SO14W

MIN	: 50.8	63.6
MAX	: 92.0	119.2
AVER	: 64.65	86.95
STD DEV	: 7.484	12.51
S/SIZE	: 50	38
BREAK M	: GD 1 :96%	39.6%
	GD 2 :4%	60.5%

GD 1 STAND FOR THERE IS NO INDICATION OF GOLD REMNANTS ON THE BOND PAD AFTER BALL SHEAR.
GD 2 STAND FOR THERE IS STILL BALL SIZE REMAIN ON THE BOND PAD AFTER BALL SHEAR.
ALL READING WERE IN (GM)

3.1 : BALL SHEAR DATA ON MDIP

MIN	: 50.1	44.1
MAX	: 69.9	59.7
AVER	: 61.32	51.96
STD DEV	: 5.02	4.44
S.SIZE	: 50	13
BREAK M	: GD 1 : 16%	GD 1 :NIL
	GD 2 : 84%	GD 2 :100%

4.0 : 3/OPT DATA (CONTROL)

DEVICE	LM324N	LM324N	LM324N	LM6218WM	LM6218WM	LM6218WM
PT NBR	YV2622E019	YV2622E027	YV2622E035	YV2621G019	YV2621G027	YV2621G035
IN QTY	805	804	406	1120	991	473
OUT QTY	797	803	405	1117	989	473
YLD(%)	99.01	99.8	99.7	99.7	99.8	100
DEFECTS:						
MISSING WIRE	-	-	-	-	0.1	-
PULL TEST	-	-	-	-	0.1	-
INSUF/EPOXY	0.89	0.2	0.3	-	-	-
MISSING DIE	0.1	-	-	-	-	-
INK DIE	-	-	-	0.3	-	-

4.1 : 3/OPT DATA(TEST NAT01)

DEVICE	LM1877MX-9	LM1877MX-9	LM1877MX-9	LM2902N	LM2902N	LM2902N
PT NBR	YV2619E019	YV2619E027	YV2619E035	YV2620J019	YV2620J027	YV2620J035
IN QTY	45	32	19	45	45	26
OUT QTY	45	32	19	45	45	26
YLD(%)	100	100	100	100	100	100

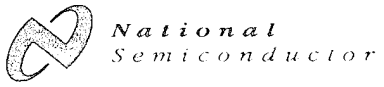
Figure 11.
Line monitor-sample data for the LLC build of 14L-SOIC and 14L-MDIP in Malacca, Malaysia.

PLASTIC PACKAGE AVAILABILITY PROGRAM

High Lead Count Environment and Electrical Test

HAST@ 130°C 159°C	Performed @ DCC*
Temperature Cycle	Performed @ DCC*
HTS @ 175°C	Performed @ NSC
Operational Life-Test	Performed @ NSC
Electrical Test	Performed @ NSC

*See Dow Corning report for details on environmental test.



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High Lead Count

For the high lead count portion of the experiment we chose SCX6244 1.5 micron, CMOS Gate Array as a test vehicle. The device has die size of 259x262 mils and has 68 pins. The device was chosen for its size and complexity of the circuitry. Since the device was packaged in 68 pin Plastic Leaded Chip Carrier (PLCC) before, it was decided that the same package be used in the experiment. As for the epoxy molding compound (EMC), four different types were used and consequently tested. These EMCs were Plaskon ULS12H, Plaskon ULS12HX (low chloride), Plaskon X9074.07 (anti-popcorn), and National Semiconductor's B24. For the purpose of comparison, ceramic packages were also incorporated into the test matrix. These ceramic units will be considered as controls and their test data will be used for baselining against that of plastic packages.

The environmental test series consisted of HAST, Temperature Cycling, High Temperature Storage, and Operational Life-Test. The environmental stressing of devices for HAST and Temperature Cycle were conducted at Dow Corning Corporation, while High Temperature Storage (refer to DCC section of the report) and Operational Life-Test were performed at National Semiconductor in Santa Clara. However, all electrical testing and failure analysis were performed at National Semiconductor in Santa Clara.

All the plastic encapsulated microcircuits were molded at the National's Singapore facility where most of the commercial products are assembled for various product lines. A team from National Semiconductor and Rome Lab were sent to monitor the manufacturing processes. The ceramic control units were assembled in the National's Santa Clara facility. About half of the assembled plastic encapsulated devices were then subjected to precondition flow. The flow is used to simulate device condition during the board assembly. All devices were visually inspected, marked, and electrically tested to MIL-883 specifications before being subjected to the environmental stress test. The table below shows the total number of units that were available after post-assembly electrical test.

Molding Compound	Preconditioned	Non-Preconditioned
ULS12HX	77	80
ULS12H	76	91
X9074.07	82	87
B24	101	87
Control (ceramic)	346	

Figure 1.

All units were electrically tested on the Sentry Tester System at National's Santa Clara testing facility. Sentry is a VLSI testing system utilized by the various National's product lines for testing production units. The program used for testing was based on Mil-883 specifications and has a National's internal designation of SCX6244-UEU. The length of the test itself was about 30 seconds. The system first tests for continuity, such as upper and lower diode test for the input pins and short test. The system next tests I_{DD} and I_{SS} parametric values at various voltages against the specification. The system next feeds in set of test vectors to simulate actual operating condition and to determine if the circuitry behaves accordingly. As a last step, output values are read and compared to the specification. These are output voltages and currents at various bias voltage levels. If a unit passes all the above tests, then it is considered as an electrically good device.

During testing, special precaution was taken to ensure that each failure was legitimate and authentic. This was achieved by employing a double screen process where each failed device went through two additional flows, with each flow under the scrutiny of the operator's observation. In the PrA, the committee has decided to

report only gross functional failures, such as opens, shorts, and logic failures. Therefore, a device not meeting the required specifications and parametric failures was not classified as a failure in this report. Once the failed devices were separated and marked, they were put through the various failure analysis steps.

HAST: 130°C and 159°C

HAST is a commonly used test in the industry to activate and accelerate the moisture failure mechanism prevalent in plastic encapsulated microcircuits. Please refer to Dow Corning section of the report for the details. Altogether, four HAST boards were assemble by HAST Solution Inc. Figure 2 and Figure 3 show the HAST circuit and the specification, respectively. For 130°C, the devices were electrically tested initially, and at 216, 432, 648, 864, 1080, and 1296 hours after the devices were removed from the HAST chamber to detect any failures. For 159°C, the devices were electrically tested initially, and at 24, 72, 108, 216, 432, 648 hours. Table 1 and 2 illustrate the readout points and the electrical test results.

The HAST environmental testing at 130°C and 159°C with 85% RH caused some degradation of the device lead finish due to the formation of corrosion. This problem was especially acute toward the later stages of the test. Therefore, the devices were manually cleaned after each HAST run to ensure good electrical contact of the devices leads in the sockets for the HAST board as well as the electrical tester. The dark discoloration on the leads were removed by polishing with very fine grain sand paper to expose the lead underneath.

High Temperature Storage:

The High Temperature Storage (HTS) test accelerates temperature induced failures such as intermetallic growth, Kirkendall Voiding and depolymerization. The HTS tests were conducted at 175°C without bias applied to the device. The electrical tests were performed at 0, 216, 432, 1080, 1512, 1944, 2500, ant 4125 hours. There were no failures after 4125 hours of storage. The industry average for the HTS is 1000 hours. Table 3 illustrates the read-out points and the electrical test results.

Operational Life-Test:

The Operational Life-Test is basically a Burn-In (exposure to high temperature with electrical bias applied) performed for extended duration. This test is designed to weed out devices subject to infant mortality or excessive parametric drift. There are two components to the Burn-In system, the Burn-In board and the clock driver. The Burn-In board would be stressed along with the devices in the chamber while the clock driver would reside outside of the oven. There are two clocks on the driver and they are asynchronous. Figure 4 shows the clock timing diagram. Altogether three Burn-In boards with thirty six sockets each and two clock driver boards were assembled by Adaptive Electronic.

Figure 5 and Figure 6 show the Burn-In circuit and Burn-In clock circuit, respectively. The Burn-In was performed at 125°C with 5V applied to the device. The electrical tests were performed at initial, 168, 1000, 2000, 3000, and 4000 hours. Table 4 illustrates the readout points and the electrical test results. There were no failures and consequent failure analysis didn't show any degradation of the devices.

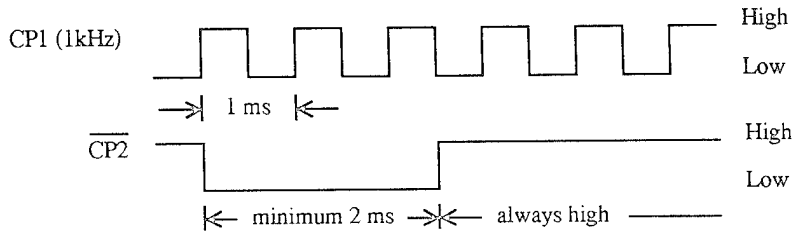


Figure 4.

Temperature Cycle:

Temperature cycle is a test whereby devices are stored for short periods (15 minutes) alternately at high and low temperatures in gas filled chambers, with a maximum transfer time between chambers of one minute. Normally 10 cycles are performed from -65°C to +150°C. This stresses device assembly because of the different thermal coefficients of expansion of the various materials used. The temperature cycling was performed at Dow Corning as in the case with HAST, while electrical tests were performed at National. The devices were electrically tested initially, and at 100, 500, 1000, 1500, and 2000 cycles. Table 5 illustrates the readout points and the electrical test results.

During the process of transferring devices between National and Dow Corning, the precondition and non-precondition devices were accidentally mixed. Therefore, the precondition portion of the test was lost and the 12 failures we observed after 2000 cycles were not distinguishable for their precondition status.

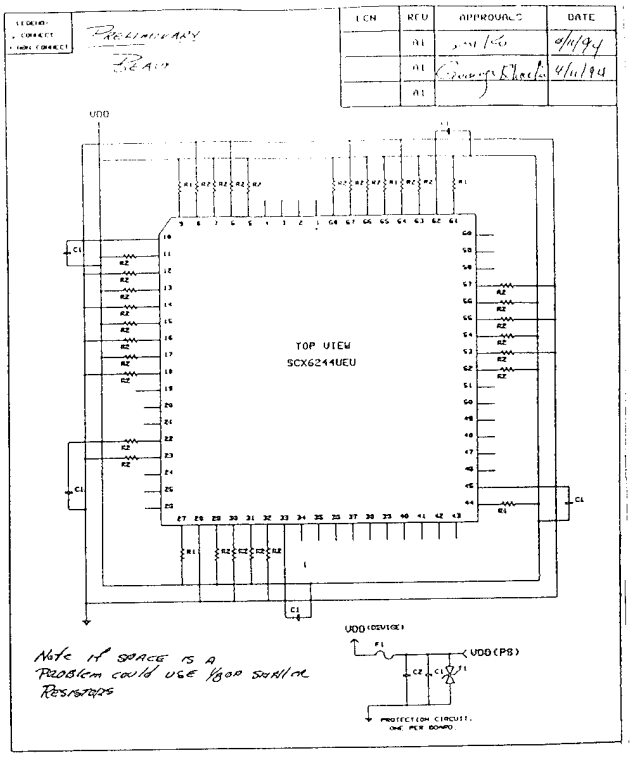


Figure 2.

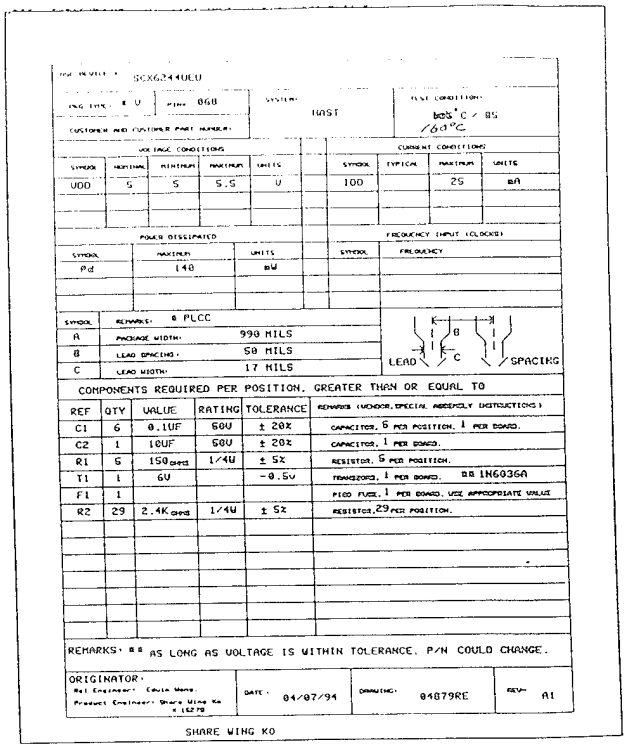


Figure 3.

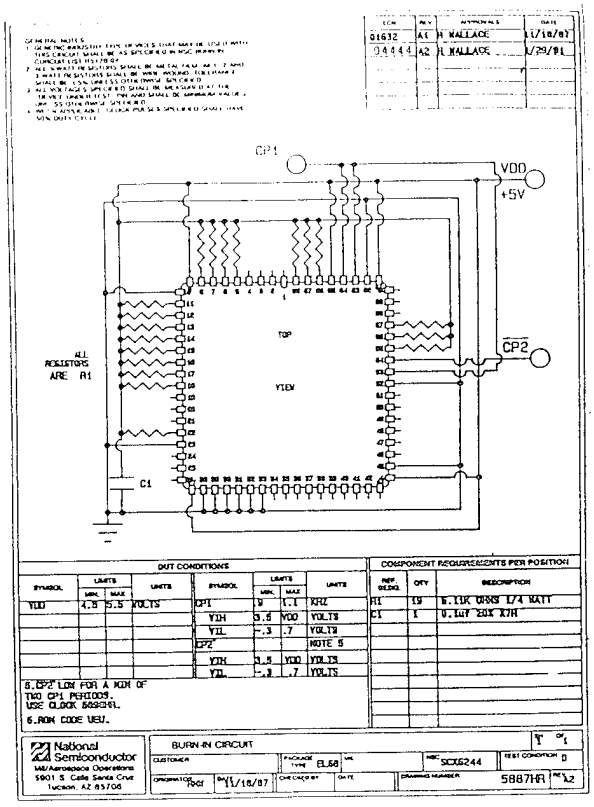


Figure 5.

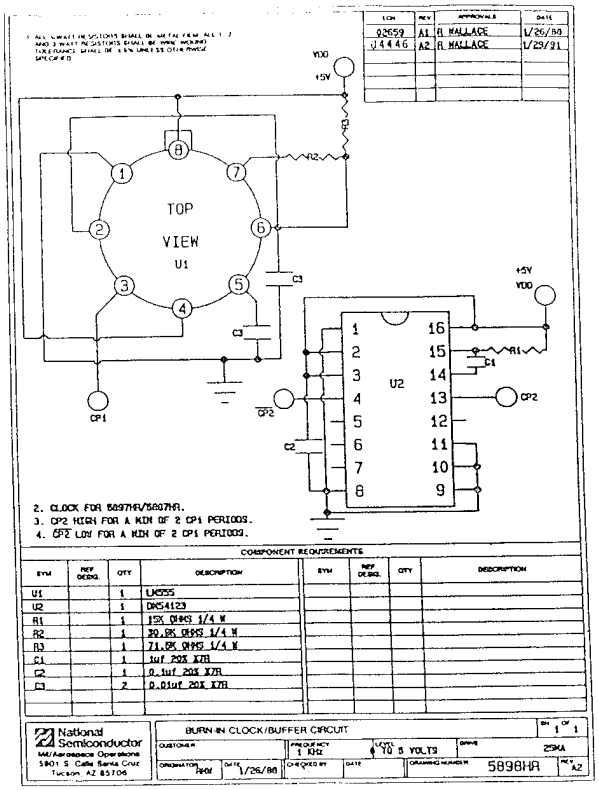


Figure 6.

National Semiconductor

PLASTIC PACKAGE AVAILABILITY
Electrical Test Results On
Temperature Cycle: -65 ~ +150°C For 68L-PLCC

COMPOUNDS	# of units at start	100 Cycles	500 Cycles	1000 Cycles	1500 Cycles	2000 Cycles
ULS12H	36	0/36	0/36	0/36	0/36	12/36
ULS12HX	36	0/36	0/36	0/36	0/36	0/36
X9074	36	0/36	0/36	0/36	0/36	0/36
B24	36	0/36	0/36	0/36	0/36	0/36
Control (ceramic)	25	0/25	0/25	0/25	0/25	0/25

NOTE:
1. The preconditioned vs. non-preconditioned comparison was lost due to the mix-up in the HAST chamber.
2. Each cell represents cumulative number of failed device to the number of sample size at each reatout (# of cum fail / # of total sample size).

National Semiconductor

PLASTIC PACKAGE AVAILABILITY
Electrical Test Results On
Operational Life-Test @125°C For 68L-PLCC

COMPOUNDS	# of units at start		168 Hours		1000 Hours		2000 Hours		3000 Hours		4000 Hours	
	P	NP	P	NP	P	NP	P	NP	P	NP	P	NP
ULS12H	15	15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15
ULS12HX	15	15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15
X9074	15	15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15
B24	15	15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15	0/15
Control (ceramic)	24		0/24		0/24		0/24		0/24		0/24	

NOTE:
1. Each cell represents cumulative number of failed device to the number of sample size at each reatout (# of cum fail / # of total sample size).

National Semiconductor

PLASTIC PACKAGE AVAILABILITY
Electrical Test Results On
Highly Accelerated Stress Test @130°C For 68L-PLCC

The electrical test is currently in progress.

COMPOUNDS	# of units at start		216 Hours		432 Hours		648 Hours		864 Hours		1080 Hours		1296 Hours	
	P	NP	P	NP	P	NP	P	NP	P	NP	P	NP	P	NP
ULS12H	--	20	--	0/20	--	0/20	--	0/20	--	0/20	--	0/20	--	0/20
ULS12HX	20	20	1/20	0/20	2/20	0/20	3/20	0/20	9/20	0/20	9/20	0/20	10/20	0/20
X9074	--	20	--	0/20	--	0/20	--	0/20	--	0/20	--	0/20	--	0/20
B24	20	--	12/20*	--		--		--		--		--		--
Control (ceramic)	22		0/22		0/22		0/22		0/22		0/22		0/22	

NOTE:
1. The shaded cells(*) exhibit test legs with greater than 50% failure, therefore testing was stopped as planned.
2. Each cell represents cumulative number of failed device to the number of sample size at each reatout (# of cum fail / # of total sample size).
3. The ULS12HX, Precon had two devices with missing package lead after 864Hrs.

National Semiconductor

PLASTIC PACKAGE AVAILABILITY
Electrical Test Results On
Highly Accelerated Stress Test @159°C For 68L-PLCC

COMPOUNDS	# of units at start		24 Hours		72 Hours		108 Hours		216 Hours		432 Hours		648 Hours	
	P	NP	P	NP	P	NP	P	NP	P	NP	P	NP	P	NP
ULS12H	21	--	0/21	--	0/21	--	0/21	--	12/21*	--		--		--
ULS12HX	--	21	--	0/21	--	0/21	--	0/21	--	0/21	--	0/21	--	5/21
X9074	21	--	0/21	--	1/21	--	1/21	--	21/21*	--		--		--
B24	21	21	0/21	0/21	11/21*	0/21		0/21		0/21		0/21		4/21
Control (ceramic)	24		0/24		0/24		0/24		0/24		0/24		0/24	

NOTE:
1. The shaded cells(*) exhibit test legs with greater than 50% failure, therefore they were pulled out as planned.
2. Each cell represents cumulative number of failed device to the number of sample size at each reatout (# of cum fail / # of total sample size).
3. The ULS12HX,NoPrecon leg had three devices with missing package lead after 648Hrs.

National Semiconductor

PLASTIC PACKAGE AVAILABILITY
Electrical Test Results On
High Temperature Storage @175°C For 68L-PLCC

COMPOUNDS	# of units at start		216 Hours		432 Hours		1080 Hours		1512 Hours		1944 Hours		2500 Hours		4125 Hours	
	P	NP	P	NP	P	NP	P	NP	P	NP	P	NP	P	NP	P	NP
ULS12H	18	18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18
ULS12HX	18	--	0/18	--	0/18	--	0/18	--	0/18	--	0/18	--	0/18	--	0/18	--
X9074	18	18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18
B24	18	18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18	0/18
Control (ceramic)	45		0/45		0/45		0/45		0/45		0/45		0/45		0/45	

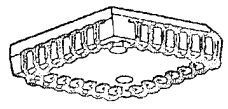
NOTE:
1. Each cell represents cumulative number of failed device to the number of sample size at each reatout (# of cum fail / # of total sample size).

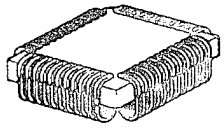
PLASTIC PACKAGE AVAILABILITY PROGRAM

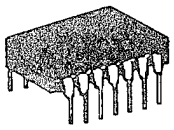
DOW CORNING FINAL REPORT

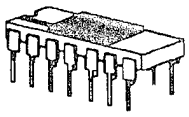
SECTION 5

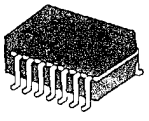
Task 6.0 RWOH Coating of Test Devices (best effort)











DOW CORNING

Plastic Packaging Availability

Final Technical Report

Prepared for:
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Preface

This final technical report describes the results obtained during the Plastic Packaging Availability (PPA) Contract sponsored by the Defense Logistics Agency (DLA) and the Tri-Service Agencies. The overall mission of the PPA program is to assess the advancements in plastic packaging materials (molding compounds) to meet harsh military environments. Dow Corning, under subcontract to National, has focused its efforts on the development of low temperature manufacturing processes for the deposition of advanced inorganic dielectrics that are compatible with semiconductor device fabrication techniques (Section 6.0). These protective coatings have been shown to provide hermetic-like performance in comparative studies. In addition, Dow Corning conducted several of the life tests on the high lead-count (HLC) devices and Sandia test chips, including high temperature HAST and Temperature Cycling (Section 7.0).

Dow Corning personnel under contract support that directly contributed to the results of the PPA contract are:

Clay Bearinger	Reliability Testing
Robert Camilletti	Principal Investigator/Program Manager
Fred Dall	Electrical (Device) Characterization
Diana Deese	Silicon Oxide Deposition Development
Mark Loboda	Technical Ldr, Thin Film Char., PECVD, a-SiC:H
Jeff Seifferly	Silicon Carbide Deposition Development

Dow Corning Corporation, headquartered in Midland, MI, is the global leader in the development, manufacture, and sale of silicon based chemicals and materials. Dow Corning's technical expertise in pre-ceramic polymers and coatings are used to derive advanced thin-film inorganic dielectrics for semiconductor device fabrication and protection.

Robert C. Camilletti
Program Manager

Mark J. Loboda
Sr. Research Specialist

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Executive Summary

In the Plastic Packaging Availability (PPA) Program, sponsored by the Defense Logistics Agency (DLA) and the Tri-Services, an attempt to integrate the dielectric coatings into National Semiconductor Corporation's (National's) existing wafer level processes did not meet the initial engineering screening tests. It was concluded that the dry etch processes used to remove the SiC passivation from the gold coated bond pad regions, severely degraded the non-corroding (gold) bond pad metallization. Not only was the corrosion resistance of the bond pad metallization reduced but also its bondability during subsequent wire bonding and packaging operations. This work was performed on a best effort basis and no further reliability / life tests was performed on these test samples.

A variety of severe and differentiating reliability / life tests were used to assess the performance of plastic encapsulated microcircuits (PEMs) in harsh environments. For this study, a National commercial device, a 68-lead SCX6244UEU CMOS Gate Array and a Sandia National Laboratory (SNL) Test Chip NAT-01 were selected as test vehicles. Comparative reliability tests were performed on devices assembled in plastic leaded chip carriers (PLCC) and in traditional hermetic packages. The reliability testing performed by Dow Corning included temperature cycling from +150 to -65°C, highly accelerated stress test (HAST) at 130°C, 85%RH, 5 volts bias and HAST at 159°C, 85%RH, 5 volts bias. The test methods, problems encountered and the analysis of the NAT-01 test chips will be discussed.

Further advancements have been made in the hermetic-like coating system using molecular designed silicon materials and have been combined in a multilayer structure to produce a "sealed IC chip" using wafer level processing. The optimization of this process technology is currently underway in an Air Force Wright Laboratory development program called, "ChipSeal™ Inorganic Coating Technology", teaming Dow Corning, the David Sarnoff Research Center (Sarnoff) and the Advanced Packaging Group at the Microelectronics Center of North Carolina (MCNC). Functional "ChipSealed" devices, with hermetic coatings and high-rel metal bond pads, have been fabricated with high yields. Reliability testing is underway.

Introduction

Compact, portable electronics demand the lowest cost solutions for achieving smaller, lighter, and faster systems with built-in reliability. Due to the declining military budget, changes in government procurement to reduce cost has necessitated the need to convert from hermetic packaged devices to "best commercial practice" plastic packages. Advantages in size, weight, and circuit performance is also realized from this packaging conversion in addition to the governments access to a larger variety of microcircuits. The reliability of these devices, including SOIC, TSOP, PQFP, and other surface mount technologies (SMT), in the harsh military environment has not been adequately addressed. New epoxy molding compounds are being developed to improve the device reliability except that these materials have intrinsic moisture permeability limitations. Their further development is focused at the use of high purity resins, the addition of ion getters, and improving the adhesion of the molding compound to the die and leadframe assembly materials. Polyimide and silicone gel die coats are being integrated into the hermetic to plastic conversion process for stress buffers on large area die. However, these interim approaches are quite costly and do not address the intrinsic material incompatibility problems. Silicone gels have been shown to provide one of the best levels of circuit reliability under severe environmental exposures in numerous studies. An alternate approach of supplying an environmentally sealed chip using inorganic thin-films after wire bonding was developed and demonstrated [1,2,]. An advancement of this technology for depositing inorganic thin-films at the wafer level which can be integrated into any commercial plastic packaging operation is proposed. This robust sealed chip is anticipated to be a cost effective, long term solution for supplying reliable IC die for a variety of system and packaging applications.

Thin film dielectrics have been developed which can be applied during IC fabrication to provide the level of protection required for single chip and multichip applications. The inorganic dielectric thin-film technology acts as a state-of-the-art passivation system. The passivation system is comprised of first, a polymer-based, silicon oxide material which planarizes the IC surface. Smoothing the surface prevents the formation of voids and defects in subsequent passivation layers which easily form at severe changes in the surface topography. The second step is the deposition of a hard, chemically inert, amorphous hydrogenated silicon carbide (a-SiC:H) film which seals the device from mechanical damage and contamination. This passivation scheme is the wafer level adaptation of the thin film protective coating technology applied at assembly level to Si and GaAs ICs. Significant improvement in device reliability was achieved [3]. This paper will review the use these silicon based materials for device passivation and report film properties and reliability data pertinent to the fabrication and protection of semiconductor devices.

Background

The feasibility of using an advanced thin-film passivation technology directly on silicon and gallium arsenide circuits was first studied under ARPA sponsorship [4]. This concept, originated by Dow Corning Corporation, was first known as the SPEC concept (Surface Protected Electronic Circuits). The feasibility study showed that the inorganic dielectric coatings (ceramic coatings) clearly demonstrated protection of the circuits when exposed to autoclave, HAST (highly accelerated stress testing), and salt fog exposures without affecting the functions of the silicon or gallium arsenide test devices.

The material and process technologies used for depositing protective, submicron thick, silicon oxide and hydrogenated silicon carbide films were developed and demonstrated in the completed Wright Laboratory Manufacturing Technology Program, Reliability Without Hermeticity for Integrated Circuits (RWOH) [5]. Under contract F33615-90-C-5009, Dow Corning, was teamed with the advanced packaging group of National Semiconductor Corporation (prime). Dow Corning had merged the inorganic dielectric thin-films with standard plastic packaging processes. The hermetic-like coating system was applied to die on chip carriers which were subsequently encapsulated in plastic. Testing of these devices demonstrated that with the incorporation of the hermetic-like coating system, the reliability of plastic packaged devices could approach that of hermetic ceramic packaged devices [6]. But application of the hermetic-like coatings at this "assembly level" is slow, performance limited by contamination resulting from handling in early assembly steps and likely to be costly. The goal of the current Wright Laboratory program "ChipSeal™ Inorganic Coating Technology", is to overcome the assembly level limitations by integration of the hermetic-like coating process with the device fabrication process [7]. Recent advances in barrier metal and gold metallization technology provide a route to the formation of high reliability electrical interconnections directly on the semiconductor circuit. This combination of the hermetic-like passivation with a noble metal contact forms a complete protective package that protects the chip similar to assembly as though

it was assembled in a hermetic package. Its use provides the industry with the flexibility to use the hermetic-like die in a large spectrum of mounting formats. These range from single-chip packages to multi-chip packaging.

SUBSECTION 1.0
RWOH Coating of Test Devices

Processes were developed for depositing the silicon oxide and plasma-SiC films on 150 mm wafers and were used for coating live device wafers, SCX6244UEU CMOS Gate arrays. The silicon oxide layer was deposited using FOx-15 precursor on a SEMIX automatic spin coater and cured for 1 hour at 350°C in N_2/H_2; the film thickness was 5700Å, >99% uniformity. The plasma-SiC layer was deposited using trimethylsilane (3MS) precursor at 13.56 MHz, 1.9 torr, 125 Watt, and 300°C (substrate) by PECVD; the film thickness was 5500Å, >97% uniformity. The live device wafers were optically inspected to 1000X using Nomarski and dark field assessment techniques with no signs of cracking or other film anomalies. Figure 1 shows a cross-sectional photomicrograph of a processed wafer. The coated live device wafers were returned to National for patterning, etch and packaging.

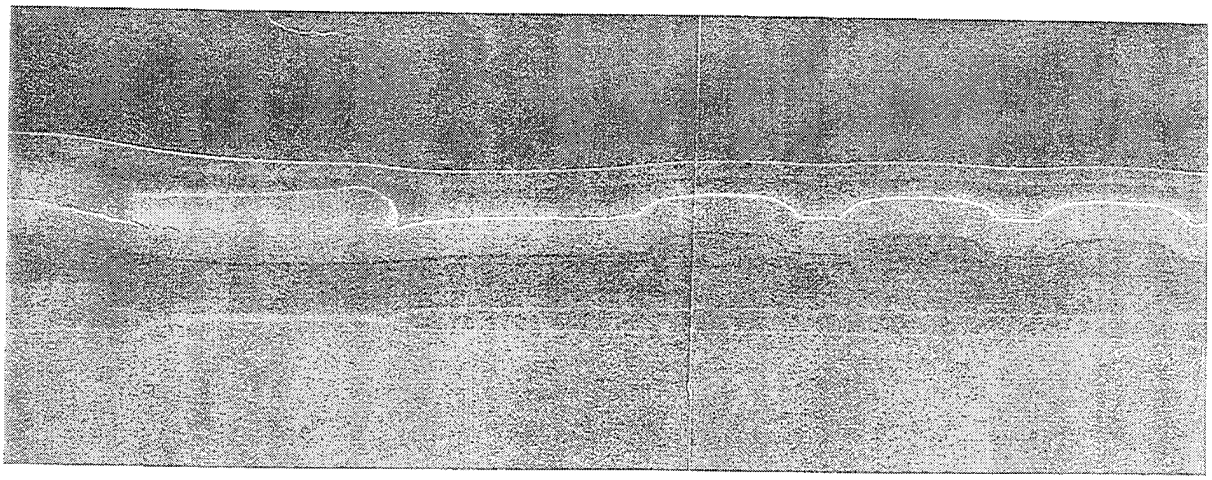


Figure 1. Cross-sectional photomicrograph showing the sealing qualities and coverage of the silicon oxide and silicon carbide thin films (5000X).

National reported a lower than expected yield of the coated wafers from both wafer probe in Santa Clara and packaged devices in Singapore. In both cases, it was believed that complete removal of the oxide/carbide films was not achieved during the final pad etch (performed by reactive ion etching, RIE) by National. SEM cross-sections provided by National confirmed the presence of a foreign film on the bond pads. Analytical data derived from Fourier Transform Infrared Spectroscopy (FTIR) and Auger Electron Spectroscopy (AES) revealed that the foreign film (or residue) does not contain any Si containing species (Si-H or Si-O) bands suggesting that the residue is a hydrocarbon polymer and not incomplete removal of the silicon oxide/carbide dielectric films as first suspected. These results also revealed that the National metallization is no longer intact; most of the gold is missing and the remainder has intermixed with the Ni alloy layer. These bond pad conditions are the causes for the lower yield and packaging problems since adequate electrical contact to the bond pad interconnect could not be made.

In addition, initial engineering evaluations were performed on sample die using the salt fog test in accordance with MIL-STD-883 M1009.8. Figures 2 and 3 shows the extensive bond pad corrosion and surface metal (trace) corrosion underneath National's passivation layer after 4 hours of salt fog exposure. Based on these

results, it is clear that the reliability of these devices have been compromised and no further reliability / life tests was performed on these test samples.

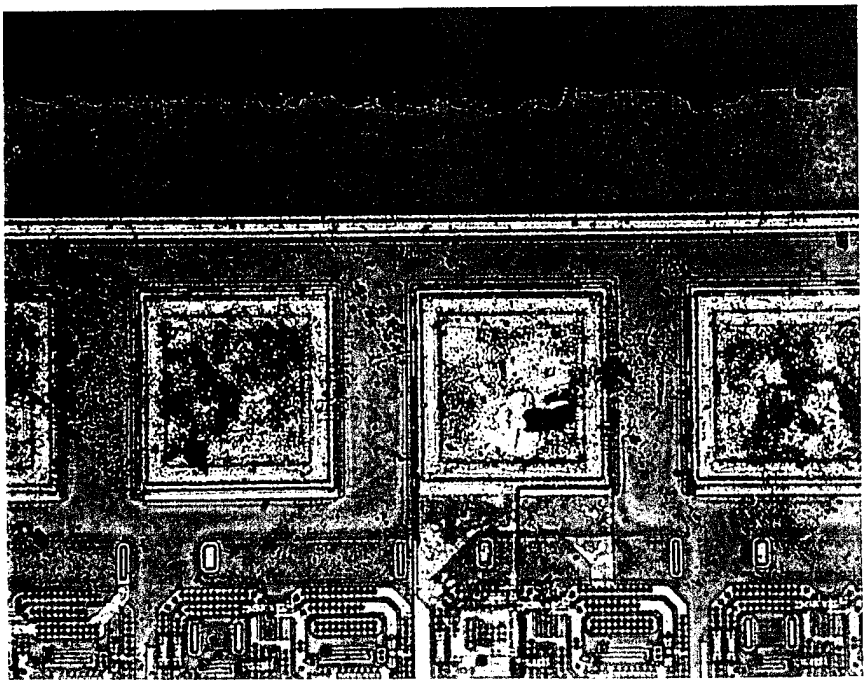


Figure 2. Appearance of the bond pad region after 4 hours of salt fog exposure.

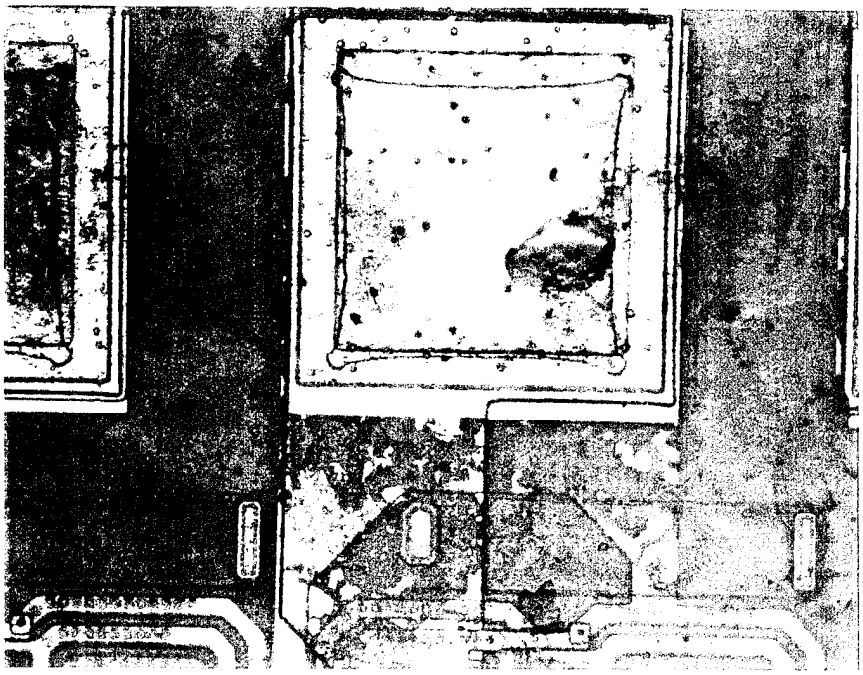


Figure 3. Appearance of the bond pad region after 4 hours of salt fog exposure.

SUBSECTION 2.0
Device Reliability Testing

A variety of severe and differentiating reliability / life tests were used to assess the performance of plastic encapsulated microcircuits (PEMs) in harsh environments. For this study, a National commercial device, a 68-lead SCX6244UEU CMOS Gate Array and a Sandia National Laboratory (SNL) Test Chip NAT-01 were selected as test vehicles. Comparative reliability tests were performed on devices assembled in plastic leaded chip carriers (PLCC) and in traditional hermetic packages. The reliability testing, performed by Dow Corning, included temperature cycling per MIL-STD-883 Method 1010.7, test condition C (+150 to -65°C) in 1 hour cycles, highly accelerated stress test (HAST) per JEDEC-STD 22B Method A110 at 130 ±2 °C, 85%RH, 5 volts bias and HAST per JEDEC-STD 22B Method A110 at 157 ±2 °C, 85%RH, 5 volts bias [8,9].

The temperature cycling test was performed using a Thermotron Model ATS-195V-5-5-LN2 vertical, air to air thermal shock unit with at working temperature range of -73 to +200 °C. The purpose of this test is to assess the material compatibility and resistance of a component to alternate accelerated exposures of high and low temperatures. Cracking, separation and eventual breakage of the die, interconnect, and package are typical failure mechanisms. This test is best used when a salt fog exposure is performed immediately thereafter to assess the integrity of the plastic to leadframe interface. The temperature recovery time for this unit, using a standard 1 lb piece of steel was 5 minutes. Annual calibration of the chamber temperature was within 1 °C in the hot zone at 150 °C and 2 °C in the cold zone at -65 °C.

The HAST or pressure, temperature, humidity, bias (PTHB) test was performed using an Express Test Model HAST-1000 horizontal, variable humidity, dual vessel steam generator unit with a working temperature range of 100-160 °C. The purpose of this test is to highly accelerate the unsaturated humidity testing of integrated circuits for process control and reliability assessment at a fraction of the time compared to using conventional humidity test equipment (85 °C/85 %RH). Corrosion of biased metallization affecting the DC parameters from either moisture penetration and/or mobile ions are typical die related failure mechanisms. A 15 point data acquisition system was incorporated into the chamber to provide an accurate on-line monitoring / profiling of the test chamber during operation. Figure 4 illustrates the locations of the thermocouples in the HAST chamber. The supply water used in the HAST chamber was 18 Meg-ohm DI water.

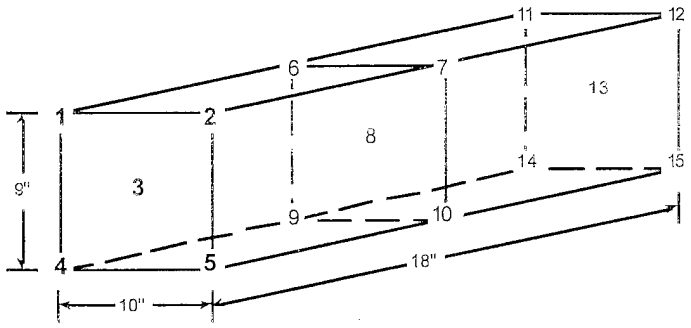


Figure 4. HAST thermocouple locations for on-line monitoring

Initial supply problems of the HAST boards and associated resistors / capacitors plagued the start-up of the reliability testing. Although ceramic discrete components were specified for the board construction, plastic coated devices were assembled by the supplier (Trio Tech) which subsequently melted together, shorted, and became unusable during a 24 hour dry run at 159°C, 85% RH. Replacement ceramic discrete components were procured and used for the actual HAST reliability testing. In addition, the sockets used to bias the PQFP also shrunk slightly after the first 24 hour run through the HAST exposure. Both the original discretes and the sockets are reported to resist prolong autoclave conditions (121 °C, 100%RH) and high temperatures (200 °C). However, having both conditions at lower exposure limits simultaneously can produced disastrous results. Figures 5, 6, and 7 show layout and construction of the HAST boards.

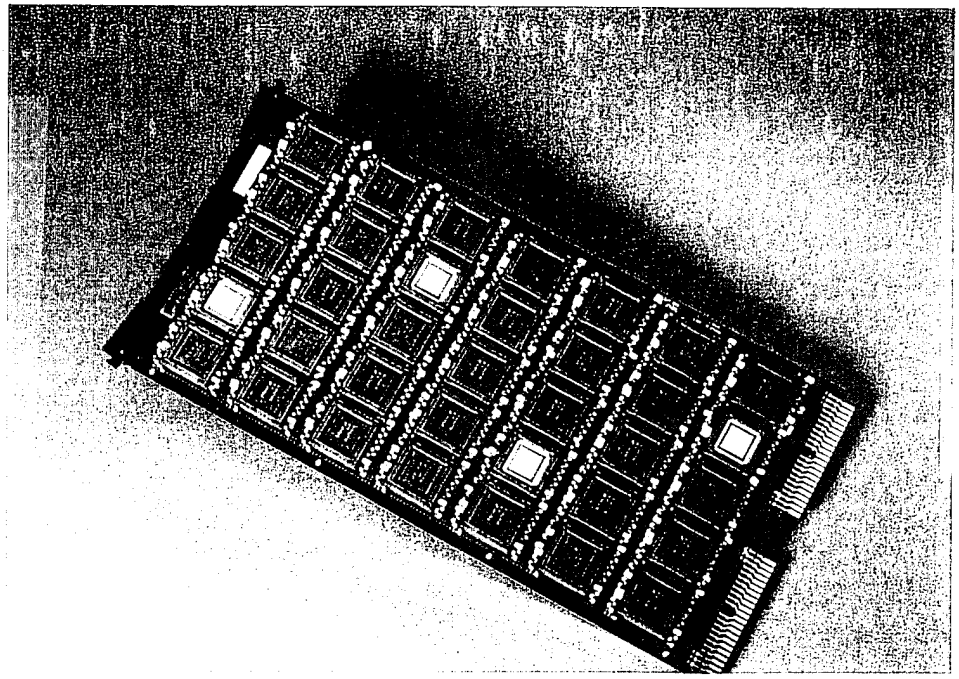


Figure 5. A photograph showing an assembled HAST board.

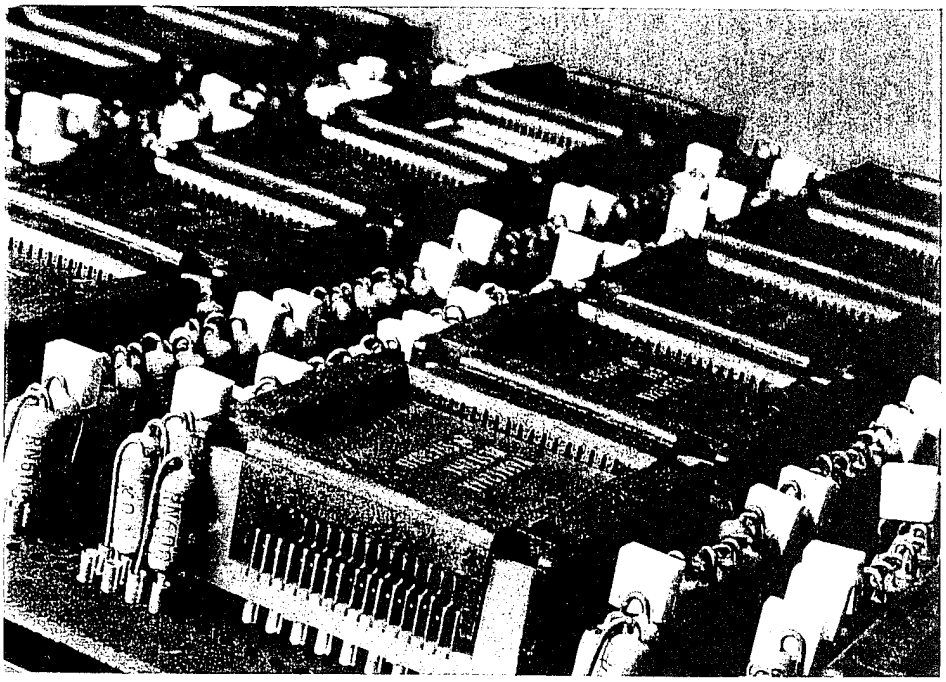


Figure 6. A close-up photograph showing the socket and discrete components of an assembled HAST board.

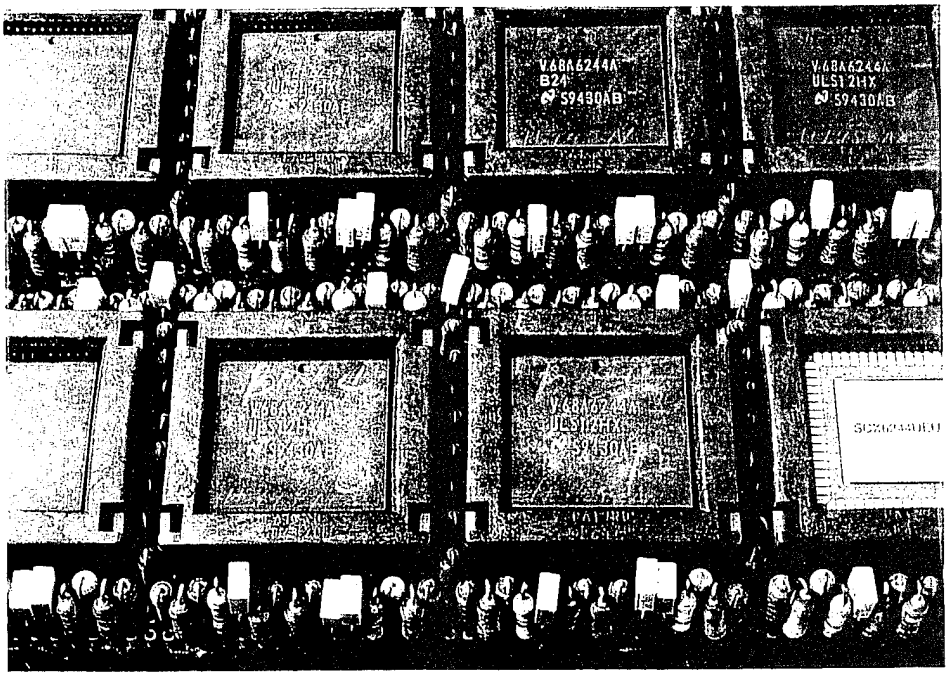


Figure 7. A close-up view showing the component density of an assembled HAST board.

The temperature data is recorded for each operation of the HAST system. The typical temperature variance in the chamber was 2 °C. A representative plot illustrating the average temperature exposure for both the 130 °C and 157°C conditions are shown in Figures 8 and 9 respectively.

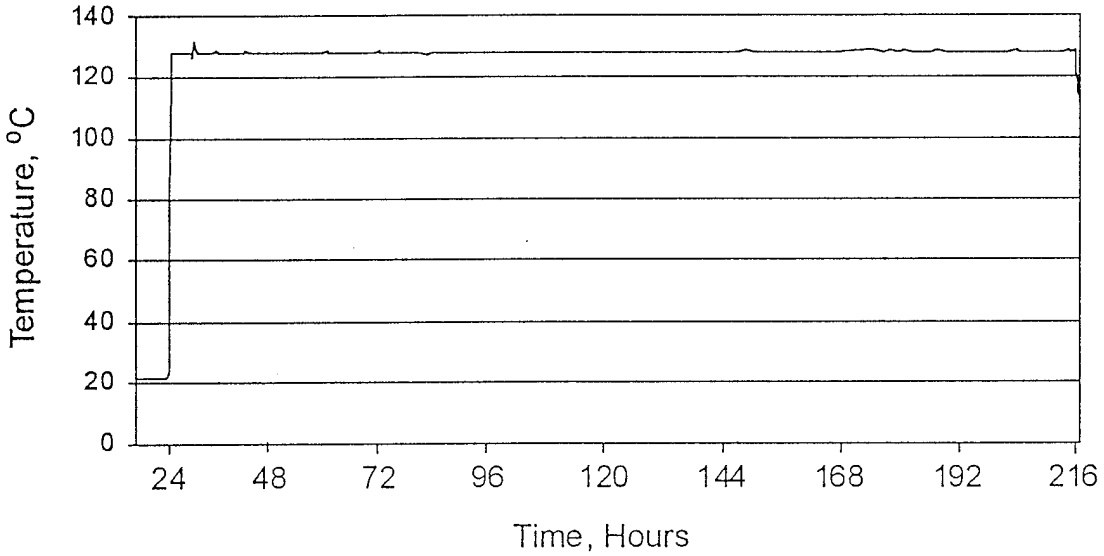


Figure 8. A typical average temperature plot of a 130 °C HAST condition during the PPA reliability testing. The typical temperature variance in the chamber was 2 °C.

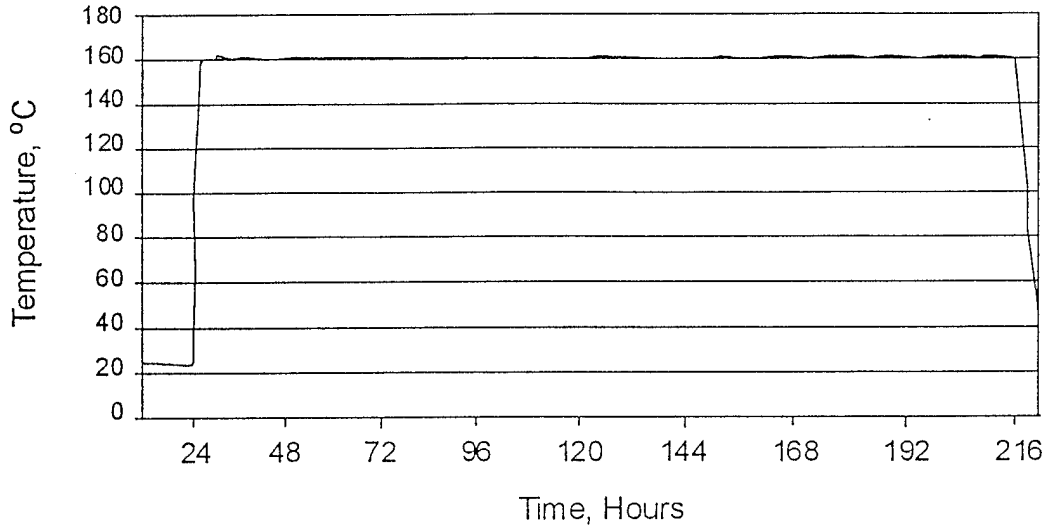


Figure 9. A typical temperature plot of a 159 °C HAST condition during the PPA reliability testing. The typical temperature variance in the chamber was 2 °C.

Both the National SCX6244UEU CMOS gate array devices and the Sandia test chip NAT-01 were exposed to the HAST conditions within the same test run. The interim device electrical tests were performed by National and the performance results, derived from the electrical testing, may be found in National's report. The interim electrical tests and its subsequent analysis for the NAT-01 test chips were performed by Dow Corning and are discussed below.

SNL Test Devices NAT-01

The Sandia National Laboratory Test Chip, NAT-01 has four separate sections: a capacitive moisture sensor which was divided into two parts, one with no passivation and one with a phosphorosilicate glass (PSG) passivation; and a section of triple tracks which was also divided into an area with passivation and one with no passivation. The triple-track areas were for corrosion measurements which consisted of resistance measurements of each line. The triple-tracks were alternately biased with the center leads positive. The bias on all devices was 5 volts DC.

A test procedure and fixture was developed for the SNL NAT-01 test devices so that measurements could be taken easily using the HP4194 analyzer and a resistance meter. Initial measurements were made on 12 test devices to be used in the first tests. Due to HAST equipment malfunctions during the preliminary study of the Sandia test chips, a total cumulative exposure of 35 hours was completed prior to a prolonged down time (for chamber repair).

The unpassivated moisture sensor showed increased capacitance and conductance with prolonged exposure; due to the diffusion of moisture or ions from the package into the sensor. The passivated sensors only showed a higher conductance. The devices were baked to return them to the pre-test condition but only the unpassivated showed reversible behavior. Both passivated and unpassivated sensors showed scattered results. The unpassivated sensors seemed more reliable than the passivated ones. Triple track results showed no change of track resistance on all passivated structures for the total 35 hour exposure. All except the unpassivated ULS12HX showed changes over the time exposure. These data may be found in Appendix A for further review.

Additional measurements were made on a second group of NAT-01 test devices which were tested in parallel with the SCX6244UEU CMOS gate arrays. Prior work by SNL indicated that the sensors should reach moisture saturation in about 7 hours and show a rise in capacitance of about 25% at saturation. The NAT-01 test devices were exposed to HAST conditions for the time periods indicated and then stored in dry nitrogen between successive exposures for periods of 1 to 6 weeks depending on the necessary HAST maintenance or interim RT electrical testing of the CMOS Gate arrays. The sensors were tested within 4 hours of being removed from the HAST condition; this would put the values for the measured capacitance within 60% of the saturation value of the sensors. The tabulated data may be found in Appendix B.

HAST @ 157 °C & 85% RH

The capacitance readings were quite erratic and are therefore shown on a log scale in Figures 10 and 12. We estimate an average 25% rise in capacitance, which translates for measurements of about 20 pF (Log 20 = 1.3) to a rise 5 pF (Log 25 = 1.40). The conductance readings, shown graphically in Figures 11 and 13 were similar in nature; the unpassivated sensors seemed to be less erratic than the passivated sensors.

The triple-track corrosion sensors, shown in Figures 14 and 15, revealed more information. The track resistances decayed to opens very rapidly (most of the unpassivated ones within the first 24 hours). The highest rate of failure was the X9074.07 molding compounds in both the unpassivated and passivated cases. The B24 and the ULS12H-X compounds showed the slowest rate of failure.

HAST @ 130 °C & 85% RH

The capacitance values, shown graphically in Figures 16 and 18, were much more stable than in the 157°C HAST. Most devices exhibited little or no change as a result of the test. The ULS12H-X and the X9074.07 compounds were the most erratic (unstable) in the passivated section; there were some large changes from the unexposed values, such as the ULS12H unpassivated material which could be attributed to flaws in the sensor or holes in the passivation. The conductance values, shown graphically in Figures 17 and 19, showed similar behavior.

The triple-track measurements, shown graphically in Figures 20 and 21, of the unpassivated sensors rapidly decayed to opens within the first test interval (216 Hrs.). The passivated sensors with the X9074.07 and the ULS12H-X compounds had the highest failure rates.

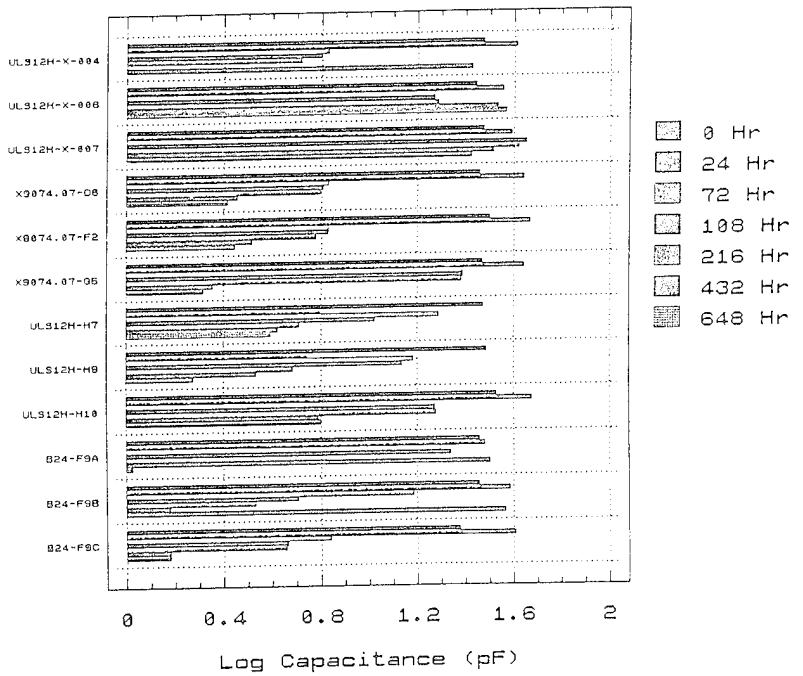


Figure 10. Cumulative capacitance measurements of MSI unpassivated moisture sensors after 157 °C HAST exposure.

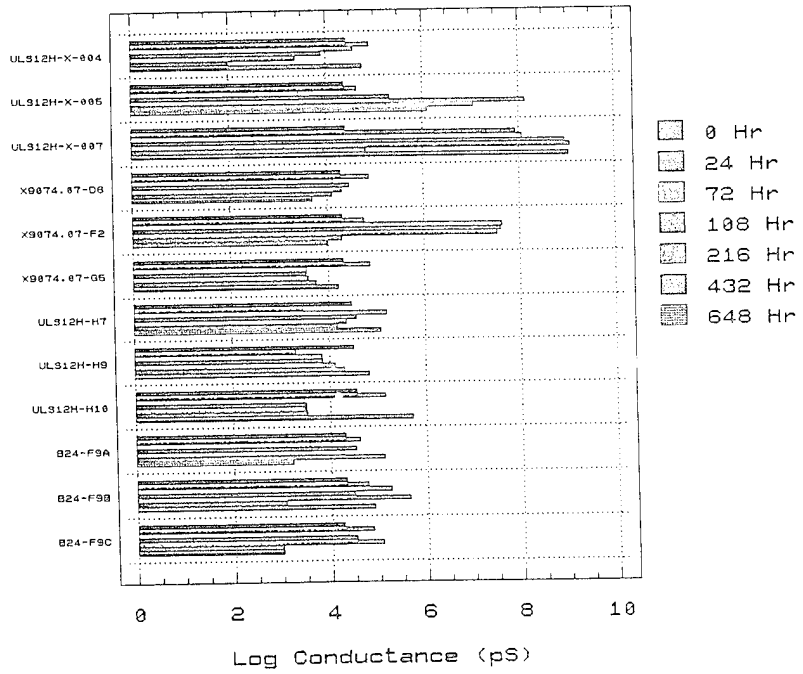


Figure 11. Cumulative conductance measurements of MSI unpassivated moisture sensors after 157 °C HAST exposure.

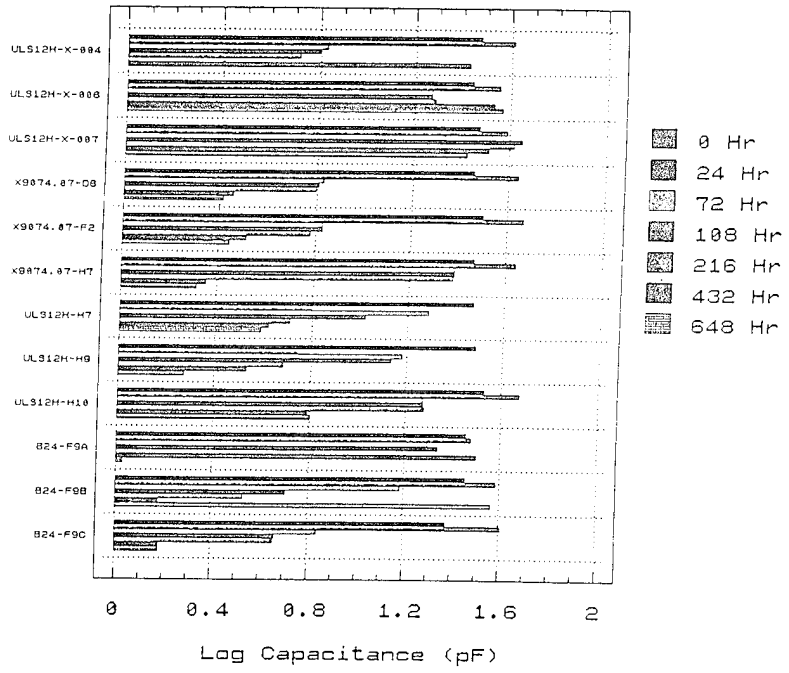


Figure 12. Cumulative capacitance measurements of MSIP passivated moisture sensors after 157 °C HAST exposure.

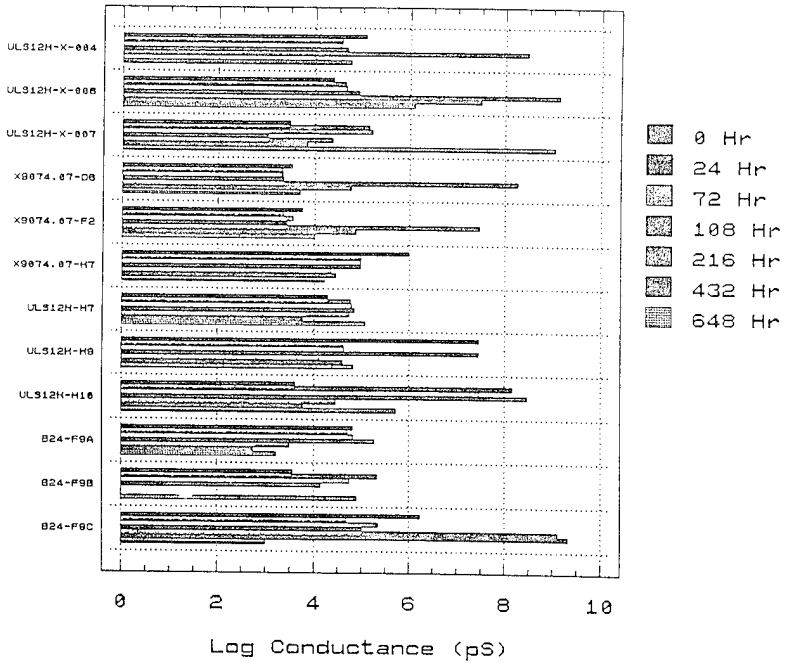


Figure 13. Cumulative conductance measurements of MSIP passivated moisture sensors after 157 °C HAST exposure.

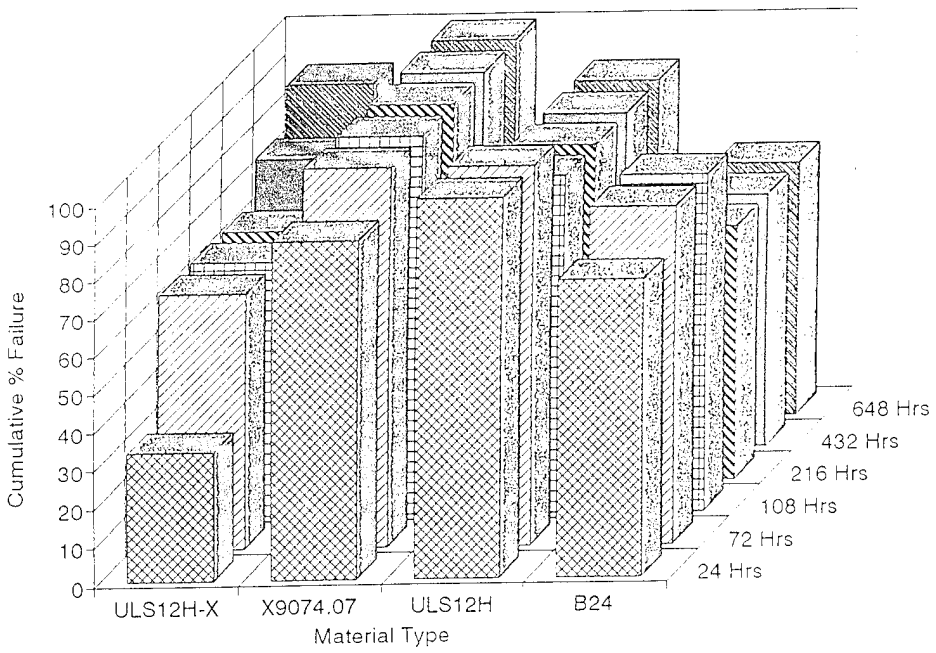


Figure 14. Cumulative resistance failures of unpassivated triple tracks after 157 °C HAST exposure.

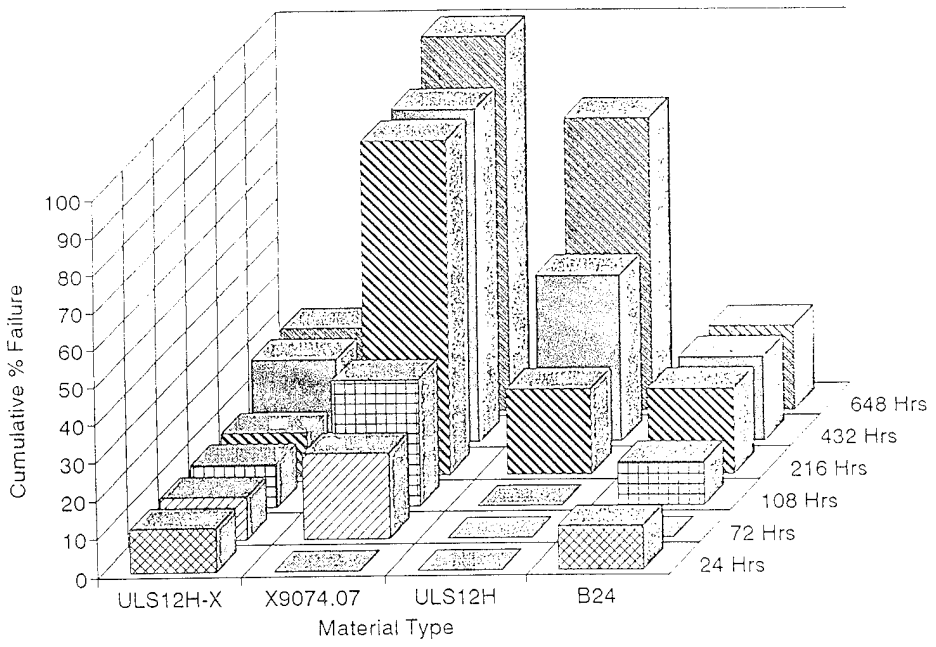


Figure 15. Cumulative resistance failures of passivated triple tracks after 157 °C HAST exposure.

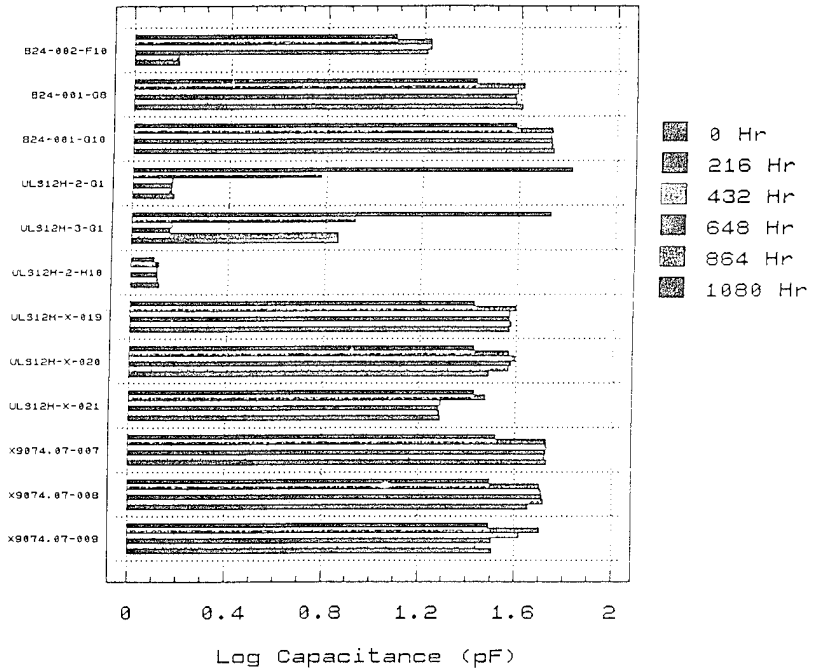


Figure 16. Cumulative capacitance measurements of MSI unpassivated moisture sensors after 130 °C HAST exposure.

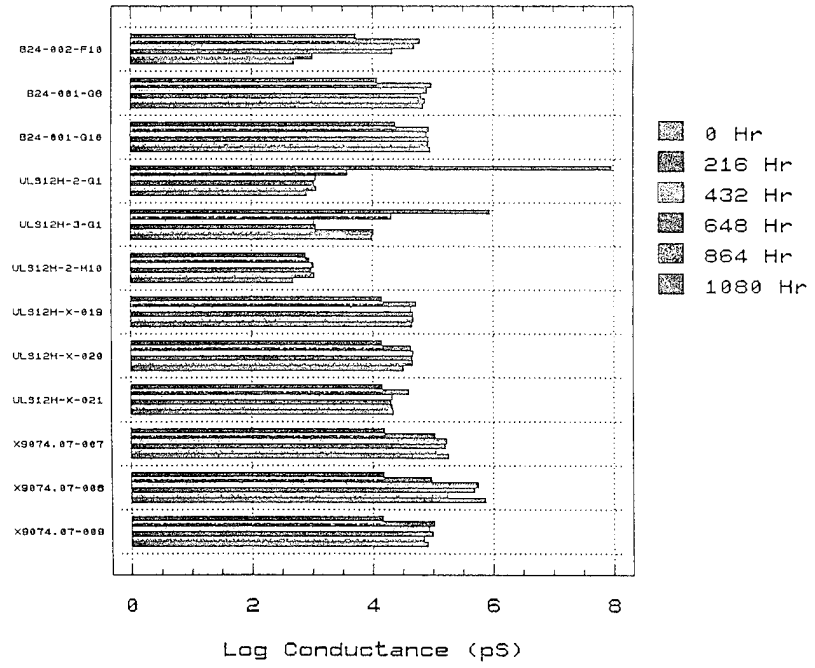


Figure 17. Cumulative conductance measurements of MSI unpassivated moisture sensors after 130 °C HAST exposure.

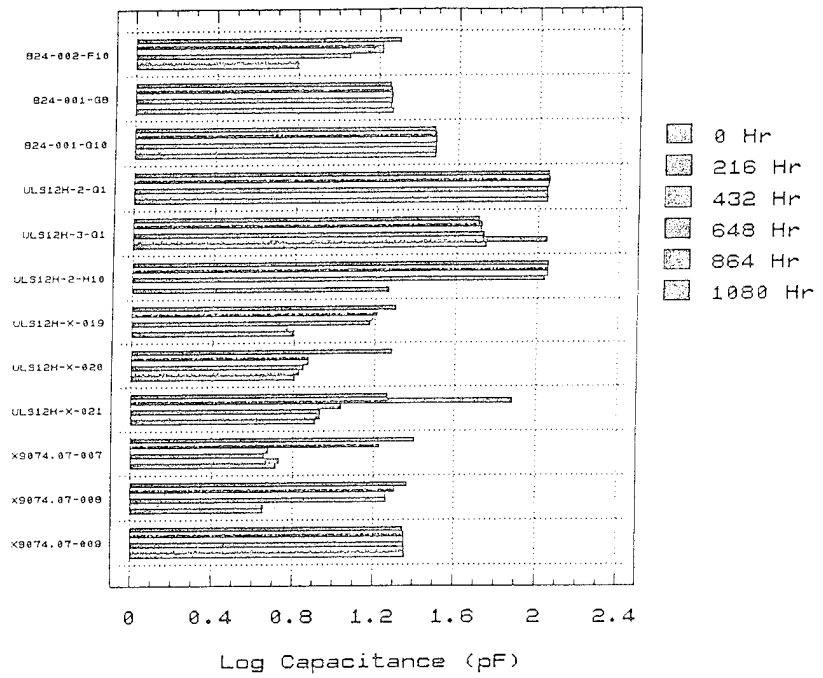


Figure 18. Cumulative capacitance measurements of MSIP passivated moisture sensors after 130 °C HAST exposure.

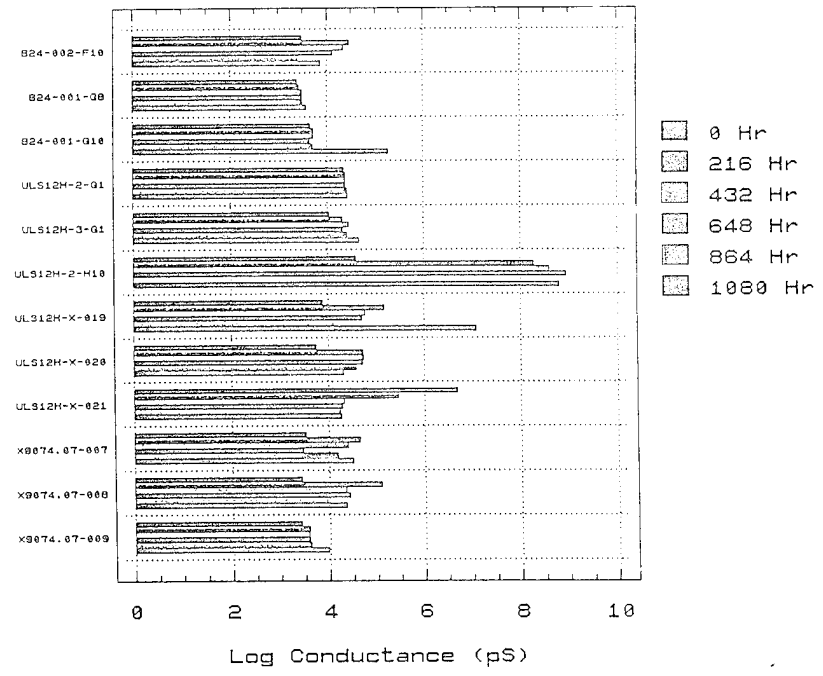


Figure 19. Cumulative conductance measurements of MSIP passivated moisture sensors after 130 °C HAST exposure.

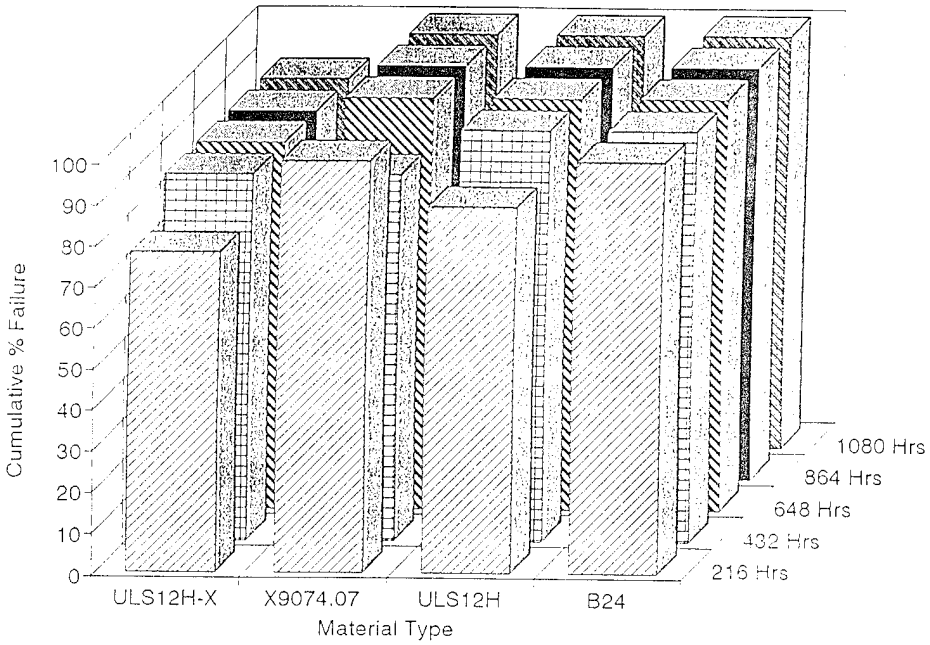


Figure 20. Cumulative resistance failures of unpassivated triple tracks after 130 °C HAST exposure.

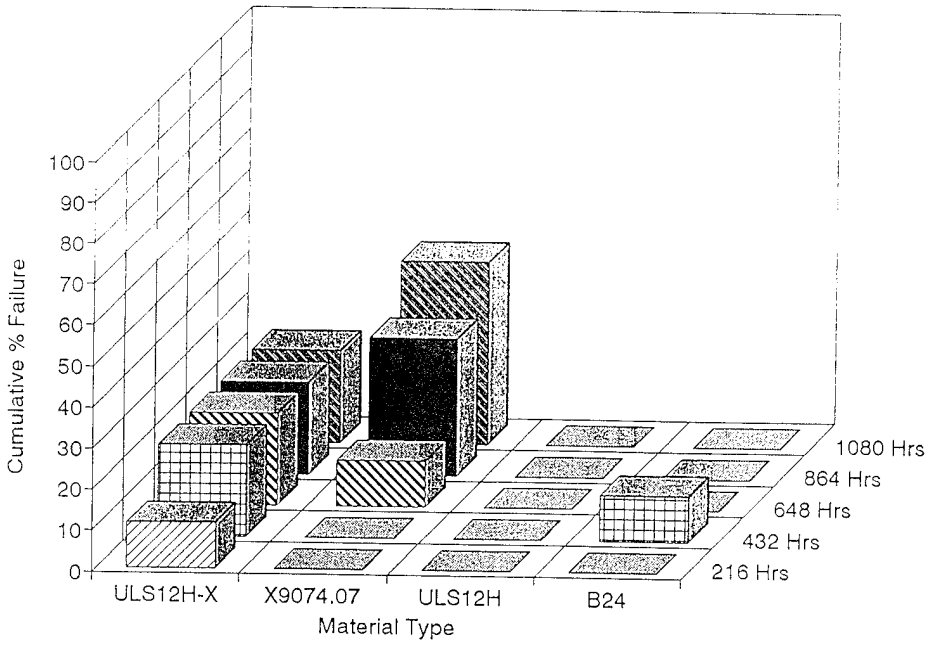


Figure 21. Cumulative resistance failures of passivated triple tracks after 130 °C HAST exposure.

Further advancements have been made in the hermetic-like coating system using molecular designed silicon materials and have been combined in a multilayer structure to produce a "sealed IC chip" using wafer level processing [7]. The optimization of this process technology is currently underway in an Air Force Wright Laboratory development program called, "ChipSeal™ Inorganic Coating Technology", teaming Dow Corning, the David Sarnoff Research Center (Sarnoff) and the Advanced Packaging Group at the Microelectronics Center of North Carolina (MCNC). Functional "ChipSealed" devices, with hermetic coatings and high-rel metal bond pads, have been fabricated with high yields. Figure 22 shows a schematic cross-section of a contact on a "hermetic-like" IC. The smoothing and sealing of the surface topography can be observed near the edge of the bond pad region. This characteristic is routinely acheived during processing. Reliability testing is underway.

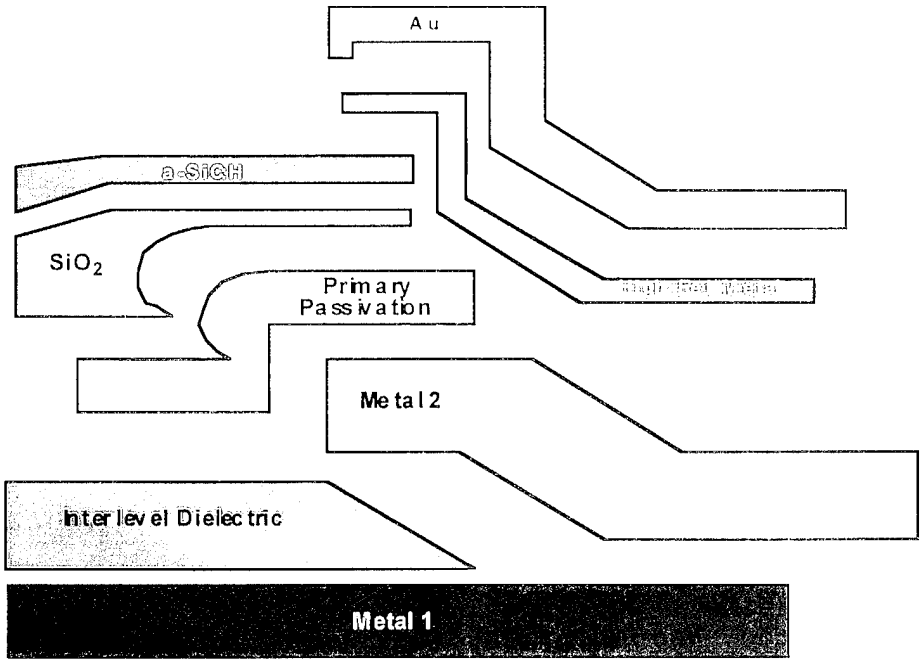


Figure 22. A Cross-sectional Illustration of a Hermetic-Like Sealed IC fabricated under an Air Force Wright Laboratory sponsored program called, "ChipSeal™ Inorganic Coating Technology".

This combination of the hermetic-like passivation with a noble metal contact forms a complete protective package that protects the chip as though it was assembled in a hermetic package. This device is fully compatible with all electrical test and interconnect technology. The use of the thin-film protection technology described, enables the semiconductor manufacturing community to supply low cost, high volume robust devices for military and commercial systems.

Program Conclusions

The objectives of the program were to investigate contemporary plastic molding compound technologies and assess their use in military systems through rigorous reliability testing. The initial attempt to integrate the SiC passivation system into National's processes did not meet minimum engineering screening tests due to unexpected bond pad degradation from the dry etch process.

Acknowledgement:
The authors gratefully acknowlegde the support and efforts of USAF Wright Laboratory, ARPA and the DoD.

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[8] Mil-Std-883D, Test Methods and Procedures for Microelectronics (1991).

[9] JEDEC Standard No. JESD-22.

Glossary of Terms

AES	Auger Electron Spectroscopy
ARPA	Advanced Research Program Office
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
DoD	Department of Defense
DI	Deionized water
DLA	Defense Logistics Agency
FOx®	Flowable Oxide
FTIR	Fourier Transform Infrared Spectroscopy
GaAs	Galliium Arsenide
HAST	Highly Accelerated Stress Test
IC	Integrated Circuit
JEDEC	Joint Electronic Device Engineering Council
MCM	MultiChip Module
Ni	Nickel
PECVD	Plasma Enhanced Chemical Vapor Deposition
PEM	Plastic encapsulated microcircuit
PLCC	Plastic Leaded Chip Carrier
PQFP	Plastic Quad Flat Pack
PPA	Plastic Packaging Availability
RH	Relative Humidity
RIE	Reactive Ion Etch
RT	Room Temperature
RWOH	Reliability WithOut Hermeticity
SEM	Scanning Electron Microscope
Si	Silicon
SiC	Silicon Carbide
SMT	Surface Mount Technology
SOIC	Small Outline Integrated Circuit
SPEC	Surface Protected Electronic Circuits
TSOP	Thin Small Outline Package
WL	Wright Laboratory

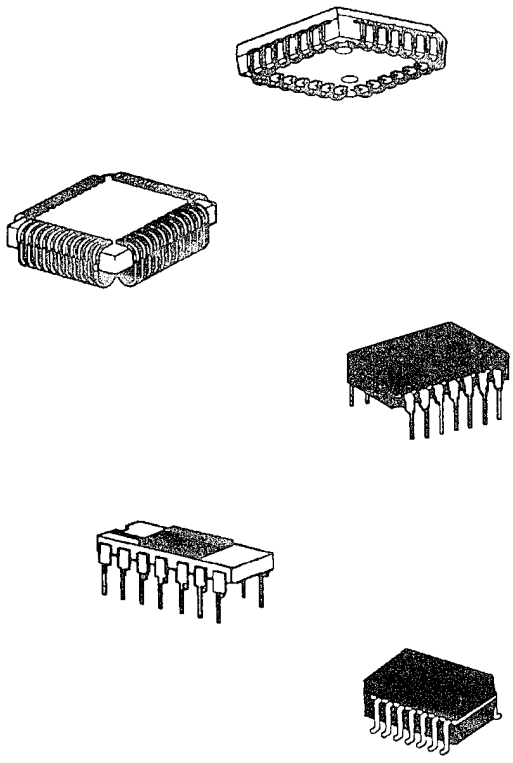
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PLASTIC PACKAGE AVAILABILITY PROGRAM

CRANE FINAL REPORT

SECTION 6

Task 7.0 Device Reliability Testing



PLASTIC PACKAGE AVAILABILITY PROGRAM

"Low Lead Count Environmental Testing"

DEPARTMENT OF THE NAVY
NAVAL SURFACE WARFARE CENTER
CRANE DIVISION
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Low lead Count Environmental Testing

Introduction

Two part types were tested for the DLA Plastic Package Availability (PPA) Program, the LM124 14 pin Quad Op Amp and the SCX 6244 68 pin ASIC device. This section will discuss the low lead count LM124 device environmental testing and the test results. These tests are part of Task 7, Reliability Testing, of the PPA Program, and were conducted at the Naval Surface Warfare Center, Crane Division, Crane, Indiana, Dan Quearry Task Manager. Figures 1 and 2 show the flow diagram of the design of experiments for the environmental testing on the LM124. The Highly Accelerated Stress Test (HAST) tests were performed at two temperatures, 130 degrees C and 159 degrees C at 85% Relative Humidity (RH). Temperature Cycling (TC) was done at -65 degrees C to +150 degrees C. High Temperature Storage (HTS) was performed at 175 degrees C. The Op Life test shown in Figure 2 was originally included in the design of experiments but was dropped because of lack of available test time and limited resources. It was also felt that not much would be gained from the Op Life testing on these components as they are mature product manufactured on a high volume line. The dye penetrant tests were performed at Rome Lab and the test results are discussed in another section. The failure analysis work was performed at National Semiconductor and will also be discussed in another section of this report.

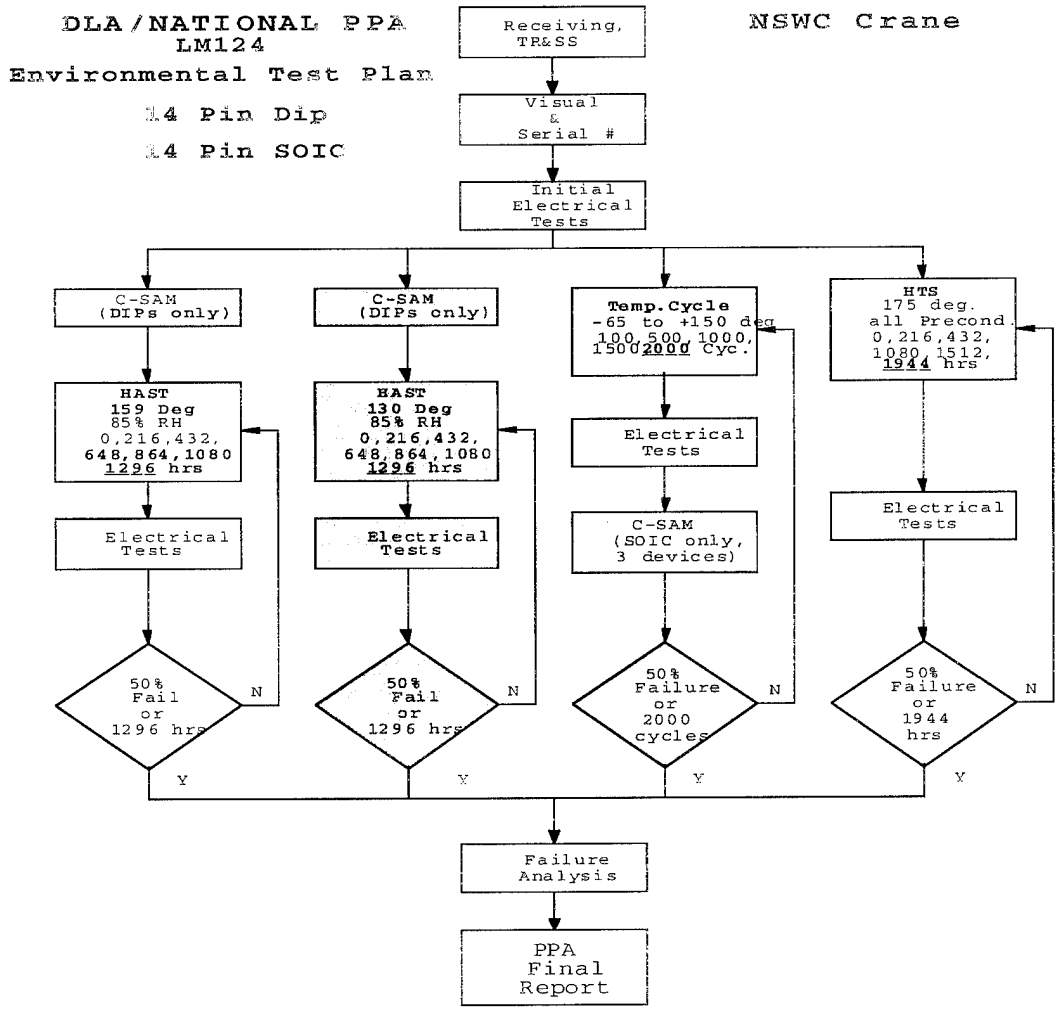


Figure 1

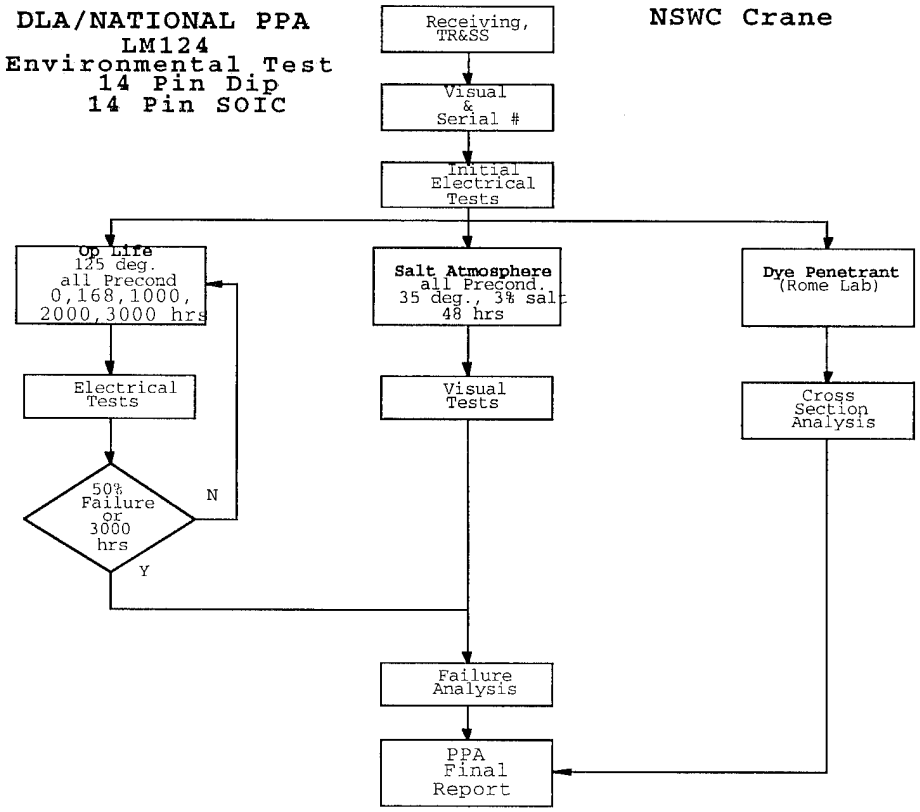


Figure 2

For the low lead count design of experiment two package types were tested, a 14 pin DIP and a 14 pin wide body SOIC. Four epoxy molding compounds (EMC) were used and tested, one specific to DIP packages, one specific to SOIC packages and two used in both the DIP and SOIC package. These EMCs were the Plaskon standard 3400, Plaskon 3400x enhanced (reduced contaminates and ion getters added), National Semiconductor's B14 (used for SOIC packages), and National's B8 (used for DIP packages). The 14 pin SOIC package was tested under two different conditions, VCC of 5 volts and 30 volts, the 30 volts VCC is within the device's rated operating range. The 14 pin DIP package style was tested with two different conditions, preconditioning and non-preconditioning.

An experimental control lot of LM124 ceramic packaged devices was included in each environmental test series, HAST, Temperature Cycling, High Temp. Storage, and Salt Fog. Also three devices with only the Sandia Sensor chip were included in each of the test legs of the HAST testing. These devices were packaged with the same EMC, same package styles and were manufactured under the same conditions as the test devices. The test results from the Sandia Sensor chips will be discussed in another section of this report.

All the plastic encapsulated microcircuits were molded at the overseas facilities that normally produce high volume commercial components for National Semiconductor. A team from National Semiconductor, Santa Clara, and Rome Lab visited the facilities and monitored the manufacturing processes. All components were visually inspected, serialized, and electrically tested to MIL Spec. standards before environmental testing began. Figure 3 shows the individual design of experiments test flow for the 130 degree C HAST test.

The scanning acoustic microscopy was used to take a C-SAM picture of all the HAST DIP devices and all the temperature cycling DIP and SOIC devices before environmental testing and then after failures.

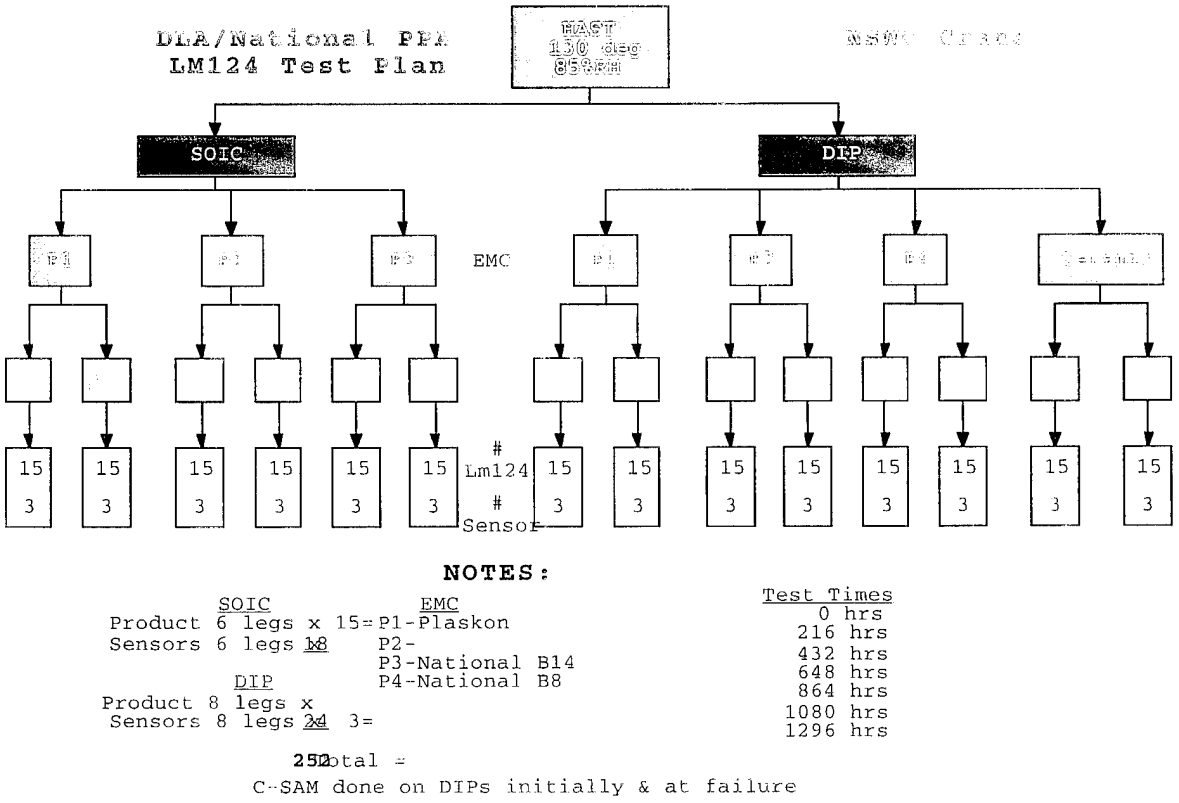


Figure 3

HAST - 130 degrees C

A commonly used test to activate and accelerate the moisture failure mechanism prevalent in plastic encapsulated microcircuits is the Highly Accelerated Stress Test (HAST). One set of HAST tests were performed at 130 degrees C at 85% RH. This test condition was selected as it is commonly used in industry for testing commercial plastic ICs.

The HAST chamber used at NSWC Crane was the Express Test 1000X. The HAST fixtures were manufactured by HAST Solutions. The HAST chamber and HAST fixturing was cleaned with alcohol and rinsed with DI water at the beginning of each test cycle. The test operator wore rubber gloves while cleaning and loading the devices in the HAST fixturing to reduce the introduction of contaminates. To maintain the 85% relative humidity DI water was used in the HAST chamber to minimize unknown contaminates.

The devices were electrically tested initially, and at 216, 324, 432, 648, 864, and 1080 hours after the devices were taken from the HAST chamber to detect any failures. Table 1, page 13, shows the test results from the 130 degree C HAST up to 1080 hours. Testing on the 130 degree HAST had to be stopped after 1080 hours because of time constraints at the end of the program. Only one failure was encountered with the non-preconditioned DIP devices and only one failure with the 5 volt VCC SOIC devices up to 1080 hours. It should be noted that 1080 hours of HAST at 130 degrees C far exceeds test times that are normally done in the commercial world. In 1994 a JEDEC survey concluded the average HAST test time at 130 degrees was 100 hours.

Figure 4 is a chart showing the comparison between the failures of the DIP preconditioned devices and the DIP non-preconditioned devices in 130 degree HAST. The preconditioning tests are performed to simulate manufacturing stresses that the plastic components will encounter. These preconditioning flows are the ones used by National for their commercial components. The DIP devices andthe SOIC devices were preconditioned as shown in figure 5.

Of the ceramic DIP control lot tested in HAST at 130 degrees C only one device failed, it was at 30 volts VCC. At the time this report was written the cause of this failure was not understood.

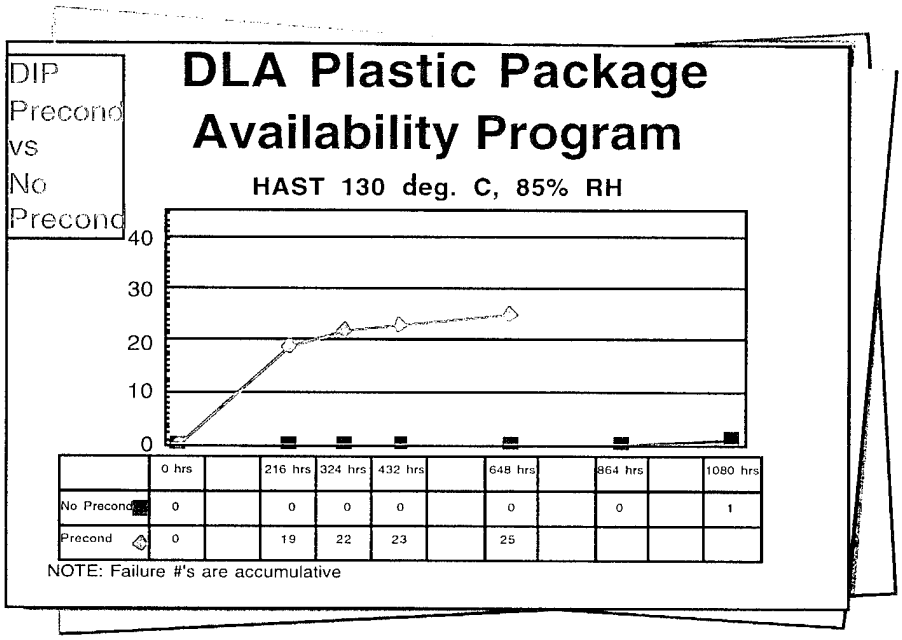


Figure 4

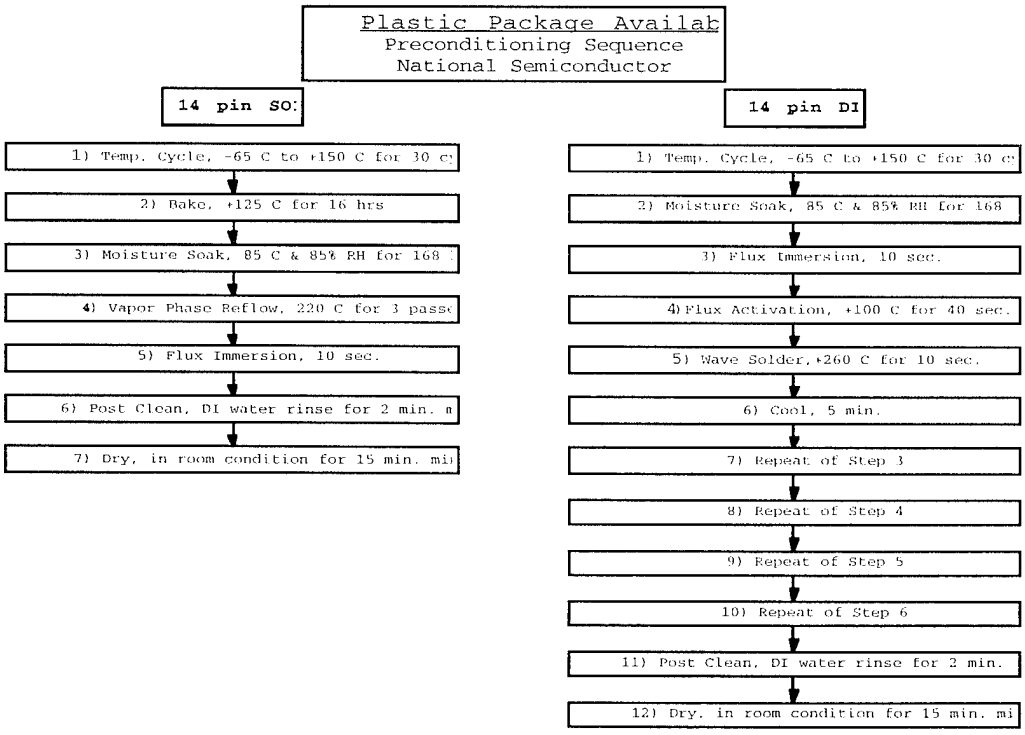


Figure 5

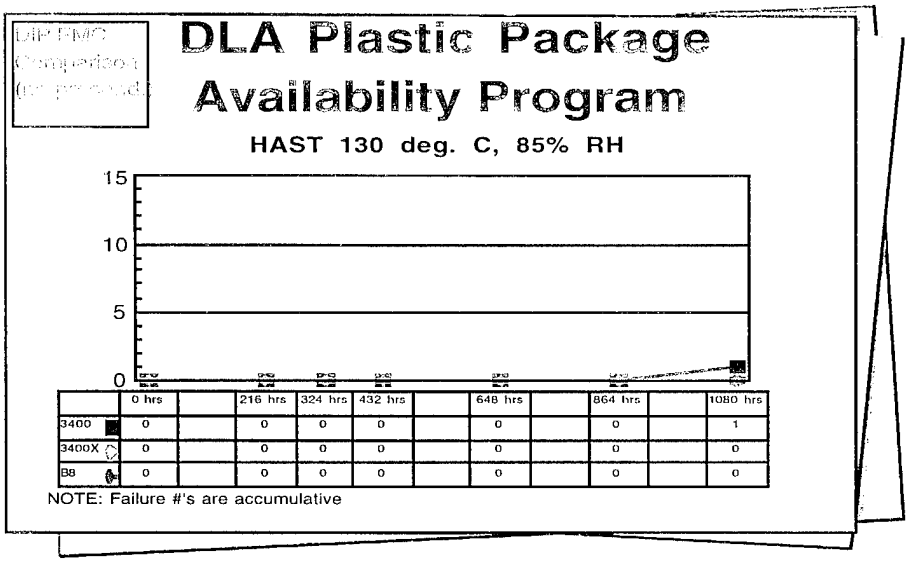


Figure 6

Figure 6 shows a test results comparison between the EMCs used in the DIP package style with no preconditioning tested in HAST at 130 degrees C. As can be seen after 864 hours of HAST, there were no failures that could help distinguish between the three different EMCs. This was one of the reasons for selecting a series of HAST tests at 159 degrees C, to further accelerate the failure to help evaluate the plastic ICs in a more timely manner.

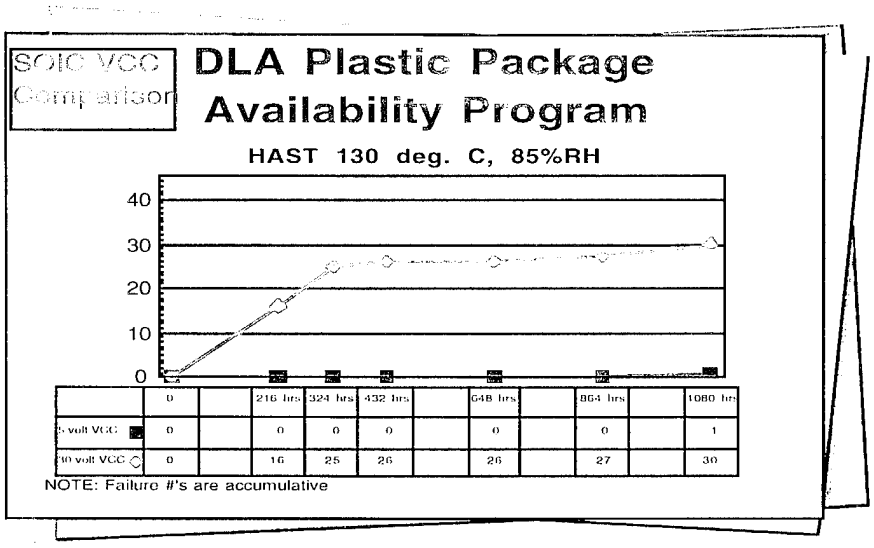


Figure 7

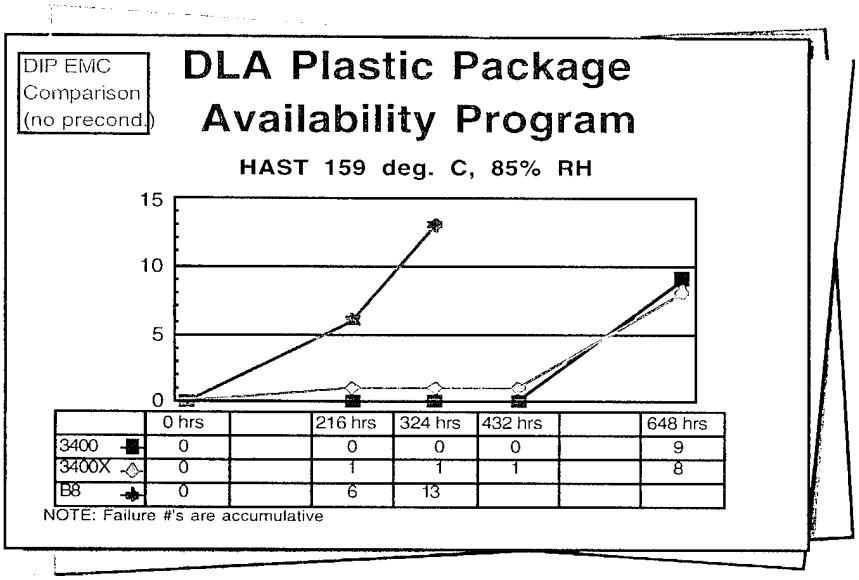
Figure 7 is a comparison of the 130 degree C HAST, 85% RH, SOIC package style, 5 volts VCC versus 30 volts VCC. As can be seen the 30 volts VCC fails sooner than the 5 volt VCC. The 30 volt VCC is within the operating range of the LM124 device.

HAST - 159 degrees C

Another series of HAST tests were performed at 159 degrees C and 85% RH. This test condition was selected to give a second temperature data point for the HAST and to accelerate the number of HAST failures to get more failure data. One concern when testing at 159 degrees in the HAST chamber is that other failure mechanisms may be activated besides the intended moisture and corrosion mechanisms. Failure analysis done on the 130 degree C and 159 degree C HAST failures did not show failure causes other than corrosion for the low lead count devices.

The devices were electrically tested initially, and at 216, 324, 432 and 648 hours the devices were taken from the HAST chamber to detect any failures. Table 2, page 14, shows the test results for the low lead count devices from the 159 degree C HAST with 85% RH. The 159 degree HAST testing was stopped after 648 hours because all the plastic IC lots had reached 50 % failure except one.

When the 159 degree 85% RH HAST testing was concluded after 648 hours none of the ceramic control devices had failed.



	0 hrs		216 hrs	324 hrs	432 hrs		648 hrs
3400	0		0	0	0		9
3400X	0		1	1	1		8
B8	0		6	13			

NOTE: Failure #'s are accumulative

Figure 8

Figure 8 shows a comparison of the three EMCs used in the DIP package with no preconditioning at 159 degrees C HAST. The older National B8 EMC failed first with the Plaskon 3400 lasting much longer. The Plaskon 3400X enhanced EMC show a slight improvement over the 3400 and is much better than the B8. All three preconditioned DIP test lots had reached at least 50% failure at the first data point of 216 hours.

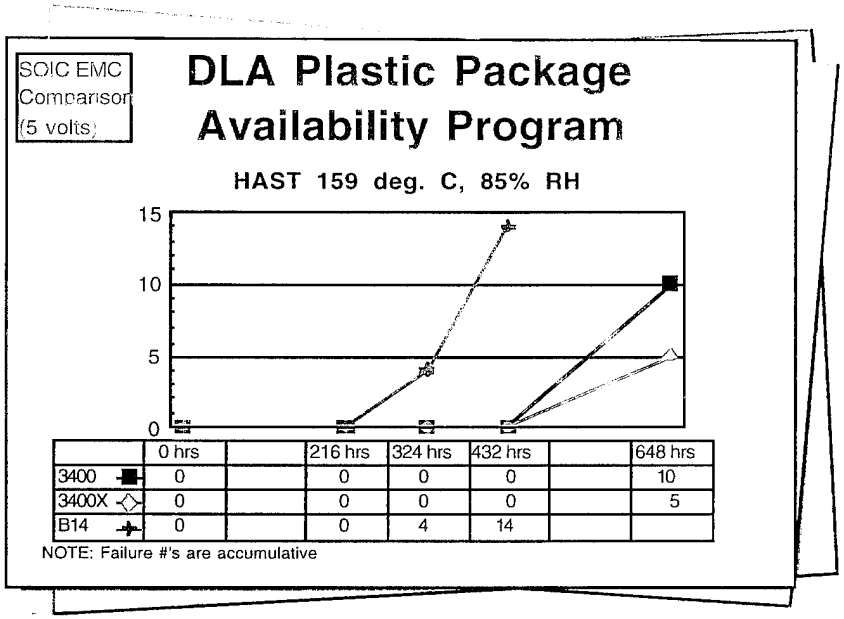


Figure 9

Figure 9 is a comparison of the three EMCs used in the SOIC package at 5 volts VCC at 159 degrees C HAST with 85% RH. The older National B14 SOIC EMC failed first with the Plaskon 3400 lasting much longer. The Plaskon 3400x enhanced EMC shows a marked improvement over the 3400 and is much better than the B14. All three of the SOIC test lots at 30 volts VCC had reached at least 50% failure at the first data point of 216 hours.

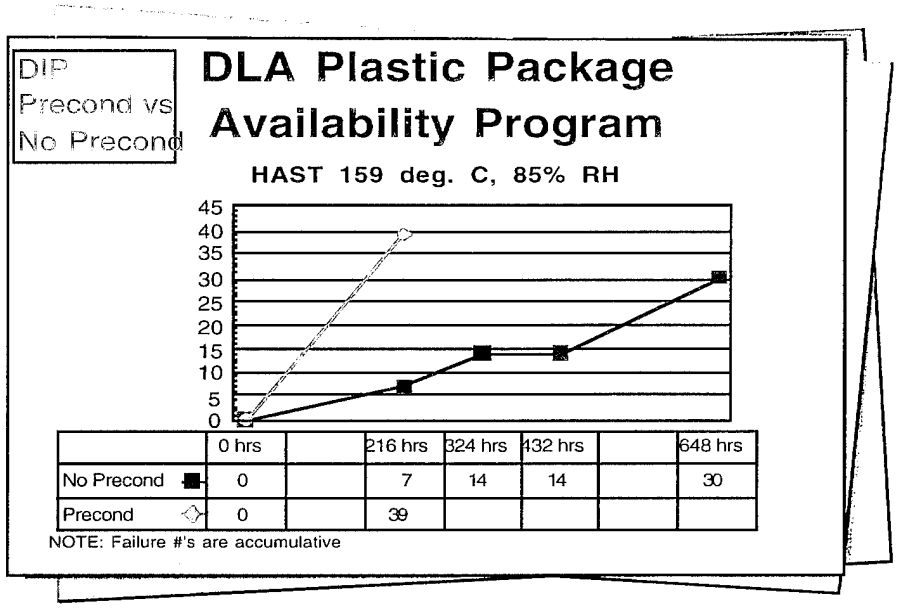
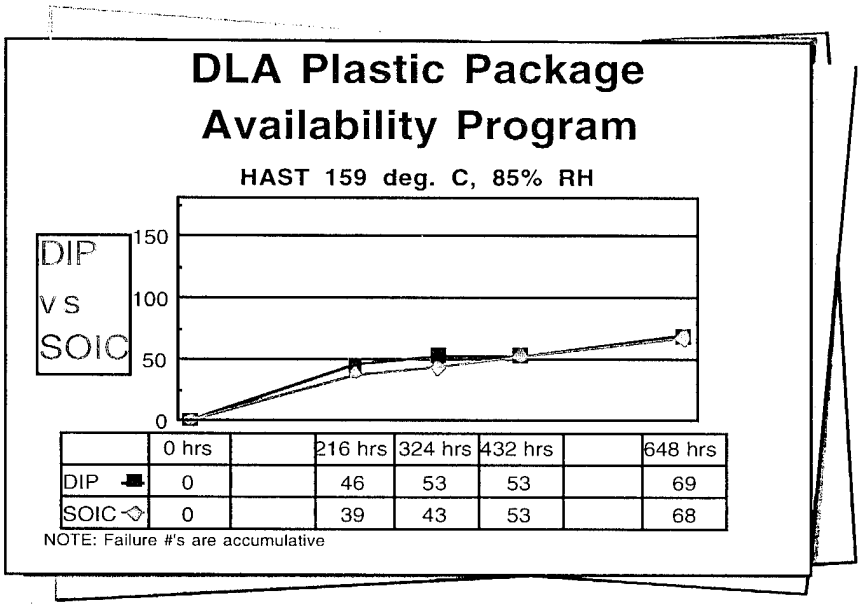


Figure 10

Figure 10 is a comparison of the three DIP lots that were preconditioning versus the three DIP lots that were non-preconditioning at 159 degrees HAST with 85% RH. As can be seen from the test results preconditioning can make a significant difference in the HAST test results. At the time this report was being prepared we do not fully understand the cause of the accelerated failures of the preconditioned devices. A customer buying PEMs should be aware of the type of preconditioning tests that are performed on the devices that they will be purchasing.



	0 hrs		216 hrs	324 hrs	432 hrs		648 hrs
DIP	0		46	53	53		69
SOIC	0		39	43	53		68

NOTE: Failure #'s are accumulative

Figure 11

Figure 11 compares the total number of failures of the DIP package versus SOIC package types in 159 degree HAST with 85% RH. This includes 90 DIP devices and 90 SOIC devices for a total of 180 devices. As can be seen from the chart, the package style, at least in this case, did not effect the HAST failure rates. This may not be true for all package styles and should be another factor that the PEM customers must be aware of.

Figure 12 compares the total number of 130 degree HAST failures (out of 180) to the total number of 159 degree HAST failures (out of 180) with 85% RH. Naturally the 159 degree HAST failure rate is higher than the 130 degree HAST but not as high as some acceleration factors would indicate with the 29 degree C temperature difference.

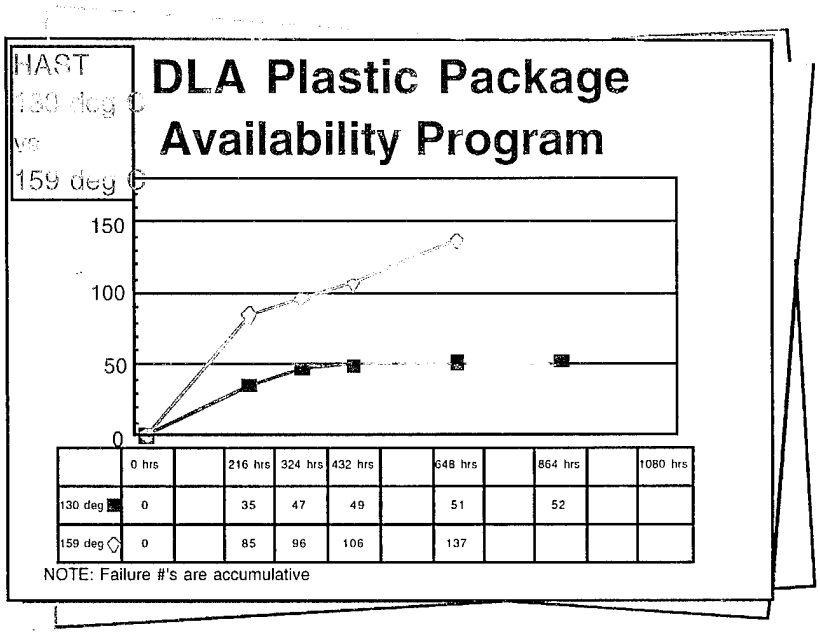


Figure 12

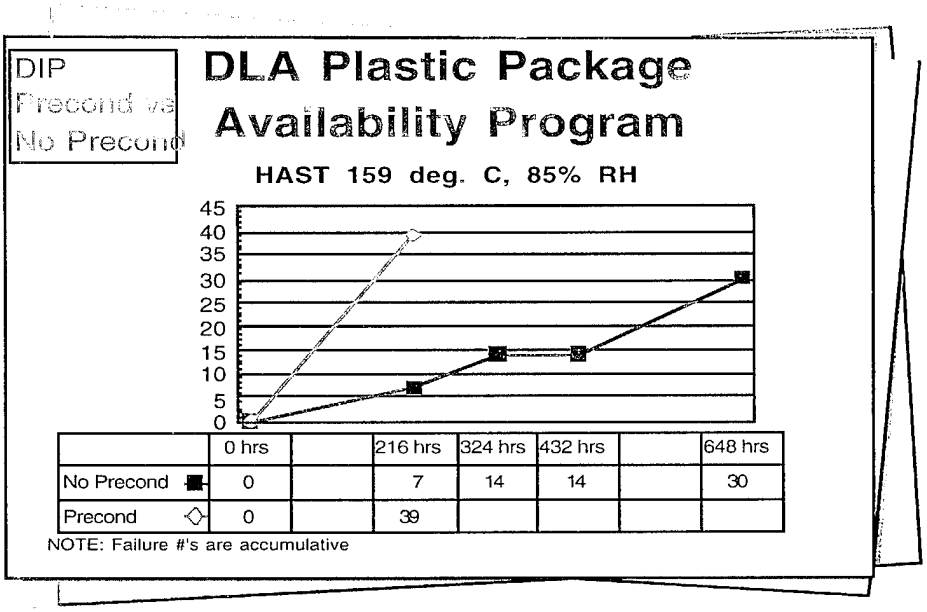


Figure 13

Difficulties With HAST Testing

HAST testing can be an effective way to accelerate the moisture and corrosion failure mechanisms that are inherent to plastic encapsulated microcircuits. There were several problems encountered by NSWC Crane in performing the HAST testing which are briefly listed and discussed below.

HAST Fixtures

The HAST fixturing used in the NSWC Crane HAST chamber was manufactured by HAST Solutions. One problem with the HAST fixturing is that it is costly. The board for a 120 position DIP fixture was $725 and a 42 position SOIC fixture with sockets was $958. To test 120 DIP devices and 90 SOIC devices for the PPA design of experiment required two DIP HAST fixtures ($1450) and three SOIC HAST fixtures ($2574) for a total fixture cost of $4024.

Another problem with the HAST fixturing is the wear out and resulting replacement of the HAST fixtures. The HAST testing at 159 degrees C with 85% RH accelerates the wear out of the fixture over the HAST at 130 degrees C. Two HAST boards were damaged during the PPA HAST testing and had to be replaced.

Cleaning of IC Leads After HAST Testing

The HAST environmental testing at 130 and 159 degrees with 85% RH caused some degradation of the device lead finish. This resulted in a device lead connectivity problem with the ATE test socket during electrical testing. This required manually cleaning the leads after each HAST run to ensure good electrical contact of the devices leads in the ATE socket. The DIP leads were a problem but the SOIC leads were even more difficult because of their smaller size.

Length of Electrical Testing

The low lead count device LM124 was electrically tested on Automatic Test Equipment (ATE) initially before each environmental test and at several monitor points during the environmental testing. The LM124 is a quad Op Amp linear device. The electrical tests were done on a Teradyne A312 ATE to Mil. Spec. Mil-M-38510/110A. This test program run time proved to be very lengthy so some tests were deleted in an effort to reduce the ATE test time to three minutes but still test most of the performance aspects of the device. In practice the actual ATE test time was approximately five minutes. The ancient operating system of the A312 also resulted in difficulties in changing programming parameters and long delays in saving test data results. The lab ATE operators averaged ten devices tested per hour for about 80 devices per eight hour shift. When testing the 350 devices from the Temperature Cycling or High Temperature Storage tests, electrical testing usually took a full five day work week or longer with unexpected delays.

Salt Fog

This test was performed at 35 degrees C with a 3% salt solution for 48 hours to a Mil.-STD-883 TM1009. Before and after environmental testing a visual inspection was performed. None of the plastic devices failed the salt fog test. The salt fog test as performed by the Mil. Spec. may not be an adequate test for plastic encapsulated microcircuits. The test does not determine if the salt solution has permeated the epoxy molding compound and reached the microcircuit die to prematurely start corrosion.

High Temperature Storage

The High Temperature Storage (HTS) test accelerates temperature induced failures such as interdiffusion, Kirkendall Voiding and depolymerization. The HTS tests were performed at 175 degrees C with no voltage applied to the devices. Electrical tests were performed at initial, 216, 432, 1080 and 1512 hours. Table 3, page 15, shows the test results for the HTS tests. Only four failures occurred after 1512 hours of testing, the industry average for the HTS is 1000 hours. After 1512 hours of HTS none of the ceramic control devices failed.

Temperature Cycling

The temperature extremes used in the temperature cycling tests are used to activate failure mechanisms related to mechanical stresses caused by the different Coefficient of Thermal Expansions (CTE) of the materials used in the plastic IC. The temperature cycling tests were performed at -65 degrees C to +150 degrees C with a dwell time of 30 minutes and a transition time of 30 seconds. Electrical tests were performed at initial and 216, 432, 1080 and 1512 cycles. In industry it is common to test up to 1000 cycles of temperature cycling. Table 4 , page 16, shows the test results of the temperature cycle tests.

One ceramic control device failure occurred after 1080 cycles of temperature cycling. This failure is being investigated, but at the writing of this report the cause of the failure was not understood.

Op Life

The Operational Life test was originally included in the design of experiments but was deleted because of limited resources available and the amount of relevant test data that we thought we would gain from the Op Life test. This is not to say that Op Life should not be done on plastic ICs. This was a mature product with existing data available.

Summary

The environmental tests performed on the LM124 low lead count devices yielded a large amount of test data and information. The interpretation of this data is discussed in other sections of this report. Some root cause of failures are still not understood and require further study. The preconditioning of the PEM device is an important factor in the environmental test results. The cause(s) of the differences between preconditioning and non-preconditioning test results is not thoroughly understood and need to be further investigated. One topic that was not fully addressed in this report, but is always requested, is how the accelerated life test results equate to system life reliability. Because of the numerous different definitions of "system life" this is a difficult question to answer but certainly needs to be addressed in a future study. There is still a lot of research and investigation that needs to be accomplished on plastic encapsulated microcircuits when used in some harsh or unique military environments.

HAST - 130 deg. C

DIP Package					FAILURES					
Lot #	Serial #	EMC	Condition	# in Lot	216 hrs	324 hrs	432 hrs	648 hrs	864 hrs	1080 hrs
DLA-1	31-45	EMC-P1 (3400)	No Precond	15	0/15	0/15	0/15	0/15	0/15	1/15
DLA-1	46-60	EMC-P1 (3400)	Precond	15	9/15	9/15	9/15	9/15	9/15	9/15
DLA-2	31-45	EMC-P2 (3400X)	No Precond	15	0/15	0/15	0/15	0/15	0/15	0/15
DLA-2	46-60	EMC-P2 (3400X)	Precond	15	6/15	6/15	6/15	6/15	6/15	6/15
DLA-3	31-45	EMC-P4 (B8)	No Precond	15	0/15	0/15	0/15	0/15	0/15	0/15
DLA-3	46-60	EMC-P4 (B8)	Precond	15	8/15	8/15	8/15	10/15	10/15	10/15
DLA-7	31-45	Ceramic	5 volts	15	0/15	0/15	0/15	0/15	0/15	0/15
DLA-7	46-60	Ceramic	30 volts	15	0/15	0/15	0/15	1/15	1/15	1/15
SOIC Package					FAILURES					
DLA-5	31-45	EMC-P2 (3400)	5 volts	15	0/15	0/15	0/15	0/15	0/15	0/15
DLA-5	46-60	EMC-P2 (3400)	30 volts	15	0/15	0/15	1/15	1/15	2/15	5/15
DLA-4	31-45	EMC-P1 (3400X)	5 volts	15	0/15	0/15	0/15	0/15	0/15	0/15
DLA-4	46-60	EMC-P1 (3400X)	30 volts	15	11/15	13/15	----	----	----	----
DLA-6	31-45	EMC-P4 (B14)	5 volts	15	0/15	0/15	0/15	0/15	0/15	1/15
DLA-6	46-60	EMC-P4 (B14)	30 volts	15	#1 5/15	12/15	-----	-----	----	----

Notes
#1 2 devices melted in HAST chamber

TABLE 1

HAST - 159 deg. C

DIP Package					FAILURES			
Lot #	Serial #	EMC	Condition	# in Lot	216 hrs	324 hrs	432 hrs	648 hrs
DLA-1	1-15	EMC-P1 (3400)	No Precond	15	0/15	0/15	0/15	9/15
DLA-1	16-30	EMC-P1 (3400)	Precond	15	13/15	-----	-----	-----
DLA-2	1-15	EMC-P2 (3400X)	No Precond	15	1/15	1/13*	1/13*	8/13*
DLA-2	16-30	EMC-P2 (3400X)	Precond	15	11/15	-----	-----	-----
DLA-3	1-15	EMC-P4 (B8)	No Precond	15	3/15	13/15	-----	-----
DLA-3	16-30	EMC-P4 (B8)	Precond	15	15/15	-----	-----	-----
DLA-7	1-15	Ceramic	5 volts	15	0/15	0/15	0/15	0/15
DLA-7	16-30	Ceramic	30 volts	15	0/15	0/15	0/15	0/15
SOIC Package					FAILURES			
DLA-5	1-15	EMC-P2 (3400)	5 volts	15	0/15	0/15	0/15	10/15
DLA-5	16-30	EMC-P2 (3400)	30 volts	15	15/15	-----	-----	-----
DLA-4	1-15	EMC-P1 (3400X)	5 volts	15	0/15	0/15	0/15	5/15
DLA-4	16-30	EMC-P1 (3400X)	30 volts	15	15/15	-----	-----	-----
DLA-6	1-15	EMC-P4 (B14)	5 volts	15	0/15	4/15	14/15	-----
DLA-6	16-30	EMC-P4 (B14)	30 volts	15	9/15	-----	-----	-----

Notes
#1 3 devices melted in HAST chamber

TABLE 2

High Temp Storage

DIP Package				FAILURES				
Lot #	Serial #	EMC	# in Lot	216 hrs	432 hrs	1080 hrs	1512 hrs	1944 hrs
DLA-1	111-160	EMC-P1 (3400)	50	0/50	0/50	0/50	3/50*	
DLA-2	111-160	EMC-P2 (3400X)	50	0/50	0/50	0/50	0/50	
DLA-3	111-160	EMC-P4 (B8)	50	0/50	0/50	1/50	1/50	
DLA-7	111-160	Ceramic	50	0/50	0/50	0/50	0/50	
SOIC Package				FAILURES				
DLA-5	111-160	EMC-P2 (3400)	50	0/50	0/50	0/50	0/50	
DLA-4	111-160	EMC-P1 (3400X)	50	0/50	0/50	0/50	0/50	
DLA-6	111-160	EMC-P4 (B14)	50	0/50	0/50	0/50	0/50	

Notes
175 deg C all device are precondioned
Serial #119 Pin 1 is missing

TABLE 3

Temp. Cycle

DIP Package				FAILURES				
Lot #	Serial #	EMC	# in Lot	216 cyc	432 cyc	1080 cyc	1512 cyc	1944 cyc
DLA-1	61-110	EMC-P1 (3400)	50	0/50	0/50	0/50		
DLA-2	61-110	EMC-P2 (3400X)	50	0/50	0/50	0/50		
DLA-3	61-110	EMC-P4 (B8)	50	0/50	0/50	0/50		
DLA-7	61-110	Ceramic	50	0/50	0/50	1/50		
SOIC Package				FAILURES				
DLA-5	61-110	EMC-P2 (3400)	50	0/50	0/50	0/50		
DLA-4	61-110	EMC-P1 (3400X)	50	0/50	0/50	0/50		
DLA-6	61-110	EMC-P4 (B14)	50	0/50	0/50	0/50		

Notes
-65 to +150 deg C all device are preconditioned

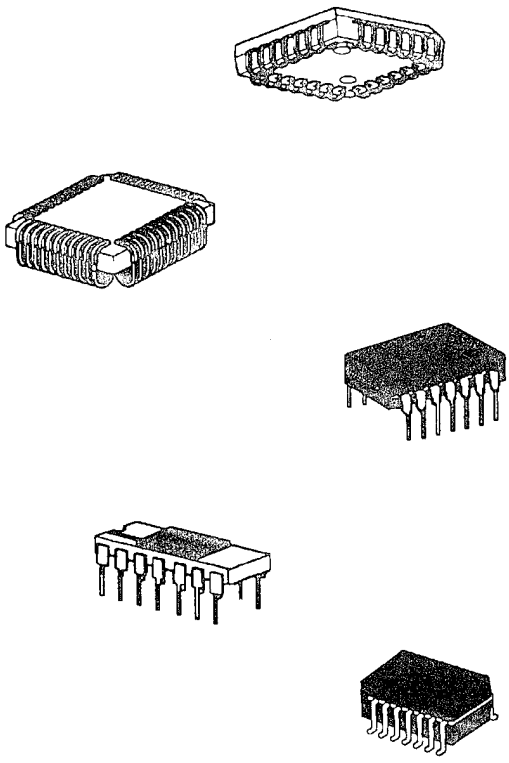
TABLE 4

PLASTIC PACKAGE AVAILABILITY PROGRAM

ROME FINAL REPORT

SECTION 7

Task 7.0 Device Reliability Testing



PLASTIC PACKAGE AVAILABILITY PROGRAM

FAILURE ANALYSIS, SCANNING ACOUSTIC MICROSCOPE AND DYE PENETRANT EVALUATION

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Commercial and Plastic Components in Military Applications Workshop
Indianapolis, Indiana
15 November 1995

PLASTIC PACKAGE AVAILABILITY PROGRAM

OUTLINE

- FAILURE ANALYSIS RESULTS
- C-SAM RESULTS
- DYE PENETRANT RESULTS
- CONCLUSIONS

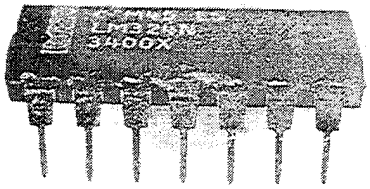
PLASTIC PACKAGE AVAILABILITY PROGRAM

FAILURE ANALYSIS RESULTS

- PACKAGES SHOWED EXTERNAL DAMAGE AT 130 AND 159°C
- ALL 130°C HAST FAILURES APPEAR TO BE THE RESULT OF CORROSION: PRIMARILY THE POWER PIN BOND PAD
- ALL 159°C HAST FAILURES APPEAR TO BE THE RESULT OF CORROSION: PRIMARILY THE POWER PIN BOND PAD
- CORROSION REACTANTS AND PRODUCTS WERE NOT IDENTIFIED

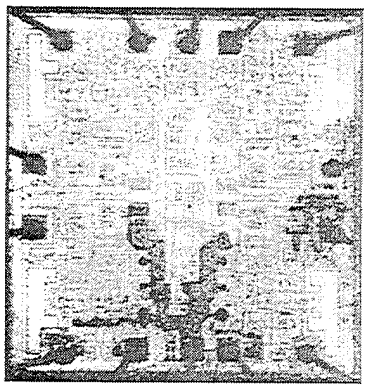
PLASTIC PACKAGE AVAILABILITY PROGRAM

TYPICAL EXTERNAL PACKAGE CORROSION



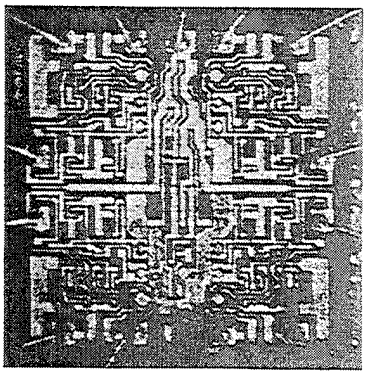
PLASTIC PACKAGE AVAILABILITY PROGRAM

CORROSION RESULTING FROM HAST AT 130°C



PLASTIC PACKAGE AVAILABILITY PROGRAM

CORROSION RESULTING FROM HAST AT 159°C



PLASTIC PACKAGE AVAILABILITY PROGRAM

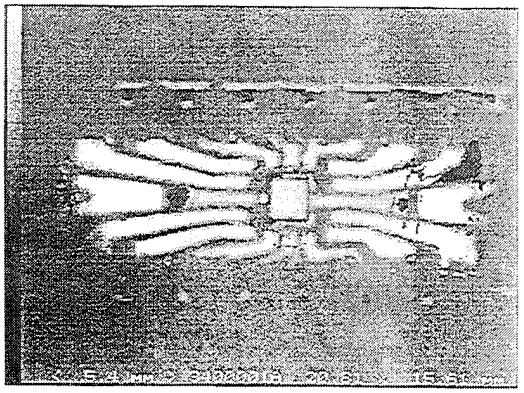
C-SAM RESULTS

- CHARACTERISTIC MANUFACTURING DEFECTS IDENTIFIED
  - DE-GATE DAMAGE
- DELAMINATION CAUSED BY PRECONDITIONING
- DELAMINATION GROWTH CAUSED BY 100 TEMP CYCLES
- CORROSION FAILURE CHARACTERISTICS IDENTIFIED
- EXTENT OF DELAMINATION DETECTED VARIED WIDELY FROM PART TO PART

PLASTIC PACKAGE AVAILABILITY PROGRAM

DIP WITH NO PRECONDITIONING

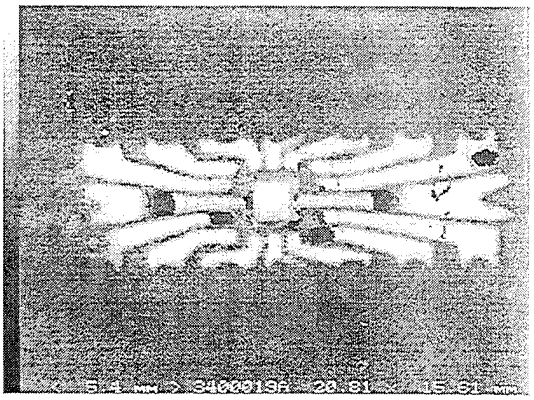
- BENDS IN TIE BAR CAUSE APPARENT OR ACTUAL DELAMINATION AT THE BENDS
- COMMON DELAMINATION ON LEAD 8 MAY BE THE RESULT OF DE-GATE DAMAGE



PLASTIC PACKAGE AVAILABILITY PROGRAM

DIP WITH PRECONDITIONING

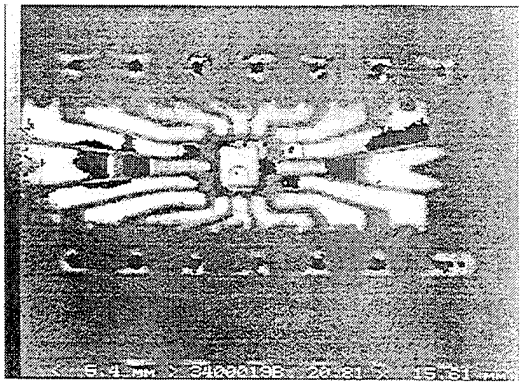
- DELAMINATION GROWTH AT WIRE BOND LOCATIONS TYPICAL OF PRECONDITIONING
- LONGEST LEADS OFTEN SHOW DELAMINATION
- SHORTEST LEADS (4 AND 11) NEVER SHOW DELAMINATION



PLASTIC PACKAGE AVAILABILITY PROGRAM

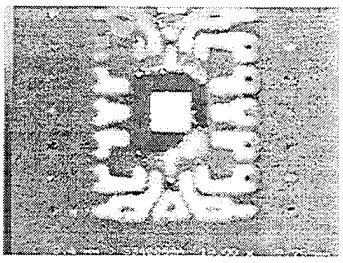
FAILED DIP

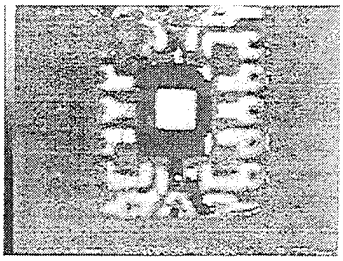
- IMAGE SHOWS DELAMINATION GROWTH AROUND TIE BAR BENDS AND DIE PADDLE, AND DE-GATE DAMAGE
- PATTERN ON THE DIE SURFACE IS TYPICAL OF PARTS WITH SEVER CORROSION OF THE POWER PIN



PLASTIC PACKAGE AVAILABILITY PROGRAM

SOIC BEFORE AND AFTER 100 TEMP CYCLES





DELAMINATION GROWTH AT THE EMC/LEAD FRAME INTERFACE AFTER 100 TEMPERATURE CYCLES APPEARS TO EXTEND TO THE EXTERIOR OF THE PACKAGE

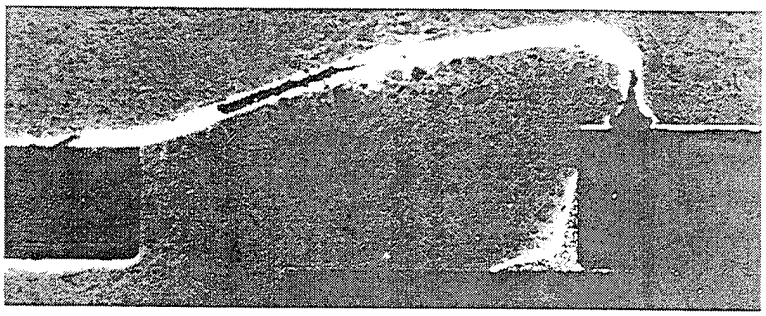
PLASTIC PACKAGE AVAILABILITY PROGRAM

DYE PENETRANT RESULTS

- TEST PERFORMED ACCORDING TO MIL-STD-883, TM-1034
- PRECONDITIONED DIP AND SOIC PACKAGES BOTH SHOW DELAMINATION PATHWAYS TO THE DIE PADDLE
- SOIC HAVE DELAMINATED PATHS TO THE DIE SURFACE

PLASTIC PACKAGE AVAILABILITY PROGRAM

LEAD, BOND WIRE, AND DIE SHOWING DYE PENETRATION

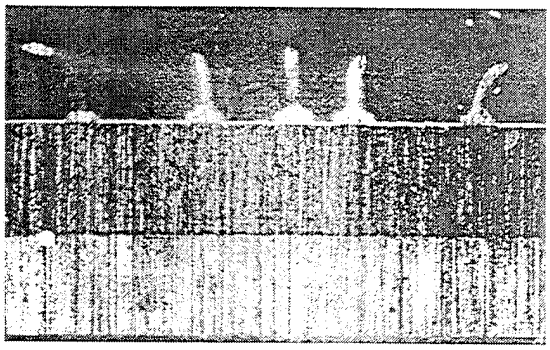


PRECONDITIONED SOIC (3400) SHOWING DIE PENETRATION ALONG LEAD (#11), BOND WIRE AND DIE ATTACH FILLET

Photography courtesy of
Oneida Research Services, Inc.

PLASTIC PACKAGE AVAILABILITY PROGRAM

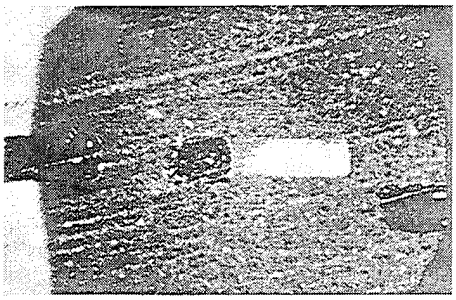
BALL BONDS 3, 4 & 5 SHOWING DYE PENETRATION



PRECONDITIONED SOIC (3400) SHOWING DIE PENETRATION AT BALL BONDS 3, 4 AND 5. BALL BONDS 2 AND 6 SHOWING NO PENETRATION

PLASTIC PACKAGE AVAILABILITY PROGRAM

LEAD PULLOUT SHOWING DYE PENETRATION



PRECONDITIONED SOIC (3400X) SHOWING DIE PENETRATION ALONG LEAD AND FULL PENETRATION AT THE VERTICAL LEAD/EMC INTERFACE

PLASTIC PACKAGE AVAILABILITY PROGRAM

CONCLUSIONS

- ALL HAST FAILURES IDENTIFIED TO DATE ARE THE RESULT OF CORROSION
- HAST AT 130 AND 159°C APPEAR TO BE CREATING SIMILAR FAILURE MECHANISMS
- DIFFERENCES IN PRECONDITIONING AND MOLDING COMPOUND MAY BE AFFECTING WHETHER INTRINSIC OR EXTRINSIC CONTAMINATION IS CONTROLLING THE REACTION RATE
- THE TYPE OF FLUX USED MAY HAVE SIGNIFICANT IMPACT ON HAST FAILURE RATES

CONCLUSIONS

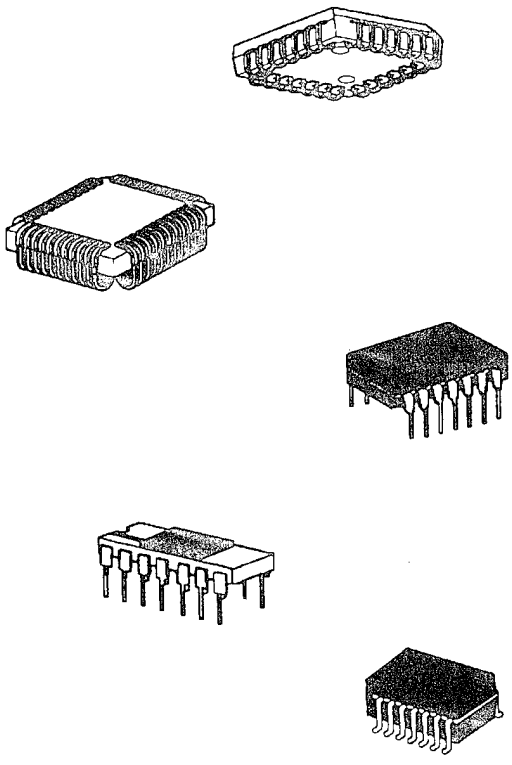
- C-SAM AND DYE PENETRANT RESULTS DO NOT ALWAYS AGREE
  - C-SAM RESOLUTION IS NOT SUFFICIENT TO DETECT ALL DELAMINATIONS
- PARTS WITH C-SAM DETECTED DELAMINATIONS DID NOT FAIL FASTER AS GROUP
- PATHWAYS EXIST INTO PEM PACKAGES WHICH ALLOW THE TRANSPORT OF EXTRINSIC CONTAMINATION

PLASTIC PACKAGE AVAILABILITY PROGRAM

HONEYWELL FINAL REPORT

SECTION 8

Task 8.0 Devices Reliability Analysis



Plastic Package Availability Program

Task 1: Military IC Package Criteria Definition and Systems Selection

Task 8: Device Reliability Analysis

Final Report (A012)
Contract Number BSC214843
Prime Contract No. DLA900-92-C-1647

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1.0 Executive Summary

This is the final report for Honeywell's subcontract on the National Semiconductor Corporation (NSC)/Defense Logistics Agency (DLA) Plastic Package Availability Program. This final report focuses upon documenting Honeywell Commercial Aviation Systems (CAS) field reliability experience. The report compiles results from multiple Honeywell CAS studies of piece part failure rates experienced in actual field usage. The studies are for seven line replaceable units (LRU's) of which the first three contain hermetically sealed microcircuits only, and the remaining 4 LRU's contain a mixture of plastic and hermetic microcircuits. The hermetic parts for LRU's 5-7 (comprising 14% of LRU's 5-7 microcircuits) were not included in this report due to the field failure data having not been collected. This report compares the resulting field failure rates between plastic and hermetic devices as well as comparing the results against predicted failure rates. Factors influencing the failure rates such as derating and thermal environment are also discussed.

This Executive Summary Section provides an overview of Honeywell's effort including the statement of work, a summary of results, and a glossary of abbreviations used throughout the report.

1.1 Statement of Work

Revised Statement of Work

BAA 92-02-MLK, Subarea E2, Plastic Availability,

For Honeywell, Inc.

(12/15/92)

This statement of work for Honeywell, Inc., Honeywell Technology Center (HTC), is part of National Semiconductor Corporation's (National) Plastic Packaging Availability Program, Defense Logistics Agency contract, DLA-900-92-C-1647, in response to BAA No. 92-02-MLK, Subarea E2. Honeywell HTC will provide service for Task 1 (Military Package Criteria Definition and Systems Selection), Task 8 (Device Reliability Analysis), and Task 12 (Preparation of Data Items Deliverable), as defined in the overall schedule of the National Program.

Task 1. Military IC Package Criteria Definition and Systems Selection

Task 1.1 Preliminary Review

The prime contractor, National, and all subcontractors (Plaskon Electronic Materials, Inc., Honeywell SRC, Dow Corning Corp., and Sandia National Laboratories) shall meet with the DoD program manager (DLA), representatives from Rome Labs, DESC, and other interested DoD participants for a single meeting to discuss the details of this effort. Honeywell HTC will provide an outline of their Statement of Work (SOW) and provide presentation foils

describing the work and a Gantt chart listing the timing of the program. This preliminary review will be on November 3, 1992 at the NWSC, Crane, IN., with a dry run scheduled for November 2.

Task 1.2 Systems Selection and Baseline Description

Systems selection and baseline description will describe and compare Honeywell Commercial Flight Systems (CFS) plastic versus ceramic IC usage and practices. This task will be comprised of the following six subtasks.

Task 1.2.1 Select Candidate Systems

Honeywell will select at least two avionics systems (to be generically but not specifically identified), one containing plastic packaged ICs and one containing hermetic/ceramic ICs. The system environments will be defined and a written discussion for selecting these systems, their relevance to the contract, and their similarity or equivalence to military applications will be provided. The system descriptions and associated information will be summarized in an interim report covering Tasks 1.2.1, 1.2.2, and 1.2.3 to be provided to NSC on 3/1/93.

Task 1.2.2 Describe System Parts

The quantity and type (part type, package type, and lead configuration) of both ceramic and plastic parts in the selected systems will be identified in addition to the minimum screening/qualification requirements for the devices. The system descriptions and associated information will be summarized in an interim report covering Tasks 1.2.1, 1.2.2, and 1.2.3 to be provided to NSC on 3/1/93.

Task 1.2.3 Identify National Semiconductor Parts

The NSC parts contained in each of the selected systems will be identified by generic number, package type, and device description. This list of NSC devices will be provided to NSC by 2/1/93 and will serve as potential candidates for the molding compound evaluation (Task 7). The system descriptions and associated information will be summarized in an interim report covering Tasks 1.2.1, 1.2.2, and 1.2.3 to be provided to NSC on 3/1/93.

Task 1.2.4 Describe IC Vendor Selection Process

Provide a description of CFS's approach to the selection and qualification of IC vendors, including standards for selecting IC vendors. The results of Tasks 1.2.4, 1.2.5, and 1.2.6 will be provided to NSC on 7/1/93 in an interim report.

Task 1.2.5 Describe Specification and Procurement of Plastic and Ceramic ICs

Provide a description of CFSG's approach to the specification and procurement of plastic versus ceramic ICs. The results of Tasks 1.2.4, 1.2.5, and 1.2.6 will be provided to NSC on 7/1/93 in an interim report.

Task 1.2.6 Describe Part Processing, Production, and Repair Flow

Provide a description of CFS's plastic versus ceramic process flows from parts receiving through to field repair detailing the critical events/processes from receipt of materials to end of system life. Sources for this data are

expected to be internal Honeywell work instructions and processing specifications in addition to manuals for installation, field repair, service, etc. Examples of critical events/processes are — temperature profiles, exposure to vapors/liquids which may adversely affect the plastic encapsulants, rework/repair limitations (number of site reworks), etc. An example of a generic flow chart would be —> Receipt, Incoming Test, Kitting, Stuffing, Soldering, Cleaning, Inspection, Testing, Subassembly, Subassembly Test, Integration into system, System test, Delivery, Installation, Trouble shoot, Field Repair —> etc. The results of Tasks 1.2.4, 1.2.5, and 1.2.6 will be provided to NSC on 7/1/93 in an interim report. Proprietary data will be so marked and reported separately for restricted distribution.

Task 8. Device Reliability Analysis

The device reliability analysis task will describe and compare plastic versus ceramic device reliability experience from actual Honeywell CFS fielded systems. This task will be comprised of the following two subtasks.

Task 8.1 Reliability Prediction Methodology

Honeywell will provide a description of and contrast its reliability prediction methodologies for systems containing plastic and ceramic integrated circuits. Predicted MTBFs for the systems selected in Task 1 will be provided.

Task 8.2 Assessment of Fielded Systems

Using the selected systems, Honeywell will perform comparative analysis of plastic versus ceramic semiconductor field failure rates. This analysis will include as a minimum:

- number of system operating hours
- number of device failures experienced
- electrical part derating requirements for semiconductors
- temperature rise information from equipment ambient to operating temperature
- representative temperature distribution for field thermal environment(s)
- device failure criteria; i.e., what criterion was applied to determine the above failures
- cause of failure (plastic parts only, if known)
- materials of construction (plastic parts only, if known)

Task 12. Data Items

Honeywell HTC shall prepare and deliver the following Data Items as follows:

Task 12.1 Reports To Be Supplied In Hard Copy and Electronic Media

Task 12.2 Photographs and Drawings

Task 12.3 Program Management and Planning

Task 12.4 R&D Status Report, DI-A-3002A: (Sequence Number A010)

Task 12.5 Scientific and Technical Report (Final), DI-MISC-80711: (Sequence Number A012)

Task 12.6 Travel and Meetings

The work associated with Task 1 has previously been documented but for completeness is herein reproduced and included as Appendix B. The CAS reliability prediction methodology was also previously documented and is included as Appendix C.

1.2 Summary of Results

This report is a compilation of three separate studies performed by Honeywell and has been revised and updated from a preliminary report previously distributed. The results of this study confirm that the approach Honeywell has taken in the use of plastic packaged microcircuits for the commercial avionics environment (see Appendix B for a detailed discussion of Honeywell practices) has maintained product reliability; i.e., the use of plastic packaged microcircuits has not been observed to degrade product reliability in commercial air transport applications.

The first study consisted of determining the failure rate of IC's installed in LRU's 1, 2 and 3. The IC's used in these LRU's were leaded, through-hole, hermetic devices. The majority of the IC's used in these LRU's are MIL-STD-883 compliant devices. A few of the devices are hermetic devices which were screened by the manufacturer with burn-in and tri-temperature testing using MIL-STD-883 test methods.

LRU 1 data includes 3,598,500 LRU operating hours which is equivalent to nearly 1.3 billion device operating hours. LRU 2 data includes 8,584,500 LRU operating hours which is equivalent to 2.4 billion device operating hours. LRU 3 data includes 668,000 LRU operating hours which is equivalent to 272 million device operating hours.

The study methodology consisted of analysis of LRU repairs, assembly replacements and their subsequent repairs to the piece part level. The raw observed failures for LRU's 1, 2 and 3 were 39, 680 and 47 respectively. However, not all repair actions were traceable to the piece part level. The percent of electronic failures that were traced to the piece part level were; 92% for LRU 1, 24% for LRU 2 and 49% for LRU 3. To compensate for the missing data the number of failures were increased assuming the same distribution (see paragraph 6.1 for details). There were significant differences in the failure rates among the IC part types (digital SSI/MSI, memory/LSI, linear). The observed failure rates (factor adjusted) for LRU's 1, 2 and 3 are as shown in Table 1.2-1.

Table 1.2-1. LRU 1-3 Failure Rate Quantities

DEVICE TYPE	LRU1 HOURS FAILURES	LRU 1 FAILURE RATE [1]	LRU2 HOURS FAILURES	LRU 2 FAILURE RATE [1]	LRU3 HOURS FAILURES	LRU 3 FAILURE RATE [1]
Digital SSI/MSI	834852000 3	0.004	1098816000 25	0.023	138276000 6	0.048
Memory/LSI	64773000 2	0.041	257535000 67	0.263	40748000 6	0.164
Linear	392236500 3	0.009	1090231500 17	0.016	93520000 2	0.029

1. Failure rates in failures per million hours

A limitation inherent in Study 1 is that data on all LRU repairs could not be collected to the piece part level. Factoring was required to compensate. Therefore, the actual failure rate may be higher or lower than calculated. Additionally, records were not available to discriminate failure rate differences between the MIL-STD-883 compliant parts and those hermetic devices which were manufacturer screened.

Study 2 consisted of determining the failure rate of IC's installed in LRU 4. This was the only study which included a combination of hermetic and plastic devices with varying levels of screening. 45% of the devices were military temperature range, thru-hole technology, hermetic devices with manufacturer screening. Some of these devices were MIL-STD-883 compliant. 26% of the devices were plastic surface mount technology, digital SSI/MSI, devices which received a lot sample screen which included both burn-in and extended temperature testing at a 3rd party test facility. 19% of the devices were plastic surface mount technology parts which received a 100% screening which included both burn-in and extended temperature testing. Most of this screening was performed by the manufacturer. The remaining 10% of the devices, all used in one assembly, were plastic surface mount parts which received no screening. During the selection process for these unscreened devices, manufacturers were consulted relative to the devices expected performance over temperature; also, the assembly that the unscreened devices are used in receives extensive electrical characterization over temperature.

LRU 4 data includes 892,000 LRU operating hours which is equivalent to over 87 million device operating hours.

The study methodology consisted of analysis of LRU repairs, assembly replacements and their subsequent repairs to the piece part level. The raw observed failures for LRU 4 were 179. However, only one-third of the repair actions were traceable to the piece part level. To compensate for the missing data the total number of failures was increased by two-thirds. See section 4.2 for a detailed discussion of how the factoring was accomplished. There

were significant differences in the failure rates among the IC part types (digital SSI/MSI, memory/LSI, linear). The observed failure rates (factor adjusted) are shown for the hermetic and plastic devices in Table 1.2-2.

Table 1.2-2. LRU 4 Failure Rate Quantities

DEVICE TYPE	HERMETIC HOURS FAILURES	HERMETIC FAILURE RATE [1]	PLASTIC HOURS FAILURES	PLASTIC FAILURE RATE [1]
Digital SSI/MSI	892000 0	0.777[2]	53520000 3	0.069
Memory/LSI	16948000 1	0.099	16948000 1	0.099
Linear	69576000 3	0.053	37464000 7	0.205

1. Failure rates in failures per million hours computed at 50% Chi-Squared confidence level

2. Failure rate artificially high due to low hours and zero failures

A limitation inherent in Study 2 is that data on all LRU repairs could not be collected to the piece part level. Factoring was required to compensate. Therefore, the actual failure rate may be higher or lower than calculated. Additionally, there were insufficient failures to discriminate failure rate differences between the two screening levels of hermetic devices or the three screening levels of plastic devices.

Study 3 determined the failure rates of IC's used in a system consisting of LRU's 5, 6 and 7. The IC's used in these LRU's are primarily plastic surface mount devices with limited use (14%) of hermetic devices. Only the plastic devices were analyzed for the study upon which this report is based. All of the plastic surface mount devices received 100% screening which included both burn-in and extended temperature testing. Most of this screening was performed at 3rd party test facilities using MIL-STD-883 test methods.

This study includes 4,772,000 operating hours for LRU 5, 4,042,250 operating hours for LRU 6 and 9,682,750 operating hours for LRU 7. This provided device hours of over 1 billion operating hours for digital SSI/MSI type devices, 315 million operating hours for memory/LSI type devices and 663 million operating hours for the linear type devices.

The study methodology consisted of collecting all replaced parts directly from the Honeywell facility performing repairs on these LRU's. A repair database was analyzed to identify removal causes for categorization between "Removal" (replacement did not correct LRU problem) and "Failure" (replacement corrected LRU problem). Numerous devices were submitted for detailed failure analysis so no factoring was required in this study since all replaced parts were available for analysis. However, the LRU from which a device was removed was not always known; so this analysis had to be made at the system level rather than at the LRU level on the three individual LRU's. Two memory device types, which experienced a high field failure rate ultimately identified as die and not package related, were eliminated from study 3 to allow a more accurate comparison between hermetic and plastic microcircuits. The values with the memory devices included are contained in parentheses throughout this report for completeness but should not be used when comparing plastic to hermetic. See paragraph 4.2 for a detailed

discussion of the failure modes and explanation for their removal. In both instances the suppliers cooperated with Honeywell to analyze the faults with the manufacturers implementing corrective action to prevent failure recurrence.

There were significant differences in the failure rates among the IC part types (digital SSI/MSI, memory/LSI, linear). The observed failure rates for the system which includes LRU's 5, 6 and 7 are shown in Table 1.2-3.

Table 1.2-3. LRU 5-7 Failure Rate Quantities

DEVICE TYPE	HOURS FAILURES [1,2]	FAILURE RATE [1,2]
Digital SSI/MSI	1,104,549,000 9	0.009
Memory/LSI	315,864,500 47 (545,475,500) 372	0.151 (0.683)
Linear	663,288,000 31	0.048

1. Failure rates in failures per million hours computed at 50% Chi-Squared confidence level
2. Values in parentheses include the two memory devices eliminated from study

For all three of the reported studies, variations were observed in the reliability of specific microcircuit groupings, and these variations may warrant some adjustment of predicted failure rates; but the changes in these failure rates will effectively cancel themselves out when viewed from an LRU reliability level and will not adversely impact the overall product reliability.

Both the digital SSI/MSI and µProc./Memory microcircuit groupings showed a plastic failure rate half that of the ceramic parts. An explanation for this is not evident from the data and further investigation was beyond the scope of this study. A three to one higher failure rate of plastic linear devices over ceramic linear was observed with concern, and the data was reviewed to more fully understand the cause. Though no clear causes or corrective actions were identified, this observation will likely lead to further investigation by Honeywell.

1.3 Abbreviations

The following abbreviations are used within this document:

ATP - acceptance test procedure

Bip. - bipolar (Microcircuit Technology Family)

CDIP - Ceramic Dual In-Line Package

Dig. - Digital

EEPROM - Electrically Erasable Programmable Read Only Memory

EOS - electrical overstress

ESD - electrostatic discharge

FAB - fabrication (Refers to the fabrication process for Microcircuit die)

FET - field effect transistor

JLCC - J leaded ceramic chip carrier

Lin. - linear

LRU - line replaceable unit

LSIC - large scale integrated circuit (>100 Gates)

Mem. - memory

MSIC - medium scale integrated circuit (20-100 Gates)

MOS - metal oxide semiconductor (Microcircuit Technology Family)

MTBF - mean time between failure

MTBUR - mean time between unscheduled removal

PAL - programmablearray logic

PDIP - plastic dual in-line package

PGA - pin grid array

PLCC - plastic leaded chip carrier

PQFP - plastic quad flat pack (package)

Proc. - processor

RAM - random access memory

REM - Removal of electronic microcircuit

ROM - read only memory

SOIC - small outline integrated circuit (package)

SOJ - small outline J leaded (package)

SOL - small outline large (package)

SRAM - Static Random Access Memory

SSIC - small scale integrated circuit (1-20 Gates)

µProc. - micro processor

2.0 Product Descriptions

2.1 LRU 1

LRU 1 is an all electronics unit consisting of 20 circuit card assemblies and a total parts count of approximately 2,500 electrical parts. The unit is normally mounted in the aircraft's equipment bay and is forced air cooled. The unit was designed using hermetic microcircuits that were MIL-STD-883 class B. In a few instances military standard microcircuits were not available. In these instances the devices were required to meet the following minimum requirements:

- Temperature Range— -55°C to +125°C
- Package Type—Hermetic (Ceramic DIP, Metal Can etc.)
- Supplier Burn-in & Tri-Temp. Testing—Per MIL-STD-883 Method 5004

LRU 1 has been in revenue service aboard commercial air transport aircraft since 1984 and has experienced a field reliability (MTBF) of greater than 100,000 equipment operating hours, compared to a predicted field reliability of 8,400 operating hours.

A listing of the part types and quantities of microcircuits used in LRU 1, including their package types, are shown in Table 2.1-1 through Table 2.1-3 for each of the three part families (Digital SSI/MSI, Digital Memory/LSI, Linear).

Table 2.1-1. Part Types for LRU 1 Digital SSI/MSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
54LS138	Dig. msic Bip	1	CDIP	16
4017B	Dig. msic mos	1	CDIP	16
4018B	Dig. msic mos	1	CDIP	16
4022B	Dig. msic mos	1	CDIP	16
45208B	Dig. msic mos	1	CDIP	16
4520B	Dig. msic mos	2	CDIP	16
4528B	Dig. msic mos	2	CDIP	16
54F138	Dig. msic mos	1	CDIP	14
54F245	Dig. msic mos	1	CDIP	20
54HC138	Dig. msic mos	23	CDIP	16
54HC139	Dig. msic mos	5	CDIP	16
54HC164	Dig. msic mos	22	CDIP	14
54HC174	Dig. msic mos	11	CDIP	16

Table 2.1-1. Part Types for LRU 1 Digital SSI/MSI Microcircuits (Concluded)

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
54HC175	Dig. msic mos	5	CDIP	16
54HC240	Dig. msic mos	2	CDIP	20
54HC244	Dig. msic mos	29	CDIP	20
54HC245	Dig. msic mos	3	CDIP	20
54HC373	Dig. msic mos	2	CDIP	20
54HC374	Dig. msic mos	32	CDIP	20
54HC393	Dig. msic mos	2	CDIP	14
5406	Dig. ssic Bip.	3	CDIP	14
4001B	Dig. ssic mos	6	CDIP	14
4011UB	Dig. ssic mos	1	CDIP	14
4013B	Dig. ssic mos	3	CDIP	14
4014B	Dig. ssic mos	2	CDIP	16
4023B	Dig. ssic mos	1	CDIP	14
4040B	Dig. ssic mos	2	CDIP	16
4045B	Dig. ssic mos	1	CDIP	16
4049UB	Dig. ssic mos	4	CDIP	16
4050B	Dig. ssic mos	9	CDIP	16
4082B	Dig. ssic mos	1	CDIP	14
54HC00	Dig. ssic mos	15	CDIP	14
54HC02	Dig. ssic mos	3	CDIP	14
54HC03	Dig. ssic mos	2	CDIP	14
54HC04	Dig. ssic mos	7	CDIP	14
54HC07	Dig. ssic mos	1	CDIP	14
54HC10	Dig. ssic mos	3	CDIP	14
54HC125	Dig. ssic mos	1	CDIP	14
54HC21	Dig. ssic mos	3	CDIP	14
54HC71	Dig. ssic mos	1	CDIP	14
54HC74	Dig. ssic mos	15	CDIP	14
15125	Dig. ssic Bip	1	CDIP	14

Table 2.1-2. Part Types for LRU 1 Digital Memory/LSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
5213	PROM 16K mos	1	CDIP	24
93427	PROM 1K Bip	4		
27259	PROM 4K Bip	1		
6116	RAM 16K mos	2	CDIP	24
2764	ROM 64K mos	8	CDIP	28
8031	uProc 8B mos	2	CDIP	40

Table 2.1-3. Part Types for LRU 1 Linear Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
1230	Lin. Bip (<50T)	28	CDIP	20
78M12	Lin. Bip (<50T)	2	CAN	3
580	Lin. Bip (<50T)	1	CAN	3
581	Lin. Bip (<50T)	1	CAN	3
LF155	Lin. Bip (<50T)	14	CAN	8
LF156	Lin. Bip (<50T)	13	CAN	8
LH0070	Lin. Bip (<50T)	1	CAN	3
LM111	Lin. Bip (<50T)	13	CAN	8
LM140	Lin. Bip (<50T)	1	CAN	2
LM149	Lin. Bip (<50T)	4	CDIP	14
LM193	Lin. Bip (<50T)	2	CAN	8
LM741	Lin. Bip (<50T)	1	CAN	8
OP-07A	Lin. Bip (<50T)	2	CAN	8
1536	Lin. Bip (<50T)	2	CDIP	18
574	Lin. Bip (>50T)	1	CDIP	28
LF11201	Lin. Bip (>50T)	1	CDIP	16
LM119	Lin. Bip (>50T)	1	CDIP	14
LM148	Lin. Bip (>50T)	14	CDIP	14
7572	Lin. mos (<50T)	1	CDIP	24
506	Lin. mos (>50T)	6	CDIP	28

2.2 LRU 2

LRU 2 is an electronic sensor unit consisting of 19 circuit card assemblies and a sensor assembly with a total parts count of approximately 3000 electrical parts. The unit is normally mounted in the aircraft's equipment bay and is forced air cooled. The unit was designed using hermetic microcircuits that were MIL-STD-883 class B. In a few

instances military standard microcircuits were not available. In these instances the devices were required to meet the following minimum requirements:

- Temperature Range— -55°C to +125°C
- Package Type—Hermetic (Ceramic DIP, Metal Can etc.)
- Supplier Burn-in & Tri-Temp. Testing—Per MIL-STD-883 Method 5004

LRU 2 has been in revenue service aboard commercial air transport aircraft since 1982 and has experienced a field reliability (MTBF) of 13,500 equipment operating hours, compared to a predicted field reliability of 7,800 operating hours.

A listing of the part types and quantities of microcircuits used in LRU 2, including package types, are shown in Table 2.2-1 through Table 2.2-3 for each of the three part families (Digital SSI/MSI, Digital Memory/LSI, Linear).

Table 2.2-1. Part Types for LRU-2 Digital SSI/MSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
4066B	Dig. msic mos	6	CDIP	14
4053B	Dig. msic mos	1	CDIP	16
9433026	Dig. lsic mos	1	CDIP	40
10089805	Dig. lsic mos	2	CDIP	68
10089806	Dig. lsic mos	1	CDIP	68
10089807	Dig. lsic mos	1	CDIP	68
10092098	Dig. lsic mos	1	CDIP	40
54LS138	Dig. msic Bip	1	CDIP	16
54LS158	Dig. msic Bip	1	CDIP	16
54LS161	Dig. msic Bip	1	CDIP	16
54LS174	Dig. msic Bip	1	CDIP	16
54LS244	Dig. msic Bip	2	CDIP	20
54LS245	Dig. msic Bip	6	CDIP	20
54LS273	Dig. msic Bip	1	CDIP	20
54LS367	Dig. msic Bip	2	CDIP	16
54LS374	Dig. msic Bip	3	CDIP	20
25L04	Dig. msic Bip	1	CDIP	24
14532B	Dig. msic mos	1	CDIP	16
40161B	Dig. msic mos	1	CDIP	16
4022B	Dig. msic mos	2	CDIP	16
4051B	Dig. msic mos	8	CDIP	16

Table 2.2-1. Part Types for LRU-2 Digital SSI/MSI Microcircuits (Concluded)

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
4520B	Dig. msic mos	5	CDIP	16
4555B	Dig. msic mos	1	CDIP	16
26001847	Dig. msic mos pal	1	CDIP	20
PAL16L8	Dig. msic mos pal	1	CDIP	20
5407J	Dig. ssic Bip	3	CDIP	14
54LS00	Dig. ssic Bip	2	CDIP	14
54LS02	Dig. ssic Bip	3	CDIP	14
54LS04	Dig. ssic Bip	11	CDIP	14
54LS05	Dig. ssic Bip	1	CDIP	14
54LS08	Dig. ssic Bip	1	CDIP	14
54LS27	Dig. ssic Bip	2	CDIP	20
54LS30	Dig. ssic Bip	1	CDIP	14
54LS33	Dig. ssic Bip	1	CDIP	14
54LS74	Dig. ssic Bip	1	CDIP	14
4085	Dig. ssic mos	2	CDIP	14
4001B	Dig. ssic mos	4	CDIP	14
4011B	Dig. ssic mos	4	CDIP	14
4013B	Dig. ssic mos	7	CDIP	14
4014B	Dig. ssic mos	1	CDIP	16
4023B	Dig. ssic mos	1	CDIP	14
4024B	Dig. ssic mos	1	CDIP	14
4025B	Dig. ssic mos	1	CDIP	14
4027B	Dig. ssic mos	1	CDIP	16
4040B	Dig. ssic mos	1	CDIP	16
4043B	Dig. ssic mos	3	CDIP	16
4049UB	Dig. ssic mos	9	CDIP	16
4050B	Dig. ssic mos	3	CDIP	16
4071B	Dig. ssic mos	2	CDIP	14
4076B	Dig. ssic mos	2	CDIP	16
4081B	Dig. ssic mos	2	CDIP	14
4094B	Dig. ssic mos	4	CDIP	16
54HC03	Dig. ssic mos	1	CDIP	14
54175	Dig. ssic mos	1	CDIP	16

Table 2.2-2. Part Types for LRU 2 Digital Memory/LSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
L1A2091	PGA (880G/40P)	1	CDIP	40
L1A2092	PGA (880G/40P)	1	PGA	84
10092421-101	Proc. 8B mos	1	CDIP	40
5301	Proc. mos	1	PGA	120
6116	RAM 16k mos	4	CDIP	24
3341	RAM 256B mos	6	CDIP	16
27LS03	RAM 64B Bip	3	CDIP	16
28C16	ROM 16K mos	2	CDIP	24
54S287	ROM 1K Bip	8	CDIP	16
27C256	ROM 256K mos	2	CDIP	28
ER2051HR	ROM 512B mos	1	CDIP	28

Table 2.2-3. Part Types for LRU 2 Linear Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
9615	Lin. Bip (<50)	1	CDIP	16
10092014	Lin. Bip (<50)	1	CDIP	16
590	Lin. Bip (<50)	9	CAN	3
55114	Lin. Bip (<50)	1	CDIP	16
LF155AH	Lin. Bip (<50)	3	CAN	8
LF156H	Lin. Bip (<50)	5	CAN	8
LF198H	Lin. Bip (<50)	4	CAN	8
LM108AH	Lin. Bip (<50)	21	CAN	8
LM111H	Lin. Bip (<50)	3	CAN	8
LM117K	Lin. Bip (<50)	2	CAN	3
LM137H	Lin. Bip (<50)	1	CAN	3
LM556J	Lin. Bip (<50)	1	CDIP	14
LM741H	Lin. Bip (<50)	3	CAN	8
MUX08	Lin. Bip (<50)	3	CDIP	16
OP07AH	Lin. Bip (<50)	3	CAN	8
OP15AH	Lin. Bip (<50)	3	CAN	8
OP16AH	Lin. Bip (<50)	6	CAN	3
78A1301XX	Lin. Bip (>50)	3	CAN	3
41140	Lin. Bip (>50)	1	CDIP	24
2620	Lin. Bip (>50)	6	CAN	8
LF11201D	Lin. Bip (>50)	4	CDIP	16

Table 2.2-3. Part Types for LRU 2 Linear Microcircuits (Concluded)

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
LM119	Lin. Bip (>50)	3	CDIP	14
LM124	Lin. Bip (>50)	7	CDIP	14
LM139J	Lin. Bip (>50)	20	CDIP	14
LM148	Lin. Bip (>50)	7	CDIP	14
M14504B	Lin. mos (<50)	3	CDIP	16
M14504B	Lin. mos (<50T)	3	CDIP	16

2.3 LRU 3

LRU 3 is an electronic sensor unit consisting of 14 circuit card assemblies and a sensor assembly with a total parts count of approximately 2700 electrical parts. The unit is normally mounted in the aircraft's equipment bay and is forced air cooled. The unit was designed using hermetic microcircuits that were MIL-STD-883 class B. In a few instances military standard microcircuits were not available. In these instances the devices were required to meet the following minimum requirements:

- Temperature Range— -55°C to +125°C
- Package Type—Hermetic (Ceramic DIP, Metal Can etc.)
- Supplier Burn-in & Tri-Temp. Testing—Per MIL-STD-883 Method 5004

LRU 3 has been in revenue service aboard commercial air transport aircraft since 1988 and has experienced a field reliability (MTBF) of 14,500 equipment operating hours, compared to a predicted field reliability of 15,000 operating hours.

A listing of the part types and quantities of microcircuits used in LRU 3, including package types, are shown in Table 2.3-1 through Table 2.3-3 for each of the three part families (Digital SSI/MSI, Digital Memory/LSI, Linear).

Table 2.3-1. Part Types for LRU 3 Digital SSI/MSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
25L04	Dig. msic Bip	1	CDIP	24
54LS109	Dig. msic Bip	3	CDIP	16
54LS138	Dig. msic Bip	9	CDIP	16
54LS139	Dig. msic Bip	1	CDIP	16
54LS157	Dig. msic Bip	2	CDIP	16
54LS161	Dig. msic Bip	1	CDIP	16
54LS163	Dig. msic Bip	3	CDIP	16

Table 2.3-1. Part Types for LRU 3 Digital SSI/MSI Microcircuits (Continued)

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
54LS174	Dig. msic Bip	2	CDIP	16
54LS175	Dig. msic Bip	1	CDIP	16
54LS182	Dig. msic Bip	1	CDIP	16
54LS244	Dig. msic Bip	15	CDIP	20
54LS251	Dig. msic Bip	2	CDIP	16
54LS253	Dig. msic Bip	2	CDIP	16
54LS259	Dig. msic Bip	1	CDIP	16
54LS273	Dig. msic Bip	5	CDIP	20
54LS367	Dig. msic Bip	4	CDIP	16
54LS373	Dig. msic Bip	4	CDIP	20
54LS374	Dig. msic Bip	7	CDIP	20
54LS393	Dig. msic Bip	1	CDIP	14
54LS92	Dig. msic Bip	3	CDIP	14
40161B	Dig. msic mos	2	CDIP	16
4020B	Dig. msic mos	2	CDIP	16
4051B	Dig. msic mos	7	CDIP	16
4052B	Dig. msic mos	2	CDIP	16
4053B	Dig. msic mos	1	CDIP	16
4066B	Dig. msic mos	7	CDIP	14
54FCT138	Dig. msic mos	8	CDIP	16
54HC138	Dig. msic mos	1	CDIP	16
54HC139	Dig. msic mos	2	CDIP	16
54HC154	Dig. msic mos	1	CDIP	24
54HC161	Dig. msic mos	1	CDIP	16
54HC244	Dig. msic mos	3	CDIP	20
54HC245	Dig. msic mos	1	CDIP	20
54HC374	Dig. msic mos	2	CDIP	20
54HC4053	Dig. msic mos	1	CDIP	16
3282	Dig. msic mos	4	CDIP	40
82C54	Dig. msic mos	1	CDIP	24
PAL16L8	Dig. msic mos pal	3	CDIP	20
54LS00	Dig. ssic Bip	4	CDIP	14
54LS02	Dig. ssic Bip	2	CDIP	14
54LS03	Dig. ssic Bip	1	CDIP	14
54LS04	Dig. ssic Bip	7	CDIP	14
54LS06	Dig. ssic Bip	1	CDIP	14

Table 2.3-1. Part Types for LRU 3 Digital SSI/MSI Microcircuits (Concluded)

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
54LS08	Dig. ssic Bip	2	CDIP	14
54LS10	Dig. ssic Bip	2	CDIP	14
54LS15	Dig. ssic Bip	1	CDIP	16
54LS20	Dig. ssic Bip	3	CDIP	14
54LS21	Dig. ssic Bip	2	CDIP	14
54LS232	Dig. ssic Bip	1	CDIP	16
54LS240	Dig. ssic Bip	1	CDIP	20
54LS241	Dig. ssic Bip	2	CDIP	14
54LS27	Dig. ssic Bip	1	CDIP	14
54LS30	Dig. ssic Bip	3	CDIP	16
54LS32	Dig. ssic Bip	4	CDIP	14
54LS33	Dig. ssic Bip	2	CDIP	14
54LS368	Dig. ssic Bip	1	CDIP	14
54LS74	Dig. ssic Bip	5	CDIP	16
14504B	Dig. ssic mos	1	CDIP	14
4001B	Dig. ssic mos	3	CDIP	14
4011UB	Dig. ssic mos	4	CDIP	14
4013B	Dig. ssic mos	5	CDIP	14
4023B	Dig. ssic mos	1	CDIP	14
4025B	Dig. ssic mos	3	CDIP	14
4040B	Dig. ssic mos	2	CDIP	16
4049UB	Dig. ssic mos	5	CDIP	16
4050B	Dig. ssic mos	3	CDIP	16
54F32	Dig. ssic mos	1	CDIP	14
54HC00	Dig. ssic mos	1	CDIP	14
54HC02	Dig. ssic mos	3	CDIP	14
54HC05	Dig. ssic mos	4	CDIP	14
54HC10	Dig. ssic mos	1	CDIP	14
54HC125	Dig. ssic mos	4	CDIP	14
54HC20	Dig. ssic mos	1	CDIP	14

Table 2.3-2. Part Types for LRU 3 Digital Memory/LSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
10071451	Dig. lsic mos	6	CDIP	28
10071452	Dig. lsic mos	2	CDIP	40
10071453	Dig. lsic mos	1	CDIP	40
10071454	Dig. lsic mos	1	CDIP	40
10071455	Dig. lsic mos	1	CDIP	40
10075553	Dig. lsic mos	1	CDIP	40
10082097	Dig. lsic mos	1	CDIP	40
10082098	Dig. lsic mos	1	CDIP	24
10089806	Dig. lsic mos	1		
6116	RAM 16K mos	6	CDIP	24
6168	RAM 16K mos	4		
2212	RAM 1K mos	4	CDIP	16
27128	ROM 128K mos	4	CDIP	28
2816A	ROM 16K mos	3	CDIP	24
54S287	ROM 1K Bip	8	CDIP	16
27LS19	ROM 256B Bip	1	CDIP	16
93448DM	ROM 4K Bip	2		
27512	ROM 512K mos	2	CDIP	28
2764	ROM 64K mos	4	CDIP	28
82S181	ROM 8K Bip	6	CDIP	20
68000-8	uProc 16B mos	2	CDIP	64

Table 2.3-3. Part Types for LRU 3 Linear Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
111	Lin. Bip (<50T)	3	CAN	8
556	Lin. Bip (<50T)	1	CDIP	14
562	Lin. Bip (<50T)	1	CDIP	24
2702	Lin. Bip (<50T)	1	CDIP	14
9614	Lin. Bip (<50T)	1	CDIP	16
11508	Lin. Bip (<50T)	3	CDIP	16
1524B	Lin. Bip (<50T)	1	CDIP	16
155A	Lin. Bip (<50T)	3	CAN	8
2001H	Lin. Bip (<50T)	1	CDIP	16
5492A	Lin. Bip (<50T)	1	CDIP	14
584	Lin. Bip (<50T)	1	CAN	8
590	Lin. Bip (<50T)	9	CAN	3
LF156	Lin. Bip (<50T)	2	CAN	8
LF198	Lin. Bip (<50T)	3	CAN	8
LH0002	Lin. Bip (<50T)	3	CAN	8
LM108A	Lin. Bip (<50T)	19	CAN	8
LM117K	Lin. Bip (<50T)	1	CAN	3
LM199	Lin. Bip (<50T)	1	CAN	4
LM741	Lin. Bip (<50T)	3	CAN	8
OP-07A	Lin. Bip (<50T)	4	CAN	8
OP-15A	Lin. Bip (<50T)	3	CAN	8
OP-16A	Lin. Bip (<50T)	6	CAN	3
REF02A	Lin. Bip (<50T)	1	CAN	8
9615	Lin. Bip (<50T)	1	CDIP	16
LM119	Lin. Bip (>50T)	3	CDIP	14
2901	Lin. Bip (>50T)	4	CDIP	14
11201	Lin. Bip (>50T)	1	CDIP	14
10071488	Lin. Bip (>50T)	3	CAN	3
2620	Lin. Bip (>50T)	6	CAN	8
LF147	Lin. Bip (>50T)	8	CDIP	14
LF444	Lin. Bip (>50T)	6	CDIP	14
LM124A	Lin. Bip (>50T)	4	CDIP	14
LM139	Lin. Bip (>50T)	20	CDIP	14
LM148	Lin. Bip (>50T)	8	CDIP	14
M14504B	Lin. mos (<50T)	3	CDIP	16
7582	Lin. mos (>50T)	1	CDIP	28

2.4 LRU 4

LRU 4 is an electronic sensor unit consisting of 17 circuit card assemblies and a sensor assembly with a total parts count of approximately 2675 electrical parts. The unit is normally mounted in the aircraft's equipment bay and is forced air cooled. The unit was designed using a combination of plastic and hermetic microcircuits. A total of 121 out of 219 total microcircuits were commercial plastic devices all of which met Honeywell qualification requirements. Of the 121 plastic devices 42 of these devices received 100% burn-in and three temperature testing (-40°C, +25°C and +125°C). Those devices not receiving 100% screening (see LRU 4 part type table for identification of these parts) fall into two groups. 58 plastic SSI/MSI devices received a lot sample screen performed by a 3rd party test house. This was done after evaluation of supplier fallout and performance data over the extended temperature range. An additional 21 plastic devices (18 linear, 3 memory) received no screening of any kind though guarantees of electrical performance over temperature were obtained from the supplier and extensive over temperature testing is performed by Honeywell on the assembly they are used in. Most of the screening performed on the plastic parts was done so by the supplier with only a few performed by a 3rd party test facility.

All of the hermetic devices were military temperature range devices which received 100% burn-in and three temperature testing by the supplier. A few of these hermetic devices were MIL-STD-883 compliant.

LRU 4 has been in revenue service aboard commercial air transport aircraft since 1991 and has experienced a field reliability (MTBF) of 13,000 equipment operating hours, compared to a predicted field reliability of 11,000 operating hours.

A listing of the part types and quantities of microcircuits used in LRU 4, including package types, are shown in Table 2.4-1 through Table 2.4-3 for each of the three part families (Digital SSI/MSI, Digital Memory/LSI, Linear).

Table 2.4-1. Part Types for LRU 4 Digital SSI/MSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
75188	Dig. msic Bip	1	SOIC	14
75189	Dig. msic Bip	1	SOIC	14
74AC174	Dig. msic mos	1	SOIC	16
74AC244	Dig. msic mos	8	SOIC	20
74AC245	Dig. msic mos	12	SOIC	20
74AC257	Dig. msic mos	2	SOIC	16
74ACT244	Dig. msic mos	2	SOIC	20
74ACT245	Dig. msic mos	2	SOIC	20
74ACT573	Dig. msic mos	12	SOIC	20
74F175	Dig. msic mos	1	SOIC	16
74AC00	Dig. ssic mos	4	SOIC	14
74AC02	Dig. ssic mos	1	SOIC	14

Table 2.4-1. Part Types for LRU 4 Digital SSI/MSI Microcircuits (Concluded)

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
74AC04	Dig. ssic mos	1	SOIC	14
74AC08	Dig. ssic mos	3	SOIC	14
74AC32	Dig. ssic Bip	1	SOIC	14
74AC74	Dig. ssic mos	5	SOIC	14
74ACT00	Dig. ssic mos	1	SOIC	14
74F04	Dig. ssic mos	1	SOIC	14
74HCU04	Dig. ssic mos	1	SOIC	14
5407	Dig. ssic Bip	1	CER DIP	14

Table 2.4-2. Part Types for LRU Digital Memory/LSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
26000893	PGA (880G/40P)	1	CER DIP	40
1800-P	PGA (880G/40P) HCMOS	3	JLCC	68
1810	PGA (880G/40P) HCMOS	3	JLCC	68
910	PGA (880G/40P) HCMOS	2	JLCC	44
L1A5065	PGA (8KG/84P) HCMOS	1	PGA	120
L1A5066	PGA (8KG/84P) HCMOS	1	PGA	100
80960	Proc. 32B MOS	1	PGA	132
6116	RAM 16K mos	2	CER DIP	24
27210	ROM 1M mos	4	CER DIP	40
28C64	ROM 64K mos	1	CER DIP	28
VGM7812	PGA (8KG/84P) HCMOS	1	PLCC	84
71256	RAM 256K mos	12	PLCC	32
7201	RAM 4K mos	2	PLCC	32
93C46	ROM 1K mos	3	SOIC	8
7C291	ROM 16K mos	1	SOIC	24

Table 2.4-3. Part Types for LRU 4 Linear Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
588	Lin. Bip (<50T)	1	CER DIP	16
590	Lin. Bip (<50T)	9	CAN	3
LF198	Lin. Bip (<50T)	3	CAN	8
LH0002	Lin. Bip (<50T)	15	CAN	8
LM113	Lin. Bip (<50T)	1	CAN	3
LM117	Lin. Bip (<50T)	1	CAN	3
LM185	Lin. Bip (<50T)	1	CAN	2
LM199	Lin. Bip (<50T)	1	CAN	4
1846	Lin. Bip (<50T)	1	CER DIP	16
OP-07A	Lin. Bip (<50T)	6	CAN	8
OP-16A	Lin. Bip (<50T)	6	CAN	3
1705J	Lin. Bip (<50T)	4	CER DIP	8
40914	Lin. Bip (>50T)	1	CAN	3
684	Lin. Bip (>50T)	1	CER DIP	14
7672	Lin. Bip (>50T)	1	CER DIP	24
LF147	Lin. Bip (>50T)	1	CER DIP	14
LM119	Lin. Bip (>50T)	3	CER DIP	14
LM139	Lin. Bip (>50T)	13	CER DIP	14
LM148	Lin. Bip (>50T)	6	CER DIP	14
OP-270	Lin. Bip (>50T)	2	CER DIP	8
507A	Lin. mos (>50T)	1	CER DIP	28
829	Lin. Bip (<50T)	6	SOIC	8
LT1013	Lin. Bip (<50T)	6	SOIC	8
LT1019	Lin. Bip (<50T)	3	SOIC	8
26007025	Lin. Bip (>50T)	1	SOIC	18
26C32	Lin. Bip (>50T)	1	SOIC	16
LM2901	Lin. Bip (>50T)	5	SOIC	14
LM319	Lin. Bip (>50T)	3	SOIC	14
1058A	Lin. Bip (>50T)	3	SOIC	16
85C30	Lin. mos (>50T)	1	PLCC	44
506	Lin. mos (>50T)	3	SOIC	28
201	Lin. mos (>50T)	5	SOIC	16
8018	Lin. mos (>50T)	5	SOIC	

2.5 LRU 5, 6, and 7

The final three LRU's make up a system, whose parts were tracked in the field independent of the LRU they were removed from. For this reason they will be treated as a system rather than individual LRU's.

LRU 5 is an all electronic unit consisting of 33 circuit card assemblies and a total parts count of approximately 3700 electrical parts. The unit consists of power supply processor, I/O, receiver and transmitter functions. LRU 5 is normally mounted in the aircraft's equipment bay and is passively cooled. LRU 5 has been in revenue service aboard commercial air transport aircraft since 1990 and has experienced a field reliability (MTBF) of 13,500 operating hours compared to a predicted field reliability of 9,700 Operating Hours.

LRU 6 is an all electronic unit consisting of 21 circuit card assemblies and a total parts count of approximately 1700 electrical parts. The unit consists of Processor, Interface, Power Supply, Receiver and Transmitter functions. LRU 6 is normally mounted in the aircraft's equipment bay and is passively cooled. LRU 6 has been in revenue service aboard commercial air transport aircraft since 1989 and has experienced a field reliability (MTBF) of 21,000 operating hours compared to a predicted field reliability of 19,000 operating hours.

LRU 7 is an all electronics unit consisting of 13 circuit card assemblies and a total parts count of 830 electrical parts. The unit consists of processor, I/O, Power Supply and Display functions. LRU 7 is normally mounted in the aircraft's cockpit and is passively cooled. LRU 7 has been in revenue service aboard commercial air transport aircraft since 1990 and has experienced a field reliability (MTBF) of 12,500 operating hours compared to a predicted field reliability of 24,000 Operating Hours. This is the only LRU whose field reliability is lower than predicted. There is no evidence that this is due to the use of plastic microcircuits but may be related to it being the only cockpit mounted display device in the study.

All three of these LRU's were designed using plastic surface mount microcircuits to the maximum extent possible. All of the plastic devices received 100% screening (burn-in and tri-temp. testing) where most of the screening was performed at a 3rd party test facility. There was limited use of hermetic microcircuits which were either 883C compliant or 883C equivalent. Only the plastic packaged microcircuits have been tracked in the field and are used in this study.

A listing of the part types and total quantities of microcircuits used in LRU's 5, 6 and 7, including package types, are shown in Table 2.5-1 through Table 2.5-3 for each of the three part families (Digital SSI/MSI, Digital Memory/LSI, Linear).

Table 2.5-1. Part Types for LRU 5, 6, and 7 Digital SSI/MSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
74ALS161	Dig. msic Bip.	1	SOIC	16
74AC174	Dig. msic mos	2	SOIC	16
74AC74	Dig. msic mos	1	SOIC	14
74FCT138	Dig. msic mos	10	SOL	16
74FCT244	Dig. msic mos	27	SOL	20

Table 2.5-1. Part Types for LRU 5, 6, and 7 Digital SSI/MSI Microcircuits (Continued)

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
74FCT245	Dig. msic mos	26	SOL	20
74FCT273	Dig. msic mos	13	SOL	20
74FCT374	Dig. msic mos	10	SOL	20
74FCT377	Dig. msic mos	2	SOL	20
74HC240	Dig. msic mos	28	SOL	20
74HC244	Dig. msic mos	4	SOL	20
74HC273	Dig. msic mos	4	SOL	20
74HC393	Dig. msic mos	2	SOIC	14
74HC4538	Dig. msic mos	3	SOIC	16
74HC74	Dig. msic mos	3	SOIC	14
74HCT138	Dig. msic mos	2	SOIC	16
74HCT244	Dig. msic mos	4	SOL	20
74HCT245	Dig. msic mos	2	SOL	20
74HCT373	Dig. msic mos	1	SOL	20
74HCT374	Dig. msic mos	3	SOL	20
PAL16L8	Dig. msic mos PAL	1	PLCC	20
PAL16L8A	Dig. msic mos PAL	1	PLCC	20
PAL16L8B-2	Dig. msic mos PAL	9	PLCC	20
PAL16R6B-2	Dig. msic mos PAL	2	PLCC	20
PAL16R6B-4	Dig. msic mos PAL	1	PLCC	20
PAL16R8B-2	Dig. msic mos PAL	1	PLCC	20
PALC22V10	Dig. msic mos PAL	1	PLCC	28
PALC22V10	Dig. msic mos PAL	10	PLCC	28
74F00	Dig. ssic Bip.	5	SOIC	14
74F109	Dig. ssic Bip.	5	SOIC	16
74F20	Dig. ssic Bip.	1	SOIC	14
74LS123	Dig. ssic Bip.	1	SOIC	16
74AC14	Dig. ssic mos	2	SOIC	14
74AC32	Dig. ssic mos	4	SOIC	14
74HC00	Dig. ssic mos	1	SOIC	14
74HC02	Dig. ssic mos	3	SOIC	16
74HC08	Dig. ssic mos	1	SOIC	14
74HC14	Dig. ssic mos	5	SOIC	14
74HCT04	Dig. ssic mos	13	SOIC	14
74HCT157	Dig. ssic mos	1	SOIC	16
74HCT158	Dig. ssic mos	2	SOIC	16

Table 2.5-2. Part Types for LRU 5, 6, and 7 Digital Memory/LSI Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
ASIC	LSI 8000g/68p	4	PLCC	68
1800	LSI 8000g/68p	1	PLCC	68
ASIC	LSI 8000g/84p	4	PLCC	84
ASIC	LSI 8000g/84p	3	PLCC	84
ASIC	LSI 8000g/84p	1	PLCC	84
ASIC	LSI 8000g/84p	2	PLCC	84
ASIC	LSI 8000g/84p	2	PLCC	84
ASIC	LSI 8000g/84p	2	PLCC	84
600	LSI 880g/40p	2	PLCC	28
44C256	MEM, RAM mos 1mb	4	SOJ	26
71256	MEM, RAM mos 256kb	20	PLCC	32
81461	MEM, RAM mos 256kb	4	SOJ	26
7198L	MEM, RAM mos 64kb	4	SOL	24
7202LA	MEM, RAM mos 8kb	8	PLCC	32
27S19	MEM, ROM Bip 256b	1	PLCC	20
27S19	MEM, ROM Bip 256b	4	PLCC	20
28C256	MEM, ROM mos 256kb	24	PLCC	32
7C225	MEM, ROM mos 4kb	2	PDIP	24
28C64	MEM, ROM mos 64kb	9	PLCC	32
34010	PROC. mos 32b	1	PLCC	68

Table 2.5-3. Part Types for LRU 5, 6, and 7 Linear Microcircuits

Generic Part Type	Description	Part Type Quantity	Package Type	Pin Count
LM211	Lin. Bip <50T	12	SOIC	16
LM218	Lin. Bip <50T	13	SOIC	08
LM219	Lin. Bip <50T	2	SOIC	14
LM336	Lin. Bip <50T	4	SOIC	08
LM348	Lin. Bip <50T	9	SOIC	14
LM348	Lin. Bip <50T	1	SOIC	14
LM393	Lin. Bip <50T	1	SOIC	08
LP311	Lin. Bip <50T	1	SOIC	08
LP339	Lin. Bip <50T	3	SOIC	14
RMS-5 MIXER	Lin. Bip <50T	2		SMT
TL7757	Lin. Bip <50T	2	PDIP	18
2003	Lin. Bip <50T	1	SOIC	16
2803	Lin. Bip <50T	6	SOL	18
26LS31	Lin. Bip >50T	3	SOIC	16
26LS32	Lin. Bip >50T	2	SOIC	16
7528	Lin. Bip >50T	8	PLCC	20
667	Lin. Bip >50T	1	PLCC	28
7528	Lin. Bip >50T	2	PLCC	20
LM2901	Lin. Bip >50T	4	SOIC	14
LM2902	Lin. Bip >50T	1	SOIC	14
LM2903	Lin. Bip >50T	1	SOIC	08
MP7684	Lin. Bip >50T	2	SOP	28
064	Lin. Bip >50T	8	SOIC	14
3526	Lin. Bip >50T	3	PDIP	18
2243	Lin. Bip >50T	1	PDIP	08
7555	Lin. mos <50T	1	SOIC	08
508	Lin. mos >50T	3	SOIC	16
574	Lin. mos >50T	1	PLCC	28
201	Lin. mos >50T	1	SOIC	16
201A	Lin. mos >50T	4	SOIC	16
271	Lin. mos >50T	1	SOIC	16
506	Lin. mos >50T	1	PLCC	28
549	Lin. mos >50T	4	PLCC	20
5537	Lin. mos >50T	1	SOIC	14

3.0 Field Assessment

3.1 Field Data Sources and Analysis Process

The analysis process used differs between LRU's 1-4 compared to LRU's 5-7.

LRU's 1 - 4—Honeywell conducts periodic reviews of field reliability for all products. These reviews include measurements of field mean time between failure (MTBF) and mean time between unscheduled removal (MTBUR). Trend analysis is performed looking at both removal causes and assembly level replacements to identify correctable problems. Analysis to the piece part level in not typically performed. These reports formed the starting point for this analysis.

Honeywell's SUMAR database system contains all repair information for both the LRU level and the assembly level. To gain visibility of the LRU and assembly level repair one or two SUMAR records may be required. In instances where a Honeywell service center performs the entire repair to the piece part level, all information would be contained in one SUMAR record. In many instances a Honeywell service center will repair an LRU to the assembly level, then return the faulty assembly to the factory for piece part level repair. In this later case two SUMAR's would be written, one for the LRU and one for the faulty assembly. This study required that the assembly level repair information be identified for each of the confirmed LRU level faults. When separate LRU and assembly SUMAR's need to be linked, the link can be accomplished by the assembly part number and its serial number which should be contained on both SUMAR's. There are instances where a lack of information on one of the SUMAR's makes it impossible to make the link resulting in lost information.

Not all circuit card failures can economically be repaired due to the level of damage, such as a part burning the board material. In these instances the circuit card is scrapped and no part failure information is recorded. Though occurrences of this are rare, they can account for additional lost piece part fault information..

An analysis was made of all records where the LRU removal was traced to the piece part level. The records include:

- Reason for LRU removal from aircraft
- Repair technician's test findings
- A coded reason for removed of each component

The review of this data consisted of a verification that the part(s) removed related the original aircraft fault description. Where multiple parts are replaced the likely cause of the fault is determined based on the available information and the coded reason for removal of each part.

Operators of commercial air transport aircraft maintain flight hour logs for each aircraft. Flight hours are the time measured between lift off and landing of an aircraft. This data is available to Honeywell either directly from airline operators or from the airframe manufacturer.

For this report aircraft flight hour information was summed for the specified time period. The sum of this flight hour data is converted to operational hours using a standard conversion factor of 1.5 operational hours per flight

hour. Operational hours are the total "ON" hours for the aircraft systems which accounts for the additional time the equipment is powered such as during taxi time and waiting time at the airport gate. The hours are converted to operational hours as this is the time unit that can be compared to the predicted failure rates which are in units of failures per million operational hours.

LRU's 5 - 7—The field reliability listed in Section 2 for these LRU's was established using the databases and process described for the earlier LRU's.

A special program was established to track the field reliability of plastic parts within LRU's 5 - 7. Since all repair of these LRU's is performed at Honeywell Service Centers, arrangements were made that all plastic parts removed would be returned to Quality Engineering and subsequently forwarded to the Component Engineering for tracking and further analysis.

A review of Honeywell's field database was performed to determine the total number of removals reported for the plastic devices. Removals solely for LRU modification or for precautionary reasons were excluded. The database was also used to determine where the part removal corrected the problem, as opposed to where the removal was the incorrect failed part. Where the removal corrected the LRU fault the part removal was categorized as a valid failure. A removal was classified as valid if a part was removed and coded to indicate that it did not correct the LRU fault, but subsequent failure analysis confirmed a part fault. Selective failure analysis was performed on the failed parts. The failure analysis results are discussed in Section 4.

Rather than tracking specific customers, for which aircraft flight hour information is available, this program tracked all fielded equipment. An alternate method to determine field usage was developed based on the average time between product shipment and installation and the average field usage in revenue service. The assumptions considered to be accurate as they are based on Honeywell's experience and feedback from customers. Specifically, the study assumed:

1) A two month interval between Honeywell shipment of the product and field installation.
2) An average field usage of 250 operating hours per month.

3.2 Failure Criteria

An LRU is considered failed if the customer's cause for removal is confirmed by means of performing an acceptance test procedure (ATP) on the LRU, by the service center or factory. LRU's returned for updating with a modification or those which pass the ATP are not classified as failures. The piece part failure criteria was discussed in the previous section.

4.0 Field Data Results

4.1 Equipment Operating Hours

The source of equipment operating hours is as described in paragraph 3.1. For each equipment type the aircraft operating hours are multiplied by the number of LRUs installed then summed. The results of this calculation and the time period used are shown in Table 4.1-1 for each equipment type.

Table 4.1-1. Total LRU Equipment Operating Hours

Equipment Type	Time Period	Total Field Operating Hours
LRU 1	July 1989 - June 1990	3,598,500
LRU 2	July 1989 - June 1990	8,584,500
LRU 3	April 1988 - June 1990	668,000
LRU 4	June 1992 - April 1994	892,000
LRU 5	Feb. 1990 - Sept. 1994	4,772,000
LRU 6	April 1989 - Sept. 1994	4,042,250
LRU 7	Feb. 1990 - Sept. 1994	9,682,750

4.2 Field Failures

The source for field failure data was described in paragraph 3.1. The following paragraphs summarize the field failure data for the LRU's.

There were difficulties with tracing the LRU failures to the piece part level for LRU's 1-4. A breakdown of the field failures for each LRU is as follows:

- LRU 1

  39 - Electronic Failures

  3 - Not Traceable To Piece Part Level

  36 - Traced To Piece Part Level

  8 - Microcircuits

  3 - Digital SSI/MSI Microcircuits

  2 - Memory/LSI Microcircuits

  3 - Linear Microcircuit

  5 - Transistors

  11 - Diode

4 - Capacitors

2 - Resistors

3 - Filters

2 - Transformers

1 - Connector

- LRU 2

680 - Confirmed LRU Failures

373 - Non Electronic Failures

307 - Electronic Failures

234 - Not Traceable To Piece Part Level

73 - Traced To Piece Part Level

26 - Microcircuits

6 - Digital SSI/MSI Microcircuits

16 - Memory/LSI Microcircuits

4 - Linear Microcircuit

11 - Transistors

9 - Diode

7 - Capacitors

4 - Resistors

2 - Crystals

10 - Filters

2 - Transformers

2 - Connectors

- LRU 3

47 - Confirmed LRU Failures

6 - Nonelectronic Failures

41 - Electronic Failures

21 - Not Traceable To Piece Part Level

20 - Traced To Piece Part Level

7 - Microcircuits

3 - Digital SSI/MSI Microcircuits

3 - Memory/LSI Microcircuits

1 - Linear Microcircuit

3 - Transistors

1 - Diode

4 - Capacitors

1 - Resistors

4 - Connectors

- LRU 4

179 - Confirmed LRU Failures

30 - Electronic Failures

19 - Not Traceable To Piece Part Level

10 - Traced To Piece Part Level

5 - Microcircuits

1 - Plastic Digital SSI/MSI Microcircuit

3 - Plastic Linear Microcircuits

1 - Ceramic Linear Microcircuit

1 - Diode

2 - Filters

2 - Connectors

1 - Workmanship

The number of microcircuit failures used for failure rate calculation was determined from the above data. Due to the electronic failures which could not be traced to the piece part level, the number of microcircuit failures, for LRU's 1 - 4, were proportionally increased. Table 4.2-1 contains the raw failure quantity, factor applied and the failure quantity used for failure rate calculation.

Table 4.2-1. Field Failure Quantities

LRU/Device Type	Raw Failure Quantity	Factor Applied	Modified Failure Quantity
LRU 1			
Dig. SSI/MSI	3	1	3
Mem./LSI	2	1	2
Linear	3	1	3
LRU 2			
Dig. SSI/MSI	6	4.205	25
Mem./LSI	16	4.205	67
Linear	4	4.205	17
LRU 3			
Dig. SSI/MSI	3	2	6
Mem./LSI	3	2	6
Linear	1	2	2
LRU 4			
PLASTIC			
Dig. SSI/MSI	1	(1)	3
Mem./LSI	0	(1)	1
Linear	3	(1)	7
HERMETIC			
Dig. SSI/MSI	0	(1)	0
Mem./LSI	0	(1)	1
Linear	1	(1)	3

NOTE: 1) No factor for this LRU see text for explanation.

The factor for LRU 4 was 3, based on the ratio of 30 confirmed electrical failures and 10 traced to the piece part level. Due to the low quantity of failures occurring it was not feasible to multiply the ratio by the number of traced piece part faults. Instead, the additional 10 faults were added based on the failure quantity and the quantity of parts used in LRU 4. The process used is described as follows:

- Since there is only one hermetic Digital SSI/MSI device in the LRU and no confirmed field failures identified, no additional failures were added to this category.

- There are a total of 19 devices each for plastic memory/LSI devices and hermetic memory/LSI devices with no confirmed failures reports, no additional failures were added to these categories.

- The plastic digital SSI/MSI and hermetic linear categories each have one confirmed failure and nearly the same quantity of devices per LRU (60 and 78 respectively). The ratio of three was applied here resulting in two additional failures being projected for these categories.

- The remaining category, plastic linear's, experienced three confirmed failures. The remaining four additional faults were added to this category.

The field data collection process for LRU's 5 - 7 differed from the other LRU's, see Paragraph 3.0 for details, such that factoring up the actual field failure quantities was not necessary. The field failure data by generic part type is shown in Table 4.2-2. The failure quantities shown represent part removals which corrected the reported fault in the LRU.

Table 4.2-2. Field Removal/Failure Quantities for LRU's 5-7

Generic	Nomenclature	REM's	Fails
74FCT244	BUFFER/DRIVER,OCTAL	5	3
74FCT245	XCVR,OCTAL BUS,3-ST	6	0
74FCT273	FLIP-FLOP,OCTAL D	2	1
74FCT374	REGISTER,OCTAL D,3-ST	1	1
74HC240	BUFFER/DRIVER,OCTAL,3-ST	3	1
74HC393	COUNTER,BINARY,4-BIT,DUAL	1	0
74HC74	OCTAL D FLIP FLOP	1	0
74HCT04	HEX INVERTERS	5	2
74HCT138	DECODER/DEMUX,3-TO-8 LINE	3	1
74HCT245	XCVR,OCTAL,3-STATE	3	0
74HCT373	LATCH,OCTAL D,3-STATE	1	0
74HCT374	FLIP-FLOP,OCTAL D,3-STATE	2	0
	SUM FOR DIGITAL SSI/MSI=	33	9
LM218	OP AMP	3	1
LM348	OP AMP,QUAD	4	0
LM393	COMPARATOR,DUAL,LO PWR	2	0
LP339	COMP.,QUAD,LOW POWER	7	1
7757	SPEECH SYNTHESIS MODULE	2	2
2803	DRIVER,OCTAL,5V TTL INPUT	3	2
7528	8 BIT D/A CONVERTER	3	2
667	DAC,12-BIT	3	0
LM2901	SLICE,4-BIT	4	1
064	OP AMP,BIFET,LOW POWER	15	2
3526	PW MODULATOR CONTROL	2	0

Table 4.2-2. Field Removal/Failure Quantities for LRU's 5-7 (Concluded)

Generic	Nomenclature	REM's	Fails
574	ADC,12-BIT MICROPROCESSOR	30	14
201	SWITCH,ANALOG,QUAD SPST	4	1
271	SWITCH,ANALOG	7	2
508	MUX,8-CHANNEL,ANALOG	3	1
506	MUX,ANALOG,16-CH,CMOS	2	0
549	MUX,ANALOG,4-CH,CMOS	6	0
5537	AMP,SAMPLE-AND-HOLD	2	2
	SUM FOR LINEAR=	102	31
ASIC	SDP185 INFC-SCX6244UEU	3	2
ASIC	UP,CUST-L1A3178MD	6	2
ASIC	RCVR/XMTR,OCTAL-609-3400	13	10
ASIC	DECODER,REPLY	5	4
ASIC	MODES VIDEO	1	1
ASIC	TCAS-PULSE DECODER	5	3
ASIC	TCAS-TRANSMIT CONTROL	6	2
600	EPLD,600 GATES	1	0
1800	EPLD,1800 GATES	2	0
71256	SRAM,32KX8/55NS	78*	61*
81461	DRAM,256K,DUAL PORT	16	7
7198L	SRAM,16KX4/70NS	2	1
7202LA	FIFO,1KX9/80NS	11	5
28C256	EEPROM,32KX8/200NS	410*	264*
28C64	EEPROM,8KX8/250NS,PG WRITE	13	3
34010	GRAPHICS,SYSTEM PROC.	8	7
	SUM FOR MEMORY/LSI=	580	372
	TOTAL=	715	412

* Failures which will not be included in the primary failure rate calculation.

Two parts, the 28C256 and 71256 both experienced a high failure rate in the field.

The primary failure mode for the 28C256 (256K EEPROM) was the inability to program selected areas of the device. The problem was identified from failure analysis of field failures. Though the part is screened by the manufacturer (burn-in and tri-temp. test) there was no indication from the manufacturer that a problem existed. The cause was identified as a weak interlayer dielectric which allowed leakage between metal I and metal II layers. The problem was corrected with a move of the fabrication facility from overseas to the US. As a result of the move of the fabrication facility changes were made to both the die and fabrication process steps.

The failure mode for the 71256 (256K SRAM) was a gross functional failure due to lack of data retention. This problem was originally identified from field failures. Once the problem was identified screening failures were also analyzed resulting in identification of the same failure mode as the field failures. Failure analysis results showed the failures were due to inferior metallization material used by the manufacturer. The problem was localized to a single datecode and corrected by the manufacturer. This instance shows the value in monitoring of screening failures. Had the screening failures been analyzed the problem would have been identified and would have reduced or eliminated the impact of field failures.

In both of these instances the manufacturer uses the same die in both the commercial products, used here by Honeywell, and in the MIL-STD-883 compliant offerings. The high level of field failures is not representative of the family and is totally unrelated to package type and package material (i.e., ceramic vs plastic). Additional scrutiny of screening data, on a real time basis, may have avoided the field problem with the 71256. These problems point out the need to take great care in the selection of suppliers and in developing cooperative relationships with them.

The resulting failure rate data will be analyzed with these failures removed. To not distort the results, all hours associated with these parts will also be removed from the failure rate calculation.

4.3 Failure Analysis Results

Failure analysis was performed on selected devices replaced during repairs of LRU's 5 - 7. The devices selected for failure analysis were selected independently of their reason for replacement, i.e. replacement corrected LRU problem, did not correct LRU problem etc. Some parts were not analyzed due to a known existing trend, in that no new information would be available if failure analysis was performed. Some parts are currently being analyzed but the results were not available for this report. Table 4.3-1 contains a breakdown of all removals relative to failure analysis results. The categories in the table are defined as follows:

- FAB—Failures that had either a die or assembly related root cause.
- EOS—Electrical overstress faults are induced failures that may arise from device testing, screening, production build, application or field usage.
- ESD—Electrostatic discharge faults are induced failures typically related to handling.
- TEMP—The device meets room temperature performance but is marginally out of specification at 125°C.
- VERIF—This category represents parts that failed failure analysis verification, but for which no root cause could be determined.
- OTHER—This category includes parts that were damaged during the replacement process such that failure analysis was not possible. Also included were parts lost during failure analysis, but were assumed to be valid failures.
- INVALID - An electrical retest of the device finds no fault with the device.

- NO FA - The failure analysis has not been completed or no failure analysis is planned.

Table 4.3-1. Failure Analysis Root Cause for all Removals

	Digital SSI/MSI	Linear	Digital MEM/LSI*	Total*	% of Total*
FAB	0	2	2 (52)	4 (5)	1.8% (7.6%)
EOS	5	5	0 (3)	10 (13)	4.4% (1.8%)
ESD	3	0	1 (2)	4 (5)	1.8% (0.7%)
TEMP	0	11	0 (0)	11 (11)	4.8% (1.5%)
VERIF.	1	3	0 (0)	4 (4)	1.8% (0.6%)
OTHER	1	3	1 (1)	5 (5)	2.2% (0.7%)
INVALID	7	33	18 (98)	58 (138)	25.5% (19.3%)
NO FA	16	45	70 (424)	131 (485)	57.7% (67.8%)
TOTAL	33	102	92 (580)	227 (715)	

* Values in parentheses represent the values with the inclusion of the 28C256 and 71256 memory devices

The FAB failure category, which represents the largest failure cause, includes those faults traceable to the manufacturer's die fabrication process. This category is driven by the Memory/LSI family and in particular the two memory devices that were previously identified as problem parts. Fifty of the 54 FAB failures occurred in these two memories with the remaining four FAB failures occurring in two different ASIC devices and two different linear devices. The two FAB failures for the ASIC devices were traced to a lifted bond and a void defect and the linear device failures were due to a pin hole in the passivation layer and a lifted ball bond.

EOS and ESD failures are elusive in both cause and corrective action. Their root cause can be a result of actions taken by the component manufacturer, during preassembly processing (component screening), by the LRU manufacturer or due to the end item user.

Component manufacturers, with few exceptions, have implemented programs that have minimized the potential for inducing EOS/ESD damage in shipped products. ESD/EOS failure modes are still present in life tests performed by manufacturers.

Preassembly processing, such as burn-in and extended temperature testing performed by third parties, remains a point where EOS/ESD damage can be induced. Though most third party facilities take all appropriate precautions, Honeywell's practice is that whenever additional processing is required, every attempt is made to have the processing performed by the manufacturer.

Though no fool proof prevention program is possible, all of Honeywell's manufacturing and repair facilities follow industry standard practices for handling of ESD sensitive components. All facilities operated by Honeywell's customers, which handle Honeywell products or perform any level of repair, also follow industry standard practices.

The "TEMP" category of faults consists solely of one linear devices (574) and this device is the leading cause of failure for the Linear family. This is likely due to the 575 being more prone to degradation of electrical

performance, particularly at the temperature extremes than the other linear devices and all digital devices. Additional investigation in this area is warranted.

The "invalid" failure category includes nearly 20% of all parts analyzed. Although most of these devices can be attributed to incorrect replacements during repair, a third of the devices were parts categorized as correcting the LRU fault. This is consistent with other analyses of part removals.

Since corrosion has been considered a predominant failure mode for plastic microcircuits, it is noteworthy that no corrosion has been seen in any failure analysis performed by Honeywell on parts failing in the field or during screening.

5.0 Reliability Predictions

5.1 Application Considerations

5.1.1 Derating Requirements

Honeywell requires, as part of the standard design process, that all products designed and built by Honeywell's Commercial Aviation Systems - Sensor Products Operation (CAS-SPO), meet Honeywell's derating criteria. The purpose of component derating is to optimize the reliability of Honeywell designs. Honeywell's derating criteria, shown in Appendix A, is to allow for the following:

1. Uncertainties which surround the rating given by the supplier.
2. Lack of knowledge concerning effects of actual environmental conditions which will be encountered.
3. Uncertainties associated with the approximate nature of mathematical models normally employed.

Derating beyond the identified criteria should not significantly improve reliability and smaller design margins could adversely affect reliability in all but special cases. Special circumstances can be such that performance tradeoffs favor exceeding these derating standard limits. Whenever this occurs, the allowable limits can be exceeded by gaining approval from the Project Engineer and the cognizant Reliability Engineer.

5.1.2 Aircraft Thermal Environment

Commercial avionics equipment is qualified per DO-160 to operate over a temperature range as wide as -55°C to +71°C, though many units have a more limited operating temperature range, such as -15°C to +65°C.

In the instances where the more limited temperature range applies, there may be additional requirements such as short term operation without cooling air and survivability temperature extremes. Survivability requirements expose equipment to wider temperature extremes (-40°C and +70°C) with the equipment operating. Though the unit is not required to meet specified performance parameters at these temperature extremes it must meet specifications when returned to nominal temperatures. Loss of cooling air requirements do not impact the equipment operating environment but may significantly change the component thermal environment (see paragraph 5.1.3 for additional details).

The actual equipment environment tends to be much more benign compared to the qualification environment. The products in this study are nearly all equipment which are mounted in an electronic equipment bay of the aircraft. This bay has a controlled environment receiving the same conditioned air as the passenger compartment. Based on inputs from aircraft manufacturers, 94.9% of the time the ambient temperature of the equipment's bay is between 18°C and 38°C with an additional 4.9% operating time between 38°C and 55°C. The remaining .2% is split between operations below 18°C and above 55°C.

5.1.3 Component Thermal Environment

It had been a common practice in aircraft design to provide flow-thru cooling air to equipment mounted in the equipment bays of commercial aircraft. Most of the products in this study were designed to accept cooling air. This allowed Honeywell to minimized the thermal temperature rise between equipment ambient temperature and part ambient temperature. Equipment so designed typically have temperature rises of from 15°C to 20°C.

The dependency on cooling air has declined, particularly on newer designs. With improved thermal management techniques Honeywell has been able to maintain the equipment to part thermal ambient temperatures to the same 15°C to 20°C level for many circuit card assemblies. Some higher power dissipating cards may have equipment to part ambient temperature rises which reach 30 or 35°C.

In either case the derating requirements must still be met. The microcircuit thermal derating requirements state that the maximum junction temperatures are 85°C under nominal operating environment (35°C equipment ambient), 110°C under a worst case continuous operating environment (65°C to 71°C equipment ambient) and supplier maximums that are typically 125°C to 150°C under high temperature transient conditions.

5.2 Predicted Reliability of LRU's Evaluated

Predicted reliability analyses have been compiled for each of the target LRU's. The prediction method is the same as that described in Appendix C. The predictions performed use earlier failure rates than are currently used on new designs to make them representative of the reliability predicted during their design and early field usage. The two most recent sets of failure rates used by Honeywell for microcircuit devices are shown in Table 5.2-1. The current failure rate values are the values used in the comparison to field results.

The reliability prediction summaries for LRU 1 thru LRU 7 are shown in Table 5.2-2 through Table 5.2-8 respectively. The summaries identify for each part grouping, the average per part failure rate, quantity of parts per grouping and total failure rate per grouping.

Table 5.2-1. Honeywell Standard Part Failure Rates

	Failure Rate (/Million Operating Hrs.)	
Part Grouping	Prior To 10/92 Update	Current Values
Small Scale, digital, bipolar (<20 gates)	0.011	0.011
Small Scale, digital, MOS (<20 gates)	0.017	0.017
Medium Scale, digital, bipolar (21-100 gates)	0.022	0.022
Medium Scale, digital, MOS (21 to 100 gates)	0.033	0.033
Large Scale, digital, bipolar (>100 gates)	0.03	0.03
Large Scale, digital, MOS (>100 gates)	0.05	0.05
Micro-Processors		
MPROC, bipolar	0.071	0.142
MPROC, (8 bit), MOS	0.096	0.192
MPROC, (16 bit), MOS	0.107	0.214
MPROC (32 bit), MOS	0.787	1.574
Analog IC's, Bipolar	0.111	0.022
Analog IC's, MOS	0.167	0.033
Memory Devices		
(E)PROM, 256 bit, bipolar	0.030	0.060
(E)PROM, 256 bit, MOS	0.044	0.088
(E)PROM, 512 bit, bipolar	0.033	0.066
(E)PROM, 512 bit, MOS	0.049	0.098
(E)PROM, 1024 bit, bipolar	0.037	0.074
(E)PROM, 1024 bit, MOS	0.153	0.106
(E)PROM, 2048 bit, bipolar	0.040	0.080
(E)PROM, 2048 bit, MOS	0.59	0.118
(E)PROM, 4096 bit, bipolar	0.044	0.088
(E)PROM, 4096 bit, MOS	0.067	0.134
(E)PROM, 8192 bit, bipolar	0.049	0.098
(E)PROM, 8192 bit, MOS	0.073	0.146
(E)PROM, 16384 bit, bipolar	0.053	0.106
(E)PROM, 16384 bit, MOS	0.081	0.162
RAM, 256 bit, bipolar	0.044	0.088
RAM, 256 bit, MOS	0.067	0.134
RAM, 512 bit, bipolar	0.049	0.098
RAM, 512 bit, MOS	0.076	0.152
RAM, 1024 bit, bipolar	0.055	0.106
RAM, 1024 bit, MOS	0.083	0.166

Table 5.2.1. Honeywell Standard Part Failure Rates (Concluded)

	Failure Rate (/Million Operating Hrs.)	
Part Grouping	Prior To 10/92 Update	Current Values
RAM, 2048 bit, bipolar	0.059	0.118
RAM, 2048 bit, MOS	0.089	0.178
RAM, 4096 bit, bipolar	0.067	0.134
RAM, 4096 bit, MOS	0.100	0.200
RAM, 8192 bit, bipolar	0.073	0.146
RAM, 8192 bit, MOS	0.111	0.222
RAM, 16384 bit, bipolar	0.081	0.162
RAM, 16384 bit, MOS	0.122	0.244

Table 5.2-2. Reliability Prediction for LRU 1

Part Grouping	Per Part Failure Rate	Part Quantity Per LRU	Total Failure Rate
Microcircuits	0.079	281	22.1401
Transistors	0.03	158	4.753
Diodes	0.02	227	4.446
Capacitors	0.005	573	2.718
Resistors	0.004	1135	4.361
Connectors	0.293	38	11.1225
Crystal/Oscillators	0.1	3	0.3
Inductors	0.065	15	0.975
Transformers	0.725	7	5.075
Lamp	0.58	1	0.58
Switch	0.47	1	0.47
Sensor	9.583	6	57.5
Printed Wiring Boards	0.248	20	4.9554
TOTAL=		2465	119.396

Table 5.2-3. Reliability Prediction for LRU 2

Part Grouping	Per Part Failure Rate	Part Quantity Per LRU	Total Failure Rate
Microcircuits	0.068	410	27.915
Transistors	0.03	129	3.917
Diodes	0.02	220	4.476
Capacitors	0.005	699	3.168
Resistors	0.004	1445	5.32
Connectors	0.219	58.9	12.9039
Crystal/Oscillators	0.1	2	0.2
Inductors	0.065	19	1.235
Transformers	0.687	8	5.495
Sensor	9.416	6	56.499
Printed Wiring Boards	0.342	19	6.4919
TOTAL=		3015.9	127.6208

Table 5.2-4. Reliability Prediction for LRU 3

Part Grouping	Per Part Failure Rate	Part Quantity Per LRU	Total Failure Rate
Microcircuits	0.055	343	18.972
Transistors	0.05	152	7.586
Diodes	0.013	214	2.708
Capacitors	0.004	641	2.715
Resistors	0.003	1221	4.109
Connectors	0.248	23	5.7075
Crystal/Oscillators	0.1	2	0.2
Filters	0.071	6	0.426
Inductors	0.065	10	0.65
Transformers	0.616	30	18.48
Printed Wiring Boards	0.141	14	1.9688
TOTAL=		2656	63.5223

Table 5.2-5. Reliability Prediction for LRU 4

Part Grouping	Per Part Failure Rate	Part Quantity Per LRU	Total Failure Rate
Microcircuits	0.148	200	29.637
Transistors	0.033	103	3.376
Diodes	0.03	282	8.546
Capacitors	0.002	666	1.625
Resistors	0.003	1347	4.677
Connectors	0.272	27	7.357
Crystal/Oscillators	0.09	3	0.27
Filters	0.071	5	0.355
Inductors	0.065	7	0.455
Transformers	0.503	11	5.535
Sensor	3.605	6	21.628
Printed Wiring Boards	0.378	17	6.429
TOTAL=		2674	89.89

Table 5.2-6. Reliability Prediction for LRU 5

Part Grouping	Per Part Failure Rate	Part Quantity Per LRU	Total Failure Rate
Microcircuits	0.088	239	21.038
Transistors	0.017	179	3.118
Diodes	0.03	334	9.994
Capacitors	0.005	1403	6.4625
Resistors	0.017	1341	23.235
Connectors	0.12	56	6.7425
Crystal/Oscillators	0.1	7	0.7
Filters	0.01	21	0.21
Inductors	0.065	137	8.872
Transformers	0.725	6	4.35
Switch	0.935	1	0.935
Printed Wiring Boards	0.5	33	16.5
TOTAL=		3757	102.157

Table 5.2-7. Reliability Prediction for LRU 6

Part Grouping	Per Part Failure Rate	Part Quantity Per LRU	Total Failure Rate
Microcircuits	0.094	124	11.688
Transistors	0.024	102	2.428
Diodes	0.023	168	3.86
Capacitors	0.005	631	3.2315
Resistors	0.014	565	7.633
Connectors	0.139	34	4.725
Crystal/Oscillators	0.1	3	0.3
Filters	0.01	34	0.34
Inductors	0.065	54	3.51
Transformers	0.725	12	8.7
Switch	0.935	1	0.935
Printed Wiring Boards	0.5	9	4.5
TOTAL=		1737	51.8505

Table 5.2-8. Reliability Prediction for LRU 7

Part Grouping	Per Part Failure Rate	Part Quantity Per LRU	Total Failure Rate
Microcircuits	0.128	86	11.044
Transistors	0.044	48	2.102
Diodes	0.019	104	1.994
Capacitors	0.007	216	1.505
Resistors	0.004	314	1.156
Connectors	0.181	34	6.17
Crystal/Oscillators	0.1	1	0.1
Filters	0.01	1	0.01
Inductors	0.065	2	0.13
Transformers	0.725	7	5.075
Display	1.833	3	5.5
Printed Wiring Boards	0.5	13	6.5
TOTAL=		829	41.286

6.0 Analysis Results

6.1 Field Failure Rates VS LRU

The following paragraphs and tables present the computed field failure rates, computed using a 50% chi^2 distribution, for each of the part groupings and for each LRU.

Tables 6.1-1 through 6.1-3 present the ceramic failure rate data for the three device groupings. There is a large variation in failure rates for each of the device groupings (1-2 orders of magnitude) which is strongly influenced by the relative volume of data for the different LRU's. LRU's 1 and 2 have the largest volume of data, accounting for from 85% to 94% of the total operating hours for the groupings. The overall failure rate difference between LRU 1 and 2 is less than 6 to 1.

Tables 6.1-4 through 6.1-6 present the plastic failure rate data for the three device groupings. The failure rate differences for the groupings range from 1.5 to 1 for digital processor/memory devices to 7.6 to 1 for digital SSI/MSI. The total values are driven almost exclusively by the LRU 5-7 data which accounts for over 94% of the total operating hours.

Table 6.1-1. Failure Rates for Ceramic Digital SSI/MSI Devices

LRU #	Total Failures	Total Operating Hours	50% CHI^2 Failure Rate (Per 10^6 Hrs.)
1	3	834,852,000	0.004
2	25	1,098,816,000	0.023
3	6	138,276,000	0.048
4	0	892,000	0.777
TOTAL	34	2,072,836,000	0.016

Table 6.1-2. Failure Rates for Ceramic Digital Processor/Memory Devices

LRU #	Total Failures	Total Operating Hours	50% CHI^2 Failure Rate (Per 10^6 Hrs.)
1	2	64,773,000	0.041
2	67	257,535,000	0.263
3	6	40,748,000	0.164
4	1	16,948,000	0.099
TOTAL	76	380,004,000	0.201

Table 6.1-3. Failure Rates for Ceramic Liner Devices

LRU #	Total Failures	Total Operating Hours	50% CHI² Failure Rate (Per 10^6 Hrs.)
1	3	392,236,500	0.009
2	17	1,090,231,500	0.016
3	2	93,520,000	0.029
4	3	69,576,000	0.053
TOTAL	25	1,645,564,000	0.016

Table 6.1-4. Failure Rates for Plastic Digital SSI/MSI Devices

LRU #	Total Failures	Total Operating Hours	50% CHI² Failure Rate (Per 10^6 Hrs.)
4	3	53,520,000	0.069
5-7	9	1,104,549,000	0.009
TOTAL	12	1,158,069,000	0.011

Table 6.1-5. Failure Rates for Plastic Digital Processor/Memory Devices

LRU #	Total Failures	Total Operating Hours	50% CHI² Failure Rate (Per 10^6 Hrs.)
4	1	16,948,000	0.099
5-7	47 (372)	315,864,500 (545,475,500)	0.151 (0.681)
TOTAL	48 (373)	332,812,500 (562,423,500)	0.146 (0.664)

1. Values in parentheses represent the values with the inclusion of the 28C256 and 71256 memory devices

Table 6.1-6. Failure Rates for Plastic Linear Devices[1]

LRU #	Total Failures	Total Operating Hours	50% CHI² Failure Rate (Per 10^6 Hrs.)
4	7	37,464,000	0.205
5-7	31	663,288,000	0.048
TOTAL	38	700,752,000	0.055

6.2 Field VS Predicted Failure Rates

Table 6.2-1 compares the field failure rates for the part groupings and package types with the predicted failure rates. Note that there is no difference in predicted failure rates between ceramic and plastic parts.

The predicted failure rates are computed as a per part failure rate by dividing the total failure rate for the parts in each grouping with the number of parts in the group. This is done due to the differing mix of parts, and their subsequent failure rates, for the different LRU's.

Though arbitrary, Honeywell has historically viewed differences in field versus predicted failure rates of less than 2 to 1 as being acceptable due to part variability and potential error sources in the field data collection process. With this in mind, all of the field failure rates are within 2 to 1 of the predicted numbers with only the ceramic µProc/Memory group and plastic linear group being above their predicted levels.

Table 6.2-1. Field vs. Predicted Failure Rates[1]

	50% CHI[2] Failure Rates (/Million Op. Hr.)		
Device Grouping	Field	Predicted	Field vs. Predicted Ratio
CERAMIC			
Digital SSI/MSI	0.017	0.024	0.71
Digital µProc./Memory	0.202	0.162	1.24
Linear	0.016	0.027	0.59
Total Ceramic	0.033	0.040	0.82
PLASTIC			
Digital SSI/MSI	0.011	0.030	0.37
Digital µProc./Memory	0.146 (0.664)	0.262 (0.270)	0.56 (2.46)
Linear	0.055	0.031	1.77
Total Plastic	0.045 (0.175)	0.065 (0.083)	0.69 (2.11)

1. Values in parentheses represent the values with the inclusion of the 28C256 and 71256 memory devices

6.3 Plastic Vs Ceramic Field Failure Rates

Table 6.3-1 compares the plastic versus ceramic failure rates by using the field versus predicted ratios shown in table 6.2-1. The digital groupings (SSI/MSI and µProc./Memory) show consistency in that the plastic failure rates are approximately half of their ceramic counterparts. The plastic linear grouping is experiencing a three times higher failure rate than for ceramic linear parts.

Combining all parts groupings, weighed by their level of usage, there is a canceling effect such that the plastic failures rates have an edge by 15%. This difference is considered insignificant given the potential margin for error. It does indicate that the use of plastic microcircuits, processed in accordance with CAS practices, will not degrade, and may enhance, product reliability..

Table 6.3-1. Plastic vs. Ceramic Field Failure Rates

Device Grouping	Plastic vs. Ceramic Ratio[1]
Digital SSI/MSI	0.52
Digital μProc./Memory	0.45 (1.98)
Linear	3.02
Total	0.84 (2.56)

1. Values in parentheses represent the values with the inclusion of the 28C256 and 71256 memory devices

6.4 Discussion of Results

The results of this study confirm that the approach Honeywell has taken in the use of plastic microcircuits in a commercial avionics environment, has not impacted product reliability. The identified variations in device failure rates may warrant some adjustment of predicted failure rates but the changes will effectively cancel themselves out when viewed from an LRU reliability level.

Both digital microcircuit groupings showed a plastic failure rate of half that of the ceramic parts. An explanation for this is not evident from the data and further investigation is beyond the scope of this study.

The three-to-one higher failure rate of plastic linear devices over ceramic linear devices is of concern and the data was reviewed to more fully understand the cause 45% of the linear device failures were due to one device type (574) which is a one-user in the system made up of LRU's 5, 6 and 7. Though no clear cause or corrective action were identified, the following discussion will likely lead to further investigation by Honeywell.

Eight of the 14 574 failures were due to degradation in performance at temperatures exceeding +125°C though their performance over the commercial temperature range was within specification parameters. These devices are not warranted to operate at +125°C by the manufacturer and instead are 100% electrically tested at the extended temperature extremes by Honeywell, at a 3rd party test facility. It cannot be concluded from this data if the failures were actually caused by the performance degradation. This is one area that Honeywell will investigate further.

If it is found that degradation of performance at high temperature is the cause of these failures, the burn-in performance parameters could be tightened or further derating of the maximum application conditions could reduce or eliminate this failure mode.

This leads us to believe, though not conclude, that the linear devices may require extra attention relative to characterization over temperature and application consideration as compared to digital devices.

Appendix A
CAS-SPO Component Derating Criteria

Table A-1. CAS-SPO Component Derating Criteria

Part Type	Parameter	Derating Factor	Remarks
Microcircuits Digital	Junction Temp. (Tj)	110°C Max.	The max. Tj is a worst case value for worst case temp. op. such as max. power dissipation at max. ambient Temp. It shall be a design requirement to hold the Tj during normal temp. op. conditions to a Tj of 85°C or less.
	Output Current/Fanout	90%	Of Maximum Specified
	Supply Voltage	V_1 + 10%	V_1 =specified nominal supply voltage.
Microcircuits Memories, Processors, ASIC's	Junction Temp. (Tj)	110°C Max.	The max. Tj is a worst case value for worst case temp. op. such as max. power dissipation at max. ambient Temp. It shall be a design requirement to hold the Tj during normal temp. op. conditions to a Tj of 85°C or less.
	Output Current/Fanout	75%	Of Maximum Specified
	Supply Voltage	V_1 +/- 10%	V_1 =specified nominal supply voltage.
Microcircuits Linear Bipolar & MOS	Junction Temp. (Tj)	110°C Max.	The max. Tj is a worst case value for worst case temp. op. such as max. power dissipation at max. ambient Temp. It shall be a design requirement to hold the Tj during normal temp. op. conditions to a Tj of 85°C or less. Reduce power to zero at 110°C with same slope as maximum rating.
	Supply Voltages	80%	Of vendors max. rating, or voltage value at which vendor measures electrical parameters.
	Input Voltage Differential (or current)	80%	Of specified voltage rating (or current rating with internal voltage limiting)
	Input voltage common mode	80%	Of specified voltage rating.
	Output Current/Fanout	75%	Of rated value

Table A-1. CAS-SPO Component Derating Criteria (Continued)

Part Type	Parameter	Derating Factor	Remarks
Microcircuit Regulators	Junction Temp. (Tj)	110°C Max.	The max. Tj is a worst case value for worst case temp. op. such as max. power dissipation at max. ambient Temp. It shall be a design requirement to hold the Tj during normal temp. op. conditions to a Tj of 85°C or less. Reduce power to 0 at 110°C with the same slope as max rating.
	Max. Input Voltage	80%	Of max. specified.
	Min. Input Voltage	V_1 + 10%	V_1 = Spec. Min. Voltage.
	Min. Input/Output Voltage	V_2 + 10%	V_2 = Spec. Min. Diff. Voltage.
	Output Current	80%	of max. specified rating.
Microcircuit Regulators	Junction Temp. (Tj)	110°C Max.	The max. Tj is a worst case value for worst case temp. op. such as max. power dissipation at max. ambient Temp. It shall be a design requirement to hold the Tj during normal temp. op. conditions to a Tj of 85°C or less. Reduce power to 0 at 110°C with the same slope as max rating.
	Max. Input Voltage	80%	Of max. specified.
	Min. Input Voltage	V_1 + 10%	V_1 = Spec. Min. Voltage.
	Min. Input/Output Voltage	V_2 + 10%	V_2 = Spec. Min. Diff. Voltage.
	Output Current	80%	of max. specified rating.

Table A.1. CAS-SPO Component Derating Criteria (Continued)

Part Type	Parameter	Derating Factor	Remarks
Diodes Rectifier and Switching	Junction Temp. (Tj)	110°C Max.	The max. Tj is a worst case value for worst case temp. op. such as max. power dissipation at max. ambient Temp. Use 125°C if the max. Tj rating is 175°C or higher. It shall be a design requirement to hold the Tj during normal temp. op. conditions to a Tj of 85°C or less. Reduce power to 0 at 110°C with the same slope as max rating.
	Reverse Voltage (Vr)	80%	of specified Vr rating
	Reverse Voltage Transients	95%	of specified Vr rating
	Average/DC Forward Current	80%	of specified rating. Reduce to 0 current at Tj max.
	Forward Surge Current	80%	of specified rating or 100% of forward current if no surge spec. exists.
	Reverse Recovery Time	120%	of maximum rated value.
Diodes Zener	Junction Temp (Tj)	110°C Max.	The max. Tj is a worst case value for worst case temp. op. such as max. power dissipation at max. ambient Temp. Use 125°C if the max. Tj rating is 175°C or higher. It shall be a design requirement to hold the Tj during normal temp. op. conditions to a Tj of 85°C or less. Reduce power to 0 at 110°C with the same slope as max rating.
	Forward Surge Current	80%	of specified rating or 100% of forward current if no surge spec. exists.
	Power	100%	of specified rating with power reduced to zero at Tj max.
	Energy	80%	of specified rating. Only applies to transorb devices.

Table A-1. CAS-SPO Component Derating Criteria (Continued)

Part Type	Parameter	Derating Factor	Remarks
Transistors Bipolar	Junction Temp. (Tj)	110°C Max.	The max. Tj is a worst case value for worst case temp. op. such as max. power dissipation at max. ambient Temp. Use 125°C if the max. Tj rating is 175°C or higher. It shall be a design requirement to hold the Tj during normal temp. op. conditions to a Tj of 85°C or less. Reduce power to 0 at 110°C.
	Voltages	80%	of specified ratings. This applies to Vce and Vds for bipolars and Vds and Vgs for FET's.
	Voltage Transients	95%	of maximum specified voltage rating.
	Current Rating	80%	of specified ratings. This applies to Ic for bipolars and Id for FET's.
	Power	100%	of specified rating. Derate to zero power at maximum derated junction temp.
Transistors Bipolar	Junction Temp. (Tj)	110°C Max.	The max. Tj is a worst case value for worst case temp. op. such as max. power dissipation at max. ambient Temp. Use 125°C if the max. Tj rating is 175°C or higher. It shall be a design requirement to hold the Tj during normal temp. op. conditions to a Tj of 85°C or less. Reduce power to 0 at 110°C.
	Voltages	80%	of specified ratings. This applies to Vce and Vds for bipolars and Vds and Vgs for FET's.
	Voltage Transients	95%	of maximum specified voltage rating.
	Current Rating	80%	of specified ratings. This applies to Ic for bipolars and Id for FET's.
	Power	100%	of specified rating. Derate to zero power at maximum derated junction temp.
Resistors - All	Power	70% (60% for Wirewound)	of Mfgr's rating at specified temp.
	Breakdown Voltage	100%	of spec. dielectric breakdown Volt.
Resistors Adjustable	Current	80%	of spec. rating
	Breakdown Voltage	100%	of spec. dielectric breakdown volt.

Table A-1. CAS-SPO Component Derating Criteria (Continued)

Part Type	Parameter	Derating Factor	Remarks
Capacitors Ceramic	DC Working Voltage	70%	of specified rating.
	RMS Voltage	50%	of specified DC working voltage when used in AC application.
	Surge Voltage	80%	of surge voltage rating or 100% of DC working voltage rating.
	Ripple Voltage/Current	80%	of specified rating where value exists.
	Temperature	100%	of specified rated case temperature.
Capacitors Solid Tantalum	DC Working Voltage	70%	of specified rating.
	Surge Voltage	80%	of surge voltage rating or 100% of DC working voltage rating.
	Reverse Voltage	Remarks	Limit reverse voltage as follows: Case Temp / Rev. Voltage as % of Rated WVDC -55°C to 25°C 15% 25°C to 55°C 10% 55°C to 85°C 5% 85°C to 125°C 1%
	Ripple Voltage/Current	80%	of specified rating where value exists.
	Series Impedance (External)	0.1 ohms/volt	at 70% working voltage derating. Can be reduced to 0 ohms/volt at 50% working voltage derating.
	Temperature	100%	of specified rated case temperature.
Capacitors Wet Tantalum	DC Working Voltage	70%	of specified rating.
	Surge Voltage	80%	of surge voltage rating or 100% of working voltage rating.
	Reverse Voltage	0 Volts	
	Ripple Voltage/Current	80%	of specified rating where value exists.
	Temperature	100%	of specified rated case temperature.

Table A-1. CAS-SPO Component Derating Criteria (Concluded)

Part Type	Parameter	Derating Factor	Remarks
Capacitors Aluminum Electrolytic	DC Working Voltage	70%	of specified rating.
	Surge Voltage	80%	of surge voltage rating or 100% of working voltage rating.
	Reverse Voltage	1 Volt	if <7 WVDC. Reverse voltage may be 3 volts if >7 WVDC.
	Ripple Voltage/Current	80%	of specified rating where value exists.
	Temperature	100%	of specified rated case temperature.
Transformers and Inductors	Voltage, Case to Winding and Winding to Winding	75%	of specified dielectric rating.
	Internal Coil Temp.	Remarks	Limit internal coil temp. to 20°C below temp. rating of insulation system used.
	Current	100%	of specified rating.
Switches & Relays	Contact Current (DC Load)	80%	Use the following derating for different load types: Lamp: For incand. lamps use 12.5% Inductive: If L/R ratio not exceeding 0.026 then use 33% Capacitive: 80%
	Contact Voltage	100%	of spec. rating
	Temperature	100%	of spec. rating
Connectors	Voltage	80%	of specified rated working voltage.
	Current	100%	of specified rating.
	Temperature	100%	of specified rating.
	Matings	75%	of specified rating where applicable.

Appendix B
Honeywell Commercial Aviation Systems Practices and Procedures for Using Plastic Packaged Microcircuits

1.0 Introduction

This interim report discusses Honeywell CAS (previously Commercial Flight Systems Group (CFSG)) practices and procedures for using plastic packaged microcircuits in Honeywell products. These practices and procedures are implemented to ensure safe, reliable, products.

The Tasks reported herein are:

- Task 1.2.2, that portion of the task dealing with the minimum screening/qualification requirements for devices;
- Task 1.2.4, Describe IC Vendor Selection Process;
- Task 1.2.5, Describe Specification and Procurement of Plastic and Ceramic ICs;
- Task 1.2.6, Describe Part Processing, Production, and Repair Flow.

Note that Task 1.2.1, Select Candidate Systems, and Task 1.2.2, Describe Systems Parts, are addressed within the main body of this final report in Section 2.0, Product Descriptions. Task 1.2.3, Identify National Semiconductor Parts, is appended to this appendix as an attachment.

2.0 Task 1.2.2: Describe System Parts....minimum screening/qualification requirements

A prior report fulfilled all the reporting requirements associated with this task but for the description of the minimum screening/qualification requirements. The quantity and type (part type, package type, and lead configuration) of both ceramic and plastic parts in the systems selected for this plastic packaging program were identified. The information to be documented here relates only to Honeywell CFSG's minimum screening/qualification requirements for these parts.

For ceramic parts Honeywell complies with MIL-STD-883. Therefore, what follows basically relates to Honeywell's use of plastic parts and the quality assurance steps of parts qualification and screening used to maintain and improve equipment reliability.

The qualification of parts is intended to verify that the parts will operate reliably in their product environment for the anticipated life of that product (typically 20 years). Parts screening is intended to continuously verify that components will have reliability that is equivalent to the original qualified parts.

2.1 Temperature Ratings Applicable to Qualification and Screening

Test Temperature Rating: Parts are tested at the end points of these limits to verify that the parts meet the specification limits over this expanded temperature range.

- Ambient Temperature -40°C to +125°C

Storage Temperature Range:

- Ambient Temperature -65°C to +150°C

2.2 LRU Operational Temperature Limits

Emergency Operational Limits: This applies to emergency operation such as loss of cooling air (worst case, abnormal).

- Junction Temperature -40°C to +125°C

High Operating Temperature: This applies to worst case normal operating conditions (derating point).

- Junction Temperature Maximum +105 °C

Recommended Normal Flight/Ground Operation:

- Junction Temperature Maximum +85°C

2.3 Device Identification/Documentation

Devices shall be identified and documented either by drawings issued by Honeywell or the vendor. The drawings shall describe the detailed requirements of devices used and other provisions pertaining to the individual device types.

2.3.1 In all cases, with the exception of 2.3.2, 2.3.3, and 2.3.4, Honeywell shall issue two sets of drawings: Specification Control Drawing (SCD) and Selected Item Drawing (SID). The SCD is a brief document that describes minimal information on the device, while the SID is the document that defines the electrical parameters and screening requirements.

2.3.2 For situations where the manufacturers conduct the screening, the SCD and/or SID shall be the controlling document that describes the electrical parameters, processing and screening requirements.

2.3.3 For Programmable parts (e.g. PAL, PROM) the following documentation options may be pursued: (1) In the first option the SCD and the individual Engineering Bulletin (EB) pertaining to that programmable part shall be the controlling document. Both the SCD and EB are called out in the Altered Item Drawing (AID) which describes the programming information. (2) Alternately, the AID corresponding to a programmed part shall describe the requirements for altering the unprogrammed part as defined on the Honeywell Specification Drawing.

2.3.4 Vendor drawings may only be used when the vendor meets the requirements defined in paragraph 4.2.2 "Configuration Management Process (CMP)" of EB4067232, Honeywell Parts Control Program. This paragraph states that parts control is established when an agreement is made with a manufacturer whereby the manufacturer's internal revision-controlled document (or military specification if applicable) becomes, in effect, the procurement specification. The manufacturers who participate in the configuration management process have submitted their internal revision control documentation to Honeywell. The configuration management agreement mandates that manufacturers must also supply notification of change to Honeywell as well as maintain a log that indicates whether a part has been CMP-approved.

2.4 Device Qualification Selection Criteria

Qualification testing is not required on every device type. Devices shall be qualified on the basis of similarity based on EB4070104, Engineering Bulletin for Plastic Part Qualification by Similarity and Requalification of Changes. This EB specifies the criteria for which qualification by similarity shall be conducted for plastic semiconductor and resistor network devices. This specification also defines which types of changes to qualified devices shall result in the need for requalification.

2.4.1 Similarity Criteria for Package Qualification

A device package may be qualified by similarity to one that was formerly tested and qualified provided that all of the following conditions apply: (1) The plastic molding compound used for both devices shall be the same; (2) Both parts are supplied by the same manufacturer; (3) Both parts are supplied in the same package type (e.g., SO, SOL, PLCC, DIP) and have the same pin count. Devices with differing pin counts may be qualified by similarity provided that either (a) for small pin-count packages such as DIP, SOIC, and PLCC, the difference in the packages' top surface areas must be no greater than 25%, or (b) for large packages such as PQFP, the difference in die area must be no greater than 40%; (4) Both parts have the same basic lead frame and material design; (5) Both parts are produced using the same fabrication process, where a fabrication process is defined as a specific device technology, such as ACMOS, HCMOS, and Schottky; and (6) Both parts have the same passivation, die coating, and external lead finish.

2.4.2 Die Qualification by Similarity

Die qualification may be extended by similarity to other die if the alternate die are categorized with the same microcircuit group number. The microcircuit group numbers are in accordance with MIL-M 38510 Appendix E. (Note that MIL-M-38510 has been superseded by MIL-PRF-38535, and Appendix E by Appendix A). If a device has passed die qualification for a specific microcircuit group, other devices that fall into the same group are thus eligible for die qualification by extension. For devices not listed in Appendix E of MIL-M-38510, (i.e., Appendix A of MIL-PRF-38535), the similarity decision shall be performed by the applicable component qualification engineer.

2.4.3 Requalification Due to Manufacturer Changes

In the event that a manufacturer implements a major change in a part (as identified in Tables 2.4.3-1 and 2.4.3-2), a requalification shall be performed. The specific test shall be performed if the designation "Yes" is indicated. The use of equivalent manufacturer data is an acceptable method to meet the die qualification requirement.

Table 2.4.3-1. Package Requalification Criteria

Major Change Description	HAST Test	Temp Cycle Test	Solderability Test
Package Material	Yes	Yes	No
Passivation or Die Coating	Yes	Yes	No
Lead Frame/ Material & Design	Yes	Yes	Yes
External Lead Finish and/or Material	No	No	Yes

Table 2.4.3-2. Die Requalification Criteria

Major Change Description	1000 Hour Life Test or Equivalent
Die Redesign	Yes
Major die fabrication change. Examples of changes that would typically require requalification include (and are defined in MIL-M 38510 (MIL-PRF-38535)): 1 Metallization changes 2. Die structure topology changes (double-diffused, epitaxial, isolation) 3. Mask changes that alter active elements.	Yes

2.5 Manufacturer Surveys

Honeywell periodically performs manufacturer surveys in order to accumulate needed information to perform qualification by similarity. An example of such a survey form is shown in Table 2.5-1.

Table 2.5-1. Sample Manufacturer Survey Form

Device Type	Generic Number	Date Code Implemented	Package	Molding Compound	Passivation	Lead Frame	Die Size
M	74HC32		SO.14				
M	74HC393		SO.14				
M	74HC74		SO.14				
M	7812 (LM)		TO.220				
M	7815		TO.220				
M	78M12		TO.252				
M	7912		TO.220				
M	7915		TO.220				

Manufacturers' qualification data (including molding material type, passivation type, life test data, manufacturing data) if available, can be used. Component and Reliability Engineering shall analyze this data and, if insufficient data exists, shall perform additional qualification as required.

2.6 Die Qualification

For all plastic packaged semiconductor devices, a package qualification shall be performed. The die will have been qualified through its military equivalent part. In the event that the die has no military qualified equivalent, the following options, in addition to package qualification, may be pursued: (1) Usage of manufacturer's die qualification data shall be used, and if insufficient data exists, Component and Reliability Engineering may invoke a die qualification; (2) Steady State Life Test can be performed in accordance with MIL-STD-883C, Method 1005.6.

Life test duration shall be 1000 hours at +125°C unless otherwise specified. Accelerated life test duration, if used, shall be the time equivalent to 1000 hours at +125°C and the junction temperature of the device shall not exceed +150°C. The sample size shall be a minimum of 32 units. The Accept/Reject criteria shall be ACCEPT on zero. Only environmentally related failures shall be considered as rejects. In the event of excessive failure rate resulting from this exposure, the manufacturer shall be notified and a mutually agreed program of corrective action shall be developed.

2.7 Package Qualification for Plastic Semiconductor Devices

Figure 2.7-1 summarizes the qualification process for plastic packaged ICs.

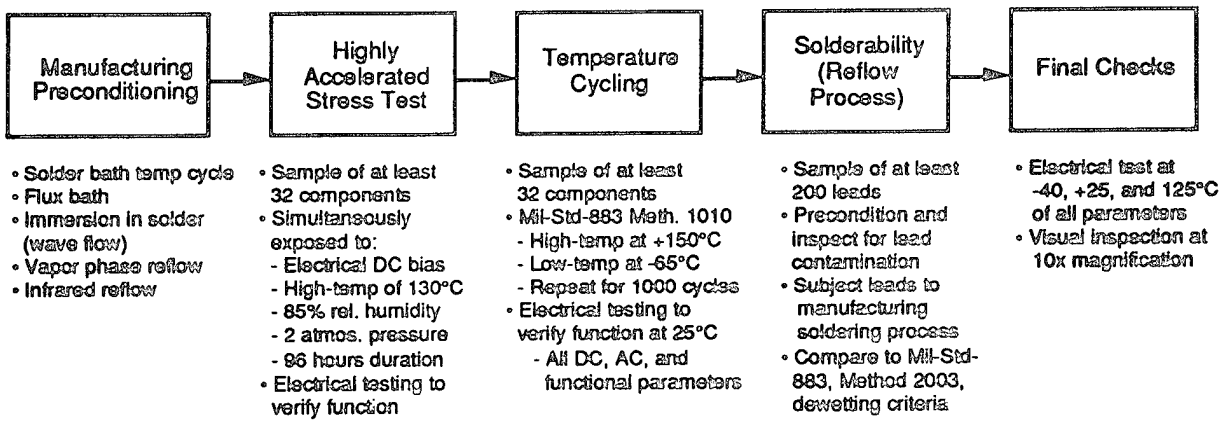


Figure 2.7-1. Qualification Process for Plastic Packaged Semiconductor Components

2.7.1 HAST Test

Highly accelerated stress test (HAST) is a destructive test that evaluates the reliability performance of plastic devices in humid environments. The electrical integrity of the device is evaluated after high relative humidity, pressure, and temperature. Biasing is provided to the devices while under exposure.

2.7.1.1 Test Sample—The sample size shall be a minimum of 30 units. The Accept/Reject criteria shall be ACCEPT on ZERO. Only environmentally related failures shall be considered as rejects.

2.7.1.2 Manufacturing Preconditioning—Preconditioning is applicable for surface mount devices only. This is applied to the devices in order to simulate the stress which occurs during card assembly. Preconditioning shall be performed in accordance with EB4070105, "Engineering Bulletin for Qualification Precondition for HAST and Temperature Cycle for Plastic SMT Semiconductor Devices," that describes the simulation of stress which occurs in the plastic semiconductor devices.

2.7.1.2.1 Materials/Equipment—Substrate material, non-metalized FR-4 or equivalent, sized to 8.0±.5 inch square, shall be used. Low profile basket carrier for the substrate material to retain the parts during vapor phase reflow and Prelete cleaning shall also be used along with a device holding fixture to hold the devices in place during in-line cleaning operations.

2.7.1.2.2 Procedure for HAST Preconditioning—

2.7.1.2.2.1 Handling Guidelines—Finger cots, gloves, or tweezers shall be used when handling any substrate or loose parts; never use bare hands. Correct ESD handling procedures shall be followed at all times. Plastic SMT parts have fragile leads and must be handled so as not to bend them.

2.7.1.2.2.2 Baking Procedures—All parts shall be baked for 24 hours at 125°C per applicable component baking specification prior to reflow. All baked parts must be stored in desiccated atmosphere prior to reflow.

2.7.1.2.2.3 Substrate Material Preparation—All substrate material shall be thoroughly cleaned with Prelete per applicable PWB cleaning specification and sprayed with a thin coat of No. 197 Kester RMA flux, or equivalent, on the top side of the substrate.

2.7.1.2.2.4 Component Placement—All parts shall be manually place onto the substrate, leads downward. If parts are not completely processed within 48 hours, the fixtures and parts must be stored in a desiccated environment.

2.7.1.2.2.5 Reflow/Rework Exposure—Parts shall be exposed to three passes through the reflow process to simulate the reflow of the initial assembly and two rework cycles. Depending on the Honeywell site, parts and substrates (not baskets) shall be run through Vitronics infrared reflow equipment using the specified reflow profile with a conveyor speed of 13 inches per minute, or, parts and substrates shall be placed in low profile baskets and exposed to HTC vapor phase reflow with the conveyor speed at 8.5 and vapor rate at 6, or, parts and substrates (not baskets) shall be run through the BGK 1672 infrared reflow equipment using the specified reflow profile. After the final reflow cycle, parts must be cleaned within two hours.

2.7.1.2.2.6 Cleaning—Depending on the Honeywell site, either (1) carefully remove parts from board and place in a cleaning basket so as not to bend leads and clean the parts using Prelete Cleaning Cycle No.3, and then clean parts once more using the Freon Inline Cycle or the following Freon Vapor Degreaser flow: (a) vapor - 1 min, (b) spray - 2 sec, (c) vapor - 1 min, (d) spray - 2 sec, (e) vapor - 1 min, (f) spray - 2 sec, (g) vapor - 1 min, (h) spray - 1 sec, (i) drain, (j) repeat cleaning cycle, (k) inspect for cleanliness. Or (2) carefully remove the parts form the board and place them onto the device holding fixture and clean the parts using the Detrex inline spray over immersion cleaning system using the standard production process of two passes through the cleaner.

2.7.1.2.2.7 Re-Package Parts—Return the parts to their original tubes and static bags.

2.7.1.2.3 Procedure for Temperature Cycle Precondition—Parts exposed to temperature cycle may be either preconditioned using the Procedure for HAST Preconditioning (see paragraph 2.7.1.2.2), or the following flow: (1) handling guidelines per paragraph 2.7.1.2.2.1, (2) baking procedures per paragraph 2.7.1.2.2.2, (3) substrate fixture preparation per paragraph 2.7.1.2.2.3, (4) omit Kester RMA flux spray, (5) component placement per paragraph 2.7.1.2.2.4, (6) reflow/rework exposure per paragraph 2.7.1.2.2.5, (7) omit use of BGK reflow equipment, (8) repackage parts per paragraph 2.7.1.2.2.7.

2.7.1.3 HAST Qualification—Preconditioned plastic semiconductor devices shall be subjected to Highly Accelerated Humidity and Temperature Stress Testing. Analysis of qualification failures form HAST test shall be

conducted by Component and Reliability Engineering to assess whether it is an environmentally related failure. For qualification purposes, only environmentally related failures shall be considered as rejects.

2.7.1.3.1 Temperature Cycle Test—This test shall be conducted to determine the resistance of a plastic packaged semiconductor device to stress induced by temperature cycles of +150 to -65°C. Resulting damage to a package shall be noted and electrical integrity maintained. The sample size shall be a minimum of 20 units. The Accept/Reject criteria shall be ACCEPT on ZERO. Only environmentally related failures shall be considered as rejects. Manufacturing preconditioning shall be performed in accordance with EB4070105, "Engineering Bulletin for Qualification Precondition for HAST and Temperature Cycle for Plastic SMT Semiconductor Devices. Preconditioned parts shall be subjected to the procedure in P4068700, "Temperature Cycle Qualification Procedure for Plastic Semiconductor Devices." Failures shall be analyzed by the Component and Reliability Group to determine if the failures are environmentally related. Permanent changes in operating characteristics and physical damage produced during temperature cycling result principally from variations in dimensions and other physical properties. Effects of temperature cycling include (1) delamination of plastic encapsulant compounds, (2) cracking and crazing of encapsulant compounds, and (3) changes in electrical characteristics due to mechanical displacement or rupture of conductors or insulating materials.

2.7.1.3.1.1 Apparatus (Refer to MIL-STD-883 Method 1010)

2.7.1.3.1.2 Conditions—All surface mount parts shall be subjected to preconditioning by Honeywell prior to any qualification testing. Preconditioning shall be performed in accordance with EB4070105 (see paragraph 2.7.1.2). This requirement is not applicable to DIP parts.

Temperature cycling conditions shall be in accordance with MIL-STD-883, Method 1010 Condition C, except that the maximum transfer time shall be 20 seconds and the minimum quantity of cycles shall be 1000.

2.7.1.3.1.3 Temperature Cycle Procedure

2.7.1.3.1.3.1 Sample Size—The minimum sample size of devices exposed to temperature cycling shall be twenty. Additional devices shall be provided to allow for pre-electrical test fallout.

2.7.1.3.1.3.2 Temperature Cycle Flow—The following is an overview of the temperature cycle flow.

Table 2.7.1.3.1.3.2-1. Overview of Temperature Cycle Procedure

Step	Description	Paragraph
1	Electrical test at 25°C	5.1.3.1.3.3
2	Temperature cycle	5.1.3.1.2
3	Electrical test at 25°C	5.1.3.1.3.3

2.7.1.3.1.3.3 Electrical Test—Electrical test shall be performed no sooner than 2 hours and no later than 24 hours after the last cycle. Exceptions shall be granted for devices when electrical testing and thermal cycling are performed by separate facilities. Devices shall be tested at a minimum of all DC, AC, and functional parameters at 25 °C to the specification provided or approved by Honeywell. Upon request by Honeywell, test programs shall be made available for review.

2.7.1.3.1.3.4 Disposition of Devices Under Test—All devices shall be shipped to Honeywell packaged in a manner to protect them from ESD or mechanical damage. Each electrical Failure shall be placed in a separate,

serialized, antistatic bag. The generic part number and the step in which the failure occurred shall be shown clearly on each bag using the Honeywell-supplied label. Data logs (paper recording parametric performance of a part including failure data) may be limited to the first five failures from a given temperature test step. Each data log shall contain the value of the failed parameters and the assigned failure serial number.

2.7.1.3.1.3.5 Component Handling—All components and failures shall be considered electrostatic sensitive and shall be handled accordingly throughout all test steps. This includes the use of wrist straps and finger cots. All tubes and bags in immediate contact with the parts shall be electrically conductive.

2.7.1.3.1.3.6 Safety—The equipment manufacturer's recommendations and local safety regulations shall be followed.

2.7.1.3.1.3.7 Test Facility Notes—The following shall be provided with the qualification purchase order if the temperature cycle is performed at a facility other than Honeywell:

1) Parts with appropriate preconditioning if any.
2) Applicable electrical test specification with a minimum of two golden samples to be kept on file at the test facility. (Once golden samples are on file, this requirement may be omitted.)
3) Serialized labels are to be applied to individual bags containing electrical failures.

Following completion of temperature cycle testing, the parts and data shall be returned to Honeywell. This shall include:

1) All passed parts.
2) All failed parts, with data, in accordance with paragraph 2.7.1.3.1.3.3.
3) Copy of traveler report including:
   a. Honeywell SCD part number
   b. Generic part number
   c. Applicable test specification
   d. Total quantity of parts by manufacturer
   e. Total quantity of mechanical failures
   f. Itemized electrical failures including: (1) failure serial number (2) test step in which failure occurred
   g. Total quantity passed
   h. Total quantity shipped
   i. Signed statement of compliance

Immediate notification of Honeywell is required if (1) electrical failures of either the pre or post electrical tests exceed 10% of the total lot quantity, or (2) the number of environmental test cycles interrupted exceeds three.

2.7.1.3.2 Solderability—This method determines the solderability of leads of surface mount plastic semiconductor devices by a reflow soldering operation. The pass/fail determination is made on the basis of the ability of the leads to be wetted or coated by solder when exposed to reflow conditions.

2.7.1.3.2.1 Test Sample—The sample size shall be a minimum of 200 leads and 5 parts for all surface mount plastic semiconductor devices except for parts having lead counts of less than 4. The accept/reject criteria shall be ACCEPT on ONE and REJECT on TWO. The sample size for parts having less than 4 leads shall be 20 parts and the accept/reject criteria shall be ACCEPT on ZERO.

2.7.1.3.2.2 Solderability Qualification—Preconditioning shall be performed in accordance with EB4070103,"Solderability Test Procedures for Plastic Semiconductor Surface Mount Devices", which describes a baking process that simulates the burn-in conditions and steam aging which simulates extended storage. The preconditioned parts shall be subjected to exposure as detailed in EB4070103 to determine whether component solderability is within control limits.

2.8 Change Notification

Minor process changes are to be expected to improve the manufacturer's products and Honeywell will cooperate with manufacturers towards attaining improved products.

2.8.1 Manufacturer Notification

The manufacturer shall immediately notify Honeywell in writing of any planned changes that effect form, fit, function, reliability, or location of wafer fabrication or packaging. The manufacturer shall obtain approval from Honeywell before shipment of parts. This is defined in the procurement specification or Basic Operating Agreement (BOA).

2.8.2 Criteria for Requalification

A requalification is necessary in cases where device process changes occur to qualified parts. Tables 2.4.3-1 and 2.4.3-2 list the requalification testing required for categories of changes. Components and Reliability Engineering shall make the final determination of testing requirements for requalification.

2.9 Screening Procedure

This procedure is established to achieve high quality and reliability of plastic semiconductor devices used in the air transport application. Screening shall be performed at a qualified screening house or by the manufacturer according to Honeywell Specification. A manufacturer screening is preferred if screening cost is not excessive.

All lots shall be tested in accordance with the requirements of P4066771, "Purchase Specification for a Screening Procedure for Plastic Semiconductor Devices," or P4073093, "Purchase Specification for a Manufacturing Screening Procedure for Plastic Semiconductor Devices," or equivalencies as defined by Components and Reliability Engineering. This specification covers the screening procedure for plastic semiconductor devices. This specification shall be used in conjunction with a Honeywell detail specification (selected item drawing). The detail specification shall include the electrical parameters needed to perform the screening tests.

Screening shall be conducted using the extended temperature military equivalent electrical parameters. When a product does not meet the extended temperature equivalent, a characterization of the parts shall be performed to obtain the electrical parameters.

2.9.1 Screening Test Sequence

The screening test sequence is summarized in Figure 2.9.1-1.

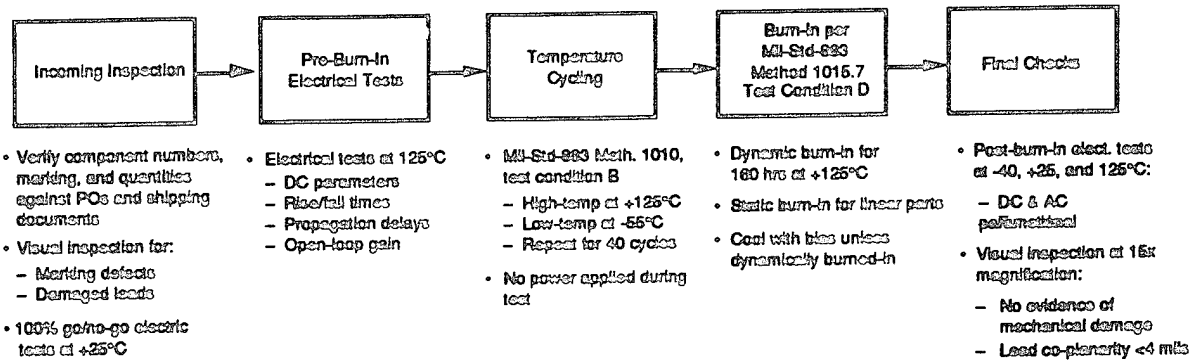


Figure 2.9.1-1. Screening Test Sequence

The screening procedure shall be performed on all parts. The screening sequence shall be as follows:

2.9.1.1 Pre-Burn-in Electrical Test—Pre-burn-in electrical test shall consist of the test specified in Table 2 (electrical test parameters table) of the applicable detail specification. Only those electrical parameters specified at TA = 125 °C shall be tested as part of the pre-burn-in test. This is to include dc, ac, and functional tests where applicable.

2.9.1.2 Burn-in Test—Burn-in test shall be performed in accordance with MIL-STD-883, Method 1015, Test Condition D. The duration shall be t = 160 hours, ± 8 hours and the temperature shall be T_A = +125°C. A copy of the burn-in circuit shall be available and shall be approved by Honeywell prior to its use. All devices shall be subjected to dynamic burn-in conditions unless prior written approval has been obtained from Honeywell to perform static burn-in. Where possible, parts shall be subjected to maximum load condition.

2.9.1.3 Post-Burn-in Electrical Test—Post-burn-in electrical test shall consist of the tests specified in Table 2 (electrical test parameters table) of the applicable detail specification. All of the parameters specified in Table 2 shall be tested as part of the post-burn-in test. Testing shall be performed at all of the temperatures specified. The test sequence shall be as follows:

T_A = 125°C tests, 100% Mil Specs, all AC/DC and functional parametric testing

T_A = 25°C tests, 100% Mil Specs, all AC/DC and functional parametric testing

T_A = -40°C tests, 100% Mil Specs, all AC/DC and functional parametric testing

A copy of the test program shall be available for audit.

2.9.1.4 Final Visual and Mechanical Inspection—Final gross visual lead check shall be performed on all devices in the lot. Devices having bent lead to a criteria of coplanarity greater than 4-mils shall be removed from the test lot.

2.9.1.5 Failure and Data Requirement

2.9.1.5.1 Certificate of Compliance—A certificate of compliance shall accompany the parts and include the following information:

a. P.O. number

b. Honeywell part number

c. Generic device type

d. Number of parts which passed screen tests

e. Statement that the parts were tested to the Honeywell part number with quality representative signature and date.

2.9.1.5.2 Screening Summary—A screening summary shall accompany parts when shipped. The summary shall include the following information:

a. Honeywell part number

b. Date code

c. Number of parts which pass and fail electrical test

d. Number of parts which pass and fail mechanical tests (bent leads)

2.10 Qualification and Screening Houses Selection Criteria

The following is a guideline defining the requirements a qualification/screening house must meet before being considered as a selectable test screening or qualification house.

2.10.1 Quality of Management

An assessment of the organizational management of the operation indirectly indicates whether parts processed at this company shall meet the quality and reliability requirements and obtain timely returns.

2.10.2 Company Profile

Information shall be obtained on how long the company has been established, on company reputation, and on review of past experiences in the areas of electrical test and environmental exposure.

2.10.3 ESD Conformance

Information shall be obtained on whether the facility is in conformance to MIL-STD-1686A or its equivalent.

2.10.4 Equipment Assessment and Availability

Information shall be obtained on the types of equipment, such as testers, chambers, and handlers available and if they are useful towards Honeywell's application.

2.10.5 Facilities Cleanliness

The general appearance and outlook of the facilities shall be noted.

2.10.6 Available Qualification/Screening Capacity and Capability

Information shall be obtained on capacity and capability of screening or performing environmental exposure.

2.10.7 Documented Mode of Operation

Assessment of the documentation aspect of all operations shall be noted. Information shall be obtained on the types of record retention being maintained.

2.10.8 Personnel Qualifications

Information shall be obtained on the personnel training and experiences in handling equipment.

2.11 Production Build

All plastic semiconductor devices acquired and used in circuit card assemblies in production shall be qualified parts. The plastic semiconductor devices, with the exception of diodes and transistors used in circuit card assemblies, shall be screened parts.

2.12 Storage of Parts

Devices requiring storage shall be in an environment of relative humidity on 20% maximum or a bake of 24 hours at +125°C prior to board mount may be implemented. Storage in a nitrogen atmosphere or a desiccant are options that may be implemented.

2.13 Waivers

If the manufacturer deviates from the requirements of the existing specification, a written approval from Honeywell is required. Materials shipped to an approved deviation shall be clearly identified and segregated from the material conforming to specification.

2.14 Date Code Control

Device date code shall be controlled by Honeywell. Date code control shall be maintained in EB4059903 by the Components and Reliability Engineering Group; if a part is qualified, the date code shall be specified therein. For the purpose of acquiring parts, it is recommended to purchase parts that are not older than 12 months as compared to the date of purchase and shall be so noted in the purchase order.

2.15 Statistical Process Control (SPC) Requirements

The manufacturer shall be actively developing an SPC program. A minimum program shall include training, definition of critical operations, installation of statistical control techniques, and a control action system.

The JEDEC Publication No. 19, General Standard for Statistical Process Control, may be used as a guideline.

2.16 Flammability Specification Compliance and Test

All plastic semiconductor device packages shall comply with the self-extinguishing characteristics as defined in the Underwriters Laboratories, Inc. document No. UL 94. Honeywell may elect to perform the test in accordance with UL 94 to determine the self-extinguishing properties of plastic packaging material.

2.17 General ESD Conformance

Packaging and handling of the plastic semiconductor devices shall be in accordance with MIL-STD-1686A.

2.18 Marking Permanency Test

Honeywell may opt to perform the marking permanency test. Part marking shall meet the requirements of the Honeywell drawings.

2.19 Audits of Manufacturers' Facilities/Screening/Qualification Houses

Honeywell reserves the right to arrange visits for the purpose of auditing the manufacturing facilities, qualification and screening, and to review process control procedures and record keeping in accordance with Honeywell Quality Document.

Record retention by manufacturers, qualification and screening houses shall be maintained in accordance with Honeywell Quality Document. Audit deficiencies and follow-up shall be in accordance with Honeywell Quality Document.

2.20 Field, Factory, and Screening Data Collection

Field, factory, and screening data collection shall be maintained by the Quality Group in accordance with relevant Quality Control Directives. Trend analysis shall be used as a basis for selective failure analysis.

2.21 Qualification and Screening Data Retention with Intent Towards Traceability

The records pertaining to screening and qualification of plastic semiconductor devices shall be retained by Honeywell for a minimum of 7 years and, thereafter, to be archived.

The qualification records retention shall be maintained by the Component and Reliability Group. The screening record retention shall be maintained by the Quality Group.

2.22 Qualification Test Reports

Test reports (qualification summary) for each device qualification shall be prepared and maintained by the Component and Reliability Group. Test reports are critical documents which shall be kept current and on file.

3.0 Task 1.2.4: Describe IC Vendor Selection Process

The IC vendor selection process begins with the design engineer who, after reviewing the system requirements, identifies the need for specific functions (or block tasks to be performed). Each block of the design is then broken into lower level functions that can be performed by specific ICs. The designer determines which of the semiconductor vendors offers each IC. The determination is based on the designer's past experience with various suppliers and their products, on data obtained from various product locator publications, and on input from the cognizant component engineer. This is the first step indicated on the IC supplier selection process flowchart, Figure

3.0. The design team then evaluates the potential suppliers by looking at the divisional preferred supplier list, the Honeywell corporate semiconductor commodity team's list, and the Honeywell Corporate Supplier Assessment.

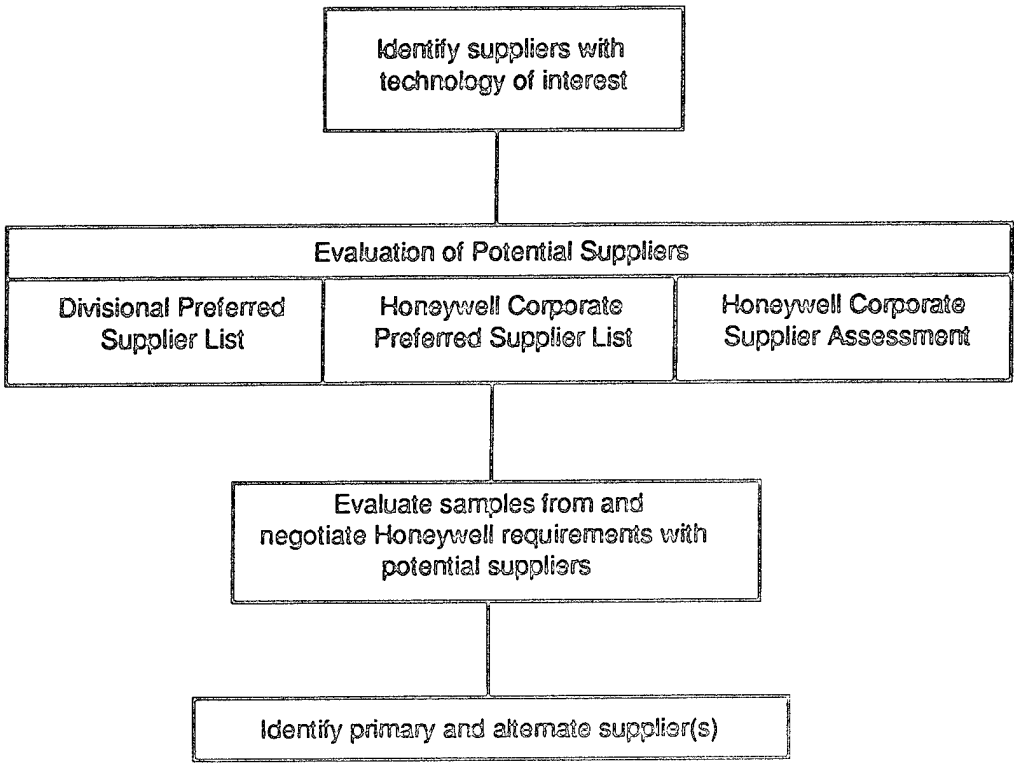


Figure 3.0. IC Supplier Selection Process

Divisional preferred supplier lists that identify preferred, approved, and restricted suppliers are maintained by each operation within CFSG. These lists are subsets of the corporate list tailored according to the needs and experience of each location. The procedure and method of communication of these lists vary by location.

The Honeywell corporate semiconductor commodity's supplier classification list is maintained by the Semiconductor Group Commodity Manager located within Honeywell Corporate Material Services. The list includes microcircuits, discrete, and ASIC semiconductors. Currently the list is based on inputs from representatives of fifteen Honeywell locations. The criteria for supplier classification of preferred, approved, or restricted, contains many facets about the supplier such as performance in delivery/quality/service, technology availability, proactive participation in new designs, cost reduction programs, and programs for product obsolescence. The classification listing is reviewed and modified where necessary on a quarterly basis.

The Honeywell Corporate Supplier Assessment would be used only in the event that the specific part functionality is unique to a non-preferred supplier. The Assessment, which is an audit of various processes within the supplier's organization including management systems, quality systems, sub-supplier control, customer satisfaction, process control, and product development, would be used to determine risk factors associated with a design-in of that supplier's part.

Once the suppliers have been evaluated and the list of potential suppliers has been narrowed, two actions begin in parallel. These actions are to request samples and to begin discussions with the suppliers. It is typical to request enough samples to populate three to four engineering units (or circuit boards). The purpose of the engineering units is to test the functionality of the parts within the application. The discussion with the suppliers centers around the part's capability to meet Honeywell's requirements. These requirements include: (1) the need to operate over an extended temperature range (often past the temperature limits specified for the part), (2) the need for burn-in, (3) the need for the part to meet a specific coplanarity requirement, (4) needs specific to a location's assembly process, and (5) the need for the part to pass Honeywell qualification. As a result of the functionality tests and the outcome of the discussions with the suppliers, the list may be narrowed further. Based on the assessment process and the supplier's ability to meet the needs identified earlier, primary and alternate supplier(s) are selected.

4.0 Task 1.2.5: Describe Specification and Procurement of Plastic

In the case of both plastic and ceramic microcircuits, control drawings are used to identify Honeywell part numbers, performance, quality, and special processing requirements deemed critical to the design, reliability, and producibility of the Honeywell device. The control drawing may be a DESC SMD where one exists for a specific part, it may be a full DoD-STD-100 format Honeywell Source or Specification Control Drawing, or it may be an abbreviated format drawing identifying only special processing needs and referencing manufacturer's performance data where the part being used is an OEM standard catalog product.

The drawings identify directly or indirectly electrical performance characteristics and limits, electrical testing requirements, and functional characteristics to assist the designer in evaluating the part in an application. Also included in the drawing are screening requirements to assure performance over the specified operating temperature and to assure the long-term reliability of the part. In addition to the screening requirements, other processing which would be identified includes: marking requirements, packaging requirements, notification of change requirements, qualification requirements, and quality conformance requirements. Military or industry standards, when available, are referenced for material specifications, test methods, and dimensional requirements. Some typical standards are JEDEC 95, Mil-Std-883, Mil-Std-202, Mil-M-38510 (MIL-PRF-38535), etc.

Key characteristics of the IC procurement process include: pooled purchase agreements, quarterly performance reviews, and the development of long-term partnerships with our suppliers. Each of these items are briefly detailed below.

The current practice of procuring IC's, whether ceramic or plastic, centers around a pooled purchase agreement. At this time, 60 suppliers of semiconductors and 15 locations within Honeywell participate in this annual activity. The locations are responsible for forecasting their annual requirements and entering this information into a joint database. Although the individual part numbers may be available from many different suppliers, pricing is requested from only the preferred or approved suppliers. The rolled-up RFQ is submitted to the suppliers and once the quotes are returned, face-to-face negotiations are scheduled with those suppliers that have a large part number base or that are utilized by several locations within Honeywell. Negotiations via telephone are conducted with the remaining suppliers. A few items worth noting include: all divisions of Honeywell utilizing the same part from the same supplier will receive the same price (regardless of the forecasted quantities), all divisions of Honeywell can utilize any of the prices received for other divisional forecasts—even if they did not forecast the part, and subcontractors of Honeywell are also authorized to use the price agreements. The major purpose of this pooled activity is to form a "one Honeywell" reputation within the semiconductor industry.

Quarterly performance reviews have become a major part of the procurement activity. Performance data is supplied to all 60 suppliers on a quarterly basis. The performance data is supplied in three formats (or charts). One of these charts shows the delivery, quality, service, and a weighted total of the divisional ratings for the supplier over a one-year period. The purpose is to show the trends over that period. Another chart is a matrix that gives the actual ratings, with 100 possible points given by each location for the evaluation of the supplier's quality, delivery, and service. The third chart is a display of best to worst suppliers using the total data (quality/delivery/service) averaged over the past three quarters. Suppliers names are included on this chart which indicates how they are ranked compared to their competitors. The suppliers often show a lot of interest in this chart.

Although the performance data is supplied to all 60 suppliers, face-to-face reviews are held only with the "strategic suppliers" defined by the Corporate Semiconductor Commodity Team. The performance data is supplied two weeks before the reviews along with the action to the suppliers to research prior to the review any ratings less than the 100 mark. The suppliers are also provided a list of various items that they are to address at the review. Some of the items are mandatory and some are optional. The mandatory items include design wins at the Honeywell locations and response to the performance issues that were highlighted in the data. The optional items include new product updates, financial updates, and cycle time reduction programs. Specific actions are generated and followed-up by designated team members.

The last and most important characteristic of Honeywell's procurement process is the development of long-term partnerships with our suppliers. The traditional buying practice of "lowest price buying" is no longer accepted or desired by Honeywell. The objective is to build long-lasting relationships with our preferred suppliers and continue to procure products from them until it becomes absolutely necessary to do otherwise. Quality problems due to slight differences in IC functionality have occurred as a result of switching suppliers, although the parts are supposed to be compatible. We have developed a trust and an expectation of our preferred/strategic suppliers that is evident in their overall performance to Honeywell.

5.0 Task 1.2.6: Describe Part Processing, Production, and Repair Flow

An overview of CFSG's production assembly process flow for surface mount technology (SMT) circuit card assemblies (CCAs) is shown in Figure 5.0. This process flow diagram emphasizes eight main steps: receiving, preparation for soldering, assembly, cleaning, post assembly, testing, delivery, and field repair . The process is supported by three primary sets of enabling requirements in the areas of materials, workmanship, and quality assurance. The process flows for plastic versus ceramic packaged parts are virtually the same except in pre-assembly.

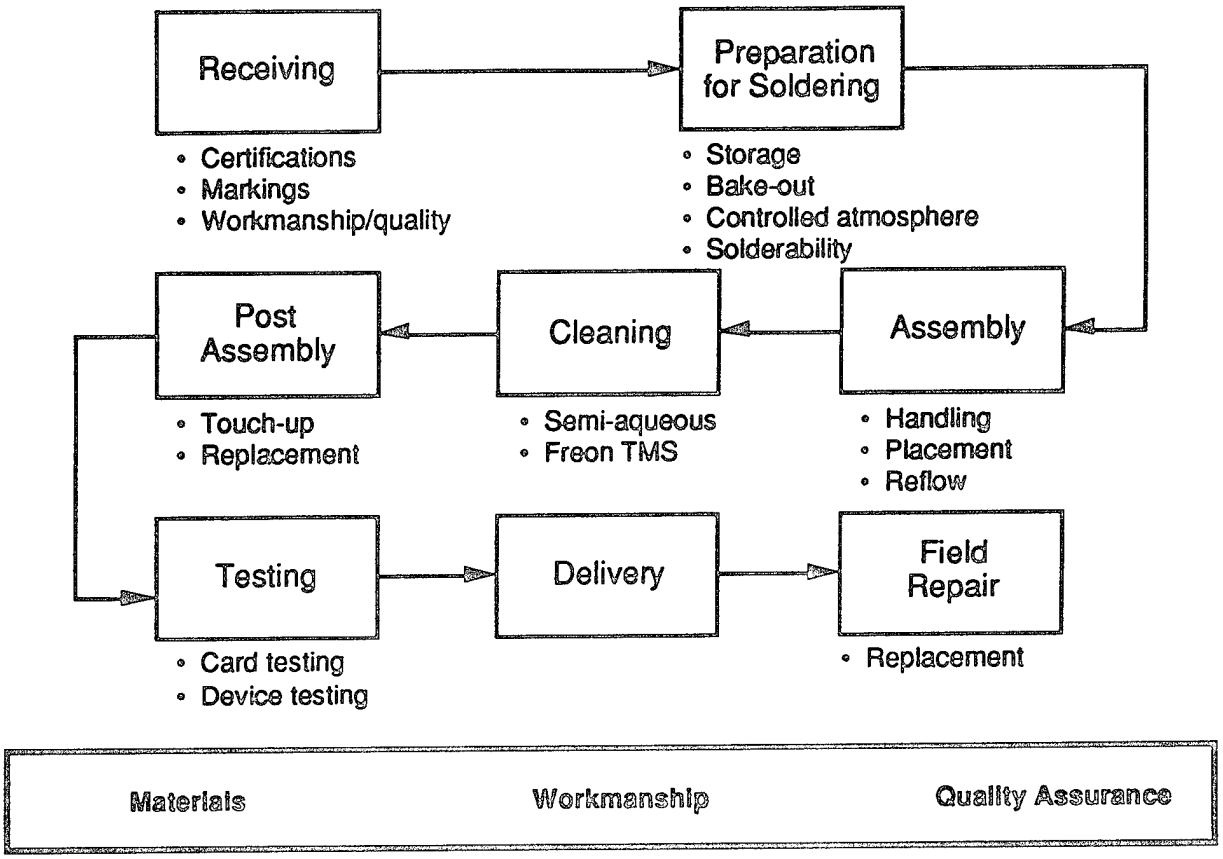


Figure 5.0 Overview of CFSG Production SMT Component Assembly Process Flow

5.1 Receiving

Plastic and ceramic SMT components are inspected for both physical attributes and paperwork compliance when received. Physical attributes are verified for package configuration, part markings, shipping damage, and workmanship. Paperwork is checked for certifications for being from an approved source of supply.

Markings must be sharply defined and legible, and should in no way degrade the electrical or physical requirements for assembly. Marking should not be applied by force marking. Marking inks should withstand the permanence of marking requirements of MIL-STD-883.

5.2 Preparation for Soldering

Printed wiring boards and SMT components should be stored under conditions that do not affect the solderability of surfaces to be soldered. A first in - first out method of using parts should be implemented when kitting for production. Moisture sensitive SMT leaded plastic components may be stored in a controlled environment to preclude baking. Moisture sealed desiccant vendor packaging with moisture indicator may be used during storage if provided for by drawing requirements. An environmentally controlled chamber may be used during storage to prevent moisture absorption.

Two methods are allowable to remove entrapped moisture from plastic SMT components prior to exposure to vapor phase or IR reflow soldering processes. Plastic SMT components must either be stored in a controlled atmosphere of nitrogen with relative humidity less than 10% for a minimum period of 30 days, or be baked at a temperature of 125°C for 22 to 24 hours immediately before assembly. Plastic SMT components must complete the vapor phase or IR reflow soldering process within 48 hours of bake out or removal from the controlled atmosphere.

To ensure solderability of SMT components and maximize solder joint strength, solder coating of the surfaces to be soldered is required unless received from the supplier with solder coating (dipped or plated). Solderability should not be degraded as a result of processing prior to reflow. Component terminations should be solder coated according to CFSG's "Manufacturing Specification for the Solder Coating of Metals." Bridging, webbing, or icicling is not permitted. Parts must be free from contamination after solder coating. The compliancy of SMT leaded component leads should not deviate from the amount initially provided per package design as a result of solder coating.

Leaded through-hole components and connectors must be prepared for soldering in accordance with CFSG's "Manufacturing Specification for Assembling and Machine Soldering of Printed Wiring Assemblies" if wave-soldered, or, "Manufacturing Specification for Soft Soldering of Electrical Connections," if hand-soldered.

5.3 Assembly

PWBs, component leads, and termination pads (including castellations) must be handled in a manner assuring no contact between bare skin and any solderable surface. Clean protective devices (finger cots, gloves, or tooling) are used to meet this requirement. ESD protection must be provided for all applicable components. Internal handling must not alter from print the coplanarity of leaded SMT components.

Solder paste must be handled in a manner that conforms to current safety requirements for lead products. Solder paste shall be stored and used within a time period and under conditions that do not degrade the paste characteristics. Verification of the integrity of solder paste reflow solderability must be performed prior to each production shift and before a newly opened jar is dispensed. Solder paste should not be thinned. A uniform layer of solder paste shall be deposited on component solder pads and subjected to specified acceptance criteria. The PWB and applied solder paste shall be stored and used within a time period and under conditions that do not degrade the paste characteristics.

Components shall be placed onto solder pads using an automatic pick and place machine whenever possible. Hand placement of some components is acceptable. The placement of components shall not cause solder paste smearing or damage to components. Placement accuracy shall be adequate to meet the requirements of post-reflow alignment. Parts that bear identifying bands, dots, or value designations shall be mounted such that all markings are visible, except when precluded by functional or assembly requirements. Adhesive may be used to hold surface mount discrete components in place on the secondary side of the PWB during soldering operations. Placement accuracy shall meet the requirements of post-reflow alignment.

The maximum exposure to any machine soldering operation is two for a single circuit card assembly (CCA). Each CCA part number shall require a documented time versus temperature profile for each machine soldering operation the CCA is exposed to prior to mass soldering production hardware. Leaded through-hole components shall be soldered in accordance with wave-soldering or hand-soldering specifications cited above. Vapor phase or infrared solder paste reflow shall be used for the automatic mass soldering of surface mounted devices. The first CCA of every lot shall be reflowed, cleaned, and submitted to inspection. Inspection's approval of the first piece is authorization for production to run the remaining CCAs in the lot. Secondary side SMT components staked to the PWB shall be soldered in accordance with CFSG's wave-soldering specification.

Solder joints should indicate evidence of wetting and adherence where the applied solder blends to the soldered termination surface. A line of demarcation or transition zone where applied solder blends with the soldered termination surface shall be acceptable provided wetting is evident. Solder joints may be shiny or dull/matte in appearance. Solder joints shall not exhibit bridging, webbing, solder balls, slivers, whiskers, contamination, cracks, fractures, blowholes or other defects, flux residues, or less than minimum conductor spacing. There are specific soldering requirements for leadless chip carriers, gull wing leads, J-leads, various-sided termination rectangular components, cylindrical end cap terminations, and flat ribbon leads.

The conformal coating process must not allow coating to flow under or fillet around the perimeter of SMT components. Dipping shall not be allowed as a method of application. Conformal coating materials shall be according to drawing requirements.

5.4 Cleaning

Prior to assembly, all PWBs shall be cleaned to remove surface contaminants. Boards shall be cleaned during that working shift in which solder paste is to be applied. SMT components supplied to the production floor without the protection of original vendor packaging, or SMT components that require manufacturing process prior to placement (solder coating) shall be cleaned prior to placement. SMT components supplied in original vendor packaging are not to be cleaned prior to placement. provided proper handling procedures are followed at incoming inspection, stock room, and assembly floor.

The cleaning processes used are semi-aqueous for sequential in-line cleaning and vapor degrease for batch processing. The solvents used are Axarel and Freon TMS respectively.

Cleaning procedures shall be adequate to remove flux residue from under all SMT components (including leadless chip carriers) after any soldering operation. Cleaning solvent shall be compatible with each individual part of the completed assembly.

Cleanliness of the assemblies shall be checked visually and by removing SMT components from a test PWB on a sample basis and confirming cleanliness under the parts using MIL-P-28809A Resistivity of Solvent Extract Method. Evidence of cleaning residues (e.g., white film, apparent flux stains surrounding components) shall be acceptable only if PWBs can be shown to meet or exceed the MIL-P-28809A resistivity test.

5.5 Post Assembly

The general requirements for assembly touch-up, rework, and replacement of plastic SMT components does not differ from ceramic components. The general requirements for assembly touch-up, rework, and repair operations must conform to the requirements for soldering preparation, solder joints, and workmanship. If present, conformal coating shall be removed in the area of the required correction using Toluene or Freon TMS. Removal will be performed prior to performing assembly correction and reapplied according to the drawing requirements after successful correction.

Diluted flux shall be used in assembly correction technique operations when reflowing solder on assemblies that will be only locally cleaned. Nondiluted mildly activated rosin flux may be used if the entire assembly will be subsequently cleaned. Visual flux residue shall be removed from the PBW if it appears during correction. Temperature extremes, gradients, and exposure time shall be minimized when correcting SMT assemblies. Use of preheat cycles prior to correction is recommended. The standard specified solder shall be used for assembly corrections.

Touch-up of solder connections is a critical process allowed to bring unacceptable solder joints of any SMT component into compliance with the solder fillet requirements. Touch-up shall be performed with the use of a soldering iron. Physical movement of components is considered rework. Correction of bent component leads shall not be allowed. Use of hot-air rework tools are not allowed for touch-up, their use constitutes rework.

Rework of SMT assemblies is allowed to restore the functional capability of a defective assembly, restoring the appearance and uniformity to that of initial assembly. Rework shall be allowed on SMT assemblies provided the assembly is not damaged below the functional requirements of the drawing. All rework operations shall be documented on the tag of the SMT assembly. Hot-air reflow tools are not to be used for discrete component rework, but only for multitermination (five or greater) SMT component packages (LCC, PLCC, SOIC, etc.).

The maximum number of individual SMT component removal, replacement, and/or realignment cycles allowed in any one SMT component PWB footprint area using hot-air repair tools is six over the entire life of the PWB. This limit is imposed to keep the failure risk of the 0.016-inch diameter (or smaller) PWB via holes used on SMT PWBs to a minimum. A single removal, replacement, or realignment of an individual SMT component constitutes one cycle for the PWB footprint area of the reworked SMT component, as well as one cycle for the PWB footprint areas of all adjacent SMT components (regardless of type, i.e., including discretes). An adjacent SMT component is defined as an SMT component with at least one 0.016-inch diameter (or smaller) PWB via hole located within the appropriately defined adjacency zone. Before removals, replacements, or realignments are made, the total number of previous cycles must be determined by examining the assembly's tag documentation. Additional cycles must not violate this requirement. The resulting cycles of SMT components adjacent to removed, replaced, and/or realigned SMT components are not documented/tracked on assembly tags. However, the operator must account for the resulting cycles when determining the total number of cycles that an area of the PWB has been exposed to.

Ceramic SMT components may be exposed to individual reflow cycles provided the functionality of the reworked components are not degraded. Mass component removal and replacement (majority of components from an existing CCA) shall be submitted for material review action.

Plastic SMT components may be exposed to one realignment cycle, provided the realignment cycle is completed immediately after initial reflow, prior to the reabsorption of moisture into the plastic SMT component. Plastic SMT components shall be discarded after one removal cycle. The replacement of plastic SMT components shall be accomplished with new parts prepared according to the applicable requirements.

A soldering iron shall be used for few lead (four or less) SMT component packages (chip capacitors, chip resistors, SOT, etc.). The maximum number of iron heating cycles allowed per PWB solder pad is limited such that the workmanship requirements are not violated. The maximum number of iron heating cycles allowed per SMT component termination is two. The cycles are allowed only to correct alignment defects. SMT components shall be discarded after one removal cycle.

5.6 Testing

Both card- and device-level testing are identical for plastic and ceramic SMT components.

5.7 Field Repair

Replacement procedures for plastic and ceramic SMT components are the same.

Repair of SMT assemblies is allowed to restore the functional capability of a defective assembly, however not to restore the appearance and uniformity of the assembly as it was after initial assembly. Repair shall be allowed on SMT assemblies provided the assembly is not degraded below the functional requirements of the drawing or standard Honeywell CFSG requirements. Repair operations not herein stated shall not be permitted without appropriate engineering instructions. All repair operations shall be documented on the tag of the SMT assembly.

5.8 Materials

Processing materials are specifically specified for the production assembly process. These include: solder (paste, bar, and rosin cored wire solder), liquid soldering flux (rosin flux, synthetically activated flux, and diluted flux), solvents (Freon TMS, Prelete, isopropyl alcohol, Toluene), adhesive, wire, rigid printed wiring boards (PWBs), and surface mount components (SMCs).

5.9 Workmanship

Specific specifications for workmanship, called out for SMT assembly characteristics, magnification aids (for visual inspection), cleanliness, handling, and packaging, are the same whether using plastic or ceramic packaged components . Contaminants, corrosion, flux residue, or fingerprints on any part of the assembly shall not be acceptable. Evidence of physical heat or solvent damage to any part of the assembly shall not be acceptable. Blistering and delamination of PWBs are unacceptable. Measling and crazing of PWBs are acceptable provided that the total area affected shall not exceed 10% of the total board area. Defects in nonfunctional areas and defects in functional areas shall not account for more than 50% of the space between noncommon conductors.

5.10 Handling and Packaging

Assemblies with plastic or ceramic packaged components shall be given ample protection against damage throughout the assembly process. Assemblies shall be placed in individual bags or compartmentalized boxes during transit or storage. All active components, static sensitive components, and assemblies shall be protected from electrostatic (ESD) damage.

5.11 Quality Assurance

Provisions for quality assurance are the same whether using plastic or ceramic packaged components, including sufficient inspection, testing, and process control, to ensure that a finished product meets all the production manufacturing requirements and the requirements of applicable engineering drawings and bulletins. Violation of any of these requirements can be submitted for material review action if the violation is repairable.

Appendix C
Task 2.1 Report–Reliability Prediction Methodology

Prepared by Bruce Johnson on August 15, 1995
Revision A Dated September 8, 1994

C.1 Scope

This report describes the reliability prediction methodology used by Honeywell's Commercial Flight Systems/Minneapolis Operation (CFS/MO). Microcircuit failure rates used in reliability predictions as well as their source and factors effecting them are discussed.

C.2 Prediction Method

The prediction method employed by CFS/MO is a piece part prediction method using CFS/MO failure rates. There are no differences in the prediction methodology or failure rates between ceramic and plastic microcircuits. This has not always been the case. Initially, when plastic microcircuits were to be introduced to Honeywell products, a failure rate multiplier of 2 was applied to the ceramic microcircuit failure rates for use with plastic microcircuits. Since that time, the failure rate multiplier was reduced to 1.5 and then to the current 1.0. The basis of this change was largely qualitative, coming from Honeywell's experience with qualification testing of plastic parts and information learned through close coordination with suppliers.

The steps in the prediction process are as follows:

- Step 1—Device parts lists are reviewed with all electrical piece parts categorized relative to failure rate groupings. These groupings are discussed further in Subsection C.3.1. Part types that do not fit into an existing category are listed individually.

- Step 2—Part failure rates are assigned to each grouping based on CFS/MO's failure rates. Failure rates for miscellaneous part types that do not fit existing groupings are developed in the manner described in Subsection C.3.1 and assigned to these part types.

- Step 3—The assigned failure rates are multiplied by the number of parts in the grouping or number of miscellaneous part, then summed to determine the total unit failure rate.

C.3 Failure Rates

C.3.1 Values

The failure rates listed in Table C.3.1-1 are the integrated circuit failure rates specifically applicable to equipment designed and built by Honeywell CFS/MO for use in commercial air transport aviation applications. The part

groupings identified below are not inclusive of all integrated circuit types but provide a base set of failure rates for which data has been historically collected and analyzed.

When part failure rates are required that do not appear in the listing, or when the environment is other than described (i.e., temperature, vibration, and nominal rate of power cycling of once every one to three hours), vendor failure rate information, comparisons with previously classified components of similar complexity, and/or modified MIL-HDBK-217 derived failure rates estimates are used as a basis for failure rate determination.

Table C.3.1-1. CFS/MO Integrated Circuit Piece Part Failure Rates

Part Grouping	Failure (Per Million Operating Hours)
Small Scale, digital, bipolar (<20 gates)	0.011
Small Scale, digital, MOS (<20 gates)	0.017
Medium Scale, digital, bipolar (21 to 100 gates)	0.022
Medium Scale, digital, MOS (21 to 100 gates)	0.033
Large Scale, digital, bipolar (>100 gates)	0.03
Large Scale, digital, MOS (>100 gates)	0.05
Micro-Processors	
MPROC, bipolar	0.142
MPROC, (8 bit), MOS	0.192
MPROC, (16 bit), MOS	0.214
MPROC (32 bit), MOS	1.574
Analog IC's, Bipolar	0.022
Analog IC's, MOS	0.033
Memory Devices	
(E)PROM, 256 bit, bipolar	0.060
(E)PROM, 256 bit, MOS	0.088
(E)PROM, 512 bit, bipolar	0.066
(E)PROM, 512 bit, MOS	0.098
(E)PROM, 1024 bit, bipolar	0.074
(E)PROM, 1024 bit, MOS	0.106
(E)PROM, 2048 bit, bipolar	0.080
(E)PROM, 2048 bit, MOS	0.118

Table C.3.1-1. CFS/MO Integrated Circuit Piece Part Failure Rates (Concluded)

Part Grouping	Failure (Per Million Operating Hours)
(E)PROM, 4096 bit, bipolar	0.088
(E)PROM, 4096 bit, MOS	0.134
(E)PROM, 8192 bit, bipolar	0.098
(E)PROM, 8192 bit, MOS	0.146
(E)PROM, 16384 bit, bipolar	0.106
(E)PROM, 16384 bit, MOS	0.162
RAM, 256 bit, bipolar	0.088
RAM, 256 bit, MOS	0.134
RAM, 512 bit, bipolar	0.098
RAM, 512 bit, MOS	0.152
RAM, 1024 bit, bipolar	0.106
RAM, 1024 bit, MOS	0.166
RAM, 2048 bit, bipolar	0.118
RAM, 2048 bit, MOS	0.178
RAM, 4096 bit, bipolar	0.134
RAM, 4096 bit, MOS	0.200
RAM, 8192 bit, bipolar	0.146
RAM, 8192 bit, MOS	0.222
RAM, 16384 bit, bipolar	0.162
RAM, 16384 bit, MOS	0.244

C.3.2 Sources

CFS/MO failure rates date back to a "Reliability Prediction Handbook," dated March 4, 1974. These failure rates are updated to assure that reliability predictions for new products reflect the revenue service reliability experience of CFS/MO design, procurement and production processes.

CFS/MO has accumulated over 120 million device operating hours in revenue service on inertial reference products over the last 11 years. Periodically, portions of this data are analyzed to assess current field failure rates. The most recent failure rate update was based on over 12 million device operating hours of revenue service. In total, the number of experienced electronic failures in this reporting period was approximately 45% of the number of failures that were predicted using the previous CFS/MO baseline failure rates (i.e., the actual MTBF of electronics is about double that was predicted).

C.3.3 Factors Effecting

Though the generic failure rate for a given part may be a fixed quantity, it can be degraded by a number of factors thus effecting the actual field failure rate experienced. Four of the major factors which are discussed in the following paragraphs, are:

1. Stress both electrical and thermal
2. Part practices such as selection, procurement and handling
3. Production processes
4. Field usage

C.3.3.1 Electrical/Thermal Stresses—Electrical and thermal derating of electrical components is part of the typical design process and, as such, is included in the basic failure rates. Part's Application Analysis of every electrical component is used to verify compliance with CFS/MO thermal and electrical derating guidelines, including criteria such as junction temperature, voltage stress and current stress levels. Piece part failure rates are not strongly influenced by temperature or electrical stress provided the CFS/MO derating standards are adhered to. The need for additional adjustment with failure rate derating curves in unnecessary.

The part failure rates listed in Table C.3.1-1 are based on data obtained in a commercial airborne equipment bay environment where temperatures are as follows:

1. Average equipment operating temperatures are on the order of 35°C.
2. Average part ambient temperatures are on the order of 50°C.
3. Semiconductor junction temperatures under normal operating conditions not to exceed 85°C.
4. Semiconductor junction temperatures under maximum operating conditions not to exceed 110°C.

C.3.3.2 Part Practices—Designing a part into a product prior to careful evaluation in the areas of, electrical and mechanical specifications, qualification, quality and production process issues, can lead to a device not being able to achieve expected reliability.

Paragraphs 3.0 and 4.0 from the "Draft Interim Report," dated August 2, 1993 contain, as Task 1.2.4 and 1.2.5, a description of CFS/MO's semiconductor supplier selection and procurement processes. The process described is considered to be a factor in the field failure rates experienced on CFS/MO products. The key is to work closely with the supplier in a partnership arrangement to find the best overall part for an application even if it means impacting the design.

C.3.3.3 Production Processes—All areas of part handling from receiving inspection, through the build process to final test and delivery, provide opportunities for defects to be introduced into a part or product. ESD is a classical example of this. It is commonly held that for every ESD damaged part identified. There is another part, termed "walking wounded," that remains operational but will likely fail in the field.

Paragraphs 5.0 from the "Draft Interim Report" dated August 2, 1993 contain, as Task 1.2.6, a description of CFS/MO's part processing and production processes. The process described is considered to be a factor in the field failure rates experienced on CFS/MO products.

C.3.3.4 Field Usage—In a similar manner to "Production Processes," field usage processes offer opportunities for defects to be introduced. Field usage processes include all customer operations (installation/maintenance/removal) and both customer and supplier repair operations.

CFS/MO prepares detailed installation manuals as well as manuals for all three levels of maintenance. The Installation Manual provide details regarding mounting, cooling and access requirement for the product. Compliance to the Installation Manual assures that both mechanical and electrical mounting as well as environmental conditions are appropriate and will not degrade field reliability.

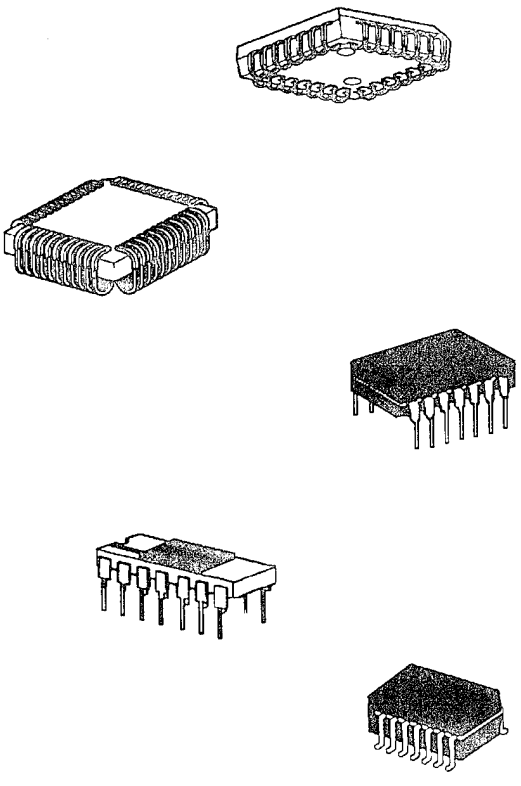
Maintenance procedures include on aircraft fault isolation, card replacement and card repair procedures to the piece part level. These procedures will be performed in part or completely by end item customers, though most piece part repair is performed within Honeywell service centers or production facilities. Improper maintenance offers another opportunity for introduction of defects into the product which will lead to a future failure of the device.

PLASTIC PACKAGE AVAILABILITY PROGRAM

NSC FAILURE ANALYSIS

SECTION 9

Task 7.0 Devices Reliability Testing



Failure Analysis Report

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The NSC Failure Analysis Team: Andrea Chen, Thomas Pak, Joseph Bendik, Clare Gomes, Chris Sanborn, Walter Bachmann, Amarjit Paintal, Eileen Desmond

Assistant Program Manager: Joseph Bendik

1.0 Introduction:

The information in this report was generated by the NSC Failure Analysis Team. Samples were prepared and analyzed in the NSC failure analysis lab in building D and the packaging lab in building 19.

1.1 Reliability and Failure Analysis:

~2000 plastic and ceramic parts were used in the PPA DOE. The majority of these parts were sent to NSC and CRANE for reliability testing; i.e., HAST, HTS, TC, OPL, and Salt Fog.

Most of the plastic and ceramic parts used for F/A were pulled from the various legs of reliability testing. The F/A team was given the task of investigating the possible cause of GROSS functional failure. The plastic and ceramic packages that were used for reliability testing are shown in the Master Failure Analysis Chart-**figure 1.** This chart can be used to quickly identify which reliability tests generated functional failures. A "zero hour base line" was created by using plastic parts which were not sent to reliability testing.

Figure 1

MASTER FAILURE ANALYSIS CHART

= ET failures found in cell

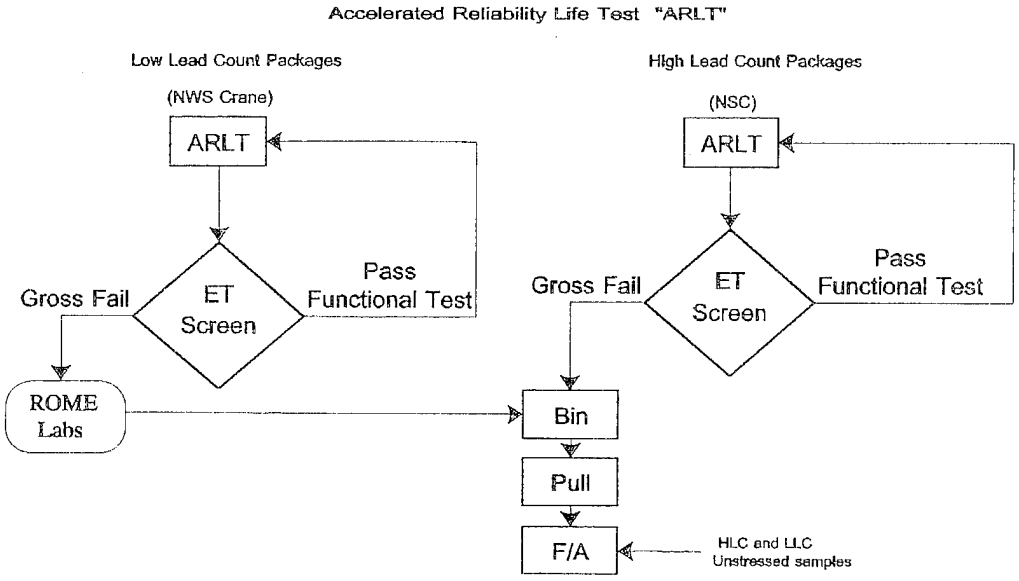
Package	130°C HAST	159°C HAST	TC-65°C/150°C	HTS 175°C	OPL 125°C
 Control 68L CQJB	0/22 @ 1296 Hrs	0/24 @ 648 Hrs	0/25 @ 2000 Cycles	0/45 @ 4125 Hrs	0/24 @ 4000 Hrs
 Preconditioned	22/40 @ 1296 Hrs	44/63 @ 216 Hrs	12/144 @ 2000 Cycles	0/72 @ 4125 Hrs	0/60 @ 4000 Hrs
Non-Preconditioned 68L PLCC	0/60 @ 1296 Hrs	9/42 @ 648 Hrs		0/54 @ 4125 Hrs	0/60 @ 4000 Hrs
 5 Volts	1/45 @ 1080 Hrs	29/45 @ 648 Hrs	0/150 @ 1512 Cycles	0/150 @ 1512 Hrs	Not Performed
30 Volts 14L SOIC	30/45 @ 1080 Hrs	39/45 @ 216 Hrs			
 Preconditioned	25/45 @ 1080 Hrs	39/45 @ 216 Hrs	0/150 @ 1512 Cycles	4/150 @ 1512 Hrs	Not Performed
Non-Preconditioned 14L DIP	1/45 @ 1080 Hrs	30/45 @ 648 Hrs			
 5 Volts	0/15 @ 1080 Hrs	0/15 @ 648 Hrs	1/50 @ 1512 Cycles	0/50 @ 1512 Hrs	Not Performed
Control 30 Volts 14L CERDIP	1/15 @ 1080 Hrs	0/15 @ 648 Hrs			

Cum Failures / Total Sample Size @ Cum Hours

1.2 Failure Analysis-process flow:

Ceramic and Plastic parts which failed ET were sent to NSC and ROME laboratories for F/A. Parts were grouped into test cells as shown in **figure 1**. The following process flow (**figure 2**) illustrates how parts moved into NSC F/A.

Figure 2

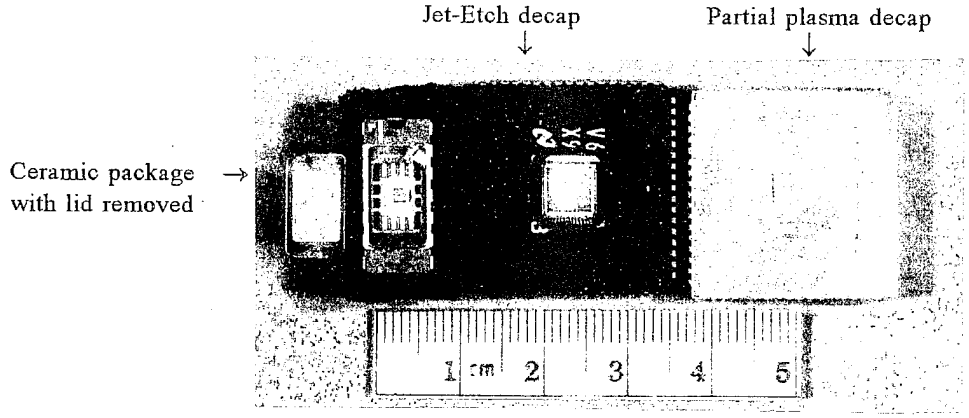


1.3 Opening Plastic Packages:

The following three methods were used to open plastic packages: **Jet Etch**-The B&G-200 nitric decapsulation system ejects a fuming stream of hot nitric and sulfuric acid onto the surface of the plastic package. A picture of a jet etched part is shown in **figure 3. Plasma Etch**-The Technics / GmbH-100E plasma etcher is a dry decapsulation system which employs a low temperature ashing system. The system automatically blows off the sample every 10 minutes to maintain an optimum etch rate. A picture of a plasma etched part is shown in **figure 3.**

Mechanical - Any method of directly opening a plastic part by force.

Figure 3



2.0 F/A Rationale:

The following general procedures were used:

Highly Accelerated Stress Test (HAST)-Plastic samples were sent for CSAM and X-Ray analysis in order to investigate potential die paddle delamination. Electrical continuity tests were performed on both plastic and ceramic samples to verify wire bond integrity. Plastic samples were decapped by jet etch, plasma, and mechanical techniques. Ceramic parts were "de-soldered" by standard techniques. Optical microscopy and SEM techniques were performed before and after PIQ / passivation removal. Several wet chemical etches were used to enhance potential defects: (KOH, HCL, 10:1 HF, Silicon type etches, and soap). These recipes and others can be found in *Thin Film Processes* [1].

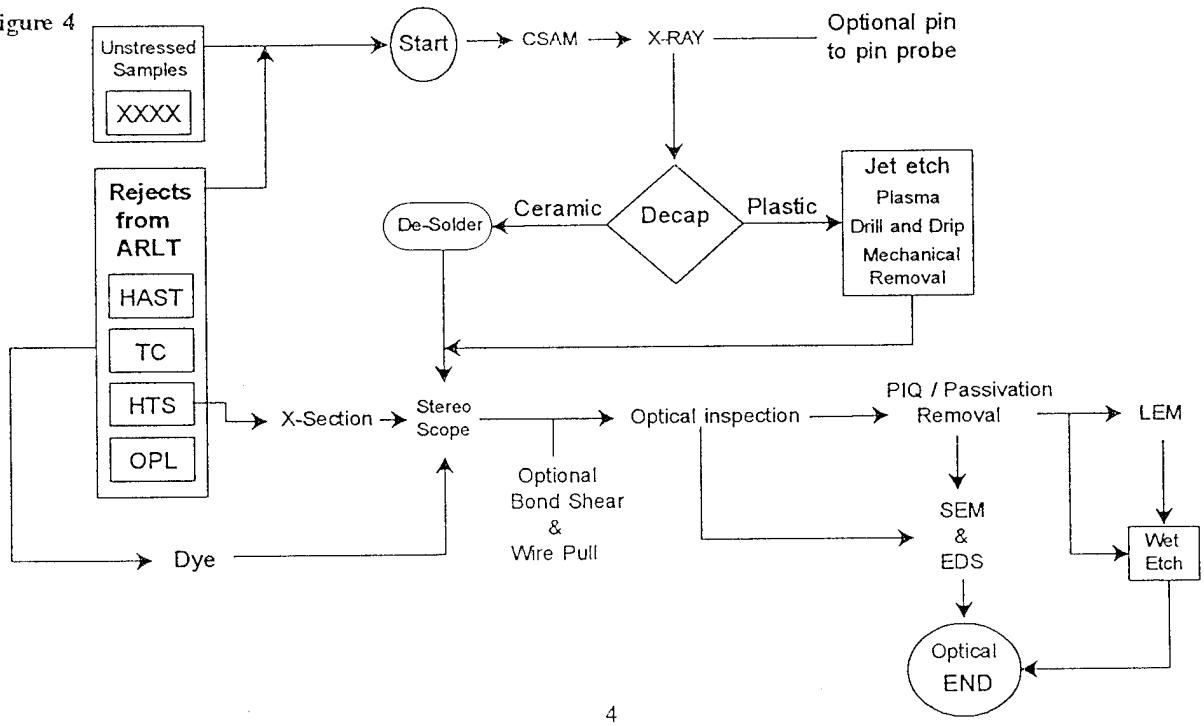
Temperature Cycle (TC)-Plastic samples were sent for CSAM and X-Ray analysis in order to investigate potential die paddle delamination. Plastic parts were decapped by both jet etch and plasma techniques. Ceramic parts were "de-soldered" by standard techniques. Optical microscopy and SEM techniques were performed before and after PIQ / passivation removal. Plastic packages that are subjected to temperature cycling usually show signs of stress induced cracking. Discussions and F/A techniques on this subject can be found in the following reference [2].

High Temperature Storage (HTS)-Plastic samples were sent for CSAM and X-Ray analysis in order to investigate potential die paddle delamination. Electrical continuity tests were performed on both plastic and ceramic samples to verify wire bond integrity. Plastic parts were decapped by jet etch, plasma, and mechanical techniques. Ceramic parts were "de-soldered" by standard techniques. Optical microscopy and SEM techniques were performed before and after PIQ / passivation removal. Cross-section, ball shear, and wire pull tests were used to investigate possible changes in bond pad metallurgy. Several discussions on HTS, Intermetallic growth, and Kirkendall effects can be found in references [3]-[4].

Operational Life Test (OPL)-No failures reported

The following flow chart (**figure 4**) illustrates how different parts moved through the F/A flow sequence.

Figure 4



3.0 High Lead Count Devices (HLC) Data Summary:

When reading sub-section 3.0 refer to figure 5-Master High Lead Count F/A Chart-for test cell information.

Figure 5

Master HLC Failure Analysis Chart

Package for SCX 6244	130°C HAST	159°C HAST	TC-65°C/150°C	HTS 175°C	OPL 125°C
68L CQJB  Control	No Fails	No Fails	No Fails	No Fails	No Fails
 68L PLCC Preconditioned ULS12H ULS12HX X9074 B24	- - - - - 10/20 @ 1296 Hrs - - - - - 12/20 @ 216 Hrs	12/21 @ 216 Hrs - - - - - 21/21 @ 216 Hrs 11/21 @ 72 Hrs	12/36 @ 2000 Cycles Preconditioned vs Non-preconditioned part identity-inadvertently lost	No Fails	No Fails
 68L PLCC Non-Preconditioned ULS12H ULS12HX X9074 B24	No Fails	- - - - - 5/21 @ 648 Hrs - - - - - 4/21 @ 648 Hrs		No Fails	No Fails

Cum Failures / Total Sample Size @ Cum Hours - - - - - = Cell Not Populated in DOE

3.1 HLC / 68L PLCC / Preconditioned samples from 130°C HAST:

Plastic packages molded with ULS12HX and B24 were processed through F/A as shown in **figure 4.** Ball shear data are listed in **Table 1**. Wire bond continuity tests were performed on each part listed in Table 1.

After jet etch decap and PIQ removal, 9 die surfaces were optically inspected; most areas appeared defect free. In addition, 6 die surfaces which were etched in KOH did not show signs of passivation cracking. (see **figure 6**).

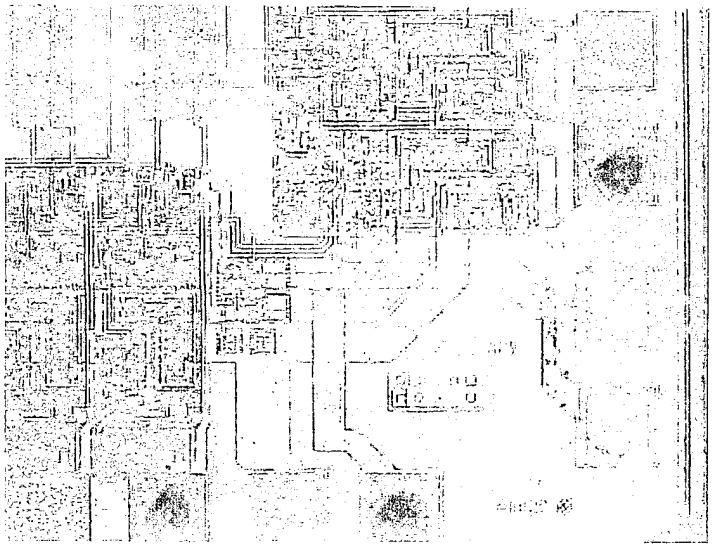
Table 1

HLC Ball Shear HAST

Unit Type		HAST	Average Ball Shear	Sigma
X9074	Preconditioned	159°C 72 hours	39.51	14.96
B24	Preconditioned	130°C 216 hours	80.28	13.99
B24	Preconditioned	159°C 72 hours	54.07	14.36
Unstressed Plastic Packages			~90	

units=grams

Figure 6

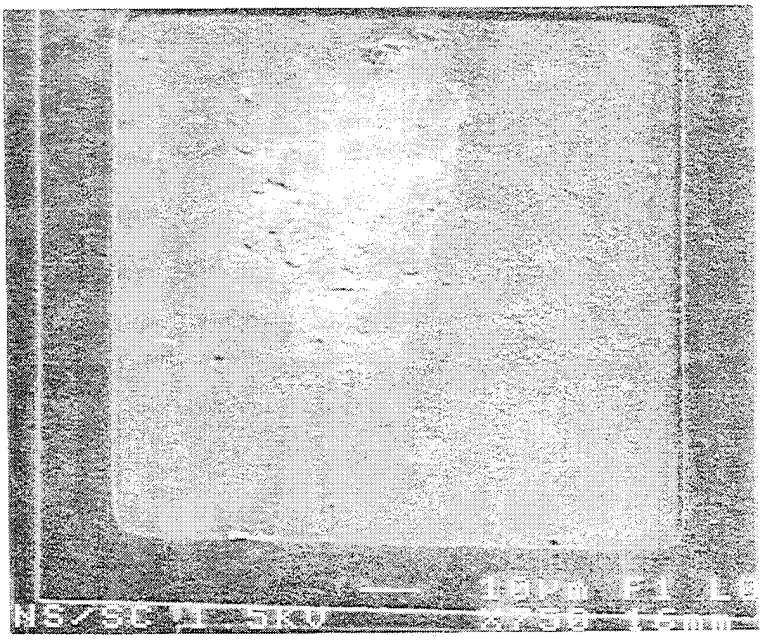


KOH Etch
No Passivation Cracks
HAST 130°C @ 1296 hrs.
ULS12HX Preconditioned
1

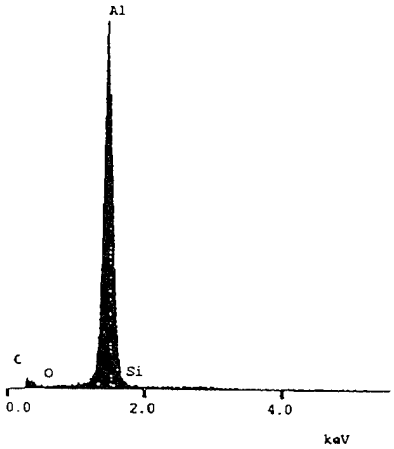
3.1 Continued HLC / 68L PLCC / Preconditioned samples from 130°C HAST:

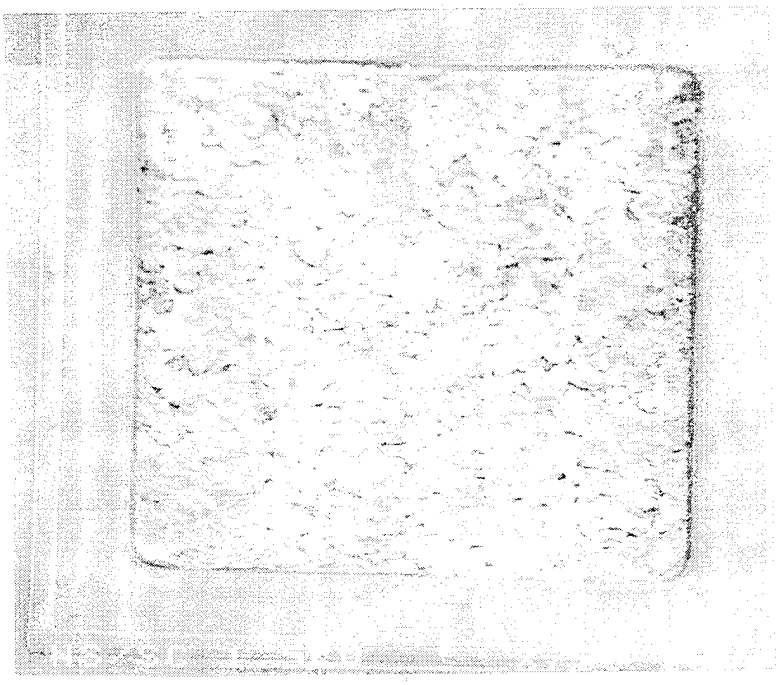
Figure 7 shows the typical surface of the aluminum bond pads from preconditioned 130°C HAST failures @ 216 hours. The SEM/EDS data indicates that the bond pads have oxidized.

Figure 7

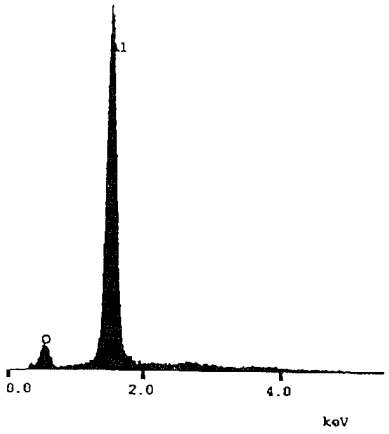


SEM & EDS Data
"Normal"
aluminum bond pad
unstressed device
(Non-Bonded Pad)





SEM & EDS Data
"Oxidized"
aluminum bond pad
HAST 130°C @ 216 hrs.
ULS12HX preconditioned
(Non-Bonded Pad)

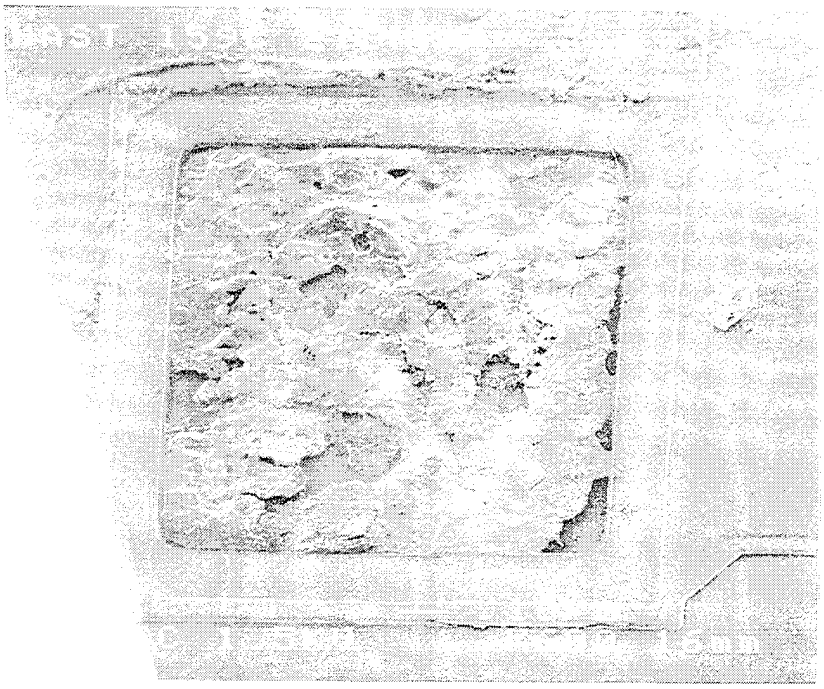


3.2 HLC / 68L PLCC / Non-Precondition / 130°C HAST:
Plastic packages molded with ULS12H, ULS12HX, and X9074 did not fail ARLT @ 1296 hours. No survey parts were analyzed.

3.3 HLC / 68L PLCC / Preconditioned samples from 159°C HAST:

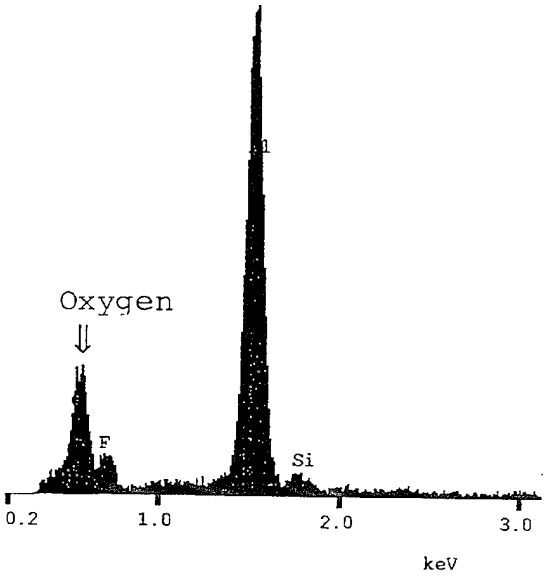
Plastic packages molded with ULS12H, X9074, and B24 were processed through F/A as shown in **figure 4**. Ball shear data for packages which failed 159°C HAST @ 72 hours are listed in Table 1. SEM inspections on preconditioned 159°C HAST failures revealed several corroded aluminum bond pads (**figure 8**). The EDS data is shown in **figure 9**.

Figure 8



Corroded Aluminum
Bond Pad
HAST 159°C @ 216 hrs.
X9074 # 15 preconditioned
(Non-Bonded Pad)

Figure 9

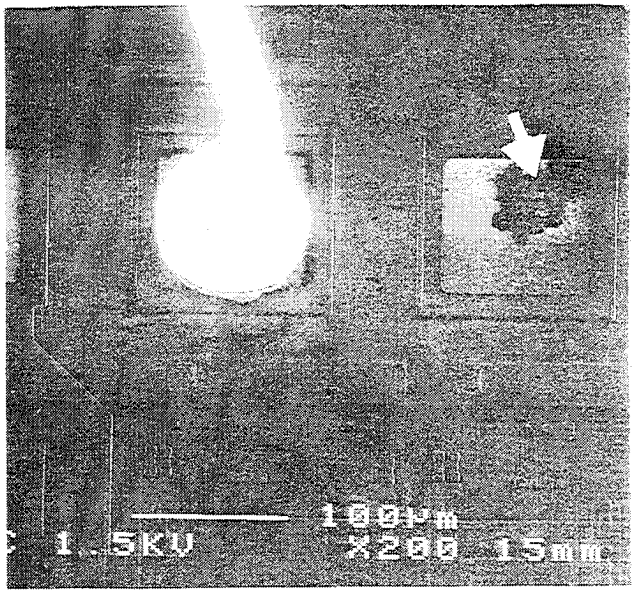


EDS Data
Corroded Aluminum
Bond Pad
HAST 159°C @ 216 hrs.
X9074 # 15 preconditioned

3.4 HLC / 68L PLCC / Non-Preconditioned samples from 159°C HAST:

Plastic packages molded with ULS12HX and B24 were processed though F/A as shown in **figure 4.** The first failures from non-preconditioned 159°C HAST occurred at 648 hours. Typical SEM/EDS data for non-preconditioned 159°C HAST failures are shown in **figure 10**. Note the dark oxidized material on the aluminum bond pad in **figure 10**. The fracture surface of a broken gold wire bond is shown in **figure 11**. Note that part of the aluminum bond pad has been removed. This was the only wire bond that was separated from the bond pad. Three out of five failed devices had broken bonds. The jet etch used in our F/A rarely removes reliable wire bonds.

Figure 10



SEM & EDS Data
Dark Oxidation
HAST 159°C @ 648 hrs.
B24 # 9 Non-preconditioned

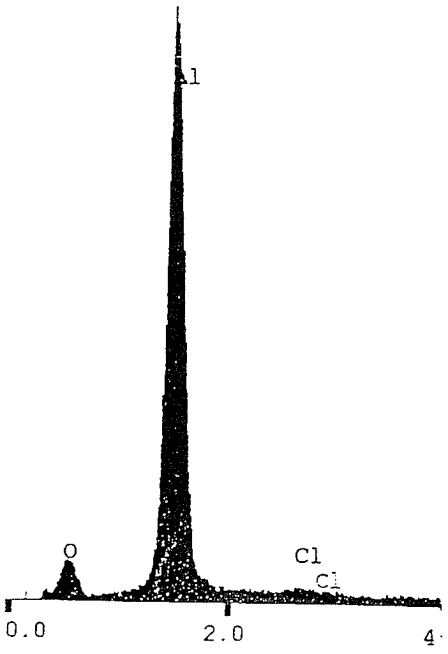
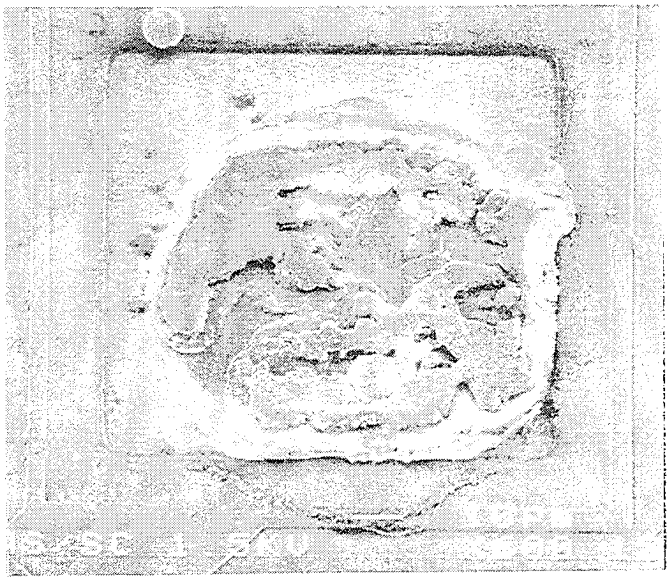


Figure 11



Broken Gold Wire Bond
HAST 159°C @ 648 hrs.
B24 # 9 Non-preconditioned

3.5 HLC / 68L PLCC / Preconditioned and Non-Preconditioned samples from (TC):

Plastic packages molded with ULS12H, ULS12HX, X9074, and B24 were processed through F/A as shown in **figure 4.** CSAM was performed on 12 parts (ULS12H) that failed @ 2000 cycles.
(see **figure 12**) Note: All 12 failed devices show delamination.
Typical X-Ray images are shown in **figure 13** Note: No cracks were detected on any of the 12 failures.

Figure 12

CSAM After 2000 Temperature Cycles
ULS12H (6 of 12 failures)

Top View

Bottom View
Note: delamination

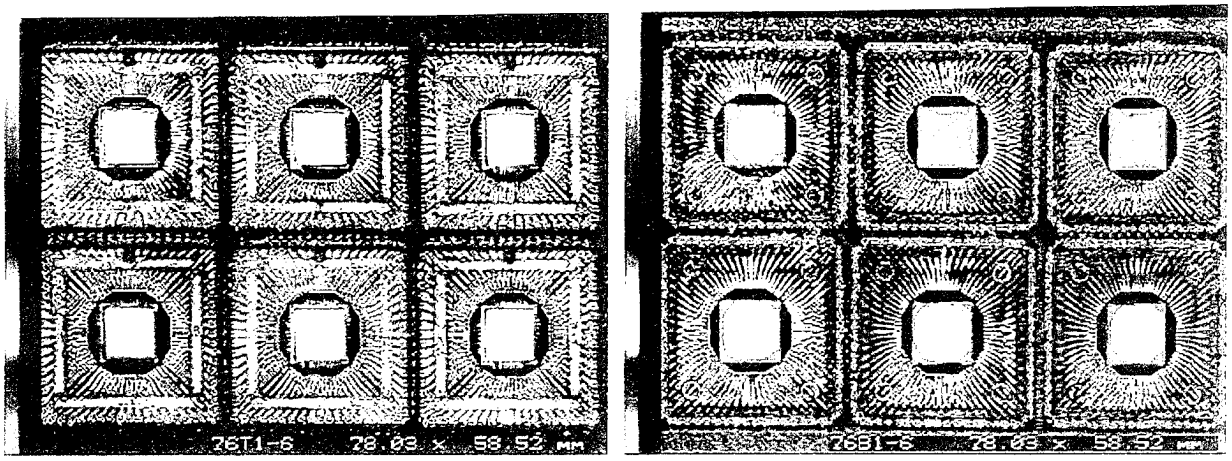
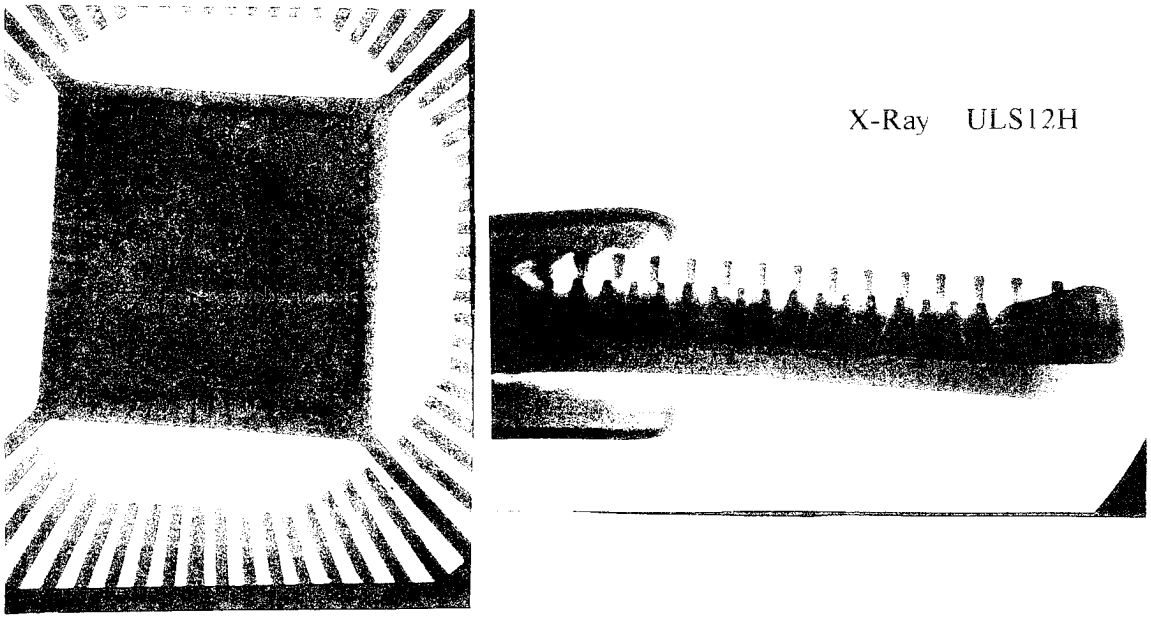


Figure 13

X-Ray ULS12H



3.5 Continued HLC / 68L PLCC / Preconditioned and Non-Preconditioned samples from (TC):

Twelve ULS12H plastic packages failed TC @ 2000 cycles. The ET data collected from ARLT indicated that shorts, opens, failed diodes, and logic problems were the main failure modes. Manual pin to pin probing identified several problem input structures. This data was used to create a "failure map" of the device. Ten of these parts were decapped and inspected optically. Only a few small defects were observed in the passivation. These flaws were not seen with the SEM both before and after PIQ / passivation removal. Several packages were prepared for LEM. The LEM system failed to find any hot spots or high current areas. (see **figure 14**) Note: The photo shows a diode in "normal" operation

Figure 14

Typical LEM Emission
Voltage Applied to Vss

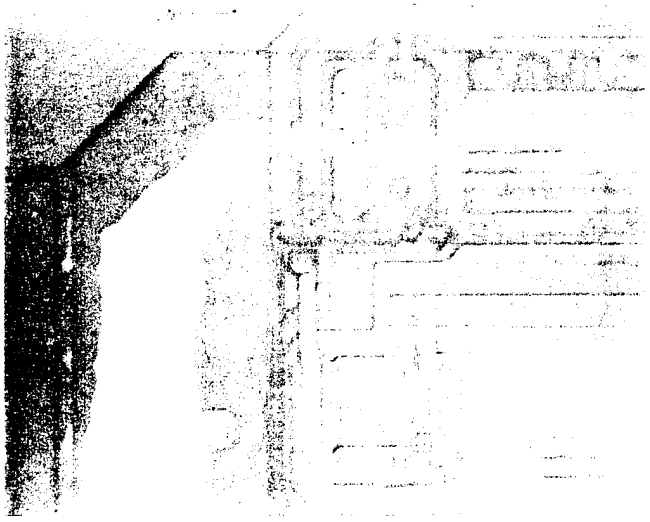


3.5 Continued HLC / 68L PLCC / Preconditioned and Non-Preconditioned samples from (TC):

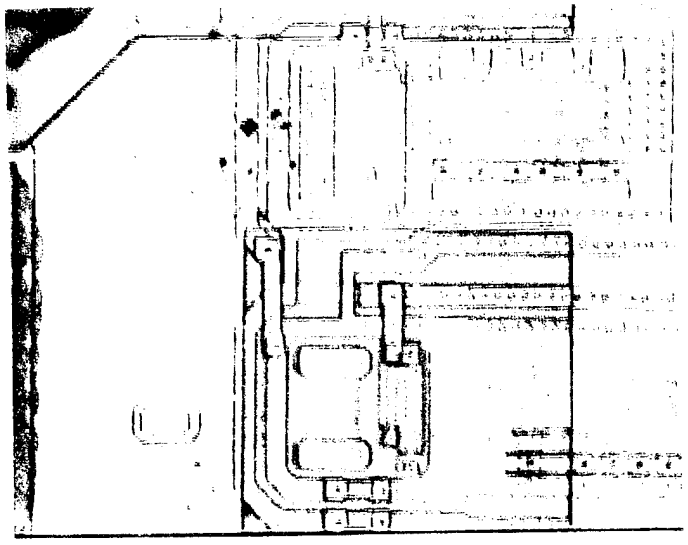
Two "good" die which passed ET after 2000 cycles and six "bad" die which failed ET after 2000 cycles were etched in a dilute KOH bath for 10 minutes. [The 2 "good" dies were molded with X9074 and ULS12H; The 6 "bad" dies were molded with ULS12H] Etch results are shown in **figure 15**. Cracks in the passivation layer, especially near the die corner are usually a sign of stress induced cracking [3]. All devices packaged with ULS12H show signs of stress induced cracking. The cracking occurred almost exclusively near a corner Vss pin. [# 45] The die packaged with compound X9074 did not show any signs of stress induced cracking.

Figure 15

KOH Etch
Passivation Cracks
@ 2000 Temperature Cycles
ULS12H Vss Pin 45



KOH Etch
No Passivation Cracks
@ 2000 Temperature Cycles
X9074 Vss Pin 45



3.6 HLC / 68L PLCC / Preconditioned and Non-Preconditioned samples from (HTS):

Plastic packages molded with ULS12H, ULS12HX (Preconditioned), X9074, and B24 were processed through F/A as shown in **figure 4.** There were zero electrical test failures @ 4125 hours. Note: Non-Preconditioned ULS12HX samples were not included in the HTS portion of the DOE.

Six packages from HTS @ 4125 hours were decapped (2 plasma, 4 jet etch), and then optically inspected; the wire bonds show no obvious signs of degradation. These six packages were sent for ball shear and pull testing. The ball shear and pull strength data are listed in **Table 2**. The ball shear and pull strength data indicate that the bonds have degraded. (*Normal shear ~90 grams, Normal pull ~13 grams*)

Table 2

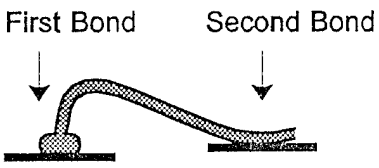
HLC Ball Shear and Wire Pull For HTS @ 4125 Hours

	Unit Type	Average Ball Shear	Sigma	Average Pull Strength	Sigma
ULS12H	Non-Preconditioned	27.59	4.32	2.73	1.29
X9074	Preconditioned	52.72	12.32	4.32	4.21
B24	Non-Preconditioned	31.57	9.53	2.35	1.54
ULS12HX	Preconditioned	33.14	4.68	3.95	3.30
ULS12H	Non-Preconditioned	N/A	N/A	2.74	1.33
ULS12H	Non-Preconditioned*	91.41	8.75	13.57	1.19

*** Zero hours HTS** **Units = grams**

Bond Structure For 68L PLCC / SCX 6244

Note:
During pull testing
first bonds failed first.



Au-ball / Al (Cu,Si)-pad **Au-wedge / Ag plated-Cu lead frame**

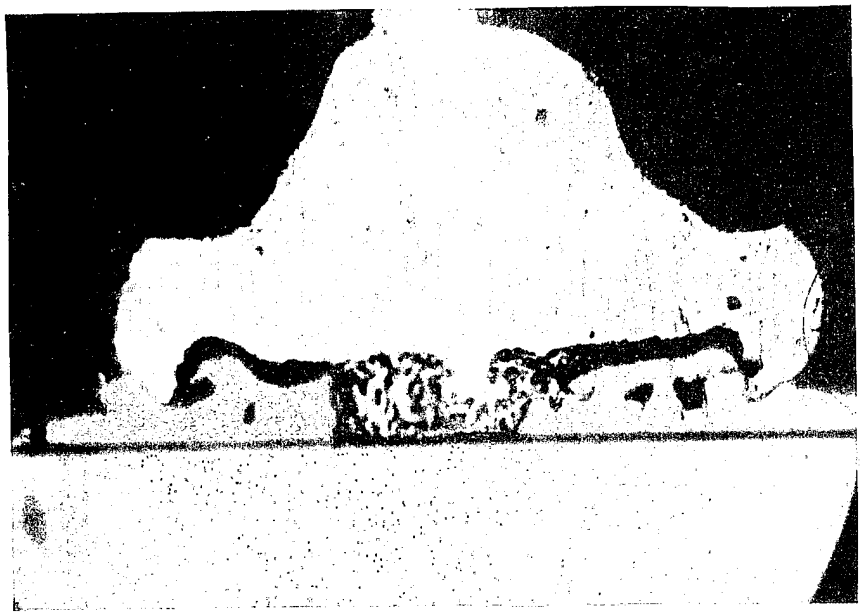
3.6 Continued **HLC / 68L PLCC / Preconditioned and Non-Preconditioned samples from (HTS):**

Figure 16 shows the metallographic cross-sections of two gold wire bonds. Staining techniques delineated several intermetallic phases.

Figure 16



Cross-Section
Through Gold
Ball Bond
unstressed sample
0 Hours HTS 175°C
Non-Preconditioned
ULS12H



Cross-Section
Through Gold
Ball Bond
Intermetallic Growth
4125 Hours HTS 175°C
Non-Preconditioned
ULS12H

3.7 **HLC / 68L PLCC / Preconditioned and Non-Preconditioned / (OPL):**
Plastic packages molded with ULS12H, ULS12HX, X9074, and B24 did not fail ARLT @ 4000 hours. No survey parts were analyzed.

3.8 **HLC / 68L CQJB / Ceramic / (HAST, TC, HTS, OPL):**
Ceramic packages did not fail ARLT-No bond degradation after 4125 hours of HTS.

4.0 Low Lead Count Devices (LLC):

When reading sub-section 4.0 refer to **figure 17**-Master Low Lead Count F/A Chart-for test cell information.

Figure 17

Master LLC Failure Analysis Chart

Package for LM124		130°C HAST	159°C HAST	TC-65°C/150°C	HTS 175°C
5 Volts (Preconditioned)  14L SOIC	3400 3400X B14	1/15 @ 1080 Hrs DLA-06 # 31-45	10/15 @ 648 Hrs DLA-05 # 1-15 5/15 @ 648 Hrs DLA-04 # 1-15 14/15 @ 432 Hrs DLA-06 # 1-15	No Fails	No Fails
30 Volts (Preconditioned)  14L SOIC	3400 3400X B14	5/15 @ 1080 Hrs DLA-05 # 46-60 13/15 @ 324 Hrs DLA-04 # 46-60 12/15 @ 324 Hrs DLA-06 # 46-60	15/15 @ 216 Hrs DLA-05 # 16-30 15/15 @ 216 Hrs DLA-04 # 16-30 9/15 @ 216 Hrs DLA-06 # 16-30		
Preconditioned (5 Volts)  14L DIP	3400 *3400X* B8	9/15 @ 1080 Hrs DLA-01 # 46-60 6/15 @ 1080 Hrs DLA-02 # 46-60 10/15 @ 1080 Hrs DLA-03 # 46-60	13/15 @ 216 Hrs DLA-01 # 16-30 11/15 @ 216 Hrs DLA-02 # 16-30 15/15 @ 216 Hrs DLA-03 # 16-30	Preconditioned No Fails	Preconditioned 3/50 @ 1512 Hrs DLA-01 #111-160 EMC-P1-3400 1/50 @ 1512 Hrs DLA-03 #111-160 EMC-P4-B8
Non- Preconditioned (5 Volts)  14L DIP	3400 3400X B8	1/15 @ 1080 Hrs DLA-01 # 31-45	9/15 @ 648 Hrs DLA-01 # 1-15 8/15 @ 648 Hrs DLA-02 # 1-15 13/15 @ 324 Hrs DLA-03 # 1-15		
5 Volts Control  14L CERDIP		No Fails	No Fails	1/50 @ 1512 Cycles DLA-07 #61-110	No Fails
30 Volts Control  14L CERDIP		1/15 @ 1080 Hrs DLA-07 # 46-60	No Fails		

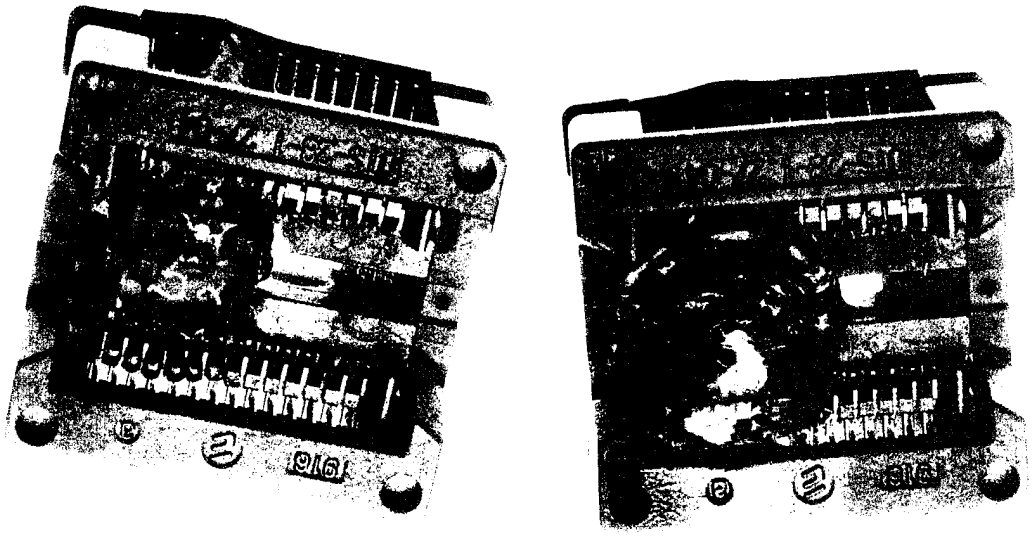
Cum Failures / Total Sample Size @ Cum Hours

4.1 **LLC / 5 Volts / 14L SOIC samples from 130°C HAST:**
One failure @ 1080 hours-package was not sent to F/A.

4.2 **LLC / 30 Volts / 14L SOIC samples from 130°C HAST:**

Plastic packages molded with 3400, 3400X, and B14 were processed through F/A as shown in **figure 4**. Two plastic packages experienced thermal runaway during HAST testing-see **figure 18**.

Figure 18



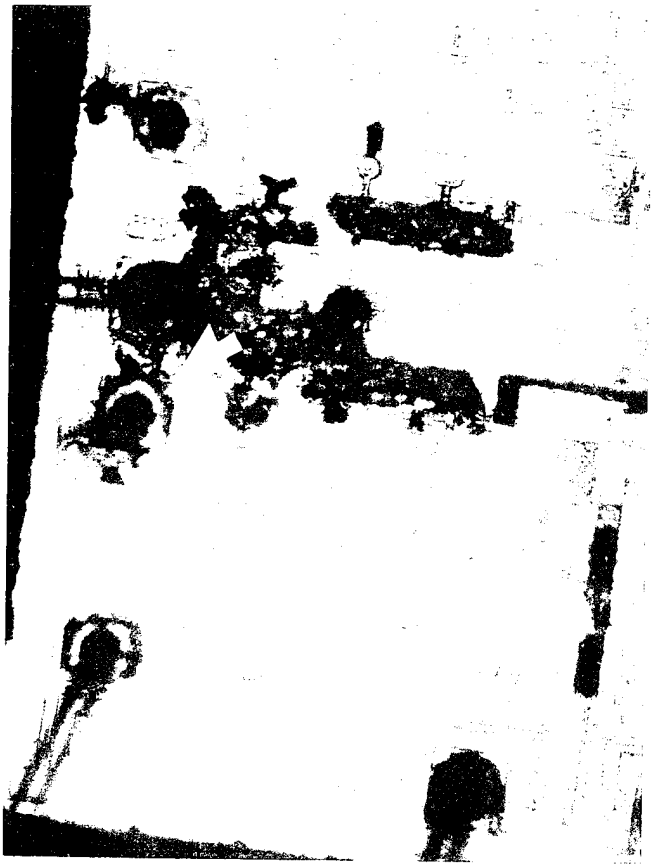
52 # 56

Thermal Runaway Failure @ ARLT
130°C HAST

4.2 Continued LLC / 30 Volts / 14L SOIC samples from 130°C HAST:

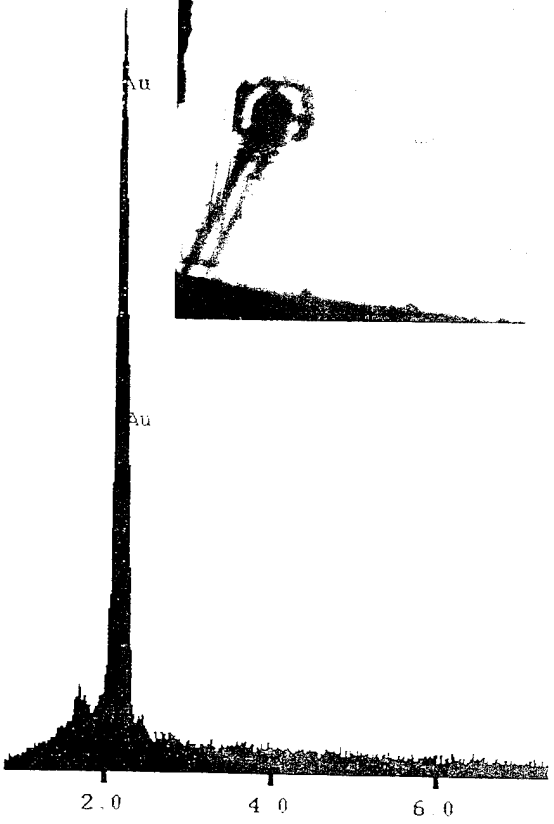
Figure 19 shows the typical surface of a failed device. Optical inspections and SEM/EDS data indicate that there is cracked passivation, broken silicon, and corroded aluminum concentrated near the power pin bond pad. In addition, there is evidence of anodic gold dissolution, stemming from the power pin bond pad. The EDS data is shown in **figure 20**

Figure 19



Corrosion Near The Power Pin
Gold in the Field
HAST 130°C @ 432 hrs.
14 L SOIC DLA-05
3400 30 Volts
46

Figure 20



EDS DATA
Gold in the Field
HAST 130°C @ 432 hrs
14 L SOIC DLA-05
3400 30 Volts
46

4.3 LLC / Preconditioned / 14L DIP samples from 130°C HAST:

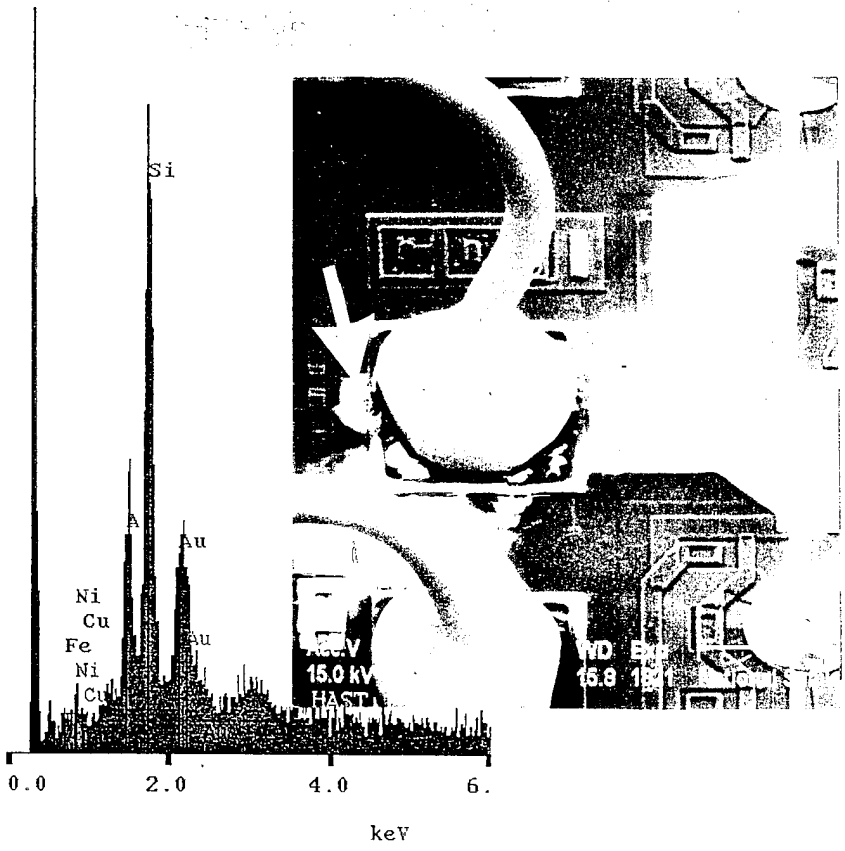
[5 Volts] Plastic packages molded with 3400, 3400X, and B8 were processed through F/A as shown in **figure 4. Figure 21** shows the typical surface of a failed device. Optical inspections and SEM/EDS data indicate that there is cracked passivation, broken silicon, and corroded aluminum concentrated near the power pin bond pad. In addition, there is evidence of anodic gold dissolution, stemming from the power pin bond pad. Note: The EDS spectrum and SEM image are shown in **figure 22**.

Figure 21



Corrosion Near The Power Pin
HAST 130°C @ 324 hrs.
14 L DIP DLA-02
3400X Preconditioned
51

Figure 22



SEM & EDS DATA
Gold in the Field
HAST 130°C @ 324 hrs.
14 L DIP DLA-02
3400X Preconditioned
51

4.4 **LLC / Non-Preconditioned / 14L DIP samples from 130°C HAST:**
One failure @ 1080 hours-package was not sent to F/A.

4.5 **LLC / 5 Volts / 14L SOIC samples from 159°C HAST:**

Plastic packages molded with 3400, 3400X, and B14 compounds were processed through F/A as shown in **figure 4**. Two plastic packages were decapped and inspected. Power pin corrosion was noted on both samples (see **figure 23**). Packages molded with B14 compound failed at 324 hours. Packages molded with 3400 and 3400X compound failed at 648 hours.

Figure 23

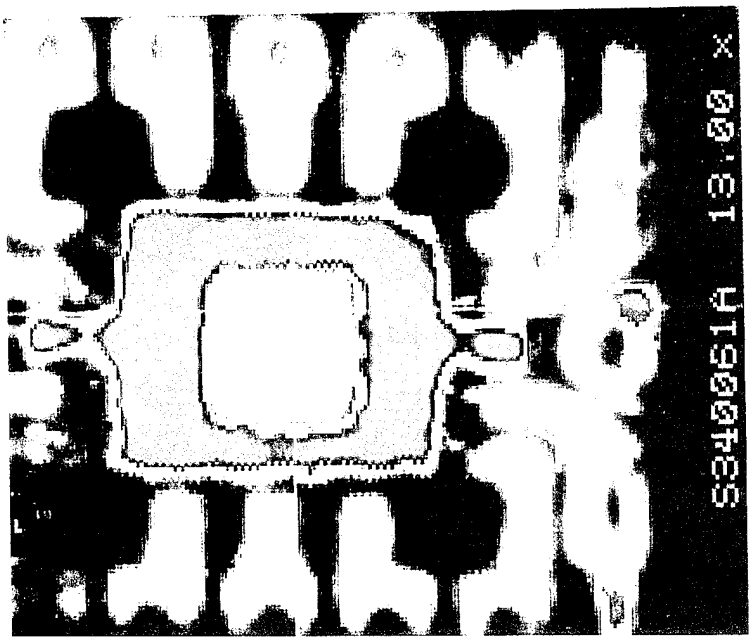


Corrosion
HAST 159°C @ 324 hrs.
14 L SOIC DLA-06
B14 5 Volts
3

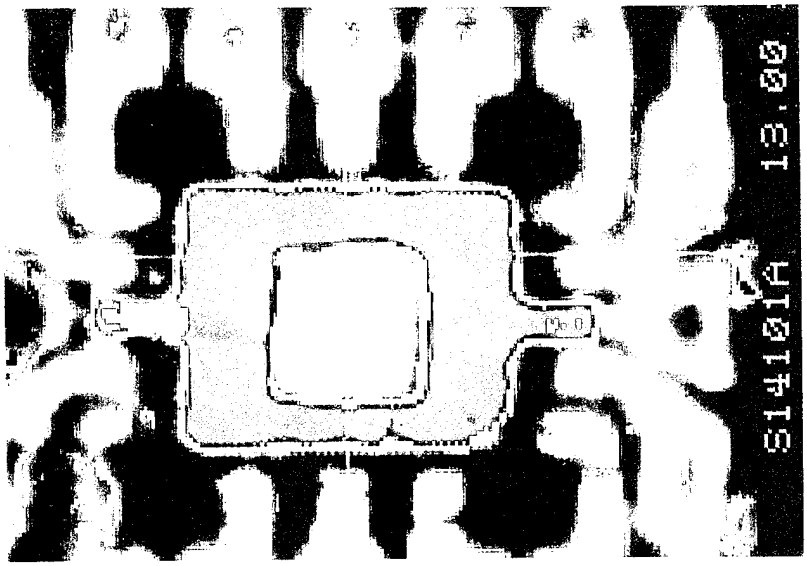
4.6 LLC / 30 Volts / 14L SOIC samples from 159°C HAST:

Plastic packages molded with 3400, 3400X, and B14 compounds were processed through F/A as shown in **figure 4.** CSAM images are shown in **figure 24**. CSAM images of B14 and 3400X mold compounds show signs of paddle delamination after 216 hours of 159°C HAST.

Figure 24



CSAM Image
Delamination
HAST 159°C @ 216 hrs
14 L SOIC DLA-06
B14 30 Volts



CSAM Image
Delamination
HAST 159°C @ 216 hrs
14 L SOIC DLA-04
3400X 30 Volts

4.6 Continued LLC / 30 Volts / 14L SOIC samples from 159°C HAST:

Figure 25 shows the typical surface of a failed device. SEM/EDS data (after oxygen plasma) are shown in **figure 26**. Corrosion was found on several bond pads. The SEM and EDS data are consistent with bond pad / field corrosion. Aluminum, oxygen and silicon can be found on any damaged area.

Figure 25

Corrosion
HAST 159°C @ 216 hrs.
14 L SOIC DLA-05
3400 # 19 30 Volts

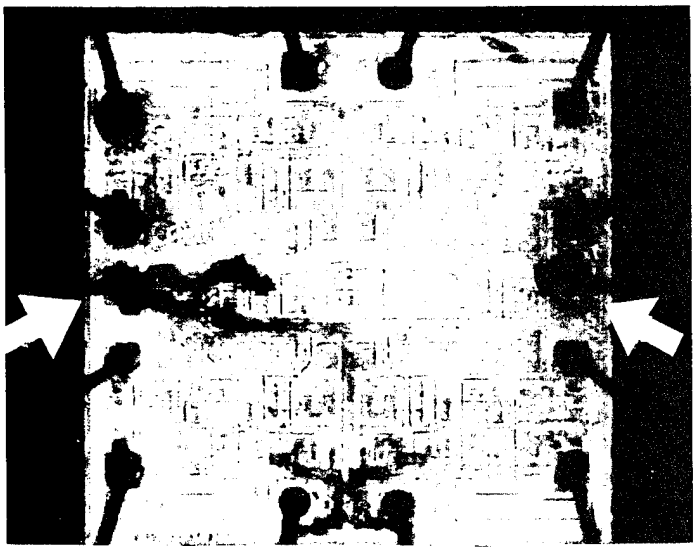
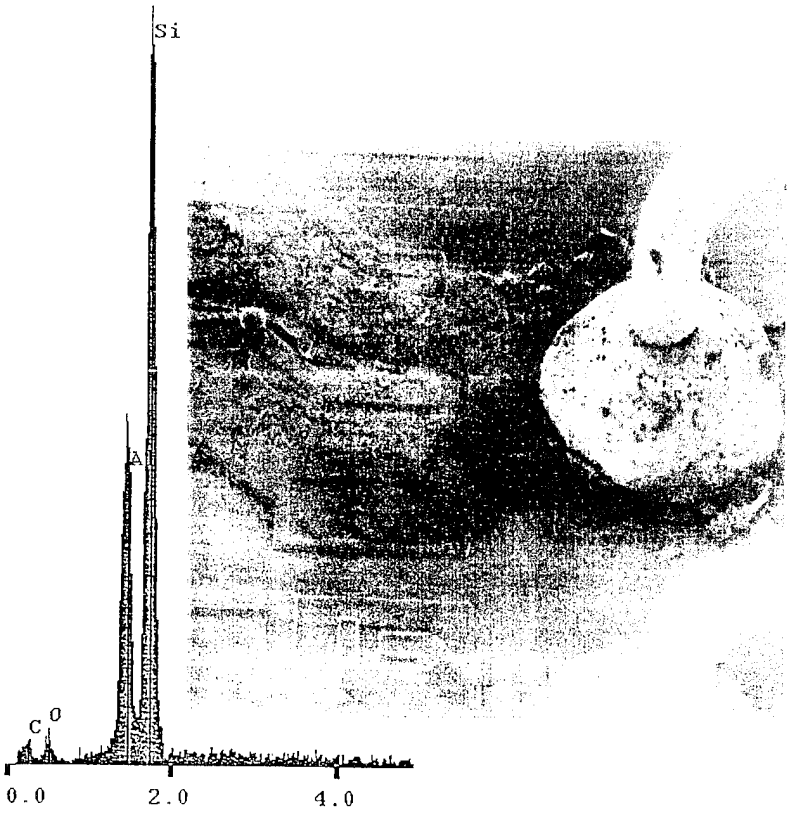


Figure 26

SEM & EDS Data
Corrosion
HAST 159°C @ 216 hrs.
14 L SOIC DLA-05
3400 # 19 30 Volts



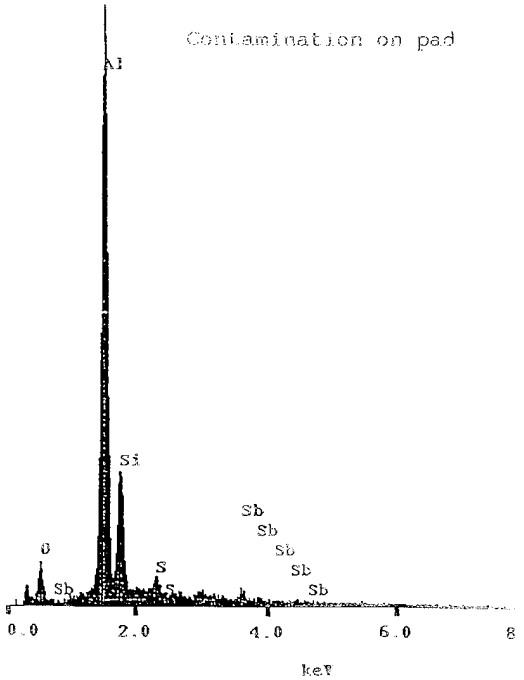
4.6 Continued LLC / 30 Volts / 14L SOIC samples from 159°C HAST:

The EDS data taken from the corroded bond pad shown in **figure 27** is shown below. Trace amounts (>.5%) of antimony were found on the surface of the power pin bond pad. Antimony is a constituent of the flame retardants used in the test mold compounds. See reference [5] for a discussion of flame retardants and corrosion.

Figure 27



Corrosion Near The Power Pin
HAST 159°C @ 216 hrs.
14 L SOIC DLA-04
3400X # 29 30 Volts



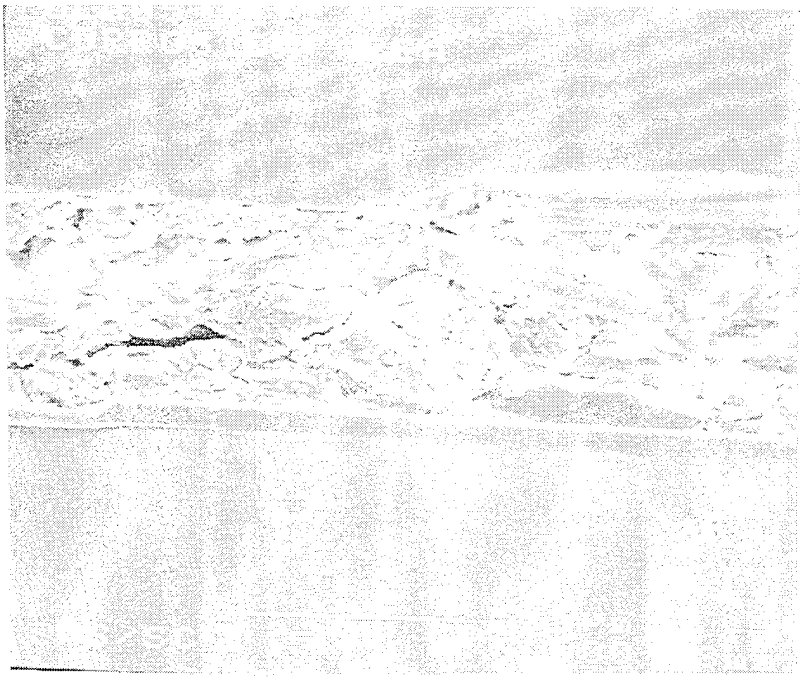
EDS Data
Antimony Peak
HAST 159°C @ 216 hrs.
14 L SOIC DLA-04
3400X # 29 30 Volts

4.6 Continued LLC / 30 Volts / 14L SOIC samples from 159°C HAST:

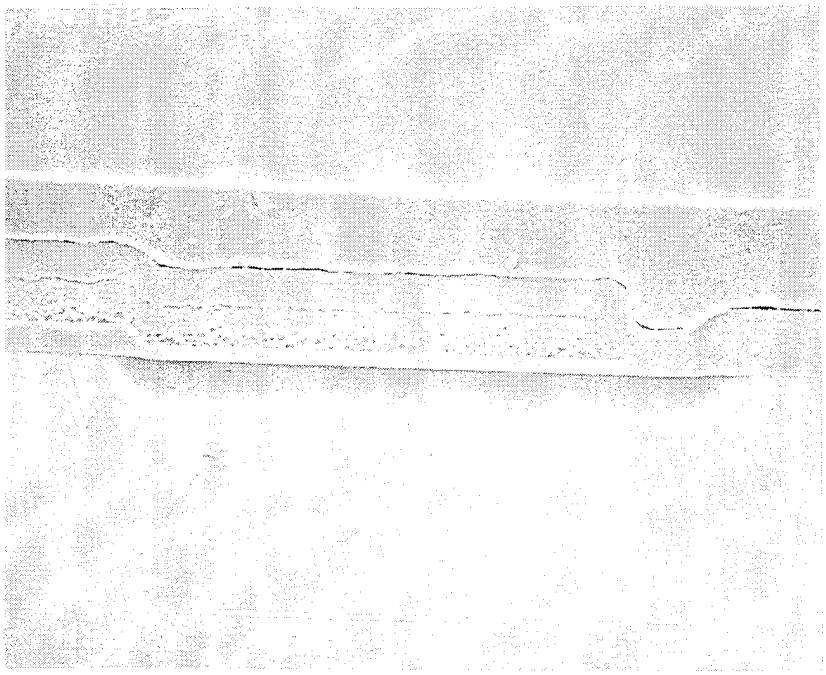
A typical cross-section through a corroded aluminum bond pad is shown in **figure 28**.

Figure 28

Cross-Section
Corroded Pad
HAST 159°C @ 216 hrs.
14 L SOIC DLA-05
3400 # 19 30 Volts



Cross-Section
Non-Corroded Pad
HAST 159°C @ 216 hrs.
14 L SOIC DLA-05
3400 # 19 30 Volts

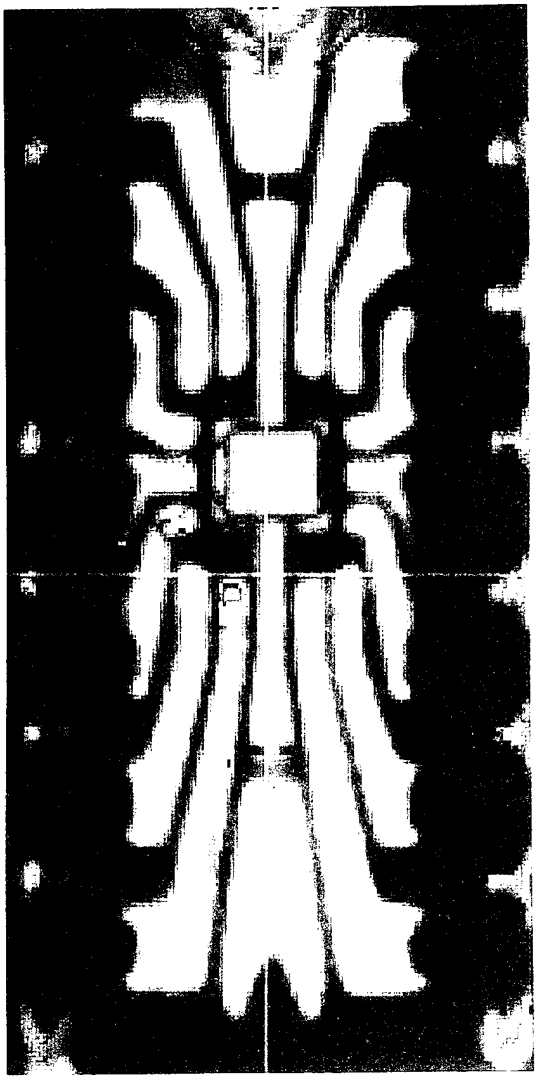


4.7 LLC / Preconditioned / 14L DIP samples from 159°C HAST:

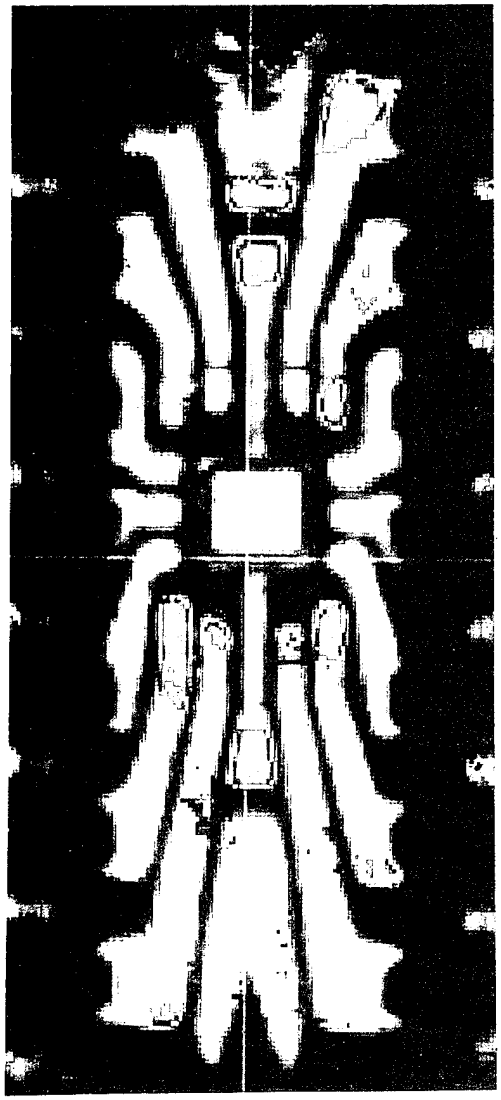
Plastic packages molded with 3400, 3400X, and B8 compounds were processed through F/A as shown in **figure 4.** CSAM images are shown in **figure 29**. CSAM images of B8 and 3400 mold compounds show signs of delamination after 216 hours of 159°C HAST.

Figure 29

CSAM Image
159°C HAST @ 216 hrs.
14L DIP DLA-03
B8 Preconditioned
Note Delamination
Shown in red



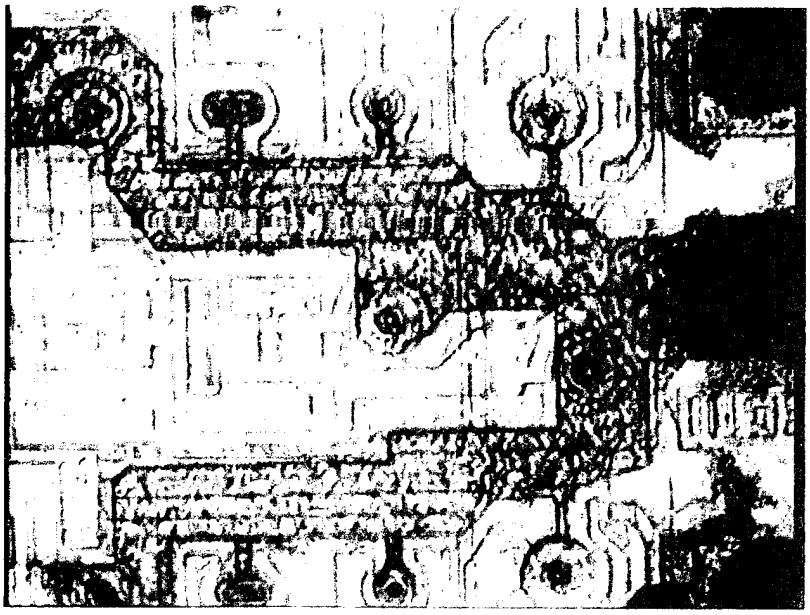
CSAM Image
159°C HAST @ 216 hrs.
14L DIP DLA-01
3400 Preconditioned
Note: Delamination
Shown in red



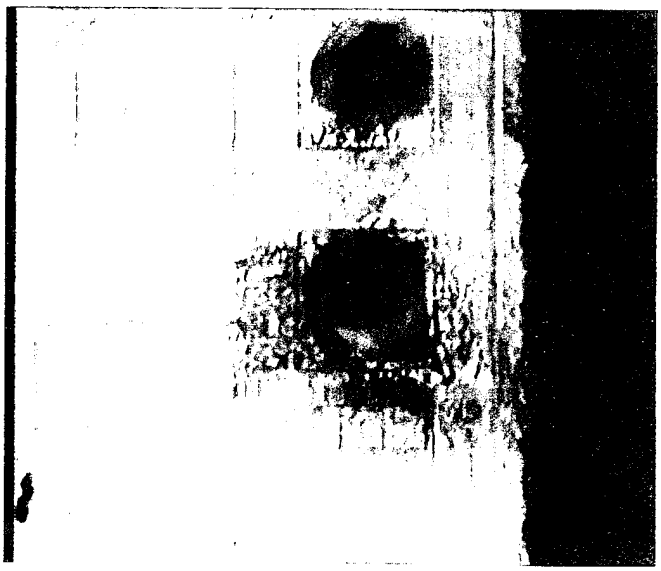
4.7 Continued LLC / Preconditioned / 14L DIP samples from 159°C HAST:

Optical photographs of two failed devices are shown in **figure 30**. Note the extreme surface damage near the power pin and adjacent field area

Figure 30



Corrosion Near The Power Pin
159°C HAST @ 216 hrs.
14L DIP DLA-02
3400X # 17
Preconditioned

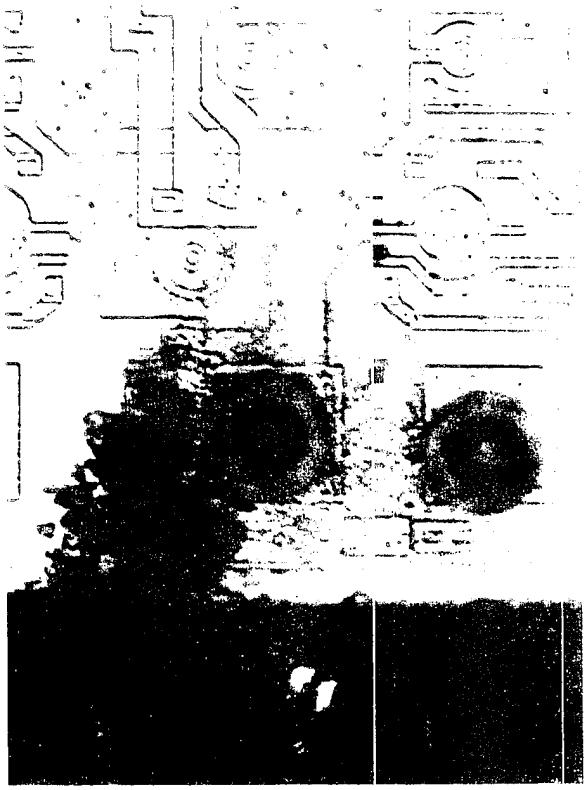


Corrosion Near The Power Pin
159°C HAST @ 216 hrs.
14L DIP DLA-03
B8 #30
Preconditioned

4.8 LLC / Non-Preconditioned / 14L DIP samples from 159°C HAST:

Plastic packages molded with 3400, 3400X, and B8 compounds were processed through F/A as shown in **figure 4.** Two plastic packages were decapped and optically inspected. Both devices show signs of corrosion near the power pin (see **figure 31**).

Figure 31



Corrosion Near The Power Pin
159°C HAST @ 216 hrs.
14L DIP DLA-03
B8 # 11
Non-Preconditioned

4.9 **LLC / 14L SOIC and 14L DIP / (TC):**
No failures at ARLT @ 1512 Cycles-No survey parts were analyzed.

4.10 **LLC / 14L SOIC and 14L DIP / samples from (HTS):**
Only one sample / DLA-03 / 14L DIP @ 1080 hours was sent to F/A. The package was decapped by a non-standard plasma technique which etched and destroyed the surface of the die.

4.11 **LLC / 14L CERDIP / 5 Volts / 130°C & 159°C HAST:**
No failures at ARLT-No survey parts were analyzed.

4.12 **LLC / 14L CERDIP / 30 Volts / samples from 130°C & 159°C HAST:**
One ceramic failure: 130°C HAST @ 648 hours. The sample was not received in time for F/A.

4.13 **LLC / 14L CERDIP / samples from (TC):**

One ceramic failure @ 1080 Cycles: After the lid was removed from the ceramic package, the die was inspected with a high power scope and SEM. The die surface appeared clean and defect free. A photograph showing the field area is shown below (see **figure 32**). Pull tests were used to check the integrity of the wire bonds. The pull strength results are listed in **Table 3.** The values listed are within the aluminum wedge bond specification limits. (Normal values ~5 grams) KOH etch was used to check the integrity of the passivation. The results are shown in **figure 33.**

Table 3

	Pull Strength after 1080 Temperature Cycles	
DLA-07 / CERDIP / # 78	Average = 5.1 grams	Std dev. = .5 grams

Figure 32 14 L CERDIP @ 1080 TC

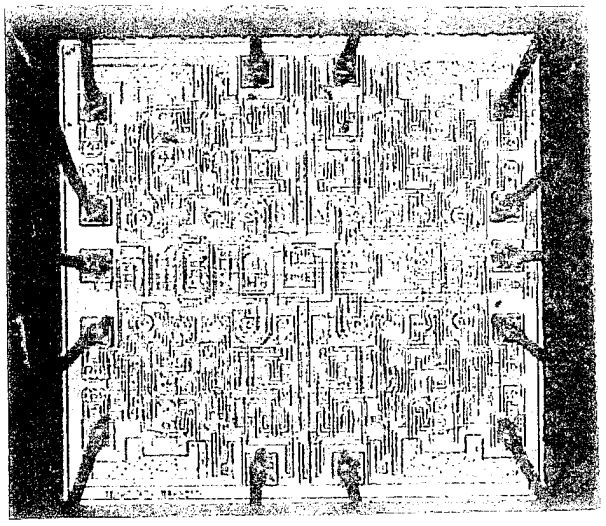
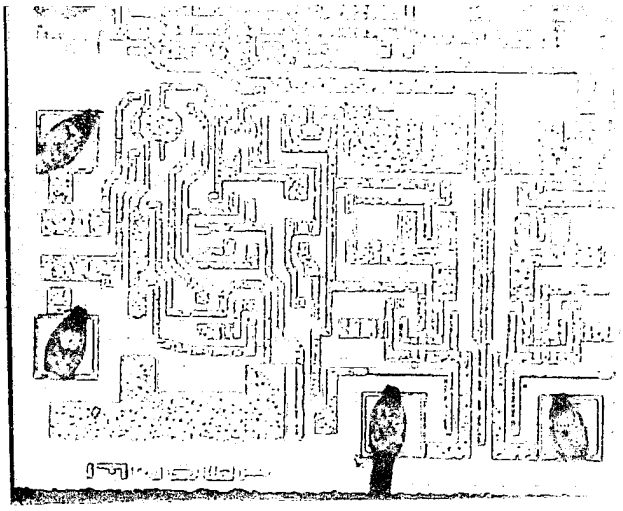


Figure 33 KOH Etch
No passivation damage



4.14 **LLC / 14L CERDIP / (HTS):**
No failures at ARLT @ 1512 hours-No survey parts were analyzed.

5.0 Summary for (HLC and LLC):

5.1 HLC plastic 130°C HAST results: The optical photographs, SEM, and EDS data of failed parts show that preconditioned plastic packages, exhibit aluminum bond pad corrosion after 216 hours of 130°C HAST. (page 7)

5.2 HLC plastic 159°C HAST results: The optical photographs, SEM, and EDS data indicate that preconditioned and non-preconditioned plastic packages exhibit aluminum bond pad corrosion. The exact mechanism which generated corrosion has not been determined. The ball shear data for preconditioned parts shows that bond degradation occurs after 72 hours of 159°C HAST (page 6). SEM images of fractured (lifted) gold wire bonds show evidence of intermetallic growth after 648 hours of 159°C HAST. Both corrosion and gold wire bond degradation can lead to gross ET failure (open circuits). Note: 159°C HAST failures (@ 216 hours) exhibit a greater degree of bond pad corrosion on unbonded pads as compared to 130°C HAST failures (@ 216 hours). (page 7 & 8)

5.3 HLC plastic TC results: KOH etch solution was used to etch the underlying circuit metal to confirm failure of the passivation integrity. The 12 plastic packages which failed TC @ 2000 cycles exhibit passivation stress cracks near a corner Vss pin (#45). All failed devices were from the ULS12H compound. A non-failing ULS12H device was analyzed and similar cracks were found. One non-failing X9074 compound device was also analyzed and did not show evidence of stress cracking. (page 12)

5.4 HLC plastic HTS results: There were no failures from HTS. Ball shear data shows that bonds exhibit degradation during HTS. (page 13) Metallographic cross-sections through gold wire bonds and aluminum bond pads show the presence of intermetallic compounds. A zero hour unit showed the typical thin intermetallic region between the aluminum bond pad and the gold ball bond. A 4125 hour unit showed significantly more intermetallic region, and the presence of at least two intermetallic phases. (page 14)

5.5 LLC plastic 130°C HAST results: The optical photographs, SEM, and EDS data show that the preconditioned failures exhibit gross aluminum bond pad corrosion at the power pin after 216 hours of HAST. This corrosion occurred on 30 Volt SOIC and 5 Volt DIP packages. This corrosion often extended well into the chip circuit area, beneath the chip passivation. 5 Volt DIPs and 30 Volt SOICs exhibit gold dissolution at the power pin. (page 17 and 18)

5.6 LLC plastic 159°C HAST results: The optical photographs, SEM, and EDS data show extensive aluminum bond pad corrosion, near the power pin on all failed parts, similar to the 130°C HAST failures. Corrosion also occurred at other bond pad locations but always most advanced at the power and ground pads. (page 21)

5.7 LLC ceramic TC results: One ceramic failure @ 1080 cycles. Pull strength data shows that the aluminum-to-aluminum wire bonds have not degraded. KOH etching did not reveal cracks in the surface passivation. No physical cause for failure was identified. (page 27)

Number of Samples Used for F/A

Package Type	Total Fails	# Inspected	Other Survey Samples	Totals
HLC 68 Lead	87	38	32	70
LLC 14 Lead	200	45	10	55

Total Plastic and Ceramic Packages

6.0 Recommendations:

Future projects which were beyond the scope of this effort, might include: 1) Sampling corrosion products using ESCA and SIMS thus characterizing various types of corrosion more completely. 2) Derive the various empirical equations representing the relationships between defect type and stress test parameters. 3) Study the root cause of failure on the parametric level.

7.0 F/A Tools / References

7.1 Failure Analysis Tools:

Optical / Stereo Microscopy: Nikon microscopes / Light and Dark field illumination / DIC
CSAM: C-mode / 10 megahertz
SEM: JEOL / .2 Kev-30 Kev / 20X to 400,000X
EDS: Energy Dispersive Spectroscopy: PGT / SEM electrons generate characteristic X-rays / / elemental detection typically .5 % (Boron-Uranium) /
X-Section: Epoxy encapsulation and mechanical cross-sectioning of samples.
Ball shear: SAG 244 Wire pull: MCT22 / destructive and non-destructive /
Pin to Pin probe: Manual electrical probing.
LEM: Hot electron analyzer / Detects the very faint light emitted from high current areas. /

7.2 References:

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The objectives and goal are to investigate contemporary technology and provide a better understanding for the potential use of plastic encapsulated microcircuits (PEM) in military system. In addition to the main thrust of evaluating PEM via accelerated life-testing; mold-compound material studies, sensor development, and fielded system failure analysis comprise a comprehensive program.

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