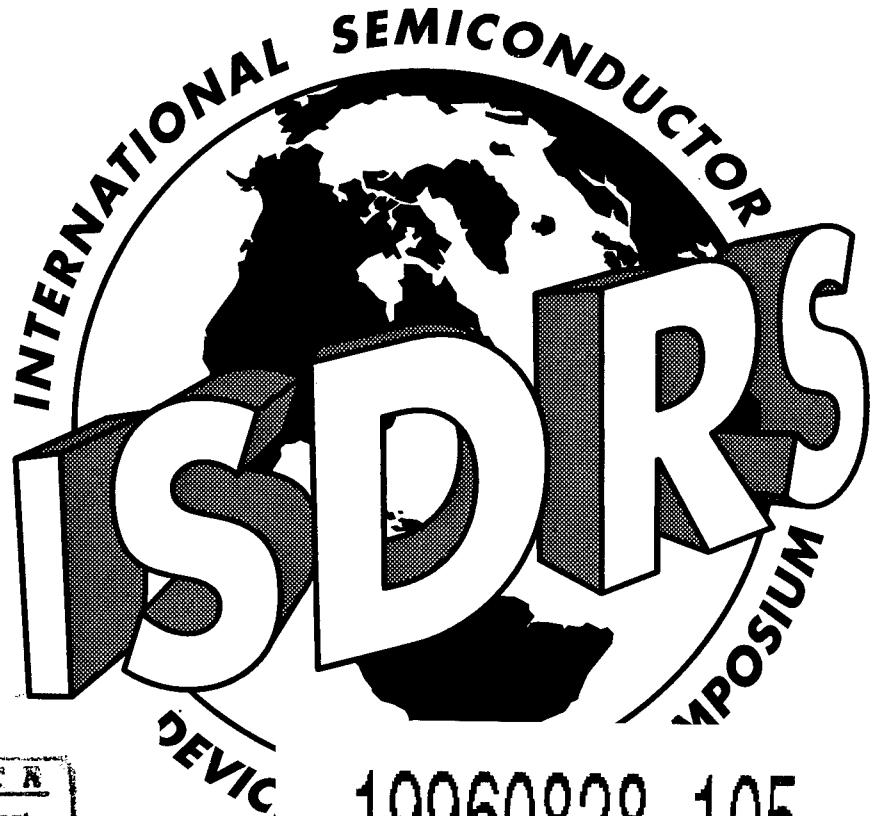
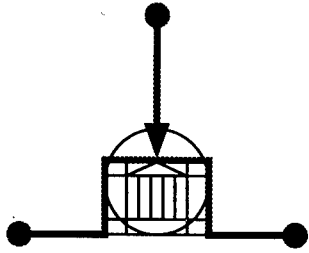


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1995 INTERNATIONAL SEMICONDUCTOR DEVICE RESEARCH SYMPOSIUM

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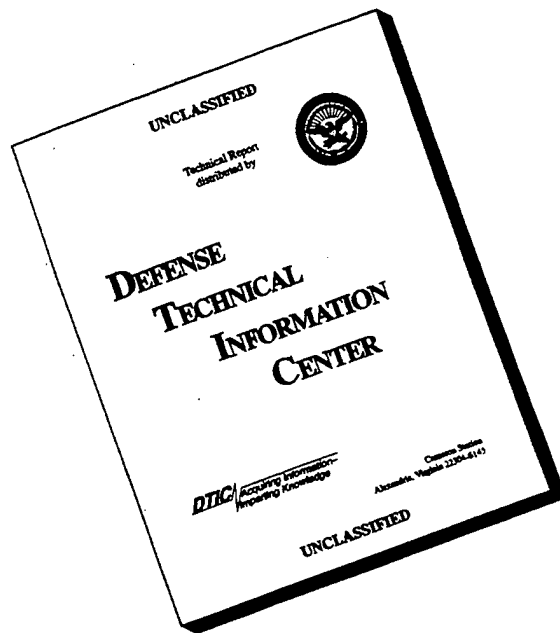
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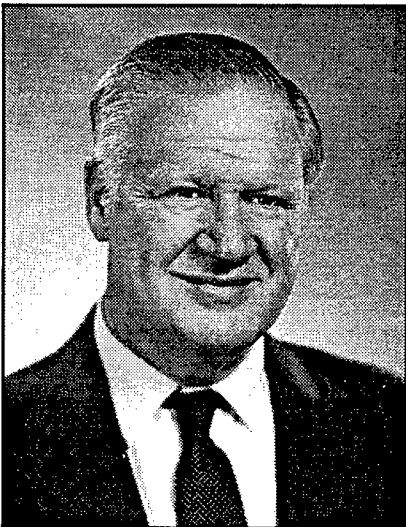
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Professor Aldert van der Ziel

(December 12, 1910 - January 20, 1991)

The van der Ziel Award, sponsored by Westinghouse Electric Company, was established in honor of Professor Aldert van der Ziel for his long, distinguished and illustrious career as an educator and a research scientist.



LESTER F. EASTMAN

Lester F. Eastman was born in Utica, NY, and obtained B.S. (1953), M.S. (1955), and Ph.D. (1957) degrees at Cornell University. He joined the faculty of Electrical Engineering at Cornell in 1957, and also serves as a member of the graduate fields of Applied Physics and Materials Science. Since 1965 he has been doing research on compound semiconductor materials, high speed devices, and circuits, and has been active in organizing workshops and conferences on these subjects elsewhere since 1965 and at Cornell from 1967. In 1977 he joined other Cornell faculty members in obtaining funding and founding the National Research and Resource Facility for Submicron Structures at Cornell (now Cornell Nanofabrication Facility). Also in 1977 he founded the Joint Services Electronics Program and directed it until 1987. He has recently joined with others at Cornell to develop a large effort in high frequency/high speed

optoelectronics. He has supervised over 97 PhD theses, over 50 MS theses, and over 50 post-doctoral studies. In his research group effort is underway on molecular beam epitaxy, microwave transistors, high speed semiconductor lasers, high frequency photo-receivers and fundamental phenomena in compound semiconductor quantum electron and optical devices. During the 1978-1979 year he was on leave at MIT's Lincoln Laboratory, and during the 1985-86 year he was at IBM Watson Research Laboratory. During 1983 he was the IEEE Electron Device Society National Lecturer. He was a member of the U.S. Government Advisory Group on Electron Devices from 1978-1988, and has served as a consultant for several industries. From 1987-1993 he served as a member of the Kuratorium (Visiting Senior Advisory Board) of the Fraunhofer Applied Physics Institute in Freiburg, Germany. He is the Chairman of the Advisory Committee for the Materials Science Research Center of Excellence at Howard University. He is a founder in 1985 and has served as chairman of the board of directors of Northeast Semiconductors, Inc. from 1985-1993. He has been a Fellow of IEEE since 1969, a member of the National Academy of Engineering since 1986, and has been appointed the John L. Given Foundation Chair Professor of Engineering at Cornell in January 1985. In September 1991 he was awarded the GaAs Symposium Award, and the Heinrich Welker medal, for his "contributions to the development of ballistic electron devices, planar doping, buffer layers, and AlInAs/GaInAs/InP heterostructures". He was awarded the Alexander von Humboldt Senior Fellowship in 1994.

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1993	Michael Shur	Elias Towe	Stephen Jones
1991	Robert Mattauch	Michael Shur	Stephen Jones
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1993	William Peatman	—	—
1991	—	—	—

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1993	Edgar Martinez	Wright Laboratory
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1991	R. Mickevičius	Wayne State University

Introduction

This volume contains the Proceedings of the third International Semiconductor Device Research Symposium (ISDRS-95, Charlottesville, Virginia, December 5-8, 1995).

The goal of this international meeting is to provide a congenial forum for the exchange of information and new ideas for researchers from university, industry and government laboratories in the field of semiconductor devices and device physics. Our other goal is to make this conference truly international. To achieve this, the symposium has sub-committees in Asia, Europe, Japan and the former Soviet Union. This conference is organized in cooperation with the IEEE MTT Society, the European Physical Society, the United States National Committee of URSI and the Russian Physical Society.

The program committee received submissions from 22 countries, representing three (3) continents. Of the submitted papers, 150 have been selected for oral presentations and about 75 for poster presentations. These papers cover a broad range of topics, including novel and ultra-small devices, photonics and optoelectronics, heterostructure and cryogenic devices, wide band gap semiconductors, thin film transistors, MEMs, MOSFET technology and devices, carrier transport phenomena, materials and device characterization, simulation and modeling. It is hoped that such a broad range of topics will foster a cross-fertilization of the different fields related to semiconductor materials and devices.

Three special symposia are also included this year: Mid-to-Far Infrared Semiconductor Lasers, Laser Modeling, and MEMs.

The first ISDRS symposium in 1991 was dedicated to the memory of Professor Aldert van der Ziel who made seminal contribution to the theory of semiconductor devices, especially to the theory of noise, and who educated literally hundreds of graduate students. At the second symposium in 1993, ISDRS established a van der Ziel Award sponsored by the Westinghouse Electric Corporation. We are pleased to announce that the 1995 award goes to Lester F. Eastman, Professor of Electrical Engineering, Cornell University.

Every year a Best Student Paper Award is chosen by the Organizing Committee at the close of the symposium from evaluations received from the participants. Two papers won the 1993 Best Student Paper Award. Recipients were Edgar Martinez, Solid State Electronics Directorate, Wright Laboratory, Wright-Patterson Air Force Base, *Factors Determining the Gate Leakage Current in Different Heterostructure Field Effect Transistor Technologies*, and Kaushik Bhaumik, Cornell University, *23 GHz_T Room Temperature SiGe Quantum Well p-MOSFETs*.

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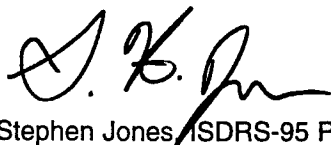
We hope that you find the symposium fruitful and that you will look forward to ISDRS-97.



Elias Towe, ISDRS-95 Symposium Co-Chair



Federico Capasso, ISDRS-95 Symposium Co-Chair



Stephen Jones, ISDRS-95 Program Committee Chair

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United States Military Academy
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Deep Submicron III-V Based Electronics

Loi D. Nguyen

Hughes Research Laboratories
3011 Malibu Canyon Road, Malibu, CA 90265, USA

1. ABSTRACT

Deep submicron III-V based electronics is an enabling technology for many modern microwave and millimeterwave systems such as direct broadcast satellite (DBS), wireless communications, weapons, and future automotive electronics. In this talk, I will review its present status and offer suggestions for future work.

2. INTRODUCTION

Deep submicron III-V based electronics is an indispensable part of the modern society. FETs, HEMTs, and MMICs with gate length between 0.10 and 0.25 μm are being mass produced for a wide range of systems, from a low-cost DBS receiver to the most advanced microwave and millimeterwave systems such as missile seekers, phased-array radar, and satellite communications payloads [1-8]. Today, the largest market for deep submicron devices is DBS. In the near future, their largest markets will most likely be millimeterwave communications and automotive electronics [9-10]. Table 1 lists the frequency bands of operation, technology, and volume requirements of these major systems.

SYSTEM	FREQUENCY BAND (GHz)	TECHNOLOGY	VOLUME
DBS receivers	C, Ku	0.15 μm	High
Radar	X	0.25 μm	Moderate to High
Missile Seekers	Ku, Ka, W	0.1 - 0.25 μm	Moderate
Space-based Communications	L, S, C, Ku, Ka, Q, V	0.10 - 0.25 μm	Low
Ground Stations	L, S, C, Ku, Ka, Q	0.10 - 0.25 μm	High
Wireless Communications	K, Ka, V	0.10 - 0.25 μm	High
Automotive	W	0.10 - 0.25 μm	High

Table 1. Major systems that employ deep submicron III-V electronics.

3. SCALING LAWS

The scaling laws of deep submicron HEMTs is now well understood. For high performance HEMTs, the aspect ratio (i.e., gatlength over gate to channel separation) must be greater than 5. Then it is a matter of proportionally reducing the parasitic capacitances and resistances [11]. Simple procedures for designing deep submicron HEMTs are given in Figs. 1(a) and (b) below.

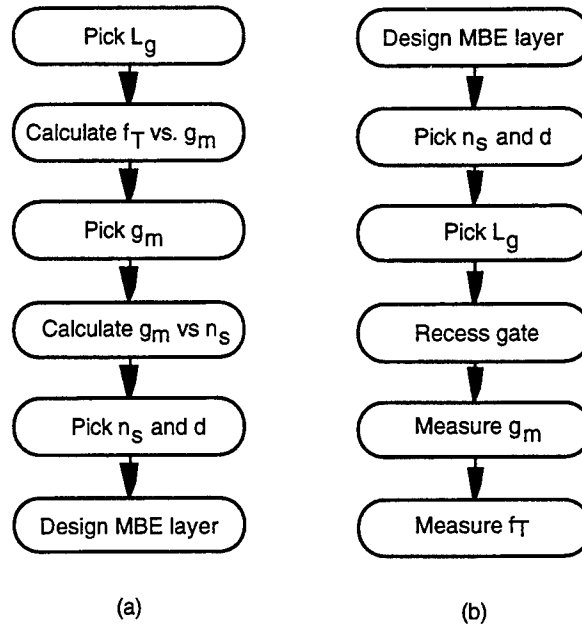


Fig. 1. Designing deep submicron HEMTs: (a) analytical and (b) trial and error.

The above analytical method can be implemented with a simple spreadsheet program [4]. For a given gatlength, the key is to design a HEMT with a sufficiently high transconductance (g_m) to overcome the parasitic effects. Figure 2 illustrates the dependence of f_T on g_m for deep submicron InP HEMTs, which highlights the important role of g_m at the shortest gatlengths. While a 0.25- μm HEMT only needs a g_m of 600 mS/mm, a 0.05- μm device will require a g_m in excess of 1500 mS/mm to overcome its parasitic effects.

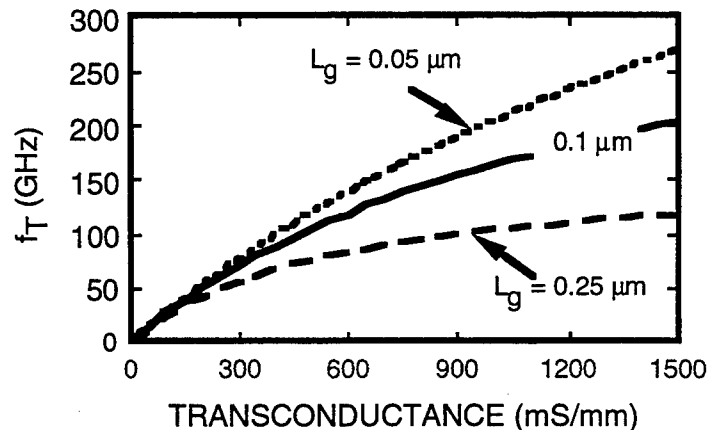


Fig. 2. Dependence of f_T on g_m for deep submicron InP HEMTs.

4. EMERGING TECHNOLOGIES

The push for the next generation of ultrahigh speed HEMTs began in 1989. This time the goal is to develop a 0.05- μm HEMT technology with significantly higher cutoff frequencies ($f_T, f_{\text{max}} > 300$ GHz). This task is rather challenging, considering that at 0.05- μm gatelength, the HEMT's active layer (Schottky, spacer, and effective channel) must be kept under 100- \AA thick to maintain an aspect ratio of 5.

In 1992, the Hughes Research Laboratories reported a successful demonstration of both lattice-matched and pseudomorphic 0.05- μm InP HEMTs with extrinsic f_T over 300 GHz (the best devices exhibited an f_T as high as 340). In 1994, the Nippon Telegraph and Telephone Laboratories (NTT) also achieved comparable results using a dielectric sidewall and non-alloyed ohmic contact process [5]. This approach is very promising and could potentially lead to a manufacturable 0.05- μm HEMT technology. Table 2 summarizes the results from both efforts.

Parameter	Scaled Model	Hughes	NTT	Unit
$C_{\text{gs}} + C_{\text{gd}}$	1.0	0.8	0.7*	pF/mm
g_m	2000	1700	1280	mS/mm
R_s	0.1	0.1	0.1	$\Omega \cdot \text{mm}$
g_{ds}	60	260	n/a	mS/mm
f_T	400	340	300	GHz
f_{max}	800	250	235	GHz

* Estimated from f_T and g_m values

Table 2. Summary of Hughes' and NTT's 0.05- μm InP HEMTs

These 0.05- μm HEMTs, despite their impressive g_m and f_T , are not quite properly scaled. Both suffer from a high rf output conductance, which degrades the f_{max} . In the Hughes' case, the high output conductance was a result of a combination of low aspect ratio (3) and self-aligned gate. Future work must concentrate on the reduction of the rf output conductance and improve the f_{max} , while maintaining a high f_T .

Future 0.05- μm HEMTs could potentially benefit from new material systems or novel bandgap engineering. The AlSb/InAs is an interesting possibility, offering high conduction band offset and mobility. Its present drawback is the premature impact ionization in the narrow-band InAs channel, which may preclude its use as a room-temperature device. The University of California at Santa Barbara (UCSB) is a widely-recognized leader in this area, with extensive research activities ranging from material growth, transport properties, and HEMT fabrication [12]. Another possibility is the InGaAs/InP composite channel pioneered by NTT Laboratories, which exploits the high mobility of InGaAs at low electric fields and the high velocity of InP at high electric fields [13]

5. SUMMARY

Deep submicron III-V based electronics is an enabling technology for many modern microwave and millimeterwave systems such as DBS, wireless communications, weapons, and future automotive electronics. The scaling laws of deep submicron HEMTs is well understood, and have been successfully applied to develop high-performance, production 0.1- μm HEMTs and MMICs. Current research activities in this area are focusing on 0.05- μm HEMT technology as well as new material systems or novel bandgap engineering approaches. These efforts hopefully will produce the next generation of for ultrahigh performance systems such as high-speed optical communications and ultralow-noise cryogenic receivers.

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Optoelectronics with Crystalline Organic Semiconductors

Stephen R. Forrest
Advanced Technology Center for Photonics and Optoelectronic Materials
Department of Electrical Engineering
Princeton University
Princeton, NJ 08544

Abstract

Numerous, exciting advances have been made in recent years which suggest that crystalline organic materials are now becoming practical for use in photonic device applications. Among the most noteworthy findings are:

1. Demonstration of "quasi-epitaxial" film growth, where highly ordered thin films of van der Waals-bonded molecular solids can be achieved using the ultrahigh vacuum process of organic molecular beam deposition (OMBD) largely independent of the need for lattice matching between the film and the substrate. This observation has led to the realization of low defect density heterojunctions consisting of material combinations with widely different crystal structures.
2. Demonstration of organic multiple quantum well structures by OMBD growth which show the effects of quantum confinement of excitons. These extremely interesting structures share properties common to both insulators and semiconductors, suggesting that new and useful physical phenomena are now accessible using such structures.
3. Demonstration of high luminance organic light emitting devices consisting of heterojunctions of two different organic molecular solids. These devices emit with high quantum efficiency in the red, green and blue spectral regions, and have promise for a wide range of display applications.
4. Demonstration of the integration of several different organic optical devices with inorganic semiconductor devices such as Si, GaAs and InP. These include organic/inorganic heterojunction detectors, organic waveguide-coupled detectors, couplers, and modulators. This broad and growing family of devices is based on highly stable, and ordered thin organic films which extend the current range of properties accessible to conventional semiconductor devices.
5. The recent demonstration of an entire new means of growth of organic thin films: organic vapor phase deposition (OVPD). This technique has been used to grow thin films of non-centrosymmetric organic salts with extremely large electro-optic coefficients. Such thin films have not previously been demonstrated, although their potential

usefulness in optical modulators has long been a "holy grail" of organic device technology.

In this talk, I will discuss some of these major advances in the field of organic molecular thin films grown by OVPD and OMBD in recent years. This work will be placed in the context of the larger family of organic thin films with potential use in photonic devices, including polymeric devices and Langmuir-Blodgett thin films. The prospects for the application of molecular organics in practical photonic devices will also be considered.

Blue-Green Semiconductor Lasers

Arto V. Nurmikko and R.L. Gunshor*
Division of Engineering and Department of Physics
Brown University, Providence RI 02912, USA

Abstract

Compact blue and green semiconductor lasers will impact significantly on such technologies as optical storage and displays. There are both fundamental physical and practical material science reasons why wide bandgap semiconductors, both of the II-VI and III-V variety, have been most elusive in light emitting device applications - until recently. Today one can find laboratory demonstrations of continuous wave blue-green ZnSe-based quantum well diode lasers at several research facilities and a GaN-based blue LED is a commercial reality. Much of this rapidly paced progress in short wavelength light sources originates from significant advances reached in material synthesis by advanced epitaxies, together with insight and exploitation of semiconductor physics in nanoscale optoelectronic device designs.

In this presentation we review key features of the blue-green diode lasers which are based on II-VI semiconductor heterostructure configurations. The design and performance of a cw laser is discussed in terms of key issues such as the impact of a quantum well layer ($<100 \text{ \AA}$) on the physics of optical gain and the use of 'bandstructure engineering' concepts to implement a low resistance electrical contacting scheme. In spite of the high degree of average crystalline perfection, specific forms of crystalline defects are seen as a major source of present device degradation and impediment to longevity, however, significant progress in this area is being made. Current research is also focusing on blue-green vertical cavity lasers where photonic nanostructures can be designed to enhance the interaction between the electronic states in the quantum wells (excitons) and the optical field. Recent work has led to the demonstration of exceptionally large coherent coupling effects in such microcavity configurations while providing a demonstration for a vertical cavity laser at room temperature.

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*School of Electrical Engineering, Purdue University, West Lafayette IN 47907

TRENDS IN ULSI SEMICONDUCTOR CHARACTERIZATION

T. J. Shaffner

Texas Instruments, Incorporated
Dallas, TX 75265

INTRODUCTION

Material and device characterization serves the essential role of defining how a manufactured integrated circuit differs from its intended design and functionality. Over the years, a variety of techniques based on probes of electrons, ions and X-rays have evolved to fill this need. Each has a specialized application for resolving specific manufacturing problems related to smaller geometry, material impurities and silicon crystal defects.

The acclaimed Semiconductor Industry Association (SIA) road map affirms the customary semilogarithmic projection of gate length reduction with each new DRAM technology node (1). Downsizing is the most frequently cited driving force for smaller analytical probes, but it is evident from Figure 1 that similar trends with contamination, metal impurities and point defects are expected to be forces of equal, if not greater magnitude in the near future. Others agree, citing that microcontamination and particle control tools will drive the infrastructure of our industry (2,3). In this review, we illustrate how key characterization techniques are evolving in response to demands for smaller geometry and reduced levels of contamination and defects. The reader is also referred to a sampling of fine books and articles covering semiconductor characterization (4-6).

SHRINKING GEOMETRY

During the past two decades, the scanning electron microscope (SEM) displaced optical microscopy as the tool of choice for critical dimension measurements and circuit failure diagnostics. However, we know today that even the SEM is unable to provide quantification of linewidths near 0.5 μm , when 10% or better tolerance is routinely required. As with optical microscopy, the procedure relies on techniques of matching an ideal step function to a fuzzy intensity profile across the edge. The ambiguity originates from the diffraction limit in optical microscopy, and electron scattering in the SEM, and only marginal improvements with these appear likely in the near future. A similar difficulty in defining dimensions of ultra-shallow junctions less than 100 nm deep is also receiving increased attention (7).

Scanning probe microscope (SPM) techniques are being extensively tested for metrology applications, but offer different challenges for achieving robust piezo-manipulators with reproducible linearity, and for deconvolving the effects of shape and atomic scale protrusions on each individual tip (8,9). We can anticipate rapid advances in probe methodologies, but today engineers still rely on transmission electron microscopy (TEM) as the absolute reference for nanometer quantifications.

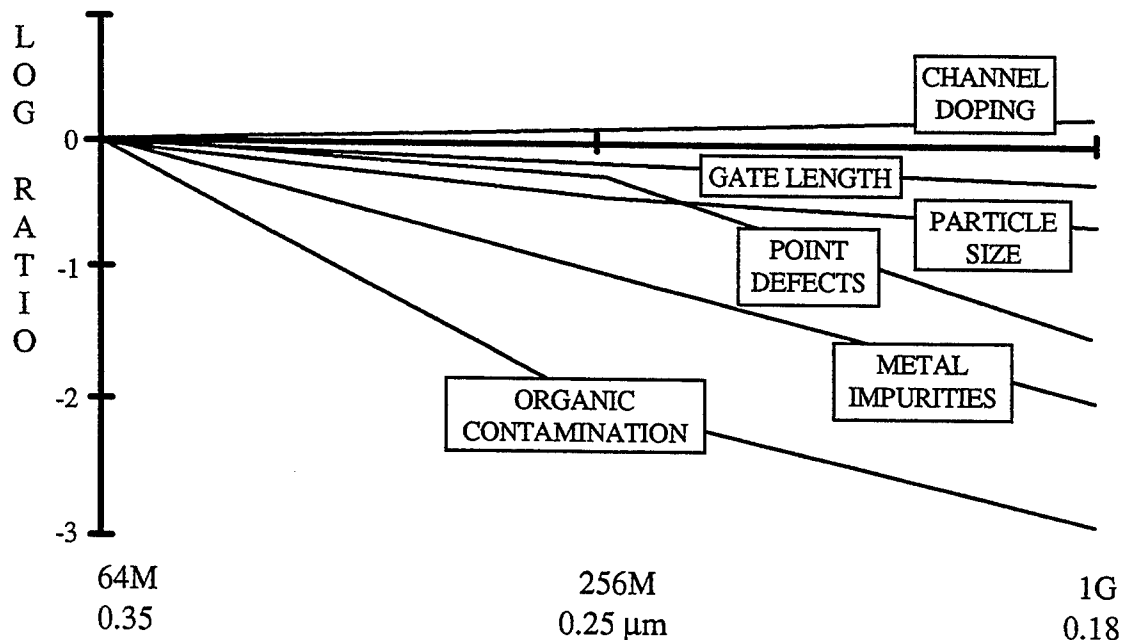


Figure 1. The SIA road map for high density DRAMs defines challenges for materials and device characterization. The vertical axis is the ratio of each metric (identified by a box) relative to today's performance. Downward slopes denote reduction in the metric as a function of technology node (1).

The difficulty in preparing samples for TEM is well known, particularly for dense integrated circuits where a specific site failure has occurred. It was believed for years that preparing a thinned section through a single faulty bit in a megabit DRAM was impractical, if not impossible to achieve. Early progress with this problem was reported in 1989 by Benedict et al. (10), who developed an ingenious tripod tool that permits precise control of repetitive polishing and inspection. More recently, focused ion beam (FIB) columns have been developed capable of carving precise free standing films as thin as 100 nm at any orientation and position within the volume of an integrated circuit.

IMPURITIES AND DEFECTS

Although electron microscopes provide insight into nanostructural problems, they remain unable to identify chemical species at the single atom level. Scanning probe techniques are at the threshold of achieving this, but current demonstrations based on single molecule imaging (11), photoluminescence (12), and Raman spectroscopies need to mature considerably before routine applications are possible. Today, secondary ion mass spectrometry (SIMS) still offers the best compromise between small spot analysis and elemental sensitivity for broad semiconductor applications.

Modern magnetic sector and quadrupole SIMS instruments achieve 0.8 μm spatial resolution with sub-parts-per-million-atomic (*ppma*) sensitivity for most elements. Sputter liberated molecular species which have a similar charge-to-mass ratio, like ^{30}SiH and ^{31}P , or ^{56}Fe and $^{28}\text{Si}_2$, can be resolved in a high mass resolution mode, but only with significant

sacrifice in sensitivity. New techniques are evolving to address this molecule interference problem, including accelerator mass spectrometry (AMS), laser assisted SIMS, and time-of-flight SIMS.

Thin film compositional analysis without standards is a recognized strength of Rutherford backscattering, but perhaps less appreciated, is the exceptional sensitivity to monolayer impurities and surface defects (13). For elements from *Cl* to *Pb* on *Si*, a monolayer or less results in a peak with excellent signal-to-noise that is isolated from matrix backscattering. Typically, a *He* projectile is applied at 2-3 MeV, but further improvement in cross section and elemental sensitivity is possible using a heavier ion accelerated at lower energy. This is incentive for the heavy ion backscattering spectroscopy technique (HIBS) which is under development primarily at Sandia National Laboratory (14), who use 400 keV ^{12}C for a 1,000X enhancement. Others are using 200 keV *He* to improve depth resolution (~1 nm) in quantitative profiles of ultra-thin oxynitride capacitor dielectric films. These techniques promise to extend applicability to impurities and stoichiometry of ultra-thin films beyond capabilities presently realized by total reflection X-ray fluorescence (TXRF) instruments, which are in common use in most wafer fabs today.

Microdefects in present-day silicon are sparsely distributed and extremely small, typically being several to hundreds of nanometers across. It is difficult to even locate these by conventional microprobe techniques, and weak signals from such small points add to the analysis dilemma. Methods of X-ray diffraction and topography circumvent these problems, because they sense minute strain fields that extend far beyond the defect center, and also simultaneously detect hundreds or thousands that are distributed throughout a large sampling volume. Techniques in common use in the semiconductor industry include Berg-Barrett, double and triple crystal topographies, and low angle X-ray reflectometry.

PERSPECTIVE

The Semiconductor Industry Association road map stresses the importance of point defects, metal impurities and organic contamination in future manufacturing. This is not to diminish the significance of single particles, but if in fact manufacturing needs evolve as outlined in Figure 1, characterization specialists need to commit equal if not more resources to the development and application of such characterization tools. The Sematech consortium centered in Austin, Texas has responded to the challenge with an analytical equipment road map that defines how resources might be best allocated in addressing the buildup of such an infrastructure (15).

Road maps exemplify our *evolutionary* approach to characterization tools, because it is difficult to forecast with any accuracy which new science and techniques will surprise us in the near future. As much as we would like to deliberately invent new ways to achieve ULSI characterization goals, they are more likely to spring from the combination or revitalization of older technologies, sometimes in unrelated fields. This random appearance of new techniques is why cutting edge characterization organizations seek to function as a collection center for new ideas, inventions and measurement science and technology. The

buildup of such infrastructure, and the merging of disciplines provides fertile ground for this *revolutionary* aspect of technique advancement.

One typically predicts where we will be five or ten years from now, based on extrapolation of known technology and historic trends. We might only guess which evolutionary and revolutionary changes to expect, but it is known that characterization technology provides a technical foundation for the fabrication tools of tomorrow. In our daily activities, we must continue to weigh the strengths and weaknesses of characterization techniques not only for the problem at hand, but also with an eye toward the future engineering and scientific foundations of the semiconductor industry.

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Student paper

Effects of Gate Doping Species, Concentration and Microstructure on the Electrical and Reliability Characteristics of Ultrathin Oxides and N₂O-oxynitrides

Kafai Lai, Anthony Chou, Kiran Kumar, Mark Gardner*, Jim Fulford*, Jack C. Lee
Microelectronic Research Center, Rm 2.604C, The University of Texas at Austin,
Austin TX 78712

*Advanced Micro Devices, 5204 East Ben White Blvd., Austin TX 78741
(512) 471-1627

Dual-gate CMOS process has attracted a great deal of attention because of the improved device characteristics from surface channel PMOSFETs and independent optimization of NMOS and PMOS FETs. Various implant species such as P, As, B and BF₂ have been used for gate doping. However, the use of boron for P+ doped gate introduces a boron penetration problem [1] and the corresponding oxide degradation. The use of amorphous gate [2] or oxynitrides [3] has been shown to reduce boron penetration. For phosphorus-doped gate of NMOS device, it was reported that a reduced gate doping concentration will significantly improve the stress-induced leakage current (SILC) [4]. These results indicate that the gate plays an important role on MOS characteristics. However, detailed understanding of the effects of various process parameters, which is important for process optimization, has not been fully developed. Therefore, the purpose of this study is to investigate in detail how gate dopant species, doping concentration, and gate microstructure affect the electrical and reliability characteristics of both N- and P-MOS structures with ultrathin oxides and N₂O oxynitrides (62Å).

MOS capacitors with ~62Å O₂-thermal oxides and N₂O-oxynitrides were fabricated on p-type (100) substrates. The gate material deposited was either polysilicon or amorphous silicon, which was then implanted with either P, As or BF₂ with doses of 3x10¹⁴cm⁻², 9x10¹⁴cm⁻², 3x10¹⁵cm⁻², or 3x10¹⁶cm⁻². All wafers were then patterned, rapid thermal annealed (RTA) at 1000°C for 30s for dopant activation and then annealed in forming gas.

The poly depletion effect was studied by measuring the ratio of inversion capacitance to oxide capacitance for As and P samples, and accumulation capacitance to oxide capacitance for BF₂ samples [5]. For the cases of As and P, poly depletion is serious for gate doping less than 10²⁰cm⁻³ (Fig. 1). However, for the BF₂ samples, poly depletion is still less than 5% at 3x10¹⁹cm⁻³ for the as-deposited amorphous case. Unlike As and P, which tend to segregate into grain boundaries, boron segregates into the grain and therefore leads to higher dopant activation and less gate depletion effect. Furthermore, since the recrystallized amorphous gate has larger final grain size, it shows better dopant activation than poly gate, and thus, less poly depletion effect.

Boron penetration was studied by monitoring flat band voltage V_{fb} (Fig. 2) and with SIMS data. For concentration less than 3x10¹⁹cm⁻³, there is a sharp decrease in V_{fb} which indicates that the amount of boron penetrating to the Si substrate is low. This is supported by the SIMS data (Fig. 3). The N₂O oxynitrides show less V_{fb} shift because the nitrogen incorporated in the Si/SiO₂ interface effectively blocks boron penetration (Fig. 4). Amorphous gate is more effective than poly gate in retarding B diffusion within the gate, thus shows less boron penetration (Fig. 4).

Charge-to-breakdown (Q_{bd}) value is obtained by applying constant current stress at both positive and negative polarities. For both As and P samples, there is no dependence

on doping level up to 10^{20}cm^{-3} for the gate injection case (-Jstress), but Q_{bd} increases dramatically for concentration exceeding 10^{21}cm^{-3} for the substrate injection (Fig.5.) It is believed that this is due to some stress reduction effect on oxide resulting from the dopant pileup at the poly/oxide interface for polysilicon heavily doped with As and P [6], while in the gate injection case, Q_{bd} is limited by the high impurity incorporation at the oxide/gate interface instead. Note that N_2O samples exhibit higher Q_{bd} in both polarities. For BF_2 samples, gate injection shows a dramatic two orders of magnitude decrease in the 50% Q_{bd} value when gate doping exceeds $3 \times 10^{19}\text{cm}^{-3}$, indicating a high concentration of B near the poly/oxide interface (Fig. 6). However, for the substrate injection Q_{bd} does not change much with gate doping, indicating that B concentration near the oxide/substrate interface is not limiting the Q_{bd} value (Fig. 7). Also, N_2O oxides show the greatest improvement in the substrate injection case in comparison to the gate injection case since the nitrogen pileup is primarily at the silicon interface (Fig. 6, 7).

The SILC is defined as the increase of the leakage current at 6MV/cm after the device is stressed (either +Vg or -Vg). Contrary to ref. [4], it was found that for both As (Fig. 8) and P samples (Fig. 9, 10), SILC is quite insensitive to gate doping for both stress polarities. It is because As and P do not segregate much into oxide and thus do not affect oxide quality. The effect of dopant enhanced grain growth, as seen in Q_{bd} measurement, was not observed in SILC. For BF_2 samples, the SILC decreases significantly for gate doping below 10^{20}cm^{-3} for negative stress (Fig. 11), correlating with the reduction in boron penetration for low doping. For positive stress, SILC does not show much doping concentration dependence (Fig. 12). This can also be explained by the fact that the boron level is lower in the substrate interface and is not a limiting factor for trap generation by positive stress. For all cases, the N_2O samples show at least an order of magnitude decrease in SILC (Fig. 8-12) because of the reduced trap generation in oxynitrides.

In conclusion, MOS characteristics such as V_{fb} and poly depletion as well as oxide integrity (Q_{bd} and SILC) are strongly affected by gate processing. Optimization for BF_2 samples is quite different from As and P samples. For BF_2 samples, a gate doping concentration of about $3 \times 10^{19}\text{cm}^{-3}$ and the use of amorphous gate and N_2O oxides appear to be an optimum point as a tradeoff between boron penetration and poly depletion (Fig. 13). For As and P samples, oxide quality does not degrade for higher dopant concentration and ΔV_{fb} is insignificant. Thus a degenerate gate doping is preferred to eliminate poly depletion (Fig. 14). Finally, N_2O oxynitrides show better oxide integrity and also more effective boron retardation, and thus are desirable for ultrathin oxide applications. [This work is partially supported by SRC/Sematech through contract # 93-MC-505]

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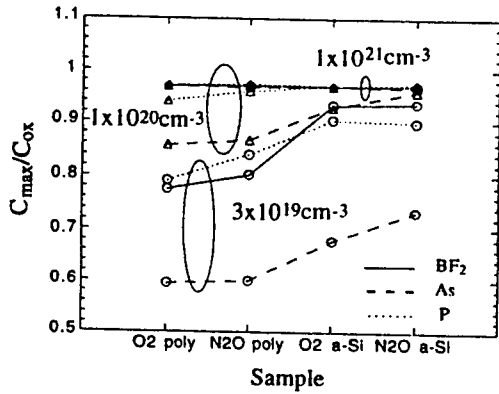


Fig. 1 Poly depletion effects for samples with gate doses from $3 \times 10^{19} \text{cm}^{-3}$ to 10^{21}cm^{-3} . C_{max} represents C_{acc} for BF_2 samples and C_{inv} for As and P samples.

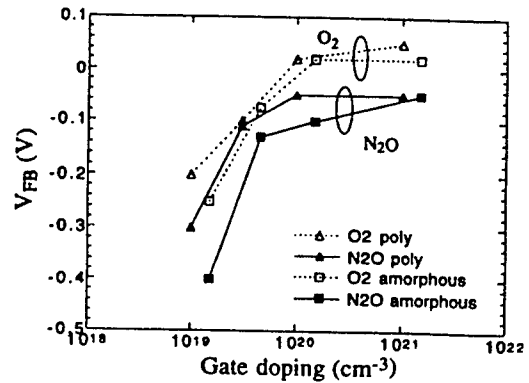


Fig. 2 Flatband voltage of BF_2 samples with different gate doping concentrations.

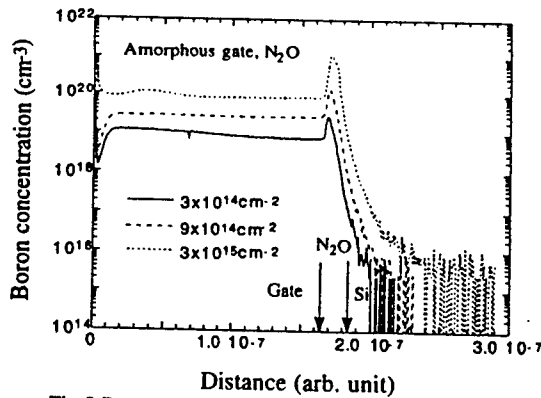


Fig. 3 Boron profiles of BF_2 samples with different gate dosages. The samples are fabricated with amorphous gate and N_2O oxides.

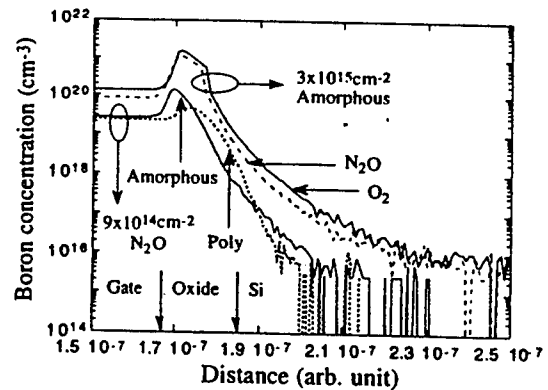


Fig. 4 Boron profiles of BF_2 samples showing the comparison between N_2O and O_2 oxides, and between amorphous gate and polysilicon gate.

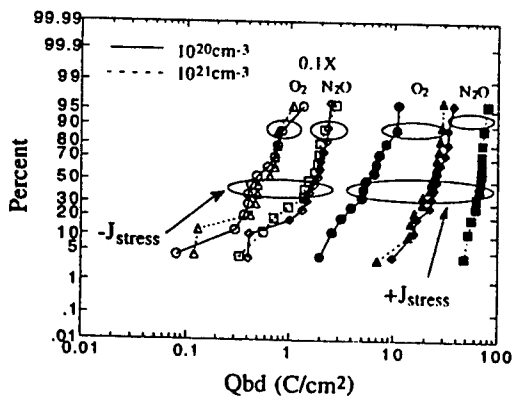


Fig. 5 Q_{bd} distributions of As samples with amorphous gate under both stress current polarities.

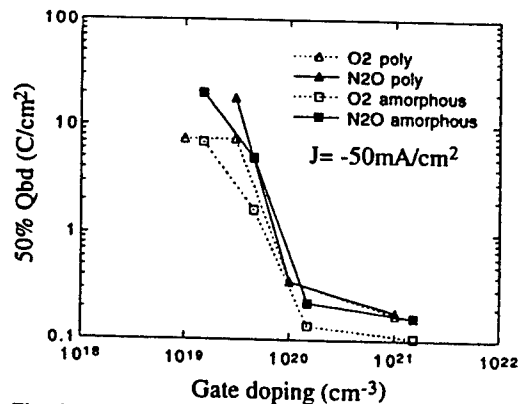


Fig. 6 The dependence of the 50% Q_{bd} value on BF_2 gate doping level under gate injection.

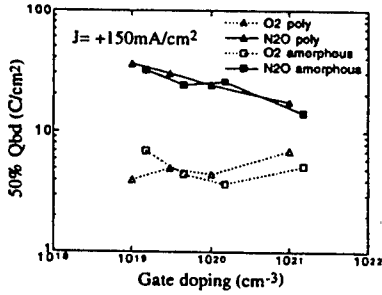


Fig. 7 The dependence of the 50% Qbd value on the BF₂ gate doping level under substrate injection.

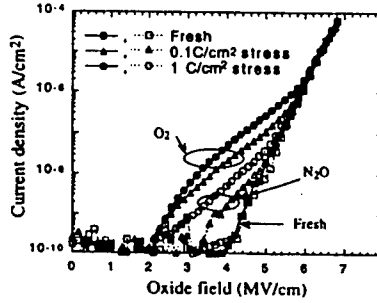


Fig. 8 Typical IV characteristics of As samples after different stress fluences of constant current stress.

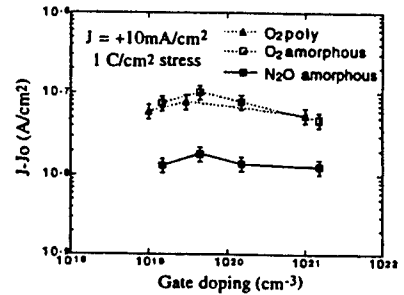


Fig. 9 Dependence of SILC at -6MV/cm on P gate doping level under substrate injection

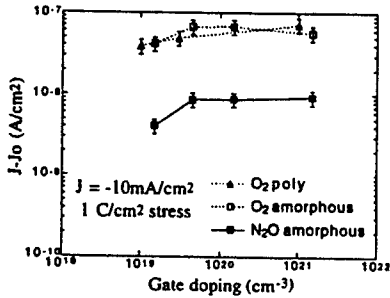


Fig. 10 SILC at +6MV/cm versus P gate doping level under gate injection.

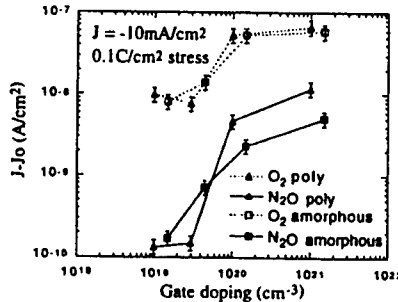


Fig. 11 SILC at +6MV/cm versus BF₂ gate doping level under gate injection.

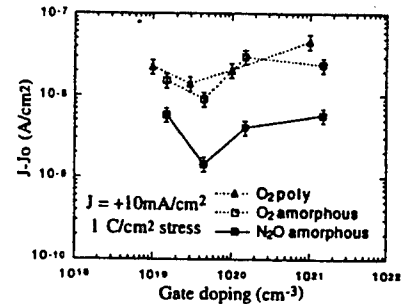


Fig. 12 SILC at -6MV/cm versus BF₂ gate doping level under substrate injection.

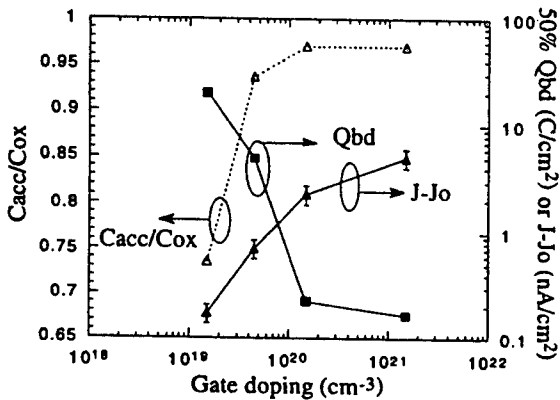


Fig. 13 Optimization of gate doping in terms of poly depletion, Qbd, and SILC for BF₂ samples.

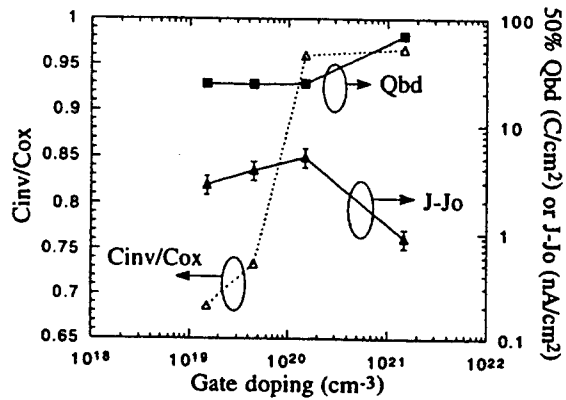


Fig. 14 Optimization of gate doping in terms of poly depletion, Qbd, and SILC for As samples.

Device Characterization with Focused Ion Beams

John F. Walker
FEI Europe Ltd. Cambridge, UK

Focused ion beam (FIB) systems have been used for some time by the microcircuit engineering community for prototype modification and process analysis. However FIB workstations now have the capabilities to take on much wider roles, many of which are relevant to device characterisation and which are discussed herewith. One of the most pertinent features of recent FIB workstations is the sub 10nm spot size routinely achievable, whereas 3 years ago 50nm was state of the art. Even at the highest milling currents, sub-micron spot sizes are expected.

FIB can be used to rapidly and efficiently give a detailed image of the structure of a device. Conventionally, FIB has been used to view the multi-layer metallization and insulator above the silicon in an integrated circuit. While this is seen as essential information in the micro-electronics industry, device physicists are more interested in the structure of devices within the semiconductor itself. While this is not possible as yet in homojunction devices, heterostructures in III-V and II-VI materials are easily imaged in FIB systems. An example of analysis of this type is the VCSEL lasers (figure 1).

Another area of device analysis particularly amenable to FIB is the sectioning of airbridge structures used in high frequency applications. Conventional grinding and polishing techniques often destroy the delicate bridge structures during preparation because of the mechanical forces used. FIB can quickly and safely section the structures, in exactly the right place, and then image the section for analysis (figure 2).

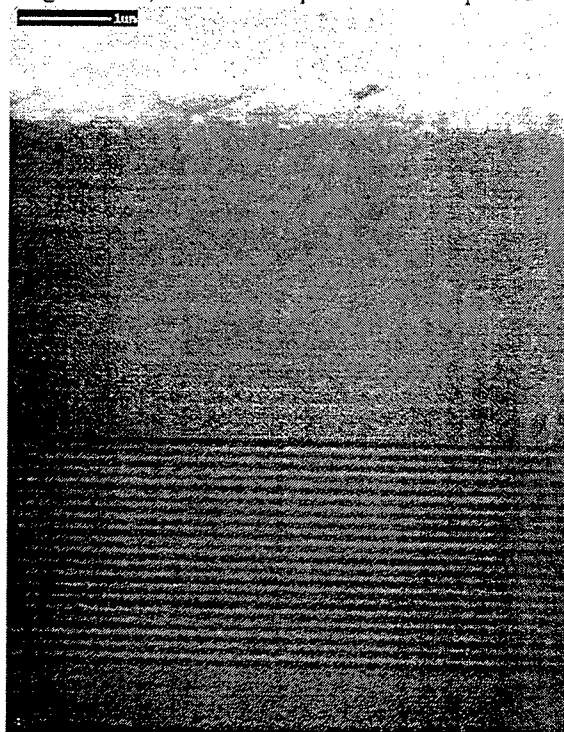


Figure 1. VCSEL laser cross sectioned and imaged by FIB.

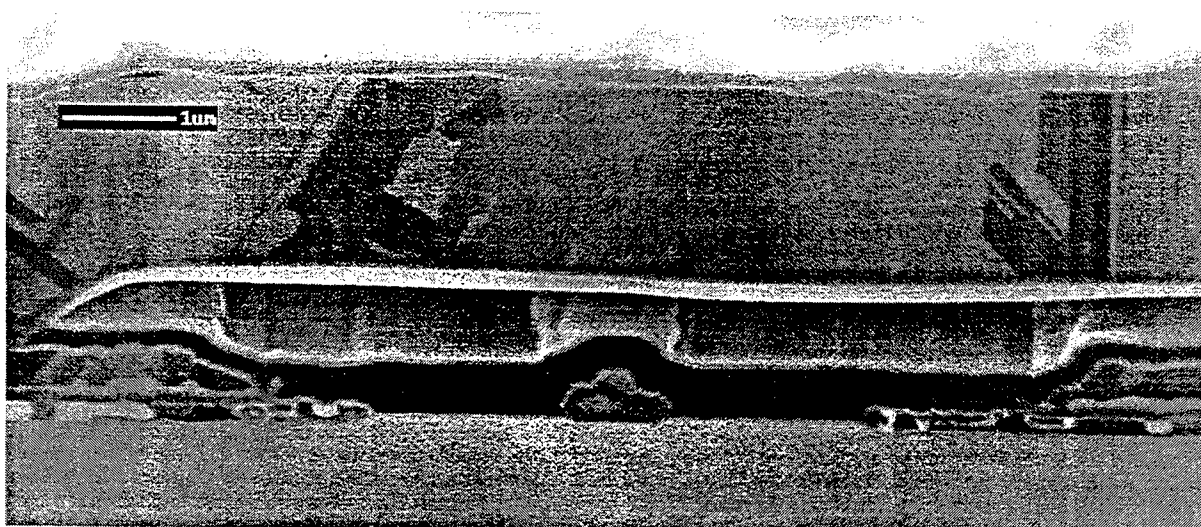


Figure 2. Cross section of airbridge HEMT structure, showing source, gate and drain. Note the channeling contrast in the metal contacts and the airbridge.

Transmission electron microscopy (TEM) provides, for many, the ultimate analytical tool because of the high resolution and the breadth of analytical techniques available. Sample preparation can often be difficult because

of the thinness of the membrane required. FIB can prepare TEM membranes in exactly the place required. If the site is visible from the surface, then it is easy to prepare the section without requiring the ion beam to image the membrane face. However, even if viewing the face is necessary to search for a hidden, sub-surface defect, for example, it is still possible to produce pristine, damage free specimens. Of current interest, at present subject to attempts to understand the phenomenon, is the ability to view doped InP material clearly in the TEM. The effect is seen only in InP and, anomalously, only in FIB prepared membranes (figure 3).

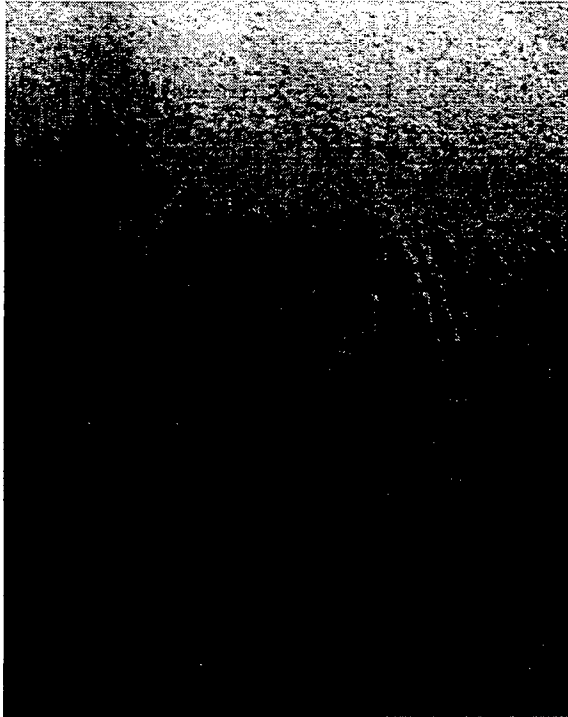


Figure 3. Doping contrast in CMBH laser.

With the addition of a mass spectrometer, the finely focused ion beam can be used to provide high spatial resolution SIMS data. SIMS may have been used for some time in device analysis but, because of the limited spot size of typical ion sources (1-100 μ m), has mostly been used in depth profile mode in layered structures. Elemental mapping in the 10nm range has been done on a number of structures, such as VCSEL lasers (figures 4a, 4b).

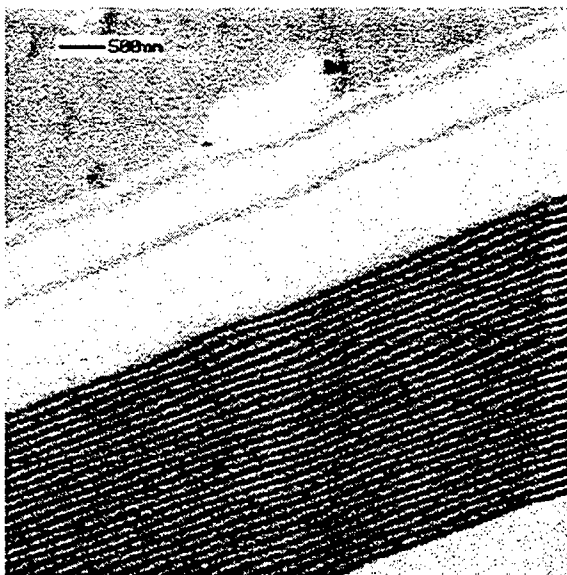


Figure 4a. Aluminium SIMS map of VCSEL.

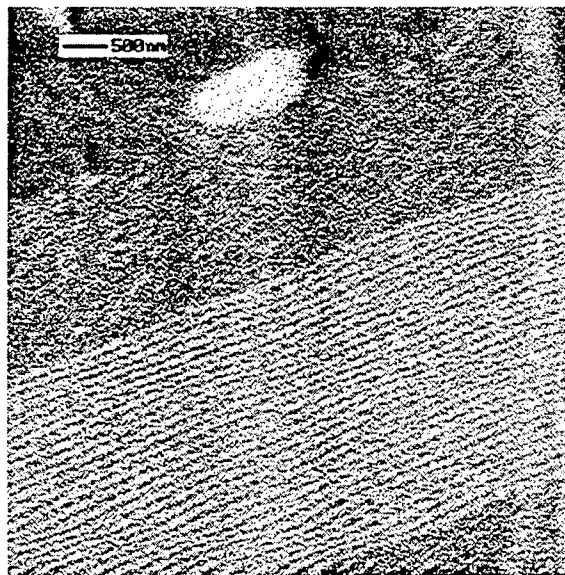


Figure 4b. Gallium SIMS map of VCSEL

Structural, electrical and optical characterization of single crystal
dysprosium phosphide (DyP) grown on GaAs by MBE

R.J.Hwu¹, P.P.Lee¹, M.Patel¹, M.Nikols¹, J.E.Shield¹, L.P.Sadwick¹
D.C.Streit², D.Brehmer³, K.McCormick³, S.J.Allen³, R.W.Gedridge, Jr.⁴

¹University of Utah, 3280MEB, Salt Lake City, UT 84112

²TRW, One Space Park, Redondo Beach, CA 90278

³Quantum Institute, Physics Dept., UCSB, CA 93106

⁴Naval Weapons Center, China Lake, CA 93555

Student Paper

ABSTRACT

The ability to grow buried high quality, epitaxial metallic or semi-metallic layers on semiconductors has many potential applications for novel device structures. The growth of such structures on GaAs is difficult as the metal/semiconductor heterostructures on GaAs reported to date are either thermodynamically unstable and diffuse into GaAs at elevated temperatures[1] or have relatively large lattice mismatches with GaAs. Also, long-term device reliability considerations require that these heterostructures must be able to withstand harsh environments and high temperatures for relatively long periods of time. One promising approach is to select a high melting point elemental metal-arsenide or metal-phosphide binary compound that displays metallic characteristics, is chemically inert and also provides a diffusion barrier to surface phosphorus evaporation and release. Recently there has been significant amount of interest in intermetallic and semimetallic compounds grown on gallium arsenide-based system. Excellent material and electrical properties have been reported for cobalt gallium (CoGa) on both GaAs and aluminum gallium arsenide (AlGaAs)[2][3], erbium arsenide (ErAs) on GaAs[4][5], scandium arsenide (ScAs) on GaAs[6], and lutetium arsenide (LuAs) on GaAs[4]. However, the rare-earth arsenide compounds studied to date have a relatively large lattice-mismatch to GaAs and rapidly oxidize when exposed to air. Although, significant amount of effort has been directed towards the study of rare-earth arsenide (REAs) compounds on GaAs, rare-earth phosphide (REP) compounds on GaAs or InP have not been appreciably studied. Thus, there is a need to investigate the growth and fundamental properties of rare-earth monophosphide binary and ternary compounds on GaAs and InP.

In this work we report the electrical and optical properties of epitaxial dysprosium phosphide (DyP) grown on semi-insulating as well as doped gallium arsenide (GaAs) substrates. The single crystal DyP layers were grown using both gas source and solid source molecular beam epitaxy (MBE). A detailed study of the structural, electrical and optical properties of DyP epilayers will also be presented. DyP is lattice matched to GaAs, with the room temperature mismatch being less than 0.01% (GaAs:5.6533 Å; DyP:5.6534 Å). Some potential applications of this work include realization of DyP/GaAs metal based transistors and DyP/GaAs heterojunction based transistors and superlattice structures. Since DyP has very high melting point and is very stable in ambient air, DyP epilayers can also be exploited as stable contacts to GaAs for high temperature applications.

The single crystal (001) dysprosium phosphide epilayers were grown on (001) GaAs using gas source MBE with tertiarybutylphosphine (TBP) as phosphorus source and solid source

MBE with solid phosphorus. The custom made MBE chamber was equipped with a diffusion pump and liquid nitrogen cooled trap. The growth temperatures were in the range of 450 - 550 °C. The full width half maximum values of DyP grown on GaAs as determined by double-crystal X-ray diffraction measurements is typically 21 arcseconds compared to 12-14 arcseconds for GaAs substrate. A two theta X-ray diffraction scan of a DyP/GaAs sample (Fig.1) shows only two peaks corresponding to the (002) and (004) reflections of DyP and GaAs. The d-spacing, structure factor and 2θ values for the (002) and (004) planes for GaAs and DyP are shown in Table 1. From Table 1, the approximate intensity ratios for the (002) to (004) peaks of GaAs and DyP are 1:138 and 4:1, respectively. Since the intensity of the (002) peak compared to the (004) peak for GaAs is very weak, the peak at 31.65° in the XRD pattern indicates that this is due to the DyP epilayer.

Table 1: X-ray parameters for GaAs and DyP

	(hkl)	2θ	d(Å)	structure factor(f)
GaAs	(002)	31.6539°	2.8266	1.83
GaAs	(004)	66.1129°	1.4133	21.48
DyP	(002)	31.6533°	2.8265	42.30
DyP	(004)	66.1115°	1.4132	21.48

The surface and interface properties of DyP/GaAs as determined from scanning electron and transmission electron microscopy will also be presented. Fig. 2, 3 and 4 show typical values of resistivity, mobility and carrier concentration of DyP on semi-insulating GaAs, respectively, as determined by variable temperature van der Pauw geometry Hall measurements. The scatter in Figs. 3 and 4 is due to the high carrier concentration ($n \approx \text{mid } 10^{20} \text{ cm}^{-3}$) which result in relatively small Hall voltages. The electrical properties of DyP/GaAs as determined from current versus voltage and capacitance versus voltage measurements will also be presented.

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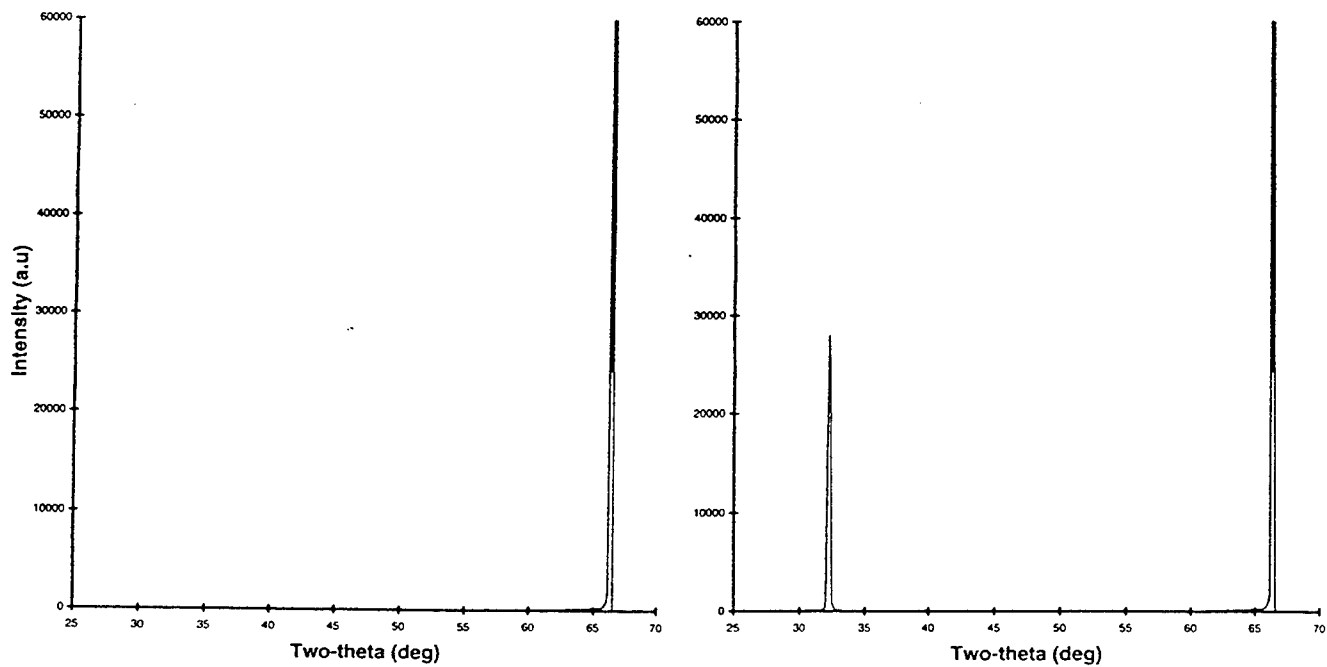


Figure 1 XRD patterns for a) (001) GaAs and b) DyP on (001) GaAs

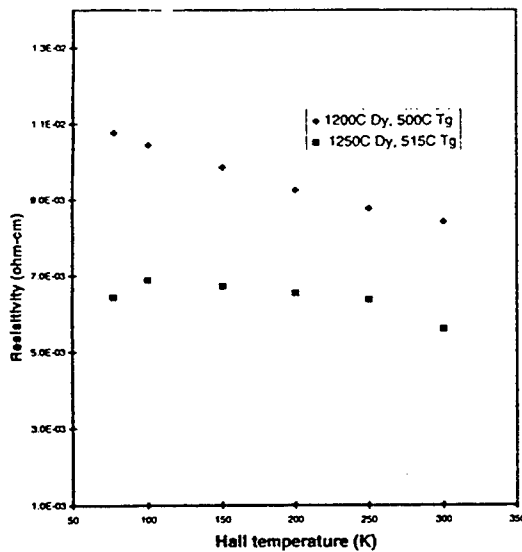


Figure 2 Resistivity versus Hall temperature for different Dy E-cell temperatures

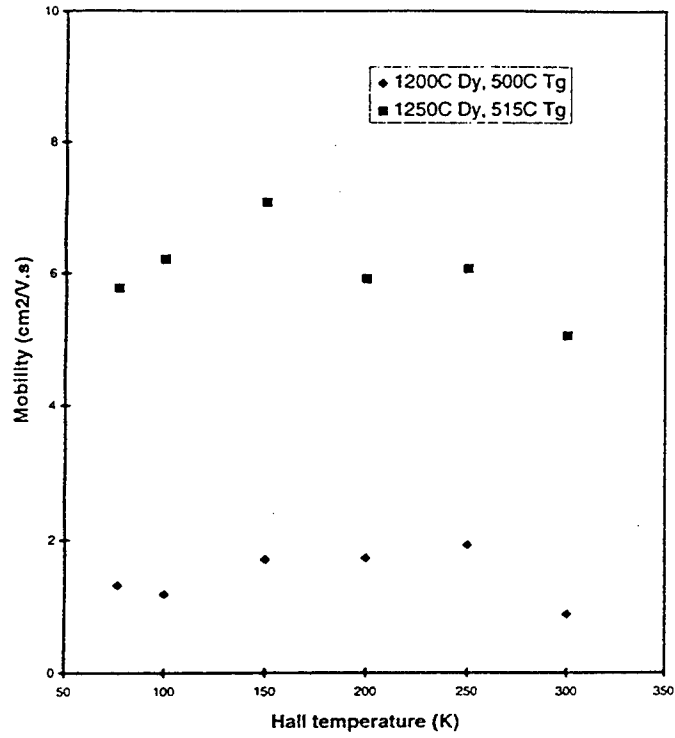


Figure 3 Mobility versus Hall temperature for different Dy E-cell temperatures

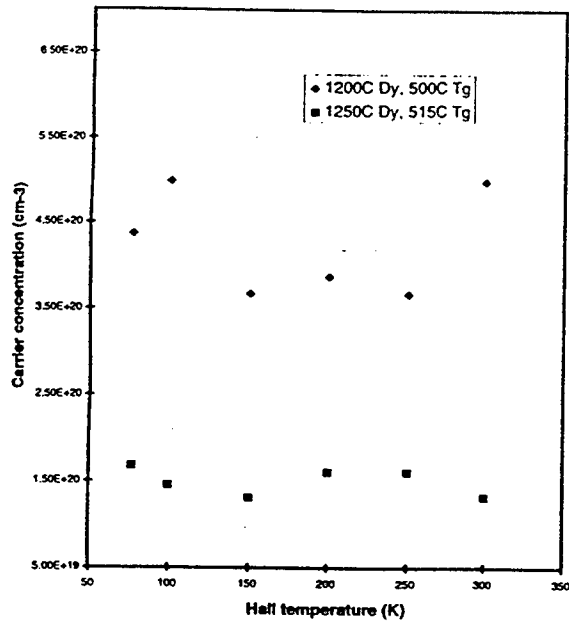


Figure 4 Carrier concentration versus Hall temperature for different Dy E-cell temperatures

OPTICAL METHODS FOR THE ROOM TEMPERATURE, NONDESTRUCTIVE CHARACTERIZATION OF WAFER-SIZED COMPOUND SEMICONDUCTOR DEVICE STRUCTURES

Fred H. Pollak, Wojciech Krystek, M. Leibovitch and L. Malikova

Physics Department and New York State Center for Advanced Technology in
Ultrafast Photonic Materials and Applications
Brooklyn College of the City University of New York, Brooklyn, NY 11210

I. INTRODUCTION

The nondestructive characterization and qualification of complex semiconductor multilayer structures is a crucial step in the fabrication of semiconductor devices. Such nondestructive qualification procedures could have a significant impact on the cost and yield of devices. Developmental efforts are driving device design toward more compact structures. This trend places ever increasing demands on device parameters and hence evaluation procedures in order to upgrade performance and yield.

This talk will review the optical techniques of photoluminescence, modulation spectroscopy [photoreflectance (PR) and contactless electroreflectance (CER)] and spectral ellipsometry which are being used for semiconductor device characterization. These methods are relatively simple, inexpensive, compact, rapid and informative and also can be performed in a nondestructive manner at (or even above) room temperature on wafer-sized samples. Recent works have clearly demonstrated their considerable potential and growing importance in the evaluation of devices such as heterojunction bipolar transistors (HBTs), pseudomorphic high electron mobility transistors (PHEMTs), quantum well lasers, vertical cavity surface emitting lasers (VCSEL), multiple quantum well (MQW) infrared detectors, solar cells, etc. [1-6].

PR/CER are particularly useful forms of modulation spectroscopy since they not only produce sharp, derivative-like spectra but also are sensitive to surface/interface electric fields. For sufficiently high built-in electric fields the PR/CER spectrum can display an oscillatory behavior above the band gap called Franz-Keldysh oscillations (FKOs) which are a direct measure of the built-in electric field [1].

II. APPLICATIONS

A. Heterojunction Bipolar Transistors

It has been demonstrated that PR/CER [1-3] and SE [3] can be effective, nondestructive screening methods for HBT structures. For example, certain features in the PR/CER spectra at 300K from GaAs/Ga_{1-x}Al_xAs HBT structures have been correlated with actual device performance and hence PR/CER can be used as a tool to evaluate entire wafers before processing.

Shown in Fig. 1 is the PR spectrum at 300K from the collector (GaAs) and

emitter (GaAlAs) regions for an MBE fabricated HBT sample. The band gap of GaAs is 1.42 eV while the band gap of the GaAlAs portion of the sample is 1.830 eV, which corresponds to an Al composition of 28 %.

The oscillatory features above the band gaps are the FKOs. From the period of these FKOs it is possible to directly evaluate the built-in *dc* electric fields in the GaAlAs emitter (F_{dc}^{emit}) as well as in the *n*-GaAs collector region (F_{dc}^{coll}). The deduced values F_{dc}^{emit} were compared with device parameters of fabricated HBT MBE samples. Below electric field values of about 2×10^5 V/cm high current gains were obtained while the current gain fell markedly at fields above this value. These observations have made it possible to use PR as a screening technique to eliminate wafers with unwanted characteristics before the costly fabrication step.

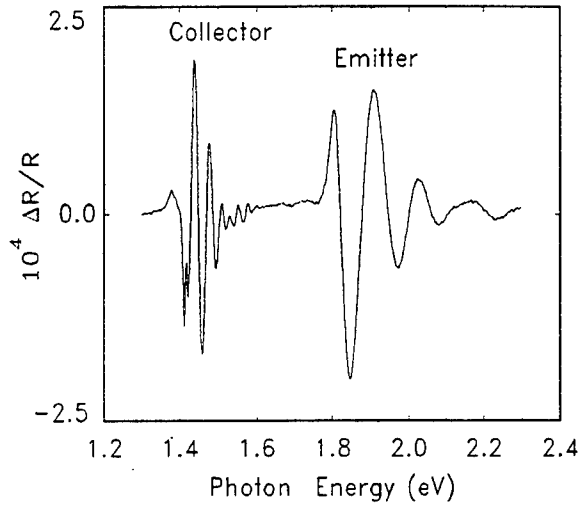


Fig. 1 300K PR spectrum of a GaAlAs/GaAs HBT.

B. Pseudomorphic High Electron Mobility Transistor Structures

Pseudomorphic high electron mobility transistor (PHEMT) structures have been characterized by room temperature PL [4], PR/CER [1,2] and SE [5]. Photoluminescence yields information about the two-dimensional (sheet) electron gas (2DEG) density, built-in field, width and alloy composition of the channel as well as the alloy composition of the confining layers. In addition to these parameters PR/CER produces information built-in fields in other parts of the structure due to Fermi level pinning, including the front cap layer.

Shown in Fig. 2 by the solid line is the 300K PL spectrum from the InGaAs channel of a double-pulsed doped GaAlAs/InGaAs/GaAlAs PHEMT [4]. The dashed line is a least-squares fit to a quantitative analysis developed by Brierly. The fit yields the values of three intersubband transitions as well as the Fermi level.

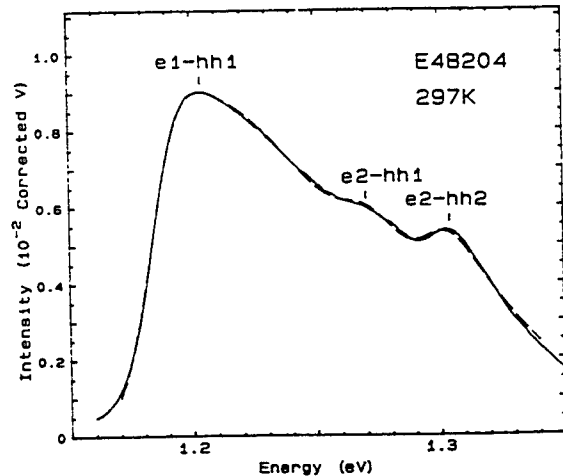


Fig. 2 300K PL spectrum (solid line) from a double-pulse doped PHEMT. The dashed curve is the fit to the model.

The notation $em-hhn$ denotes a transition from the m^{th} electron to n^{th} heavy-hole level. From this data it is possible to deduce the 2DEG as well as the width (100Å) and In composition (924%) of the channel.

PR/CER can be used to obtain the entire potential profiles in such structures [1,2]. Displayed by the solid line in Fig. 3 is the CER spectrum originating in the InGaAs section of a step-doped GaAlAs/InGaAs/GaAs PHEMT, except for the feature denoted $E_0(\text{GaAs})$ which corresponds to the direct band gap of GaAs and originates in the GaAs buffer/substrate. The trace of Fig. 3 consists of four peaks, labelled mnH (transition from the m^{th} electron to n^{th} heavy-hole level), riding on a background, which is due to the thermal tail of the Fermi distribution function. The dashed line in Fig. 3 is a fit to a lineshape function which is the derivative of a broadened step-like two-dimensional density of states, due to the screening of the excitons by the 2DEG, and a Fermi level filling factor. The obtained energies of the mnH transitions are denoted by arrows. By comparing these experimental energies with a theoretical self-consistent calculation it is possible to evaluate the channel width, In composition and built-in electric field. The fit to the background yields the Fermi energy and hence the sheet density.

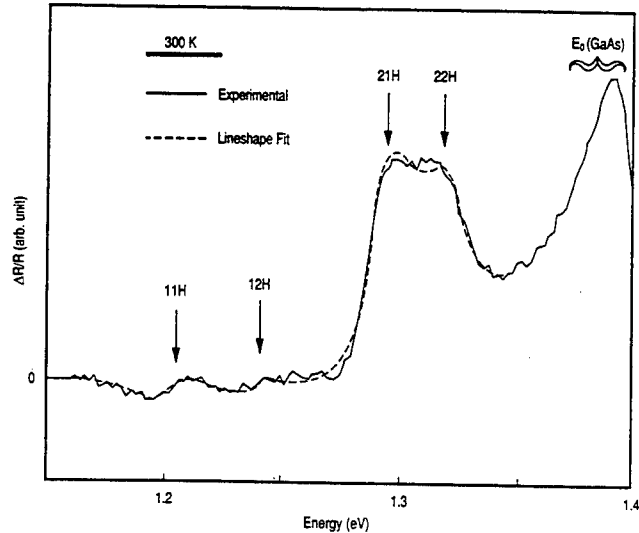


Fig. 3 300K CER spectrum (solid line) from the InGaAs portion of a GaAlAs/InGaAs/GaAs PHEMT. The dashed line is a lineshape fit yielding the energies of the quantum transitions (denoted by arrows) and the Fermi energy.

The observed GaAs and GaAlAs signals exhibit FKOs from which it is possible to obtain information about the electric fields in these regions and the Al composition.

SE has been used to obtain alloy composition and layer thicknesses on these structures [5].

C. Quantum Well Laser Structures

Although the most commonly used optical technique to characterize these structures is PL it has recently been demonstrated that PR/CER can be used to obtain information about every relevant portion of a wide variety of quantum well laser structures including vertical cavity surface emitting lasers [1,2,6]. Quantum well laser structures employ complex sequences layers where a few light-emitting QWs are embedded in the waveguide [separate confinement heterojunction (SCH)]

regions and enclosed by p - and n -doped contact layers. In PR/CER signals are observed from both the QW (or MQW) and SCH regions and often from the upper (generally p -doped) contact layer. Shown in Fig. 4 by the solid line is the 300K PR spectrum from a 1.3 μm pseudomorphic InGaAsP/InP MQW laser [6]. The signal up to about 1.1 eV originates in the MQWs. From the detailed lineshape fit, denoted by the crossed line, it is possible to obtain the energies of five quantum transitions, as designated by the arrows. Comparison of these energies with a theoretical calculation makes it possible to completely characterize the MQWs, i.e., well widths, alloy composition and strain. The lowest lying feature is related to the lasing wavelength. Its energy can readily be determined to better than ± 1 nm at 300K. The signals from both the InGaAsP SCH and InP portions exhibit FKOs, from which the built-in fields can be evaluated. The SCH field is related to the doping levels in the InP regions. Also the SCH signal yields the InGaAsP composition.

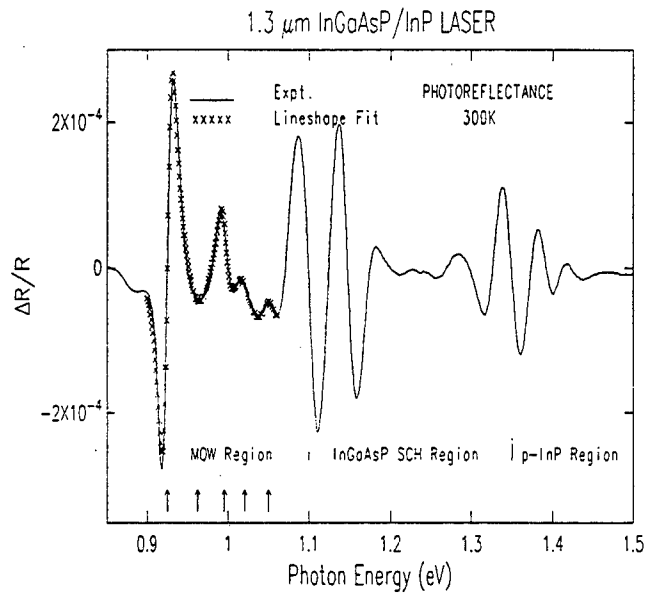


Fig. 4 300K PR spectrum (solid line) from a 1.3 μm pseudomorphic InGaAsP/InP MQW laser. The crossed line is a lineshape fit yielding the energies denoted by arrows.

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Interference Technique for a-Si:H Films Optical Measurements.

T. Globus, Department of Electrical Engineering, University of Virginia,
Charlottesville, VA 22903

Over the past two decades, considerable efforts were made in order to find efficient, reliable, and nondestructive methods for hydrogenated amorphous- and poly-silicon film characterization. The work has been motivated by the many of applications of these materials for large area microelectronic devices, such as thin film transistor arrays for active-matrix-liquid-crystal flat panel display technology, terrestrial-based large area photovoltaics for solar cells and linear line-sensors.

Optical measurements are among the most powerful methods of materials characterization. These methods can be used for the fast nondestructive control of quality of materials for device fabrication. The information gained from the optical studies allows one to determine the optimal conditions of materials growth and film processing. The absorption spectrum itself, as well as the refractive index spectrum, are important characteristics of hydrogenated amorphous silicon (a-Si:H) and related materials used for applications such as solar cells and photonics. The optical absorption spectrum provides information about the energy gap, the hydrogen content, concentration and energy of localized defect states, and can be used as a method of defect spectroscopy for electronic states with energies below the mobility edge.

This work introduces a new interference technique for determination of absorption coefficient and refractive index spectra of a-Si:H thin films. The technique is based on computer analysis of simultaneous transmission and specular reflection measurements of thin films on substrates. The proposed method is verified by comparing the experimental data with theoretical computations and with previous measurements of the absorption spectra. Preliminary applications of the new technique to a-Si:H indicate new features of the absorption spectra. These include previously unreported structure of the absorption spectra in the photon energy range near the mobility gap of a-Si:H films.

Several different techniques are often used for the measurements of absorption coefficient as a function of photon energy. These include conventional transmission spectroscopy, photothermal deflection spectroscopy, the constant photocurrent method, and photo-pyroelectric spectroscopy. All these techniques yield only relative absorption spectra. Fitting these data to absorption spectra determined by transmission measurements is required in order to place relative spectra on an absolute scale. This is usually done by matching experimental data to the results of optical transmission in the photon energy range corresponding to large absorption coefficient. Even more important is the fact that all methods which include reflection of incident light from the front and the back surface of thin film have serious limitations caused by interference. As a result, the uncertainty in the absorption coefficient can be as large as an order of magnitude. In conventional transmission spectroscopy it is common to assume incoherent multiple reflection in the film and in the substrate and to average adjacent fringes in order to obtain the incoherent form for the optical transmission. Removing the interference fringes from the transmission spectra, i.e. estimating a baseline, is one of the error sources in conventional transmission spectroscopy [1]. The application of conventional techniques is further limited by the fact that the interference induced uncertainty in the measured absorption spectra increases with the improvement in the film thickness uniformity and in the surface morphology.

In this work, we employed the alternative interference technique for the absorption coefficient and refractive index spectra determination from the results of transmission (T) and reflection (R) measurements. Recently, the variation of this technique was applied to films of a-Si:H and alloys [2,3] and was found effective in the photon energy range above the optical gap. The absorption coefficient has been determined by using the ratio $T/(1-R)$, which almost completely eliminates disturbance from the interference effect. This, however, limits the sensitivity of the interference method which is potentially close to the sensitivity of modulation

spectroscopy. The analysis presented here is based on exact interference equations for the system of a film on a substrate. These account not only for the interference in the a-Si:H film but also for the absorption inside the substrate and for the reflection from both substrate surfaces. The method is based on a self-consistent interference analysis of the measurement results. The formulae for the optical transmission and reflection by a plane parallel sheet on a transparent substrate have been applied to semiconductor films by Hall and Ferguson [4]. Transmission and reflection are given in a more convenient form in [5], together with some important details of the interference technique.

When light is incident on a thin parallel sheet of a partially transparent material, multiple reflection take place on both surfaces and cause constructive or destructive interference in the reflected and transmitted beams at selected wavelengths. The transmission T_{13} and reflection R_{13} of the medium / film / substrate system in the case of a near normal angle of incidence, and without allowance for multiple reflection in the substrate, are:

$$T_{13} = \xi T_{12} T_{23} e^{-\alpha_2 d_2}, \quad R_{13} = \xi (R_{12} - 2 e^{-\alpha_2 d_2} \cos 2\delta_2 (R_{12} R_{23})^{1/2} + R_{23} e^{-2\alpha_2 d_2}), \quad (1)$$

$$\text{where} \quad \xi = (1 - 2 e^{-\alpha_2 d_2} \cos 2\delta_2 (R_{12} R_{23})^{1/2} + R_{12} R_{23} e^{-2\alpha_2 d_2})^{-1}. \quad (2)$$

Here $\delta_2 = 2\pi n_2 d_2 / \lambda$ is the phase thickness of the film at the wavelength λ ; α_2 , n_2 and d_2 are the absorption coefficient, the refractive index and the thickness of the film. The coefficients of transmission and reflection $T_{i,i+1}$ and $R_{i,i+1}$ at the medium i / medium $i+1$ interface are given by

$$T_{i,i+1} = 4 (n_{i+1} / n_i) (n_i^2 + k_i^2) / [(n_i + n_{i+1})^2 + (\kappa_i + \kappa_{i+1})^2], \quad (3)$$

$$R_{i,i+1} = [(n_i - n_{i+1})^2 + (\kappa_i - \kappa_{i+1})^2] / [(n_i + n_{i+1})^2 + (\kappa_i + \kappa_{i+1})^2], \quad (4)$$

where n_i are refractive indices, and $k_i = \lambda \alpha_i / 4\pi$ are corresponding extinction coefficients. These expressions are valid in the case of a relatively weak absorption coefficient of the film, i.e. when $n_2^2 > k_2^2$. For a bulky substrate, the measured values of the transmission T_{ex} and reflection R_{ex} of the system, with allowance for incoherent reflection in the substrate, are

$$T_{ex} = T_{13} (1 - R_i) e^{-\alpha_3 d_3} / (1 - R_i R_{31} e^{-2\alpha_3 d_3}), \quad (5)$$

$$\text{and} \quad R_{ex} = R_{13} + R_i T_{13}^2 / (1 - R_i R_{31} e^{-2\alpha_3 d_3}). \quad (6)$$

Here $R_i = (n_1 - n_3)^2 / (n_1 + n_3)^2$ is the reflection from the air-substrate interface, and

$$R_{31} = \xi (R_{32} - 2 e^{-\alpha_2 d_2} \cos 2\delta_2 (R_{12} R_{23})^{1/2} + R_{12} e^{-2\alpha_2 d_2}) \quad (7)$$

is the reflection of a medium / film / substrate / medium system illuminated from the substrate side. The transmission spectrum of the system is the same for the front-side and back-side illumination. However, the measured values of reflection in these two configurations are slightly different. Nevertheless, since the factor $R_i R_{31}$ in (5) and (6) amounts to a small correction, it can be replaced with sufficient accuracy by the quantity $R_i R_{13}$.

The transmission and reflection spectra are measured with Cary 5E Spectrophotometer using a two-beam scheme with specular reflection attachments which ensure a near normal ($\sim 8^\circ$) angle of incidence on the sample. We used undoped samples of device quality a-Si:H thin films with hydrogen content $\sim 8-10\%$. Both transmission and reflection spectra reveal deep interference fringes in the IR region. The interference pattern is almost the same for different regions of the wafer (the variations of the wave-lengths corresponding to extrema do not exceed 1-2%) which means that film thickness uniformity is sufficiently high for implementing interference method. Similarly, positions of T and R extrema practically coincide in

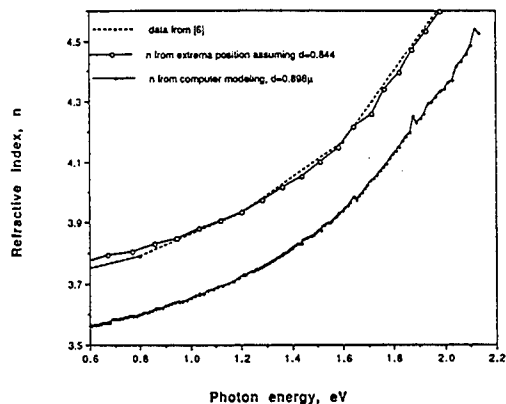


Fig. 1. The refractive index dispersion.

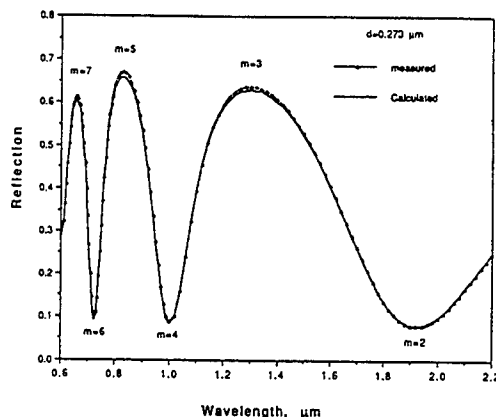


Fig. 2. The reflection spectra: measured and calculated.

the range of small absorption, which is important for further analysis. The high degree of film thickness uniformity is also evidenced by the fact that experimental values of fringes amplitudes, i.e. the ratios R_{max}/R_{min} and T_{max}/T_{min} are in excellent agreement with those computed from equations (1)-(7). The thickness of the film and the dispersion curve for n_2 can be estimated as usually from the position of extrema λ_m by using the relationship $d_2 = m \lambda_m / 4n_2$ with the value of refractive index n_2 taken from the literature [6]. The order of extrema m is found from the wavelengths of two adjacent extrema, since n_2 does not change appreciably when m is increased by one. The dispersion curve for n_2 is shown in Fig. 1 together with published results [6]. The agreement is very good. However, the numerical value of the refractive index of a-Si:H can vary significantly between different samples depending on the hydrogen content and the film density. Consequently, the values of d_2 and n_2 obtained in this manner are only used as the initial estimates which have to be corrected as discussed below.

Using preliminary results for $n_2(\hbar\omega)$ at the specified photon energies $\hbar\omega$, the absorption spectrum $\alpha_2(\hbar\omega)$ which fits the measured transmission spectrum $T_{ex}(\hbar\omega)$ can be calculated from equation (5) by an iterative procedure. Knowing both $n_2(\hbar\omega)$ and $\alpha_2(\hbar\omega)$ permits one also to calculate the spectrum of reflection R_{ex} using eq.(6). This method serves as an additional verification of the extracted parameters d_2 and n_2 . The reflection spectrum calculated using a single iteration is compared with experimental data in Fig. 2. The calculated interference pattern closely follows the experimental data. There are, however, small discrepancies, because d_2 and n_2 accepted for simulation are not exact. As a result, the calculated absorption spectrum reveals fictitious interference fringes in the range of weak absorption. To obtain correct absorption data in the subgap range where $\alpha \approx 10 - 100 \text{ cm}^{-1}$, the thickness of the film has to be determined with the accuracy better than $0.01 - 0.005 \mu\text{m}$. After corrected values of the film thickness and refractive index at specified photon energies are found, the computer program that compares the measured and calculated transmission and reflection spectra is used to obtain both $\alpha_2(\hbar\omega)$ and $n_2(\hbar\omega)$ by the second iteration.

Two similar samples with slightly different thicknesses were measured in order to establish the reproducibility of the results obtained by interference technique (Fig. 3). The numerical values of the absorption coefficient are close to the published data [7] also shown. At $\alpha_2 > 10^4 \text{ cm}^{-1}$ the absorption coefficient follows the well known Tauc dependence (Fig. 4) $(\alpha \hbar\omega)^{1/2} = B (\hbar\omega - E_1)$ with the threshold energy $E_1 = 1.685 \pm 0.01 \text{ eV}$ which is usually

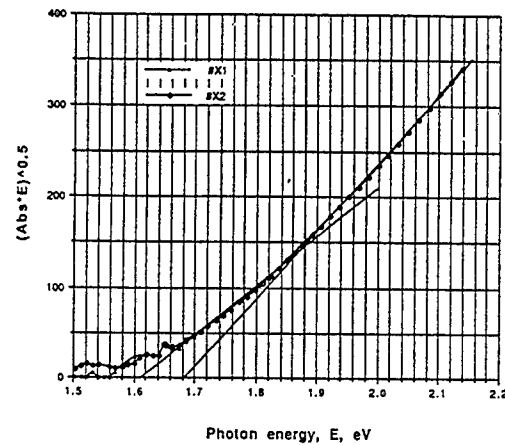
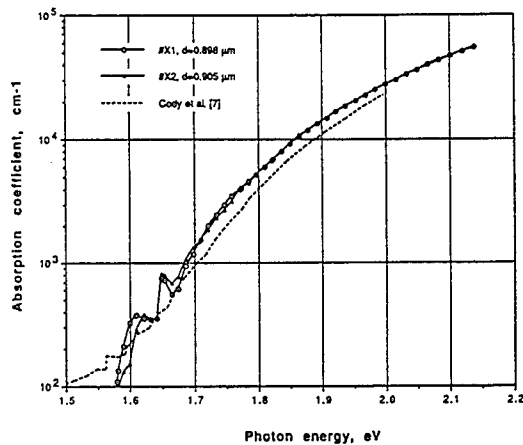


Fig. 3. The absorption coefficient spectra for two samples. Fig. 4. The Tauc plot for the absorption coefficient.

interpreted as the optical gap E_g . The data for $\hbar\omega < 1.85$ eV follow a different Tauc law with the threshold energy $E_2 = 1.615 \pm 0.01$ eV. At the same time, our measurements indicate a new structure in the absorption spectrum near the fundamental edge. These are several peaks and steps with the most pronounced peak centered at the photon energy 1.65 eV. Tauc has discovered the tail near absorption edge in amorphous Ge and suggested that this tail is caused by excitons bound to neutral acceptors [8]. In our case, the asymmetry of the peak form around 1.65 eV, with sharp rise of absorption at low energy side and more slow reduction at high energy side, can also indicate the exciton related absorption and the presence of localized defects.

The proposed technique ensures a high accuracy of the measured optical characteristics. The resolution of the method is not less than a few meV. This makes it possible to determine the spectra of the derivatives of these characteristics by point by point numerical differentiation in steps of several meV on the energy scale and consequently to analyze the details in the electron density of states. As a result, this technique is no less sensitive in determining energy spectra than modulation spectroscopy based methods (for example, electroabsorption or electroreflectance measurements), but it yields more information due to the possibility of simultaneous analysis of optical characteristics and their derivatives. In particular, the interference technique makes possible high precision measurements of the absorption in the region near the fundamental edge, where absorption coefficient varies over several orders of magnitude, and to measure the absorption related to impurities and defects in the subgap energy region. The results of absorption measurements in the subgap energy range will be discussed later.

Acknowledgment

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Characterization of Pseudomorphic Heterostructure FETs by the Photoconduction Technique

Fritz Schuermeyer, Charles Cerny, J.P. Loehr, and R.E. Sherriff
Wright Laboratory, Wright Patterson AFB, OH 45433, USA

Photoelectric or optoelectronic techniques are routinely used to study the energy configuration in semiconductor materials. Techniques such as photoluminescence (PL) and photoreflectance (PR) have become invaluable in obtaining bandgap energies as well as conduction- and valence-band discontinuities in heterostructure materials. Recently, the photoelectric technique was applied to fully fabricated PHEMTs [1], studying photoconduction in these FETs under backside illumination. Primarily, transistors without a charge supply layer underneath the channel (underdoping) were evaluated. The lack of underdoping resulted in a flat quantum well for the depleted device and the $\Delta n=0$ selection rule for square-well interband transitions is strong. Consequently, only a few interband transitions in the absorption spectrum are allowed and these transitions are easily identified in the photoconductance characteristics of the PHEMTs. In this paper the photoelectric studies are extended to the characterization of transistors with underdoping and for the first time the ground state intersubband transition is identified.

Figure 1 presents a sketch of the experimental setup for the photoemission and conduction (PEC) studies. The PEC measurements are performed on-wafer at room temperature using either Cascade or shielded Pico probes. The wafer chuck contains a hole in its center. A micromanipulator positions one end of an optical fiber directly underneath a device, and the other end of the optical fiber is connected to the exit slit of

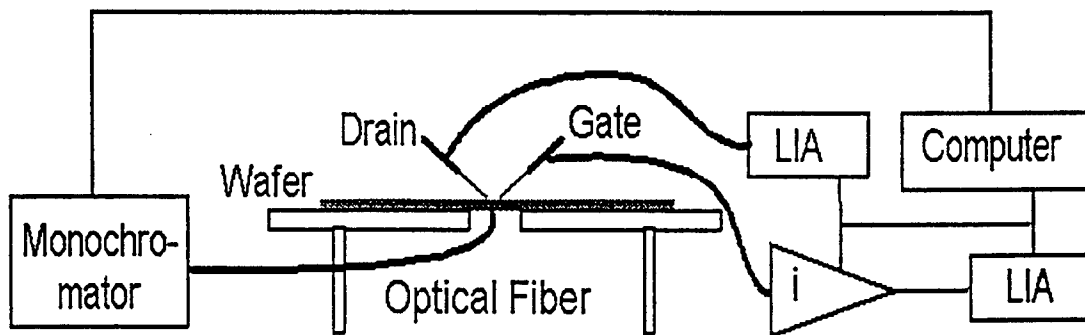


Figure 1 Experimental setup for PEC measurements

a SpectraPro-150 (Acton Research Corporation) monochromator. A 50 W tungsten light source is employed and the light is mechanically chopped. Stanford Research SR530 lockin amplifiers are utilized to measure the photocurrents at the drain and gate electrodes. A low noise current preamplifier SR570 is used to amplify the gate photocurrent and to provide the gate voltage. The measurements are performed on GaAs based PHEMTs, grown by MBE. The channel and barrier consist of 12.5 nm

$\text{In}_{0.22}\text{Ga}_{0.78}\text{As}$ and 24 nm $\text{Al}_{0.24}\text{Ga}_{0.76}\text{As}$ layers respectively. The barrier layer is doped to supply carriers to the channel. The structure is grown on top of a GaAs buffer layer. Devices on two wafers were studied where one wafer contained underdoping with a nominal charge density of $1 \times 10^{12} \text{ cm}^{-2}$. The second wafer was grown without underdoping. In this paper photoconductance results obtained on devices with a nominal gate length of 1 μm are reported.

Figure 2 presents typical photoconduction (PC) results obtained on a pseudomorphic HFET that contained no underdoping [1]. The measurements were performed under pinch-off condition and it was shown [2]

that the transistor amplifies the photocurrent in this gate voltage regime. The lower curve in Fig. 2 presents the PC characteristic versus photon energy E . This characteristic resembles the theoretical absorption curve, obtained using a self-consistent solution to the Schrödinger and Poisson equations. One observes that at low photon energies the PC signal is negligible. At photon energies of 1.19, 2.27, and 1.37 eV step-like increases in PC become evident due to E1-HH1, E2-HH2, and E3-HH3 interband transitions respectively. To better analyze these transitions the PC versus E curve was differentiated (upper part of Fig. 2) and three peaks are observable due to the indicated transitions. At photon energies larger than 1.4 eV the PC signal becomes extinct since the GaAs substrate is not transparent in this energy range. The PC results complement data obtained by PL, PLE, and PR and can be used to more accurately model dc and rf behavior of these FETs.

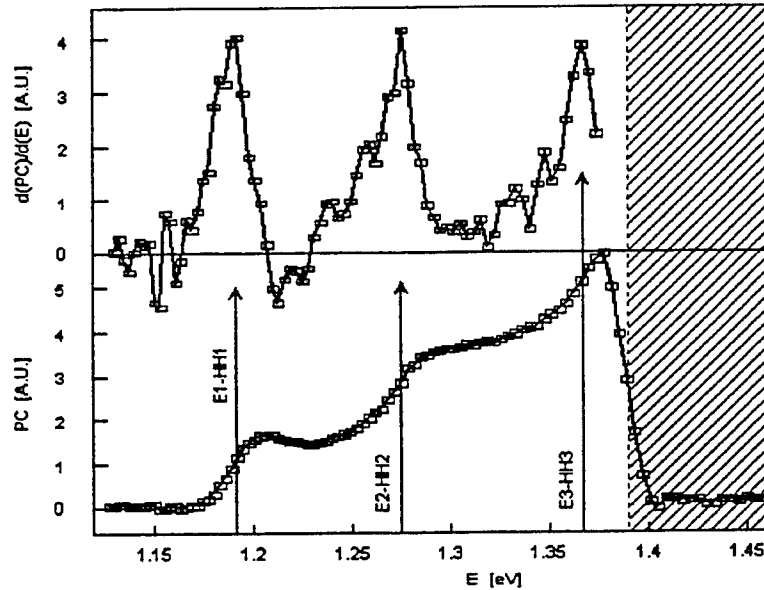


Figure 2 Typical photoconduction results of a PHEMT without underdoping [1]

At photon energies larger than 1.4 eV the PC signal becomes extinct since the GaAs substrate is not transparent in this energy range. The PC results complement data obtained by PL, PLE, and PR and can be used to more accurately model dc and rf behavior of these FETs.

In devices with underdoping, a flat quantum well cannot be obtained under any gate voltage and the selection rule is not valid. Figure 3 shows the PC characteristic of such an HFET at pinch-off ($V_g = -2.3 \text{ V}$). The step-like behavior is not apparent in this figure. Figure 4 shows the derivative of the PC curves for two gate voltages, -2.3 and -1.7 V. At $V_g = -2.3 \text{ V}$ the device is pinched off while at $V_g = -1.7 \text{ V}$ the transistor is in the 'on' condition. At pinch-off, an electric field in the channel causes the electrons to gravitate towards the substrate and the holes towards the gate. No individual transitions can be identified in the spectrum under this bias condition. When the gate bias is changed towards more positive gate potentials then the electron and hole wavefunctions change and the strength of the individual interband transitions vary. As a result, one observes peaks in the derivative spectrum which appear and disappear with changing gate

voltage. The spectrum obtained at $V_g = -1.7$ V is an example where several individual transitions are apparent. In this curve only the ground state interband transition can be identified.

In a symmetrical channel (the top part of the quantum well is a mirror image of the bottom part) some selection rules are valid: transitions where Δn is an odd number are forbidden. We performed theoretical studies to investigate if a symmetrical well can be achieved at certain gate voltages. We observed that due to the disparity of the top and bottom heterobarrriers (InGaAs/AlGaAs and InGaAs/GaAs respectively) symmetry in the quantum well cannot be obtained. This disparity is aggravated by the electric field below the channel due to the underdoping, which drastically reduces the effectiveness of the bottom barrier. Note that this disparity also exists in FETs without underdoping. However, due to the negligible electric field in the GaAs buffer layer in such devices, the GaAs/InGaAs conduction band discontinuity forms an effective barrier resulting in symmetrical wavefunctions even for the third electron subband. We expect that a symmetrical well can be achieved with AlGaAs at the top and bottom of the channel, even in devices with underdoping.

The authors would like to express their appreciation to Robert Bacon for help in performing the measurements, to Ross Dettmer, Greg Desalvo, Jack Ebel, Dave Via, Tony Quach, Charles Havasy, Chris Bozada, and Ken Nakano for device processing and to Keith Evans and Jim Ehret for wafer growth.

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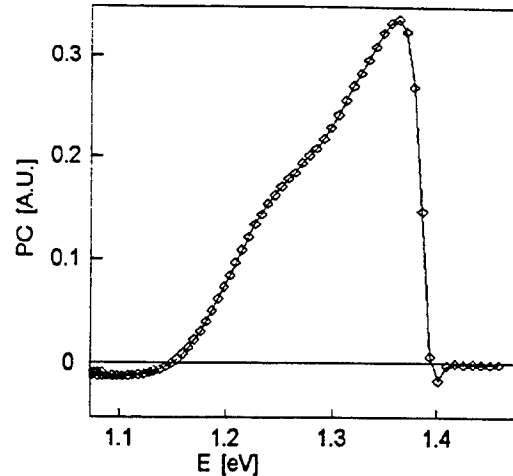


Figure 3 Photoconduction vs photon energy of an HFET with underdoping

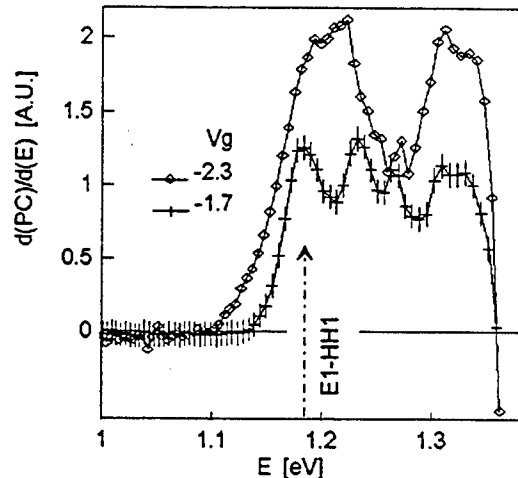


Figure 4 Derivative of PC characteristics of HFET with underdoping for two gate voltages

Near-field Photoelectronic Studies of Nanometer-scale Defects in Relaxed GeSi Films

J. W. P. Hsu

Department of Physics, University of Virginia, Charlottesville, VA 22901

E. A. Fitzgerald,* Y. H. Xie, and P. J. Silverman

AT&T Bell Laboratories, 600 Mountain Ave., Murray Hill, NJ 07974

Using a near-field scanning optical microscope (NSOM), we investigate defects and morphology on the surface of relaxed GeSi films that arise from the strain release caused by lattice mismatch between the heteroepitaxial films and the Si substrates. Threading dislocations are identified by simultaneously imaging the surface topography and the photoelectric signals. Characterization using an electron microscope is commonly used for this type of defect imaging. Images based on photoelectrical contrast is analogous to electron beam induced current (EBIC) imaging. The resolution achieved with a NSOM is ten times higher than with conventional far-field optical techniques, and similar to that of EBIC. We will present results of surface morphology and photoelectric response near threading dislocations, as well as compare our results with EBIC results.

The ability to integrate devices made of different materials is the key to advancing modern electronic and optoelectronic technologies. Thus, the growth of good quality films having bulk properties on lattice mismatched substrates and the characterizations of such films have been a major area of study in material science. We will report the use of a novel optical technique, the near-field scanning optical microscope (NSOM), to simultaneously study, with spatial resolution better than 100 nm, the surface morphology and electric-optical activity of individual threading dislocations on relaxed $\text{Ge}_x\text{Si}_{1-x}$ films. Because the size of each crystalline defect is much smaller than the diffraction limit of visible light, such defect characterization has been limited until now to electron microscopy techniques. This study also demonstrates the power of the NSOM, which achieves a more than ten-

* Present Address: Department of Materials Science and Engineering, MIT.

fold increase in spatial resolution from conventional far-field optical methods. The capability to simultaneously study morphology and photoresponse of the same defect structure is the major advantage of the NSOM over electron microscopy.

The NSOM used in this experiment operates in reflection mode, and was modified from a commercial scanning force microscope (PSI BD-2). The tips were tapered, Al-coated optical fibers similar to those reported in Ref. 1. Shear force feedback [2,3] was used to regulate the tip-sample separation between 10 and 20 nm. Topographic images are generated by applying a voltage to the z piezo scanner to keep the shear force signal constant, while the spatially resolved near-field photoresponse is measured simultaneously.

Samples studied in this experiment are grown by molecular beam epitaxy and

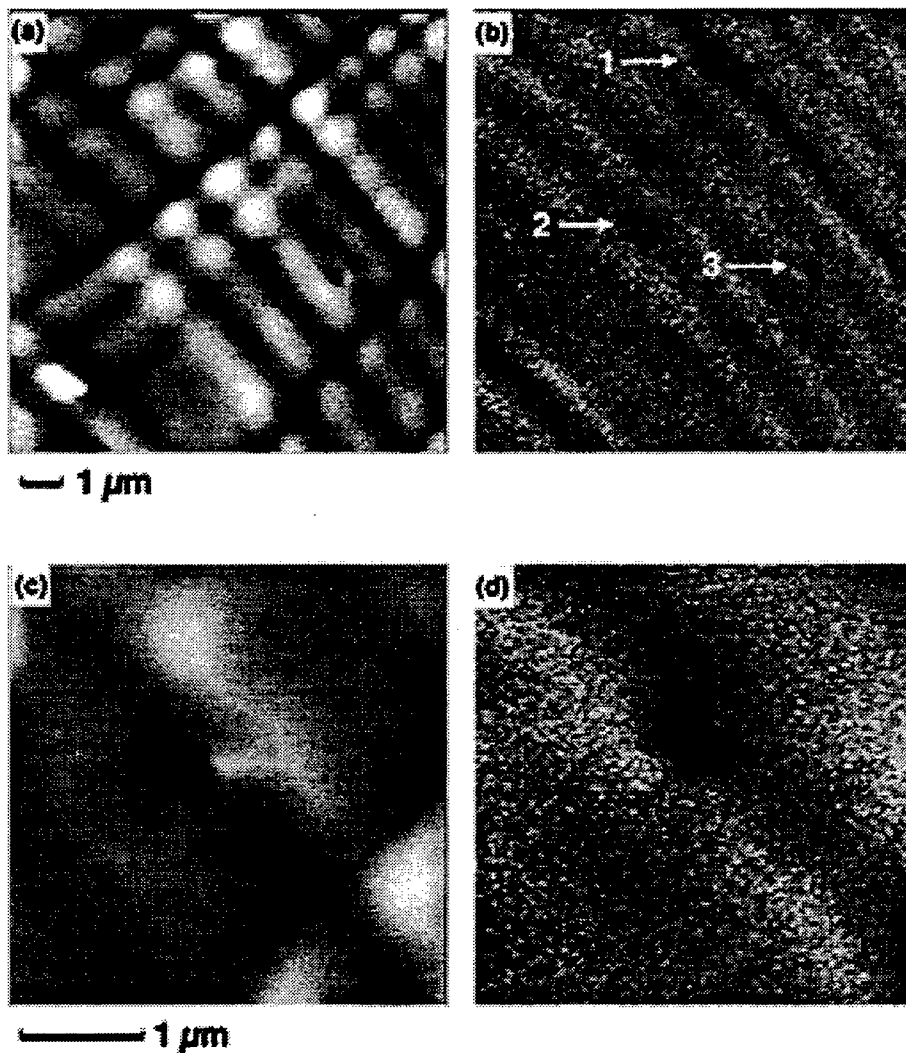


Fig. 1 (a) Topographic and (b) photovoltage images taken simultaneously of a $10.9 \mu\text{m} \times 10.9 \mu\text{m}$ area. (c) Topographic and (d) photovoltage images of a $3.6 \mu\text{m} \times 3.6 \mu\text{m}$ area near dislocation #1, indicated in (b). The full gray scale for (a) & (c) are 100 \AA and for (b) & (d) correspond to a 10 % change.

consist of a uniform $\text{Ge}_x\text{Si}_{1-x}$ cap layer of $\sim 1 \mu\text{m}$ on top of a compositionally graded layer on Si (100) substrates. They are completely relaxed, exhibiting bulk $\text{Ge}_x\text{Si}_{1-x}$ optical properties.[4,5] Typically, these graded films have threading dislocation densities $\leq 5 \times 10^6 \text{ cm}^{-2}$. This was determined with electron beam induced current (EBIC) [6] because the density is too low to be detected by transmission electron microscopy.

Fig. 1 shows side by side (a) topographic and (b) photovoltage images in a $10.9 \mu\text{m} \times 10.9 \mu\text{m}$ area taken simultaneously. In Fig. 1(b), three threading dislocations are easily identified by the three dark spots in the image. The corresponding topographic image (Fig. 1(a)) is dominated by the cross-hatch pattern that is due to the underlying misfit dislocation network characteristic of these graded samples. Nevertheless, three shallow depressions corresponding to the region of reduced photoresponse can be identified. These electrically-active shallow depressions are individual defects since their photoresponse is similar in both magnitude and spatial extent to their morphology. Fig. 1(c) and (d) show topography and photoresponse near threading dislocation #1 from Fig. 1(a) and (b) with higher magnification ($3.6 \mu\text{m} \times 3.6 \mu\text{m}$). It is now clear that these threading dislocations display a distinctive morphology as reported in Ref. [7] and act as carrier recombination centers. The average spatial extent of the photovoltage reduction for a threading dislocation is $(0.66 \pm 0.16) \mu\text{m}$, larger than that of the depressions, $(0.39 \pm 0.11) \mu\text{m}$. This is because the electrical activity length scale is determined by carrier diffusion length, which can be large in good materials, as well as aperture size. EBIC images of threading dislocations in these samples show dark spots with $\sim 1 \mu\text{m}$ diameters. The full scale of Fig. 1(b) and (d) represents a 10 % change about the average photovoltage. Typical reduction of threading dislocation photoresponse is measured to be 5 ~ 10 %. A few percent change is also what is observed in EBIC.

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Phonon Kinetics and Heat Removal From Low Dimensional Nanostructures

V. Mitin^(a), G. Paulavičius^(a), N. Bannov^(a), M. A. Stroscio^(b), and G. J. Iafrate^(b)

^(a)*Department of Electrical and Computer Engineering
Wayne State University*

^(b)*U.S. Army Research Office*

INTRODUCTION

Heat removal from electronic devices has always been a significant technical problem [1]. Miniaturization of electronic devices and high integration densities have made the heat removal problem fundamentally important. Along with the well-known problem of the overall overheating of a chip, which may result in deterioration of device operation, there occur additional problems due to nonequilibrium distribution of the emitted phonons. These new problems may not be solved by employing more efficient cooling systems because the excessive energy removal is not limited by the usual thermal conductivity of crystal lattice, but rather by processes which are substantially nonequilibrium and nonlinear.

For example, in the case of double heterostructure-based nanodevices the optical phonons generated by electrons cannot escape from the active regions due to their spatial confinement. This results in the growing their population and perhaps may even damage a device active region due to excitation of monochromatic lattice vibrations [2, 3]. In addition, the generation of a large number of nonequilibrium phonons by electrons results in a phonon distribution function which is far from equilibrium and significantly affects electron transport in nanostructures. On the other hand, there are conditions, when the energy supplied to the electron subsystem from the parallel to the quantum well electric field may be efficiently removed from electrons by fluxes of acoustic phonons in the direction (preferably) normal to the quantum well.

The heat transfer process in macrodevices represents diffusion of thermal energy and is govern by the thermoconductivity equation [4]. When characteristic sizes of heterostructure devices approach nanodimensions, the physical picture of heat removal undergoes a substantial modification; the thermal energy removal from nanodevices differs significantly from similar processes in relatively large devices [5]. Therefore, the heat removal from nanodevices requires thorough investigation employing an adequate mathematical description. The quantum kinetic equations for phonons and electrons provide adequate means for describing the heat removal from nanostructures in which both electron and phonon quantization are important.

EQUATIONS FOR HEAT REMOVAL

The problem at hand may be described by the kinetic equations for electron and phonon density matrices, $f_{k,k'}$ and $\sigma_{q,q'}$, where k and q denote sets of all quantum numbers for electrons and phonons, respectively. These equations have a similar structure and for the phonon density matrix, for example, the kinetic equation has the following form:

$$\partial\sigma_{q,q'}/\partial t + i(\omega_q - \omega_{q'})\sigma_{q,q'} = I_{PE} + I_R, \quad (1)$$

where I_{PE} is the phonon collision integral with electrons, I_R is the phonon relaxation term due to interactions other than electron scattering. The phonon-electron collision integral in the case of two-dimensional electron gas is given by the formula

$$I_{PE} = -2i \sum_{n,n',k_{\parallel}} \frac{|\langle n|\Gamma_{\mathbf{q}'}|n' \rangle|^2 [(1-f_{n,k_{\parallel}})f_{n',k_{\parallel}+\mathbf{q}_{\parallel}}\delta_{\mathbf{q},\mathbf{q}'} + (f_{n',k_{\parallel}+\mathbf{q}_{\parallel}} - f_{n,k_{\parallel}})\sigma_{\mathbf{q},\mathbf{q}'}]}{\varepsilon_{n,k_{\parallel}} - \varepsilon_{n',k_{\parallel}+\mathbf{q}_{\parallel}} + \omega_{\mathbf{q}} - i\lambda}$$

$$+ 2i \sum_{n,n',k_{\parallel}} \frac{|\langle n|\Gamma_{\mathbf{q}}|n' \rangle|^2 [(1-f_{n,k_{\parallel}})f_{n',k_{\parallel}+\mathbf{q}_{\parallel}}\delta_{\mathbf{q},\mathbf{q}'} + (f_{n',k_{\parallel}+\mathbf{q}_{\parallel}} - f_{n,k_{\parallel}})\sigma_{\mathbf{q},\mathbf{q}'}]}{\varepsilon_{n,k_{\parallel}} - \varepsilon_{n',k_{\parallel}+\mathbf{q}_{\parallel}} + \omega_{\mathbf{q}'} + i\lambda}.$$

The electron states are determined by subband number n and electron in-plane wave vectors \mathbf{k}_{\parallel} . The phonon states are determined by wave vectors $\mathbf{q} = (\mathbf{q}_{\parallel}, q_z)$, where \mathbf{q}_{\parallel} is the phonon in-plane wave vector, and axis z is normal to the quantum well. We restrict ourselves by the case of the acoustic phonons interacting with electrons through the deformation potential. The matrix elements in Eq. (1) are given by the formulae

$$|\langle n|\Gamma_{\mathbf{q}}|n' \rangle|^2 = \frac{E_a^2 q^2}{2\rho V_{pr} \omega(q)} \mathcal{G}(n', n, q_z),$$

where the overlap integral is determined by the formula

$$\mathcal{G}(n', n, q_z) = |\langle n' | \exp(iq_z z) | n \rangle|^2,$$

E_a is the deformation potential constant, V_{pr} is the principal volume, $\omega(q)$ is the phonon dispersion relation, and we use units, such that $\hbar = 1$.

Because our system is translationally invariant in the plane of the quantum well, we will use the following Wigner function

$$N_{\mathbf{q}_{\parallel}}(q_z, z) = \sum_{\Delta q_z} \sigma_{(\mathbf{q}_{\parallel}, q_z + 0.5\Delta q_z); (\mathbf{q}_{\parallel}, q_z - 0.5\Delta q_z)} \exp(i\Delta q_z z),$$

which satisfies the kinetic equation

$$\partial N_{\mathbf{q}_{\parallel}}(q_z, z) / \partial t + S_z(\mathbf{q}) \partial N_{\mathbf{q}_{\parallel}}(q_z, z) / \partial z = I_{PE} + I_R \quad (2)$$

In Eq. (2), $S_z(\mathbf{q})$ is the z -component of the phonon velocity, $S_{\mathbf{q}}$. At distances from quantum well d_z which are much larger than the inverse z -component of phonon wave vector, the collision integral I_{PE} is equal to zero. Thus, it may be taken into account through the boundary conditions for function $N_{\mathbf{q}_{\parallel}}(q_z, z)$:

$$S_z (N_{\mathbf{q}_{\parallel}}(q_z, +d_z) - N_{\mathbf{q}_{\parallel}}(q_z, -d_z)) = \sum_{n,n'} \int d\mathbf{k}_{\parallel} \frac{E_a^2 q^2}{2\pi\rho\omega(q)} \mathcal{G}(n', n, q_z) \times \quad (3)$$

$$[(1-f_{n,k_{\parallel}})f_{n',k_{\parallel}+\mathbf{q}_{\parallel}} + (f_{n',k_{\parallel}+\mathbf{q}_{\parallel}} - f_{n,k_{\parallel}})N_{\mathbf{q}_{\parallel}}(q_z, z)] \delta(\varepsilon_{n,k_{\parallel}} - \varepsilon_{n',k_{\parallel}+\mathbf{q}_{\parallel}} + \omega_{\mathbf{q}}).$$

In Eqs. (1), (2) and (3) we have assumed that the electron subsystem is homogeneous in the $x-y$ plane and is described by a diagonal density matrix (distribution function) $f_{n,\mathbf{k}_{\parallel}}$. For the function $f_{n,\mathbf{k}_{\parallel}}$ we have the kinetic equation which allows for a strong (in-plane) electric field and electron scattering by optical and acoustic phonons. We have used equilibrium distributions for phonons in the collision integrals of electrons with phonons. Our basic approach is very close to that, used in Ref. [6]. However,

in contrast to this paper, we have taken into account the effect of hot electrons on phonon emission and absorption; in addition, we have allowed for both spontaneous and stimulated phonon processes.

RADIATION PATTERNS

The kinetic equation for electrons and Eq. (2) have been solved by the Monte Carlo technique. We have obtained the electron distribution function $f_{n,k_{\parallel}}$ and the phonon Wigner function $N_{q_{\parallel}}(q_z, z)$. The primary objects of our interest in this report are the fluxes of energy carried by acoustic phonons. We will use the three densities of energy fluxes which are defined as follows

$$\mathcal{N}(\Omega, \omega) = \frac{L_x L_y}{8\pi^3 \Delta\Omega \Delta\omega} \int_{\Delta\Omega \Delta\omega} dq S_q \omega_q N_{q_{\parallel}}(q_z, z)$$

$\mathcal{N}_{\Omega}(\omega) = \int \mathcal{N}(\Omega, \omega) d\Omega$, $\mathcal{N}_{\omega}(\Omega) = \int \mathcal{N}(\Omega, \omega) d\omega$, where Ω is the solid angle, ω is the phonon frequency, $L_x L_y$ is the area of the quantum well. $\mathcal{N}(\Omega, \omega)$ is the energy flux due to emitted (and/or absorbed) acoustic phonons per unit energy range, per unit solid angle (dimension is 1/(s srad)). We restrict our consideration to a nondegenerate electron gas, then, in accordance with Eqs.(1) and (2), the densities of phonon energy fluxes are proportional to the electron concentration and we normalize these quantities per one electron.

We have calculated functions $\mathcal{N}(\Omega, \omega)$, $\mathcal{N}_{\Omega}(\omega)$, and $\mathcal{N}_{\omega}(\Omega)$ for a wide range of external parameters. To demonstrate the results we will use the following coordinate system: axis x is in the direction of the average electron velocity, axis z is perpendicular to the quantum well, axis y augments the axis $x - z$ to a right basis. We also use

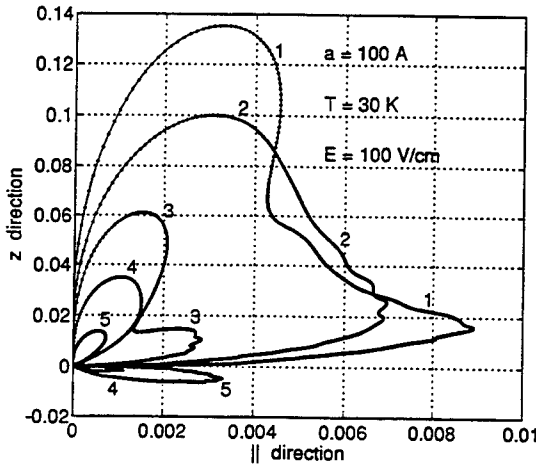


Figure 1. Radiation pattern of acoustic phonons, $\mathcal{N}_{\Omega}(\omega)$, in units $meV/ps\ srad\ electron$ for azimuthal angles $\varphi = 5^{\circ}(1)$, $55^{\circ}(2)$, $85^{\circ}(3)$, $115^{\circ}(4)$, $175^{\circ}(5)$; both emitted and absorbed phonons are counted. GaAs/AlAs quantum well of width 100\AA , electric field $100\ V/cm$, lattice temperature $T=30K$. Negative fluxes (below the abscissa) correspond to prevailing phonon absorption.

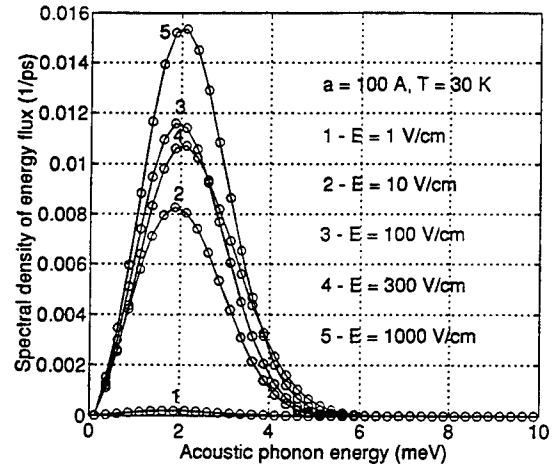


Figure 2. The spectra of the acoustic phonon energy flux, $\mathcal{N}_{\Omega}(\omega)$, for electric fields $1\ V/cm$, $10\ V/cm$, $100\ V/cm$, $300\ V/cm$, $1000\ V/cm$; both emitted and absorbed phonons are counted. GaAs/AlAs quantum well, $T = 30K$, $a = 100\text{\AA}$.

the conventional spherical angles θ and φ . Fig. 1 demonstrates a radiation pattern in the electric field $E=100$ V/cm. It is worth mentioning that the ordinate in Figs. 1 has a much larger scale than the abscissa. Therefore, acoustic phonons carry energy basically always in directions close to the z -direction. This results from the fact, that the z -component of the phonon wave vector is conserved only within an accuracy π/a (where a is the width of the quantum well) and this quantity is usually larger than the electron (and phonon) in-plane wave vector. At the same time, the flux of energy exactly along the z -direction is equal to zero. This is merely a consequence of the conservation laws. The in-plane distribution of the energy flux has a well pronounced dependence on angle φ and has higher values for small φ ($0 < \varphi < \pi$) because the electron distribution function is shifted in the x -direction. The large bend on the curve 1 in the Fig. 1 for $\varphi = 5^\circ$ for θ close to 60° is due to much larger scale in the z -direction on Fig. 1 and due to stretching the electron distribution function in x -direction.

The spectra of the acoustic phonon energy flux (Fig. 2) have maxima at the phonon energy of about 2 meV, what corresponds approximately to a phonon with wave vector $2\pi/a$. The magnitude of the maximum has nonmonotonical dependence on the electric field. When the electric field increases, the magnitude of the maximum increases too; however, it has a plateau at electric fields in the range 100 V/cm – 300 V/cm. This plateau is related to the changing the shape of the electron distribution function due to intense optical phonon emission, which results in the effective narrowing of this function in the x - y plane.

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Computation of Semiconductor Noise for Semiclassical Transport

Can E. Korman

Department of Electrical Engineering and Computer Science
The George Washington University, Washington, DC 20052

Isaak D. Mayergoyz

Electrical Engineering Department
University of Maryland, College Park, MD 20742

This paper describes semiconductor noise calculations when electron motion is described by semiclassical transport. The differential equations which model semiclassical transport of electrons in semiconductors can be interpreted as stochastic differential equations (SDE) driven by inhomogeneous randomly weighted Poisson processes. The Poisson process models the scattering of electrons in momentum space. The solution of these stochastic differential equations is a Markov process and is generally characterized by a transition probability density function (p.d.f.). In the theory of SDE, it is well known that this transition probability density satisfies the forward Kolmogorov-Feller equation. In the case of semiclassical transport this equation is identical to the nondegenerate Boltzmann transport equation (BTE). Based on this formalism, the autocovariance function of current fluctuations are computed from the transient solutions of the BTE. The distinguishing feature of this approach is that current fluctuations due to scattering are directly accounted for in the model without the addition of the "Langevin source term." Consequently, this approach directly connects the noise characteristics with the characteristics of the scattering mechanisms of the semiclassical transport model. In this sense, our framework is similar to one used in Monte Carlo simulations of noise, [2]. However, this approach greatly relies on the interpretation of the semiclassical transport model as SDEs and the interpretation of the BTE as the corresponding Kolmogorov-Feller equation of the stochastic process. In the practical case of ohmic contacts, an explicit expression for the current noise spectral density is derived in terms of the total scattering rate

and the steady-state distribution function. Furthermore, as an illustrative example, numerical results on the spectral density of current fluctuations in bulk silicon due to acoustic and optical phonon scattering are presented.

According to semiclassical transport theory, an electron in a semiconductor drifts under the influence of electric and magnetic fields and experiences occasional random jumps in its momentum due to the scattering mechanisms in the crystal, such as acoustic and optical phonons, ionized impurities, etc. When the effects of magnetic fields are neglected, the motion of an electron is described by the following stochastic differential equations:

$$\begin{aligned}\frac{d\vec{x}}{dt} &= \vec{v}(\vec{k}) = \frac{1}{\hbar} \nabla_{\vec{k}} \epsilon(\vec{k}) \\ \hbar \frac{d\vec{k}}{dt} &= -q\vec{E} + \vec{F}_r, \quad \vec{F}_r = \sum_i \hbar \vec{u}_i \delta(t - t_i)\end{aligned}\quad (1)$$

where \vec{x} , \vec{v} and \vec{k} are the electron position, drift velocity and wave vector, respectively, \vec{E} is the electric field, $\epsilon(\vec{k})$ is the energy-wave vector relationship in the given energy band and \vec{F}_r is the random impulse force on the electron due to scattering. The random force is characterized by the *transition rate* $W(\vec{k}, \vec{k}')$ and the *scattering rate* is $\lambda(\vec{k})$ is defined by

$$\lambda(\vec{k}) = \int W(\vec{k}, \vec{k}') d\vec{k}'.$$

These are the same equations which are used to simulate the electron motion in Monte Carlo simulations, [2].

The equations above define a compound Poisson process which is discontinuous in \vec{k} -space and is a Markov process. In stochastic differential equation theory, such a process is usually characterized by a *transition probability density function* ρ , which satisfies the Kolmogorov-Feller forward equation, (for instance, see [3]). As a result, the corresponding equation for the above process is derived to be

$$\frac{\partial \rho}{\partial \tau}(\vec{x}_0, \vec{k}_0, t; \vec{x}, \vec{k}, t + \tau) + \vec{v}(\vec{k}) \cdot \nabla_{\vec{x}} \rho - \frac{q}{\hbar} \vec{E}(\vec{x}, t + \tau) \cdot \nabla_{\vec{k}} \rho =$$

$$= \int \rho(\vec{x}_0, \vec{k}_0, t; \vec{x}, \vec{k}', t + \tau) W(\vec{k}', \vec{k}) d\vec{k}' - \lambda(\vec{k})\rho, \quad (2)$$

where \vec{x}_0, \vec{k}_0 are the initial electron position and wave vector at some time t . When integrated over the initial conditions (or backward coordinates) one obtains the well known Boltzmann transport equation.

In general, noise in semiconductors is characterized by the spectral density of current fluctuations. The spectral density is defined as the Fourier transform of the autocovariance function. The autocovariance function of any random process can be found from the joint probability density function of the random process. For a scalar and stationary Markov process we need the transition and stationary probability density functions in order to compute the autocovariance function. Here we consider the problem of a semiconductor under steady-state conditions such that an average electric field and current density are established. Under such conditions, it is clear that the electron distribution function is given by the stationary solution of Eqn. (2), $f_\infty(\vec{x}, \vec{k})$. The transition probability density function is the transient solution of Eq. (2):

$$\begin{aligned} \frac{\partial \rho}{\partial \tau}(\vec{x}, \vec{k}', 0; \vec{x}, \vec{k}, \tau) + \vec{v}(\vec{k}) \cdot \nabla_{\vec{x}} \rho - \frac{q}{\hbar} \vec{E}(\vec{x}) \cdot \nabla_{\vec{k}} \rho = \\ = \int \rho(\vec{x}, \vec{k}', 0; \vec{x}, \vec{k}'', \tau) W(\vec{k}'', \vec{k}) d\vec{k}'' - \lambda(\vec{k})\rho, \end{aligned} \quad (3)$$

subject to the following initial condition:

$$\rho(\vec{x}, \vec{k}', 0; \vec{x}, \vec{k}, \tau) \Big|_{\tau=0} = \delta(\vec{k} - \vec{k}') \quad (4)$$

As a result, one observes that the autocovariance matrix for the fluctuations in the electron wave vector can be computed directly from the transient and stationary solutions of the Boltzmann transport equation. It is important to note that the only information which is needed is the electron scattering rates of semiclassical transport theory. Since this information is included in the corresponding Kolmogorov-Feller equation (the BTE, Eq. (2)), there is no need to include additional random fluctuations into the system. This is in contrast to the usually held notion that the BTE

reflects the average behavior of the system and that a stochastic field term, referred to as the “Langevin source term”, must be added in order to account for the random fluctuations in the current, [4]. In [5], it is shown that the autocovariance matrix of the electron wave vector can be computed from the transient solution of the BTE subject to an initial condition in terms of the stationary electron distribution and the average electron wave vector. Based on this approach, a closed form expression is derived for the noise spectral density at highly doped ohmic contacts in terms of the scattering rate and the steady-state electron distribution function. As an illustrative example, numerical results are presented for the spectral density of current fluctuations due to elastic acoustic and optical phonon scattering in silicon.

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The Influence of Hydrodynamic Transport Models on the Prediction of Submicron Semiconductor Device Characteristics

Mei-Kei Jeong, Ting-wei Tang and Gang Fang

Department of Electrical and Computer Engineering
University of Massachusetts
Amherst, MA 01003-5110

Introduction

In recent years, the hydrodynamic (HD) model has been extensively used in the simulation of submicron semiconductor devices because of its capability for predicting nonstationary and nonlocal phenomena occurring in these devices. However, there exist varieties of HD model differing primarily in modeling of transport coefficients (mobility, energy relaxation time, thermal conductivity, etc.) Depending on which transport model is used, the simulation result can be quite different. The purpose of this investigation is to compare how different transport models predict different device characteristics of submicron semiconductor devices.

Physical Transport Models

We have recently developed a two-dimensional semiconductor device simulator [1] based on the improved HD model[2]. The conservation equations for momentum and energy flux used in the simulation are, respectively,

$$qn\vec{V} = n\mu^* [\vec{F} - \hat{U} \cdot \nabla n - (1 - \lambda_p)\nabla \cdot \hat{U}], \quad (1)$$

$$\begin{aligned} n\vec{S} = & \frac{\mu_s^*}{\mu^*} n(W\hat{I} + \hat{U}) \cdot \vec{V} + \frac{\mu_s^*}{q} [(W\hat{I} + \hat{U}) \cdot \hat{U} - \hat{R}] \cdot \nabla n \\ & - \frac{\mu_s^*}{q} n [(1 - \lambda_{ep})\nabla \cdot \hat{R} - (1 - \lambda_p)(W\hat{I} + \hat{U}) \cdot (\nabla \cdot \hat{U})], \end{aligned} \quad (2)$$

where $\vec{V} = \langle \vec{v} \rangle$, $\vec{F} = -q\vec{E}$, $\hat{U} = \langle \vec{v}\hbar\vec{k} \rangle$, $W = \langle \epsilon \rangle$, $\vec{S} = \langle \epsilon\vec{v} \rangle$, $\hat{R} = \langle \vec{v}\epsilon\hbar\vec{k} \rangle$, \hat{I} is the unity tensor, λ_p and λ_{ep} are dimensionless parameters. By suitably choosing the transport parameters λ_p , λ_{ep} and closure relations, this generalized HD transport equation can be reduced to most HD transport models reported in the literature [3]. For instance, with the choice of $W = \frac{3}{2}k_B T_e$, $U = \frac{2}{3}W$, $R = \frac{10}{9}W^2$, $\mu_s^* = \mu^*$ and $\lambda_p = \lambda_{ep} = 0$, the above equations reduce to the simplified HD model. The conventional Fourier heat law and the Wiedemann-Franz law for thermal conductivity corresponds to choosing $W = \frac{3}{2}k_B T_e$, $U = \frac{2}{3}W$, $R = \frac{10}{9}W^2$, $\mu_s^* = 0.8\mu^*$ and $\lambda_p = 2\lambda_{ep}$. Stratton's energy balance formulation is equivalent to choosing $\lambda_p = -\frac{W}{\mu^*} \frac{\partial \mu^*}{\partial W}$ [4]. Thus, using our generalized HD solver, we can study the influence of all different transport models on the simulation result.

Numerical Implementation

The system of the generalized HD equations is discretized using the optimum artificial diffusivity approach[5]. The Jacobian matrix is assembled either by a numerical differentiation or by the analytical method. The state-of-the-art linear solver incorporating LU-decomposition with an appropriate reordering scheme and the conjugate gradient-like iterative method is used to solve the resulting linear equations. In order to speedup the simulation, parallel computing using a local network of workstations has also been implemented.

Simulation Results

Previously, we used this generalized HD solver to study the effect of different hydrodynamic transport models on the simulated characteristics of deep submicron SOI-MOSFET's[6]. There, we found that different transport parameters (e.g., λ_p and λ_{ep}) yield different output characteristics. In this study, we investigate the influence of HD models on the prediction of high frequency performance of $\text{Si}_{1-x}\text{Ge}_x$ HBT's. Fig.1 shows the doping profile of a simulated SiGe HBT. Table 1 lists different choices of transport parameters corresponding to different transport models appearing in the literature. The so-called "energy transport(ET)" model advanced by Chen et.al.[7] is basically similar to Stratton's energy balance model[4]. Lee and Tang's model [8] follows an idea originally proposed by Hansch & Miura-Mattausch[9]. A recent model proposed by Tang et.al.[2] is based on Monte Carlo data calibration. The model designated as "ET-B" is a special case of the ET-model using a Baccarani-type mobility. Finally, "SHDE" refers to the conventional simplified HD model in which the collision moments are modeled by the relaxation time approximation using the homogeneous Monte Carlo data. Fig.2 shows DC current gains predicted by the different HD models. The variation is seen as much as 200% in the extreme case. Fig.3 shows a similar variation in the prediction of unity current gain cutoff frequency, f_T , by the different HD models. Here, the range of variation is about 20%. The physical origin of these variations can be traced to different modeling of the thermal diffusion component of current density and the energy-dependent mobility. The f_T is highly dependent upon the competing effects between the thermal diffusion and the nonlocal phenomena related to the energy relaxation. Our simulation results indicate that some kind of experimental verification for the proper choice of HD model is urgently called for.

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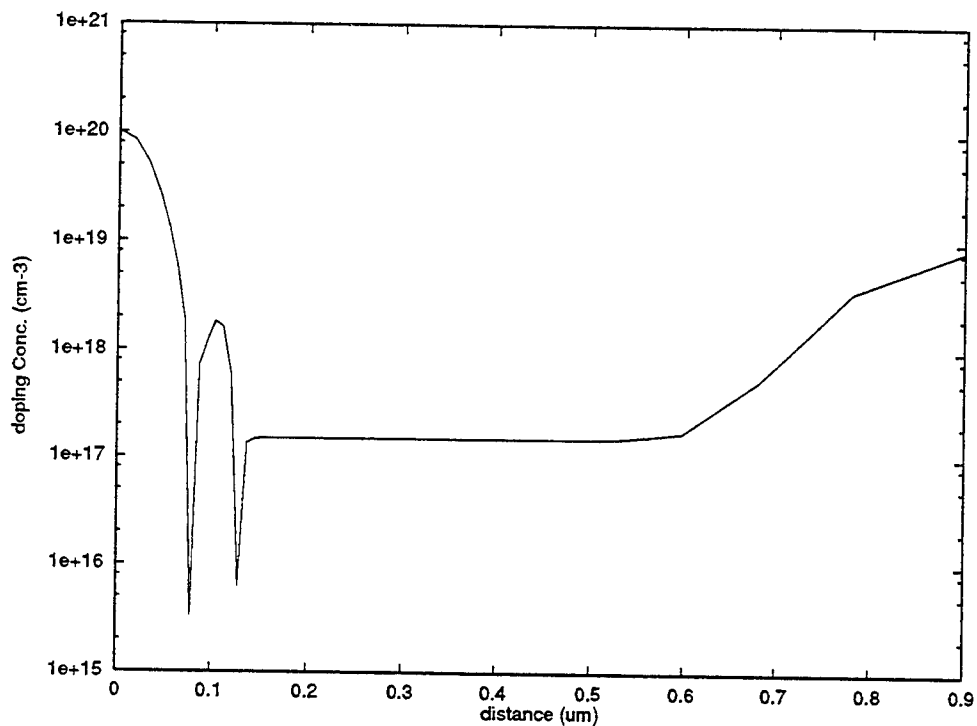


Figure 1: Doping profile

Chen (ET)	$\lambda_p = \frac{\mu^* W^*}{q \tau_\epsilon v^2_{sat}}$	$\lambda_{\epsilon p} = 0.5 \lambda_p$
Lee	$\lambda_p = \frac{3 \Delta \mu^* W^*}{2 \delta q \tau_\epsilon v^2_{sat}}$	$\lambda_{\epsilon p} = 0.5 \lambda_p$
Tang	$\lambda_p = 0.15$, if $\nabla \cdot \hat{U} > 0$; $\lambda_p = 0.5$, if $\nabla \cdot \hat{U} < 0$	$\lambda_{\epsilon p} = 0.5 \lambda_p$
ET-B	$\lambda_p = 1.0$	$\lambda_{\epsilon p} = 0.5 \lambda_p$
SHDE	$\lambda_p = 0.0$	$\lambda_{\epsilon p} = 0.5 \lambda_p$

Table 1: Models for λ_p and $\lambda_{\epsilon p}$

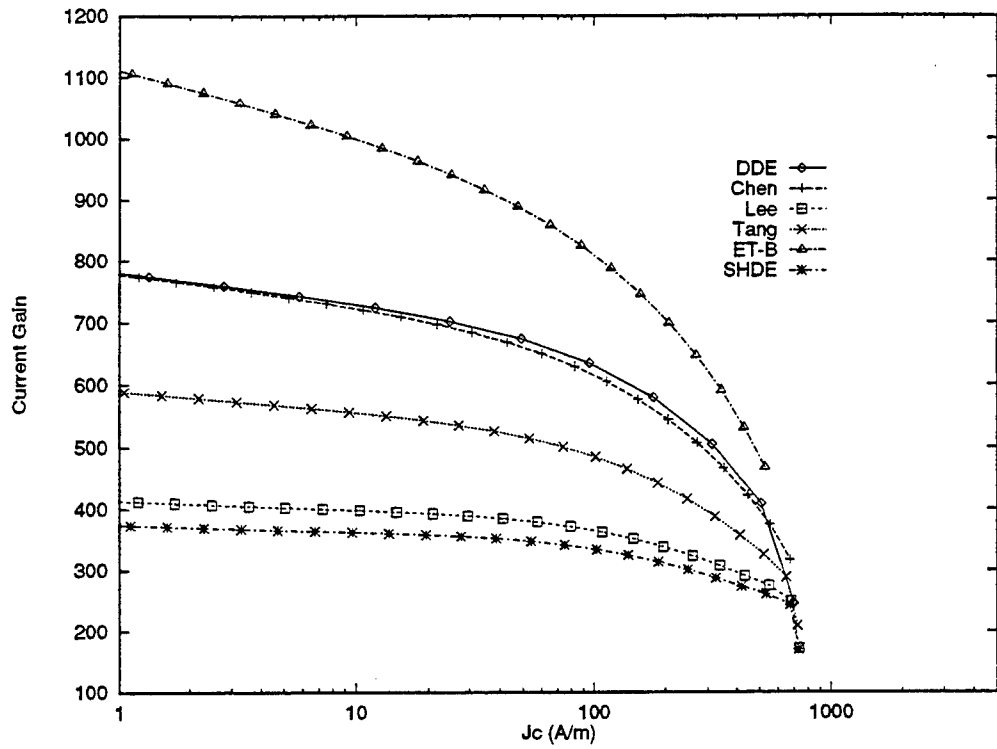


Figure 2: DC current gain

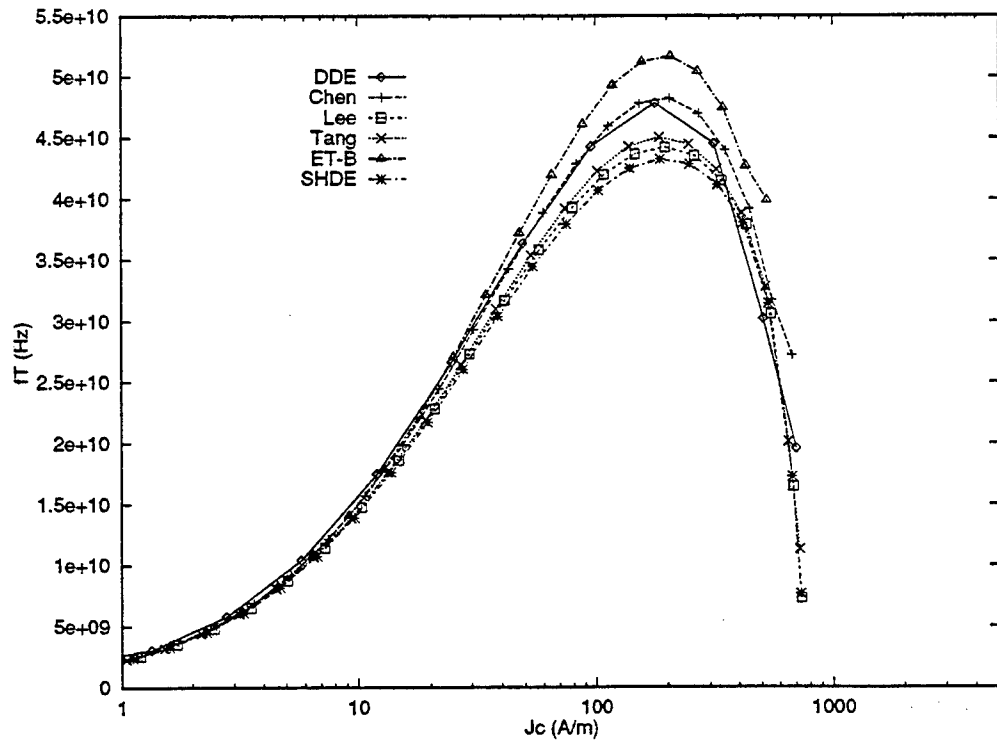


Figure 3: Unity current gain cut-off frequency, f_T

Electrothermal Effects in Semiconductor Power Devices Analyzed by Numerical Simulation and Internal Laser Deflection Measurement

R. Thalhammer, G. Deboy[†], W. Keilitz, U. Müller, G. Wachutka

Chair for Physics of Electrotechnology, Technical University of Munich

[†]Corporate Research and Development, Siemens AG, Munich

1 Introduction

As increasingly higher blocking voltage of some thousand Volts and higher forward current of some hundred to thousand Amps are achieved in modern power semiconductor devices, electrothermal self-heating and heat dissipation has become a crucial problem in the optimization of the device operation, especially during transient switching. For the detailed experimental analysis of the local internal distribution of temperature and carrier flow, a new contactless probing technique, the *internal infrared laser deflection method* [1], has been introduced. On the basis of accurate numerical simulation, a correct interpretation and understanding of the complicated measurement signal can be obtained. In addition, the experimental results allow us to validate and calibrate the physical models for electrothermal coupling with an accuracy such that predictive modeling of the device operation and, thereby, computer-aided design optimization becomes practicable.

2 Numerical Modeling

The electrical behavior of the device is governed by Poisson's equation

$$\vec{\nabla} \cdot (\epsilon \vec{\nabla} \Psi) = q (n - p + N_A^- - N_D^+)$$

and the particle balances for the mobile charge carriers (electrons and holes)

$$\frac{\partial n}{\partial t} - \frac{1}{q} \vec{\nabla} \cdot \vec{J}_n = -R \quad \text{and} \quad \frac{\partial p}{\partial t} + \frac{1}{q} \vec{\nabla} \cdot \vec{J}_p = -R$$

The current densities are driven by the gradients of the quasi-Fermi potentials (i.e., electrical drift and chemical diffusion) and the temperature gradient (thermal diffusion):

$$\vec{J}_n = -q \mu_n n (\vec{\nabla} \Phi_n + P_n \vec{\nabla} T) \quad \text{and} \quad \vec{J}_p = -q \mu_p p (\vec{\nabla} \Phi_p + P_p \vec{\nabla} T)$$

Using the principles of irreversible thermodynamics, heat generation and conduction in a semiconductor can be treated consistently with the drift-diffusion model [2], yielding the following heat flow equation

$$c \frac{\partial T}{\partial t} - \vec{\nabla} \cdot (\kappa \vec{\nabla} T) = H$$

with the heat generation rate

$$H = -\vec{\nabla} \cdot [(\Phi_n + P_n T) \vec{J}_n + (\Phi_p + P_p T) \vec{J}_p] + q \left(\Phi_n - T \frac{\partial \Phi_n}{\partial T} \right) \frac{\partial n}{\partial t} - q \left(\Phi_p - T \frac{\partial \Phi_p}{\partial T} \right) \frac{\partial p}{\partial t}$$

Evaluating the divergence operator in the above equation gives four terms contributing to the total heat generation. First, the Joule heat of holes and electrons, $\frac{J_p^2}{qp\mu_p}$ and $\frac{J_n^2}{qn\mu_n}$, respectively. Second, the recombination heat $qR(\Phi_p + TP_p - \Phi_n - TP_n)$. Third, the Peltier/Thomson heat $-\vec{J}_p T \vec{\nabla} P_p - \vec{J}_n T \vec{\nabla} P_n$ arising from the spatial variation of the absolute thermoelectric powers P_p and P_n , and fourth, an additional positive or negative heat generation rate caused by transient variations of the carrier densities. The latter contribution can be neglected in many practical situations. The numerical results presented in this work were calculated using the general purpose device simulator DESSIS^{ISE}, with the electrothermal model implemented as sketched above.

3 Measurement Principle

Absolute carrier concentration and temperature gradients have been determined by internal infrared laser deflection. This recently presented experimental technique [1] exploits the dependence of the refractive index of silicon on carrier concentration and temperature. A basic sketch of the experimental setup is shown in Fig. 1.

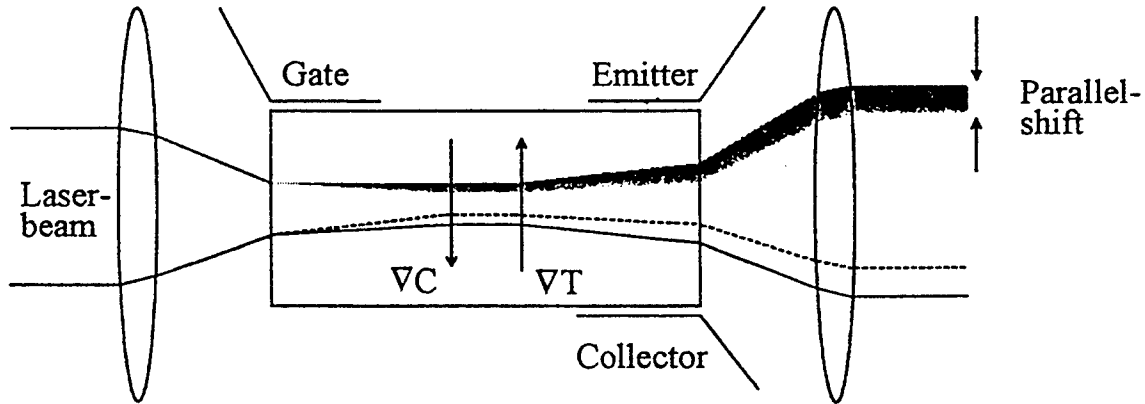


Figure 1: Sketch of the experimental setup

Under transient switching conditions, both the injection (or removal) of carriers and a local change in temperature cause a local modulation of the refractive index which, in turn, deflects the focused laser beam. The internal deflection is transformed into a parallel shift by a long distance objective. From the parallel shift and the total intensity detected by a four quadrant photodiode we can extract carrier concentration and temperature gradient. Both contributions to the measured signal can be separated due to their widely differing time constants. Vertical profiles of carrier density and temperature are obtained by shifting the device along its vertical axis.

4 Results

4.1 Carrier densities

Fig. 2 shows the carrier concentration of a high voltage pin diode at a current density of $150 \frac{A}{cm^2}$. The measured carrier concentration profile in the weakly doped drift region provides valuable information about emitter efficiencies and carrier lifetimes, which is needed for the calibration of the physical model parameters.

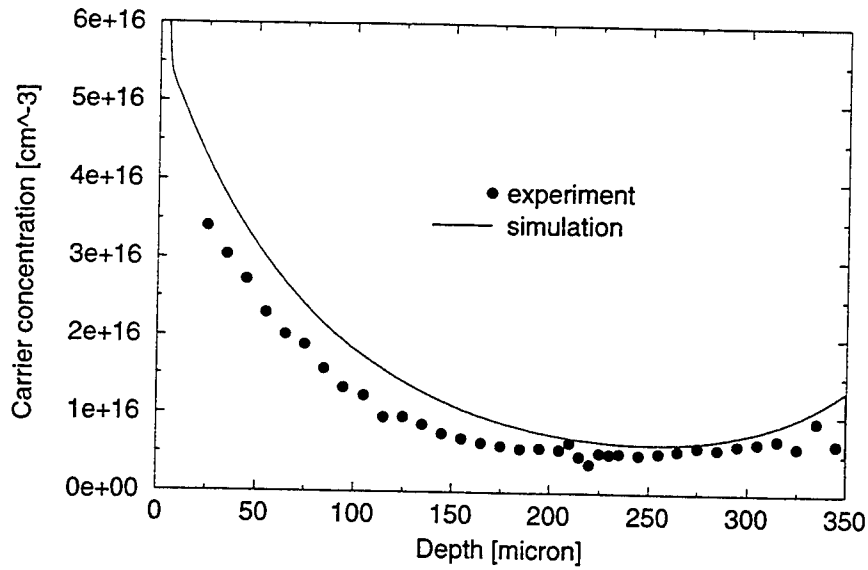


Figure 2: Carrier distribution of a pin diode at a current density of $150 \frac{A}{cm^2}$.

4.2 Thermal properties

Fig. 3 shows the temperature distribution in the interior of the pin diode after turn-on. Our simulation reveals that the local maximum in the bulk of the device is caused by Joule heating of electrons and holes in the drift region, whereas the temperature increase at the anode side arises from recombination heat at the p^+n^- -junction.

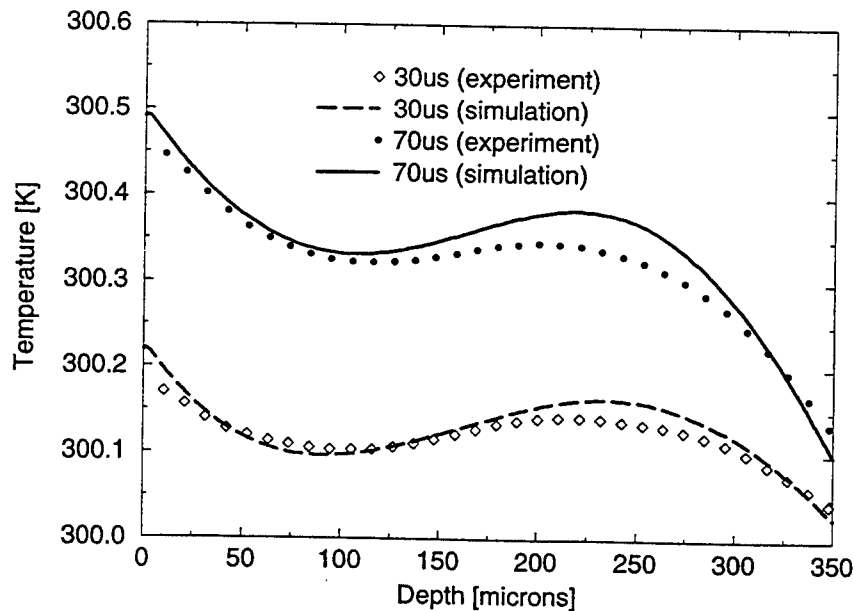


Figure 3: Temperature profile after turn-on of a pin diode

Another example is shown in Fig. 4. Joule heating of holes and electrons in the channel region and in the bulk of the IGBT causes the most significant effect on the temperature profile. An additional contribution originates from Peltier heating at the p^+ -emitter on the rear side, which is negative at the p^+n^- -junction but positive at the p^+ /metal-junction. Although the present version of the simulator DESSIS^{ISE} does not allow for the surface Peltier effect at the p^+ /metal-junction (as a consequence of simplified thermal boundary

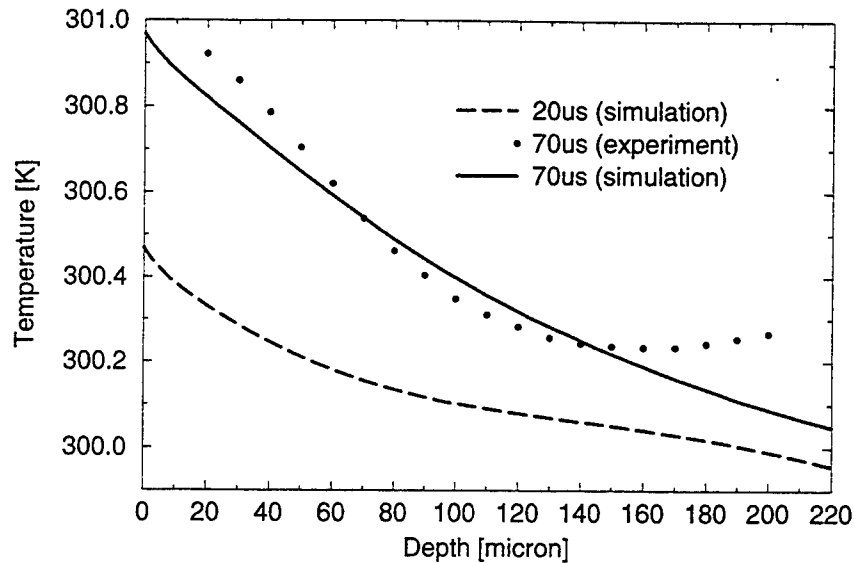


Figure 4: Temperature profile in the bulk of a 1200 V IGBT after turn-on

conditions), it can be calculated directly from the thermoelectric powers. The net Peltier heating of $15 \frac{W}{cm^2}$ is comparably small in view of the total Joule heating of $280 \frac{W}{cm^2}$, but sufficient to cause the temperature rise at the rear side.

5 Conclusions

Carrier concentration and temperature gradients in power semiconductor devices can be measured using the recently developed method of internal IR laser deflection. Comparison of experimental data and simulation provides both a detailed interpretation of the measured signal and the validation of the physical models. It shows that the large heat dissipation rate in power devices requires careful and accurate thermal modeling. The most significant contribution to the total heat dissipation originates from Joule heating and recombination heat. Although the additional contribution introduced by the Peltier effect is relatively small, it can be detected by measuring the temperature profile.

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TEMPERATURE DEPENDENCE OF EARLY VOLTAGE IN HBTs: THEORY, SIMULATIONS, AND EXPERIMENT

Clifford M. Krowne

Code 6850.3, Microwave Technology Branch, Electronics Science & Technology Division,
Naval Research Laboratory, Washington, DC 20375-5347

Kiki Ikossi-Anastasiou and Elias Kougiianos

Electrical & Computer Engineering, Louisiana State University,
Baton Rouge, Louisiana 70803-5901

I. Introduction

The Early voltage is a characteristic quantity that can describe the output conductance and the load drive capability of bipolar transistors in an IC environment. It is therefore desirable to have a representative Early voltage model of today's advanced devices. Here we provide an extension of the thermionic emission expression for the Early voltage V_A for heterojunction bipolar transistors (HBTs) including quantum mechanical tunneling and base recombination effects. The theoretical model is based on a single flux treatment of the carrier transport invoking the concise notation of scattering matrices. V_A is numerically evaluated under the WKB quantum mechanical approximation for triangular and parabolic barriers. The temperature dependence of the Early voltage is simulated numerically and compared to earlier theoretical V_A predictions and actual experimental results of V_A in heterojunction bipolar transistors. This is the most extensive model yet prepared and includes all the relevant temperature dependences of the material parameters.

II. Theory

Early voltage V_A is defined as that voltage determined from an asymptotic extrapolation backwards on a current-voltage (I-V) characteristic of a transistor biased in the active region. In the linear slope approximation we are implicitly using in this Early voltage construction, the slope S_{JV} is given by,

$$S_{JV} = \left. \frac{\partial J_c}{\partial V_{ce}} \right|_{V_{be}} = J_c (V_A + V_{ce}) \quad (1) \quad \Rightarrow \quad V_{Ac} = J_c / S_{JV} - V_{ce} \quad (2)$$

This graphically determined Early voltage we notice is corrected for the collector-emitter voltage V_{ce} at which the asymptote is identified. We define this graphically corrected early voltage as V_{Ac} . For cases where the slope S_{JV} is gentle, the ratio in (2) can be very substantial, and V_A approximated by

$$V_{Ac} \approx J_c / S_{JV} \quad (3) \quad \Rightarrow \quad V_A = J_c / S_{JV} = J_c / \left[\left. \frac{\partial J_c}{\partial V_{ce}} \right|_{V_{be}} \right] \quad (4)$$

giving the slope determined Early voltage in (4).

Early voltage may be evaluated from (4) using the expression for the base current dependent collector flux $F_{cn} = -J_c/q = a_3 - b_3$ which includes quantum mechanical tunneling. a_3 and b_3 are the outgoing and incoming flux at the collector end of the heterojunction bipolar transistor, respectively. The electron flux is [1]:

$$F_{cn} = M_1 F_{cn1} - M_1 F_{cna1} - M_1 \phi_2 \delta_B b_3 \quad (5)$$

The first term in (40) represents the flux contribution without the injection of electrons from the collector (i.e., $b_3 = 0$), the second term F_{cna1} (excluding the M_1 prefactor) the contribution from collector electron injection without base current recombination, and the third term the contribution from the combined collector injection and base recombination currents. F_{cn1} is the flux without either the injection or base recombination currents. Putting this into (4) gives

$$V_A^{CE} = F_{cn} / \left[\left. \frac{\partial F_{cn}}{\partial V_{CE}} \right|_{V_{be}} \right] = M_1 F_{cn1} \left[1 - \frac{\alpha_3}{\alpha_1} b_3 - \phi_2 \delta_B b_3 / (t_B \alpha_1) \right] \times$$

$$\left\{ \left(M_1 \frac{\partial F_{cn1}}{\partial V_{CE}} \Big|_{V_{be}} + F_{cn1} \frac{\partial M_1}{\partial V_{CE}} \Big|_{V_{be}} \right) \left[1 - \frac{\alpha_3}{\alpha_1} b_3 - \phi_2 \delta_B b_3 / (t_B \alpha_1) \right] + M_1 F_{cn1} \left(- \frac{b_3}{\alpha_1} \frac{\partial(\phi_2 / t_B)}{\partial V_{CE}} \Big|_{V_{be}} \delta_B \right) \right\}^{-1} \quad (6)$$

III. Numerical Results

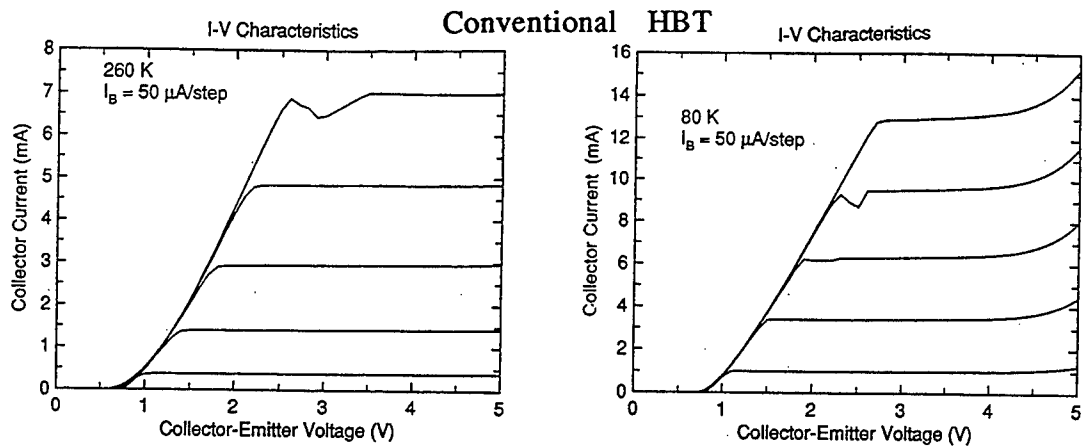
Fig. 1 shows the experimental I-V characteristics [2] as a function of temperature and the calculated V_A for graded emitter-base heterointerface AlGaAs/GaAs HBTs for base width (a) $W_B = 1000\text{\AA}$ and abrupt narrow base (b) $W_B = 50\text{\AA}$. Numerical results for V_A using a classical (Fig. 2) and Roulston/Liou [3], [4] (Fig. 3) formulations for different base widths yields curves (a) and (b). Figs. 4 (a) and (b) give the results using a Tanaka/Lundstrom formulation [5], [6], for abrupt HBTs with $W_B = 1000\text{\AA}$ and 50\AA , with conduction band discontinuities: curves (a) - (e) $\Delta E_C = 230, 100, 20, 10$ meV, and 1 meV. Figs 5(a) and (b) give numerical results for Early voltage including quantum mechanical tunneling effects for abrupt HBTs with $W_B = 1000\text{\AA}$ and 50\AA , with conduction band discontinuities: curves (a), (c), (e), (f) with $\Delta E_C = 230, 100, 20, 10$ meV using a triangular barrier approximation; and (b), (d), (f) with $\Delta E_C = 230, 100, 20$ meV using a parabolic barrier approximation. Finally, Figs. 6(a) and (b) show the numerical results for Early voltage including quantum mechanical tunneling and base recombination effects for abrupt HBTs with $W_B = 1000\text{\AA}$ and 50\AA , with conduction band discontinuity given by the same cases as in Fig. 5.

IV. Conclusions

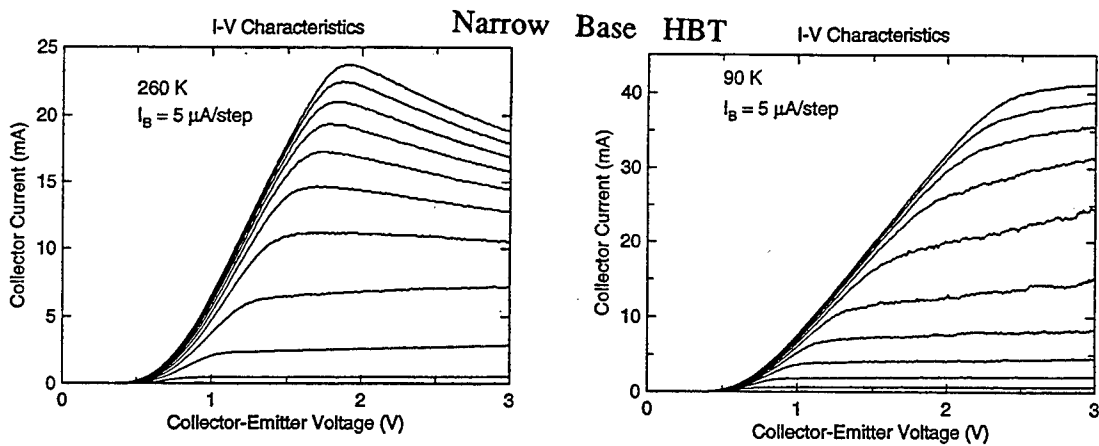
Good qualitative agreement between the classical extension of the Roulston/Liou model and experiment is observed for the conventional graded emitter-base HBT Early voltage temperature dependence. For abrupt HBTs, the Tanaka-Lundstrom theory predicts the correct temperature dependence for the Early voltage but overestimates the experimentally observed values of the Early voltage. The extended theory presented in this work results in better agreement with the experimental results for the narrow base HBT. The work performed here indicates that the effective base-emitter tunneling barrier for the examined HBT structures might be significantly smaller than what is expected from classical considerations. The extended theory offers a more accurate calculation for the Early voltage and correctly predicts the observed temperature performance of an abrupt heterojunction narrow base HBT. This paper has demonstrated that it is feasible using our new approach to include both quantum mechanical tunneling and base recombination in the determination of the Early effect in HBTs.

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(a)



(b)

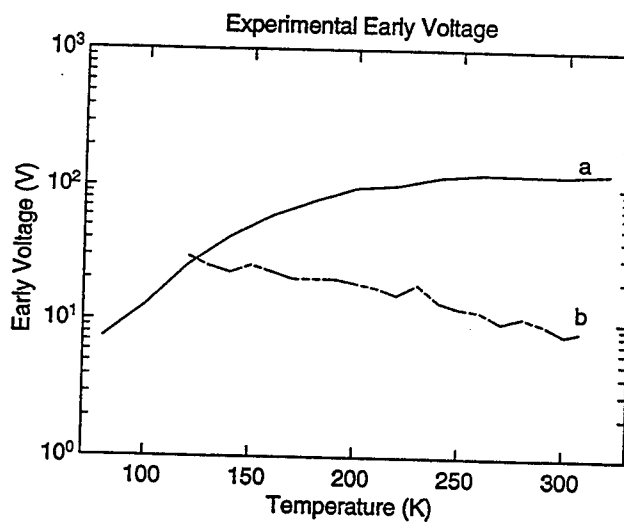


Fig. 1

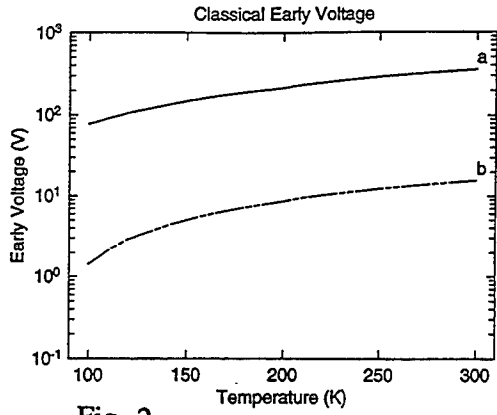


Fig. 2

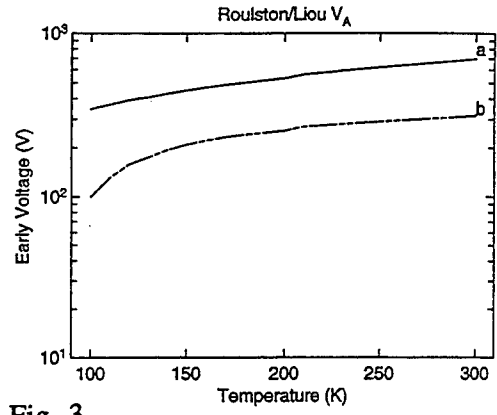


Fig. 3

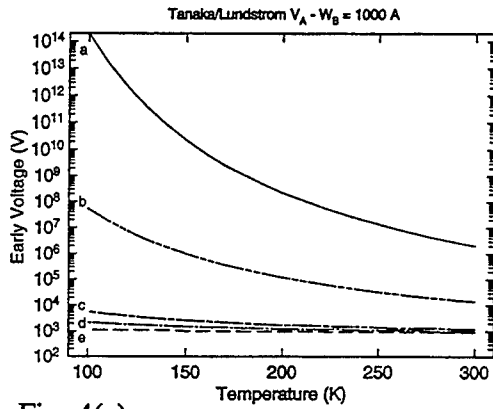


Fig. 4(a)

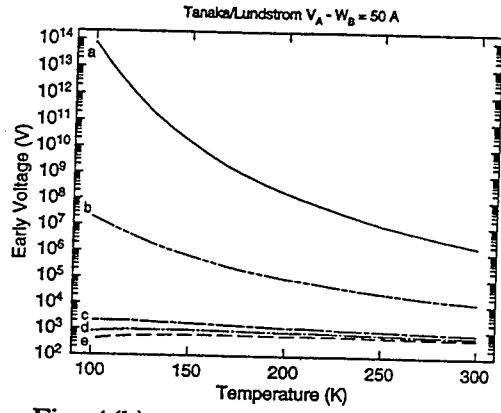


Fig. 4(b)

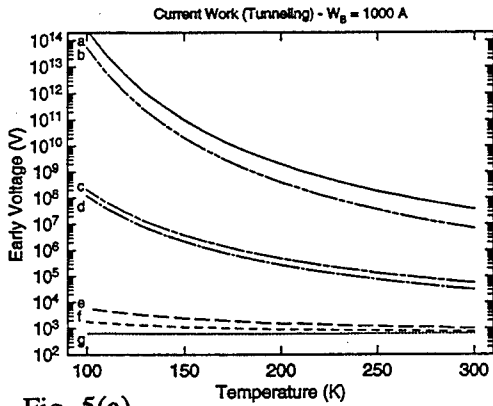


Fig. 5(a)

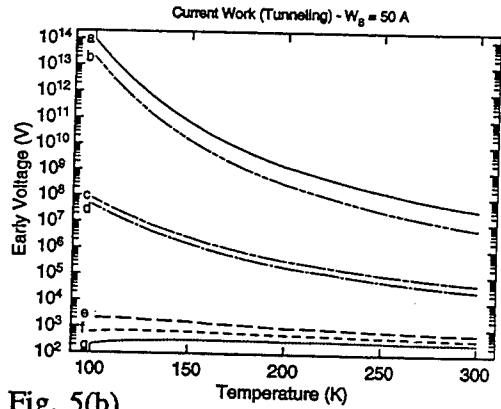


Fig. 5(b)

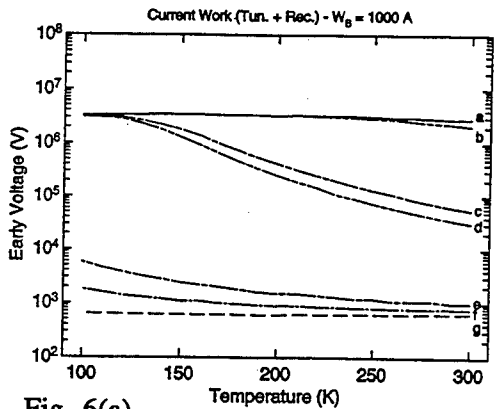


Fig. 6(a)

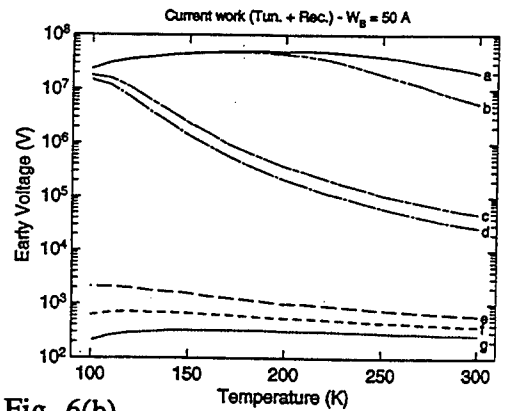


Fig. 6(b)

Optimization of Light Emitting Diodes Based on Bipolar Double-Barrier Resonant-Tunneling Structures

K. A. Chao

Department of Physics, University of Trondheim-NTH, N-7034 Trondheim, Norway

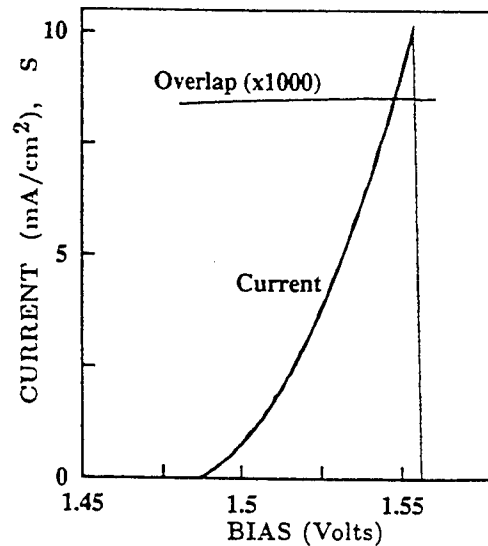
We assume a bipolar DBRT structure with perfect interfaces, and restrict ourselves to direct bandgap materials with negligible lattice mismatch. As an example, the structure of the DBRT sample used in our calculation is specified in the Table. To take into account the diffusion of impurities into the spacers, we introduce two 10 Å wide Error-function tails of impurity concentration.

We include in our model only the electron band and the heavy hole band, and solve the Schrödinger equation within the effective mass approximation. To obtain the self-consistent solution, we have to solve eight coupled equations: the Schrödinger equation for electrons, the Schrödinger equation for heavy holes, the Poisson equation for the potential, the electron current from the emitter to the well, the electron current from the well to the collector, the electron density in the well, the hole current from the emitter to the well, the hole current from the well to the collector, the hole density in the well, and the rate equation for the electron-hole recombination. The DBRT LED is optimized according to the conditions (1) electrons and holes simultaneously resonant-tunnel into the quantum well, (2) the charge carriers are entirely trapped in the well as the only light source, (3) the device operates at nearly zero-field condition, and (4) the electroluminescence spectrum is insensitive to temperatures.

We have performed a theoretical modeling to optimize such DBRT LED with respect to the geometric structures, the chemical compositions, and the doping profiles. All physical parameters are calculated from first principle, except the electron-hole recombination rate which is treated as an input parameter. Our calculated electroluminescence spectrum is proportional to the I-V characteristics. By shifting the threshold bias according to the temperature-dependent energy bandgap, all I-V curves between 10 K and 300 K collapse into a single spectrum, which is shown in the Figure.

A completely automated computer code has been constructed for such theoretical modeling of light emitting diodes.

Electron Emitter	$2 \times 10^{18} \text{ n}^+ - \text{Al}_{0.11}\text{Ga}_{0.89}\text{As}$	400Å
Spacer	un-doped $\text{Al}_{0.11}\text{Ga}_{0.89}\text{As}$	50Å
Barrier	$\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$	40Å
Well	GaAs	60Å
Barrier	$\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$	40Å
Spacer	un-doped $\text{Al}_{0.0775}\text{Ga}_{0.9225}\text{As}$	50Å
Hole Emitter	$4 \times 10^{18} \text{ p}^+ - \text{Al}_{0.0775}\text{Ga}_{0.9225}\text{As}$	400Å



*** MODULATED S-PARAMETER MEASUREMENTS, FOR ACTIVE MICROWAVE DEVICE CHARACTERIZATION, USING PULSED-BIAS OPERATION**

George Metze^{*}, Senior Member IEEE; Mark Calcaterra[†], Member IEEE; Chris Eppers[†]; Bob Neidhard[†]; James Whalen[‡], Senior Member IEEE

University of North Carolina, Charlotte, N.C.^{*}

Wright Laboratory, WPAFB, Dayton, OH[†]; State University of New York at Buffalo, Buffalo, N.Y. [‡]

Introduction

Traditionally, simulation of microwave circuits employing active device components (such as MESFETs, HBTs and HEMTs), has relied almost exclusively on the utilization of CW I-V and S-parameter characteristics. The data from these continuous wave measurements is then used in the parameter extraction process to help arrive at an equivalent circuit representation for the active device. Exclusive reliance on such data, however, can result in either an incomplete and/ or inaccurate data set. In particular, on-wafer CW characterization of large power devices is almost never undertaken (over the complete I-V plane), due in part, to breakdown and thermal run-away (i.e., destructive) problems resulting from the higher biasing currents and voltages used in typical power operation. Furthermore, it is a well known fact that CW characterization, and particularly under non-isothermal conditions, does not necessarily reflect the true microwave characteristics. Over the past few years, a number of investigators [1]-[4] have reported the use of pulsed DC or pulsed S-parameter characterization techniques to help generate more accurate device models, which now include thermal and/ or dispersive equivalent circuit elements. Even with these new set of measurements, however, CW S-parameter measurements are very rarely (if ever) obtained under pulsed DC bias operation. In this presentation, we will report on a unique technique that incorporates both pulsed DC biasing techniques with CW S-parameter measurements. Furthermore, we will illustrate how the individual vector properties of the modulated S-parameters (i.e., $\text{Re}[S_{11}]$, $\text{Im}[S_{11}]$, $\text{Re}[S_{21}]$, $\text{Im}[S_{21}]$, etc.) can be used to extrapolate/interpret the isothermal (i.e., no heating), CW S-parameters.

Experiment & Results

The experimental setup used in this work is shown in Figure 1. No modifications to the HP pulse generator or network analyzer were required/made. The tektronix digital analyzer was used only to accurately set the gate and drain pulsed biases and timing sequence. The microwave devices under test were multi-fingered, $0.5 \mu\text{m} \times 200 \mu\text{m}$ MESFETs.

* This work was sponsored by the Solid-State Electronics Division of Wright Laboratories, WPAFB, Ohio

Prior to performing the pulsed measurements, standard CW S-parameter measurements were made at numerous DC biases (from $V_{ds} = 0 \rightarrow 8\text{v}$ and $V_{gs} = -4.0 \rightarrow 0.5\text{v}$). The initial bias conditions for the pulsed measurements were with the device in the "OFF" (pinched-off) state. That is, the device was initially biased with $V_g = -4.0\text{v}$ and $V_d = 0\text{v}$. Then, the device was biased "ON" to some predetermined gate and drain biases. While a number of different gate and drain biases were tried, much of the data was tabulated at biases that showed indication of thermal heating (as determined by "droop" in DC I_{ds} characteristics). With the onset of the gate and drain pulses, the bias levels changed from: $V_g = -4.0\text{v} \Rightarrow 0.0\text{v}$ and $V_d = 0.0\text{v} \Rightarrow 5.0\text{v}$. The changes to the drain and gate biases were applied simultaneously, with correspondingly identical pulse widths and pulse repetition frequencies (PRF). The resultant reflected and/ or transmitted microwave signal (from the DUT), is essentially modulated (see Figure 2) by the bias to the device. In other words, while the device is biased in the "ON" state, the incident microwave signal(s) (ie, from DUT and back to the HP test set), represent the isothermal (for short pulse widths and duty cycles) S-parameters for the period of time that the device is in this state. A similar analysis would apply to the device in the "OFF" state. However, the analysis of this measurement is somewhat complicated by the IF band-pass filter (10 KHz) of the HP network analyzer (see Figure 2). Nevertheless, if the bias pulse repetition frequency (PRF) is ≥ 30 KHz, the resultant spectral response is a continuous wave carrier, whose microwave signal has the same fundamental frequency as the original source signal, but whose amplitude and phase represent the "scattered" response from the DUT (see Figure 2). Therefore, during the network analyzer measurement period (for non-swept mode $\sim 100 \mu\text{sec}$), the network analyzer averages (i.e., sample and holds) signals associated with the two different biasing states (i.e., "ON" and "OFF") of the device. That is, the resultant S-parameter measurement is a weighted average (with duty factor, DF) of the devices S-parameters, with the device in its "ON" and "OFF" states. Assuming little or no thermal effects, the measured S-parameters can be accurately described by the following linear relationship:

$$S_{ij} = \{S_{ij}^{\text{ON}} - S_{ij}^{\text{OFF}}\} * \text{DF} + S_{ij}^{\text{OFF}} \quad (1)$$

Thus, the resultant real and imaginary components of the S-parameter phasors, are linearly related to the biasing duty factor, with slope determined from the difference in the ON and OFF-state S-parameters. However, the aforementioned assumption assumes no other perturbations to the measurements, such as heating effects. Additional perturbations to this linear model, would most likely show up as 2nd or 3rd-order polynomial variations in the fit to the measured S-parameter data. That is, if the non-isothermal effects due to heating are included, the functional relationship might best be described by the following non-linear relation:

$$S_{ij} = \{S_{ij}^{\text{ON}} - S_{ij}^{\text{OFF}}\} * \text{DF} + S_{ij}^{\text{OFF}} + \xi\{T(\text{DF})\} \quad (2)$$

A sampling of the results, from our modulated S-parameter measurement experiments, is shown in Figure 3 (@ $f = 10$ GHz, $V_g = 0.0\text{v}$ and $V_d = 5\text{v}$). In this figure, we have plotted both the real and imaginary parts of S_{21} as a function of duty cycle/factor. In these experiments, the pulse width was kept constant at $1 \mu\text{sec}$, while the period was varied accordingly to produce duty factors ranging from approximately 1% to 95%. Measured S-parameter data, with duty factors below 20% (i.e., isothermal) were fitted to linear curves (e.g., equation 1) with remarkable accuracy ($R > .9999$). If one then extrapolates these linear curves (for low DF) to where the $\text{DF} = 1.0$ (or CW operation), it is our contention

that the intercept, with either the real or imaginary axis for S_{ij} , represents the S-parameter values for isothermal operation. Deviations from linearity, of the measured S-parameters, become apparent under operation with duty factors exceeding 50%. The actual curve fit to the measured S_{21} data is a second order polynomial. Further, and as a check on the validity of our measurements, we have included in Figure 3, the S-parameter values resultant from the standard CW measurements. Therefore, it is our belief that this small (but noticeable) difference between the linearly extrapolated and CW measured S-parameter values is a direct measure of the effects of heating due to biasing.

Finally, and totally independent of these measurements, CW S-parameter measurements were made, as a function of chuck temperature and of DC bias on a number of 0.5 mm X 200 μ m MESFETs. Shown in Figure 4 are the measured variations in the real and imaginary parts of S_{21} with varying substrate temperature. The "Bias 1" curve is similar to the bias conditions used in the modulated S-parameter experiments previously described. Comparing the results from Figure 3, and using Figure 4 as an approximate temperature "calibration curve", one might estimate the temperature rise, in the previous experiments, to be approximately 20 C. Interestingly enough, this is in rough agreement with the temperature rise calculated using thermal resistance.

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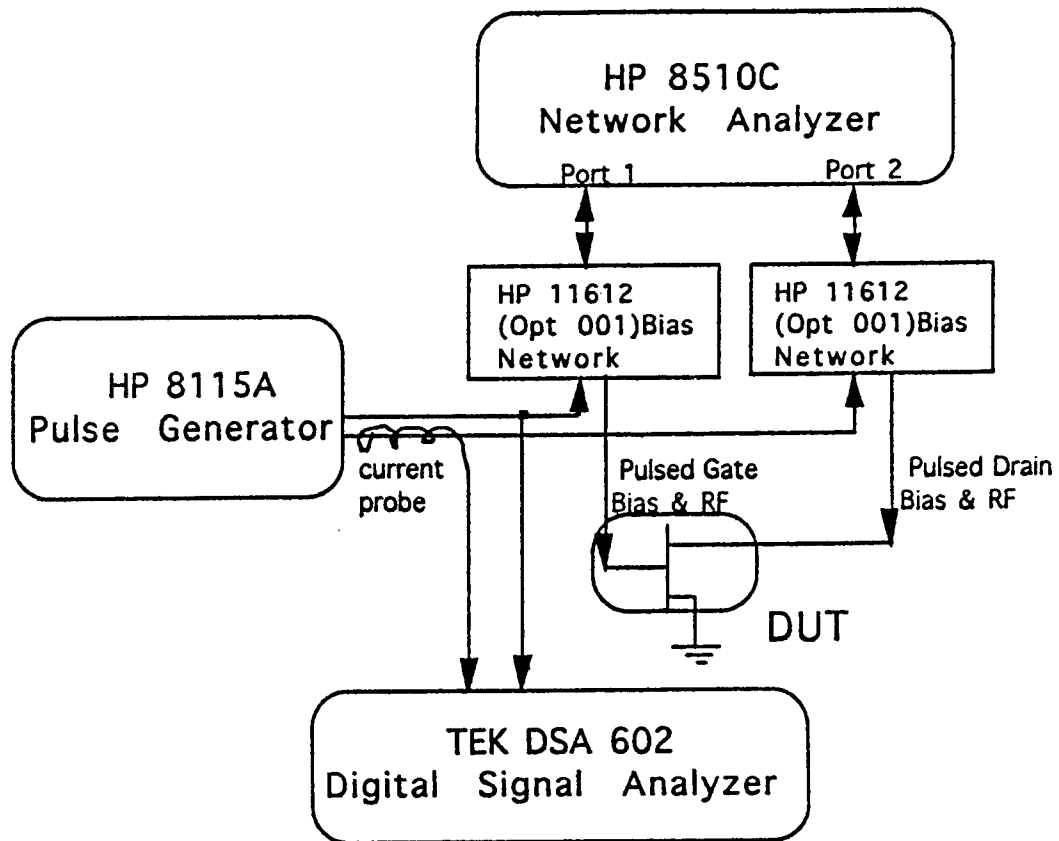


Figure1. Gated S-parameter with pulsed-bias test set-up

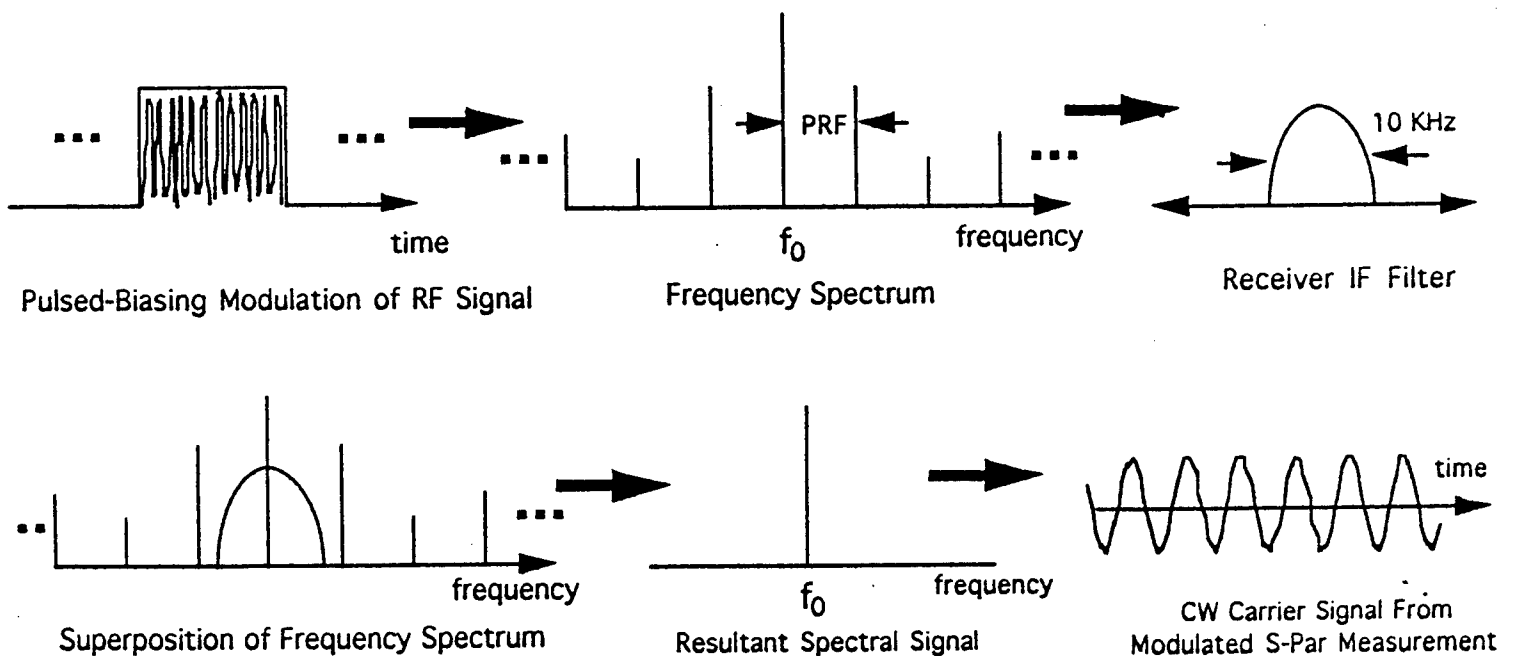


Figure 2. Pulsed Bias Modulation With Gated S-Parameter Measurement

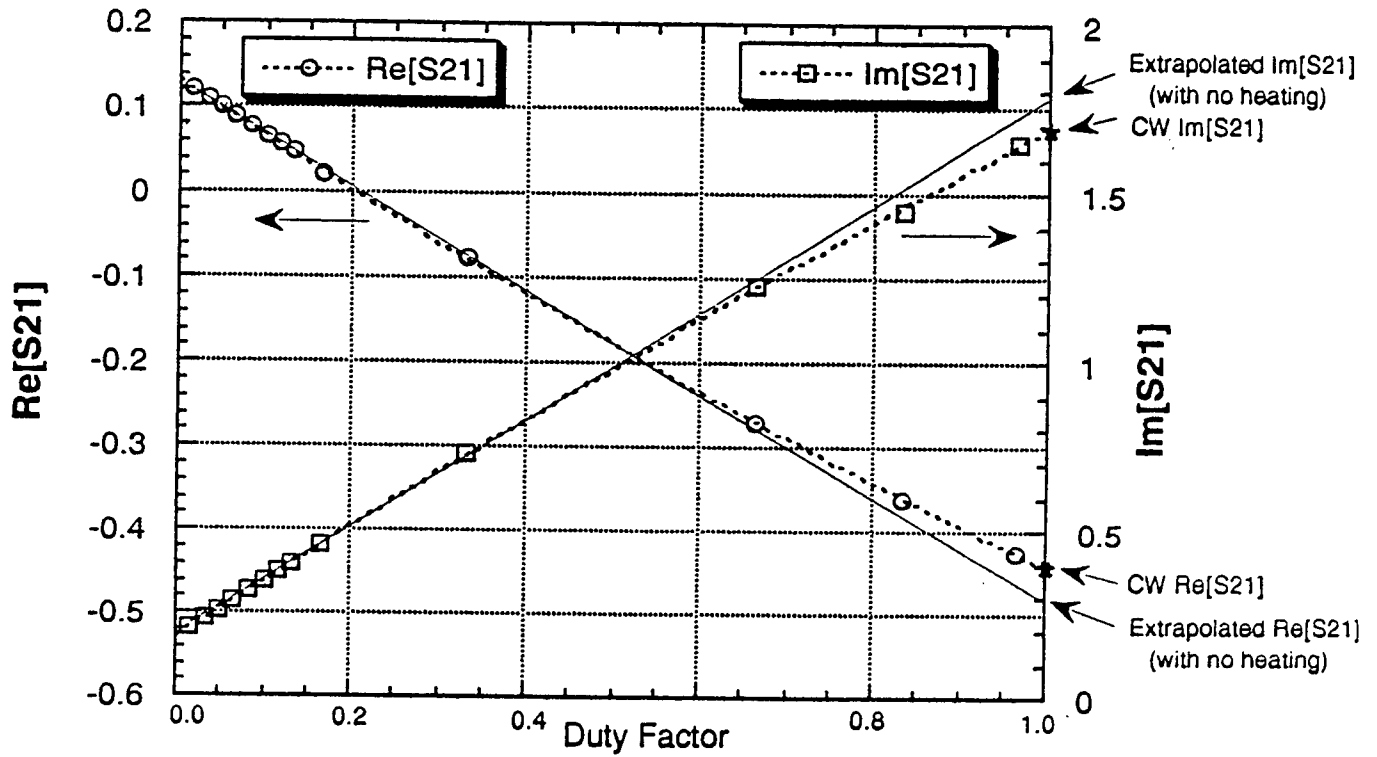


Figure 3 $Re[S_{21}]$ & $Im[S_{21}]$ versus DF

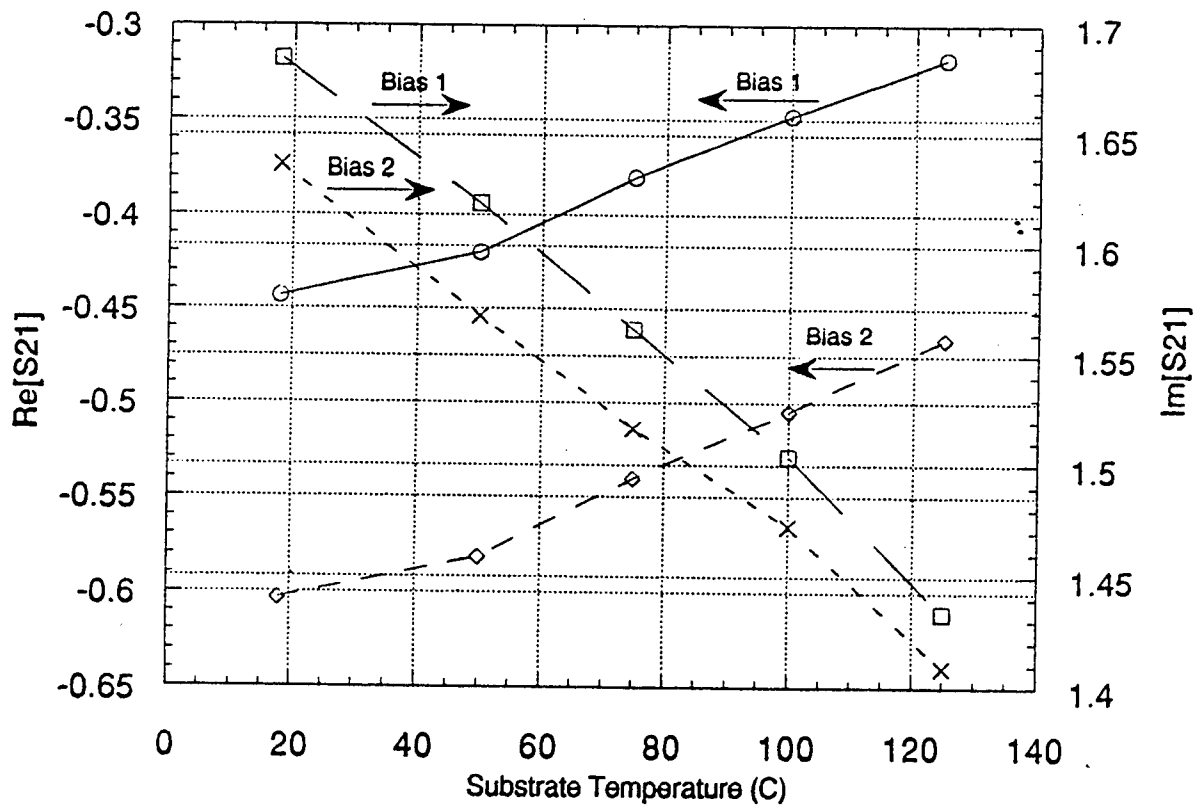


Figure 4 $Re[S_{21}]$ & $Im[S_{21}]$ versus temperature & bias
 Bias 1: $V_g=0, V_d=5.0, I_d=44mA$; Bias 2: $V_g=-1.0, V_d=5.0, I_d=22.4$

MODEL OF BACKGATING AND LIGHT SENSITIVITY IN GaAs AND LT MBE GaAs MESFET'S

De-Xin Wu¹, Rui-Gang Li¹, Zhan-Guo Wang², Ji-Ben Liang², and Lan-Ying Lin²

1. Microelectronics Research & Development Center, Chinese Academy of Sciences, P. O. Box 9819, Beijing 100029, P.R.China

2. Laboratory of Semiconductor Materials Science, Institute of Semiconductors, Chinese Academy of Sciences, P.O.Box 912, Beijing 100083, P.R.China

Backgating and light sensitivity are the most significant side-effects in GaAs MESFET's and GaAs VLSI. For the devices in GaAs VLSI is placed increasingly near, the isolation between adjacent devices become serious.

It is well known that the GaAs grown by molecular beam epitaxy (MBE) at low substrate temperature of 200~250°C (LT MBE GaAs) can be used as a buffer layer to eliminate backgating (or sidegating) and light sensitivity in GaAs MESFET's^[1]. However, the insight of the behavior is still not clear^[2]. In this paper we attempt to present a model to explain the light sensitivity phenomenon. Three different types of MESFET devices, A) the MESFET's in Si²⁹⁺ ion implanted active layer ($2 \times 10^{17} \text{ cm}^{-3}$) without buffer layer, B) the MESFET's in Si doped epitaxial active layer ($2 \times 10^{17} \text{ cm}^{-3}$) upon common MBE GaAs buffer layer, and C) the MESFET's in Si doped epitaxial active layer ($2 \times 10^{17} \text{ cm}^{-3}$) upon LT MBE GaAs buffer layer, were fabricated and studied in detail.

A theoretical model describing the light sensitivity in these devices is given based on the following equations: i) the Poission's equation, ii) the charge neutrality equation, and iii) the electron continuity equation.

LT MBE GaAs samples used in this study were grown by Riber-32 MBE system at 250°C using As and Ga beam flux ratio of 10 under arsenic-stable growth conditions. A 1000 Angstrom GaAs epilayer was first grown at 580°C, and then the substrate temperature was lowered to 250°C, while continuing to grow a 2µm-thick GaAs layer, the growth rate was about 1µm/h. The epilayers contain an excess arsenic of about 2.0%. The reflected high-energy electron diffraction (RHEED) pattern observed during growth, for substrate temperature down to 250°C, indicated that the LT MBE GaAs layers are high-crystalline quality, which were also confirmed by double-crystal X-ray diffraction measurements after growth. After annealing at 600°C for 30min., a 0.3µm Si-doped active layer with $2 \times 10^{17} \text{ cm}^{-3}$ and 0.05µm highly doped cap layer was subsequently grown at conventional temperature.

Three kinds of MESFET's shared the same standard 1µm process. Ohmic contacts on n⁺ cap layer were made by using Ni/Ge/Au metal. The drain-source spacing was 5µm and 5µm spacing between the MESFET and backgating testing pad was designed. Aluminum gate was employed after etching off the cap layer in the gate area, the gate length L_g and gate width W_g were 1µm and 100µm respectively. The pinch-off voltage was controlled by means of active layer etching. The device structure is shown in Fig.1.

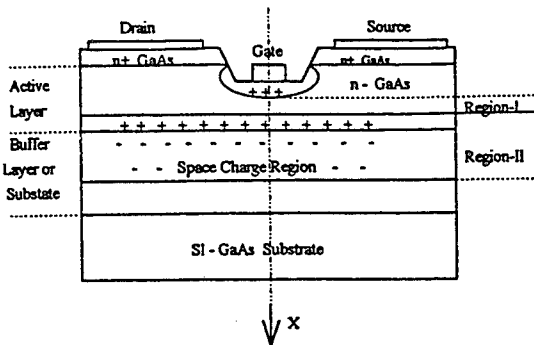
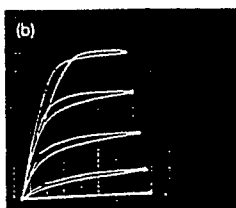
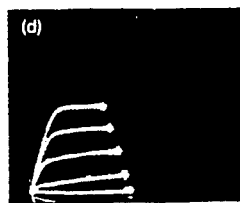


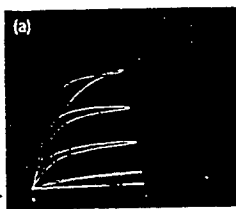
Fig. 1. Schematic cross section of three types of device structures



in the light

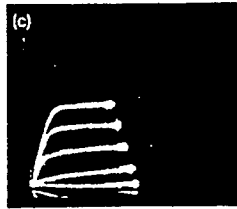


in the light



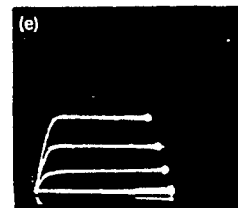
in the dark

A)



in the dark

B)



in the dark and in the light

C)

Fig.2. MESFET $I_{ds} - V_{gs}$ characteristics: The uppermost trace in figures is for $V_{gs} = 0V$. Subsequent traces are for V_{gs} increment of $-1.0V$. horizontal scale: $1.0 V/div.$, A) bulk i-GaAs device with an implantation active layer, vertical scale: $5mA/div$, B) undoped GaAs buffered device, vertical scale: $10mA/div$, and C) LT MBE GaAs buffered device, Vertical scale: $10mA/div$

DC characteristics of three kinds of devices in Fig. 2. are quite different in the dark and in the light. The R_d of the MESFET's incorporating the LT MBE GaAs buffer was much larger than that of the other two structures. Comparing with two other devices, the R_d was increased by over factors of 10 and 100 by using the LT MBE GaAs buffer (typically, the R_d of 500, 4000 and 50000 Ω for type A, B and C). The peak transconductance g_m of MESFET with LT MBE GaAs epilayer was also higher than that of the other structures which is different from the reports in literatures.

The devices on the LT MBE GaAs buffer layer show neither light sensitivity nor backgating, as illustrated by Fig.3. In order to check the backgating effect, a sidegate spaced $5\mu m$ from MESFET was designed. The MESFET with LT MBE GaAs buffer layer still showed no backgating, while $-20V$ applied to the sidegate and $V_{ds} = 2.5V$. For the same voltage, I_{dss} of the conventional MBE GaAs buffered devices was

reduced by 80 percent and only for -10V applied to the sidegate, I_{dss} of the ion implantation devices was reduced to zero.

In this paper, we proposed an one-dimensional model in which the light sensitivity of devices is mainly governed by the space charge region-II, and a little effect is contributed by region-I in active layer (see Fig.1). To better understanding the physical origin of the light sensitivity of the devices, according to our model, the following equations must be solved

$$\frac{\partial \Delta n}{\partial t} = \frac{1}{q} \nabla \cdot J_{\Delta n} + G_n - R_n, \quad (1)$$

$$\nabla(\epsilon \cdot \nabla \Psi) = e \left[n - p + \sum_{\text{all}} (N_A^- - N_D^+ + N_{AA}^- - N_{DD}^+) \right], \quad (2)$$

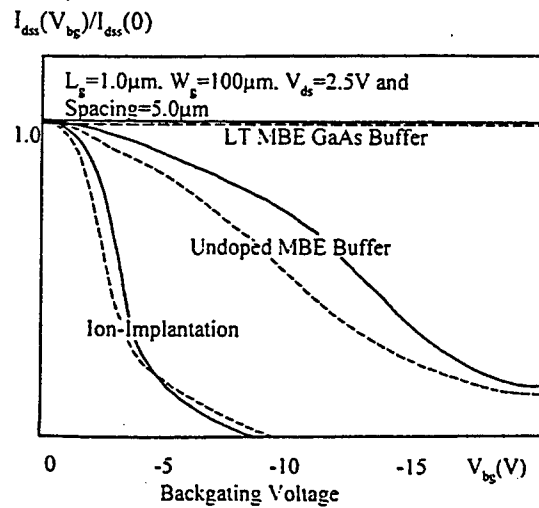


Fig.3. Backgating characteristics: The solid lines indicate the results obtained in the dark and the dashed lines in the light

where G_n is the generation rate for electrons, R_n ($R_n = \Delta n / \tau_n$) is the recombination rate, $J_{\Delta n}$ is the excess electron current density, τ_n is the excess electron life time, Ψ is the electrostatic potential, ϵ is the permittivity, e is the electronic charge, N_A^- and N_D^+ are the concentrations of ionized acceptors and donors, N_{AA}^- and N_{DD}^+ are the concentrations of ionized acceptor-like and donor-like traps, respectively. At the equilibrium condition, the $\partial \Delta n / \partial t = 0$. Combining the charge neutrality equation,

it is easy to know from the solutions of Eq.(1) and Eq.(2) that the excess carrier life time plays a very important role for controlling the light sensitivity. The excess electron life time is quite different for three kinds of materials. It is about 10^{-13} sec. in the LT MBE GaAs^[3] and about 10^{-9} sec. in the conventional MBE GaAs and semi-insulating GaAs. Due to the very short life time of excess carrier in LT MBE GaAs buffer, there are nearly no photo-induced carriers to

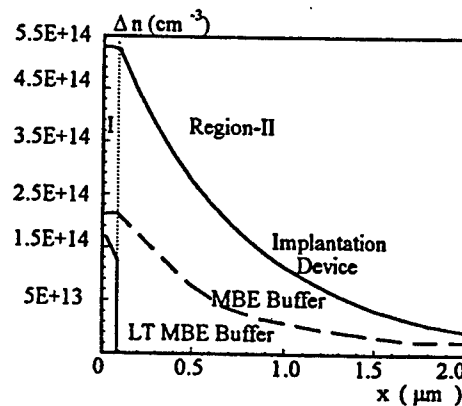


Fig. 4. The distribution of Δn versus x for three different devices

be driven to active layer. From the solution of Eq.(1) and Eq.(2), the dependence of the photo-induced excess electron concentrations Δn on x is shown in Fig. 4.

The increment of drain current ΔI_{dss} is determined by substituting Eq.(1) and Eq.(2) into Eq.(3)

$$\Delta I_{dss}(\Phi_0) \propto e\mu_{n1} \int_0^d \Delta n_1(x) dx + e\mu_{n11} \int_d^\infty \Delta n_{11}(x) dx, \quad (3)$$

where d is the thickness of the region-I, and the initial photon flux Φ_0 can be measured by the calibrated detector. Since the mobility of the hole is much smaller than that of the electron, Δp was not considered in the model. The calculation results demonstrated that $\Delta I_{dss}(\Phi_0)/I_{dss0}$ is about 7% for ion implantation devices, 3% for conventional MBE buffered devices and nearly zero for LT MBE GaAs buffered devices respectively, which are well agreement with the experimental data.

The insight of backgating effect for ion implantation and conventional MBE GaAs buffer layer devices can be easily understood according to electron injection into traps in the substrate and active layer/buffer layer interface^{[4]-[5]}. However, for the devices with LT MBE GaAs buffer layer, the mechanism mentioned above is on longer valid. Based on the Warran's Schottky barrier model of LT MBE GaAs, we present a new model in which the depleted region exists in the whole LT MBE GaAs buffer layer and the V_{bg} is screened by the metallic As precipitates as quantum points burred in the buffer layer which are similar to the role of quantum well. That is why no backgating can be observed for LT MBE GaAs buffered devices. The density, diameter and spacing of the As precipitates is about $1.7 \times 10^{17} \text{ cm}^{-3}$, 6nm and 18nm respectively according to our TEM measurement. The details of this model will be published elsewhere.

We have also employed LT MBE GaAs technique in high electron mobility transistors (HEMT's), very high speed GaAs digital integrated circuits (VHSIC's), analog to digital converters(ADC's) and microwave monolithic integrated circuits (MMIC's). And the performances were highly improved.

ACKNOWLEDGMENT

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Analysis of the charge injection in MOS analog switches using physical models

Etienne Robilliart and Emmanuel Dubois,
Tel: (+33) 20.19.79.17 Fax: (+33) 20.19.78.84 e-mail: ero@isen.fr
IEMN/ISEN UMR CNRS 9929
Avenue Poincaré, Cité Scientifique, BP 69, 59652 Villeneuve d'Ascq Cedex, France

Introduction

Elementary sample-and-hold functions are widely used in advanced analog MOS architectures [1]. The sampling function is generally realized by the storage of an input signal on a capacitor through a MOS switch transistor. The holding function is subsequently performed when the switch is turned off. However, the major limitation of this basic sample-and-hold scheme is the charge disturbance of the storage node related to the intrinsic charge released from the channel and also due to the feedthrough currents from the gate to diffusion capacitances. With the progress of low voltage submicron technologies, charge injection effects play an increasingly important role and constitutes a major issue for the design of high precision analog circuits, such as A/D converters [2]. Conventional analytical compact models [3] [4] reveal poor prediction capabilities of the charge sharing effects during fast transient because based on the quasi-static (QS) approximation. Previous investigations of the switch charge injection problem have been carried out through analytical and/or first order numerical calculation [5] [6]. Their domain of validity is, however, limited by restrictive conditions on the switching speed.

In this paper, we first present a rigorous two-dimensional (2D) analysis of the charge injection effect using mixed device/circuit simulations [7]. We subsequently introduced a one-dimensional (1D) numerical MOSFET model suitable for circuit simulations in terms of computational burden. It is shown that this last approach retains the same advantages than 2D physical analysis : continuity over all operating regimes and non-quasi-static (NQS) description of the charge dynamics without any restrictive assumptions on the charge partitioning between source and drain terminals [8] [9].

Circuit description

The circuit schematic corresponding to the charge injection problem is a simple transmission gate loaded by the capacitance C_L as shown in Fig. 1. R_{in} and C_{in} are the lumped resistance and capacitance associated with the rest of the circuit. The data holding capacitance C_L was set to 1.6 pF and the pass transistor size ratio was $W/L=3\mu\text{m}/1\mu\text{m}$ implemented in a $1\mu\text{m}$ technology [10]. The input resistance was first considered infinitely large to allow a comparison with previous analytical investigations. A constant falling rate α was assumed for the command of the MOS switch. Typical falling times ranged from 10 ps to 110 ns in order to analyze the charge repartition on the input and data holding nodes. Universal charts present the charge ratio Q_L/Q_G as a function of the dimensionless quantity $(V_{Gon}-V_{TH}-V_L).(\mu C_{ox} W/L/(\alpha.C_L))^{1/2}$ where Q_L stands for the charge released on the data holding capacitance, Q_G is the charge stored on the gate, $V_{Gon} = 5V$ is the maximum gate voltage and V_{TH} is the threshold voltage including the body effect.

2D device/circuit simulation results

The charge sharing was first analyzed for a gate voltage varying from V_{Gon} to the threshold $V_{TH}+V_L$ to follow the same assumptions used in previous works [5] [11]. Fig. 2 presents the corresponding charge repartition for different values of the C_L/C_{in} ratio. The observed discrepancy between our full treatment and the analytical results remains small but shows the impact of the NQS effects on the charge dynamics. The upper curve in Fig. 2 reveals a typical error of 2.5 % on the prediction of the charge that perturbs the data-holding node. In the case under study, this results in a voltage deviation of 350 μV which is much larger than the resolution required for high precision analog functions. For instance, a resolution of 45 μV is needed for a 16 bit A/D conversion under a supply voltage of 3 V. Fig. 3 presents the charge repartition normalized to the total charge flowing to the source and drain terminals $\Delta Q_L + \Delta Q_{in}$ for a gate voltage ranging from V_{Gon} to 0V. The rigorous numerical treatment still differs significantly from the analytical solution that overlooks the coupling through the overlap capacitances which is the predominant effect in the subthreshold gate voltage range. In that case, an error as high as 7.5% can be observed which corresponds to a voltage deviation of 1 mV on the data-holding

node. Fig. 4 shows the influence of a finite value of the input resistance R_{in} on the charge repartition. As long as the time constant $R_{in} \cdot C_{in}$ remains large with respect to the fall time, the charge stored on C_L does not vary. A decrease of the source resistance contributes effectively to the reduction of the charge perturbation on the load capacitance. Finally, the $\Delta Q_L / \Delta Q_G$ ratio levels off to a minimum value for small input resistances as the input circuit behaves as a ideal voltage source. Fig. 5 and 6 show the time dependent variations of the load and input currents corresponding to a fall time of 1 ns and 10 ps, respectively. It is clearly observed that the charging currents flowing to the source and drain nodes converge to the same waveform when the fall time is reduced.

A new CAD model for circuit simulation : comparison to BSIM3

2D numerical simulations are accurate, but require excessive CPU times within the context of circuit design. To obtain the same accuracy, we have developed an efficient 1D CAD-oriented model continuous over all operating regimes suitable for long and short channel devices. In addition, the NQS charge redistribution is implicitly taken into account. This model is based on a rapid numerical resolution where Poisson and the current continuity equations are consistently solved using a newton method [12]. This model was coded in C and introduced in the ELDO circuit simulator [13] which retains the same functionality than SPICE. The comparison between our new MOSFET model, BSIM3 and 2D simulations is given in Fig. 7 for the fast turn-on of a single device in linear regime. The currents given by BSIM3 are strongly disturbed due to charge discontinuities and to the inappropriate channel charge partitioning for a gate voltage close to the threshold. In contrast, the currents given by our model follow the smooth variations of 2D simulations. In the case of the complete circuit of Fig. 1 transient currents are shown in Fig. 8 and 9. Although small discrepancies still exist in the sub-threshold region, our new model does not exhibit unphysical current spikes, typical of QS charge based models like BSIM3. The same conclusions can be drawn from Fig. 10 and 11 that present the input (I_{in}) and load (I_L) currents of the MOS switch for different loading conditions ($C_L / C_{in} = 1, 3, 10, 100$). Finally Fig. 12 and 13 present the time-dependent variations of the voltage perturbations induced on the data holding node (V_L) and on the input node (V_{in}). It is clearly shown that a QS model like BSIM3 overestimates the voltage deviation under fast transient conditions for which QS operations is violated.

Conclusion

Charge injection has been investigated by accurate 2D numerical simulations of the transport equations that implicitly take into account small geometry effects and the non-quasi-static nature of the charge dynamics. An efficient CAD-oriented NQS MOSFET model for circuit applications has been developed and compared to results of 2D and BSIM3 simulations. This model, implemented in the circuit simulator ELDO proved to be very useful for the simulation of critical part of large analog circuits, and does not require an excessive extra computational burden (10% to 300%) depending on circuits size and complexity.

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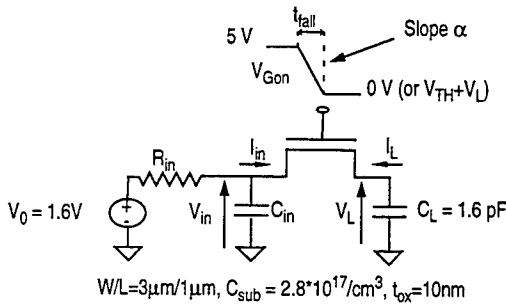


Fig 1: Circuit analysis for charge injection

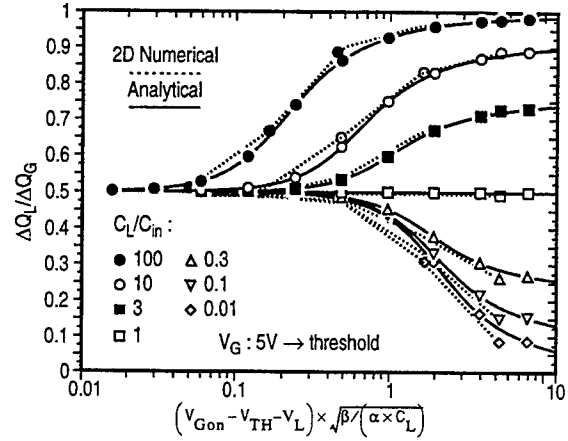


Fig 2: Percentage of injected charges on the load capacitance ($\beta = \mu \cdot C_{ox} \cdot W/L$; $\alpha =$ slope of V_G)

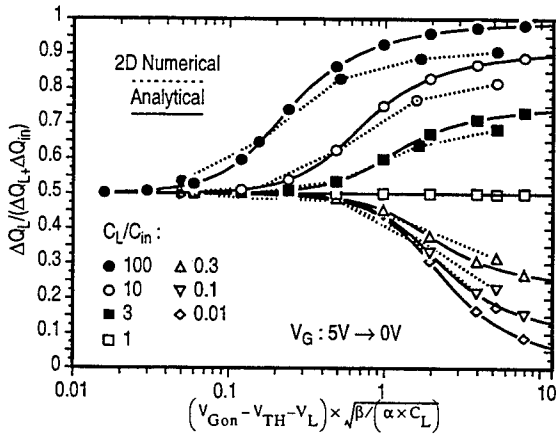


Fig 3: Percentage of injected charges on the load capacitance ($\beta = \mu \cdot C_{ox} \cdot W/L$; $\alpha =$ slope of V_G)

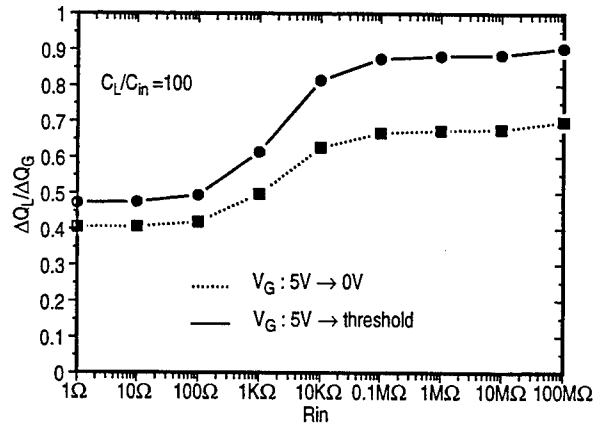


Fig 4: Percentage of injected charges on the load capacitance versus input resistance: $(V_{Gon} - V_{TH} - V_L) \times \sqrt{\beta / (\alpha \times C_L)} = 0.5$

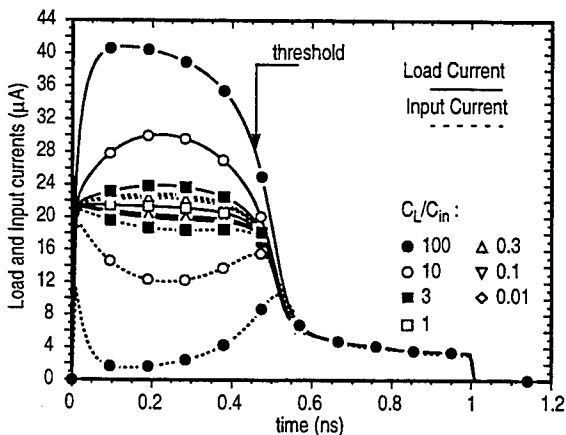


Fig 5: Load and Input Currents for: $(V_{Gon} - V_{TH} - V_L) \times \sqrt{\beta / (\alpha \times C_L)} = 0.5$ ($\beta = \mu \cdot C_{ox} \cdot W/L$; $\alpha =$ slope of V_G ; $t_{fall} = 1$ ns; $R_{in} = \infty$)

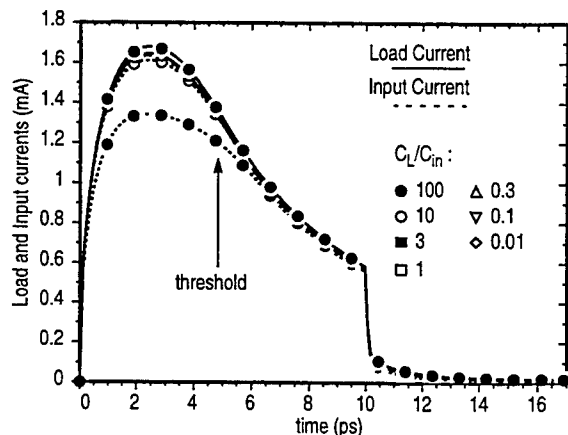


Fig 6: Currents for: $(V_{Gon} - V_{TH} - V_L) \times \sqrt{\beta / (\alpha \times C_L)} = 0.05$ ($\beta = \mu \cdot C_{ox} \cdot W/L$; $\alpha =$ slope of V_G ; $t_{fall} = 10$ ps; $R_{in} = \infty$)

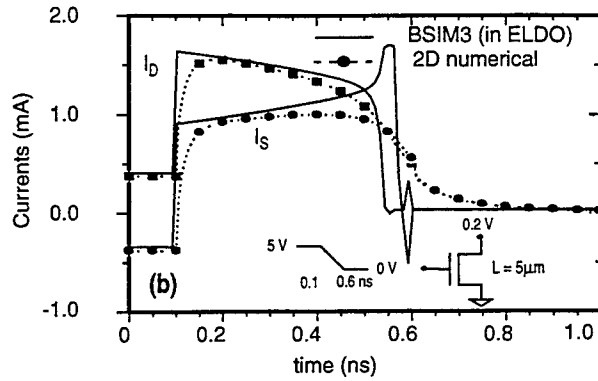
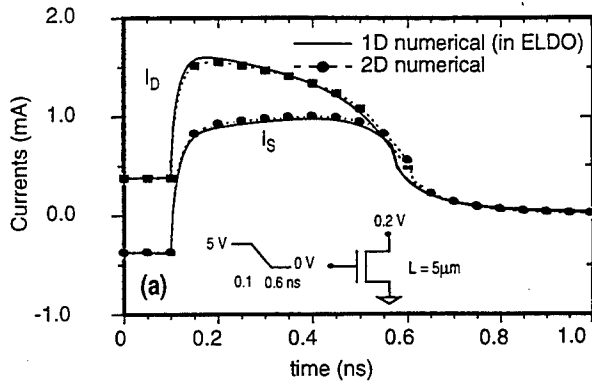


Fig 7: Transient source and drain currents during switch-off in linear regime : (a) 1D numerical model (b) BSIM3

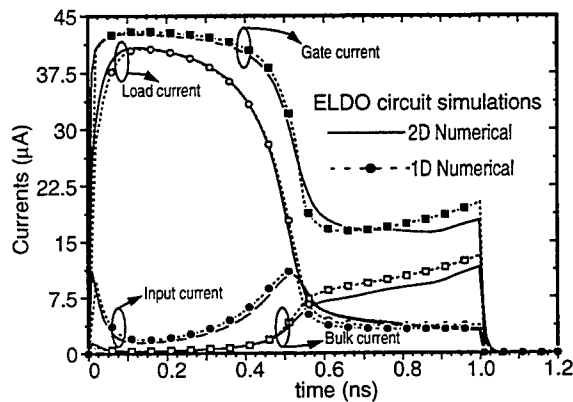


Fig 8: Transient gate, drain, source and bulk currents during the switch-off ($t_{fall} = 1ns$; $C_L/C_{in} = 100$; $R_{in} = 10M\Omega$)

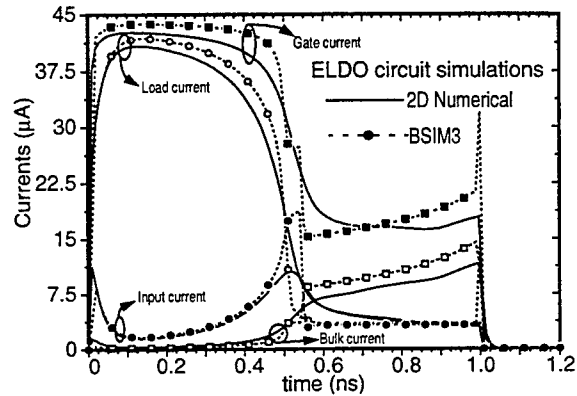


Fig 9: Transient gate, drain, source and bulk currents during the switch-off ($t_{fall} = 1ns$; $C_L/C_{in} = 100$; $R_{in} = 10M\Omega$)

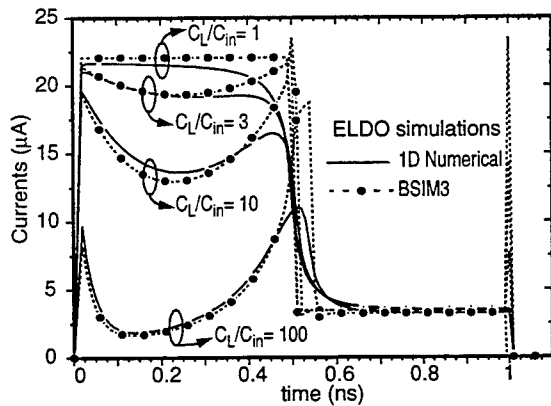


Fig 10: Comparison of the input current for the 1D numerical model and the BSIM3 model ($t_{fall} = 1ns$; $R_{in} = 10M\Omega$)

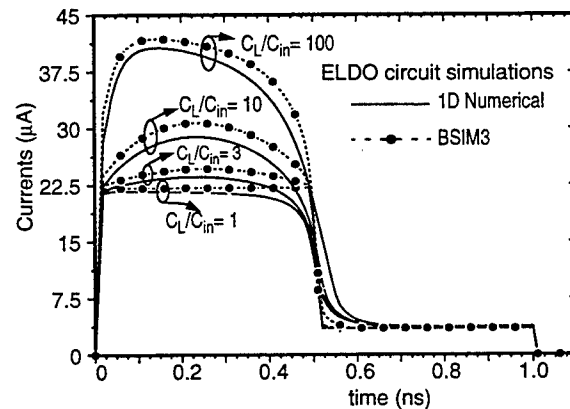


Fig 11: Comparison of the load current for the 1D numerical model and the BSIM3 model ($t_{fall} = 1ns$; $R_{in} = 10M\Omega$)

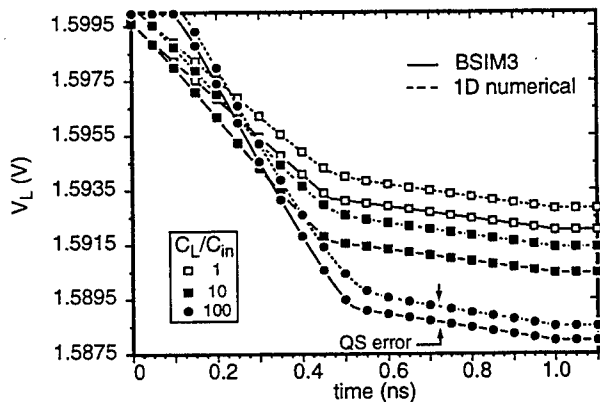


Fig 12: Error voltage on capacitance C_L during a switch-off variation of gate voltage ($t_{fall} = 1ns$; $R_{in} = 10M\Omega$)

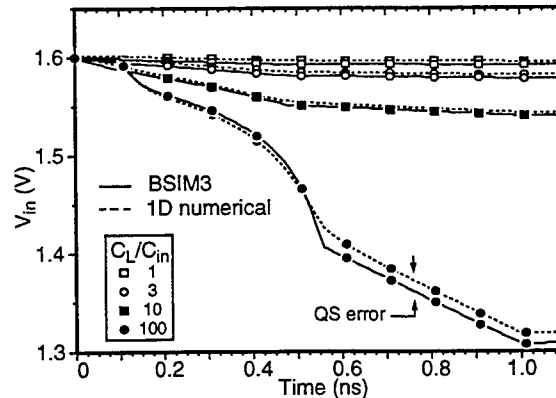


Fig 13: Error voltage on capacitance C_{in} during a switch-off variation of gate voltage ($t_{fall} = 1ns$; $R_{in} = 10M\Omega$)

Analytical Investigation of Electrical Performance of III-V Semiconductor Metal-Insulator-Semiconductor Field-Effect Transistors

Franck Stengel, S. Noor Mohammad and Hadis Morkoç
University of Illinois at Urbana-Champaign,
Materials Research Laboratory & Coordinated Science Laboratory
104 South Goodwin Ave., Urbana, IL 61801

An analytical model for the drain current characteristics and related properties of an n-channel MISFET is developed. For this, an approximation leading to a two-dimensional analytical potential is used. In order to calculate the potential created by the gate, the Poisson's equation is rewritten to a form amenable to analytical modelling. Taking diffusion and velocity saturation in the channel into account, the current resulting from applied drain and gate biases is then modelled. This model is used to compare ideal properties of GaAs/Si₃N₄ MISFET to those of Si/SiO₂ MOSFET. For all of them the channel doping concentration was chosen to be 10^{16} cm⁻³. The variation of the calculated drain-source current as a function of drain-source voltage for GaAs and InGaAs MISFETs and of Si MOSFET is shown in Fig. 1. The channel length for all of them were 5 microns, and the gate voltages 1 and 3 V, respectively. InGaAs MISFETs showed the best performance. The calculated variation of transconductance with the applied gate bias is shown for InGaAs and GaAs MISFETs and Si MOSFETs in Fig. 2. For all of them, the drain-source voltage was 1 V, and the channel length was 1 micron. The insulator thickness was 100 Å and 200 Å, respectively. Again, the InGaAs MISFETs showed the best performance.

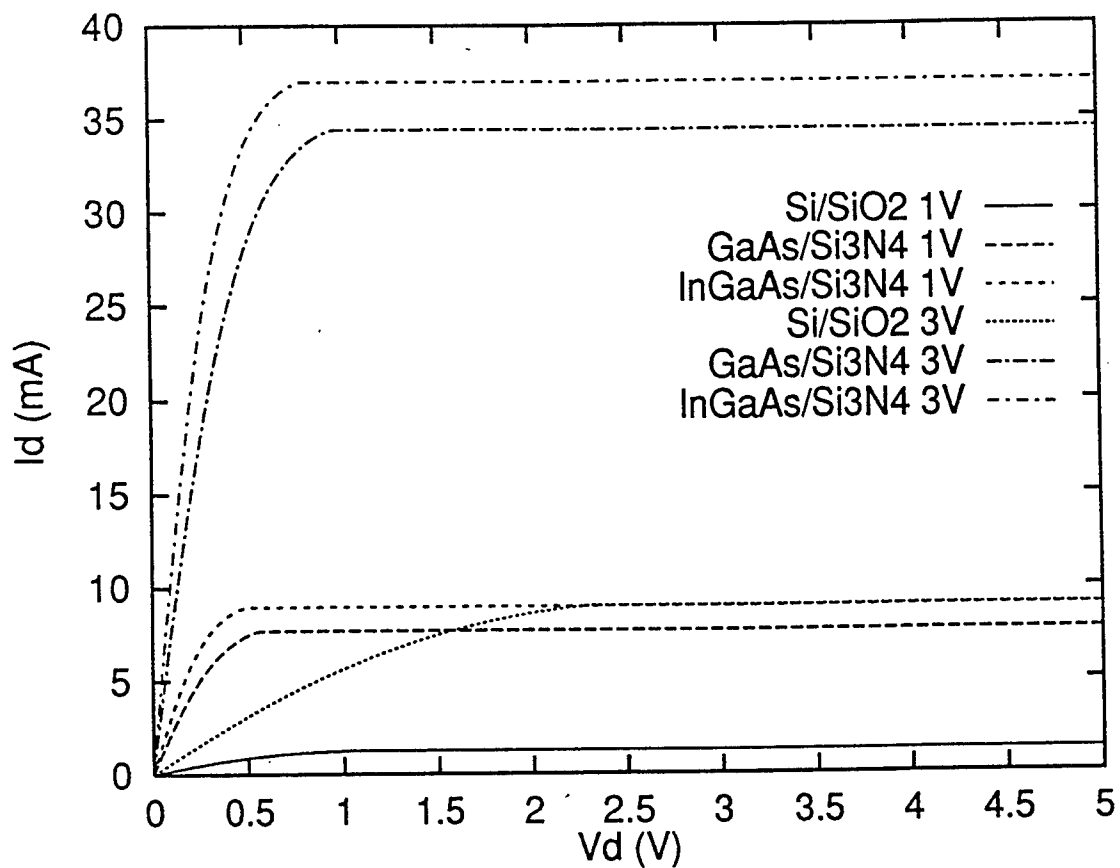


Fig.1 Id-Vd characteristics for Si, GaAs, and InGaAs L=5um

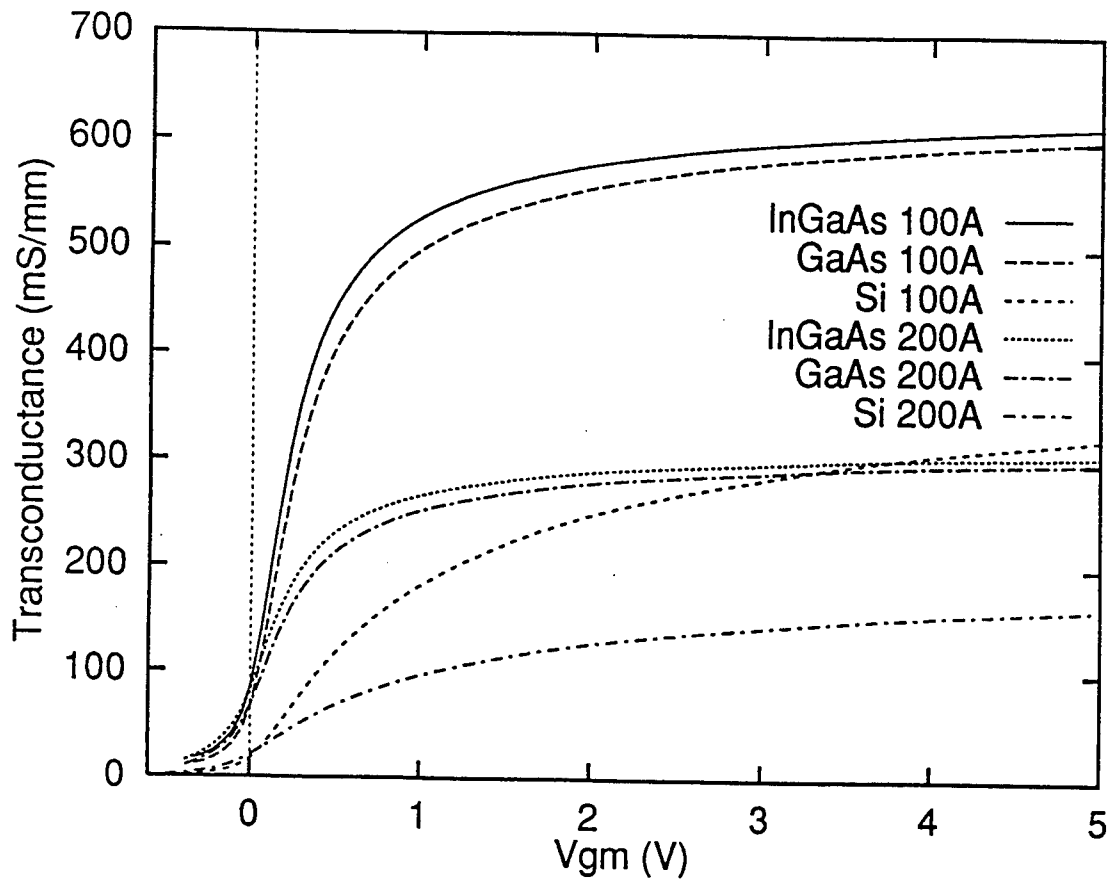


Fig.2 Transconductance as a function of V_{gm} for different delta for InGaAs, GaAs and Si.

Comparison of 2-D and 3-D Side-gated FETs

M. J. Hurt¹, W. C. B. Peatman^{1,2}, R. Tsai², B. J. Moon³, T. Ytterdal², and M. Shur²

¹Advanced Device Technologies, Inc., Charlottesville, VA 22903

²Department of Electrical Engineering, University of Virginia, Charlottesville, VA 22903

³Vitesse Semiconductor Corporation, Camarillo, CA 93012

Abstract—Two sidewall gate transistors, the 2-D MESFET and the 3-D MESFET, are compared. The 2-D MESFET is formed by electroplating Pt/Au onto the side of an AlGaAs/InGaAs/GaAs heterostructure, while the 3-D MESFET utilizes the same gate process but with an ion-implanted, bulk n-GaAs material structure. DC I/V measurements are performed on each device. The results suggest that both of these side-gated FETs are promising candidates for low power electronics applications. Gate current measurements reveal that the effective Schottky barrier height is comparable in each device. Temperature measurements of both sidewall gate FETs are also performed.

I. Introduction

Recently, a new sidewall gate transistor technology, based on the heterodimensional 3-d metal/2-d electron gas Schottky junction [1, 2], has been reported [3-7]. A schematic of one such side-gated transistor, the 2-D MESFET, is shown in Fig. 1. The 2-D MESFET utilizes Schottky contacts on either side of an AlGaAs/InGaAs/GaAs heterostructure. One of the principle advantages of this device is that the narrow channel effect (NCE), in which charges at the edges of the channel in a top-gated structure contribute to parasitic currents as the gate width decreases, is eliminated by the unique sidewall gate geometry. This permits width scaling to submicron dimensions without degradation of the electrical characteristics; in fact, the current/voltage characteristics of the 2-D MESFET actually improve with shorter gate widths [5]. Coupled with the high-speed characteristics of GaAs devices, this new device technology is a promising candidate for future low power electronics applications.

In this paper, we investigate a new sidewall gate FET fabricated on ion-implanted, bulk n-GaAs material and compare this new device to the 2-D MESFET. The bulk n-GaAs side-gated FET, or 3-D MESFET, represents the middle ground between conventional MESFETs and the heterodimensional 2-D MESFET. The new device utilizes the same geometry as the 2-D MESFET and therefore experiences no deterioration due to the NCE at submicron widths. However, the bulk n-GaAs material structure, while being cheaper to fabricate, does not have some of the inherent advantages of the 2-D MESFET, such as the high mobility of the InGaAs

channel and the low-capacitive interface between the 3d Schottky gates and the 2d electron gas.

The focus of this paper is to compare the ion-implanted 3-D MESFET to the pulse-doped 2-D MESFET. Specifically, we compare and contrast the fabrication details, DC current/voltage measurements, effective Schottky barrier heights, and temperature characteristics of the 2-D MESFET and the 3-D MESFET.

II. Fabrication

The fabrication processes of the 3-D MESFET and the 2-D MESFET are nearly identical. The layout of the bulk n-GaAs FET is the same as shown schematically in Fig. 1 for the 2-D MESFET. Prototype 3-D MESFETs were fabricated on n-type GaAs material having a buried Be-doped p-layer ($1.5 \times 10^{12} \text{ cm}^{-2}$ at 150 keV) and a $7 \times 10^{12} \text{ cm}^{-2}$ Si channel implanted at 40 keV. After activation, the wafer was Hg probed and found to have a doping of $3 \times 10^{17} \text{ cm}^{-3}$ down to a depth of approximately 800 Å. This value corresponds to a sheet density of $n_s \sim 2 \times 10^{12} \text{ cm}^{-2}$, which is the same as the sheet density in the MBE material used to fabricate heterodimensional 2-D MESFETs. Ni/Ge/Au ohmic contacts were formed using standard contact UV lithography and evaporation/lift-off techniques. The gate pattern was defined using electron beam lithography. The electron beam resist served as the

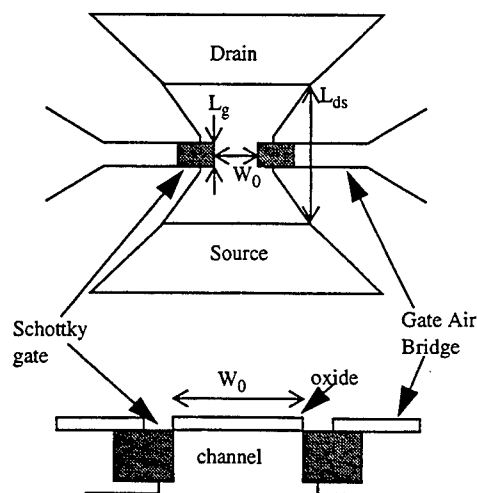


Fig. 1. Top view and cross section of 2-D and 3-D side-gated FETs.

mask for the gate electroplating. The Pt/Au gates were deposited into the gate trench using capacitor discharge electroplating. Cr/Au contact pads were evaporated on the wafer and a wet etch was used to isolate the ohmic and Schottky pads. The remaining fabrication details for the 3-D MESFET are identical to those for the 2-D MESFET and can be found in [3, 4, 6]. The sequential layers of the 2-D MESFET structure above the semi-insulating GaAs substrate include a 5000 Å undoped GaAs buffer, a 120 Å undoped $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ channel, a 50 Å undoped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ spacer, a δ -doped layer ($n_s = 3 \times 10^{12} \text{ cm}^{-2}$), a 300 Å n-type $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ layer doped to $5 \times 10^{17} \text{ cm}^{-3}$, and a 40 Å n^+ GaAs cap layer. For both devices, the gate-to-gate widths W_0 were in the range 0.5-1.0 μm , the gate lengths L_g in the range 0.2-1.0 μm , and the drain-to-source lengths L_{ds} were about 3 μm . Both gates were electrically connected in the measurements discussed here; however, multi-gate inputs may be used for higher functionality, as described by J. Robertson, et al, elsewhere in these proceedings.

III. Results

Room temperature device measurements of the 2-D MESFET and the 3-D MESFET were performed using a Micromanipulator 7000 probe station and an HP4145 parameter analyzer. Table 1 presents the measured parameters of a representative 1.0 x 1.0 μm ($W_0 \times L_g$) and 0.5 x 0.5 μm 2-D MESFET and 3-D MESFET. The I/V data for the 0.5 x 0.5 μm devices are plotted in Figures 2-7. The gate pattern for these devices was defined in the same fabrication run and therefore the channel dimensions of the two devices are identical. Since the electron concentrations in the channel of each FET are also equivalent ($n_s \sim 2 \times 10^{12} \text{ cm}^{-2}$), the only significant difference between the two devices is the material structure.

The 1.0 x 1.0 μm 3-D MESFET is characterized by a large negative threshold voltage, high reverse bias leakage current, and a large DIBL voltage shift. Compared to the bulk n-GaAs device, the 1.0 x 1.0 μm 2-D MESFET has a less negative threshold voltage, lower leakage current, and a smaller DIBL shift. Also, there is proportionally a larger change

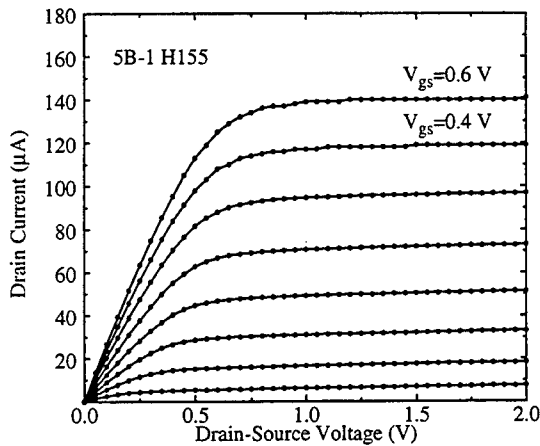


Fig. 2. I_d vs. V_{ds} for 0.5 x 0.5 μm 3-D MESFET (bulk n-GaAs device).

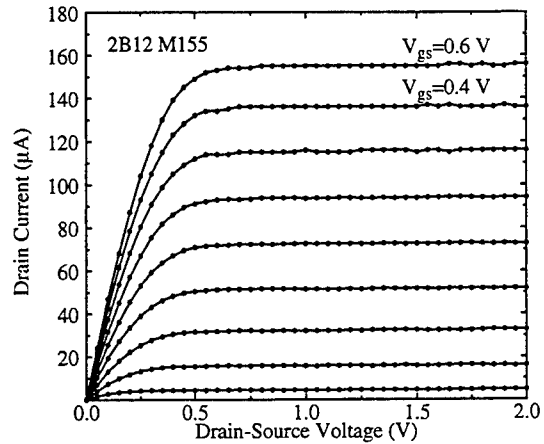


Fig. 4. I_d vs. V_{ds} for 0.5 x 0.5 μm 2-D MESFET.

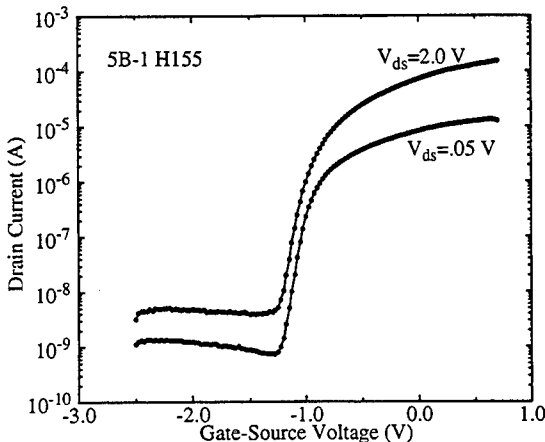


Fig. 3. I_d vs. V_{gs} for 0.5 x 0.5 μm 3-D MESFET (bulk n-GaAs device).

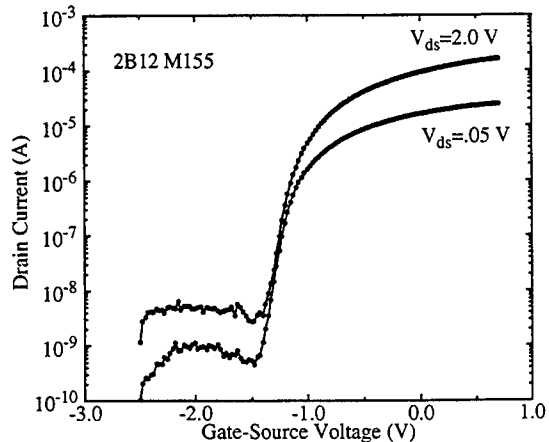


Fig. 5. I_d vs. V_{gs} for 0.5 x 0.5 μm 2-D MESFET.

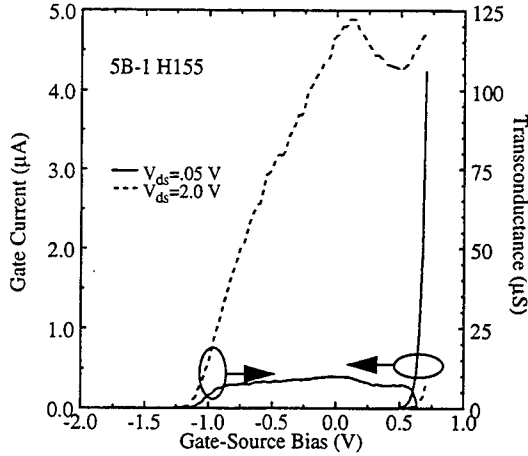


Fig. 6. I_g and g_m vs. V_{gs} for $0.5 \times 0.5 \mu\text{m}$ 3-D MESFET.

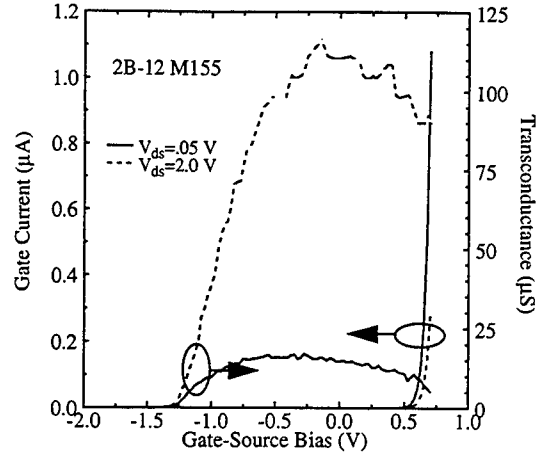


Fig. 7. I_g and g_m vs. V_{gs} for $0.5 \times 0.5 \mu\text{m}$ 2-D MESFET.

in the peak transconductance of the 2-D MESFET compared to the 3-D MESFET when scaling from $1.0 \mu\text{m}$ channel dimensions to $0.5 \mu\text{m}$ dimensions. On the other hand, the electrical characteristics of the $0.5 \times 0.5 \mu\text{m}$ bulk n-GaAs FET (Figs. 2, 3, and 6) and the $0.5 \times 0.5 \mu\text{m}$ 2-D MESFET (Figs. 4, 5, and 7) are nearly identical. Also, the transconductance of each $0.5 \times 0.5 \mu\text{m}$ device is flat over a large range of gate bias values. Together, this illustrates that the electrical characteristics of both of these sidewall gate FETs improve upon scaling to smaller submicron channel dimensions.

The effective Schottky barrier heights of the sidewall gates were extracted for the 3-D MESFET and the 2-D MESFET using the gate current data shown in Figs. 6 and 7, respectively, and the following expression (see, for example, [8]):

$$J_g = A^* T_s^2 \exp\left(-\frac{\phi_b}{k_B T_s}\right) \quad (1)$$

where J_g is the gate saturation current density, A^* is the effective Richardson constant, T_s is the temperature on the source side of the channel, k_B is Boltzmann's constant, and ϕ_b is the barrier height. The area for each contact was taken as the product of the gate perimeter and the channel thickness ($3.5 \mu\text{m} \times 800 \text{ \AA}$ for the 3-D MESFET and $5 \mu\text{m} \times 200 \text{ \AA}$ for the 2-D MESFET). The extracted Schottky barrier height was 0.67 eV for both the ion-implanted FET and the 2-D MESFET. Typically, InGaAs has a significantly lower barrier height than GaAs. Since the extracted barrier heights are identical, we conclude that there is enhancement of the effective barrier height in the 2-D MESFET due to the heterodimensional 3d/2d junction.

There are three aspects of the 2-D MESFET's electrical characteristics that, independent of channel dimensions, indicate a potential for better low-power performance than the 3-D MESFET.

First, the knee voltage of the 2-D MESFET was lower than that of the ion-implanted devices by $0.1\text{--}0.2 \text{ V}$ for all channel dimensions. Second, the 2-D MESFET consistently had a lower output conductance. For the $0.5 \times 0.5 \mu\text{m}$ device, the output conductance of the 2-D MESFET was 0 while that of the 3-D MESFET was $2.2 \mu\text{A/V}$. Third, the DIBL voltage shift was smaller in the heterodimensional device than the bulk-doped device for all channel widths. However, the ion-implanted device has the advantage that it does not require MBE growth and is therefore cheaper to manufacture. Either approach should lead to improved low power performance due to elimination of the NCE.

IV. High Temperature Measurements

The measured drain current characteristics of the 3-D MESFET are plotted versus gate-source voltage in Fig. 8 for different temperatures. The threshold voltage of the device varies according to:

$$V_T = V_{T0} - 2K(T - T_0) \quad (2)$$

where $K \approx 1.4 \text{ mV/K}$ [9] (the factor of 2 is due to the dual gates). This temperature dependent threshold voltage shift is the same as for conventional GaAs MESFETs. The 2-D MESFET, on the other hand, has no measurable temperature dependent shift in the threshold voltage [10]. The much weaker temperature dependence of the 2-D MESFET is due to a nearly temperature independent built-in voltage related to the degeneracy of the two-dimensional electron gas. The low-field mobility in the 2-D MESFET also exhibits much less degradation than conventional MESFETs and the 3-D MESFET. This is due to a more effective screening of impurity scattering by the two-dimensional electron gas [10].

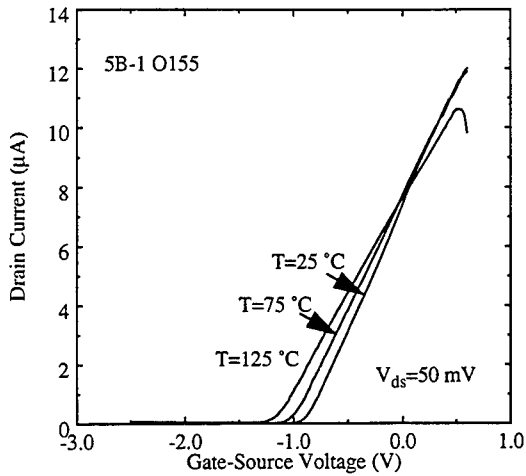


Fig. 8. I_d vs. V_{gs} characteristics of the 3-D MESFET for $T=25, 75,$ and 125 °C.

V. Summary

Two sidewall gate transistors, the hetero-dimensional 2-D MESFET and an ion-implanted 3-D MESFET, were described. The 2-D MESFET has the advantage of a high mobility InGaAs channel and low capacitance due to the 3d metal/2d electron gas interface, while the 3-D MESFET is cheaper to fabricate. The NCE is eliminated in both of these FETs due to the unique sidewall gate geometry. The electrical characteristics of both devices are similar, especially at submicron dimensions. The 2-D MESFET has lower knee voltage, lower output conductance, smaller DIBL shift, higher average transconductance, and a smaller threshold voltage temperature dependence than the bulk device. Also, the extracted Schottky barrier heights were found to be identical for both devices, indicating that there is enhancement of the effective Schottky barrier height in the 2-D MESFET. Overall, the similarities between the two devices indicate that it is possible to combine the idea of the sidewall gate 2-D MESFET with a more conventional, ion-implanted technology. Both the 2-D MESFET and the 3-D MESFET appear promising for low power electronics applications and further study of each is needed.

Acknowledgments

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Table 1: Representative 2-D MESFET and 3-D MESFET parameters

device type	$W_0 \times L_g$ (μm)	V_t (V)	I_{max} (μA)	g_{max} (μS)	$I_{\text{d,leak}}$ (nA)	$I_{\text{g,leak}}$ (nA)	V_{knee} (V)	sub-slope (mV/dec)	DIBL shift (V)
2-D	1.0 x 1.0	-1.7	318	172	19	25	0.53	117	0.18
3-D	1.0 x 1.0	-4.1	310	114	335	466	NA	385	0.35
2-D	0.5 x 0.5	-1.1	165	112	3.7	5.3	0.35	83	.05
3-D	0.5 x 0.5	-1.1	148	118	3.8	4	0.5	87	0.13

Coplanar-Strip Geometry Multiple-Quantum-Well Heterostructure Devices

Steven W. Kirchoefer

Naval Research Laboratory
Washington, DC 20375-5347, (202) 767-2862

Multiple-quantum-well heterostructures exhibit a variety of nonlinear conduction properties which are of interest for high-speed device applications. Conduction measurements on channel devices employing a variety of multiple-quantum-well sequences have shown nonlinear behavior and negative differential conductivity in low-frequency and high-frequency measurements of terminal device characteristics [1]. The responses thus acquired are typically frequency-limited by the parasitic elements associated with discrete device designs. This makes it difficult to experimentally identify the frequency limitations that are due to the carrier transport properties of the intrinsic heterostructure.

A novel device design utilizing an oxide-isolated coplanar-strip transmission line has been used to measure the microwave-frequency properties of conduction nonlinearities in multiple-quantum-well heterostructure devices in a manner which avoids the discrete design parasitics associated with conventional measurement approaches. The dc-bias contacts and conduction channel structures are isolated from the microwave coplanar-

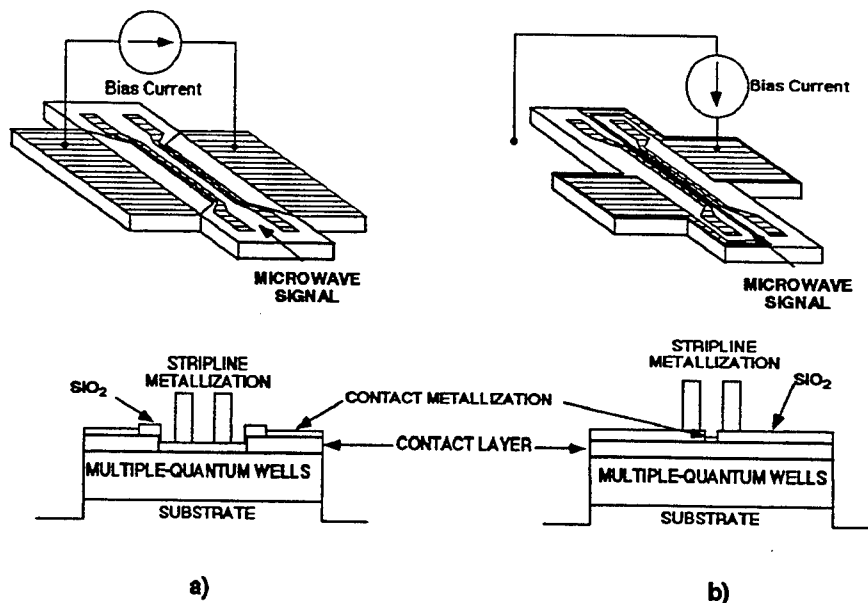


Fig. 1. Coplanar-strip devices for current injection a) parallel and b) perpendicular to the plane of growth. Cross sections through the center of the devices are shown below each diagram.

strip device structures by means of a 300-nm-thick oxide layer. The only interaction between the dc-bias device structures and the coplanar-strip device structures is via the common substrate. Changes in the substrate properties with respect to the coplanar strip that are induced by the dc biasing of the substrate can be determined through this interaction. This arrangement allows one to independently design the coplanar structures, using physical dimensions that are optimal for a 50-ohm-referenced measurement, and independently design the dc-biasing device structures without concern for the introduction of additional microwave parasitics that would be present in a more conventional terminal configuration. Two basic device styles are employed for these measurements. These are shown in Fig. 1. The type shown in Fig. 1a is used in conjunction with heterostructures typically grown on semi-insulating substrates and requiring current flow parallel to the sample surface. The style depicted in Fig. 1b is associated with samples requiring current injection perpendicular to the surface. Both device styles occupy a substrate area of 700 microns by 700 microns. Although the dc-biasing structures differ greatly in geometry, the coplanar-strip portions of these devices are identical and exhibit practically identical zero-bias behavior.

A number of devices have been constructed and tested for various heterostructures. The best data has been obtained from devices fabricated in the form of Fig. 1a [2]. Because of the insulating oxide layer, it is expected that a simple lumped-element model of the coplanar strip would be dominated by a series capacitor. This leads to the conclusion that any conductivity changes in the multiple-quantum wells will be most strongly observed in open-circuit reflection measurements. Fig. 2 shows the results of such measurements made in the frequency range from 50 MHz to 10 GHz. At low frequencies, nearly all of the signal is reflected, resulting in data points near the open-circuit point on the Smith Chart. This is expected, since the oxide layer is capacitive in its effect and presents a

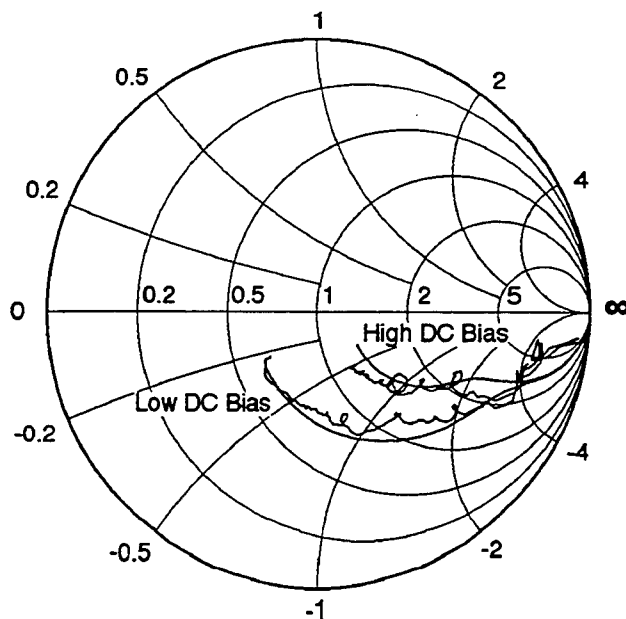


Fig. 2 Reflection data for low (0 volts) and high (40 volts) dc bias levels over the frequency range from 50 MHz to 10 GHz.

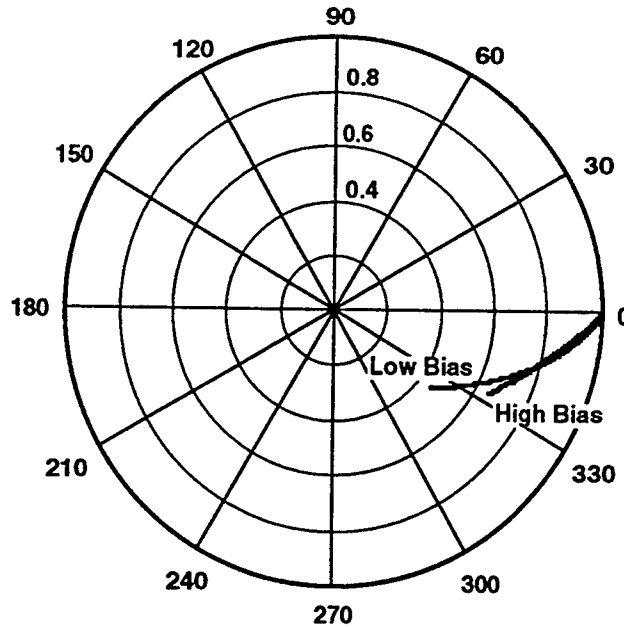


Fig. 3. Equivalent circuit best fit to data for low (0 V) and high (45 V) bias levels for the frequency range spanning 50 MHz to 12 GHz.

high series impedance which reduces the interaction with the quantum-well layers at low frequencies. As the excitation frequency is increased, the data points move toward the center of the chart. Equivalent-circuit-element values representing the data sets for a range of applied bias conditions have been determined. The calculated response obtained from the equivalent-circuit model is shown as a smooth line overlying the data curves of Fig. 2. The bias dependencies of the variable resistance and capacitance are consistent with the dc and low-frequency results, which are assumed to originate from interactions between the heated electron populations in adjacent quantum wells [3].

Interaction between the substrate under bias and the microwave coplanar stripline has been observed in transmission measurements, as shown in Fig. 3. At low frequencies, transmission is near unity, resulting in data points near the unity-transmission point on the transmission coefficient plane. As the frequency is increased, coupling to the substrate through the insulating oxide layer results in microwave signal loss, causing the measured points to move toward the center of the chart. An analysis of the bias-dependent data shows that the microwave losses present at low dc bias are reduced at high dc bias. A standard numerical design model for coplanar lines has been utilized to analyze this observation, and a change in loss tangent from 8 to 5 is observed over the dc bias range of the measurement.

Additional measurements for other quantum-well sequences will be discussed. Numerical calculations using standard field-simulation software will be presented and compared with the experimental data. Circuit models for the measured data will be

included and individual parameter and element variations will be correlated with the conduction properties of the multiple-quantum-well heterojunction structures.

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Corrugated Quantum Well Infrared Photodetector structures for Normal Incidence Light Coupling

C. J. Chen[†], K. K. Choi^{*}, M. Z. Tidrow^{*}, and D. C. Tsui[†]

[†]Dept. of Electrical Engineering, Princeton University, Princeton NJ 08540

^{*}U.S. Army Research Laboratory, Fort Monmouth, NJ 07703

Abstract

In this paper, we report the study of a novel device geometry for quantum well infrared photodetector (QWIP) normal incident light coupling. The new detector structure will be referred as the corrugated QWIP (C-QWIP) structure. In this structure, V-grooves are etched through the active detector region to create a collection of facets within one detector pixel. These facets then direct normal incidence light into the QWIP through total internal reflection. In order to demonstrate the advantages of this light coupling scheme, a two-color C-QWIP covering the two infrared atmospheric windows is used for the study. The experimental data show that while the photoresponse of the detector is maintained to be the same as that of a 45° incidence sample, the dark current density is reduced by more than a factor of two, thus increasing the detectivity. At the same time, no spectral linewidth narrowing or wavelength selectivity is observed, which is critical for multi-color infrared detection.

Long wavelength infrared detection using intersubband transition in AlGaAs/GaAs multiple quantum well (MQW) system has been progressing rapidly during the past several years.¹ Based on a simple theory, one can predict the opto-electronic properties and the potential performance of a quantum well infrared photodetector (QWIP) for a given set of structural parameters.² Consequently, optimized structures can be designed for various functions. However, there is a well-known drawback for these detectors: due to the dipole selection rule, only the light component with electric field perpendicular to the QW planes can be absorbed. Therefore, much effort has been made toward designing an effective light coupler for the normal incidence geometry. Among different light coupling schemes, the 2D grating³⁻⁵ and the random scattering coupler⁶ have been shown to be quite effective in obtaining a high quantum efficiency.

In this paper, we report a study of the novel light coupling scheme in the new detector structure which we refer here as the corrugated QWIP (C-QWIP) structure. In this structure, a large number of V-grooves with slanted sidewalls are etched through the active detector region to create an array of facets within one detector pixel. These facets then direct normal incidence light into the QWIP through total internal reflection. Unlike the conventional gratings which require a thick top contact layer as grating layer, the V-groove structure is fabricated by employing wet chemical etching to create an array of light coupler directly in the active QW region, thus eliminating the requirement of a thick contact layer. Because of the different etching rate for different crystallographic planes, the resultant groove sidewalls are inclined at 54° with the (100) surface along the [01-1] direction, forming a triangular profile as shown in Fig. 1. This corrugated structure substantially reduces the dark current due to the triangular cross-section area in the active region. Because the light coupling mechanism of the C-QWIP is based on total internal reflection instead of the usual diffraction, it couples light of different wavelengths equally into the detector. No spectral linewidth narrowing and wavelength selectivity are thus expected, making this structure superior to the conventional grating. In addition to the formation of

this desirable geometry for total internal reflection, another advantage of wet chemical etching is to avoid the sample damage caused by plasma etching and thus reduce the leakage current considerably. Furthermore, the processing of C-QWIP is much simpler because there are no stringent grating parameters such as periodicity, cavity size, and etching depth, etc to be observed.

To evaluate the performance of this new coupling scheme, a two-color C-QWIP covering both the 3-5 and 8-12 μm atmospheric windows is fabricated. It has two stacks of MQW's in the active region. The first stack has 20 periods of 300-Å $\text{Al}_{0.38}\text{Ga}_{0.62}\text{As}$ barrier and 5-Å GaAs / 25-Å $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ / 5-Å GaAs well. This MQW is designed to have the detection peak at a wavelength $\lambda_p = 4.8 \mu\text{m}$. The second stack consists of 20 periods of 500-Å $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ barrier and 50-Å GaAs well, and λ_p is designed at 9.4 μm . The conduction band diagram of this sample, which has only one bound state in each quantum well, is given in Fig. 2.

Three devices employing three different light coupling structures are characterized. Device C uses a standard 45° incidence coupling. Device B has no special coupling structure. Device A contains a C-QWIP structure, fabricated using a grating mask with a period and an opening width of 7 μm and 2 μm respectively. Inside the QW regions, the light beam follows the path shown in Fig. 1 for all incident angles equal to or greater than the total reflection angle of the air-GaAs interface. This structure allows at least two passes of the light within one single pixel without thinning down the substrate (625 μm in this case) and at least four passes with a thinned substrate. The substrate of the present devices have not been thinned. For the first pass the direction of light propagation is nearly parallel to the QW planes, thus more efficient in light coupling than the 45° incidence case. For the second pass, the coupling is less effective because the propagation is less parallel to the QW planes. On the average, without substrate thinning we can expect a quantum efficiency comparable to that in the 45° incidence sample and two times higher with substrate thinning. No crosstalk between pixels is expected in this new structure.

The dark current of the three devices are measured in a liquid helium dewar. The window photocurrent due to 300 K background radiation is also measured at 10 K with a 36° field of view. Fig. 3 shows the 77 K dark current densities and the window photocurrent densities of all three devices. The dark current densities of devices B and C are almost identical, indicating the high uniformity of the intrinsic detector characteristics. On the other hand, the dark current density of device A is substantially lower, only half that of device B at most at V~9V. This dark current reduction is advantageous in relaxing the charge handling requirement of the read-out circuit. The window photocurrent densities of devices A and C are roughly equal, consistent with the expectation that the light coupling of this C-QWIP without substrate thinning is comparable to that of a standard 45° incidence sample.

In order to compare the spectral efficiency of different coupling schemes, photocurrent spectra are measured using a monochromator with a 1000 K glowbar source. In all measurements, positive bias is applied on the top contact with the bottom contact grounded. At low bias (V<5V), most of the voltage drop is across the 3-5 μm stack due to its larger resistance and only a single detection peak at $\lambda_p = 4.7 \mu\text{m}$ is observed. When the bias increases to 6V, the voltage drop across the 8-10 μm stack becomes appreciable and a second detection peak appears at $\lambda_p = 9.4 \mu\text{m}$. With a further increase in V (V>7V), the

peak at $\lambda_p = 9.4 \mu\text{m}$ becomes dominant. The operating bias is therefore set to be 4V for the short wavelength detection window and 9V for the long wavelength detection window. The responsivity spectra of devices A, B, and C are shown in Fig. 4. The power of the glowbar source is calibrated by a commercial HgCdTe detector. No power correction is made for the reflection from the substrate for all devices, neither is the optical area correction made for the 45° incidence device. Because of the 1D character of the C-QWIP, the photoresponse of device A depends on the polarization direction of the incident light.

In a previous publication⁵, we measured the photoresponse of the same two-color detector with a conventional 2D grating designed for $10 \mu\text{m}$ light coupling. It was found that, in addition to the shortcoming of spectral linewidth narrowing, the light coupling is not as effective in the 3-5 μm window in comparison to the 45° incidence coupling. In contrast, the C-QWIP represented by device A does not show such shortcomings. As clearly shown in Fig.4, the responsivity of device A is 1.2 times higher than that of device C in both detection windows. This result leads to the conclusion that the C-QWIP structure is equally effective in coupling light of different wavelengths, and there is no spectral linewidth narrowing. This optical coupling improvement, together with the dark current reduction, leads to an increase of background limit temperature and an enhancement of detectivity.

Additional improvements can further be made for the C-QWIP structure. By optimizing the detector processing, 2D corrugated patterns can be made, which can double the coupling efficiency. Also, by thinning down the substrate for more passes, the quantum efficiency can be improved by another twofold. Since this new coupling scheme is compatible with the infrared hot electron transistor (IHET) structure, the combined approach should make it possible to have IHET focal panel arrays operable at 90K.

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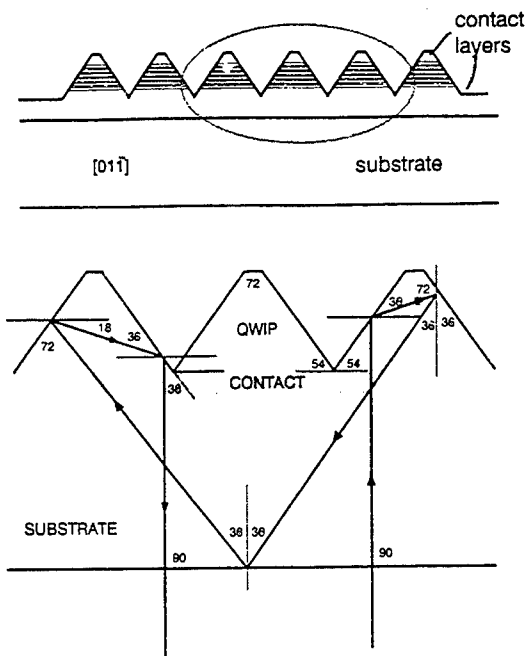


Fig. 1 The upper part shows the triangular cross-section of the C-QWIP. The lower part is an enlargement of the V-grooves, showing the light path inside one single pixel with a thinned substrate.

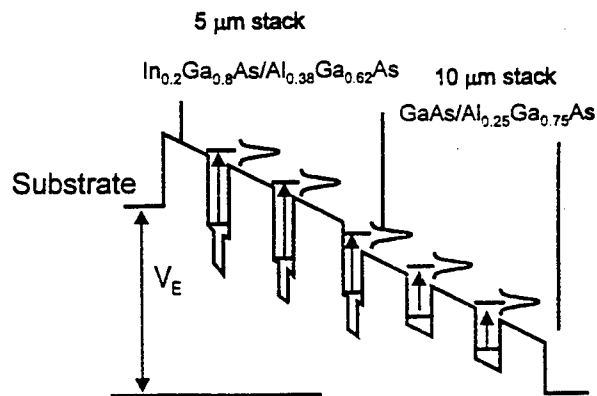


Fig. 2 The energy band structure of the two-color QWIP.

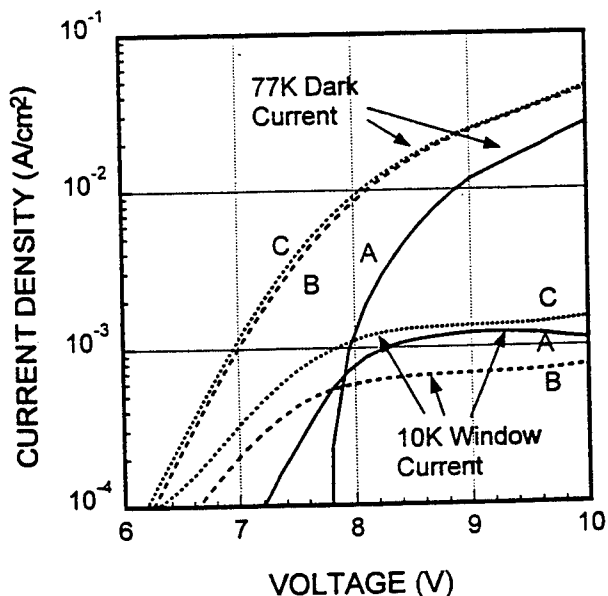


Fig. 3 The 77 K dark current densities and the window photocurrent densities of the two-color QWIP: A the corrugated structure, B normal incidence without any pattern, C the 45° coupling incidence.

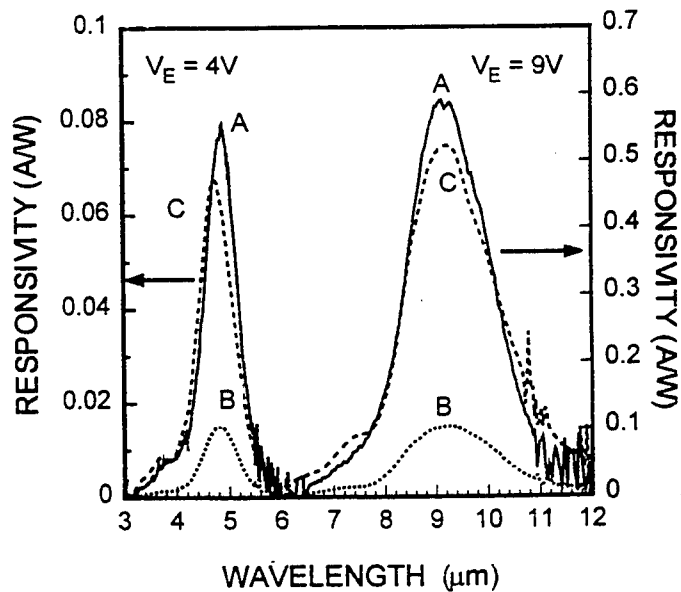


Fig. 4 The responsivity of the two-color QWIP: A the corrugated structure, B normal incidence without any pattern, C the 45° coupling incidence.

The Silicon Hot Avalanche Injection Transistor (HAIT)

G. Müller, G.A.M. Hurkx, W.B. de Boer, R. Dekker, W.T.A. van den Einden, and M.J.J. Theunissen
Philips Research Laboratories, Prof. Holstlaan 4, 5656 AA Eindhoven,
The Netherlands

The speed of bipolar transistors is limited by high injection effects [1]. To achieve high cut-off frequencies unipolar hot carrier transistors are an attractive alternative [2,3]. Here we describe results of a novel fast hot carrier transistor with an Impatt-diode structure as emitter resulting in an inductive impedance. This device offers high speed without the disadvantage of the capacitive impedance of the previously mentioned transistors.

As it is shown in Fig. 1, by biasing a silicon n^+pp^+ -diode into Avalanche breakdown, a high differential conductance, which is limited by the space-charge resistance, is found. This conductance under reverse bias in this regime can be larger than the conductance of the forward biased diode. In addition it is well known, that the imaginary part of the impedance of an Impatt-diode is inductive for frequencies below the resonance frequency [1,4]. Taking the Impatt-diode as the emitter-base junction of the Hot Avalanche Injection Transistor (HAIT), the second building block of the HAIT consists of a planar doped n^+ -barrier layer, electrically separating the p^+ -base layer from the p-collector. In Fig. 2 the calculated electrostatic potential is shown. In order to contribute to the collector current, the holes generated by impact ionization in the high field region of the emitter-base junction under reverse bias, have to overcome the planar doped potential barrier. If they loose too much energy and can therefore not reach the collector, the base current increases resulting in a low current gain. Since with an Impatt-diode as hot current injector, high injection energies can be realized, reasonable current gains can be expected.

To investigate the high frequency performance we have analyzed an equivalent circuit of the HAIT (Fig. 4). First the total current through the Impatt-diode I_{Impatt} is determined from the impedance of the Impatt-diode. The hot carriers (I_{hot}), which reach the collector are modelled as a certain fraction of the conduction current of the Impatt-diode. The current carried by generated carriers, that have lost so much energy, that they cannot reach the collector, is then given by $I_{Impatt} - I_{hot}$. Using realistic values for all the parameters, Fig. 5 demonstrates, that high cut-off frequencies can be achieved.

To avoid substantial energy relaxation of the hot holes, which would deteriorate the current gain, the distance between the place of Avalanche generation and the top of the barrier (Fig. 2) has to be as short as possible. This requires a steep junction between the narrow p^+ -base and the planar doped n^+ -barrier, making low temperature processing an absolute necessity. The highest processing temperature after the growth of the wafers was 400°C . Another technological challenge is the etching of the contacts to the 20nm thick base layer. In order to increase the selectivity of the KOH-etching of the contacts to the base, the major part of the base layer consists of $\text{Si}_{0.85}\text{Ge}_{0.15}$ (Fig. 3).

The HAITs were fabricated on 6" silicon wafers, grown at atmospheric pressure in an ASM Epsilon One epitaxial reactor (Fig. 6). First a deep mesa structure is etched down to the substrate in order to electrically isolate the active regions of the different

transistors. Then by selectively etching a shallow mesa on top of the deep mesa down to the base layer the emitter is defined. For masking and as insulating layer a 350° PECVD-TEOS silicon oxide was used. The SIMS profile of one of the wafers (Fig. 7) demonstrates, that the necessary steep junctions between highly doped layers were obtained. The dc-characterization of a HAIT with an emitter length of 20 μm and an emitter width of 1.5 μm is shown in the Figs. 8-9. The measured IV-traces of the two building blocks of the HAIT, the emitter-base Impatt-diode and the base-collector camel diode indicate a successful selective etching of the base contact (base sheet resistance < 10k Ω). The leakage current of the base-collector junction is negligible up to a voltage of 8V across the potential barrier. The low current gain of the HAIT ($h_{fe} = 0.35$, Fig. 9) is due to a large built in barrier height, which cannot be changed experimentally by applying a voltage across the barrier. A calculation of the barrier height (Fig. 10) for this structure (Fig. 3b) confirms that for a 15nm thick planar doped barrier of 10¹⁹cm⁻³ the barrier can not be depleted up to voltages of 15V resulting in a fixed barrier height of $\approx 1V$. By choosing a lower doping concentration of 5 · 10¹⁸cm⁻³ we expect a substantially higher current gain. To demonstrate that the observed current gain is due to hot carriers and not due to parasitic effects, we have compared the "cold" carrier current gain with the hot carrier current gain (Fig. 11-12). Using transistor structures with two separate base contacts the "cold" carrier current gain was determined by injecting the current in one of the two base contacts (current injection lateral to the barrier, inset Fig 11). The hot carrier current gain measured at the same device (Fig. 12) is found to be 10⁶ times larger.

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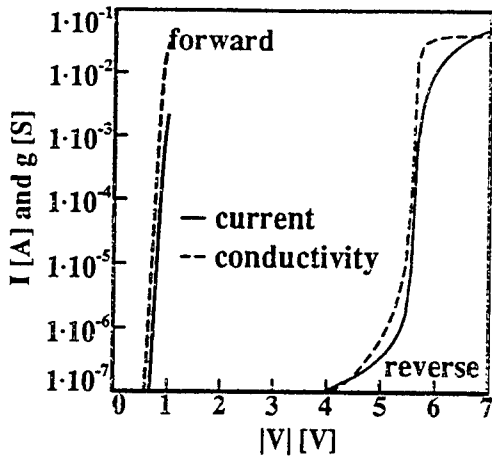


Fig. 1. Current and differential conductivity as function of the applied voltage for an n^+pp^+ -diode. Avalanche breakdown for the reverse biased diode occurs at $\approx 5.5V$.

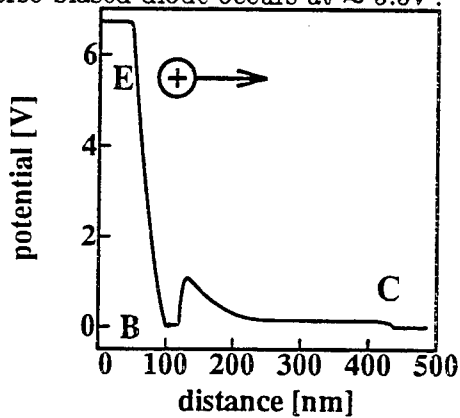


Fig. 2. Electrostatic potential of the HAIT as function of the distance from the surface for the design of Fig. 3a. E, B and C denote the emitter, base and collector of the transistor. The breakdown voltage ($-5.6V$) is applied to the emitter-base junction, $V_{bc} = 0$.

	E	a)	b)
		50nm nSi $3E19cm^{-3}$	
		50nm pSi $2E18cm^{-3}$	25nm nSi $3E18cm^{-3}$
		15nm pSi $3E18cm^{-3}$	
		5nm pSi $4E19cm^{-3}$	
base		15nm pSiGe $x=0.15$ $4E19cm^{-3}$	
barrier		15nm nSi $1E19cm^{-3}$	
		300nm pSi $1E17cm^{-3}$	
		50nm pSi $3E19cm^{-3}$	
		C	

Fig. 3. Doping concentrations and layer thicknesses of the HAIT with an n^+ -emitter on top, a 20nm thick p^+ -base, then the 15nm thick n^+ -barrier and the p^+ -collector at the bottom.

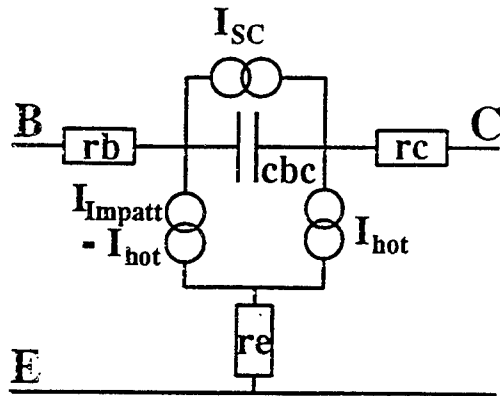


Fig. 4. Equivalent circuit of the HAIT with r_e , the emitter resistance, r_b , the base resistance, r_c , the collector resistance, and c_{bc} the base-collector depletion capacitance. The current source I_{sc} takes the finite transit time through the base-collector depletion layer into account.

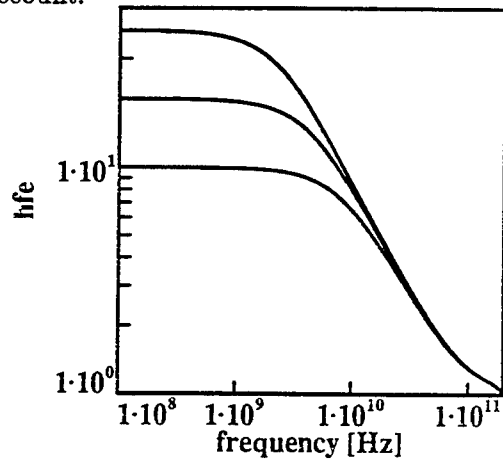


Fig. 5. Calculated common emitter current gain as function of the frequency for the equivalent circuit of the HAIT (Fig. 4). The lines correspond to different dc current gains.

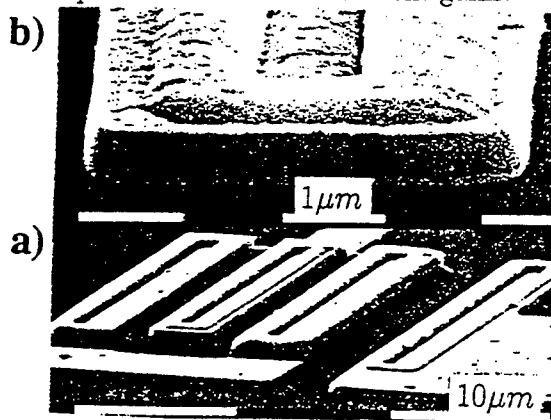


Fig. 6. a) SEM of the HAIT with b) the emitter finger (contact hole and shallow mesa).

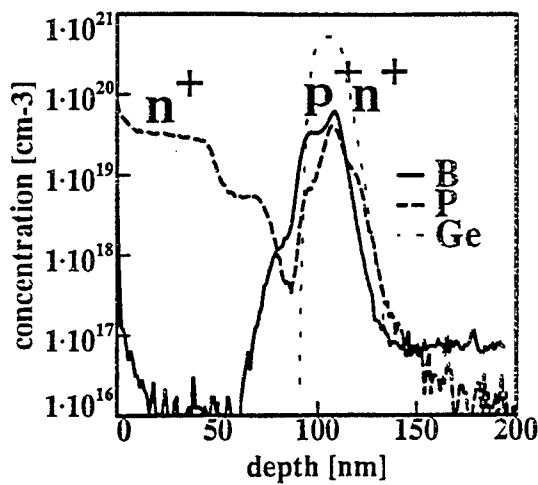


Fig. 7. SIMS profile of the wafer, grown according to the design of Fig. 3b. The boron (p-type doping), phosphorus (n-type doping) and germanium concentrations are shown as function of the distance from the surface. The very steep and narrow P-'shoulder' at a depth of 120nm produces the potential barrier.

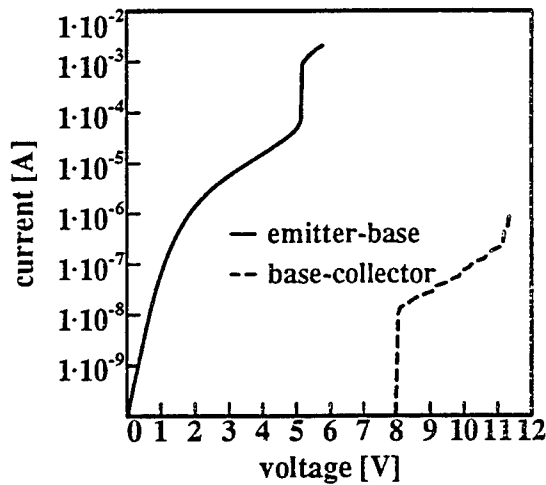


Fig. 8. Measured current-voltage characteristics. Avalanche breakdown of the reverse biased emitter-base junction occurs at $\approx 5V$.

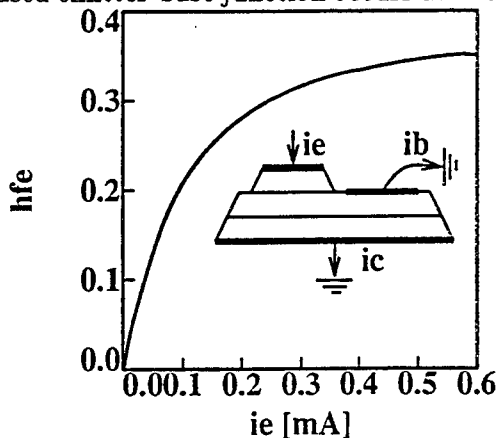


Fig. 9. Measured dc current gain as function of the injection current. The biasing of the device is indicated in the inset.

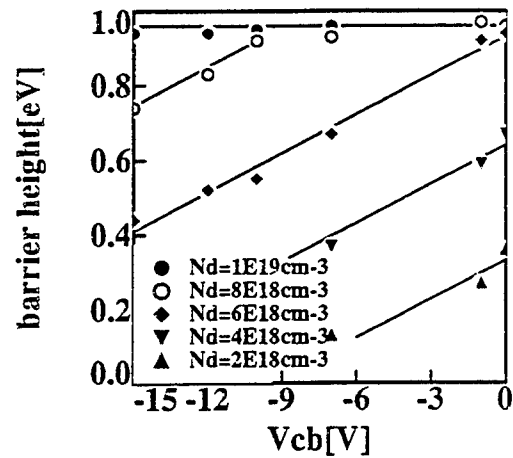


Fig. 10. Calculated barrier height as function of the voltage across a 15nm thick n-type barrier for different doping concentration of the barrier.

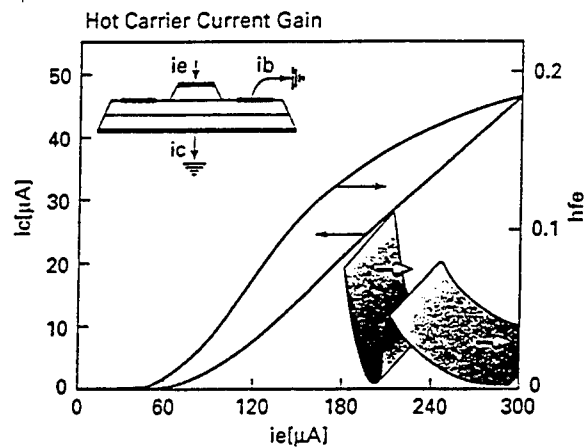


Fig. 11 Collector current and "cold" carrier current gain as function of the current injected into one of the two base contacts.

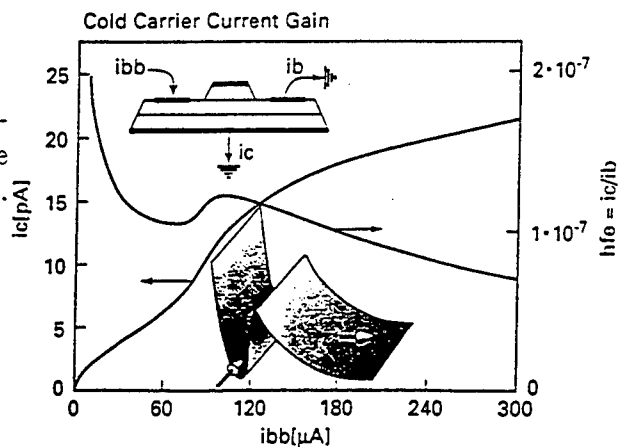


Fig. 12. Collector current and hot carrier current gain as function of the current injected into the emitter.

The Design and Performance of the Uniphase CMCCD and Its
Possible Application as an Analog Memory

L.Chen and H.L.Kwok, Dept. of Electrical & Computer Engg.,
University of Victoria, Victoria, BC Canada V8W 3P6

The first charge-coupled device (CCD) [1] was proposed by Boyd and Smith in 1970 and since then it has found its way in numerous important electronic applications. The principle of operation of a CCD is relatively simple and it relies on the electron transfer between the neighboring MOS gates or Schottky gates in the device. To facilitate an efficient charge transfer, normally, submicron gaps between the transport gates are required and this, sometimes, poses a reliability problem. More recently, resistive-gate charge-coupled devices (RGCCDs) [2] have been used to offset this requirement on submicron gaps and high-efficient RGCCDs (with a charge transfer efficiency of 0.998 or better) have been fabricated. In addition, since cermet is the material most frequently used for the resistive gates, RGCCDs are also called cermet-gate charge-coupled devices (CMCCDs). This work may be divided into three parts. The first part deals with the structural optimization and the performance of the uniphase CMCCD. The second part investigated the effect of the clock voltages and their waveforms on the performance of the devices. Finally, in the last part, we investigated the linearity and noise in the CMCCD in light of its possible application as an analog memory.

Numerous work have been performed on the modeling of CCDs and CMCCDs and the basic charge transfer operation is well understood. The key mechanisms are due to the self-induced drift, the fringing field and the thermal diffusion. Both analytical models as well as equivalent-circuit models have been studied. The later are claimed to offer a better computational efficiency when compared with the analytical models [3]. One clear advantage of the equivalent-circuit model is in its application for the study of transient voltage effects. Fig.1 shows a cross-section of a uni-phase CMCCD. The geometrical parameters as are $X = [L_1, L_g, x_t]$. To optimize device performance, we can set up of an objective function which in our case is chosen to be the error function:

$$\hat{e}(X) = \frac{\sum_{j=0}^{M-1} (\Phi_{\max}(j) - \Phi_{\max -i}(j))^2}{M} \quad (1)$$

where M is the number of grids used in the direction of charge transfer, $\Phi_{\max}(j)$ is the potential maximum profile in volt in the direction of the charge transfer, and Φ_{\max}

$\phi_{-i}(j)$ is the "ideal" potential maximum profile in volt in the direction of the charge transfer.

ϕ_{\max} is determined by solving the two-dimensional Poisson equation in the channel and $\phi_{\max -i}$ is the ideal profile determined for maximum charge storage. By minimizing $\hat{\epsilon}(X)$ with respect to the geometrical parameters, we can obtain ϕ_{\max} closest to $\phi_{\max -i}$. This can be done using the Fletcher-Reeves method [4]. The optimized profiles of ϕ_{\max} are plotted in Fig.2. Table I lists the theoretical charge transfer efficiencies of the optimized CMCCDs at different transfer times. The initial charge size was $5 \times 10^{11} / \text{cm}^2$.

<u>Transfer Time (ps)</u>	200	400	600	800	1000
<u>Efficiency</u>	0.6490	0.8531	0.9514	0.9884	0.9990

Table I

As observed, the optimized structure can theoretically operate at a charge transfer efficiency of 0.999 up to 1 GHz. At a higher clock frequency, the charge transfer efficiency will decrease due to velocity saturation. The charge transfer efficiency versus the charge density and the peak clock voltage are shown in Figs.3 and 4. As expected, the charge transfer efficiency will fall-off rapidly when either the charge density is too high (due to spill-over from the potential wells) or when the peak clock voltage is too large (due to the presence of energy "troughs"). The rise time of the clock voltage τ_{rise} is often considered to be an important parameter in determining the charge transfer efficiency [5]. Fig.5 compares the charge transfer efficiencies resulting from different values of τ_{rise} as a function of the transfer time t_{tf} for the uniphase CMCCD. As expected, the effect of the rise time is more pronounced in the later part of the transfer process (when the self-induced drift effect has subsided). A small τ_{tf} apparently will allow the fringing field to be established more quickly and that will facilitate charge transfer. The linearity of the CMCCD depends primarily on the input and the output (I/O) structures. Fig.6 shows the measured transfer characteristics. As expected, good linearity can be observed over a reasonable dynamic range (0 - 0.5 V) up to about 50 MHz.

In an analog device, noise will frequently limit the performance and in the CMCCD, the main noise contributions are due to thermal generation, bulk trapping and the I/O structures. The noise figures (expressed in equivalent number of electrons) from the various sources are listed in Table II together with the equations used for their estimation. Assuming that the maximum charge storage is given by the product of the depletion layer capacitance and the value of the potential well, it can be shown that the maximum charge

storage is $6.0 \times 10^5 e^-$. Fig.7 shows the measured signal-to-noise ratio of a GaAs CMCCD as a function of the clock frequency.

Noise source	Equation	Two-phase CMCCD	Uni-phase CMCCD
Thermal generation [12]	$n_{th} = \sqrt{(J_d A_c N_T)/(q f_c)}$	31 e^-	32 e^-
Bulk trapping [13]	$n_{trap} = \sqrt{N_T V_{SIG} N_t \times \sqrt{\exp(-T_t/\tau_e)[1 - \exp(-T_t/\tau_e)]}}$	36 e^-	51 e^-
Input [13]	$n_{input} = \frac{1}{q} \sqrt{KTC_{inp}}$	179 e^-	179 e^-
Output [13]	$n_{output} = \frac{1}{q} \sqrt{KTC_{op}}$	127 e^-	127 e^-
Total noise		373 e^-	389 e^-
Max. charge size		$8.6 \times 10^5 e^-$	$6.0 \times 10^5 e^-$
S/N ratio	$20 \log(Q_{max}/Q_{noise})$	67 dB	63 dB

Table II

In general, CCDs are used primarily for signal processing and as imagers. A novel application of the CCD is to use it as an analog memory. For instance, a 100 pixel CCD with a charge transfer efficiency of 0.9999 connected in a closed loop will experience only 10% signal degradation after 10 cycles and theoretically, this is often adequate for a number of analog signal processing applications such as the case of adaptive learning in neural nets [6]. Fig.8 shows schematically a CMCCD configured to operate as an analog memory. The purpose of the level-shift circuit is restore the dc voltage levels and Fig.9 shows the photomicrograph of the measured output waveforms for a sinusoidal input. As observed, other than for the minor signal distortion, the output is a good replica of the input.

Acknowledgement: The authors like to express their appreciation to NSERC Canada and Micronet, NCE Canada for their support. The technical support of TRIUMF is much appreciated.

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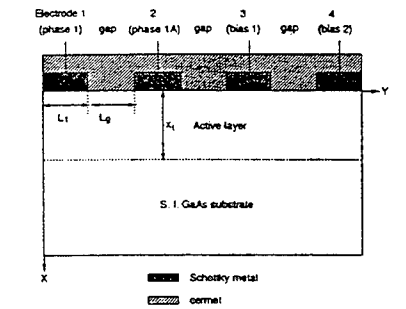


Figure 1

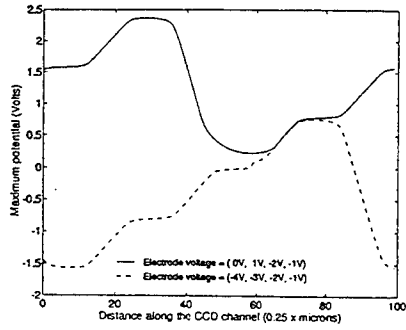


Figure 2

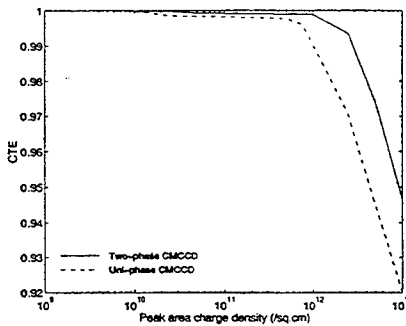


Figure 3

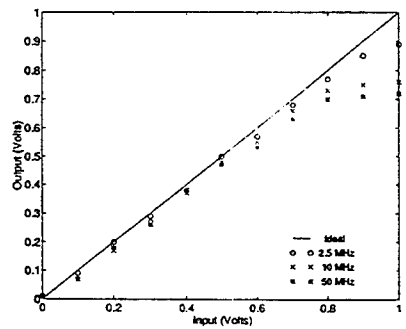


Figure 4

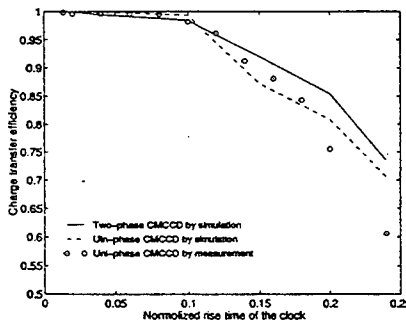


Figure 5

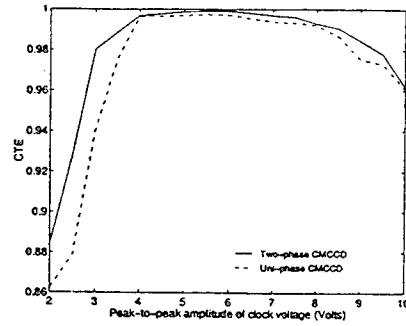


Figure 6

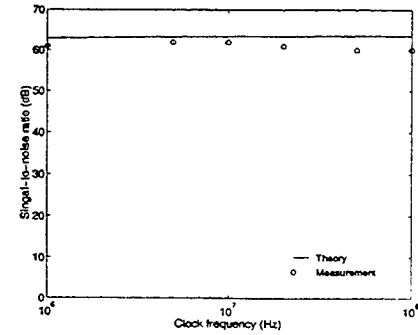


Figure 7

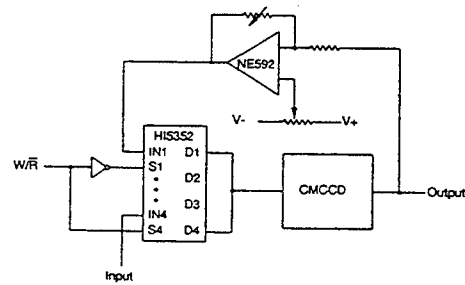


Figure 8

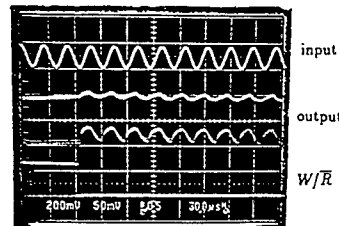


Figure 9

EFFECT OF PULSED FIR LASER RADIATION ON TUNNEL AND CHANNEL RESISTANCE OF δ -DOPED GaAs

I.N. Kotel'nikov, A.Ya. Shul'man, N.A. Mordovets, N.A. Varvanin
Institute of Radioengineering and Electronics of the Russian Academy of Sciences
Moscow 103907, Russia

S.D. Ganichev¹⁾

A.F. Ioffe Physico-Technical Institute of the Russian Academy of Sciences
St.-Petersburg 194021, Russia

B. Mayerhofer, and W. Prettl

Universität Regensburg, Institut für Experimentelle und Angewandte Physik,
93040 Regensburg, Germany

Investigations of the fast response of Schottky-barrier tunnel junctions (SBTJ) to high power pulsed FIR laser radiation have shown that under the condition of plasma reflection the change in the junction resistance is connected with a deformation of the self-consistent potential barrier [1-3]. This deformation is caused by radiation pressure on the free electron plasma in the semiconductor. The observed photoresistive effect allows to consider SBTJ as a detector of pulsed FIR laser radiation with high temporal and spatial resolution [4]. The two-dimensional electron gas (2DEG) in the potential well of the δ -doped semiconductor represents a similar system with a self-consistent potential. The properties of this system depend on the redistribution of free carriers in the direction perpendicular to the plane of the δ -layer. This work presents the first results of photoresponse experiments with δ -doped GaAs structures.

The investigated samples consist of MBE grown GaAs with one δ -layer, 5 mm long and 1 mm wide, at a distance of 20 nm from the semiconductor surface. The donor atoms are Si with a density of $6 \cdot 10^{12} \text{ cm}^{-2}$. The 2DEG density is $3 \cdot 10^{12} \text{ cm}^{-2}$ due to the spatial redistribution of carriers between the surface states and the δ -layer.

Two different types of samples were used: structures with a plain GaAs surface and structures with an aluminum gate. In gated samples the current through the Schottky barrier between the gate and the channel is carried by tunneling electrons. Investigations of the samples at 4.2 K temperature have shown, that the tunneling-spectroscopy and magneto-transport data are in a good agreement with the results of self-consistent calculations of the energy structure of two-dimensional subbands in a δ -doped layer of 5 nm thickness [5].

The radiation sources used were pulsed NH_3 and CH_3F molecular lasers optically pumped by a

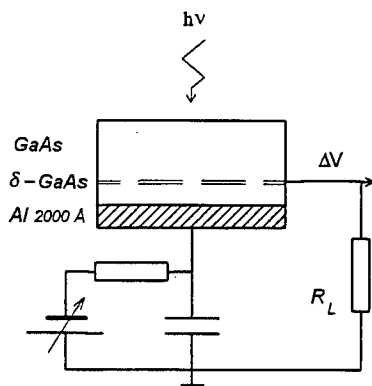


Fig. 1. Scheme of measurements

TEA CO_2 laser providing ≤ 100 ns pulses. The measurements have been carried out at the wavelengths λ of 90.55 μm and 250 μm . The maximum intensity of radiation in the sample was 1 MW/cm^2 . For varying the intensity calibrated teflon attenuators have been used. The intensity incident on the sample has additionally been controlled by a fast photon drag detector.

The gated samples have been irradiated from the substrate side. The photoresponse measurements of gateless samples have been performed with irradiation on the δ -layer side. It was proved that the magnitude of the signal is only slightly smaller when the substrate side is irradiated. Fig. 1 shows a sketch of a sample and the measurement scheme.

¹⁾ Present address: Universität Regensburg, Institut für Experimentelle und Angewandte Physik, FRG

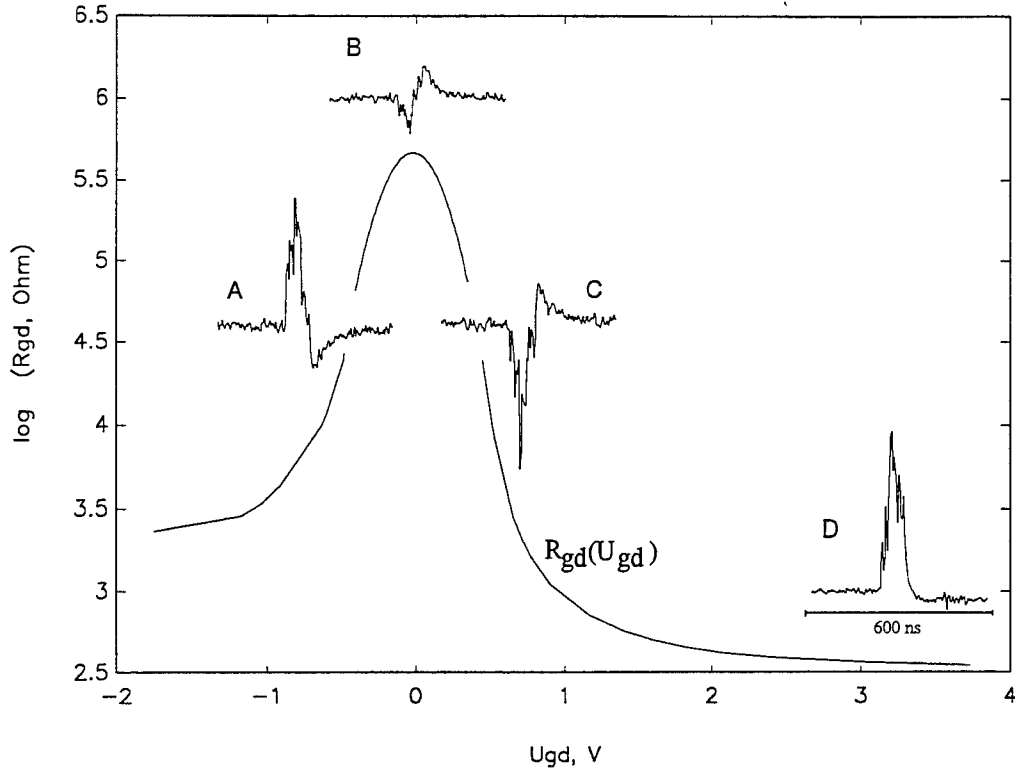


Fig. 2. Gated structure. Photoconductive response (A, C, D) at different gate voltages and photo-e.m.f. (B) due to the FIR laser pulse (duration 100 ns, $\lambda=250$ μm). The sample temperature is 77 K. Corresponding gate voltages are $U_{gd} = -0.48$ V (A), 0 V (B), 0.45 V (C), and 3.73 V (D). The resistance R_{gd} versus the gate voltage is also shown. The same results were observed for $\lambda=90.55$ μm .

A fast response has been observed with a time constant smaller than the laser pulse duration. Signal pulses are displayed in Fig. 2 for different gate voltages U_{gd} . Note that the response in the unbiased case ($U_{gd} = 0$) is a voltaic signal indicating a spatial redistribution of free charges.

The response at $U_{gd} \neq 0$ changes its sign when the sign of the bias voltage is changed. This means that the response is due to a change in the conductance of the structure at $U_{gd} \neq 0$, i.e., it is a photoconductivity effect. The sign of the photoconductivity reveals that during the laser pulse the conductance decreases at low bias and increases at high bias. Radiation heating of 2DEG in δ -doped layer would result in an increase of the tunnel junction conductivity, since the latter rises about ten times with increasing sample temperature from 77 to 300 K.

Thus, we conclude that the low-bias response is of non-thermal origin. However, it must be noted that at low bias the dominant negative component of photoconductivity is followed by a small positive tail, which may be due to electron heating effects.

At low bias voltage, $U_{gd} < 0.5$ V, the resistance R_{gd} between the gate and the δ -layer is about 100 times higher than the channel resistance measured directly. Thus, the response at low bias should be considered as the result of a decrease of the tunnel conductance during the laser pulse. Such a sign of the observed photoconductivity in the gate-channel tunnel junction is completely different from what has been observed in usual tunnel junctions with Schottky barriers where the photoconductivity is always positive [2-3].

The change in the sign of the photoconductivity with the increase of the bias voltage may be related to the crossover from the tunnel junction resistance, decreasing exponentially with the bias, to the channel resistance. This can be seen from the resistance-voltage characteristic shown in Fig. 2, where the resistance assumes an approximately constant value for bias voltages $U_{gd} > 2$ V.

To clear up the origin of the response of the gated structure at high bias voltage, the photoresponse of the structure without gate has been measured. It turned out that the response observed in the gateless structure is very similar to the response of the tunnel structure at large bias voltages and both should be related to an increase of the channel conductance.

This fast positive photoconductivity of the channel could qualitatively be explained by electron heating. To check this assumption, the temperature dependence of the channel resistance must be known. We have measured the channel resistance as a function of the lattice temperature under different conditions: a) in the dark, b) the sample permanently illuminated by visible light, c) after illumination switched off (persistent photoconductivity). It is of interest that a long-time signal tail of opposite sign occurs under the condition of steady-state illumination with visible light, in addition to the fast positive photoresponse (Fig. 2, curve D). However, this will not further be considered here since the fast channel response related to 2DEG mobility change does not depend on the illumination conditions which affect mainly the 2DEG density.

To test the assumption about the thermal origin of the fast photoresponse of the δ -layer, measurements of the dependence of the channel photoconductivity on the intensity of laser radiation have been carried out at various sample temperatures in the range of 77-300 K. The illumination by external visible light was rejected with a black polyethylene film, when it was necessary. It was found that the values of the fast photoresponse in darkness and under persistent photoconductivity condition are identical despite the large difference of the temperature dependencies of the channel resistance in these two cases. Therefore, in the following the data obtained under dark conditions are discussed only.

Fig. 3 shows the temperature dependence of the response. The magnitude of the response drops by two orders of magnitude in a range where the temperature increases about by a factor of three. This behaviour can be attributed to an exponential factor like $\exp(-\hbar\omega_0/kT)$ in the electron energy loss rate ($\hbar\omega_0=36.5$ meV is the energy of longitudinal optical (LO) phonons in GaAs). As known, such a term is present in the expressions for the electron energy loss rate due to scattering by LO phonons irrespectively of the possible heating of the LO phonons (see for example [6]).

To analyze the heating effects in 2DEG it is necessary to know the electron distribution in two dimensional subbands. Following [5] we have obtained the value of the Fermi energy, $E_F \approx 93$ meV for the lowest subband and 17 meV for first excited subband. A rigorous treatment of hot 2D electrons, taking into account the subband filling, is quite cumbersome. Therefore as a first

approach, we have analyzed the measured photoresponse in a one-subband approximation. Effective parameters of the 2DEG were taken from Hall measurements.

The density of 2DEG in our samples is high enough that the electron temperature approximation can be applied. As known, in GaAs at temperatures > 50 K the energy of hot electrons is transferred to the lattice due to the emission of LO phonons. In this case the expression for the energy loss rate per electron can be written in the form:

$$P = \hbar\omega_0 v_e [\exp(-\frac{\hbar\omega_0}{kT_e}) - \exp(-\frac{\hbar\omega_0}{kT})] \quad (1)$$

where v_e is the effective emission frequency of LO-phonon by electrons, T_e and T are the temperature of electrons and the lattice at equilibrium, respectively. It can be rigorously proved that Eq. (1) is valid in the case of LO-phonon heating, too.

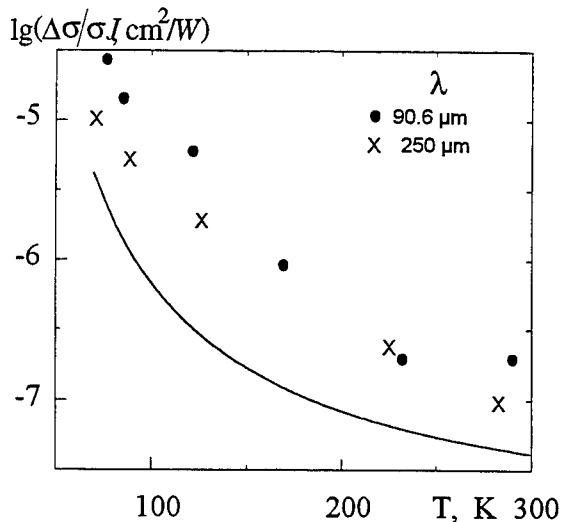


Fig. 3. Gateless structure. Temperature dependence of the relative photoconductivity $\Delta\sigma/\sigma$ normalized to the intensity J at two wavelengths. The solid line shows the $\exp(-\hbar\omega_0/kT)$ behavior.

Using the data shown in Fig. 3, we have determined the magnitude and temperature dependence of the emission frequency ν_e . It takes a value of the order of 10^{12}s^{-1} at 77 K and of 10^{13}s^{-1} at room temperature. It could be verified that these values of ν_e give the correct order of the measured electron energy loss rate in GaAs as a function of T_e (see, for example, [7]) and the cooling rate of hot LO phonons due to the coupling with acoustical phonons [8]

Hence, the presented data show that the channel photoconductivity of δ -layers is stipulated by electron heating owing to the absorption of radiation by free carriers but the photoresponse of the tunnel junction is not due to hot-electron effects.

It seems likely that the decrease in tunnel conductance observed under the action of radiation can be related to a change in the shape of the self-consistent barrier-well potential due to the ponderomotive force of the electromagnetic wave, just as it was found in the case of tunnel Schottky-barrier junctions [3]. However, the momentum transfer from the radiation to electrons of the δ -layer may be provided here by the magnetic field of the free carrier current (like pinch-effect) instead of the free carrier plasma reflection of the radiation in the bulk of the semiconductor. To explain the observed phenomena, the change in the shape of the δ -layer potential well must be taken into account. This change is caused by ponderomotive forces in the nonuniform field of the reflected electromagnetic wave near the GaAs surface.

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Harmonic Generation in Bloch Miniband Transport Across a Quantum Wire Superlattice Subject to a Strong AC Signal

X.L. Lei^{1,2}, N.J.M. Horing², H.L. Cui², and K.K. Thornber³

¹State Key Laboratory of Functional Materials for Informatics
Shanghai Institute of Metallurgy, Chinese Academy of Sciences
865 Chang Ning Road, Shanghai, 200050, China

²Department of Physics and Engineering Physics

Stevens Institute of Technology Hoboken, New Jersey 07030

³NEC Research Institute, 4 Independence Way, Princeton, New Jersey 08540

We examine vertical Bloch miniband transport in a GaAs-based superlattice of quantum wires arrayed on a plane, following similar recent studies of planar quantum-well superlattices¹ and quantum-dot superlattices². In particular, we determine the current due to a dc field E_0 which may drift the system into the regime of negative differential mobility, jointly with a perturbing single-frequency electric field $E_\omega \sin(2\pi t/T_\omega)$. We consider $E_\omega \sim E_0$, so that the perturbing ac field is strong, and the responding steady periodic miniband current exhibits distortion and harmonic content beyond the impressed single frequency, characteristic of nonlinear time-harmonic generation.

Our nonlinear balance equation formulation takes account of strong electron-electron interactions which tend to rapidly thermalize the system about the center-of-mass motion, and which dynamically, nonlocally screen the scattering interactions. In our treatment of the latter, we employ a realistic microscopic description of random impurity, acoustic phonon and polar optic phonon scatterings in momentum and energy balance equations. Our model quantum wire superlattice consists of periodically spaced potential wells and finite-height barriers in the z -direction. In the lateral plane, wire definition is achieved by electron confinement within a distance d_x in the x -direction, while the electrons move freely in the y -direction. Thus the electron energy dispersion can be written in the form ($\hbar = 1$)

$$\varepsilon_{n,k_y}(k_z) = \varepsilon_{n,k_y} + \varepsilon(k_z), \quad (1)$$

where

$$\varepsilon_{n,k_y} = \varepsilon_n + \frac{k_y^2}{2m}, \quad (2)$$

and m is the effective mass in the y -direction and ε_n represents quantized lateral subband energies for confined electron motion in the x -direction. Furthermore, we employ a tight-binding approximation for the lowest z -miniband energy

$$\varepsilon(k_z) = \frac{\Delta}{2}(1 - \cos k_z d), \quad (3)$$

where d is the superlattice (SL) period, Δ is the miniband width, and $-\pi/d < k_z \leq \pi/d$.

The momentum and energy balance equations are most conveniently described in terms of the average drift velocity v_d

$$v_d = \frac{2}{N} \sum_{n,k_y,k_z} \frac{d\varepsilon(k_z)}{dk_z} f(\varepsilon_{n,k_y}(k_z - p_d), T_e), \quad (4)$$

(N is the total number of electrons) and the average electron energy

$$h_e = \frac{2}{N} \sum_{n,k_y,k_z} \varepsilon_{n,k_y}(k_z) f(\varepsilon_{n,k_y}(k_z - p_d), T_e). \quad (5)$$

In these terms, the momentum balance (expressed in terms of v_d) is given by ($v_m = \Delta d/2$)

$$\frac{1}{v_m} \frac{dv_d}{dt} = eE(t)d\alpha(T_e) \cos(p_d d) + \frac{2}{\Delta d} (A_i + A_p), \quad (6)$$

and the energy balance is

$$\frac{2}{\Delta} \frac{dh_e}{dt} = eE(t)d\alpha(T_e) \sin(p_d d) - \frac{2W}{\Delta}, \quad (7)$$

where $\alpha(T_e)$ depends on the electron temperature T_e , to the exclusion of the center-of-mass drift momentum p_d , and it is given by

$$\alpha(T_e) = \frac{2}{N} \sum_{n,k_y,k_z} \cos(k_z d) f(\varepsilon_{n,k_y}(k_z - p_d), T_e). \quad (8)$$

Above, $f(\varepsilon, T_e)$ is the Fermi-Dirac distribution at the electron temperature T_e , with chemical potential μ . The detailed expressions for the frictional decelerations A_i and A_p induced by impurity and phonon scatterings, respectively, and the energy transfer rate W from electrons to phonons, were derived in Ref. 3, using a realistic 3D microscopic treatment of acoustic and polar optic phonon and random impurity scatterings. In the interest of brevity, we refer the reader to Ref. 3 for these formulae.

As indicated above, we treat quantum wire SL miniband transport driven by an electric field of the form

$$E(t) = E_0 + E_\omega \sin(\omega t), \quad (9)$$

where the dc component E_0 drifts the miniband current and E_ω is the magnitude of the large superposed ac signal field. The resulting high frequency steady state drift velocity v_d (current) and electron temperature T_e are periodic functions of time with period $T_\omega = 2\pi/\omega$. However, they are not simple periodic functions as they suffer distortion due to harmonic generation in their highly nonlinear environment. Nonetheless, their periodicity permits analysis in terms of a Fourier series in time, of the form

$$v_d(t) = v_0 + \sum_{n=1}^{\infty} [v_{n1} \sin(n\omega t) + v_{n2} \cos(n\omega t)]. \quad (10)$$

The dc component v_0 and the harmonic coefficients v_{n1} and v_{n2} are given by

$$v_0 = \frac{1}{T} \int_0^T v_d(t) dt, \quad v_{n1} = \frac{2}{T} \int_0^T v_d(t) \sin(n\omega t) dt, \quad v_{n2} = \frac{2}{T} \int_0^T v_d(t) \cos(n\omega t) dt. \quad (11)$$

The particular quantum wire superlattice treated here is a periodic array of quantum wires on a plane having period $d = 10nm$, lateral confinement within $d_x = 45nm$, 2D density $N_s = 6.75 \times 10^{15}/m^2$, low-field dc mobility $\mu(0) = 1.0 m^2/Vs$ at lattice temperature $T = 300K$ and miniband width $\Delta = 900K$. The driving field is $E(t) = E_0 + E_\omega \sin(2\pi t/T_\omega)$ with $T_\omega = 0.4ps$, $E_0 = 12kV/cm$ and $E_\omega = 10kV/cm$. Using parameters appropriate to GaAs (four transverse subbands are included in the calculation), we determine the periodic (but not simple harmonic) miniband drift velocity as a function of time, exhibited in Figure 1, where the nonlinear generation of higher harmonic content is manifested in substantial distortion associated with higher Fourier coefficients $v_{n1,2}$ in the drift velocity.

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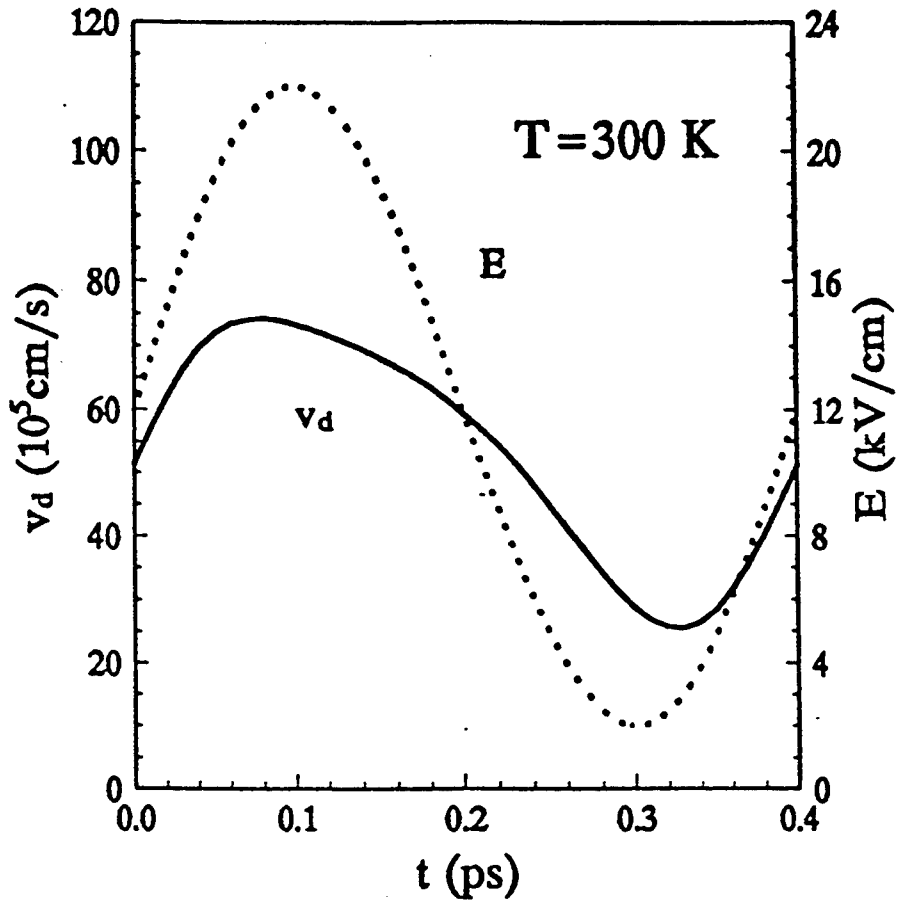


Figure 1: dc component of electron drift velocity as a function of time. The applied total electric field (one period) is also shown for reference.

A new concept for low-power all-optical switching in MQW structures

C. Knorr, U. Wilhelm, V. Härle, F. Scholz, and A. Hangleiter

*4. Physikalisches Institut, Universität Stuttgart,
Pfaffenwaldring 57, D-70550 Stuttgart, Germany*

All-optical switches play a central role in high speed optical computing and optical data processing. Various kinds of optical nonlinearities are presently under investigation for their potentially use in all-optical switching devices. The conventional SEED (self electro-optic effect device) is a bistable optical switch, which is already commercially available in digital systems [2]. It is based on the quantum confined Stark effect (QCSE) in low-dimensional semiconductor structures and a positive feedback is realized by an external electrical circuit [1,2]. In the InGaAs(P)/InP system however the contrast ratio and speed of the SEED are limited due to saturation at low optical power: The difference of the valence band and conduction band discontinuity and the different effective masses of electrons and heavy holes lead to an accumulation of photogenerated holes in the active region and therefore to a net space charge, which screens the external field in the quantum wells.

Another kind of photonic switch is based exactly on this field-screening mechanism, which is maximized to give an internal positive feedback [3]. This charge-induced self-feedback device in principle works in short circuit and needs no external connections. Nevertheless both, the conventional SEED and the field-screening device are based on a light-induced field reduction, so the operating wavelength for the positive feedback mode lies on the high energy side of the exciton line, therefore requiring a high input power.

We developed a novel type of pin-SCMQW (separate confinement multiple quantum well) structure, where photogenerated carriers lead to a strong enhancement of the internal field rather than to screening. The basic device structure consists of a conventional InGaAs(P)/InP SCMQW system, where additional larger InP barriers are introduced. These barriers are positioned in such a way that photogenerated holes screen the optical confinement layer and increase the field in the quantum

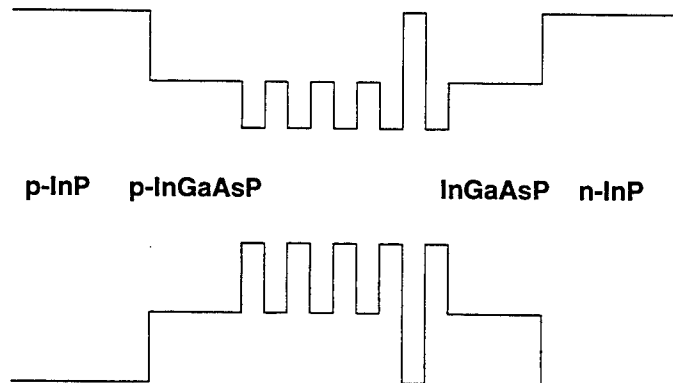


Figure 1: Basis layer structure designed to yield field enhancement in the quantum wells due to photogenerated carriers.

wells (Fig. 1). This field increase leads to a red shift of the band edge due to the QCSE and therefore to an absorption increase below the band gap, which is utilized for optical

switching. The effect of these additional barriers on electron transport is negligible, since both the barrier height and the effective mass are much smaller for electrons.

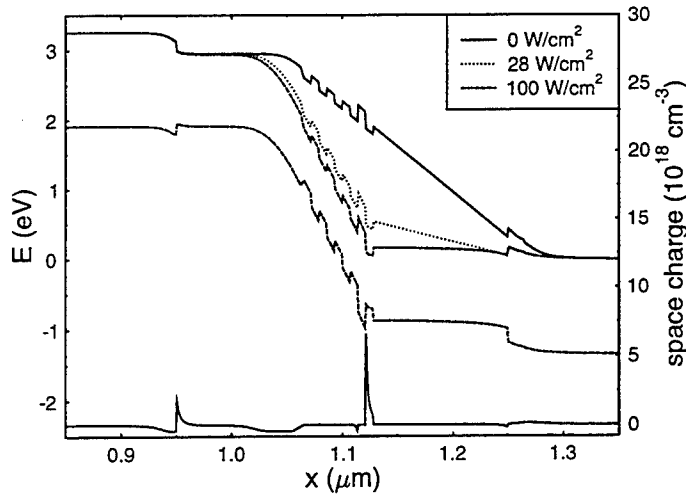


Figure 2: Calculated potential profile of the field enhancement structure with varying illumination and space charge at the highest power density.

sible field enhancement, which is determined by the relative width of the undoped region to the left and to the right of the InP barrier.

On the basis of the modeling we realized such structures and investigated the nonlinear behaviour by measuring the change of transmission due to photogenerated carriers at fixed bias levels. We got a clear evidence of charge carrier induced field enhancement.

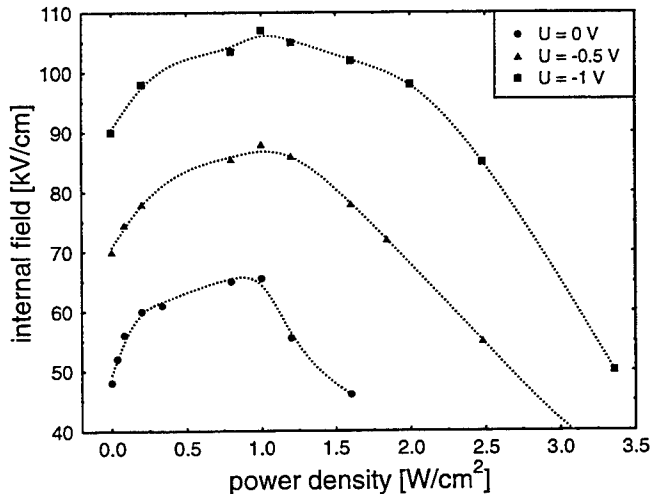


Figure 3: Internal electric field across the MQW region vs. pump power at different bias levels. The dotted line is a guide for the eye only.

photogenerated holes in all quantum wells, which reduces the field enhancement and finally screens the entire MQW-region. Fig. 4 shows the potential profile and the space charge in the high power regime of our calculations, which consistently describe the experiment.

We performed detailed calculations of the spatial band diagram with optical excitation by self-consistently solving Poisson's equation and the continuity equation [4]. Fig. 2 shows the potential profile of the structure with one additional InP barrier under varying optical generation. The positive space charge at the large barrier (Fig. 2) screens the field in the right confinement layer and increases the field in the MQW region. The left confinement layer is p-doped to increase the maximum possible

field enhancement, which is determined by the relative width of the undoped region to the left and to the right of the InP barrier. By comparing the phototransmission spectra with electro-transmission spectra we were able to determine the internal field at different pump power densities (Fig. 3). At all bias levels we observe a sharp increase of the electrical field at low power densities, which flattens somewhat at higher power levels. We observe a maximum field enhancement of about 40% at an optical input power of 1 W/cm². Above 1 W/cm² the field decreases again. This is due to an accumulation of photo-

So the same screening mechanism, which limits the operation of SEEDs and QCSE modulators, is present in our device structure. The maximum field enhancement is given by the ratio of the escape times for the photogenerated holes over the large InP barrier and the quaternary barrier.

Based on the results of the first field enhancement structure above there are several possibilities to improve the switching properties concerning high contrast ratio and low input power. Our first improvement was based on a simple geometrical consideration: The positive charge accumulated behind the large InP barrier creates a 'step' in the electric field, which contributes on the one hand to the field enhancement in the MQW region and on the other hand to field screening in the n-side confinement layer (Fig.5). The ratio of the electric field change in the quantum wells and in the confinement layer is fixed with the thickness of both regions.

Starting from the same dark field E_0 and introducing the same amount of positive charge into the last quantum well the change of the electric field in the MQW layer is substantially larger in structures with thicker n-side confinement layers. So our second device structure had an undoped region at the n-side, which was more than twice as large as in the first structure. To keep the waveguide structure symmetrical, we just shifted the n-doping front into the InP layer (Fig. 5). Differential transmission

measurements yield a maximum field enhancement of 18 kV/cm at a power density of 400 mW/cm², which is less than half the power required for the same shift in the standard structure. Above 400 mW/cm² the field enhancement is again reduced due to hole

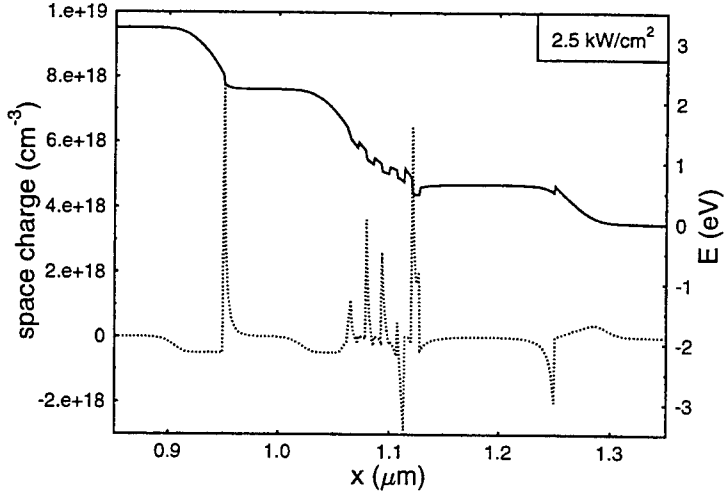


Figure 4: Space charge distribution and conduction band of the field enhancement structure under strong illumination.

Figure 5: Calculated relative position of the electric field 'step' of our first field enhancement structure (dashed line) and the second device with a thicker undoped region at the n-side (line). The step is shifted towards higher fields in the MQW region.

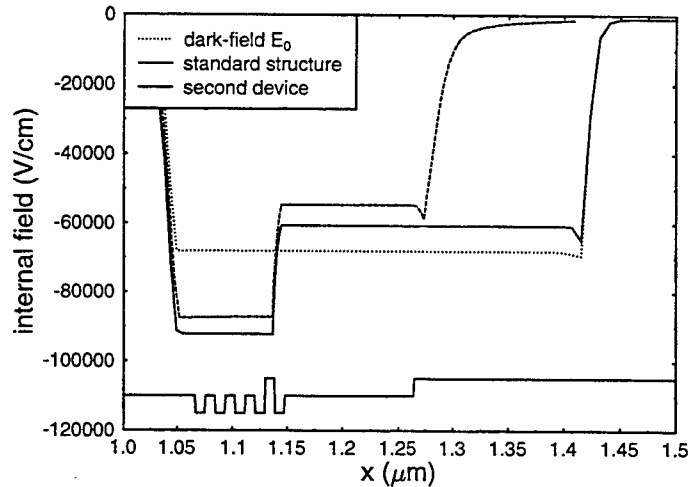


Figure 5: Calculated relative position of the electric field 'step' of our first field enhancement structure (dashed line) and the second device with a thicker undoped region at the n-side (line). The step is shifted towards higher fields in the MQW region.

accumulation in all quantum wells. Further optimization of the structures based on the modeling and experimental results is currently in progress.

The light induced enhancement of the internal field leads to an increase of the absorption below the bandgap and it should be possible to achieve hysteresis effects if the device is operated with a single wavelength. The wavelength for the positive feedback mode lies on the low energy side of the excitonic resonance and our novel switching structure might be useful for realizing low-power optical switching devices.

Support of this work by the Deutsche Forschungsgemeinschaft under contract No. Ha 1670/6 is gratefully acknowledged.

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Photonic Control of DC and Microwave Characteristics in AlGaAs/GaAs/InGaAs Double Heterostructure Pseudomorphic HEMT's

H.J. Kim, S.J. Kim, D.M. Kim, H. Chung, D.H. Woo, ...
I.K. Han, W.J. Choi, S.H. Kim, J.I. Lee, K.N. Kang, K. Cho

Div. of Electronics and Information Technology, KIST,
P.O. BOX 131, Cheongryang, Seoul, 130-650, Korea
Dept. of Electronics Engineering, Kookmin University,
861-1 Jungnung-dong Sungbuk-gu, Seoul, 136-702, Korea
Dept. of Physics, Kyunghee University,
Kihung-eup, Yongin-gun Kyengki-do, 449-701, Korea
Dept. of Physics, Sogang University,
Sinsu-dong, Mapo-gu, Seoul, 121-742, Korea

Photonic control of DC and high-frequency characteristics of HEMT's and related devices attract a great deal of attention with their possible applications to the optically controlled MMIC's for high-speed switches[1], phase shifters[2], oscillators[3] and mixers[4], etc. Previously reported experimental results show, however, rather small amount of improvement in DC and microwave characteristics in conventional AlGaAs/GaAs HEMT's and MESFET's with optical illumination.[5,6] This has been one of the problems in implementing application systems with optically controlled microwave devices.

In this work, we report DC and microwave characteristics of optically controlled double heterostructure n-Al_{0.3}Ga_{0.7}As(100Å)/i-Al_{0.3}Ga_{0.7}As(50Å)/GaAs(50Å)/In_{0.13}Ga_{0.87}As(100Å) pseudomorphic n-channel HEMT's, which is more efficient for the collection of channel carriers and the improvement of carrier transport, as shown in Fig.1. Epitaxial layer structures were grown on S.I. GaAs by gas-source MBE system. Hall mobility and density of 2-DEG in the pseudomorphic In_{0.13}Ga_{0.87}As channel at 300K were measured to be ~5,000cm²/(V·s) and 1.2×10¹²cm⁻², respectively. Devices for characterization have gate length L_g=1μm, gate width W_g=240μm, gate-to-source spacing L_{gs}=1μm, and gate-to-drain spacing L_{gd}=1μm, which are fabricated by using chemical wet etching process with Au-Ge/Ni/Au and Ti/Au for ohmic and Schottky contacts, respectively.

For the characterization of photonic responses of HEMT's, λ=0.83μm AlGaAs/GaAs laser diode module (Spectra-Physics : Model 7200) and HP8510B network analyzer have been used. We measured fabricated HEMT's on wafer in the frequency range of 45MHz~40GHz and optical power density(P_{opt}) of 0-440mW/cm² at room temperature. Measured low frequency performances of a fabricated pseudomorphic HEMT, with and without optical illumination, are shown in Fig.2 and Fig.3. Threshold voltage for the device was obtained from I_{ds}^{1/2}-V_{gs} plot at the saturation drain bias region, and found to be V_{th}=-0.87V without optical illumination. Transconductance was increased with optical illumination as shown in Fig.3. This mainly attributes to the photoconductive and photovoltaic effect with photogenerated electron-hole pairs, which are generated both in the GaAs spacer layers and InGaAs channel. Photogenerated carriers are finally collected in the narrow bandgap pseudomorphic InGaAs channel which resulting in the increase of carriers in the channel. Output conductance(g_{ds}) was decreased and showed less channel length modulation effect under optical illumination.

Typical microwave characteristics (small-signal current gain : H₂₁, maximum available gain : G_{max}) of the fabricated HEMT are plotted in Fig.4, which are measured at V_{ds}=2.5V, V_{gs}=-0.1V, and P_{opt}=52mW/cm². Current gain cut-off frequency(f_T) and maximum frequency of oscillation(f_{max}) were increased as shown in

Fig.5. f_{\max} and f_T were sharply increased. However, they are saturated above $P_{\text{opt}} \sim 50\text{mW/cm}^2$. This is probably due to the increased gate-to-source capacitance (C_{gs}) by the enhanced photovoltaic effect and the reduced channel mobility by the increased carrier-carrier scattering in the InGaAs channel. As shown in Fig.6, this agrees well with the small-signal equivalent circuit parameters, which are extracted from high frequency characterization. The enhancement of f_{\max} with optical illumination is more significant than that of f_T . This comes from reduced source, channel, and drain parasitic resistances (R_s , R_{ch} , and R_d , respectively) even with saturated f_T . f_T and f_{\max} depend on these parasitic elements through

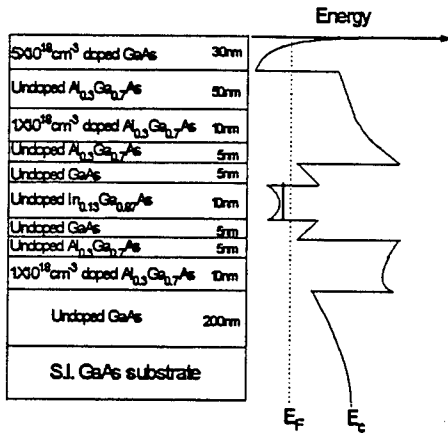
$$f_T = \frac{g_m}{2\pi(C_g + C_p)}, \quad f_{\max} = \frac{f_T}{2\sqrt{(R_s + R_{ch} + R_d)g_{ds} + 2\pi f_T R_g C_{gd}}}$$

Improved microwave performances under optical illumination ($P_{\text{opt}}=52\text{mW/cm}^2$) as functions of gate bias (V_{gs}) and drain bias (V_{ds}) are also shown in Fig.7 and Fig.8, respectively. The improvement of f_{\max} , compared with dark condition, is much more significant with the identical reason as in Fig.5. However, the relative change in f_{\max} at low V_{ds} is smaller than that of at high V_{ds} , while f_T is not quite significant with V_{gs} for dark and under optical illumination. This is because g_m and C_{gs} are almost constant both for V_{gs} and V_{ds} while there are large changes in R_s and R_d with drain bias. We also plotted bias-dependent capacitances (C_{gs} , C_{gd} , and C_{ds}) for $P_{\text{opt}}=52\text{mW/cm}^2$ in Fig.9 through Fig.11. C_{gs} and C_{gd} were increased with optical illumination near the pinch-off voltage as shown in Fig.9.[5,7] However, C_{gs} were decreased with optical illumination for small reverse gate bias as shown in Fig.10 and Fig.11. This probably comes from combination of photogenerated carriers from deep levels in the doped AlGaAs layer and GaAs/InGaAs layers because of their relatively different responses to the reverse gate bias and optical illumination.

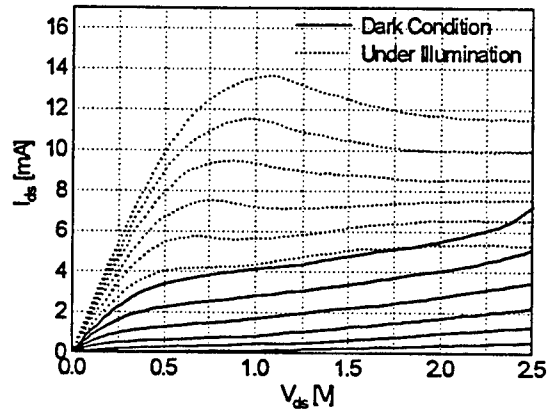
The variations of device performances and model parameters with optical illumination for $V_{ds}=2.5\text{V}$ and $V_{gs}=-0.1\text{V}$ are summarized in Fig.12. With optical illumination, a significant improvement of g_m , f_{\max} , and f_T was obtained in the efficiently designed AlGaAs/GaAs/InGaAs double heterostructure pseudomorphic HEMT's. This experimental results show possible applications of optically controlled AlGaAs/GaAs/InGaAs double heterostructure pseudomorphic HEMT's to the optically controlled MMIC's and high speed optoelectronic signal processing systems.

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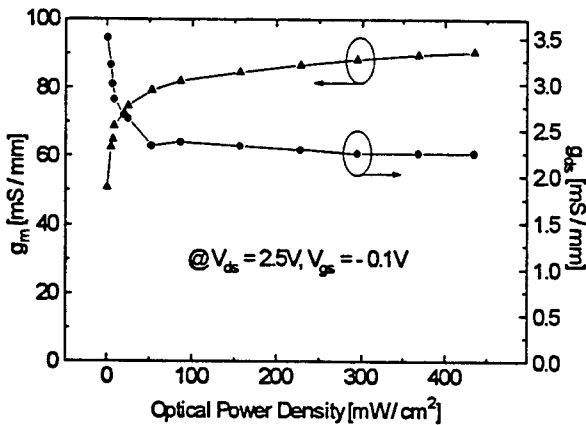
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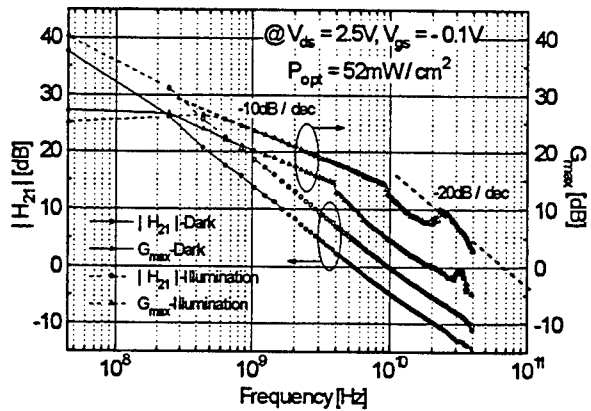
[Fig. 1] Epi-structure and energy band diagram of fabricated pseudomorphic n-HEMT.



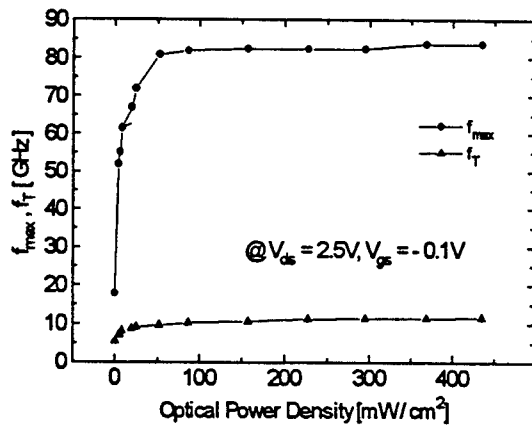
[Fig. 2] I_{ds} - V_{ds} of pseudomorphic n-HEMT without illumination. ($P_{opt} = 52 \text{ mW/cm}^2$, $V_{gs} = 0\text{V}$ (Top Curve) to -0.5V (-0.1V Step))



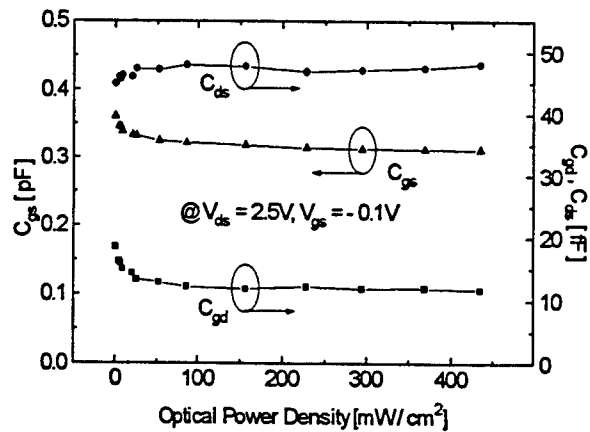
[Fig. 3] g_m and g_{ds} vs. optical power density. ($V_{ds} = 2.5\text{V}$, $V_{gs} = -0.1\text{V}$)



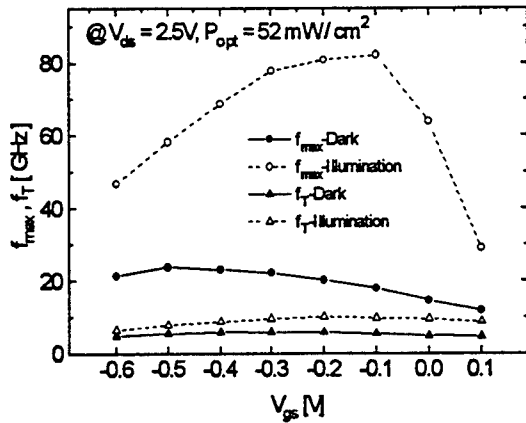
[Fig. 4] Frequency characteristics of current gain ($|H_{21}|$) and maximum available gain (G_{max}). ($P_{opt} = 52 \text{ mW/cm}^2$, $V_{ds} = 2.5\text{V}$, $V_{gs} = -0.1\text{V}$)



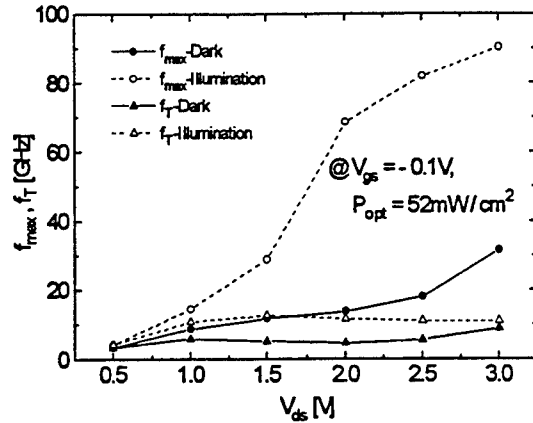
[Fig. 5] f_{max} and f_T vs. optical power density. ($V_{gs} = 2.5\text{V}$, $V_{ds} = -0.1\text{V}$)



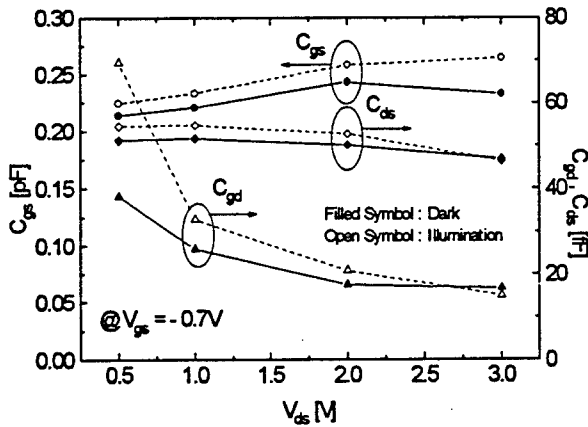
[Fig. 6] Capacitances vs. optical power density. ($V_{ds} = 2.5\text{V}$, $V_{gs} = -0.1\text{V}$)



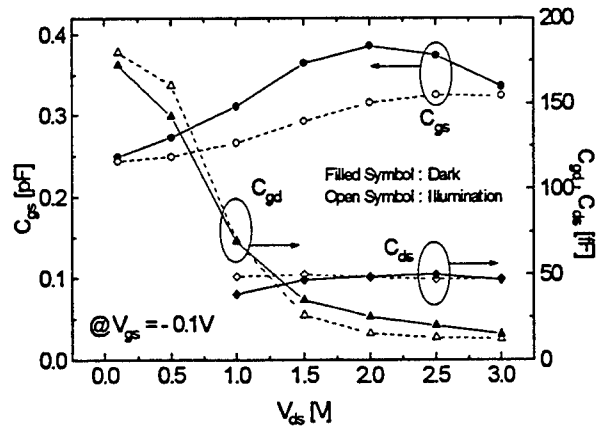
[Fig. 7] f_{max} and f_T vs. V_{gs} with/without illumination. ($P_{opt} = 52mW / cm^2$, $V_{ds} = 2.5V$)



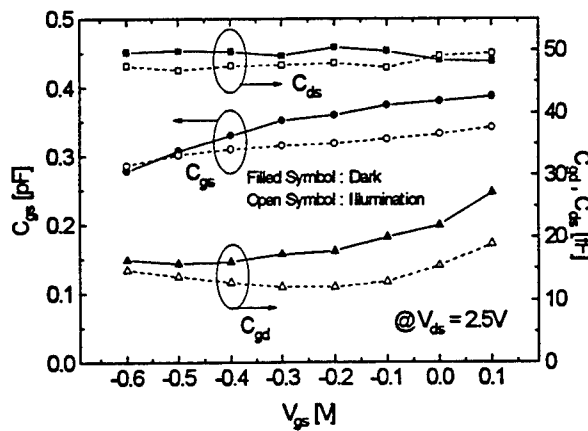
[Fig. 8] f_{max} and f_T vs. V_{ds} with/without illumination. ($P_{opt} = 52mW / cm^2$, $V_{gs} = -0.1V$)



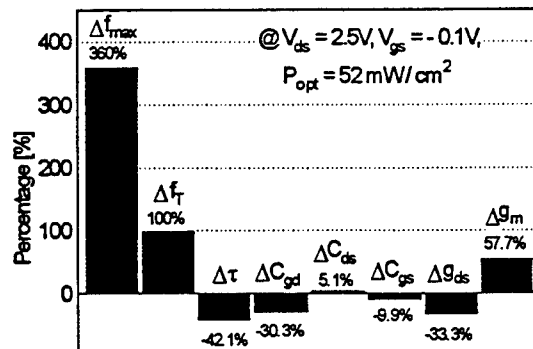
[Fig. 9] Capacitances vs. V_{ds} with/without illumination. ($P_{opt} = 52mW / cm^2$, $V_{gs} = -0.7V$)



[Fig. 10] Capacitances vs. V_{ds} with/without illumination. ($P_{opt} = 52mW / cm^2$, $V_{gs} = -0.1V$)



[Fig. 11] Capacitances vs. V_{gs} with/without illumination. ($P_{opt} = 52mW / cm^2$, $V_{ds} = 2.5V$)



[Fig. 12] The variations of device model parameters with/without illumination. ($P_{opt} = 52mW / cm^2$, $V_{ds} = 2.5V$, $V_{gs} = -0.1V$)

Si/SiGe Heterojunction Phototransistors

Karl D. Hobart, Fritz J. Kub, Nick Papanicolaou, and Phillip E. Thompson
Naval Research Laboratory, Washington, D.C. 20375

This paper reports for the first time the realization of a Si/SiGe heterojunction phototransistor (HPT). The process technology used to fabricate the HPT also yields SiGe heterojunction bipolar transistors (HBTs) with f_T and f_{max} of 10 and 25 GHz, respectively [1]. The HPTs demonstrated test system-limited bandwidth of over 100 MHz and a responsivity of 0.40 A/W at 850 nm laser wavelength.

The Si/SiGe heterostructure has been shown to enhance the performance of many silicon devices. In this instance, the heterostructure technology is utilized to implement phototransistors with high bandwidth and good optical responsivity. By utilizing the Si/SiGe heterojunction, a number of deficiencies in the Si phototransistor are addressed. Inserting SiGe in the base increases the transistor injection efficiency, which effectively decouples the base and emitter doping from the current gain. A reduction of the emitter doping is advantageous for low emitter-base capacitance, and the base transit time may be reduced by incrementally decreasing the base width while increasing the base doping. In addition, through bandgap grading the base transit time may be reduced by positioning a drift field in the base [2]. For increased absorption, multiple quantum wells (MQWs) can be inserted into the collector region of the transistor. For example, Si_{0.5}Ge_{0.5} produces a two order of magnitude absorption coefficient increase over Si at 850 nm [3]. A 500 nm MQW collector with twenty 5 nm Si_{0.5}Ge_{0.5} wells would produce a 70% increase in generated carriers for the same Si thickness. For low temperature growth processes such as molecular beam epitaxy the MQW structure would be metastable since the average Ge fraction would be 12-15%.

In this work, HPTs with Si collectors are characterized. The device fabrication scheme is similar to that used previously for HBT fabrication (see Ref. 1). A schematic drawing of the device structure is shown in Fig. 1. The device features a self-aligned emitter fabrication approach with air-bridge interconnects for low parasitic pad losses. Although HPTs with base contacts for supplying bias current were fabricated, only devices with a floating base are reported here. The layers were grown by molecular beam epitaxy on high resistivity p-substrates with n⁺-subcollector regions defined by implant. The nominal layer specifications are given in Table I. The self-aligned emitter fabrication sequence utilizes two selective etching processes to define the emitter and heavily doped emitter contact layers using the emitter contact metal as a mask. The nominal emitter width was 2 μ m. After masking the collector-base mesa with a photomask operation, CF₄/O₂ plasma etching isolates devices and exposes the n⁺ subcollector. In addition, air bridge interconnects are simultaneously formed by isotropic etching of the silicon from beneath the narrow metal interconnect. The collector contact is then made by depositing metal on the n⁺-subcollector. Fig. 2 is a micrograph of one such HPT device. Four HPT devices with differing active areas were investigated.

Devices were characterized under both d.c. and a.c. conditions using Cascade Microtech on-wafer probing with a calibrated normal incidence fiber probe fed by an 850 nm HP8850 laser source. The transistors were biased with the collector at ground and tied to the substrate to avoid collection of carriers generated in the substrate. The emitter was connected to a digital oscilloscope through 50 Ω coax and biased negatively through a bias-T. HBTs on the same chip, which were designed for high voltage, had excellent microwave characteristics with peak f_T and f_{max} of 10 and 25 GHz, respectively (Fig. 3).

TABLE I. HETEROJUNCTION PHOTOTRANSISTORS LAYER SPECIFICATIONS.

Layer	Type	Ge Fraction (%)	Doping (cm ⁻³)	Thickness (nm)
Emitter Cap	n ⁺	0	1x10 ²⁰	200
Emitter	n	0	2x10 ¹⁸	100
E-B Spacer	i	0-17	undoped	3
Base	p	17	2x10 ¹⁹	50
B-C Spacer	i	17-0	undoped	10
Collector	n	0	1x10 ¹⁶	2500
Sub-Collector	n ⁺	0	1x10 ²⁰	1000
Substrate	p ⁻	0	1x10 ¹³	—

The responsivity, R , and photocurrent gain, g , of the HPT were characterized through the relations $R = I_C/P_{ave}$ and $R = g \cdot \eta_{ex} \cdot (q/h\nu)$, respectively. Where I_C , P_{ave} , and η_{ex} are the collector current, average optical power, and external quantum efficiency without photocurrent gain, respectively. P_{ave} is the optical bias power upon which a constant 200 μ W, 50% duty cycle pulse is superimposed. Fig. 4 shows a plot of I_C as a function of P_{ave} at $V_{CE} = 5$ and 10 V. Fig. 5 shows the corresponding responsivity for the same device and bias conditions. The maximum responsivity observed was approximately 0.40 A/W. No saturation in I_C or R was observed, however, the increase in R with optical power was due to the increasing photocurrent gain with increasing collector current. The external quantum efficiency of the base-collector photodiode was measured on a separate test structure and was ~ 0.02 . The measured maximum photocurrent gain was approximately 25-30, which is consistent with concurrent HBT measurements of common-emitter current gain.

High frequency measurements were made to assess the response of the HPTs. Fig. 6 shows the measured rise, τ_r , and fall, τ_f , times as a function of emitter-base area at $V_{CE} = 10$ V. The risetime of the two smallest HPTs were faster than the system response under the test conditions. Fig. 7 shows the behavior of τ_r and τ_f as a function of V_{CE} for the smallest HPT (30 μ m²). The reduction in the risetime is due to a reduction in the collector-base capacitance with increasing collector-emitter bias. Fig. 8 shows the effect of P_{ave} or equivalently, I_C , on τ_r and τ_f with a 10 V bias and a 200 μ W optical swing for the 96 μ m² device. The increase in the risetime at low power is a direct result of charging the emitter-base capacitance. The HPT response is compared to the output of the pulse generator in Fig. 9. The HPT clearly reproduces the source waveform which was limited to ~ 3.3 ns risetime. This risetime corresponds to a cut-off frequency of ~ 106 MHz. Additional picosecond pulse measurements are currently underway.

Summarizing, Si/SiGe heterojunction bipolar phototransistors have been fabricated and characterized. The results indicate that SiGe HPTs are potential candidates for high-speed detectors and optoelectronic applications. The additional advantage of integration with high-speed SiGe HBTs is attractive.

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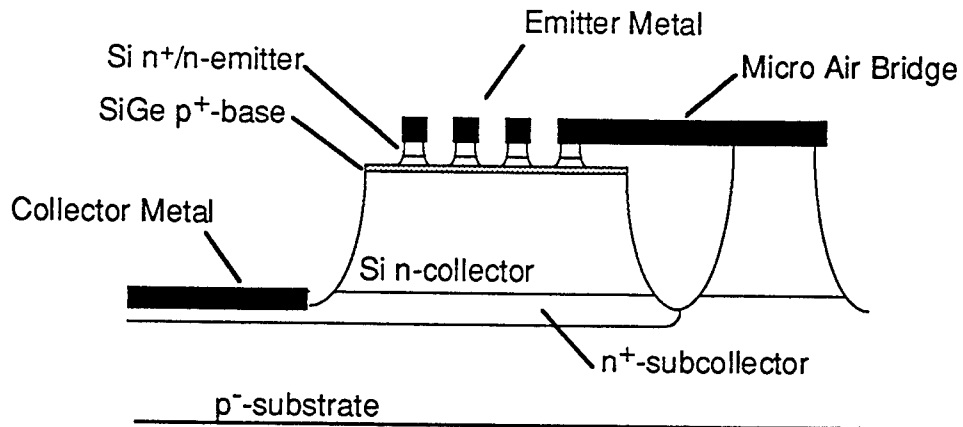


Figure 1. Schematic drawing of heterojunction phototransistor structure.

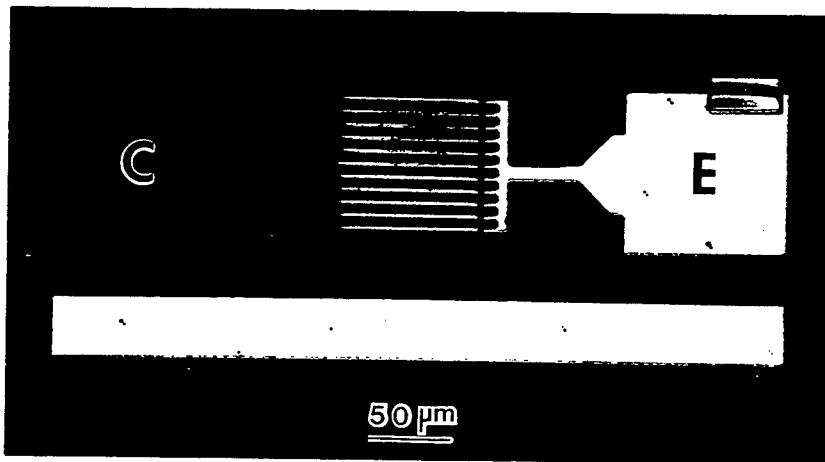


Figure 2. Micrograph of largest heterojunction phototransistor studied.

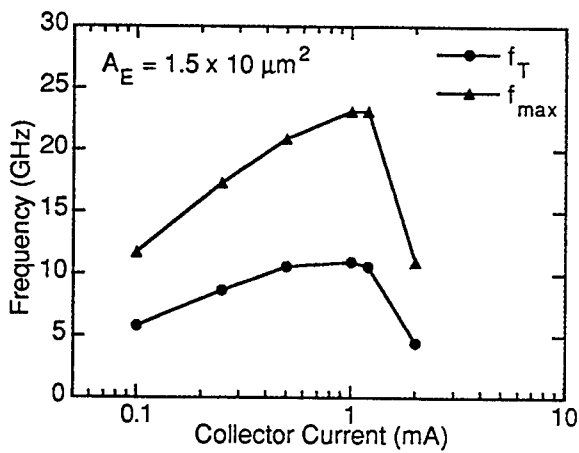


Figure 3. Microwave properties of Si/SiGe HBTs fabricated on same chip as heterojunction phototransistors. $V_{CE}=14$ V.

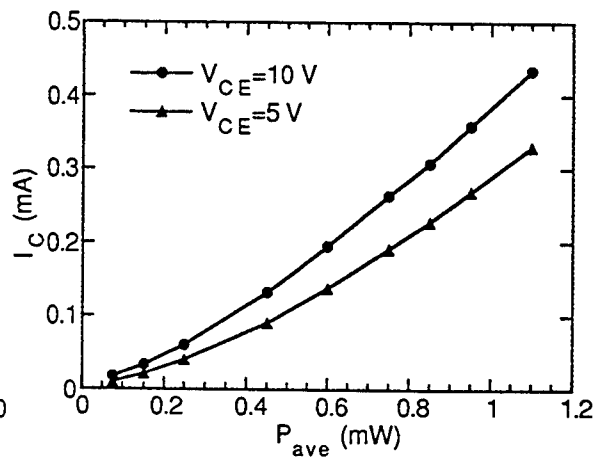


Figure 4. Average collector current as a function of average optical power incident on phototransistor for two collector-emitter biases. $A_E=30$ μm^2 .

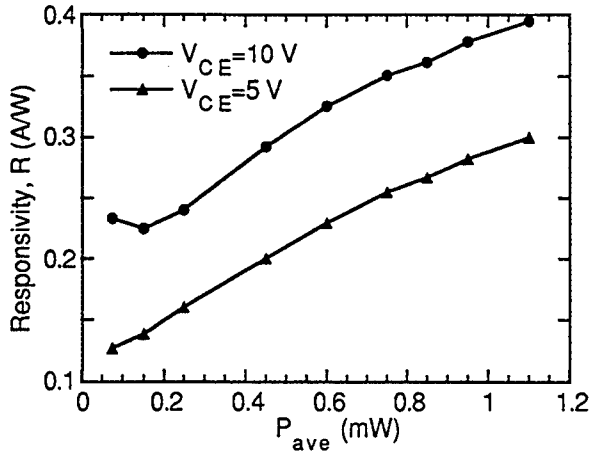


Figure 5. Responsivity, R, vs. average power, P_{ave} , at two collector-emitter bias points.

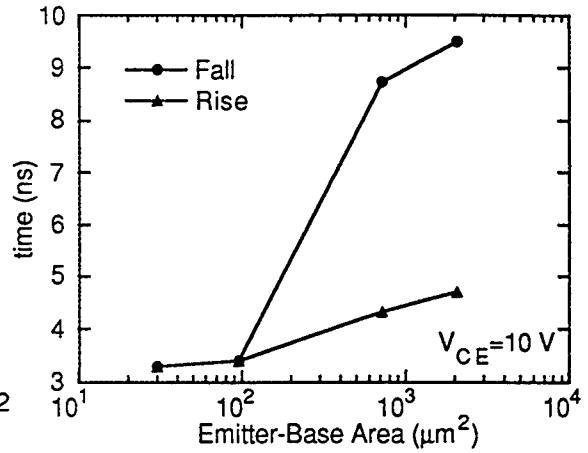


Figure 6. Response time of photo-transistors vs. various active area.

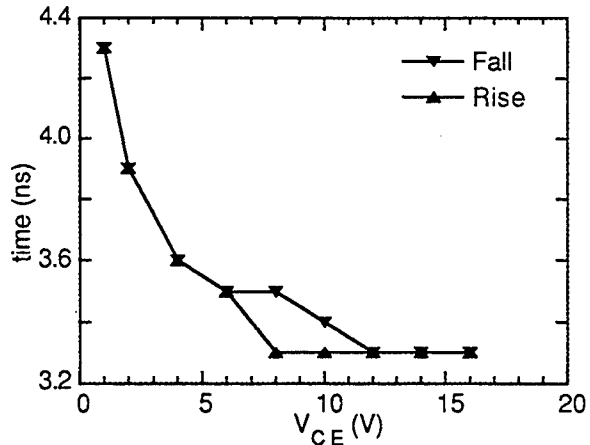


Figure 7. HPT response time as a function of collector-emitter bias voltage.

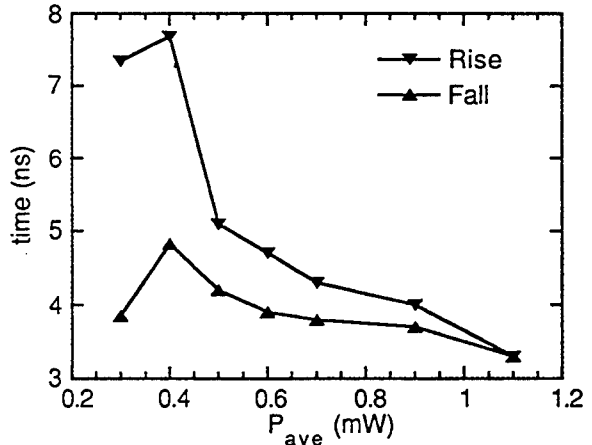


Figure 8. HPT response time as a function of average optical (bias) power.

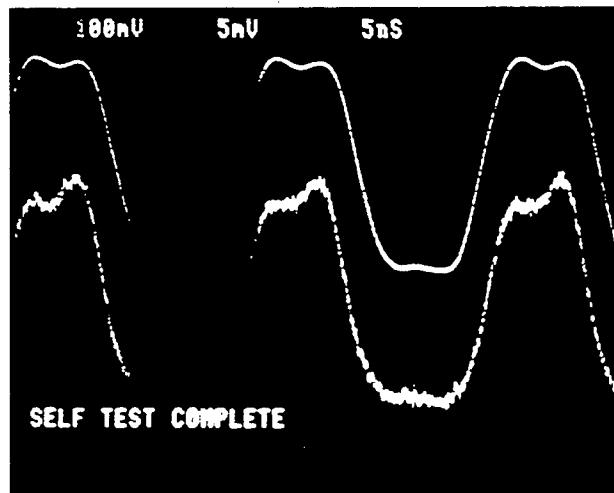


Figure 9. Time domain response of Si/SiGe HPT showing test system limited response. Top trace is pulse generator monitor and lower trace is HPT output.

Device Physics of Modulation Doped Type I and Type II GaAs/AlAs and AlGaAs/AlAs Quantum Well Structures

Mitra Dutta
Physical Sciences Directorate
Army Research Laboratory

Athos Petrou
Physics Department
State University of New York, Buffalo

We have studied modulation doped GaAs/AlAs and AlGaAs/AlAs multiple quantum well structures and compared them with the results from the respective undoped structures. Our motivation in studying this was to determine some of the unknown quantities associated with and the device potential of this class of structures. These unknown quantities include where the 2D electron gas is formed as well as where the parent donor is resident, the binding energy of the exciton, type I to type II transitions as compared with the undoped structures, the screening and the many body effects that come into play in these structures. Finally we will discuss the device possibilities and potential of these novel structures.

The first extensive investigations on GaAs/AlAs were on the vibrational modes in short period superlattices. Folded acoustic modes^{1,2}, confined optical modes^{3,4}, resonantly excited confined^{5,6} and interface phonon modes^{5,7,8} are some examples from the existing literature. It was realized quickly that these materials have an interesting band structure due to the indirect band gap of the AlAs barrier layers and that there is significant coupling between the lowest energy Γ band of the GaAs and the lowest energy X band of the AlAs. Review articles in which these studies have been systematically discussed are also available⁹⁻¹². In GaAs/AlAs structures with wider wells a significant reduction of the e_2-h_2 excitonic binding energy as well as associated interwell charge transfer processes^{13,14} have been observed. In addition, Raman studies¹⁵ on these structures showing interface phonon assisted $\Gamma-X$ transitions in structures where there is coupling between the X and Γ levels. Calculations have been performed in which the relative transition probabilities have been calculated for the interface-phonon assisted $\Gamma-X$ transitions in selected short period superlattices are estimated by using the dielectric continuum model for both symmetric¹⁵ and antisymmetric¹⁶ interface optical phonons together with a Kronig Penney model of the superlattice electronic models.

We have subsequently started an extensive investigation of n-type modulation doped GaAs/AIAs multiple quantum well structure as well as AlGaAs/AIAs structures which has the AIAs layers as the wells in the structures and the X conduction band edge has the lowest energy in both AIAs and the AlGaAs layers. Initially photoluminescence and Raman studies of the GaAs/AIAs of the modulation doped multiple quantum well structures were performed¹⁷. Wide wells were chosen in the initial study where the 150 Å AIAs barriers were doped $1.2 \times 10^{18} \text{ cm}^{-3}$, without spacer layers. The zero field spectrum has the typical form of luminescence from the free electron-hole recombination in modulation doped quantum well structures, showing that the Si donors of the barriers release their electrons in the GaAs wells. The feature is broad and all excitonic features are absent due to screening by the dense electron plasma. The position of the Fermi level determined by the width of the luminescence (42 meV) yields an approximate value of 10^{12} cm^{-2} for the electron areal density. In the presence of a magnetic field, the broad zero field luminescence breaks into a series of well defined features attributed to interband transitions between Landau levels in the conduction and valence subbands. The interband transitions are similar in character to those observed in GaAs/AlGaAs, InGaAs/GaAs as well as InGaAs/InP quantum wells. There is a deviation from a linear field dependence which is associated with many body effects.

The Landau transitions extrapolate to approximately 1510 meV, an energy which is well below the effective bandgap of an undoped well having the same dimensions. The reduction of the energy gap has been attributed to a bandgap renormalization due to the presence of the two-dimensional electron gas in GaAs wells. In addition the photoluminescence excitation spectra has a well developed onset at 1553 meV which coincides with the high energy edge of the PL spectrum. The Raman spectra were excited resonantly at the energy of the e_3-h_3 transition. In the cross polarized situation of the Raman spectra is seen a single feature associated with the e_1-e_2 intersubband transition. This feature is absent in the parallel polarization, and instead two weaker features appear in addition to the longitudinal (LO) phonon and 2LO phonon lines. They are attributed to coupled collective intersubband LO phonon excitations. In the presence of a magnetic field applied parallel to the growth direction the energy of the the intersubband transition Raman feature varies with B. The slope corresponds to a cyclotron effective mass that is very close to the electron mass. This feature is therefore interpreted as a combination mode of the intersubband transition and the electron cyclotron resonance¹⁸.

We then continued our studies with narrow wells where the well widths were so chosen that the lowest conduction subband e_1 lies above the donor states. At low temperatures the electrons remain attached to the silicon donors from where they can recombine with photogenerated holes confined in the GaAs

wells. An impurity related feature is identified as the donor to valence band transition. A comparison of the energy of this feature with that of the AlAs X-valley to valence band transition yields the donor binding energy. This binding energy is found to be 104 meV for these donors which are associated with the AlAs X-valley minima. This large binding energy is due to the heavy effective masses for the X-band in AlAs.

The type I and type II interband transitions in AlGaAs/AlAs multiple quantum well structures were studied using optical spectroscopic techniques. The simultaneous observation of both types of transitions allows an accurate determination of the band offsets in this system. In undoped samples the spatially indirect transition is dominated by replicas which involve single and multiple phonon emission. In n-type modulation doped samples in which the AlAs X-valley minima are populated by an electron gas, the zero phonon type II transition intensity becomes comparable to that of the phonon replicas. This indicates a violation of the k-vector conservation selection rule that could be attributed to many body effects. Some of the device possibilities of these structures including optical modulators, phase shifters and tunneling devices will be discussed.

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Study of I-V Characteristics of Asymmetric Double Barrier Resonant Tunneling Diodes with Superlattice Emitters

Kausar Banoo* and Theda Daniels-Race
Duke University, Department of Electrical and Computer Engineering
PO Box 90291, Durham NC 27708-0291

* *Student Paper*

This work is a study of the electronic properties of Asymmetric Double Barrier Resonant Tunneling (ADBRT) diodes grown with different superlattice (SL) emitters. The layer thickness and period of the superlattices were systematically varied in order to define a unique emitter state in each structure grown. In each case, the emitter state was determined theoretically by calculating the miniband formation in the constituting superlattice. The relationship between the emitter state defined by the superlattice structure parameters and the current-voltage behaviour of the diode at 77 K has been investigated here.

Extensive research of the physical and electrical properties of superlattices has led to the development of an interesting body of device physics based on these structures and their incorporation in various semiconductor devices such as double barrier resonant tunneling (DBRT) structures, high electron mobility transistors (HEMTs) and semiconductor lasers, to name a few. In the case of symmetric DBRT structures, Portal *et al.* [1] and Reed *et al.* [2] have conducted studies involving the use of short-period superlattices as emitters and barriers of the quantum well respectively. Optimising these configurations was found to increase the peak-to-valley current ratio (PVCR), which is a figure of merit for the performance of DBRT structures. The ADBRT diode is, on the other hand, not noted for a high PVCR. It has, however, been observed to produce greater electron-phonon interaction and therefore, a greater degree of phonon-assisted tunneling [3, 4]. Such phenomena could be applicable to the operation of exciting new devices such as the quantum cascade laser [5]. Thus, to the authors' best knowledge, this study represents the first work in which superlattice emitters have been used to investigate resonant tunneling phenomena for ADBRT structures.

Three distinct structures were grown as shown in Figure 1. Briefly, a sample of each structure consisted of a graded doped emitter region, a variable composition five-period superlattice, the ADBRT structure of an 80 Å GaAs well with 45 Å and 33 Å AlAs barriers and a graded doped collector (listed in the order of growth). The superlattice had five periods with alternating layers of GaAs and AlAs of equal thicknesses. The three different superlattices were grown with a characteristic layer thickness namely 50 Å, 30 Å and 15 Å respectively. A 1 μm heavily doped GaAs cap layer was finally deposited to allow ohmic contact to be made to the device.

The electron transmission probability across each superlattice emitter structure

was numerically calculated using the transfer matrix approach [6]. The results of these calculations are shown in Figure 3 where the transmission probability is plotted against electron energy. The position of the peaks (transmission probability of 1) indicates the position of the energy levels in the superlattice. The energy band in a five-period superlattice has four discrete quasi-bound levels [7] and therefore forms a primitive “miniband” when these discrete levels are spaced close together. Upon analysis of the numerical calculations, it can be seen that the 50 Å superlattice has the densest and highest energy band among all the superlattices. In the 30 Å and the 15 Å superlattices the multiple quasi-bound levels are positioned lower and wider apart. It follows that this difference in the superlattice states would have a noticeable effect on electron tunneling through the entire device structure when the superlattice acts as an emitter.

Experimental study showed resonant tunneling peaks in all the samples in the *reverse* bias. This is what we would expect because the flow of electron current encounters the ADBRT diode before the superlattice structure. Therefore, the ADBRT diode would tend to predominantly influence the resonant tunneling behaviour. This was seen clearly in the I-V characteristics of a 50 Å five-period GaAs/AlAs superlattice emitter sample shown in Figure 2. Presence of satellite peaks, evident in the inset, indicated the occurrence of phonon-assisted tunneling through the ADBRT quantum well. The 50 Å five-period GaAs/AlAs superlattice emitter sample was also the only structure, among all the three samples in this study, that was observed to exhibit resonant tunneling in *forward* bias. In the forward bias the electrons flow through the superlattice emitter before the ADBRT diode and it is known that resonant tunneling peaks occur when tunneling through the superlattice emitter states takes place. This happens under the condition that the potential drop across the superlattice period is equal respectively to the width of the first and second miniband [8], according to the predictions of the Dohler-Tsu-Esaki theory [9]. Interestingly enough, in this case, the valley current shows no other peaks that could be attributed to phonon assisted tunneling.

Therefore, as a result of this study, it can be concluded that in spite of the discrete nature of the energy levels, a five-period GaAs/AlAs superlattice emitter is sufficient to support electron tunneling provided the thickness is large enough to allow the formation of a primitive “miniband”. In general, it can be stated that manipulation of the emitter levels in an Asymmetric Double Barrier Resonant Tunneling Diode changes its electronic properties significantly.

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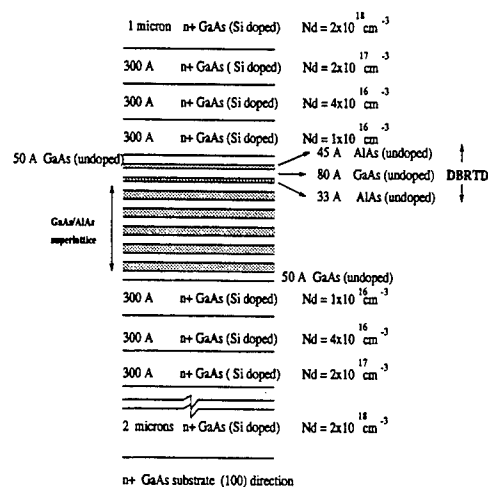


Figure 1: Layer schematic of the asymmetric DBRTDs with superlattice emitters.

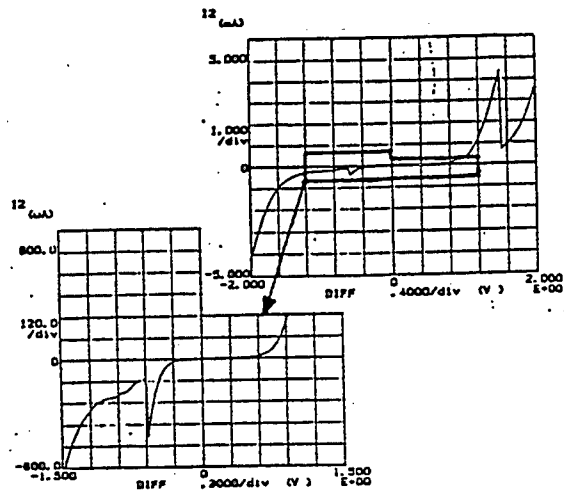


Figure 2: I-V characteristics for the 50 Å five-period GaAs/AlAs superlattice emitter sample at 77 K showing the forward and reverse bias resonant tunneling peaks. Contact area = $1.963 \times 10^{-3} \text{ cm}^2$.

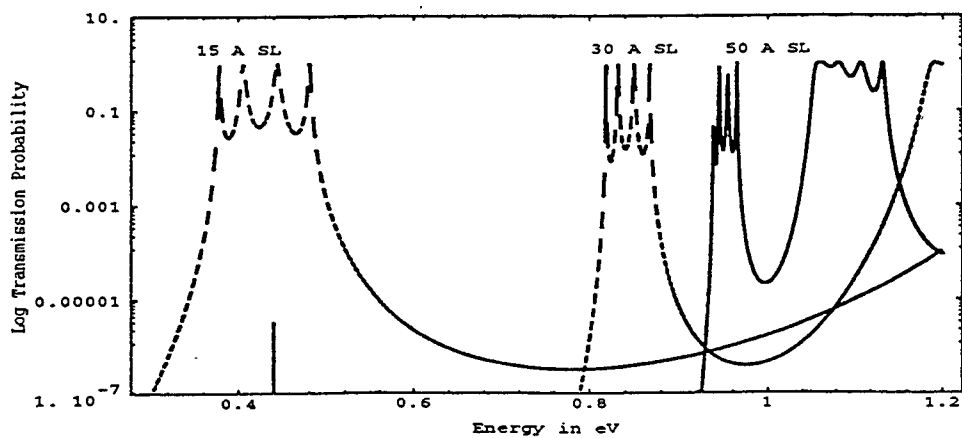


Figure 3: Electron transmission probability for the three superlattice structures calculated for zero bias

Correlation Between Charge-to-Breakdown (Qbd) and the Endurance (Program/Erase cycling) of Thin Tunnel Oxide.

Sik-Han Soh

National Semiconductor Corp.

3333 West 9000 South,

West Jordan, Utah 84088

Tel:(801) 562-7492

Fax:(801) 562-7337

Email: cshssl@tevm2.nsc.com

Chuan-Pu Liu, Rex Peterson, Brian Baker and Larry Sadwick

Electrical Engineering Department,

University of Utah,

Salt Lake City, Utah.

ABSTRACT

Thin oxide wearout and breakdown is one of the principle failure mode in CMOS VLSI circuits. In the case of nonvolatile memories such as EEPROM and FLASH where carrier transport through the oxide is normal mode of operation, the reliability of the thin tunneling oxide represents one of the most critical parameters. The predominant method for measuring and monitoring the quality and reliability of thin oxide at wafer level is Charge-to-breakdown (Qbd). This paper investigates how well Qbd predicts the endurance (program/erase cycling) of thin tunnel oxide. Qbd data on 8.0 nm silicon dioxide was obtained from constant current stressing over a series of temperatures. The thermal activation energy of the oxide Qbd was compared to the activation energy of endurance (program/erase cycling) of similar oxide structures on the same wafer. The data shows that the activation energies for Qbd and endurance are very different (Figure 1), suggesting that Qbd is not a good predictor of endurance. To check if the differences seen might be due to bipolar current injection in endurance, Qbd for gate and substrate injection was studied. Results for different size capacitors as shown in Figure 2 indicate that differences seen in the TDDDB is from pre-factor (intercept) and not from the activation energy (slope of log (TDDDB) vs $1/T$). Investigation on the effect of different current densities also show no observable impact on the thermal activation energy of the Qbd (Figure 3). Based on the results we conclude that Qbd might not be measuring the same oxide degradation mechanism that endurance cause. A wafer level test structure for accelerated endurance testing of tunnel oxide will be proposed.

DATA COMPARING QBD AND ENDURANCE FOR F3 AT VARIOUS TEMPERATURES

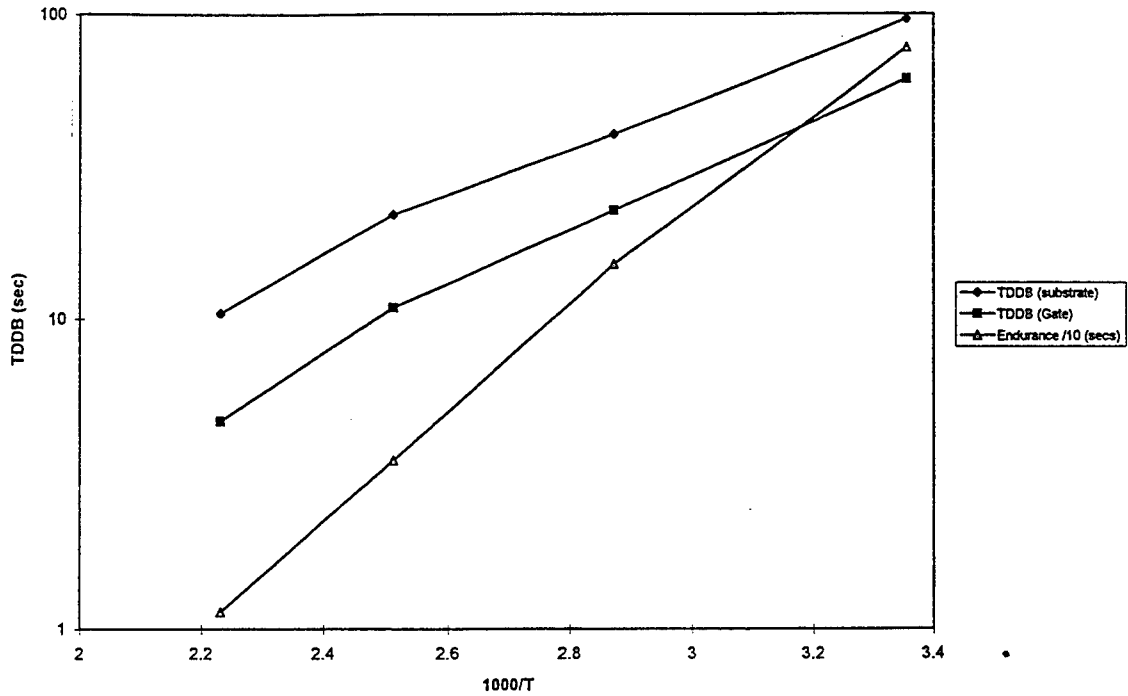


Figure 1. Plot of Log (TDDB) versus 1000/Temp(K) showing the difference in the slope for constant current QBD and the endurance for capacitor F3. The Qbd plot for both Gate(polysilicon) and Substrate (silicon) current injection are shown.

COMPARING QBD OF GATE AND SUBSTRATE INJECTIONS

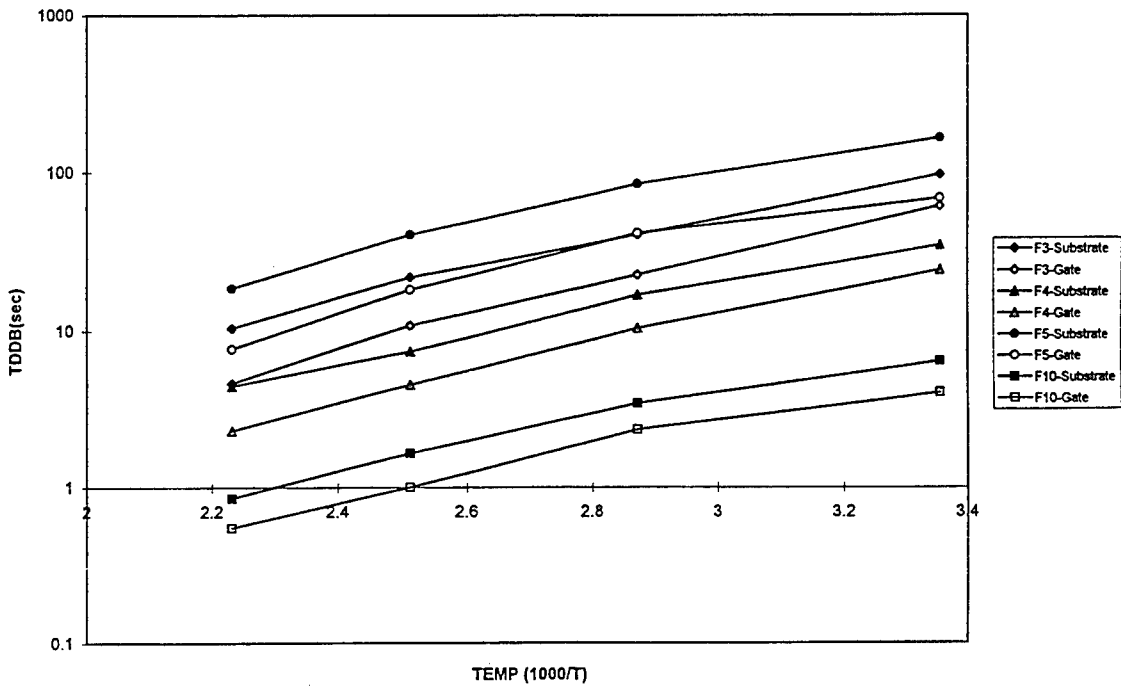


Figure 2. Plot of Log(TDDB) versus 1000/Temp(K) for constant current stress for four different size area capacitors. Both Gate and Substrate injection are included. The difference in the TDDB between Gate and Substrate injection is reflected as a shift in the line, indicating no change in the thermal activation energy.

EFFECT OF DIFFERENT CURRENT DENSITY ON QBD AT DIFFERENT TEMP

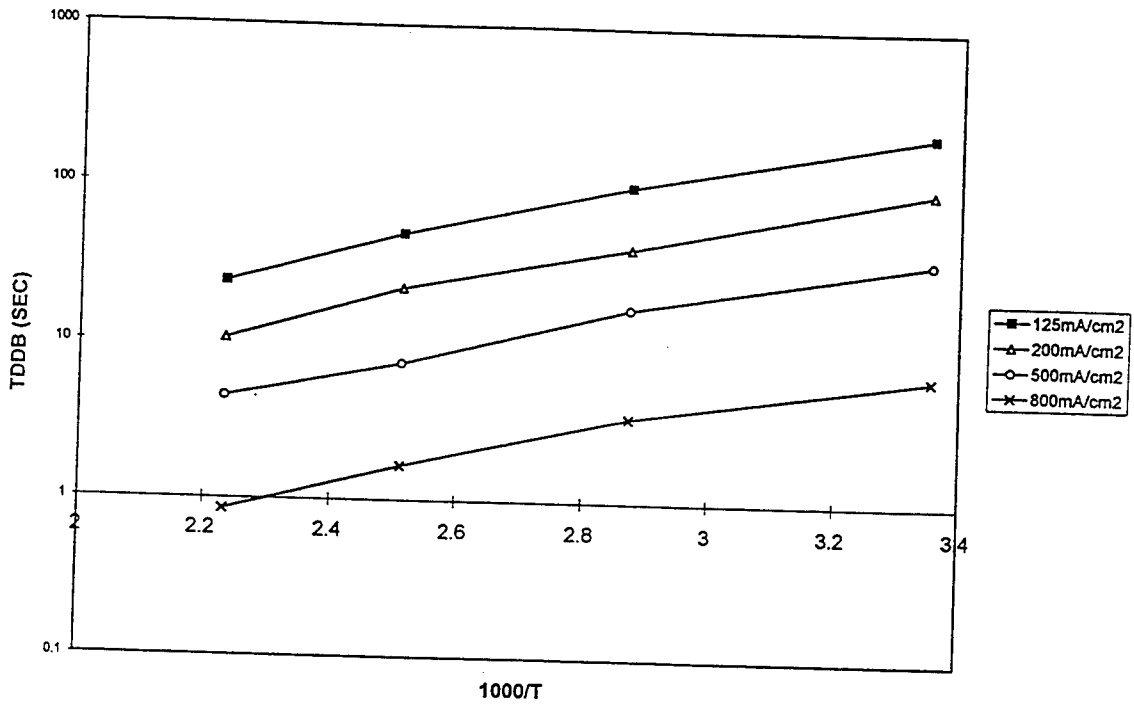


Figure 3. Plot showing the effect of different current densities used in QBD stressing. Effects is also vertical shift in the plot indicating no change in the thermal activation energy.

A novell MOSFET series resistance measurement technique using one single MOSFET

J.A.M. Otten and F.M. Klaassen
Faculty of Electrical Engineering
Eindhoven University of Technology
P.O. Box 513, 5600 MB Eindhoven, The Netherlands

1 Abstract

A novel measurement method to determine the series resistance from one single MOSFET is discussed. Not only the gate voltage dependence of the series resistance R_{series} at low drain bias can be measured now but also the increase of the drain series resistance R_d with increasing drain bias. In addition attention is paid to the modeling of the series resistance in the full bias range. The measurement principle is based on the measurement of the (trans)conductance as a function of externally added series resistors keeping the 'intrinsic' bias constant. From the slope of this plot information is obtained about the derivative of the series resistance with respect to terminal bias. At low drain voltage the accuracy of the single transistor measurement technique is comparable with a measurement technique using a set of identical MOSFETs except for the mask channel length [8]. In accordance with our 2-D device simulations it is also found that R_d increases linear with the voltage across the drain resistance due to velocity saturation. The increase of R_d is effectively modelled. Including this model for R_d into a compact MOSFET model better physical based parameters are obtained.

2 Introduction

Although much attention has been given to MOSFET series resistance and L_{eff} measurement techniques [1, 2, 3] to determine $R_{series}(V_{gs})$ and $\Delta L = L_m - L_{eff}$ all these methods need a set of identical MOSFETs, except for the mask channel length, leading to additional errors in the determination of R_{series} and ΔL . Furthermore these methods are not suited to measure the series resistance as a function of drain bias. In addition the significance of a correct R_{series} determination increases rapidly as shown in fig. 1. Therefore in this paper a new method is discussed to solve the above deficiencies. Finally attention is paid to the modeling of the series resistance as a function of the terminal biases.

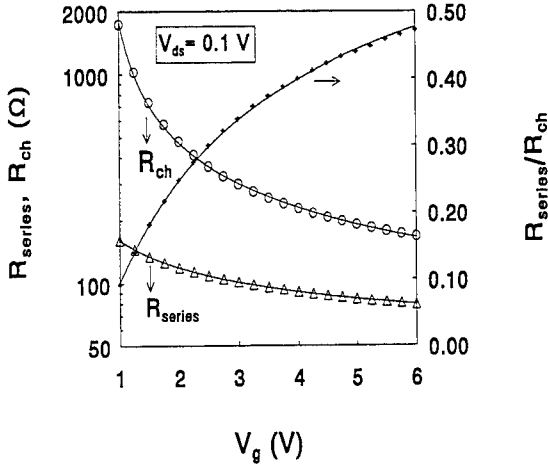


Figure 1: Series resistance, channel resistance and their ratio for a LDD device from to 2-D device simulations ($L_m=0.25 \mu m$, $W_m=10 \mu m$, $V_{ds}=0.10$ Volt).

3 Theory

The new method only needs one single MOSFET to measure (a) the series resistance as a function of the gate and drain bias, (b) the ratio of the intrinsic conductances and (c) the mobility degradation coefficients. In [4] already such a method was presented to measure R_{series} as a function of gate bias. However, due to some inaccuracies inherent to the method incorrect results can be easily obtained [5], which are still valid despite of recent improvements [6]. Our new method measures the conductance and transconductance as a function of externally added resistance as a function of the terminal biases. It can be easily derived that the expression for the conductance G_d equals

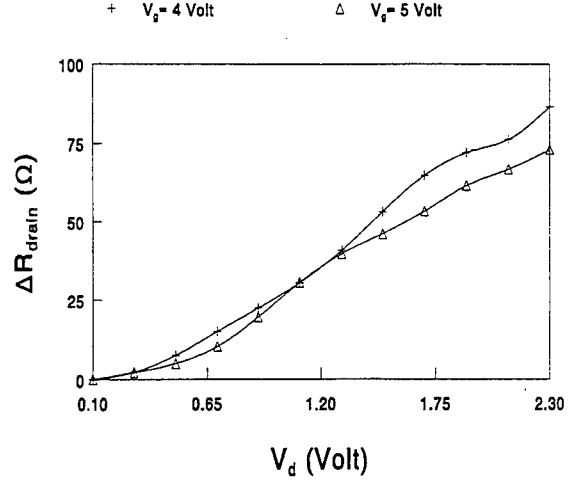


Figure 2: Increase in the drain series resistance as a function of drain bias at various values of gate bias ($W_m=2 \mu m$, $L_m=0.70 \mu m$, $V_g=4$ and 5 Volt).

$$G_d = \frac{G_{di} * (1 - I_{drain} \frac{\partial R_d}{\partial V_d})}{1 + G_{di}(R_s + R_d) + (G_{mi} + G_{bi})R_s} \quad (1)$$

Similar expressions can be derived for the transconductance G_m and influence of bulk bias on the drain current $G_b = \partial I_{drain} / \partial V_b$. Next the derivatives of the series resistance with respect to bias are obtained from these conductance measurements. If for instance an external drain series resistance R_{extd} is added and the internal bias conditions for the MOSFET are thus also the drain current are maintained, the derivative of G_d^{-1} with respect to R_{extd} equals:

$$\frac{\partial G_d^{-1}}{\partial R_{extd}} = \frac{1}{(1 - I_{drain} \frac{\partial R_d}{\partial V_d})} \quad (2)$$

from which $\partial R_d / \partial V_d$ can be calculated. Using the same approach $\partial R_s / \partial V_g$ can be extracted too. Integration of the derivatives yields the series resistance. Since we are now able to distinguish the intrinsic MOSFET from the extrinsic MOSFET, the 'ohmic' region compact MOSFET model parameters such as the gain factor β and the mobility reduction coefficients are obtained, independent from the series resistance as shown in equation 3.

$$\begin{aligned} \frac{\partial R_{ch}}{\partial V_g} &= \left(\frac{\partial R_t}{\partial V_g} - \frac{\partial R_{series}}{\partial V_g} \right) \\ &= \frac{1}{\beta} \left(\theta_d - \frac{2}{3} \theta_a V_{gt}^{-1/3} - V_{gt}^{-2} \right) \end{aligned} \quad (3)$$

Since the compact model parameters can be determined, the missing integration constant for the series resistance at low drain bias can be determined

too. Since our method 'measures' the series resistance by distinguishing between the intrinsic and extrinsic behavior of the device, our method is not limited to MOSFETs only.

4 Results

In fig. 2 the measured increase of the drain series resistance R_{drain} is plotted as a function of drain bias at various values of gate bias. In comparison with our earlier results [7], the new method is also so able to measure the drain series resistance in saturation as shown in fig. 3 where measurement results are compared with theoretical results (dotted line). In this case R_{drain} is plotted as a function of the bias across this resistance.

A similar method is used to determine R_{series} as a function of gate bias at low drain bias. Since we can measure the ratio of the intrinsic conductance and transconductance (fig. 4) we are able to determine the bias across the intrinsic MOSFET and thus also the value of $R_{series}(V_g)$. In fig. 5 a measurement example is given where the results are compared with results of another method [8] where a set of MOSFETs is needed to determine $R_{series}(V_g)$.

5 Modeling

Our compact model for the series resistance only needs 5 parameters to model the series resistance in the full bias range. Since according to 2-D device simulations the main current path in the junction is near the inter-

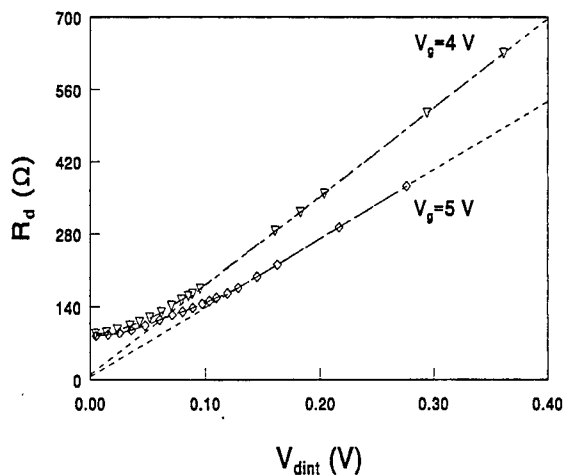


Figure 3: Measured drain series resistance at several values of gate bias as a function of the bias across R_{drain} ($W_m = 2 \mu m$, $L_m = 0.70 \mu m$).

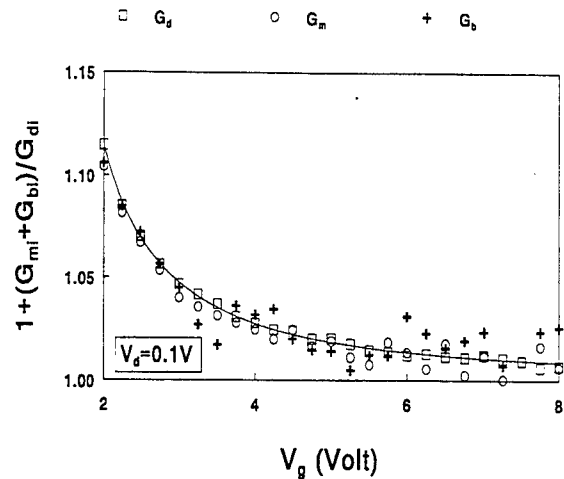


Figure 4: Ratio of intrinsic conductances as function of gate bias ($V_d = 0.10$ Volt, $W_m = 10 \mu m$, $L_m = 0.80 \mu m$). Solid line is according to our model.

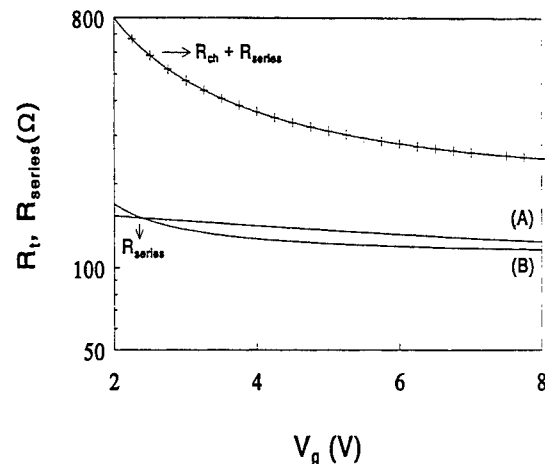


Figure 5: $R_t(V_g)$ and $R_{series}(V_g)$ for (A) set of identical MOSFETs and (B) the single transistor measurement technique ($W_m = 10 \mu m$, $L_m = 0.80 \mu m$).

face as illustrated in fig. 6 where the dissipation in the MOSFET is plotted, the gate bias dependent part of R_{series} (at low drain bias) can be modelled as a sum of two accumulation resistances in parallel with a sheet resistance, giving.

$$R_{part}(V_g) = \frac{R_{par} K_{ac0}}{K_{ac0} + R_{par}(V_g - V_{th})} \quad (4)$$

In the above equation the sum of the accumulation resistances was assumed to equal $K_{ac0}/(V_g - V_{th})$ and the parallel resistance R_{par} . For the total series resistance the constant contact resistance R_{co} and the sheet resistance R_{sh} have to be added to equation 4. The final result is that the measured series resistance

can be perfectly fitted using equation 5

$$R_{series}(V_g) = (R_{co} + R_{sh}) + \frac{a_1}{a_2 + (V_g - V_{th})} \quad (5)$$

From 2-D device simulations we have derived that the increase in R_{drain} is mainly due to velocity saturation in the LDD region of the drain junction resulting in a linear increase of R_{drain} with the bias across this resistance V_{d1} as given by equation 6.

$$R_{ldd} = \frac{1 + \theta_{c1} V_{d1}}{Aq\mu_0 k} \ln \left(\frac{N_{d0} + k * x_{ldd}}{N_d} \right) \quad (6)$$

with θ_{c1} equal to $C_0/(C_1 + V_g)$. The variables C_0 and C_1 are two constants, modeling the slope of R_d versus V_{d1} as a function of the gate bias. Of course the increase of the drain series resistance becomes noticeable when the MOSFET is in saturation as shown in figure 5 where the measured 'intrinsic' $I_d - V_{ds}$ characteristics of the intrinsic MOSFET are shown. In this case the voltage drop across the drain series resistance is in saturation larger than the voltage drop across the channel of the MOSFET. Due to this large voltage drop across R_d it is no longer possible to include the drain series resistance into the compact MOSFET model. Instead an additional node has to be added for R_d .

A important advantage of separately modeling the series resistance is that better physical parameters for the intrinsic MOSFET are obtained. Since the determination of the gain factor β is no longer affect by the influence of series resistance, a better (larger) value for ΔL is obtained ($0.30 \mu\text{m}$ instead of $0.25 \mu\text{m}$). Also the transversal electric field mobility reduction coefficient becomes channel length independent. As far as the average fit error is concerned, results show that a

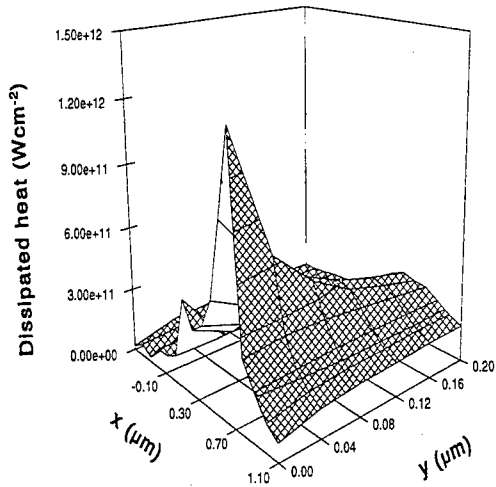


Figure 6: Local heat dissipation for N-channel device. The gate lies between $x=0.0$ and $x=0.60 \mu\text{m}$. As expected the dissipated heat peaks near the interface.

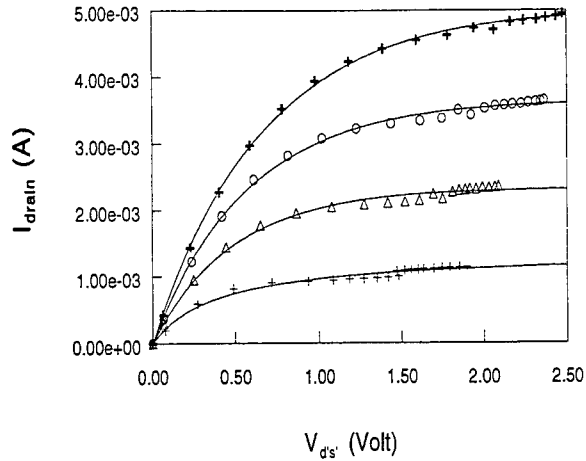


Figure 7: (a) Measured and fitted $I_{drain} - V_{ds'}$ curves for the intrinsic MOSFET ($V_g = 2, 3, 4, 5$ Volt, $L_m = 0.80 \mu\text{m}$ and $W = 10 \mu\text{m}$). The external drain bias varied between 0 and 5.0 Volt.

reduction of 50% in the average fit error is possible for the fitted $I_{ds} - V_{ds}$ characteristics. The disadvantage is of course the increase in the time needed to extract the series resistance parameters and for circuit simulation, an additional has to be added for each MOSFET.

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In situ Doping of Epitaxial Silicon at Low Temperature and Very Low Pressure

X. D. Huang, P. Han, Y. D. Zheng
L. Q. Hu, R. H. Wang, and S. M. Zhu

Department of Physics, Nanjing University, Nanjing 210008, China
Institute of Solid State Physics, Nanjing 210008, China

Remarkable progress in silicon-based device technology has been made by taking advantage of the low-temperature preparation of epitaxial films in the Si/Ge materials system. A variety of unique devices with high performance have been fabricated. Lately, the world's first highly integrated SiGe IC, a 1.0GHz 12-bit digital-to-analogue converter, was developed by IBM and Analog Devices [1]. Low-temperature growth of boron and phosphorus doped films will be necessary in future integrated circuit fabrication. In previous studies the boron doping of Si epilayers may be achieved satisfactorily. However, n-type doping to high levels in low-temperature (450-750°C) Si deposition processes has been difficult due to the heavy reduction of the growth rate [2], [3]. In addition when attempting to incorporate phosphorus concentrations in excess of $1 \times 10^{18} \text{P/cm}^3$ a steady flow of PH_3 produces an unstable level of phosphorus doping [3], [4]. In this instance, it is believed that phosphorus accumulates on and eventually passivates the growth surface. Study of high level ($> 5 \times 10^{19} \text{cm}^{-3}$) n-type doping using SiH_4 as gaseous source has not been reported in the literature. In this paper, we report an investigation of *in situ* doping of Si epi-layers, especially phosphorus doping at high levels.

Doped layers in this study were prepared in Rapid Thermal Process/ Very Low Pressure Chemical Vapor Deposition (RTP/VLP-CVD) reactor which has been previously described elsewhere [5]. The main feature of RTP/VLP-CVD is the use of tungsten-halogen lamps around the quartz tube reactor as energy source to activate deposition reaction. Previous study has shown that the reactant gases are decomposed not only thermally but also photochemically. In this paper, all samples were grown at 600°C. Epitaxial layers were deposited on (100)-oriented Si substrates. Overall initial substrate preparation involved a standard "RCA" cleaning process followed by a 10:1 DI water/HF bath for 15s. This preclean process produces an oxide-free, hydrogen passivated silicon surface. Before deposition the wafers are prebaked in H_2 at 600°C for 15 min, then the major residual species in the reactor is hydrogen. The main growth gaseous source is SiH_4 . The gaseous sources employed for the purpose of doping was 2000ppm B_2H_6 in H_2 and 1800ppm PH_3 in H_2 . The partial pressure of SiH_4 was maintained at 10mtorr during deposition. The ratio of diluted dopant flow rate to SiH_4 flow rate varied from 0.1 to 1.6. Growth duration was between 45 and 150 min producing 80-350-nm-thick epitaxial layers. epi-layer thickness and phosphorus incorporation were determined from spreading

resistance(SRP), secondary-ion mass spectroscopy(SIMS) profiling.

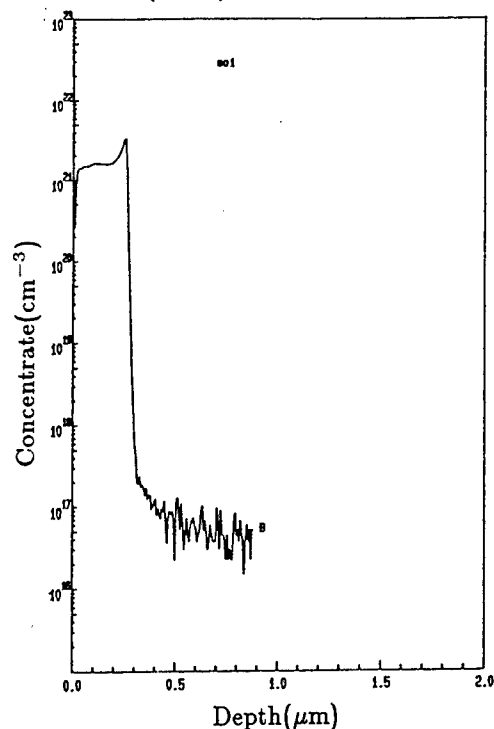


Fig. 1. A typical SIMS profile of boron epitaxial Si deposited at 600°C from SiH₄ and 2000ppm B₂H₆ in H₂.

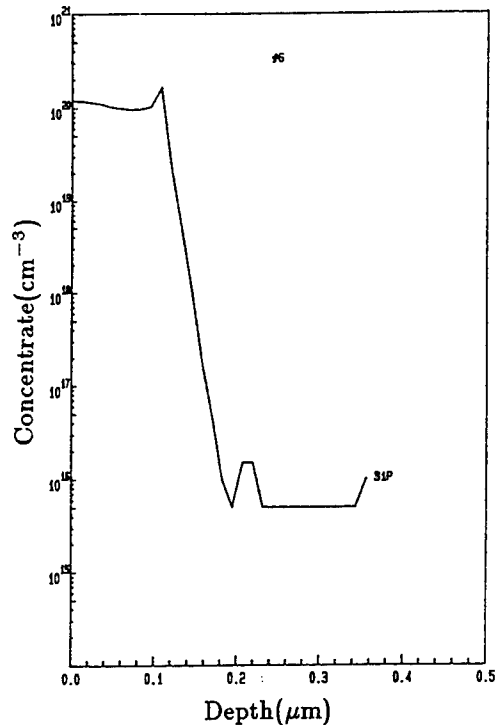


Fig. 2. A typical SIMS profile of phosphorus in epitaxial Si deposited at 600°C from SiH₄ and 1800ppm PH₃ in H₂.

Figure 1 shows a SIMS profile of boron doped Si epi-layer in which boron concentration up to $1.4 \times 10^{21} \text{ B/cm}^3$ has been achieved and sharp doping transition has been obtained. In addition, the boron concentration is proportional to B₂H₆ flow rate (not shown). This is consistent with a simple picture of boron incorporation in which B₂H₆ has a small sticking coefficient and does not block surface sites.

Figure 2 shows a typical SIMS profile of phosphorus doped Si epi-layer in which chemical stability and abrupt dopant transition have been achieved. The flat depth profile shows that epitaxial layer has nearly constant phosphorus level. The incorporation efficiency of phosphorus from the gas phase is stable. A steady flow of PH₃ produces a constant level of incorporated phosphorus rather than a monotonically increasing one [4]. Phosphorus content of epitaxial layer is determined by the phosphine atomic fraction present in the growth source. In this instance of n-type film growth, a surface poisoning effect [6] is not observed. There is no dopant buildup on the growth surface or the reactor wall. Figure 2 also shows that the dopant concentration turn-on slope is about 180Å/decade. In addition, Figure 3 shows the phosphorus doping concentration as a function of the ratio of diluted PH₃ flow rate to SiH₄ flow rate. Chemical concentration as high as $2.5 \times 10^{20} \text{ P/cm}^3$ was achieved. The data suggest that the phosphorus concentration is proportional to diluted PH₃ flow rate and phosphorus does not block surface sites. Many phosphorus doped samples show that the reproducible range of phosphorus concentration is from 1.5×10^{18} to $1.2 \times 10^{20} \text{ P/cm}^3$. We obtained growth rates from a series of SIMS profiles related to samples grown under different PH₃ flow rates, as plotted in Figure 4. The growth rate decreases as the ratio of diluted PH₃ flow rate to

SiH₄ flow rate increases. When the flow rate ratio varies from 0.1 to 1.4, the growth rate decreases from 30 Å/min to 4 Å/min.

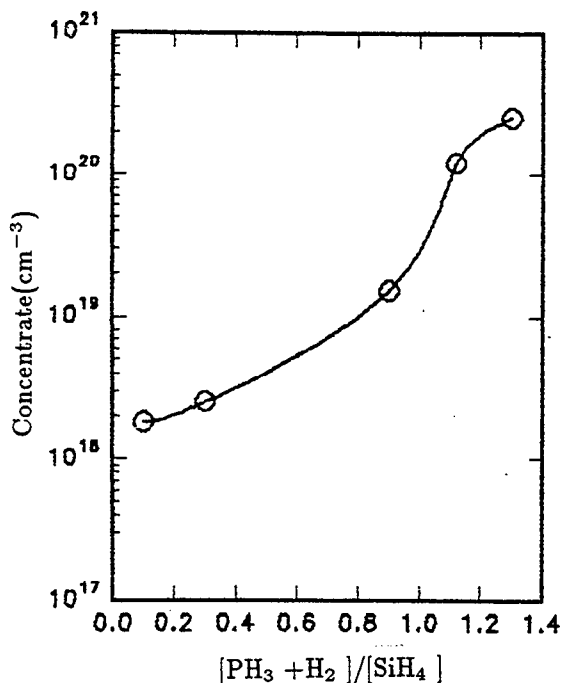


Fig. 3. Phosphorus incorporation in Si as a function of the ratio of diluted PH₃ flow rate to SiH₄ flow rate.

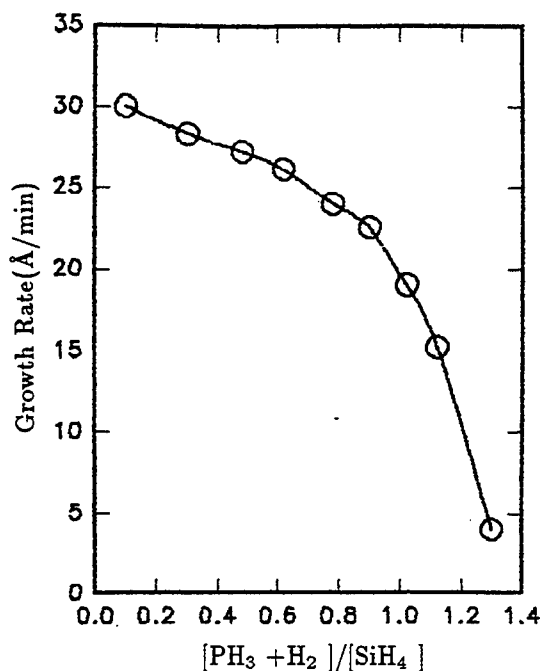


Fig. 4. Phosphorus doped epitaxial Si growth rate dependence on the ratio of diluted PH₃ flow rate to SiH₄ flow rate.

The reason why a constant level of incorporated phosphorus is achieved should attribute to the features of RTP/VLP-CVD and the introduce of a large amount of diluted gas H₂. As reported in previous literature [6], the study of the interaction of SiH₄ and PH₃ with Si(100) surface demonstrates that a stable layer of adsorbed phosphorus will form during the phosphorus-doping deposition process. This high phosphorus coverage leads to accumulation of phosphorus on Si surface, which accounts for the rapid reduction of the Si deposition rate and the unstability of phosphorus content. However, in RTP/VLP-CVD the main feature of selecting tungsten-halogen lamps as energy source to activate deposition reaction has very important effect on the phosphorus doping process. Previous study has shown that the reactant gases are decomposed not only thermally but also photochemically. The consequent activation energy is 4.5Kcal/mol [7], which is much lower than 37Kcal/mol, the activation energy of SiH₄ pyrolysis [8]; so the adsorption coefficient of SiH₄ on Si(100) is high in RTP/VLP-CVD. The reaction probability of SiH₄ on Si(100) will be higher under lower activation energy. The coverage of adsorbed SiH₄ on Si(100) surface will promote greatly; and coverage of adsorbed PH₃ on Si(100) surface will reduce relatively. Consequently, the effect of phosphorus buildup on growth surface will be weakened to a large extent. Furthermore, with presence of a large amount of dilute gas H₂, the desorption of the reaction by-product, H₂ from surface becomes less efficient, so the surface reactive sites are mostly occupied by surface species, H, SiH, SiH₂, SiH₃ rather than phosphorus. The formation of the overlayer of adsorbed phosphorus is hindered by the presence

of dilute gas H_2 . In this instance, there is no accumulation of phosphorus on Si surface. This results in a constant level of incorporated phosphorus. On the other hand, the dilute gas H_2 will decrease the growth rates, since the desorption rate of hydrogen which is the reaction-limited process will decrease with introduce of a large amount of dilute gas H_2 . This reduction of growth rates we believe is a result of the introduce of dilute gas H_2 rather than phosphorus.

In this paper, boron doped Si epi-layer with boron up to $1.4 \times 10^{21} B/cm^3$ has been grown. The results of boron doping are similar to those on other CVD using the same reactant gases. Specially, by using 1800ppm PH_3 diluted in H_2 as dopant in RTP/VLP-CVD, we obtained samples in which phosphorus doping concentrations are constant. Phosphorus concentration as high as $2.5 \times 10^{20} P/cm^3$ was achieved. No evidence shows time-dependent accumulation of phosphorus on the growth surface or the reactor wall. In addition, the growth rates decrease as the flow rate of diluted phosphine increases.

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Formation and optical properties of Ge-Si-Fe alloys

H.Chen, P.Han, L.Q.Hu, Y.Shi, Y.D.Zheng
Department of Physics, Nanjing University, Nanjing 210093,
P.R.China

Recently, there is an increased interest in the use of SiGe layered material for integration with Si technology [1],[2]. The SiGe system has the potential for high speed and optical devices which may compensate for deficiencies of conventional Si devices. But, the biggest problem with SiGe when it comes to optoelectronic application is its indirect band structure. As a result, it is not an efficient light emitter. At the same time, we have noticed a promising material β -FeSi₂ as a semiconductor with a direct band structure [3],[4]. The band gap was measured to be 0.85eV, which makes it an ideal candidate material for both source and detector devices in the 1.3-1.6 μ m wavelength range. In addition, the fabrication procedure is compatible with the silicon-based microelectronic technology, which reveals its brilliant prospects in the optoelectronic industry field.

So, it occurs to us that if we can combine the benefit of direct band structure of β -FeSi₂ with today's developed SiGe techniques, chance is good that we will obtain a new semiconducting material. In another word, since the lattice parameter of Ge is larger than that of Si atom, when some Si atom in the β -FeSi₂ lattice structure are replaced with Ge atom, a certain kind of lattice distortion will take place, resulting in respective changes of β -FeSi₂ band structure and especially a shift of band gap.

As we know, the conventional method to fabricate β -FeSi₂ thin films is solid phase epitaxy(SPE) or reactive deposition epitaxy(RDE), which involves iron deposition process on silicon substrate and a following annealing process. In our experimental work, to form the Ge-Si-Fe alloys, a new attempt is made to first grow iron thin films epitaxially onto hot SiGe substrate and then take annealing process at higher temperature.

In this paper, we report for the first time the synthesis of Ge-Si-Fe alloy, a new semiconducting material. The whole process of Ge-Si-Fe alloy fabrication includes the SiGe strain relaxed epitaxial layer preparation, iron deposition onto the SiGe layer and annealing process. The SiGe layer were prepared by grow epitaxial strain relaxed SiGe layer on silicon substrate. A very low pressure chemical vapor deposition system (RTP/VLP-CVD) has been used to grow epitaxial SiGe layer on Si substrate. The deposition process details of the growth system has been described elsewhere [5]. Auger electron spectroscopy(AES) shows the SiGe layer has been successfully grown on Silicon substrate with the Ge content of 7%. Then iron was deposited onto hot SiGe layer followed by a annealing process at about 700°C for 30min in a high vacuum evaporation system. The ex-situ Auger electron spectra shows that the thickness of Ge-Si-Fe alloy films

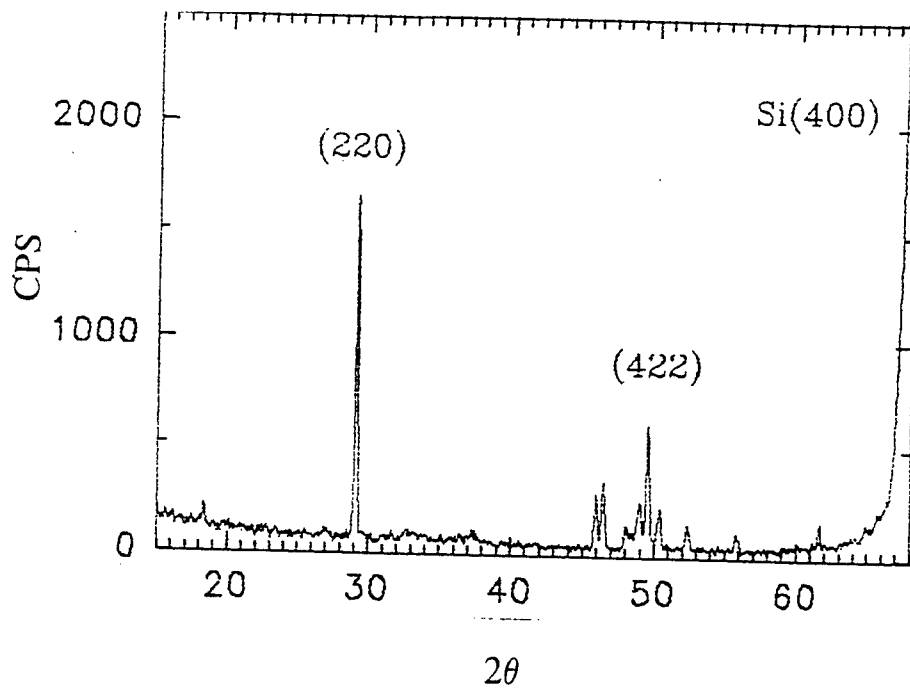


Fig1.X-ray diffraction pattern for Ge-Si-Fe alloy thin film.

grown on SiGe layer is about 1700\AA . For comparison, a Si(100) substrate has been taken into the evaporation chamber together with the SiGe layer to grown epitaxial $\beta\text{-FeSi}_2$ Thin film under the same process condition.

X-ray diffraction(XRD) measurement and Auger electron spectroscopy (AES) have been applied to investigate structure properties and depth profile of the new Ge-Si-Fe alloy thin film. Optical transmission measurement was followed to investigate its optical properties. XRD plot is shown in fig.1, which gives a set of diffraction peaks of Ge-Si-Fe alloy. The set of peaks is almost the same as that of $\beta\text{-FeSi}_2$ [6] thin film. On the other hand, Ge in the Ge-Si-Fe alloy has been detected by Auger electron spectroscopy. The content of Ge is very low, about 2.5%. So, We can draw a conclusion that the distortion caused by the Ge replacement is so small that the changes of lattice parameters of $\beta\text{-FeSi}_2$ can't be observed from the XRD results due to the very low content of Ge in alloy films. For convenience, we continue to use the Miller indices of $\beta\text{-FeSi}_2$ to represent the diffraction peak of Ge-Si-Fe alloys. Among the peaks, (220) peak is the most prominent one, sharp and intense, which gives a strong evidence of high crystal quality.

Optical transmission spectroscopy technique has been employed to study the band structure of Ge-Si-Fe alloy thin films. Fig.2 shows the transmission spectra of Ge-Si-Fe alloy and $\beta\text{-FeSi}_2$. Both Ge-Si-Fe alloy and $\beta\text{-FeSi}_2$ thin film exhibits a strong absorption, while the absorption edge energy of Ge-Si-Fe alloy is lower than that of $\beta\text{-FeSi}_2$. This result shows that Ge-Si-Fe is a new semiconducting material with direct band gap a little lower than that

Fig.2 Optical transmission spectra of Ge-Si-Fe alloy and β -FeSi₂ thin film , which shows apparent shift of absorption edge of Ge-Si-Fe alloy from that of β -FeSi₂.

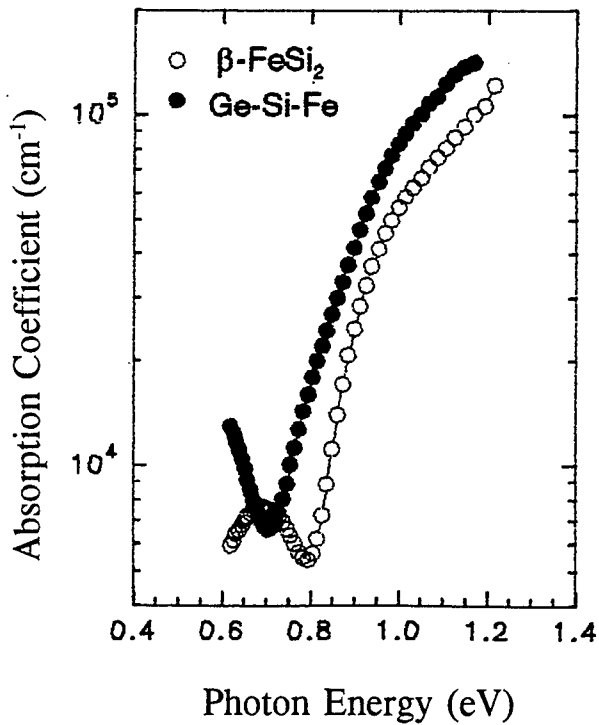
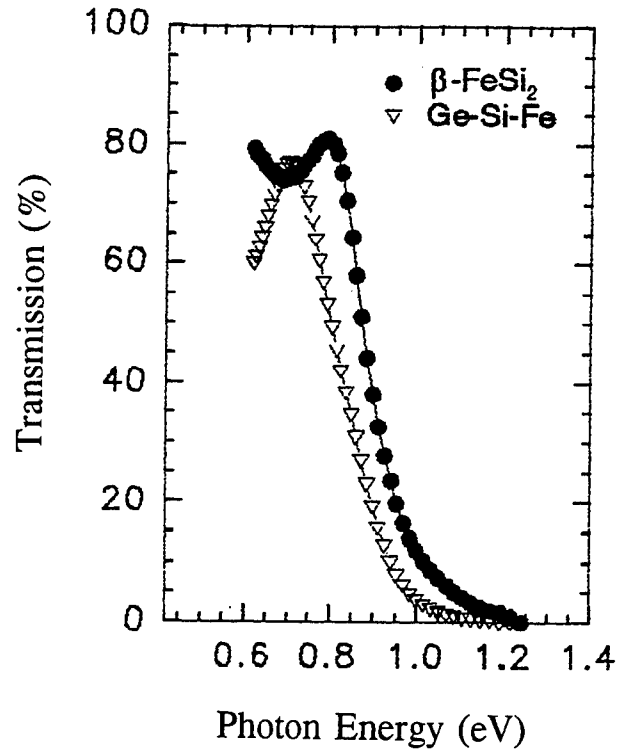


Fig.3 Absorption coefficient vs photo energy for Ge-Si-Fe alloy and β -FeSi₂ thin film. The strong increase of absorption coefficient up to 10⁵cm⁻¹ is consistent with the existence of direct energy gap.

of β -FeSi₂. The onset of absorption just below 0.6eV is due to extrinsic transitions involving defect states within the forbidden energy gap [6]. Absorption coefficient of Ge-Si-Fe alloy and β -FeSi₂ as fig.3 shows is deduced from the transmission data. A strong increase of absorption coefficient up to 10^5cm^{-1} can be observed, which is consistent with the existence of a direct optical gap of the new alloy. In order to estimate the energy gap of Ge-Si-Fe alloy, plots of absorption coefficient square versus the photon energy were made, which exhibit straight line and indicate a direct band gap of 0.83eV while β -FeSi₂ at 0.87eV.

In conclusion, a new semiconducting material Ge-Si-Fe alloy thin film has been achieved by using reactive deposition epitaxy on strain relaxed GeSi layer. The new Ge-Si-Fe alloy exhibits exciting direct optical absorption near 0.83eV in the optical transmission measurement, which means a shift of band gap from β -FeSi₂ thin film. It offers new choice for silicon-based optoelectronic device engineers to "tailor" the optoelectronic properties to the need. We are suggesting that by changing the content of Ge in the alloy, Ge-Si-Fe alloy with desired energy gap can be formed, following the way opened for GeSi system several years ago. The first step has been taken to study the formation and properties of the new alloy in our research work, further investigation is quite necessary about the role of Ge atoms in the new alloy, the kinetics of fabrication process and the potential prospect of application.

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Evaluation of Silicon Ion Implant Damage in Epitaxial MBE-Grown GaAs from Room and High Temperature Capacitance-Voltage Measurements

Edward Russell¹, R. Jennifer Hwu¹, Larry P. Sadwick¹, and Nick A. Papanicolaou²

¹Department of Electrical Engineering, The University of Utah, Salt Lake City, UT 84112
(801) 581-8282 FAX (801) 581-5281

²Naval Research Laboratory, Washington, D.C. 20375
(202) 767-4898 FAX (202) 767-0455

Abstract

Damage and diffusion caused by silicon (Si^+) ion implantation into epitaxial gallium arsenide (GaAs) was studied by capacitance versus voltage (C-V) measurements as a function of temperature from 25 to 300°C. The C-V measurements were performed on gallium arsenide low doped (n-type, 10^{15} cm^{-3}) epitaxial material grown by molecular beam epitaxy (MBE) to a nominal thickness of 5 μm on semi-insulating gallium arsenide (GaAs) substrates. The GaAs material was separated into three regions labeled A, B, and C, respectively. The first (A) and second (B) regions each received an implant at a dose of $5 \times 10^{12} \text{ cm}^{-2} \text{ Si}^+$. Region A was implanted at an energy of 250 KeV and region B was implanted at an energy of 100 KeV. The third region (C) served as a reference region and was not implanted. To gain further understanding into the damage caused by ion implantation, no annealing was performed after the ion implantation.

The technology of solid state devices and circuits is constantly moving towards increased speed, miniaturization, and higher temperature operation. High speed devices that operate effectively from room temperature (25°C) to 300°C are needed for use in such areas as the automotive industry, the aerospace industry, geothermal exploration, space exploration, and super computers. Systems required for cooling electronic components add weight and complexity to the product. In the aerospace industry, weight is an especially critical factor. If the weight and space utilized by cooling equipment can be reduced or eliminated by using more heat resistant components, critical factors such as payload and range can be increased. The pursuit of high speed and high temperature devices for use in industry has prompted research in semiconductors including III-V materials and silicon carbide (SiC) both of which have reached a relatively high level of processing and device maturity. III-V materials such as gallium arsenide (GaAs) offer the capability of operating both at higher speeds and higher temperatures than silicon (Si) and have a more mature technology base than SiC. For these and other reasons, we have been investigating the high temperature electrical properties of GaAs-based devices. Ion implantation of GaAs is an attractive, cost-efficient, and established technology to produce active regions in semi-insulating GaAs for low-parasitic, high speed devices. However, ion implantation does cause damage to GaAs [1-7]. Although most of this damage can be thermally annealed out, certain carrier compensating defects remain [1-4]. Some of these carrier compensation defects may be due to gallium (Ga) vacancy-donor complexes which have been detected by photoluminescence (PL) [3] and cathodoluminescence [4] while other defects related to ion implantation damage remain undetected. Others have reported the on the effects of background doping and implant damage on the diffusion of implanted Si in GaAs [6,7]. To fully understand, characterize, and exploit GaAs-based electronics at high temperatures, it is necessary to investigate trap-related phenomena and ion-implanted damage in GaAs at high temperatures. In this paper, we continue our investigation of the capacitance vs. voltage (C-V) characteristics as a function of temperature on ion-implanted GaAs first reported at the 1993 ISDRS [1].

The C-V measurements were performed on circular capacitor structures which consisted of a 1000Å, 130 μm diameter titanium tungsten (TiW) Schottky metal contact surrounded by a TiW field separated from the circular metal contact by an annular gap. These C-V structures were specially designed to investigate the effects of high temperatures on ion-implanted GaAs. Figure 1 shows the room temperature C-V curves for the unimplanted, 250 KeV, and 100 KeV capacitors. As can be clearly seen, for any voltage, between +0.5 to -15 volts, the unimplanted reference region has the highest capacitance value of the three regions. This can be easily understood in terms of carrier trapping caused by the ion implantation process. The 250 KeV region has considerably more damage than the 100 KeV region. Carrier concentration vs. depth measurements of the two implanted regions (region A: 250 KeV, region B: 100 KeV) and the reference region (C) as a function of temperature from room temperature to 300°C were calculated from the raw C-V measurement data. No unusual or unexpected features were observed in the region C C-V characteristics at high temperatures. Figure 2 shows the semi-log room temperature carrier concentration versus depth plots for all three regions. Figure 3 shows a linear plot of the data shown in Figure 2. As can be clearly seen from Figures 2 and 3, in addition to the implant damage, there is some activation of the implant. Also easily observable is that for the ion implanted regions the free carriers are absent up to a distance of 2 μm from the surface. This situation changes significantly at higher temperatures. Figure 4 shows the carrier concentration versus depth at room temperature, 100°C, 150°C, and 200°C for a 250 KeV ion implanted capacitor.

From the data presented in Figures 1 through 4 we can draw some general conclusions that have been verified on the three-region capacitors and other capacitors not shown or discussed in this paper. Temperatures as high as 300°C did not result in any permanent change, redistribution of carriers, or other damage to any of the three regions. However, as seen previously in other samples presented at the 1993 ISDRS, a carrier peak is observed at elevated temperatures that moves closer to the surface as the temperature increases. This subsurface peak was observed for all region A and B capacitors tested at high temperatures. The onset of the subsurface peak can be clearly detected at temperatures as low as 100°C (more typically, in the range of 125 to 175°C) and moves monotonically closer to the surface with increasing temperature. For regions B and C, the concentration near the surface first increases monotonically with temperature (in this case up to about 200°C) and then decreases monotonically as temperature is further increased. To more fully understand these effects we have performed C-V measurements on region A and B material that has received standard annealing treatment after implantation. Details of the damage, diffusion, and redistribution of the both the epitaxial and implanted Si will be presented.

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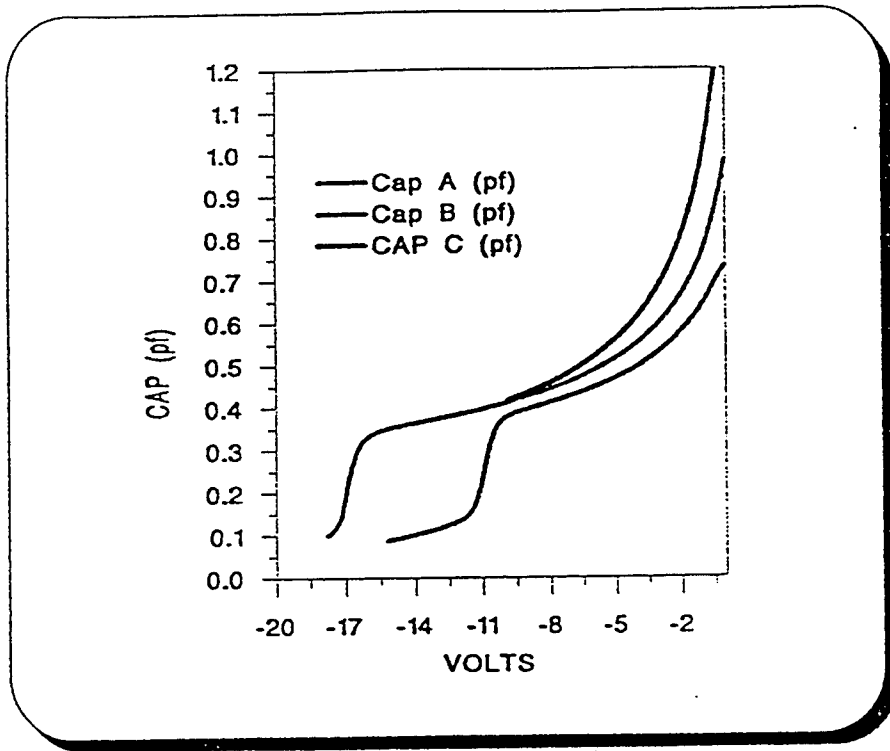


Figure 1. Plot of capacitance versus voltage for samples A, B and C at room temperature.

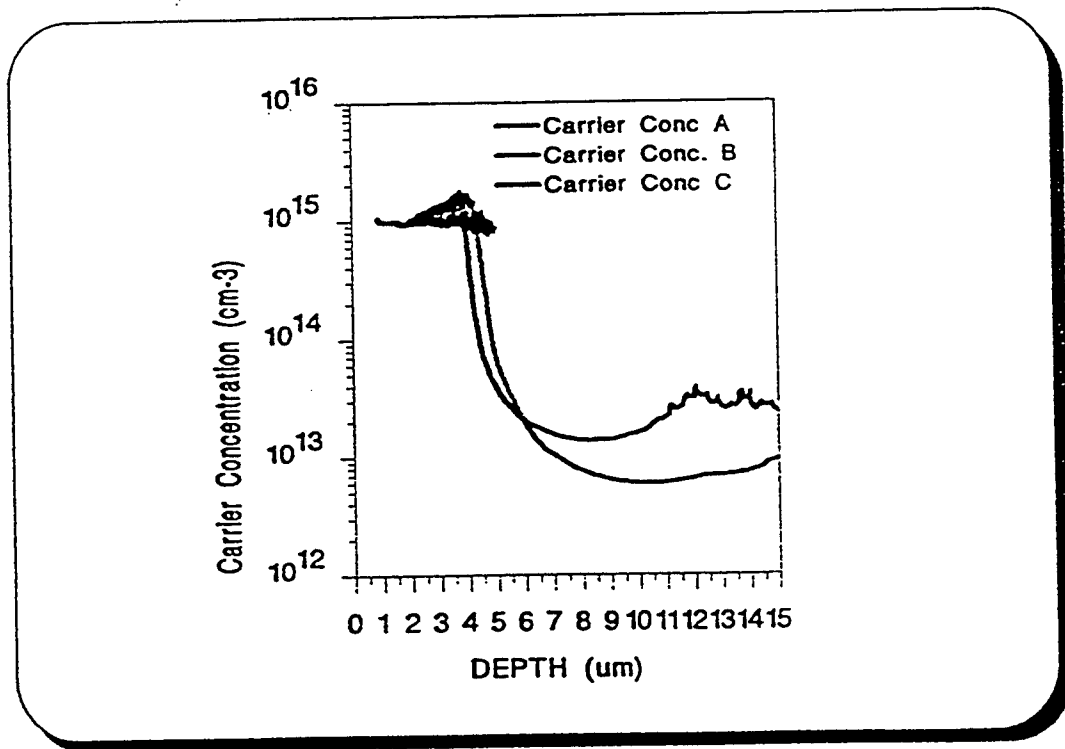


Figure 2. Plot of carrier concentration for samples A , B and C at room temperature

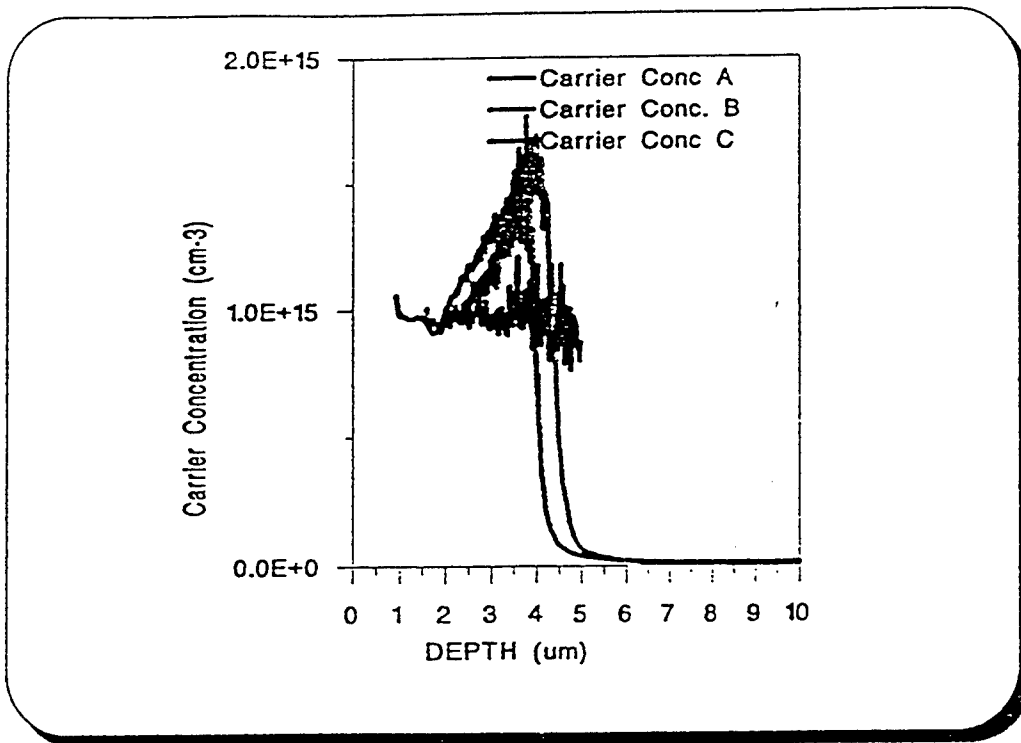


Figure 3. Linear plot of carrier concentration versus depth for samples A , B and C at room temperature

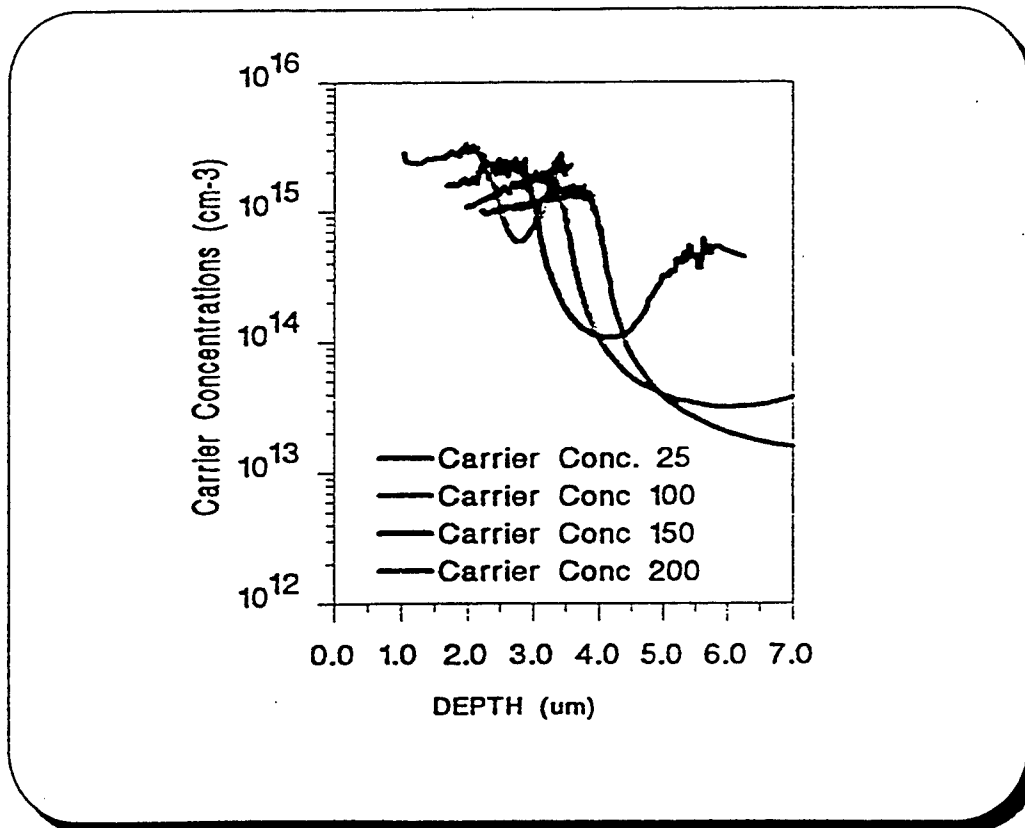


Figure 4. Plot of carrier concentration versus depth for sample A from room temperature to 200 Celsius.

NANOMETER-SCALE MAPPING OF DOPED LAYERS IN InP STRUCTURES AND DEVICES

M. V. Moore and R. Hull, Department of Materials Science, University of Virginia, Charlottesville, VA 22903; R.F. Karlicek, Jr. and M. Geva, AT&T Bell Laboratories, 9999 Hamilton Blvd., Breinigsville, PA 18301; P. D. Carleson, FEI Company, 7451 N.E. Evergreen Pkwy., Hillsboro, OR 97124; J.F. Walker, FEI Europe Inc., Brookfield Business Center, Cottenham, Cambridge CB44PS, England

We have observed strong contrast between organometallic vapor phase epitaxy-grown p-doped (Zn), i-doped (Fe), and n-doped (Si, S) layers in InP samples which are prepared with a Ga⁺ focussed ion beam (FIB) for imaging with a transmission electron microscope (TEM) [1]. This unexpected contrast is extremely powerful for nanometer-scale mapping of dopant distributions in InP-based structures and devices.

Doping concentrations as low as 10^{17} cm^{-3} can be imaged with this technique; contrast levels of 20%-50% between p- and i- (dark in the image) and n-type (light) layers have been observed in the dopant range of 10^{17} cm^{-3} - 10^{18} cm^{-3} . Spatial resolution is on the order of tens of nanometers or better. These resolution limits extend the capabilities of mapping of dopants in InP-based devices.

We have only observed this contrast in doped InP, not in comparably doped Si, GaAs, or ZnSe. The anomalous contrast is only present in samples milled in a FIB, which uses a 30 keV Ga⁺ beam at glancing incidence to the sample surface; the contrast is not observed in samples prepared with conventional Ar⁺ ion milling, which employs a 5 keV beam at an incident angle of 14-18 degrees. The contrast present in the FIB-prepared samples increases under electron irradiation in the TEM. We are currently seeking to explain the physical mechanism for producing this contrast. It is not conventional TEM diffraction contrast, since the polarity of the image does not reverse under any imaging condition, including when the diffraction condition is changed from bright field to dark field. The contrast is determined to be of the "absorption" type, corresponding to differential scattering of electrons out of the image collection system, although it is not clear how a change of 1 in 10^5 atoms can produce 20% - 50% contrast. Our current understanding of the contrast mechanism centers upon generation of point defects in the FIB and TEM and on the nature of the bonds in the material. To see if the contrast mechanism depends on the covalent-ionic nature of the bonds in InP, we are examining InGaAs(P) ternary and quaternary materials that have bonds of varying degrees

of covalency and ionicity. We are also investigating the sensitivity of the contrast to types of dopant atoms as well as their concentrations.

Examination of the InP doping superlattice (grown as 200 nm of $2 \times 10^{18} \text{ cm}^{-3}$ Si + 200 nm of 2×10^{18} Zn bilayers) shown in Figure 1 shows the application of this technique to studying growth and diffusion over nonplanar surfaces. Growth rates were obtained by measuring the bilayer thickness, and Zn diffusion lengths were calculated by subtracting half the bilayer thickness from the dark p-doped (Zn) layer; the results are shown in the contour map of Figure 2. This is a new technique for studying nonplanar growth and diffusion in InP structures with direct application in the study of regrowth of current blocking layers around etched mesas in CMBH (capped mesa buried heterostructure) lasers.

In summary, we have found a new technique for nanometer-scale mapping of dopants in InP. Our future goals are fourfold: (1) to further calibrate and, we hope, extend, the limits of the technique in InP; (2) to understand the mechanism of the contrast; (3) to extend the capability of high-resolution dopant mapping to other materials; (4) to apply the technique to other structures of technological interest.

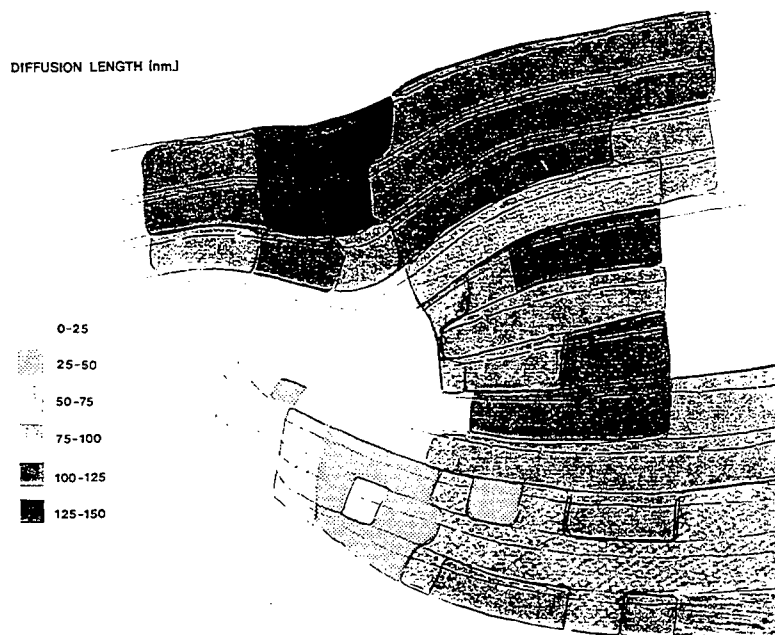
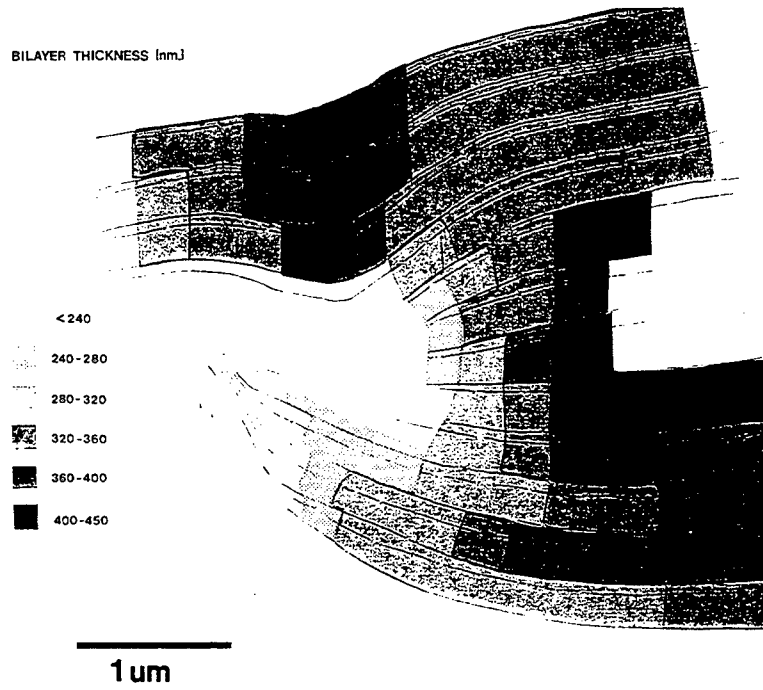
We gratefully acknowledge critical prior collaboration with D. Bahnck and F.A. Stevie of AT&T.

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FIG. 1. InP doping superlattice (200 nm of n-type $2 \times 10^{18} \text{ cm}^{-3}$ Si + 200 nm of p-type $2 \times 10^{18} \text{ cm}^{-3}$ Zn bilayers) grown over the etched mesa in the geometry which is intermediate to the CMBH laser fabrication process; shown are p- (dark) and n- (light) doped layers and laser stripe labelled "A."

FIG.2. (a) Bilayer thickness and (b) Zn diffusion length of the image in Figure 1.



Effects of Emitter Set-Back Layer Thickness on the Performance of GaInP/GaAs Heterostructure-Emitter Bipolar Transistors⁺

Y. F. Yang, C. C. Hsu*, and E. S. Yang
Department of Electrical Engineering
Columbia University, New York, N. Y. 10027

* Department of Electronic Engineering
The Chinese University of Hong Kong, Hong Kong

Recent studies showed that heterostructure-emitter bipolar transistors can not only overcome some drawbacks of conventional HBTs, but can also offer a high current gain, a low offset voltage and good uniformity [1-3]. The thickness of the emitter set-back layer plays an importance role for the HEBT performance. However, previous studies were mainly based on DC performance [1, 2]. In this paper, the investigations of the effects of the emitter set-back layer on both DC and RF performance of GaInP/GaAs HEBTs are presented experimentally and theoretically.

C-doped GaInP/GaAs HBTs and HEBTs were fabricated same as reference [3]. HEBTs with two emitter set-back layer thicknesses (W_e) of 150Å and 300Å are designated HEBT(150Å) and HEBT(300Å), respectively. Non self-aligned cross section of devices is shown in Fig. 1. The heterostructure-emitter consists of an n-GaAs emitter set-back layer sandwiched between an n-GaInP confinement layer and a p-GaAs base layer. There are two possible cases for the emitter junction under forward bias. The emitter set-back layer is fully depleted when the base-emitter bias is low or the emitter thickness is thin. In this case, if the emitter potential spike is below the base conduction band, the electron injection from the emitter to base is the same as homojunction,

otherwise the electron injection is like the heterojunction. The hole injection current from the base to emitter follows that of the heterojunction. When the base-emitter bias is high or the emitter set-back layer is thick, the emitter set-back layer is partially neutral. The band diagram for this case is shown in Fig. 2. The electron injection current is like the homojunction. The hole current consists of the recombination current (J_{p1}) in InGaP layer region and the recombination current (J_{p2}) in neutral n-GaAs region due to the hole storage. The hole storage also contributes diffusion capacitance to the total emitter capacitance. By solving the one dimensional Poisson's equation, diffusion equation and current continuity equation under depletion approximation, the current gain, collector to emitter offset voltage and emitter capacitance are calculated.

Fig. 3 shows calculated and measured gains for HBT and HEBTs. The results show that the current gains of HEBTs are the same as those of HBTs at a low current regime. The gain of HEBT(150Å) tracks that of HBT, while the gain of HEBT(300Å) is lower than that of HBTs in the high current regime. Calculation indicated that the lower gain of HEBT(300Å) is due to the hole recombination in the n-GaAs region under high forward bias.

⁺ This work was supported by JESP and NSF

The offset voltage versus the emitter set-back layer is shown in Fig. 4. The offset voltage decreases with the increase of W_e and becomes constant for $W_e > 100\text{\AA}$. This indicates that W_e of 100\AA is enough to eliminate the effect of the emitter potential spike on the emitter injection current.

The calculated emitter capacitance (C_e) versus collector current density for HBT and HEBTs is shown in Fig. 5. The emitter capacitance consists of depletion and diffusion capacitances. The calculation indicates that the diffusion capacitance of HBT and HEBT(150\AA) can be neglected so that the emitter capacitances of them consist of only depletion capacitance for a collector current density (J_c) less than $7 \times 10^4 \text{ A/cm}^2$. However, the contribution of the diffusion capacitance to C_e is significant for HEBT(300\AA) at a $J_c > 10^3 \text{ A/cm}^2$. This is because the hole storage in the emitter set-back layer. The value of C_e for HBTs is slightly higher than that of HEBT(150\AA) for $J_c > 1 \times 10^3 \text{ A/cm}^2$ due to the higher base-emitter bias necessary for HBT to reach the same current level as HEBT. However, the difference in C_e is insignificant. In order to compare the calculated results with measured values, the emitter capacitances of fabricated small size devices [3] were extracted based on the measured S-parameters [4]. Fig. 6 shows the calculated and measured emitter capacitances as a function of the emitter set-back layer thickness at J_c of $1 \times 10^4 \text{ A/cm}^2$. The values of C_e of HBT and HEBT(150\AA) are the same, but the value of C_e of HEBT(300\AA) is about twice as large as that of HBT.

Cutoff frequencies were calculated by using calculated emitter capacitances and assuming that the devices have the same parasitic resistances ($R_{CC}+R_{EE}$) and collector capacitances as measured from HBT sample and the same base to collector transit times as estimated from device structure.

Fig. 7 shows the cutoff frequencies versus emitter set-back layer thickness at J_c of $1 \times 10^4 \text{ A/cm}^2$. The cutoff frequencies from calculation are the same for the devices with W_e less than 200\AA and decrease for the devices with W_e larger than 200\AA . The peak cutoff frequencies also shown in Fig. 7 from fabricated $5 \times 5 \mu\text{m}^2$ devices are 37, 31 and 20 GHz for HBT, HEBT(150\AA) and HEBT(300\AA), respectively. The lower values of measured cutoff frequencies for HEBTs than those of calculation are due to the higher values of $R_{CC}+R_{EE}$ for HEBTs than that of HBT. Small signal parameters of each sample extracted from measured S-parameters show that the collector capacitances are the same for all samples. The value of $R_{CC}+R_{EE}$ for HBT is lowest and the value of $R_{CC}+R_{EE}$ is highest. If the values of $R_{CC}+R_{EE}$ are the same for all samples, the agreement of the experiment and the calculation should be good.

In summary, it is shown that the emitter diffusion capacitance due to the hole storage degrades the HEBT DC and RF performance, if the emitter thickness is not properly designed. From above results, the optimal thickness of the emitter set-back layer has been found to be $100\text{-}200\text{\AA}$ for GaInP/GaAs HEBTs. Devices with an optimal W_e show good DC and RF performance. In addition, because the p-n junction of the HEBT is away from the heterointerface, the HEBT structure can be more reliable in terms of the base dopant outdiffusion and will be attractive in circuit applications.

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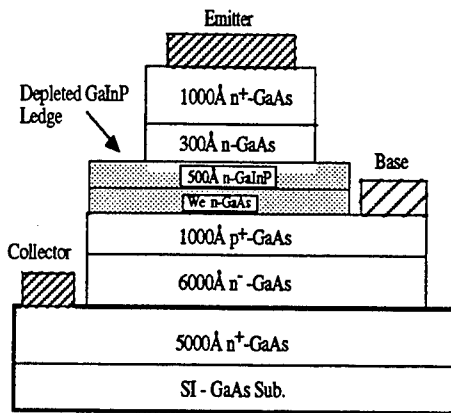


Fig. 1 Cross section of GaInP/GaAs devices. $W_e = 0, 150\text{\AA}$ and 300\AA for HBT, HEHT(150\AA) and HEHT(300\AA), respectively.

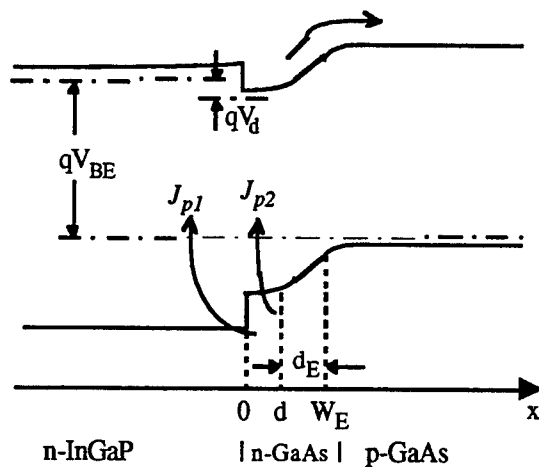


Fig. 2 Band diagram of the heterostructure-emitter junction under forward bias. $0 < x < d$ is the neutral emitter region and $d < x < W_E$ is the depletion region.

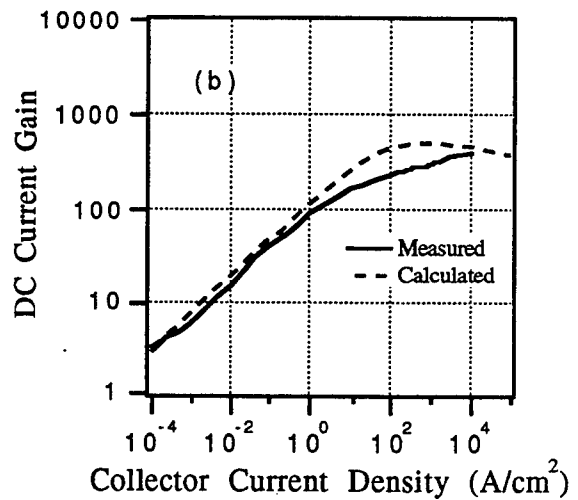
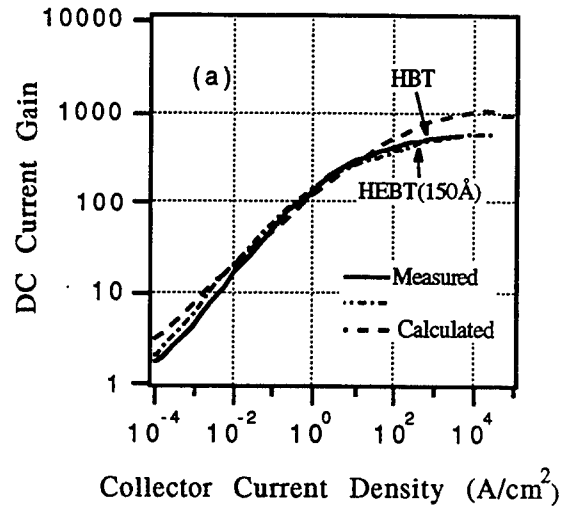


Fig. 3 Calculated and measured current gains versus collector current density (a) HBT and HEHT(150\AA) and (b) HEHT(300\AA).

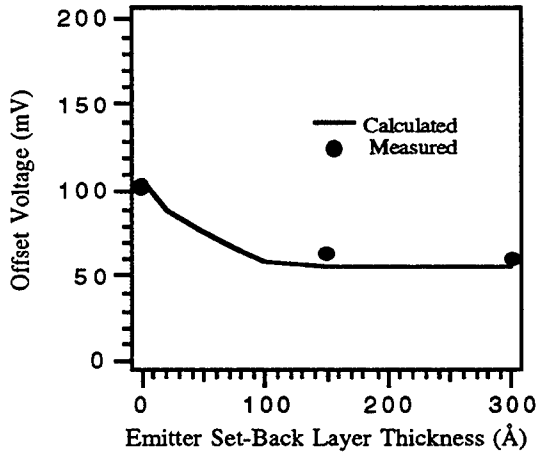


Fig. 4 Calculated and measured offset voltages versus emitter set-back layer thickness.

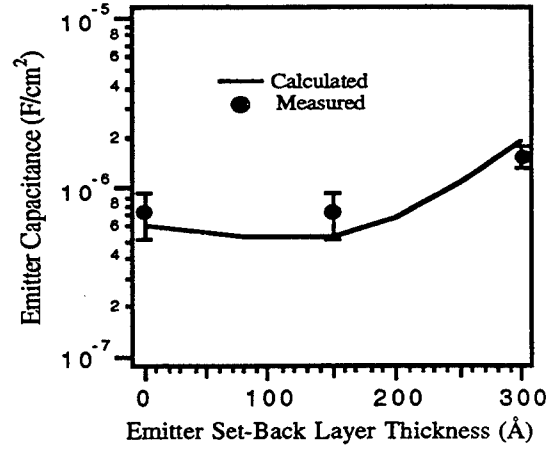


Fig. 6 Calculated and measured emitter capacitances versus emitter set-back layer thickness at J_c of 1×10^4 A/cm².

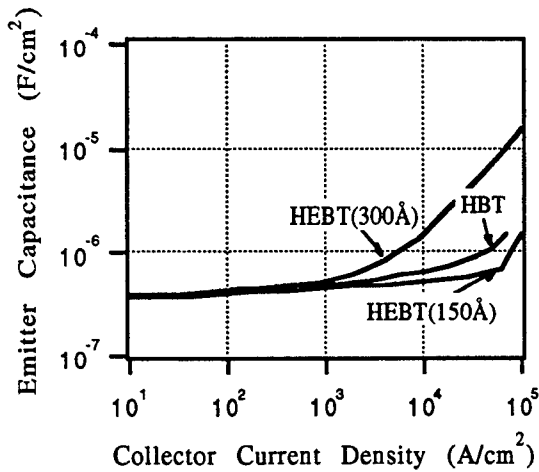


Fig. 5 Calculated emitter capacitances versus collector current density for HBT, HEBT(150Å) and HEBT(300Å).

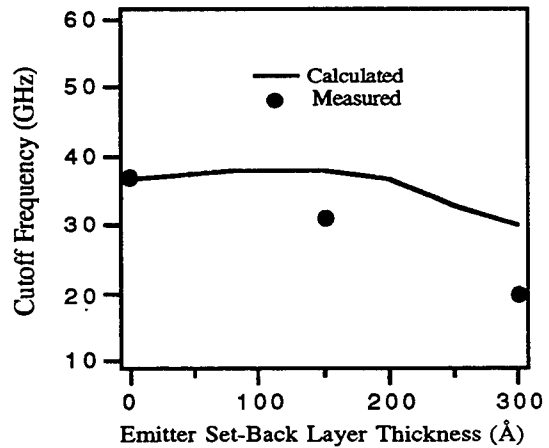


Fig. 7 Calculated and measured cutoff frequencies versus emitter set-back layer thickness at J_c of 1×10^4 A/cm².

Optical Techniques for the Nondestructive Characterization of 3-580 μm Thick Si Substrates

C.S. DeMain, S.H. Jones, T. Globus
University of Virginia
Applied Electrophysics Laboratory
Department of Electrical Engineering
Charlottesville, Virginia 22903

With the advent of micromachining and microelectromechanical devices, there is an increasing need for ultra-thin silicon substrates. Similarly, there is need for simply measuring and verifying the substrate absolute thickness and thickness uniformity. We report simple and accurate techniques of nondestructive optical characterization for measuring the absolute thickness and total thickness variation (TTV) of ultra-thin and nominally thick (3-580 μm thick) silicon substrates (1-4 inch diameter).

To measure TTV, an interferometer system has been built. The interferometer uses a long wavelength semiconductor laser, simple optics, and an infrared camera so that an image of each wafer and its interference fringes can be viewed. The surface of the wafer is only touched when handling the substrate. The fringes, caused by interference of the infrared light bouncing off front and back silicon surfaces, relate directly to the thickness variation across the substrate; each fringe corresponding to a quarter wavelength variation in thickness (approximately 100nm). Clear and sharp fringe patterns allow for rapid inspection of substrates. This TTV system is used to verify both flatness and thickness uniformity with 100 nm resolution. Typical results are shown in Figure 1.

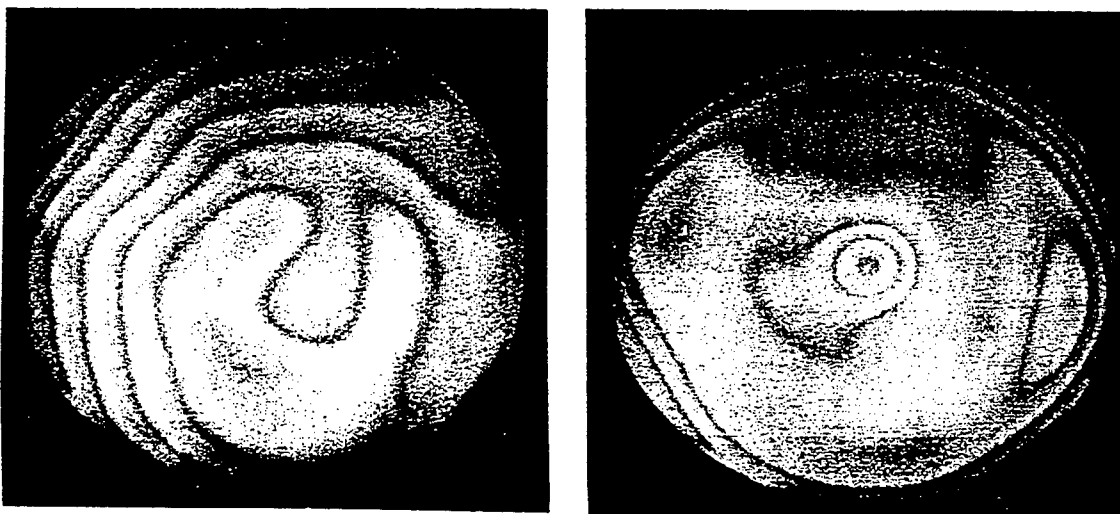


Figure 1. Interference fringe patterns of two Si substrates as seen by interferometer system.

A spectrophotometer has been used to develop a set of standards by determining and mapping the absolute thickness of several substrates. The spectrophotometer scans through a series of wavelengths, ranging from $3.3\mu\text{m}$ to $0.6\mu\text{m}$, resulting in an interference fringe signature as shown in Figure 2.

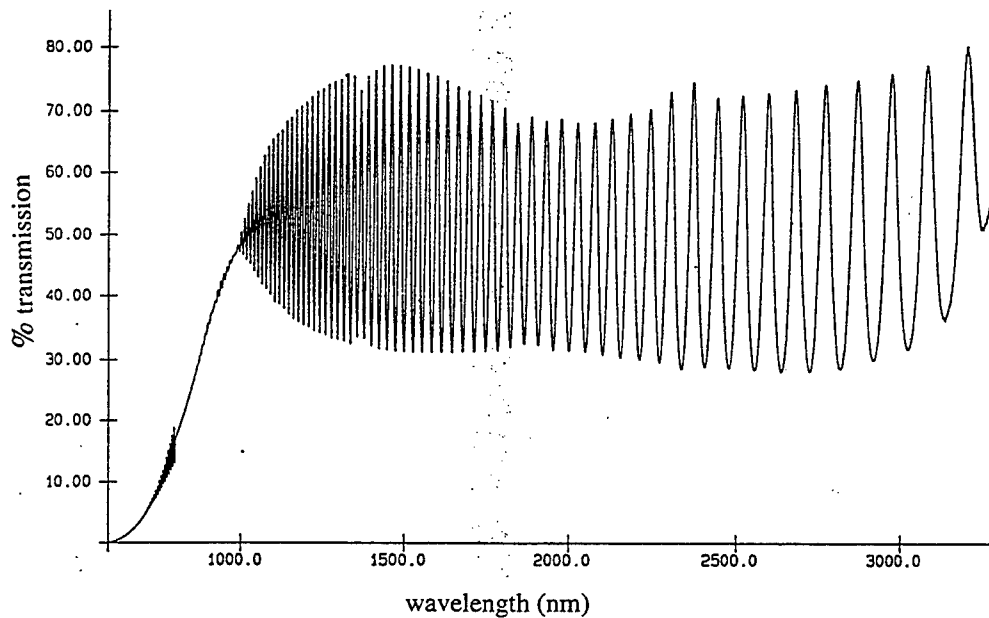


Figure 2. Interference fringe signature from spectrophotometer of a $12\mu\text{m}$ thick Si substrate.

From this data, the average absolute thickness is derived. Also, the interference signature at near band edge wavelengths as well as longer wavelengths are related to the overall quality of the silicon substrate.

Based on the spectrophotometer results, a simple optical transmit-and-receive system has been calibrated to measure the substrate absolute thickness from the detected absorption. The LED transmit-and-receive system can be used to scan the wafer absolute thickness without subjecting the wafer to any mechanical stress. This simple nondestructive absolute thickness measurement is more accurate than a mechanical micrometer, and is integrated with the TTV system. A green LED system is used for measuring $3\text{-}7\mu\text{m}$ thick substrates, a red LED is used for measuring $5\text{-}150\mu\text{m}$ samples, and an IR LED is used for the thicker wafers. Characterization results for a series of high quality double side polished $3\text{-}580\mu\text{m}$ silicon substrates will be presented. Substrates have been provided by Virginia Semiconductor Incorporated.

PHONON OSCILLATIONS IN A SPECTRUM OF REVERSIBLE BLEACHING
OF GALLIUM ARSENIDE UNDER INTERBAND ABSORPTION OF A
HIGH-POWER PICOSECOND LIGHT PULSE

I.L.Bronevoi

Institute of Radioengineering and Electronics, Moscow

This text describes the results of studies with picosecond resolution of the optical transparency T spectra of a thin layer of a high-purity GaAs exposed to a high-power light pulse having the photon energy $\hbar\omega_{ex}$, which is somewhat larger than the forbidden gap width E_g . Experiments were carried out at room temperature. The duration of both the exciting and probing pulses was about 14 ps. Figure 1 shows results of the sample transparency measurements as a function of the energy of a photon of the probing pulse $\hbar\omega_p$ (the bleaching spectrum) within the $\hbar\omega_p < \hbar\omega_{ex}$ range. In this spectrum, which has been measured nearly at the moment of the maximum of the exciting pulse intensity, were found local minima. An oscillating character of the bleaching has been observed for a variety of values of $\hbar\omega_{ex}$ and the exciting pulse integral energy W_{ex} , the spectral localization of minima being retained. However at the drop of excitation and after its cessation the oscillations smoothed and

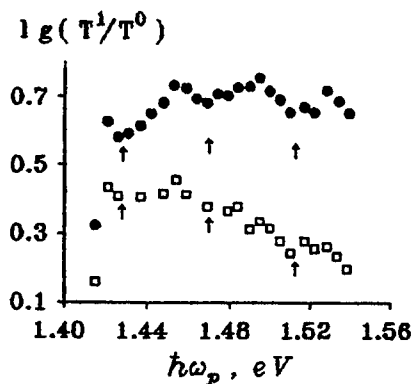


Fig.1. Transparency T variation (indices 1 and 0 show the presence and absence of the excitation, respectively) of GaAs as a function of $\hbar\omega_p$. The delay time of the probing pulse with respect to the exciting one $\tau_d = -3$ ps, $\hbar\omega_{ex} = 1.558$ eV: \bullet - $W_{ex} = 1.0$ a.u.; \square - $W_{ex} = 0.19$ a.u., W_{ex} being the energies of the excitation pulse.

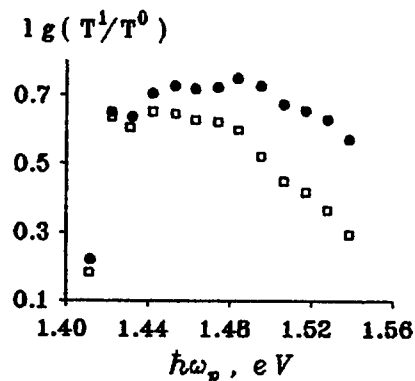


Fig.2. GaAs transparency variation as a function of the photon energy of the probing pulse $\hbar\omega_p$ at $\hbar\omega_{ex} = 1.558$ eV, $W_{ex} = 1.0$ a.u.: \bullet - $\tau_d = 13$ ps; \square - $\tau_d = 31$ ps.

then disappeared (Fig. 2) despite the bleaching degree being nearly equal to that shown in Figure 1. Oscillations have also been far less strong at $\hbar\omega_p > \hbar\omega_{ex}$. This behavior of oscillations, as well as the fact that there is an anti-reflective coating on the sample surface, do not permit to attribute the oscillations to the interference in the sample. It should be noted that during the excitation pulse there appears a recombinative edge superluminescence from the sample [1]. Recombination should result in the appearance of a carrier flow in the energy space (partially due to emitting by electrons optical phonons having the energy $\hbar\Omega_0$) towards the level at which the carrier recombination occurs. The recombination must lead to a dip on the curve of electron distribution at a certain energy E_0 near the conduction band bottom. This dip is inevitably followed by another dip when $E_1 = E_0 + \hbar\Omega_0$ since the energy transitions from E_1 to E_0 under phonon emission are more frequent than those in the opposite direction occurring with phonon absorption (in the absence of the dip at E_0 the transition rates should have been equal) and so on. This must lead to minima in the bleaching spectrum that are spaced by energy intervals $\hbar\Omega_0(1+m_e/m_h)$, where m_e and m_h are the masses of electrons and holes, respectively. In Figure 1, the arrows indicate the positions of the supposed minima spaced by 42 meV. It is seen that they all agree well with minima observed experimentally thus proving the model suggested (the brief report about this effect was published in [2]).

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A MONTE-CARLO STUDY OF DIFFUSION PHENOMENA IN III-V HETEROSTRUCTURES

A. Sleiman, J.L. Thobel, F. Dessenne, P. Bourel, R. Fauquembergue
IEMN UMR CNRS 9929 Avenue Poincaré BP 69 59652 Villeneuve d'Ascq, France

We present a study of noise phenomena in III-V heterostructures used in devices, such as HEMTs and MIS-like-FETs. We examined mainly the diffusion noise, the only one which subsists at very high frequencies.

In any case, the simulation of devices seems to be a necessary step before any large scale production. Moreover, reliable physical simulation of devices requires a good knowledge of the transport properties in materials and heterostructures.

To this aim, we have developed a Monte-Carlo model of electron transport in heterostructures. Special features of the model are the following: The wave functions and eigenenergies are calculated by self-consistent resolution of Poisson and Schrödinger equations. The nonparabolicity effect, quantization of satellite valleys and Pauli exclusion principle[1] are included. All major scattering mechanisms are accounted for.

This method provides the electron velocity and the diffusion coefficient as a function of the applied electric field.

To determine the noise diffusion coefficient we used two methods, by analysing either the carriers velocity fluctuations or the spreading of a narrow pulse of carriers[2]. We have checked that the results obtained by the two methods are in a good agreement.

We have investigated the influence of temperature on diffusion coefficient. Results for $\text{Al}_x \text{Ga}_{1-x} \text{As}/\text{In}_{0.15} \text{Ga}_{0.85} \text{As}$ heterostructure with carrier density $n_s = 8 \cdot 10^{15} \text{ m}^{-2}$, $x=0.15$ at 300 K are shown in Fig 1-3. We have compared our results for heterostructures and bulk material InGaAs. The first difference we have noticed is that the values of the diffusion coefficients are lower for heterostructures. The field dependences of parallel diffusion coefficient are also different; in 2D system it decreases monotonously whereas in bulk material InGaAs it exhibits a peak.

At 77 K results for the same heterostructure with $n_s = 8 \cdot 10^{15} \text{ m}^{-2}$ are presented in Fig 4. We can observe that the longitudinal coefficient D_z exhibits strong variations with the electric field. For fields below 1 kV/cm, D_z increases sharply, that may be explained by the reduction of the magnitude of impurity scattering which dominates at low field. Above 1 kV/cm owing the heating of electron gas, the optic polar phonon emission can take place[3][4]. This results in a strong reduction of D_z . At still higher field, the transport is dominated by intervalley scattering and D_z decreases, as it does in bulk material.

At 300 K we have studied the $\text{Al}_{0.48} \text{In}_{0.52} \text{As}/\text{In}_{0.53} \text{Ga}_{0.47} \text{As}$ heterostructure (Fig 5). We have noticed that the values of diffusion coefficients, shown in Fig 6, are higher than the values for $\text{Al}_{0.15} \text{Ga}_{0.85} \text{As}/\text{In}_{0.15} \text{Ga}_{0.85} \text{As}$ heterostructure.

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Results of Monte-Carlo simulation
for an $\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}/\text{In}_{0.15}\text{Ga}_{0.85}\text{As}/\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$ structure

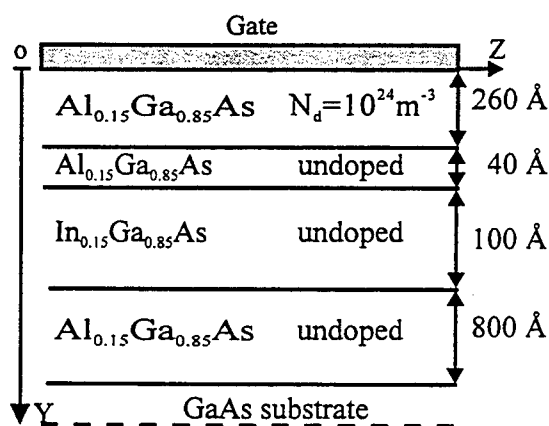


Fig. 1. The simulated structure

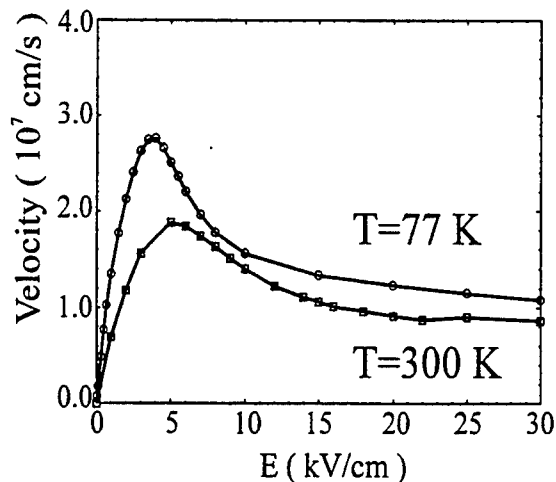


Fig. 2. The velocity as function of the electric field.

Structure of figure 1;
 $x=0.15$, $n_s=8.10^{15} \text{ m}^{-2}$, at 77 K
 and 300 K.

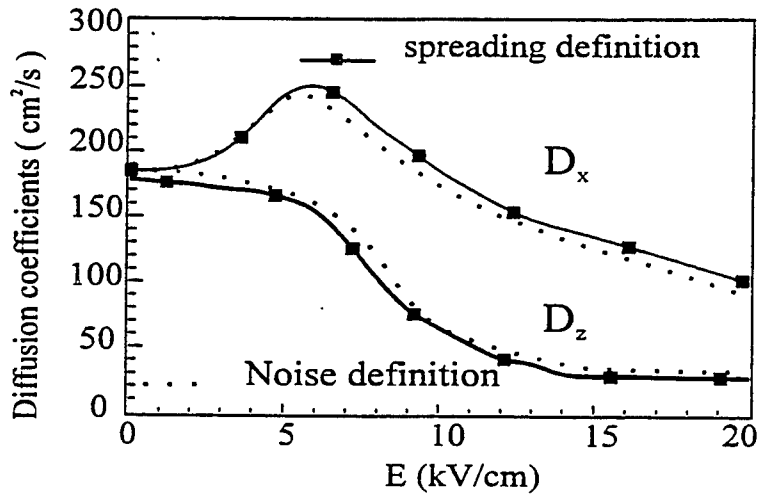


Fig. 3. Longitudinal (D_z) and transverse (D_x) diffusion coefficients as function of the electric field. Spreading and noise definitions are in good agreement.

Structure of figure 1 at 300 K, $x=0.15$, $n_s=8.10^{15} \text{ m}^{-2}$.

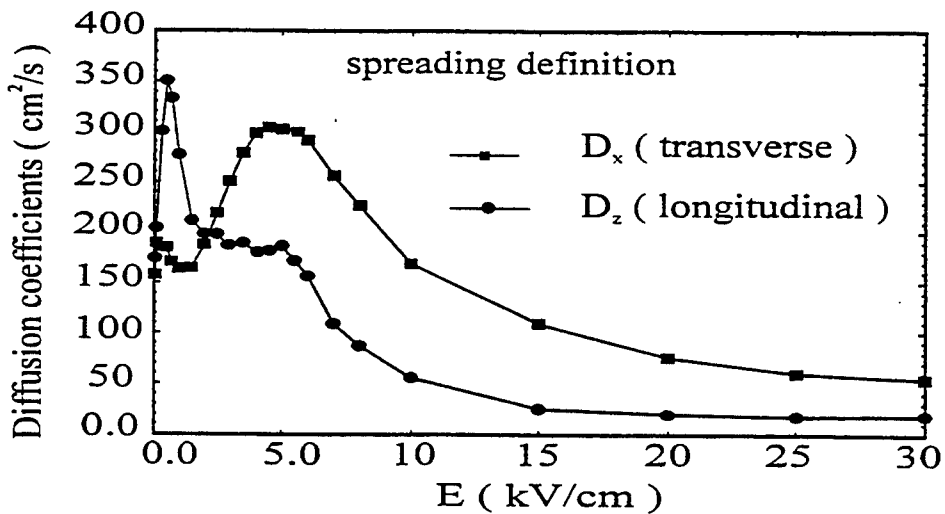


Fig. 4 Diffusion coefficients along the field. longitudinal (D_z) and transverse (D_x) as function of the electric field.

Structure of figure 1 at 77 K, $x=0.15$, $n_s=8.10^{15} \text{ m}^{-2}$.

Results of Monte-Carlo simulation
for an $\text{Al}_{0.48}\text{In}_{0.52}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{Al}_{0.48}\text{In}_{0.52}\text{As}$ structure

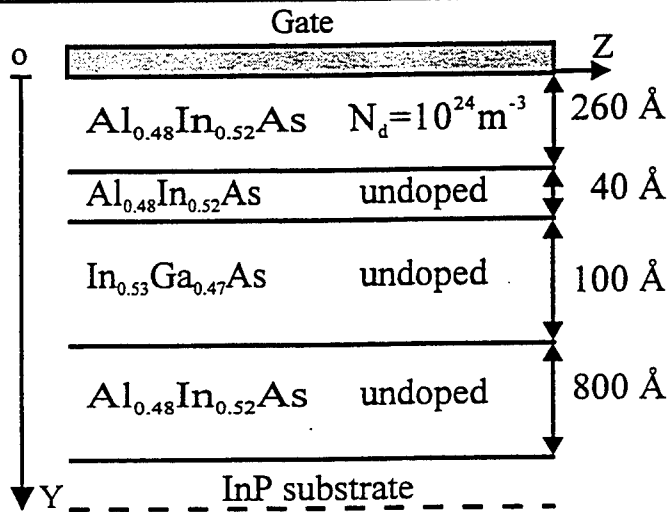


Fig. 5. The simulated structure

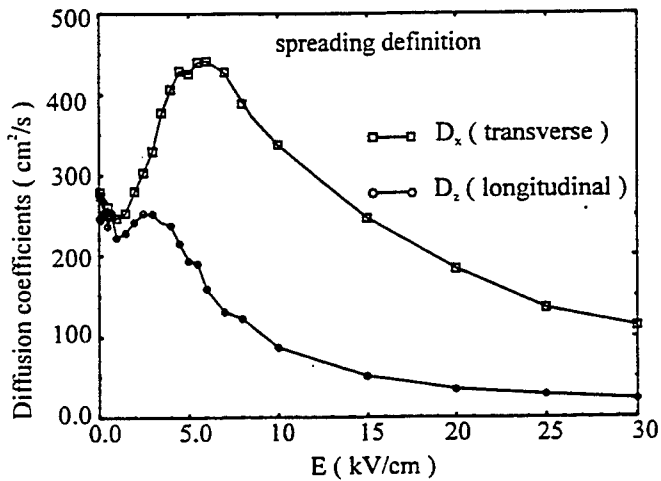


Fig. 6 Diffusion coefficients along the field. Longitudinal (D_z) and transverse (D_x) as as function of the electric field. Structure of figure 5 at 300 K, $n_s = 8 \cdot 10^{15} \text{ m}^{-2}$

Simple Hydrodynamic Transport Model

J. O. Bark and G. Gildenblat

The Department of Electrical Engineering
and
Electronic Materials and Processing Research Laboratory
Pennsylvania State University, University Park, PA 16802, USA.

Introduction

Hydrodynamic model (HDM) of carrier transport is a valuable tool in the analysis of submicron semiconductor devices [1,2]. One of the main problems with this approach is the choice of various relaxation times entering the equations of HDM. A simplest and earliest approach is to rely on the results obtained for the uniform material [3,4]. This, however, limits the accuracy of the model in the regions of rapidly varying electric field. In particular, it has been noted that reliance on the uniform field approximation for collision integral in Boltzmann transport equation (BTE) produces spurious velocity overshoot in $n^+n^-n^+$ diodes [5-7].

There are several ways to alleviate this problem. One can use post-factum correction by adjusting the value of the thermal conductivity κ in the Wiedemann-Franz law used to close the equations of HDM [8]. Alternatively, one can use more accurate expressions for the collision integral which explicitly (through gradient terms) account for the essential nonuniformity of the field pattern [6]. This approach relies on the Monte Carlo simulations in order to extract several parameters of the model. Finally, one can discard HDM in favor of the advanced version of the energy transport model [5].

In this paper we propose a modification of the HDM which is sufficient to suppress the spurious velocity overshoot without significant increase in the complexity of the model. The changes concern the relaxation times and truncation method. The main purpose is to develop a relatively simple version of HDM which alleviates some of the problems associated with the conventional version without relying on the Monte Carlo calculation for the extraction of transport parameters.

Transport Model

The transport model developed in this work is based on equations

$$\text{div}(\vec{J}_n) = 0, \quad (1)$$

$$\vec{J}_n - \frac{\tau_m}{q}(\vec{J}_n \cdot \text{grad}) \frac{\vec{J}_n}{n} = \frac{q^2 \tau_m}{m^*} \left[\frac{k_B T_e}{q} \text{grad}(n) + n \text{grad} \left(\frac{k_B T_e}{q} - \phi \right) \right], \quad (2)$$

$$\text{div}(\vec{J}_w) = \vec{E} \cdot \vec{J}_n - \frac{nw - n_0 w_0}{\tau_w}, \quad (3)$$

and

$$\vec{J}_w = -\tau_{j_w} \text{div}(\hat{X}) - \frac{\tau_{j_w}}{m^*} n w \vec{E} - 2 \frac{q \tau_{j_w}}{m^*} n \hat{w} \cdot \vec{E}. \quad (4)$$

where \vec{J}_n is the current density, n denotes the electron concentration, n_0 is the equilibrium value of n , T_e -the electron temperature, τ_m -the ensemble momentum relaxation time, τ_w -the ensemble energy relaxation time, τ_{j_w} -the ensemble kinetic energy flux relaxation time, m^* -the conductivity effective mass, k_B -the Boltzmann constant, \vec{E} -the electric field, ϕ -the electrostatic potential, \vec{J}_w -the kinetic energy flux, w -the average kinetic energy per electron, w_0 -the equilibrium value of w , \hat{w} -the average kinetic energy tensor, and $\hat{X} = n\langle\epsilon\vec{v}\vec{v}\rangle$. Here the angular bracket denotes average over the distribution function, i.e., $\langle\phi\rangle = \int d\tau_p \phi f / \int d\tau_p f$.

In a conventional HDM [1], eq. (4) is not used and the system of equations (1)-(3) is closed using the phenomenological Fourier law $\vec{Q} = -\kappa \text{grad}(T_e)$ which is then substituted into the equation

$$\vec{J}_w = nw\vec{v}_d + nk_B T_e \vec{v}_d + \vec{Q}, \quad (5)$$

where \vec{v}_d is the drift velocity. The thermal conductivity κ is related to the electrical conductivity $\sigma_n = nq^2\tau_m/m^*$ by the Wiedemann-Franz law $\kappa = (5/2 + c)(k_B/q)^2\sigma_n T_e$, where coefficient c is characteristic of the scattering mechanism.

As an alternative we rely on the fourth moment balance equation (4). This equation is derived from the exact fourth moment balance equation. The system of four balance equations is truncated (i.e. closed) by simplifying eq. (4) via the ansatz of

$$f(\vec{r}, \vec{p}) = f_0(\vec{r}, \vec{p}) + \vec{E} \cdot \vec{p} f_1(\vec{r}, \vec{p}), \quad (6)$$

of Ref. [9], where f_0 is the spherically symmetric part of the distribution function taken in the form of a heated Maxwellian and f_1 is an even function of momentum. However, unlike [9] we use this ansatz only in order to simplify the expression for \vec{J}_w and not in the balance equations for the first three moments of the distribution function. This yields

$$\vec{J}_w = -\frac{20}{9} \frac{\tau_{j_w}}{m^*} n w \text{div}(w) - \frac{10}{9} \frac{\tau_{j_w}}{m^*} w^2 \text{div}(n) - \frac{5}{3} \frac{q\tau_{j_w}}{m^*} n w \vec{E}. \quad (7)$$

The ensemble momentum relaxation time is obtained from experimental data for high-field mobility $\mu_n(E)$ in bulk silicon as

$$\tau_m = \frac{m^*}{q} \mu_n(E). \quad (8)$$

Following [4], the ensemble energy relaxation time τ_w is found by applying eq. (3) to the uniform case. The ensemble kinetic energy flux relaxation time τ_{j_w} is found by applying eq. (7) to the uniform case. This yields

$$\tau_{j_w} = \frac{3}{5} \left(1 + \frac{k_B T_e}{w}\right) \tau_m. \quad (9)$$

Numerical calculations show that according to (9) $\tau_{j_w} \approx \tau_m$, which agrees with the results of the more sophisticated calculations in Ref. [5].

Simulation Results

To facilitate the comparison with the conventional hydrodynamic model, the silicon $n^+n^-n^+$ device simulated in this work is chosen to be the same as that used in [1]. The doping levels are $n^+ = 5 \times 10^{17} \text{cm}^{-3}$ and $n^- = 2 \times 10^{15} \text{cm}^{-3}$. Two n^+ outer regions are $0.1 \mu\text{m}$ long, the length of the inner region is $0.4 \mu\text{m}$. The applied voltage is 1.5V , and the lattice temperature $T_L = 300\text{K}$. The saturation velocity v_s , which is needed in order to compute mobility, is $1.1 \times 10^7 \text{cm/s}$.

The results of computations performed using two types of HDM are shown in Figs. 1 and 2 (two computations from the conventional HDM with different momentum relaxation times). Fig. 1 shows the normalized drift velocity, and the normalized electron temperature is shown in Fig. 2. To be specific we set $c = -1/2$ in the Wiedemann-Franz law used in the conventional HDM. The energy relaxation time for the conventional HDM is computed as suggested in [4]. If one relies on the traditional form of the energy balance equation, then the spurious velocity overshoot (solid line in Fig. 1) is present as has been already pointed out in the literatures [5-7]. In a new approach this undesirable feature of the HDM is suppressed without increasing the complexity of the model. Another consequence of the proposed HDM modification is to bring the temperature profile (i.e. average kinetic energy per electron) closer to that obtained by Monte Carlo simulation for similar scattering mechanisms [10].

In conclusion, we presented a new HDM which is both simpler and more accurate than the traditional model.

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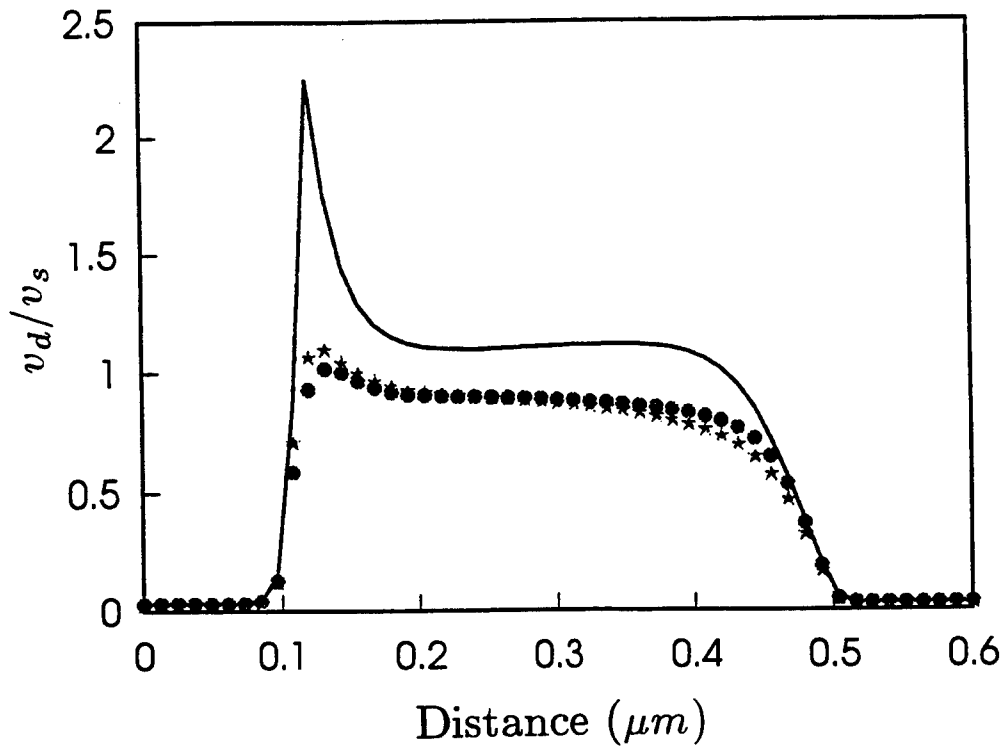


Fig. 1 The normalized drift velocity (— conventional HDM with $\mu_n = \mu_{n0}T_L/T_e$, * conventional HDM with $\mu_n = \mu_n(E)$, • new HDM with the same $\mu_n(E)$).

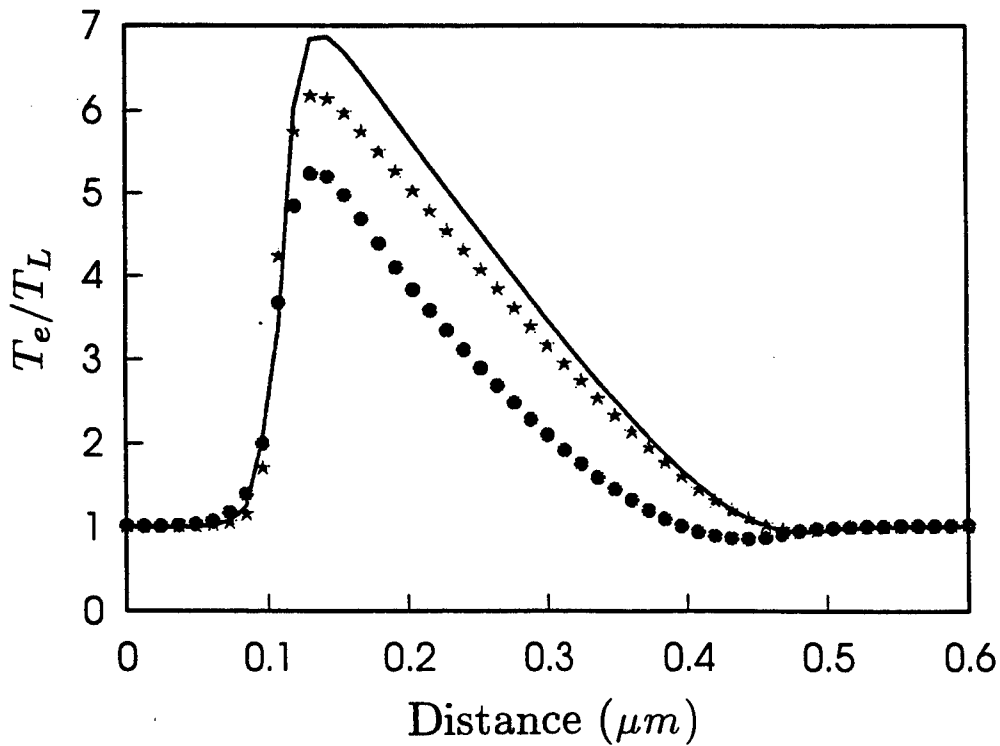


Fig. 2 The normalized electron temperature (— conventional HDM with $\mu_n = \mu_{n0}T_L/T_e$, * conventional HDM with $\mu_n = \mu_n(E)$, • new HDM with the same $\mu_n(E)$).

A Large Signal HBT Model for Two-Tone Intermodulation Analysis

Bin Li, TaoLing Fu and Sheila Prasad
ECE Dept., Northeastern University, Boston, MA 02115

Heterojunction bipolar transistors (HBT's) are presently being used in many analog and digital applications [1]. Although small-signal models of HBT's have been studied extensively [2, 3], the same is not true for large signal models. The Volterra series method has been used for modeling the nonlinear operation of the HBT at the medium drive level. An Ebers-Moll large-signal HBT model [4] which includes many high order effects has been reported, however, it is rather complex and needs complicated semiconductor physics analysis and a knowledge of the device fabrication.

This paper presents a simple Ebers-Moll model [5] based on the quasi-static technique which makes use of multi-bias scattering parameters and DC measurements to extract a bias-dependent nonlinear equivalent circuit model. The device under investigation is a $5 \times 10 \mu m^2$ InGaAs/InAlAs/InP inverted HBT with $f_T = 23$ GHz and $f_{max} = 20$ GHz. The small signal equivalent circuit of the device is shown in Figure 1. $L_b, L_c, L_e, C_{be}, C_{bc}$ and C_{ce} are parasitic inductances and capacitances respectively, R_b, R_c and R_e are extrinsic resistances. The active portion of the HBT was modeled by intrinsic elements C_e, r_e, C_{jc}, α and R_{jc} . All elements except five intrinsic elements C_e, r_e, C_{jc}, R_{jc} and α are considered to be invariant with bias [6]. The elements $C_{be}, C_{bc}, C_{ce}, L_b, L_c, L_e$ are extracted at zero bias by numerical optimization. The intrinsic elements at non-zero bias are extracted by the following approaches:

- Convert the s-parameters to z-parameters and subtract the parasitic series elements L_b and L_c .
- Convert the z-parameters to y parameters and subtract the parasitic shunt elements C_{be}, C_{ce}, C_{bc} .
- Convert the y-parameters to h-parameters.

The elements of the equivalent circuit excluding the parasitic effects, are easily extracted using the procedure described in [3].

In the large signal model, C_e, r_e are represented by BE junction diode and C_{jc}, R_{jc} are represented by BC junction diode. The following equations are used to characterize intrinsic elements

$$R_e = \frac{n_{be}KT}{qI_e} \quad (1)$$

$$C_e = C_{je} + \tau_e/R_e \quad (2)$$

$$C_{jc} = C_{jc0} (1 - V'_{bc}/V_{jc0})^{-M_{jc}} \quad (3)$$

$$C_{je} = C_{je0} (1 - V'_{be}/V_{je0})^{-M_{je}} \quad (4)$$

$$R_{jc} = \frac{n_{bc}KT}{qI_{sR}} \exp\left(-\frac{qV'_{bc}}{KT}\right) \quad (5)$$

$$I_e = I_{sF}(e^{qV'_{be}/KT} - 1) \quad (6)$$

where V'_{be}, V'_{bc} are intrinsic base-emitter and base-collector voltages respectively, $I_{sF}, n_{be}, C_{je0}, M_{je0}, V_{je0}, \tau_e$ are BE junction model parameters, $I_{sR}, n_{bc}, C_{jc0}, V_{jc0}, M_{jc0}$ are BC junction model parameters. In the small signal device model, the plot of $R_e + r_e$ versus $1/I_e$ is used to extract n_{be} . The model parameters are extracted from these equations by fitting them to bias-dependent intrinsic elements since a medium power drive level was applied to the device. M_{je} is assumed to be 0.5 for the abrupt emitter-base junction. M_{jc} is assumed to be 0.33 for the graded base-collector junction. The variation of α (α_0, f_α, τ) with bias is not included in the presented model.

Given extrinsic values of voltages and currents, the intrinsic base-collector voltage, base-emitter voltage and emitter current are given as follows:

$$I_e = I_c + I_b \quad (7)$$

$$V'_{be} = V_{be} - I_e R_e - I_b R_b \quad (8)$$

$$V'_{bc} = V_{bc} - I_b R_b + I_c R_c \quad (9)$$

These equations are fitted to the bias variation of the intrinsic element values and the corresponding constants are determined.

The two-tone third order distortion simulation is performed to verify the resulting HBT model. The simulation was made by harmonic balance simulator in LIBRA [7]. Figure 2 shows the measured and simulated distortion at the bias of $V_{ce} = 1.5 \text{ V}, I_b = 170 \mu\text{A}$. The two fundamental signal frequencies are 6.02 and 6.08 GHz respectively. The third order intermodulation distortions are averaged at 5.96 and 6.14 GHz. The source and load impedance are assumed to be 50Ω . The difference between simulation and measurement are well within 1.5 dBm.

The simple Ebers-Moll model is based on the experimental characterization of the frequency and bias-dependent behavior of the device small-signal s parameters. The model parameters are deduced by fitting the bias-dependent intrinsic elements to the underlying equations from physics. The model was validated by simulation.

ACKNOWLEDGMENT

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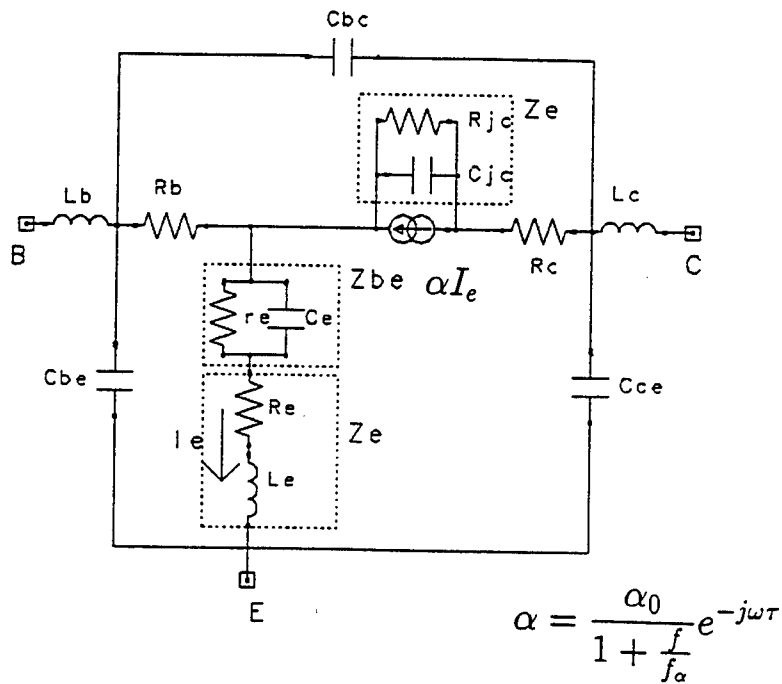


Figure 1: Small signal equivalent circuit of the inverted HBT

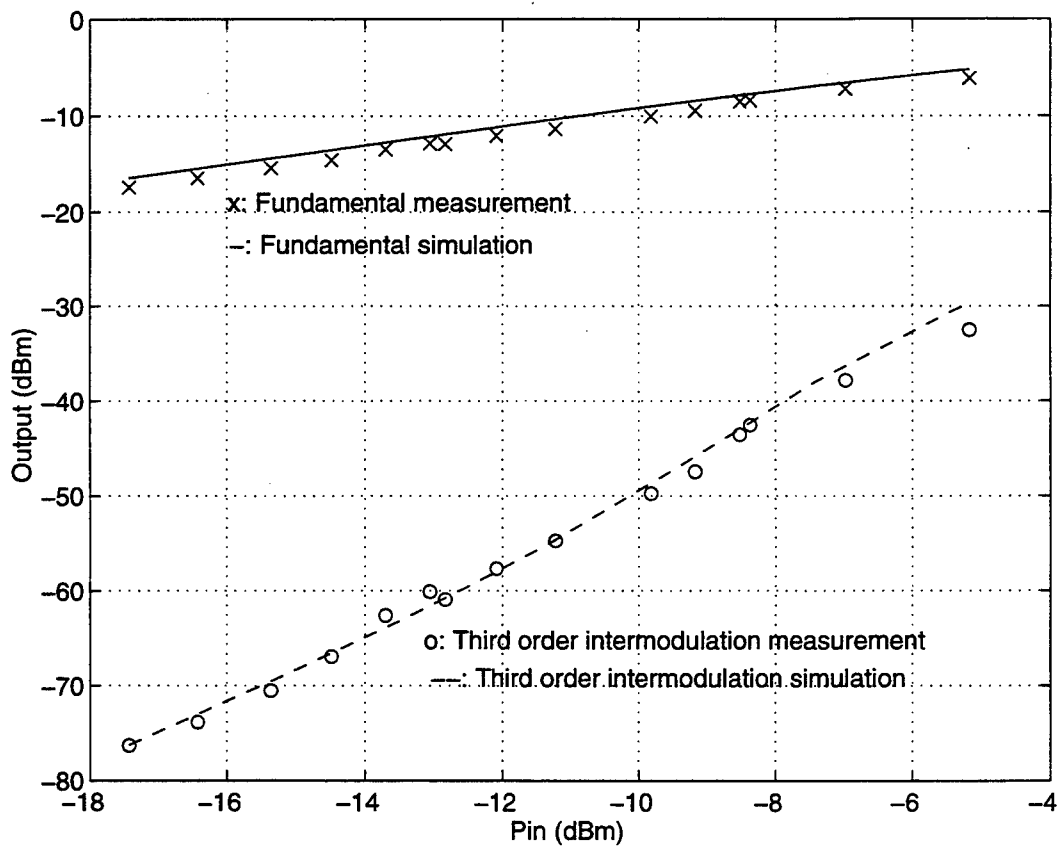


Figure 2: Two tone third order intermodulation distortion of the inverted HBT at $V_{ce} = 1.5 V, I_b = 170 \mu A$

AIRY'S FUNCTION IMPLEMENTATION OF THE TRANSFER MATRIX METHOD FOR RESONANT TUNNELING

S. Vatannia, G. Gildenblat

Department of Electrical Engineering, The Pennsylvania State University, University Park, PA 16802

and

B. Gelmont

Department of Electrical Engineering, University of Virginia, Charlottesville, VA 22903

Introduction Within the effective mass approximation, the exact solution of the Schrödinger's equation via Airy's functions is the most accurate method of computing the tunneling transmission coefficient in electrically biased superlattices. For multiple-barrier structures this approach is implemented using the transfer matrix method in the form developed for piece-wise linear potentials [1]. It is then natural to use the calculations of this type to evaluate the accuracy of various approximate methods such as piece-wise constant potential approximation [2], or the argument-principle based method [3]. However, there are several problems associated with the implementation of this approach. First, the asymptotic behavior of Airy's functions often results in numerical overflow which significantly reduces the computational efficiency of the method at low applied biases [4,5]. Thus, the low-voltage region is usually not included in the Airy's functions based computations, and some of the resonant peaks of the I-V characteristics are lost. In this work we show that, with proper ordering, the computations of the transmission coefficient and tunneling current in the low-bias region present no difficulty. Second, it was pointed out that the energies of certain quasi-bound states (QBS) cannot be evaluated by investigation of the tunneling transmission coefficient of multibarrier structures whose complex energy $E_Q = E_r - i\Gamma/2$ has the real part E_r in the energy range where tunneling is impossible [3]. We show that the energies of all QBS with sufficiently large lifetimes can be obtained by considering the resonant behavior of the transfer matrix in the extended energy range. Finally, some of the previous investigation have shown the discrepancy between the Airy's function method and other approaches for the QBS [1] and the I-V characteristics [5]. We show that the accurate implementation of the transfer matrix method eliminates this problem.

Transfer matrix The potential energy profile of the general multibarrier structure studied in this work is shown in Fig. 1. The height of the j -th barrier corresponding to $x_{2j-1} < x < x_{2j}$ is denoted as U_j . The solutions of the Schrödinger's equation within the contact and the j -th regions are

$$\Psi_0 = A_0 \exp(ik_0 x) + B_0 \exp(-ik_0 x); \quad x < x_1 \quad (1)$$

$$\Psi_{2n} = A_{2n} \exp(ik_{2n} x) + B_{2n} \exp(-ik_{2n} x); \quad x_{2n} < x \quad (2)$$

$$\Psi_j = A_j \text{Ai}(z_j) + B_j \text{Bi}(z_j) \quad x_j < x < x_{j+1} \quad (3)$$

where $A_0, B_0, A_{2n}, B_{2n}, A_j,$ and B_j are constant coefficients, Ai and Bi represent Airy's functions,

$$k_0 = (2m_0 E / \hbar^2)^{1/2}, \quad k_{2n} = [2m_{2n} (E + eV_a) / \hbar^2]^{1/2} \text{ and}$$

$$z_j(x) = (2m_j)^{1/3} (e\hbar F_j)^{-2/3} [\Gamma_j - eF_j(x - x_j)];$$

m_0, m_{2n} and m_j are the effective masses within corresponding region, the energy E is counted from the bottom of the conduction band of the left contact (i.e. $V = 0$ for $x < x_1$ in Fig. 1), V_a applied voltage, F_j is the electric field within j -th region and Γ_j is defined in Fig. 1. We next define the interface transfer matrices W_j for $j = 1, 2, \dots, 2n$:

$$\begin{bmatrix} A_j \\ B_j \end{bmatrix} = W_j \begin{bmatrix} A_{j+1} \\ B_{j+1} \end{bmatrix}. \quad (4)$$

The matrix elements of W_j are readily found from the continuity conditions for the wave function and its derivative (the latter weighted by the inverse of effective masses [6]). Application of these conditions to the contact interfaces yield

$$W_1(11) = (1/2)[\text{Ai}(\beta_1) + i\xi \text{Ai}'(\beta_1)] \exp(-ik_0 x_1), \quad (5)$$

$$W_1(12) = (1/2)[\text{Bi}(\beta_1) + i\xi \text{Bi}'(\beta_1)] \exp(-ik_0 x_1), \quad (6)$$

$$W_1(21) = (1/2)[\text{Ai}(\beta_1) - i\xi \text{Ai}'(\beta_1)] \exp(ik_0 x_1), \quad (7)$$

$$W_1(22) = (1/2)[\text{Bi}(\beta_1) - i\xi \text{Bi}'(\beta_1)] \exp(ik_0 x_1), \quad (8)$$

$$W_{2n}(11) = \pi[\text{Bi}'(\alpha_{2n}) + i\eta \text{Bi}(\alpha_{2n})] \exp(ik_{2n} x_{2n}), \quad (9)$$

$$W_{2n}(21) = -\pi[\text{Ai}'(\alpha_{2n}) + i\eta \text{Ai}(\alpha_{2n})] \exp(ik_{2n} x_{2n}) \quad (10)$$

$$W_{2n}(12) = [W_{2n}(11)]^*, \quad W_{2n}(22) = [W_{2n}(21)]^*. \quad (11)$$

where

$$\alpha_j \equiv z_{j-1}(x_j) = (2m_{j-1})^{1/3} (e\hbar F_{j-1})^{-2/3} (\Gamma_{j-1} - \Delta E_{j-1}) \quad (12)$$

$$\beta_j \equiv z_j(x_j) = (2m_j)^{1/3} (e\hbar F_j)^{-2/3} \Gamma_j, \quad (13)$$

$$\xi = m_0 (2eF_1)^{1/3} / k_0 (m_1^2 \hbar^2)^{1/3}, \quad (14)$$

$$\eta = k_{2n} (m_{2n-1}^2 \hbar^2)^{1/3} / m_{2n} (2eF_{2n-1})^{1/3}. \quad (15)$$

and ΔE_j denotes corresponding band bending in j -th region. Similarly, for $j = 2, 3, \dots, 2n-1$ we find

$$W_j(11) = \pi \left[Ai(\beta_j) Bi'(\alpha_j) - \gamma_j Ai'(\beta_j) Bi(\alpha_j) \right] \quad (16)$$

$$W_j(12) = \pi \left[Bi(\beta_j) Bi'(\alpha_j) - \gamma_j Bi'(\beta_j) Bi(\alpha_j) \right] \quad (17)$$

$$W_j(21) = \pi \left[-Ai(\beta_j) Ai'(\alpha_j) + \gamma_j Ai'(\beta_j) Ai(\alpha_j) \right] \quad (18)$$

$$W_j(22) = \pi \left[-Bi(\beta_j) Ai'(\alpha_j) + \gamma_j Bi'(\beta_j) Ai(\alpha_j) \right] \quad (19)$$

where $\gamma_j = (m_{j-1}^2 F_j / m_j^2 F_{j-1})^{1/3}$.

The transmission coefficient and the overall transfer matrix are given by

$$D(E) = (k_{2n} m_0 / k_0 m_{2n}) |W(11)|^{-2}; \quad W = \prod_{j=1}^{2n} W_j$$

Equations (8) - (19) represent the Airy's function implementation of the transfer matrix method. The only remaining problem is numerical evaluation of the transmission coefficient for the low applied voltages. For $V_a \rightarrow 0$ numerical overflow results if expressions (8) - (19) are used. In order to deal with the overflow problem, we introduce a large dimensionless parameter ζ_0 ($\zeta_0 = 25$ in our computations) and use the following procedure. If the arguments of Airy's functions used to compute the transfer matrices do not exceed ζ_0 we use equations (8) - (19) directly. Otherwise we use asymptotic expressions for Airy's functions, to evaluate the transfer matrix $\tilde{W}_i = W_{2i-1} W_{2i}$ for the i -th barrier:

$$\tilde{W}_i(jk) = R_{jk}^i \exp(-\theta_i) + S_{jk}^i \exp(\theta_i), \quad \text{where } i = 1, 2, \dots, n, \\ j, k = 1, 2, \text{ and } \theta_i \equiv (2/3)(\beta_{2i-1}^{3/2} - \alpha_{2i}^{3/2}) \quad \text{or} \\ \theta_i = (2/3)(2m_{2i-1})^{1/2} (e\hbar F_{2i-1})^{-1} \left[\Gamma_{2i-1}^{3/2} - (\Gamma_{2i-1} - \Delta E_{2i-1})^{3/2} \right]$$

In the asymptotic expressions for matrix elements of \tilde{W}_i , the argument of the exponent is no longer α_{2i} or β_{2i-1} (which tend to $+\infty$ for $V_a \rightarrow 0$), but their difference. Consequently, when $F_{2i-1} \rightarrow 0$, and $\Delta E_{2i-1} \rightarrow 0$ we have $\theta_i = O(1)$, and the overflow problem does not arise while computing \tilde{W}_i .

Resonant behavior and symmetry of the transfer matrix

There are several techniques for extracting the energies of the quasi-bound states. The simplest one is to consider the peaks of the transmission coefficient as a function of energy [1,2]. Strictly speaking, $D(E)$ is defined only for $E > 0$; otherwise, there is no plane-wave solution of the Schrödinger's equation in the left contact region. Consequently, other techniques have been developed to evaluate the energies of QBS with $E_r < 0$ [3,4].

For QBS with complex energy $E_r - i\Gamma/2$ we note that the asymptotic expression for the wave function contains no incoming waves, i.e., $A_0(E_r - i\Gamma/2) = B_{2n}(E_r - i\Gamma/2) = 0$ and consequently $W_{11}(E_r - i\Gamma/2) = 0$. For sufficiently small Γ

$$W_{11}(E) = \gamma(E - E_r + i\Gamma/2) + O(E - E_0)^2 \quad (20)$$

where $\gamma = (dW_{11}/dE)_{E=E_0}$.

Equation (20) is valid regardless of the energy range. When $E > V_{x1}$ the QBS - induced root of W_{11} at $E = E_0$

results in a Lorentzian resonance of the transmission coefficient $D \propto |W_{11}(E)|^{-2}$ and the time reversal symmetry implies [11]

$$W_{11} = W_{22}^*, \quad W_{12} = W_{21}^*; \quad E > V_{x1} \quad (21)$$

In the energy range $V_{x2n} < E < V_{x1}$ where there is no tunneling, k_0 is purely imaginary. In such case Eq. (20) still follows from the absence of the incoming wave for $x > x_{2n}$ and of the exponentially growing term for $x < x_1$ in the asymptotics of the QBS wave function. The resonance behavior of $|W_{11}|^{-2}$ remains in place, but instead of (21) we have [7]

$$W_{11} = W_{12}^*, \quad W_{22} = W_{21}^*; \quad V < E < V_1 \quad (22)$$

For this energy range a physically meaningful problem is the reflection of a plane wave propagating from the right in the negative direction. The reflection amplitude θ near the resonance is given by [7,12],

$$\theta(E) = \text{const} - 2 \arctan[\Gamma / 2(E - E_r)] \quad (23)$$

The negative energy resonances can be studied analytically using WKB approximation which confirms the resonant behavior of $|W_{11}|^{-2}$ in the energy range where the tunneling is impossible [7].

Numerical results We first consider a single well with effective masses are taken as $m_w^* = 0.067m_0$ inside the well and $m_b^* = 0.1087m_0$ within the barrier. The energy dependence of the transmission coefficient is shown in Figs. 2 for the bias voltages $V_a = 0, 0.16$ V and $V_a = 0.4$ V. The negative-energy resonance peak corresponding to a QBS with $E_r = -119$ meV which exists for $V_a = 0.4$ V is clearly seen in this figure. The formation of both positive-energy and negative-energy resonances is further investigated by considering the double-well structure. At zero bias only resonant states with $E_r > 0$ are present. As the bias is increased to 0.16 V the negative-energy resonance with $E_r = -22$ meV becomes apparent. For $V_a = 0.4$ V there are two negative-energy QBS with $E_r = -198$ meV and $E_r = -24$ meV (Fig. 3), respectively.

Next we consider the variably spaced finite superlattice in Fig. 4. The related calculations are summarized in Tables I and II and compared with published results. Since in the literature the negative-energy resonances were not studied using $|D(E)|$ dependence, we used the computations of Refs. [3,4], employing a different technique (developed within a step approximation for the transfer matrix) as a comparison for $E_r < 0$. With the exception of Ref. [1] in all cases an excellent agreement was reached with previous investigations. This verifies various approximations by comparison with the exact solution obtained here. Furthermore, this comparison supports the validity of computing E_r using the resonance property of $|W_{11}|^{-2}$ in the energy region $E_r < 0$ where the tunneling does not occur. Apart from the resonance peaks the numerical computation indicate singular behavior of $|W_{11}|^{-2}$ near $E = V_{x1}$.

which is in agreement with the threshold singularity of $|W_{11}|^{-2} \propto (E - V_{x1})^{1/2}$ established in [7].

Finally, we calculate the I-V characteristics of a double barrier structure; $m_w = 0.041m_0$ inside the well, $m_b = 0.078m_0$ within the barrier, barrier and well thicknesses are 5 and 9 nm respectively, and barrier height is 0.5 eV, Fermi level in left contact is 0.04eV and $T = 4K$. In contrast to [5] we find that a step approximation is in a good agreement with the results of the exact solution. However, we find that the calculation of I-V characteristics of multilayer structures with more than three barriers using step approximation method is much slower than Airy's function technique.

Conclusions: We have developed a version of the transfer matrix method based on the exact solution of the Schrödinger's equation with a piece-wise linear potential in terms of Airy's functions. Particular care is taken in order to eliminate the numerical problems which arise in the computation of the transmission coefficient and I-V characteristics of the multibarrier tunneling structure at low applied voltages. The results presented in this work eliminate the discrepancies between the exact solution and various approximate computations of transmission coefficients, energies of the QBS, and I-V characteristics in finite superlattices. The QBS with negative energies do not affect the transmission coefficient but are related to resonances of the $|W_{11}|^{-2}$ or those of the reflection amplitude.

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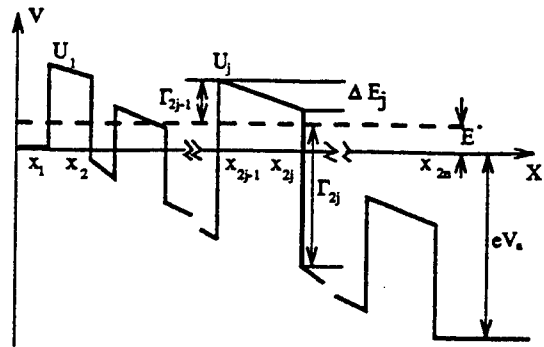


Fig. 1. Potential energy profile.

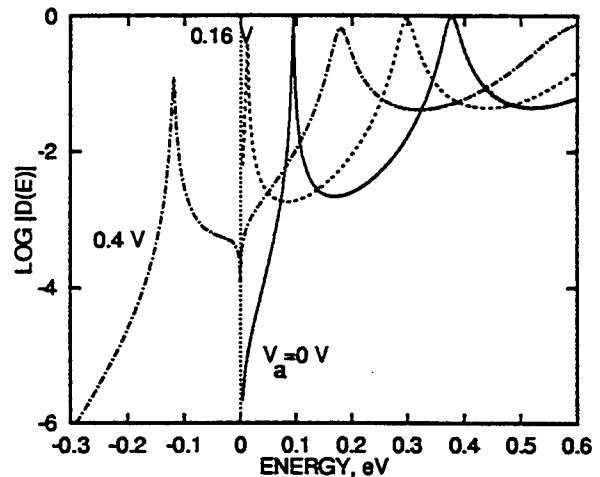


Fig. 2. Energy dependence of transmission coefficient of double-barrier structure for $V_a = 0$ volt (solid line), 0.16 volt (dash), and 0.4 V (dash-dot). Barrier height is 0.5 eV, barrier and well thicknesses are 2nm, and 5nm respectively. Note that $|D(E)|$ for $E < 0$ should not be interpreted as a transmission coefficient.

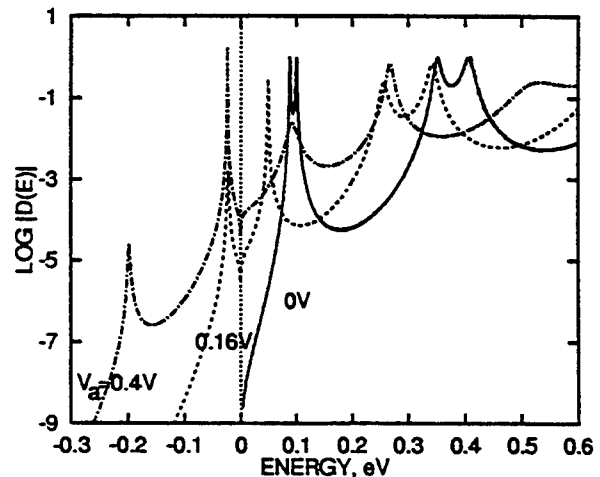


Fig. 3. Same as Fig. 2 for a triple barrier

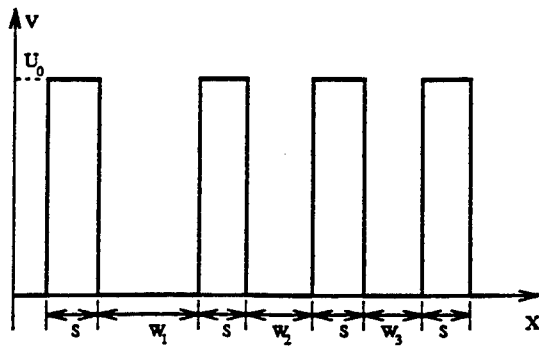


Fig. 4. Potential energy profile of an unbiased variably spaced superlattice. $s = 3.5$ or 5 nm, $w_1 = 11$ nm, $w_2 = 2.82$ nm, $w_3 = 2.2$ nm, $U_0 = 0.477$ eV, $m_b = 0.1043 m_0$, and $m_w = 0.067 m_0$.

Table I
The energy of QBS
Double barrier

Bias (V)	Energy level ⁽¹⁾	[3] (meV)	[2] (meV)	[1] (meV)	this work (meV)
0	E_1	93.9	94	*	93.8
	E_2	379.8	380	*	378
0.16	E_1	11.6	12	40	12
	E_2	297.2	300	350	298
0.4	E_1	-118.8	*	*	-119
	E_2	178.9	180	230	180

Triple barrier

Bias (V)	Energy level ⁽¹⁾	[3] (meV)	[2] (meV)	[1] (meV)	this work (meV)
0	E_1	87.9	89	*	88
	E_2	100.4	100	*	100
	E_3	351.4	353	*	352
	E_4	407.2	404	*	406
0.16	E_1	-21.9	*	*	-22
	E_2	48.8	46	80	48.5
	E_3	255.6	257	317	256
	E_4	343.1	342	*	343
0.4	E_1	-197.5	*	*	-197.5
	E_2	-23.4	*	*	-23.5
	E_3	91.1	90	120	91.5
	E_4	267.6	260	320	267.5

* - not computed.

(1) - We use notations of Refs. [3], and [4] in Tables I and II respectively, but redefine the reference energy level as shown in Fig. 1. The numerical values of energies given in [3] and [4] are adjusted accordingly.

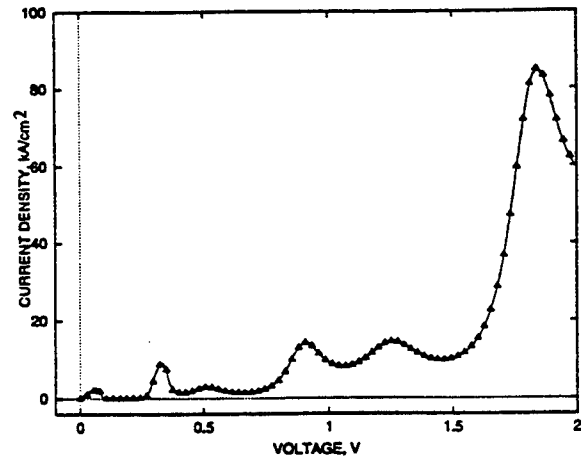


Fig. 5. I-V characteristic of a double barrier structure. The exact result and step approximation are represented by solid line and triangles respectively.

Table II

The energies of QBS in Variably Spaced Superlattice (cf. Fig. 4)

Field kV/cm	E level ⁽¹⁾	[4] (meV)		[1] (meV)		This work (meV)	
		$s=3.5$ nm	$s=5$ nm	$s=3.5$ nm	$s=5$ nm	$s=3.5$ nm	$s=5$ nm
0	E_1	29.7	29.8	*	*	29.7	29.7
	E_2	119	119.1	*	*	119	119.1
	E_3^a	266.3	266	*	*	266	266.3
	E_4^a	180.9	181.4	*	*	181	181.4
	E_5^a	229.2	228.2	*	*	229.4	228.3
20	E_1	12	9	*	*	11.6	8.5
	E_2	101.6	98.7	*	*	101	98.2
	E_3^a	248.8	245.5	*	*	248.3	245
	E_4^a	142.4	137	*	*	142	136.5
	E_5^a	179.1	168.9	*	*	178.8	168.4
555	E_1	-21	-29.2	*	*	-22.3	-30.6
	E_2	74.3	62.8	*	76.3	73.1	61.4
	E_3^a	216.5	209.2	*	214.3	216.4	207.8
	E_4^a	69.5	57.8	*	70.3	68.2	56.4
	E_5^a	90.9	63.9	*	81.3	89.8	62.6
666	E_1	-31.7	-41.7	*	*	-33.3	-43.3
	E_2	61.1	51.4	69.6	*	59.8	50
	E_3^a	208	197.7	215.6	*	206.6	196.3
	E_4^a	49.6	29.5	56.6	*	48.4	28
	E_5^a	64.6	34.2	86.6	*	63.4	32.8
100	E_1	-64.3	-79.3	*	*	-66.8	-81.8
	E_2	33.5	18.2	*	*	31	15.8
	E_3^a	179.3	163.9	*	*	176.8	161.5
	E_4^a	-7.9	-40.4	*	*	-10.2	-42.7
	E_5^a	-26.1	-69	*	*	-28.2	-71.2

SIMULATION OF THE GaAs MESFET ELECTRICAL BURNOUT

V.A.VASHCHENKO, J. B. Martynov, V. F. SINKEVITCH, A. S. Tager
Russia

INTRODUCTION Electrical source-drain breakdown limits operating drain voltage, output power of GaAs MESFETs and HEMTs, therefore its understanding is important for problems of FETs design, optimization and reliability [1,2]. Electrical current instability which results in negative differential conductance (NDC) and reversible switching in the current filament state of GaAs MESFETs was observed under 20 ns drain voltage pulse duration for all operation gate biases [3]. In the filament state increase of the drain current or pulse duration resulted in instantaneous local burnout of MESFETs in the filament area [3]. It was supposed, that electrical burnout of GaAs MESFETs is the consequence of: (i) uncontrollable drain current increase due to modulation of the semiinsulating buffer by injected holes from the drain avalanche area and electrons from source n^+ -contact; (ii) NDC and current filament formations and following local melting [3,4]. The purpose of this study is to demonstrate with the help of 2D simulation, that: (i) GaAs MESFET's really have NDC area of drain-source I_D - V_{DS} characteristics due to buffer conductivity modulation; (ii) the breakdown of GaAs n^+ -i- n^+ structures having parameters typical for contact and buffer layers of power MESFETs results in NDC and filament formation.

SIMULATION METHOD AND MODELS Drain breakdown characteristics of the MESFET were simulated under steady-state conditions. For carrier motion specification the equations of the quasi hydrodynamic model were used. The equation system was solved with "mixed" boundary conditions: the constant gate bias and drain current. The breakdown characteristics of the simple MESFET (Fig.1(a)) and GaAs n^+ -i- n^+ (Fig.1(b)) structures were calculated. The 1D ($W = 0.3 \mu\text{m}$) n^+ -i- n^+ models were calculated for a number of i-area length (L_i); 2D n^+ -i- n^+ model -- for $L_i = 1.6 \mu\text{m}$, $W = 10 \mu\text{m}$, $n^+ = 10^{18}\text{cm}^{-3}$ (Fig.1(b)).

RESULTS The calculated drain I_D - V_{DS} characteristics of GaAs MESFETs (Fig.2(a)) have NDC branches for all gate biases. The electric field strength and carrier concentration depth profiles for NDC condition of the MESFET (Fig.3(a,b,c), gate bias $V_{GS} = -2 \text{ V}$) in the SI layer are changed significantly in comparison with condition typical for drain avalanche breakdown [2]. Injection level of electrons and holes in SI layer is greatly increased. The electrons, injected from the source n^+ -contact and the avalanche holes create quasi neutral domain of electron-hole plasma in SI layer near the source n^+ -contact (Fig.3(b,c)). With following increasing of the drain current this domain expand and electric field near the drain increase. The calculated I-V characteristics of 1D n^+ -i- n^+ structures for various i-area lengths (L_i) have similar peculiarities (Fig.2(b, dashed lines)). The electric field and carrier concentration distributions in the n^+ -i- n^+ structure are presented on the Fig.4. Introduction of deviations in model structural parameters allowed to conclude, that NDC formation primarily is defined by the properties of carrier transport through the i-GaAs area. In the GaAs p^+ -i- p^+ model the NDC branch was not formed (Fig.2(b), dotted line). Calculated C-V characteristic of n^+ -i- n^+ structure of $W = 10 \mu\text{m}$ and $L_i = 1,6 \mu\text{m}$ (Fig.2(b, solid

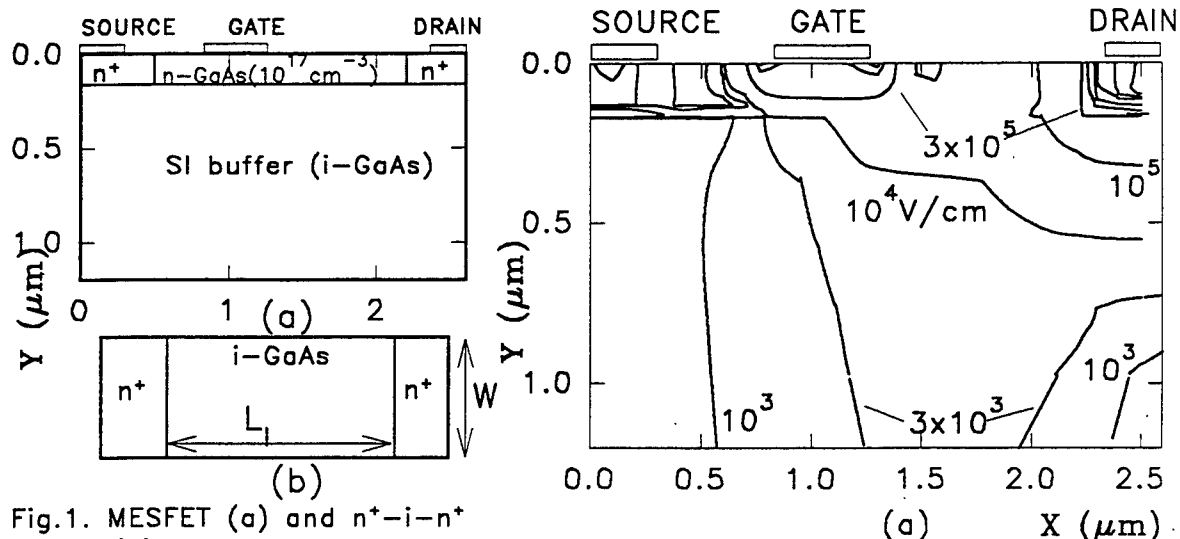


Fig. 1. MESFET (a) and $n^+ - i - n^+$ (b) structure models.

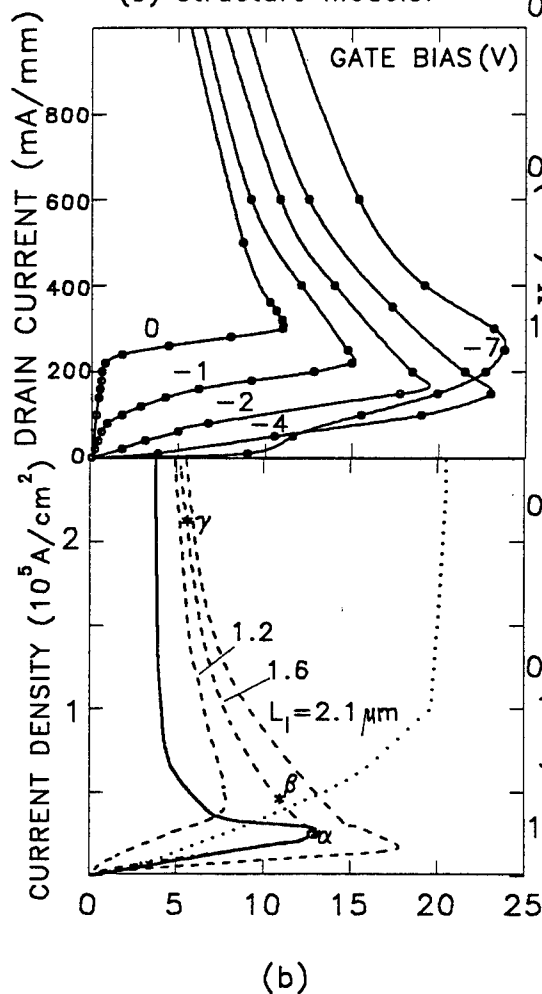


Fig. 2. Calculated drain current-voltage characteristics of the GaAs MESFET (a) and $n^+ - i - n^+$ (b) structures. Solid line 2D $n^+ - i - n^+$ structure $W = 10 \mu\text{m}$, dotted line $p^+ - i - p^+$ structure.

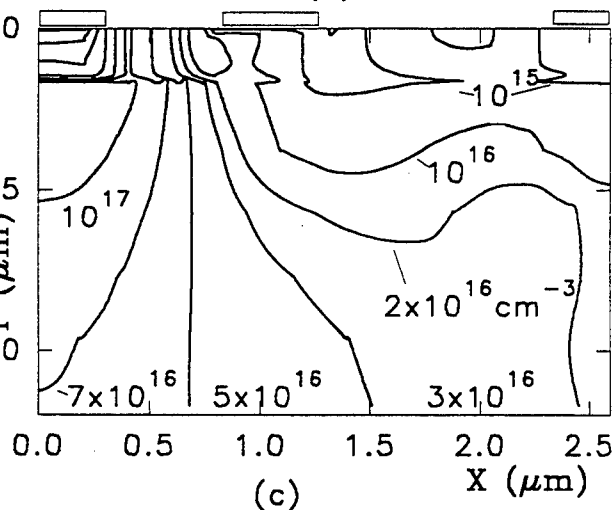
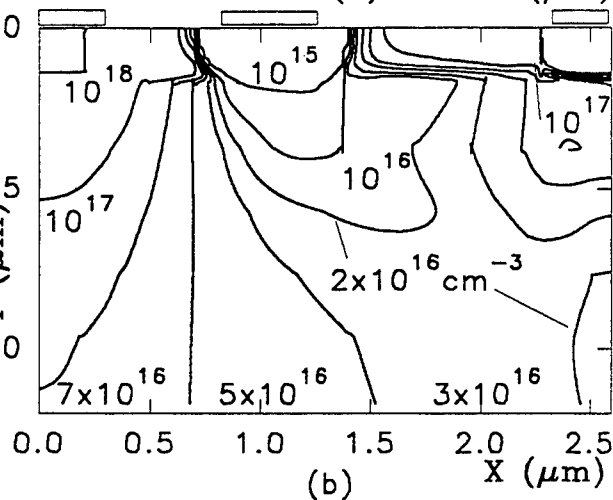
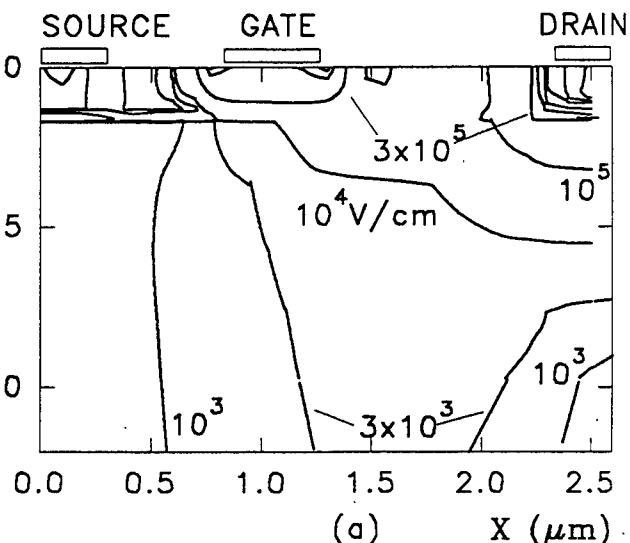


Fig. 3. Depth profiles of the electric field (a) electron (b) and hole (c) concentration for GaAs MESFET NDC condition ($I_D = 1000 \text{ mA/mm}$, $U_{GS} = -2 \text{ V}$)

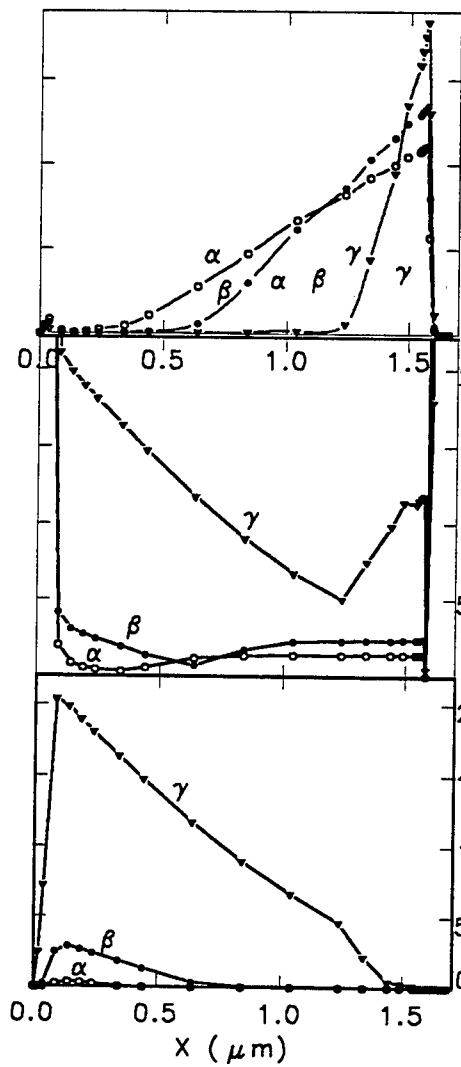


Fig.4. Electric field (a), electron (b) and hole (c) concentration distributions in 1D GaAs $n^+ - i - n^+$ ($L_1 = 1.6 \mu\text{m}$, $W = 0.3 \mu\text{m}$) in the states (α, β, ψ) (fig.2a).

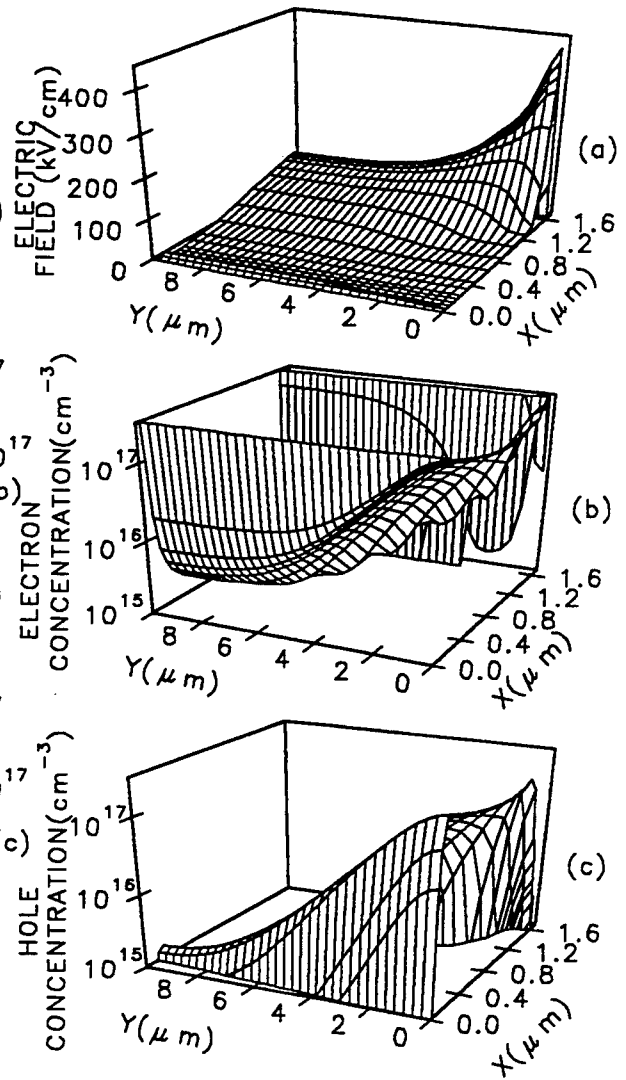


Fig.5. Electric field (a), electron (b) and hole (c) concentration distributions in 2D GaAs $n^+ - i - n^+$ structure ($L_1 = 1.6 \mu\text{m}$, $W = 10 \mu\text{m}$) in the current filament state.

line)) have the NDC branch corresponding to the carrier filamentation regime (Fig.5). In this regime distributions of electric field and carriers between n^+ contacts are the same as in the state (γ) of 1D model, but far from this regime-as those in the state (α).

DISCUSSION The calculated I_D - V_{DS} characteristics of GaAs MESFET model agree with the experiment [3]; electron-hole plasma distribution in the 2D GaAs n^+ -i- n^+ structure corresponds to the spectral and intensity distributions of the electroluminescence [3]. Therefore presented 2D model is acceptable for explanation of the observed I_D - V_{DS} characteristics and electrical burnout mechanism of GaAs MESFETs. The last can be explained as follows. With increasing of the drain voltage the high electric field domain is formed near the drain n^+ -contact in the SI layer due to and dropping dependence of the electron velocity vs electric field. A portion of holes generated near the drain is accumulated in the SI buffer layer near the source n^+ -contact. The holes positive space charge cause the injection of additional electrons into the SI layer from the source. The injected electrons create an additional negative space charge in the drain avalanche region. This results in the increase of the avalanche generation rate and holes injection. Such positive feedback leads to the formation of the spatial quasi neutral area (Fig.3 and 4(b,c)). The NDC branch of MESFET 's and n^+ -i- n^+ structures I-V curves are due to the extension of the quasi neutral domain in the SI substrate with increasing of the drain current. Current filamentation in the wide 2D GaAs n^+ -i- n^+ structure may be explained by spatial instability of current distribution typical for the S-type NDC [5].

CONCLUSION Using 2D simulation the breakdown mechanism of the GaAs MESFETs has been studied. The isothermal drain I-V characteristics of GaAs MESFETs have NDC branch at any gate bias. The mechanism of the NDC formation of GaAs MESFET is of an avalanche-injection nature [4] and presents itself as a modulation conductivity of the "built in MESFET" n^+ -i- n^+ structure (SI buffer & n^+ -contacts). The instability of current spatial distribution under NDC results in formation of 5-10 μ m high current filament in GaAs buffer. The GaAs MESFETs electrical burnout mechanism may be explained by: formation of the NDC, switching according to the drain load characteristics into the state with high conductivity; the filamentation of the avalanche injection drain current in the buffer and following rapid local melting of the MESFETs structure.

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INTRINSIC OSCILLATIONS IN MODIFIED HETEROJUNCTION BIPOLAR TRANSISTORS

Vladimir A. Posse and Bahram Jalali

Electrical Engineering Department, University of California, Los Angeles, California, 90095
e-mail: vposse@ee.ucla.edu, phone: (310)206-4554, fax: (310)206-8495

The transferred-electron (Gunn-Hilsum) effect resulting from the non-linear velocity-field characteristic in III-V semiconductors is widely utilized in micro- and millimeter-wave technology. If the electric field in a conventional n^+nn^+ Gunn diode exceeds the threshold value ($E_p \approx 3$ kV/cm for GaAs), injected electrons transfer from the central Γ valley to lower mobility L and X valleys resulting in the formation of propagating charge domains. There exists a great similarity between the active region of a Gunn diode and the collector drift region of a III-V npn heterojunction bipolar transistor (HBT). This has motivated us to investigate the transferred-electron effect in HBTs [1,2]. In a Gunn diode with $E > E_p$ and supercritical length $L > \kappa/N$ (where N is the doping of the active region and $\kappa = 10^{12}$ cm⁻² for GaAs) the transferred-electron effect causes current oscillations under a d.c. bias. However, such oscillations are not observed in HBTs even when the collector region satisfies the above criteria. We have previously shown that the stability of the collector current in conventional HBTs is ensured by the Kirk effect occurring at high levels of injection [2]. In this paper we discuss the physics of the transferred-electron effect and high injection phenomenon under transient conditions. We establish requirements for observing current driven instabilities in HBT structures.

In a conventional Gunn diode, a region where the magnitude of electric field has a positive gradient is a prerequisite for the formation of instabilities. Dynamics of a charge accumulation is related to the local electric field gradient through charge conservation, $\partial\rho/\partial t = -\nabla J$, where J is the local current density. For Gunn diodes with a high-field cathode this requirement results in the threshold condition on current density $J_G \geq eN_d v_s$, where $v_s \approx 10^7$ cm/s is the electron saturation velocity, e is the electronic charge, and N_d is the donor concentration [3]. The collector drift region of an npn HBT is analogous to a Gunn diode with a high-field cathode. The solid line in Fig.1 shows the electric field profile in the collector of an exemplifying transistor biased in the forward active region. The dash line there illustrates the conditions sufficient to observe the Gunn-Hilsum effect in the collector at current density $J_c > J_G$.

In an HBT high collector current leads to the Kirk effect (base widening). The base widening occurs at the collector current density $J_K \geq eN_d v_s + 2\varepsilon v_s \phi / L^2$, where ε is the dielectric constant, L is the length of the collector, and ϕ is the total base-collector potential. For HBTs with a collector design that satisfies the NL product criterion, the second term can be ignored. Kirk effect is detrimental to formation of charge instabilities since it eliminates high electric field at the cathode (the p - n junction) as shown by the broken line in Fig.1. Since the threshold current for Kirk effect, J_K , coincides with the threshold for Gunn effect, J_G , it effectively prevents transferred-electron induced instabilities. This explains the absence of the Gunn-Hilsum phenomenon in HBTs even when the collector drift region satisfies conditions sufficient to cause such oscillations in a Gunn diode.

To observe Gunn oscillations in an HBT one may attempt to increase the threshold

for Kirk effect. It has been suggested that an n^+ doping spike inserted at the base-collector interface of an npn HBT would suppress the Kirk effect [4]. However, detailed investigation by Lee *et al.* [5] later showed that this modification does not improve J_K under d.c. conditions. We have investigated the transient behavior of HBTs modified with an n^+ spacer layer using numerical simulations. Our results indicate that while the n^+ layer does not suppress the Kirk effect, it does delay its onset in time. This provides an opportunity for charge instabilities to nucleate under proper switching conditions.

We consider a GaAs HBT with a 1500\AA $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ emitter doped to $5 \times 10^{17} \text{cm}^{-3}$ preceded by a contact region consisting of an n^+ GaAs layer and 500\AA graded transitional layer. The 1000\AA p^+ GaAs base is doped to $1 \times 10^{19} \text{cm}^{-3}$, and collector consists of a $1.5\text{ }\mu\text{m}$ long GaAs drift region with $N_d = 1 \times 10^{16} \text{cm}^{-3}$ followed by an n^+ subcollector. The length and doping of the collector were chosen in order to satisfy the NL product condition. In the modified structure, a thin $2 \times 10^{13} \text{cm}^{-2}$ n^+ doping spike was placed at the base edge of the collector drift region. To investigate the behavior of HBT structures we use the hydrodynamic model of electron transport to simulate the transient device response. The self-consistent algorithm includes the first three moments of the Boltzmann transport equation along with the Poisson equation. The non-linear velocity-field characteristic leading to the Gunn effect is realized through a field dependent mobility model [6]. Recently, it has been shown by Zybura *et al.* that the hydrodynamic model can accurately simulate conventional Gunn diodes [7].

We have studied the transient response when the transistor is excited by step biases applied to the base and collector terminals [1]. The conventional HBT reveals a perfectly stable behavior, whereas the modified structure exhibits charge accumulation layers nucleating at the n^+ doping spike and propagating towards the subcollector. The behavior is similar to that of a Gunn diode operating in the stable-anode-domain mode. In order to understand the significance of the n^+ layer we investigate its influence on Kirk effect.

Figure 2 shows the simulated transient responses of the modified HBT at biases corresponding to $J_c < J_K$ (dot line: $V_{be}=1.5\text{ V}$, $V_{ce}=4\text{ V}$) and $J_c > J_K$ (dash line: $V_{be}=1.57\text{ V}$, $V_{ce}=4\text{ V}$), along with that of a conventional transistor at $J_c > J_K$ (solid line: $V_{be}=1.57\text{ V}$, $V_{ce}=4\text{ V}$). For demonstration we use a silicon-like mobility model since otherwise the Gunn effect induces current instabilities in the modified structure (as shown below). Figure 2 reveals that at high injection levels the n^+ spike causes a delay in the collector *terminal* current which may reach hundreds picoseconds. Inspection of the carrier densities and currents inside the collector shows that this delay is associated with the formation of the current-induced-base region. For base widening to occur, electron density in the collector must exceed the background ionized donor concentration. The time necessary for the build-up of electron density is longer in the modified structure, since the n^+ spike creates an additional reservoir to be filled by electrons injected from the base. During this charging time the terminal collector current is low, whereas the electron current in the vicinity of the cathode (base-collector junction) is high and may exceed J_C . Furthermore the electric field in the cathode region is high since the base widening has not yet occurred. Therefore, the n^+ spike provides a time period when *both* the electron current density and the electric field exceed threshold values for initiation of Gunn oscillations.

In a conventional transferred-electron device, self-maintaining oscillations are characterized by the propagating dipole domains in which a charge depletion layer precedes the accumulation layer. Formation of dipole domains may be triggered by random

doping fluctuations of sufficient magnitude [8]. To emulate the effect of doping inhomogeneities in the collector drift region we include a doping notch ($5 \times 10^{15} \text{ cm}^{-3}$, 400 nm long) in the collector. Similar techniques are commonly used to simulate conventional two terminal transferred-electron oscillators [9]. Figure 3(a) shows the simulated collector current density as function of time after applying step biases $V_{be}=1.525 \text{ V}$ and $V_{ce}=4 \text{ V}$ at $t=0$. The oscillation period is about 25 ps corresponding to the distance between the nucleation site and subcollector. Time evolution of the electron density reveals that when the incipient electron accumulation layer nucleated at the n^+ spike reaches the doping notch, a dipole charge domain forms behind the notch creating a high-field layer. After initial growth the latter propagates towards the anode where it is absorbed while the next domain forms at the notch. Results of analogous simulations performed with the silicon-like mobility model do not exhibit charge instabilities proving the transferred-electron nature of observed oscillations.

To underline the effect of the n^+ doping spike we perform the transient analysis of the same structure under identical bias conditions but without the spike at the base-collector junction. The result presented in Fig. 3(b) shows that after initial stabilization no oscillations are detected in such a structure. Although a doping fluctuation in the quasi-neutral region of the collector may create an electric field disturbance with characteristics adequate for Gunn domains nucleation ($E > E_p$, $\partial E / \partial x > 0$), the growth of a domain there would be prevented by the lack of voltage drop in the direction of possible domain propagation. On the other hand, in the proposed structure with the n^+ spike, an initial charge accumulation layer propagating away from the spike causes the electric field in front of it to rise, so that the base-collector voltage drop is effectively redistributed from the p - n junction to the region between the accumulation layer and subcollector. This leads to the growth of a dipole domain at the doping notch and hence triggers the oscillatory process.

In summary, we have investigated the prospects for transferred-electron induced instabilities in the collector of n pn HBTs. We have established that stability of conventional HBTs is ensured by the classical Kirk effect. Our study suggests that HBT structures with properly engineered collector doping profile may exhibit oscillatory behavior under d.c. bias conditions.

Acknowledgments: We are grateful for helpful discussions with Dr. M. Levinshtein of Ioffe Physical-Technical Institute, Russia. This work was supported by NSF grant ECS-9422538.

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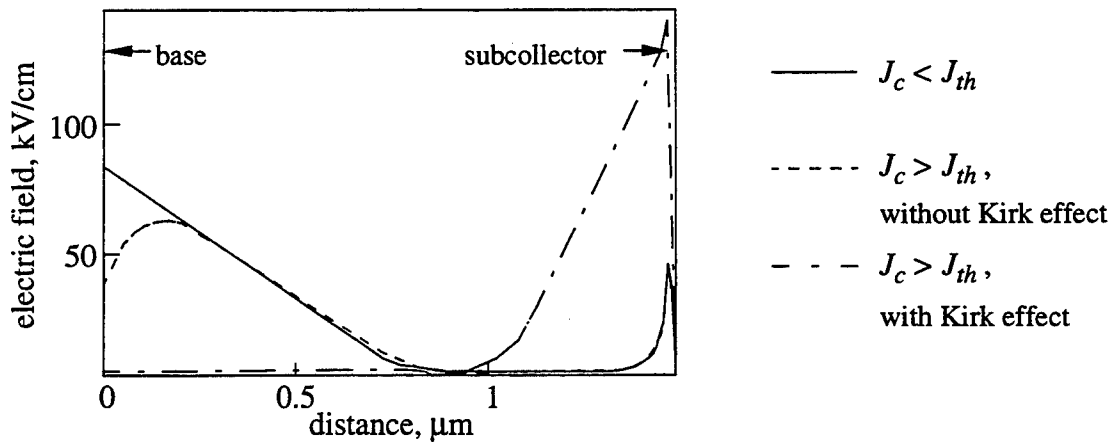


Figure 1: Electric field profiles in an HBT collector drift region at different levels of injection.

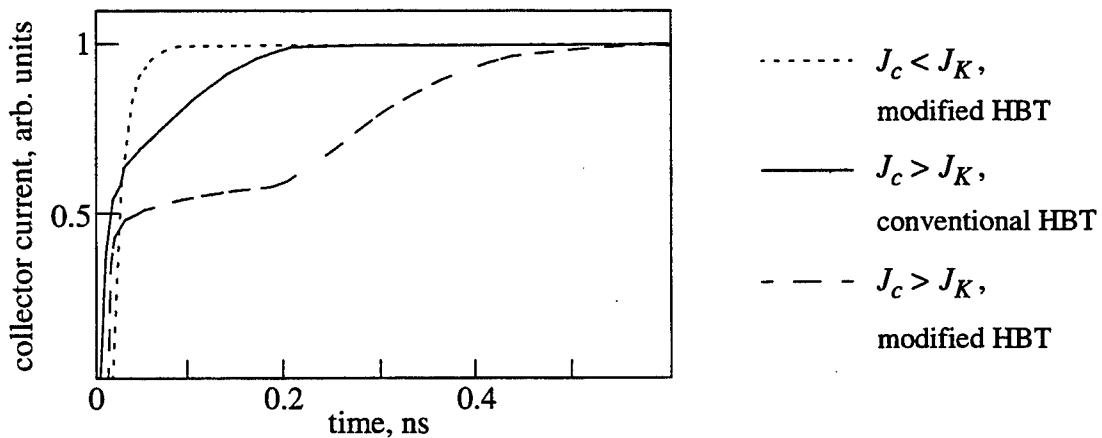


Figure 2: Normalized collector currents in conventional and modified HBTs at different levels of injection in the absence of negative differential mobility.

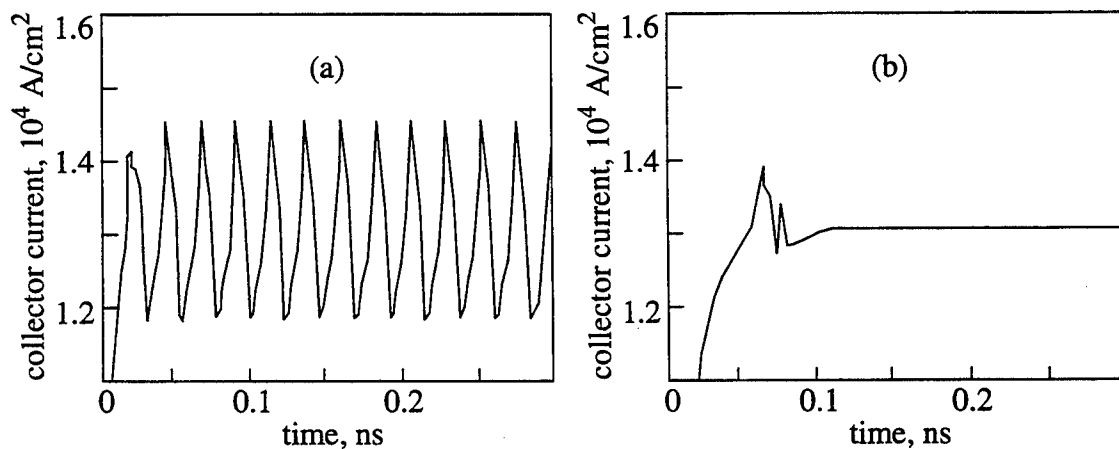


Figure 3: Collector current density after applying the bias $V_{be}=1.525$ V, $V_{ce}=4$ V to HBT structures with n^+ doping spike (a) and without it (b).

Electron System Properties In Semiconductor Structures Based On PbS And ZnCdHgTe Thin Layers

G.Khlyap, A.Andrukhiv

I.Franko Pedagogical Institute, Drogobych, 293720, Ukraine

L.V. Bochkariova

Yaroslavl State University, Yaroslavl, 150014, Russia

I. INTRODUCTION

The contacts of different semiconductor materials attract interest for investigation of their electron system properties and the application in device construction. The special interest is attracted by heterostructures based on narrow gap semiconductors which are obtained by MBE technology. In this work we report for the first time such results in n-PbS/n-ZnSe and Pb/p-ZnCdHgTe heterostuctures.

We present the main results of electrophysical and photoelectrical characteristics in 77-293 K range studies and energy band diagrams which are built according Harrison-Kroemer-Frensley theory [1,2].

II. EXPERIMENTAL

A. n-PbS/n-ZnSe heterostucture fabrication.

n-PbS films were grown in home-made equipment. The growth process was controled by modern methods of the surface monitoring. The film thickness was in the range 1-3 μm , the carrier concentration and the Hole mobility were $4.5 \cdot 10^{17} \text{cm}^{-3}$ and $1 \cdot 10^4 \text{cm}^2 / \text{V s}$, respectively.

B. ZnCdHgTe samples preparation.

ZnCdHgTe layers were grown by LPE and served as substrates for Pb/p-Zn_{0.17}Cd_{0.07}Hg_{0.76}Te Schottky barrier fabrication. The as-grown LPE layers had the Hole concentration $3 \cdot 10^{16} \text{cm}^{-3}$ and Hall mobility $600 \text{cm}^2 / \text{V s}$ at 77K.

III. RESULTS

The model [1,2] used for energy diagrams building is appicable only for abrupt heterostructures, so we investigated I-V and C-V characteristics for examination of their abruption (Fig.1).

The most interesting point in semiconductor heterostructures investigations is the construction of energy band diagrams. In our work we present the diagrams of n-PbS/n-ZnSe and Pb/p-ZnCdHgTe structures (Fig.2,3).

The C-V dependence is a straight line in coordinates $C^{-2}=f(V)$ and I-V characteristics are described by the following equations:

$$I_f = 0.25 evn_1 X \exp[-(\Delta E_c + E_{SS})/2kT] \exp(eV/nkT) \quad (1)$$

$$I_r = I_s X V (F_1 + F_2 - eV)^2 \quad (2),$$

where I_f and I_r are forward and reverse currents, respectively, I_s is saturation current, v is a thermal velocity, n_1 is the carrier concentration in substrates, X is a tunneling transparency coefficient, ΔE_c is the conduction band discontinuity, E_{SS} is the energy of surface electron states, F_1 and F_2 are quasi Fermi levels for majority carriers in heterocomponents.

The energy band diagrams were built according to the triangle potential well approximation [3,4]. The energy levels E_0 and E_1 are appeared in the narrow interlayer range on the heterointerface with the electron states concentration about $10^{11}-10^{13} \text{ cm}^{-2}$ (this value was determined by C-V measurements).

Both heterostructures were photosensitive in the 2-5 and 2-11 μm wave range respectively. The investigations of the carrier life time were carried out for the Pb/p-ZnCdHgTe heterostructures.

Minority carrier lifetime was measured by the photoconductivity decay technique. Experimental data were compared with the calculated values obtained using band-to-band radiative and two Auger recombination mechanisms. In the calculation analytical expressions for the energy gap, dielectric constants, and intrinsic carrier concentration vs temperature and composition of quaternary solid solutions ZnCdHgTe were used. Satisfactory coincidence of the experimental temperature dependence and the calculated according to the chosen model proves that concentration of the recombination centers in the epilayers to be negligible.

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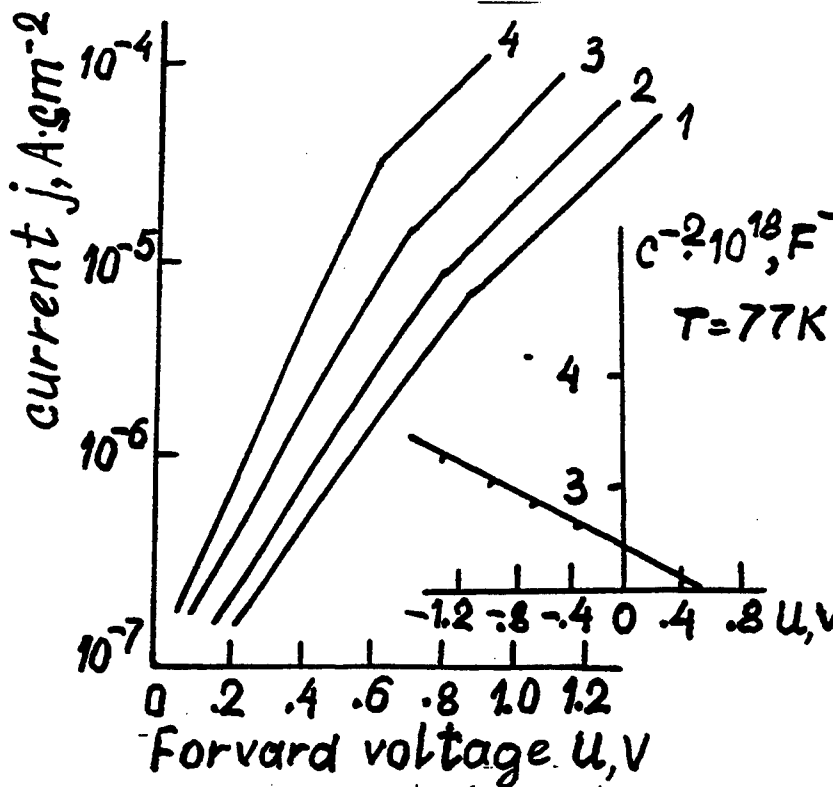


Fig. 1. I-V and C-V (insert, $T = 77$ K) characteristics of n-PbS-n-ZnSe heterostructure. T , K: 1 - 77, 2 - 180, 3 - 235, 4 - 293.

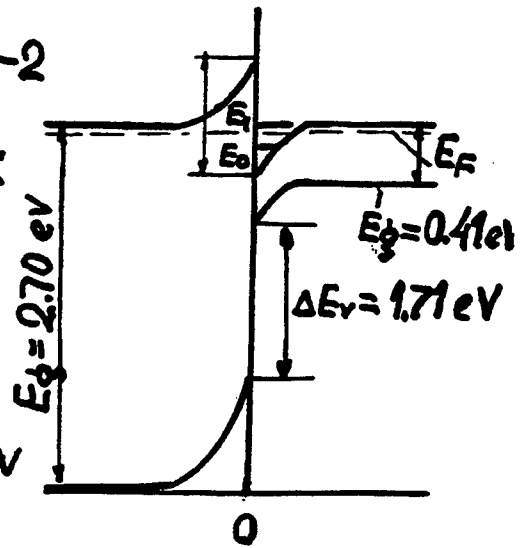


Fig. 2. Energy band diagram of n-PbS-n-ZnSe heterostructure, $T = 77$ K. $E_0 = 3.76$ meV, $E_1 = 4.12$ meV

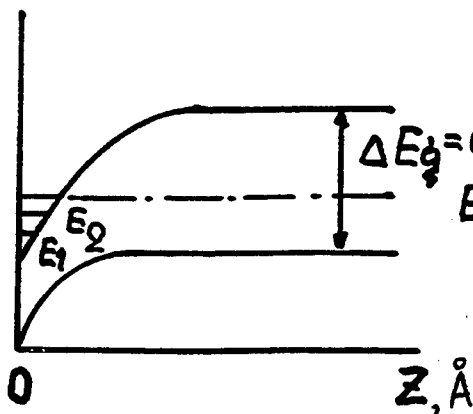


Fig. 3. Energy band diagram of Pb-p-ZnCdHgTe heterostructure, $T = 77$ K.

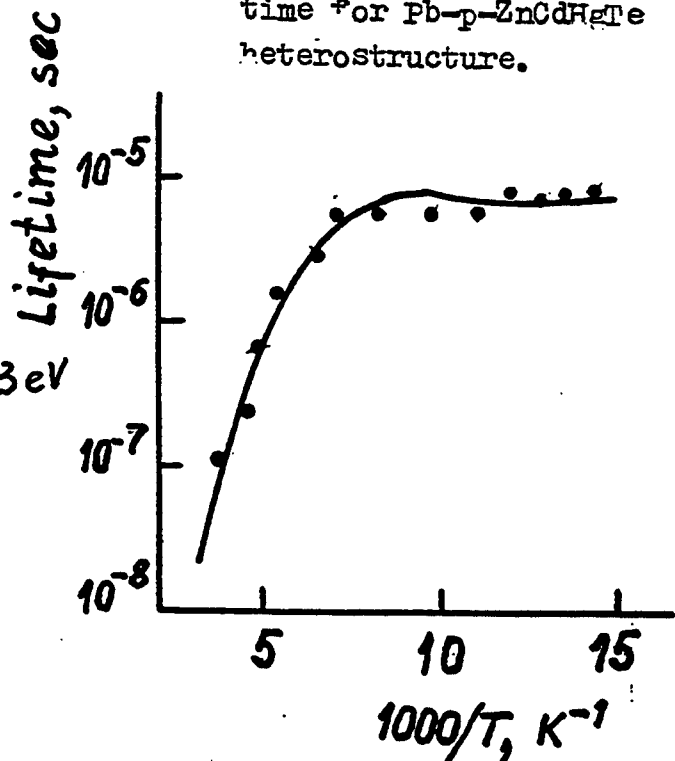


Fig. 4. Temperature dependence of carrier lifetime for Pb-p-ZnCdHgTe heterostructure.

Phonon Wall as a Mean of Enhancing Electron Mobility in 2D Structures

Juras Požela, Vida Jucienė, and Karolis Požela
Vilnius, Lithuania

In two-dimensional (2D) AlAs/GaAs MODFET heterostructures where impurity scattering is eliminated by spatial separation between the carriers and the parent donors electron - polar optical phonon scattering play a dominant role at temperatures $T > 80$ K. It determines an electron mobility and other electrical properties of semiconductor devices [1]. In order to improve high-speed parameters of MODFETs it is a considerable interest to enhance an electron mobility in 2D channels by reducing electron - optical phonon scattering.

It is well known that electrons and polar optical phonons due to their different physical nature can be confined in heterostructures independently in their quantum wells (QWs). These structures can be used for the enhancement of an electron mobility by reducing the electron - optical phonon scattering rate [2-5]. Recently it has been shown that the most significant reduction of the scattering is expected when a new type of barrier - phonon wall (phonon-reflecting barrier transparent to electrons) is inserted into an electron QW [6]. Thin AlAs layer (one to three monolayers) can serve as a phonon wall in GaAs QWs.

In this work we analyze the possibilities for designing phonon walls in electron QWs and calculate the confined electron - phonon scattering rate dependencies on the phonon wall position, thickness and surrounding heterostructure. It is shown that the decrease of the intrasubband ($l \rightarrow l$) scattering rate is maximal when the phonon wall is placed in the center of the electron QW, mainly due to the great reduction of confined phonon scattering rate (5 times in the QW with the width lower than 50 \AA) (Fig. 1). The reduction of the total scattering rate (due to confined and interface phonons) is a function of the electron - phonon coupling constant that depends on the parameters of the phonon wall and surrounding heterojunctions.

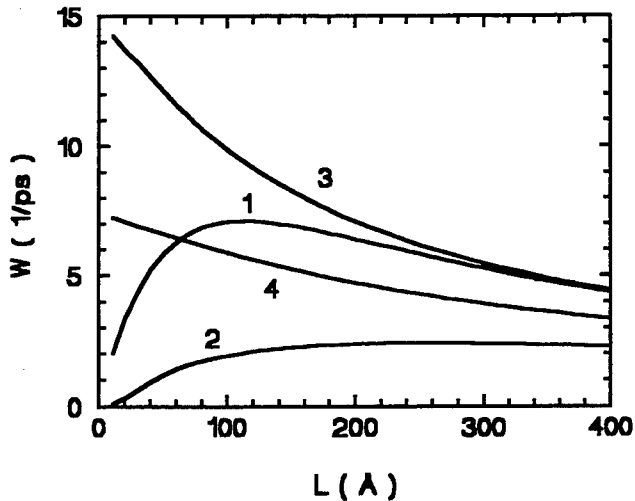


Fig. 1. Electron-phonon scattering rates in QW. Curves 1 and 2 are for confined phonon scattering without Ph-wall (curve 1) and with Ph-wall (curve 2), curves 3 and 4 are total scattering without Ph-wall (curve 3) and with Ph-wall (curve 4).

insertion of the phonon wall into the FET 2D channel is a powerful method of improving the characteristics of the transistor.

The reduction of the scattering rate in the case when bulk phonons are divided by the phonon wall inserted in the electron QW with a low width is about twice.

The calculations of the scattering rate in the single heterostructure with the inserted phonon wall (analogous with the MODFET channel) show that the enhancement of 2D electron gas mobility is more than 1.4 times at temperatures $T = 80 - 300$ K. The

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Identification of a Coulomb Correlation Gap and its Influence on Carrier Transport in Non-Metallic Si:B

Mark Lee and J. G. Massey

Department of Physics, University of Virginia, Charlottesville, VA 22903

Using a metal-insulator-semiconductor (MIS) tunneling device fabricated on single crystal boron-doped silicon (Si:B) with dopant density below the metal-insulator transition, we have been able to identify quantitatively the properties of the Coulomb correlation gap in the density of states $N(\epsilon)$ first predicted 20 years ago by Efros and Shklovskii (ES).¹ In agreement with this analytic model, $N(\epsilon)$ is found to have a nearly parabolic energy dependence, resulting in a “soft” zero at the Fermi energy, with a gap width ≈ 0.75 meV. We have further done ultra-low temperature resistivity measurements of the Si:B itself to demonstrate precisely how this Coulomb gap governs the crossover between non-interacting and correlated hopping transport.

In insulating doped semiconductors, carrier transport occurs via inelastic hopping. Mott showed² that at low temperature electrons seek accessible energy states by hopping distances beyond the localization length, leading to variable-range hopping conductivity $\sigma(T) \propto \exp(-T_0/T)^\nu$. For non-interacting electrons $\nu = 1/4$ in 3-D. ES argued¹ that, including Coulomb interactions, the ground state is stable with respect to a single carrier excitation only if $N(\epsilon)$ has a quadratic dependence on ϵ near ϵ_F :

$$N(\epsilon) = \frac{3}{\pi} \left(\frac{\kappa}{e^2} \right)^3 (\epsilon - \epsilon_F)^2 \quad (1)$$

where κ is the dielectric constant. Because $N(\epsilon)$ vanishes only at ϵ_F , this is a “soft” Coulomb correlation gap with a width $\Delta_C = e^3(N_0/\kappa^3)^{1/2}$, where N_0 is the non-interacting density of states. In general,³ a power-law $N(\epsilon) \propto (\epsilon - \epsilon_F)^m$ results in a hopping exponent $\nu = (m+1)/(m+4)$ as $T \rightarrow 0$, so that (1) gives $\nu = 1/2$. When T is high enough for a hopping electron to explore an energy range $k_B[T^3T_0]^{1/4} > \Delta_C$, where $T_0 = 18/(k_B\xi^3N_0)$ and ξ is the localization length, the influence of the Coulomb gap can be neglected and the $\nu = 1/4$ exponent is expected. Below a temperature $T_x = 0.38e^4\xi N_0/k_B\kappa^2$, only states inside the gap are accessible and a crossover to $\nu = 1/2$ is predicted.

Using a MIS tunnel junction, we have made a quantitative measurement of the soft Coulomb correlation gap and have measured its relationship to the conductivity in Si:B.

The conductivity of Si:B across its MIT was extensively studied by Sarachik and co-workers,⁴ whose measurements show a critical boron density $n_c = 4.0 \times 10^{18} \text{ cm}^{-3}$. Electron tunneling in metallic Si:B crystals was reported by Wolf, *et al.*⁵, using Schottky contacts. They observed a conductance cusp.

When a conductor is separated from a conventional metal by a rectangular potential barrier high enough to prevent classical current flow but thin enough to permit quantum tunneling current, the tunneling conductance, $G(V) = \partial I / \partial V$ is given by:

$$\frac{G(V)}{G_0} = \int_{-\infty}^{+\infty} \frac{N(\epsilon)}{N_0} \left[-\frac{\partial f(\epsilon - eV)}{\partial(eV)} \right] d\epsilon \quad (2)$$

where G_0 is the conductance in the non-interacting case, f is the Fermi function, and V is the applied voltage between electrodes. We take $\epsilon_F = 0$. In many cases, interactions alter $N(\epsilon)$ within at most a few meV of ϵ_F , so that G_0 is taken as the conductance at a high enough voltage bias where $I(V)$ is nearly ohmic. The conductance then gives $N(eV)/N_0$ thermally broadened by $-\partial f / \partial(eV)$. The classic application is in superconductor gap spectroscopy, where $N(\epsilon)/N_0 = \text{Re}[\epsilon / (\epsilon^2 - \Delta^2)^{1/2}]$ has a distinctive shape. When one electrode is a superconductor, observation of this structure definitively establishes that the junction current is due to quantum tunneling.

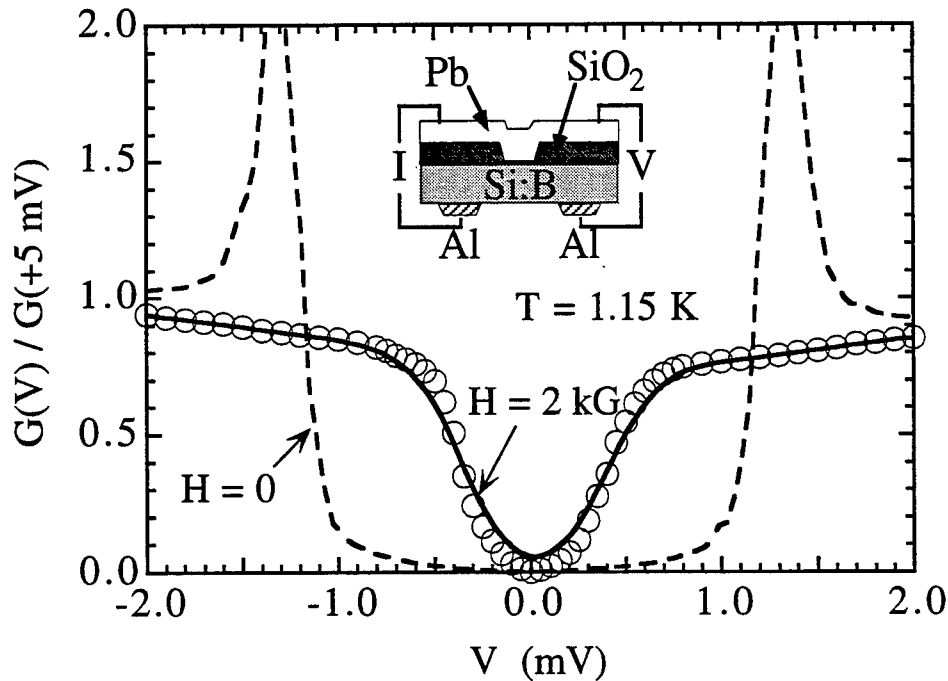


Figure 1. Conductance vs. voltage bias of a Pb-SiO₂-Si:B device at 1.15 K. The dashed curve is in zero magnetic field. The solid curve is in 2 kG. The circles are this data with the thermal broadening removed. **Inset:** Schematic cross section (not to scale) of the junction.

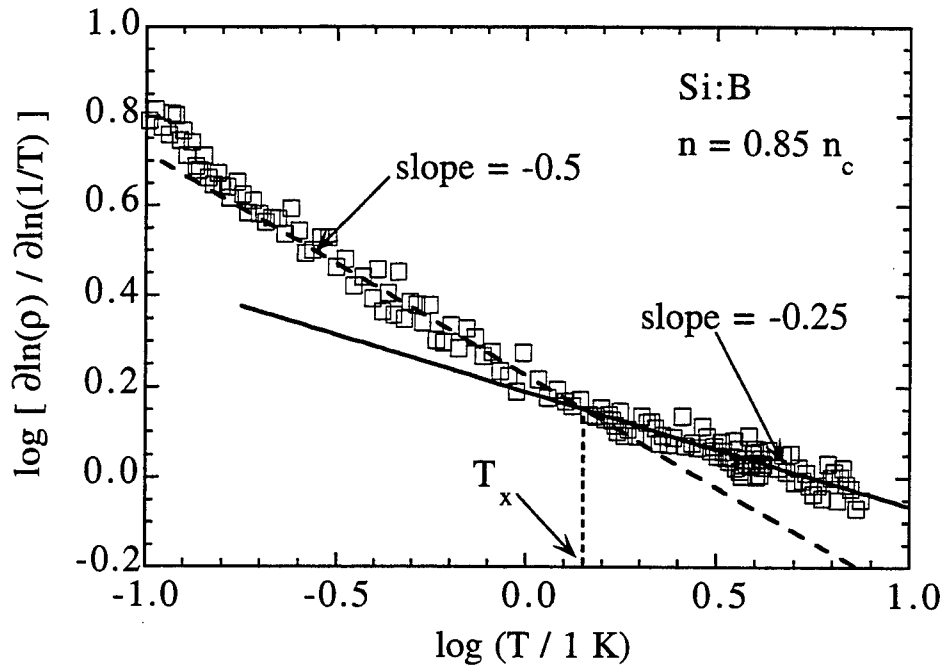


Figure 2: Plot of $\log[\partial \ln(\rho)/\partial \ln(1/T)]$ vs. $\log[T]$. The slope of the data gives the negative of the hopping exponent. The solid line is a linear fit to the range $1.5 \text{ K} < T < 10 \text{ K}$. The dashed line is a linear fit to the range $0.3 \text{ K} < T < 0.8 \text{ K}$.

We fabricated tunnel junctions on $\langle 100 \rangle$ -oriented single crystal wafers of Si:B grown by PureSil, Inc. The resistivity ratio $\rho(4.2 \text{ K})/\rho(300 \text{ K})$ gave a boron density $n = 3.4 \times 10^{18} \text{ cm}^{-3}$, or $n/n_c = 0.85$. We fabricated a more ideal tunnel junction by the following procedure. Both sides of 12 mil thick crystals were cleaned,⁶ and a 150 nm SiO_2 layer was grown. The SiO_2 was stripped off one side (the “back”) and four Al stripes were evaporated. Ohmic contacts were formed by briefly annealing the Al stripes. The tunnel junction was made on the “front” by etching a slot in the SiO_2 down to the Si. A very thin (5 to 8 Å) SiO_2 layer, the tunnel barrier, was then grown using the methods described in Ref. 7. Pb stripes were evaporated through a mask, crosswise to the patterned slot, to serve as the counterelectrodes. Junction quality was sensitive to the fabrication details. The “failure” mode was a junction resistance $> 10 \text{ M}\Omega$. To prove that the conductance was due to quantum tunneling, our criterion for a “good” junction was observation of the superconducting gap of Pb. The Pb could be driven to its normal state by a 2 kG magnetic field, which allowed measurement of the density of states of the Si:B alone.

Figure 1 shows a normalized tunneling conductance spectrum taken at 1.15 K in both zero field, where the Pb is superconducting, and in 2 kG, where the Pb is normal. The zero field data clearly show the superconducting density of states of Pb, *proving* that the

junction conductance is due to quantum tunneling. A “soft” depletion in the density of states of the Si:B is revealed when a 2 kG field drives the Pb normal. There is a clear dip in $G(V)/G_0$ between ± 0.5 mV, which is the signature of the Coulomb gap. Near $V = 0$, the measured conductance is approximately parabolic but does not go to zero. At 1.15 K the conductance is broadened by thermal smearing. Using the $G(V)/G_0$ data, the thermal smearing can be deconvoluted from the integral in (2). The result is depicted by the circles in Fig. 1. This gives a functional form $N(eV)/N_0 \propto |eV|^{2.2}$, and a width $\Delta_C \approx 0.75$ meV. Also, most of the small measured conductance at $V = 0$ is removed from $N(eV)$.

The hopping exponent ν can be determined without prior assumptions about carrier transport by plotting $\log[\partial \ln(\rho)/\partial \ln(1/T)]$ against $\log(T)$, the linear slope of which gives $-\nu$. This is shown in Fig. 2. Clearly, a single line does not fit the data over the entire temperature range. A linear fit for $T > 1.3$ K yields a slope of -0.25 , indicative of Mott hopping. A fit over a limited temperature range ($0.3 \text{ K} \leq T \leq 0.8 \text{ K}$) yields a slope of -0.5 , consistent with ES hopping. The empirical crossover temperature T_x between non-interacting and Coulomb correlated regimes can be defined where the slope = -0.5 and slope = -0.25 lines in Fig. 3 intersect. This gives $T_x = 1.4$ K.

The independent measurements of both density-of-state structure and resistivity on the same Si:B sample allow us to definitively establish the influence of the Coulomb gap on charge transport. The measured Coulomb gap form $N(\epsilon) \propto \epsilon^{2.2}$ predicts a hopping exponent $\nu = 0.52$ near 1 K, consistent with the transport data. This demonstrates that the shape of the gap determines the hopping characteristics in the expected manner. Moreover, the size Δ_C of the Coulomb gap, as measured by tunneling, determines the crossover temperature T_x , as measured by the resistivity. This can be shown by noting that, within the ES model, Δ_C , T_x , and T_0 are defined to satisfy the consistency relation $\Delta_C = k_B(T_x^3 T_{0M})^{1/4}$. From the data, using the *independently measured* values $\Delta_C = 0.75$ meV, $T_x = 1.4$ K, and $T_{0M} = 1500$ K, we obtain a relation $\Delta_C/k_B = 1.1(T_x^3 T_{0M})^{1/4}$, in reasonable agreement with the model, given our empirical definition of T_x .

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Hot-Electron Fluctuations in n-type GaAs at Extremely High Electric Fields

V.Aninkevičius, V.Bareikis, R.Katilius, J.Liberis, I.Matulionienė,
A.Matulionis, P.Sakalas, and R.Šaltis

Semiconductor Physics Institute, A.Goštauto 11, LT-2600 Vilnius, Lithuania

We are presenting experimental results on hot-electron noise in GaAs at electric fields over 25 kV/cm. The intervalley noise temperature is found to saturate at 15000 K in the field range over 100 kV/cm. The scattering time of high-energy electrons from the Γ -valley into the X-valleys is estimated: $20 \text{ fs} < \tau_{\Gamma X} < 60 \text{ fs}$.

Noise spectroscopy is known [1] to be a powerful tool to study hot-electron kinetic processes. In particular, microwave fluctuations in n-type GaAs at sufficiently high electric fields are dominated by intervalley transfer. The hot-electron transfer from the Γ -type valley to the L-type satellite valleys of the conduction band appears at fields over 2 kV/cm, and the intervalley Γ -L fluctuations remain the most important source of microwave noise in long samples until the hot electron velocity fluctuations are obscured by Gunn instabilities. The latter can be avoided in short channels; as a result both Γ -L and Γ -X transfer contributions to microwave noise have been resolved in n-type GaAs at fields below 30 kV/cm [2]. On the other hand, electric fields over 100 kV/cm are often found in channels of field-effect transistors. The electrons are extremely hot in the high-field region of the channel, and investigation of hot-electron velocity fluctuations is important for understanding low-noise performance of field-effect transistors at microwave frequencies.

In this contribution, results of microwave noise measurements in n-type GaAs at electric fields up to 300 kV/cm are presented. Ungated channels of submicron length were investigated. Figure 1 gives a sketch of a sample: a recessed silicon-doped GaAs channel on an insulating substrate has two ohmic electrodes of Au-Ge evaporated onto an n^+ -doped cap layer. The electrons are heated up by pulsed voltage to reduce the channel overheat.

Short 100 ns voltage pulses were necessary, and a nanosecond/microwave sample holder was designed to perform short-time-domain pulsed measurements of hot-electron noise power at microwave frequencies. Equivalent noise temperature of hot electrons was measured in 10 GHz frequency band. The typical pulse repetition frequency was 55 Hz. The principle of measurement is illustrated by Fig.2 [3]. The sample was placed into a coaxial

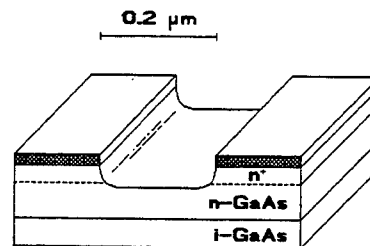


Fig.1. A schematic view of a recessed ungated n-type channel of GaAs on an insulating substrate.

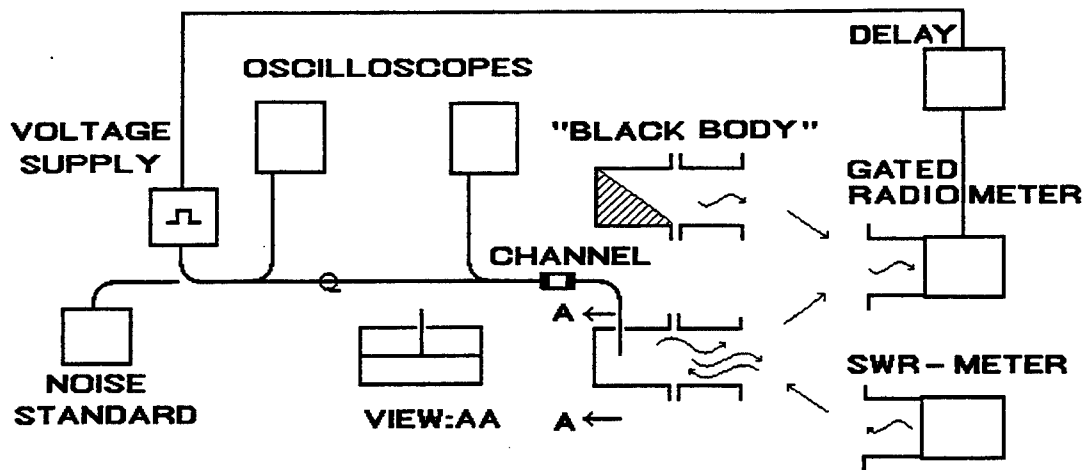


Fig.2. Main blocks used to measure hot electron noise temperature.

cable of the nanosecond circuit and coupled to the waveguide by means of a T-shaped antenna (Fig.2, the cross-section view: AA). When the voltage pulse was applied the incident/reflected pulse waveforms were fed into the oscilloscopes and analyzed to obtain voltage dependence of the channel current. The coupling and transmission coefficients and waveguide losses were determined using the noise standard. The delay of the gating ensured the noise power measurements before, during, and after the voltage pulse. This was sufficient to control the channel overheat and keep it low enough. Matching of the channel circuit to the waveguide was controlled by the standing-wave-ratio-meter (SWR-meter). Its readings were voltage-dependent, they were taken into account while determining the noise temperature. The noise power radiated by the channel and detected by the gated radiometer was compared to that of the "black body" radiation source kept at known temperature. This technique enabled to measure the equivalent noise temperature of hot-electron velocity fluctuations in the channel in the direction of applied electric field.

Figure 3 shows dependence of the equivalent noise temperature on the average electric field defined as $E = U/L$, where U is the applied voltage and L is the sample length. Exploitation of 100 ns voltage pulses opens an essentially wider range of fields and noise temperatures as compared to the microsecond time-domain data. An essential increase of the hot-electron noise temperature takes place at 25 kV/cm average field (Fig.3, open squares). This increase is followed by the noise temperature saturation at fields around 100 kV/cm and by another, a much stronger, source of fluctuations dominating at fields over 200 kV/cm.

The excess noise temperature $\Delta T_n = T_n - T_0$, where $T_0 = 293$ K, is plotted as a function of the applied voltage U in Fig.4. A decomposition of the $\Delta T_n(U)$ dependence into four sources of noise is given: thin lines in Fig.4 represent possible contributions of each source. The contributions sum up into the solid line, which fits the experimental results pretty well. The lowest threshold appears at around 0.2 V. It has been associated with the resonant scattering of hot electrons by the impurity levels located inside the conduction band [2]. The next two sources with thresholds at 0.3V and 0.5V are caused by the intervalley transfer of

hot electrons. Since the hot-electron noise in short samples at very high fields is contributed quite a bit by ballistic electrons, the sources due to the L-type and X-type valleys of the conduction band (with the threshold energies close to 0.3 eV and 0.5 eV, correspondingly) are resolved at different voltages. Our experimental results show that the maximum contribution to the noise temperature due to L-valleys is essentially lower than that due to the Γ -X transfer (Fig.4).

The extrapolation of $\Delta T_n(U)$ data obtained at fields over 200 kV/cm yields the threshold energy for the fourth source; the energy exceeds the forbidden gap (Fig.4). This source of noise is accompanied by the steep increase of the current and consumed power (Fig.5); impact ionization is thought to be responsible for.

The saturation of hot-electron noise temperature on field at $E < 100$ kV/cm and $E > 200$ kV/cm. This very specific behaviour suggests two independent ways for estimation of the time constant of the intervalley scattering experienced by the high-energy electrons present in the Γ -valley at/over the X-valley energy ($\epsilon > 0.5$ eV).

The observed strong dependence of the intervalley noise temperature on field at $E < 100$ kV/cm means that the hot-electron intervalley fluctuations are limited by the electron acceleration rather than the Γ -X transfer of the already accelerated electrons. Contrary, the saturation of the noise temperature at $E > 100$ kV/cm means that the acceleration no longer decides the result. Consequently, the acceleration time at these fields is already shorter than the Γ -X transfer time. On the other hand, some of the high-energy electrons in the Γ -valley can avoid Γ -X transfer and be accelerated up to the energies

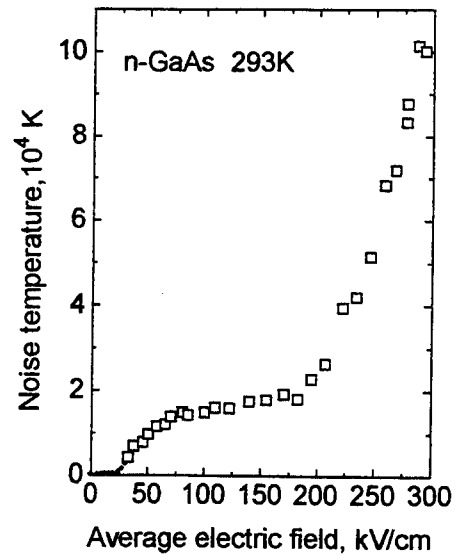


Fig.3. Field dependent hot-electron noise temperature: 2 μ s pulses (dots) and 100 ns pulses (squares). $n=3 \cdot 10^{17} \text{ cm}^{-3}$, $T_0=293 \text{ K}$, $L=0.2 \mu\text{m}$.

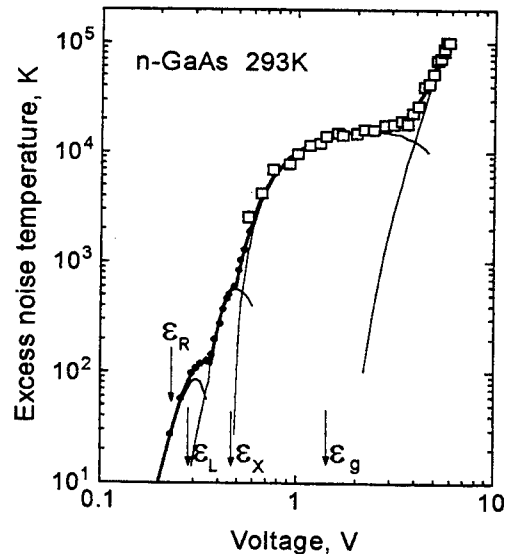


Fig.4. Voltage-dependent excess noise temperature of hot electrons ($n=3 \cdot 10^{17} \text{ cm}^{-3}$, $L=0.2 \mu\text{m}$) at $T_0=293 \text{ K}$. 2 μ s pulses (closed circles), 100 ns pulses (squares), different sources of noise (thin lines) and sum of the source contributions (solid line).

sufficient for impact ionization. The related noise becomes dominant when the time required for electron acceleration inside the Γ -valley from 0.5 eV to the impact ionization energy becomes shorter than the Γ -X transfer time. Our experimental results show that the Γ -X transfer is too weak to eliminate impact ionization in n-type GaAs at fields exceeding 200 kV/cm.

Supposing that the Γ -valley electrons are accelerated ballistically, the acceleration time of a cold electron to the X-valley energy (0.5 eV) is 60 fs at 100 kV/cm. The additional acceleration time of the high-energy electron to the impact ionization energy (i.e. from 0.5 to 1.5 eV) at 200 kV/cm is 20 fs. Since the obtained acceleration times are short as compared to the time of spontaneous

emission of an optical phonon (190 fs, [4]), one finds out that the evaluation based on ballistic acceleration is self-consistent. Thus the Γ -X transfer time falls into the range $20 \text{ fs} < \tau_{\Gamma X} < 60 \text{ fs}$. This estimation, based on hot-electron noise data, does not contradict to that obtained from optical cw spectroscopy data [5].

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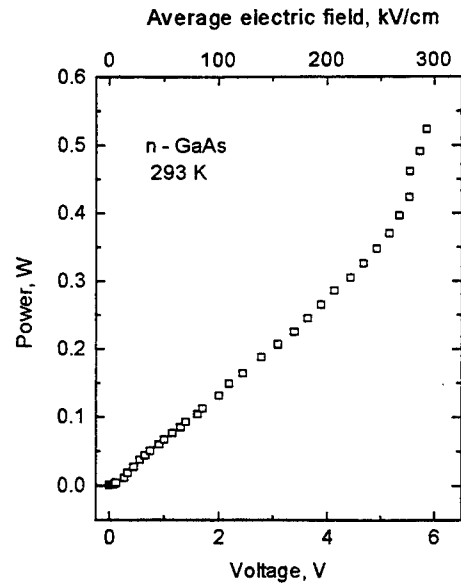


Fig.5. Dependence of consumed power on voltage. $n=3 \cdot 10^{17} \text{ cm}^{-3}$, $L=0.2 \text{ }\mu\text{m}$.

Concept of the realization of the ultimate possible
photogain in intrinsic photoresistors under given
concentration of the impurity recombination centres

A.A. Drugova,

V.A. Kholodnov

Research, Development, and Production Centre "Orion",
Plekhanov St. 2/46, Moscow, 111123, Russia

The greatest photogain in the intrinsic photoresistor is attained when the electron and hole lifetimes τ_n and τ_p exceed their times of the transit [1-4]. Often τ_n and τ_p are conditioned by the recombination of carriers via impurity centres [2,3,5], which sometimes especially introduced [6,7].

It might seem that the increase in the concentration of recombination impurity atoms N always reduces τ_n and τ_p due to the increase in the capture rate of non-equilibrium carries. However, as we are able to show [8-10], under certain conditions the τ_n and τ_p very strongly increase with the N increase within a certain interval (Fig.1) due to weak non-equilibrium occupation of the recombination level with the energy E_t . Let semiconductor is doped with a shallow donors and recombination centres be acceptors. Consider a small departure from equilibrium. In this case $\tau_p(N)$ may be a non-monotonic function if

$$\sqrt{2N_D} \gg \sqrt{n_t}, \quad 3n_t^2 \ll 4\theta n_i^2 \ll \theta N_D^2, \quad (1)$$

where N_D and n_i - shallow-levels donors and carrier intrinsic concentrations, n_t - equilibrium concentration of electrons when Fermi level energy $E_F = E_t$, $\theta = w_p/w_n$,

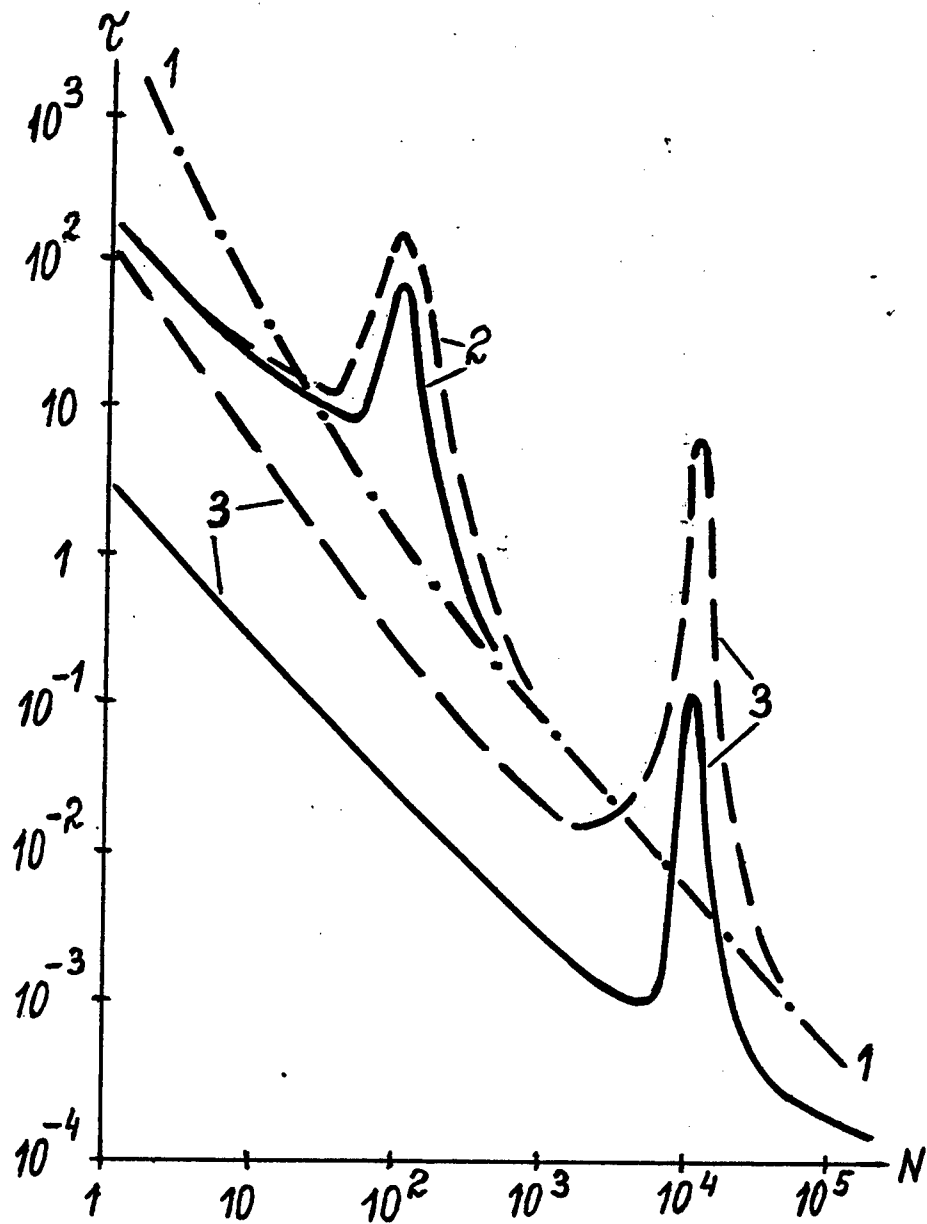


Fig.1. The dependences of $\tau_p \langle - \rangle$ and $\tau_n \langle - - - \rangle$ on N at different values of N_D . 1 ($\tau_n \cong \tau_p$) - $h \cong N_D / n_i < 1$; 2 - $h = 10^2$; 3 - $h = 10^4$. Lifetimes are measured in the units $(n_i w_p)^{-1}$, N - in units n_i . It is assumed that $\theta = 10^2$, $n_t = 10^{-2} n_i$.

w_p and w_n - hole and electron capture probability. The $\tau_n(N)$ non-monotonic dependence takes place if

$$\sqrt{N_D} \gg \sqrt{2n_t}, \quad 2\tilde{n}_i \ll N_D. \quad (2)$$

The value of N when $\tau_p(N)$ and $\tau_n(N)$ attain their maximum

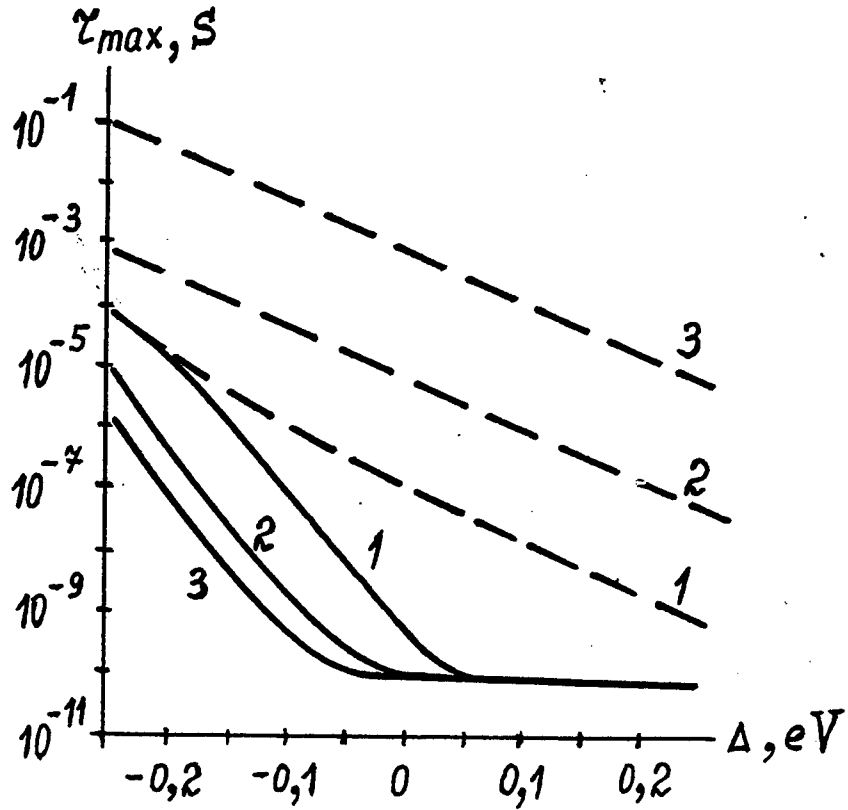


Fig.2. The dependences of τ_{pmax} $\langle - \rangle$ and τ_{nmax} $\langle - - - \rangle$ for Ge(1), Si(2) and GaAs(3) on $\Delta \equiv E_t - E_g/2$ under temperature 300 K. It is assumed that $N_D = 10^{16} \text{cm}^{-3}$, $w_n = 10^{-8} \text{cm}^3/\text{s}$, $\theta = 10^2$. E_g - bandgap.

extrema in a zero approximation is N_D . The ratio τ_{max}/τ_{min} may be several orders [8-10]. The τ_{pmax} , τ_{nmax} values strongly depend on E_t (Fig.2) and increase with the N_D decrease (Fig.1). We are able to show that the coefficients a_1 and a_2 for example, in the continuity equation of electron current [11]

$$D^n \frac{\partial^2 \Delta n}{\partial x^2} + a_1 \frac{\partial \Delta n}{\partial x} + a_2 \left[\frac{\partial \Delta n}{\partial x} \right]^2 = \frac{\Delta n}{\tau_n} - g, \quad (3)$$

vanish at the same concentration of $N = N_D$ when $\tau_p(N)$ and $\tau_n(N)$ attain their maximum extrema, where D^n - effective diffusion coefficient of electrons, Δn - concentration of non-equilibrium electrons, g - rate of photogene-

ration. It means that the electrical field E does not affect the space distribution of non-equilibrium carriers [11]. The diffusion distribution remains of course in the some vicinity of $N = N_D$ too. Therefore, in these conditions the photogain saturation with E increase [1,2] does not occur even under the extracting contacts. Thus, concept on which we should like to report consists in the doping of the semiconductor with shallow donors to $N_D=N$. At the cost of that it is possible to increase photogain very strongly even under large values of N . The photogain increasing is the more the lower E_t and occurs at an arbitrary low excitation level.

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Study of the effects of high temperature and substrate biasing on the D.C./high frequency characteristics of GaAs-based devices

R. P. Rozario, R. Narasimhan, L. P. Sadwick and R. J. Hwu
Department of Electrical Engineering
University of Utah
Tel: 801-581-8282, Fax: 801-581-5281

ABSTRACT

A novel high temperature electronic technique (HTET) has been developed to stabilize the performance of GaAs-based devices (MESFETs, HEMTs) at elevated temperatures [1-5]. In this technique, a voltage of correct magnitude and polarity is applied to the substrate which substantially reduced the leakage currents in the substrate, improved the output resistance and the breakdown voltage. The HTET also aids in obtaining comparable high frequency gain at elevated temperatures to the gain obtained at room temperature. Due to space limitations, we will only discuss the D.C. results for depletion MESFETs, and high frequency gain (S_{21}) results for HEMTs in this abstract.

D.C.RESULTS:

Device performance tends to degrade due to changes in various semiconductor electronic properties with increasing temperature. The effects of elevated temperatures and HTET on the I_d - V_d and g_m characteristics are described elsewhere [1-5]. Figure 1 shows the effect of elevated temperatures and substrate biasing (HTET) on leakage currents for a depletion MESFET. The X-axis corresponds to the voltage from drain to the substrate, considering the substrate as the fourth active terminal of the device. The Y-axis corresponds to the leakage currents from the drain ohmic contact to the substrate. If 5V is applied to the drain terminal and substrate is grounded then $V_{d-sub} = 5V$, for which, the leakage current is around 3 mA at 300°C. If +6V is applied to the substrate then $V_{d-sub} = -1V$ for which the leakage current reduces to a near-zero, negligible value. Figure 2 shows the variation of output or drain conductance (G_o) with substrate bias at 300°C for a 20x3 μm MESFET. Typical geometries tested ranged from 20x1 to 10x3 μm . From Figure 2 it is clearly seen that the +6V substrate bias produces the lowest G_o , or the highest R_o value at 300°C which is comparable or better than the room temperature R_o value. These results are well explained elsewhere [3].

HIGH FREQUENCY RESULTS:

Figure 3 shows the effect of elevated temperatures and HTET on the magnitude of the high frequency gain or forward transmission coefficient (S_{21}) of a HEMT. At 100 MHz and at an ambient temperature of 220°C the gain increased by 1.15 dB from what it was at the same temperature without using the HTET. But, as seen from Figure 3, the gain is still lower than the room temperature gain.

This is due to the fact that HTET helps to reduce the leakage currents which increases R_o , which in turn leads to a partial increase in the gain at elevated temperatures. However, HTET has no effect on the gain decrease related to the electron mobility and saturation velocity. Since HTET increases the breakdown voltage at elevated temperatures, devices can be operated at higher gate biases at elevated temperatures to achieve similar gain levels to that of room temperature on the application of the HTET. This effect is shown in Figure 4. The bottom line is the gain (S_{21}) at 210°C without HTET, the middle line is for room temperature and the line on the top is the gain at 210°C with the HTET applied and gate bias increased. From this figure it is evident that HEMTs and MESFETs can achieve equal or even higher gain than room temperature gain at 210°C with the HTET applied.

The HTET technique has been shown to stabilize the low/high frequency performance of various GaAs based devices. Experiments were performed on various devices which represent different geometries, processes, and foundries. Therefore, the results produced by the HTET are generic in nature. The HTET technique has already been applied to stabilize the performance of digital inverters upto 300° C (4). Currently research is going on to develop enhanced thermally stable Schottky and ohmic contacts and high performance digital circuits which will also be presented.

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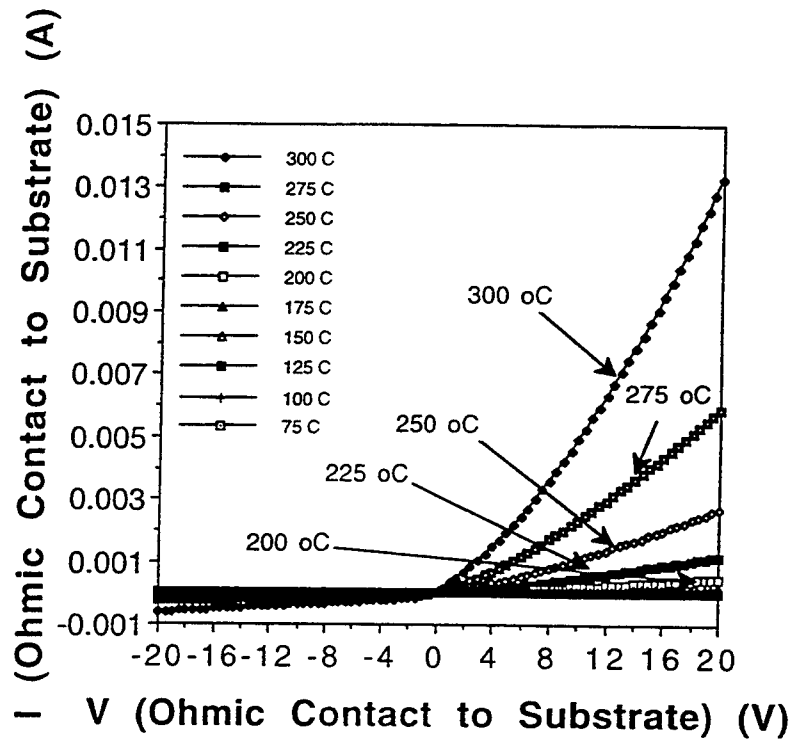


Figure 1. Drain to substrate leakage current as a function of drain to substrate voltage, note: when drain voltage is greater than the substrate voltage, appreciable leakage current is present.

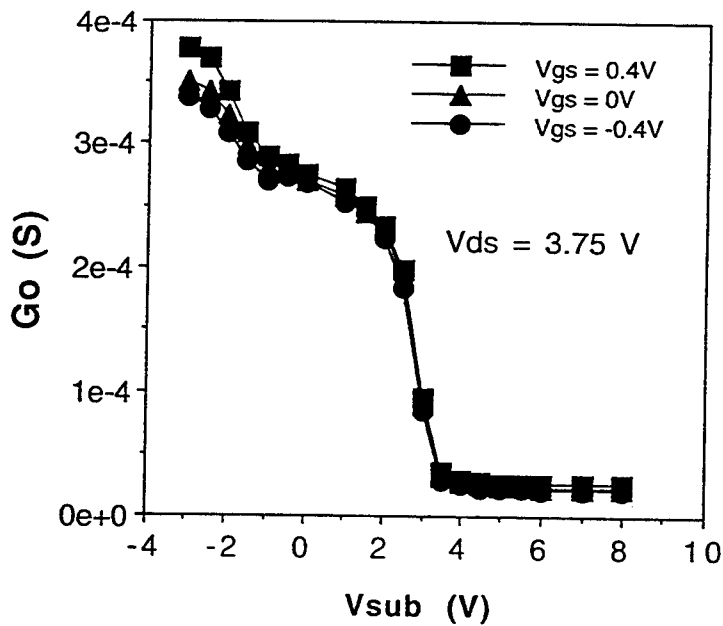


Figure 2. Output conductance (G_o) vs. substrate voltage (V_{sb}) at 300°C for $20 \times 3 \mu\text{m}$ MESFET.

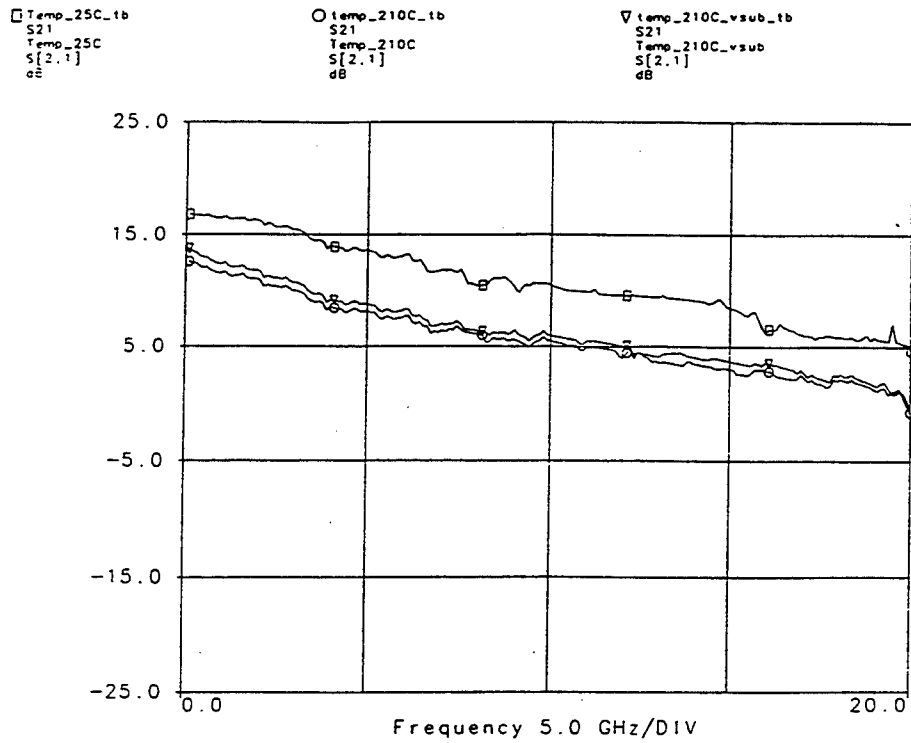


Figure 3. Effect of substrate bias and elevated temperature on the gain (S_{21}) of a HEMT.

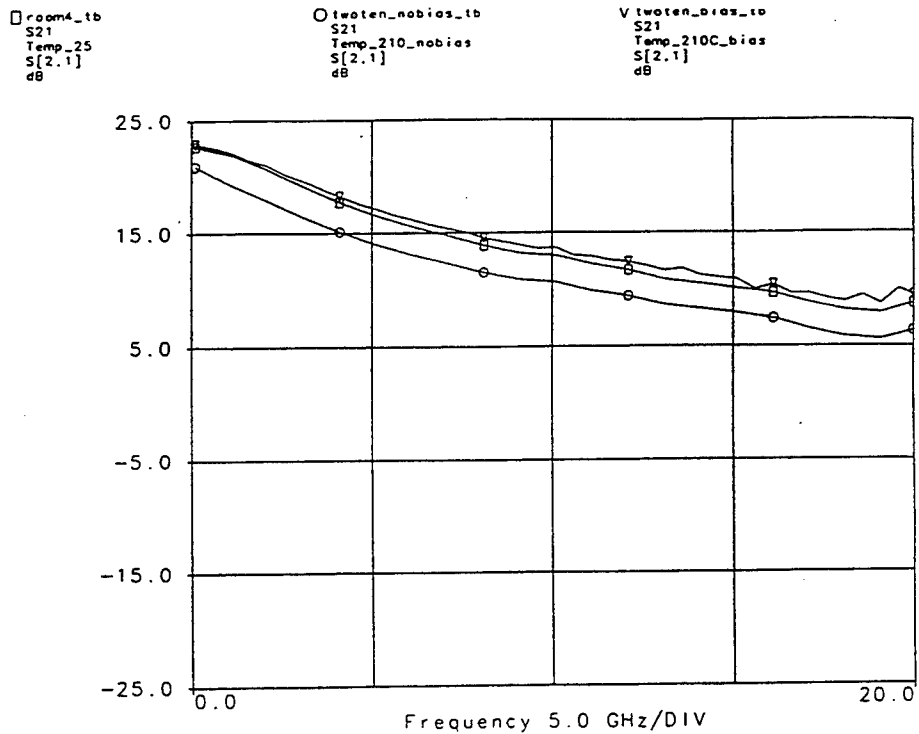


Figure 4. Effect of substrate bias and gate bias variation on the gain.

Bipolar-Mode Programming Method of EPROM/Flash EEPROM for Low Voltage Applications

Yeong-Seuk Kim and Kee-Yeol Na*

Dept. of Semiconductor Science, Chungbuk National University,
Gaeshin-Dong, Cheong-Ju, Chung-Buk, 360-763, KOREA
*Dept. of Electronics, Chungbuk National University,
Gaeshin-Dong, Cheong-Ju, Chung-Buk, 360-763, KOREA

Introduction

This paper presents a new programming method of the EPROM and flash EEPROM, which utilizes the channel bipolar transistor (n^+ -source/p-sub/ n^+ -drain). As the size of EPROM and flash EEPROM shrinks down below half-micron for high density and low voltage applications, the channel bipolar transistor action becomes more pronounced when the source is negatively biased [1]. We use this naturally formed bipolar transistor as an emitter of hot electrons to program the EPROM and flash EEPROM instead of using the channel hot electron (CHE) programming method. The advantage of this method is that the EPROM and flash EEPROM can be programmed at lower voltages as well as higher speed.

Results and Discussion

To demonstrate our proposed programming method we used a single-poly EEPROM fabricated by $0.8\mu\text{m}$ standard CMOS process [2]. Fig. 1 shows the cross section of the single-poly EEPROM. The p^+/n^+ diffused layers in the n -well are used for the control gate and the polysilicon layer is used for the floating gate. Note that the p^+ -diffused layer in the n -well increases the coupling ratio during programming. This cell can be programmed by the CHE method or our proposed method. For the CHE programming method we typically apply $V_S=0\text{V}$, $V_D=6\text{V}$, $V_{CG}=12\text{V}$. With high drain voltage the horizontal electric field near the drain junction increases and hence generates hot electrons. These hot electrons are injected into the floating gate by aided vertical electric field. For our proposed bipolar programming method we apply $V_S=-1.5\text{V}$, $V_D=4\text{V}$, $V_{CG}=10\text{V}$. In this case, channel electrons are horizontally injected by forward-biased source-channel junction and getting hot due to high electric field near the drain junction. The control gate attracts these hot electrons.

The characteristics of the channel bipolar transistor are shown in Fig. 2-5. The gummel plot of the channel bipolar transistor in Fig. 2 shows that the dc gain is very high (over 1000) at low source voltage due to the presence of the gate electrode, but reduces to 1.2 at $V_S=-1.2\text{V}$ as shown in Fig. 3. With the application of control gate voltage the MOS channel current adds to the bipolar collector (drain) current and thereby the dc gain is getting even bigger as shown in Fig. 4. Fig. 5 shows I_D-V_{DS} characteristics for $V_S=0\text{V}$ (MOS) and $V_S=-1.5\text{V}$ (MOS+bipolar).

The one-shot programming characteristics for the CHE method and bipolar method with the substrate current are shown in Fig. 6. For the CHE method the cell is programmed at $V_D\sim 5.5\text{V}$ and the substrate current is almost negligible. For our proposed bipolar method the drain current is already flowing at $V_D=0\text{V}$ due to the bipolar action and slowly increases with the increase of V_D . The cell is now programmed at $V_D\sim 3.5\text{V}$ and the substrate current is about 1mA . If we compare the power consumption during programming to achieve same V_T shift, the bipolar method consumes less power.

Programming characteristics of the cell are compared between two methods. Fig. 7 shows the V_T shift as a function of control gate voltage for two methods. It indicates that the bipolar programming method requires smaller control gate voltage compared to the CHE method. Fig. 8 shows the V_T shift as a function of drain voltage for two methods. In case of the CHE programming method the drain voltage of $\sim 5.5\text{V}$ is required

to get $V_T \sim 7.5V$, but for the bipolar programming method the drain voltage of only $\sim 3.5V$ is required to get same V_T . Fig. 9 shows the V_T shift as a function of source voltage. This figure reveals that at least source voltage of $-1.1V$ is required to program the cell above $V_T=7V$. Finally the programming speed of two methods is compared in Fig. 10. The same control gate voltage and about same drain-source voltage are applied for two methods. The programming speed for our bipolar programming method is about 10 times faster than that of the conventional CHE method.

Summary

We proposed the bipolar programming method of the EPROM and flash EEPROM replacing the CHE method. This method requires lower control gate voltage ($\sim 10V$) and lower drain voltage ($\sim 3.5V$). Also the programming speed of this method is about 10 times faster than that of the CHE method.

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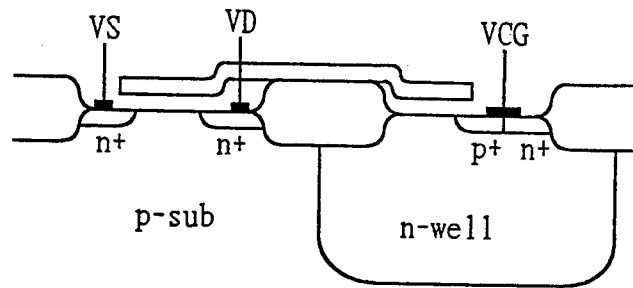


Fig. 1. Cross section of the single-poly EEPROM used to verify our proposed bipolar programming method.

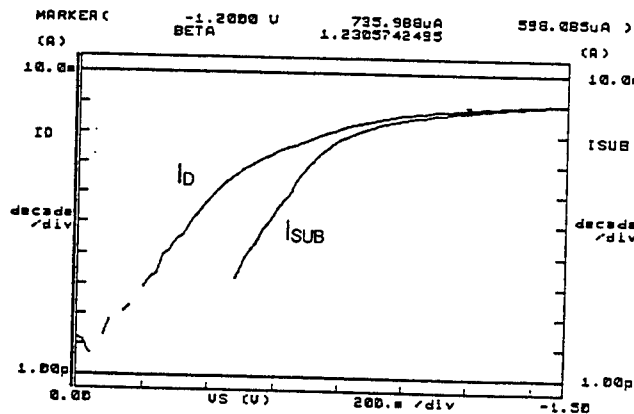


Fig. 2. Gummel Plot of the channel bipolar transistor (n^+ -source/ p -sub/ n^+ -drain). $V_D=0V$, $V_{CG}=0V$.

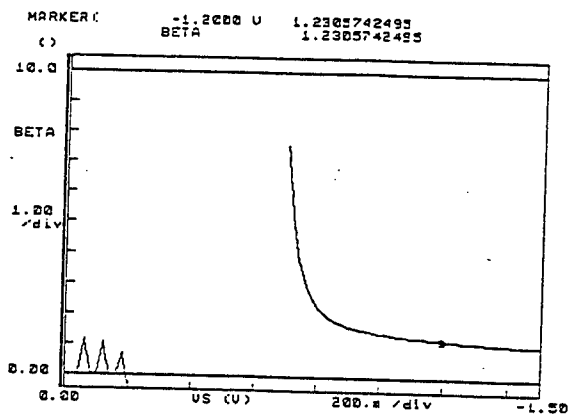


Fig. 3. DC gain of the channel bipolar transistor. $V_D=0V$, $V_{CG}=0V$.

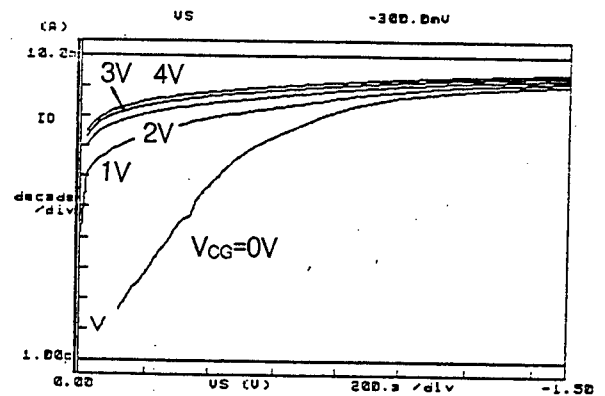


Fig. 4. Drain current of the channel bipolar transistor for various control gate voltages (0 to 4V). $V_D=0V$.

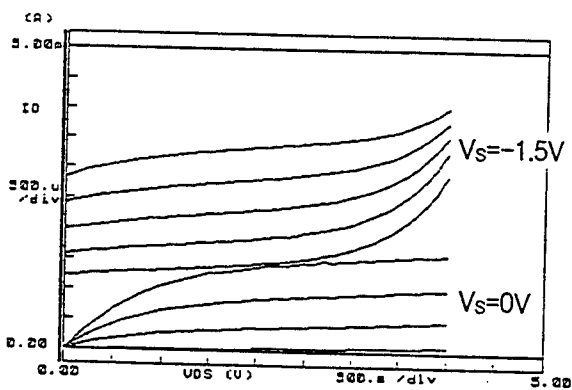


Fig. 5. I_D - V_{DS} characteristics for $V_S=0V$ and $V_S=-1.5V$. $V_{CG}=0V$ to $4V$.

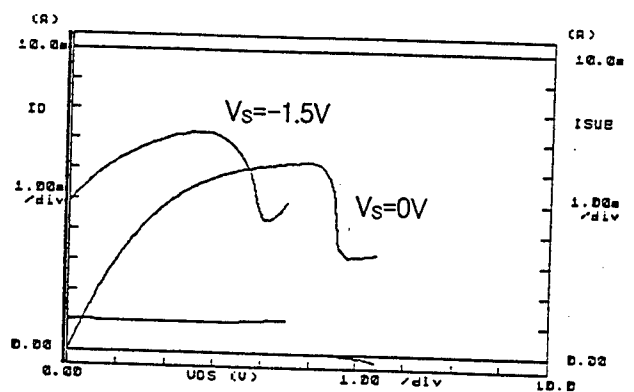


Fig. 6. One-shot programming characteristics for the CHE method ($V_S=0V$) and proposed bipolar method ($V_S=-1.5V$). $V_{CG}=12V$.

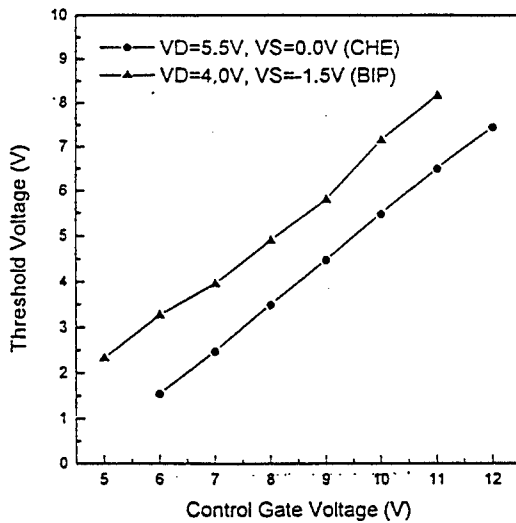


Fig. 7. Threshold voltage shift versus control gate voltages for the CHE method and bipolar method.

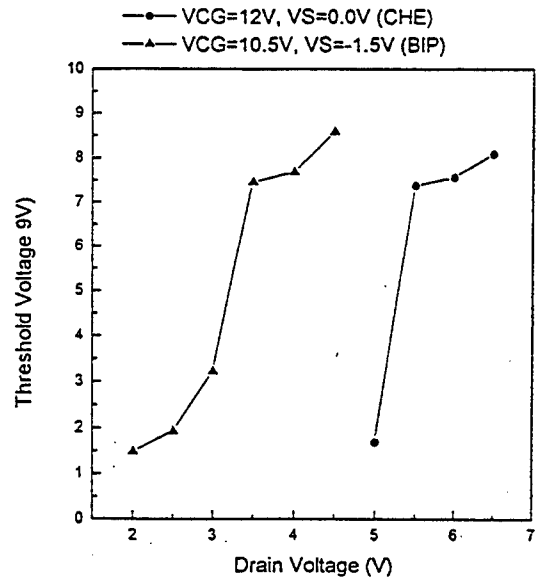


Fig. 8. Threshold voltage shift versus drain voltages for the CHE method and bipolar method.

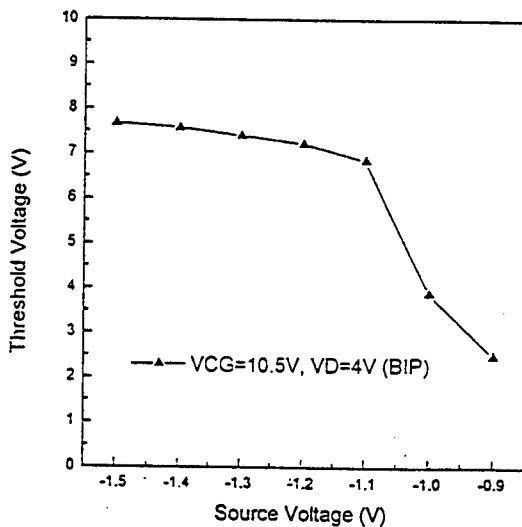


Fig. 9. Threshold voltage shift versus source voltages for bipolar method.

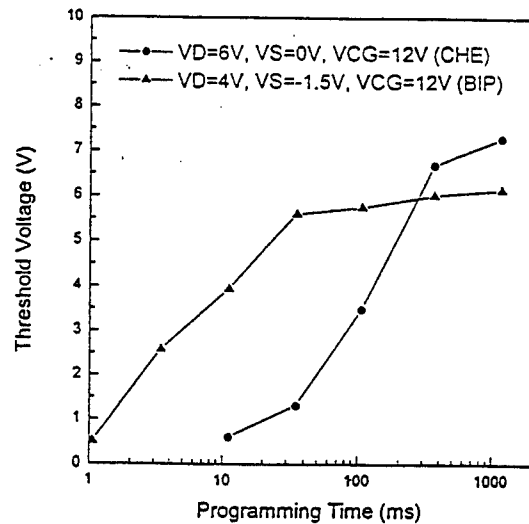


Fig. 10. Threshold voltage shift versus programming time for the CHE method and bipolar method.

New heterostructures PbS-HgCdTe and their main properties

G. Khlyap, Drogobych Pedagogical Institute,
24 Franko street, Drogobych, 293720, UKRAINE

Abstract. The results of complex investigations of new heterostructures p-PbS-p-Hg_{1-x}Cd_xTe (x=0.2; 0.4), which were obtained by low-temperature (T=540 K) MBE technology, are presented.

1. Introduction. The narrow-band semiconductors, such as lead sulphide and solid solutions HgCdTe, are good studied and their properties are presented in hundreds of various works. But the investigation of these narrow-band gap materials contacts gives possibility to examine new physical processes, which are realizing in such heterostructures, and in the same time these structures are useful for different devices modelling.

So we present at the first time the results of p-PbS-p-HgCdTe heterostructures study.

2. Experimental. p-PbS films were grown in a home-made MBE system. The growth was monitoring with reflection high energy electron diffraction. Growth rates were ranged from 0.05 - 0.1 μ m/hr and substrate temperature was about 540 K. Monocrystalline p-Hg_{1-x}Cd_xTe (x=0.2, 0.4) was used as a substrate. PbS film thickness was in range 1 - 3 μ m. The carrier concentration was determined to be about 4.5×10^{17} cm⁻³ and Hall mobility was 8000 cm²/V.s at 77 K. Surface morphology was examined by TEM and Auger-spectroscopy.

The main electrophysical (I-V and C-V) measurements were realized in temperature range 77-293 K. This study showed the heterostructures p-PbS-p-Hg_{0.8}Cd_{0.2}Te were abrupt heterojunctions [1].

The I-V characteristics of new heterostructure p-PbS-p-Hg_{0.6}Cd_{0.4}Te are plotted on Fig.1. They appear as exponential functions with two sections in all temperature range. The detail study of carrier transport processes in these heterostructures allows to suggest the following approximation of I-V curves:

$$j_1 = j_s kT / e (V_d - V_a) \exp[(eV_a + E_{ss}) / h_1 kT], \quad (1)$$

$$j_2 = j_s kT / (eV_a - E_{ss})^{1/2} \exp(eV_a / h_2 kT), \quad (2)$$

where j_s is a saturation current, e is an elemental charge, V_d is a diffusial potential, V_a is an applied voltage, E_{ss} is an energy of heterointerface electron states, h_1 and h_2 are the non-ideality factors of first and second sections of I-V-characteristic.

The C-V-measurements of this heterostructure revealed some peculiarities which are called Mott's plateau's (Fig.2). The "b"-section is existing only at 270-293 K and it's degenerating to a point at temperature decreasing.

3. Results. The band diagram is built according Anderson-Cervený-Liou model [2-3]. It's necessary

to determine the valence band ΔE_V and conduction band ΔE_C discontinuities. It is known that ΔE_V and ΔE_C are binding by the root [4]:

$$\Delta E_g = \Delta E_C + \Delta E_V. \quad (3)$$

So we determined ΔE_C from C-V-measurements according [5]. We had the set of equations for voltages V_1 and V_2 :

$$V_1 = V_a' + \Delta E_C + V_d - (4\pi Q_{ss}/\chi_2 \epsilon_2) - 2 [V_a' (\Delta E_C - 4\pi Q_{ss}/\chi_2 \epsilon_2)]^{1/2}, \quad (4)$$

$$V_2 = V_a' - V_d + \Delta E_C + (4\pi Q_{ss}/\epsilon_1)a, \quad (5)$$

where $V_a' = 2\pi e N_1 a^2 / \epsilon_1$ (N_1 is carrier concentration of lead sulphide film, a is a thickness and ϵ_1 is dielectrical constant of PbS), V_d is diffusial potential, $Q_{ss} = e N_{ss}$, N_{ss} is charge defects concentration, $\chi_2 = (4\pi e^2 N_2 / \epsilon_2 kT)^{1/2}$, $V_a' = 2\pi e N_1 a^2 / \epsilon_1$, and N_2 , ϵ_2 are carrier concentration and dielectrical constant of $\text{Hg}_{0.6}\text{Cd}_{0.4}\text{Te}$. So the value of ΔE_C is consisting of 110 meV, $T = 293$ K.

The current mechanism in these heterostructures is following: tunneling-recombination current is dominated at forward voltage 10-500 meV and diffusion current is dominated at the increasing of forward voltage up to 1.5 V. We suggest that this current mechanism is realizing due to presence of sufficient number of heterointerface electron states with energy $E_{ss} = 254$ meV. This value was calculated on C-V-measurements basis.

The full heterointerface electron states' charge Q_{ss} is a sum of the charges $Q_{ss}(1)$ and $Q_{ss}(2)$ which are arising on both sides of heterojunction:

$$Q_{ss} = Q_{ss}(1) + Q_{ss}(2), \quad (6)$$

the capacitance C_{ss} of space charge region is determined as $C_{ss} = C_{ss}(1) + C_{ss}(2)$, (7)

$$\text{where } C_{ss}^i = -(e/kT) \partial Q_{ss}^i / \partial y_{ss}, \quad i=1,2; \quad (8)$$

$$y_{ss} = E_{ss}/kT, \quad Q_{ss}^i = 2en_0^i L_D^i (p_i/n_0^i)^{-1/2} \exp(y_{ss}/2), \quad (9)$$

here n_0 is an intrinsic carrier concentration of both heterocomponents, L_D is Debay length, p_i is doping

impurity concentration. After the mathematical transformations we found E_{ss} is determined by the expression

$$(10): \quad E_{ss} = 2(kT/e) \ln \frac{0.5(kT/e) (P_2/n_{i2})^{-1/2} C_{ss} - Q_{ss}}{2e[(P_2/n_{i2})^{-1/2} - (P_1/n_{i1})^{-1/2} n_{i1} L_{D1}]} \quad (10)$$

The band diagram of p-PbS-p- $\text{Hg}_{0.6}\text{Cd}_{0.4}\text{Te}$ hetero-

structure is plotted in Fig.3.

These results showed that the full electron states charge on heterointerface is stored during 3 years without significant alterations and these heterostructures would be a base for operative memory devices manufacturing.

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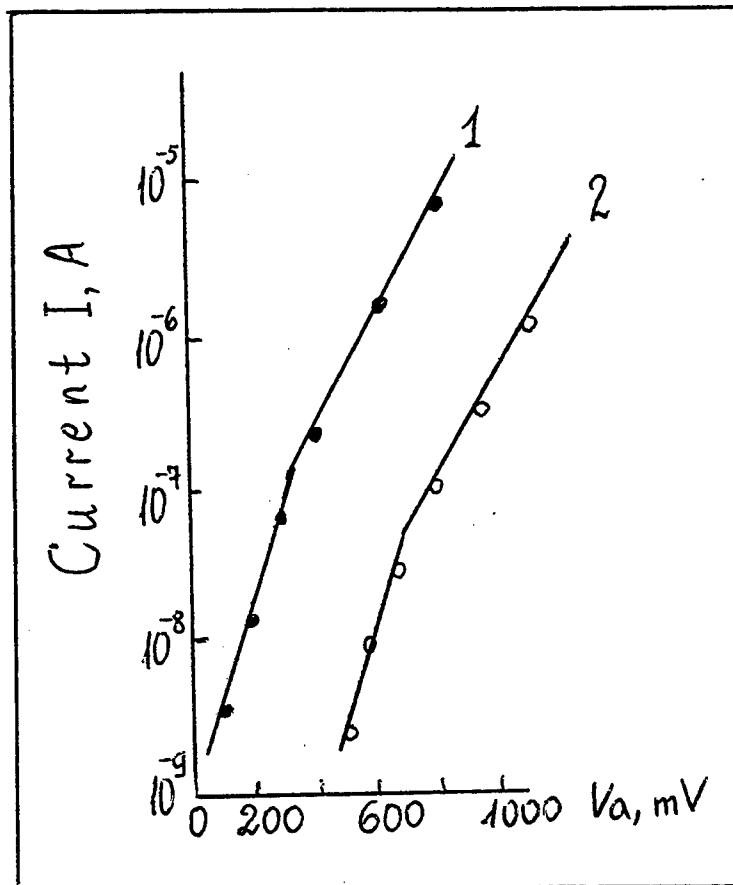


Fig.1. I-V-characteristics of heterostructure p-PbS-p-Hg_{0.6}Cd_{0.4}Te. T,K: 1 - 77, 2 - 293.

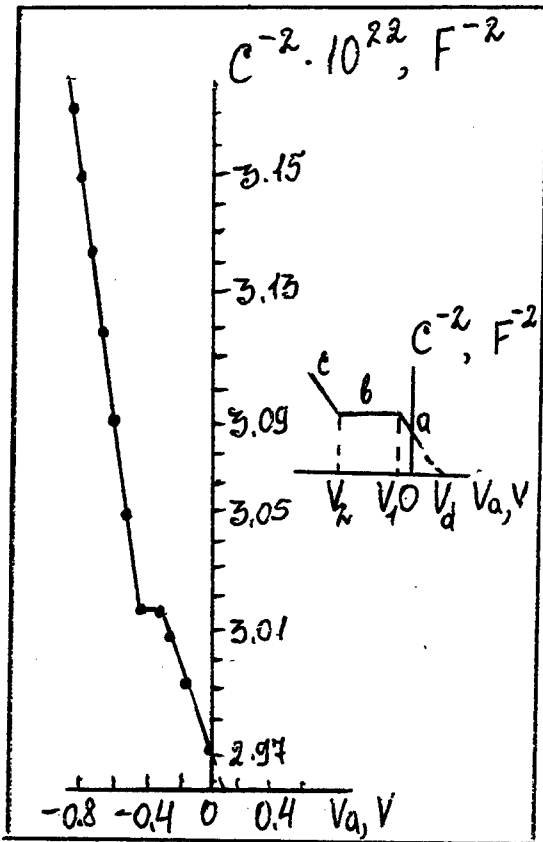
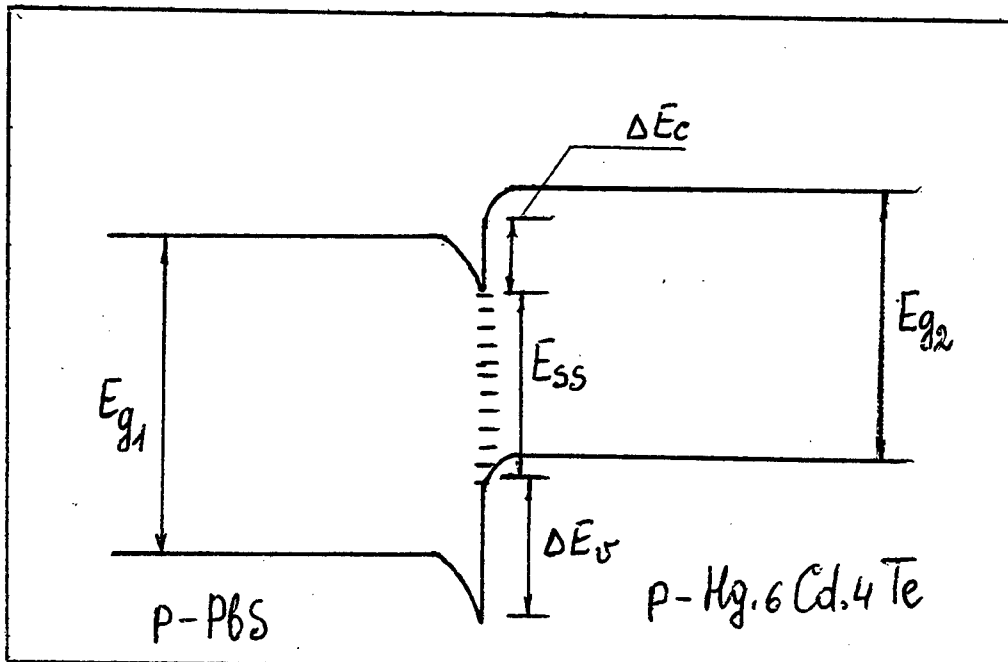


Fig. 2. a) The theoretical C-V-characteristic of the isotype p-p-heterojunction 5. The inclines of "a" and "b" sections are determined by free carriers concentration of PbS layer and the narrow-band substrate, respectively. V_1 voltage is corresponding to appearance of Mott plateau on C-V-characteristic. b) C-V-characteristic of heterostructure p-PbS-p-Hg_{0.6}Cd_{0.4}Te, $T = 293$ K, $f = 1$ MHz.

Fig. 3. The band diagram of heterostructure p-PbS-p-Hg_{0.6}Cd_{0.4}Te. $T = 293$ K, $V_a = 0$.



FAST IMPACT IONIZATION FRONTS IN LARGE AREA DIODE STRUCTURES:
AN ANALYTICAL APPROACH TO THE STABILITY AND 3D DYNAMICS

A. M. Minarsky, P. B. Rodin

Department of Power Electronics, Ioffe Physical Technical
Institute, Politechnicheskaya 26, St. Petersburg, 194021, Russia
E-mail: agor@pulse.pti.spb.su, FAX: (812)-247-10-17

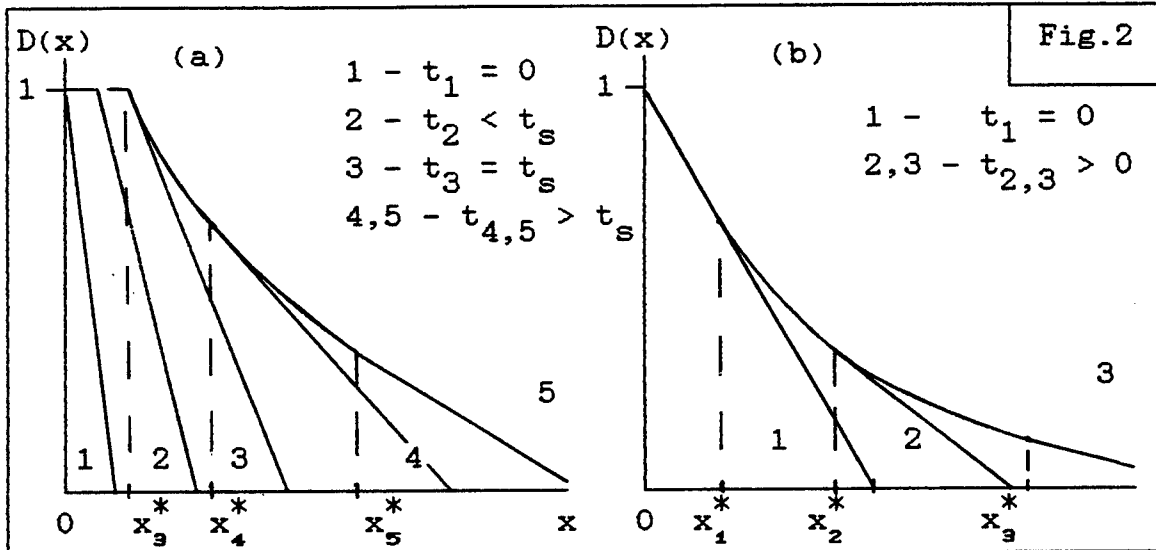
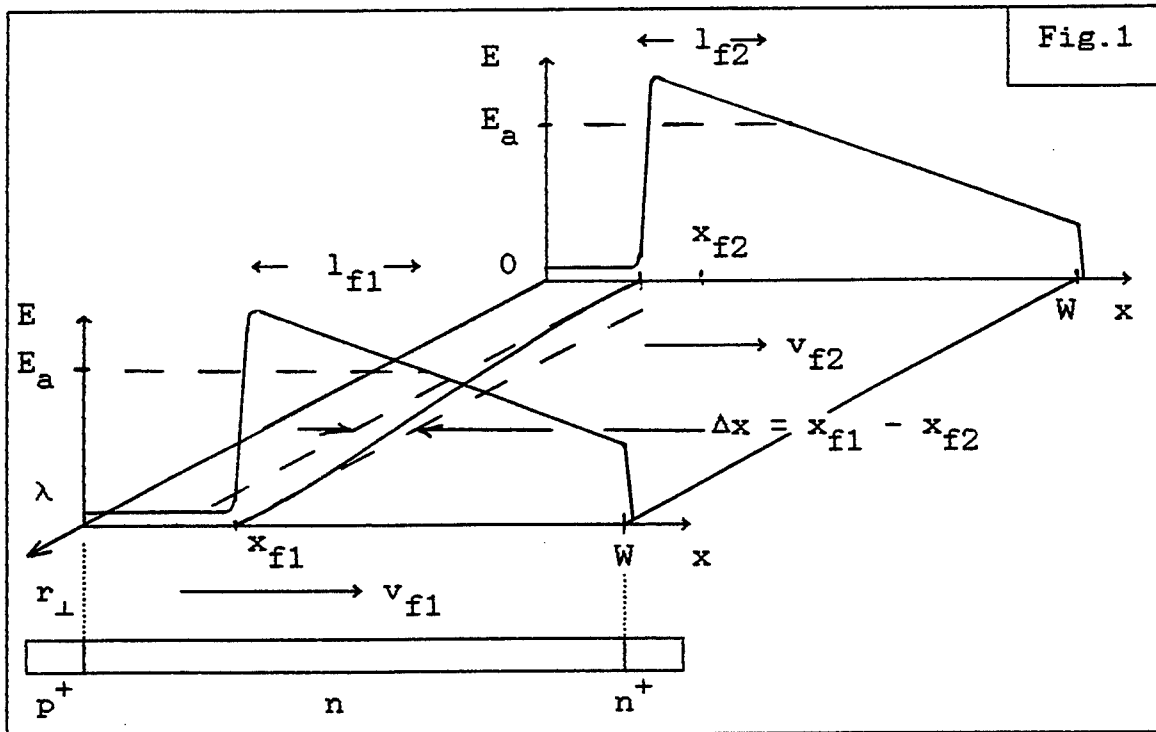
1. Introduction. The propagation of superfast impact ionization front (IIF, $v_f > v_s$, v_s - the saturation drift velocity) is the fastest of presently known mechanisms for diode switching. This phenomenon being originally observed for low voltage Ge TRAPATT diodes [1] also occurs in high voltage Si [2] and GaAs structures [3]. It has formed the basis of powerful nanosecond diode peakers performance [4] and appears to have considerable promise in laser applications [5]. For large area structures the still unsolved problem of IIF transverse stability and realistic 3D dynamics takes on major importance. In the present work we develop an analytical approach to the stability problem providing as well the qualitative description of nonhomogeneous dynamics of large area IIF.

2. Transverse stability. The stability analysis is based on the following front propagation model [6,7]

$$(1,2) \quad \dot{x} = \frac{1}{q N_d} J[u, x(r_{\perp})], \quad u = V - \left[q N_d R S \langle x \rangle \right].$$

Here u is the voltage applied to the diode, S , V , R denote the area of the structure, e.m.f. of the power source and external load respectively; angle brackets denote the average value over the device area.

According to (1,2) the growth of long-wavelength fluctuations ($\lambda > W$, fig.1) is an inherent feature of planar IIF dynamics [8]: as the front length l_f increases in the the leading part of the wave but reduces in the lagging part the difference in velocities v_1 and v_2 arises and lead to the



further development of transversal fluctuation. In actual practice IIF behavior is determined by the relation between the characteristic time of instability τ_c which depends dramatically on specific field profile $E(x)$ [6,8] and the total time of IIF passage $\tau \sim W/v_f$. Low fluctuation increments take place if $E_a \gg E(W)$. In the contrary, when $E(W) \sim E_a$ the wave stratificates rapidly. The waves in long base diodes ($W > [2e\epsilon/u]^{1/2}$) are expected to be quasi stable.

The instability eventually leads to the formation of

several local switching channels (LSC) or even a single one. The minimum transverse dimension of LSC and current per channel can be estimated as

$$(3,4) \quad r_{\min} \sim (W - x_a) \sim W, \quad J_{\max} = \left[2qN\nu_s \right] \pi \left[u/E_a \right]^2$$

3. Nonhomogeneous dynamics. For the purpose of describing nonhomogeneous wave dynamics we treat the problem in terms of the front area distribution function over the longitudinal coordinate $D(x,t)$: $D(x',t)$ is a part of device area where $x_f \gg x'$. According to (1,2) for the linearized dependence $j(u,x)$ the evolution of the distribution is ruled by the following equations [6,7]

$$(5) \quad \left. \begin{aligned} \partial_t D(x,t) + \lambda (x - x^*) \partial_x D(x,t) &= 0, & x > x^*, \\ \partial_t D(x,t) &= 0, & x < x^*, \end{aligned} \right\} x^* > 0.$$

$$x^* = -\frac{\nu}{\lambda} + \varepsilon \int_{x^*}^W D(x,t) dx, \quad x > 0.$$

$$(6) \quad \partial_t D(x,t) + \lambda \left[\frac{\nu}{\lambda(1+\varepsilon)} + x - \frac{\varepsilon}{1+\varepsilon} \langle x \rangle \right] \partial_x D(x,t) = 0, \quad x^* = 0.$$

Coefficients $\lambda, \varepsilon, \nu$ are determined by structure and external circuit parameters. Eqns (5,6) have been solved analytically for all possible modes of the IIF propagation and arbitrary initial distribution $D(x,0)$ [6,7]. The qualitative pictures of IIF dynamics for small and large initial dispersion of its position are presented in Fig.2 (cases a and b respectively, $D(x,0)$ is assumed to be linear). Behind the freezing front (FF) $x = x^*$ there is no wave propagation, t_s corresponds to the origin of the FF.

4. Conclusion. The instability of the large area IIF is due to the long-wavelength mechanism which is caused by the interaction of front regions through the external circuit. The front propagation is accompanied by exponentially fast growth of initial dispersion of its position which may lead to the termination of the propagation process on the part of the device area. The degree of switching inhomogeneity decreases with load resistance, device area, impact ionization coefficients and threshold field increase and

applied voltage decreases.

The short wave length enhancement of electrical field at nonuniformities of small radius becomes significant on the stage of LSC formation and limits reducing of its radius at the value close to the n-base thickness W . As $r_{LSC} \sim W$ the field enhancement near the LSC head is insignificant and so the streamer discharge mechanism does not make essential contribution to the LSC propagation. Although the LSC and streamer discharge are similar in appearance, the mechanism of LSC propagation remains mostly the same as for planar IIF.

The present consideration justifies the empirical reliability criterion [9] of Si diode peakers performance which demands the existence of a neutral undepleted region in the n-base when the wave starts: $W > [2\epsilon\epsilon_0/u]^{1/2}$. It also agrees with the results of direct observation of local [10] and homogeneous [5] switching of GaAs diodes.

Acknowledgements. We are grateful to M.E.Levinstein who has turned our attention to this problem, and A.V.Gorbatyuk, I.V.Grekhov and A.F.Kardo-Sysoev for their useful discussions.

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Spin-Polarized Electron Photocathodes Based on $\text{In}_x\text{Ga}_{1-x}\text{P} - \text{GaAs}$ Superlattices

Arsen Subashiev

Department of Experimental Physics, State Technical University,
195251 St.Petersburg, Russia

Major efforts have recently been devoted to the investigations of new sources of highly polarized electrons. Spin-polarized electron beams have numerous applications in modern physics¹. In solid-state physics the studies of the magnetic properties of the subatomic layers and nanosandwiches has become possible². In atomic physics the experiments on the spin-dependent inelastic scattering of electrons with atoms come now to be an area of active studies³. In high energy physics the observation of the parity violation in the inelastic electron scattering⁴ and the Weinberg angle measurements⁵ show potential role of the polarized electron beams.

In the experiments using polarized electrons to ensure high sensitivities a source which gives as large an electron current as possible and as high a polarization as possible is required. During last three years two efficient ways to obtain very high polarization were experimentally demonstrated. One of them is to employ semiconductor structures activated to negative-electron-affinity with strained thin films when the lattice mismatch generates substantial stress in the overlayer. The stress lifts the orbital degeneracy of the $P_{3/2}$ multiplet at the valence band maximum. A lattice mismatch of typically 1% results in a splitting of the heavy and light valence band states by about 0.05 eV. The optical excitation of a single band transition by circularly polarized light leads potentially to 100% polarization of the emitted electrons. With GaAs strained overlayers on $\text{Ga} - \text{P}_x\text{As}_{1-x}$ substrates polarization up to $P = 90\%$ has been achieved^{6, 7}. A workable alternatives to the strained layer polarized electron sources (PES) make short-period $(\text{Al}, \text{Ga})\text{As} - \text{GaAs}$ superlattices (SL) in which the splitting of the valence band levels is imposed by the hole confinement in quantum wells. Then, further enhancement of the polarization can be obtained by using strained-layer SL-based PES⁸.

Besides the polarization, the main problem remains to obtain high quantum efficiency(QE). The QE limitation in the strained layer PES comes from two physical reasons. First, the lattice strain in the strained layer PES can be maintained only in sufficiently thin layers. Though the calculated critical thickness is as small as 12 nm, the layers of 150 nm thickness have usually enough residual strain for PES fabrication. Since this dimension is still far less than the escape depth of the electrons from the bulk negative electron affinity photocathodes - e.g. CsO-activated GaAs - the quantum yield is significantly reduced. Second, the optical excitation of a single band transition near the edge of the band gap where the density of states is very low results in small absorption in the active layer.

In the SL-based PES the thickness of the active layer is not restricted by critical

thickness. Nevertheless the electrons escape depth is rather small, however, as a result of the inevitable necessity for the electrons to tunnel through the SL barriers. This leads to electron depolarization and losses during their diffusion to the surface. As a result the quantum yield is still less than 0.15 % for the polarization of about 70 %⁸.

Recently semiconductor alloys exhibiting spontaneous superlattice (SSL) ordering were proposed as possible candidates for PES⁹. Most experimental and theoretical studies of SSL are reported for $\text{In}_x\text{Ga}_{1-x}\text{P}$ alloys with $x \approx 0.5$. These alloys have rather low electron mobility and the largest ordering induced valence band splitting observed by now is less than 40 meV which does not seem to be sufficient for effective PES.

The purpose of this paper is to suggest the use of $\text{In}_x\text{Ga}_{1-x}\text{P} - \text{Al}_y\text{Ga}_{1-y}\text{As}$ superlattices to achieve small height of the electron barriers and large valence band splitting appropriate for the effective polarized electron emission. Good quality $\text{In}_x\text{Ga}_{1-x}\text{P} - \text{GaAs}$ quantum well structures and SL have already been obtained by gas source and metalorganic molecular beam epitaxy¹⁰.

The main advantage of the SL comes from the band line-up between the semiconductor layers of SL. In the case of (Ga, Al)As – GaAs the ratio of the conduction-band offset ΔE_c to the valence-band offset ΔE_v is $\Delta E_c/\Delta E_v \approx 2$, while in the $\text{In}_x\text{Ga}_{1-x}\text{P} - \text{GaAs}$ heterostructures the value is close to 0.4¹⁰. As a result of the conduction-band line up, the barriers for the electrons in the short-period SL are transparent and the along-the axis electron effective mass is small. At the same time sufficiently large hole-miniband splitting can be obtained. The small addition of Al to the well composition is to make the band structure less sensitive to the parameters of the structure. Finally, as a result of larger valence band splitting the optical absorption coefficient can be large enough in this case.

The parameters of the SL-based PES can be optimized treating the superlattice as an artificial bulk material, and applying for the PES analysis a diffusion model.

For the spin asymmetry experiment applications the efficiency of the PES is measured by the product PI^2 where I is emitted current. The analysis of the limitations of the excitation power due to nonlinearity of the emission and the surface degradation shows that quantum yield is appropriate quantity for PES characterisation. In the framework of the diffusion model quantum yield Y of the semiinfinite layer is given by

$Y = B(1 - R)\alpha L/(1 + \alpha L)$, where B is probability of the electron emission from the band bending region into vacuum, α is absorption coefficient, L is diffusion length $L = \sqrt{D\tau}$, τ is the electron lifetime and D is diffusion coefficient for the electrons, R is the light reflection coefficient.

The emitted electron polarization can be expressed as follows

$$P = P_0(\hbar\omega) \frac{(1 + \alpha L)}{(1 + \tau/\tau_s)^{1/2} [(1 + \tau/\tau_s)^{1/2} + \alpha L]}, \quad (1)$$

Eq.(1) is obtained in the assumption of the absence of the electron depolarization at the surface. In Eq.(1) $P_0(\hbar\omega)$ is the electron polarization at the moment of the excitation, τ_s is the spin relaxation time.

The estimates of Y and P are based on the electronic band structure, effective mass and absorption coefficient calculations. The SL electron and hole subband spectrum has been calculated using the envelope-function approximation, in the framework of the Kane model including the conduction band Γ_6 , and the states of light and heavy holes of the valence band Γ_8 ¹¹. The conduction and valence band offsets were chosen as follows. The photorefectance experiments on the multiple quantum well structures with GaAs wells separated by $\text{In}_x\text{Ga}_{1-x}\text{P}$ barriers yielded a value for the conduction band offset $\Delta E_c = 130$ meV for $x=0.55$ at low temperatures. The results of the interpolation procedure proposed by Krijn¹² give values which are very close to experimental values for InGaAsP and InAlGaAs systems for both low and room temperatures. Therefore we follow the¹² interpolation scheme.

In Fig 1. the assumed relative energy positions of the band edges of the $\text{In}_x\text{Ga}_{1-x}\text{P} - \text{GaAs}$ and $\text{In}_x\text{Ga}_{1-x}\text{P} - \text{Al}_y\text{Ga}_{1-y}\text{As}$ for the matched SL are shown. The effects of the internal strain on the valence band offsets are incorporated by assuming that the center of the strain-split valence bands coincides with unstrained valence bands.

The dependence of the positions of the miniband edges for the SL with the well material thickness d_1 and barrier material thickness d_2 at $Q = 0$ and at $Q = \pi/d$, where Q is the momentum component along the SL axis and $d = d_1 + d_2$ was calculated as a function of well thickness for $y = 0$ and for $y = 0.2$. A particularly important feature of the energy band structure is large energy dispersion of the electron subband along the growth axis. This large energy dispersion occurs because the SL barriers are low and transparent. The other important feature is large distance between the upper hole minibands, which provide high electron polarization and the single band absorption. The transport properties of the electrons were calculated using the electron effective masses. The masses were determined both from the energy dispersion curves and using analytical expressions¹³ and were found to be nearly isotropic: $m_{\parallel}^*/m = 0.095, m_{\perp}^*/m = 0.075$, for SL with $y = 0$ and $m_{\parallel}^*/m = 0.117, m_{\perp}^*/m = 0.090$, for SL with $y = 0.2$. Since the electron mobility is predicted to be as large as in the bulk $\text{In}_x\text{Ga}_{1-x}\text{P}$ composition, the QE is predicted to be the same as from the bulk $\text{In}_x\text{Ga}_{1-x}\text{P}$ at the equal absorption excitation energy. The absorption coefficient of the SL was calculated in the region where only the first heavy-hole to the first conduction band transitions contribute to it using optical matrix elements and the effective masses of the SL. The calculations demonstrate that close to the threshold the absorption is larger than in the strained layer PES or superlattices on the base of GaAs as a result of wider band gap (all the effective masses are larger) and larger subband splitting. Then, the electron depolarization in the considered SL is predicted to be smaller than in $\text{Al}_y\text{Ga}_{1-y}\text{As}$ SL, also as a result of smaller barriers for the electrons.

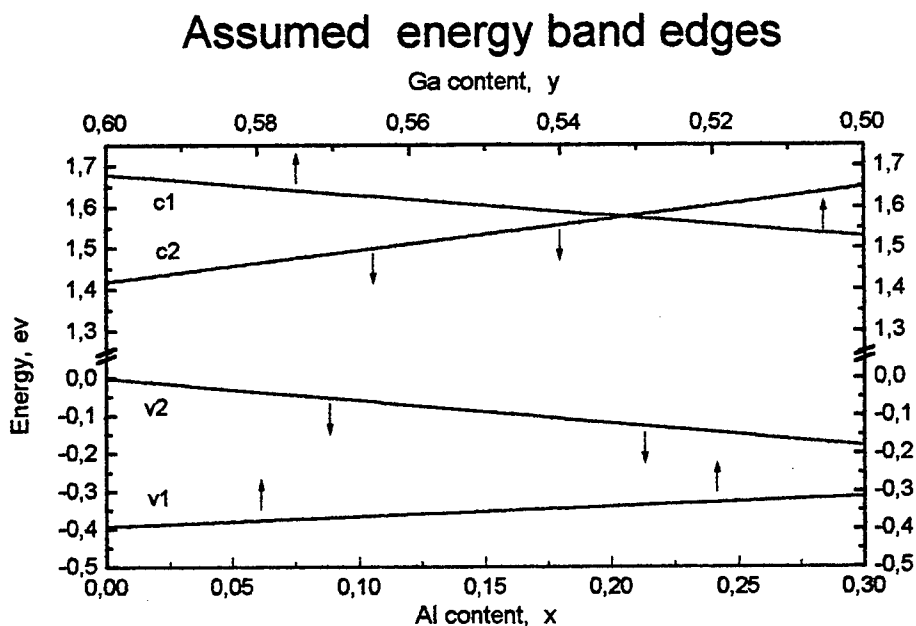
Note that the thickness of the SL have no severe limitations since the layer mismatch is small. Finally, the $\text{In}_x\text{Ga}_{1-x}\text{P}$ surface is reported to be better activated than $\text{Al}_y\text{Ga}_{1-y}\text{As}$ that imposes the choice of the last layer.

Overall, we predict that the electronic and the optical properties of $\text{In}_x\text{Ga}_{1-x}\text{P} - \text{Al}_y\text{Ga}_{1-y}\text{As}$ strained layer superlattices with $x \approx 0.5 - 0.6$ and $y \approx 0 - 0.2$ are expected to have superior properties for spin-polarized electron emission applications than commonly used stressed thin films and AlGaAs -based superlattices.

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CHAOTIC OSCILLATIONS EMISSION BY NDC SEMICONDUCTOR DEVICES G.S.Simin*, A.L.Fradkov**, S.A.Shadchin***

* GIRICOND Sci.-Res. Institute, St.-Petersburg, Russia

**Institute for Problems of Mechanical Engineering, Academy of Sci. of Russia
St.-Petersburg, Russia

***Physico-Technical Lyceum, St.-Petersburg, Russia

The possibility of chaotic oscillations' emission using semiconductor devices with Negative Differential Conductivity (NDC) is demonstrated by modeling the circuits containing Tunnel Diodes and Gunn Diodes - some of the most important high-speed NDC devices. A simple rule for evaluation the circuit parameters providing chaotic oscillations with N- or S-type NDC devices has been suggested. The results obtained are in actual practice important for the generation of high-frequency and microwave chaotic oscillations.

INTRODUCTION

Chaotic oscillations [1, 2] have attracted much attention in recent years. That was caused not only by a purely scientific view of this uncommon dynamic problem [3], but also by extremely promising practical applications such as secure communication systems, radars, image recognition, sound synthesis, artificial memory [4], brain investigations [5], medicine [6] and so on. Hundreds of publications concerning both theoretical and experimental treatment of electrical chaotic oscillations appeared during the last 10 - 15 years [7,8].

Nonlinearity is of basic importance for chaotic oscillations. In theoretical studies the nonlinear terms appear in differential equations describing the system; under experimental conditions it is simulated by electric circuits with operational amplifiers, diodes, transistors, and R, L, C components.

Analyzing numerous papers devoted to chaotic oscillation investigations, one can see that in most cases (excluding systems with explicit delays) the necessary nonlinearity is equivalent to incorporating an element with NDC into the oscillatory circuit. In some cases the necessity of NDC element is pointed out explicitly, in others it follows from the analysis of the circuit equations.

On the other hand it is well known that the effect of NDC is an essential feature of a large variety of semiconductor devices, many of them exhibiting the NDC properties up to very high frequencies, including microwaves, and in large intervals of the voltage, current and temperature. That is why it seems very interesting and important to prove the possibility and to study the conditions of chaotic oscillations excitation in circuits which include semiconductor devices with NDC, mainly those working on high frequencies. Chaotic relaxation oscillations in a circuit with two tunnel diodes were studied in [9]. Here more general approach is proposed.

RESULTS AND DISCUSSION

The N-type elements were investigated in the circuit shown in Fig.1. This circuit can be easily implemented as a printed microwave IC. Besides, it incorporates the diode's equivalent circuit containing parallel junction capacitance. The non-linearity is represented by specific $I(U)$ curve of active element N. With the use of dimensionless variables $z=\omega_2 t$; $\omega_2=1/\sqrt{LC_2}$; $q=R/\omega_2 L$; $C_{21}=C_2/C_1$, the circuit can be described by the following system of equations:

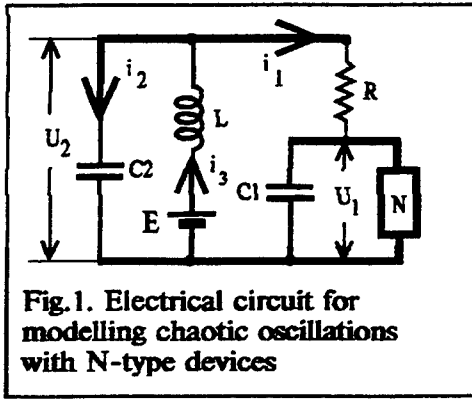


Fig. 1. Electrical circuit for modelling chaotic oscillations with N-type devices

$$\frac{\partial U_1}{\partial z} = C_{21} [U_2 - U_1 - Ri(U_1)] / q; \quad (1)$$

$$\frac{\partial U_2}{\partial z} = (U_1 - U_2 + Ri_3) / q; \quad (2)$$

$$\frac{\partial i_3}{\partial z} = q(E - U_2) / R; \quad (3)$$

The system (1-3) was studied with different $i(U)$ functions representing various semiconductor devices with NDC.

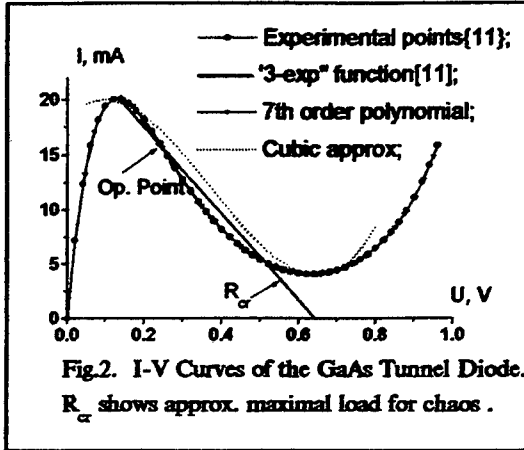


Fig. 2. I-V Curves of the GaAs Tunnel Diode. R_{cr} shows approx. maximal load for chaos.

The best known and most widespread example of the microwave NDC devices is a tunnel diode. Experimental $I(U)$ curve of a typical GaAs tunnel diode [11] is shown in Fig. 2. When studying the tunnel diode microwave generators, the diode's $I(U)$ curve is usually approximated by cubic polynomial function. In this case the system (1-3) can be reduced to one described in [10] where chaotic oscillations were observed. However, such an approximation describes the tunnel diode's $I(U)$ curve only qualitatively, as can be seen from Fig. 2. So it cannot prove the

possibility of chaotic oscillations with a real device, because the nonlinear behavior of the circuit is extremely sensitive to specific shape of nonlinear $I(U)$ curve. That is why we investigated the circuit with a tunnel diode using more accurate approximations. Fig. 2 shows "classical" 3-exponential tunnel diode $I(U)$ curve [11] together with the 7th order polynomial approximation. The behavior of the system (1-3) was studied for the above mentioned approximations (and for some others as well) and we have found that the results do not depend significantly on a specific method of describing the experimental curve.

Several operating regimes have been found which allow the chaotic oscillations with a tunnel diode. Fig. 3 shows phase diagram (a) and spectrum (b) for one corresponding to operating point $U_0=0.24$ B, $I_0=18$ mA and the circuit parameters $C_{21}=9.0$; $q=3.7$; $R=0.026$ k. The presence of chaotic dynamics was verified visually from the attractor form in the phase diagram. Since the presence of continuous signal spectrum is also a good indirect criterion of chaoticity [1], we computed the voltage spectrum in all cases. As it is clearly seen from Fig. 3, b the oscillations have a typical continuous spectrum as opposed to a discrete spectrum of periodic oscillations.

The problem of locating the set of parameters corresponding to a chaotic regime is one of the most significant and difficult problems in chaos investigations. As applied to semiconductor devices this problem becomes still more complicated due to a large scatter of device parameters. For the case of smooth $I(U)$ curves peculiar to most NDC devices we have found a simple empirical rule allowing to find the parameters of the chaotic regime. Let the value of the device differential resistance at the operating point be $-R_{d0}$. Let the load line R_{cr} (Fig. 2) intersect the device $I(U)$ curve in one (or both) extreme points. Then the circuit load R providing chaotic oscillations falls within the approximate range of

$$R_{d0} < R < R_{cr}; \quad (4)$$

Besides, other circuit parameters must meet an approximate condition

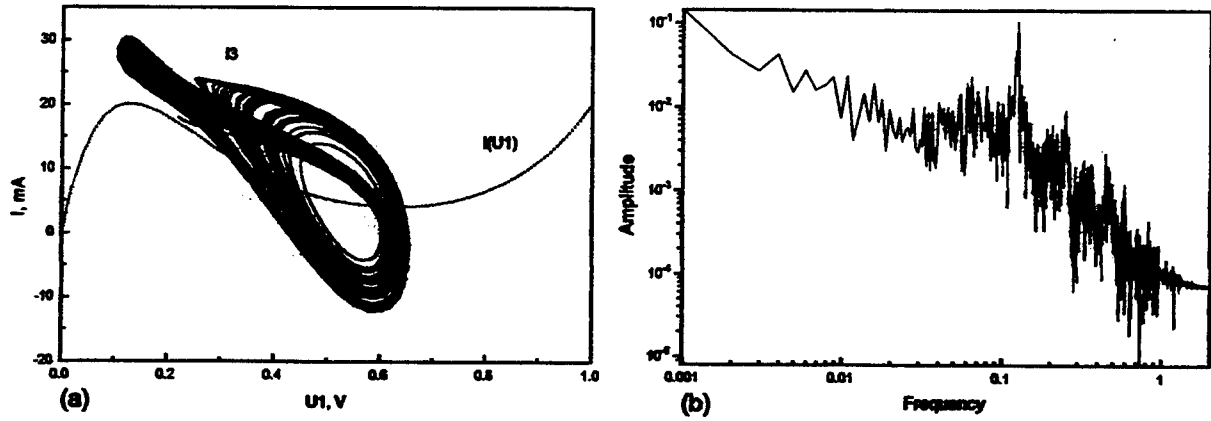


Fig. 3. Chaotic oscillations in a circuit with the GaAs tunnel diode.

$E=0.71$ V; $R=0.026$ k; $q=3.7$; $C_{21}=9.1$;

(a) - phase diagram; (b) - $U_1(z)$ spectrum.

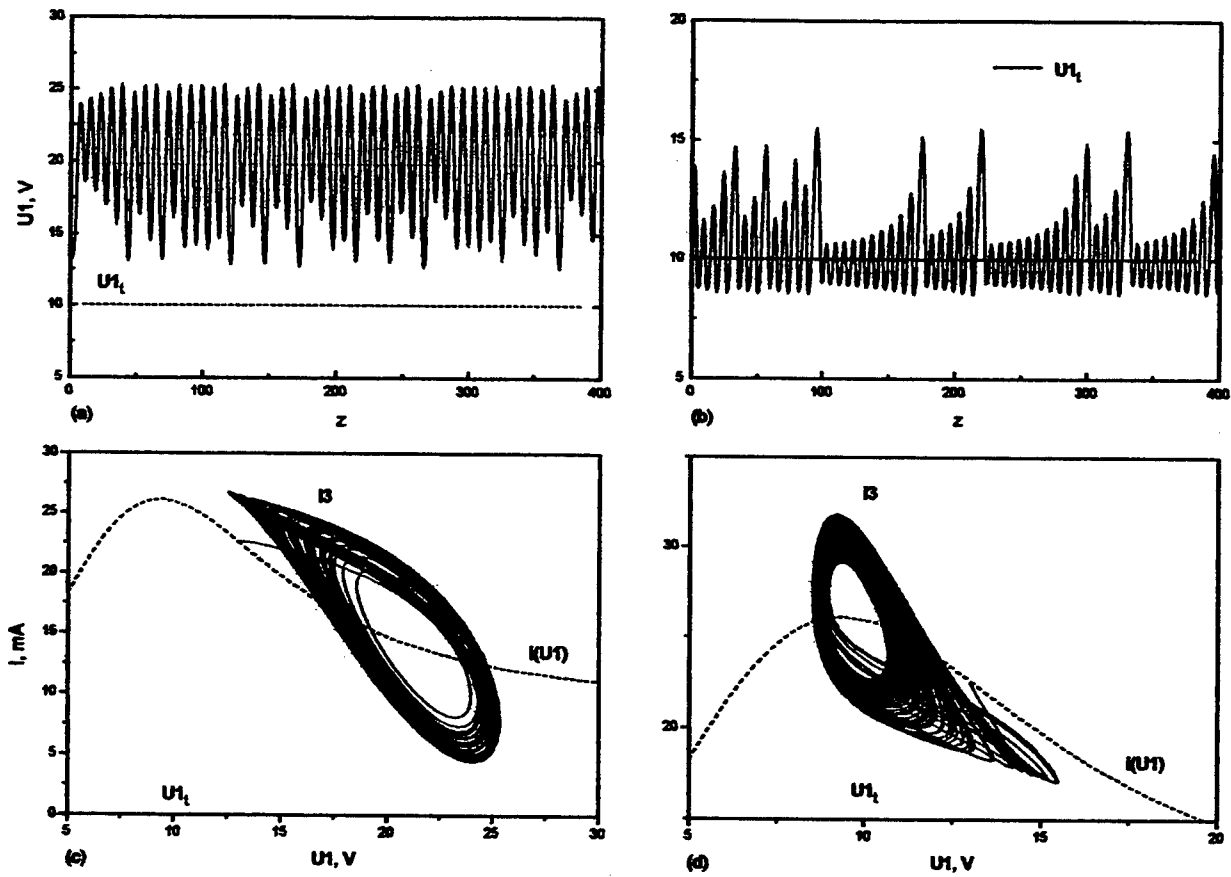


Fig. 4. Chaotic oscillations in a circuit with the Gunn diode.

(a,b) - waveforms; (c,d) - phase diagrams;

(a,c): $E=35$ V; $R=0.97$ k; $q=2.75$; $C_{21}=5.1$;

(b,d): $E=32.3$ V; $R=0.87$ k; $q=3.70$; $C_{21}=8.9$;

$$C_{21}R \geq q^2 R_{d0} \sqrt{1 - \frac{\omega^2}{\omega_2^2}}, \quad (5)$$

ω being the basic oscillation frequency (it may be found e.g. by harmonic balance method [13]). This rule gives simple (much more simple than one in [13]) approximate necessary condition for chaos and makes a definite physical sense: equations (4), (5) correspond to the condition that all the 3 operation points available are unstable. We have also tested the validity of this rule for numerous different I(U) curves and for the results which have already been published.

Chaotic oscillations in a circuit with a hypothetical InP Gunn-effect diode are shown in Fig. 4. Such diodes serve as powerful microwave oscillators [12]. I(U) curve corresponding to device active region length 10μ and to the uniform electric field distribution (so-called LSA mode [12]) is shown by a dashed line in Fig.4,c,d. Two essentially different kinds of oscillations are shown. In Fig.4,a,c the diode voltage is always above the threshold value of NDC U_{1t} . Thus the circuit does not control the space charge growth and the device operates in the Gunn domain mode. Possible types of diode - circuit interactions seem to be very interesting in this case because the device acts as a source of external signal in a chaotic circuit. Obviously, more rigorous treatments are necessary to take account of nonuniform and time-dependent field distribution.

Fig. 4,b,d represents the oscillation mode with a space charge growth fully controlled by the voltage. With ω_2 sufficiently high it corresponds to the most effective LSA mode of the Gunn diode operation providing a generation up to several hundred HGz.

We also applied the above method to some S-type devices (avalanche transistors, thyristors etc.) and found several chaotic regimes in the circuit dual to one shown in Fig. 1.

To conclude, it was shown in this paper that NDC semiconductor devices can be used as high frequency and microwave generators of chaotic signals which have various applications in communications and other fields of engineering.

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EXTRINSIC HOPPING PHOTOCONDUCTIVITY IN DIAMOND-LIKE SEMICONDUCTORS

O.I.Smimova, Ya.E.Pokrovskii, N.A.Khvalkovskii
Institute of Radioengineering & Electronics, Moscow 103907

1. INTRODUCTION

Fast response of extrinsic photoresistors made from diamond, silicon or germanium doped with III and V group impurities is due to giant capture cross-sections of electrons and holes to ionized impurities under Coulomb attraction. At low temperatures these cross-sections are much larger than that corresponding to geometric dimensions of impurity orbitals in ground states. As was shown by M.Lax [1] and then in a large number of papers (see, for ex., [2]), the carriers are captured initially on shallow excited states and then they go down by a ladder of excited states with emission of acoustical phonons. The model [2] is based on the suggestion about quasi-continuous distribution of excited states and is in a good agreement with experimental data. It is possible to calculate the lifetime τ of photocarriers if the impurity contents in semiconductor is known. But the relaxation process of impurity excitation is completed only after localization of carrier on the ground state. This process could be not so fast if the carrier reaches a deep excited state having the same parity as the ground state. In this case dipole optical transitions between those states are forbidden. In diamond-like semiconductors those states can be the lowest 1S- states splitted from ground state by valley-orbital interaction for donors and spin-orbital interaction for acceptors. If the lifetime τ^* of charge carriers on these states is much longer than that of free carriers τ , so the carriers should be accumulated on longliving excited states. At low temperature and high concentration of impurities it leads to predominance of extrinsic hopping photoconductivity (PC) with participation of longliving excited states of impurities. Long relaxation time and strong increase of photoresponse with temperature decrease should be specific for hopping PC.

2. DIAMOND

Monocrystals of synthetic diamond doped with B in concentrations $N=10^{17}-10^{19}\text{cm}^{-3}$ were investigated. Boron impurity creates an acceptor level with ionization energy 370 meV. Hopping PC in diamond predominates in temperature and concentration regions where the dark conductivity is also determined by hopping process [3]. For $N>10^{18}\text{cm}^{-3}$ it takes place at $T < 220\text{ K}$ (Fig. 1a). Typical behavior of hopping PC through excited states is an exponential increase of photoresponse with lowering T . The activation energies of the photoresponse were equal to 170 or 130 meV and were dependent on exciting photon energy $h\nu$. Both these values periodically changed as functions of $h\nu$ with period 165 meV, corresponding to energy of optical phonon. Oscillations with the same period were also observed in PC spectra and were in opposite phase in low and heavy doped crystals. It points to the existence of two longliving excited states of boron impurity in diamond with ionization energy 130 and 170 meV. At $T<90\text{ K}$ when thermal ionization of the excited states is hardly probable lifetimes of the excited states were determined from dependence of photoconductivity

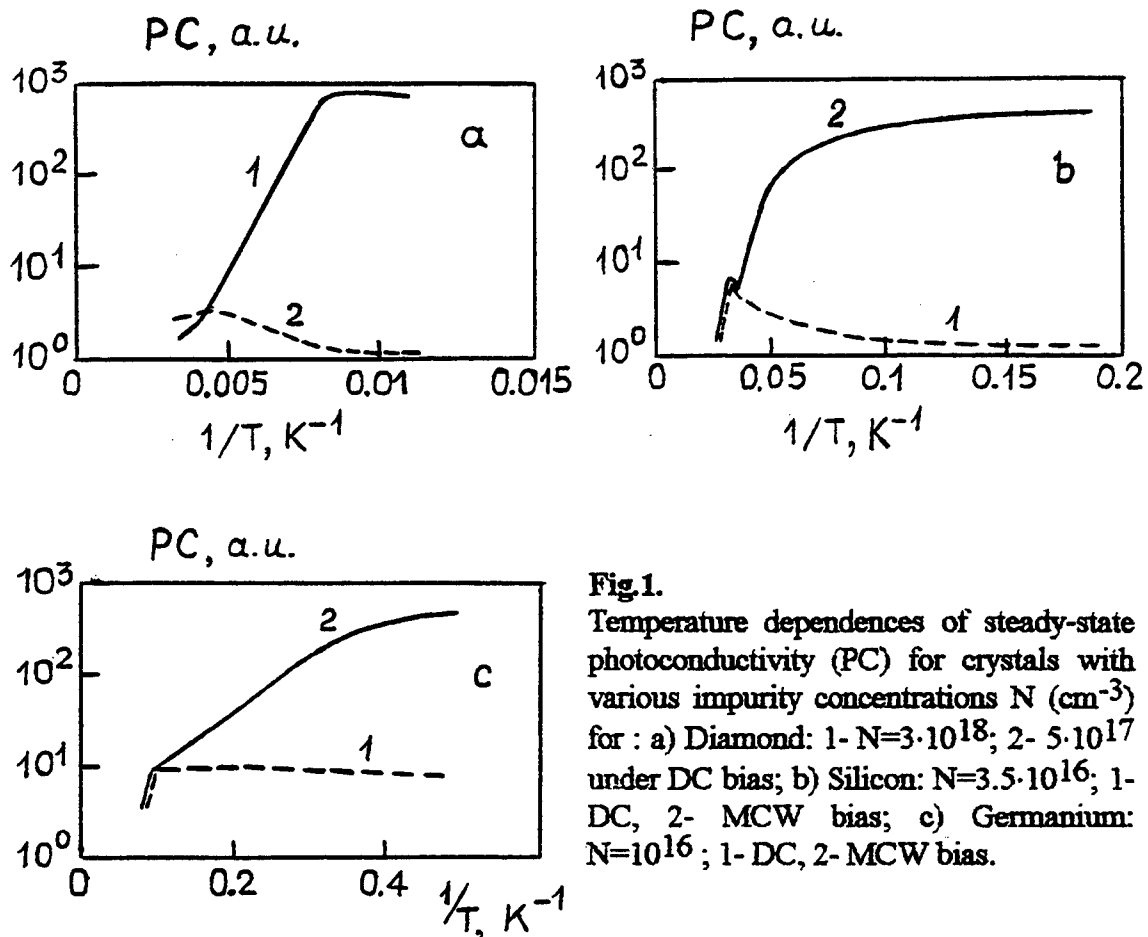


Fig.1. Temperature dependences of steady-state photoconductivity (PC) for crystals with various impurity concentrations N (cm^{-3}) for : a) Diamond: 1- $N=3 \cdot 10^{18}$; 2- $5 \cdot 10^{17}$ under DC bias; b) Silicon: $N=3.5 \cdot 10^{16}$; 1- DC, 2- MCW bias; c) Germanium: $N=10^{16}$; 1- DC, 2- MCW bias.

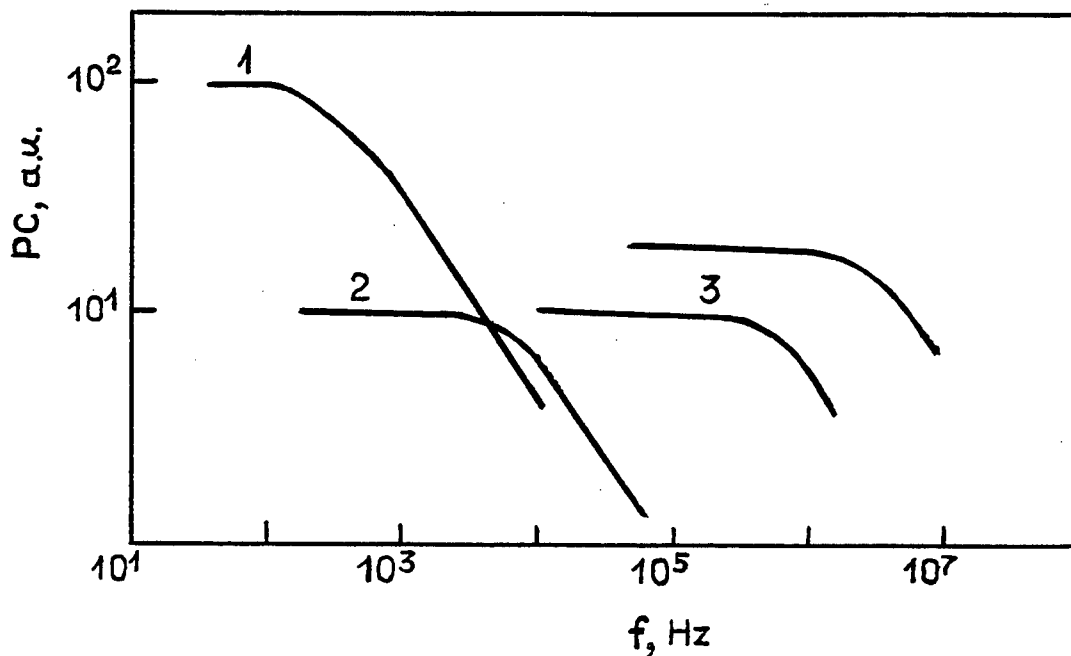


Fig.2. Dependences of photoconductivity (PC) on modulation frequency f of exciting light for : 1- Si (5K); 2 - Ge (2.2 K); 3 - Diamond (90 K)

on modulation frequency of exciting radiation (Fig.2). The values obtained from Fig.2 were $\tau^* = 2 \cdot 10^{-7}$ sec for level 170 meV and $\tau^* = 4 \cdot 10^{-8}$ sec for level 130 meV. The lifetime of free holes $\tau = 10^{-11}$ sec estimated from the value of steady-state PC at higher temperatures. Therefore the lifetime of longliving excited states of boron impurity in diamond exceeds free holes lifetime by 3 - 4 orders.

3. SILICON

We studied PC of silicon doped with donors (P, As, Sb, Bi) and acceptors (B, Ga, In) in concentration $N = 10^{15} - 10^{17} \text{ cm}^{-3}$ and with minority impurity concentration $10^{12} - 10^{14} \text{ cm}^{-3}$ [4]. The ionization energies of the impurities are from 42,7 meV for Sb to 160 meV for In. Under DC bias PC was determined by free carriers with lifetime $\tau = 10^{-7} - 10^{-10}$ sec. The lifetime values and their temperature dependences (5 - 50 K) were in a good agreement with cascade capture theory (Fig.1b). Under microwave (MCW, 37 GHz) bias and $N > 5 \cdot 10^{15} \text{ cm}^{-3}$ the relaxation time of PC increased to 10^{-3} sec (Fig.2) and the value of steady-state MCW PC exceeded that under DC bias almost by three orders at low T (Fig.2b). It was observed for all impurities except of Ga and Bi. For these impurities MCW and DC photoresponses were similar. To explain the experimental dependences of MCW PC on excitation intensity, temperature, majority and minority impurity concentrations we suggested the model of polarization PC in MCW electric field. In a doped and compensated semiconductor photocarriers, captured on dipoles, create charged pairs consisting of minority impurity ion and majority impurity atom in excited state with lifetime τ^* . Coulomb attraction between the charged pair and the nearest majority impurity free ion leads to a drift of the ion to the charged pair. If the drift time is shorter than τ^* , so triplets created, consisting of majority and minority ions and localized nearby longliving excited atom. Polarization PC is a result of hopping transitions between excited and ionized majority impurity atoms induced by MCW electric field. It leads to a strong absorption of MCW electric field energy. We estimated that polarization PC can be much higher than DC PC for heavy doped and compensated semiconductor at low temperature. The model is in a good agreement with experimental data. The absence of slow relaxation of MCW PC in Si doped with Ga and Bi is due to a possibility of fast relaxation of excitation by emission of only optical phonon. Long lifetime 10^{-3} sec of excited states of other donors and acceptors in Si leads to a strong influence of excitation intensity on the results of optical experiments. So, the relaxation time of absorption of room temperature background radiation of excited crystals, due to population of excited states, increase with decrease of background intensity. The excitation of doped Si also leads to capture of photocarriers to neutral impurity atoms and creation of H^- -like centers. DC PC due to H^- -centers was clear observed in far IR spectra obtained by FTS method. However in a strong electric field ($> 100 \text{ V/cm}$) H^- -like centers were distructed, MCW PC and absorption of background radiation did not changed sufficiently. Therefore the observed phenomena of slow relaxation can not be explained by existence of H^- -like centers. In IR absorption spectra of Si doped with B and As broad bands were observed and investigated in a region of energies lower than ionization energies of the impurities. Low-energy edges of the step-like bands correspond to ionization energies of 1S excited states of B (23 meV) and As (32 meV) in silicon.

4. GERMANIUM

We carried out the preliminary investigation of germanium doped with As in concentrations $N=10^{15} - 10^{16} \text{ cm}^{-3}$ [5]. Ionization and valley-orbital splitting energies of As in Ge are equal to 14,18 and 4,24 meV respectively. As in a case of Si, the difference between DC and MCW PC was observed in strongly doped Ge crystals. At 2,2 K this difference exceeds two orders (Fig.1c). The relaxation time τ^* determined from frequency dependence of photoresponses is about $3 \cdot 10^{-5}$ sec (Fig.2) and it is much longer than free electrons lifetime τ . It points to the existence of longliving excited states of donor impurities in germanium.

5. CONCLUSION

We established that in diamond, silicon and germanium there are simple donor and acceptor impurities having longliving excited states. The lifetime of those excited states are by a few orders longer than the lifetime of free photocarriers. This difference of lifetimes leads to accumulation of charge carriers on longliving excited states. That manifests itself in a predominance of hopping PC under DC or MCW bias. Localization and ionization energies of impurities in diamond, silicon and germanium are sufficiently different, so hopping PC is observed at various concentrations and temperatures for these semiconductors (Fig.1). The lifetime τ^* of excited states also differs by a few orders (Fig.2). In spite of so strong difference the general regularity of the established phenomena for these semiconductors are similar because of the similar physical nature of longliving excited impurity states - the splitting of impurity ground states in semiconductors with diamond-type crystalline lattice.

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THEORY OF SCHOTTKY-BARRIER TUNNEL JUNCTION RESPONSE TO RADIATION PRESSURE

A. Ya. Shul'man

Institute of Radioengineering and Electronics of the Russian Acad. Sciences
103907 Moscow GSP-3, Russia. E-mail: ash@cplire.ru

A metal-semiconductor tunnel junction with a Schottky barrier is a structure in which the form of potential barrier and therefore the tunneling current depends significantly on the profile of the self-consistent distribution of electrons in the semiconductor [1-2]. Under ordinary conditions this distribution is established by the electric field generated by charges of impurities and of surface states at the boundary with the metal. The equilibrium position of the boundary of the electron gas corresponds to the balance of forces, acting on each volume element of the monopolar electron plasma due to the presence of the electron pressure gradient and of electric field in the plasma. When this balance is disrupted by an external perturbation, the plasma boundary is displaced and the shape of the potential barrier changes. That change can be detected as the change in the tunneling conductivity of the junction. We consider the case when such a perturbation is the radiation pressure force, arising due to the plasma reflection of the light by free electrons of the semiconductor.

The effect described above was predicted in [3], observed in [4] and experimentally investigated in [5]. The photoresistive effect in n-GaAs/Au tunnel junctions was found under the action of electromagnetic radiation in the region of the plasma reflection at the wavelength $\lambda=90.55 \mu\text{m}$. Here the theoretical consideration of the radiation-pressure-deformed self-consistent Schottky barrier is presented and the photoresistive response of tunnel junction produced by this mechanism is calculated.

Let a degenerate electron gas occupy the half-space $x < 0$ to the left of the semiconductor-metal interface. If an electromagnetic plane wave, whose frequency ω is much lower than the plasma frequency ω_p of the electrons, is incident on the electron gas from the right, then the reflection of radiation is accompanied by transfer of momentum to the electron subsystem. This should disturb the equilibrium of force and shift the plasma-depletion layer boundary. As a result, the shape of the potential barrier changes and correspondingly the resistance of the tunnel junction has to change.

In order to find this change, we consider the condition of equilibrium of the plasma in a static electric field of the depletion layer, taking into account also the ponderomotive forces produced by the radiation incident in a direction normal to the surface. Let us begin with well-known hydrodynamic equation of momentum balance for electrons:

$$mn \frac{d\mathbf{u}}{dt} = -\nabla p - ne\mathbf{E} - n \frac{e}{c} [\mathbf{u}\mathbf{H}] - mn \frac{\mathbf{u}}{\tau} \quad (1)$$

Here \mathbf{H} is the magnetic field of the wave, m is the effective mass, $n(x)$ is the density, $p(x)$ is the pressure, $\mathbf{u}(x,t)$ is the drift velocity, and τ is the momentum relaxation time of the electrons. Now we transform this expression, using the fact that the density of the ponderomotive force $\mathbf{F}_{em}(\mathbf{r},t)$, exerted by the electromagnetic field on charges with density $\rho(\mathbf{r},t)$ and currents with density $\mathbf{j}(\mathbf{r},t)$, can be represented as a divergence of the Maxwell stress tensor $T_{ik}(\mathbf{r},t)$:

$$F_{em,i}(\mathbf{r}, t) \equiv \rho E_i(\mathbf{r}, t) + \frac{1}{c} [\mathbf{j} \mathbf{H}(\mathbf{r}, t)]_i = \frac{dT_{ik}}{dx_k}. \quad (2)$$

Here we dropped the time derivative of the Poynting vector in the matter (Minkovski force) since the quasistationary pulse field is considered. It may be shown in the case of non-dissipative reflection of the radiation from plasma half-space in quasistationary approximation

$$\frac{\kappa}{4\pi c} \frac{\partial}{\partial t} [\mathbf{E} \mathbf{H}] = \frac{(\omega / \omega_p)^3}{c^2 \kappa^{1/2} \omega_p} \frac{1 - (\omega / \omega_p)^2}{\left[1 - (\frac{\omega}{\omega_p})^2 (1 - \kappa^{-1})\right]^3} \frac{\partial^2}{\partial t^2} \mathbf{J}, \quad (2a)$$

where κ is the lattice part of the dielectric constant of the semiconductor, \mathbf{J} is the Poynting vector of incident wave. It is interested to note that the first non-vanishing approximation for Minkovski force under considered conditions turns out to be proportional to the second time derivative of the slow-varying intensity of the incident radiation instead of first order of time derivative usually obtained (cf. with [6], Sec. 80). Since we will assume $\omega < \omega_p$, the pulse duration τ_d is of order $10 \div 100$ ns, and $\omega \tau_d \gg 1$ (quasistationary condition), the Minkovski force can be estimated as negligibly low (of order of 10^{-12}) in comparison with the terms kept in (2).

Setting $\rho = e[N - n(x)]$ and $\mathbf{j} = -enu$ and using Eq. (2), the r.h.s of Eq. (1) can be put into the form

$$mn \frac{d\mathbf{u}}{dt} = \mathbf{F}(x, t) - mn \frac{\mathbf{u}}{\tau}, \quad (3a)$$

where

$$F_i(x, t) = -\nabla_i p - eNE_i + \frac{dT_{ik}}{dx_k} \quad (3b)$$

Assuming now

$$\mathbf{E}(x, t) = \mathbf{E}_{st}(x) + \mathbf{E}_1(x) \cos(\omega t), \mathbf{H}(x, t) = -\mathbf{H}_1(x) \sin(\omega t)$$

averaging Eq. (3a) over the period of the high-frequency field, we obtain the condition of equilibrium of a collisionless plasma in the form $\overline{F_x} = 0$ (the overbar indicates time-averaging). Integrating this equality from $-\infty$ up to point x in the depletion layer ($x_0 < x < 0$), we find that the total force, acting on the plasma, is zero:

$$p(-\infty) - N\Phi(x) + \overline{T_{xx}}(x) = 0. \quad (4)$$

Here we took into account the fact that $p(x) = \overline{T_{xx}}(-\infty) = 0$ and

$-eE_{st}(x) = -d\Phi/dx$, where $\Phi(x) = -e\phi(x)$ is the potential energy of an electron in the electrostatic potential $\phi(x)$. The point x_0 is the boundary point of the degenerate plasma in the depletion layer and is determined by the condition $\Phi(x_0) = \mu$, where μ is the Fermi energy in the bulk of the semiconductor. Since

$$T_{xx}(x) = \frac{1}{8\pi} (\kappa E_{st}^2 - \frac{\kappa}{2} |E_1|^2 - \frac{1}{2} |H_1|^2)$$

for the geometry chosen and the amplitude H_1 of the magnetic field, decaying as $\exp(kx)$ with $k = (\omega/c)[\kappa(\omega_p^2/\omega^2 - 1)]^{1/2}$ into the plasma, can be expressed with the help of the first Maxwell equation

$$\text{rot} \mathbf{E} = -\frac{1}{c} \frac{\partial \mathbf{H}}{\partial t}$$

in terms of E_1 by the relation

$$H_1 = [\kappa(\omega_p^2/\omega^2 - 1)]^{1/2} E_1,$$

we obtain

$$T_{xx}(x) = \frac{\kappa}{8\pi} E_{st}^2(x) - \frac{\kappa}{16\pi} \frac{\omega_p^2}{\omega^2} |E_1(x)|^2.$$

It should be noted that the transverse components of the electromagnetic field are almost constant in the depletion layer owing to their characteristic length (skin length $L_{\perp} = c / \omega_p \kappa^{1/2}$ or wavelength in pure semiconductor $\lambda / \kappa^{1/2}$) is much greater than the thickness L of the depletion layer. Hence, we will use further the value of $E_1(x_0)$ as the electric field amplitude of the electromagnetic field.

An equation for the static field E_{st} in the depletion layer in the presence of an electromagnetic wave can be derived from Eq. (4):

$$\frac{\kappa}{8\pi} E_{st}^2 = N\Phi(x) - \frac{2}{5} N\mu + \frac{\kappa}{16\pi} \frac{\omega_p^2}{\omega^2} |E_1(x_0)|^2. \quad (5)$$

In order to understand the consequences of the change in the field E_{st} in the Schottky barrier owing to the action of the radiation pressure, we examine the expression for the tunneling current [2]

$$I \propto \int_0^{\infty} dE [f(E) - f(E + eV)] \exp \left[-\frac{2(2m)^{1/2}}{\hbar} \int_{x_E}^0 dx (\Phi(x) - E)^{1/2} \right].$$

Here x_E is the turning point of the trajectory of an electron incident with energy E on the barrier. We denote the argument of the exponential by $-G$ and transform it using (5):

$$G(E, \Phi_b, |E_1|^2) \equiv \frac{2(2m)^{1/2}}{\hbar} \int_{x_E}^0 dx (\Phi(x) - E)^{1/2} = \frac{2(2m)^{1/2}}{\hbar} \int_E^{\Phi_b} d\Phi \frac{(\Phi - E)^{1/2}}{\Phi'(\Phi)}, \quad (6)$$

where Φ_b is the height of the Schottky barrier. The expression for the static electric field Φ' in the barrier as a function of the potential Φ can be obtained from (5). The change occurring in the current I when the tunnel junction is irradiated at the constant bias voltage V is related to the change in the argument of the exponential

$$\delta G = G(E, \Phi_b, u) - G(E, \Phi_b, 0), \quad (7a)$$

where known high-frequency potential $u = e^2 |E_1|^2 / 4m\omega^2$ is introduced. As a result we can obtain the explicit expression for the relative response to the radiation pressure

$$\frac{\Delta I}{I} \Big|_{V=const} = \frac{\Delta \sigma}{\sigma} \Big|_{V=const} \quad (7b)$$

where $\sigma = I / V$ is the conductance (not the differential one!) of the tunnel junction and ΔI is given by the simple expression

$$\Delta I = \int_0^{\infty} dE [f(E) - f(E + eV)] \{ \exp[-(G + \delta G)] - \exp(-G) \}. \quad (7c)$$

The following qualitative features of the tunnel junction response to the radiation pressure results from the expressions (7): 1) the tunnel transparency of the barrier has to increase under the action of the radiation; 2) the magnitude of the response does not depend on the radiation frequency (if $\omega < \omega_p$); 3) at low radiation intensity in linear approximation for ΔI as a function u the relative response depends on the free carrier density N approximately as $1/N^{3/2}$. All these results are in agreement with the measurements [5].

The most striking conclusion above stated is the increase of the barrier transparency since the transfer of radiation momentum to the free carrier should seemingly shift the plasma boundary inside semiconductor, giving rise to the increase the barrier thickness and to decrease of the transparency. Formally it follows from the Eq.(5) that shows the increase of the static electric field in the depletion layer as the radiation presents. The point is that the force acting on a volume element of the plasma is not a simple sum of the forces exerted by the external electromagnetic field on the each electron. It includes also the interaction of the electrons by means of the self-consistent field. The existence of the plasma reflection is itself due to this interaction. Thus, one can expect that although the radiation-pressure force acts on the entire free carrier plasma as a whole in the direction away from the illuminated surface of the semiconductor, the part of the transition layer of the plasma boundary, where the electron density drops from its bulk value to zero, can move in the opposite direction. This makes thinner the barrier width at the energy of order of Fermi level and increases the barrier width at the energies of the electron states well below Fermi level. However, the main contribution to tunnel current is determined by the electron states near the Fermi level, the tunnel transparency of which is increased.

A detailed analysis of the field and electron distributions in the transitional layer would require solving the time-dependent Vlasov kinetic equation in the inhomogeneous barrier field, which is a quite hard problem. At the same time, the use of the momentum-balance equation and the Maxwell stress tensor makes it possible to find exactly the change in the Schottky barrier in the depletion layer for electron energies $E > \mu$. Moreover, the general expressions (7) allow us to analyze the response in non-linear region of its intensity dependence. This may open the way to the absolute measurements of the radiation field strengths in the near-surface region and lead to an explanation of the observable enhancement of the measured response [5] in comparison with the theoretical estimations.

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PHYSICAL LIMITATION FOR DRAIN VOLTAGE OF POWER PHEMTs

V.A.Vashchenko and V.F.Sinkevitch
Russia

INTRODUCTION Monolithic microwave integrated circuits based on pseudomorphic GaInAs channel HEMT (PHEMT) has held a leader position among these devices for power applications [1]. High power performance requires a high drain-source breakdown voltage [1]. The drain breakdown, along with the other things, limits the major parameters of PHEMTs -- operating drain voltage and reliability. That is why, the understanding of breakdown mechanisms is important. Up to now such mechanisms have not been clarified. Modern technology of the PHEMT chip attachment allow one to avoid a high level of channel temperature and conditions of current thermal instability during its operation. That's why breakdown mechanisms which limit the drain supplying voltage are of an electrical nature and probably have the same features both in the DC and pulse operation of PHEMTs. The purpose of this study is to establish the electrical mechanisms of the drain-source breakdown, which result in a maximum drain voltage limitation and, particularly, in the catastrophic failures under a drain voltage increase. In this paper the results on the drain--source current-voltage (I_D - V_{DS}) characteristics of the PHEMTs and the light emission spectral and intensity distributions are presented for pulse and DC regimes.

EXPERIMENTAL For the experimental investigation the test structures of serial PM HEMTs (Fig.1(a)) were used. The PHEMTs structures have topology (Fig.1(b)) : 180 μm gate width, 0.3 μm gate length, 3 μm drain-source spacing, V-Au gate and AuGe-Au-V-Au drain and source metallization. The I_D - V_{DS} characteristics were measured using method [2] at 20 ns pulse duration of the drain voltage, 0.01 % duty factor, constant gate biases and 1000 ohms drain load resistor. The light emission intensity distribution was measured using the scanner with a narrow gap and the photomultiplier with S-20 photocathod. The scanner allowed one to measure a light emission distribution over an active PHEMT surface with 1 μm spatial resolution. The DC I_D - V_{DS} characteristics and the light emission distributions were measured on the PHEMTs matched in the amplifier, having 1000 Ohms resistor in the drain circuit.

RESULTS The typical pulse I_D - V_{DS} characteristics of investigated PM HEMTs at various constant gate biases are presented in Fig.2(a). After the saturation region a slight drain current increase was observed in the I_D - V_{DS} characteristics due to a drain avalanche breakdown (Fig.2(a)). In this state (α) the light emission was distributed uniformly along the drain contact and electroluminescence spectrum was typical for the GaAs avalanche breakdown (Fig.2(b,c,d), curves (α)). At operation and pinch off gate biases the reversible switching of PHEMT to a new state (β) was observed (Fig.2(a)). The switching time was less than 1 ns. After switching the light emission intensity distribution along the drain changed (Fig.2(b), curve (β)) due to current filament formation. Within the current filament area the light emission distribution in the drain--source spacing also changed (Fig.2(c), curve (β)). The current filament dimension increased with the drain current increase. The

radiation intensity of 0.88 μm wave length increased in the light emission spectrum (Fig.2(d)) after switching. This increase was the result of an additional radiation from the gate-source spacing (Fig.2(c), curve (β)). Under the following drain current increase the spectrum was not changed. For positive or small gate biases a sharp drain current increase was observed at the positive differential conductivity (PDC) (Fig.2(a)). This increase was limited by a thermal overheating. In a high state condition the light emission was distributed uniformly along the drain contact, but the light emission distribution in the drain--source spacing was similar to the distribution after switching (Fig.2(c), curve (β)). In high conductivity conditions both at the PDC and at the NDC states the light emission spectra were the same.

A decrease of the drain load resistance, an increase of the duty factor or a pulse duration led to the PHEMT local burnout under the measurements of switching voltage. As a result of the burnout the active area of the structure was locally melted in areas of 10 μm dimension, which coincided with the places of current filament formation. DC and pulse I_D - V_{DS} characteristics of the investigated PHEMTs were the same before switching. At small gate biases the switching was reversible, but in pinch off conditions the switching led to a local instantaneous burnout. The switching or burnout voltages in DC regime coincided with a good accuracy with switching voltages in 20 ns pulse regime. After DC switching the light emission distribution on the PHEMT surface coincided with the distribution in 20 ns pulse regime.

In 20 ns pulse regime, at a duty factor of more then 1% and pinch-off gate biases the filament formation showed new interesting features. In such conditions after switching into the current filament state the PHEMT differential conductivity became positive and the following drain current increase was accompanied by a number of the breaks and hysteresis in the I_D - V_{DS} characteristic (Fig.2(a) dashed line). These peculiarities corresponded to the transitions to new multifilament states. Under a high drain current of the PHEMT the multifilament states have a spatial periodic structure (Fig.2(b), curve (γ)). Under a drain current increase the filaments in the initial state became expanded at first and then the spatial period decreased. Depending upon the way of the electrical load and the duty factor the filament states with the same number of filaments may localize in various places of the PHEMT structure.

DISCUSSION From the presented results it follows, that in the condition of a low thermal overheating at a constant gate bias the drain voltage increase is limited by a sharp drain current increase at the PDC or the NDC. The NDC formation results in the HEMT switching to a filament state according to the drain load characteristics. Depending upon conditions of channel Joule's heating (a pulse duration, a duty factor or a drain current level in the filament state) the filament formation may end with a local burnout both in a pulse and DC regimes at voltage of the NDC formation and switching. Before switching or a sharp drain current increase the light emission spectrum was typical for the avalanche breakdown of GaAs, and not depends upon the drain voltage value. After switching or a sharp drain current increase the spectrum changed due to the GaAs band gap electroluminescence from the gate-source spacing. This electroluminescence from gate-source spacing pointed out the intensive recombination of injected holes and electrons near the source in the i--GaAs layer of PHEMT (Fig.1(a)).

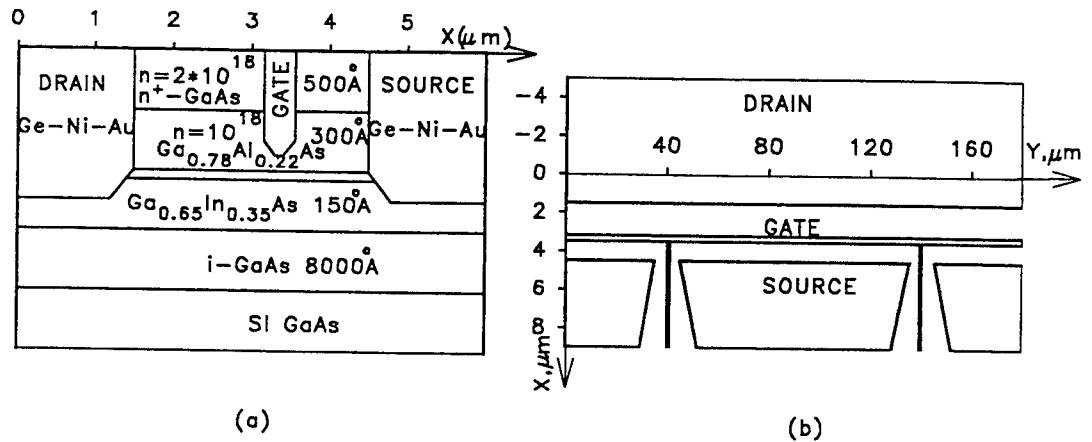


Fig.1. The structure (a) and topology (b) of the investigated PHEMT.

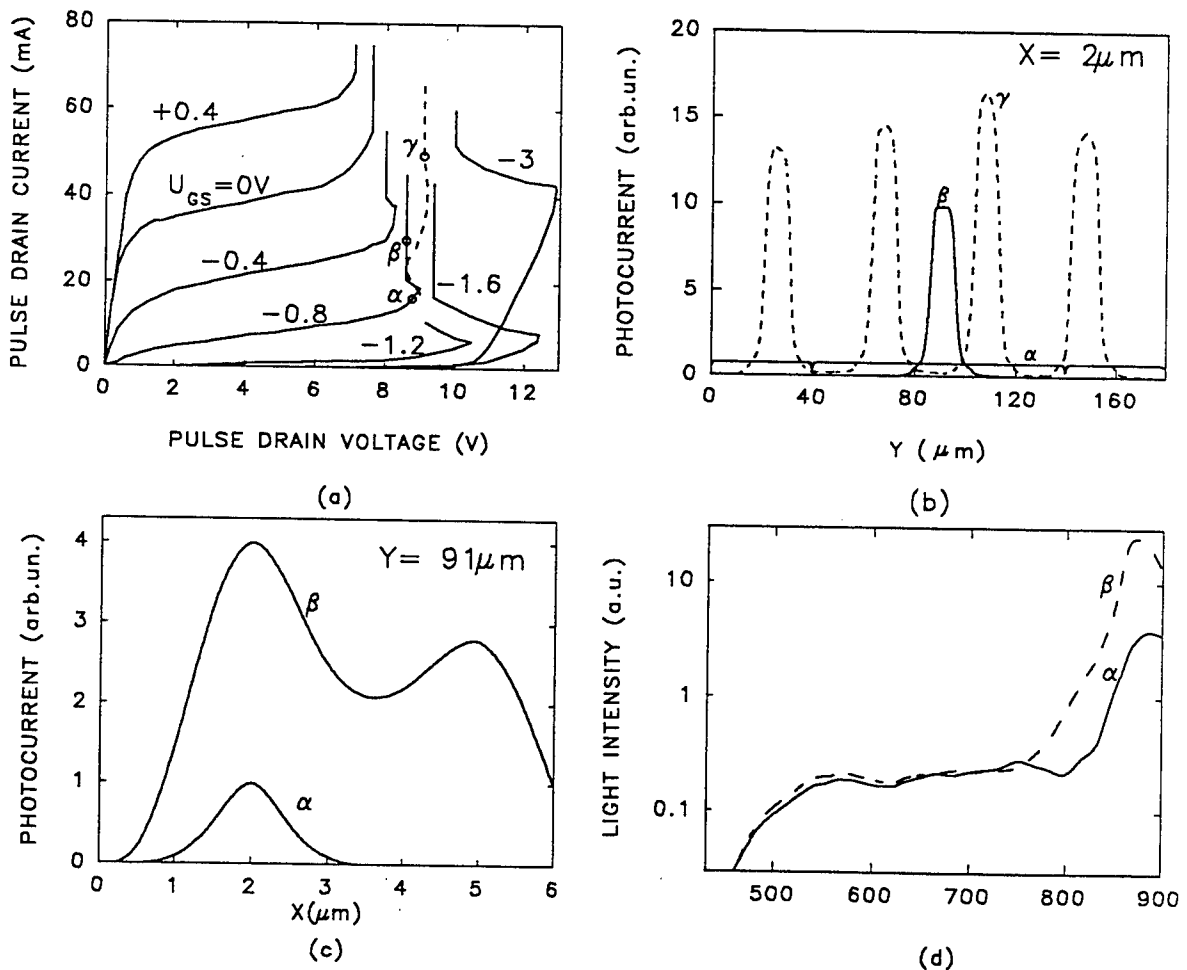


Fig.2. Pulse drain-source characteristics of PHEMT (a). The light emission intensity (photomultiplier current) distributions on the active surface of PHEMT: along the drain (b) and in the source-drain spacing (c). Light emission spectra (d). The state (α) before switching, corresponding to curves (α), and conditions (β, γ) after switching, corresponding to curves (β, γ), are marked in fig.(a).

The main characteristics of the PHEMTs breakdown (the I_D - V_{DS} characteristics, the spectra, the filament formation) are close to the characteristics of the GaAs MESFET's breakdown [2]. This allows to conclude that observed breakdown mechanism is the same with isothermal current instability at an avalanche injection breakdown of SI buffer of GaAs MESFET's [2,3]. The mechanism that produces this breakdown is as follows: first there is accumulating the holes from the drain avalanche area in the i-GaAs layer near the source. It results in an electron injection increase from the source, the formation of the quasi neutral area of the electron-hole plasma near the source, the modulation of the i-GaAs layer conductivity, an electric field redistribution in the drain-source spacing and the change of HEMTs differential conductivity. Apparently, the sign of differential conductivity is defined by the effective distance between an avalanche and injection areas, and is controlled by the gate space charge region and also defined by the channel length.

Formation and evolution of multifilament states under the HEMT breakdown demonstrated the main properties of dissipate structures behavior and are an example of selforganization in strong nonequilibrium systems [4,5]. The formation of multifilament states appears to be defined by difference between two spatial parameters: channel NDC and the distributed resistance of the drain and source contacts.

CONCLUSION According to the presented results the maximum drain voltage of the PHEMTs at a constant gate bias is limited by an avalanche injection breakdown of the undoped i-GaAs layer. The evolution of this breakdown results in a the sharp drain current increase at PDC or in the appearance of NDC and the following switching to the filament state of a high current density. The instantaneous burnout of the PHEMT under an increase of the drain voltage is the result of a local overheating and melting in current filament area after switching. Such a local burnout appears to be the main kind of a catastrophic failures of power PHEMT in the applications under the drain voltage overloads. Since the values of switching voltages at 20 ns pulse regime coincide with switching or burnout voltages in DC regime, therefore the method of 20 ns measurements may be successfully used for direct reversible measurements of the safe operating area of PHEMTs.

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Comparative Study on Resonant Tunneling Diode (RTD) and Traditional Tunnel Diode (TD) and Their Co-integration with Heterojunction Bipolar Transistors (HBTs)

X. Wang, W. L. Chen, G. O. Munns, J. R. East, and G. I. Haddad
Solid-State Electronics Laboratory
Department of Electrical Engineering and Computer Science
The University of Michigan, Ann Arbor, MI 48109-2122

This paper discusses a comparison of resonant tunneling diodes (RTD's) and conventional tunnel diodes (TD's) for use in negative differential resistance based digital circuits. The comparison includes processing, switching speed, temperature dependence, stacking, as well as I-V characteristics. The RTD is a highly strained AlAs/InGaAs/AlAs structure, while traditional Si TD (dopant concentration greater than $3 \times 10^{19} \text{ cm}^{-3}$) and InGaAs TD (dopant concentration $5 \times 10^{19} \text{ cm}^{-3}$) are both fabricated and tested.

Chemical Beam Epitaxy (CBE) is used to co-integrate InP-based heterojunction bipolar transistors (HBTs) and RTDs for the first time. The integrated transistor achieves dc and differential current gain of 53.6 and 122 respectively, with breakdown voltages $V_{\text{ceo}} \sim 6 \text{ V}$ and $V_{\text{beo}} \sim 9 \text{ V}$. For microwave performance, f_T of 77 (63) and f_{max} of 60 (53) GHz after (before) the onset of negative differential resistance is obtained. Co-integration of high speed HBTs and TDs are also experimentally realized for the first time. A dc current gain of 20 with NDR characteristics and breakdown voltages of $V_{\text{ceo}} \sim 6 \text{ V}$ and $V_{\text{beo}} \sim 9 \text{ V}$ are shown. Estimated f_T of the fabricated transistor is around 50 GHz.

A hybrid integration circuit of Si bipolar junction transistors (BJTs) and Si TD is being improved by comparing different ways of doping for the TD, including diffusion, ion implantation, and molecular beam epitaxy (MBE), to achieve higher dopant concentration.

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MICROWAVE CHARACTERISTICS OF HIGH ELECTRON MOBILITY TRANSISTORS

Hyungkeun Ahn*, Kasemsuwan Varakorn and M. El Nokali

*Department of Electrical Engineering, Kon-Kuk University
Mojin-Dong 93-1, Kwangjin-Ku, Seoul, Korea 143-701

Department of Electrical Engineering, University of Pittsburgh
348 Benedum Hall, Pittsburgh, PA 15261

The characterization of HEMTs in the microwave range is done by measuring the S or Y parameters. Analytically, two distinctive approaches exist for the calculation of those parameters which are essential to analyze and design circuits in the microwave range. The first approach calls for deriving a small signal equivalent circuit from the dc model using a quasi-static approximation [1]. The circuit is then used to find the Y and S -parameters. The second approach known as the non-quasistatic approach [2] consists of solving the device wave equation to directly find the Y -parameters without having to find a physical equivalent circuit representation for the device.

In this paper, a physically based model describing the HEMT is used to predict the scattering and admittance parameters as function of the applied gate bias and the operating frequency. The Y -parameters are compared with those resulting from solving the device wave equation and found to be in excellent agreement. The model accounts for second order effects such as mobility degradation, velocity saturation as well as the conduction in the AlGaAs layer. The elements of the small signal equivalent circuit namely the transconductance, the output conductance and the capacitances are used to derive the Z -parameters and to project both the S and Y -parameters in three-dimensions. The model is used to estimate the operating power gain (P_W), the transducer power gain (P_G), the maximum stable gain (MSG) and the maximum available gain (MAG).

The theoretical predictions of the model are compared with the experimental data for a $250 \mu m \times 0.32 \mu m$, pulsed-doped HEMT [3] and a $350 \mu m \times 1 \mu m$ HEMT [2] and shown to be in excellent agreement over a wide frequency range.

Figure 1 compares Y_{11} obtained from this model to that resulting from the non quasi-static approximation. The figure shows an excellent agreement which was made possible by adjusting the values of C_{GS} and C_{GD} in our model.

The experimental data available for device 1 [2] are the admittance parameters of which we have selected Y_{11} and Y_{12} to reproduce in Figure 2. Those data are compared with the theoretical predictions of the model over a frequency range extending from 2 GHz to 18 GHz and show a good agreement over the entire range.

The data available for device 2 are the scattering parameters [3]. We have selected a representative sample of these parameters namely the real and imaginary components of S_{11} and superimposed them in Figure 3 on the predictions of the model over a frequency range extending from 1 to 25 GHz. The agreement between the theory and the experimental data is excellent.

Since we have established the accuracy of the model by comparing its predictions to the experimental data available for devices fabricated by independent research groups, we like to explore the potential of the model in projecting the admittance and scattering parameters as well as the power gains in three dimensions i.e. as functions of voltage and frequency. Towards that purpose, we have selected device 3 [4]. The experimental data available for device 3 are restricted to the dc and small signal parameters. We have established [1] the match between the predictions our dc and ac models with those published data. No experimental data are available for Y or S -parameter. We however have projected in Figure 4 the real and imaginary part of S_{11} , as function of both gate voltage and frequency.

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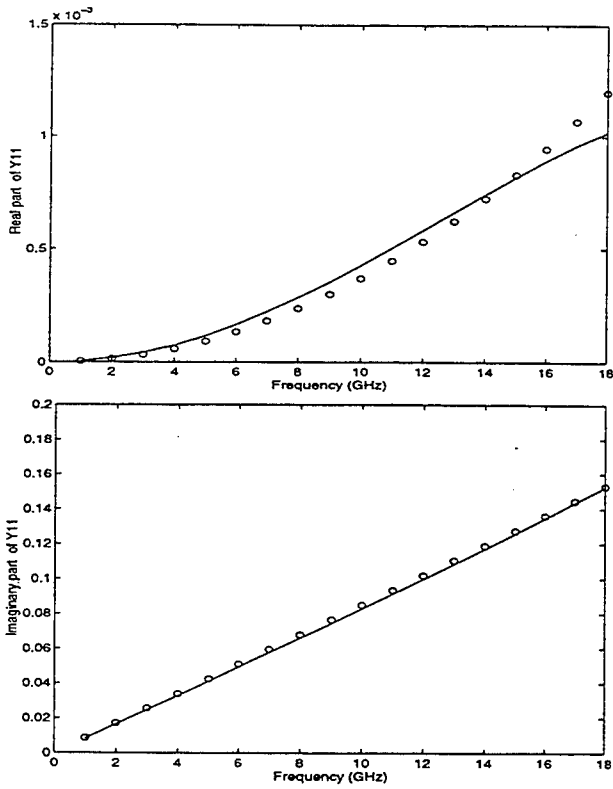


Fig 1. Real(upper) and imaginary(lower) part of intrinsic Y_{11} from the wave equation approach(o) and the theoretical predictions(-).

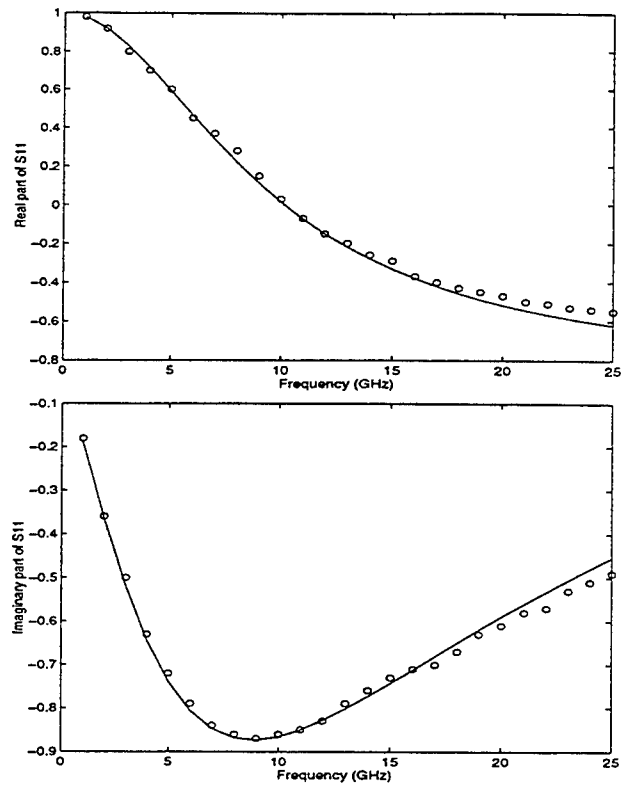


Fig 3. Real(upper) and imaginary(lower) part of S_{11} with experimental data(o)[1] and theoretical predictions(o) at $V_{DS} = 1.5$ (V).

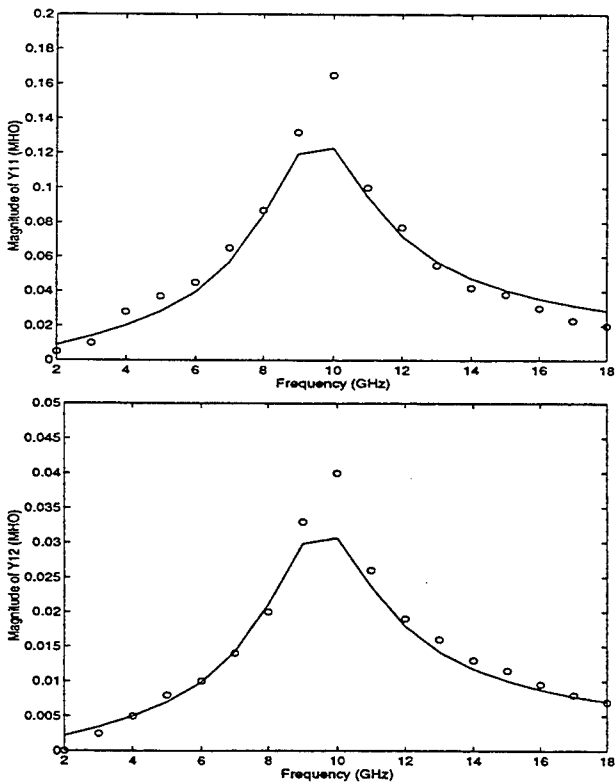


Fig 2. Y_{11} (upper) and Y_{12} (lower) amplitude from the experimental data(o)[2] and the theoretical predictions(-).

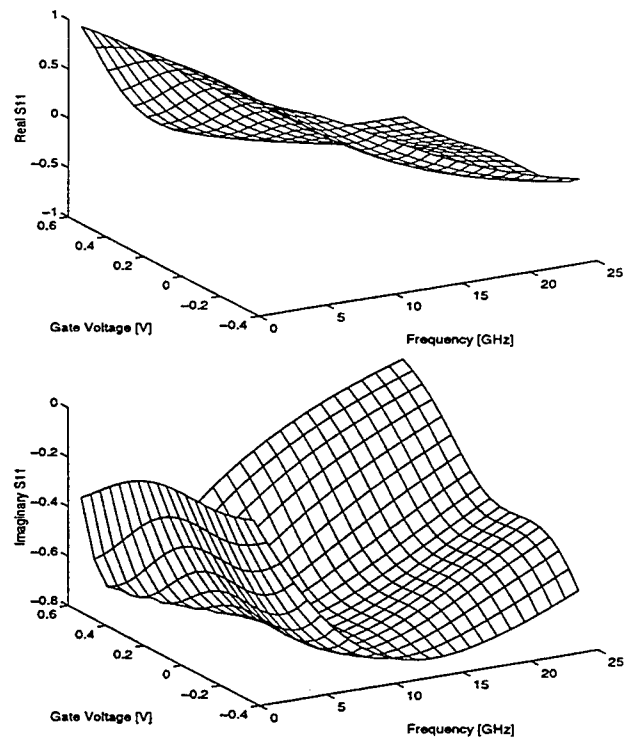


Fig 4. Three dimensional real(upper) and imaginary(lower) parts of S_{11} .

Quasi-optical Power Combining Techniques for Dielectric Substrates

H. Hwang, T. W. Nuteson, M. B. Steer, and J. W. Mink
Electronics Research Laboratory, Department of Electrical & Computer Engineering
North Carolina State University, Raleigh, NC 27695-7911

J. Harvey
United States Army Research Office, PO Box 12211, Research Triangle Park, NC 27709

A. Paoella
Microwave & Lightwave Components Division, AMSRL-EP-MA
United States Army Research Laboratory, NJ 07703

1 Introduction

Several quasi-optical systems have been reported, including grid oscillators [1] and amplifiers [2], resonant cavity oscillators [3,4], microstrip-based rotator arrays [5], and dielectric slab beam waveguides (DSBW) [6] for power combining. The dielectric slab system described here has the advantage of being two-dimensional and is thus more amenable to photolithographic reproduction than the conventional open quasi-optical power combining structures. Previous investigations of the quasi-optical dielectric slab cavity and waveguide [7,8] demonstrated the suitability of this structure for the integration of quasi-optical power combining with MMIC technology.

A complete DSBW quasi-optical system, as shown in Fig. 1, could consist of the following: a source, active or injection, [7], an amplifier array [8], triplers, and a leaky wave antenna which would be used for steering the energy out of the system. Between each of the stages lenses are used to focus the guided waves for optimal field concentration on the elements in the system. In this work we present the amplifier array stage using both convex and concave lenses as shown in Fig. 2. The DSBW amplifier system incorporates four MESFET amplifiers and two thin convex/concave lenses. The waveguide system was adjusted with the transistors turned off so that the guided waves are focused near the aperture of the receiving horn. The dielectric slab is Rexolite ($\epsilon = 2.57$, $\tan\delta = 0.0006$ at X-band), and it is 27.94 cm wide, 62 cm long, and 1.27 cm thick. The convex lenses are fabricated from Macor ($\epsilon = 5.9$, $\tan\delta = 0.0025$ at 100 kHz) with a radius of 30.48 cm, and the focal length, f , is 28.54 cm. The concave lenses are air ($\epsilon = 1$) with a radius of 30.48 cm, and the focal length, f , is 40.4 cm. The aperture width of both horn antennas is 9 cm, designed to be wide enough to catch most of the amplified power. Energy emitted from the input radiator propagates in a quasi-optical TE Gaussian mode in the dielectric slab waveguide, and is focused by the first lens in the middle area of the slab. This system is designed so that the amplifier unit cells are within the beam waist (the $1/e$ field points).

The amplifier unit cells are 7 cm x 1.5 cm and employ HP ATF-10235 MESFETs. This design was derived from the active slot-line notch antenna by Leverich, et al. [9]. An amplifier unit includes two end-fire Vivaldi antenna tapers which are gate-receiver and drain-radiator, and is specifically designed to eliminate surface-of-slab to ground-plane resonance. The advantage of locating the amplifiers on the ground plane is that it reduces beam-mode perturbation, scattering losses, and reflection of the input energy due to the amplifier structure. These are problems with amplifiers mounted on the surface of the slab [8] and in the more conventional grid system.

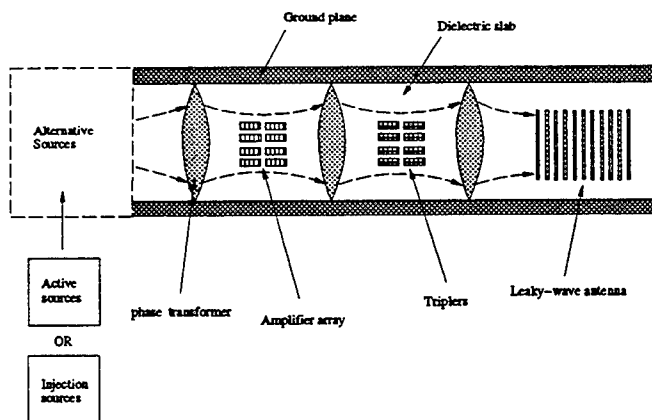


Figure 1: A dielectric slab beam waveguide system.

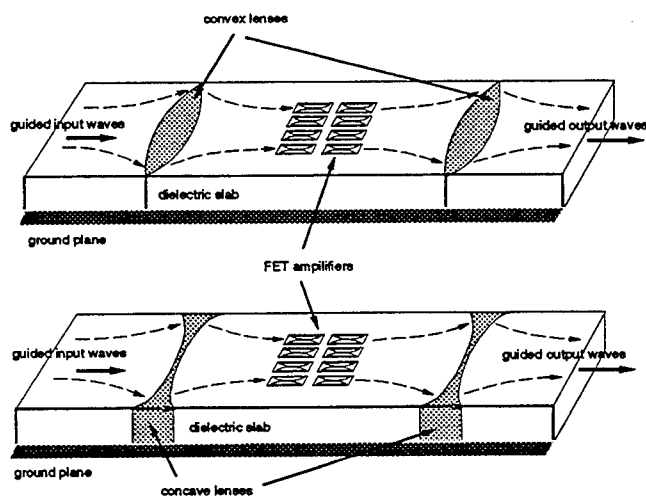


Figure 2: Amplifier array stage with convex and concave lenses.

2 Experimental Results and Discussions

Passive measurements were made on the DSBW system with no amplifiers present comparing the convex and concave lenses. The concave lens system has less loss than the convex lens system as shown in Fig. 3. Fig. 4 shows the electric field measured at a frequency of 7.28 GHz for both the convex and concave lenses. This measurement estimates the loss due to the lenses where the convex lens loss is approximately -3.66 dB and the concave lens loss is approximately -1.18 dB. This loss estimation is obtained by integrating the areas under the E -field patterns before and after lenses. In Fig. 5, the insertion loss is given for both cases where the convex lens system is showing lower loss. The reason for this is that the input wave scattered by the amplifier array goes into the air more easily for the concave lens system than for the convex lens system.

The amplifier gain, computed as the ratio between $P_{out}(\text{Amp ON})$ and $P_{out}(\text{Amp OFF})$, is shown in Fig. 6 for both concave and convex lens systems. The amplifier gain is 16 dB for the concave case and 14 dB for the convex case as P_{in} is -12.4 dbm. This implies that the concave lens system

has better performance than the convex lens system. In these measurements the four MESFET amplifiers were placed on the ground plane underneath the Rexolite.

The system gain (defined as P_{out}/P_{in}) is shown in Fig. 7 for both the concave and convex systems with and without a metallic top cover. For the concave case the system gain is approximately 7.7 dB with and without the metallic top cover. For the convex case the metallic cover gives a system gain of about 6 dB and without the cover 4 dB. The reason that there is a difference in the convex system gain with and without the cover is because the passive scattering loss for the convex lens system is higher than for concave lens system. Therefore, using a metallic cover can save more scattering energy for convex lens system.

3 Conclusions

We have demonstrated quasi-optical power combining in a dielectric substrate with the amplifier array located on the ground plane for both a concave and convex lens system. The overall performance of the concave lens system was better than the convex lens system including passive system gain, amplifier gain, and active system gain.

Acknowledgment

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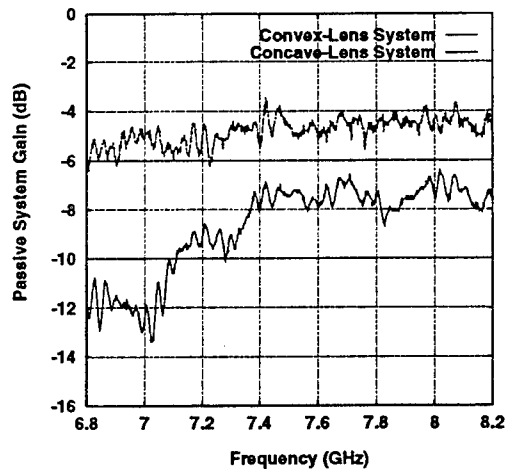


Figure 3: Passive system gain for convex-lens and concave-lens systems.

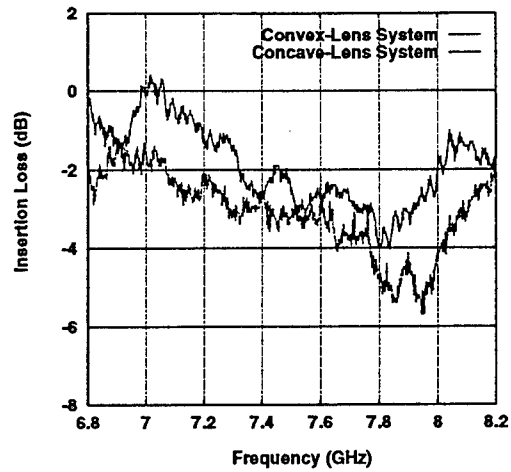


Figure 5: Insertion loss of convex-lens and concave-lens systems.

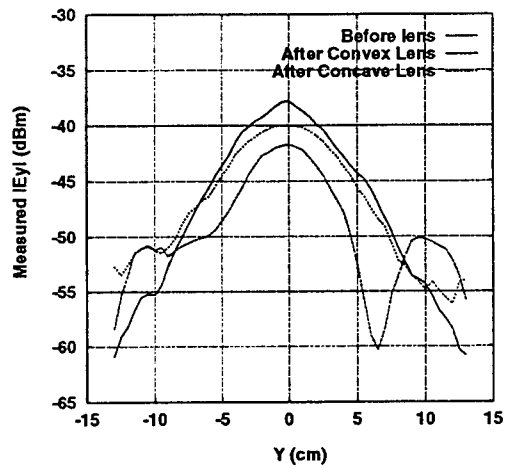


Figure 4: $|E_y|$ distributions before and after lenses.

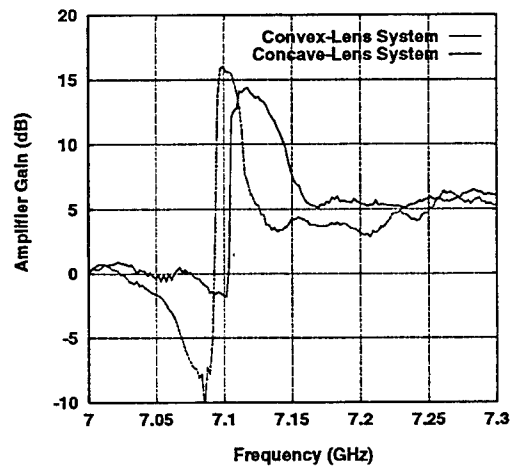


Figure 6: Amplifier gain in convex-lens and concave-lens systems.

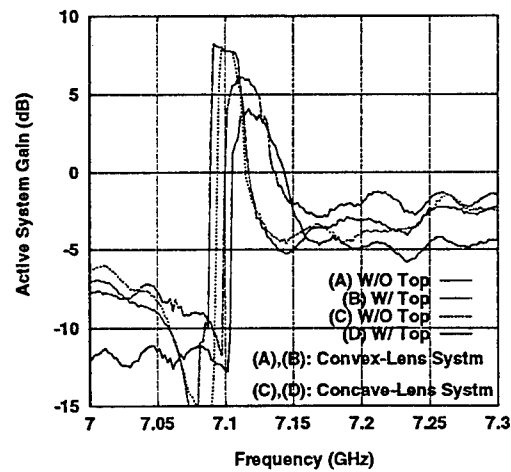


Figure 7: Active system gain for convex-lens and concave-lens systems.

GaInP/InGaAs MODFETs on GaAs grown by OMVPE for high frequency and power applications

†Boris Pereiaslavets, ‡Karl Bachem, †Jürgen Braunstein,
and †Lester F. Eastman

†Cornell University, School of Electrical Engineering, Ithaca, NY 14853-5401

‡Fraunhofer Society, IAF, Tullastr. 72, D-79108 Freiburg, Germany

Abstract

Ga_xIn_{1-x}P/In_yGa_{1-y}As/GaAs MODFETs with a pseudomorphic barrier and a pseudomorphic channel were grown by OMVPE. This Al-free material system is the most promising material system for advanced MODFETs on GaAs for high frequency and power applications. Record 2DEG carrier densities of $3.1 \cdot 10^{12} \text{cm}^{-2}$ for single sided MODFET were measured. 0.25 μm device yield 0.45 W/mm rf power.

1. Introduction

There is a high demand in a low noise power MODFETs. Ga_xIn_{1-x}P is a very promising barrier material for the MODFET fabrication on GaAs substrates for RF and power applications. Following the initial simple analytical design by Eastman [1], MODFET structures were grown by OMVPE [2] The novel concept of grading the barriers was implemented in these structures. Grading the channel results in further improvement [3]. Hall measurements were made on the wafers and compared well with the predictions.

The idea of graded barriers is given in section two. Hall data of the designed structures are shown in section three. Device fabrication and results are given in section four. Section five summarizes the paper.

2. Concept of graded barriers

There is a simple way of optimizing MODFET structures. A conduction band profile of a conventional MODFET is shown schematically in fig. 1(a). As can be seen from this figure the problem of this structure is the dip in the conduction band due to the d-doping. Since this region is closest to the Fermi level a high probability arises to accumulate parasitic charges there. The solution of this problem is to increase the distance of the dip to the Fermi level by increasing the Ga mole fraction in the Ga_xIn_{1-x}P barrier. Therefore the barrier will be pseudomorphic and still be constrained by the Matthews-Blakeslee limit [4] However, it is not necessary to strain the whole barrier. It is important to raise the potential of the mainly problematic part of it. In the case of GaInP one needs to increase the GaP concentration at the doped region. The Ga composition in the graded barrier is shown schematically in fig 1(b). The resulting conduction band profile is shown schematically in fig 1(c). The advantages of the graded barriers are obvious. First of all they lead to the

enhanced electron sheet density. The simple analytical model [1] showed 30% increase of the carriers in the channel. Second, material can be strained to a higher value where needed. And the most important is the reduced amount of parasitic electrons in the barrier.

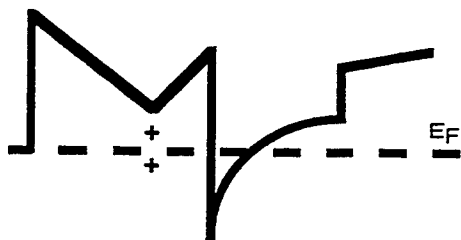


Fig. 1(a) Conventional MODFET Conduction Band

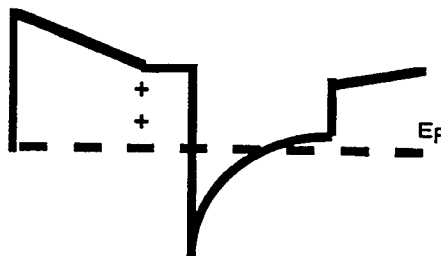


Fig. 1(c) Ideal Conduction Band after Grading

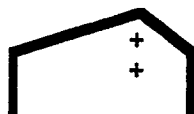


Fig. 1(b) Grading of the Ga Composition in GaInP

The graded barrier MODFET layer structure was grown at the Fraunhofer Institute [2]. An example of the layer structure is shown in table 1.

Table 1. Graded barrier MODFET, layer structure.

Material	In Composition	Description	Doping 10^{18}	Thickness (Å)
GaAs	0	Cap layer	Si 5	200
GaInP	0.5	Barrier	n.i.d.	106
GaInP	0.35	Barrier	n.i.d.	30
GaInP	0.25	Supply layer	Si 13	24
GaInP	0.35	Spacer	n.i.d.	30
GaInP	0.5	Spacer	n.i.d.	10
GaAs	0	Smoothing Layer	n.i.d.	10
GaInAs	0.22	Channel	n.i.d.	120
GaAs	0	Buffer	n.i.d.	100

The Hall measurements are shown in fig.2. As one can see the mobility of the single side doped transistors is above $6100\text{cm}^2/\text{Vs}$ and for the double side doped devices with graded channels it is above $5800\text{cm}^2/\text{Vs}$ at room temperature.

5. MODFET fabrication and device results

MODFET fabrication was done in a standard way utilizing the GaInP / GaAs system advantages. Mesa definition was carried out by wet etching. An acetic acid based etchant was chosen. The selectivity between GaInP and GaAs was 1:1. The mesa definition was followed by ohmic contact formation. Au/Ag/AuGe/Ni metal was evaporated for the ohmic contacts, followed by rapid thermal annealing for 10s. Several annealing temperatures

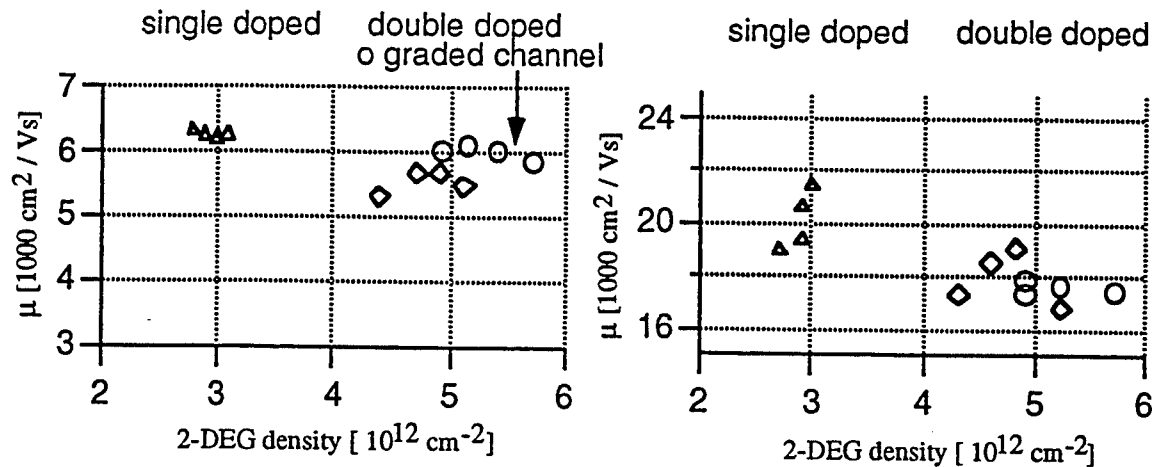


Fig. 2 Hall results for 300K (a) and 77K (b). Graded channel mobilities are higher at room temperature.

were investigated to minimize the contact resistance. $0.15\Omega\text{mm}$ ohmic contacts for single side doped MODFETs were achieved at the temperatures between 390 and 400°C.

0.1 — 0.25 μm mushroom gates were defined using electron beam lithography. Recess etching was done with a phosphoric acid based solution. The selectivity between GaInP and GaAs is >300. Such a selectivity cannot be achieved for AlGaAs/GaAs MODFETs.

Device results are shown in fig. 3. The single side doped layer design was optimized for 0.25 μm gate length MODFETs which have good DC performance. Fig. 3(a) shows the IV curve for such a device. The saturation current is nearly 640mA/mm with a negligible gate current of less than 1mA/mm. A recent publication reported saturation currents of only 550mA/mm with a doped channel [5]. Rf power was estimated as $1/8 \cdot \Delta I \cdot \Delta V$. It is as high as 450mW/mm. Future transistor designs will shift the threshold voltage towards more positive values to make use of the device's potential for power applications. The transconductance, as shown in fig. 3(b), is 560mS/mm with a drain bias of 1.5V and a current of 224mA/mm. With the output conductance of 15mS/mm at this bias point a voltage gain of about 37 is achieved. No dispersion was observed between DC and RF data. The 0.25 μm gate length MODFETs achieved f_T 's about 70GHz. Record RF performance for this material system can be reported here for 0.1 μm devices with $f_T = 106\text{GHz}$ and $f_{\text{max}} = 188\text{GHz}$. With an optimized design for short gate lengths like 0.1 μm f_T values greater 200GHz and f_{max} greater 300GHz can therefore be expected soon.

7. Summary

MODFETs with record characteristics for the GaInP/GaAs system were successfully fabricated and tested. The device structures implement new ideas of graded barriers. The rf power of 450mW/mm was achieved. The carrier sheet density of the 2D electron gas is as high as $3.1 \cdot 10^{12}\text{cm}^{-2}$ for single side doped MODFETs. The saturation current of the devices was 640mA/mm with a negligible gate current of less than 1mA/mm. Record RF performance for this material system can be reported for 0.1 μm devices with $f_T = 106\text{GHz}$ and $f_{\text{max}} = 188\text{GHz}$. Advantages of GaInP over AlGaAs now become obvious.

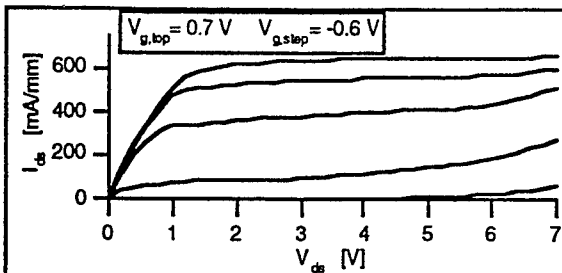


Fig. 3(a) 0.25 μ m 100 μ m MODFET.
Output conductance is 15mS/mm.

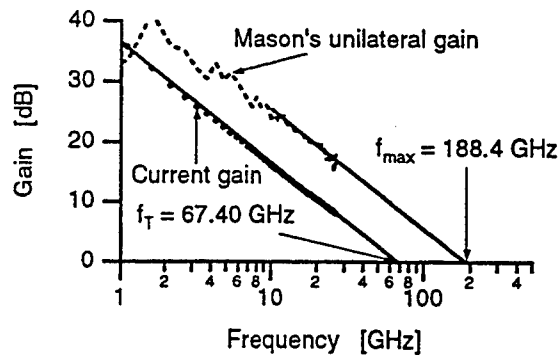


Fig.3(b) 0.1 μ m · 70 μ m MODFET. $V_{ds} = 4V$.

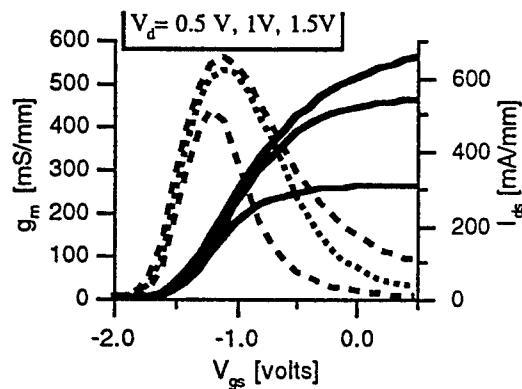


Fig. 3(c) 0.25 μ m 100 μ m MODFET.
Maximum g_m at $V_{ds}=1.5V$ is
460mS/mm

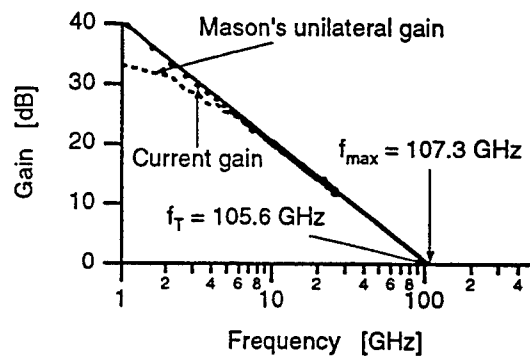


Fig. 3(d) 0.1 μ m · 100 μ m MODFET. $V_{ds} = 1.5V$.

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Low Frequency Triggering of Oscillators with a Series Connection of Tunneling Diodes

Olga Boric-Lubecke, Dee-Son Pan, and Tatsuo Itoh

Department of Electrical Engineering, University of California at Los Angeles,
405 Hilgard Avenue, Los Angeles, CA 90095-1594

ABSTRACT

RF triggering of oscillators with series-connected tunneling diodes was shown to be an effective method to overcome the biasing problem associated with the DC instability of the series connection. Excitation with the signal of frequency as low as one-sixth of the oscillation frequency was reported so far. The experimental demonstration of RF triggering with the signal at frequency as low as 200 Hz is reported here, for a 2 GHz oscillator with two tunnel diodes connected in series. This findings show practically that there is no lower limit on the triggering frequency, as long as triggering power can be sufficiently increased.

INTRODUCTION

A Resonant Tunneling Diode (RTD) can generate signals at frequencies above 700 GHz, but with the output power of less than a μW [1]. Connecting several tunnel diodes in series was shown to be a feasible method for increasing the output power of oscillator circuits using these devices at low frequencies [2]. Since RTD's and tunnel diodes exhibit very similar behavior, this scheme was also proposed to increase the power of RTD oscillators at millimeter-wave frequencies [3]. As was originally observed in [2], biasing difficulties are the main disadvantage of an oscillator with several tunneling (RTD or tunnel) diodes connected in series. If a DC voltage sufficient to bias all tunneling diodes in the middle of the negative differential resistance (NDR) region is applied gradually, the DC instability will divide this voltage so that all the diodes are biased in the positive

differential resistance (PDR) region. An external RF source may be used to switch the bias points from the PDR region to the NDR region, and initiate the oscillation. RF triggering with the signal of frequency close to the oscillation frequency (fundamental excitation) was originally proposed in [4]. Fundamental excitation was demonstrated in proof-of-principle experiments at microwave frequencies, for oscillators with two, three and four tunnel diodes connected in series [5, 6, 7]. Triggering by an RF signal at considerably lower frequency (subharmonic excitation) was also proposed [8], and experimentally demonstrated [6]. Subharmonic excitation was reported with the signal at frequency as low as one-sixth of the oscillation frequency [6].

In this paper, we report new experimental findings that show that there is no lower limit on the frequency of the triggering signal. CW signal at frequency as low as 200 Hz was successfully used to initiate 2 GHz oscillation in an oscillator with two tunnel diodes connected in series. This low frequency triggering may be very significant for the generation of signals at millimeter- and submillimeter-wave frequencies.

THEORETICAL CONSIDERATIONS

Series connection of tunneling diodes is initially biased with a DC battery, with a voltage sufficient to bias all diodes in the middle of the NDR region. In this state all diodes are biased in the PDR region, and conductive currents through all diodes are equal. When an RF signal is applied, the DC components of the conductive currents

will change due to the high nonlinearity of tunneling diode I-V curve. This change in current will initiate the motion of DC bias points towards the NDR region [6]. If the triggering signal has a sufficiently large power, diode bias points will eventually switch to the NDR region. After the triggering signal is turned off, oscillation may build-up and sustain, depending on initial conditions in the circuit. In some cases, oscillation signal already exists during excitation, which makes it easier for the oscillation to be sustained [9]. The exact mechanism through which an oscillation builds-up and sustains will be published later.

Signal at any frequency may be used to switch the bias points from the PDR to the NDR region, provided that sufficient power is applied. Voltage amplitude on each diode during excitation has to be sufficiently large to trigger and carry on the rectification process. At very low frequencies, another phenomena will constrain the excitation power. Even though a single tunneling diode does not have a lower limitation on the oscillation frequency, series connection exhibits a low frequency cutoff associated with the DC instability [10]. At frequencies below this low frequency cutoff bias points cannot be maintained in the NDR region during free-running oscillation. However, if an RF signal of such a low frequency is applied externally, bias points can be maintained in the NDR region provided that voltage amplitude on each diode is large enough. Therefore, signals of frequencies below the low frequency cutoff can be used for triggering, but required power will be very high.

EXPERIMENTAL RESULTS

Since RTD's were not available, back tunnel diodes manufactured by Metelics Co. (M1X1168) were used for the experiment. Tunnel diode, oscillator configuration and experimental set-up are described in detail in [5,6]. Several oscillators were designed at 2 GHz with two series-connected tunnel diodes, for oscillation amplitudes between 0.14 V which is the minimum oscillation amplitude [10], and 0.176 V at which negative

differential conductance approaches zero. The RF excitation signal is applied to the oscillator circuit through a circulator. An HP 8350B sweep oscillator with HP 83592C plug-in was used as an external RF source for excitation frequencies above 1 MHz. Wavetek programmable waveform generator, model 154, was used to supply the excitation signal at lower frequencies. The oscillator signal was detected by an HP 8562A spectrum analyzer. By monitoring current through diodes, it was possible to determine when bias points switched to the NDR region.

Excitation was attempted with signals of frequencies below 100 MHz. Similarly as for subharmonic excitation reported in [6], low frequency excitation was possible in all circuits but for circuit which was designed for the smallest oscillation amplitude of 0.14 V (circuit 2D2 in [6]). Switching of bias points, judged by a current level, was possible with any frequency in all circuits provided that power level was adjusted. In all cases, oscillation was not always sustained, and the probability of successful excitation was very much dependent on the excitation power. As discussed previously, for each frequency there is a low power limit below which switching cannot happen. As triggering power increases, switching happens always, and probability of sustained oscillation increases to a certain point. During excitation, different spectrum is observed as a function of triggering frequency and power.

Fig. 1 shows the spectrum of the triggering signal, for the triggering frequency of 1.767 MHz, and the triggering power of 5 dBm. At such low frequencies signal generator produces high harmonics, but they are still about 20 dB lower than the fundamental and should not affect the excitation. Power shown in the spectrum is the power reflected from the oscillator, and therefore considerably lower than 5 dBm (-12 dBm). There is also about 3 dB loss in the measurement system. Fig. 2 shows the oscillator spectrum during and after triggering with the signal of frequency 1.767 MHz, for the circuit designed at the oscillation amplitude of 0.176 V (circuit 2D5 in [6]). Since triggering frequency is

thousand times lower than the oscillation frequency, oscillator signal is shown on a different scale. For the triggering power of -10 dBm, oscillation signal is present during excitation (Fig. 2(a)). This signal is stable but not clean, it is about 6 dB lower in power than the free-running oscillation signal and its frequency is somewhat lower than the free-running frequency (Fig. 2 (c)). For the triggering power of 5 dBm, oscillation signal at 2.042 GHz is clearly visible during excitation, but there is also a stronger component at 1.957 GHz. During triggering, power is exchanged between these two spectral lines, and their frequencies also shift slightly. Fig. 2(b) shows one snapshot of the spectrum for such a case.

After the triggering signal was turned off, oscillation was not always present in the circuit. Experiment was repeated at least twenty times for each triggering power, to determine the probability of the sustained oscillation. For the triggering power from -15 dBm to -10 dBm, probability was about 10 %. As triggering power was increased, probability gradually increased to about 50 %, at -4 dBm. As power was further increased, probability started to decrease, and at 5 dBm it was about 30 %. Once initiated, the output signal of the oscillator was completely independent of the excitation signal power and frequency (Fig. 2(c)).

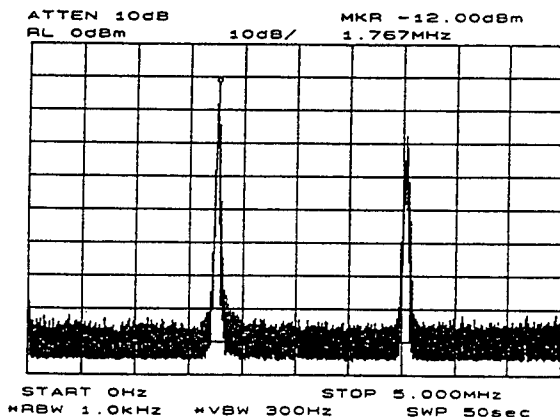
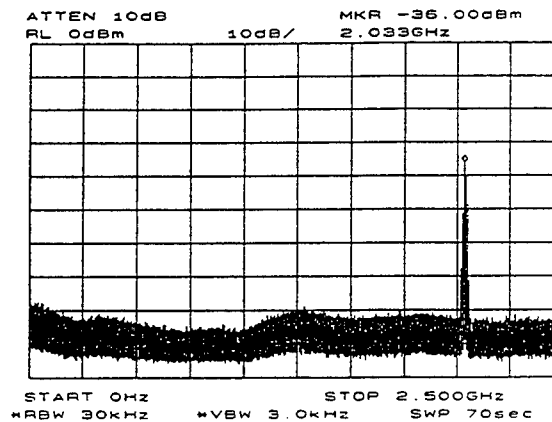
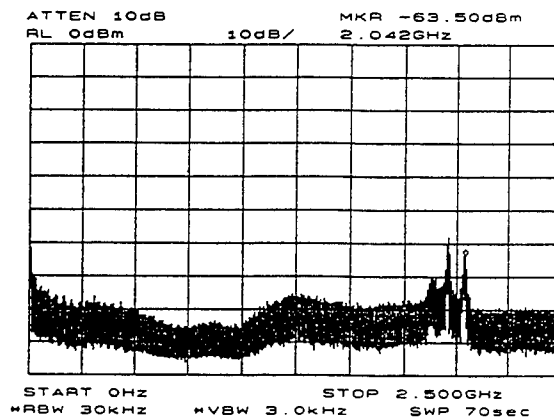


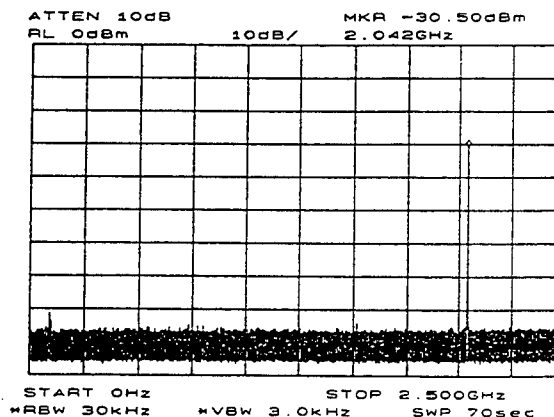
Fig. 1 Spectrum of the triggering signal of frequency 1.767 MHz and power of 5 dBm.



(a)



(b)



(c)

Fig. 2 Oscillator signal during triggering with the signal of frequency 1.767 MHz and power of (a) -10 dBm and (b) 5 dBm, and (c) after the triggering signal was turned off.

Excitation was possible with the signal of frequency as low as 200 Hz, with the probability of about 30 %. At this frequency maximum power that can be supplied by Wavetek generator was used (9.99 V of peak-to-peak amplitude if delivered to 50 Ω), and therefore lower frequency excitation could not be tested. During excitation with the signal at frequency of 200 Hz, oscillator signal was always present, and it exhibited chaotic behavior. Frequency and power of the spectral components were constantly changing, with some components temporarily disappearing.

CONCLUSIONS

RF triggering is an efficient method to circumvent the biasing problem of series-connected tunneling diode oscillators. We reported new experimental findings that show that there is no lower limit on the triggering frequency, as long as triggering power can be sufficiently increased. CW signal at frequency as low as 200 Hz was successfully used to initiate 2 GHz oscillation in an oscillator with two tunnel diodes connected in series. In this case, excitation frequency is not related to the oscillation frequency, and therefore it does not necessarily increase as oscillation frequency increases. Even though this low frequency triggering is not 100 % repeatable, it still may be useful for the generation of signals at millimeter- and submillimeter-wave frequencies.

ACKNOWLEDGMENT

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Semi-classical effects of ballistic electrons in Schottky diodes

D. W. van der Weide

Abstract—Modern small Schottky diodes have anode diameters $d \sim 20\lambda_F$, the electron Fermi wavelength in the semiconductor, and hence may exhibit indirect evidence of an electron standing-wave effect at room temperature under AC stimulus. They can thus be modeled as dynamic Sharvin point contacts (using only d and λ_F) to get a frequency-scaled bias current for lowest noise. Published observations of this bias condition are well-predicted by this new model.

I. INTRODUCTION

MUCH attention lately has been focused on structures and conditions in which electron transport is quantized[1]. For cases in which a geometrical constriction in a conductor gives rise to quantized conduction, the Fermi wavelength of the electrons λ_F is typically on the order of the width of the constriction d , while the elastic mean-free path of electrons l_e is long compared to the length of the constriction l . These conditions for “ballistic quantum transport”[2] often involve using patterned semiconductor heterostructures at cryogenic temperatures; they rely on two-dimensional (2-D) electron reservoirs connected by one-dimensional (1-D) constrictions.

Ballistic electrons—those which undergo no inelastic scattering events and maintain their phase coherence[3]—can also be prepared in bulk (3-D) semiconductors. For GaAs, the technique of “hot-electron spectroscopy”[4] shows $T = 4.2$ K ballistic transport, while at $T = 300$ K, Fermi velocities are at least 2×10^7 cm/sec and characteristic times for LO phonon relaxation have been measured at $< 200 \times 10^{-15}$ sec[5], which would give a “ballistic horizon” of ~ 400 Å. For most experiments, this length is too short to directly observe effects of room-temperature quantized transport through a constriction at DC; indeed, conductance steps of the “Coulomb staircase” in 1-D quantum point contacts[6] are thermally smeared out even at $T < 10$ K[2], so at room temperature one expects the DC conductance to be ensemble-averaged to a bulk, macroscopic value.

In short, experiments seeking direct evidence of quantized conduction have most often been performed at cryogenic temperatures on patterned heterostructures at DC. Here I point out, however, that an indirect observation of phase-coherent 3-D electrons traversing a 2-D constriction can be (and likely has been[7]) made at room-temperature under AC stimulus, specifically under conditions for highest sensitivity (i.e. lowest noise) operation in small (diameter $d < 1 \mu m$) n -type GaAs Schottky mixer diodes. Such

diodes are widely used in receivers for radio astronomy[7], [8] because they have junction capacitances $C_j \sim 10^{-15}$ F, together with low series resistance R , resulting in RC cut-off frequencies on the order of 10^{13} Hz. Despite their importance, however, a complete picture of the conduction mechanism in such Schottky contacts has yet to emerge.

II. DYNAMIC SHARVIN POINT CONTACT (DSPC) MODEL

For operation as a mixer (multiplying two high frequencies to get the difference) or as a detector (rectifying only one frequency for DC output), a small Schottky diode is biased to near-forward conduction (“flat-band”). As shown in Fig. 1, an AC electric field at frequency ν applied across the diode (here via antenna coupling) drives it from reverse bias into forward conduction with period $1/\nu$. For this DSPC model, AC conduction current I arises from a packet of N ballistic electrons accelerated from the edge of the depletion region in the semiconductor bulk through the small Schottky contact, a 2-D constriction whose length $l < \lambda_F$ and whose diameter $d \sim 20\lambda_F$. Like an over-moded microwave waveguide[9], spin-paired electron waves should form transient 2-D conduction channels in the constriction up to N_{ch} , the maximum number determined by d and $k_F = 2\pi/\lambda_F$ (set by doping density in the semiconductor n_d), beyond which point excess electrons are reflected back into the semiconductor, a noisy process of inelastic scattering. If $N < N_{max} = 2N_{ch}$, however, the signal current could still be increased by changing V_{bias} , I_{bias} and/or V_{rad} , the amplitude of the AC electric field (Fig. 1). Thus, by varying these three parameters (which can be done independently and with considerable precision), one would expect to measure an optimum diode current at highest sensitivity,

$$I_{opt} = qN_{max}\nu, \quad (1)$$

where q is the electronic charge. At this optimum, a countable number ($N_{max} \sim 10^3$) of electrons should traverse the diode junction with period $1/\nu$, independent of ν . Equation 1 has in fact been reported for different n -type GaAs Schottky mixer diodes by Röser *et al.*[7], [10] over a very wide frequency range, $3 \text{ GHz} < \nu < 3 \text{ THz}$. Attempting to increase diode current beyond I_{opt} will increase inelastic scattering, hence also junction shot noise[11]. Mixing sensitivity thus decreases with more inelastic collisions and resultant heating; if the current density and voltage in these small diodes is not limited to $< 10^6$ A/cm² (~ 1 mA for the “1T15” diode type[12]) and $V_{bias} < 20\%$ above flat-band[8], sensitivity is permanently lowered. By contrast, when $N = N_{max}$ for coherent transport through a constrict-

The author is with the Department of Electrical Engineering, University of Delaware, Newark, DE 19716-3130. E-mail: dan@eecis.udel.edu

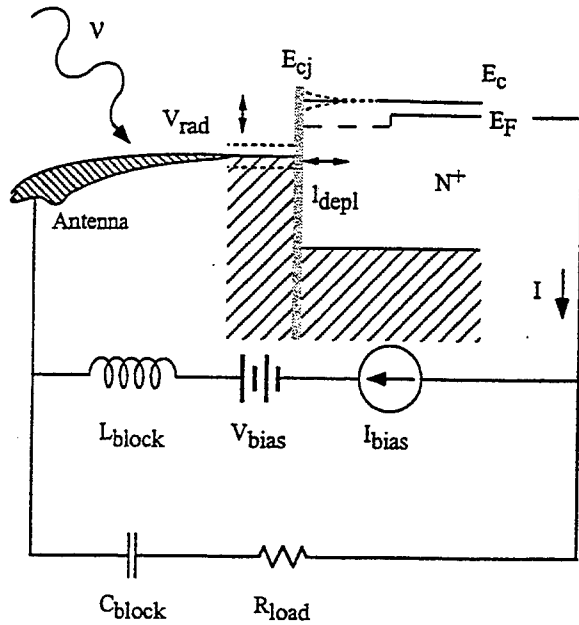


Fig. 1. Band diagram of a Schottky diode under near-forward bias, together with external circuitry to form a frequency mixer: the output current appears as a signal on R_{load} . Also shown is the tip of a wire antenna, which acts as a transducer of incoming high-frequency radiation to modulate the conduction-band energy at the junction, E_{cj} , with AC voltage V_{rad} . This modulation periodically creates a depletion region of depth l_{depl} . The Schottky contact is deliberately depicted as having a short transition region [24], and the diode backside contact is indicated as N^+ .

tion, Landauer and Martin[13] argue that, because electrons obey Fermi statistics, “a fully occupied set of states, within a given energy range, is noiseless.” They argue further that Coulomb repulsion tends to “smooth out” the current flow through a constriction; both arguments reinforce the observations in [7] and this DSPC model.

The universality of this AC effect is supported by similar observations of maxima in the responsivity γ [14] of metal-insulator-metal (MIM) diodes[15]. While the peak γ of MIM diodes is lower than that of Schottky diodes, it is a weak (nearly flat) function of frequency from 0.6–30 THz, while peak γ of a Schottky diode rolls off at ~ 20 dB/decade at higher ν , presumably because of comparatively large parasitic resistances of the semiconductor and its ohmic contact[16] (see Fig. 1).

III. DEVELOPMENT OF THE DSPC MODEL

Now I explain and model this effect as a dynamic Sharvin point contact (DSPC). The semi-classical conductance obtained by Sharvin[17] of a 2-D constriction connecting two ideal conductors is often cited in the study of mesoscopic systems[18] and point-contact spectroscopy of metals[19]. The constriction and k_F give rise to a limited number of conductance channels N_{ch} , each channel having conduc-

tance $G_{ch} = e^2/h$, ignoring spin.

The condition of ballistic transport needs closer examination, and might seem difficult to achieve in a real device at room temperature[9], though most discussions of this topic implicitly assume quasi-DC measurements whereas I describe an AC effect. The semiconductor part of the diode at flat-band bias provides electrons via diffusion from the backside contact to the edge of the depletion region. There, the electric field periodically accelerates electrons through the constriction in a time less than that for inelastic scattering. Such collisions could be with longitudinal optical phonons (at $\hbar\omega_o = 0.035$ eV in GaAs[20]), electron-electron collisions (less likely in highly-doped semiconductors due to screening[21]), impurity scattering (dependent on material quality), and roughness at the perimeter of the anode (dependent on the fabrication process and difficult to predict). With impurity scattering, the above-mentioned “ballistic horizon” of ~ 400 Å could be somewhat shorter[22], but still exceeds the depletion depth from which electrons travel to the junction ($l_{depl} \approx 310$ Å for the “1112” diode type[7]). Finally, cryogenic cooling of the diodes has only a minimal effect on the measured noise[23], so it is reasonable to suppose that the electrons are already ballistic at room temperature.

There are “non-idealities” in the metal-semiconductor diode which could actually reinforce the effect. The interface between a metal and a compound semiconductor is not abrupt on the 10–100 Å scale—though still shorter than λ_F —but rather encompasses an extended region of metal-induced gap states[24], [25], as indicated in Fig. 1. This DSPC model draws on the analogy between the modes in a microwave waveguide and the electronic eigenstates in the constriction[9]: the scattering of electrons back into the semiconductor (where their phase would be destroyed by the thermal bath) could be suppressed in part due to this smoother transition, in a manner analogous to a dielectric “matching layer” which slows electromagnetic waves and reduces reflections. My simple model has also ignored the mismatch in electron effective masses between the metal and the semiconductor[26], but these two “non-idealities” in fact may lengthen the time the sheet of ballistic electrons spends in the constriction.

Thus, for the DSPC model I assume an ideal 2-D constriction with no inelastic scattering (in particular no backscattering) for packets of ballistic electrons with $N \leq N_{max}$, and ignoring higher-order terms due to perimeter roughness and to fluctuations of geometry (which are negligible for the diodes here)[27], I calculate both I_{opt} and the dynamic junction conductance G_{ch} resulting from the N_{ch} conduction channels; because $l < \lambda_F$ in the constriction, only two electrons per channel are allowed during the conduction event.

To find N_{ch} , I calculate k_F in the 3-D bulk by assuming all states below E_F are filled; the heavy doping n_d of the epitaxial layer makes this zero-temperature argument more plausible[21]:

$$\frac{2}{(2\pi)^3} \frac{4\pi}{3} k_F^3 = n_d. \quad (2)$$

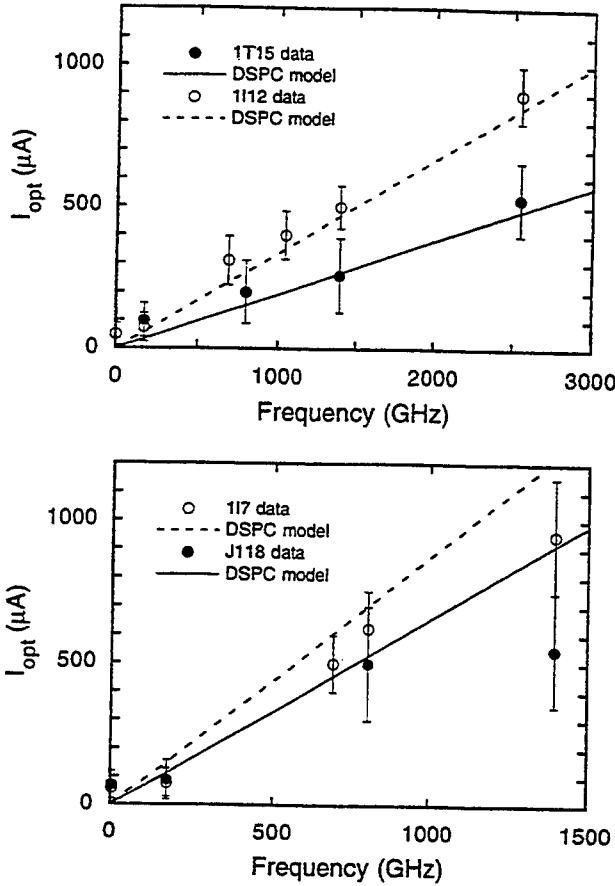


Fig. 2. Comparison of optimum mixing current I_{opt} from DSPC model to measured data. Data for diode type "1T15" from [10]; other data from [7]. What appear as error bars are in fact "tuning ranges" [7] over which lowest noise in mixing changes by < 10 %.

I project this 3-D k_F onto the 2-D area S of the (junction) constriction, which limits the areal density of conductance channels, n_{ch} :

$$\frac{1}{(2\pi)^2} \pi k_F^2 = n_{ch}. \quad (3)$$

Finally, $N_{ch} = S n_{ch}$.

Using this model, I calculate I_{opt} for four different diode types according to Eq. 1 and compare the results to measured data in Fig. 2. As expected, agreement of the model with the data is better for smaller, more highly-doped diodes, while for the larger, lower-doped diode types, the data deviate systematically from the frequency-independent DSPC model. This deviation could result from more inelastic collisions due to $l_{depl} > l_e$ arising from the lower n_d of these diodes. Numerical details are given in Tables I and II.

The DSPC model can also be used to calculate a dynamic

TABLE I
DIODE PARAMETERS: DOPING LEVEL NEAR THE JUNCTION IS n_d ;
SCHOTTKY CONTACT DIAMETER IS d ; k_F IS CALCULATED FROM n_d .

Diode type	n_d (cm^{-3})	d (μm)	k_F (cm^{-1})
1T15	1.0×10^{18}	0.25	3.90×10^{-6}
1I12	4.0×10^{17}	0.45	2.87×10^{-6}
1I7	3.0×10^{17}	0.8	2.61×10^{-6}
1J118	2.0×10^{17}	1.0	1.81×10^{-6}

TABLE II
DSPC MODEL RESULTS: n_{ch} FROM k_F *bulk* AND EQ. 3; N_{max}
RESULTS FROM n_{ch} AND JUNCTION AREA; I_{opt} RESULTS FROM EQ. 1
AT $\nu = 1000$ GHz.

Diode type	n_{ch} (cm^{-2})	N_{max}	I_{opt} (μA)
1T15	12.1×10^{11}	1190	190
1I12	6.56×10^{11}	2090	330
1I7	5.42×10^{11}	5450	870
1J118	2.60×10^{11}	4090	660

junction conductance,

$$G_{ch} = \frac{2e^2}{h} N_{ch} = \frac{2e^2}{h} \pi \left(\frac{d}{2}\right)^2 \left[\frac{1}{(2\pi)^2} \pi k_F^2\right]. \quad (4)$$

If each channel is independent and effective, the series resistance due to the channels is the reciprocal of Eq. 4; this should be a measurable fraction of the total diode series resistance [16]. Strictly speaking, this expression assumes the cross-sectional area of the constriction $S = \pi(d/2)^2 \ll l_e^2$ [18]. This is not the case here, since for gold at room temperature, $l_e \approx 400$ Å, and for the diodes, $l_e < 500$ Å, while $0.25 < d < 1.0$ μm. However, I take the condition of ballistic *longitudinal* transport as the most important one for AC operation.

In summary, I have proposed that a semi-classical effect of periodically-created electron standing waves is responsible for the observation of systematic conditions for peak sensitivity in small Schottky mixer diodes. I have developed a dynamic Sharvin point contact model whose results agree quite well with measured data from different devices, so it appears the effect falls in the "middle ground" between transport which is completely coherent and that which is completely incoherent [9]: transport coherent on a short time scale.

IV. CONCLUSIONS

While the DSPC model shows that today's smallest, most highly-doped GaAs diodes probably attain geometrically-limited maxima in sensitivity (given n_d), it also suggests that slight improvements might come from whatever would reduce inelastic scattering near flat-band conditions, such as smoother anode perimeters or fewer impurities. Other materials with longer l_e at room temperature, such as InP, may enable diode designers to reduce

dynamic capacitance by allowing lower doping levels and longer l_{depl} while still achieving transient ballistic transport.

Second, with this AC model it is no longer clear what role, if any, is played by the (disordered) contacts; their role in quasi-DC transport has been the subject of much discussion [28]. Since this effect is dynamic, and the electron standing waves are only transient entities, their interaction with the originating Fermi sea may no longer be important.

Finally, determination of N_{max} via peak sensitivity could be an interesting new probe of high-frequency transport in metal-semiconductor contacts since the wire antenna as a field transducer enables such a wide range of energetic stimulus. One could effectively measure l_e for example by raising the temperature of the diode while monitoring this effect, looking for a significant increase in noise due to loss of ballistic conditions.

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Numerical Device/Harmonic-Balance Circuit Analysis of Schottky Barrier Varactors

L. F. Horvath, J. R. Jones, S. H. Jones, G. B. Tait[†]

Department of Electrical Engineering, University of Virginia, Charlottesville, VA 22903

[†]Department of Electrical Engineering and Computer Science, United States Military Academy, West Point, NY 10996

Introduction

The design of nonlinear circuits including frequency multipliers requires an understanding of the strong interaction between the nonlinear active device and its linear embedding circuit. Our approach to the analysis and design of high frequency nonlinear circuits uses a physics-based numerical device model coupled with a harmonic-balance circuit analysis technique. Recently novel device simulators have been designed for generic InGaAs/InP and GaAs/InGaAs/AlGaAs Heterostructure Barrier Varactors (HBVs) [1], for GaAs Schottky Barrier Varactors (SBVs) [2], and for InP, GaAs, and GaN Transferred Electron Oscillators (TEOs) [1,3]. In this paper we report on a robust simulator which has been developed for GaAs and InP SBV frequency multipliers with arbitrary doping profiles. The large-signal time- and temperature-dependent numerical device simulator facilitates a self-consistent analysis with good convergence properties and speed. The novel and efficient harmonic-balance circuit simulation technique is specifically designed to expedite the inclusion of a numerical device simulator. The use of the numerical device model in conjunction with the harmonic-balance circuit model allows co-design from both a device and circuit point of view.

Frequency Multiplier Simulation

Numerical Device Simulation Technique

Carrier transport through the bulk region of the SBV has been described [2] by a set of coupled nonlinear differential equations. The numerical device simulator is based on the first two moments of the Boltzmann transport equation coupled to Poisson's equation. The resulting equations are

$$\frac{\partial n(x,t)}{\partial t} = \frac{1}{q} \frac{\partial J_n(x,t)}{\partial x}, \quad (1)$$

$$J_n(x,t) = -q\mu_n(x,t)n(x,t) \frac{\partial \phi_n(x,t)}{\partial x}, \quad (2)$$

and

$$\frac{\partial}{\partial x} \left[\epsilon(x) \frac{\partial \psi(x,t)}{\partial x} \right] = q[n(x,t) - N_D(x)], \quad (3)$$

where

$$n(x,t) = n_{i,ref} \exp \left[\frac{q}{kT} (\psi(x,t) + V_n(x) - \phi_n(x,t)) \right], \quad (4)$$

and where n is the electron density, q is the electron charge, J_n is the electron particle current density, ϕ_n is the electron quasi-Fermi potential, ψ is the electrostatic potential, $n_{i,ref}$ is the intrinsic electron density in

the reference material (GaAs or InP), k is Boltzmann's constant, T is absolute temperature, and V_n , μ_n , N_D , and ϵ are the spatially-dependent alloy potential [4], electron mobility, donor impurity concentration, and dielectric permittivity, respectively.

In an attempt to account for hot electron effects and high-field velocity saturation effects, field- and temperature-dependent mobility is considered here. Mobility values were computed from three-valley Monte Carlo simulations under static electric field conditions [3]. These static mobility values differ somewhat from the high-frequency values, but give a good approximation compared to low field values and yield significant insight into the physics of electron transport. For InP and GaAs, mobility values were obtained at 50 degree increments from 300 to 500 K, for fields of 1 to 100 kV/cm with uniform doping concentrations of $1 \times 10^{16} \text{ cm}^{-3}$, $5 \times 10^{16} \text{ cm}^{-3}$, $1 \times 10^{17} \text{ cm}^{-3}$, and $5 \times 10^{17} \text{ cm}^{-3}$.

The transport equations are solved at discrete points throughout the device using a finite-difference approximation to the differential equations over a user-defined mesh. The total device current density is the sum of J_n and J_D where J_D , the displacement current density, is given by

$$J_D(x,t) = \epsilon(x) \frac{\partial}{\partial t} \left[\frac{\partial \Psi(x,t)}{\partial x} \right] \quad (5)$$

For accurate modeling of SBVs, current transport through the device bulk is combined with thermionic and thermionic-field emission current imposed at the metal-semiconductor contact. This approach is analogous to the analytical thermionic-emission/diffusion theory of Crowell and Sze [5]. Following the work of Adams and Tang [6,7], we have adopted a current density boundary condition at the metal-semiconductor interface which assumes a drifted Maxwellian electron distribution at the interface. This boundary condition allows us to avoid the unphysical accumulation of electrons at the metal-semiconductor interface above the flat-band voltage. The resulting current density interface constraint at $x=0$ is

$$J_n(0,t) = qv_{r,n} [n(0,t) - n_o] \quad (6)$$

where $n(0,t)$ is the electron density at the metal-semiconductor interface and n_o is the equilibrium electron density at the interface. The effective surface recombination velocity for electrons is

$$v_{r,n} = v_d + \sqrt{\frac{2kT}{\pi m^*}} \left[\frac{\exp \left[-v_d^2 \left(\frac{2m^*}{kT} \right) \right]}{1 + \operatorname{erf} \left(v_d \sqrt{\frac{2m^*}{kT}} \right)} \right] \quad (7)$$

where m^* is the effective electron mass at the metal-semiconductor interface. The amount of drift in the electron distribution at the metal-semiconductor interface is modeled as

$$v_d = \frac{J_n(0,t)}{qn(0,t)} \quad (8)$$

The electrostatic potential at the metal-semiconductor interface, assuming a constant potential of zero for the metal, is

$$\Psi(0,t) = \frac{\chi_{ref} - \Phi}{q} + \frac{kT}{q} \ln \left(\frac{N_{C,ref}}{n_{i,ref}} \right) \quad (9)$$

where χ_{ref} is the electron affinity in the reference material, Φ is the metal work function, and $N_{C,ref}$ is the total effective conduction band density of states in the reference material. The barrier height at the metal-semiconductor interface, ϕ_b , is given by the first term in equation (9) multiplied by the electronic charge.

This barrier height is lowered due to the Schottky effect by the amount

$$\Delta\phi_b(t) = \sqrt{\frac{q|\xi(0,t)|}{4\pi\epsilon(0)}} \quad (10)$$

where $\xi(0,t)$ is the electric field at the metal-semiconductor interface. Tunneling of electrons also introduces a barrier height reduction term. The barrier height reduction Φ [8] is given by

$$\Phi = q\xi\Delta x_c, \quad (11)$$

where ξ is the total electric field in the barrier, and Δx_c is a fixed critical tunneling width.

Through careful investigation of solution methods we have developed a robust method with excellent numerical convergence and good speed. For ease of combining the numerical device simulator with a harmonic-balance analysis technique, the state variables J_n , ϕ_n , ψ , and D are used. The carrier transport equations are solved for a given bias voltage, and subject to the metal-semiconductor interface constraints and an ohmic contact boundary condition, using the coupled equation Newton-Raphson method.

Harmonic-Balance Circuit Analysis Technique

The novel harmonic-balance circuit analysis utilized in our simulator, termed the Accelerated Fixed-Point (AFP) method, is derived from the multiple reflection algorithm [9]. One period of the time-domain current through the device, calculated by the numerical device simulator, is used in the harmonic-balance analysis. For SBVs, as well as for TEOs, six harmonic components of the current plus the DC term are extracted from the time-domain total current waveform using a discrete Fourier transform. Thirteen harmonics plus the DC term are utilized for HBVs. The AFP method [10] is then used to update the total voltage applied across the active region of the device in terms of the circuit embedding impedances, the harmonic components of the current, and the harmonic components of the voltage from previous iterations. This iterative process is repeated until the harmonic components of the voltage converge to their steady-state values. The AFP method utilizes the fact that the nonlinear device impedance will equal the negative of the linear embedding impedance of the circuit for each of the undriven harmonics in steady-state. Frequency-dependent parasitic impedances, external to the active region of the device and similar to those of [9], are included in the analysis as additional contributions to the linear embedding circuit.

Results

Good correlation has been achieved between the SBV hydrodynamic device simulator utilizing field- and temperature-dependent mobility and experimental I-V results for the UVA 6P4 GaAs SBV frequency doubler. The experimental UVA 6P4 output power versus incident pump power is shown in Figure 1 for a pump frequency of 100 GHz. This figure also shows the simulated results obtained from the harmonic-balance circuit analysis coupled to both the analytical and hydrodynamic device models. Results from the hydrodynamic device model using field- and temperature-dependent mobility and constant electron mobility are shown.

Conclusions

An efficient and accurate large-signal time- and temperature-dependent simulator for SBV frequency multiplier circuits has been developed by combining a physics-based numerical device model with a harmonic-balance circuit analysis technique. We have demonstrated the use of this analysis and design tool in the simulation of the UVA 6P4 GaAs SBV frequency doubler. Overall, this approach allows for the self-consistent analysis of the nonlinear active device and its linear embedding circuit and provides for the careful investigation of the internal physical phenomena occurring in highly nonlinear active devices.

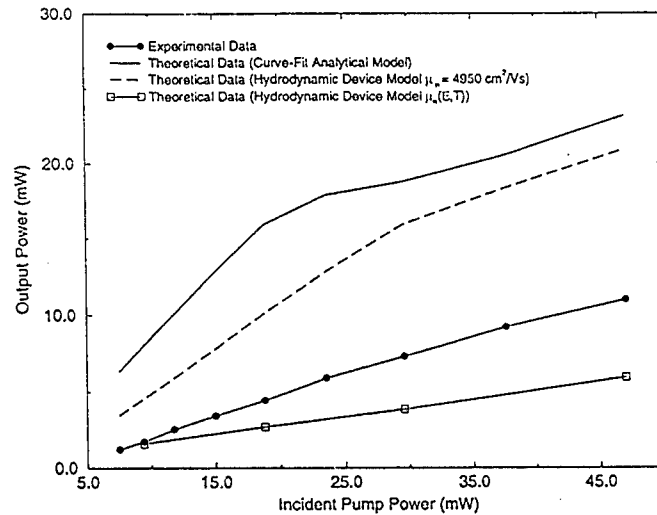


Figure 1: Experimental and theoretical doubling output power versus incident pump power for the UVA 6P4 GaAs diode subject to 100 GHz pump excitation.

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Monte Carlo Simulation of Terahertz Frequency Schottky Diodes

Udayan V. Bhapkar and Robert J. Mattauch
Semiconductor Device Laboratory
Department of Electrical Engineering
The University of Virginia
Charlottesville, VA 22903-2442, USA

Abstract

Monte Carlo simulations of degenerately-doped, GaAs Schottky diodes for terahertz frequencies are performed. It is demonstrated that the maximum velocity of the depletion layer edge imposes a limitation on their cutoff frequency, and that it substantially overshoots both the steady-state saturation velocity and the thermal velocity in bulk n-GaAs. It is shown that, up to the cutoff frequency, transit time effects cause a phase delay in the particle current that increases with frequency, and is accompanied by an increase in the magnitude of the current. The displacement current is shown to be approximately 90 degrees in phase ahead of the particle current. Beyond the cutoff frequency, both the particle and displacement current components are shown to drop abruptly in magnitude.

I. Introduction

A number of recent workers have suggested that, in the operation of terahertz frequency Schottky diodes, the velocity of the depletion layer edge may be limited by the saturation velocity of GaAs, and that this may provide an inherent physical limitation on their operation as varactors and mixers [1-3]. Other workers have remarked that, instead, the thermal velocity may limit the excursion of the depletion layer edge [4]. In this paper we answer these questions by showing results from time-dependent, one-dimensional Monte Carlo (MC) simulations of GaAs Schottky diodes. The simulations consider effects important in degenerately doped material, such as electron degeneracy and the electron-electron and electron-plasmon scattering mechanisms. The usual scattering mechanisms, such as ionized impurity, polar optical phonon, deformation potential acoustic, and intervalley scatterings, are also included. Image force lowering as well as electron tunneling through the Schottky barrier are considered. The electrons are injected from a Fermi-Dirac distribution. The assumed applied voltage waveform is an AC component at the local oscillator (LO) frequency in addition to a DC bias. The MC program, as well as the theory behind it, are more fully described in Ref. [5].

II. Simulation Results

The ionized impurity concentration of the semiconductor was assumed to be $5 \times 10^{24} \text{ m}^{-3}$. Only the "epitaxial" layer was simulated, and electrons were injected directly into the "ohmic contact" at the side opposite the Schottky contact. The simulated region was assumed to be 320 angstroms in thickness, which is substantially greater than the zero bias depletion length. The assumed voltage waveform was a 0.7 V DC bias in addition to a 0.3 V AC component, which is typical for Schottky diodes operating as mixers. The assumed Schottky barrier height was 1.0 V.

Velocity and Position of Depletion Layer Edge

In this context, the position of the depletion layer edge is defined as the coordinate at which the free electron concentration, as determined by the MC simulation, is equal to one-half of the ionized donor concentration. The velocity of the depletion layer edge is calculated by simply dividing the change in the position of the depletion layer edge by the time interval.

Figure 1a shows the velocity of the depletion layer edge, $v_{x\text{dep}}$, as a function of time, over one period, T , after achieving convergence. For the sake of comparison, we have also shown in Figure 1b the depletion edge velocities that would result simply from using the depletion approximation, given by

$$x_{\text{dep}} = \left(\frac{\epsilon(\phi_B - V)}{qN_d^+} \right)^{1/2}, \quad (1)$$

and subjecting it to a time-dependent voltage waveform, but ignoring all high frequency effects. It is clear from the illustration that the preceding approximation results in a velocity of the depletion layer edge with a step function type change when the voltage reaches the flat-band condition. Such behavior is not, of course, physically realizable because electron inertia prevents infinite, instantaneous accelerations from occurring. Instead, our MC simulations show that $v_{x\text{dep}}$ increases at a finite rate, and overshoots the

velocity curves predicted from the depletion approximation. In many cases, this overshoot is followed by velocity undershoot.

As the frequency is increased, the peak velocity of the depletion layer edge increases roughly in proportion to the frequency. The peak velocity of the depletion layer edge reaches a maximum of about 4×10^5 m/s at a frequency of 8 THz. At a frequency of 16 THz, however, the peak velocity of the depletion layer edge does not increase further beyond 4×10^5 m/s; in fact, it shows a slight decrease. Thus, we designate the cutoff frequency in this context as the frequency at which the maximum current is reached, which in this case is 8 THz.

It should be noted that these velocities are roughly four times the steady-state saturation velocity of n-GaAs. They are also substantially greater than the maximum velocities found in the steady-state velocity-field curves [5,6]. In fact, the maximum velocities we observe are even greater than the thermal velocity of GaAs, which is 2.7×10^5 m/s. The sub-picosecond time scales involved make it possible for the electrons to exhibit velocity overshoot, and not be constrained by either the steady-state saturation or maximum velocities.

The curves are far from smooth, and instead show much ringing behavior, indicating the presence of higher harmonics of the LO frequency. The ringing appears to reflect velocity overshoot and undershoot phenomena, and may also be influenced by transit time effects across the epitaxial layer. We mention that velocity overshoot and undershoot in various two-terminal devices have been predicted by others [7]. These effects are similar to the velocity overshoot and undershoot effects seen in bulk n-GaAs [8].

Figure 2a shows the position of the depletion layer edge as a function of time, and is compared with the prediction using the depletion approximation, Eqn. (1), which is plotted in Figure 2b. Below the cutoff frequency, the excursion of the depletion layer edge, as predicted by the MC simulations, is significantly greater than that predicted by the depletion approximation, and this effect increases with frequency. Evidently, a type of overshoot effect exists. The increasing excursion of the depletion layer edge coexists with an increase in the particle current through the device, which is described next. Beyond the cutoff frequency, however, it is evident that the excursion of the depletion layer edge is vastly smaller than that at lower frequencies.

Particle and Displacement Current

Figures 3 and 4 show the particle and displacement current components, respectively, as a function of time. The plots show that there is substantial particle current only during the "on" phase of the LO cycle, which corresponds to roughly the first half of each cycle. The displacement current shows a ringing behavior similar to that observed in the velocity of the depletion layer edge.

Figures 5a-b show the magnitude and phase relationships, respectively, of the particle and displacement current components, as a function of frequency. The effects of including the electron-electron and electron-plasmon scattering mechanisms are also shown. The magnitude and phase of the current components were obtained by performing Fourier Transforms of their waveforms. Figure 5b clearly demonstrates the existence of a phase delay in the particle current that, up to the cutoff frequency, increases approximately in proportion to the frequency. The time or phase delay is due to the time needed for the electrons at the depletion layer edge to travel towards the Schottky contact. We refer to this phenomenon as a transit time effect. The magnitude of the particle current, as shown in Figure 5a, increases slightly as the frequency approaches the cutoff frequency of 8 THz. Beyond this frequency, however, its magnitude drops abruptly. The cutoff frequency observed here is consistent with the frequency at which the maximum velocity of the depletion layer edge no longer increases, and is also consistent with the maximum frequency at which the full, expected excursion of the depletion layer edge can be sustained. Figure 5a also shows that the displacement current increases approximately linearly with frequency up to 8 THz, but beyond that point it decreases abruptly. This indicates an effective capacitance that is roughly constant up to the cutoff frequency. However, beyond the cutoff frequency, velocity saturation and transit effects severely reduce the charge that can be displaced, and therefore also reduce the effective capacitance of the device. Furthermore, Figure 5b shows that, up to the cutoff frequency, the phase of the displacement current stays nearly 90 degrees with respect to the particle current, as opposed to the applied voltage waveform. We remark that electron-electron and electron-plasmon scattering are shown to decrease the magnitude of the particle current and displacement current components, and this is an effect that increases with frequency.

The behavior of the particle current deviates from the classical series inductor-resistor lumped element model in that its magnitude continues to increase as the cutoff frequency is approached, even as

transit time effects increase the phase delay. By contrast, the classical series resistor-inductor circuit used to model bulk material predicts a gradual drop in the magnitude of the current: a reduction by a factor of the square root of two is expected at the corner frequency, where the phase delay is 45 degrees. In any case, the cutoff frequency that we observe here is much higher than the scattering frequency connected with inductive behavior in bulk material, which is around 1 THz for the doping concentration considered here. Furthermore, the observed cutoff frequency is also different from the plasma frequency of GaAs, which is about 25 THz for the same electron concentration. Thus, while electron inertia accounts for the phase delay in both Schottky diodes and bulk material, it is misleading to model the phenomenon in Schottky diodes as merely an inductive effect. Instead, it is more nearly correct to consider the effect in Schottky diodes as being due to transit delays in the *spatial* transfer of charge caused by the finite maximum velocity of the electrons.

III. Conclusion

In this paper we have shown the results of time-dependent Monte Carlo simulations of Schottky diodes at terahertz frequencies. We believe these are the most comprehensive simulations to date. They have considered effects such as electron degeneracy and electron-electron and electron-plasmon scattering, in addition to the phenomena usually considered in MC simulations. One of our most significant demonstrations is that the maximum velocity of the depletion layer edge imposes an inherent physical limitation on the cutoff frequency of GaAs Schottky diodes. Equally important, we predicted that the peak velocity of the depletion layer edge substantially exceeds the steady-state saturation velocity of GaAs, and is even greater than the thermal velocity. We showed that these transit time effects cause a phase delay in the particle current that increases with frequency, but that this phase delay is not accompanied by a gradual roll-off in the magnitude of the conduction current. Instead, we expect a slight increase in the magnitude of the particle current up to the cutoff frequency, followed by an abrupt drop beyond that frequency. Thus, our simulations show that Schottky diode behavior at terahertz frequencies cannot be modeled accurately by a traditional lumped-element circuit model. The inclusion of the electron-electron and electron-plasmon interactions is shown to reduce the high frequency response and the higher harmonic content of both the particle and displacement current components.

Acknowledgments

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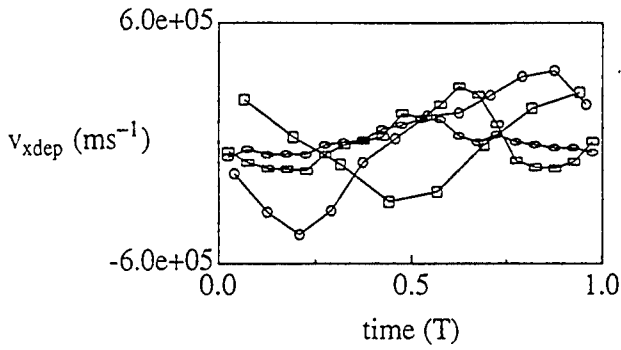


Fig. 1a. Depletion layer edge velocity vs. time, from MC simulation.

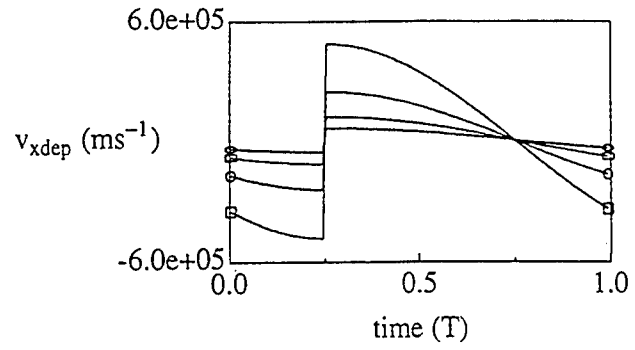


Fig. 1b. Depletion layer edge velocity vs. time, from depletion approximation.

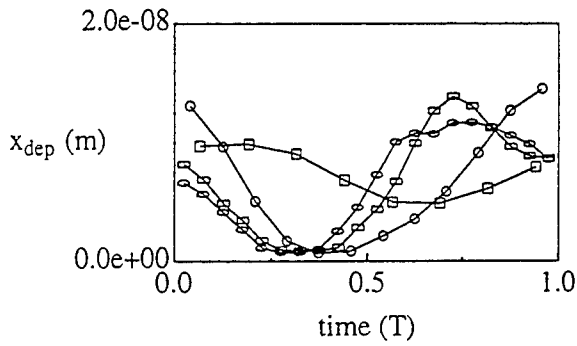


Fig. 2a. Depletion layer edge position vs. time, from MC simulation.

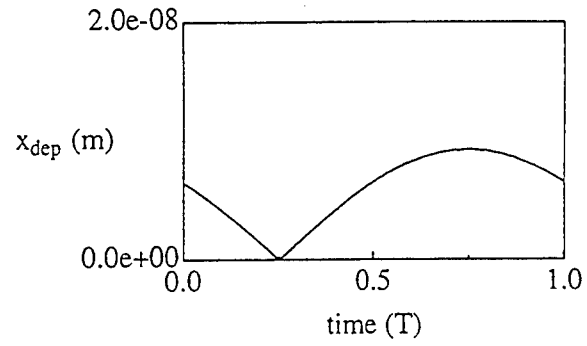


Fig. 2b. Depletion layer edge position vs. time, from depletion approximation.

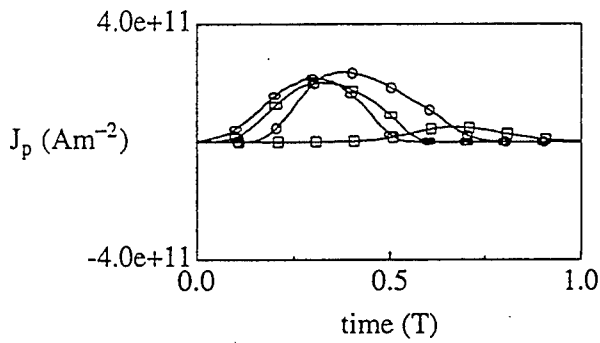


Fig. 3. Particle current vs. time.

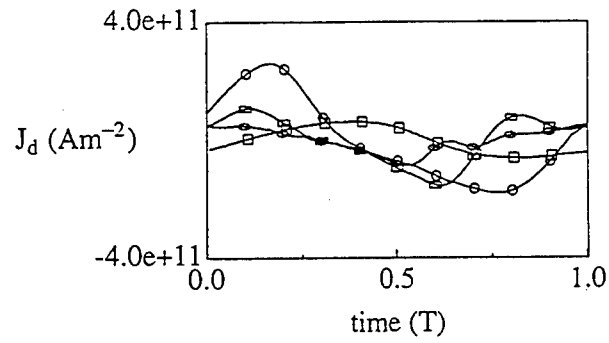


Fig. 4. Displacement current vs. time.

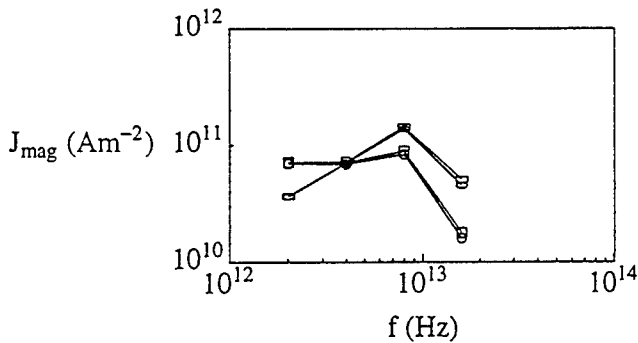


Fig. 5a. Particle and displacement current magnitude vs. frequency.

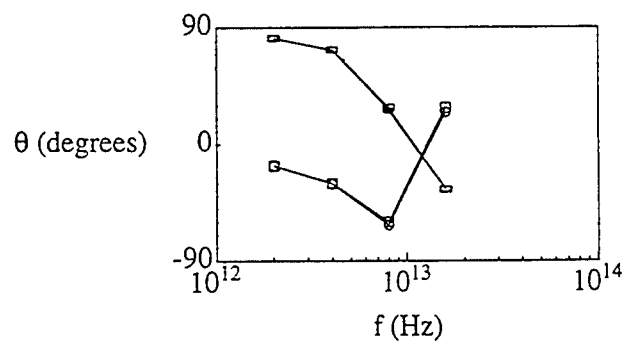


Fig. 5b. Particle and displacement current phase vs. frequency.

Key for Figs. 1-4: ellipses, 2 THz; rectangles, 4 THz; circles, 8 THz; squares, 16 THz.

Key for Figs. 5a-b: circles, part. current, w. e-e, e-pl scat.; squares, part. current, w/o. e-e, e-pl scat.; ellipses, disp. current, w. e-e, e-pl scat.; rectangles, disp. current, w/o. e-e, e-pl scat..

Planar Schottky Varactor Diode Arrays for Millimeter-Wave Frequency Multipliers

P. J. Koh, W. C. B. Peatman, T. W. Crowe,
University of Virginia, Charlottesville, VA, and
N. R. Erickson,
University of Massachusetts, Amherst, MA

I. INTRODUCTION

Varactor elements are commonly used to multiply the output of Gunn diodes to higher frequencies for use as local oscillator sources in heterodyne receivers. At frequencies over 100 GHz, the standard varactor element is a GaAs Schottky diode. The typical configuration has traditionally been a single whisker contacted varactor; this configuration's main strength is its minimal parasitic capacitance. Recently, however, techniques for fabricating planar Schottky diodes have evolved to the point where they are competitive with or superior to whisker contacted devices, particularly in varactor applications [1]. The most obvious benefit of moving to planar devices is their ruggedness relative to whisker contacts. However, another significant benefit is the ability to integrate several devices onto one chip. Recent improvements in yield and parasitics have opened up a wide range of possibilities for improved varactor elements made of arrays of planar Schottky diodes in various configurations.

The first stage of a multiplier chain obviously has the highest requirements for power handling. In traditional single-diode varactor designs, higher power handling is obtained by increasing the epilayer thickness and reducing doping density. This increases the reverse breakdown voltage (V_{br}), allowing higher pump powers to be used, but at the expense of higher series resistance. For example, the UVa 6P4 whisker-contacted varactor has a doping density of $3.5 \times 10^{16} \text{ cm}^{-3}$ and a thickness of $1 \mu\text{m}$, with a large V_{br} of 20v. However, due to velocity saturation of carriers in GaAs under high fields, it may not be possible to fully deplete this $1 \mu\text{m}$ depth on each cycle at 80 GHz [2]. In this case, efficiency drops off quickly under higher pump powers, and the extra epilayer thickness is of no benefit.

II. SERIES ARRAY BALANCED DOUBLERS

Arrays of devices do not suffer the same trade-offs, however. Power handling can be increased by distributing

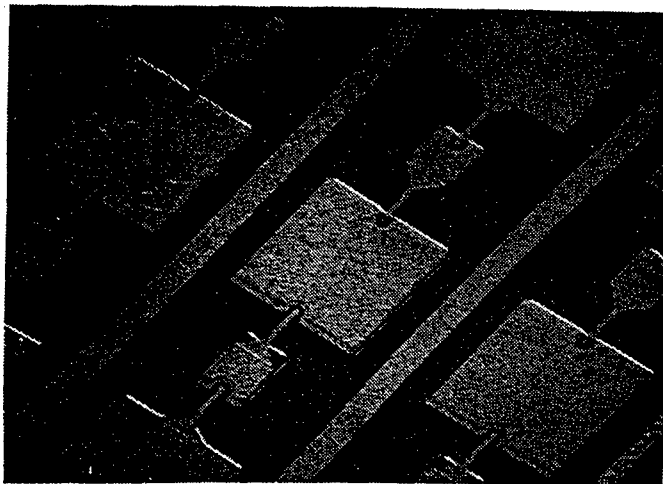


Fig. 1. SEM photograph of optimized 160 GHz balanced doubler devices.

the power among several diodes without increasing the epilayer thickness. A series array of n devices of area A may be used to replace a single diode of area A/n , while keeping the same overall capacitance. Thus, such an array can handle n^2 times the power of a single diode. Such an approach was used in UVa SC10V2 devices [1], which divided power among four diodes to deliver 55 mw at 174 GHz, twice the power available from the previous best multiplier at a nearby frequency. This was the first instance in which a planar device displayed significantly higher performance than whisker contacted devices, demonstrating extremely high power-handling capability. Indeed, it appeared that the chip could handle far more power than what would be available from a Gunn source.

It should be noted that each individual anode of the SC10V2 adhered fairly closely to traditional designs for varactors in this frequency range. The doping and thickness of the epilayer were similar to 6P4-type diodes, and so their cutoff frequency were about the same. The only benefit of the series array of four diodes was to increase power handling by a factor of four over the 6P4; no attempt was made to improve the cutoff frequency or reduce series resistance.

Table 1

Batch#	t_{epi} (Å)	N_{epi} (cm ⁻³)	diam. (μm)	Single Anode		
				C_{jo} (fF)	R_s (Ω)	V_{br} (V)
SC10V2	6400	4.5×10^{16}	9	38	6	15
SC6T6	4500	1.2×10^{17}	6	40	1.5	11

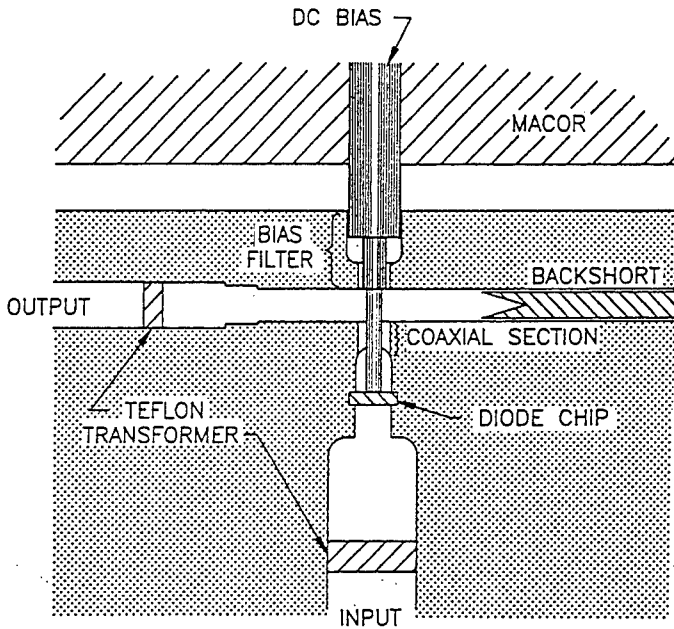


Fig. 2. A cross section through the doubler block

III. OPTIMIZED 160 GHz BALANCED DOUBLER

In this research, an improved balanced doubler chip, shown in Fig. 1, was fabricated and RF tested at 160 GHz output. The array is laid out identically to the SC10V2 - four diodes, two in series on each side. Priority was placed on reducing series resistance rather than increasing power handling capability, in an effort to achieve a higher cutoff frequency and improve efficiency. In this case the chief benefit of using this configuration versus a single 6P4 is that we were able to use a much higher doped and thinner epilayer than are typically used at this frequency, while maintaining adequate power handling levels. It is believed that the epilayer thickness (4500 Å) is now thin enough that velocity saturation effects do not seriously degrade performance, and the epilayer may be fully depleted on each cycle at 80 GHz.

The characteristics of this batch (SC6T6) are compared with those of the SC10V2 in Table 1. By using high doping and thin epilayers, the series resistance was reduced to 1.5 Ω per anode, a significant improvement over

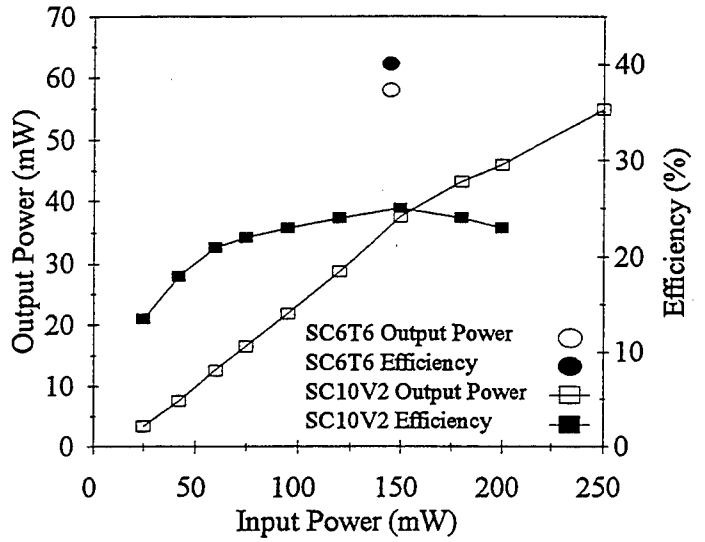


Fig. 3. Output power and efficiency of optimized 160 GHz doubler (SC10V2) vs. previous results (SC6T6) [1]. Data for input powers other than 145 mW is not yet available.

the 6 Ω per anode of the SC10V2. This was accomplished while still maintaining the 40 fF per anode capacitance which was desired for matching to the RF circuit. Since two diodes are in series on each side, the V_{br} for the pair (22 V) is still large enough to handle the full available power of an 80 GHz Gunn source.

The fabrication followed the surface channel process, described in detail elsewhere [3,4]. After forming the long metal 'finger' which connects the outer pad to the diode, a deep (9 μm) etch is used to isolate the two pads and to undercut the 'finger' of metallization, forming an air bridge. This air bridge allows the parasitic capacitance to be reduced to very low levels. The fabrication deviated somewhat from the standard surface channel process - special care was taken to keep the resistance as low as possible. To this end, evaporated Ni/Ge/Au ohmic contacts were substituted due to their lower contact resistance. Also, all contact pads and 'fingers' were plated with thick (~2.2 μm) gold metallization to minimize resistance. During lapping, the chips were thinned to 15 - 25 μm. Lapping the chips very thin, in an effort to minimize the amount of GaAs within the waveguide, is necessary to get good RF performance.

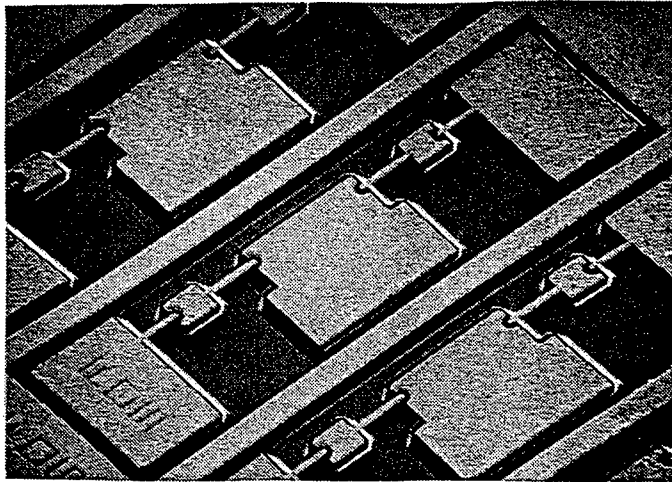


Fig. 4. SEM photograph of the 320 GHz doubler devices

IV. DOUBLER MOUNT AND RF EVALUATION

The doubler mount is the same as was used in [1], and is shown in Fig. 2. The diode is soldered to the waveguide top and bottom walls as well as to the center pin in one operation. The chip is supported by the solder joints, and the resulting structure is quite robust.

The highest efficiency was obtained at an input power of 145 mw at 80 GHz. The output was 58 mw at 160 GHz, corresponding to 40% efficiency - considerably higher than the 25% obtained from SC10V2 diodes. We believe this is a record for both output power and efficiency from a multiplier at this frequency. This result is compared with the output power and efficiency of the SC10V2 in Fig. 3. Data for input powers other than 145 mw is not yet available.

V. 320 GHz BALANCED DOUBLER ARRAY

Other planar diode arrays have been fabricated, but no RF results are available yet. One configuration, which we will briefly describe here, is a scaled version of the above 160 GHz doubler which is intended for operation as the next stage in a chain of multipliers. These doublers receive input power at 160 GHz and doubles it again to 320 GHz. These devices (SC3T5) are also a linear array consisting of two pairs, as seen in Fig. 4. The shapes of the pads are changed slightly, to facilitate easy soldering and handling despite the smaller size. These have smaller anode sizes and higher

doping than the 160 GHz devices, since their capacitance must be lower to operate at higher frequency, but their power handling requirements are lower, with 40 mw available for pumping.

VI. CONCLUSION

Several new designs for varactor anode arrays have been fabricated. A 160 GHz doubler was fabricated as a four diode array with a highly doped ($1.4 \times 10^{17} \text{cm}^{-3}$), thin (4500Å) epilayer, in order to minimize parasitic series resistance. This and other improvements resulted in a factor of four reduction in series resistance below previous devices. It is believed that the 4500Å epilayer is thin enough so that velocity saturation effects are not significant. This device was RF tested and produced 58 mw output and 40% efficiency. This is the highest power and efficiency yet reported for a doubler at this frequency.

A scaled version of the above device was fabricated for doubling from 160 to 320 GHz. RF testing of this device is under way.

ACKNOWLEDGEMENTS

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The Design, Construction and Evaluation of a 585 GHz Planar Schottky Mixer

Jeffrey L. Hesler, Thomas W. Crowe, and Robert M. Weikle
Department of Electrical Engineering
University of Virginia
Charlottesville, VA 22901

Richard F. Bradley and Shing-Kuo Pan
National Radio Astronomy Observatory*
Charlottesville, VA 22903

Introduction

There is a need for sensitive receivers at submillimeter wavelengths for such applications as radio astronomy, atmospheric studies, plasma diagnostics, molecular spectroscopy and compact range radars. Mixers using GaAs Schottky diodes can provide excellent sensitivity at either cryogenic or room temperature, making them flexible detectors with proven performance at submillimeter wavelengths. Unfortunately, the best Schottky receivers have used whisker-contacted diodes, which make the design and assembly of the receiver quite expensive, and complicates the space qualification process. This research is an investigation of the use of planar Schottky diodes [1] in waveguide receivers which are optimized through the use of modern circuit simulators and design tools, with the goal of achieving the same level of performance that has already been demonstrated with whisker-contacted Schottky diodes.

This paper describes the design, fabrication and testing of a 585 GHz waveguide receiver which utilizes state-of-the-art planar Schottky diodes. The design of the mixer, including numerical modeling of the diode and circuitry with Hewlett Packard's High Frequency Design Software is described. The results of testing with several mixer configurations are presented.

Mixer Configuration

The mixer block, shown schematically in Fig. 1, was originally designed for use with a superconductor-insulator-superconductor junction. The primary modification was the redesign of the microstrip circuitry to present the proper embedding impedance to the planar diode. The LO and RF signals are coupled into an 8x16 mil waveguide by a diagonal feedhorn [2]. The signals are then coupled into a 4x4.5 mil shielded microstrip channel by a microstrip probe in the waveguide. The diode, a UVa SC1T5 diode with a 1.2 μm anode diameter, is mounted across a gap in the microstrip.

Mixer Modeling and Design

In order to determine the embedding impedance presented to the diode, Hewlett Packard's High Frequency Structure Simulator (HFSS), a three-dimensional finite element solver for Maxwell's equations, was used to determine the fields for the diode mounted across a gap in the microstrip. A coaxial probe was inserted in the HFSS model near the diode's anode, and the input impedance of this probe was used to predict the diode's embedding impedance. The main mixer tuning parameter is the distance between the diode and the low-pass filter. Other key parameters affecting the diode's embedding impedance are the diode's finger length, the impedances of the transmission lines on either side of the

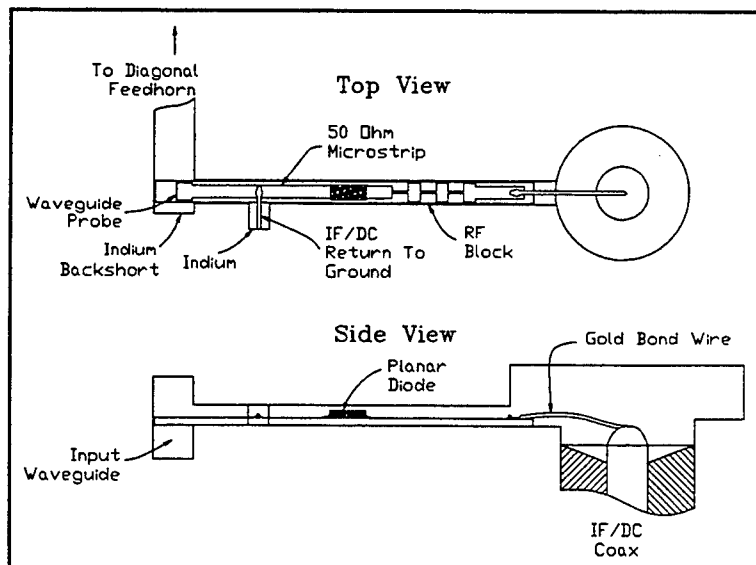


Fig. 1. Schematic of the planar diode mixer block interior.

diode, and the length of the gap across which the diode is mounted.

Once the variation of the diode's embedding impedance with system parameters was determined, the harmonic balance routines in Hewlett Packard's Microwave Design System (MDS) were used to design RF coupling structures for the diodes. Typical diode parameters for an SC1T5 diode are $R_s = 15 \Omega$, $\eta = 1.16$, $I_{sat} = 3E-17$ A, and $C_p = 2$ fF. The values for R_s , η and I_{sat} were determined by a least squares fit of the measured diode I-V to the nonlinear diode equation. Mixer circuits were designed at 585 GHz for diodes with finger lengths of 5, 10 and 20 μm lengths.

The microstrip circuits were fabricated on 1.5 mil quartz substrates. The thin quartz wafer was mounted with wax on a silicon support wafer, allowing the use of standard photolithography techniques to fabricate the circuitry. The quartz wafer was then diced into individual circuits before being removed from the silicon carrier. The IF/DC connection wires were then bonded onto the choke and the diode was soldered across the gap. Finally the quartz structure was mounted into the mixer block and held in place by the wires which were pressed into indium. Once the mixer block halves have been put together, there are no variable tuning elements.

Receiver Measurements

A diplexer and an off-axis parabolic mirror with a focal length of 60 mm are used to couple the LO and RF power into the feed horn. The LO power is supplied by an FIR gas laser which is in turn pumped by a CO₂ gas laser. Testing was performed at both 585 and 690 GHz. For the 690 GHz testing, the mixer block tuned for 585 GHz was used with no adjustments. Table 1 gives a summary of the best mixer results obtained using this mixer block. At 585 GHz, the mixer required less than 0.5 mW of LO power for optimum mixer performance. The 690 GHz result required approximately 1 mW of LO power.

Future testing is planned using chokes with a shorter length of microstrip line and using diodes with higher doping and smaller anode diameter. With these changes, the modeling predicts that the planar diode mixer performance will approach that of the best room temperature whisker-contacted diode mixer. Additionally, the modeling predicts that the if the mixer circuit is designed specifically for 690 GHz then its performance at 690 GHz will be comparable to that at 585 GHz.

Acknowledgments

The authors would like to acknowledge the assistance of William L. Bishop and Frank Li in the fabrication of the diodes used in this research and Hewlett Packard for the donation of their High Frequency Design System software to the University of Virginia. This research has been supported by the U.S. Army National Ground Intelligence Center through grant DAHC90-91-C-0030. The first author was supported by an Augmentation Award for Science and Engineering Research Training from the Army Research Office (AASERT Grant DAAL03-92-G-0057).

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	ν_{RF} (GHz)	T_{sys}^{DSB} (K)	T_{mix}^{DSB} (K)	L^{DSB} (dB)
SC1T5-S10	585	2500	2030	8.6
SC1T5-S20	690	4290	3610	10.2

Table 1.1. Summary of the best receiver results at 585 and 690 GHz.

Generation and Modulation of Infrared Light by Hot Carriers in Ge and GaAs/(Al,Ga)As Structures

*L. E. Vorobjev, S. N. Danilov, D. V. Donetsky, Yu. V. Kochegarov,
D. A. Firsov and V. A. Shalygin*

Saint Petersburg State Technical University
Saint Petersburg, RUSSIA 195251

We describe new results of the investigations of hot carriers in certain electro-optic devices: first, we describe the characteristics of hot hole carriers in far infrared (FIR) Ge lasers. Next, we describe the characteristics of hot electrons in n -type modulation doped GaAs/(Al,Ga)As structures. The Ge laser is inserted in crossed electric and magnetic fields in the Faraday and Voigt field configurations. It is found that the generation regime, emission spectra, FIR light gain, optical power and operation temperatures for the two configurations are different. In our presentation, we will discuss the mechanism of population inversion and optical gain. A new mechanism for mode selection in the FIR spectrum and continuously tuning the radiation wavelength from 80 to 200 micrometers is suggested. This tuning mechanism is made possible through the use of a thin absorbing film placed inside the resonator. The continuous tuning characteristics of the Ge laser will be presented.

In the second part of our presentation, we discuss the fast (on the order of a picosecond) modulation of carbon-dioxide laser emission at 9.6 and 10.6 micron by hot electrons in selectively and non-selectively doped n -type, multiple quantum well GaAs/(Al,Ga)As structures. In this experiment, the electron population in the structures is heated by applying a pulsed electric field parallel to the layer structures. We find that the laser modulation depends on its polarization; this modulation is believed to be caused by a change of the light absorption coefficient and a birefringence induced by the hot two-dimensional electrons. The physical origin of this phenomenon will be discussed. It is different for the two types of structures investigated. For the selectively doped multiple quantum well structure, the main cause of the light modulation is probably the change of space charge due to the hot electrons. The light modulation in the non-selectively doped structures is probably caused by the interaction of the hot carriers and the non-parabolicity of band spectra.

Optical Pumping of Lattice-Matched ZnCdMgSe Quaternaries and ZnCdMgSe/ZnCdSe Quantum Wells on InP Substrates

Neal Bambha and Fred Semendy, Army Research Laboratory
10235 Burbeck Rd. Ste. 110 Ft. Belvoir, VA 22060

Zn_{1-x}Cd_xSe quantum wells with Zn_xCd_yMg_{1-x-y}Se barrier layers were characterized by photoluminescence, x-ray topography, and optical pumping. These layers can be grown entirely lattice matched to InP, making the material system attractive for blue, green, and yellow laser diodes. Emission resulting from the optical pumping of these layers by a pulsed dye laser is presented.

To date, the only successful blue laser diodes have been fabricated with ZnSe based alloys. The rapid degradation of these devices is the biggest obstacle remaining towards their successful commercialization. These devices have all been grown on GaAs, using a Zn_{1-x}Cd_xSe quantum well. The lattice mismatch in the quantum well produces strain which may lead to degradation during operation. It would be interesting to test a laser structure that is completely lattice matched and free of strain. At x=0.525, Zn_{1-x}Cd_xSe has a lattice constant of 5.87 angstroms, equal to that of InP. Using the quaternary Zn_xCd_yMg_{1-x-y}Se, lattice matched cladding and barrier layers can be grown.

The layers were grown at CUNY by MBE in a Riber 2300P growth chamber. Elemental Zn, Cd, Mg, and Se sources were used. Growth was performed under Se-rich conditions with a beam equivalent pressure ratio group VI to group II of approximately 4. Growth temperatures of 270 C and growth rates of about 1 micron per hour were used. InP (100) substrates having defect densities of $< 5 \times 10^3 \text{ cm}^{-3}$ were obtained from Sumitomo Electric. Oxide desorption of the InP substrate was performed by heating with an As flux impinging on the InP surface as previously reported.¹

To investigate the quality of the layers grown by this method, low temperature photoluminescence and double crystal x-ray rocking curve measurements were performed. A 1 micron layer of ZnCdSe grown by this method produced extremely narrow (8meV) and efficient PL bandedge emission with very low level of defect-related deep emission. X-ray rocking curves having widths of 270 arc sec (FWHM) were obtained for these layers. These are the narrowest values reported for ZnCdSe layers grown on any substrate.

The optical pumping experiments were performed with a dye laser pumped by a N₂ laser. The N₂ laser had a pulse energy of 250 microjoules, 3ns pulse at 337 nm. The samples were thinned to 100 micron and manually cleaved to small bar-like samples with cavity lengths of 0.5mm to 2 mm. The cleaved bars were attached with thermal epoxy to a copper mount attached to a cold finger. The temperature of the cold finger could be varied from 10K to 300K. The laser beam was attenuated using neutral density filters and focused onto the sample surface using a cylindrical lens, forming a rectangular excitation spot. A p-i-n photodiode was used to record the incident pump intensity. The light emission from the sample was focused with a lens into a 0.8 m Spex double grating spectrometer. The spectrum of the emission was measured for several pump intensities, at temperatures from 10K to room temp. The emission characteristics were found to be a strong function of pump wavelength and temperature.

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Theory of Dark Resistance in Photodiodes for Arbitrary Diode Geometry

B. L. Gelmont, M. S. Shur, and R. J. Mattauch
*Department of Electrical Engineering, University of Virginia
Charlottesville, VA 22903-2442*

The dark resistance of far infrared photodetectors is described by the analytical theory of Grimbergen [1], which is applicable in the limiting case, when the diffusion length is much greater than the detector size. We derive an integral equation, which is valid for any ratios of the layer thickness, the recombination length, and the detector radius. This equation can be easily solved by standard numerical techniques. We compare our results with Grimbergen's approximation and show that, for a typical detector design, the error of this approximation may be as large as 30%.

1. Introduction.

Infrared focal plane arrays of photodetectors require small pixel size with uniform response over large areas. As the detector area decreases, surface and geometrical effects become increasingly important. In particular the zero-bias resistance of the photodetector has to be calculated taking into account the lateral spreading of the flow of the minority carriers [2]. A simple one-dimensional model is applicable when the layer thickness, b , and the diffusion length, L , are small in comparison with the detector radius, R ($b, L \ll R$), see Fig. 1. Grimbergen [1] derived an equation for the current, which takes into account the lateral spreading of the flow. His equation is valid when $b \ll L, R$.

In practical photodetector arrays, b is comparable with L . Since the absorption coefficient is relatively large and the light is absorbed near the surface, the collection of the photogenerated carriers improves when the junction is closer to the back surface of the device (see Fig. 1), i. e. when b is decreased. On the other hand, the spreading resistance decreases with an increase in b . Choosing b to be on the order of L is a reasonable trade-off, since at such values of b nearly all photogenerated carriers are collected by the junction. When b is comparable to L , analytical treatment does not apply. Briggs [3] used numerical techniques to solve directly the three dimensional diffusion equation for planar circular photodiodes.

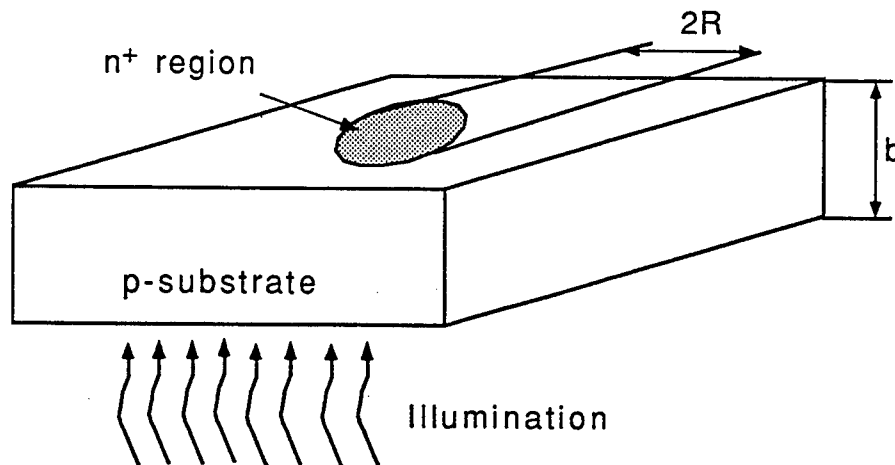


Fig. 1. Schematic device geometry.

In this paper we derive an integral equation which permits us to find the current for circular geometry at any ratio of the layer thickness, the recombination length, and the detector radius. This approach is a reasonable alternative to a full numerical solution, such

as discussed in [3]. We calculate the dependence of the current on the ratio of the recombination length to the detector radius for different values of b and compare our results with the Grimbergen approximation.

2. Basic equations and boundary conditions.

For a circular geometry (see Fig. 1), the minority carrier concentration, $n(r,z)$, can be determined from the diffusion equation in the p-type region

$$\frac{\partial^2 n(r,z)}{\partial z^2} + \frac{\partial^2 n(r,z)}{\partial r^2} + \frac{1}{r} \frac{\partial n(r,z)}{\partial r} = n/L^2 \quad (1)$$

with the boundary conditions

$$n(r,0) = n(0) \quad \text{for } r < R \quad (2)$$

$$\frac{\partial n}{\partial z} = 0 \quad \text{at } z=0 \text{ for } r > R, \quad (3)$$

$$\frac{\partial n}{\partial z} = 0 \quad \text{at } z=b \quad (4)$$

These boundary conditions assume that the depletion region thickness is small in comparison with both the layer thickness and the recombination length.

3. Integral equation and its solution.

Following the approach discussed by [4], we can find the solution of eq.(1) satisfying boundary conditions (3) and (4)

$$n(r,z) = \int_0^\infty \frac{dt t F(t) L n(0)}{R \sinh\left(\frac{b}{LR} \sqrt{t^2 L^2 + R^2}\right) \sqrt{t^2 L^2 + R^2}} \cosh\left(\frac{(b-z) \sqrt{t^2 L^2 + R^2}}{LR}\right) J_0\left(\frac{r t}{R}\right) \quad (5)$$

where J_n is the Bessel function,

$$F(t) = \int_0^1 dv f(v) \cos(vt) \quad (6)$$

and $f(v)$ is a function defined in the interval $0 < v < 1$, which can be determined from the boundary condition given by eq. (2). This boundary condition leads to the following integral equation for $f(v)$:

$$\frac{R}{L} = \int_0^\infty \frac{dt t F(t) \cos(ut)}{\sqrt{t^2 L^2 + R^2}} \coth\left(\frac{b \sqrt{t^2 L^2 + R^2}}{LR}\right) \quad (7)$$

The resistance R_s is related to the function $f(v)$ as follows

$$1/R_s = 2\pi q D_n R n(0) F(0) / (k_B T) \quad (8)$$

where q is the electron charge and D_n is the electron diffusion coefficient.

The solution of eq. (7) depends on two parameters b/R and L/R . In the limit of a small layer thickness ($b \ll L, R$), this integral equation is simplified

$$\frac{b}{R} = \int_0^{\infty} \frac{dt \, t \cos(utR/L)}{1+t^2} F\left(\frac{tR}{L}\right) \quad (9)$$

The solution of this equation is

$$f(v) = \frac{2bR}{\pi L^2} \left(\sqrt{1-v^2} + \frac{A}{\sqrt{1-v^2}} \right) \quad (10)$$

where

$$A = \frac{LK_1(R/L)}{RK_0(R/L)} \quad (11)$$

and K_n is the modified Bessel function.

Substituting eq. (10) into eq. (8) we obtain Grimbergen's equation

$$R_g = R_0 / (1 + 2A) \quad (12)$$

where

$$R_0 = \frac{k_B T L^2}{\pi q D_n R^2 b n(0)} \quad (13)$$

is the current predicted by the one-dimensional model based on the assumption that the layer thickness, b , and the recombination length, L , are small in comparison with the detector radius, R .

In a general case, the integral equation (7) has to be solved numerically. For the numerical solution, it may be re-written in a more convenient form:

$$\frac{\pi}{2} f(u) = 1 + \int_0^1 dv f(v) - \frac{R}{L} \int_0^1 dv B(u,v) f(v) - \frac{R}{2L} \int_0^1 dv [\Lambda(u+v) + \Lambda(|u-v|)] f(v) \quad (14)$$

where

$$B(u,v) = \int_0^{\infty} \frac{dt \, t}{\sqrt{t^2+1}} \left[\coth\left(\frac{b\sqrt{t^2+1}}{L}\right) - 1 \right] \cos\left(\frac{vtR}{L}\right) \cos\left(\frac{utR}{L}\right) \quad (15)$$

and

$$\Lambda(z) = z \int_0^{\pi/2} d\theta \sin^2 \theta \exp(-z \cos \theta) \quad (16)$$

We solved eq. (14) numerically for different ratios of b/R and L/R and compared the results with the Grimbergen approximation (see Fig. 2).

Conclusions

As expected and as seen from Fig. 2, the Grimbergen approximation works quite well when $b/L \ll 1$. For practical photodetectors, this ratio is on the order of unity, and the error introduced by the analytical approximation may be quite large (30% or so). The proposed method allows us to obtain a more accurate solution quite easily. This method may be also applicable for a large variety of other problems involving diffusion of electrons and holes in semiconductor devices, such as the current spreading in semiconductor diodes of different geometries.

Acknowledgment

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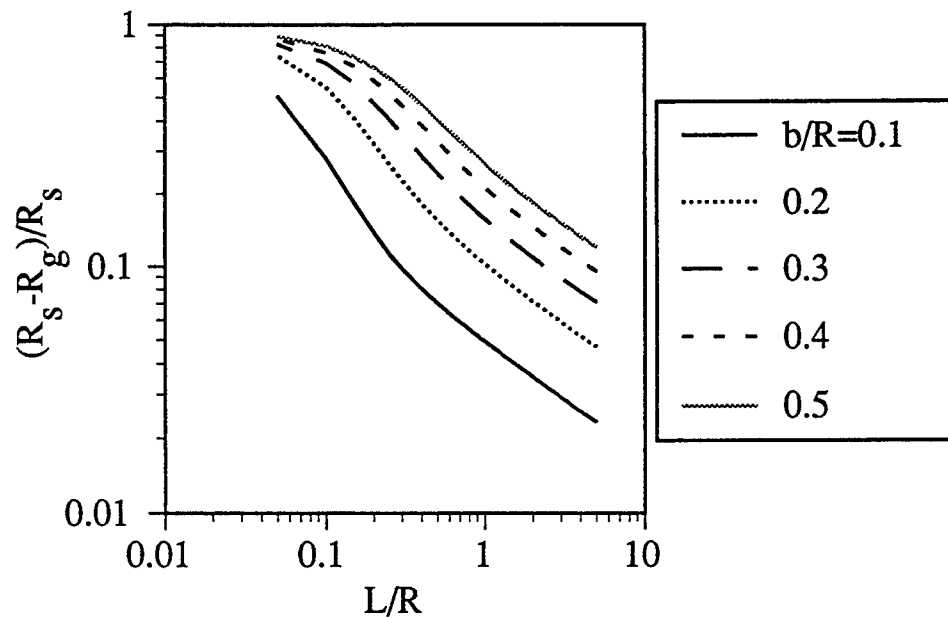


Fig. 2. Relative difference between the computed dark resistance, R_s , and the dark resistance, R_g , predicted by Grimbergen's theory versus the ratio of the recombination length to the detector radius for different layer thicknesses.

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LASER BEAM INTERFERENCE EFFECTS on the PHOTOVOLTAGE of a GaAs P-N JUNCTION

K. Weiser, F. Dahan and S.E. Schacham- Dept. of Electrical Engineering, Technion, Haifa, Israel

E.Towe and H. Park- Dept.of Electrical Engineering, U. of Virginia

We present measurements of the photovoltage ϕ observed for a GaAs p-n junction diode when illuminated through a mask by a sinusoidally varying light pattern produced by the interference of two coherent He-Ne laser beams. Using a theory (1) which relates ϕ both to the fringe spacing and to the phase of the interference pattern relative to markers placed parallel to the fringes, but at a distance l apart, we deduce the diffusion length of minority carriers in the top layer of the diode.

By the use of a mask the illuminated area (typically $0.5 \times 0.5 \text{ mm}^2$) was kept much smaller than the surface area. Under these conditions it was found that the photovoltage between the n- and the p- layers in the absence of interference increased logarithmically with the exposed area and, of course, with the light intensity. The edges of the mask along the fringe direction were metallic stripes which served both as ohmic contacts to the p-layer and as the "markers" relative to which the interference pattern was measured. By using a beam expander the region between the contacts was uniformly illuminated, except for the interference effects. The photovoltage was measured between these contacts and an ohmic contact on the n-side.

By passing one of the beams through a phase modulator the interference pattern could be swept across the region between the top contacts. The effect of this sweep on the photovoltage ϕ depended on the angle between the beams. If b , the number of fringes between the two stripe contacts, equaled an integer N , ϕ did not change during the sweep. For $b = N + 1/2$, however, the voltage alternated between maxima and minima as the phase of the interference pattern changed with respect to the position of the two contacts. The magnitude of the voltage swing decreased with increasing values of b .

From the dependence of the voltage swings $\Delta\phi$ on b it is possible to obtain the diffusion length of the minority carrier (electrons) in the top layer. A simplified theory(1) which accounts for this dependence starts with the fact that for $b = N + 1/2$ (but not for $b = N$) the sweep results in periodic changes in the total light flux reaching the illuminated area. This phenomenon is due to the fact that for zero phase difference between a maximum in the phase pattern and one of the stripe contacts the total light flux reaching the illuminated area is equal to that in the absence of interference, I_0 . As the phase angle changes during the sweep the total

light flux first exceeds and then becomes smaller than I_L ; after a phase change of $\pi/2$ the cycle repeats itself. Hence, even without taking minority carrier effects into account ϕ undergoes periodic variations during the sweep. This effect alone does not, however, correctly predict the dependence of the voltage swings $\Delta\phi$ on the wavevector k of the interference pattern.

To explain the dependence of $\Delta\phi$ on k observed experimentally one must take into account the spatial distribution of minority carriers in the illuminated layer of the diode. Since the light intensity varies sinusoidally along the direction of k the minority carrier concentration exhibits an analogous pattern. The amplitude of the oscillations is, however, much smaller than that of the light pattern because of diffusion of carriers from regions of high light intensity to those of low light intensity(2). It can be shown that the amplitude of the oscillation is proportional to an attenuation factor $(1 + k^2 L^2)^{-1}$ (2) where L is the minority carrier (electrons) diffusion length in the top layer. Since the photovoltage depends on the rate of arrival of minority carriers at the junction(3) we have derived an equation for the swing in the photovoltage during the sweep of the interference pattern which takes this attenuation factor into account. The theory predicts (1) that the voltage swing $\Delta\phi$ depends on the wavevector k according to the relation:

$$\frac{e \frac{q \omega D}{2kT} - 1}{e \frac{q \Delta\phi}{2kT} + 1} = \frac{k l}{2} (1 + k^2 L^2) \quad \text{Eq.1}$$

From a plot of the l.h.s of Eq.1 at different $\Delta\phi$'s vs k , with L as a fitting parameter, we obtain a value of $L = 13.4$ microns which is in excellent agreement with the value calculated from the lifetime and mobility of electrons in GaAs at the doping level of the diode studied.

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High Speed Turn-Off of a GaAs Optoelectronic Thyristor

V. Korobov, V. Mitin

*Department of Electrical and Computer Engineering
Wayne State University, Detroit, MI*

1. INTRODUCTION

Recently, extensive research has been performed on light-emitting thyristor-like PnpN structures [1, 2]. Their applications for optical parallel processing schemes and optoelectronic integrated circuits require high speed of operation. Switching times of the order of several nanoseconds have been obtained using gate contacts [3]. The fast recovery of *two-terminal* PnpN structures could essentially expand applications of optothyristors for optical parallel processing, copying and transmission of optical images [4]. Recent experiments [5] have demonstrated that two-terminal optoelectronic thyristors with ultrasmall n-base region can be turned off in a few nanoseconds simply by applying the negative voltage to the anode. An improvement in turn-off time by about three orders of magnitude over traditional two-terminal thyristors has been achieved. Theory of this phenomena has not been reported yet.

Our goal is to present results of numerical simulation of reverse recovery processes in a GaAs optothyristor with a narrow n-base, when its punch-through occurs after reversing anode voltage. The simulation is based on the numerical solution of the full set of nonstationary semiconductor device equations. Analysis of our simulation results has allowed to show that n-base punch-through allows essentially decrease switching times and increase immunity with respect to dV/dt switching. We have derived an expression for a recovery time in terms of device parameters for the first time. Comparison with available experimental results will be discussed in our talk.

2. PnpN STRUCTURE WITH A "WIDE" BASE

In the ON state the voltage drop across the device is small and there are many excess electrons and holes in the inner n,p regions of the thyristor. In order to switch the device off, excess carriers, supporting the ON state, have to be reduced below the holding level. Attempts to remove excess carriers by reversing the anode voltage were not successful. It was reported [5] that several microseconds were required for an excess charge to reach equilibrium after applying a negative anode voltage to the two-terminal device, which initially operated in the ON state. Simulation results show, that the reason of this long turn off is that only one type of carriers (fast diffusing electrons) can be pulled out after applying a negative anode voltage. Decrease of electron concentration takes place only near the Pn junction, where a space charge region forms. Practically all voltage drop occurs across this region. After this region has been formed, the next slow stage of relaxation starts, when electric field practically does not change its magnitude and carrier concentrations slowly decrease with time. It can be shown, that hole concentration $p_0(t)$ at the boundary of depletion and quasineutral regions decreases proportionally to the total current $j(t)$ at this moment of time. Hole concentration in the quasineutral region $\bar{p}(t)$ can be found to be proportional to $j(t)$ also. The ratio $\bar{p}(t)/p_0(t) \sim \sqrt{V}$ is time independent. Part of the structure outside the depletion region remains quasineutral and is flooded by excess carriers, whose concentrations decrease proportionally to

the current density $j(t)$. The latter is not a strong function of the negative applied voltage. Reverse recovery process for this traditional structure is a slow process, because electric field has a little effect on the rate of holes removal.

3. "NARROW" BASE

In this case the n-layer becomes completely depleted and is unable to consume all applied voltage. We call an n-base "narrow" if its width W_n is less than the width of a Pn space charge region at a given reverse voltage V . The simulated structure consists of two outer regions (P and N) doped with 10^{17} cm^{-3} , and inner regions (p and n) equally doped with 10^{15} cm^{-3} . Widths of P, n, p and N layers are $3.5 \mu\text{m}$, $1.5 \mu\text{m}$, $5 \mu\text{m}$, and $3 \mu\text{m}$ respectively. Figs. 1 shows electric field distribution at different moments of time after applying a negative voltage $V = -6V$ at $t = 0$. It is seen, that after a depletion region has been formed near the Pn junction all n-base is completely depleted and field starts to penetrate into the p-base. On this stage of recovery process we can indicate three different regions in the device: the depletion region I, which coincides with the whole n-base, and two neutral regions II and III in the p-base. In the region II there is a constant electric field $E_0(t)$, electrons concentration is small and hole concentration has decreased up to the equilibrium level: $p = N_A$. Electron and hole densities in the region III are $n(x, t) \approx p(x, t) \approx \bar{n}(x, t) \gg N_A, N_D$. Electric field in this region is small as well as a space charge. At $t \approx 1.7\text{ns}$ the boundary between regions II and III reaches the pN junction. It means that at this moment all excess holes have been evacuated from the p-base and the depletion region near the pN junction has been formed. Electric field distribution at $t > 1.7\text{ns}$ shows two depletion regions, the first is near the Pn and the second is near the pN junction. It means, that in the regime of n-base punch-through not only electrons, but also holes have been removed from the center regions of the device during a short period time $\approx 1.6\text{ns}$.

It is possible to obtain a closed expression for time t_p , required for the electric field to go through the whole p-base. This time determines a rate of excess carrier removal from the device and, as we will see, is crucial for the increase of immunity with respect to dV/dt switching. Poisson's equation in the completely depleted n-region can be integrated with the boundary condition $E(x = W_n) = E_0(t)$. $E_0(t)$ is the electric field in the region II. It is position independent, because the total current here is controlled by holes, whose concentration is equal to doping concentrations N_A : $j \approx j_p(t) = q\mu_p E_0(t) N_A$. At $x = l_0(t)$ $E_0(t)$ goes to zero. Assuming that its drop is abrupt, the voltage V across the device can be written as:

$$V = \frac{E_M W_n}{2} + E_0(t) (l_0(t) + W_n), \quad (1)$$

where $E_M = (4\pi q/\epsilon) N_D W_n$. The boundary $x = l_0(t)$ moves to the right with the velocity $|\frac{dl_0}{dt}|$. To get a relationship between $|\frac{dl_0}{dt}|$ and the current $j(t)$ we integrate the hole continuity equation over the p-base:

$$\frac{\partial P}{\partial t} + \frac{j(t)}{q} = \int_0^{W_p} R(n, p) dx, \quad (2)$$

P is the total number of holes in the p-base, which can be written as $P = N_A l_0(t) + \bar{n} (W_p - l_0(t))$. The last term in Eq. (2) is small and can be omitted. Using (2) we obtain, that the boundary $x = l_0(t)$ moves to the right with the velocity $|\frac{dl_0}{dt}|$ so that the carrier content of the swept-out region just covers the current density $j(t) = q\bar{n} |\frac{dl_0}{dt}| = q\mu_p E_0(t) N_A$. Assuming that $\bar{n} = \text{const}$ we get an equation for $l_0(t)$:

$$l_0^2(t) + 2l_0 W_n = \frac{2\mu_p N_A}{\bar{n}} (V - V_0)(t - t_0), \quad (3)$$

where $V_0 = E_M W_n / 2 = (2\pi q / \epsilon) N_D W_n^2$, t_0 is the moment of time, corresponding to the beginning of electric field penetration into the p-base: $l_0(t_0) = 0$. Using (4), we can estimate the current density when $l_0 \gg W_n$:

$$j(t) = q\bar{n} \frac{dl_0(t)}{dt} \sim q \sqrt{\frac{\mu_p \bar{n} N_A (V - V_0)}{2t}} \sim \frac{1}{\sqrt{t}}. \quad (4)$$

The time t_p , necessary for electric field to reach the pN junction (when $l_0(t) = W_p$) is given by

$$t_p = t_0 + \frac{1}{2} \frac{\bar{n}}{N_A} \frac{W_p^2 + 2W_p W_n}{(V - V_0)\mu_p}. \quad (5)$$

Substitution into this expression values $N_A = N_D = 10^{15} \text{ cm}^{-3}$, $\bar{n} = 2 \cdot 10^{16} \text{ cm}^{-3}$, $W_p = 5 \cdot 10^{-4} \text{ cm}$, $W_n = 1.5 \cdot 10^{-4} \text{ cm}$ gives $V_0 = 1.85 \text{ V}$ and for $V = 6 \text{ V}$ we obtain $t_p \approx 2.1 \text{ ns}$. It is in a good agreement with the results of direct numerical modelling.

4. IMMUNITY WITH RESPECT TO dV/dt SWITCHING

It is well known experimentally, that a fast increase of the anode voltage induces switching of a thyristor before a quasistatic break-over voltage is reached. It was pointed out in [?], that remaining majority carriers (holes in the p-base) supporting the ON state, provide a forward bias for the emitter-base pN junction and induce dV/dt switching. To reveal the effect of electric field penetration into the p-base we have performed a transient simulation for the applied anode voltage, which has the following form. Starting from the positive value $V = 0.5 \text{ V}$, the anode voltage V then pulsed to a negative value V_{neg} . After an interval of time T_{neg} the voltage V increased during 1 ns to the value V_{pos} . Maximum positive voltage V_{pos}^{max} , up to which the thyristor can be pulsed in 1 ns without switching on, versus T_{neg} is depicted in Fig. 2. For negative voltages $V < V_0$ small positive bias switches the device ON and this positive bias practically does not depend on the magnitude T_{neg} . For $V > V_0$ immunity sharply increases for $T_{neg} \approx t_p$. This shows, that t_p , calculated in the previous section, has a meaning of a switching time of our device. The increase of immunity has been observed experimentally in [5].

Acknowledgment. This work was supported by ARO.

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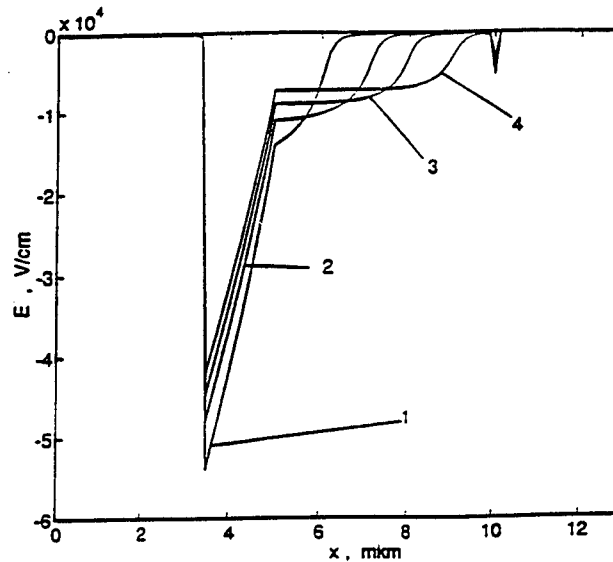


Figure 1. - Electric field after applying the voltage $-6V$ to the anode at various moments of time t . 1 - $t = 0.3ns$, 2 - $t = 0.7ns$, 3 - $t = 1.1ns$, 4 - $t = 1.5ns$.

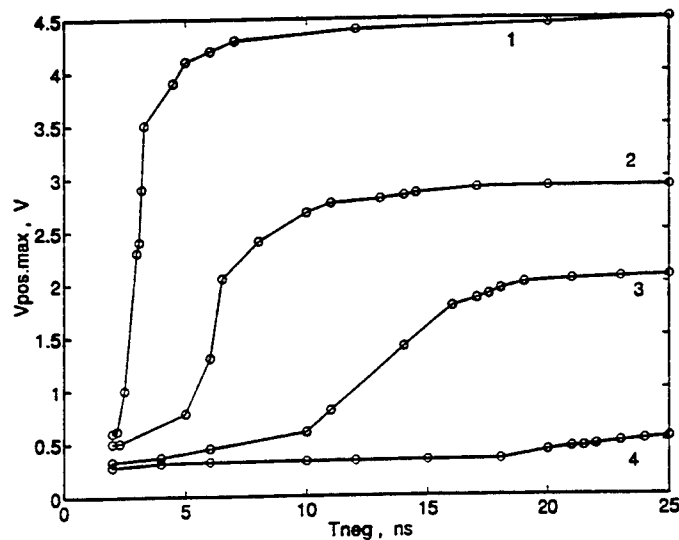


Figure 2. - Maximum positive voltage $V_{pos,max}$, up to which the thyristor can be pulsed in 1 ns without switching on, versus T_{neg} . T_{neg} is the time interval, during which a negative voltage V_{neg} was applied. Curves 1, 2, 3, 4 correspond to $V_{neg} = -4.5$ V, -3.5 V, -2.5 V and -0.5 V.

Optimizing p-i-n/HBT Receivers for Bit-rate and Sensitivity Using SPICE

Moon-Jung Kim, Dae-Keun Kim, Sung-June Kim
 Seoul National University
 Mukunda B. Das
 Pennsylvania State University

Abstract

Recently there have been several reports on the high speed OEIC receiver frontends of bit rate exceeding 10 Gbps[1-3]. These receivers are typically characterized by the 3-dB bandwidth of their low pass frequency responses, and also by the minimum detectable power or the sensitivity. No analytical method, however, has been developed to determine the optimum 3-dB bandwidth, $f_{3dB-opt}$, one can operate a device with the highest sensitivity at a given data rate. The condition of $f_{3dB-opt}$ comes from detailed behavior of the active and passive components of the receiver circuit. This includes a distortion called intersymbol interference (ISI) that exists in the pulse train response.

In this paper, we present the results of determination of $f_{3dB-opt}$ versus bit rate B using SPICE transient simulations based on a p-i-n/HBT OEIC transimpedance receiver designed with optimized load resistance and feedback resistance. For accurate determination of the sensitivity, we have employed direct integration of the transfer function $Z_T(f)$ instead of using Personick's integration constants, and combined it with the ISI noise obtained from transient simulations. At 10 Gbps operation, $f_{3dB-opt}$ is 6.5 GHz for the optimum sensitivity of -22.6 dBm, and at 18 Gbps operation, $f_{3dB-opt}$ is 8.6 GHz for the optimum sensitivity of -22.0 dBm. The ratio $f_{3dB-opt}/B$ was found to vary from 0.65 to 0.45 when f_{3dB} changes from 6.5 to 9.5 GHz.

Fig. 1 (a) and (b) show the epi and device structures we employed. The collector of the HBT also acts as the photoabsorption layer for the p-i-n diode, and therefore some trade-offs are made between the speed of HBT and the quantum efficiency of the p-i-n photodiode. We choose a transimpedance amplifier circuit for its wide bandwidth and large dynamic range, as shown in Fig. 2. The size of the components and the corresponding small signal equivalent circuit of the HBT(D1) are shown in the figure as well. In the circuit we take R_f , C_f , and R_L as the key variables in optimizing the photoreceiver in terms of bandwidth and sensitivity. The advantageous point of variable C_f lies in that we can make various values of C_f keeping that of R_f constant by varying the geometrical aspect ratio of R_f . The capacitance C_f arises mostly from fringing effects between the end pads of R_f . The range of the value of C_f can be a few fF's.

In determining the sensitivity, the circuit noise should be analyzed first. Conventionally, the total noise is estimated using the following expression

$$\langle i_n^2 \rangle_{CIR} = \left(\frac{4kT}{R_f} + 2q(I_B + I_{DARK}) \right) \cdot I_2 B + \left(\frac{4kT}{r_{bb}} \cdot \left(\frac{1}{f_{ex}} \right)^2 + 2qI_C \left(\frac{1}{f_T} \right)^2 \right) \cdot I_3 B^3 \quad (1)$$

where I_2 and I_3 are the Personick's integrals in the forms of $\int_0^\infty |Z_T'(f)|^2 df / B$, and $\int_0^\infty f^2 \cdot |Z_T'(f)|^2 df / B^3$, respectively. These expressions are valid, however, as long as the equalization is done to make the output of the photoreceiver ISI free. In actual cases this assumption does not hold because equalization is not used or because it is also input pulse

shape dependent. In the evaluation of the noise, we have taken a new approach of taking the direct integral of the frequency response function from the SPICE simulation directly [4]. Fig. 3 shows the effect of changing C_f on the transfer function. Fig. 4 shows the bandwidth-dependent integral factors and compares those with the conventional Personick's integral constants. If the effective integral factor is larger than Personick's constant, the conventional noise analysis gives more optimistic results, and vice versa.

Another novel respect of our approach in the evaluation of the noise is that we deal with ISI noise which cannot be neglected because the raised-cosine assumption is not valid. We have analyzed the effects of ISI by examining rectangular pulse responses of receiver with a given bandwidth operating at various bit rates for some levels of ISI. Fig. 5 shows the change in SNR (signal-to-noise ratio) due to ISI. For a given data rate, an optimum 3-dB bandwidth exists. As the 3-dB bandwidth increases above $f_{3dB-opt}$ the transfer function tends to transmit all higher harmonics and this increases ISI noise, whereas the 3-dB bandwidth decreases below $f_{3dB-opt}$ the transient response tends to attenuate the pulse height causing ISI noise to increase monotonically.

By combining the transient analysis to observe ISI and the SPICE-based noise bandwidth analysis, we can then more accurately analyze the sensitivity of the p-i-n/HBT circuit. The overall sensitivity can be obtained by

$$\eta \bar{P} = \frac{h\nu}{q} \sqrt{\frac{\langle i_n^2 \rangle_{CIR}}{\frac{1}{Q^2} - \frac{1}{SNR}}} \quad (2)$$

where η is the quantum efficiency, P is the sensitivity, ν is the frequency of light, $Q = 6$ for 10^{-9} BER. Fig. 6 shows the overall sensitivities of the circuit with C_f as variable for several bit-rates. As C_f increases, the bandwidth decreases, and the circuit noise decreases as well due to reduced noise bandwidth. At the same time, for a given bit rate, the ISI noise can increase. Thus one can optimize the sensitivity of the p-i-n/HBT circuit including both the circuit noise and the ISI.

We can establish a proportional relationship between the bandwidth and the bit-rate, so we can define k factor by $f_{3dB-opt} = kB$, where B is the operating data rate. Fig. 7 shows the optimum bandwidth for a given data rate and corresponding k values. Using this analysis, we determine the best sensitivity that can be obtained at 10 Gbps operation is -22.6 dBm with the k factor specified at 0.6. Smaller k factors are expected at higher bit-rates. For example, at 18 Gbps operation, $k = 0.48$ and a bandwidth of 8.6 GHz for the optimum sensitivity of -22.0 dBm. The difference is less than 1 dB and this is only due to difference in noise bandwidth in the estimation of circuit noise.

In summary, we have shown that the sensitivity of an OEIC receiver can be optimized using SPICE timing and frequency domain simulations, by applying correct noise bandwidth and including ISI. We have accurately determined the values of ISI and circuit noises for changing bandwidth, which enabled the detection of the optimized bandwidth for a given data rate. The ratio $f_{3dB-opt}/B$ was found to vary from 0.65 to 0.45 when f_{3dB} changes from 6.5 to 9.5 GHz for the OEIC receiver.

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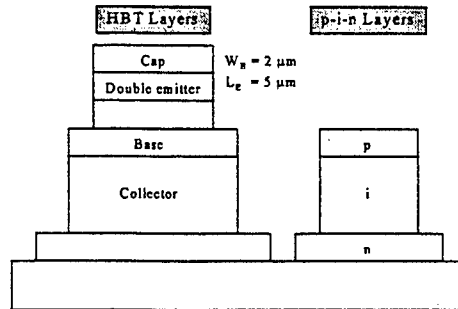
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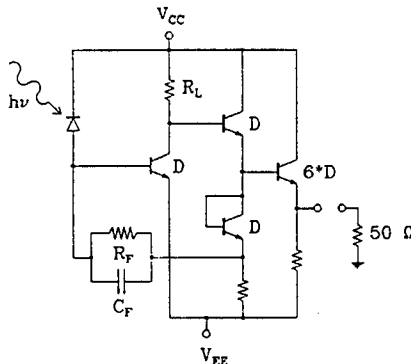
n+ InGaAs	
n+ InP	
n- InP	$t_E = 50 \text{ nm}, N_{dE} = 5 \cdot 10^{16} \text{ cm}^{-3}$
p+ InGaAs	$t_B = 50 \text{ nm}, N_{dB} = 5 \cdot 10^{19} \text{ cm}^{-3}$
n- InGaAs	$t_C = 1 \mu\text{m}, N_{dC} = 5 \cdot 10^{15} \text{ cm}^{-3}$
n+ InGaAs	
S.I. InP Substrate	

(a)

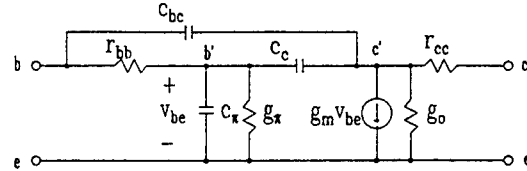


(b)

Fig. 1. InP/InGaAs p-i-n/HBT Device (a) The epitaxial layer structure (b) The schematic cross-sectional view of the device structure.



(a)



(b)

Fig. 2. (a) Transimpedance Frontend Circuit and (b) Small-signal Equivalent Circuit: The design parameters used in this paper are $C_{bc} = 1.5 \text{ fF}$, $C_c = 4 \text{ fF}$, $C_\pi = 52.8 \text{ fF}$, $r_{bb} = 60 \Omega$, $r_{cc} = 40 \Omega$, $r_o = 12.5 \text{ k}\Omega$, $r_\pi = 3.5 \text{ k}\Omega$, and $g_m = 14.28 \text{ mS}$, respectively. These values are extracted from epi layer structure, geometric structure of the device, and DC biasing conditions.

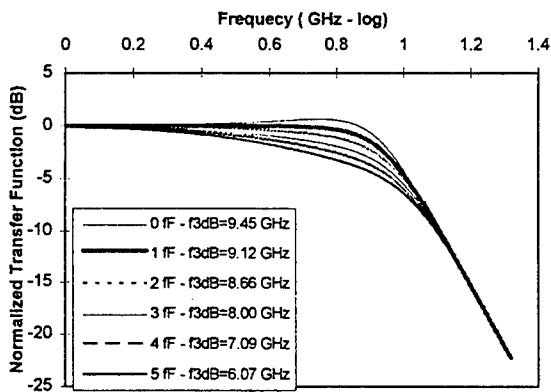
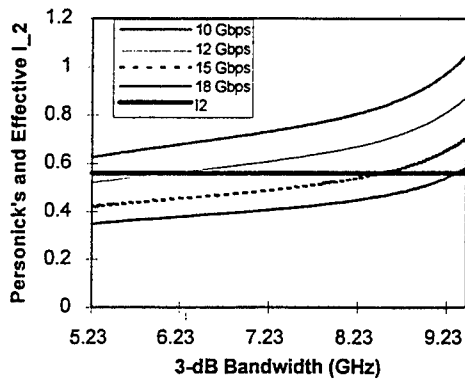
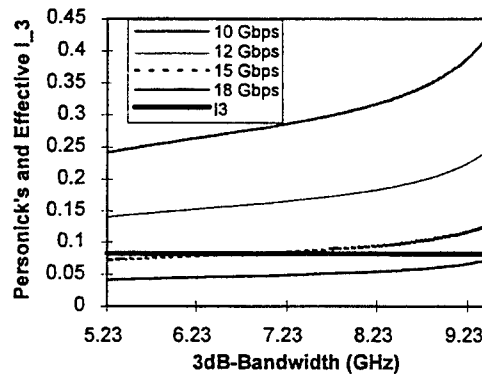


Fig. 3. Transfer Function for variable C_f : When C_f is 1 fF, the transfer function is maximally flat, and further increase in C_f leads to overdamping with reduced 3-dB bandwidth while further decrease in C_f leads to peaking with enlarged bandwidth.



(a) $I_2 = 0.56$ and $I_{2\text{eff}}$



(b) $I_3 = 0.083$ and $I_{3\text{eff}}$

Fig. 4. Comparison between the integral factors in the conventional Personick's constants and in the exact noise analysis using direct integration of transfer function : The Personick's constants I_2 and I_3 are 0.56 and 0.083, respectively, for rectangular input pulses. We define the effective integral factors as $I_{2\text{eff}} = \int_0^\infty |Z_T'(f)|^2 df/B$, $I_{3\text{eff}} = \int_0^\infty f^2 \cdot |Z_T'(f)|^2 df/B^3$ respectively.

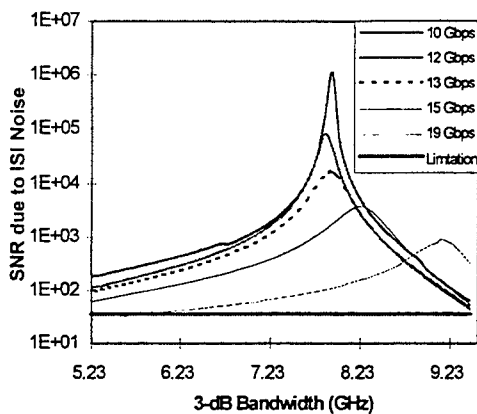


Fig. 5. The Bandwidth Dependent Signal-to-ISI -noise Ratio : For a given bit-rate, there exists an optimum bandwidth for an almost ISI free operation.

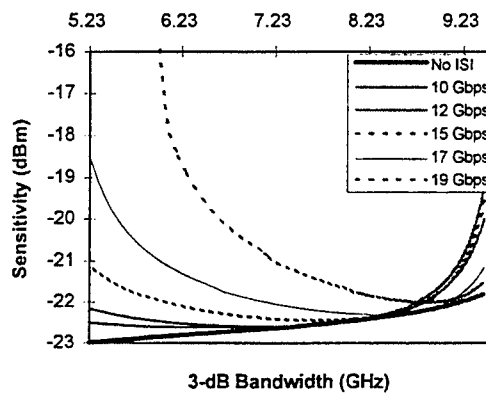


Fig. 6. The Bandwidth Dependent Overall Sensitivity : Both the circuit noise and the ISI noise are included.

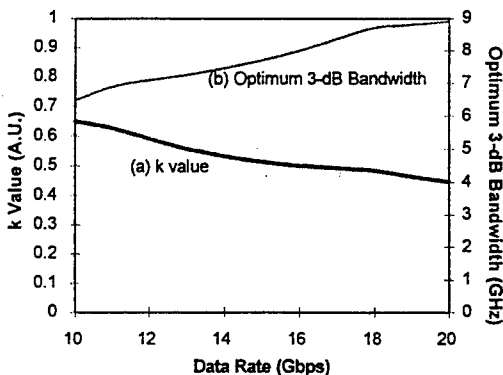


Fig. 7. k versus Data Rate : We define the k factor as $f_{3\text{dB_opt}} = k B$ ($k < 1$) where $f_{3\text{dB_opt}}$ is the optimum 3-dB bandwidth obtained as in Fig. 6. and B is the operating data rate. We can see that k value exhibits the values from 0.65 to 0.45.

Deep Cooling 2x128 Elements Hybrid Photoresistor Device for Spectral Range 6-20 μ Based on Epitaxial PbSnTe<In> Films Prepared by MBE Technique

V. N. Shumsky, G. N. Feofanov, A. A. Frantsuzov,
A. G. Klimenko, A. E. Klimov, N. I. Petikov,
T. U. Shafirova, S. N. Shalapaev, V. V. Soldatenkova

Institute of Semiconductor Physics, Russian Academy of Science,
pr. Lavrentjjeva 13, Novosibirsk 630090, Russia

The working out of photoresistor device (PD) appeared to be possible not only because of using PbSnTe<In> films with extraordinary properties as photosensitive elements, but also due to Si-multiplexers operating at $T < 20\text{K}$ and due to hybrid assembly technique with metallized polyimid ribbon cables.

The properties of lead-tin-tellurium (LTT) solid solution ($x=0.24-0.26$) doped with indium (In) have been investigated for the last few years [1,2]. The most interesting and unusual properties of this narrow gap compound ($E_g=0.06\text{ eV}$ corresponds to the red edge of sensitivity about $20\ \mu$) are almost intrinsic charge carriers concentration in darkness till liquid helium temperature and very long lifetime of nonequilibrium photoexcited charge carriers below temperature about 25K . Lifetime may achieved a value of a few seconds and more at $T=4.2\text{K}$. Nevertheless we have no any information about the creation of matrix or array PD based on LTT<In> epitaxial films.

PD consists of 2×128 elements photoresistor array having $100\ \mu$ period and $120\ \mu \times 80\ \mu$ area of each element, of four Si-multiplexers with 64 entrances on each of them which are connected to the array by metallized polyimid ribbon cables and of electronic units to control multiplexers. Fig.1 gives the general view of the PD.

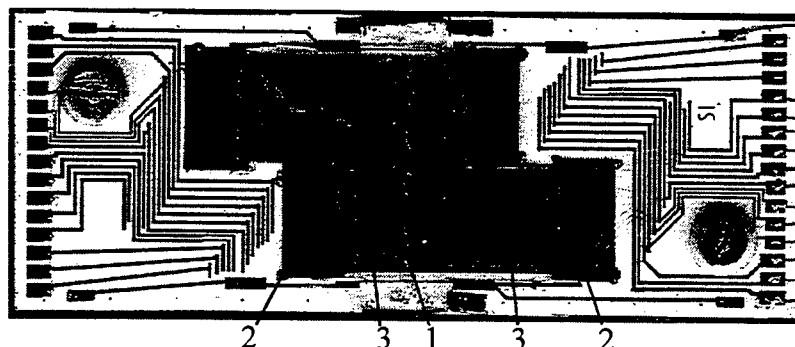


Fig.1 PD assembly. 1 - 2×128 elements photoresistor array, 2 - Si-multiplexers, 3 - polyimid ribbon cables.

Photoresistor arrays were formed on epitaxial LTT<In> films prepared by MBE technique on BaF₂ substrates. The thickness of the films was 1.35-1.5 μ. The average concentration of In through the films from the substrates to the film surfaces equals to 2-5 at.%. The peculiarities of the structure, composition and some other properties are described in [3]. As a rule the darkness resistance of a particular array element exceeds 10¹⁰ Ohm below T=20K and 10¹³ Ohm at T=4.2K.

PD characteristics were measured in special deep cooling chamber which contained blackbody source of irradiation supplied with ZnSe window and mechanical shutter. This chamber provides low level of background irradiation which stays below 10¹⁰ photons/cm²/s.

The spectral dependence of the array sensitivity was measured in optical helium cryostat with the level of background irradiation being rather high. Therefore in this case the element resistance didn't exceed (1-3)×10⁵ Ohm. The red edge of photosensitivity was disposed near 20μ.

The typical dependence of PD photosignal vs the element number for one of four multiplexers is given in fig.2. Bias voltage at photoresistors is equal to U=2.2 V, the base multiplexer frequency is equal to f=1 kHz (accumulation time - 1 ms). The sensitivity dispersion does not exceed ±20%. The noise of PD as a whole is determined by multiplexer noise and it is several times more than calculated 2qI noise of a particular photoresistor.

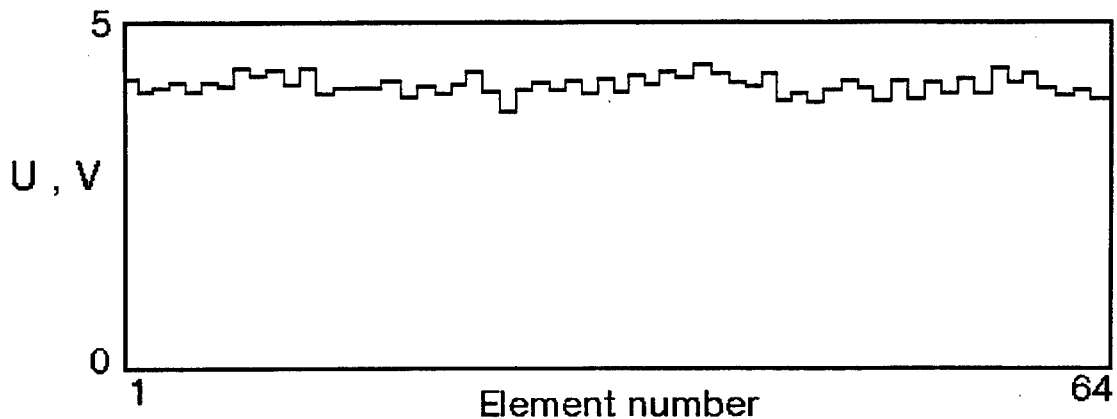


Fig.2 The dependence of output photosignal vs element number. T=10.4K.

The dependence of PD sensitivity vs blackbody temperature seems to be of special interest. It is given in fig.3. Current sensitivity was calculated using the values of output voltage, amplification coefficient, accumulation time and entrance capacity. The irradiation of the element vs blackbody temperature was calculated using transmission coefficient of ZnSe window. One can see that the sensitivity is rising about 30 times during blackbody cooling from room temperature to liquid nitrogen temperature and exceeds 200 000 A/W at bias voltage U=2.2 V. The sensitivity rises due to the increase of nonequilibrium charge carriers lifetime with the level of

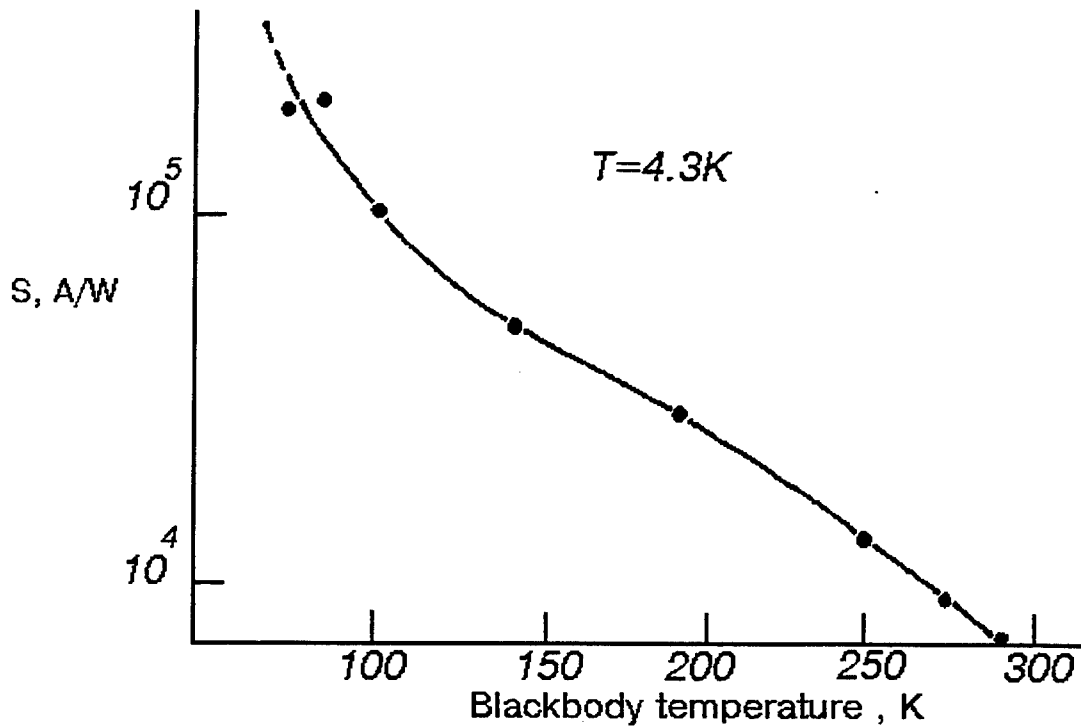


Fig.3 The dependence of the single element sensitivity vs blackbody temperature.

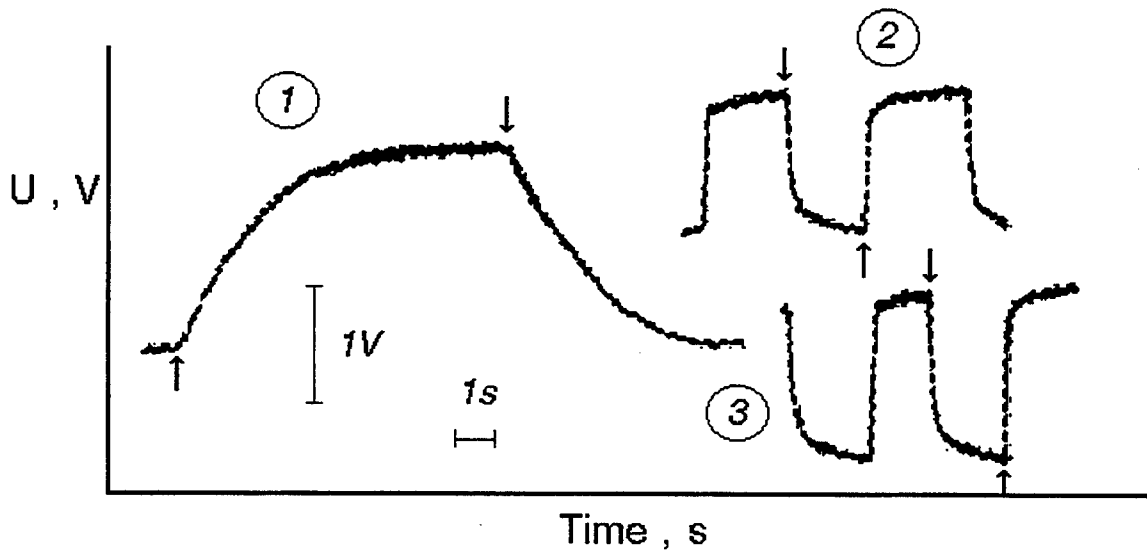


Fig.4 The time dependence of output signal for the three values of blackbody temperature, 1- $T_{bb}=77K$, 2- $T_{bb}=250K$, 3- $T_{bb}=300K$. Shutter "on" and "off" are marked by the arrows.

generation being lower at lower blackbody temperatures. It is proved by relaxation data of PD output photosignal of a particular element given in fig.4 for three blackbody temperatures.

In general the temperature dependence of the conductivity of LTT<In> being used as well as the dependence of relaxation time of the conductivity vs generation level

corresponds to radiative recombination. In addition radiative recombination seems to be more preferable because LTT is well known as a compound used for creation of injection lasers. On the other hand there are not enough experimental data for LTT<In> used in this work which would allow us to come to the final conclusion. We hope the wide possibilities of PD which is described in this paper will help us to find the answer on this question in the nearest future.

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HIGH-PRECISION DESCRIPTION OF MEMORY EFFECTS IN LOW-BACKGROUND IR DETECTORS.

Boris I. Fouks

Institute of Radioengineering and Electronics of RAS, Moscow.

The devices incorporating high-resistivity semiconductors, such as wide band gap or low-temperature devices, suffer often from memory effects. These effects are due to traps being abundant in such semiconductors. The traps vary their charges by generation and capture of free carriers over nonstationary processes caused by various actions. The trap charge integrated for a long time becomes so high that creates the field variations affecting essentially the current or the other characteristics of the operating devices. The higher the semiconductor resistivity, the longer the typical time of a trap recharging. Hence the characteristics of the mentioned devices at the moment depend on the long prehistory, that is, on all the events which affected such a device over a long period before the moment. This worsens the performance of the devices.

Below the memory effects are studied in more detail by the example of low-background IR detectors. We discuss the way these effects hamper the use of these detectors, present a high-precision description of the memory effects for the detectors of one important type, and show that such a description allows to use the mode of the fast detection of incident fluxes that markedly improves the performance of the detectors.

Low-background IR detectors are used to study the radiation of the Universe between 3 and 200 μm . This radiation is very low. To detect such a radiation the extrinsic silicon and germanium photoconductors doped by shallow impurities and cooled to helium temperatures have to operate in space. An accuracy of $\sim 1\%$ is required for such measurements. In the process the detectors exhibit the pronounced memory effects with the typical time being as much as 10^3 s or even longer. The length of an exact measurement has to be longer than this time as the detectors are calibrated at a direct current. There is no way to make the calibration under frequent step-like flux changes being best suited for the space applications, since the current in the process is coupled ambiguously with the intensity of the incident flux at the moment and depends nonlinearly on a great body of variable parameters: the flux intensities incident on the detector for a long time before the moment, their durations and order. The long time of the measurement makes it very costly, confines a list of measurements over a space flight.

To detect fast the incident fluxes one has to have an exact description of the transient current caused by frequent flux changes. The memory effects render the deduction of such a description particularly intricate. Nevertheless it has been deduced and is presented here. It generalizes the theory¹ of the response on a flux step after a steady state and, that is of first importance, gives a key to a large dividend in the ability of the detectors to solve space problems. Now it is being used to improve the operation of the Si:Ga detector arrays of the Infrared Space Observatory (ISO) being launched this year.

To study the physics of the trap memory we consider the simplest model of an extrinsic p-type photoconductor containing acceptors and donors in concentrations N and $N_d < N$; the donor level lies higher than

the acceptor one. With no generation all the donor electrons go in the acceptors (traps) with the result that their occupancy by holes f has the equilibrium value: $f_0=1-N_d/N$. The holes come to the valence band when generated from the traps by an IR radiation. Since the generation is so low that the free-hole concentration p satisfies the condition

$$p \ll N_d, N - N_d, \quad (1)$$

the occupancy of the traps remains close to f_0 . The detector has the contacts situated in the planes $x=0$ and $x=l$ and is under the voltage V_0 , that is, the mean field in the detector is $E_0=V_0/l$.

The detector operation is described by the simplified equations of the total current conservation, of Poisson, and of the trap recharging:

$$J/A = e\mu E p + (\varepsilon/4\pi) \partial E/\partial t, \quad (2)$$

$$\partial E/\partial x = 4\pi e N(f-f_0)/\varepsilon, \quad (3)$$

$$N\partial f/\partial t = p/\tau - G(t). \quad (4)$$

Here J is the total current, $E(x,t)$ the electric field, e the charge of a hole, ε the permittivity, A the cross-section area; μ and τ are the hole mobility and capture time; $\tau^{-1}=\gamma N(1-f_0)$, γ the capture coefficient. If the generation is optic its rate $G(t)=\alpha I(t)$, where α is the absorption coefficient and $I(t)$ is the variable photon flux.

A boundary condition describing the contact injection of holes has to be added to Eqs.2-4. Under the chosen positive voltage the injecting contact lies at $x=0$ and the boundary condition has a form:²

$$p(0, \Delta t) = p(0, 0) \exp[\Delta E(0, \Delta t)/E_j]. \quad (5)$$

Eq.5 shows the way the deviation $\Delta E(x, \Delta t)$ from the field distribution existing in the bulk at an arbitrary initial instant, $\Delta t=0$, varies the near-contact hole concentration $p(0, \Delta t)$ from its initial value. $E_j \approx T/eL$ is the characteristics of the injection ability of the contact; L the width of the near-contact space charge region, T the temperature in the energy units. Eq.5 implies a very important general feature of the contacts to high-resistivity semiconductors: they are ohmic at a steady state but inject highly the nonequilibrium free carriers during nonstationary processes owing to even small field variations. If IR detectors operate in space conditions the field E_j is low: ~ 10 V/cm or even less.

Consider the physics of the photoresponse for the detector being in a steady state before a flux change. Let the flux rises by step. A flux rise generates from traps the added free holes which drift to the drain contact with the velocity $v_0 = \mu E_0$. This process gives a step-like response on the flux step: its typical time is equal to the shorter of the times, τ or l/v_0 .³ This current step the higher, the more the share of the generated holes swept-out in the drain contact; the rest holes are trapped again fell short of the contact. The lower the field, the lower the efficiency of the hole sweep-out and hence the current step. After the step the current varies very slowly. When a hole leaves a trap this latter remains negatively charged. The trap charge rises as time passes since the holes continue to be generated and swept-out. This charge deviates the field from the steady-state value E_0 . Initially the field rises mainly to the injecting contact and falls to the drain one. Next,⁴ spatial field oscillations caused by the trap-recharging waves (TRWs)⁴ appear.^{1,3,5} Their amplitude rises and spatial period shortens as time

passes. The field changes affect the current by two ways. Firstly they affect the hole velocity in the bulk and thus the sweep-out efficiency. This causes variously shaped current changes, including oscillations, with the typical TRW time $\tau_b = \epsilon A E_0 g / 4\pi J^{\infty}$; here J^{∞} is the steady-state current at the given flux, $g = \tau v_0 / l$. Secondly, the field rise at the point $x=0$ increases the contact injection and thus the current with the typical time $\tau_j = \epsilon A E_j / 4\pi \beta J^{\infty}$, where $\beta = 1 - g[1 - \exp(-1/g)]$. The times τ_j and τ_b depend on the incident flux. The lower the flux, the slower the integration of such a charge which is able to vary the field sufficiently for an essential current change.

Hence the memory effects are due to the inhomogeneous field structure caused by the trap charge which is generated by the elapsed flux changes. This field governs the contact injection and the sweep-out efficiency, and thus controls the current response on a new flux step. In order to describe with a high degree of accuracy this response one has to describe first the processes caused by the previous flux changes, to find the field everywhere over the bulk after these processes, and then to use this field distribution as the starting one for the required description. This way is real, promises a great benefit when applied to space observations, but demands cumbersome numerical calculations.

The above physical picture says that this procedure can be highly simplified without loss in accuracy, if the next inequality is true:

$$E_j / E_0 \ll 1, \quad (6)$$

If the left side of Eq.6 is negligibly small one can ignore the effect of field changes on the hole velocity. This means that the field change at the point $x=0$ only, but not at every point x , is responsible for the current relaxation; that is, the effect of the elapsed flux changes on a photoresponse is described by one parameter. Indeed, solving Eqs.2-5 in the case of a current relaxation at a fixed flux after arbitrary flux changes and designating $\gamma = 4\pi\beta / \epsilon A E_j$, we obtain the next expression:

$$J(\Delta t) = \beta J^{\infty} + \frac{(1-\beta)J^{\infty}[J(0) - \beta J^{\infty}]}{J(0) - \beta J^{\infty} + [J^{\infty} - J(0)] \exp(-\gamma J^{\infty} \Delta t)}, \quad (7)$$

where the initial current $J(0)$ reflects the effect of any prehistory. With Eq.7 and the calibrated detector parameters, β and γ , one can calculate J^{∞} from the response on a short irradiation by a fixed flux and defines this flux from J^{∞} and the detector calibration at a dc.

In practice this general approach has to be frequently specialized, as low-background detectors are very sensitive not only to an IR irradiation but also to the the other actions, say, to the fast temperature changes creating the same contact injection.⁶ This has been found in the ISOPHOT Si:Ga detector arrays where flux changes cause low temperature changes.⁷ As in these detectors $E_j / E_0 \sim 0.01$, one would expect a precision of $\sim 1\%$ from Eq.7. But the values β and γ calibrated in various experiments had a scatter far beyond 1% and ranged up to $\sim 100\%$. The analysis has pointed to the temperature changes as a reason of this scatter. With this effect one can derive the next expression instead of Eq.7:

$$J(\Delta t) = \beta J^{\infty} + \frac{(1-\beta)[J(0) - \beta J^{\infty}] \exp[\gamma J^{\infty} \Delta t + \Delta T(\Delta t) / T_j]}{1 - \beta + \gamma [J(0) - \beta J^{\infty}] \int_0^{\Delta t} dt' \exp[\gamma J^{\infty} t' + \Delta T(t') / T_j]}, \quad (8)$$

with the temperature change $\Delta T(t)$; $\Delta T(0)=0$. The detector parameter T_j is to be of order 0.1 K. Hence even the temperature changes of such an order vary markedly transient processes. Experimental tests have confirmed that Eq.8 describes the operation of the ISOPHOT Si:Ga detector arrays with a high degree of accuracy, that is exemplified by Fig.1.

As noted at the beginning of this paper the memory effects are inherent in any devices incorporating high-resistivity semiconductors. In line with this notion the analysis have shown that at the moment the main obstacles for the treatment of the operation of these arrays with an accuracy of 1% are created by their cold-readout electronics (CRE) which consists of silicon MOSFETs operating at helium temperatures and thus exhibiting the effect of traps of the frozen substrate. An additional trap memory can be also due to a high density of the interface slow traps which have to exist in the real MOSFETs operating at low temperatures and currents.⁸ The distortions of the CRE amplification ranges up to 10% that limits now the precision of the treatment.

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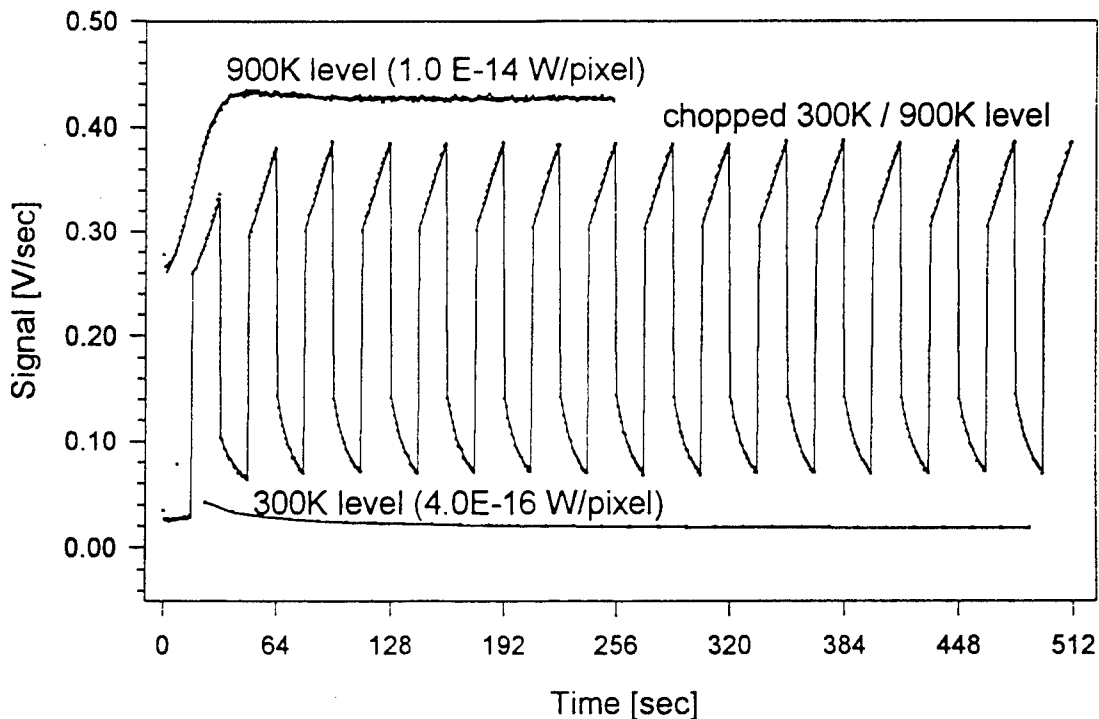


Fig.1.⁷ Measured (dots) and fitted (lines) photoresponses of the Si:Ga detector; the used parameters: $\beta=0.575$, $E_j=20.8$ V/cm, $T_j=0.276$ K.

GaSb/AlSb/InAs HBT-LED-RTD Structures for Complex Nanoelectronic Signal Processing and Computation

Lutz J. Micheel, Hans L. Hartnagel[†]

Wright Laboratory, U.S. Air Force, Wright-Patterson Air Force Base, Ohio

[†]Institut für Hochfrequenztechnik, Technische Hochschule Darmstadt, Darmstadt, Germany

1. Introduction: Internal Photon Streams

For future nanoelectronic arrays, complex signal processing and efficient computation are required. A proposed new family of HBT-LED-RTD circuitry addresses the former with A/D conversion circuitry and the latter with both binary and multivalued logic. We are applying optical methods of current summation to otherwise electronic circuitry. Precision photon streams are generated, and summed, that are equivalent to electron currents in conventional circuitry. *Strictly local* interactions of HBTs and LEDs are employed, and combined with stacks of vertically integrated RTDs for staircase and bit pattern generation. Non-local (especially vertical free-space) optical interconnects are also possible, and quite useful [1], but not addressed here.

The basic building block is an LED (or laser) as the load element of an HBT amplifier. Fig. 1a shows a very simple case of the new circuitry. The LED's photon stream drives the depleted base-collector regions of one or several HBTs in the next stage (Fig. 1b). Full optical switching of HBTs and HBT-like FETs was recently demonstrated by Breglio [2].

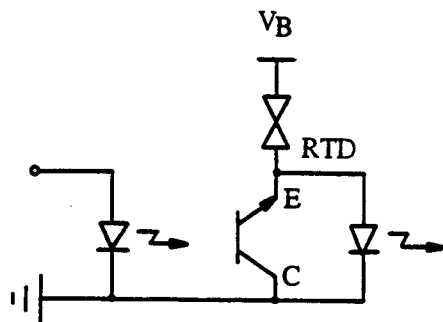


Fig. 1a Simple HBT-LED-RTD Circuit

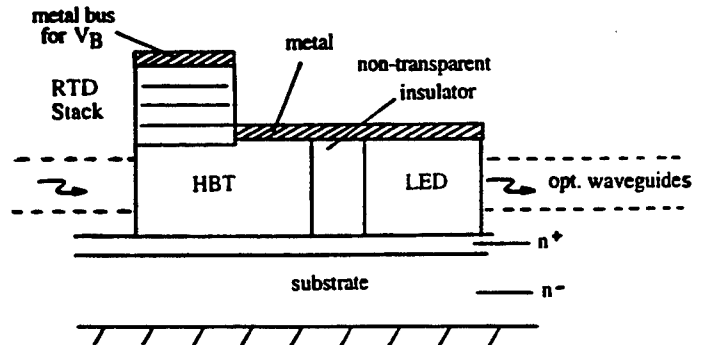


Fig. 1b Basic Structure

This new circuitry is aimed at very high packing density: it is essentially resistor free; it requires no voltage signal-level shifting subcircuits; the RTD-HBT structure is 3-dimensional; and parasitic electrostatic interaction of densely packed circuits is prevented by the optical isolation and the buried optical interconnects.

2. Fabrication Sequence

The fabrication sequence for the LED is based on a significant body of recent accomplishments by the workers in the field [3]: GaSb substrate, n-GaSb(2 μ m, n-AlSb(4nm), GaSb(50nm), p-AlSb(4nm), p-GaSb(1 μ m), metal (Fig. 2). Electron-hole

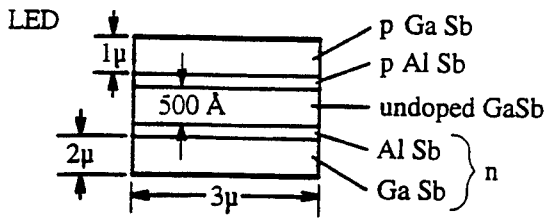


Fig. 2a LED Structure

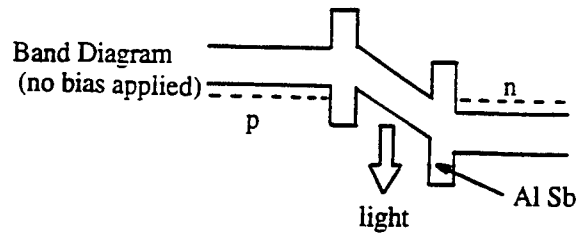


Fig. 2b Band Diagram, no bias applied (direction of light emission indicated)

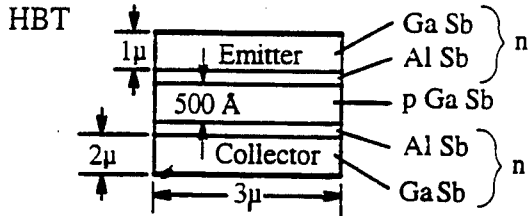


Fig. 3a HBT Structure

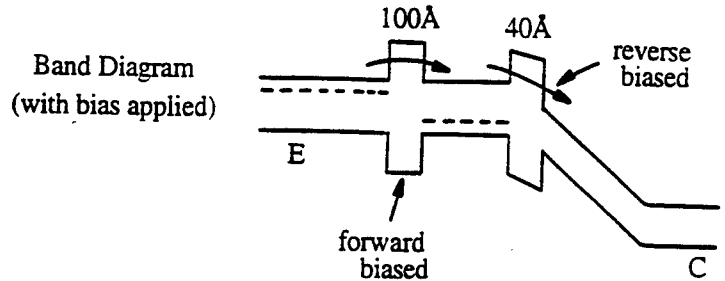


Fig. 3b HBT Band Diagram

recombination occurs in the undoped GaSb layer which has a refraction index of 4.0 and is also used as the optical conduit between stages. The AlSb barriers are thin enough for carrier tunneling and also act as confinement layers ($RI=3.8$) for the optical conduit. For the HBT, the top three layers are etched off preferentially, and are regrown: p-GaSb(50nm), n-AlSb(10nm), n-GaSb(1 μ m), metal (Fig. 3).

Resonant tunneling transistors (RTTs) are some of the most important components in nanoelectronic circuitry [1, 4, 5]. Near-term and quite robust RTTs are implemented as HBTs with series of RTDs in the emitter branch. For this purpose a stack of equal-sized RTDs is grown on the HBT emitter: m times {spacer, AlSb(5nm), InAs(5nm), AlSb(5nm)}, GaSb(500nm), metal (Fig. 4a). The RTDs exhibit peaks of similar height (Fig. 4b). To implement certain ternary and quaternary logic functions, RTDs with *different* peak currents are used (Fig. 4c) which will be covered in a future publication.

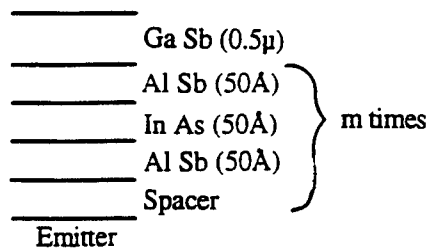


Fig. 4a Multiple RTD (or "RTD Stack")

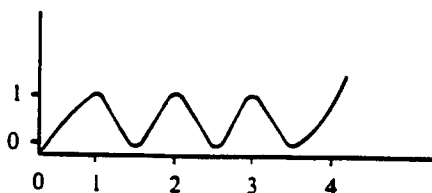


Fig. 4b RTDs of Equal Design (not to scale)

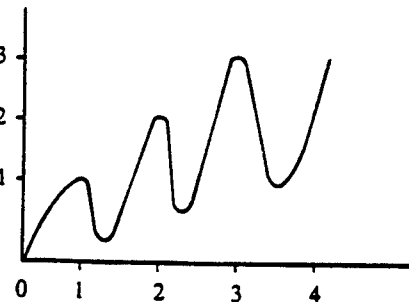


Fig. 4c RTDs with Different Peak Currents (not to scale)

3. Metering of the Photon Stream

In earlier A/D converter and multivalued logic work, resistor ladders were used to divide the signal input voltage in ratios of the powers of two [4, 5], but resistors are very wasteful in chip area and preclude attempts at extremely dense component packing. In the optical domain, however, the width of the waveguides can be tailored in highly compact fashion; precision metering of the photon stream in a 4:2:1 (or possibly 8:4:2:1) ratio affords a most compact implementation of A/D converters and redundant positive-digit multivalued logic similar to the earlier work. There are two ways of accomplishing this. In the first approach the *photon stream* is tailored (Fig. 5a) and the recipient RTDs are all of the same size; the HBTs act only as photon-to-electron/hole-pair converters, and as linear amplifiers [5]. The least-significant-bit subcircuit (LSB) receives the full photon stream, with a conduit width of *four*, and—in terms of the transfer functions of Fig. 5b—it switches most rapidly. The next bit (width of *two*) switches at 1/2 that rate, and the most significant bit (MSB, width of *one*) at 1/4 the rate. This 4:2:1 ratio generation by means of tailoring the photon stream is equivalent to *resistor ladder* tailoring of the voltage each bit-subcircuit receives [4, 5]. The transfer curve is equally well suited for non-Gray code ADCs similar to [4], for redundant positive-digit multivalued logic [5], and for higher-order binary adder building blocks [6].

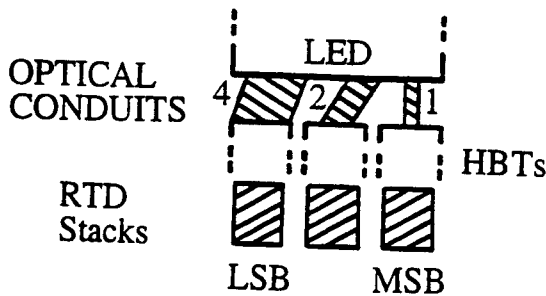


Fig. 5a 4:2:1 Tailoring of the Photon Stream

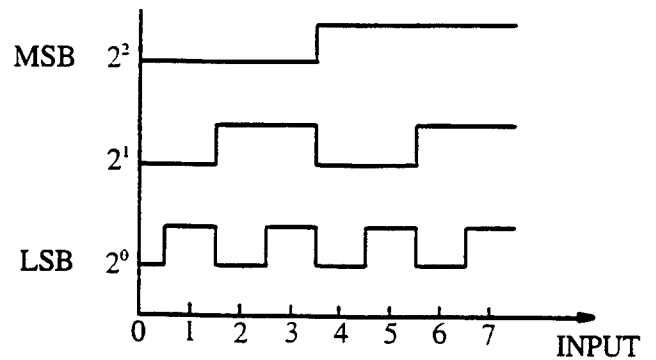


Fig. 5b Transfer Function

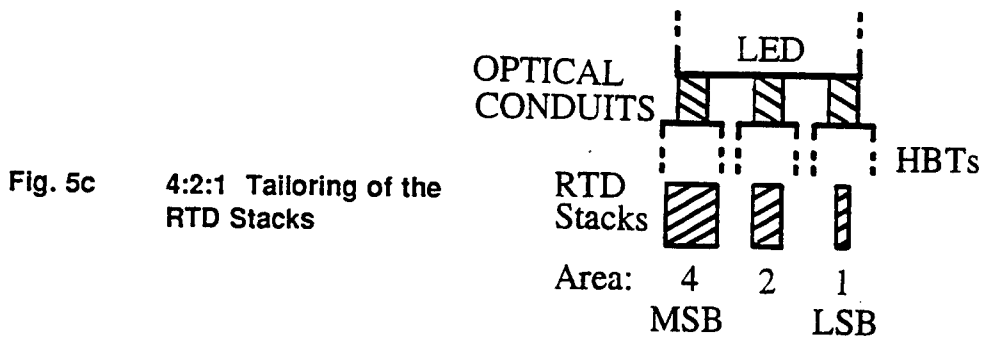


Fig. 5c 4:2:1 Tailoring of the RTD Stacks

In the second approach all the photon streams are the same, and the *recipient RTD stacks* are tailored instead (Fig. 5c) [7]. Here the RTD stack with an area of *one* switches most often (LSB), in terms of the transfer function, and the one with an area of *four* least often (MSB). This again replaces (in the photon-stream domain) the resistor ladder operation (in the voltage domain) of the earlier circuit concepts. The second method is preferred initially, before experimental data is available on design methods for the accurate photon stream metering under the first approach.

4. Device Designs

Device calculations and initial layout designs were conducted. Minimum LED dimensions of $3 \times 3 \mu\text{m}^2$ appear most suitable for the early experiments in order to get an even, high-intensity light output. Minimum HBT dimensions of $1 \times 3 \mu\text{m}^2$ are considered initially but may have to be increased when the 4:2:1 area-tailored RTD stacks are grown on the emitter. For future implementations of this new IC family with highly scaled-down devices, area reductions of over 180:1 are expected in comparison to conventional implementations using resistor ladders.

5. Conclusions

Many *electron current* properties of conventional circuits are duplicated, or improved upon, by the *photon stream* properties of this new HBT-LED-RTD circuit family. Of particular importance is the precision metering of these photon streams and the highly compact bit pattern generation for ADCs, multivalued logic and multivalued arithmetic. Very high component packing densities appear feasible.

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Periodic Conductance Oscillations at Room Temperature in Novel Metal-Nano-Tip/Insulator/Semiconductor Anti-Dot Arrays

Junji Haruyama¹, Martin Moskovits², Dmitri Routkevitch², Alex A. Tager¹, and J.M. Xu¹
¹Dept. of Electrical Engineering and ²Dept. of Chemistry, University of Toronto,
10 King's College Rd., Toronto, ON, Canada, M5S 1A4. Tel.: (416)978-8935

ABSTRACT

One- or zero-dimensional structure devices, such as single electron memory[1] and point contact devices[2], have recently attracted great interest. Although much experimental and theoretical research has been reported, the mainstream technology such as epitaxial growth followed by nanolithography and etching remains costly and complicated and seems to approach its limits both in terms of minimum size and increasing packing density. Recently, we have reported on novel nanowire array devices [3] made by electrochemical deposition (ED) of metals into pores of anodic aluminum oxide (AAO) templates. This method allows us to prepare different nano-scale structures (i.e. metal [3] or semiconductor [4] nano-wire arrays and their combinations) with a high packing density and high aspect ratio. Arrays of Ni nano-wires sandwiched in between metal/oxide layers have shown stair-case I-V characteristics at room temperature[3], reminiscent with features of single-electron tunneling through low-capacitance oxide junction[3][5].

In this presentation, we report some new interesting features observed in a novel structure of metal nano-wire/semiconductor anti-dot array fabricated by using the above non-lithographic method. The Ni-wire array was obtained by ED of Ni into the pores of AAO film [3]. The diameter of Ni-wires and area density were about 35-40 nm and $2 \times 10^{10} \text{ cm}^{-2}$ respectively. After etching back part of the AAO matrix to expose the top portion of the wires, a 1 μm thick film of n-CdS was electrochemically deposited. The semispherical top of Ni nano-wire in this structure is surrounded by a n-type CdS (Fig. 1). The interface between the Ni core and the CdS shell consists most probably of several to tens monolayers of nickel oxide enriched with S as a result of exposure to air prior to CdS deposition and to the CdS deposition medium at elevated temperatures.

To date, DC measurements on several samples have been performed by using a semiconductor parameter analyzer(HP4145A) and an electrical shield box in order to avoid the affect of noise from outside at room temperature. Nearly periodic oscillations of conductance were observed at room temperature as shown in Fig.2 when a negative voltage (V_R) was applied to CdS as shown in Fig.1-(a). The periodic oscillation is superimposed on an ohmic current-voltage dependence at $|V_R| < 300 \text{ mV}$. As many as 41 oscillations were counted in the range 0 to 500 mV ($|V_R|$). The period of oscillations is as small as 12 mV, which is smaller than $kT/q \sim 26 \text{ mV}$, at $|V_R| < 200 \text{ mV}$ as shown in Fig.3. The current step for a single oscillation is 20 μA . The periods and the oscillation amplitudes tend to increase at higher $|V_R|$ as shown in Fig.3 and 4. Furthermore, a negative conductance appears at around 400 mV (Fig. 4). Currently we are collecting additional results to correlate the oscillation features with dimensional and compositional parameters of the arrays.

Although at the present stage, any explanation must remain largely speculative due to the complex combination of many classical and quantum effects involved in this system, several models are being examined for these observed features, including Coulomb Blockade from coupling the nano-wires to the CdS, resonant tunneling through the nanometric half-shell potential well induced at the $\text{NiO}_x\text{S}_y/\text{CdS}$ interface, quantization of the conductance by point contact at the tip of Ni-wire, and quantum fluctuation. In the explanation using a Coulomb Blockade theory, it will be needed to extend the theory to that of the multi-coupled nano-wires system because tunneling resistivity of our sample is approximately 0.25Ω which is smaller than $25.8 \text{ K}\Omega$ of resistance quantum(h/e^2). Also in the explanation using a resonant tunneling model, it will be needed to extend the usual model to that of semispherical system with electron transportation from 3-dimension to 1-dimension. Actually, it has been reported that the top of tip of nanoprobe makes the potential shape at the surface of the measuring tunneling device parabolic[6]. In such parabolic system, periodic conductance oscillation may be observed because the energy spacings of localized states are equal. Details will be presented in our talk.

One of the intended device applications of this novel structure is in large area electroluminescence display with reduced voltage. To this end, different material combinations are being explored, and will be reported as well.

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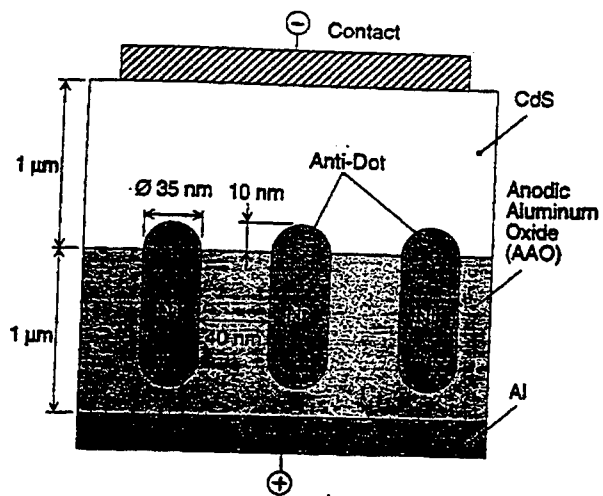


Fig. 1(a): Schematic Cross Section of Arrays

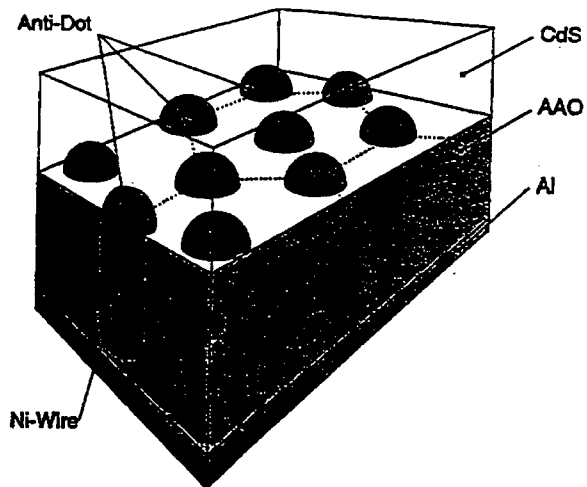


Fig. 1(b): Schematic Overview of Arrays

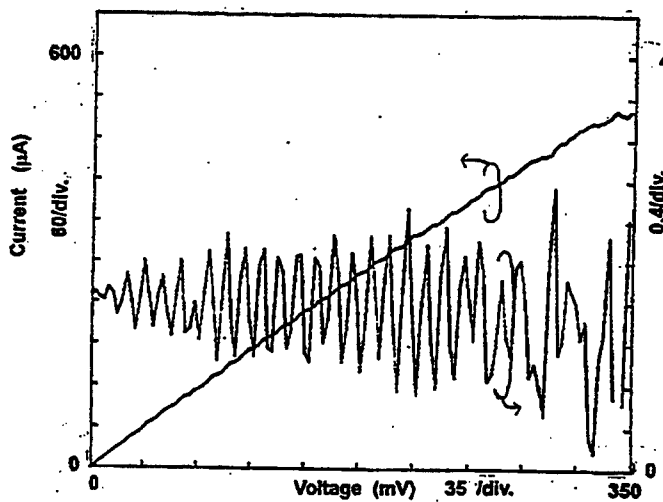


Fig.2 (a) : Current and Conductance vs. Voltage

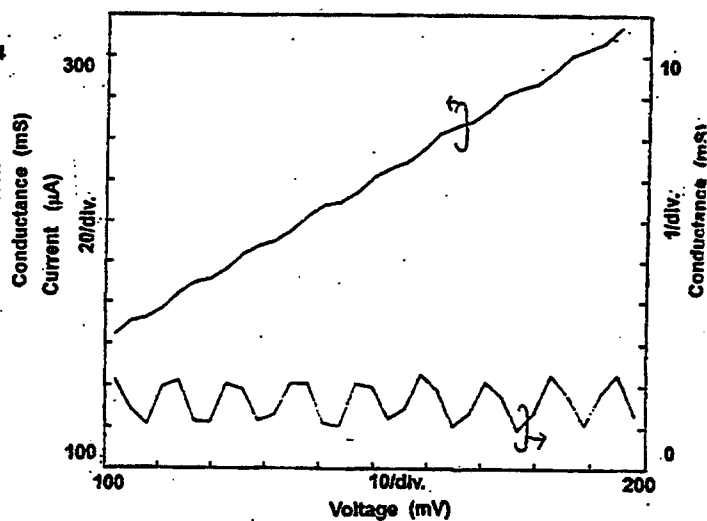


Fig.2 (b) : Characteristics in Voltage range from 100 to 200 mV in (a)

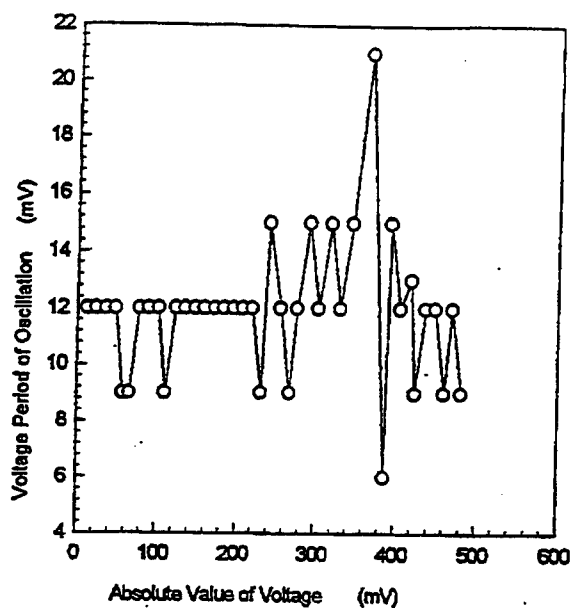


Fig.3 : Voltage Period of Oscillation on Applied Voltage(V_x)

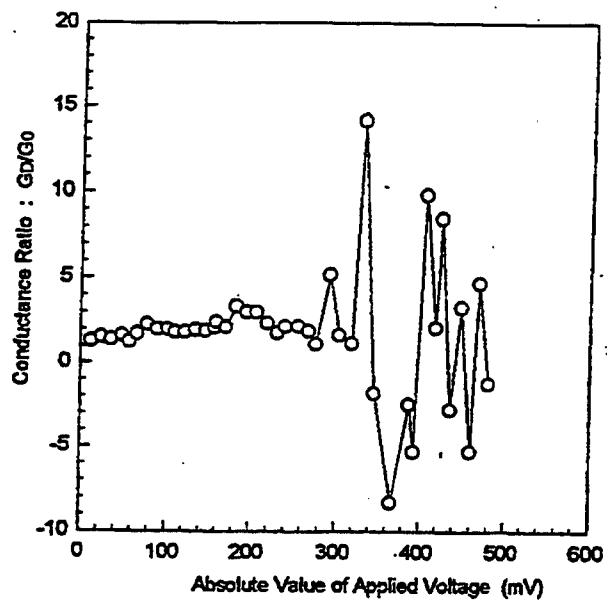


Fig.4 : Conductance ratio on Applied Voltage(V_x)

G_D and G_0 are maximum and minimum values of conductance oscillation respectively

Photoeffect as a possible explanation for conductance quantization in nanostructured GaAs Schottky diodes

*H.-W. Hübers, E. Bründermann, H. P. Röser
DLR, Institute for Space Sensor Technology
Rudower Chausse 5, D-12489 Berlin, Germany*

Nanostructured GaAs Schottky diodes are frequently used as mixers in THz heterodyne receivers. Experiments have shown (see paper of H. P. Röser et al. at this conference) that the optimum current I_{opt} which is necessary to achieve lowest receiver noise is given by

$$I_{opt} = N_e e \nu, \quad (1)$$

where ν is the frequency of the local oscillator (LO) radiation (from a far-infrared laser or a klystron) which pumps the Schottky diode mixer and e the electron charge. N_e is the number of electrons which contribute to the optimum current I_{opt} (about 1300 to 4500). These electrons are due to an active depletion volume of thickness D_{depl} (about 200Å to 300Å). A remarkable result is that the electron transport in these diodes is governed by h/e^2 .

The electrons move ballistically through the active depletion volume. This is supported by the experimental fact that cooling of the diodes down to 20 K lowers the noise only by a small amount (less than 30%). Part of this improvement is not due to the Schottky contact itself but due to the embedding network. In addition, the thickness of the active depletion volume D_{depl} is smaller than the mean free path L_{fp} indicating ballistic transport of the electrons already at room temperature (see table 1).

Diode		J118	1I7	1I12	1T15
D_{depl}	[Å]	324	270	260	210
L_{fp}	[Å]	835	635	520	350

Table 1: Thickness D_{depl} of the active depletion region and mean free path L_{fp} of the electrons.

As a possible explanation for these results we propose a photoeffect. At the LO power levels used in the experiments the Schottky diode can be considered as a

square law type mixer. For such a device the photocurrent is given by

$$I = \eta \frac{e}{h\nu} P_{LO}, \quad (2)$$

where η is the quantum efficiency of the mixer. The LO power can be replaced by $P_{LO} = n h \nu^2$ with n the number of photons emitted by the LO. Under optimum mixing conditions (i.e. lowest receiver noise) the quantum efficiency is given by $\eta = N_e/n$. Together with eq. (2) this yields eq. (1). Furthermore we assume that one photon is absorbed by one electron. The energy of the photon is transformed into kinetic energy of the electron. If one expresses the kinetic energy W_{kin} in terms of a voltage V_0 , meaning

$$W_{kin} = eV_0 = h\nu, \quad (3)$$

one gets in combination with eq. (1)

$$V_0 = \frac{1}{N_e} \frac{h}{e^2} I_{opt}. \quad (4)$$

The voltage V_0 can be determined from the mobility of the electrons. A plot of V_0 as a function of I_{opt}/N_e yields $(25750 \pm 600)\Omega$ in close agreement with h/e^2 .

The important consequence of eq. (4) is that a single electron is connected to the fundamental resistance h/e^2 . Since the active depletion region of the Schottky diode has to be filled and emptied within one cycle of the LO radiation the electron has to move the distance $2D_{depl}$ within the time of one LO cycle. The classical resistance of a sample of length $2D_{depl}$ and cross section A is given by $R = 2D_{depl}/(\sigma A)$ with the conductivity given by $\sigma = e\mu N_d$. This leads to

$$R = \frac{1}{N_e} \frac{h}{e^2}. \quad (5)$$

The measured series resistance R_S is bigger than R because it includes contributions from the undepleted epitaxial layer and the GaAs bulk material (see table 2). Eq. (5) describes the resistance of a classical network of N_e resistors of magnitude h/e^2 in parallel. This view is supported by a power analysis. If the energy is of N_e photons is transformed into the optimum current through a resistor R , i. e. $N_e h \nu^2 = R I_{opt}^2$, one gets again eq. (5). This equation might be viewed as a special case of the Landauer Büttiker formula with two electrons per channel.

Diode		J118	1I7	1I12	1T15
R_S	[Ω]	30	13	33	20
$R = h/(N_e e^2)$	[Ω]	9.2	5.7	11.7	19.9

Table 2: Resistances of the Schottky contact. R_S is the measured series resistance which is bigger than R because it includes contributions from the GaAs bulk material.

Switching Behavior of Quantum Cellular Automata

P. Douglas Tougaw and Craig S. Lent
Department of Electrical Engineering
University of Notre Dame, Notre Dame, IN 46556

There has been considerable recent interest in the possibility of developing a device technology based on interacting quantum dots. It has been shown theoretically that digital circuits could be constructed from cells composed of Coulomb-coupled quantum dots in a so-called quantum cellular automata (QCA) design. Within each cell, electrons can tunnel from dot to dot. Between cells tunneling is suppressed but the Coulomb interaction remains. This transistor-less technology would be based on mapping the ground-state of the many-electron problem onto the solution of the computational problem at hand. To date, attention has focussed primarily on determining the ground state of the cellular array and verifying that the correspondence with useful computational problems can be made. Here we focus on the dynamic switching behavior of QCA arrays.

Each QCA cell consists of four quantum dots with two electrons tunnelling between the dots. A fabrication schematic and two examples of such cells are shown in Fig. 1. While the near-neighbor distance between two dots within one of these cells could be as large as 20 nm, cell response will improve as this distance is reduced.

Due to the electrostatic interaction between the two electrons within a cell, they tend to align on antipodal dots as shown in Fig. 1. To measure how closely the state of a given cell matches one of these two arrangements, we define the cell polarization. As indicated in Fig. 1, the cell on the left has a polarization of +1 while the cell on the right has a polarization of -1. Cells that are in a mixture of these two states will have an intermediate polarization between -1 and +1.

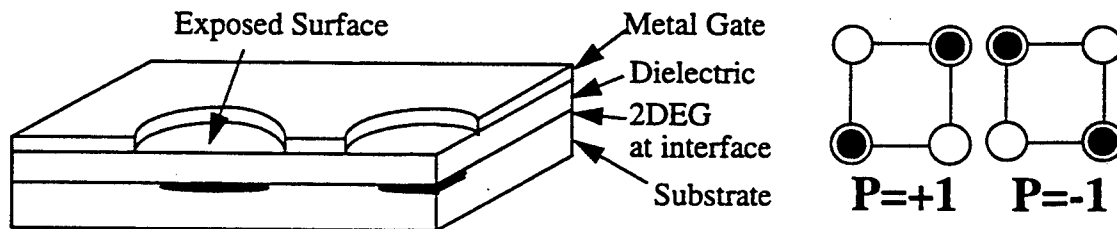


Figure 1. Schematic diagram of typical quantum-dot cells. The fabrication schematic shows how such cells could be fabricated. The two cells shown on the right demonstrate the two polarization states of the QCA cell.

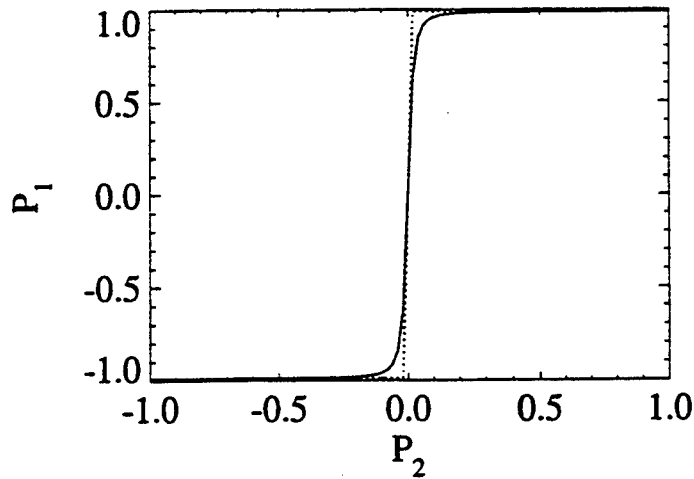


Figure 2. The cell-cell response function. The effect of the polarization of one cell on the polarization of a neighbor is highly nonlinear and bistable.

When such cells are placed near one another, the electrons interact Coulombically (tunneling between cells is suppressed). This Coulombic interaction causes the polarization of one cell to have an effect on the polarization of its neighbors. If we vary the polarization of one cell and measure its effect on the polarization of a neighboring cell, we can generate the “cell-cell response function”, which is shown in Fig. 2. The highly nonlinear and bistable nature of this response function indicates that it will be possible to rapidly recover from local decreases in polarization due to fabrication irregularities. Essentially, one is using the physics of the two-electron system to provide the nonlinearity which plays the role of gain in conventional devices — restoring signal levels at each stage. Note that current gain or voltage gain are not appropriate concepts here because the signal is being encoded in the cell state rather than in a classical voltage or current.

When a linear array of these cells is created, the information encoded at one end of the wire is transmitted to the other end. The behavior of a line of cells is shown in Fig.3.

Such a “binary wire” can be used to connect logical devices constructed using QCA cells. The most fundamental QCA logical device is the majority logic gate, shown in Fig. 4. In a majority logic gate, the device cell (in the middle) and the output cell (shown here on the right) align in the same direction as a majority of the three inputs. The output can then be connected to other devices using a binary wire. In addition, a majority gate can be used to create a programmable AND/OR gate if one of the three inputs is taken to be a program line to select between the two functions. Using majority logic gates, binary wires,

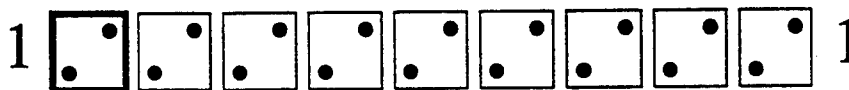


Figure 3. Transmission of information along a binary wire.

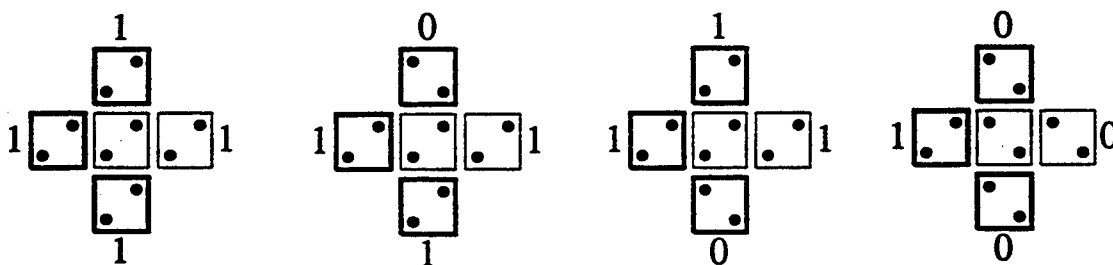


Figure 4. Four different majority logic gates. The device cell (in the center) and the output cell (to the right) always match a majority of the three inputs.

and inverters (which are realized by using the cell's diagonal anti-voting behavior), it is possible to generate any Boolean function. The most complex function simulated thus far is a one-bit full adder, which requires only 1.5 square microns using the largest design rule.

The dynamic behavior of a binary wire is shown in Fig.5. At $t=0$ ps, the cell on the left side of the wire has been switched and is held at $P=+1$. In the time immediately following this switch, the other cells in the line also proceed to switch in that direction. By $t=20$ ps, the polarization "kink" has almost completely left the system. The propagation time of approximately 2 ps per cell will decrease as cell size shrinks; a macromolecular

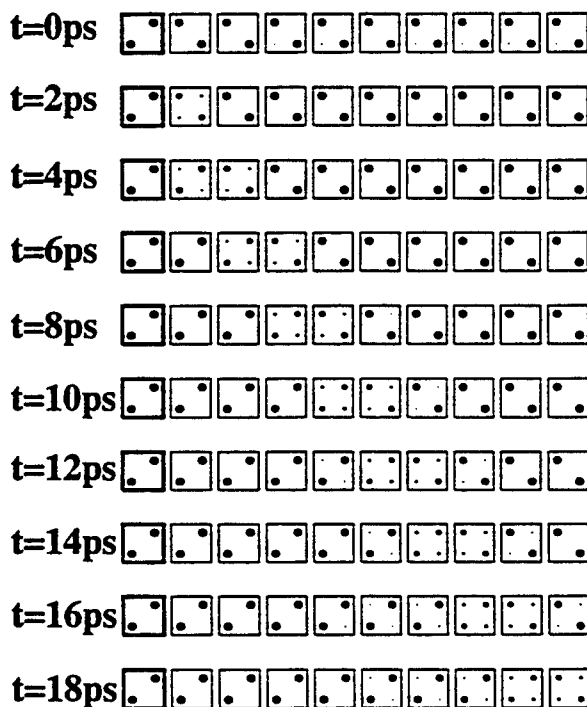


Figure 5. The dynamic behavior of a binary wire. Propagation of information between neighboring cells requires approximately 2 ps, but this time will decrease as cell size shrinks.

implementation of these cells would propagate information 100 times faster than this.

Finally, the dynamic response of a majority logic gate is shown in Fig. 6. In this case, the binary wires leading up to each of the inputs and away from the output have been included for completeness. Before $t=0$, a majority of the three inputs are in the $P=-1$ state, but the bottom input is then switched so that the majority changes to $P=+1$. The device cell and the output cell correspondingly change directions, and the kink begins to propagate away from the majority gate just 10 ps after the input was fully switched.

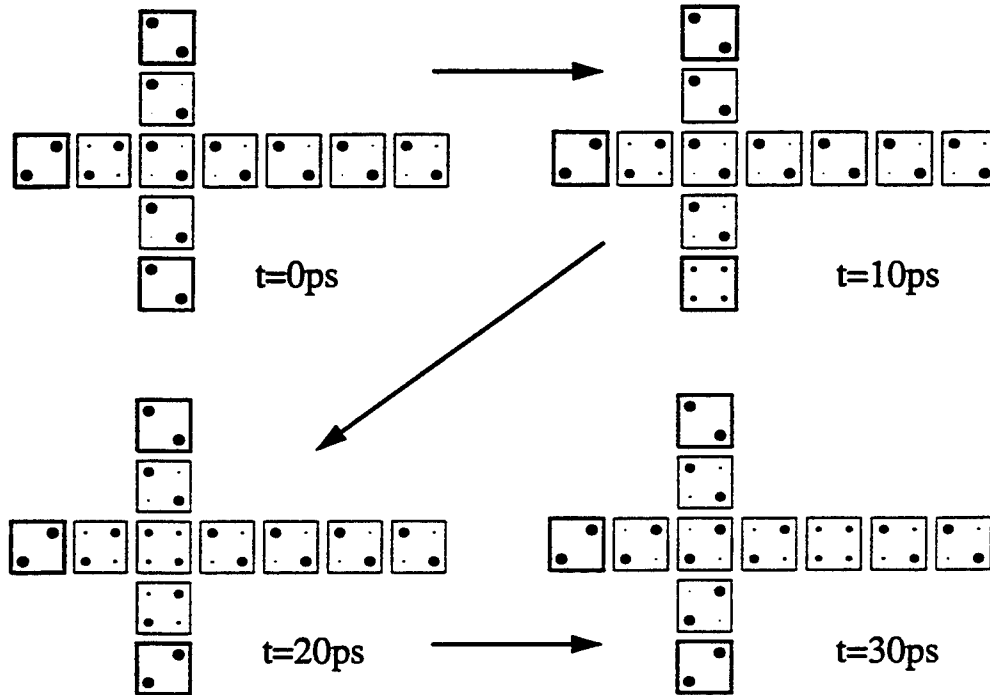


Figure 6. The switching response of a majority logic gate with input and output leads. A change in the bottom input causes the output cell to change, and the kink is propagating away from the device just 10 ps after the cell is switched.

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A Percolation Model for Rapid Vacancy Diffusion during Initial Void Growth in Minimum-Size VLSI Conductors

Barbara. A. Oakley and Hoda S. Abdel-Aty-Zohdy

Microelectronics System Design Laboratory
Department of Electrical and Systems Engineering
Oakland University, Rochester, Michigan 48309

Abstract

High concentrations of vacancies at the initial stages of void growth in narrow metal film very large scale integrated circuit conductors can affect vacancy diffusion in ways which cannot be modeled through straightforward application of Fick's laws of diffusion. This effect can be seen in the nonlinear relationship between atomic flux and atomic density in the initial stages of the high resolution resistance measurements which are indicative of void growth within metal films. To date, the various models for void growth contain only partially satisfactory explanations for observed experimental behavior. In this paper, a model utilizing percolation theory is presented that allows for mathematical analysis of the observed non-linear incremental resistance. This model can account more simply and realistically for experimental results.

I. Introduction

As line widths have narrowed in VLSI circuits, an in-depth understanding of the complex modes of failure in minimum-size conductors has become imperative. Electromigration, because of its ubiquitous nature and catastrophic results (including complete opening or shorting of circuits), has received especial attention. A variety of different models related to the basic physical mechanisms leading to electromigration have been suggested [1-6] but, as De Munari, et al. [7] have stated: "Overall comprehension of the phenomenon is still unsatisfactory." What is known, however, is that a key cause of failure in metal film conductors is void growth.

There is a substantial amount of stress on thin metallic films deposited on oxidized silicon substrates. This stress has been hypothesized to be alleviated through void growth that occurs during cooling and room temperature aging. Voids grow by the diffusion of vacancies provided by dislocation climb to the stress free void surface. A dislocation climbing under the influence of the vibrational frequency of the lattice will continue until:

$$C_v = C_{v_0} \exp(-\sigma \Omega_v / kT) \quad (1)$$

where C_{v_0} is the thermal equilibrium vacancy concentration in the absence of stress, Ω_v is the vacancy volume, and σ is the amount of stress retained in the metal conductor after passivation[8]. Each dislocation leaves behind a sheet of vacancies which disperse throughout the metal crystal. In a narrow conductor with "bamboo" structure containing

voids at some of the grain boundaries, vacancy diffusion along the grain boundaries to the voids can be assumed to be practically instantaneous compared to lattice diffusion. Thus the flux of vacancies can be considered to be equal to the flux of lattice vacancies into a grain boundary with a void.

Furthermore, if two vacancies are formed on neighboring lattice sites in aluminum, the resulting double vacancy is more stable than the configuration consisting of two single vacancies far apart. The activation energy for the motion of a double vacancy through any face centered cubic metal crystal is about one-half that for a single vacancy. Vacancy pairs are, therefore, highly stable and highly mobile in metals such as aluminum [9].

A common misconception about diffusion is that it occurs when atoms or, in this instance, vacancies, simply switch places. In actuality, a simple exchange of position does not allow long-range migration to occur. After any exchange, a given vacancy must move yet again *away* from, instead of back into, its initial position. After these *two* moves, the vacancy will have completed *one* diffusion step in an fcc lattice. (In the silicon lattice, by way of contrast, a vacancy must diffuse to at least a third-nearest neighbor in order to complete one diffusion step.)

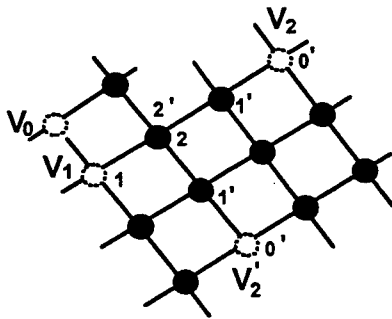


Figure 1a: Configuration of vacancies at high concentration.

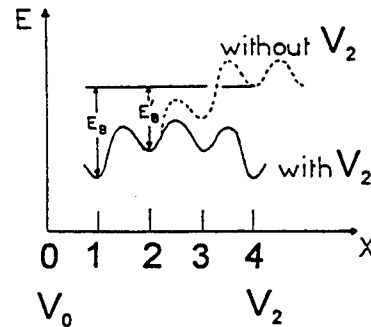


Figure 1b: Corresponding energies of the vacancies.

Figure 1 illustrates the vacancy potential as a function of coordination site away from a pair of vacancies. The important idea to catch here is that the presence of a vacancy within four "moves" of a vacancy pair lowers the effective energy of formation of a vacancy by E_b : the binding energy between a vacancy at position "0" and a vacancy on a second neighbor site "2". In this case the second neighbor site "2" is also a second neighbor site "2'" from V_2 or V_2' ; thus the vacancy has the same energy in this site as in site "2", and it can diffuse directly from V_1 to V_2 or V_2' with a potential barrier height smaller than that existing for the diffusion of an isolated vacancy. If a sufficient number of vacancies are connected in this way, they can freely diffuse in accelerated fashion through that portion of the lattice. Using the language of percolation theory, we will refer to that portion of the aluminum lattice which is exceptionally dense with vacancies as a "cluster." The concentration of vacancies in that cluster would be considered as having reached or surpassed the percolation threshold, p_c .

II. The Percolation Threshold and High Concentration Vacancy Diffusion

When concentrations of vacancies become very high, in fact, high enough that the effective energy of formation is lowered, we find that D_v (the general vacancy diffusion coefficient within the lattice) does not linearly relate J_v (the vacancy flux) to the variation in vacancy concentration. That is:

$$J_v \neq D_v \partial C_v / \partial x. \quad (2)$$

This inequality occurs because an implicit, yet fundamental assumption contained within Fick's Laws is that diffusing particles execute diffusion jumps independently. As we have shown, however, when the vacancy concentration is increased, the number of available lattice sites at which vacancies can remain unperturbed by other vacancies begins to diminish significantly. The result is that the effective concentration of vacancies is increased by a factor of $F = \exp(E'/kT)$ [10]. The corresponding flux at these high "percolation" vacancy concentrations is therefore given by:

$$J_v^{\text{Perc}} = F J_v^{\text{Low}} \quad (3)$$

If P_∞ is the probability that a given vacancy belongs to a cluster large enough to have the accelerated diffusion, the total vacancy flux is given by:

$$J_v = (1 - P_\infty) J_v^{\text{Low}} + P_\infty J_v^{\text{Perc}} \quad (4)$$

with the effective diffusion being characterized by the expression:

$$D_v^{\text{eff}} = (1 - P_\infty) D_v^{\text{Nom}} + P_\infty D_v^{\text{Perc}} \quad (5)$$

We note that P_∞ is actually the strength of an infinite network,¹ for which we have a formula:

$$P_\infty = K'(p - p_c)^\beta = K(p/p_c - 1)^\beta \quad (p > p_c) \quad (6)$$

Using this formula, we find that:

$$P_\infty = 0 \quad \text{for } C_v \leq C_v^{\text{perc}} \quad (7a)$$

$$P_\infty = K(C_v / C_v^{\text{perc}} - 1)^{0.4} \quad \text{for } C_v > C_v^{\text{perc}}. \quad (7b)$$

The lattice of fourth-neighbor positions that have equivalent lowered binding energy at the second-neighbor position has a coordinance of 20.² For this lattice, $p_c \approx$

¹ P_∞ is the first moment, M_1 , of percolation theory, which is the probability of an arbitrary site belonging to the infinite network. It should not be confused with p , which is the probability of an arbitrary site being occupied by a vacancy.

²The coordinance of this particular configuration is calculated by counting the number of positions on an fcc lattice which, at four moves away from the given initial position, also have the same number of moves away from each other at the second position.

0.073. The beta parameter of 0.4 is the critical order exponent in three dimensions [11]. K is computed to be 0.85, so that $P_\infty = 1$ for $C_v > 2.5 C_v^{\text{perc}}$ [10][12].

From geometrical considerations, then, we find that the critical "percolation" concentration of vacancies is

$$C_v^{\text{perc}} \approx 4.4 \times 10^{21} \text{ cm}^{-3}.$$

Note that this concentration of vacancies is not found throughout the metal crystal, but rather only in those clusters large enough and concentrated enough to have the accelerated diffusion. Since sheet dislocations, for instance, introduce vacancies along a single plane at concentrations even higher than that of C_v^{perc} , this value appears to be quite reasonable.

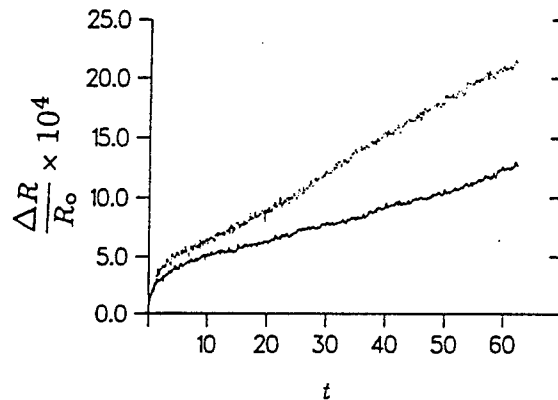


Figure 2. Two different behaviors of resistance changes during and after electromigration experiments on passivated, Al-1% Si/TiN/Ti submicron lines subjected to a current density of 2 MA cm^{-2} . Measurements taken at a true test temperature of 240°C on a common time scale. (From De Munari, et al. [7]).

It has been assumed [7] that relative resistance variations are proportional to relative volume variations. The linear region of Fig. 2 has been analyzed by hypothesizing that the relative resistance variations are proportional to the atomic drift velocity, $\Delta R/R \propto v_d = J_s/N_s$. Utilizing the expression for vacancy flux developed in (4), above, this proportionality can be extended to the non-linear region, assuming that $\Delta R/R \propto v_d = J_s/N_s$. By means of a percolation model, then, we have arrived at a general expression for vacancy flux which describes both the linear and nonlinear regions.

III. Conclusions

Traditional modeling of void growth in minimum-size VLSI conductors almost invariably assumes a constant coefficient of diffusivity. However, the active production of metal lattice vacancies in distinct clusters of high concentration, particularly at the early stages of void growth, leads to a lowering of the energy of formation of vacancies throughout these clusters. This in turn leads to distinctly accelerated diffusion which is very different from that characterized by the constant coefficient of diffusivity used for low level vacancy concentrations. As a consequence, the non-linear region of resistance measurements in minimum-size conductors has heretofore been inaccurately modeled. Expressions have been developed in this paper for variable, concentration

dependent flux and diffusivity using the mathematical techniques of percolation theory. These expressions should allow for far better understanding and more accurate modeling of the complex mechanisms of void growth.

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3-D Self-Consistent Simulation of Grid Gate Quantum Dot Devices

V.Y.A. Thean, S.H. Nagaraja, P. Matagne and J.P. Leburton

Beckman Institute for Advanced Science and Technology and Coordinated Science Laboratory, University of Illinois, Urbana, Illinois 61801

Advances in nanostructure technology have enabled the fabrication of semiconductor devices with submicrometer feature sizes. In order to gain insight into basic device operation and to achieve optimum device performance, computer simulation is an important tool that provides guidelines for design and device fabrication.

In this paper we present a self-consistent Schrödinger-Poisson simulation of a delta-doped AlGaAs-GaAs quantum dot grid gate device(Fig. 1). The potential profile of the device is obtained from the solution of the 3-D Poisson equation. Since the lateral potential variations(x and z-directions) are much more gradual than the vertical potential change(y-direction) across the AlGaAs-GaAs heterojunction, we have assumed that quantum confinement is realized only in the vertical direction. Hence, to obtain the electron density, only the 1-D Schrödinger equation in the vertical direction is solved adiabatically for the whole device. The exchange-correlation energy within the local density approximation, when more than one electron sits in the unit cell of the device, is also taken into account. The Poisson and Schrödinger equations are discretized by a nonuniform mesh finite-difference method. The potential and charge distributions were then computed self-consistently using the Newton-Raphson Successive Over-Relaxation (NRSOR) approach.

The simulation was performed for a unit cell of the device with a pocket of electrons formed in the quantum well under the electrostatic confinement potential arising from the gate. We have examined the variations of bound states in the quantum dot as a function of the 3-D potential distribution(Fig. 3). We have also investigated the change in the potential and electron density within the device for different gate bias and device temperatures(Fig. 2). Moreover, we have simulated single-electron charging effects when the condition for integer number of electrons in the device is imposed on the self-consistent computations(Fig. 4). The quantum dot capacitance was also derived for a wide range of temperatures. Furthermore, we have also simulated the influence of material interface disorder on the potential and fluctuations in the coulombic impurity charge distribution in the device.

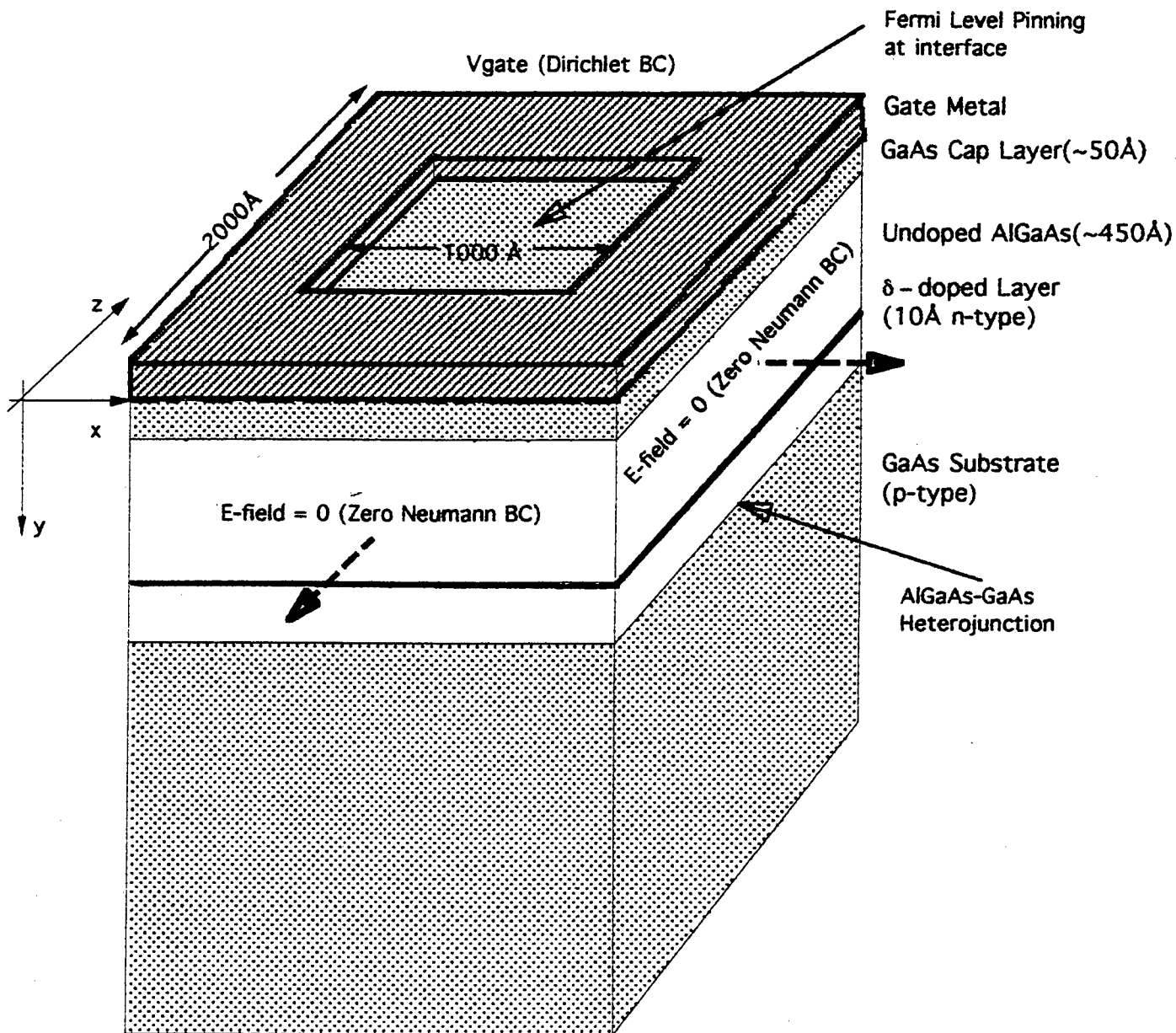


FIG. 1. Device model and boundary conditions imposed for the 3-D simulation.

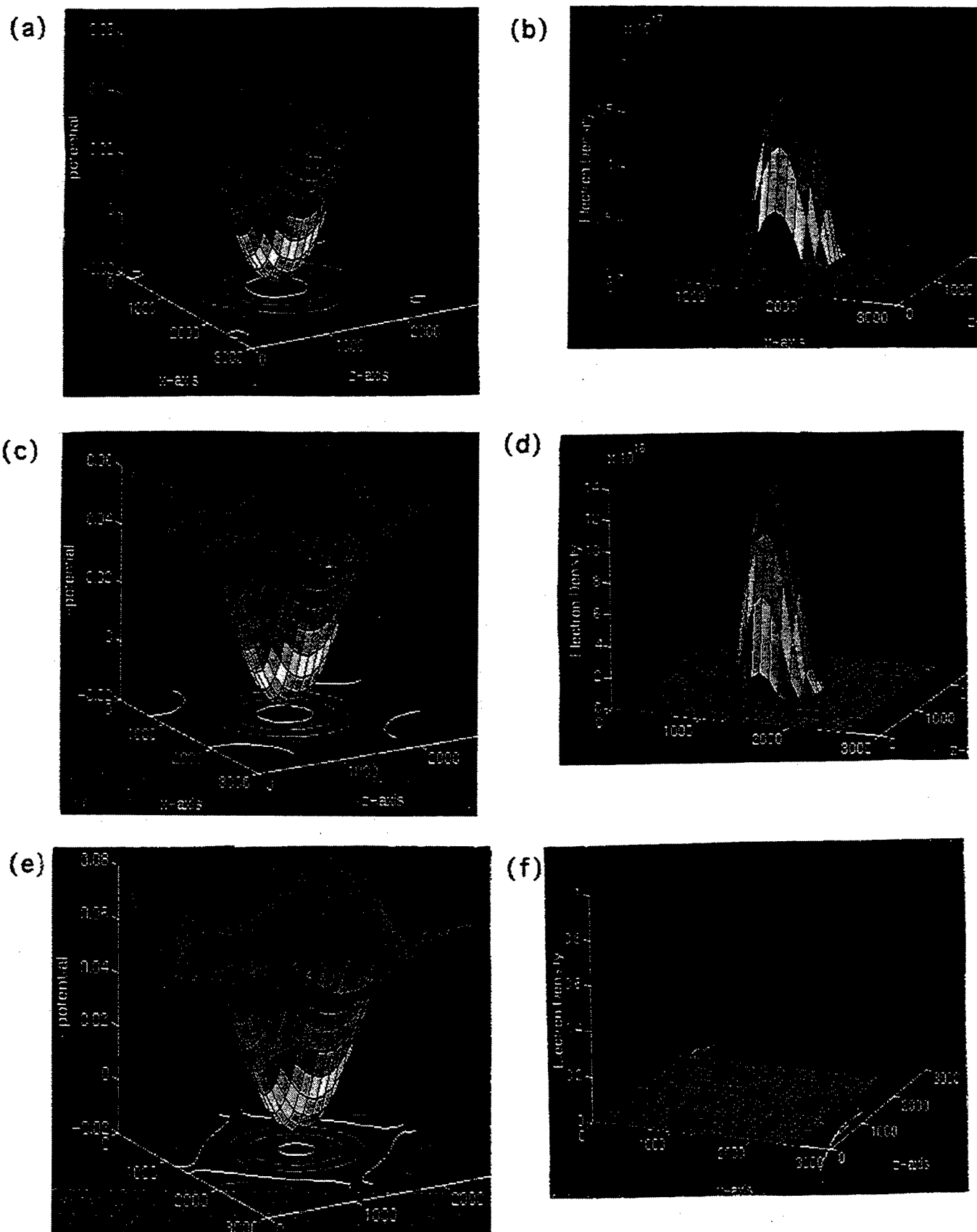


FIG. 2. (a) Conduction band surface (xz-plane) at the heterojunction for $V_{gate} = -320\text{mV}$ (b) Electron density (xz-plane), corresponding to 2 electrons, at the heterojunction for $V_{gate} = -320\text{mV}$. (c) Conduction band surface for $V_{gate} = -330\text{mV}$. (d) Electron density (1 electron) for $V_{gate} = -330\text{mV}$. (e) Conduction band surface for $V_{gate} = -345\text{mV}$. (f) Electron density (0 electron) for $V_{gate} = -345\text{mV}$. (Device temperature at $T = 4.2\text{K}$)

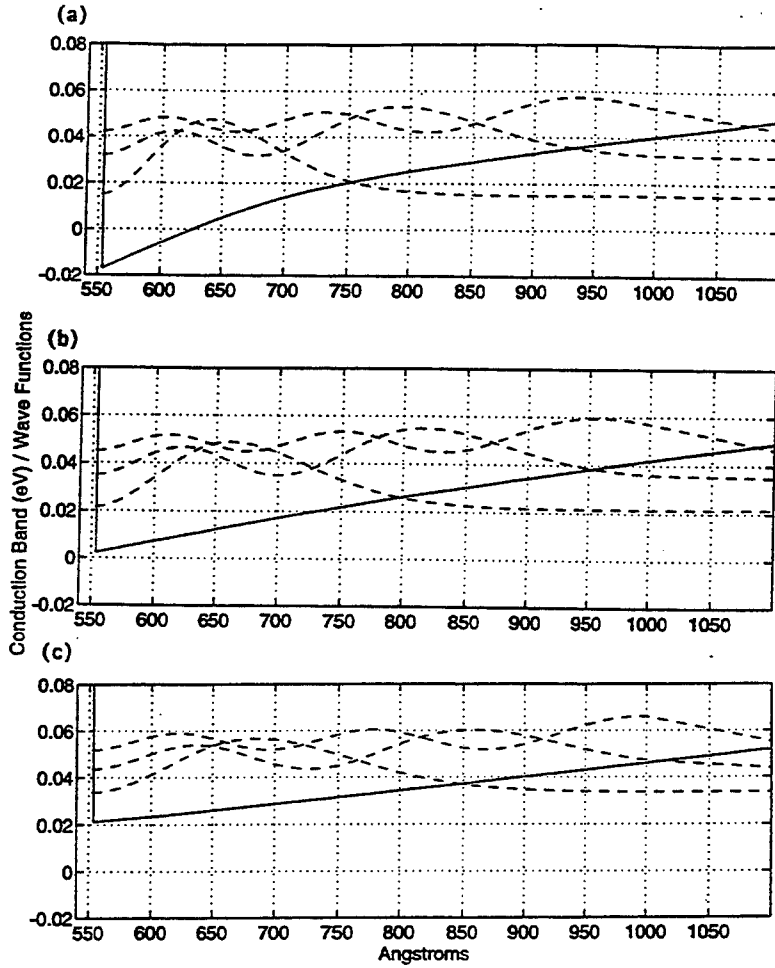


FIG. 3. (a) Conduction band profile (y-direction) of the quantum well and wavefunctions of the first three bound states at the center of the electron pocket. (b) Conduction band and wavefunctions away from the center. (c) Conduction band and wavefunctions under the gate.

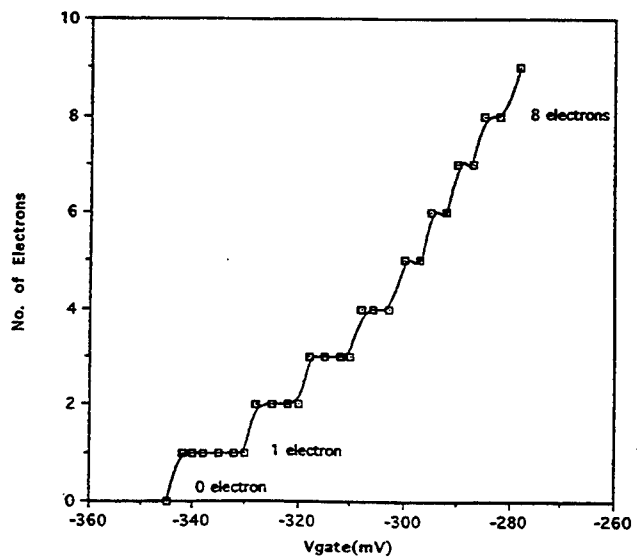


FIG. 4. A plot showing the change in the number of electrons in the device as the gate bias changes. (Device temperature at $T=4$ 2K)

MULTI-PHONON PROCESSES IN OPTICAL TRANSITIONS IN QUANTUM NANOSTRUCTURES

I.P.Ipatova, A.Yu.Maslov, O.V.Proshina.

A.F.Ioffe Physical Technical Institute, 194021, St.-Petersburg, Russia

In a spectrum of ionic crystals there are intense phonon replicas of electron transition lines in deep impurity centers. They occur due to lattice polarization by localized electron in materials with strong electron-phonon interaction [1].

Similar effects should be of great importance in optoelectronic devices based on quantum nanostructures due to the strong localization of carriers. However the free motion of electrons in a quantum well plane or along axis of quantum wire prevents to the appearance of static polarization.

In a present paper it is shown that additional confinement of carriers within quantum well and quantum wire which give rise to the polarization of surrounding medium may be realized in semiconductors with high ionicity. In these materials the polaron effect occurs due to electron - polar optical phonon interaction [2].

As this take place, the electron movement in well plane or along wire axis is limited by a polaron radius. The additional polaron localization lead to the static displacements of the atom equilibrium positions within a localization area. In calculating the electron optical transition probability the static displacements manifest themselves in appearance of phonon replicas of the lines of an electron transition between size quantisation levels. The intensity of these phonon replicas has the same order of magnitude as direct transition lines.

The electron state is initially localized in quantum dots therefore the multi-phonon effects similar to those in deep impurity centers may occur without regard for polaron polarization. Nevertheless a polarization within a quantum dot can enhance the multi-phonon processes.

1. Quantum well.

In ionic crystals the strong interaction with LO phonons results in electron autolocalization in the area of a radius a_0 . In other words, the Pekar polaron appears. We will consider the situation when a quantum well size L is less than a polaron radius a_0 ,

$$L < a_0. \quad (1)$$

This condition implies that the multi-phonon processes are allowed by energy conservation law for electron interlevel transition in quantum nanostructures.

The Schrödinger equation for an electron located in a quantum well is:

$$\begin{aligned} -\frac{\hbar^2}{2m} \Delta \Psi_n(\mathbf{r}) + V(z)\Psi_n(\mathbf{r}) + eU(\mathbf{r})\Psi_n(\mathbf{r}) \\ + \left(\frac{\varepsilon}{8\pi} \int d^3r (\nabla U(\mathbf{r}))^2 \right) \Psi(\mathbf{r}) = E\Psi_n(\mathbf{r}), \end{aligned} \quad (2)$$

where $V(z)$ is one-dimensional potential of a quantum well and $U(\mathbf{r})$ is the potential created by the polar optical phonons. The last term of the left side of equation (2) is the energy of polarized medium [2]. Here m is the effective mass of carrier and ε is

so-called optical dielectric constant, $1/\varepsilon = 1/\varepsilon_\infty - 1/\varepsilon_0$, by which the inertial part of a medium polarization is taken into account.

The condition (1) means that an electron movement across the well is fast and a polaron movement is slow, and therefore the adiabatic approximation can be used.

The adiabatic wave function of an electron has a form:

$$\Psi_n(\mathbf{r}) = \psi_n(z)\chi_n(\mathbf{r}_{\parallel}), \quad (3)$$

where $\psi_n(z)$ is the wave function of an electron in the quantum well, n is number of the size quantisation level and $\chi_n(\mathbf{r}_{\parallel})$ is the wave function of two-dimensional polaron movement, and \mathbf{r}_{\parallel} is a two-dimensional vector. The variation of the energy E from the equation (2) with respect to potential $U(\mathbf{r})$ results in the Poisson equation. The solution of this equation gives:

$$U(\mathbf{r}) = -\frac{e}{\varepsilon} \int \frac{d^3r_1 \chi_n^2(\mathbf{r}_{\parallel 1}) \psi_n^2(z_1)}{|\mathbf{r} - \mathbf{r}_1|} \quad (4)$$

The optimal potential energy $U(\mathbf{r})$ (4) corresponds to the deepest potential well for an electron being at the size quantisation level n .

Substituting (4) in the Schrödinger equation and averaging over the fast movement, one obtains:

$$\begin{aligned} -\frac{\hbar^2}{2m} \Delta_{\mathbf{r}_{\parallel}} \chi_n(\mathbf{r}_{\parallel}) - \frac{e^2}{2\varepsilon} \left[\int \frac{dz dz_1 d^2r_{\parallel 1}}{|\mathbf{r} - \mathbf{r}_1|} \psi_n^2(z) \psi_n^2(z_1) \chi_n^2(\mathbf{r}_{\parallel 1}) \right] \chi_n(\mathbf{r}_{\parallel}) = \\ = (E - E_n^{(0)}) \chi_n(\mathbf{r}_{\parallel}), \end{aligned} \quad (5)$$

Here $E_n^{(0)}$ is the energy level of size quantisation. The solution of this equation with an accuracy up to the first order on parameter (1) gives:

$$E_n = E_n^{(0)} + \alpha^2 \hbar \omega_0 (C_0 - C_1 \alpha_{nn} \frac{L}{a_0}), \quad (6)$$

where

$$\alpha = \frac{e^2}{2\hbar\omega_0} \left(\frac{2m\omega_0}{\hbar} \right)^{1/2} \left(\frac{1}{\varepsilon_\infty} - \frac{1}{\varepsilon_0} \right) \quad (7)$$

is the Fröhlich constant, ω_0 is the optical phonon frequency, $a_0 = \hbar^2 \varepsilon / m e^2$ is the polaron radius. The coefficient $C_0 = 0,4047$ has been found in the theory of two-dimensional polaron [3]. We have obtained that the numerical coefficient C_1 is equal to $C_1 = 0,0682$ by using the function $\chi(\mathbf{r})$ of two-dimensional polaron [3].

The equation (6) shows that the polaron energy dependence on the quantum well shape and the size quantisation level number is determined by the value of the coefficients α_{nn} only. These coefficients are determined by the wave functions of an electron in the quantum well in a following way:

$$\alpha_{nn} = \frac{1}{L} \int dz dz_1 \psi_n^2(z) \psi_n^2(z_1) |z - z_1|. \quad (8)$$

2. Quantum wire.

In the quantum wire an electron oscillates in two directions transversely to the axis of the wire (directions \mathbf{r}_\perp). These oscillations are fast corresponding to condition (1). A slow movement occurs along the wire direction (axis z).

Using the adiabatic approximation, the wave function may be written as: $\Psi_n(\mathbf{r}) = \psi_n(\mathbf{r}_\perp)\chi_n(z)$. Averaging over the fast two-dimensional movement, one obtains the equation in $\chi_n(z)$

$$-\frac{\hbar^2}{2m} \frac{d^2}{dz^2} \chi_n(z) - \frac{e^2}{2\epsilon} U_n(z) \chi_n(z) = (E - E_n^{(0)}) \chi_n(z), \quad (9)$$

where the optimal potential $U_n(z)$ is determined by variational procedure similar to that which was used in obtaining equation (5). It was obtained:

$$U_n(z) = \int \frac{d^2 r_\perp d^2 r_{\perp 1} dz_1 \psi_n^2(\mathbf{r}_\perp) \psi_n^2(\mathbf{r}_{\perp 1}) \chi_n(z_1)}{|\mathbf{r} - \mathbf{r}_1|}, \quad (10)$$

The solution of nonlinear one-dimensional equation (9) was found to have a form:

$$E_n = E_n^{(0)} - \frac{1}{4} \alpha^2 \hbar \omega_0 \ln^2 \left(\beta_{nn} \frac{a_0}{L} \right), \quad (11)$$

where

$$\ln \beta_{nn} = \int d^2 r_\perp d^2 r_{\perp 1} \psi_n^2(\mathbf{r}_\perp) \psi_n^2(\mathbf{r}_{\perp 1}) \ln \left[\frac{|\mathbf{r}_\perp - \mathbf{r}_{\perp 1}|}{L} \right] \quad (12)$$

The logarithmic dependence of energy (11) on parameter (1) accounts for the necessity of cutting off the one-dimensional Coulomb potential in both small and large distances.

The dependence of the energy on the size-quantisation level number and the cross section shape of a quantum wire is determined by the coefficients β_{nn} from the equation (12).

3. Quantum dot.

We suggest that in a quantum dot the condition (1) is satisfied for all directions. The medium polarization which exists within the dot due to electron-phonon interaction depends on the electronic state.

Correspondingly, the polaron energy within the quantum dot takes the form

$$E_n = E_n^{(0)} - \alpha^2 a_0 \hbar \omega_0 \int \frac{d^3 r d^3 r_1 \psi_n^2(\mathbf{r}) \psi_n^2(\mathbf{r}_1)}{|\mathbf{r} - \mathbf{r}_1|}, \quad (13)$$

where $\psi_n(\mathbf{r})$ is the wave function of an electron within the quantum dot. For the dot with characteristic size L this energy is:

$$E_n = E_n^{(0)} - \alpha^2 \hbar \omega_0 \frac{a_0}{L} \gamma_{nn}, \quad (14)$$

where the numerical coefficients γ_{nn} is determined by specific form of the wave functions $\psi_n(\mathbf{r})$.

4. Optical transitions.

The expressions (6), (11) and (13) show that the polarization state of a medium depends on the electron level number. It means that atoms vibrate about different equilibrium positions for various electronic states [1].

Lattice relaxation is a very slow process in comparison with optical transitions. Therefore instantaneous electronic transition in absorption of light takes place in a fixed value of the potential which is optimal for the lower level.

Correspondingly, the emission transition occurs when the optimal potential of upper level is fixed.

Therefore the frequency of a vertical absorption transition differ from that of an emission transition [4]. This difference of two energies (Stocs shift) is equal to:

$$\Delta E = \int d^3r U_n(\mathbf{r})[\psi_n(\mathbf{r}) - \psi_m(\mathbf{r})] + \int d^3r U_m(\mathbf{r})[\psi_m(\mathbf{r}) - \psi_n(\mathbf{r})], \quad (15)$$

In the structures being considered the Stocs shift is found to be:

$$\frac{\Delta E(QW)}{\hbar\omega_0} = C_1 \alpha^2 \left(\frac{L}{a_0} \right) \left(\alpha_{nn} + \alpha_{mm} - 2\alpha_{nm} \right); \quad (16)$$

$$\frac{\Delta E(QWW)}{\hbar\omega_0} = -0,5 \alpha^2 \left(\ln \beta_{nn} + \ln \beta_{mm} - 2 \ln \beta_{nm} \right) \ln \frac{a_0}{L}; \quad (17)$$

$$\frac{\Delta E(QD)}{\hbar\omega_0} = -\alpha^2 \left(\frac{a_0}{L} \right) \left(\gamma_{nn} + \gamma_{mm} - 2\gamma_{nm} \right); \quad (18)$$

From the expressions (16) - (18) one can see that a value of Stocs shift is determined by the Fröhlich constant α which is close to unity in *II - VI* semiconductors and by the factor depending on the type of nanostructures.

In a quantum well the Stocs shift is small in the *II - VI* semiconductors because it involves a small factor L/a_0 . In a quantum wire the Stocs shift is larger since it involves a factor $\ln(a_0/L) > 1$. In a quantum dot the Stocs shift has a maximum value due to large factor $a_0/L > 1$.

In optical spectra the intensive phonon replicas should appear when values of the dimensionless Stocs shift is close to unity [4].

In experimental paper [5] up to five phonon replicas was observed in a set of *CdSe* quantum dots in a glass matrix.

The constant α for this material is equal to 0.5 and the Stocs shift calculated in the spherical potential well with infinite walls takes the value $\Delta E/\hbar\omega_0 = 0.35 - 0.70$ for the quantum dots of sizes $L = 1.4 - 2.8$ nm.

According to eq. (18) the intensities of phonon replicas should increase with decreasing of dots size. The same behavior was observed experimentally [5].

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Nonlinear Electrothermomechanical Equations of Deformable Ferroelectric Semiconductors

N. Daher
LPNO-CNRS, France

Introduction :

Since the discovery of the ferroelectric properties of crystals of Rochelle Salt, ferroelectricity has been traditionally considered one of the divisions of the physics of dielectrics. In this context, wave propagation in rigid and deformable bodies has been the subject of many works [1] where the basic equations used are either postulated or based on intuitive guidance. More recently, two phenomenological theories of piezoelectric ferroelectric dielectrics has been performed in a consistent manner through deductive schemes starting from the basic principles of continuum physics. One of them [2] is based on the fruitful notion of internal coordinates and starts from a Lagrangian variational approach. The other [3] is based on the notion of polarization sublattices introduced by Néel in Ferrimagnets and uses the principle of virtual power (d'Alembert's principle) and the first and second principles of thermodynamics. A fundamentally new stage in the investigation of ferroelectrics is associated with the discovery of the ferroelectric properties of Barium Titanate. The latter is a ferroelectric semiconductor with a not too wide forbidden band so it appeared possible to use it to investigate electron conductivity, diffusivity and other transport phenomena. Sometime further the semiconductor properties of ferroelectrics with the perovskite structure began to be investigated. The class of ferroelectric semiconductors now includes a large number of compounds so that the study of ferroelectric semiconductors has evolved into an independent research direction. From a phenomenological point of view, consistent theories have been recently devoted to the study of elastic piezosemiconductors [4, 5, 6]. However, none of them accounts for electromagnetic ordering and polarization inertia or inertia associated with internal coordinates, which are characteristic features of the ferroelectric behavior [1, 2].

In the present paper we shall construct a nonlinear rotationally invariant and thermodynamically admissible theory of deformable ferroelectric semiconductors. On the one hand, since semiconduction is, by essence, a dissipative irreversible process, the use of the Lagrangian variational approach is discarded, the latter being restricted to thermodynamically reversible phenomena. On the other hand, since the vectorial approach (conservation of momentum, moment of momentum etc) does not provide a guiding principle in the construction of the different interacting continua, we use the energy approach known as d'Alembert principle in so far as the mechanical and electromechanical fields are concerned. The latter uses weaker assumptions than those on which the Lagrangian formulation is based so that nonintegrable systems needed for the study of irreversible processes are included. This extended mechanical and electromechanical energy formulation accommodates invariance principles and uses the concept of duality [3-6]. The principle of objectivity (invariance under a rigid body motion also called rotational invariance) is essential to the derivation of the interacting fields for which constitutive relations are needed. Recently, this approach was extended by the author in view of obtaining a unified mode of expression including pure electromagnetism (invariance under gauge transformation) and interfacial properties (invariance under a scale-change transformation) [7].

In section 1, the notations are specified and the distinction between the reference (material) and actual (spatial) configurations, essential to account for nonlinearity, is exposed. Section 2 is devoted to mass and charge conservation equations where the different charge carriers that will play a major role when introduced in the second principle of thermodynamics to account for diffusion processes, are given in both configurations and in terms of concentration of carriers. The electromechanical, ferroelectric and thermodynamical equations including heat and electronic conduction and diffusion processes are derived in section 3. Comments and comparisons with previous works are performed.

1. Notation and distinction between material and spatial descriptions

We use the classical notation of nonlinear continuum physics [2], either in rectangular tensor components or in intrinsic notation. An absolute Newtonian chronology is used. The

general nonlinear deformation of a body, between its reference configuration K_R at time $t=t_0$ and its current configuration K_t at time t is described, at fixed t , by the transformation

$$x_i = X_i \left(X_{K,t} \right) \quad (1)$$

which carries the position of a material particle at t_0 , X_K , $K=1, 2, 3$ from the undeformed region into the position x_i , $i=1, 2, 3$ at t in the deformed region. Equation (1) is assumed to be continuous and differentiable as many times as needed. The material body occupies the open set D_t of physical Euclidean space E^3 at t . The velocity v , the motion gradient F and its inverse F^{-1} are classically defined by

$$v = \frac{\partial X}{\partial t} \Big|_{X \text{ fixed}} = \{v_i\} \quad (2)$$

$$F = \left\{ x_{i,K} = \frac{\partial x_i}{\partial X_K} \right\} \quad F^{-1} = \left\{ X_{K,i} = \frac{\partial X_K}{\partial x_i} \right\} \quad (3)$$

with

$$x_{i,K} X_{K,j} = \delta_{ij} \quad , \quad X_{K,i} x_{i,L} = \delta_{KL} \quad (4)$$

where δ_{ij} and δ_{KL} are Kronecker symbols. The Einstein summation convention on dummy indices is understood. For all times, the Jacobian determinant satisfies

$$J = \det |x_{i,K}| = \frac{1}{3!} \varepsilon_{ijk} \varepsilon_{KLM} x_{i,K} x_{j,L} x_{k,M} \quad (5)$$

where ε_{ijk} and ε_{KLM} are permutation symbols in x and X systems. The change in a function, referred to the reference configuration (material description), with time as seen by an observer riding with the moving mass point X is called a material time derivative and is denoted by

$$\dot{F}(X,t) \equiv \frac{d}{dt} F(X,t) = \frac{\partial F}{\partial t}(X,t) \quad (6)$$

its counterpart in the current configuration (spatial description) reads

$$\dot{F}(x,t) \equiv \frac{d}{dt} F(x,t) = \frac{\partial F}{\partial t} + \frac{\partial F}{\partial x_i} \frac{dx_i}{dt} \quad (7)$$

2. Mass and charge conservation equations

Let ρ_0 and ρ denote the matter density in K_R and K_t , respectively. Then the continuity or mass conservation equation takes either one of the following two forms :

$$\rho_0 = \rho J \quad , \quad \dot{\rho} + \rho \nabla \cdot v = 0 \quad (8)$$

Semi-conductors include various species of carriers (electrons, holes, impurities, etc) and present generation and recombination phenomena. In order to describe these effects, we shall decompose the total charge density and the total current as follows :

$$q_f = \sum_a q_f^a \quad J = \sum_a J^a \quad J^a = q_f^a v^a \quad (9)$$

where each upperscript a denotes one of the various species of carriers. Similarly to the mass conservation ($d/dt \int_D \rho dv=0$) that leads to equation (8)₂ but accounting for possible recombination and generation processes, one may postulate the following equation for charge carriers :

$$\frac{d^a}{dt} \int_D q_f^a dv = \int_D \rho \gamma^a dv \quad , \quad \sum_a \gamma^a = 0 \quad (10)$$

with

$$q_f^a = \rho c_\lambda^a \quad \frac{d^a}{dt} = \frac{\partial}{\partial t} + v^a \cdot \nabla \quad (11)$$

where γ^a and c_λ^a are source terms and the concentration defined per unit mass. The local expressions referred to K_t and K_R take on the following forms :

$$\rho \dot{c}_\lambda^a + \nabla \cdot \mathcal{J}^a = \rho \gamma^a \quad , \quad \rho_o C_\lambda^a + \nabla_R \cdot \mathcal{J}^a = \rho_o \gamma^a \quad (12)$$

where ∇ and ∇_R denote gradients with respect to K_t and K_R and where we have set

$$c_\lambda^a(x, t) = C_\lambda^a(X, t) \quad (13)$$

and

$$\mathcal{J}_K^a(X, t) = JX_{K,i} \mathcal{J}_i^a(x, t), \quad \mathcal{J}_i^a = J_i^a - q_f^a v_i \quad (14)$$

The latter current \mathcal{J}_i^a is an objective or observer independent field since only a relative velocity is included in its expression. This is precisely the current to which one ultimately needs to construct a constitutive relation through thermodynamical arguments.

3. Thermoelectromechanical equations

The thermoelectromechanical balance laws of an electromagnetic continuum may be deduced in an elegant manner from three general principles written in global form for the material volume D_t . These are the principle of virtual power and the first and second principles of thermodynamics. This procedure has proven to be efficient in the construction of involved models of electromagnetic continua such as simple dielectrics, conductors and semiconductors [4, 5, 6] or ferroelectric and ferromagnetic dielectrics [3] etc. Following this now well established method that we do not reproduce here for lack of space, we deduce the coupled electromechanical balance laws and the thermodynamical equations which complement Maxwell equations (not explicitated here) and apply to deformable ferroelectric semiconductors as follows :

a) Generalized mechanical continuum equations

$$\ddot{x}_i = \frac{1}{\rho} \left[t_{ij,j} + f_i + f_i^{em} \right] = \frac{1}{\rho_o} \left[T_{iK,K} + J(f_i + f_i^{em}) \right] \quad (15)$$

b) Ferroelectric continuum equations

$$d\bar{\pi}_i = \mathcal{E}_i + {}^L E_i + \frac{1}{\rho} {}^L E_{ij,j} = \mathcal{E}_i + {}^L E_i + \frac{1}{\rho_o} {}^L E_{iK,K} \quad (16)$$

c) Clausius-Duhem inequality in K_t and K_R

$$\begin{aligned} & -\rho \left(\dot{\psi} + \eta \dot{\theta} - \sum_a \mu^a \dot{c}_\lambda^a \right) + p_{(i)} - \phi \cdot \nabla \theta \\ & + \sum_a \left(\mathcal{J}^a \cdot \mathcal{E}^{a\text{eff}} - \rho \mu^a \gamma^a \right) \geq 0 \end{aligned} \quad (17)$$

with

$$\mathcal{E}^{a\text{eff}} = \mathcal{E} - \nabla \mu^a \quad (18)$$

and

$$\begin{aligned} & -\rho_o \left(\dot{\psi} + \eta \dot{\theta} - \sum_a \mu^a \dot{C}_\lambda^a \right) + {}^E T_{KL} \dot{E}_{KL} - {}^L E_K \dot{\Pi}_K \\ & + {}^L E_{KL} \dot{\Pi}_{KL} + \sum_a \left(\mathcal{J}^a \cdot \mathcal{E}^{a\text{eff}} - \rho_o \mu^a \gamma^a \right) - \phi \cdot G \geq 0 \end{aligned} \quad (19)$$

The elaboration of a set of thermodynamically admissible constitutive equations is entirely based on the exploitation of this last inequality. The nonsymmetric Cauchy stress tensor t_{ij} which couples the two continua is defined by

$$t_{ij} = \sigma_{ij} + t_{[ij]}^{int} \quad (20)$$

where the σ_{ij} is the symmetric tensor of elasticity and $t_{[ij]}^{int}$ is the skew symmetric part of the "interaction" stress tensor given by

$$t_{ij}^{int} = \rho \, {}^L E_i \pi_j - {}^L E_{ip} \pi_{j,p} \quad , \quad \pi_i = P_i / \rho \quad (21)$$

The parameters π_i , d , f_i and f_i^{em} account for polarization per unit mass, polarization inertia, mechanical body forces and the electromagnetic one that generalizes the well-know Lorentz force. As to the parameters ψ , η , θ and Φ , they denote respectively the free energy density, the entropy, the temperature, and the heat flux. The scalar $p_{(i)}$ in equ. (17) indicates the power of internal generalized electromechanical forces. Although its expression is not given in K_t , it appears in K_R through the expression (19). Finally, let us give the relations that link the fields defined in K_R and K_t , where the distinction is essential in a nonlinear continuum framework while it vanishes in a linear frame.

$$E_{KL} = \frac{1}{2} \left(x_{i,K} x_{i,L} - \delta_{KL} \right) = E_{LK} \quad \Pi_K = J X_{K,i} P_i \quad (22)$$

$$\Pi_{KL} = X_{K,i} \pi_{i,j} x_{j,L} \quad G_K = \theta_{,i} x_{i,K} = \theta_{,K} \quad (23)$$

and also the fields

$$E_{TKL} = J X_{K,i} E_{t_{ij}} X_{L,j} = E_{T_{iK}} X_{L,i} \quad {}^L E_K = {}^L E_i x_{i,K} \quad (24)$$

$${}^L E_{KL} = J x_{i,K} {}^L E_{ij} X_{L,j} = {}^L E_{iK} R_{i,L} \quad \phi_K = J X_{K,i} \phi_i \quad (25)$$

$$\mathcal{E}_K^{aeff} = \mathcal{E}_i^{aeff} x_{i,K} \quad (26)$$

The field \mathcal{E}^{aeff} given through eq. (18) is an effective electromotive intensity. It includes, in addition to the Maxwellian (by opposition to the local field ${}^L E_i$ due to the interaction between the deformable and ferroelectric continua) electric field \mathcal{E}_i defined in K_t , the spatial non uniformities in the chemical potential of a species μ^α . This feature characterizes the state of semiconduction as opposed to simply conductive or dielectric media where diffusion processes are not taken into account. The fact that the concentration of carriers c^α_λ appears only in the Clausius-Duhem inequality and it satisfies, simultaneously, an equation eq. (12) - which may be considered as a particular form of a time evolution equation, shows that c^α_λ may be called "internal" or "hidden" variable insofar as the mechanical description of the medium is concerned. Indeed, by its very nature, such a notion is introduced to account for an internal structure hidden to external observers, so that it does not modify, neither the conservation laws of continuum physics, nor the general form of the principles of thermodynamics.

Comments and comparison with previous works

Equation (15) is a generalization of the usual Euler-Cauchy equation of motion. Equation (16) is the bulk relation governing the polarization density in a ferroelectric material. The

parameter ${}^L E_{ij}$ accounts for spatial nonuniformities in the polarization field, and therefore for the local orientational deviation from the ordering prevalent in ferroelectrics which are in an ordered phase below the curie ferroelectric phase-transition temperature θ_c . The above obtained local thermoelectromechanical equations reduce to those of simpler theories when some effects are not taken into account. Thus (i) in the case of a dielectric medium ($\mathcal{F}^a = 0$, $q_f^a = p c^a_\lambda = 0$) the present equations reduce to those obtained in Ref. [3], dealing with ferroelectric dielectrics ; (ii) in the case of a nonlinear elastic semiconductor where both polarization inertia and gradients are neglected, the above mentioned equations are comparable to Ref. [4, 5] (iii) in the absence of electromagnetic ordering and chemical potentials, the theory describes then simple electromagnetic media given by the theory of nonlinear elastic dielectrics derived by Toupin in the early sixties. Finally, let us note that if one neglects deformation but keeps polarization and electronic diffusion properties, then the present approach coincides with the one given in Ref. [1] concerning rigid ferroelectric semiconductors.

Conclusion

To sum up, let us recall that the basic laws that govern deformable ferroelectric semiconductors have been derived in a coupled nonlinear framework. In order to obtain the differential equations needed for the study of practical and experimental aspects such as wave propagation problems (wave modes of acoustical or optical types known as polaritons, couplings between polaritons and acoustic modes, induction waves as well as electrical instability, etc.) one needs to add Maxwell equations and develop nonlinear constitutive relations. Both features, that we do not reproduce here, follow a now well established procedure. Here, the attention has been focussed on the elements that cannot be easily derived by the classical methods such as the vectorial newtonian or saclar lagrangian approaches. More details on the subject matter may be found in Ref. [1] for rigid ferroelectric semiconductors, in Ref. [3] for deformable ferroelectric dielectrics and in Ref. [4, 5, 6] for deformable semiconductors in the absence of ferroelectric properties.

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Ultra Electronics : Overview of ARPA's Nanoelectronics Program

Gernot S. Pomrenke
ARPA/ETO, Arlington, VA

The goals of the Ultra Dense, Ultra Fast Computing Components or Nanoelectronics Program are to explore and develop material, processing technologies, quantum and conventional devices and device architectures for a next generation of information processing systems. The Ultra program seeks improved speed, density, and functionality beyond that achieved by scaling transistors. These improvements should manifest themselves in systems operating 10 to 100 times faster than current systems, and denser by a factor of five to 100.

Phase I of the Ultra Electronics program explores, assesses, and benchmarks alternative electronic approaches to embedded and stand alone computing architectures. The program has demonstrated methods for applying novel quantum well electronic devices to improve densities of integrated electronic devices, developed methods of improving the control of epitaxial deposition to realize these devices. Other achievements include developing nanoprobe to study nanometer material structures and devices with picosecond time resolution.

Phase II of the program develops further the most promising approaches that were identified in Phase I. Efforts in nanoelectronics includes the design, fabrication, and testing of electronic devices with critical feature sizes below 0.1 microns. Combining conventional transistors with nanoelectronic devices will greatly reduce the complexity and size of sophisticated DoD circuits. This approach, when applied to silicon-based nanoelectronics, will allow nanoelectronics to leverage all the continuing improvements of conventional electronic devices, while providing the density improvements of nanoelectronics.

Main thrusts include developing silicon based nanoelectronics, chemical self-assembly techniques for nanoelectronics and improved semiconductor processing, and molecular beam epitaxy (MBE) in situ process control and other fabrication techniques for nanoelectronics. Silicon-germanium-carbon (SiGeC) -based devices are being developed to enable scaled silicon nanoelectronic. Another program focus is to develop high speed supercomputer visualization. This effort involves innovative approaches to software and hardware for coupling experimental data or methods of nanostructure analysis to graphic representations of physical or electronic properties. The program focuses also on nanolithography that targets patterning with critical dimensions below 50 nanometers.

Device and Circuit Applications
of Tunneling Phenomena

G. I. Haddad
Center for High-Frequency Microelectronics
Electrical Engineering and Computer Science Department
University of Michigan
Ann Arbor, Michigan

As device dimensions approach the submicron regime quantum tunneling mechanisms become extremely important. In some instances they limit conventional device performance. However, in many other instances they can be utilized to enhance the frequency/speed performance, decrease power requirements and result in novel devices. The basic properties of tunneling mechanisms and potential applications in devices and circuits will be discussed and recent results will be presented.

High-frequency ($f \sim 1$ THz) Studies of Quantum-effect Devices

Qing Hu⁽¹⁾, S. Verghese⁽¹⁾, R. A. Wyss⁽¹⁾, Th. Schäpers^(1,5), J. del Alamo⁽¹⁾, S. Feng⁽²⁾,
K. Yakubo⁽²⁾, M. J. Rooks⁽³⁾, M. R. Melloch⁽⁴⁾, and A. Förster⁽⁵⁾

*(1)Department of Electrical Engineering and Computer Science
and Research Laboratory of Electronics,
Massachusetts Institute of Technology, Cambridge, MA 02139*

(2)Department of Physics, University of California, Los Angeles, California 90024

(3)National Nanofabrication Facility, Cornell University, Ithaca, NY 14853-5403

(4)Purdue University, West Lafayette, Indiana 47907-1285

(5)Institut für Schicht- und Ionentechnik (ISI), Forschungszentrum Jülich

We have performed extensive studies on antenna-coupled semiconductor quantum-effect devices under irradiation at far-infrared (or THz) frequencies. The motivation of this investigation is two fold. First, studying the response of quantum-effect devices (or artificial atoms) to radiation at frequencies comparable to the intersubband spacings (the subbands are formed by lateral confinements) is analogous to optical spectroscopy in atomic physics. Therefore, new information can be revealed that dc transport measurement alone may not. Second, the intrinsically lower capacitance (and therefore the time constant RC) of laterally confined quantum-effect devices should make them competitive candidates for applications at and above one THz, where currently no photonic devices are available.

We first investigated the simplest quantum-effect device, quantum point contact (QPC).^{1,2} The electron transport from the source to drain can be modeled by an one-dimensional quantum mechanical system with a barrier at the narrowest constriction. Under a far-infrared irradiation whose photon energy is sufficient to raise the electron energy over the barrier, a radiation-induced drain/source current could be produced. This process is called photon-assisted quantum transport (PAQT),³ and it is directly analogous to the photoemission phenomenon in metals. Following the spirit of Tien-Gordon's theory of photon-assisted tunneling, we have developed a theory to quantify the PAQT process.⁴ In essence, photon absorption (or emission) can be characterized by a new electron density of states, which is a superposition of the original density of states with the energy shifted by $n\hbar\omega$ and weighted by a probability factor $J_n^2(\alpha)$, where α is a dimensionless number that is proportional to the radiation field strength. Consequently, the curve of the drain/source conductance G_{DS} vs. the gate voltage V_{GS} will be a superposition of the original G_{DS} - V_{GS} weighted by $J_n^2(\alpha)$ and shifted by $n\hbar\omega/e\eta$, where η is a dimensionless geometric factor that relates the gate voltage to the energy of the subbands. Thus, photon-induced substeps should appear on top of well-quantized conductance steps if the photon energy is much greater than thermal broadening kT .

Motivated by this idea, we have investigated response of antenna-coupled QPCs to coherent radiation in the frequency range from 100 GHz to 2.5 THz.⁵ The purpose of the integrated planar antennas is to couple far-infrared radiation (with wavelengths on the order of one millimeter) to individual QPCs of submicron dimensions. Figure 1 (a) and (b) show SEM pictures of a QPC coupled to a log-periodic antenna. Dc transport measurement on this device yielded fifteen visible conductance steps at 1.6 K, as shown by the staircase curve in Fig. 1(c). These sharply defined step structures indicate that the drain/source transport is mostly ballistic. Under coherent irradiation at 285 GHz, a pronounced photon-

induced current was observed which is shown as the oscillatory curve in Fig. 1(c). The radiation-induced current is positive below the threshold of a conductance step, and negative above the threshold. This feature qualitatively agrees with the theoretical prediction of PAQT. However, no photon-induced substeps were observed. At 285 GHz, $\hbar\omega = 1.2$ meV, which is approximately 1/3-1/2 of the spacing between adjacent subbands. Thus, photon-induced substeps, if exist, should be quite visible.

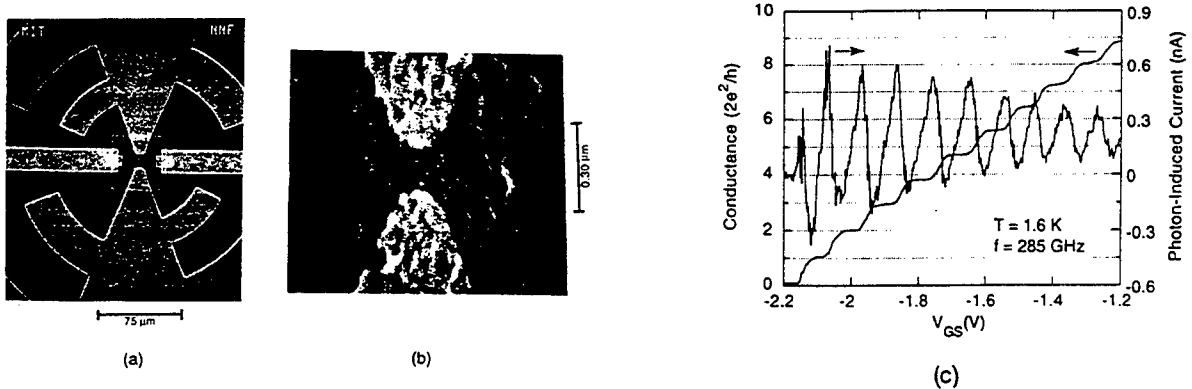


Figure 1. (a) SEM (with a magnification of 400) of a QPC with a log-periodic antenna. (b) Central region of the QPC. (c) Radiation-induced current in a gate voltage region where the conductance steps (measured without radiation) are well defined.

The most likely cause of the observed radiation-induced current is heating of the electron gas by the far-infrared radiation. Due to the gapless nature of excitations in two-dimensional electron gas (2DEG), radiation heating will always be present. This is in great contrast to superconducting tunnel junctions, in which the energy gap prevents energy absorption everywhere except across the junctions. Our further investigation of thermal current (which is the difference of drain/source currents measured at 3.7 K and 1.6 K) yielded very similar features as those of the radiation-induced currents.⁵ The assumption of the heating effect is further supported by our recently observed radiation-induced photovoltaic effect in the QPC devices.⁶ Figure 2 shows a set of drain/source current of an irradiated QPC with zero external bias voltage. This radiation-induced current tracks the subband structures in a regular manner that it resembles the transconductance dI_{DS}/dV_{GS} of the device. We have identified this photovoltaic effect as a result of thermopower generated by asymmetric heating of the drain and source. By shifting the focal spot of the far-infrared beam, we can reverse the asymmetry of this radiation heating, and thus reverse the polarity of the radiation-induced current, as shown in Figure 2.

Although our investigation on QPCs has yielded interesting bolometric response which may lead to device applications, a fundamental question remains why the photon-assisted quantum transport (which is analogous to so many well-established phenomena, such as photoemission in metals) has not been observed in QPC devices. In order to understand the conditions necessary for photon-excited processes to be achieved, we have carried out a simulation study by numerically solving time-dependent Schrödinger equation.⁷ Our main finding is that the selection rule, which is the mathematical statement of the momentum conservation of the electron/photon systems, determines whether the electron transport (under irradiation) is adiabatic or photon-excited. Mathematically, in order to achieve an appreciable photon-excited transition probability, the dipole-moment integration must be truncated to a region that is not much greater than the coherence

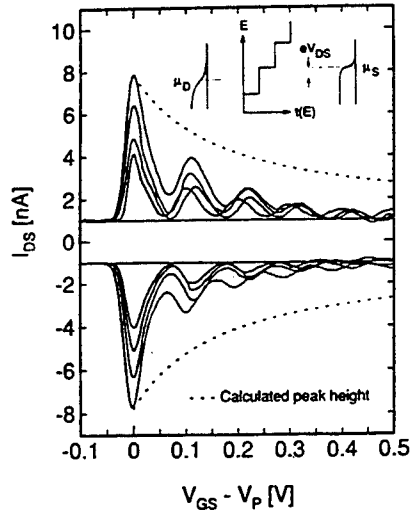


Figure 2. Far-infrared radiation-induced currents with zero externally applied drain/source bias voltage taken at different power levels. Positive currents correspond to beaming towards the source region while negative currents correspond to beaming towards the drain region.

length $1/\Delta k$, where Δk is equal to the momentum difference between the electrons before and after photon absorption/emission. This truncation can be achieved experimentally by either a localized electron state or a localized photon-field profile. Physically, this spatial localization of the electron or photon field provides the momentum spread that is necessary for the momentum conservation in the photon excitation process. Figure 3(a) shows a wave function (in k -space) in the presence of an ac field. The main peak at $k = 0$ corresponds to the wave function in a free space without radiation. The satellite peaks on the right correspond to photon absorptions, and the ones on the left correspond to photon emissions. Fig. 3(b) shows the amplitudes of these peaks as functions of the ac-field spatial width. Clearly, photon-excitation process decreases exponentially as the ac-field spatial confinement loosens.

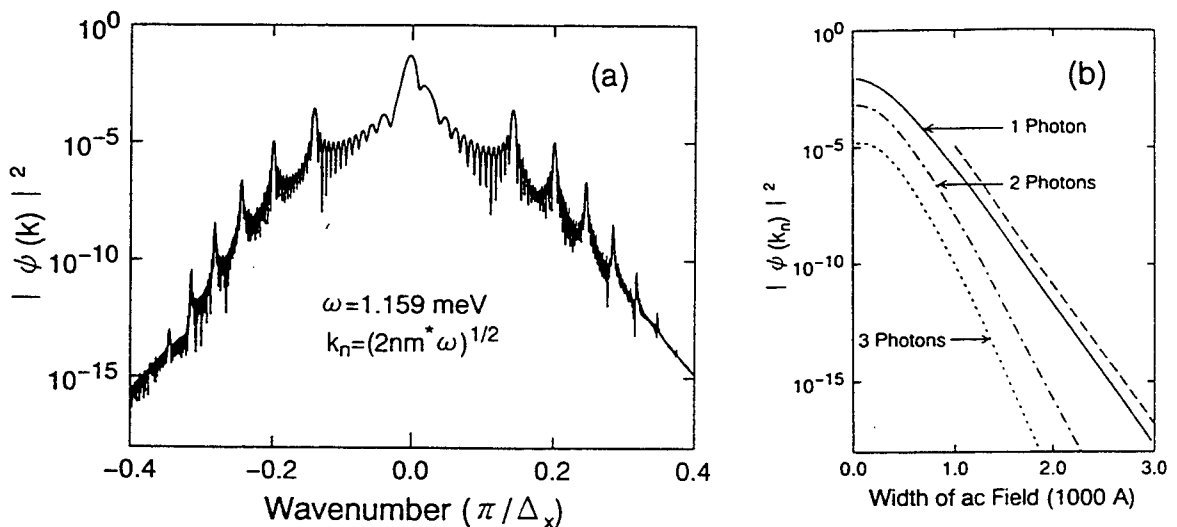


Figure 3. (a) Square of a wave function of free electrons (in k -space) under the irradiation of an ac field. The satellite peaks correspond to photon absorption (on the right of the main peak) and emission (on the left). (b) Amplitudes of photon-excited states as functions of the width of the ac field.

Our simulation study indicates that the selection rule requires a spatially confined ac field if the photon-excited transition is between two extended electronic states, such as the case for quantum-point-contact devices. This can be achieved by bringing the antenna terminals very close to the central region. Photon excitation can also be achieved by using double- or multiple-barrier structures to create quasibound electronic states. The spatially localized nature of these quasibound states provide the momentum transfer for the photon-assisted process. Following this understanding, we have designed and fabricated antenna-coupled dual-gate devices.⁸ An SEM picture of one of these devices is shown in Fig. 4, along with a side view of the device, a self-consistently calculated dc potential profile in the drain/source direction, and the transmission coefficient $T(\epsilon)$ through such a structure. The peaks in the transmission coefficient correspond to the energy levels of the quasibound states, while the peak width correspond to their lifetimes. In the presence of an ac field, photon-assisted transport can be modeled by an effective transmission coefficient $T_{\omega}(\epsilon)$, whose main peaks correspond to the original $T(\epsilon)$ and the sidebands correspond to photon absorption or emission, as shown in Fig. 5(a). Photon-induced current can be calculated in this model by taking the difference between the current calculated using $T_{\omega}(\epsilon)$ and $T(\epsilon)$.

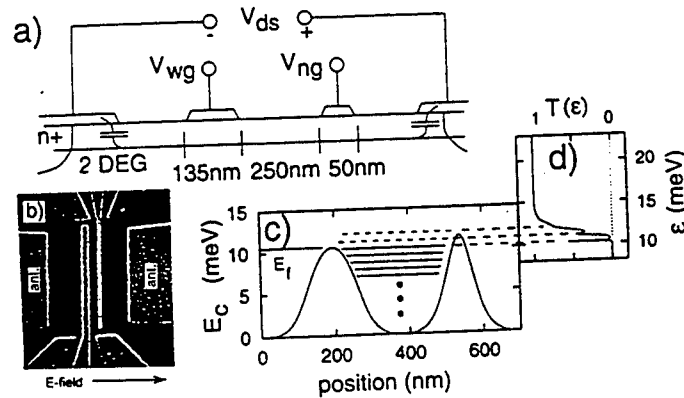


Figure 4. (a) Side view of a dual-gate device. (b) SEM picture of the device. (c) Self-consistently calculated dc potential profile for the device. (d) Transmission coefficient as a function of the energy.

Fig. 5(b) and (c) show the measured radiation-induced current as functions of the drain/source bias voltage V_{ds} (curves labeled by (i)). The two sets of curves are taken with radiation frequencies at 90 GHz (in (b)) and 270 GHz (in (c)). The radiation power level at both frequencies is approximately the same. It is clear that the two sets of curves exhibit distinctively different features at the two radiation frequencies. The ones at 90 GHz show much sharper modulations of the radiation-induced current, while the ones at 270 GHz have much smoother features, which is due to the overlap of photon subbands at this high frequency, as illustrated in Fig. 5(a). This frequency-dependent feature is the strongest evidence that the radiation-induced current is a photonic effect that depends on the energy of an individual photon. The curves labeled (ii) in Fig. 5(b) and (c) are calculated photocurrent based on the model of photon-assisted transport. They agree with the experimental results quite well. In comparison, the calculated radiation-induced current based on a bolometric model (labeled (iv)) is frequency independent and cannot explain the experimental results taken at 270 GHz.

In conclusion, our work indicates that heating will always accompany any possible photonic effects in semiconductor quantum-effect devices. In order to enhance the coherent

photon-excited process relative to the incoherent heating process, careful design must be taken to assure that the selection rule to be satisfied. Our measurement on dual-gate devices

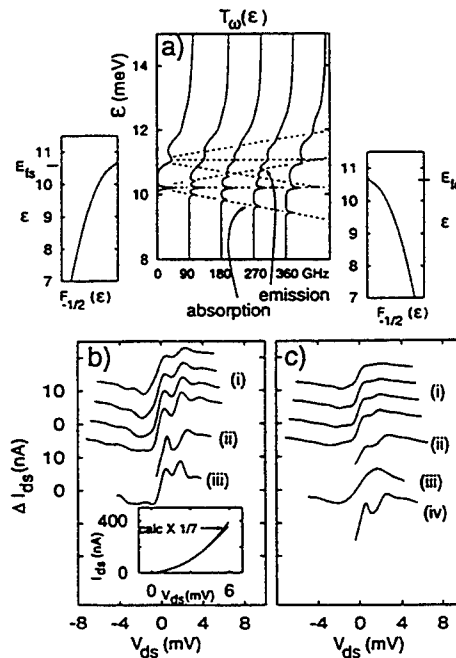


Figure 5. (a) Effective transmission coefficient that includes the effect of photon absorptions and emissions. (b) and (c) Curves (i): measured radiation-induced current at 90 GHz (b) and 270 GHz (c). Curves (ii): calculated radiation-induced current based on the model of photon-assisted transport. Curve (iv): calculated radiation-induced current based on heating model.

has yielded strong evidence of photonic effect that depends on the energy of individual photons. Further investigations by using broadband spectroscopies and tighter photon-field confinements should provide further evidence to test the theory. This work was supported in part by the MRSEC program of the National Science Foundation under award number DMR-9400334, and by MIT Lincoln Laboratory under grant number BX-5464.

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LOW FREQUENCY NOISE IN TWO-DIMENSIONAL METAL-SEMICONDUCTOR FIELD EFFECT TRANSISTOR

M.E.LEVINSHTEIN^{*}, H.PARK^{**}, W.C.B.PEATMAN^{**},
S.L.RUMYANTSEV^{*}, G.S.SIMIN^{*} and M.S.SHUR^{**}

^{*}A.F.Ioffe Institute of Russian Academy of Science, 194021, St.Petersburg, Russia

^{**}Department of Electrical Engineering, University of Virginia, Charlottesville, VA 22903, USA

Abstract

Low frequency noise in a novel 2-Dimensional Metal-Semiconductor Field Effect Transistor (2D-MESFET) has been investigated for the first time. It has been shown that the noise level S is rather small. At room temperature the value of Hooge constant α was about $2 \cdot 10^{-5}$ for frequency $f = 20$ Hz. The frequency dependence of the relative spectral density of current fluctuations S_I/I^2 at 300K was close to $S \sim 1/f^{0.6}$ in the frequency range 20 Hz - 20 kHz. Two local maxima have been observed on the temperature dependence of S in the temperature ranges 100 - 180 K and 200 - 300 K.

I. Introduction

Recently a novel 2-Dimensional Metal-Semiconductor Field Effect Transistor (2-D MESFET) on the base of modulation-doped AlGaAs/InGaAs heterostructure has been described [1]. It has been shown that the narrow channel effect, which is a serious limitation to the minimum power consumption in conventional FETs, is practically eliminated in this device. Therefore this device may become a promising base element of low power high frequency electronics. The level of low frequency noise is one of the important parameters for microwave devices. This frequently determines the usefulness of such devices in communication systems. The investigation of the low frequency noise also allows one to judge the degree of structural perfection of a material, quality of ohmic contacts, density of surface states etc. [2]

II. Results and Discussion

AlGaAs/InGaAs 2D-MESFETs studied here were similar to those described in [1]. For samples under investigation saturation current value I_{S0} was about 150 - 160 μ A at $V_{gs}=0$, and the threshold voltage V_T was - 0.8 V. The value of n_s in the InGaAs channel was $2 \cdot 10^{12}$ cm^{-2} and the Hall electron mobility was 6000 $\text{cm}^2/\text{V}\cdot\text{s}$ at 300 K. The gate length L was nominally 1 μ m.

The resistance in the linear (ohmic) region was equal to $R_0 \approx 3.5 \text{ k}\Omega$ at $V_{gs} = 0$ and $R_{0.6} \approx 14.5 \text{ k}\Omega$ at $V_{gs} = -0.6 \text{ V}$.

In Fig.1 the frequency dependence of relative spectral density of current fluctuations S_I/I^2 at 300 K is shown for two different drain-to-source voltages $V_{ds} = 0.23 \text{ V}$ and $V_{ds} = 0.8 \text{ V}$ at $V_{gs} = 0 \text{ V}$ (curves 1 and 3) and for two different gate-to-source voltages $V_{gs} = 0 \text{ V}$ and $V_{gs} = -0.6 \text{ V}$ at $V_{ds} = 0.23 \text{ V}$ (curves 1 and 2). It is seen that for all three curves the dependence is very close to $S \sim 1/f^{0.6}$. This type of dependence is not necessarily unique among semiconductor devices ($S \sim 1/f^{0.5}$ and even $S \sim 1/f^{0.3}$ have been observed), but as far as we know, it has never been reported from modulation doped structures or highly-doped GaAs or GaAlAs structures. For such kind of structures the $S \sim 1/f$ (flicker noise) or even $S \sim 1/f^{1.5}$ type dependences are typical [3, 4]. It is also seen from Fig.1 that the level of the low frequency noise is quite small. Estimating the total number of electrons in the channel to be $N \sim 1000$ at $V_{gs} = 0 \text{ V}$ it is easy to show that Hooge constant $\alpha = f \cdot N \cdot S_I/I^2$ is equal to $2 \cdot 10^{-5}$ for $f = 20 \text{ Hz}$. According to the criteria established for Si and GaAs such a low value of α indicates a high degree of structural perfection of the channel material comparable to the best epitaxial GaAs channels in FETs [5]. When the negative value of V_{gs} increases, the noise value increases as well (compare curves 1 and 2). Estimates show that the noise level increases at somewhat faster rate than can be explained by the decrease of the total number of electrons in the channel alone. This is due to the contribution of the gate leakage current [6].

In Fig. 2 dashed line shows $I_d - V_{ds}$ characteristic of the 2-D MESFET (at $V_{gs} = 0 \text{ V}$) below the current saturation. Solid lines show S_I/I^2 vs V_{ds} for different frequencies of analysis. It is seen that for frequencies in the range 20 Hz - 20 kHz the characteristics are similar in form. The increase of the noise level with the increase of V_{ds} results from the decrease of the number of carriers in the channel and the change of channel shape as the saturation is approached.. The form of S_I/I^2 vs V_{ds} characteristics agrees quite well with theory [7] which is based on the gradual channel model for FETs.

Measurements in low temperature region show clearly two local temperature maxima (Fig. 3). It is seen that the room temperature ($T=300\text{K}$) corresponds to the high temperature edge of the second maximum, especially for the frequencies $f \geq 160 \text{ Hz}$. This fact provides a natural explanation for small value of $\gamma=0.6$ ($S \sim 1/f^{0.6}$ at 300 K - see Fig.1).

The mechanism for the localization of local levels which is responsible for the observed maxima in the S_I/I^2 vs temperature characteristics, is very complicated for conventional FETs. It is even more complicated for modulation doped structures due to the additional interfaces. It is worthwhile to note that analyzing the observed low temperature maximum according to the technique proposed in paper [8] shows two temperature exponents (Fig.4). In the scope of standard theory for nondegenerate semiconductors [8] this level should be characterized by the position in the forbidden gap $E_c - E_0 = 0.04 \text{ eV}$ and the exponential dependence of the capture cross section $\sigma_n = \sigma_0 \cdot \exp(-E_1/kT)$ where $E_1 = 0.08 \text{ eV}$. It is necessary to perform further analysis to establish definite local levels for this device.

III Conclusion

The low frequency noise in a novel 2D-MESFET has been investigated experimentally for the first time in the temperature range 100 - 300 K and frequency range 20 Hz - 20 kHz. The low frequency noise in this device was small. Two local maxima observed in the temperature range 100 - 180 K and 200 - 300 K are the main contributors to this noise.

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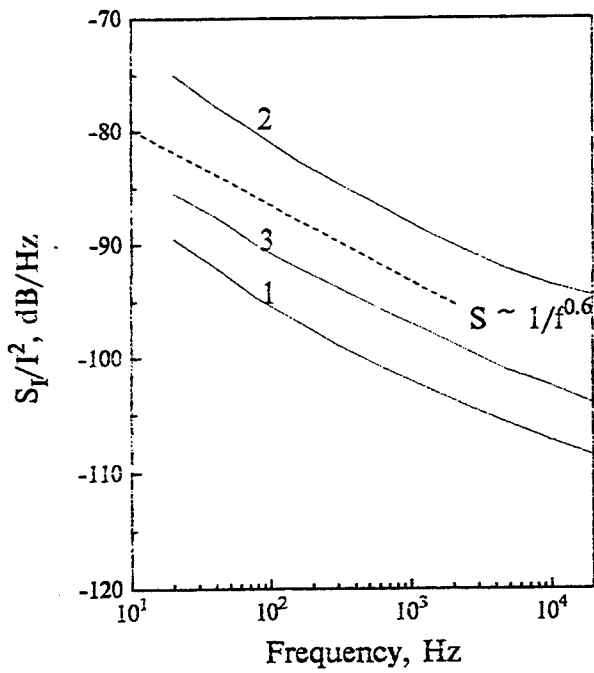


Fig. 1 Frequency dependences of current relative spectral density fluctuations S_I/I^2 at 300 K.

- 1 - $V_{gs}=0, V_{ds}=0.23$ V;
- 2 - $V_{gs}=-0.6$ V, $V_{ds}=0.23$ V;
- 3 - $V_{gs}=0, V_{ds}=0.8$ V;

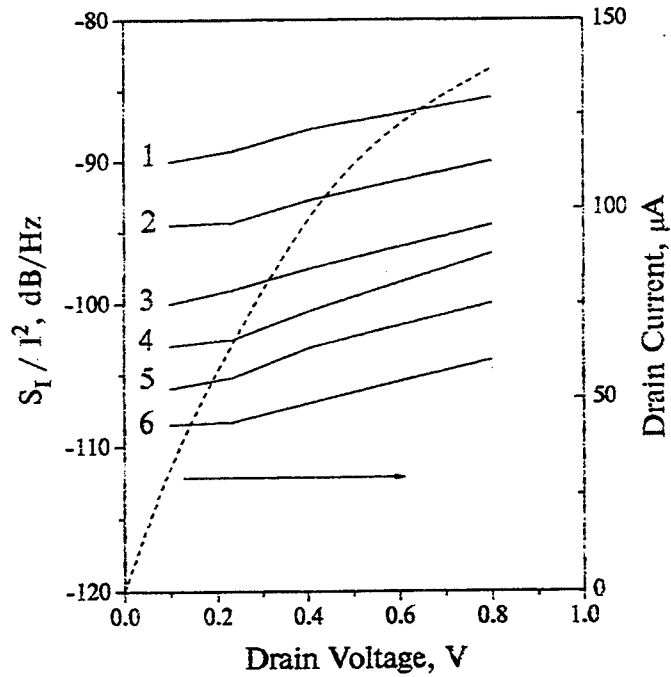


Fig. 2. Dependences of S_I/I^2 vs V_{ds} for different frequencies of analysis. $T=300$ K. Dashed line shows $I_d - V_{ds}$ characteristic for $V_{gs}=0$.

- Frequencies, Hz : 1 - 20; 2 - 80; 3 - 320;
4 - 1300; 5 - 5000; 6 - 20000.

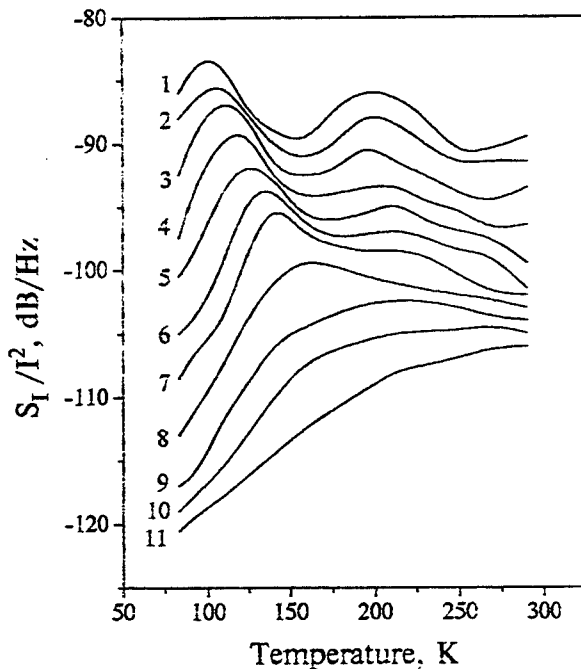


Fig. 3. Temperature dependences of S_I/I^2 for different frequencies of analysis.

$V_{gs}=0; V_{ds} 0.1$ V (linear region).

- Frequencies, Hz: 1 - 20; 2 - 40; 3 - 80; 4 - 160;
5 - 320; 6 - 640; 7 - 1300; 8 - 2500; 9 - 5000;
10 - 10000; 11 - 20000.

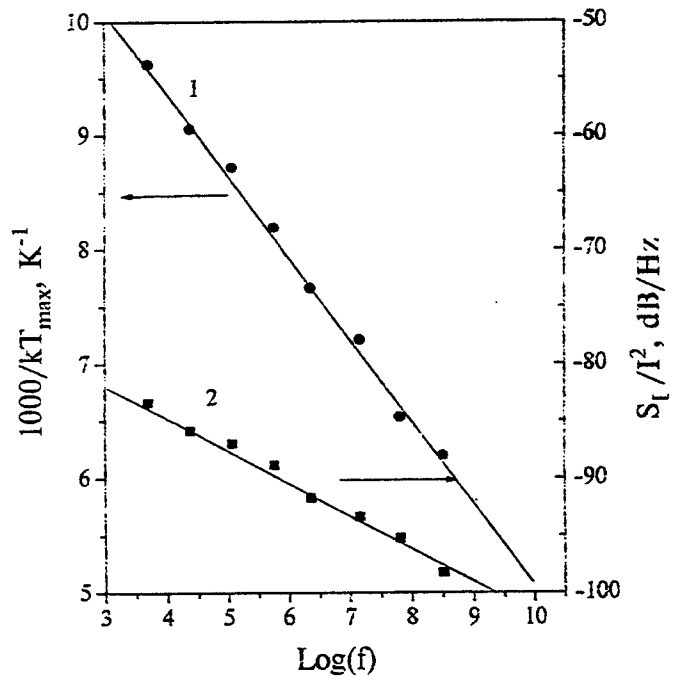


Fig. 4. Dependence of $1/kT_{max}$ vs $\text{Log}(f)$ (curve 1) and S_{max} vs $\text{Log}(f)$ (curve 2) for the low-temperature maxima of Fig. 3.

TRANSPORT OF MANY ELECTRONS IN NANOSTRUCTURED GaAs SCHOTTKY DIODES AT 300 K GOVERNED BY h/e^2

H. P. RÖSER, E. BRÜNDERMANN, H.-W. HÜBERS

DLR, INSTITUTE FOR SPACE SENSOR TECHNOLOGY
RUDOWER CHAUSSEE 5, D-12489 BERLIN, GERMANY

In recent years there has been great interest in transport phenomenon of electrons travelling through samples with mesoscopic structure. This has been strongly influenced by advances in nanostructure fabrication technology for semiconductors with the capability of engineering 1-, 2- and 3-dimensional mesoscopic systems. One of the simplest electronic elements with mesoscopic structure are GaAs Schottky barrier diodes which have anode diameters down to $0.25 \mu\text{m}$ with capacitances as low as $C \geq 0.25 \text{ fF}$.

To investigate the electron transport we used different Schottky diodes (table 1) as rectifier and mixer in a heterodyne receiver with a laser as local oscillator (LO). Heterodyne detection is a coherent process, so that the sensitivity is extremely dependent on the electron transport behavior in the Schottky contact, where the phase sensitive mixing process takes place.

It has been shown in several experiments, if a Schottky diode is driven by an external bias current source, it will be especially sensitive and shows lowest noise for heterodyne detection when the optimum mixing current I_{opt} is proportional to the operating frequency according to $I_{\text{opt}} = (N_e \cdot e) \cdot v$ and the coherent LO radiation generates an optimum amplitude across the diode of $V_{\text{LO}} = (N_e \cdot e) / 2C$ which is independent of the operating frequency. As an example see figure 1. The number of electrons, N_e , passing through the Schottky contact (figure 2) each LO cycle is constant, can be as low as 1, 300, and has a characteristic value for a particular type of diode (table 1). The constant charge transferred each LO cycle can be considered as a result of an "active detection or depletion volume" of thickness D_{depl} which can be determined by two independent methods ranging from $\sim 200 \text{ \AA}$ to $\sim 300 \text{ \AA}$.

The effect on diode performance of cryogenic cooling from 300 K down to $\sim 20 \text{ K}$ was also investigated resulting in no significant improvement. This is a surprising effect because the current density through the Schottky contact is as high as $\sim 10^6 \text{ A/cm}^2$ and at the same time the sensitivity at 300 K is only a factor 30 - 50x above the quantum noise limit.

Further experiments show that the resistance of one single electron moving across the active thickness is $25,750 \pm 600 \Omega$ by plotting the voltage across D_{depl} versus the normalized optimum current I_{opt}/N_e for all diodes (figures 3). This result is very close to the inverse quantized conductance h/e^2 .

Another interesting relation can be found by plotting the square of D_{depl} versus the mobility of different diodes resulting in a proportionality factor of $(2.07 \pm 0.13) \cdot 10^{-15} \text{ V}\cdot\text{s}$ which is very close to $h/2e$ (figure 4).

A possible theoretical explanation for these experimental results achieved at room temperature and with no external magnet field will be given in the paper by Hübers et al. at this conference.

Table 1: Parameters of the investigated Schottky diodes.

Diode		J118	117	1112	1T15
Anode Diameter	[μm]	1.0	0.8	0.45	0.25
Capacitance at Zero Bias C_{j0}	[fF]	1.8	0.9	0.45	0.25
Series Resistance R_S	[Ω]	30	13	33	20
Epitaxial Layer Doping N_D	[10^{17} cm^{-3}]	1.0	3.0	4.5	10
Electrons per Laser Cycle N_e		2800	4500	2200	1300
Rectified LO Signal V_{LO}	[mV]	70	160	260	330
Mobility μ	[$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	5000	3600	3100	2100

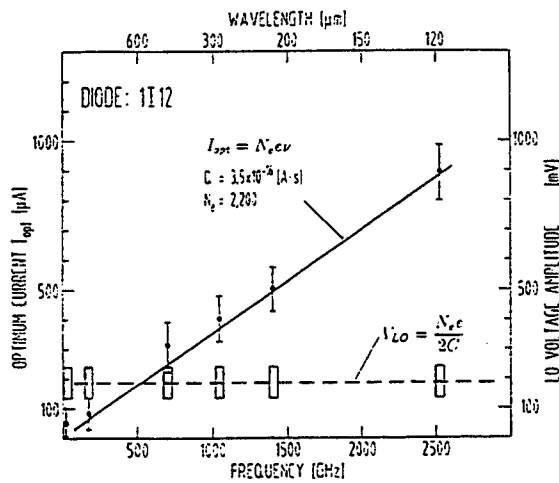


FIG. 1: Optimum current I_{opt} and rectified LO signal V_{LO} as a function of frequency.

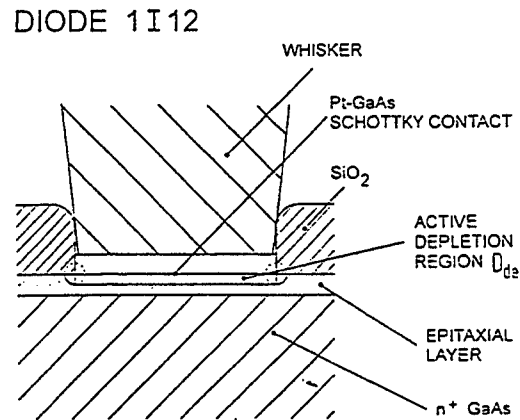


FIG. 2. The Schottky contact of the diode 1I12 with the active depletion region including edge effects. The dimensions are to scale.

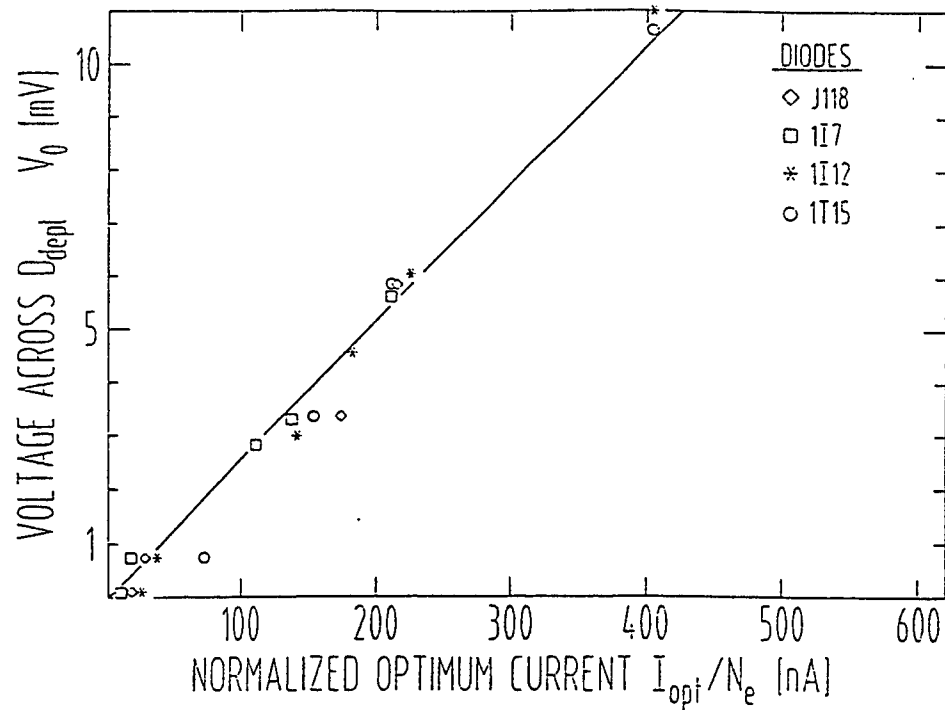


FIG. 3. Voltage across the active depletion thickness V_0 as a function of the normalized optimum current I_{opt}/N_e for four diodes. The fitted line has a slope of $(25750 \pm 600)\Omega$ which is close to h/e^2 .

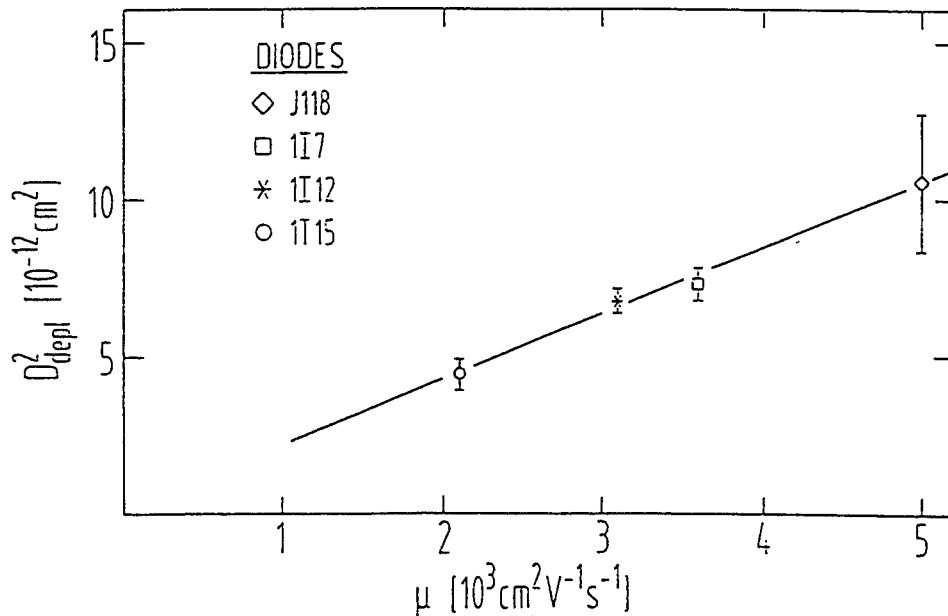


FIG. 4. The square of the active depletion thickness, D_{depl}^2 , as a function of the mobility μ of the different diodes at room temperature. The slope of the fitted line is $(2.07 \pm 0.13) \times 10^{-15} \text{ Vs}$ close to $h/(2e)$.

A Fully Implanted Heavy Ion 0.10 μm gate length NMOS transistor with Gallium channel implantation and Indium pocket doping

F. BENISTANT (Ph.D. Student), G.GUEGAN, M. LERME
S.TEDESCO, F.MARTIN, M.HEITZMANN

LETI (CEA) 17, rue des Martyrs 38054 Grenoble Cedex 9 France

Phone : (33) 76 88 97 95 - Fax : (33) 76 88 94 57 - email : benistan@dmel.ceng.cea.fr

Introduction :

This paper demonstrates, for the first time, the feasibility of fabricating 0.10 μm NMOSFET using heavy ion implantations to suppress short channel effect (SCE). In this work, Gallium and Indium ions are used respectively for channel and pocket implantation.

As the MOS device gate length is reduced, the supply voltage V_{dd} , is decreased and the channel doping is increased to suppress SCE. At the same time, the threshold voltage, V_t , should be approximatively maintained at $V_{dd}/4$ [1]. Therefore, the scaling laws [2] lead to a contradiction. The use of pocket implantation is an efficient way to reduce channel doping without increasing SCE. However, as Boron is a light impurity the containment of the pockets is difficult under the extensions without increasing both junction capacitances and channel doping. Therefore heavy ions are good candidates for this purpose [3]. Moreover, the strong need to obtain symmetrical NMOS and PMOS devices in terms of V_t leads to the use of heavy ions to obtain a retrograde profile in the channel. Figures 1 and 2 show the acceptor and donor pairs necessary to obtain identical channel profiles in NMOS and PMOS devices respectively. Arsenic and Antimony for PMOS and Indium for NMOS have already been published [4,5], however no work on Gallium is known to the authors.

Device fabrication:

In this paper, 0.10 μm NMOS devices have been fabricated, for the first time, with Gallium implanted channel, and either Indium or Gallium pocket doping. As already mentioned, the use of Gallium in the NMOSFET channel gives the same retrograde profile as Arsenic in the PMOSFET channel, for the same implant conditions. Moreover, Gallium has an higher solubility limit than Indium. On an other hand, Gallium is known to have high diffusivity in silicon. However, as the gate length is reduced, the thermal budget of the process is dramatically decreased, and the diffusivity becomes less important. Therefore, no major drawback exists to use Gallium in deep submicron MOS technology. In addition, heavy ion architectures are compatible with conventional processing (Fig.3) without increasing design complexity. For this process, the gate stack consists of 4.5 nm gate oxide and 150 nm α Poly-Si (Fig.4). Figure 5 shows the measured breakdown field (E_{bd}) for MOS capacitors with Indium (150keV), Gallium (140keV) or Boron (25keV) implanted substrate. Sample with uniform Boron doping ($1 \times 10^{16} \text{cm}^{-3}$) is given as standard. High values of E_{bd} show that the growth on a heavy ion implanted substrate does not affect the gate oxide integrity for doses lower than $1 \times 10^{13} \text{cm}^{-2}$. The gate level is patterned by a hybrid e-beam and DUV process which fully integrates e-beam lithography with optical process and equipment. After gate etch, instead of gate reoxidation, a thin 4.5 nm oxide has been deposited to suppress the Bird's Beak in the gate oxide corner (Fig.6). The extension and pocket implantations were made through this thin oxide layer. After formation of the 0.10 μm spacer, the deep S/D implantation was performed (Table 1). The doping profiles were obtained by SIMS measurements (Fig.7, 8). The extension junction depth is 0.05 μm and the deep S/D one is 0.10 μm .

Results and Discussion:

While the device without pocket operates in punchthrough mode, the SCE is suppressed for Indium pocket device (Fig.9), due to both retrograde channel profile and localised pockets. In addition, the roll-up is dramatically reduced with this device, due to both no Indium diffusion and reduced thermal budget. Moreover, because of the electric field in the S/D depletion regions, all the Indium impurities are activated and no frozen carrier effect occurs in these regions. For Gallium pocket devices, the SCE is observed because the implanted pocket dose is five times lower than that Indium pocket devices. However, the V_t shift, for 0.10 μm Gallium pocket device is less than 150mV. The Indium pocket implantation clearly reduces the leakage current (Fig.10), and leads to a 440 mA/mm saturation current at 1.5V (Fig.11) for 0.10 μm device. Saturation transconductance and subthreshold slope have also been evaluated for the three architectures (Fig.12,13). The low V_t value explains the leakage current increase for short channel devices. Because the devices without pocket work in DIBL and punch-through mode, the saturation current is higher for these devices. The drain current versus drain voltage plots show good saturation characteristics for pocket devices (Fig.15, 16).

Conclusion :

For the first time the feasibility of 0.10 μm gate length NMOS device with heavy ion channel and pocket implantation have been demonstrated. The SCE have been suppressed for 0.10 μm device with Gallium doping in the channel and Indium doping in the pockets. In addition, the G_{msat} reaches 325 mS/mm and the saturation current is 440 mA/mm at 1.5V. Therefore, the use of heavy ion implantation is a promising solution for optimization of deep submicron CMOS

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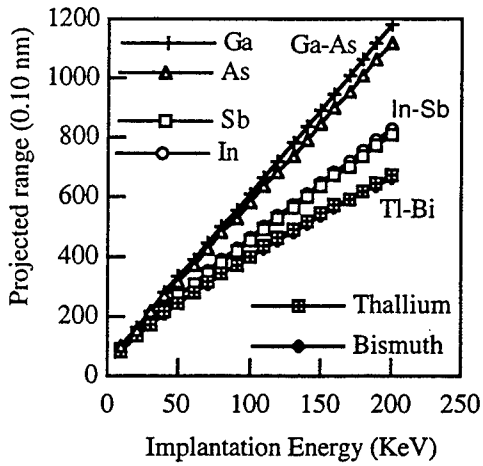


Fig.1 : Rp for acceptors and donors

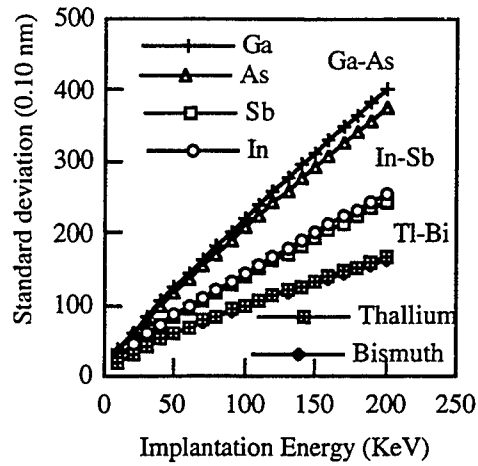


Fig.2 : ΔRp for acceptors and donors

- * Well definition - Isolation (SILO)
- * Gallium channel doping (140 KeV)
- * Gate Oxide (4.5 nm)
- * αPoly Si deposition (in situ doped)
- * Hybrid lithography (e-beam/DUV)
- * Gate etch (Dry) - Thin oxide side wall (4.5 nm)
- * Arsenic extension implantation
- * Pocket implantation
- * Spacer (0.10 μm)
- * S/D implantation - RTA 950°C - 15 sec
- * Metallization

Fig.3: Process steps

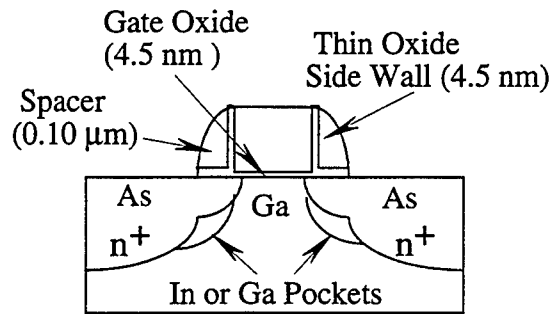


Fig.4: Cross-sectional view of 0.10 μm NMOSFET

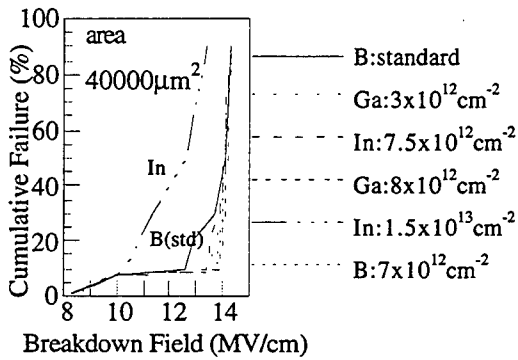


Fig.5: Ebd for implanted and standard (std) samples

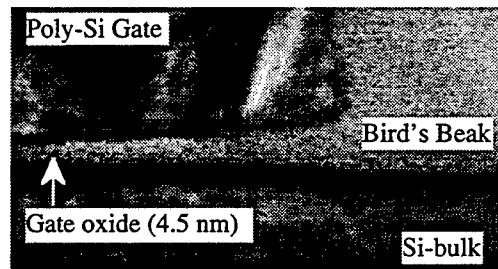


Fig.6: XTEM view of Bird's Beak in Gate Oxide

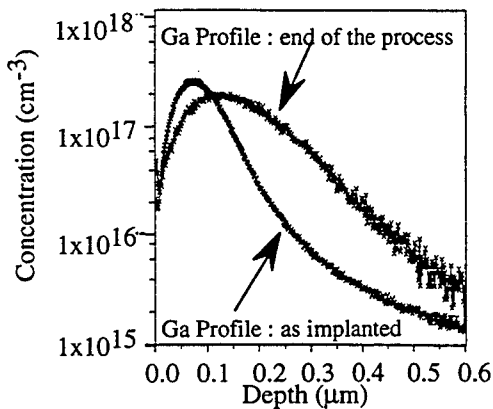


Fig.7: SIMS - Channel Profile

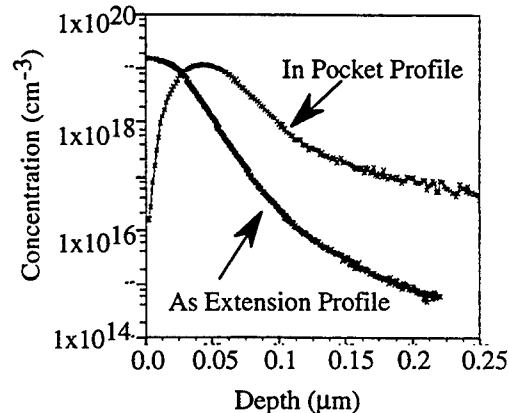


Fig.8: SIMS - Extension and In Pocket Profiles

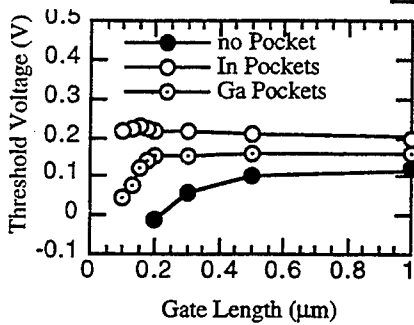


Fig.9 : V_t ($V_{ds}=0.1V$) vs. gate length

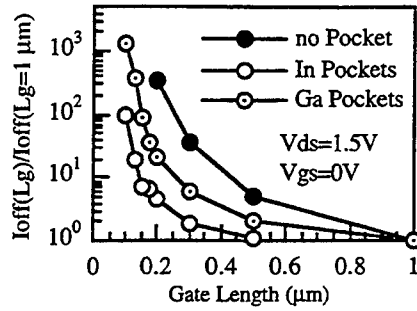


Fig.10: Leakage Current vs. gate length

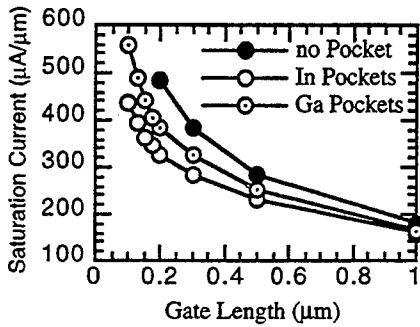


Fig.11: I_{dsat} vs. gate length ($V_{gs}=V_{ds}=1.5V$)

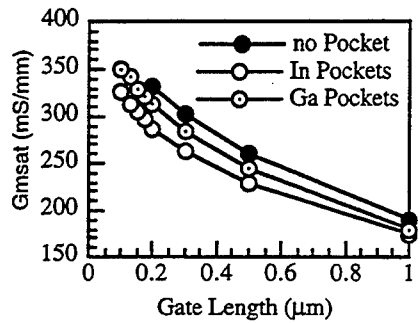


Fig.12: Saturation Transconductance vs. gate length

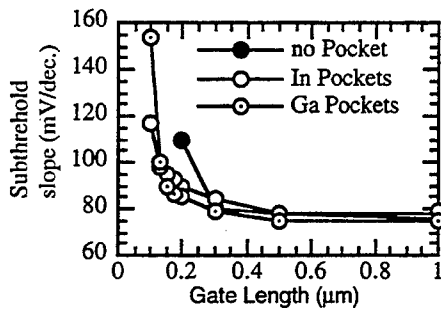


Fig.13: Subthreshold slope vs. gate length

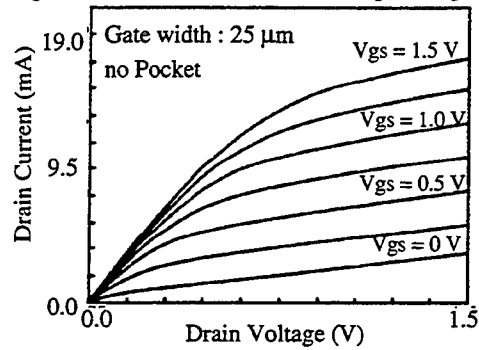


Fig.14: I-V Characteristics of $0.10 \mu m$ NMOSFET

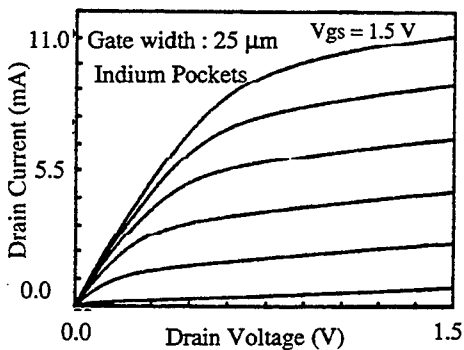


Fig.15: I-V Characteristics of $0.10 \mu m$ NMOSFET

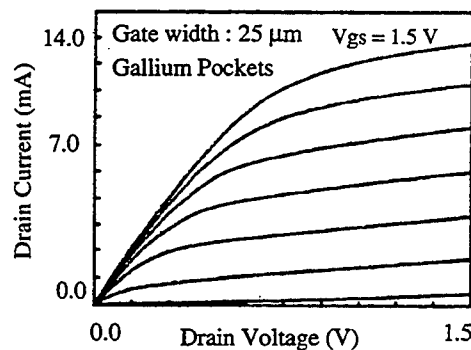


Fig.16: I-V Characteristics of $0.10 \mu m$ NMOSFET

Gallium Pockets	Ga : 80 keV - $1 \times 10^{13} \text{ cm}^{-2}$
Indium Pockets	In : 100 keV - $5 \times 10^{13} \text{ cm}^{-2}$
S/D Extension	As : 12.5 keV - $1 \times 10^{14} \text{ cm}^{-2}$
Deep S/D	As : 40 keV - $1 \times 10^{15} \text{ cm}^{-2}$

Table I: Implantation conditions of Pockets and source/drain

Ultradense Hybrid SET/FET Dynamic RAM: Feasibility of Background-Charge-Independent Room-Temperature Single-Electron Digital Circuits

K.K. Likharev and A.N. Korotkov

Department of Physics, State University of New York at Stony Brook, NY 11794-3800

1. Introduction

To our knowledge, correlated single-electron tunneling [1, 2] remains the only known realistic physics basis for future nanoelectronic digital circuits [3-4]. In contrast to the semiconductor transistors, operation of single-electron devices is based on the ubiquitous Coulomb interaction of electrons, and as a result these devices can be in principle scaled down to single-atomic size [5]. Nevertheless, until recently digital single-electronics faced several serious problems.

Firstly, attempts to directly imitate CMOS digital circuits by replacing FETs by SETs (Single-Electron Transistors [1-4]) would lead to an unacceptable power dissipation, $\sim 3 \text{ kW/cm}^2$ for room-temperature devices with $\sim 10^{11}$ transistors per cm^2 [4, 6]. This problem may be circumvented by using one of the Single-Electron Logics [4, 7] where digital bits are presented by single electrons and static power dissipation is negligible. Secondly, in order to avoid thermally-induced digital errors, the structures with extremely small capacitance, $C \sim 0.01 k_B T / e^2$, and hence of extremely small size should be employed [6]. For room temperature operation, this results in the need of ~ 1 -nm patterning of circuits with the terabit integration scale - a technological level which is hardly in sight. Finally, the switching thresholds of digital single-electronic devices are very sensitive to charged impurities trapped in their non-conducting environment [1, 4]. For example, a single charged impurity located near a conducting island of the device, may shift its background charge Q_0 by $\delta Q_0 \sim e$, while the switching thresholds are e -periodic functions of Q_0 . Moreover, for nanometer-scale devices, a considerable contribution into the threshold position may be provided by energy quantization of electrons in conducting islands. In this case, even small random variations of the island size or shape may lead to unpredictable variations of the switching thresholds, making operation of LSI circuits impossible.

The objective of the present work is to suggest the first Q_0 -insensitive single-electronic devices which may not only allow the last problem to be avoided completely, but also facilitate fabrication of the single-electron circuits by softening size requirements by a factor of ~ 5 (i.e. allowing ~ 5 -nm minimum feature size for room-temperature operation).

2. The Basic Concept

The basic idea of the Q_0 -independent operation of the capacitively-coupled single-electron transistor is demonstrated in Fig. 1. The "source-drain" current I through the transistor is a e -periodic function of $Q_f = Q_0 + C_g U_{in}$, with amplitude $\Delta I \sim eG/C$, where G and C are the tunnel junction conductance and capacitance, respectively, while C_g is the gate capacitance. The randomness of the background charge Q_0 makes the response of the device to small signals ΔU_g unpredictable. Let us consider, however, a ramp-up of U_g by $\Delta U_g > e/C_g$. The transistor response will be an oscillation of the current I with the

full swing equal to ΔI , regardless of Q_0 . After amplification (say, by a FET sense amplifier) this response may be rectified and serve as the output signal. In order to prevent its contamination by the Q_0 -dependent dc background, a high-pass filter (say, just a blocking capacitor C_b) may be used between the SET and FET stages (Fig. 1a).

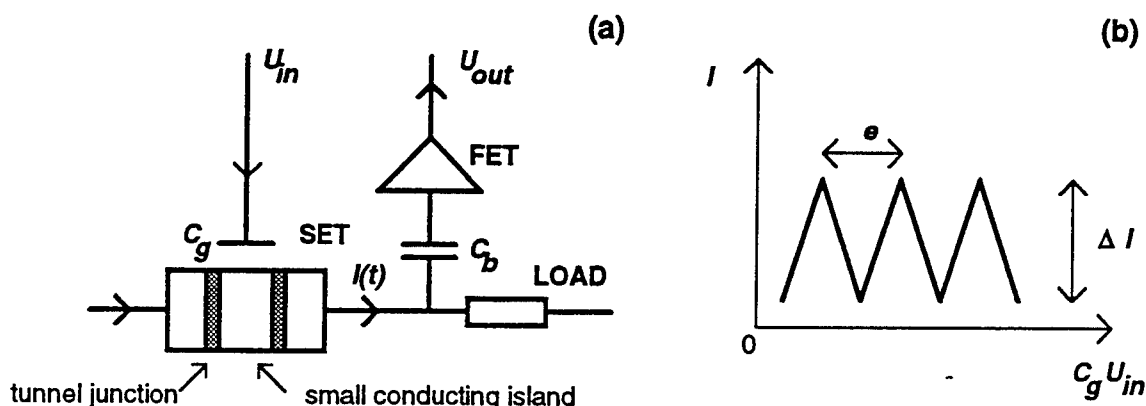


Figure 1. (a) SET-FET transistor system and (b) transfer function of the single-electron transistor (schematically)

3. Memory Cell

As an example of the application of this general concept, consider a non-volatile dynamic RAM combining SET-based cells and FET sense amplifiers (Fig. 2). As in traditional non-volatile semiconductor memories [8, 9], digital bits are stored in the form of electric charge Q of a floating gate, in our case the gate is extremely small (of the order of 10 nm; see Sec. 4 below) and the charge is just a few electrons. The charge may be changed by its injection/extraction via an element with a sharp conduction threshold V_f . We have considered two possible implementations of this element. The simplest option is to use just a relatively thick dielectric layer with Fowler-Nordheim tunneling above V_f , similar to that used in the usual semiconductor non-volatile memories [8, 9]. An alternative is to use an Ohmic resistor $R_f \gg h/e^2 \sim 10^4 \Omega$ in series with a small tunnel junction (similar to those used in the SET) [1, 10, 11].

The system dynamics is presented by the phase diagram shown in Fig. 2c; in this diagram, each thin horizontal line corresponds to a certain number n of electrons trapped in the floating gate. The writing threshold V_f for the effective voltage $V_{ef} = C_g(V_w - V_b)/C_\Sigma$ may be reached by the application of positive voltage V_D to the word line and similar negative voltage to both bit lines (C_Σ is the total capacitance of the floating gate). Before reading, the cell is preconditioned by the application of a voltage V_D to the corresponding bit lines (this operation increased parameter margins substantially). Finally, write 0/read 1 operation is achieved by the application of positive $V_b = V_D$ and negative $V_w = -V_D$. The charge of the floating gate changes by $\Delta Q = e\Delta n = -C_\Sigma V_D$, the effective charge Q_f of the SET island changes by $\Delta Q_f = e\Delta n C_g / C_\Sigma > e$. Because the drain-source voltage $2V_f \sim e/C$ is applied to the transistor simultaneously, its current performs several oscillations (Fig. 1b) during the last process. These oscillations are picked up by a FET sense amplifier (Fig.

2a), which may serve simultaneously a block of $N \gg 1$ SET cells connected in parallel. After rectification, this waveform is sent to the output, signaling that the selected cell had the state 1 before the write/read operation; if the state was 0, then $\Delta n = 0$, and no output signal is formed.

An elementary analysis shows that for this bit-addressable operation the charge difference $\Delta Q = Q_1 - Q_0$ should be below $2C_\Sigma V_t/3$; random spread of the switching thresholds would force a further reduction of the upper bound for ΔQ , which vanishes if $(V_t)_{\max} > 2(V_t)_{\min}$.

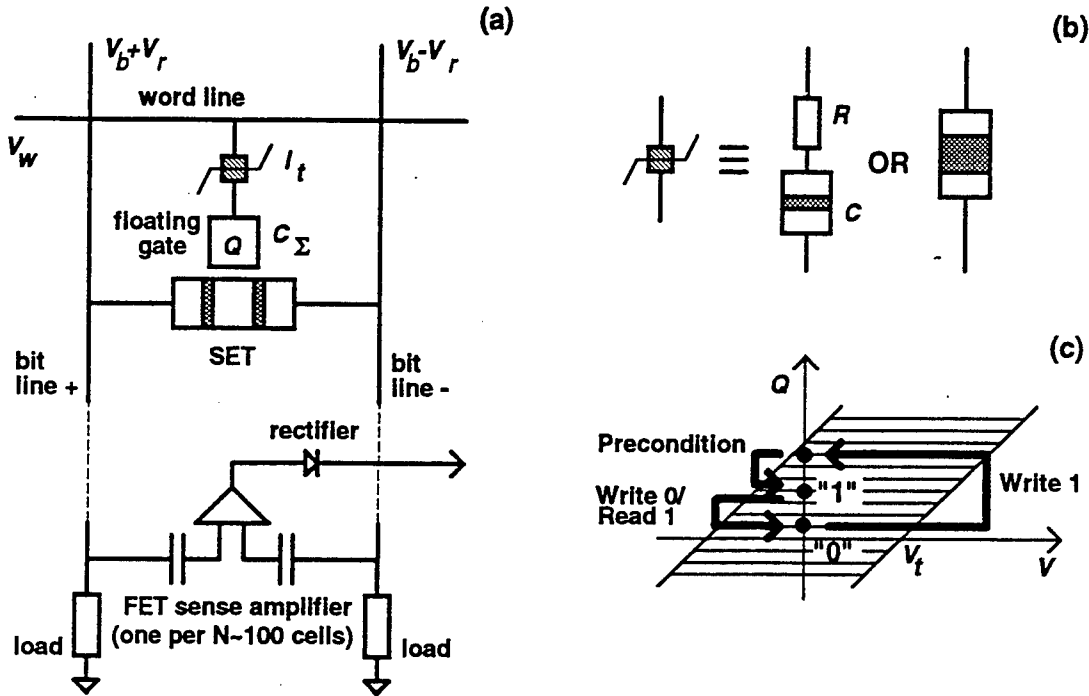


Figure 2. Hybrid SET/FET memory: (a) structure, (b) possible threshold elements, and (c) memory cell dynamics shown schematically on its phase diagram.

4. Parameter Estimate

In order to estimate the possible density of the hybrid DRAM, we have carried out a detailed analysis of a particular example, where the middle electrode of SET and the floating gate are islands of highly n-doped ($n = 3 \times 10^{20} \text{ cm}^{-3}$) Si islands of size $5 \times 5 \times 3 \text{ nm}^3$ and $7 \times 7 \times 5 \text{ nm}^3$, respectively. Such a high doping ensures that fluctuations of the number of background electrons in the islands (~ 25 and ~ 75 , respectively) are relatively small. The threshold element with $V_t = 3 \text{ V}$ is a 2-nm-thick layer of an insulator providing the low-field energy barrier of height $U = 3 \text{ eV}$, while the SET-gate insulation is a 10-nm-thick SiO_2 layer. SET has lateral SiO_2 tunnel junctions of area $5 \times 3 \text{ nm}^2$ and barrier thickness of 2 nm. The word and bit lines and gaps between them are 10 nm wide; it is this width which determines the area $S = 20 \times 40 \text{ nm}^2$ of the whole cell. With due allowance for FET sense amplifiers (one per $N = 100$ SETs), this size corresponds to the cell density of $10^{11} \text{ bits/cm}^2$.

In this case we get $C_{\Sigma} \approx 0.8$ aF, $\Delta Q \approx 10e$, $C_g \approx 0.1$ aF, $\Delta Q_g \approx 1.5e$. Capacitance C and conductance G of each junction of the SET is about 0.2 aF and 20 μ S, respectively, so that the total capacitance C_m of the middle island is close to 0.6 aF, and the single-electron charging energy $e^2/C_m \sim 250$ meV $\sim 10k_B T$ is sufficiently high for operation at room temperature (electron energy quantization in the middle island increases the total electron addition energy to ~ 400 meV). In particular, the r.m.s. noise of the transistor [12] within the 300 MHz bandwidth, reduced to its input charge, is close to $5 \times 10^{-3}e$. This is why even if $N=100$ SETs are connected in parallel, the signal-to-noise ratio (~ 10) is still acceptable for a reliable read-out. The cycle time is restricted to ~ 10 ns mostly by charge injection to/extraction from the floating gate; processes of charging the SET-FET interconnects (~ 0.1 ns) and of FET output lines (~ 1 ns) are considerably faster. The total power dissipation (~ 3 W/cm²) is mostly due to that in FET sense amplifiers; power consumption of SETs (~ 30 mW/cm²) and energy loss due to recharging of interconnects and floating gates (~ 3 mW/cm²) are considerably lower.

To summarize, we do not see any insurmountable problem with implementation of such DRAMs, provided that 5-nm patterning technology is on hand.

5. Conclusion

The ultradense DRAM considered above is not the only possible application of this basis concept. Recently we have suggested use of the same concept for implementation of electrostatic mass data storage with density in excess of 10^{12} bits/cm² [13]. Other suggestions are certainly forthcoming. Generally we believe that using single-electron devices to complement silicon technology, rather than compete with it, may lead to the demonstration of room-temperature digital circuits of unprecedented density in the near future.

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Tailoring Acoustic Modes in Mesoscopic Devices

Michael A. Stroschio, Gerald J. Iafrate and John Zavada
U.S. Army Research Office
Research Triangle Park, NC 27709-2211

K. W. Kim, Yuri Sirenko and SeGi Yu
Department of Electrical and Computer Engineering
North Carolina State University
Raleigh, NC 27695-7911

V. Mitin, N. Bannov and V. Mickevicius
Department of Electrical and Computer Engineering
Wayne State University
Detroit, Michigan 48202

Mitra Dutta and Arthur Ballato
Physical Sciences Directorate
U.S. Army Research Laboratory

In numerous publications of the last several years [1,8], acoustic phonons have been quantized for a variety of nanoscale and mesoscopic structures in order to assess to role of electron--acoustic-phonon scattering in limiting the performance of nanoscale and mesoscopic electronic devices. These structures include quantum wells, quantum wires with cylindrical and rectangular cross sections, and quantum dots with spherical, cylindrical and rectangular boundaries. These quantized phonons have been studied for the two cardinal boundary conditions of classical acoustics: free boundaries (open boundaries) where the phonon displacements are unrestricted and allowed to balance all normal traction forces to zero; and clamped boundaries (rigid boundaries) where phonon displacements are required to vanish at the boundaries. For quantum wells, scattering rates have been calculated for free-standing structures [4,8]. For the case of quantum wires, scattering rates have been calculated only for the case of infinitely long quantum wires and, as appropriate for this case, the acoustic phonons have been quantized in only the lateral dimensions. However, for realistic mesoscopic device designs, the quantum wire input and output "leads" as well as the active regions of the devices with quantum-wire geometries have finite lengths. Accordingly, deformation and piezoelectric scattering rates must be based on acoustic phonons that are quantized in all three spatial dimensions. The international community does not appear to have considered the role of three dimensional confinement of acoustic phonons in mesoscopic devices but it is clear from the solutions of classical acoustics that boundary conditions imposed at the ends of wire-like regions can have a profound effect on the properties of acoustic

modes. The results presented here are based, in part, on a consideration of the role of acoustic phonon confinement in mesoscopic devices containing finite wire-like regions. Based on our current understanding of such finite wire-like structures, we believe that it is possible to "engineer" mesoscopic structures so that electron--acoustic-phonon scattering is reduced. This reduction is likely to be most important in mesoscopic device which operate in the basis of "coherent" electron-wave interference effects.

In the domain of classical acoustics, especially revealing examples of the role of wire-like regions in modifying and tailoring selected acoustic mode patterns are those of the organ pipe and of the muffler. In the first example, the open boundary conditions at the ends of the organ pipe result in wave reflections with the reflected and transmitted waves having amplitudes with the same sign at the ends of the organ pipe. Subject to these boundary conditions, the acoustic modes in an organ pipe evolve so that standing wave amplitudes are maximized and anti-nodes are formed at the ends of the pipe; that is, the dominant modes are those having wavelengths such that the length of a half-integral number of wavelengths is equal to the length of the pipe. Thus, an organ pipe produces sounds at well defined and reproducible wavelengths. In the second example, a muffler suppresses sounds at exit ports through the use interfaces which produce modes with the required node and anti-node structures.

In the case of mesoscopic devices the situation is, perhaps, more complex than in the case of classical acoustic waveguides with open boundaries since, in general, the boundary conditions at the ends of the quantum wires require that both the mode displacements and the normal components of the stress be continuous. However, for the case of a quantum wire which couples to an "end" region composed of the same material as that in the interior of the quantum wire, the open boundary condition such be appropriate. Thus, for, example, in the case of a quantum wire with two "open" ends the ambient acoustic phonons in the wire will evolve so that the dominant modes are those having wavelengths such that the length of a half-integral number of wavelengths equals the length of the quantum wire. Just as in the organ pipe these modes will have their maximum amplitudes at the ends of the wires; that is, anti-nodes will be present at the ends of the quantum wire. Similar behavior may be expected for the case of free-standing quantum well structures. For the case of a quantum wire which couples to (or terminates on) a region composed of a material with acoustic properties different from those of the material in the interior of the wire, the exact boundary condition must, in general, be applied. From classical acoustics it is known that few analytical solutions are available for the cases where the complete boundary

conditions must be used. A useful simplification arises in the case where the material in the interior of the quantum wire and the material at the end of the quantum wire have such different properties that the phonon modes are damped abruptly at the interface between the two materials; in this case, the so-called "clamped" boundary condition is adequate and the modes amplitudes may be assumed to vanish at such interfaces. Such a case applies at some metal-semiconductor interfaces. In particular, for a mesoscopic device having wire-like regions which terminate on a variety of metal regions (regions used as contacts, gates, barriers, etc.) it is satisfactory to apply clamped boundary conditions. At these boundaries, the acoustic modes will have nodes instead of the anti-nodes that are established in the case of an open boundary.

With this set of simplified boundary conditions it is possible to design mesoscopic structures with the phonons "engineered" to produce desired standing wave patterns. As an example, consider a four-terminal generalization of the three-terminal "tee"-shaped de Broglie wave interference device [9]. More specifically, consider a mesoscopic structure with quantum wires intersecting each other at right angles such that the two wire "centers" are at the same point. For this structure the ends of one wire are taken to be open and the ends of the other wire are taken to be clamped. Hence, it is possible to select some acoustic modes such that nodes will occur in "center" of one wire and anti-nodes will occur at the "center" of the other wire. By selecting various wire lengths it is possible to define a standing wave pattern that either maximizes or minimizes the amplitudes of specific acoustic phonon modes in regions where the electronic wavefunctions are dominant. Furthermore, by "engineering" interfaces within a quantum wire which are perpendicular to the quantum-wire axis, it should be possible to control the acoustic modes in wire-like regions of mesoscopic devices just as the classical acoustic modes are controlled in a muffler. Thus, the deformation and piezoelectric scattering rates may be partially tuned by tailoring the ambient phonon standing wave patterns in such mesoscopic structures.

In this effort to "engineer" the ambient phonon modes, the quantum-wire phonon modes obtained previously [1,8] should correctly describe the lateral quantization of the phonon modes. Elementary examples of such effects are implicit in the results of Ref. [8]. The quantization along the lengths of the quantum wires will be treated approximately under the simplifying "open" and "clamped" boundary conditions to assess the extent to which mesoscopic device properties may be controlled through the "engineering" of the phonon modes in mesoscopic devices. It is emphasized once again that the major payoff from the "quantum engineering" of acoustic phonons in quantum wires is the

reduction of electron--acoustic-phonon scattering and the consequent preservation of "coherent" electron waves in mesoscopic devices. Achieving nearly-coherent electron waves may ultimately depend sensitively on reducing electron--acoustic-phonon scattering even though such processes may be considered to be weak by normal standards.

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2-D MESFET/RTD LOGIC ELEMENT FOR COMPACT, ULTRA LOW-POWER ELECTRONICS

J. Robertson, T. Ytterdal, W. C. B. Peatman¹, R. Tsai, E. Brown², and M. Shur

Department of Electrical Engineering, University of Virginia Charlottesville, VA 22903

¹on leave from UVA to Advanced Device Technologies, Inc. Charlottesville, VA 22901

²MIT Lincoln Laboratory, Lexington, MA 02173

ABSTRACT

We describe highly functional logic elements utilizing a two-dimensional (2-D) MESFET as a driving device with a resonant tunneling diode load. The 2-D MESFET uses lateral Schottky contacts¹ to modulate the 2-D electron gas width. The novel contact geometry results in reduced capacitance, low parasitic resistance, ultra low power performance, and the elimination of the narrow channel effect (NCE)² compared to conventional HFETs or MESFETs. The advantage of using a RTD as the load device is the reduction of the static power consumption at the logical high input level. We demonstrate low power 2-D MESFET/RTD inverter operation and use our AIM-Spice models to prescribe device optimizations to further reduce power consumption. Finally, using the multiple-gate feature of the 2-D MESFET, we demonstrate compact NAND and NOR gates using a single 2-D MESFET/RTD pair.

1. INTRODUCTION

High speed, low-power IC operation has become an increasingly important area of research, with applications to battery-powered portable electronic devices such as notebook computers and wireless communications. This consideration dictates the ideal inverter load element as one that exhibits low current at digital logic levels for low static power but high current otherwise for high speed switching, as shown in Fig. 1. Lehocvec first demonstrated the use of a *p-n* tunnel diode featuring a negative differential resistance (NDR) region to meet these requirements.³ These were later replaced with resonant tunneling diodes (RTDs) featuring higher speed, lower capacitance, and compatibility with present materials technology.^{4,5}

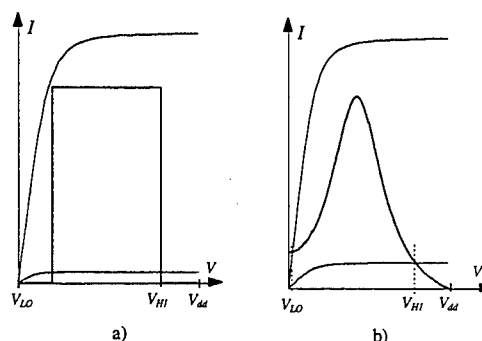


Fig. 1. *I-V* characteristics of an 2-D MESFET with a) ideal load line and b) RTD load line.

Further improvements have come from increasing the performance of the driving device, in particular using materials with higher carrier mobilities and smaller dimensions. However, parasitic effects such as NCE ultimately limit the performance of these devices. In this paper we present measurements and simulations of the RTD-load inverter using the 2-D MESFET for driving. Since the NCE is practically eliminated in the 2-D MESFET, very low power operation and compact NAND and NOR gates are achieved. Furthermore, due to higher mobility, smaller parasitics, absence of short-channel effects and suppression of hot-electron effects, we expect smaller power-delay products compared to Si-based technologies.

2. DEVICE STRUCTURES

The 2-D MESFETs were fabricated from a pseudomorphic $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ heterostructure grown on a semi-insulating GaAs substrate by molecular beam epitaxy (MBE). Typically, the 2-D MESFET structure consists of an undoped GaAs buffer layer, an AlGaAs/GaAs superlattice buffer, an $\text{Al}_{0.24}\text{Ga}_{0.76}\text{As}$ layer imbedded with a Si δ -doped plane, an InGaAs channel, an $\text{Al}_{0.24}\text{Ga}_{0.76}\text{As}$ layer imbedded with a Si δ -doped plane, and an

n^+ GaAs cap layer doped to $4 \times 10^{18} \text{ cm}^{-3}$. This structure gives a sheet density of $2\text{-}3 \times 10^{12} \text{ cm}^{-2}$ and a carrier mobility of $6000 \text{ cm}^2/\text{Vs}$ at room temperature. Fabrication details and schematics for the dual-gate device are discussed in Peatman *et. al.*² Fig. 2 shows a schematic of a 3-gate structure, as well as a cross-section of the device. Both two-gate (one on either side of the 2-deg channel) and three-gate devices (as shown in Fig. 2) were fabricated.

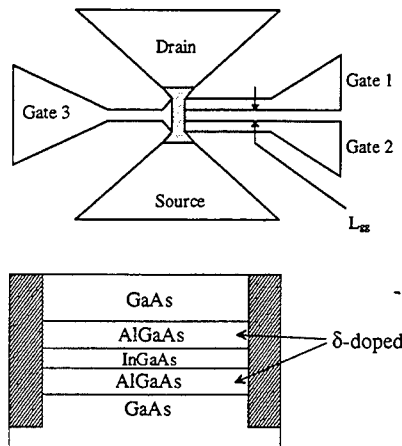


Fig. 2. Schematic of the 3-gate AlGaAs/InGaAs/GaAs 2-D MESFET device structure. Top view (above) and cross-section (below) showing a typical layer structure (not drawn to scale).

The RTDs were fabricated from an epitaxial layer structure grown on a semi-insulating GaAs substrate by MBE. The resonant tunneling occurs through two 3 nm thick $\text{Al}_{0.69}\text{Ga}_{0.31}\text{As}$ barriers surrounding a 5 nm thick $\text{In}_{0.21}\text{Ga}_{0.79}\text{As}$ well. There is a 10 nm undoped GaAs spacer layer on the collector side of the double barrier and the ohmic contacts are made to n^+ GaAs layers doped to $3 \times 10^{18} \text{ cm}^{-3}$. This material structure gives a room temperature peak current density of around 500 A/cm^2 and peak and valley voltages of 0.9 V and 1.6 V, respectively.

3. 2-D MESFET/RTD INVERTER CHARACTERISTICS

Fig. 3 shows the measured (symbols) and simulated (lines) current-voltage characteristics of a dual-gate 2-D MESFET and the load-line characteristics of an RTD. All measurements were made at room temperature using a HP4145 parameter analyzer and a Micromanipulator probe station. The simulations were performed on AIM-Spice⁶ using accurate I - V and C - V models for the 2-D MESFET² and an empirical

I - V model for the RTD representing a voltage-shifted diode in parallel with a current source:

$$I = \frac{A_I V}{1 + A_V (V - V_{pe})^2} + V \cdot B_1 \exp[B_2 (V - B_3)]$$

where A_I and A_V determine the resonant peak current, V_{pe} is the peak voltage, B_1 and B_2 determine the diode current and B_3 represents the diode voltage shift. The RTD capacitance is modeled as $C = C_0 A$, where C_0 is a constant determined by the material structure and A is the cross-sectional area. The 2-D MESFET had nominal dimensions of $W_0 = L_g = 0.5 \mu\text{m}$.

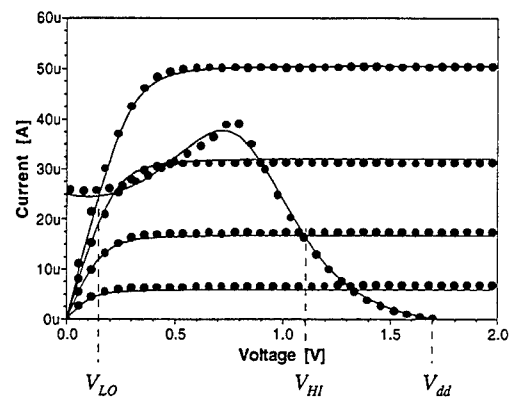


Fig. 3. 2-D MESFET I - V characteristics and RTD load line. Solid lines are simulated data and symbols are measured data. For the 2-D MESFET characteristics the topmost curve represents $V_{gs} = 0.5 \text{ V}$, and the stepsize is -0.25 V .

Here, the gates were electrically connected. The pinch-off voltage was -0.55 V , the peak drain current was $75 \mu\text{A}$ at $V_{gs} = 0.7 \text{ V}$ (150 mA/mm). The RTD diode area was approximately $8 \mu\text{m}^2$ and exhibited a peak current of $39 \mu\text{A}$ at 0.9 V and a valley current of $25 \mu\text{A}$ at 1.6 V , giving a peak-to-valley current ratio (PVCR) of 1.6.

Fig. 4 demonstrates the measured and simulated inverter performance using these devices. When connecting inverters in a chain with the output of one inverter driving the input of the next, the output voltage level does not exceed around 0.8 V due to leakage through the Schottky barrier of the next stage. This results in a minimum voltage drop across the RTD of around 0.8 V , causing a current through the device of approximately $32 \mu\text{A}$. At low output voltages the current is limited by the valley current of the RTD of $25 \mu\text{A}$. The resulting average static power dissipation is about $46 \mu\text{W}$.

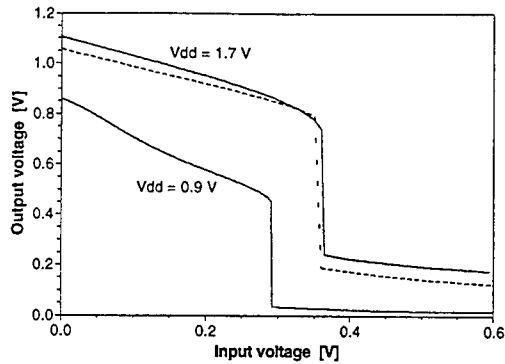


Fig. 4. Measured and simulated inverter transfer characteristics. Solid lines are simulated results and dashed line is measured data. The curve labeled $V_{dd} = 0.9$ V represents the transfer curve for an optimized inverter discussed in Section 5.

This relatively high value is due to the high RTD valley current and the negative pinch-off voltage of the driving FET. Furthermore, by assuming $C_0 = 1.25 \text{ fF}/\mu\text{m}^2$ (1000 Å depletion width), we simulated the power-delay product of the inverter to be 10 fJ.

4. COMPACT NAND AND NOR GATES

The 2-D MESFET geometry, having gates on either side of the channel, lends itself naturally to multiple input logic gates. To illustrate this, the operation of two-input NAND and NOR gates utilizing a single 2-D MESFET/RTD pair are demonstrated in Fig. 5 and 6.

The NOR gate of Fig. 5 uses a two-gate driving device. The channel is pinched-off when both gates are biased at the logic low level, giving a high output. Applying a logic high level to either gate allows the channel to conduct, giving a low output. The NAND operation of Fig. 6 uses a three-gate driving device, with the inputs applied to the two same-side gates and a reference voltage (V_{ref}) applied to the opposite gate. Biasing either input gate at the logic low level results in pinch-off, giving a high output. Biasing both gates at the logic high level allows the channel to conduct, giving a low output.

The input signals of Figs. 5 and 6 were 0.8 V for the high logic level and -2.2 V for the low logic level, while the supply voltage was at 1.6 V. These values were used to demonstrate the gates' principle of operation, and the device characteristics may be optimized to obtain consistent DCFL logic levels as discussed in the next section.

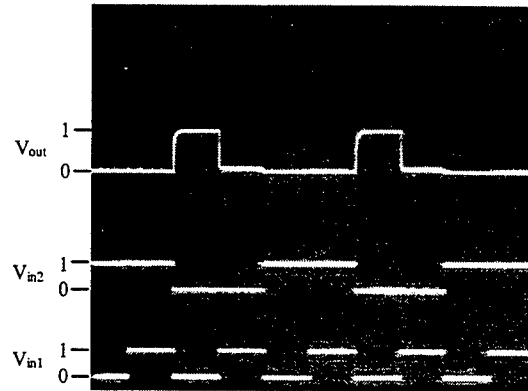


Fig. 5. Demonstration of NOR operation using 2-D MESFET driving device. Top trace is output and lower 2 traces are inputs.

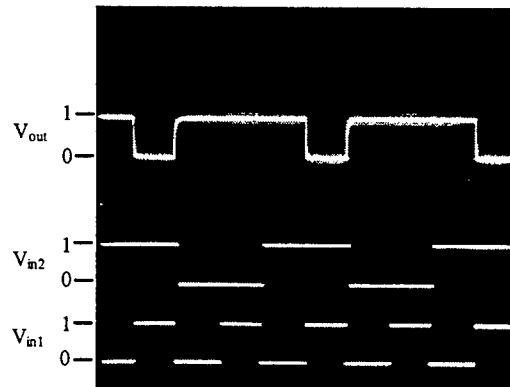


Fig. 6. Demonstration of NAND operation using 3-gate 2-D MESFET driving device. Top trace is output and lower 2 traces are inputs. $V_{ref} = 0$ V.

5. DEVICE OPTIMIZATION AND FUTURE DIRECTIONS

The static power dissipation of the inverter presented in Section 3 can be substantially improved by optimizing the device characteristics. First, to obtain consistent DCFL logic levels and to reduce the power dissipation in the low-input-high-output logic state an enhancement mode 2-D MESFET driving device should be used. Next, the PVCR should be increased to obtain lower static power dissipation. Furthermore, the peak and the valley voltages of the RTD should be shifted to lower levels to accommodate lower power supply levels. Finally, the current level of the RTD can be scaled to maximize the noise margin. Figures 4 and 7 show the resulting transfer characteristics and I - V characteristics, respectively, after optimizing the inverter from Section 3.

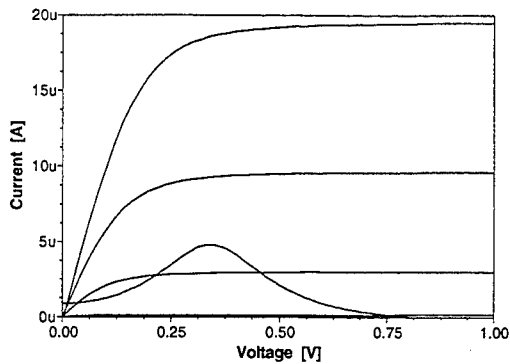


Fig. 7. Optimized 2-D MESFET I-V characteristics and RTD load line. For the 2-D MESFET characteristics the topmost curve represents $V_{gs} = 0.5$ V, and the stepsize is -0.25 V.

The driving device's I - V characteristics of Fig. 7 are typical of enhancement-mode 2-D MESFETs,⁷ while the peak and valley voltages and PVCR of the RTD are obtainable using standard material growth and fabrication techniques. The simulated static power dissipation through one stage of an inverter chain based on optimized inverters is calculated to be $1 \mu\text{W}$. For comparison, the simulated power dissipation using the same driving device and a 2-D MESFET load is calculated to be $3 \mu\text{W}$. Assuming a diode area of $2 \mu\text{m}^2$, the power-delay product of the optimized inverter was estimated to be approximately 0.5 fJ .

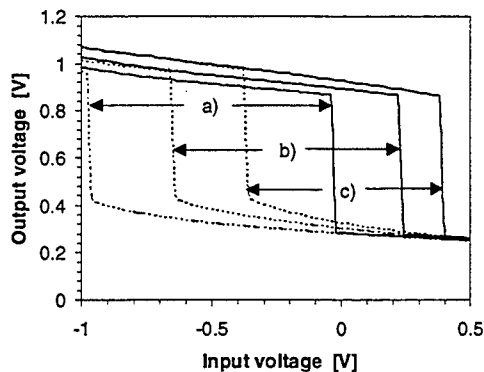


Fig. 8. Dependence of driving voltage on second gate bias in a dual gate 2-D MESFET/RTD inverter. Solid lines and dashed lines correspond to sweeping the input voltage up and down, respectively. The second gate bias voltages were a) 0.5 V, b) -0.5 V, and c) -1.5 V.

Since one of the three gates in the 2-D MESFET shown in Fig. 2 can be used to control the threshold voltage, this device allows us to realize programmable gate arrays containing both NAND and NOR gates. It can be also used for many other programmable logic applications. For example, Fig. 8 suggests a possible

application of a dual-gate inverter, as a sample-and-hold element, utilizing both the hysteresis inherent with RTD loads and the "programmable" switching point.

6. SUMMARY

We have demonstrated the operation of an inverter using a 2-D MESFET as the driving device and a RTD load. Low power operation arising from the MESFET's 2D-3D geometry and the RTD's NDR was presented. The unique multiple-gate capacity of the 2-D MESFET was used to demonstrate the compact NAND and NOR gates by using only one driving device and one load device. Finally, optimized device simulations showing significantly lower power performance were presented and potential applications were discussed.

ACKNOWLEDGMENTS

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Independent Control of Electron Density and Spatial Electron Distribution of Wire Gate Quantum Wire

R. Yang, and P. P. Ruden

Department of Electrical Engineering
University of Minnesota, Minneapolis, MN 55455

Introduction

There are several ways to form a dynamically one-dimensional electron system (quantum wire) in a semiconductor structure. Etched ridge, step, and V-groove structures have been proposed and successfully demonstrated[1-3]. In their simplest form, however, these structures do not allow for easy control of the electron density or its distribution. In recent years, a split gate on top of a semiconductor heterostructure such as AlGaAs/GaAs has been widely used to realize tunable one-dimensional electron systems[4-7]. In this structure, the formation of the quantum wire (channel) can be readily controlled by the split gate voltage which determines both the total electron density and its spatial distribution. More recently, a novel wire gate quantum wire structure has been proposed and demonstrated[8]. This device, which incorporates an additional narrow wire gate in the gap of a split gate, achieves excellent control and confinement of the one-dimensional electron system. Comparing it to the conventional split gate quantum wire, the additional wire gate voltage offers a new degree of freedom in adjusting the confinement potential profile and hence the energy level spacing, the electron density, and the effective width of the quantum wire. In this paper, we present results of self-consistent calculations of the electronic structure and of the electron density and its distribution for a wire gate quantum wire as functions of the two control voltages. We show that the split gate voltage and the wire gate voltage control in different ways the confinement potential profile of the induced electrons and therefore the energy level spacing, the effective wire width, and the total density of electrons in the wire. A schematic plot of our simulated structure, which corresponds to the device demonstrated in reference[8], is shown in Figure 1. It consists of an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ / GaAs heterostructure with an AlGaAs layer thickness of 35 nm. A δ -doped layer with doping concentration of $3.2 \times 10^{12} \text{ cm}^{-2}$ is incorporated into the AlGaAs and is located 20 nm from the AlGaAs / GaAs interface. The gap width of the split gate is 300 nm and the width of wire gate is 30 nm. Fabrication details pertinent to this wire gate quantum wire can be found in reference[8].

Theory

The self-consistent calculation of the electronic structure in the Hartree approximation requires the simultaneous solution of the coupled two-dimensional Schroedinger and Poisson equations. A finite element method with a nonuniform triangular mesh was employed in our calculations. A

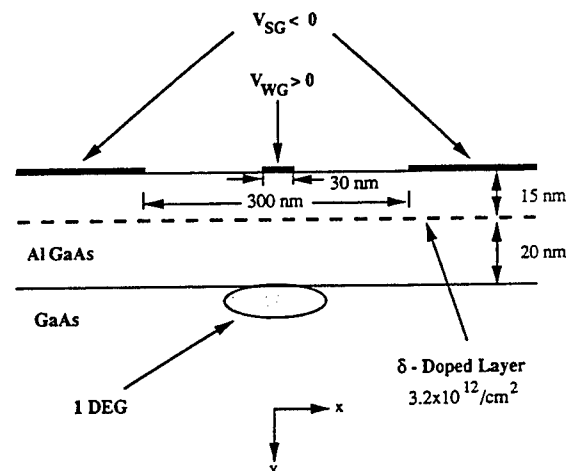


Figure 1: Schematic diagram of a wire gate quantum wire structure.

self-consistent semiclassical calculation in the Thomas-Fermi approximation is first carried out to determine the classical potential. Then the Schroedinger and Poisson equations are solved self-consistently using the semiclassical potential as a starting point. For a detailed description of the method, see reference[9].

A difficulty in executing this kind of calculation is that the boundary condition on the exposed III-V semiconductor surface between metal gates is not well understood. There are two simple limits for the surface potential. One is the assumption of a fixed uniform charge density at the exposed surface in narrow gate openings[10,11]. The other is the assumption of a constant surface potential determined by a pinned surface Fermi level[9]. The constant potential model overestimates the effective surface potential width in the gap while the fixed charge density model underestimates the effective surface potential width in the gap. Under conditions of low temperature operation, it is physically reasonable to expect the surface charge density to remain constant when the gate voltage is varied. We therefore adopted this as the appropriate model for the surface potential. However, for computational reasons we chose to model the surface potential by three constant segments with widths determined as follows.

Assuming a fixed surface charge density, the potential at the exposed surface of a single wire gate and of a single split gate were found by using the conformal mapping method[12]. The effective split gate separation and the effective wire gate width based on constant surface potential segments were then obtained by numerical integration of the surface potential requiring equal averages for the step-like and the continuous surface potentials. For the structure we discuss here, the effective split gate separation and the effective wire gate width were found to be 200 nm and 70 nm, respectively. These parameters were used in defining the surface potential boundary condition for all applied voltages.

Results and discussions

The self-consistently calculated energies for the first four subband minima are shown in Figure 2a as a function of the split gate voltage for a fixed wire gate voltage (V_{WG}

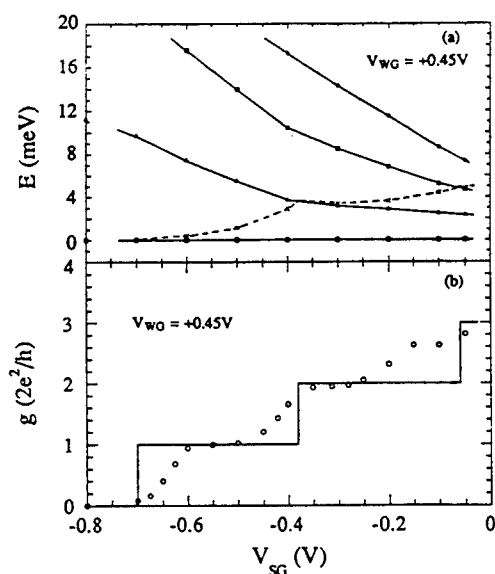


Figure 2: The four lowest subband energies, the Fermi energy, and the corresponding ballistic conductance as functions of the split gate voltage for a fixed wire gate voltage. Experimental data points ($T = 5K$) are shown as open circles.

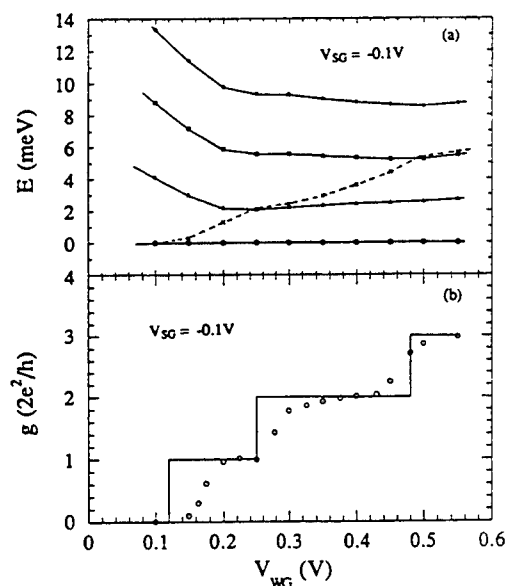


Figure 3: The four lowest subband energies, the Fermi energy, and the corresponding ballistic conductance as functions of the wire gate voltage for a fixed split gate voltage. Experimental data points ($T = 0.5K$) are shown as open circles.

$\approx +0.45V$). The split gate threshold voltage is found to be about $-0.7V$. The level spacings range from about 10 meV near threshold to about 2 meV in the split gate voltage range considered here. The decrease of the level spacings with the split gate voltage can be well explained by the fact that the increase of the electron density in the channel due to the less negative voltage applied to the split gate widens the confinement potential and hence the effective channel width. It therefore reduces the energy level spacing. Figure 2b shows the ballistic quantum conductance of the quantum wire which is derived from the corresponding electronic structure calculation (Figure 2a). Experimental results[8] measured at temperature $T = 5K$ are also plotted in Figure 2b. The discrepancy between the experiment and the calculated results can be attributed to the fact that the experiment was carried out at a relatively high temperature with significant thermal excitation of electrons while the calculation assumes zero temperature statistics. Therefore the conductance steps observed in the experiment are smoothed and the conductance value associated with each subband is slightly less than $2e^2/h$.

The calculated first four energy levels as a function of the wire gate voltage for a fixed split gate voltage ($V_{SG} = -0.1V$) are shown in Figure 3a. The variation of the level spacing with the wire gate voltage shows the control effect of the wire gate on the electronic structure of the channel. Figure 3b shows the corresponding ballistic conductance of the quantum wire. Experimental results[8] measured at a temperature of $0.5K$ are also plotted in the figure. One can clearly see the satisfactory agreement both for the threshold voltage and for the conductance plateau widths between our calculated results and the experimental data, which has more abrupt steps than the data shown in Fig 2b, due to the lower ambient temperature. In particular, we find good qualitative agreement in the non-uniformity of the step widths, which contrast markedly to those obtained with varying V_{SG} .

Due to the abrupt potential offset at the AlGaAs/GaAs interface, the electron density at the interface is not at its maximum value and the electrons have a distribution that extends to some depth into the GaAs layer. Figure 4 shows the calculated channel electron density along the x - (lateral) direction at several planes which are parallel to but have different distances from the AlGaAs/GaAs interface for a fixed split gate voltage ($V_{SG} = -0.1V$) and a fixed wire gate voltage ($V_{WG} = +0.3V$). As expected, the channel electron density at first increases with increasing distance from the interface, reaches its maximum near 4 nm and then decreases asymptotically to zero.

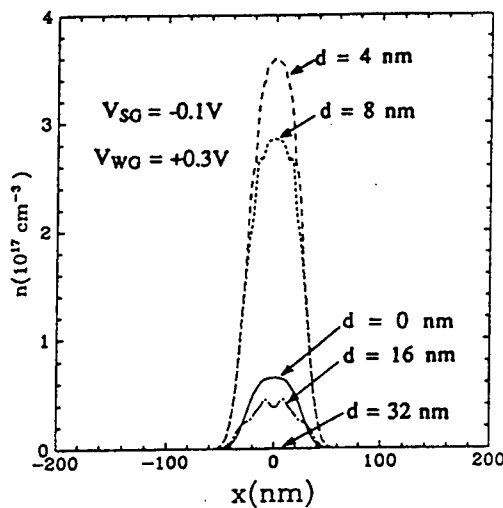


Figure 4: The channel electron density distribution at several planes parallel to the AlGaAs/GaAs interface on the GaAs side for a fixed split gate voltage and fixed wire gate voltage. d is the distance from the interface.

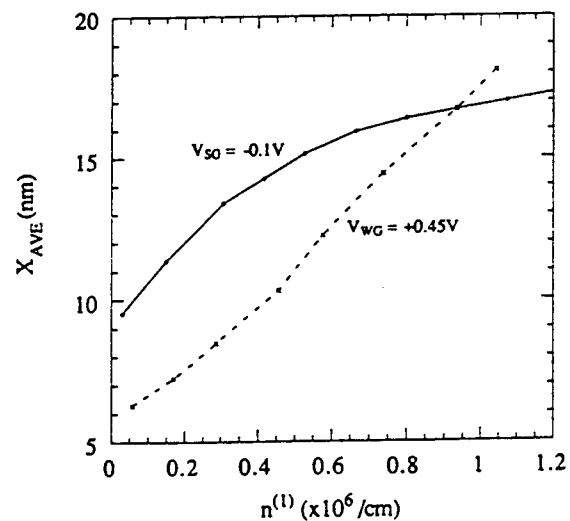


Figure 5: Average lateral channel half width of the electron distribution as function of the one-dimensional electron density in the channel. Solid line ($V_{SG} = -0.1V, V_{WG} = +0.1V \dots +0.55V$). Dashed line ($V_{WG} = +0.45V, V_{SG} = -0.7V \dots -0.05V$).

The calculated average channel half width, X_{AVE} , defined as the mean absolute distance of all quantum wire electrons from the center of the channel in the lateral direction, is plotted in Figure 5 as a function of the effective one-dimensional electron density $n^{(1)}$. The solid line is the result for a fixed split gate voltage and varied wire gate voltage. The dashed line corresponds to a fixed wire gate voltage and varied split gate voltage. The difference between the solid line and the dashed line reflects the different control effects on the channel electron distribution exercised by the wire gate and the split gate. In the range of effective one-dimensional channel electron density from 10^5 to 10^6 cm^{-1} , the average channel half width varies from about 7 nm to 18 nm for split gate control and from about 10 nm to 17 nm for wire gate control.

By judicious simultaneous adjustment of both split gate voltage and wire gate voltage, it is possible to vary the channel electron density without changing the effective channel width or to vary the effective channel width without changing the channel electron density as is shown in Figure 6. The differences between the constant X_{AVE} line and the constant $n^{(1)}$ line indicates the different control effects of wire gate and split gate voltages on the effective channel width and on the channel electron density. The split gate voltage has a noticeably stronger control effect than the wire gate voltage on the effective channel width while the wire gate voltage has a slightly stronger control effect than the split gate voltage on the electron density in the channel.

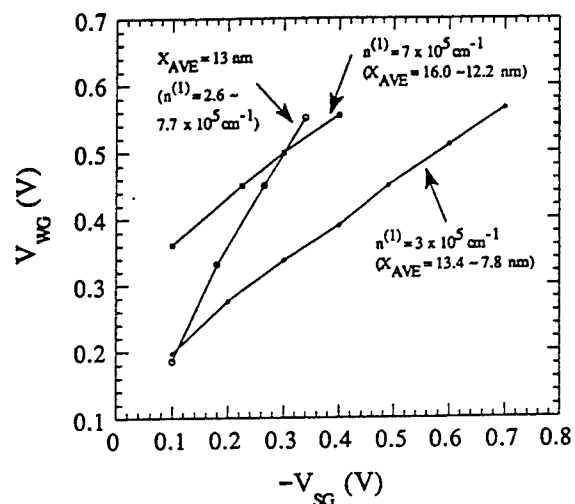


Figure 6: V_{WG} vs V_{SG} plots of constant channel half width and constant channel electron densities.

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Self-Consistent Simulation of Vertical Quantum Dot Structures with Residual Coulombic Impurities

P. Matagne, S. Nagaraja, V.Y. Thean and J.P Leburton
Beckman Institute, University of Illinois, Urbana, IL 61801

J. Destine and G. Cantraine
Institut Montefiore, Universite de Liege, B4000, Liege, Belgium

Abstract

Advances in nanostructure technology have enabled the fabrication of semiconductor devices with submicrometer feature sizes. At this small scale, electronic properties become relatively sensitive to Coulombic fluctuations arising from random doping and residual impurities present in the active region. In particular, in quantum dots with a small number of electrons, this effect is expected to affect significantly the quantized energy spectrum and charge localization.

In this paper, we present a model for calculation of the electronic properties of vertical quantum dots structures (fig1) in the presence of residual coulombic impurities[1]. We use a full 3D self-consistent Poisson-Schrödinger simulation to compute the quantized energy spectrum of the entire nanostructure encompassing the modulation doped region and the electron emitter (substrate). The structure is discretized using finite difference method with non uniform mesh, and Poisson & Schrödinger equations are iteratively solved, respectively by the conjugated gradient method and by a new iterative extraction orthogonalization method developed by our group[2]. The charge in the quantum dot is computed quantum mechanically with zero-dimension density of states while semi-classical Thomas-Fermi approximation is used in the bulk region. Exchange and correlation between electrons are treated by using the Kohn-Sham density functional method. The effect of residual impurities in the dot was simulated by adding self-consistently a Coulombic potential to the model.

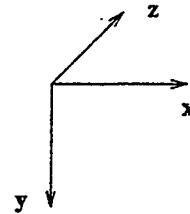
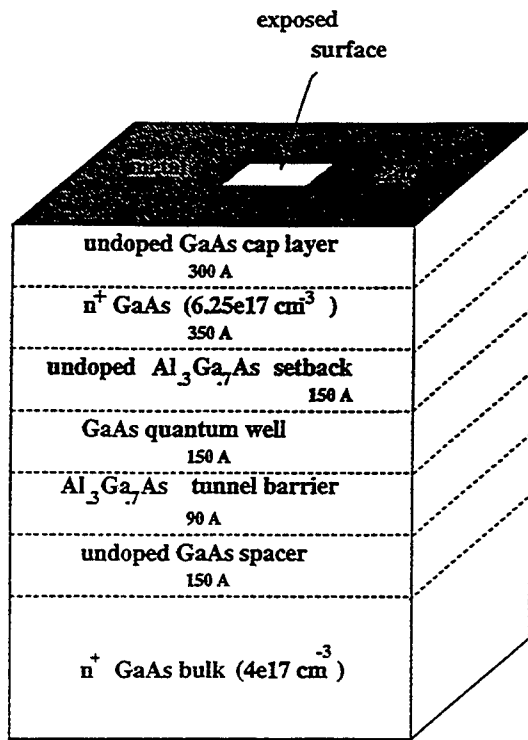
A comparison of the potential distribution, electron density, wave functions and eigenenergies with and without a residual positive coulombic center, is shown on figs 2 for a given gate polarisation. For remote impurity, the major effect is a lowering of the electrostatic potential in the dot which induces a shift in the energy spectrum and a displacement of the total electron charge toward the

positive impurity ion. At closer range, the influence of the coulombic potential is more dramatic, involving a mixing between coulombic and dot eigenstates (fig 2(f)) with a net electron charge on the impurity center (fig 2(e)). We have also simulated the effect of negative impurity and observed an opposite effect with a raising of the potential and a displacement of the charge away from the negative ion, as expected.

Finally, we have simulated single electron charging effect, related to the discrete nature of the electron charge, and discussed the influence of residual coulombic centers on the quantum dot capacitance.

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(a)

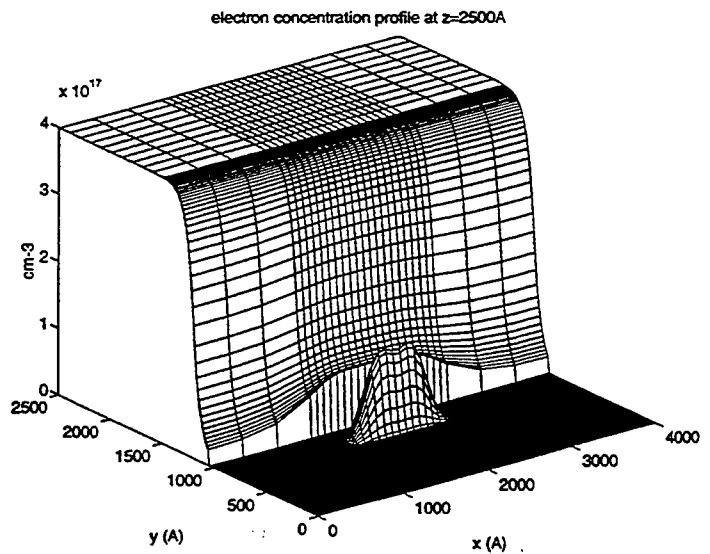
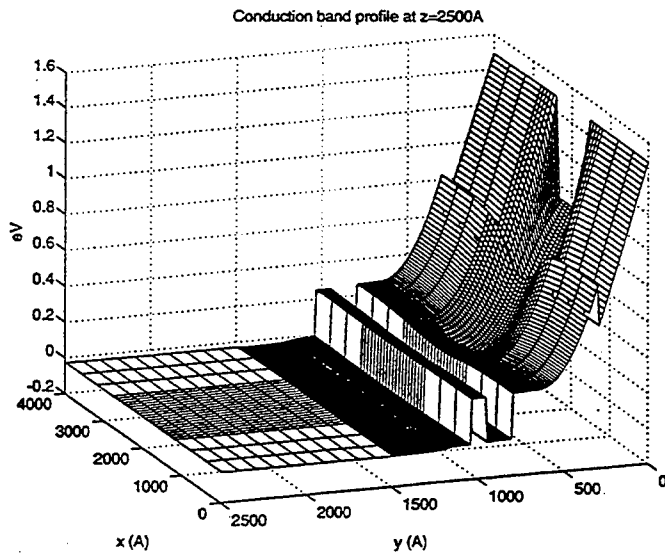


Figure 1: (a) Quantum dot structure with its different semiconductor layers. The dimensions are $4000\text{Å} \times 2500\text{Å} \times 5000\text{Å}$, the exposed surface is $800\text{Å} \times 1000\text{Å}$. (b) conduction band profile at $z=2500\text{Å}$ and (c) electron concentration profile for a gate bias of -0.56V (Fermi level = 0V). The origine of xyz axis is in the upper front right corner of (a).

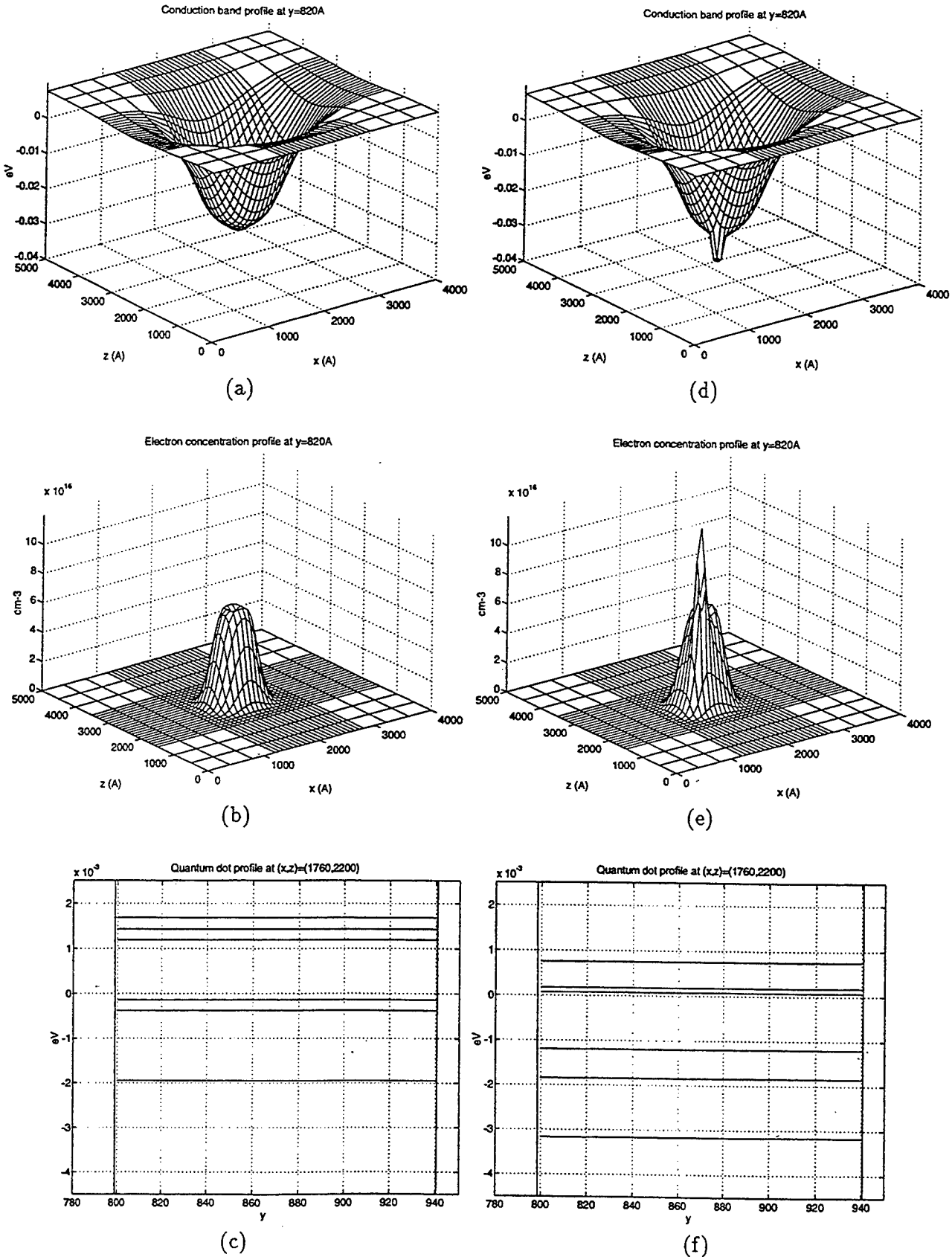


Figure 2: Conduction band, electron concentration, eigenenergies at $y=820\text{\AA}$ for a gate bias of -0.56V without (figs a,b,c) and with (figs d,e,f) the presence of a Coulombic center, situated in the quantum well at $x=240\text{\AA}$ and $z=300\text{\AA}$ from the center of the dot.

Piezoresistive Silicon Accelerometer Using Porous Silicon Etching Method and Bump Bonding Technique

Jun-Hwan Sim*, Sang-Ho Lee*, Jin-Sup Kim**, Jung-Hee Lee*, and Jong-Hyun Lee*

*School of Electronic & Electrical Eng., Kyungpook National University, Taegu, 702-701, South Korea

**Department of Electronics, Inje University, Kimhae, 621-749, South Korea

Recently, many kinds of silicon accelerometers using silicon micromachining techniques with both piezoresistive and capacitive sensing elements have been reported [1-2]. However, most of the development concerning silicon accelerometers has been performed on bulk micromachined elements. Conventional chemical etching methods have several drawbacks, such as the etch-stop control problem, limitations of microstructure directions and substrate orientations, and relatively long etch time (several hours). Silicon microstructures fabricated by anodization in aqueous HF solution have been reported [3-4]. However, it is found difficult to control the thickness of the air-gap and to define the exact shapes of the microstructures, because of undesirable side etching due to the isotropic anodic reaction.

In this research, a convenient technique, which overcome these difficulties, was suggested for the fabrication of well-defined microstructure. We first prepared a structure of n-epitaxial layer/patterned n⁺-diffused layer/n-substrate and then rendered the only n⁺-layer to become porous, which resulted in excellent control on defining the air-gap and the beam thickness, as well as the shape of the microstructure. The solder bump flip-chip mounting process [5] was adopted as the electrical connections of the accelerometer fabricated in this research. The main advantage of the bump bonding lies in cost reduction, increased reliability, high joint strength, ruggedness, and ability to make large numbers of bonds simultaneously.

A configuration of 4-beam bridge type piezoresistive accelerometer is shown Fig. 1. It consists of a loaded mass at the center of the structure, four beams supporting a mass, and four bump pads for electrical contact at the corner of the structure. The structural parameters are determined as $R=500\mu\text{m}$, $L=350\mu\text{m}$, $W=120\mu\text{m}$, and $T=5\mu\text{m}$, where R is the radius of the mass paddle (the region suspended by the four beams), L is the length of the beams, W and T are the width and thickness of the beams, respectively. The diameter of the bump paddle is 1.2mm and the overall size of the chip is 3.9mm \times 3.9mm.

The fabrication of the accelerometer started with 5-10 Ω -cm, phosphorus-doped (111) silicon wafer of $625\pm 25\mu\text{m}$ thickness. The n⁺ region, which serves as the sacrificial layer yielding the air-gap, was selectively formed by ion implantation with phosphorus (60 keV, $1\times 10^{16}\text{ cm}^{-2}$) and subsequent diffusion. The resultant n⁺-region should have a doping density higher than $5\times 10^{17}\text{ cm}^{-3}$ to be anodizable in the HF solution. A low-doped n-type epitaxial layer was then grown on the substrate. The thicknesses of the n⁺-diffused layer and the n-epitaxial layer were about $10\mu\text{m}$ and $5\mu\text{m}$, respectively. The piezoresistors were formed by boron ion implantation with a dose of $2.7\times 10^{14}\text{ cm}^{-2}$ at 40 keV and followed by an annealing at 1070°C for 70 minutes in N₂ atmosphere. The measured sheet resistance of the piezoresistor was approximately 240 Ω/\square . 1000Å thick passivation oxide was thermally grown and 1500Å thick LPCVD silicon nitride was deposited for stress-relief. To provide a masking layer for anodization, a 1000Å thick Ni-Cr adhesion and 6000Å thick Au were

sequentially deposited by e-beam evaporation. After Au/Ni-Cr masking layer was patterned by wet etching, the nitride layer was removed by plasma etching and the oxide was etched in BHF solution. N-epitaxial silicon layer was etched with Reactive Ion Etching to provide a pass for anodization. The Etch depth of the silicon was about $8\mu\text{m}$. Porous silicon was formed in selectively diffused n^+ region of $n/n^+/n$ silicon structure by anodic reaction in 12 wt% aqueous HF solution using voltage source (1.85V) at room temperature, and etched away in 5 wt% NaOH solution. After that, the Au/Ni-Cr masking layers were fully etched off. Surface and cross-sectional SEM views of the fabricated 4-beam microstructure of the accelerometer are shown in Fig. 2. Since anodic reaction does not occur with the low-doped n silicon substrate, the reaction stops automatically after complete conversion of the n^+ region to porous layer [6]. The side etching phenomenon of the microstructure thus does not occur, as shown in Fig. 2(b). The respective beam thickness and air-gap height exactly match the thicknesses of the $5\mu\text{m}$ thick epitaxial n -si layer and the $10\mu\text{m}$ diffused n^+ -layer, showing precise controllability on determining the the microstructures of the devices.

For the formation of bump pads and mass paddle, 1000\AA thick Ni-Cr and 6000\AA thick Au were sequentially deposited by e-beam evaporation. Lead-tin solder was then loaded simultaneously on the bump pads and mass paddle by dispensing Pb/Sn (Pb:Sn=37:63) solder paste. The die was heated. Hemispherical solder balls were formed on top of the Au/Ni-Cr pads as shown in Fig. 3. The loaded mass on the mass paddle weighed about 2.5mg.

Finally, the dies were placed face-down on a ceramic substrate. Temperature was increased, causing the solder to reflow, and the die was bonded directly to the interconnections on the substrate. Solder balls provide functions of both electrical interconnection and die attachment. This bump bonding can be adopted to a surface mounting on circuit boards for signal processing if necessary.

The characteristics of the fabricated devices were measured by an accelerometer calibration system with a high-precision reference accelerometer. The output response of the devices have measured from the full-bridge detection circuits and the voltage difference was amplified by a differential amplifier with gain of 120. The measured result in Fig. 4 shows the output response of the sensor in the acceleration range from 0 to 1.1g. The measured sensitivity is 0.04mV/g/V and the nonlinearity of the sensor is less than 0.8% of the full scale output. The result shows good linearity, although the measured range is limited to 1.1g due to our measurement set up. The measured frequency response in the range of $0\text{Hz}\sim 3.2\text{kHz}$ is shown in Fig. 5. The first resonant frequency was 1.4kHz, 7% higher value than the designed frequency. It was found that loaded mass error becomes the major source of the discrepancy between the estimated and the measured resonant frequency.

A piezoresistive silicon accelerometer using porous silicon etching method and bump bonding technique was fabricated and characterized. It was demonstrated that porous silicon etching method has made it possible to precisely define dimensions of the beam and the air-gap of the microstructure by controlling the thicknesses of the n -epitaxial and n^+ -diffusion layers of the $n/n^+/n$ structure, and also bump bonding technique is very attractive for the electrical connections of accelerometer in view of cost, density, and reliability, compared to wire bonding.

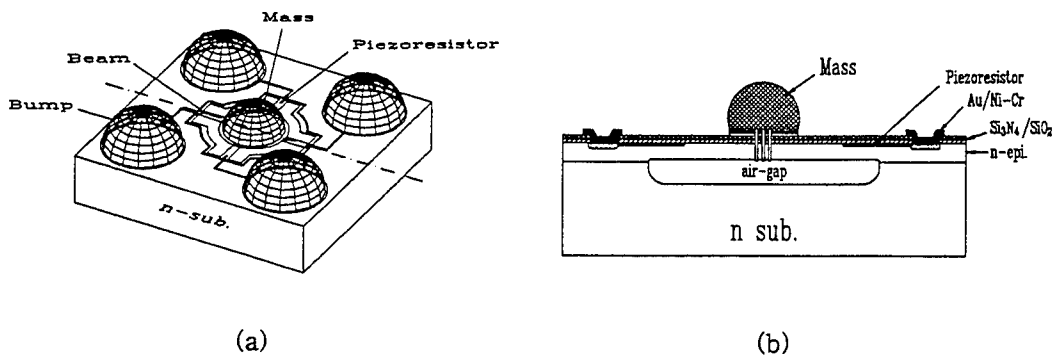


Fig. 1. Top and cross-sectional views of the accelerometer.

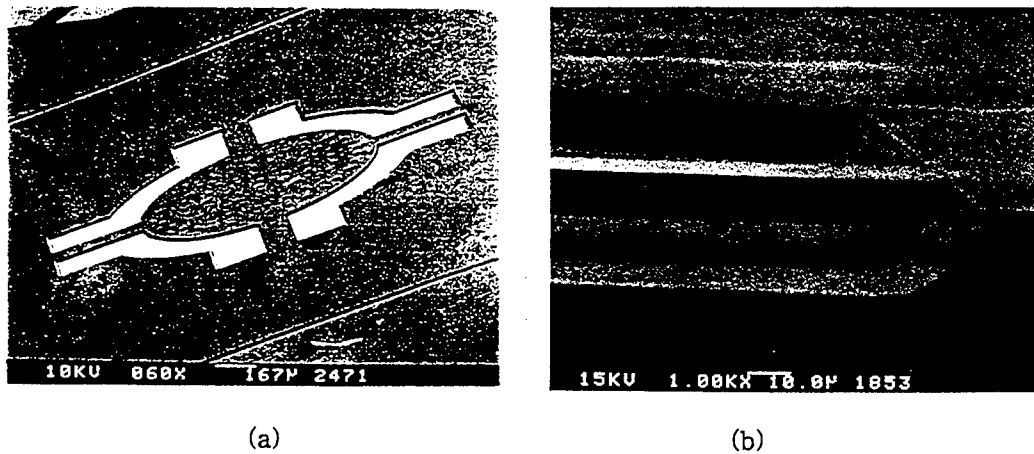


Fig. 2. Surface and cross-sectional SEM views of the microstructure.

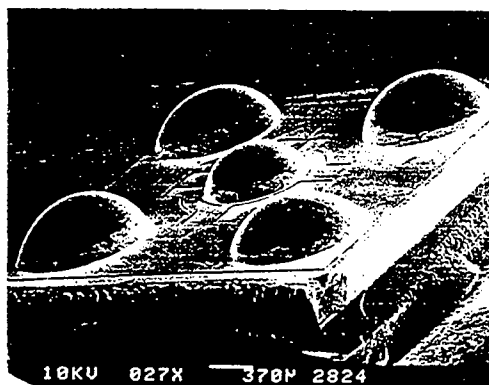


Fig. 3. SEM photograph of the loaded mass and bumps.

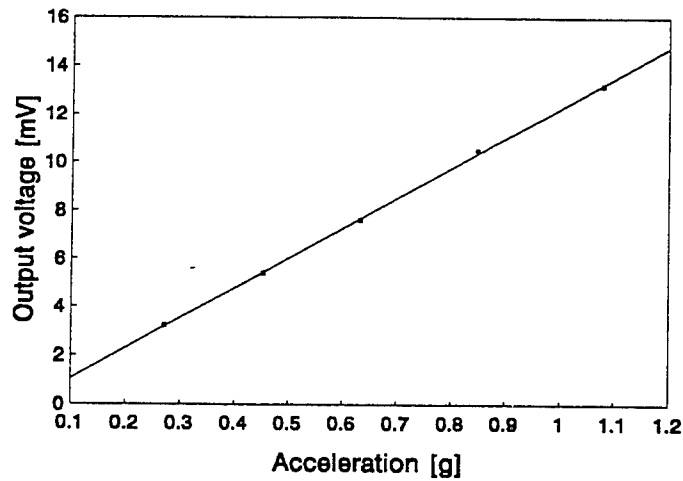


Fig. 4. The output voltage of the accelerometer.

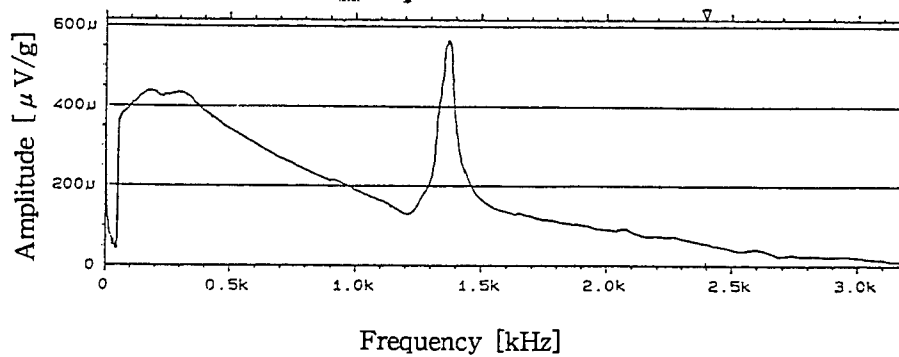


Fig. 5. The frequency response of the accelerometer.

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Polysilicon-micromachined optical devices

N. C. Tien, M. J. Daneman, M-H. Kiang, O. Solgaard[†], K. Y. Lau, and R. S. Muller

Department of Electrical Engineering and Computer Science
Berkeley Sensor & Actuator Center
University of California, Berkeley, CA 94720-1770.

Abstract- Actuated polysilicon surface-micromachined micromirrors for micro-optical systems on silicon have been designed and fabricated. Microhinge technology has been used to achieve the required vertical dimensions and functionality for these beam-steering mirrors. Both electrostatic comb-drives and impact-actuated linear vibromotors have been used to move the mirrors. The fabrication of these devices involves the surface-micromachining of up to four polysilicon layers. The mirrors are relatively insensitive to shock, vibration and temperature fluctuations and have been used in laser-to-fiber coupling and laser scanning applications.

I. INTRODUCTION

Advances in surface-micromachining technology offer a new approach to the development of micro-optical systems on silicon. We describe actuated polysilicon mirrors for optical-beam steering, a basic optical device used in many applications. For example, the mirror can be used for precise beam positioning in laser-to-fiber coupling, for low-loss optical switching, for external cavity lasers, or for laser scanning like that found in supermarket check-out counters, laser-light shows and displays.

The compatibility of the surface micromachined structures with VLSI fabrication techniques allow for the integration of control electronics on the same chip [1]. The combination of optical elements, actuators, and electronics on one chip will result in compact, high-performance, low-cost, "smart" optoelectronic modules.

For this "optical bench on a chip," movable high-aspect-ratio optical elements, such as mirrors and lenses [2,3,6] will be needed to interact with optical beams propagating parallel to the substrate surface. Because the diameters of collimated laser beams are greater than tens of microns (i.e. large compared to film thicknesses which are on the order of a micron or less in traditional surface-micromachining technology) an optical-beam steering mirror cannot be implemented without three-dimensional structures.

II. MOVABLE MICROMIRRORS

We describe polysilicon surface-micromachined mirror systems that can swing out from the surface and be linearly translated. To create these structures, while retaining the advantages of VLSI fabrication technology, we use polysilicon hinges [4] to connect the mirror to a movable platform. A mirror system with two degrees of freedom is shown in Fig. 1.

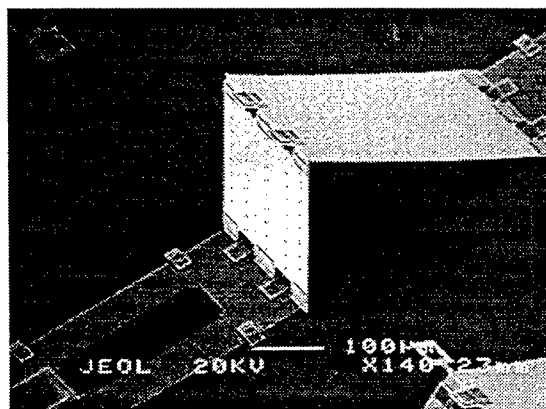


Fig. 1. A scanning-electron-microscope image of a folded-up micromirror.

[†]Now with the Department of Electrical and Computer Engineering, University of California, Davis, CA .

It is comprised of a 300 μm high by 200 μm wide mirror and a support plate between two sliders. Microhinges connect the slider to the bottom of the mirror, the top of the mirror at the top of the support plate, and the bottom of the support at the second slider. Linearly translating the sliders, which are guided by flanged polysilicon guides, toward each other, causes the mirror and support to fold-up and rise off the substrate. If the sliders are moved together in the same direction, the mirror is also translated without changing its tilt. If one slider is moved with respect to the other, the mirror angle is changed. An optical beam propagating parallel to the substrate and incident on the mirror at a 45 degree angle can be positioned horizontally by translating the mirror and simultaneously vertically by tilting the mirror.

A. Fabrication

The fabrication of the micromirrors is based on conventional polysilicon surface micromachining and uses three layers of structural polysilicon above a polysilicon ground plane. After deposition of sequential passivation layers of thermal silicon oxide and nitride, a 0.5 μm n^+ polysilicon ground plane is deposited and patterned. The first sacrificial layer of LPCVD phosphosilicate glass (PSG) is then deposited and patterned. Depressions are wet etched into the PSG using 5:1 hydrofluoric acid to create dimples under the mirror, sliders and back support (for reduced surface-to-surface contact). The dimples lessen stiction between these structures and the substrate. Next, the first structural polysilicon layer is deposited by LPCVD and patterned using a chlorine-based (Cl_2) plasma etch. This layer forms the mirror, sliders, back supports and comb drives. A second sacrificial layer is then deposited and patterned to allow the second polysilicon layer to be anchored to the substrate. The openings for the anchors were etched in fluorine-based (CF_4) plasma. After deposition, the second structural polysilicon layer is etched to form the guides for the sliders and the pins of the hinges. The third sacrificial layer and the third structural layer are then deposited and patterned to complete the hinge structures. The polysilicon structural layers are 2- μm thick, and the sacrificial oxide layers range from 1 to 2 μm in thickness. The sacrificial layers are removed through wet etching in hydrofluoric acid to release the movable structures. The last step is the evaporation of 50 nm of gold to increase mirror reflectivity. We measured a reflectivity of 85% at 1.3 μm . The reduction from the theoretical 96% reflectivity of a perfect gold mirror, is due to scattering caused by polysilicon surface roughness and by etch holes and dimples in the mirror.

B. Mechanical Properties

The mechanical characteristics of the mirror system such as its flatness, the precision of the motion and its integrity under environmental stresses are important factors in evaluating the mirror's performance. Curvature of the mirror due to stresses in the deposited polysilicon film is essentially eliminated by a 1050°C stress relief anneal [5]. The position accuracy of the mirror was measured by following a laser-beam that was bounced off the mirror as it was being tilted. A small deviation of less than 0.2 μm by the mirror from the expected straight line was found [2].

The mechanical integrity of the mirror under some environmental stresses was tested. To test the ability of the mirrors to withstand shocks caused by normal handling and operation, an unpackaged mirror was subjected to 500 g and 1000 g shock tests (three drops for each of the six axes) with only a slight movement (up to 2 μm) of the slider observed after the 1000 g test [2]. This was not unexpected as the extremely light masses of the mirrors (on the order of a few μgm) cause inertial forces to be extremely small. The friction is dominated by the adhesive forces between surfaces that are on the order of $\mu\text{N}/\mu\text{m}^2$.

Interferometric measurements were made to characterize the vibration and temperature sensitivity of the mirror [6]. An optical fiber was mounted onto the substrate in front of a raised micromirror so that the fiber face and the mirror formed a Fabry-Perot interferometer. Mirror movement could be measured with a resolution of at least 10 nm. The mirror appears to be fairly insensitive to vibrations up to 60 kHz. Temperature measurements between 25 and 200°C were made by placing the interferometer in a convection oven. The observed movement of the mirror is accounted for by the thermal expansion of the silicon substrate.

III. ACTUATION

Electrostatic actuators can be fabricated from common VLSI materials such as polysilicon and generally consume less power and are faster than thermal actuators. Surface-micromachined polysilicon resonators which are driven by interdigitated capacitors or electrostatic combs [7] can be used to move the mirrors. Though the range of motion is limited to

a few 10's of microns, the actuator can precisely position a mirror to within $0.2 \mu\text{m}$ [12] for a given dc bias or harmonically scan a mirror when an ac bias is applied.

Impact-actuated linear vibromotors have been developed [8-10] to move sliders along the chip surface over large distances (up to several hundred microns) with submicron resolution. The actuator consists of an electrostatic resonator with a rigid arm extending from it, which impacts a linear-motion slider and has been shown to be capable of moving the micromirrors [9]. As is shown in Fig. 2, the bottom of a $400 \mu\text{m}$ long mirror is hinged to the substrate while the top is hinged to a support arm which, in turn, is hinged to the slider of the actuator. The vibromotor moved the slider nearly $50 \mu\text{m}$, tilting the mirror 8 degrees. One feature of the linear vibromotor is that the actuator is only engaged with the slider during movement. Once disengaged, the adhesion forces between the slider and the substrate (stiction) tend to prevent movement.

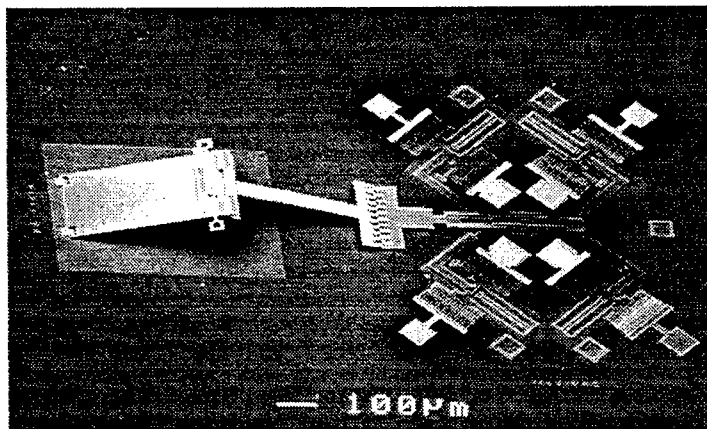


Fig. 2. A scanning-electron-microscope image of the linear vibromotor-driven mirror.

IV. APPLICATIONS

A. Laser-to-fiber coupling module

A micromirror of the type shown in Fig. 1 was incorporated into a laser-to-fiber coupling module, an example of which is shown in Fig. 3, and used to improve the optical alignment so that a coupling efficiency of 40% has been repeatedly achieved [11]. A semiconductor laser, aspheric lens and an optical fiber were positioned on a chip using standard silicon-optical-bench (SOB) techniques. The mirror is used to compensate for the inaccuracies inherent in the SOB technology which limit the coupling efficiencies to 5-10%.

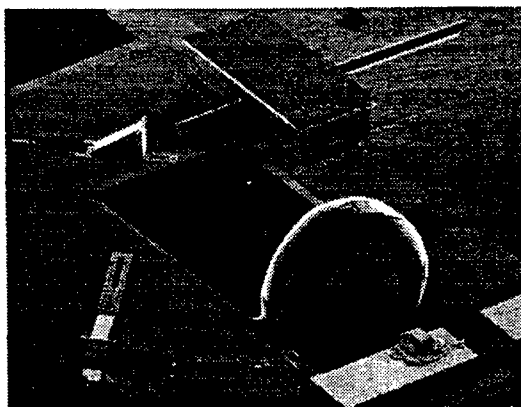


Fig. 3. Integrated laser-to-fiber coupling chip with a movable micromirror.

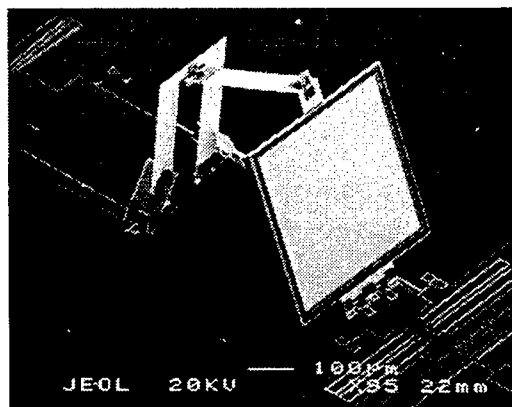


Fig. 4. Scanner for off-chip beam positioning.

B. Scanners and External Cavity Lasers

The structure shown in Fig. 4 was designed to be the external mirror of an external cavity

laser. In this structure, the bottom of both the mirror and the support are attached to electrostatic comb-drive actuators [12]. The mirror measures 500 by 500 μm , and the comb drives have maximum displacements of 15 μm , corresponding to a maximum angle variation of 3 degrees. The mirror angle can be controlled in a dc fashion for laser-beam positioning or the mirror can be driven harmonically for laser scanning. The measured precision of the mirror movement is better than 0.2 μm resulting in an angular accuracy of 0.02 degree. We have made mirrors with up to 20 degrees of angular range of motion.

V. CONCLUSION

We have designed and fabricated movable micromirrors based on polysilicon microhinge technology. The micromirrors have the mechanical functionality, vertical height and area required for optical beam-steering. These mirrors can be used in on-chip beam positioning as part of a micro-optical system or for off-chip laser-beam scanning. The stability of the micromirrors is sufficient under stresses imposed by temperature changes, vibration, and shock. Successful production of these hinged mirrors will lead to low-cost, batch-assembled, high-performance optoelectronic systems for a wide variety of applications.

ACKNOWLEDGMENT

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THERMALLY BASED SYSTEMS IN CMOS TECHNOLOGY

Erno H. Klaassen, Richard J. Reay, Gregory T.A. Kovacs
Center for Integrated Systems
CIS 130, Stanford, CA 94305-4070
Tel: 415.725.3637 Fax: 415.725.6278

INTRODUCTION

Single crystal silicon is very thermally conductive. At 1.57 W/cm·K its thermal conductivity is close to that of aluminum (2.36 W/cm·K). This high conductivity is beneficial for integrated circuitry, since it allows for efficient heat dissipation away from circuits through the substrate into the package. There are applications, however, where it is necessary to create and/or detect small, very localized changes in temperature at the surface of an integrated circuit, using as little power as possible. In these cases, the selective removal of portions of silicon substrate allows for the fabrication of microstructures with high thermal isolation.

Several specialized processes have been developed for the fabrication of thermally isolated structures [1, 2, 3]. The many departures from standard circuit processing steps, however, limit the versatility of these techniques. A different approach is to perform post-process micromachining steps on otherwise unmodified circuit processes, preferably without the need for additional masking steps. With this technique, any appropriate foundry or in-house IC process can yield a variety of electro-thermal devices. Since the process is optimized for circuitry, signal amplification, filtering, buffering, and a variety of other electronic processing can be done on chip, yielding a fully integrated system.

One of these post-processing methods allows for etching away silicon underneath dielectrics in standard CMOS processes [4]. Using this technique, it is possible to fabricate thermally isolated polysilicon heaters and thin film thermopiles, using the interconnect layers available in the IC process. These can be combined to make micro hot-plates [5], IR detectors [6], flow sensors [7], power sensors [8], and a variety of other devices.

The limitation of undercutting dielectrics is that all the silicon underneath the cantilever or hot-plate is removed. The only devices that can be thermally isolated are those built with interconnect layers, which are typically limited to aluminum and polysilicon. In order to extend the capabilities of CMOS post-process micromachining, a technique was developed to provide thermally isolated regions of silicon, supported by dielectric beams over cavities etched in the substrate [9]. The method requires no modifications to the circuits process, and no extra masks are necessary.

FABRICATION

Figure 1 shows a cross section of the undercutting process. Fig. 1(a) shows a cross section of a typical thermo-element at the end of a CMOS process. Regions of silicon substrate are exposed by superimposing the device active, diffusion contact, intermetal via, and overglass via layers in the chip layout. The field oxide and other interlevel dielectrics then form a masking layer for the subsequent

silicon etch. Since the bondpads are exposed during the silicon etch, it is necessary to use a silicon etchant that is selective to aluminum, as well as the oxide masking layer. We use tetramethyl ammonium hydroxide (TMAH), which has very good selectivity to oxide, and does not attack aluminum when doped with the appropriate amount of dissolved silicon [10].

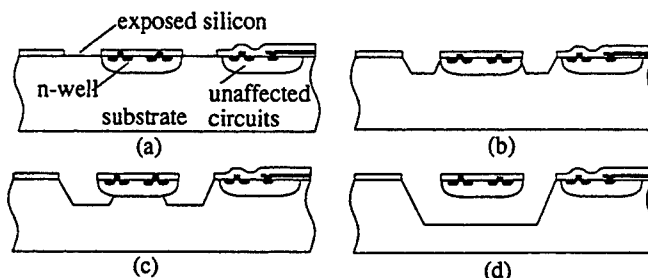


Figure 1: Cross section of silicon undercutting process. (a) After completion of standard CMOS process. (b) and (c) The p-type silicon is etched while the n-well is passivated by an electrochemical etch stop. (d) Thermally isolated circuitry suspended over an etched cavity.

The silicon n-well is passivated by an electrochemical etch stop. A potentiostat is used to maintain the potential of the n-wells at -0.8 V and the p-substrate at -1.5V, relative to an Ag / AgCl electrode in solution, by driving a platinum counter electrode. The final structure is a region of single crystal silicon suspended by dielectric beams. Electrical connection to devices in the n-well is provided by aluminum interconnect traces inside the beams. This technique allows for the thermal isolation of a wide range of devices. In the Mosis 2.0 μm analog CMOS process used for building our systems, these devices include not only the polysilicon resistors and thermocouples that are possible with dielectric undercutting, but also PMOS transistors, NPN bipolar transistors, PN diodes, and diffused resistors. The oxide support beams provide high thermal isolation, since the oxide has a low thermal conductivity (0.014 W/cm·K for thermal oxide) and the aluminum traces are minimum width (3 μm).

THERMALLY BASED SYSTEMS

A wide range of thermally based measurement systems are made possible by using thermally isolated structures. These include flow sensors, power or root-mean-square (RMS) sensors, vacuum sensors, and infrared detectors. We are exploring the applications of thermal vacuum and RMS measurement. The latter will be described below.

The high thermal isolation of these devices (routinely 30,000 K/W to 60,000 K/W in air) also makes

it possible to regulate the temperature of the silicon at the tip of the support beams with very little power. An application based on this is a low-power temperature-regulated bandgap reference, which will also be described below. All these systems take advantage of the fact that the process used is optimized for analog circuits; circuits are integrated with the undercut microstructures.

THERMAL AC TO RMS CONVERTER

The expression for RMS voltage is

$$v_{RMS} = \sqrt{v_{AC}^2} \quad (1)$$

Measuring this value for an AC waveform is important for applications such as oscillator leveling, automatic gain control, and AC signal measurement. The most common method for measuring the magnitude of AC signals is precision rectification and filtering, which yields the average value of a waveform. This yields only a relative measure of RMS, and only for a sinusoidal signal.

Measuring true RMS is very desirable for general-purpose measurements. One common method for obtaining true RMS is through analog computational techniques. While these methods are widely employed in hand-held measurement equipment, bandwidths are limited to several megahertz, and depend strongly on the magnitude of the input signal.

Due to the wide bandwidths attainable, the thermal domain has long been used for the determination of the RMS value of AC signals [11, 12, 13]. Our integrated thermal converter uses polysilicon resistors as heaters and diodes as temperature sensors [14]. The heater and sensor are located at the tip of two dielectric support beams. The fabricated thermoelements were designed with several different beam lengths, ranging from 85 μm to 225 μm , and have a measured thermal resistance (in air) of up to 37,000 K/W. The suspended diodes have a measured temperature sensitivity of -2mV/K .

The feedback topology used to obtain the RMS value of the input signal is shown in Fig. 2. The negative feedback constrains the forward voltages of the two diodes to be equal. One can therefore write,

$$V_{dd} - V_{d1} + S_1 \cdot \overline{(V_{in}^2)} = V_{dd} - V_{d2} + S_2 \cdot (V_o^2) \quad (2)$$

where S_1 and S_2 are the thermal sensitivities (a function of

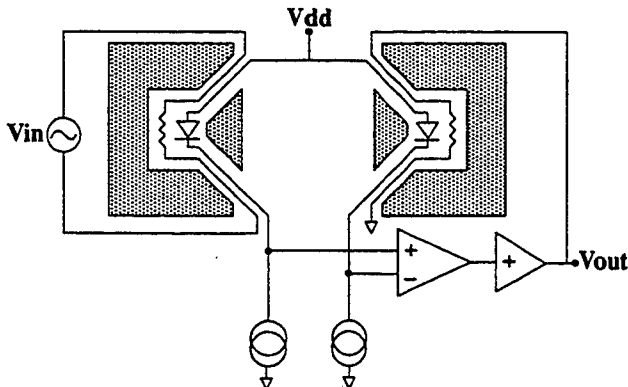


Figure 2: Feedback topology used in the RMS converter.

thermal efficiency of the elements and electrical resistance of the heater), and V_{d1} and V_{d2} are the forward diode drops with no signal applied to the polysilicon resistors. Since these forward drops are equal, or can be set equal by adjusting the bias currents, and the thermal efficiencies are equal due to the excellent matching of the diode temperature sensitivity and the geometry of the devices, the expression simplifies to the definition of RMS. The averaging operation in Eqn. 2 is due to the thermal pole of the input thermoelement.

The amplifier shown in Fig. 2 is implemented as an integrated folded cascode CMOS operational amplifier, in combination with a source follower / emitter follower buffer. The output stage is capable of driving the load with currents in excess of 50 mA, which is more than sufficient to realize the upper end of the dynamic range of the thermoelements. The quiescent power consumption of the amplifier is 950 μW .

The -3 dB frequency of the RMS converter was measured to be 415 MHz. This is limited primarily by the 20 nH parasitic inductance of the bondwires going to the heating resistor. Better packaging or the use of multiple parallel bondwires is expected to increase the bandwidth of the RMS converter even further, potentially up to the gigahertz range.

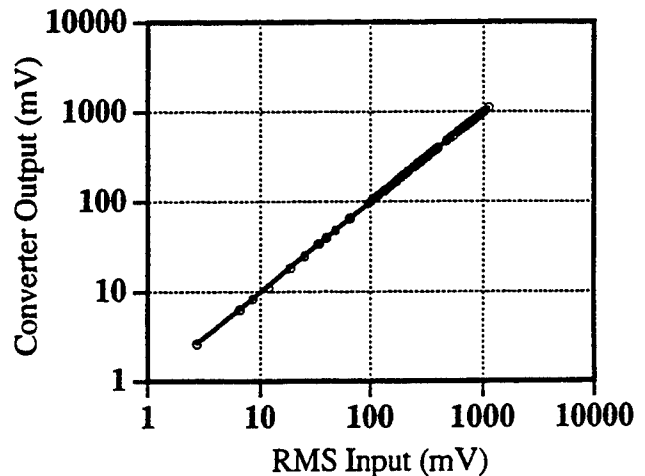


Figure 3: RMS converter measured transfer function.

A plot of input RMS versus output voltage for a sinusoidal input signal of 1 kHz is shown in Fig. 3. The dynamic range of the RMS converter system covers 2.4 mV to 1.1 V (53 dB). The measured nonlinearity of the converter is better than 1%, and settling times (2%) are on the order of 20 ms for maximum signal excursions. The entire converter, including both thermoelements and the buffered amplifier, occupies an area of 400 μm by 400 μm . The converter can be readily implemented with other CMOS circuitry, such as data converters or RF circuits. Since the input heating resistor is electrically floating, it can be referenced to an RF ground, which can be offset from the analog ground of the measurement system.

Fig. 4 shows a scanning electron micrograph of the complete RMS converter system. The folded cascode amplifier and output buffer are visible at the right. The

oxide beam length of the thermoelements in this picture is 85 μm .

Figure 5 shows a closeup view of one of the thermoelements of an RMS converter. The polysilicon heater is visible at the tip of the element.

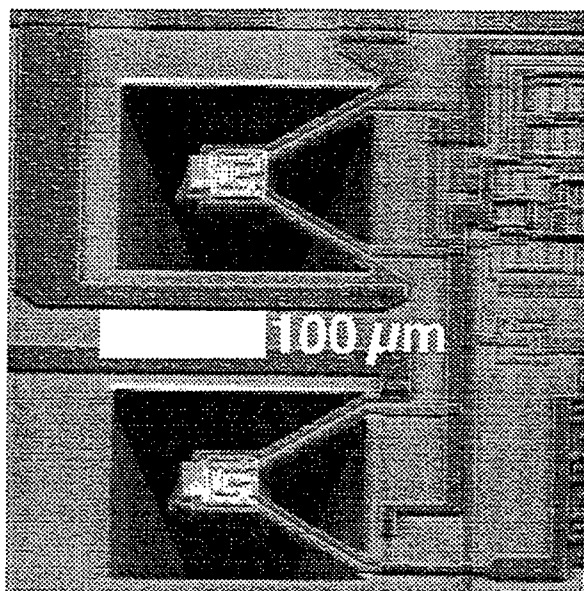


Figure 4: SEM of the Integrated RMS Converter System

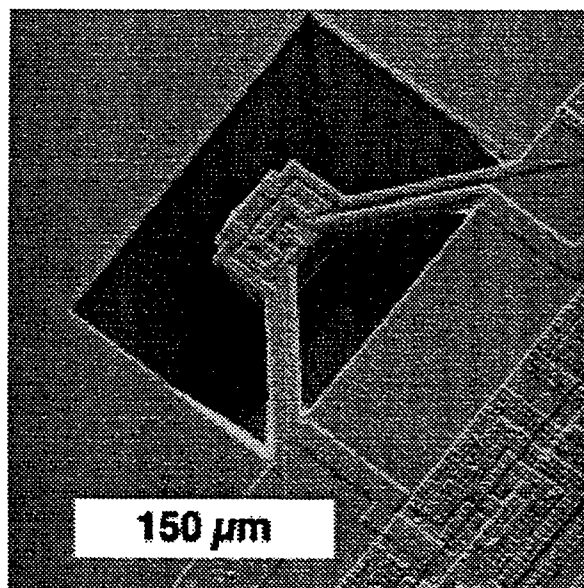


Figure 5: SEM showing a close-up view of an RMS converter thermoelement.

MICROMACHINED BANDGAP REFERENCE

One of the other applications of thermally isolated single crystal silicon is to build circuits that can be regulated at a constant temperature with very little power. A type of circuit that benefits from temperature regulation is the voltage reference. Voltage references provide a fixed output voltage that is designed to vary as little as possible with ambient temperature. Even the best voltage references still exhibit a certain amount of output voltage drift with temperature. To further improve the temperature stability, the reference can be maintained at a fixed temperature.

This has been implemented in the past by heating the entire substrate of a reference chip. While this has provided references with very low drift (tenths of parts-per-million per degree) [15] the main drawbacks are high power dissipation (several hundreds of mW) due to low thermal resistance and the slow warm-up time (several seconds) due to large thermal capacitances.

Both these drawbacks were eliminated by using the electrochemical etch technique described above to realize a thermally isolated bandgap voltage reference by creating a suspended reference core through underetching n-wells in a CMOS process [16]. A schematic of the bandgap circuit is shown in Fig. 6. The shaded areas indicate devices inside thermally isolated n-wells. The ratio of the transistor emitter areas is 2:1, which was chosen to limit the area of the devices. A servo amplifier adjusts the reference voltage such that the currents in the two branches of the Brokaw cell are equal, thus generating the bandgap voltage output given by

$$V_{ref} = V_{be1} + 2 \cdot \frac{R_1}{R_2} \cdot V_T \cdot \ln(2) \quad (3)$$

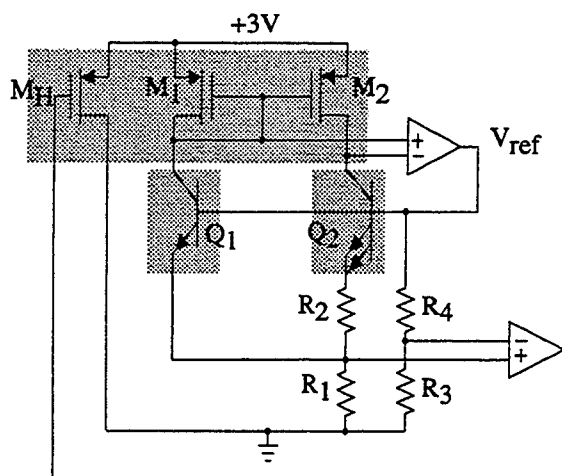


Figure 6: Schematic of the bandgap reference. The shaded areas indicate thermally isolated devices. R_1 and R_2 are implemented as polysilicon resistors on the suspended element

The two resistors, R_1 (5.9k Ω) and R_2 (360 Ω) are constructed in polysilicon, and laid out in unit cells for optimal matching.

A PMOS transistor connected between the positive supply and ground functions as a voltage-controlled heater. A transistor was chosen over a diffused resistor to improve the overall power efficiency. With a heating transistor, all of the power is delivered to the element, while the transistor driving a heating resistor would dissipate a significant amount of wasted power. Since the total current in a Brokaw cell is proportional to absolute temperature (PTAT), the voltage across the lower resistor R_1 is used as a temperature signal. This voltage is servoed to a nominally constant reference voltage, which is a the bandgap output, scaled by the voltage divider formed by R_3 and R_4 .

Fig. 7 shows an SEM of an etched bandgap reference. The thermal resistance of the micromachined bandgap reference was measured to be 53,000 °C/W. A typical heated-substrate reference has a package resistance of 200 °C/W. The higher isolation is due to the excellent insulation properties of the thin support beams. The thermal time constant of the structure was measured to be 2.5 ms which is two orders of magnitude faster than previous heated references. These characteristics lead to significant reductions in heater power and warm-up time.

The output voltage drift was measured from 0°C to 80°C with the heater off and with the heater regulating the temperature at 90°C. The unregulated temperature coefficient was 400 ppm/°C. With closed loop temperature control, the temperature coefficient dropped to 9 ppm/°C. The remaining temperature drift is most likely due to small thermal gradients across critical devices. Further study into reducing the effects of these gradients is currently under way.

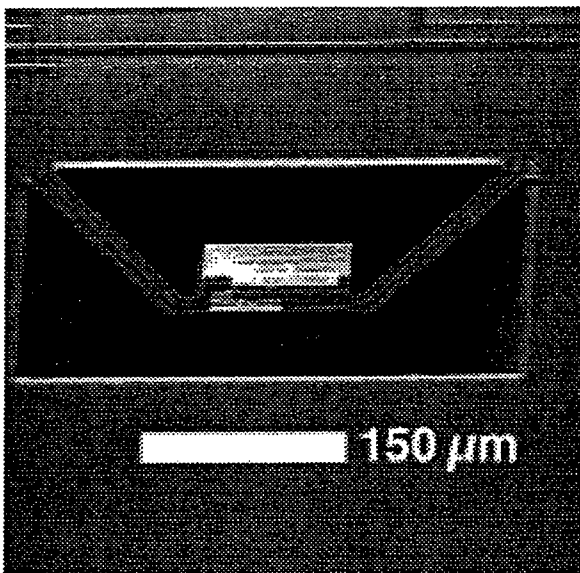


Figure 7: SEM of a micromachined bandgap reference.

A concern with a suspended device such as the RMS converter and the bandgap reference is that they might break due to a mechanical shock. The silicon at the tip of the bandgap reference weighs only 0.15 micrograms, however, so the 3.1 μm thick oxide beams are strong enough to make the device quite robust. Several devices were tested on a shock tester and exposed to shocks of up to 1500 g (150 μs half-magnitude duration), which did not produce any electrically or visually observable adverse effects. This level of shock tolerance meets military specifications (MIL-STD-883, Method 2002), and is sufficient for normal handling.

CONCLUSION AND OUTLOOK

We have demonstrated a new method for the fabrication of thermally isolated single crystal silicon structures in a completely unmodified CMOS process. Different types of devices can be integrated on this thermally isolated silicon, making it possible to create circuitry that is separated from the silicon substrate by an etched cavity.

Since the technique requires no extra masking steps, and the equipment necessary for the postprocessing step is inexpensive, these types of devices are within the capabilities of anyone with access to an industrial or foundry CMOS process. Since amplification and control circuitry is readily integrated with the microstructures, fully monolithic systems can be realized.

Our future work will focus on improving the performance of the RMS converter and the bandgap reference, and the realization of a thermal conductivity vacuum sensor.

ACKNOWLEDGMENTS

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A μ -MAGNETOMETER BASED ON ELECTRON TUNNELING

L.M. Miller, J.A. Podosek, E. Kruglick,
Center for Space Microelectronics Technology, Jet Propulsion Laboratory,
California Institute of Technology, Pasadena, CA

T.W. Kenny
Department of Mechanical Engineering,
Stanford University, Stanford, CA

J.A. Kovacich
Eaton Corporation
Milwaukee, WI

W.J. Kaiser
Electrical Engineering Department
University of California, Los Angeles
Los Angeles CA

To produce miniaturized, low power sensors without loss of sensitivity, novel transducer technologies are often necessary. This is the case with the development of miniature, highly sensitive magnetometers. Although SQUID technology provides the most sensitive measurement, SQUIDs also require additional power for cooling. In this paper, the development of a μ -magnetometer based on electron tunneling is described. Electron tunneling provides $\text{m}\text{\AA}$ sensitivity to displacement while requiring very small active areas. The purpose of this work is to develop a 3-axis magnetometer which can be integrated into a micro-spacecraft to measure magnetic fields on the order of a nT. The magnetometer must be small and require very little power. For dual-use purposes, the magnetometer must also be inexpensive, reliable, insensitive to temperature variations, and provide a wide dynamic range. The tunneling μ -magnetometer offers a unique combination of advantages including high sensitivity ($\sim 10^{-9}$ Tesla), vector sensitivity, wide bandwidth (> 10 kHz), low power (< 100 mW), small size (4mm X 4mm X 0.6mm), robustness, wide dynamic range (> 100 dB), and small temperature coefficients.

Prototype devices have been designed, fabricated using bulk micromachining techniques, and characterized. A cross-section of the tunneling μ -magnetometer is shown schematically in Figure 1. The device consists of two silicon components: 1) a silicon substrate which supports an electron tunneling tip and a deflection electrode, and 2) a membrane which supports a counter deflection electrode and a coil of wire on either side of the membrane. A scanning electron micrograph of a typical electron tunneling tip is shown in Figure 2. The electron tip is ~ 30 μm high and is micromachined in the center of a 3.5 mm X 3.5 mm well.

The principle of operation of the tunneling μ -magnetometer is based on a Lorentz force measurement. The wire coil supported by the membrane is positioned such that the wire segments supported by the membrane are straight line segments. A current through

the wire coil produces a Lorentz force F which is proportional to $nLIB\sin\theta$, where n is the number of loops in the coil, L is the length of the wire segment supported by the membrane, I is the bias current through the wire coil, B is the magnetic field, and θ is the angle between the magnetic field vector and the wire segments. This force is monitored by the electron tunneling transducer which is capable of detecting $\text{m}\text{\AA}$ of deflection. The bias current frequency can be adjusted for operation at ~ 1 kHz where the $1/f$ noise, inherent in the tunneling transducer, is reduced. The electronics which drive the tunneling transducer are shown in Figure 3. A feedback loop is closed around the electron tunneling tip and deflection electrodes to produce a force-rebalance mechanism. Therefore, once the membrane is brought to within the proper distance for electron tunneling to occur ($\sim 10\text{\AA}$), the membrane does not move. The output of the comparator is the Lorentz force measurement. Wide bandwidth (>10 kHz) and wide dynamic range (>100 dB) are typical in this tunneling transducer design.

A prototype tunneling μ -magnetometer has been fabricated and characterized. Linear response to both increasing magnetic field and to drive current have been demonstrated and are shown in Figures 4 and 5, respectively. In these figures, V_t is the electron tunneling voltage monitored at the output of the comparator as described above. Minimum detectable magnetic fields in these devices have been measured at $\sim 8\mu\text{T}/\sqrt{\text{Hz}}$ for a single wire coil ($n=1$) and a bias of 10 mA at 200 Hz. This is within a factor of 2 of the theoretical value for this structure. Development of optimized structures are underway to increase sensitivity to the $\text{nT}/\sqrt{\text{Hz}}$ range, to improve device packaging and to demonstrate flight readiness.

The research described in this paper was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was jointly sponsored by Eaton Corporation and the National Aeronautics and Space Administration, Office of Space Access and Technology.

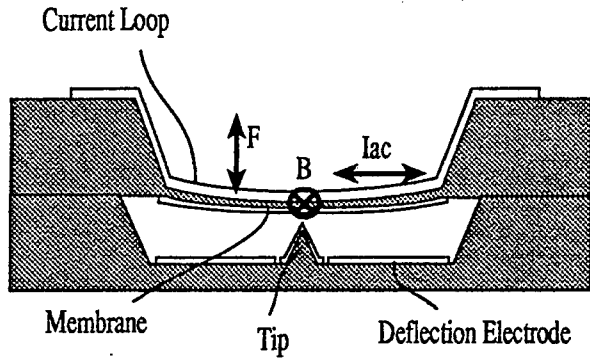


Figure 1. Schematic of electron tunneling μ -magnetometer. A magnetic field, B , perpendicular to the current, I_{ac} , produces a Lorentz force, F , which is monitored by the electron tunneling transducer.

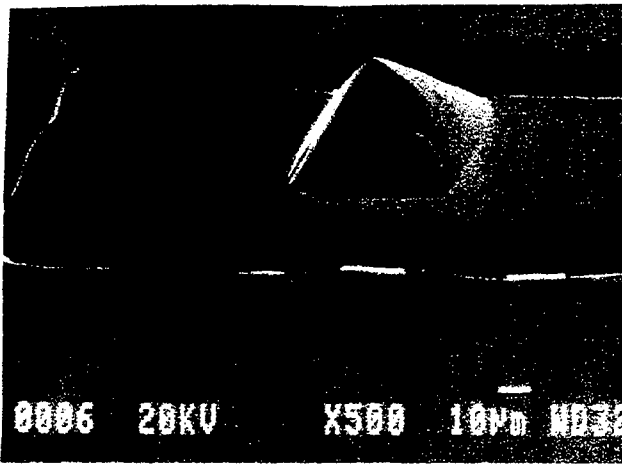


Figure 2. Scanning electron micrograph of a bulk silicon micromachined electron tunneling tip used in the design of the tunneling μ -magnetometer

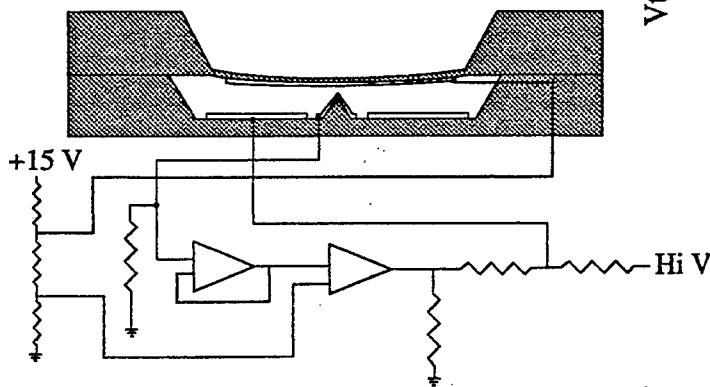


Figure 3. Feedback control loop for the electron tunneling transducer.

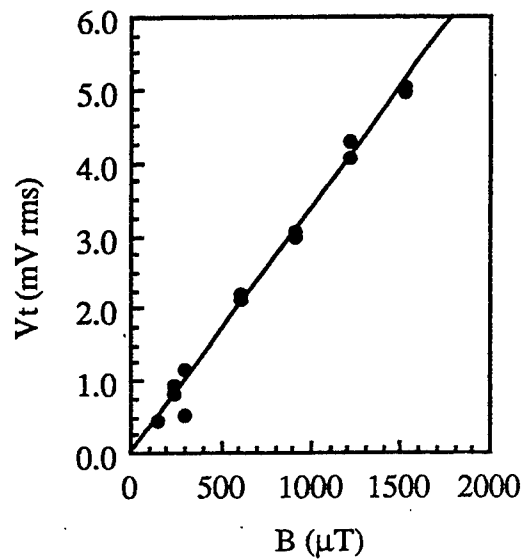


Figure 4. Tunneling μ -magnetometer response to increasing magnetic field. Bias current in the device is 10 mA at 200 Hz.

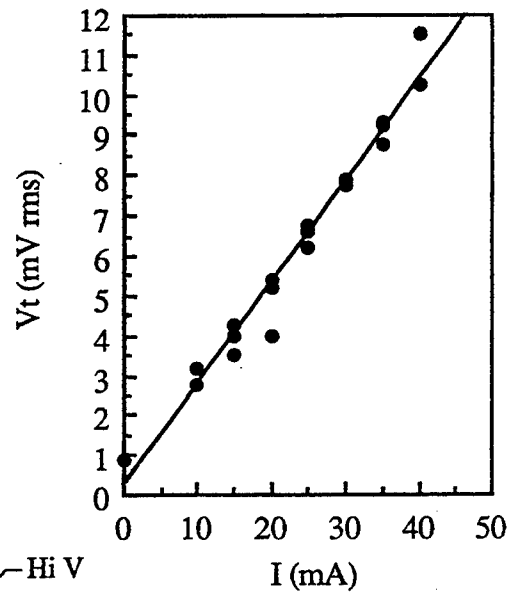


Figure 5. Tunneling μ -magnetometer response to increasing bias current. The magnetic field is ~ 1.5 mT at 50 Hz.

DESIGN AND FABRICATION OF A THERMALLY ACTUATED SILICON MICROPUMP

Chang-Qing ZHAN and Tai-chin LO

*Department of Electrical and Electronic Engineering,
The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong*

Li-Tian LIU and Pei-Hsin TSIEN

Institute of Microelectronics, Tsinghua University, Beijing 100084, P.R. China

Abstract

A membrane micropump with integrated driving component based on bi-metal structure was first fabricated using advanced silicon micro-machining techniques. The processings and materials used were fully compatible to standard VLSI fabrication technology. The micropump consists of three silicon chips which form two passive check valves and a pump membrane. The outer dimensions of the micropump was $6 \times 6 \times 1 \text{ mm}^3$. The membrane itself has an area of $4 \times 4 \text{ mm}^2$ at a thickness of $20 \text{ }\mu\text{m}$. The orifice size of the valves is $400 \times 400 \text{ }\mu\text{m}^2$. The movable flaps have a size of $1 \text{ mm} \times 1 \text{ mm} \times 10 \text{ }\mu\text{m}$. The volume stroke of the membrane is in the range between $0.4 \text{ }\mu\text{l}$ and $0.7 \text{ }\mu\text{l}$. A pumping yield of $40 \text{ }\mu\text{l} / \text{min}$ was measured with a pumping frequency of 1 Hz and driving voltage of 10V. At present the performance of our micropump is similar to micro pumps developed previously, but operating at much lower driving voltage.

I. INTRODUCTION :

Among membrane micropumps developed so far, the driving component is the most important part to be addressed. Signal conversion from electrical to mechanical range in silicon devices is generally complicated due to the fact that silicon itself does not exhibit any piezoelectric effect. Up to now, various methods for signal conversion have been tried such as via electrostatic attraction, magnetic effect, thermopneumatic actuation, or by introducing piezodisc [1,2,3,4,5,6]. The above-mentioned techniques, however, are either too complicated to be integrated, requiring very high driving voltages with low driving force, large power consumption, or incompatible to VLSI fabrication technology.

The driving component of the proposed micropump was designed based on the "bi-metal effect" which can provide strong driving force and distinct vertical displacement. Bi-metal effect was caused by differences of thermal expansion coefficients of materials in a sandwich structure. When heated, the structure will deflect, providing driving force and causing displacement. Bi-metal structure has two main features: 1) it can achieve large displacement in vertical movement symmetrically and, 2) the deflection is directly coupled with the dissipated electrical power and, therefore, the actuator can be operated at standard microelectronics voltage levels. Moreover, the fabrication of the driving component based on bimetal structure is fully compatible to standard CMOS processings which can be batch processed at low cost.

II. THE DESIGN AND FABRICATION OF THE PUMP :

The bi-metal actuated membrane pump, as depicted in Figure 1, consists of 3 micro-machined silicon chips : a membrane chip with the bi-metal driving component fabricated on top and two identical valve chips. Stacking of two valve chips symmetrically forms the inlet and outlet valves. The volume between the membrane and the passive check valves is the pump chamber. The orifice size of the valves is $400 \times 400 \mu\text{m}^2$. The movable flaps have a size of $1 \text{ mm} \times 1 \text{ mm} \times 10 \mu\text{m}$. The SEM micrograph of the valve is shown in Figure 2. The driving component, fabricated in between the silicon membrane and the aluminum film, consists of Poly-Si heating resistor encapsulated by SiO_2 film for isolation. Upon applying a driving signal, the poly-Si resistor will heat the Si-Al bi-metal membrane. Because of the difference of the thermal expansion coefficients, the whole membrane will deflect distinctly. As a result, pressure difference inside and outside the micropump is created. Thus the fluid is pulled in and pushed out of the micropump under alternative driving signals.

All chips used are n-type doped, 100-oriented with resistivities between 2 to 4 ohm-cm. For processing the two valve chips, the most difficult part is the formation of the thin movable flap at a thickness of $\sim 10 \mu\text{m}$. Using Si_3N_4 (200 nm thick with refractive index ~ 2.0) as the etching mask, anisotropic etching in aqueous KOH (35%, 75°C) was conducted at a rate of $0.75 \mu\text{m} / \text{min}$ for etching of the orifice and the movable flap.

For processing the membrane chip with the bi-metal driver, 500 nm thick LPCVD poly was deposited and etched to form the serpentine poly Si resistor. LPCVD Si_3N_4 was then deposited as an insulating spacer and etched for metal contact holes. Aluminum was then sputtered and etched to wire the resistor as well as to form the top layer of the bi-metal structure. After the formation of the bi-metal driver on top, the back side of the wafer was then masked and etched to form the membrane. After processing of the valve chips and the membrane chip, assembling of the first prototype micro pump took place by sticking the three chips together with epoxy.

III. RESULTS AND CONCLUSION :

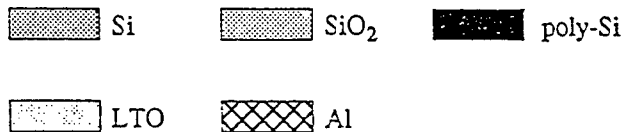
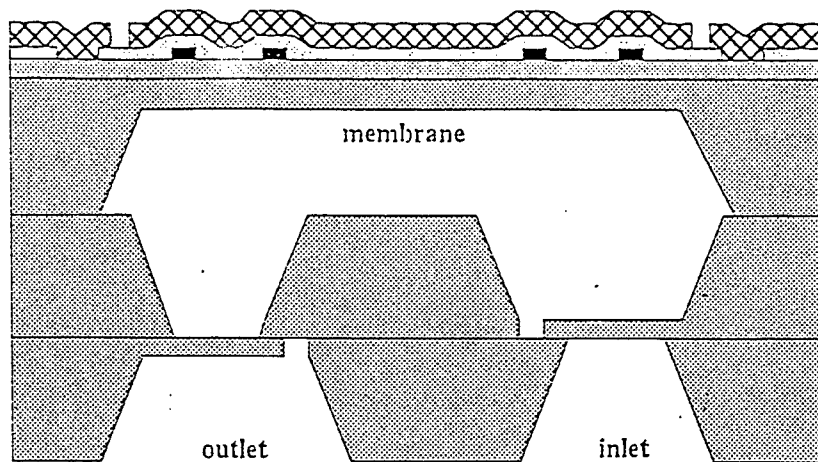
Figure 3 illustrates the measurement setup. The volume stroke of the membrane is in the range between $0.4 \mu\text{l}$ and $0.7 \mu\text{l}$. A pumping yield of $40 \mu\text{l} / \text{min}$ was measured with a pumping frequency of 1 Hz and driving voltage of 10V. At present the performance of our micropump is similar to micropumps developed previously, but operating at much lower driving voltage. Optimization of the processings are underway and dramatic improvement in the performance of the pumping speed is expected.

ACKNOWLEDGMENT

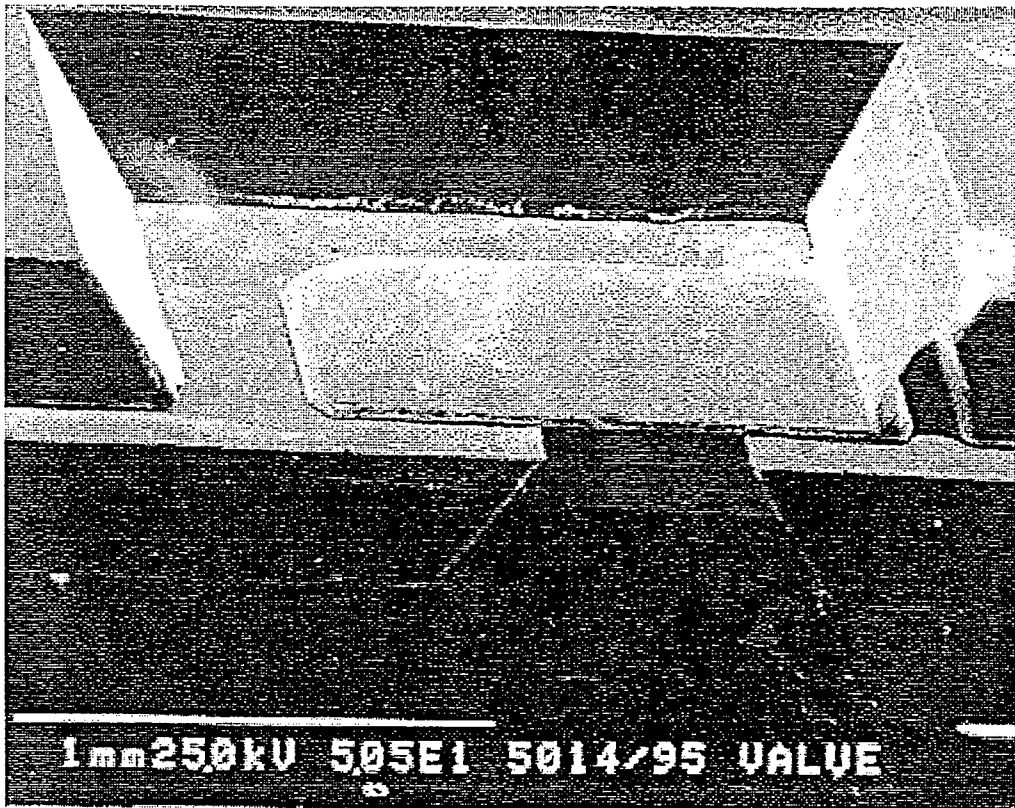
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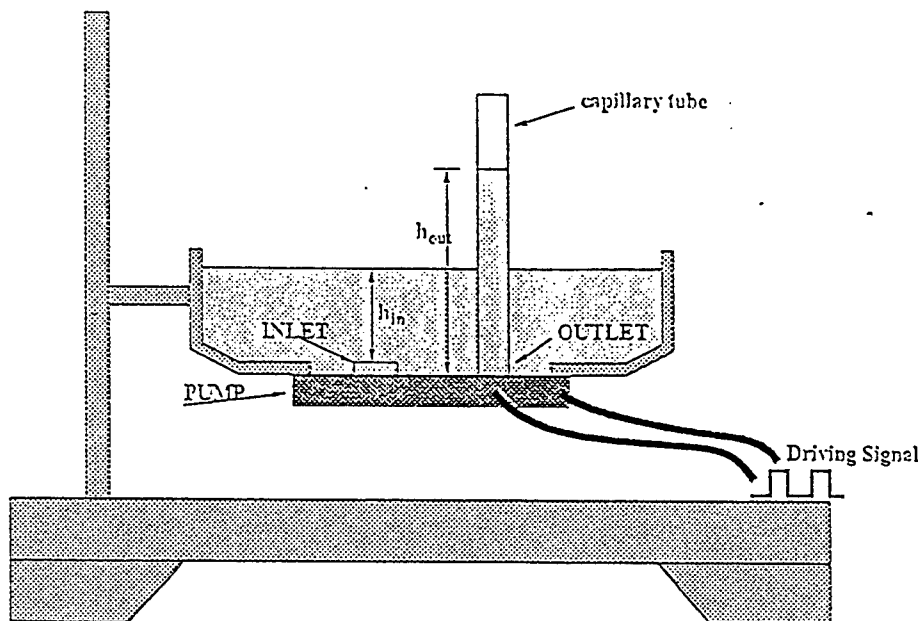
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- 1) Schematics of the bi-metal actuated membrane pump.



2) SEM micrograph of the fabricated valve chip.



3) Experimental set up for measuring the pumping speed of the membrane pump.

DEEP X-RAY LITHOGRAPHY BASED PROCESSING FOR MICROMECHANICS

T.R. Christenson
Dept. 2643, Sandia National Laboratories
P.O. Box 5800, MS-0329, Albuquerque, NM 87185

Introduction

Micro electro mechanical systems or MEMS encompass two broad areas: sensors and actuators. Both areas are concerned with component dimensions under one millimeter with features as small as a few microns. Progress in the microactuator area, however, has lagged that of the microsensor field which is a result that stems from the differences in requirements of the two areas. Ideally, a sensor does not affect the environment which it is sensing - an attribute which micromachined sensors exploit due to their small size. Process technologies based on thin films are therefore appropriate. Useful microactuators, on the other hand, are required to do work on their environment and thus are volume dependent devices. In addition, maintaining a batch processing mode is desired in order to minimize production cost. Such a constraint implies photoresist processing on a planar substrate to produce prismatic components. To achieve large actuator volume changes per unit substrate area, therefore, requires correspondingly large structural heights normal to the substrate. This requirement is a major reason for the activity in high aspect ratio processing technology [1,2].

Achieving high aspect ratio micromechanical components is further complicated by tolerance requirements. Component and intercomponent dimensional accuracies of the order of 1 part in 10^5 which are achievable for serially produced precision machined components translate to tolerances well into the submicron range for microscale components. Alleviating friction at this scale also points to the availability of a large variety of materials which preferably also provides for magnetic materials.

The above process requirements are accommodated by an extension of the German LIGA process which has been pursued at the University of Wisconsin - Madison under Prof. H. Guckel [3]. LIGA, a German acronym representing the processes of deep x-ray lithography, electroforming, and injection molding was first described in the early 1980's by Prof. W. Ehrfeld while at the Karlsruhe Research Center in Karlsruhe, Germany [4]. The x-ray source is synchrotron radiation generated by an electron storage ring which has the properties of high collimation, high intensity, and wavelengths with large absorption length into an x-ray sensitive photoresist, typically poly methyl methacrylate (PMMA). Such an exposure source has yielded prismatic structures with up to 10 cm thickness [5] and vertical flank run-out of less than $0.1 \mu\text{m}$ per $100 \mu\text{m}$ of structural height. The exposed photoresist is developed in order to provide a mold for electroforming. The resulting metal components may then be replicated via injection molding independent of the need for a storage ring x-ray source and is demanded by the requirement for cost-effectiveness.

X-Ray Assisted Micro-Fabrication

A primary technical difficulty in high aspect-ratio photolithography based processing lies with establishing sufficiently thick photoresist. The LIGA process requires this thick photoresist layer to be applied to a substrate covered with a suitable plating base. Standard photoresist spinning is not practical at millimeter thicknesses and direct polymerization leads to large built-in strain. An application method using room temperature solvent bonding of high-purity pre-cast PMMA sheet typically one millimeter thick was therefore adopted which allows for practically unlimited thickness strain-free photoresist application [6].

Additional benefits of this photoresist application technique include the ability to use the photoresist as a mechanically stable material for multiple layer processing as well as for plastic mechanical parts.

Patterning of the resulting photoresist layer is provided for with a suitable x-ray mask which is composed of a low x-ray absorbing carrier such as silicon that supports an absorbing pattern, typically gold. Exposure depth and time is dependent on the particular storage ring. The majority of components to date have used component thickness near the 200 μm range and are limited by low energy storage rings. In order to achieve exposure depths of the order of 1 cm, x-ray photon energies of 20 keV are required as are available from a source such as the 2.5 GeV National Synchrotron Light Source at Brookhaven National Laboratory. Estimates on exposure cost approach \$0.10 per square centimeter for such high energy exposures and provide an alternative to injection molding for achieving cost effectiveness.

Following exposure, a highly selective developer is used to remove the exposed photoresist areas and expose the plating base layer. A variety of metals including alloys may subsequently be electroplated. A release procedure results in free components such as shown in Fig. 1.



Fig. 1 Released electroformed nickel gears patterned via deep x-ray lithography. The gear thickness is 100 μm and the gear tooth width is nominally 5 μm .

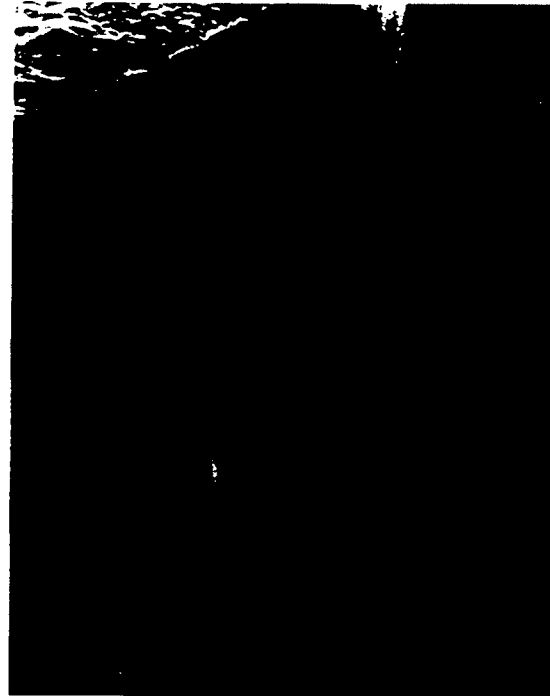


Fig. 2 Assembled nickel rotor on shaft. The difference in shaft and rotor inner diameter is 0.5 μm . Structure height is 100 μm .

The availability of free components makes possible the ability to use assembly to achieve more three-dimensional structures as are commonly encountered in actuators. Achieving sub-micron gaps directly in a journal bearing, for example, is not feasible with photoresist technology at these extreme aspect ratios. Assembly techniques, however, may be used to assemble separately fabricated components with submicron biased dimensions. Fig. 2 demonstrates this. The high degree of fabrication repeatability also lends itself to part interchangeability.

A further attribute of LIGA based processing is that it is a low-temperature process and is therefore amenable to post fabrication on a microelectronics processed substrate. Integrated position sensing and drive electronics are thus readily possible, thereby facilitating system integration. Such integration has been demonstrated by using integrated silicon photodiode shaft encoders to sense real time dynamics of magnetic micromotors rotating at 150,000 rpm.

Magnetic Microactuators

Dominant application areas for microactuators and coupled micromechanisms such as microrelays and micropositioners require output forces in the 1 milliNewton range with travel of at least 300 microns at power dissipation levels in the milliWatt range. This guideline has been used to develop generic linear and rotary microactuators based on deep x-ray lithography processing. An actuation means with the greatest ultimate energy density is desired. Among the possible forms this means may take in a micro-scaled actuator, ultimate energy density increases from electric to magnetic to pneumatic drive. Fabrication complexity, unfortunately, also increases in a corresponding manner. Pneumatics requires tubes which are now just being realized. Electric drives suffer most notably from low energy densities and high voltages. Magnetic drives are directly suitable for system integration due to the low driving point impedance of a coil.

Magnetic drives may be implemented if two fundamental components can be accommodated. A soft ferromagnetic material and suitable coil must be realized. Further possibilities arise if a permanent magnet material could be implemented. A soft magnetic material has been provided with electroplated 78/22 nickel-iron or 78 Permalloy. The as-electroplated magnetic properties of this material include an initial permeability of 2000 and saturation flux density of 1.0 Tesla which is sufficient for variable reluctance actuation. Micro-coil fabrication has evolved to a stage to utilize automatic coil winding technology. Magnetic core preforms are made via deep x-ray lithography which can accept several hundred turns of 50 AWG magnet wire. The resulting coil is inserted with spring loaded tabs as shown in Fig. 3.

Fig. 3 shows a magnetic linear actuator fabricated by deep x-ray lithography. The thickness of material is 150 μm which yields a maximum output force of 1 milliNewton. Travel of 450 μm is possible and position is sensed through an inductance change of 1 microHenry per micron of motion. Resonant operation with 200 μm amplitude is sustained with 200 microWatt power dissipation.

Fig. 4 shows the result for a rotational device. A three-phase variable reluctance stepping motor is shown coupled to a planar gear train which operates into a single phase electromagnetic brake. Electrical control of a mechanical load is therefore provided which allows dynamometry measurements to be performed. Such measurements indicate output torque near 1 microNewton-meter with maximum output power of 20 microWatts.

Conclusions

Deep x-ray lithography based fabrication provides a means to fabricate microactuators with useful output forces. High energy x-ray exposure provides a tool for fabrication of the next generation of precision engineered components. Device characterization, materials science, an metrology continue to pose challenges at this scale.



Fig. 3 Linear magnetic microactuator with $80\mu\text{m}$ thick assembled Permalloy spring and plunger, $150\mu\text{m}$ thick Permalloy magnetic circuit and 400 turn coil.

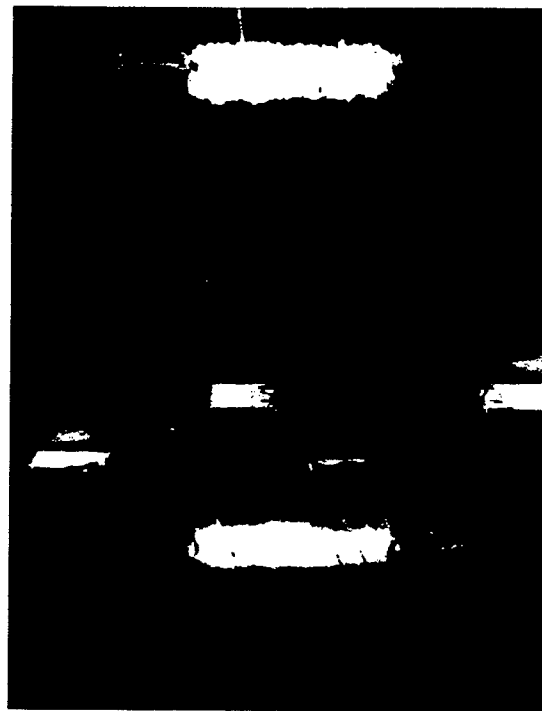


Fig. 4. Variable reluctance stepping microdynamometer system with driving rotor radius of $500\mu\text{m}$ and $150\mu\text{m}$ thickness. A $75\mu\text{m}$ radius idler gear couples the rotor to a $300\mu\text{m}$ radius braking gear.

Acknowledgments

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BIOMEDICAL MICRODEVICES: A MICROMACHINING APPROACH

By
Babak Ziaie and Khalil Najafi

Center for Integrated Sensors and Circuits
University of Michigan
Ann Arbor, Michigan 48109-2122

ABSTRACT

This paper reviews the application of silicon micromachining techniques in fabricating biomedical microdevices. The main emphasis will be on devices developed at the University of Michigan Center for Integrated Sensors and Circuits. These include: intracortical recording and stimulating electrode arrays, a nerve regeneration sieve electrode, and a telemetry based microstimulator for stimulating denervated muscle groups in paraplegic and quadriplegic patients. These examples demonstrate the ability to fabricate high performance miniature devices using silicon micromachining and microfabrication techniques.

INTRODUCTION

Advances in biomedical sciences have mostly been due to our technological ability in obtaining meaningful information from biological systems. These systems are very complicated and are the result of millions of years of evolutionary forces and even our most advanced computing systems are dwarfed compared to the complexity of human brain. Of the most recent exciting technological developments that have found immediate applications in the biomedical area are: various imaging systems like computed tomography (CT) magnetic resonance and ultrasound, applied neural control systems for functional neuromuscular stimulation, and interventional and implantable systems like cardiac pacemakers, implantable defibrillators, infusion pumps, and implantable sensors [1]. In this paper we discuss the application of microelectronics technology and silicon micromachining in fabricating implantable biomedical devices. These devices for the most part are used as sensors to obtain information regarding physical and chemical parameters within biological systems and in some applications in applied neural control systems as recording or stimulating electrode to interface with the nervous system.

Biomedical sensors serve as an interface between living and electronic systems. The interaction between the sensor and biological system is in both directions, i.e., in order to faithfully measure the desired physical or chemical parameter the sensor should not disturb the system in which it is located and simultaneously it must also be protected from the deleterious interactions with the biological system. Miniaturization can reduce the disturbing effect of the sensor on the measurement system since in biological environments one has often a limited anatomical space in which the device must reside and take the measurement. Biocompatible materials can be used in fabricating implantable sensors in order to reduce the unwanted attack of the living system on the sensor.

Recent advances in microelectronics technology and silicon micromachining have provided a strong tool in fabricating miniature sensors for biological applications. Biomedical sensors have traditionally been fabricated using standard machining techniques and piece by piece individual assembly. These usually resulted in bulky devices that were expensive and could only be produced in small quantities. Microelectronics techniques and micromachining, however, can produce miniature devices in large quantities at a low price. During the last fifteen years we have developed a number of biomedical microdevices at the University of Michigan. After a brief review of the silicon micromachining techniques several devices, including: recording and stimulating intracortical electrode arrays, a nerve regeneration sieve electrode and a microstimulator for muscular stimulation will be reviewed.

SILICON MICROMACHINING

Silicon micromachining is defined as the selective precision etching of the silicon substrate [2]. This technique is an offspring of the integrated circuit process technology which has been most successfully used in fabricating microsensors. Development of beam-lead process for the integrated circuits marks the beginning of the micromachining era [3]. Following this work anisotropic silicon etchants (e.g.,

potassium hydroxide KOH [4], Hydrazine [5], and ethylene diamine pyrocatechol EDP [6]) were developed to supplement the existing isotropic etchants (normally HF in combination with HNO₃). The anisotropic etchants have higher etch rates in specific crystallographic directions, for example KOH attacks <100> and <110> directions faster than <111>. This enables one to create V-shaped grooves in (100) silicon. EDP has another useful property and that is its dopant dependent etch rate. Heavily doped silicon areas (doping > 5 x 10¹⁹ cm⁻³) are not etched away in EDP. This enables the designer to control the vertical etch dimensions to better than 1 μm. A new technique for controlling the vertical etch dimensions without introducing high dopant concentrations in silicon (this concentration is too high to allow for fabricating electronic devices in these regions) is the electrochemical etch stop [7]. This method uses applied bias to a p-n junction (usually n epitaxial layer grown on the p substrate) to etch the p region in KOH or EDP solution, the etch stops once the p substrate is etched. The recent developments in dry etching of silicon and other thin film materials (silicon dioxide, silicon nitride, polysilicon and polyimide) have added new tools to micromachining armament.

The aforementioned micromachining techniques use bulk silicon as a starting material (for this reason it is called bulk micromachining technique) and the final structure is produced by etching silicon to produce membranes (for pressure sensors), proof mass (for accelerometers), or various other structures. Another micromachining technique uses a sacrificial layer (this can be polysilicon, silicon oxide, or low temperature oxide LTO) which is subsequently covered by a layer of polysilicon or silicon nitride or other material of interest. The initial sacrificial layer is then etched away leaving free standing structure like diaphragms or cantilever beams. This technique is called surface micromachining and can produce movable parts on silicon substrates with less than 1 μm gap. Although surface micromachining can yield smaller devices than bulk micromachining, stress in deposited films should be annealed and can limit the scaling of the devices [8].

RECORDING AND STIMULATING ELECTRODE ARRAY

Recording electrical activity of the neurons in the central nervous system is a powerful tool in understanding the brain function. In addition the ability to stimulate small population of neurons can be used to restore function in some disabled individuals (e.g., cochlear and visual prostheses). Over the past few years we have developed a high-yield batch fabricated technique based on silicon micromachining to fabricate thin-film recording and stimulating electrodes [9,10]. Figure 1 shows the structure of a multichannel silicon recording microprobe. The recording sites are located along the shank and are connected to the back end of the probe with polysilicon conductor lines which are passivated on top by dielectric layers. The back end contains the bonding pads and can also house the signal processing circuitry. The whole structure is defined by a deep boron diffusion step which produces 12-15 μm thick boron areas of the shank and back end. At the final step the devices are etched in EDP which as mentioned before etches the lightly doped substrate and stops on the deep boron diffusion areas. Figure 2 shows the fabrication process of the microprobes.

A NERVE REGENERATION SIEVE ELECTRODE

In addition to the penetrating type electrodes described in the previous section, the silicon micromachining technique allows us to fabricate other types of electrodes as well. A nerve regeneration sieve electrode developed in our group during the past couple of years is an example of such devices [11]. This electrode is used to study nerve regeneration in peripheral nervous system by allowing the severed ends of a nerve to regrow through small holes micromachined in a silicon substrate. Figure 3 shows the structure of the sieve electrode. It consists of a thick silicon rim supporting a thin (~3 μm) silicon diaphragm fabricated by a shallow boron diffusion step. Small holes (diameter = 5 μm) are produced in the thin diaphragm and the recording site is made of iridium and has an area of ~ 100 μm². Silicon integrated ribbon cables are also included in this device to connect the electrode end of the device to the back end. These ribbon cables are fabricated as part of the electrode using shallow boron diffusion step at the same time with the diaphragm. Figure 4 shows a photograph of a sieve electrode.

A TELEMETRY BASED MICROSTIMULATOR

Figure 5 shows the structure of a telemetry based microstimulator developed [12,13]. This microdevice is only 2x2x10 mm³ and can be injected into denervated muscles of paraplegic and quadriplegic patients using a gauge 10 hypodermic needle. It consists of five individual elements: a micromachined

silicon substrate; a silicon IC chip; a hybrid capacitor used for charge storage of the stimulation pulse; a hybrid receiver coil for power and data reception; and a custom machined glass capsule. The silicon substrate contains a reference electrode and a stimulating electrode. The IC chip is used for data reception and microstimulator control and is affixed atop the silicon substrate, while the hybrid capacitor and receiver coil are mounted on the IC chip. Lastly, a hermetic package is provided for the microstimulator circuitry and hybrid components by electrostatic bonding of the glass capsule to the silicon substrate. The stimulating electrodes are outside of the package and feedthroughs are used to connect the internal electronics to the electrodes. Power and data are transmitted to the microstimulator using wireless RF telemetry, and the device is capable of delivering a constant current pulse of 10 mA for durations of up to 200 μ sec into loads of $\leq 800 \Omega$, and it is able to repeat this stimulation at a rate of up to 40 Hz. Figure 6 shows a photograph of the microstimulator.

CONCLUSION

We reviewed the application of silicon micromachining in fabricating biomedical microdevices. We used three devices that were developed in our laboratory during the past decade as a vehicle to demonstrate the attractive features of micromachining in biological applications. These devices were silicon intracortical microprobes, a nerve regeneration sieve electrode, and a telemetry based microstimulator. Using silicon micromachining technology one can batch fabricate high performance miniature devices at a low cost and high yield.

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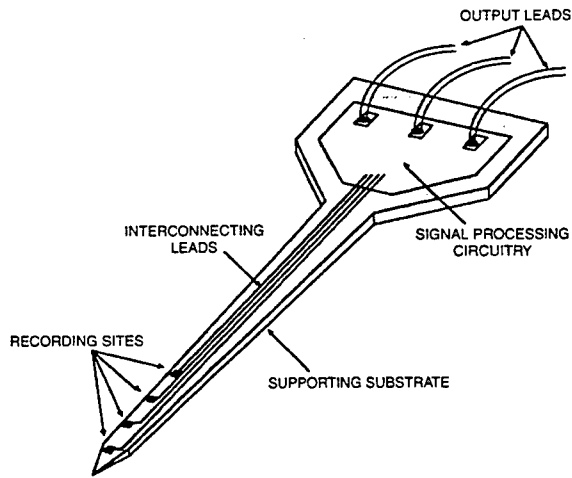


Figure 1: Structure of a multichannel silicon recording microprobe.

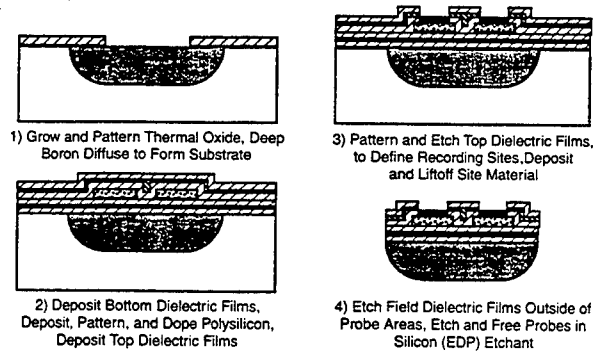


Figure 2: Fabrication sequence for passive multielectrode microprobes.

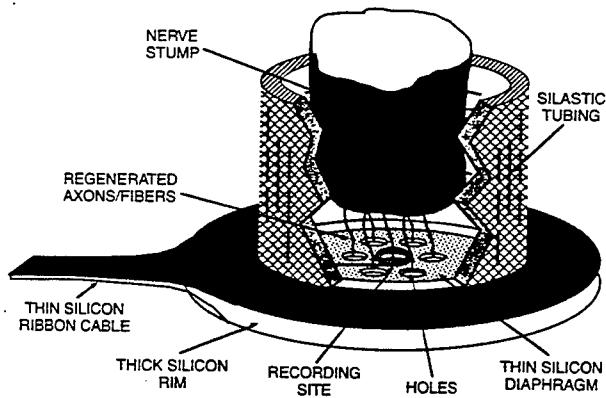


Figure 3: Structure of a nerve regeneration sieve electrode.

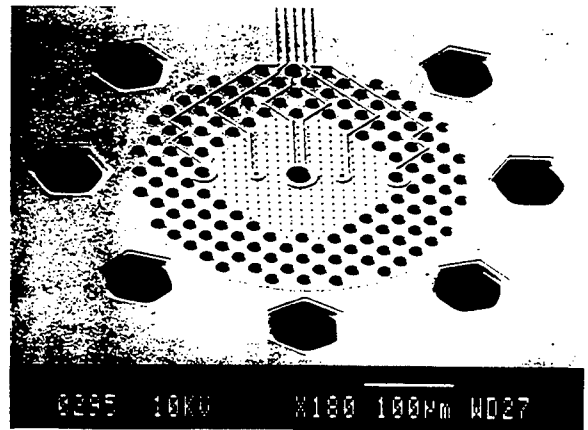


Figure 4: SEM photograph of a silicon sieve electrode.

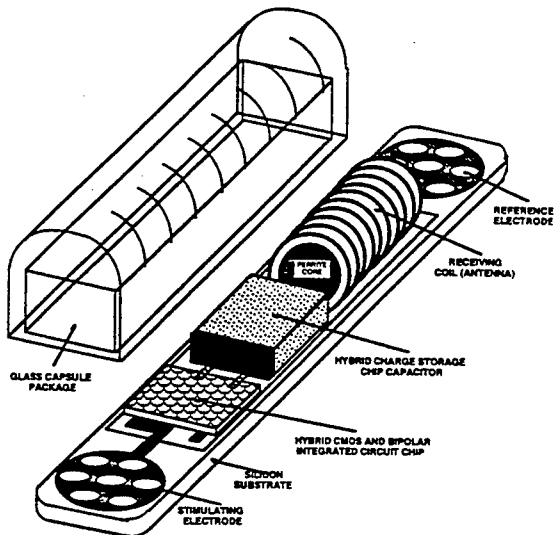


Figure 5: Structure of a single channel microstimulator.



Figure 6: A photograph of an assembled microstimulator.

Large-Area Imaging with Amorphous Silicon Photodiode Arrays

Raj B. Apte, P. Mei, R. Weisfield, R. Lujan, X.D. Wu, S.E. Ready, R.A. Street

Xerox Palo Alto Research Center

3333 Coyote Hill Road

Palo Alto, CA 94304

P. Nylén

Department of Physics

University of Stockholm

Stockholm, Sweden

Abstract—An active matrix of amorphous silicon thin-film transistors and photodiodes on glass are used to make a large area (10x8 sq. in.) imaging array consisting of 1920x1536 picture elements. This page-sized imager can be used for contact imaging of documents and medical imaging at a resolution of 200 spi. Design of hydrogenated amorphous and polysilicon thin-film transistors on glass is reviewed in this paper along with a discussion of the operation of the amorphous silicon array.

I. INTRODUCTION

Similar to the way DRAM technology has driven semiconductor processing, the active-matrix liquid crystal display has led the way for large-area, low-temperature electronics on glass. This paper will discuss the basic device design for incorporating amorphous silicon (a-Si:H) and polysilicon (p-Si:H) thin-film transistors (TFTs) on glass with a maximum processing temperature of 350°C using laser recrystallization. a-Si:H TFTs and photodiodes may be integrated into an imaging array. Work at Xerox PARC has progressed steadily to the point where six million electronic elements—three million TFTs and three million photodiodes—can be integrated onto a glass substrate 8x10 square inches. While not presently capable of performing advanced signal detection and processing, amorphous silicon transistors are ideal for switching applications. Laser-recrystallized p-Si:H has fifty times the mobility and might be used for higher current applications.

The a-Si:H photodiode array is a full-page scanner that can address a complete 1920x1536 pixels with 8 bits of gray scale at 10 frames per second. Following sections will deal cover the basics of amorphous and polysilicon TFT design, the imager system design, and a discussion of the imager's performance limits.

II. AMORPHOUS AND POLYSILICON TFTS

The basic strategy in building a-Si:H and p-Si:H transistors on the same substrate is to keep the process of the two as similar as possible. The process is demonstrated in Figure 1. Gate metal and gate dielectric are first deposited on the glass substrate. The gate dielectric may be silicon oxide, nitride, or a mixed oxynitride and is deposited at 350°C. Intrinsic a-Si:H is then deposited at 250°C as the channel. Until this point both types of transistors have been treated identically. A mask is used and the wafer exposed to a 308 nm XeCl excimer laser. Three separate exposures are done with increasing pulse energy to avoid ablating the film or creating hydrogen voids [2]. After the amorphous silicon has crystallized, a hydrogen plasma is used to re-hydrogenate the polysilicon channels. A passivation oxide or nitride is then deposited and processing continues with source and drain deposition. Figure 2 shows curves for both types of TFTs on the same substrate. Laser recrystallized p-Si:H TFTs may have extensive application in replacing the driver circuitry for active matrix drivers.

In addition to TFTs, amorphous silicon can be used to fabricate photodiodes. In the imagers that will be the subject of the remainder of this paper, a-Si:H TFTs and photodiodes are fabricated together as in Figure 3.

III. SYSTEM DESIGN AND PERFORMANCE

Figure 4 shows the basic circuit used for imaging. The gates of the TFTs are connected to a shift register whose output swings from 0 to 20 V. When the gate is "on," charge from the 0.4 pF photodiode drains onto the 50-100 pF data line. This charge is detected by an amplifier and sampled onto a capacitor. a-Si:H is a very good switching element for matrix addressing because of its very high (Teraohm) "off" resistance. The leakage charge from 1935 "off" rows must be considerably less than the signal charge from the one "on" row [2].

Because the quantum efficiency of amorphous silicon photodiodes is around 80-90% [3], the two limits on the efficiency of the imager are fill factor and noise. The fill factor, or how much of the face of the circuit is photosensitive, reduces the number of photons that may be converted to photocharge. The current imager has a fill factor of 35%. A tightening of the design rules or a lower pitch of pixels is needed to improve the fill factor further [2].

Noise governs the minimum detectable photocharge. The KTC sampling noise, which is a consequence of the sampled photodiode capacitance is 290 electrons. This gives a theoretical detectable illumination of the order of 100 pW/cm². However, the large capacitance of the data line lowers the value of the signal by 100 so that read-out amplifier noise dominates the system. Although the best dynamic range for a 5V bias is 10,000:1 at the pixel, the amplifier limited dynamic range is only 256:1 in the present system. Improvements in the amplifier are possible by using a charge-sensitive configuration and a noise level of less than 1000 electrons appears to be possible with room-temperature CMOS.

Document imaging and radiography have very different requirements. Document imaging frequently emphasizes spatial resolution and requires only limited dynamic range.

200 spi is sufficient for facsimile quality resolution, but 400 spi or greater is needed for small text or lines. Typically a dynamic range of 16:1 is sufficient to capture simple halftones. Radiography excluding dental x-rays and mammography has limited need for resolution. One system limit is geometric unsharpness from the finite x-ray source size. Another is the smearing of the x-ray image by light-piping in the scintillator. 200 spi appears to meet the requirements in this case. Because of pulse-to-pulse fluctuations in the x-ray source, the large differences in x-ray absorption in the body, and the need to minimize the number and doses of patient x-ray exposures, a large contrast ratio is needed for x-ray detection, typically greater than 256:1. New readout circuits could make 1024:1 possible. At this level the imager would be close to the x-ray shot noise limit and the patient would be exposed to the minimum possible x-ray dose. To achieve the shot noise limit, gain at the pixel is likely to be needed. p-Si:H pixel amplifiers may be able to achieve the shot noise limit.

SUMMARY

This paper has present a review of some activities at the Xerox Palo Alto Research Center. Amorphous and polysilicon transistors have been fabricated on glass substrates at 350 °C. Amorphous silicon transistors have been integrated with photodiodes onto 8x10 inch arrays to make image sensors with three million pixels. The prospects for using this technology driven by the display business for medical and document imaging are excellent.

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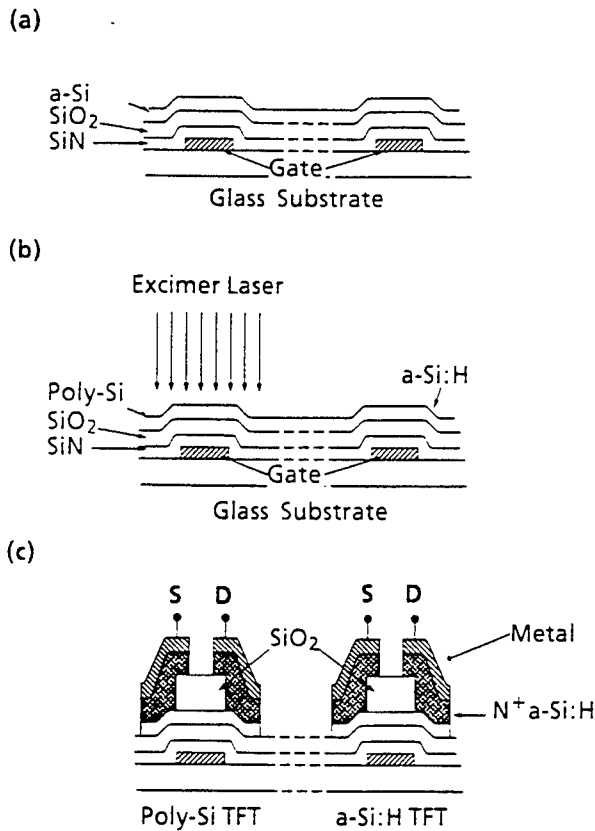


Fig. 1. Flow chart of the fabrication process for hybrid a-Si:H and poly-Si TFTs. (a) PECVD deposition of the nitride, oxide, and a-Si:H thin films over gate electrodes. (b) Selective laser dehydrogenation-crystallization of PECVD a-Si:H. (c) The final structure of a-Si:H and p-Si:H TFTs on the same glass substrate [1].

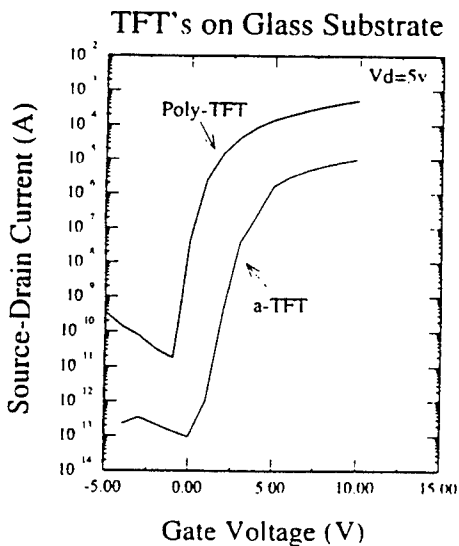


Fig. 2. Characteristic source-drain current of both a-Si:H and p-Si:H TFTs with optimized gate dielectric as a function of gate voltage. [1]

Poly-Si:
 Mobility = $50 \text{ cm}^2/\text{V}\cdot\text{sec}$
 STS = $0.33\text{V}/\text{dec}$
 $I_{\text{ON}}/I_{\text{OFF}} = 2 \times 10^7$
 $I_{\text{Leak}} = 0.05 \text{ pA}/\mu\text{m}$

a-Si:H:
 Mobility = $1 \text{ cm}^2/\text{V}\cdot\text{sec}$
 STS = $0.5\text{V}/\text{dec}$
 $I_{\text{ON}}/I_{\text{OFF}} = 10^8$
 $I_{\text{Leak}} = 10^{-3} \text{ pA}/\mu\text{m}$

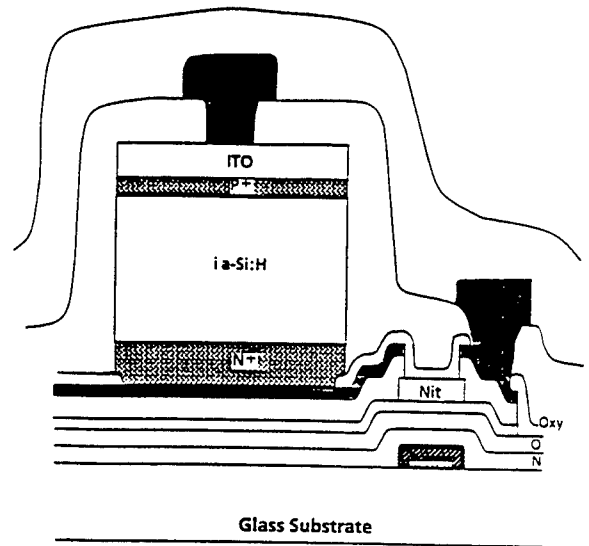


Fig. 3. a-Si:H photodiode and TFT integrated onto glass substrate.

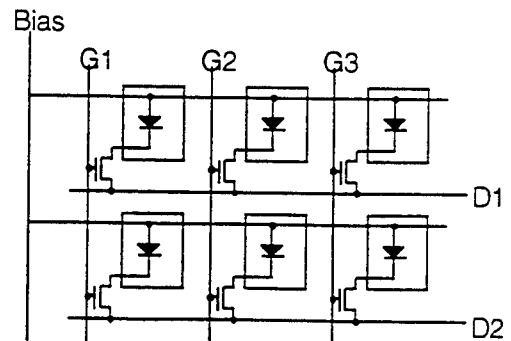


Fig. 4. Schematic of photodiode/TFT array. Photodiodes are biased to -5V. The gate lines (G1, G2, G3) are pulsed from -8V (off) to +12 V (on). The data lines are held at 0V. Note that there is no ground plane.

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Tsai, R.	79	Yakovlev, Y.P.	421		
Tsien, P.-H.	393	Yakubo, K.	337		
Tsui, D.C.	87	Yang, E.S.	151		
Turner, G.W.	491	Yang, G.M.	417		
Ünlü, M.S.	429	Yang, J.W.	535		
Unterrainer, K.	495	Yang, K.	525		
Vagidov, N.Z.	451	Yang, R.	369		
Vai, M.	725	Yang, Y.F.	151		
Van Calster, A.	785	Yeap, C.-F.	811		
van den Einden, W.T.A.	91	Yngvesson, K.S.	619		
van der Weide, D.W.	255	Yoh, K.	731		
Varakorn, K.	239	Yoh, K.	789		
Varvanin, N.A.	99	Yoo, S.D.	677		
Vaschenko, V.A.	175	Yoshida, M.	607		
Vaschenko, V.A.	233	Ytterdal, T.	365		
Vatannia, S.	171	Ytterdal, T.	79		
Vendik, I.	627	Yu, S.G.	359		
Vergheese, S.	337	Yuan, S.	505		
Vergheese, S.	433	Zahurak, J.K.	571		
Volkov, V.A.	665	Zamdmer, N.	433		
Vorobjev, L.E.	273	Zavada, J.	359		
Voronov, B.M.	619	Zegrya, G.G.	421		
Wachutka, G.	51	Zeng, L.	275		
Wada, H.	729	Zengingönül, H.P.	429		
Wadley, H.N.G	567	Zhan, C.-Q.	393		