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THESIS

CONTROLLER DESIGN, ANALYSIS, AND PROTOTYPE FOR SHIP SERVICE CONVERTER MODULE

by

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June 1996

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**CONTROLLER DESIGN, ANALYSIS, AND PROTOTYPE
FOR
SHIP SERVICE CONVERTER MODULE**

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of the requirements for the degree of

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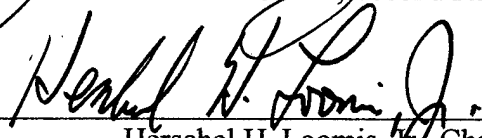
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ABSTRACT

The Navy has invested in an effort to update the ship electrical distribution system for new vessels. The new architecture divides the ship into specific zones containing common energy conversion devices. Rather than the traditional AC distribution, DC will be produced at the source (a multiphase alternator connected to a controlled rectifier). An integral part of the proposed DC distribution system is the Ship Service Converter Module (SSCM) which acts as a buffer between a main DC bus and a specific zone in the ship. Currently a research effort is underway to make available two Reduced Scale Advanced Development (RSAD) 100kW SSCMs for testing at the Naval Surface Warfare Center, Annapolis. The Power Laboratory at the Naval Postgraduate School is responsible for delivering two identical prototype controllers based on digital signal processing for the RSAD SSCMs. The focus of this thesis is the design, construction and testing of the prototype controllers. This engineering effort includes the following: the analysis of the performance of various control algorithms through simulation; the refinement of the selected algorithm; the design, assembly, and testing of the controller and its supporting hardware; the development and testing of the software; and the integration and testing of the complete system.

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I. INTRODUCTION

A. PURPOSE

The focus of this thesis research is on the development of a working controller for a reduced-scale Ship Service Converter Module (SSCM) prototype. The prototype is currently being constructed through a cooperative joint effort between the Naval Postgraduate School (NPS) Power Systems Group, the Naval Surface Warfare Center (NSWC) of Annapolis, Md., and Power Paragon Incorporated (PPI) of Anahiem, Ca.. The controller development process included the following: the performance analysis of various controller algorithms through simulation; the refinement of the selected algorithm; the design, assembly, and testing of the supporting hardware; the design, assembly, and testing of the controller hardware; the development and testing of the software; and the integration and testing of the complete system.

This document provides the background and technical reference information on the final working controller. It is structured to facilitate further development of the controller and enable its incorporation into the targeted SSCM. The document also provides recommendations for refinements in the current controller and improvements in subsequent designs. This chapter presents the background information on the SSCM and DC Zonal Distribution. Chapter II presents theoretical information about the power conversion process which takes place within the SSCM and specific information on both the NPS and 100kW buck converters. Chapter III describes the general requirements for the control of an SSCM. Chapter IV presents the simulation of four control algorithms in order to justify the selection of the implemented algorithm. Chapters V presents the specifics of how the controller is actually implemented in the digital hardware and software. Chapter VI presents the specifics of how the controller is implemented in the analog hardware. Chapter VII presents the test results of the SSCM as implemented at NPS. Chapter VIII offers guidance for both improvement on the present controllers and incorporation of the controllers into the 100kW SSCMs.

B. SSCM GENERAL DESCRIPTION

The SSCM is a solid-state DC device that provides a regulated output voltage at a reduced level from the applied input voltage. It performs the voltage reduction at high efficiency with a high power, high voltage buck chopper. The buck chopper's operation is governed by signals from the controller. The controller is responsible for maintaining the stable regulated output voltage on the SSCM and, during changes in the SSCM load or supply, minimize the transients on the output voltage. Additionally, it can be assigned numerous auxiliary functions such as external communications, fault handling, and SSCM mode control.

C. RESPONSIBILITY

NSWC is coordinating the development of six Reduced Scale Advanced Development (RSAD) 100 kW SSCMs. These units will be the prototype for the SSCMs of the Navy's proposed DC distribution system. PPI is responsible for the design, construction and operational testing of the power portion of the buck chopper and its associated circuits. Final testing of the units will be conducted at NSWC.

NPS is responsible for delivering the first two prototype controllers and supervising the melding of these controllers with PPI's power portion of the SSCMs. The two controllers are to be identical and incorporate a digital signal processor (DSP) for the RSAD SSCMs. The controller should be capable of a local mode for maintenance and a remote mode with control via an RS422 serial port. The controller must provide fault handling and support the parallel operation of two SSCMs. [Ref. 1]

D. DC ZONAL ELECTRICAL DISTRIBUTION SYSTEM

1. Background

Since the end of the Cold War, the U.S. Navy has begun to place special emphasis on affordable modular designs for future ship construction. Reduced funding and the continuous reduction in the U.S. naval construction base have forced re-evaluation of the design criteria and shifted the focus from performance enhancement to affordability. This represents a fundamental shift in priorities. The following eight initiatives identified in Ref. 2 maintain affordability at a higher priority than

performance:

- 1) Extended architectural advantage,
- 2) Promote commonality,
- 3) Exploit producibility,
- 4) Reduce infrastructure,
- 5) Reduced component costs,
- 6) Reduced manning,
- 7) Reduced energy costs,
- 8) Assess potential for combat systems cost reductions.

The Advanced Surface Machinery (ASM) and Affordability Through Commonality (ATC) programs both seek affordability while improving performance over current designs. The programs propose that the design of ship systems be comprised of common modules based on standardized parts. An element of the ASM program is the Integrated Power System (IPS) initiative which seeks to extend these concepts to the power systems for all naval ships of the future, both surface ships and submarines [Ref. 3].

The IPS stresses the use of common components which leads to the reduced cost of design and production. The elimination of any specialization of power components in ship designs will reduce the Navy construction infrastructure, further reducing cost. Commonality also reduces the maintenance cost in both training and part acquisition. A common module with standardized parts will more effectively lend itself to repair and reuse. Additionally, since parts are not platform specific, depots can maintain a smaller inventory to meet the needs of a large variety of vessels. The common modules can be configured to meet the specific platform needs, whether it is for a warship, an auxiliary ship, or a commercial ship.

A subset of the IPS is the Zonal Electrical Distribution System (ZEDS). ZEDS incorporates the concepts of IPS on the electrical system architecture that outperforms today's radial electrical distribution system in many ways (Figure 1.1). It provides for both a cost and weight savings, and allows for enhanced ship production, easy upgrades, and component commonality with other ship classes [Ref. 4]. In addition, it enhances ship integrity by reducing the number of bulkhead penetrations. The advantages of ZEDS

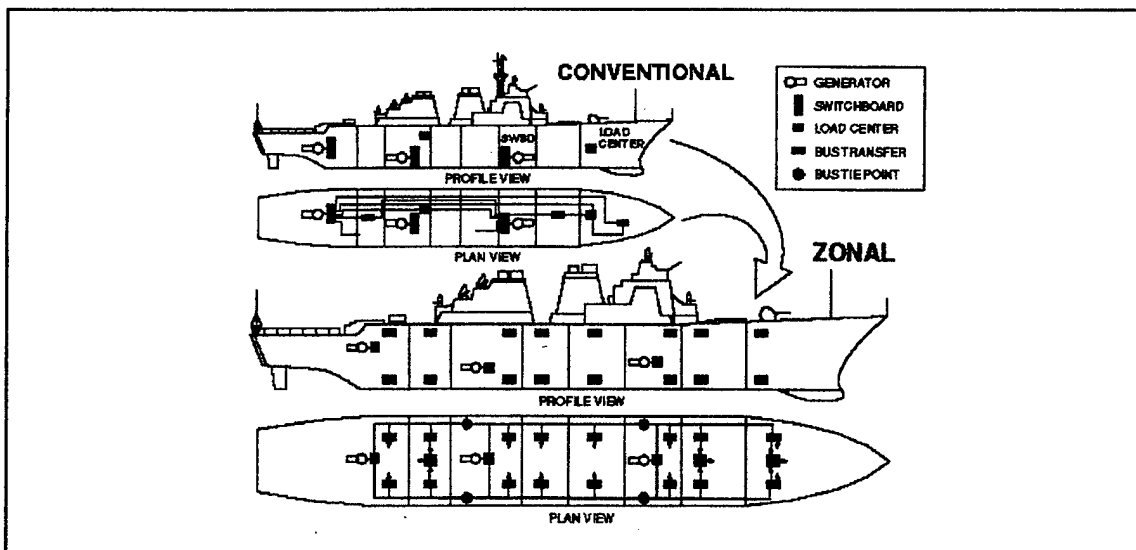


Figure 1.1. DC Zonal Electrical Distribution System (DC ZEDS) [After Ref. 5]

is further enhanced when coupled with DC distribution.

DC electrical distribution provides the capability to integrate the power conversion with the protection circuitry. Modern solid-state converters can identify and respond quicker to transients on a DC bus than the mechanical devices used in current ship designs. In addition, converters and inverters used in the zonal distribution system can prevent faults from affecting the main bus by imposing limits on fault currents. This aspect of the DC ZEDS will allow the ship to fight through with sustained damage without the performance of a fault isolation procedure. DC distribution will reduce power conversion steps and eliminate transformers. Distribution systems can be designed with fewer components. Mechanical bus transfer switches can be replaced with diode logic that would provide uninterrupted power should one power source fail in a many source system.

Currently, the electrical distribution systems on major combatants provide power to combat systems through an intermediate 400 Hz conversion unit. With DC distribution combat systems can be supplied directly from the bus. This increases the reliability of combat systems by minimizing the number of components between combat systems and its power source.

DC distribution has become more viable with the invention of the Insulated Gate

Bipolar Transistor (IGBT). Inverter and converter capabilities have been greatly broadened by the relatively high switching frequency and large currents the IGBT supports. But at present, IGBT technology limits the maximum bus voltage to about 1000V. Higher voltages would be preferred to reduce the current carrying requirements and therefore the size and weight of the transmission lines. In addition to the IGBT, the MOS - Controlled Thyristor (MCT) has recently received considerable interest as a potential switch device capable of sustaining higher voltages and currents. At present, fabrication technologies limit its breakdown to approximately 3000 V and 200 A [Ref. 6 pg 655].

2. DC ZEDS Zone Description

Generally, two types of modules are found in the typical DC ZEDS zone (Figure 1.2), an SSCM and a Ships Service Inverter Module (SSIM). The function of the SSCM is to provide regulated DC power within the zone at a voltage lower than that of the ship service DC bus. It also offers protection of the ship service DC bus by minimizing any fault currents and thereby keeping the effect of a fault within the zone. The SSIM receives power from the SSCMs in the zone and provides the AC power for the zone. It also offers fault tolerance by limiting the currents of an AC fault, thereby preventing these currents from affecting the DC bus within the zone and the other SSIMs. Large machinery within a zone can be DC, eliminating the need for an additional power

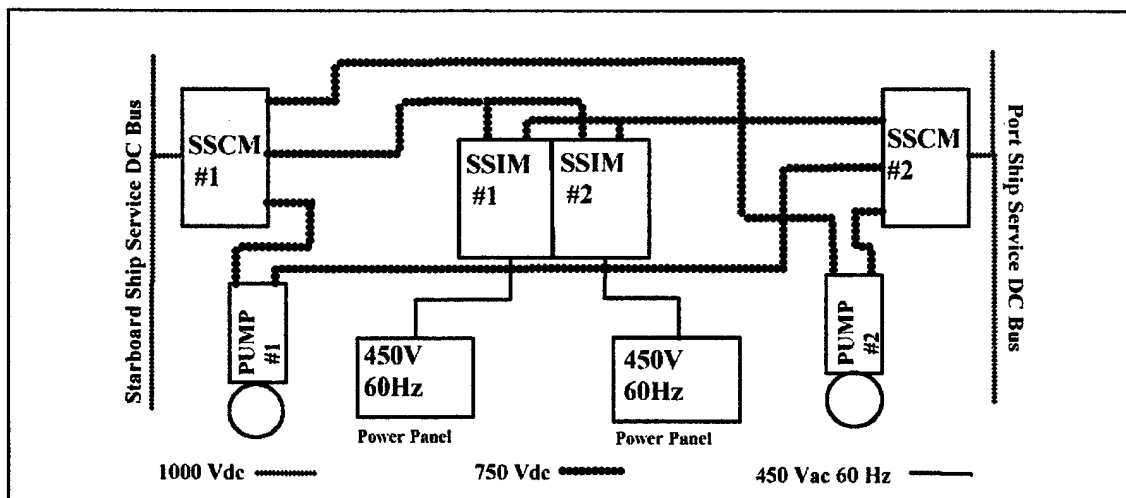


Figure 1.2. Typical DC ZEDS Zone

conversion with the SSIM and allowing them the benefit of power redundancy through diode isolation.

Naval combatant ships will have multiple ship service DC buses running from zone to zone across the entire length of the ship. These zones will have at least an equal number of independent SSCMs to take full advantage of the redundancy and fault tolerance of the system. Auxiliary ships can have as few as one ship service DC bus running the length of the ship. A zone on such an auxiliary ship may have just one SSCM providing power to one or multiple SSIMs. Although this eliminates the redundancy, it still offers many of the advantages inherent to the DC ZEDS design.

Two SSCM topologies are possible for the future combatant. In the first topology, one SSCM provides power to a collection of loads such as pumps and SSIMs. Loads can be added or removed as long as the total load is below the maximum capacity of the SSCM. But some situations may involve loads which exceed the power of a single SSCM. In these cases, multiple SSCMs will operate in parallel, sharing the power requirements of the larger load. The advantage of this scheme is the need for only one type of SSCM. In zones with low to medium power requirements a single SSCM will be present. For zones with higher power requirements numerous copies of that same SSCM will be employed.

II. SSCM POWER CONVERSION

A. THE BUCK CHOPPER

The dc-to-dc power conversion in the SSCM is achieved through the use of a buck chopper. The buck chopper provides an average output voltage that is less than its input voltage. This is accomplished through a combination of high-speed switching and reactive components. The use of a buck chopper for the efficient dc-to-dc voltage conversion eliminates the power consumption and maintenance requirements of rotating machinery or linear regulators. Inertial and frictional losses found in generator sets can be minimized but only at great expense in both design complexity and financial cost. The additional maintenance concerns associated with rotating machinery, including cleaning, lubrication, brush inspection and replacement can be minimized, if not fully eliminated, with the buck chopper. Linear regulators are only a viable option when efficiency is not a concern or the value of the regulated voltage is very close to the value of the source voltage. When only a small voltage drop exists across the linear regulator the majority of the power delivered by the source is transferred to the load and less must be dissipated as heat. Modern solid-state devices, such as the IGBT, allow the buck chopper to achieve high power dc-to-dc conversion with efficiencies comparable to ac transformer coupling.

1. Basic Circuit Description

The basic buck circuit includes an inductor, a switch, a diode, and a load. While this circuit will provide the reduced average voltage on the output, the circuit becomes more practical when a capacitor is added to smooth the output voltage (Figure 2.1). The buck circuit is controlled by cyclically closing and opening the switch. The frequency is generally held constant with the ratio of switch on time to switch off time, termed the duty cycle, modulated according to a control law. A typical cycle of the converter is explained by first considering the interval when the current flows through the inductor and charges the capacitor and provides current to the load. The energy in the inductor field grows as its current increases. The switch is then opened and the polarity of the inductor potential reverses as its magnetic field collapses. The inductor becomes the

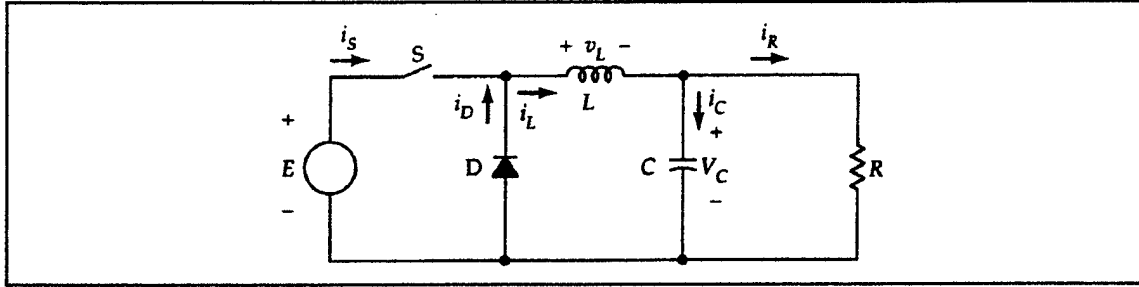


Figure 2.1. Typical Buck Chopper

source. The diode turns on as it is forward biased by the new inductor potential. Current continues to flow to the capacitor and the load as the magnetic field of the inductor collapses. If the inductor is small, the field will collapse completely before the switch is closed for another cycle and the inductor current will be changed to zero until the next cycle (the diode prevents any negative currents from flowing through the inductor when the switch is open). This is the discontinuous mode. If the switch re-closes before the inductor loses all of its energy, the inductor current will not have decayed to zero and will begin to ramp up again. This is the continuous mode.

2. Circuit Analysis

The buck chopper analysis is performed to provide both the steady-state model and a linear state space representation. Information from both is used to correctly model the SSCM in the Simulink environment.

a. Assumptions

In order to obtain simplified mathematical expressions to describe the steady-state buck chopper operation, a set of assumptions is required. Additional assumptions are also used in the derivation of a dynamic state-space model. The specific assumptions are:

1. The voltage drop of the diode and switch when forward biased are negligible.

In this application the diode voltage drop was found to be less than 1.5 volts at full load (current) and the IGBT voltage drop was found to be less than 2.0 volts.

In both cases this is less than 3% of the nominal 75 volt output voltage used in

the controller development. The assumption is even more valid when considering the 750 volt output of the 100 kW buck converter.

2. The capacitor is large enough so that the voltage variations on the output may be considered negligible. This voltage is denoted V_c . The assumption is useful in determining the steady state voltage relationship between input and output, but not the state-space representation.

3. The buck chopper will remain in the continuous mode of operation. This condition simplifies the analysis and was dictated by the design requirements of the SSCM [Ref. 8]. The load range of the SSCM is bounded by the power and current limitation for large loads and the discontinuous mode of operation for small loads.

b. Steady-State Analysis

For steady-state analysis the buck chopper can be modeled as two different circuits; one when the switch is closed as in circuit (a) of Figure 2.2, and one when the switch is open as in circuit (b) of Figure 2.2. A complete cycle of the switch occurs in time period T . The fraction of that period that the switch is closed is the duty cycle, D . During the time the switch is closed, DT , the inductor current is driven by the difference between V_c and the input voltage, E . The inductor current starts at some initial value I_{min} and increases at a constant rate to a final value of I_{max} . When the switch is

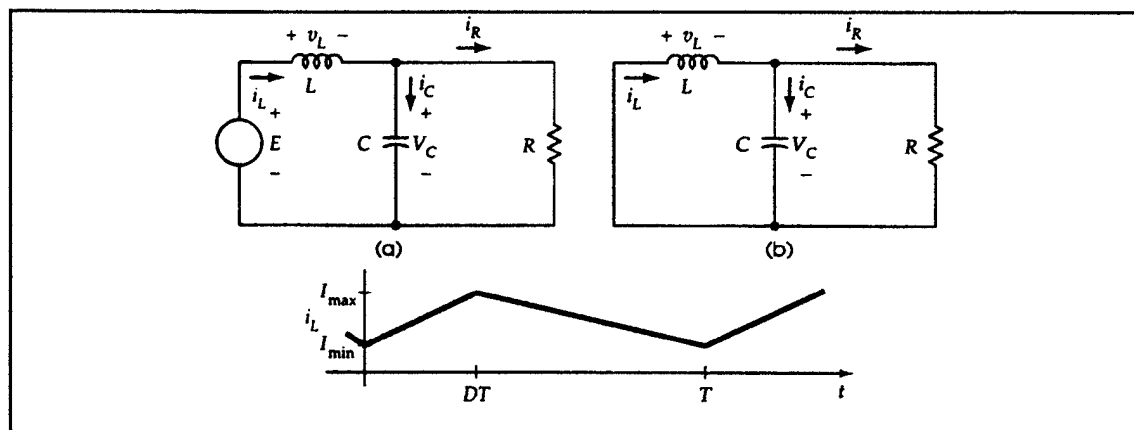


Figure 2.2. Buck Chopper Steady State Models [After Ref. 7]

opened, the inductor acts as the source for time $(1-D)T$ and the current returns at a constant rate to I_{min} . These statements are expressed in Equations 2.1 and 2.2.

(Switch Closed) (2.1)

$$I_{max} - I_{min} = \frac{E + V_c}{L} DT$$

(Switch Open) (2.2)

$$I_{min} - I_{max} = -\frac{V_c}{L} (1-D)T$$

where:

D = the duty cycle

T = the time period of one cycle

L = the inductance of the buck chopper

Since the buck chopper is at steady state and its operation is periodic, I_{min} and I_{max} of Equation 2.1 are equal to I_{min} and I_{max} of Equation 2.2, and solving gives:

(2.3)

$$\frac{E - V_c}{L} DT = \frac{V_c}{L} (1-D)T$$

From which the required steady-state duty cycle can be uncovered:

(2.4)

$$D = \frac{V_c}{E}$$

c. *State Space Representation*

The state space representation of the buck chopper is useful in simulating transient response. To accurately develop a continuous-time state space representation of

the buck chopper, the inductor current must remain in the continuous mode. For analysis, the buck chopper is divided into two separate circuits. The first circuit, the chopper portion, is comprised of the input source, switch and diode. The second circuit is a low-pass filter. In the continuous current mode of operation the output of the first circuit can be modeled as an equivalent voltage source v_e . This output is a periodic rectangular pulse of period T with the duty cycle of d . The duty cycle includes a steady-state duty cycle component D from above, and a time-variant component $d(t)$. It is bounded by the values 0 and 1 inclusively. The waveform's peak voltage is that of the input source e , which, like d , includes both a steady-state component E , and a time-variant component $e(t)$.

(2.5)

$$d = D + d(t)$$

$$e = E + e(t)$$

The output waveform is therefore a series of periodic rectangular pulses, amplitude modulated by the variation in the input source and pulse width modulated by the variation in the duty cycle.

By removing the modulation from the output, the salient characteristics of the output waveform can be determined. Uncovering this reduced-order model of the converter is important from the standpoints of simulation speed and ease of controller synthesis. The time variations in v_e may be represented by the Fourier series:

(2.6)

$$\begin{aligned} v_e &= V_e + \sum_{n=1}^{\infty} a_n \sin n\omega t + \sum_{n=1}^{\infty} b_n \cos n\omega t \\ &= \sum_{n=1}^{\infty} c_n \cos(n\omega t + \theta_n) \end{aligned}$$

where ω is the angular chopping frequency defined as

(2.7)

$$\omega = \frac{2\pi}{T} \quad \text{rad/s}$$

V_e evaluates as

(2.8)

$$V_e = \frac{1}{T} \int_0^T v_e \, dt = \frac{1}{T} \left[\int_0^{DT} E \, dt + \int_{DT}^T 0 \, dt \right] = DE$$

Both a_n and b_n are determined by standard application of Fourier analysis and are given by

(2.9)

$$a_n = \frac{2}{T} \int_0^T v_e \sin n\omega t \, dt = \frac{2}{T} \int_0^{DT} E \sin \frac{2n\pi t}{T} \, dt = \frac{E}{n\pi} (1 - \cos n\omega DT)$$

and

$$b_n = \frac{2}{T} \int_0^T v_e \cos n\omega t \, dt = \frac{2}{T} \int_0^{DT} E \cos \frac{2n\pi t}{T} \, dt = \frac{E}{n\pi} \sin n\omega DT$$

therefore;

(2.10)

$$c_n = [a_n^2 + b_n^2]^{\frac{1}{2}} = \frac{\sqrt{2}E}{n\pi} (1 - \cos n\omega DT)^{\frac{1}{2}}$$

and

$$\theta_n = \tan^{-1} \frac{b_n}{a_n} = \tan^{-1} \frac{\sin n\omega DT}{1 - \cos n\omega DT}$$

The similarity between Equation 2.4 and Equation 2.8 can be explained using a different, but just as valid, analysis of the operation of a buck chopper. The chopper generates a signal whose components are the average dc term, V_e and an infinite series of high frequency sine and cosine terms. The fundamentals of the sine and cosine series are at the switching frequency, $1/T$. In order to recover only the average dc term and any variations that occur in it, the second circuit, a second-order low-pass filter, suppresses the high frequency ac terms.

The low-pass filter circuit is simply an LRC network. The resistor represents the load. Since the first circuit is only a voltage source and all the reactive components are in the second circuit, only the second circuit needs to be analyzed to find the governing state equations from which a state space based model can be developed. The modulation of the input can be handled external to the state space with use of a multiplier as modeled in simulation. Thus,

(2.11)

$$L \frac{\partial i_L}{\partial t} = v_e - v_C$$

and

(2.12)

$$C \frac{\partial v_C}{\partial t} = i_L - \frac{v_C}{R}$$

define the operation of the second circuit. These equations can be expressed in the following state space form

(2.13)

$$\dot{x} = Ax + Bu$$

where the state variables are

(2.14)

$$\mathbf{x} = \begin{bmatrix} i_L \\ v_C \end{bmatrix}$$

and the derivatives of the state variables are

(2.15)

$$\dot{\mathbf{x}} = \begin{bmatrix} \frac{\partial i_L}{\partial t} \\ \frac{\partial v_C}{\partial t} \end{bmatrix}$$

and the input matrix is

(2.16)

$$\mathbf{u} = \begin{bmatrix} v_e \\ 0 \end{bmatrix}$$

The characteristic matrix is defined as

(2.17)

$$\mathbf{A} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$$

and the input matrix is

(2.18)

$$B = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 0 \end{bmatrix}$$

The output of the system can be expressed as a linear combination of the states and the inputs

(2.19)

$$y = Cx + Du$$

For simulations the output variables were chosen to be the state variables so that Equation 2.19 reduces to

(2.20)

$$y = Cx$$

where

(2.21)

$$y = \begin{bmatrix} i_L \\ v_c \end{bmatrix}$$

and C is the identity matrix.

B. NSWC/PPI POWER CONVERTER MODULE

1. Description

Two 100 kW buck converters based on the schematic of Figure 2.3 have been built for evaluation in the DC ZEDS system being installed at NSWC, Annapolis. This is the target platform for the present controller. The final evaluation will include six of the

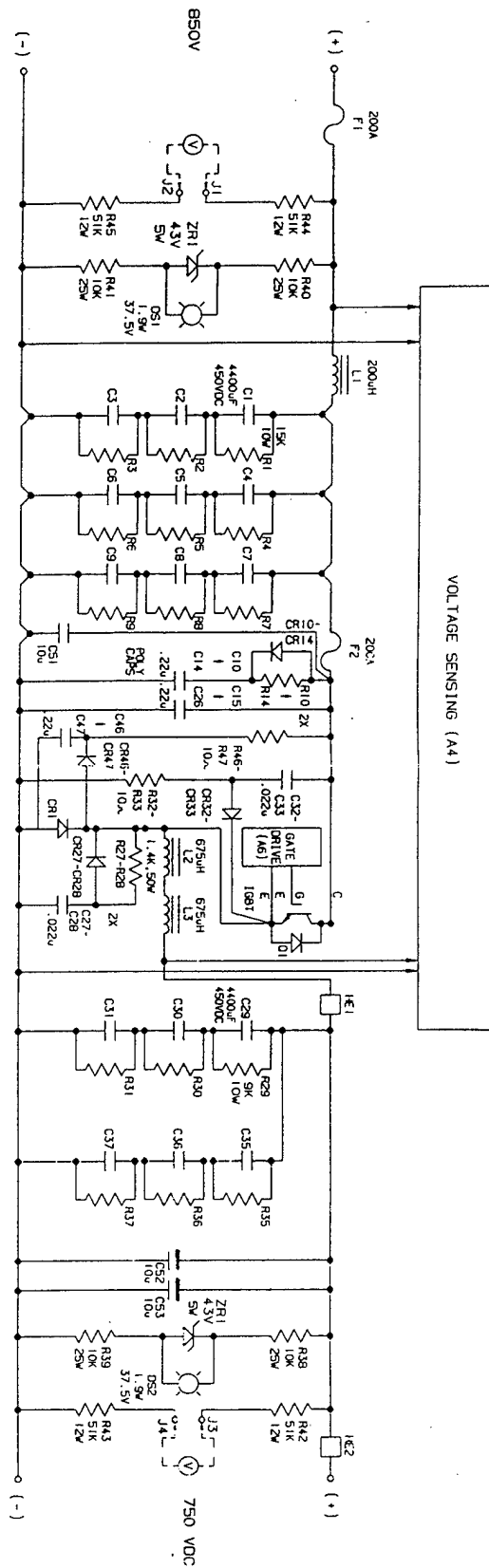


Figure 2.3. 100 kW Buck Converter Schematic [From Ref. 8]

prototype SSCMs. The SSCMs design is a more advanced version of the basic buck converter described in section A. Additional circuits were required to minimize the choppers impact on the feeder supply bus and compensate for real-world phenomena which can cause destructive voltage transients. These circuits include snubbers and an input filter.

a. The Chopper

The chopper functions as described in subsection A.2.c. The IGBT device, Q1, serves as the chopper's switch. It is driven by a 5 kHz pulse width modulated (PWM) signal from the gate driver. Diode CR1 freewheels and provides a path for the current when Q1 is off.

b. Snubber Circuits

The snubber circuits reduce transient voltage ringing and therefore reduce IGBT voltage stress that could cause catastrophic failure of the switch. This is accomplished by the two parallel circuits composed of C32-33, R32-33 and CR32-33. The circuit, comprised of CR46-47, C46-47, and R46-47, perform the same function on diode CR1. In addition, the snubbers share the switching loss when the IGBT turns off. This is accomplished by C27-28, R27-28, and CR27-28. Additional circuits comprised of C10-14, CR10-14, C15-26, and R10-14 offer protection by reducing dc bus transients and limiting dc bus overshoot.

c. Input Filter

The input filter prevents the current surges from the switching action of the chopper from influencing the feeder supply bus, and, provides a near-solid dc voltage source for the buck chopper with the minimal variations inherent to the feeder supply bus. The input filter inductor, L1, ensures that the input current is close to an ideal dc current. The capacitor bank, C1-9, provides 4400 μF of capacitance to minimize voltage fluctuations caused by the ripple current due to switching. Resistors, R1-9, in addition to providing the capacitors a discharge path when the power is secured, are used to equalize any difference in the voltage potential across each of the series capacitors. This difference may develop from trapped charges or different dielectric leakage currents.

Without the resistors it is very possible and probable that one of the capacitors would exceed the 450 WVDC rating and fail. A 10 μ F polypropylene capacitor is shunted across the capacitor bank to reduce the ESL of the DC capacitors.

d. Output Filter

The output filter functions as discussed in Section A.2.c. The inductor of the typical buck converter is actually two separate inductors, L2-3, in this application. The use of two inductors minimizes the internal capacitance effect of a heavily wound single inductor. The inductors combined value is 1.35 mH. The filter's capacitor is a bank of capacitors, C29-31 and C35-37, configured similar to that of the input filter. Its combined capacitance of 2933 μ F results in the resonant frequency of the output filter of 80 Hz, well below the 5 kHz switching frequency. Capacitors, C33-34, reduce the ESL effect of the DC capacitors. Resistors R29-31 and R35-37 function identically to their counterparts in the input filter.

2. General Ratings

The following ratings apply to the 100 kW SSCM operating at a 50 kW prototype imposed power limit:

Power output:	$P_{out} = 100 \text{ kW}$
Switching Frequency:	$1/T = 5 \text{ kHz}$
Input Voltage:	$V_{in} = 850 \pm 25 \text{ Vdc}$
Output Voltage (normal regulated):	$V_{out_norm_reg} = 750 \text{ Vdc}$
Maximum Output Voltage (regulated):	$V_{out_max_reg} = 790 \text{ Vdc}$
Minimum Output Voltage (regulated):	$V_{out_min_reg} = 700 \text{ Vdc}$
Full Load Output Current:	$I_{out_fl} = 133.3 \text{ Adc}$
Overload Current Limit (125%):	$I_{overload} = 166.6 \text{ Adc}$ for two seconds
Current Limit (150%):	$I_{limit} = 200 \text{ Adc}$ for one second

3. Controller Interface

a. IGBT Driver

The controller developed by NPS interfaces with the IGBT switch of the 100kW SSCM through a proprietary IGBT gate driver circuit. Schematics of the IGBT gate driver circuit can be obtained from PPI [Ref. 8]. The controller sends two gating

signals to the IGBT gate driver circuit via separate control lines. One signal is a 15 volt pulse to gate "on" the IGBT, and the other is a 15 volt pulse to gate "off" the IGBT. The IGBT driver circuit is activated by the leading edge of the pulses and provides the correct bias to the B-E junction of the IGBT to turn it on or off. In steady-state operation, the time between the leading edge of the first gating pulse and the leading edge of the second gating pulse is proportional to DT of Equation 2.1. The IGBT driver provides isolation between the low voltage controlling hardware and the high-voltage switching hardware through transformer coupling. Power to the IGBT driver circuit is also transformer isolated from the high voltage. A special 48 volt, 15 kHz power supply provides power to the IGBT driver through a transformer. The output of the multiple secondaries of the transformer are rectified and filtered to provide the required voltages for the IGBT gate driver circuit.

The IGBT driver interprets the control signals with a high power bistable multivibrator. The "on" signal latches the bistable's output low and an "off" signal latches the bistable's output high. The signal from the bistable multivibrator is applied to a high current inverter driver. The output of the inverter driver is connected to the base of the IGBT. Additional circuits provide protection for the IGBT by turning the IGBT gate driver off should a sustained high-voltage condition occur on the IGBT's B-E junction.

b. Voltage Sensors

Three voltage signals are provided to the controller from the SSCM power circuits. The input voltage and the output voltage signals are 1/100th their original values, and the 24 volt control voltage is supplied directly. The input and output voltage signals are provided by a proprietary AC/DC transducer. Schematics of the circuit can be obtained from PPI [Ref. 8]. The transducer circuit performs both signal conditioning and voltage isolation. The measured parameter is first reduced by a voltage divider to 1/100 of its original value. An AD210 three port isolation amplifier then provides the voltage isolation and a one-to-one voltage gain. The signal from the isolation amplifier is applied to a buffer/driver stage that both allows for a fine gain adjustment and provides a low output impedance. The transducers circuit is also isolated from its 24 volt power source

with a DC to DC converter, thereby providing total isolation of the voltage signals from the SSCM power circuits.

c. Current Sensors

Two current signals are provided to the controller from the SSCM power circuits. The signals represent the value of the inductor current and output current. The signals originate from two NNC-20GA Hall effect sensors manufactured by Nana Electronics. The Hall effect device allows isolation of the sensor from the power circuits. The sensors have built in amplifiers that receive power from a +/- 15 volt power supply present specifically for this purpose. The sensors provide a four volt output for every 200 amps sensed.

C. NPS BUCK CHOPPER (1 kW - 4 kW)

1. Description

The NPS buck chopper is a scaled down development version of the 100 kW prototype (Figure 2.4). All voltages and currents are 1/10 the value of those on the final prototype. This results in a significant reduction in the power requirements (1/100th) for full-load testing with minimal impact on the results. The lower operating voltages and currents allowed construction of a 5 kHz buck chopper from "in house" components. Plagued with a power source that displayed significant droop at higher loads, the scaled version was also able to minimize this droop and allow transient testing from minimum to maximum loads.

a. Snubberless Chopper

The buck chopper was constructed in such a manner as to eliminate the need for any resistive snubber networks. The snubberless design was accomplished by placing all components within close proximity of each other and using a 3/4 inch wide and five inch long strip of copper for the common negative node. The buck chopper has a 470 μ F input filter capacitor, C1, to minimize the effect of any inductance in the source and associative cabling (Figure 2.5). C2, a .6 μ F capacitor, reduces the amplitude of any transient ringing on the supply side caused by the IGBT switching. It is comprised of

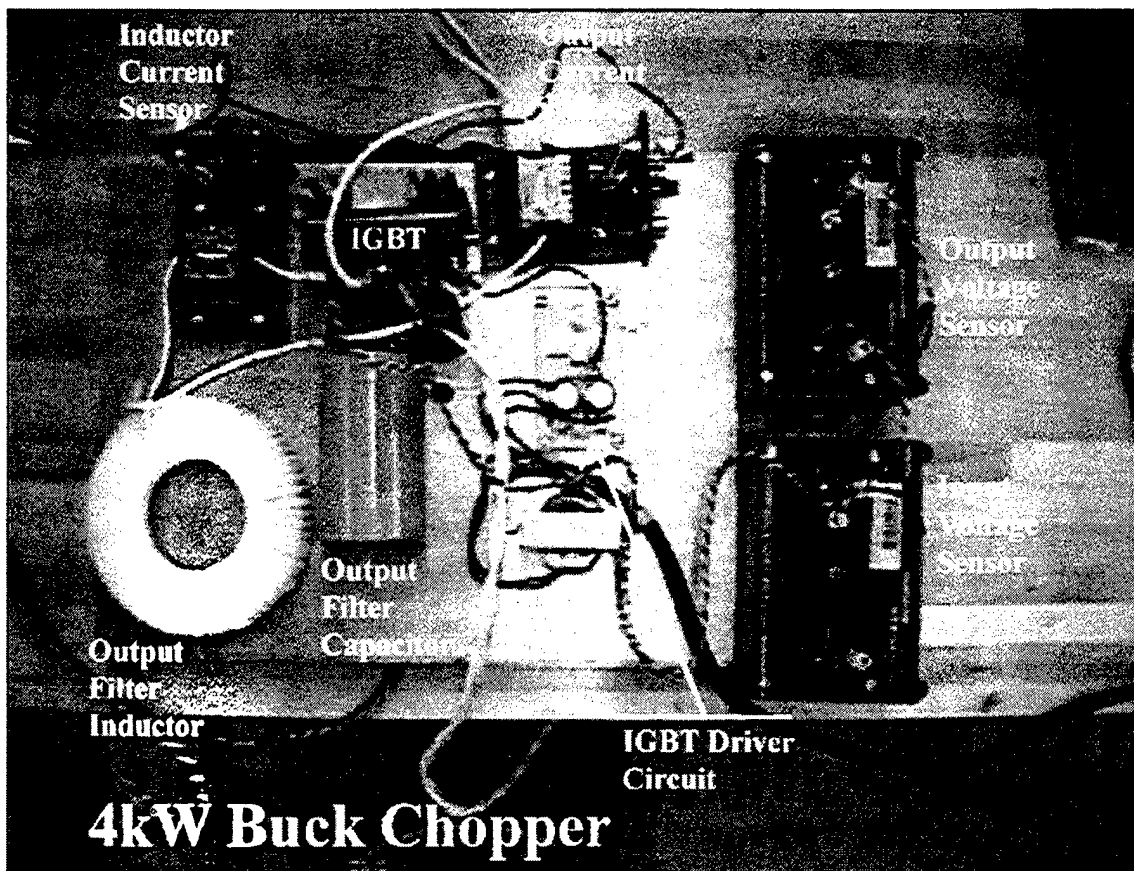


Figure 2.4. NPS Buck Chopper

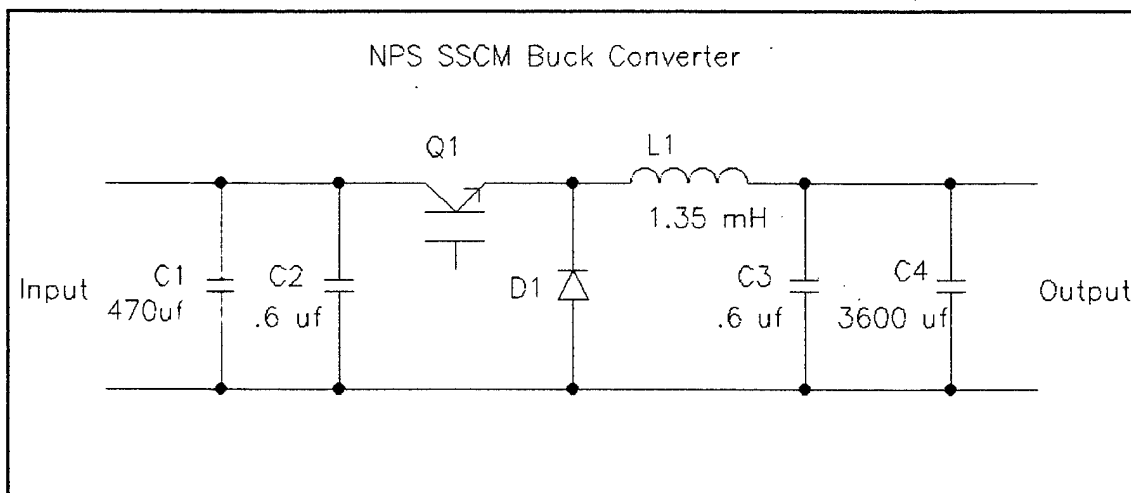


Figure 2.5. NPS Buck Chopper Schematic

three .2 μF capacitors in parallel mounted directly to the IGBT, Q1. The IGBT switch is one half of a symmetric dual IGBT (Toshiba MG50Q2YS9) with the second IGBT disabled (not shown). Both IGBTs have internal diodes. The diode for Q1 is not shown. D1, the free-wheeling diode, is the diode for the second IGBT. This allows the design to have both the switch and diode in the same package, minimizing the distance, and thus the transients during switching.

b. Output Filter

The output filter is comprised of an inductor and two parallel capacitors. The inductor, L1, is based on a 6" toroid core wrapped with 75 turns of #10 wire. This resulted in a highly efficient inductor that displayed no saturation throughout the testing and at currents exceeding 20 amps. The correct number of turns for 1.35 mH was determined by trial and error measurements since no core information was available. The finished inductor was dipped in wax in an attempt to minimize the noise generated during switching operations and increase the mechanical stability of the winding.

The output filter capacitor, C4, is a 3900 μF capacitor. This capacitance is higher than the 2933 μF of the 100 kW prototype and was replaced with a more conservative 2400 μF on the second buck converter assembled at NPS. The resonant frequency of the output filter at 3900 μF is 69.4 Hz, compared to 80.0 Hz for the 2933 μF and 88.4 Hz for the 2400 μF . All resonant frequencies are well below the 5 kHz switching frequency, although the transient response is more pronounced with the smaller output capacitance.

2. General Ratings

The NPS SSCM prototype was rated so as to be similar to the 100 kW SSCM prototype. This facilitated controller development that would easily map to the large SSCM when full-scale testing occurs. The ratings do not reflect the true capability of the NPS buck chopper. In laboratory testing, the buck chopper has sustained loads greater than four kilowatts with no degradation. The following ratings apply to the NPS SSCM prototype:

Power output:	$P_{out} = 1000 \text{ W}$
Switching Frequency:	$1/T = 5 \text{ kHz}$
Input Voltage:	$V_{in} = 85 \pm 7 \text{ Vdc}$
Output Voltage (normal regulated):	$V_{out_norm_reg} = 75 \text{ Vdc}$
Maximum Output Voltage (regulated):	$V_{out_max_reg} = 79 \text{ Vdc}$
Minimum Output Voltage (regulated):	$V_{out_min_reg} = 70 \text{ Vdc}$
Full Load Output Current:	$I_{out_fl} = 13.3 \text{ Adc}$
Overload Current Limit (125%):	$I_{overload} = 16.6 \text{ Adc}$ for two seconds
Current Limit (150%):	$I_{limit} = 20 \text{ Adc}$ for one second

Actual performance met the ratings in all areas. The input voltage range was expanded from the ± 2.5 volts that the 1/10th scaling would have suggested, to ± 7.0 volts. This change was to compensate for the droop in the laboratory power source during large loads and is more conservative and demanding on the controller.

3. Controller Interface

a. IGBT Driver

The NPS controller sends a single PWM signal to gate the IGBT in the 1kW SSCM prototype. This differs from the two signals used in the 100 kW SSCM. The signal, a 15 volt pulse, is applied via a 270 ohm limiting resistor, R1, to the LED of the TLP250 photocoupler, U1 (Figure 2.6). When the pulse is high the TLP250 applies 15 volts to the isolated gate base-emitter junction of the IGBT, Q1. When the pulse is low the TLP250 applies -15 volts to the junction to quickly force the IGBT off. The duration of the pulse directly corresponds to the ordered duty cycle. The photocoupler optically isolates the controller from the buck chopper. Power for the IGBT driver comes from the dual voltage full wave rectified supply of transformer TX1 and diodes D2-5. Capacitors C5-6 filter the supply voltages and minimize the effect of any capacitive coupling from the primary to the secondary of TX1. Bypass capacitor C7 removes switching transients from the supply voltages during the high slew rate transitions of the TLP250.

The circuit was located close to the IGBT to minimize the wire length from the TLP250 to the IGBT. This minimizes the ringing on the base of Q1. In addition, the 15 volt Zener diodes, D6-7, protect the IGBT static sensitive isolated gate

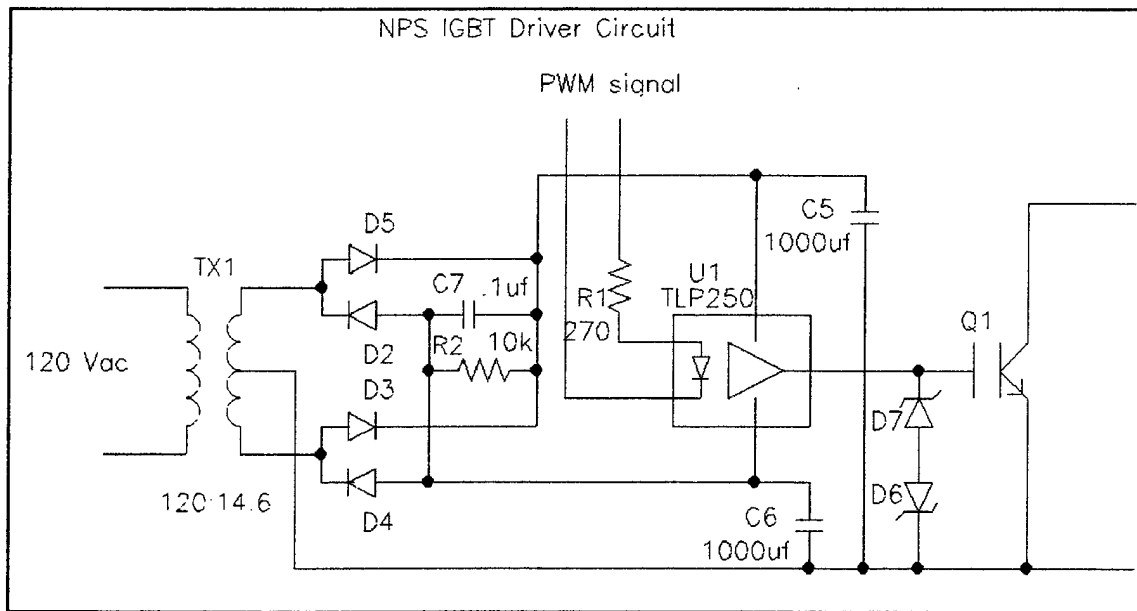


Figure 2.6. NPS IGBT Gate Driver Schematic

base-emitter junction from any excessive voltages.

All components of the IGBT driver circuit with the exception of the transformer are mounted on a perforated development board. The transformer, the IGBT driver circuit and the components that make up the buck chopper are mounted on a 3/8 inch aluminum sheet. This provides rigidity to the assembly and allows access to the components during the development that an enclosure would not permit. The sheet is grounded to the laboratory bench through the third wire of the three prong plug that provides power to the IGBT driver transformer.

b. Voltage Sensors

Both input and output voltages of the NPS buck chopper are sensed using L109VIB voltage isolators. The isolators are NPS Power Systems laboratory equipment and provide a 100:1 volt reduction of the measured voltage, the same as the 100 kW versions. The isolators are powered from the +15 volt power supplies provided in the lab. The outputs of the voltage isolators connect to the controller.

The 24 volt signal of the 100 kW SSCM is mimicked with a variable DC power supply. The voltage is sent directly to the controller.

c. Current Sensors

Two LT 100-S Hall effect current sensors are used to monitor the inductor and output current of the NPS buck chopper. The current sensors provide an output current that is 1/1000th the value of the measured current. A 100 ohm resistor is used to obtain a 10 A/V output to the controller. Power for the Hall effect comes from the +15 and -15 power supplies available in the NPS Power Systems lab.

III. BUCK CHOPPER PWM CONTROLLER

A. GENERAL REQUIREMENTS

The NPS controller design is based on meeting specific functions implemented in hardware and/or software. Software implementations allow future upgrades to the controllers without hardware replacement or modification. The specific functions can be classed as primary or auxiliary. The primary functions are those that directly support the generation of the duty cycle for the buck chopper. Auxiliary functions support protective actions, mode control, and external communications with remote monitoring or controlling stations.

1. Primary Functions

a. IGBT Gate Driver Signal Generation

The controller generates a switching signal that is compatible with the appropriate IGBT gate driver. The signals are based on the ordered duty cycle as determined by the controller. Two signals are generated for the NSWC/PPI interface. These signals are each a series of pulses at the switching frequency. The leading edge of the pulses in the first signal turns the IGBT on, the leading edge of the pulses in the second signal turns the IGBT off. Only one signal is generated for the NPS interface. It is a PWM signal at the switching frequency with a pulse duration directly proportional to the ordered duty cycle.

b. Control Parameter Sensing

The controller senses the value of four parameters from which the current state of the SSCM is determined. Each specific signal originates from an individual sensor in the power section of the SSCM. All signals are voltage levels that represent the present value of their respective measured parameter. The signals are conditioned by the controller before being used in the determination of the duty cycle. The parameters measured and available for the control algorithm are input voltage, output voltage, output current, and inductor current. The input and output voltages are measured across the input and output filter capacitors, respectfully. The output current is measured at the load

side of the output filter with a Hall effect sensor. The inductor current is measured on the IGBT side of the inductor with an additional Hall effect sensor.

c. *Duty Cycle Determination*

The controller attempts to maintain the output voltage at a predetermined reference level by generating the correct duty cycle for the pulse width at which the IGBT switches. It also minimizes the fluctuations in the output voltage during load transients. The algorithm accepts the reference voltage and the measured parameters from which it determines the required duty cycle. The algorithm is implemented in both software and hardware.

2. Auxiliary Functions

a. *Mode Control*

The reference level used by the controller originates from one of three sources. The specific source used is determined from the controller's operating mode which is selected by two single throw switches on the front of the controller (Table 3.1). One switch is for setting local or remote control of SSCM's operation. The remote control of the SSCM is not implemented at present. When remote is selected the reference voltage is zeroed, the PWM is disabled, and all protective trips are reset. The other switch establishes the parallel or single operation of the SSCM. Parallel operation is designed to allow multiple SSCMs to supply a single load. When the controller is in parallel operation and local control the reference is based on a constant value internal to the software. When the controller is in the single operation and local control the reference voltage is based on adjustments to potentiometers on the front of the controller.

b. *Protection*

The controller provides protective trips for excessive output current, high temperatures and loss of 24 volt control power for the power conversion section of the SSCM. The output current and 24 volt control power protective trips are implemented in hardware and are monitored by the software. The hardware receives and conditions voltage signals representing the measured parameters of output current and 24 volt control power. If a trip condition exists, the hardware sends a disable signal to the PWM.

Table 3.1. Reference Voltage Source

Local / Remote Switch	Local	Local	Remote	Remote
Parallel / Single Switch	Single	Parallel	Single	Parallel
Source of Reference Voltage	External Potentiometer	Software Based on Constant	Software Set to Zero	Software Set to Zero

The software will also send a disable signal to the PWM should any of the protective trips occur or if the controller is in parallel control mode. The software is responsible for resetting the protective trip circuits. This is accomplished after clearing the condition which caused the trip by momentarily taking the local / remote switch to remote and then back to local.

Pulse-by-pulse current limit is an additional protective feature which is fully implemented in the hardware and has no software interface. It receives a voltage signal representing the instantaneous inductor current and disables the output of the PWM should the current exceed the limit. When the current has decreased below the limit the protective action only lasts until the end of the present IGBT switching period. Table 3.2 summarizes the protection designed into the controller.

c. External Communications

The controller sends to remote stations the current status of the controller. The information may include any of the measured parameters, the mode of the controller, and/or the state of the protective trips. The information is presently configured for the measured parameters. When remote control is incorporated into the controller, the external communications will also include control commands from the remote station. The communication's information structure is based in software. The specific protocols and structures have not been finalized in the design. The hardware medium is

Table 3.2. Controller Protection Methods

Protection	Excessive Output Current Timeout Limit	High Temperature	24 Volt Control Power	Pulse-by-Pulse Inductor Current Limit
Limit or Trip Condition	125% of maximum* for 2s OR 150% of maximum* for 1s		20 volts and decreasing	150% of maximum*
Implementation Method	Hardware with Software Monitoring	Software	Hardware with Software Monitoring	Hardware

* Maximum current is 13.3 Amps for NPS SSCM and 133 Amps for NSWC/PPI SSCM.

presently a serial RS232 link from the controller to a remote personal computer. An RS232 to RS422 aftermarket converter exists for the final serial communication interface.

B. ADDITIONAL DESIGN CONSIDERATIONS

1. Parallel Operation

The SSCM must be able to operate as an independent unit, yet work in parallel with other SSCMs to supply power to large loads. In addition, the SSCM must continue to maintain the output voltage under variations in line or load while it is in parallel operation. To obtain correct load sharing, a voltage droop was incorporated into the controller. The voltage droop effectively programs the output impedance of the SSCM. but this, in turn, degrades the load regulation and prohibits zero voltage regulation. Even with these disadvantages, the droop method best suits the SSCMs requirements.

Four methods of load sharing were considered. The methods were voltage droop, dedicated master, external controller, and automatic current sharing. Dedicated master involves selecting one unit to perform the voltage control and the rest of the units act as

current sources. This method offers no redundancy and requires reconfiguration of units for current mode. In addition, load reductions can cause a loss of voltage regulation; specifically when the output of the current sources exceeds the load current at the regulated voltage. The next method uses an external controller to measure the total load current and then send control signals to each SSCM. This method requires additional hardware and connections to each controller. The SSCMs are no longer independent and failure of the external controller will cause failure of the system. Automatic current sharing involves an additional bus between all the SSCMs. The bus would have a signal representing the highest or average current of all the SSCMs. Each SSCM would adjust its respective voltage to optimize sharing of the load by minimizing the difference between the signal of the shared bus and the output current of the respective SSCM. This method requires additional hardware and connections to the SSCMs.[Ref. 9]

The droop method was chosen for its simplicity, robustness, and its minimal change to the hardware. It benefits from the fact that the SSCMs are identical in capabilities and programming. The droop method offers redundancy and reliability over the other methods. The voltage droop was implemented by reducing the reference voltage of the controller by an amount proportional to the output current.

2. Redundant Control

The control algorithm is implemented in both software and hardware for redundancy. The DSP boards mandated for the project provided inconsistent results and proved to be unreliable with four complete failures and replacements during development. An analog hardware control algorithm was completed to allow testing and refinement of the controller. It was incorporated into the final controller design as a backup. It offers a complete analog version of the control algorithm used with the DSP. The redundant control also provides a means of comparison which could be used to detect any performance degradation of the digital controller.

IV. CONTROLLER ALGORITHMS PERFORMANCE ANALYSIS

A. OVERVIEW

The selection of the optimum control algorithm was based on the comparison of the simulated performance of various potential algorithms. Four of the controller algorithms considered are presented here to document the rationale as the foundation of support for the choice of the implemented algorithm. The algorithms include: linear feed-forward, integrator based feedback, multiloop feedback, and state difference feedback. The state difference feedback algorithm is implemented in the design.

Performance evaluation primarily concentrates on the step change transient response. This is accomplished by a prompt increase or decrease of the load in the simulation, and is easily reproduced with the actual SSCM in the lab. Simulations were achieved through the use of a software extension to the MATLABTM high performance numeric computation and visualization software. The software extension, SIMULINKTM, allows construction and simulation of systems which are modeled by objects in a graphic environment [Ref. 10].

B. SIMULINK ENVIRONMENT

The system models are implemented in two distinct levels. The highest level is the graphic interface of Simulink. At this level the various graphic objects that represent the system components are connected with lines which represent the signal paths between the components. The specific components can be obtained from the included Simulink libraries or constructed by the user. Once the required variables are initialized, the simulation can be started from the Simulink window (Figure 4.1).

The second level is the workspace of Matlab itself. At this level the variables are initialized and records are maintained for the plots. In addition, commands issued at the Matlab command window force the change of variables during the simulations, and direct the compilation and plotting of the data. Two types of commands are issued. The first type is a call for an m-file script. An m-file script is a series of Matlab commands that execute each time the script is called. The second type of command is the

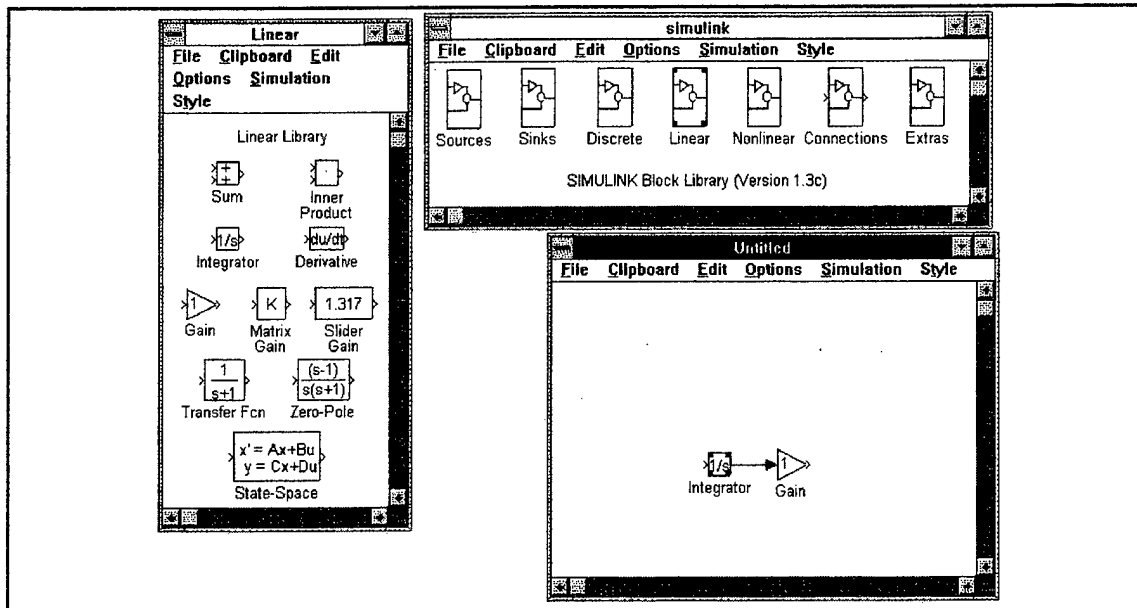


Figure 4.1. Simulink Graphic Interface and Libraries

assignment of a new value to a variable. This allows the user to change parameters between runs to simulate prompt changes in load. Both are illustrated in Figure 4.2.

Simulink models are generally simulated through the integration of a set of ordinary differential equations [Ref. 10]. Fifth-order Runge-Kutta was selected as

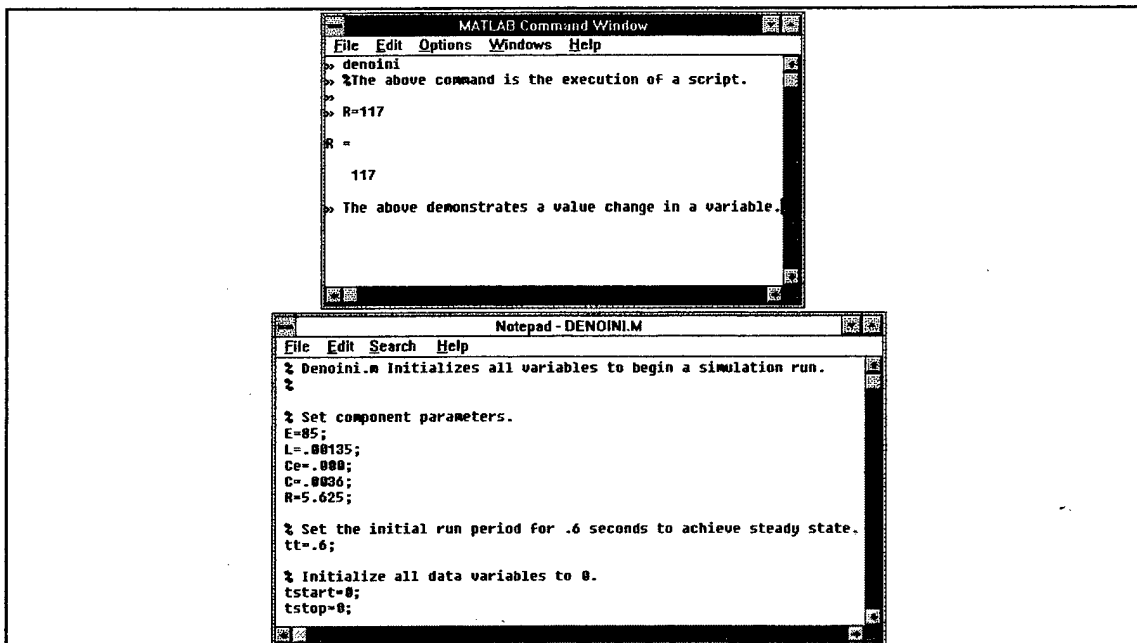


Figure 4.2. Matlab Command Window and Sample M-file

the algorithm to numerically integrate this set of equations. The method works well with mixed continuous and discontinuous systems. The accuracy of the method is based on a preselected minimum time step size and tolerance band for the solution. While minimizing either will help simulation accuracy, it also demands more computations and therefore more time. In addition, with increased accuracy, comes larger data bases for plotting that can further slow down the process. The minimum time step size selected for simulations was two microseconds and the tolerance was the default of .001.

The simulations were executed on an AMD 486DX4-100 based personal computer under the Windows for Workgroups™ version 3.11 graphic user interface which was layered on top of the MS DOS™ version 5.0 operating system. The computer is equipped with 48 megabytes of 70ns DRAM and over 1.4 gigabyte of harddrive.

The basic procedure followed for completion of a model simulation is illustrated in Figure 4.3. The m-files contents vary from model to model. The m-files for the state difference feedback simulations are enclosed as Appendix A.

C. STATE SPACE SIMULATIONS

The state space simulations were developed for resistive and capacitive loads. The capability to simulate capacitive loads is present in all models, but is only used in the model of the actual control implementation. The simulations use a state space model for only the LRC network of the output filter (Chapter II). The output filter's components became a single Simulink object which simplified the simulations and increased simulation performance. The input signal to the state space is based on the average voltage of Equation 2.7. This ignores the high frequency components of the PWM signal that are successfully suppressed by the output filter. Figure 4.4 is a frequency plot of a Pspice simulation of the output filter. It demonstrates the extent to which these high-frequency terms are suppressed. A one volt sinusoidal signal at the switching frequency is reduced to 0.3 millivolts at the output.

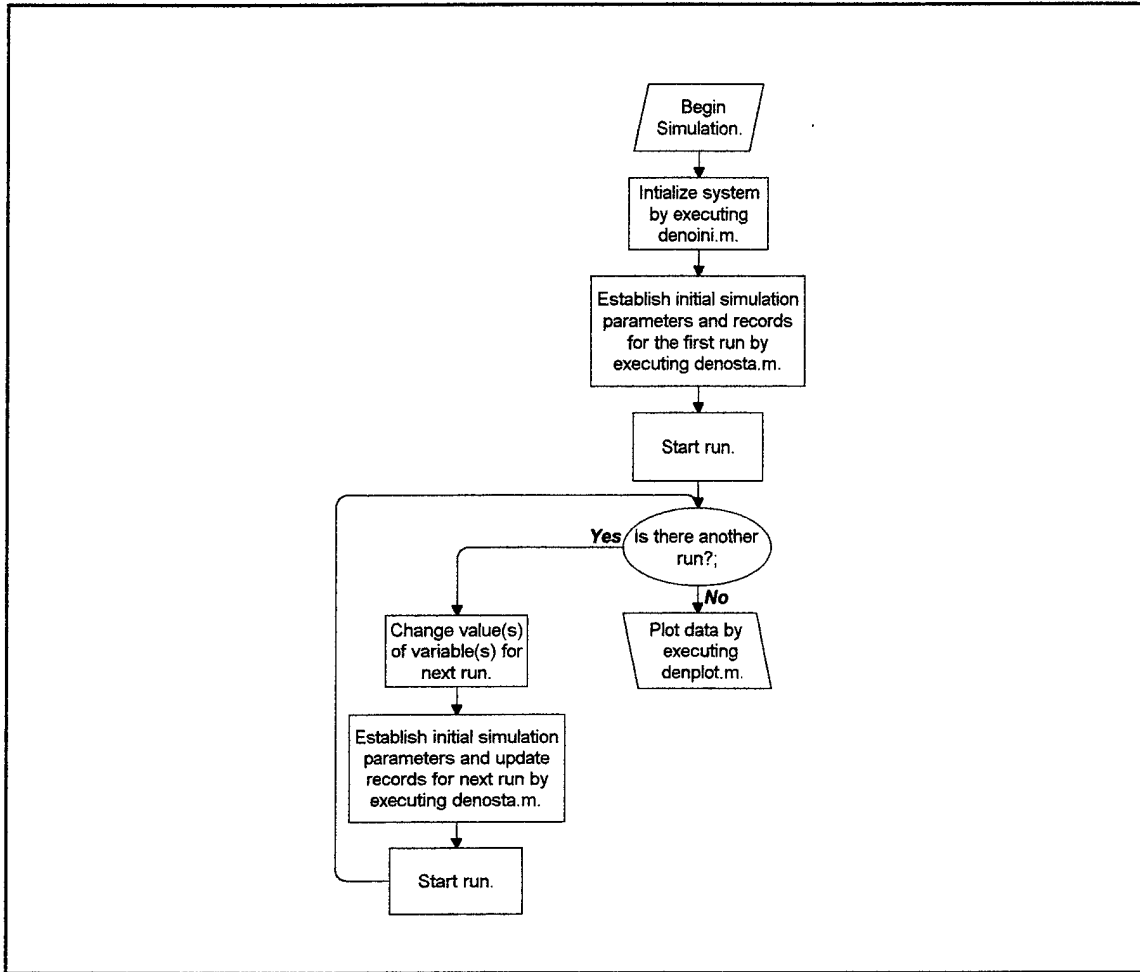


Figure 4.3. Flow Chart of Simulation Process

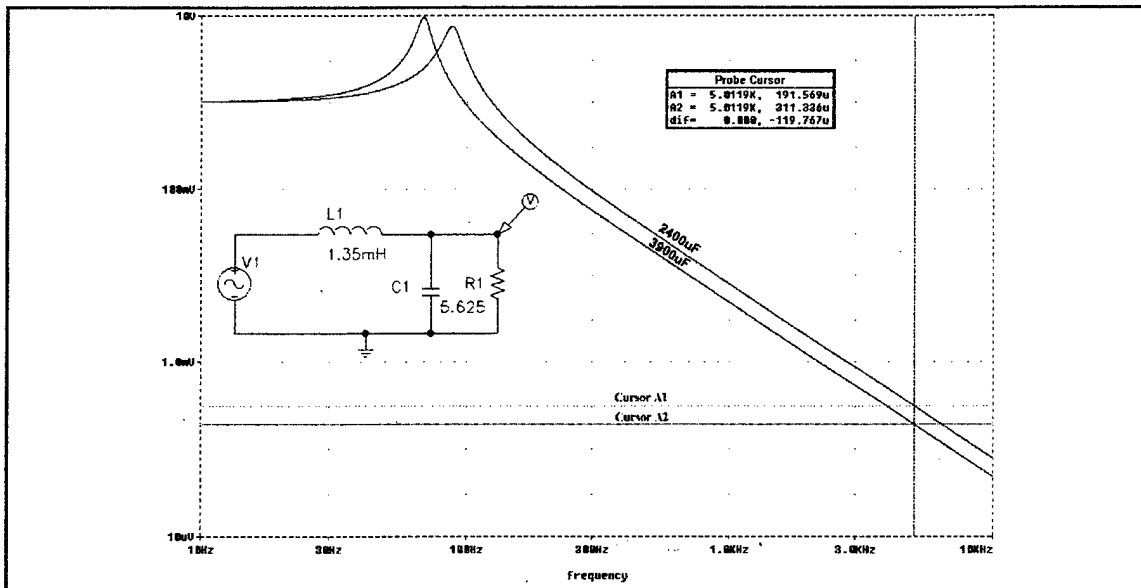


Figure 4.4. Pspice Output Filter Simulation

1. Linear Feed Forward

The simplest method of control is based on Equation 2.4 for the steady-state duty cycle. The duty cycle is determined from the ratio of the desired output voltage to the input voltage (Figure 4.5). This desired output voltage is the reference voltage in all control schemes investigated. Feed forward can achieve good steady-state regulation in low-loss buck choppers as long as the buck chopper is operating in the continuous mode where the governing equations are valid. Its major failing is with transients. The values of L and C required to filter the chopping frequency for a specific load are always such that the load resistance is not small enough to effectively damp the resonant peak [Ref. 7 pg 367]. A small change in the load can cause the output filter to resonate and create large voltage peaks that would be detrimental to downstream loads (Figure 4.6).

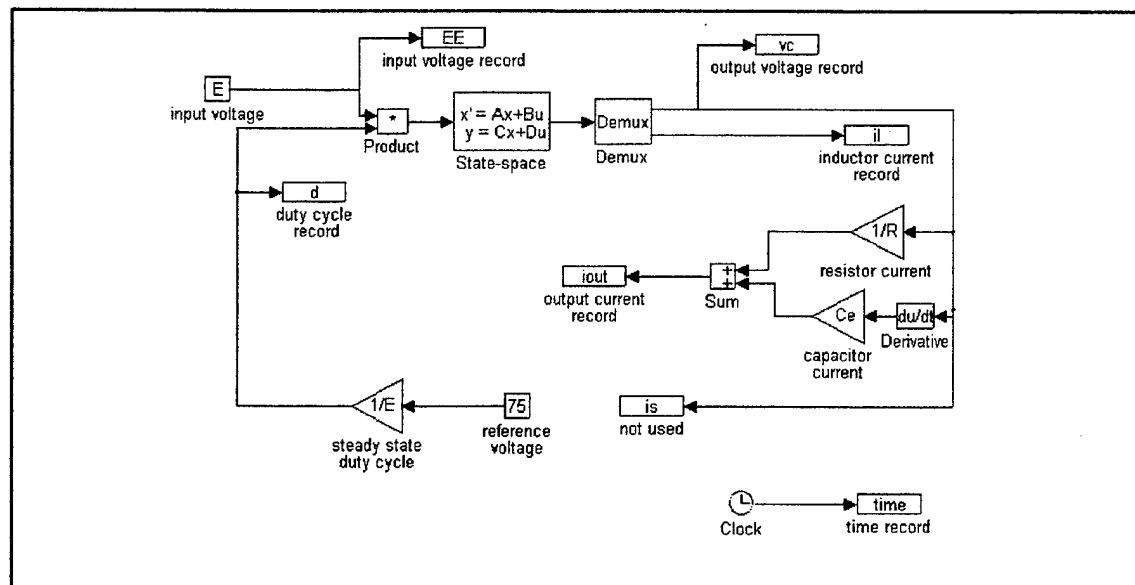


Figure 4.5. Linear Feed Forward Simulation

The feed forward control eliminates any coupling of variations in the input voltage to the output of the buck chopper (Figure 4.7). This makes feed forward a highly desirable component of other control schemes.

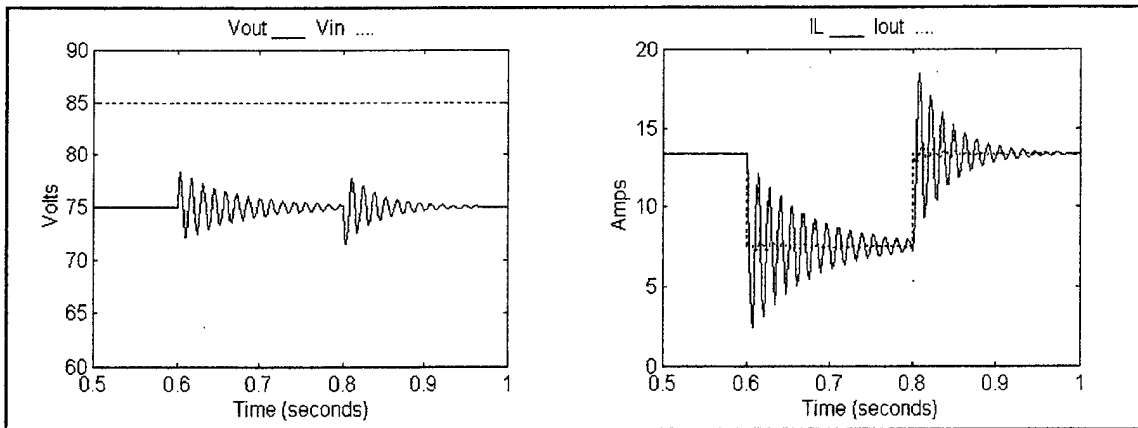


Figure 4.6. Linear Feed Forward with Resistive Load Change

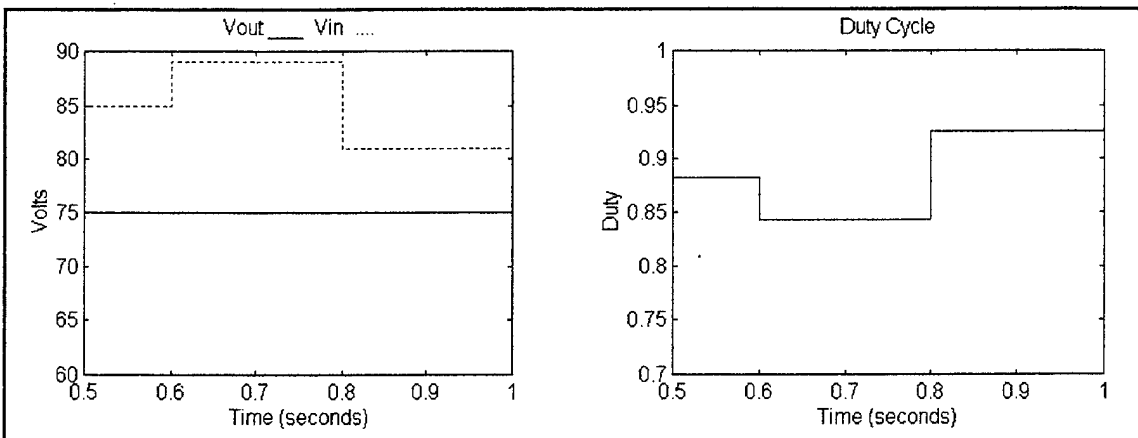


Figure 4.7. Linear Feed Forward with Input Voltage Change

2. Integrator Based Feedback

An integrator control can achieve zero-voltage regulation which is not possible with the linear feed forward control. The integrator control functions by first creating an error signal based on the difference between the output voltage and the reference voltage. The integral of the error signal then becomes the commanded duty cycle (Figure 4.8). Therefore, if the output voltage is different from the reference voltage, the duty cycle is changed to zero the error.

The integrator control will compensate for nonlinear elements that introduce a relatively fixed bias into the required duty cycle. Non-ideal switching components, such as the IGBT and diode, have small voltage drops when conducting. These voltage drops

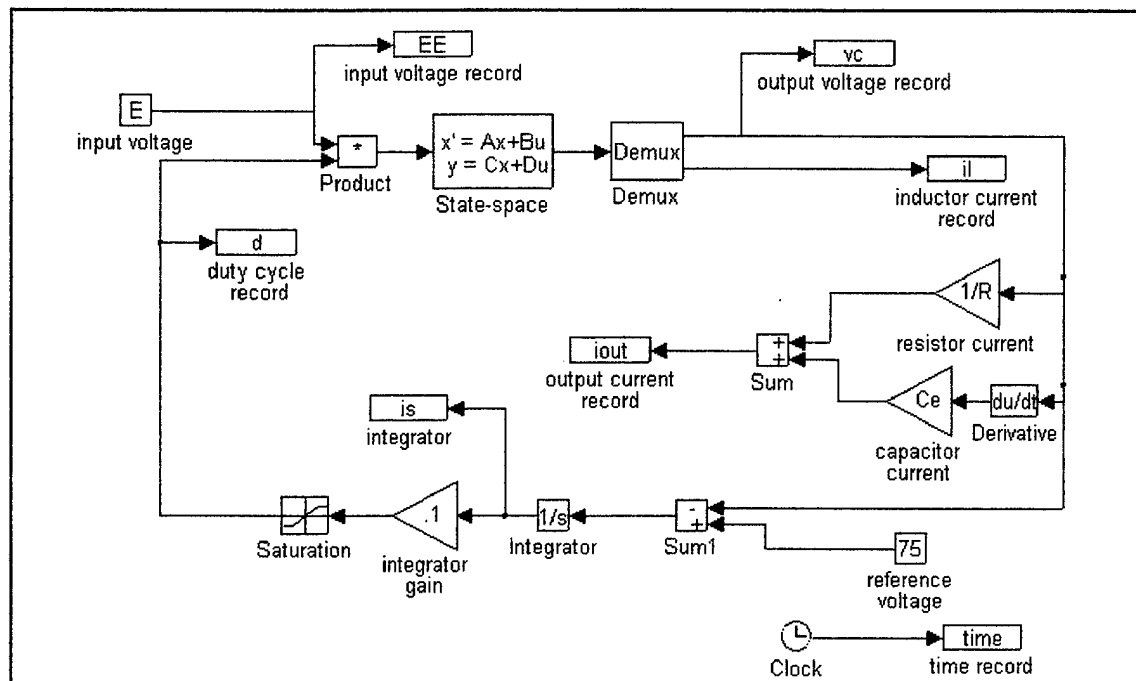


Figure 4.8. Integrator Based Feedback Simulation

will result in a voltage signal at the input to the output filter that is lower than predicted. The output voltage will also reflect this reduction. The control eliminates this problem by providing an ordered duty cycle that includes the required bias in order to overcome these voltage reductions.

The integrator control does not decouple the input source as does the feed forward method of control (Figure 4.9). Usually the integrator's gain is sufficiently low as not to excessively reduce the damping of the LRC circuit. This low gain prohibits the integrator from quickly responding to an error in the output. Therefore, an abrupt change in the input voltage can be seen on the output, and only those variations sufficiently below the frequency of the integrator will be minimized. If the input voltage sees an abrupt increase at time $t = 0$, the output voltage will see a prompt increase that is proportional to the value of the duty cycle at the time of the change multiplied by the increase in the input.

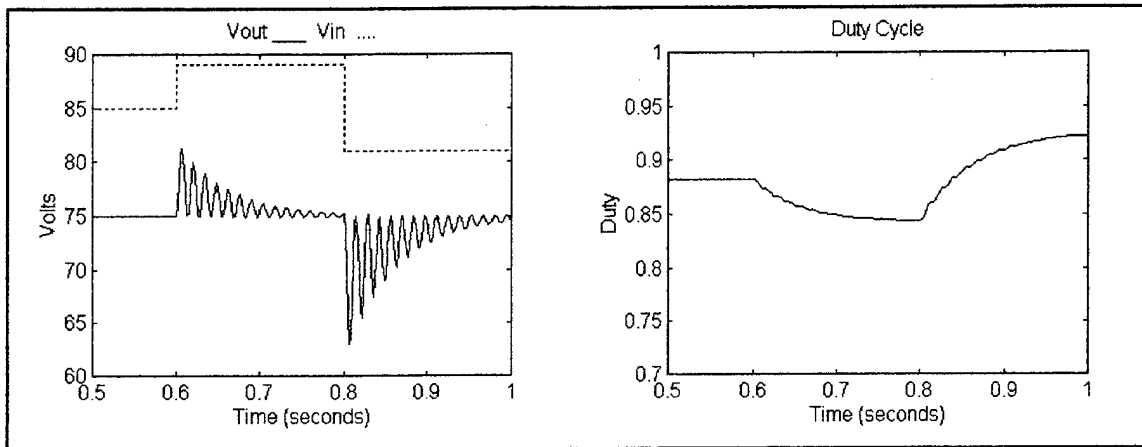


Figure 4.9. Integrator Feedback with Input Voltage Change

(4.1)

$$\Delta v_{out} = d_{t=0} \Delta v_{in}$$

This does not include any variation in the output from the resonance of the LRC network that actually results in voltage changes of almost $2(d_{t=0} \Delta v_{in})$.

The transient response of the buck chopper with integrator control is similar to that of the feed forward control method (Figure 4.10). It still suffers from the resonance of the LRC network. Specifically, it does not provide the means to adequately control the system's natural frequencies and dampen this transient. Yet, the advantage of zero voltage regulation makes it favorable as a component in a more complex control scheme.

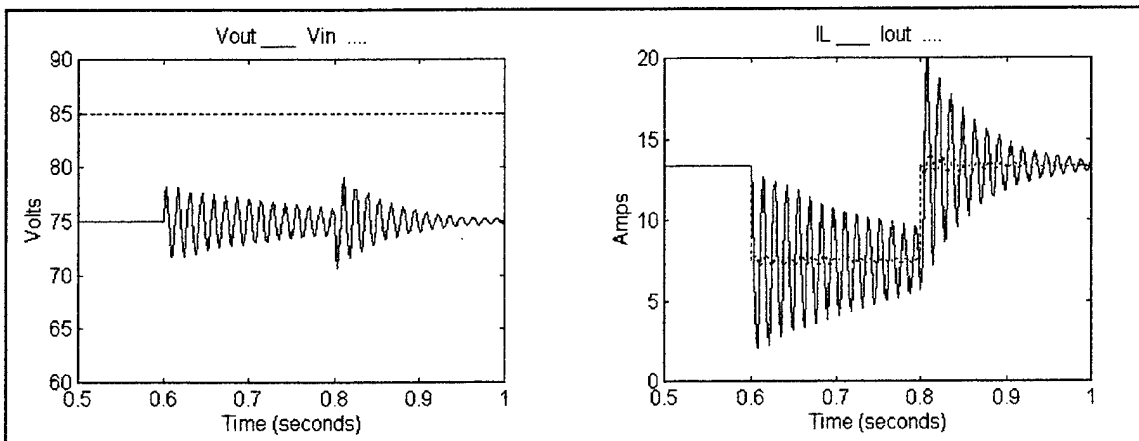


Figure 4.10. Integrator Feedback with Resistive Load Change

3. Multiloop

The transient response of both the feed forward and integrator control scheme is unacceptable. Both methods failed in their ability to adequately control the overall natural frequencies of the system. This can be primarily attributed to the fact that the state space model for the output filter involves two state variables. Multiloop involves the feedback of more than one signal. It offers an enhanced ability to control the system and reduce the effects of the LRC network by including both state variables, i_L and v_{out} , into the control.

The control law explored parallels the control law of Ref. 11, pg 387. Specifically, the control law is

(4.2)

$$d = -h_I i_L - h_V (v_{out} - v_{ref}) - h_N \int (v_{out} - v_{ref})$$

The integrator term of Equation 4.2 ensures that zero-voltage regulation occurs in the steady state. Therefore, with the reference voltage v_{ref} constant, the term $(v_{out} - v_{ref})$ equates to the perturbations in the output voltage. The inductor current referred to in Equation 4.2 is the average inductor current. Through the proper selection of the gain terms h_I , h_V , and h_N , the natural frequencies of the system can be adjusted to optimize the transient response, a rapid settling time with little overshoot.

The gains were selected to place the system poles to provide a high degree of damping and quick transient response. In addition, the highest frequency of any pole is below the switching frequency of 5 kHz. This reduces the gain requirements and keeps with the assumption that the high frequency terms of the chopper can be ignored. Finally, the imaginary components are kept smaller than the real components to avoid any undesirable oscillatory behavior. The A matrix for the state space representation of the averaged small-signal model of the system provides the information from which the system poles can be determined. Referring to Figure 4.11, the averaged model of the buck chopper can be found as follows:

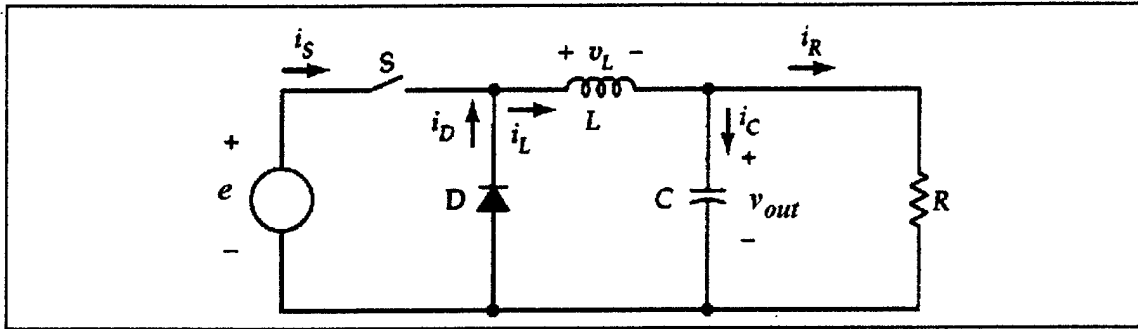


Figure 4.11. Typical Buck Circuit

With S closed for time dT (4.3)

$$\frac{\partial v_{out}}{\partial t} = \frac{1}{C} \left[i_L - \frac{v_{out}}{R} \right]$$

$$\frac{\partial i_L}{\partial t} = \frac{1}{L} (e - v_{out})$$

With S open for time $(1-d)T$ (4.4)

$$\frac{\partial v_{out}}{\partial t} = \frac{1}{C} \left[i_L - \frac{v_{out}}{R} \right]$$

$$\frac{\partial i_L}{\partial t} = \frac{1}{L} (0 - v_{out})$$

The weighted combination of Equations 4.3 and 4.4 yields the averaged equations (4.5)

$$\frac{\partial v_{out}}{\partial t} = \frac{1}{C} \left[i_L - \frac{v_{out}}{R} \right]$$

$$\frac{\partial i_L}{\partial t} = \frac{1}{L} (de - v_{out})$$

After separating the average and perturbation terms from Equation 4.5 and collecting the small-signal terms

(4.6)

$$\frac{\partial \hat{v}_{out}}{\partial t} = \frac{1}{C} \left[\hat{i}_L - \frac{\hat{v}_{out}}{R} \right]$$

$$\frac{\partial \hat{i}_L}{\partial t} = \frac{1}{L} (E \hat{d} + D \hat{e} - \hat{v}_{out})$$

where the ^ above a term indicates that it is a small-signal term.

From Equation 4.2 the small-signal equation for the derivative of the duty cycle is obtained:

(4.7)

$$\frac{\partial \hat{d}}{\partial t} = - \left(h_I \frac{\partial \hat{i}_L}{\partial t} + h_V \frac{\partial \hat{v}_{out}}{\partial t} + h_N \hat{v}_{out} \right)$$

Substituting Equation 4.6 into 4.7 yields

(4.8)

$$\frac{\partial \hat{d}}{\partial t} = - \frac{h_V}{C} \hat{i}_L + \left(\frac{h_I}{L} + \frac{h_V}{RC} - h_N \right) \hat{v}_{out} - \frac{h_I E}{L} \hat{d} - \frac{h_I D}{L} \hat{e}$$

From Equations 4.6 and 4.8 the A matrix is found to be

(4.9)

$$A = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{E}{L} \\ \frac{1}{C} & -\frac{1}{RC} & 0 \\ -\frac{h_V}{C} & \left(\frac{h_I}{L} + \frac{h_V}{RC} - h_N \right) & -\frac{h_I E}{L} \end{bmatrix}$$

From the A matrix the characteristic equation is determined to be

(4.10)

$$s^3 + \left(\frac{1}{RC} + \frac{h_I E}{L} \right) s^2 + \left(\frac{h_I E}{RLC} + \frac{h_V E}{LC} + \frac{1}{LC} \right) s + \frac{h_N E}{LC} = 0$$

or

$$K(1)s^3 + K(2)s^2 + K(3)s + K(4) = 0$$

The process for determining the required gains for obtaining specific pole placements is based on the coefficients of this characteristic equation. The second and fourth coefficients will reveal the required gain of h_I and h_N directly. The third coefficient will yield h_V after h_I has already been determined.

(4.11)

$$h_I = \frac{L}{E}K(2) - \frac{L}{RCE}$$

$$h_V = \frac{LC}{E}K(3) - \frac{h_I}{R} - \frac{1}{E}$$

$$h_N = \frac{LC}{E}K(4)$$

where $K(x)$ is the value of the coefficient term that is x from the left in Equation 4.10.

The multiloop model used for simulation has the system poles placed at $[-3141.6+0.0i, -150.0-140.0i, -150.0+140.0i]$. The pole selection is consistent with the earlier discussion. The gains required for pole placement were calculated at minimum load of R equal to 114 ohms. As the load decreases the poles tend to migrate from the real axis. Computing the gains at the minimum load ensures that the poles will be sufficiently damped for all valid values of load. The gains h_I , h_V , and h_N are calculated to be

(4.12)

$$h_I = 0.0546$$

$$h_v = 0.0441$$

$$h_N = 7.5622$$

In addition, feed forward was incorporated into the design to decouple the input from the output (Figure 4.12). The multiloop control offers a significant improvement in the transient response when compared to simple feed forward or integrator based design (Figure 4.13). The oscillations that follow a load change are not present as they were in the integrator feedback and linear feed forward methods of control. The ability to minimize the transient peak, while much better than designs presented so far, is still inadequate for the SSCM. The primary cause is the feedback parameters used in the control loop. Both the inductor current and output voltage lag the event which causes the transient (Figure 4.14). Specifically, the load changes forcing an immediate change in the

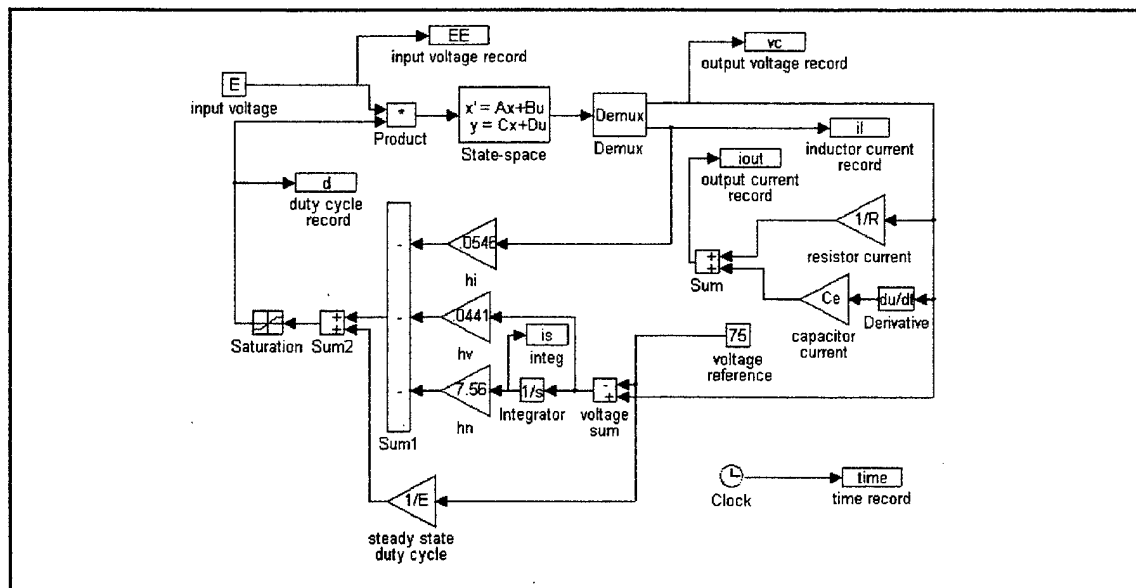


Figure 4.12. Multiloop Feedback Simulation

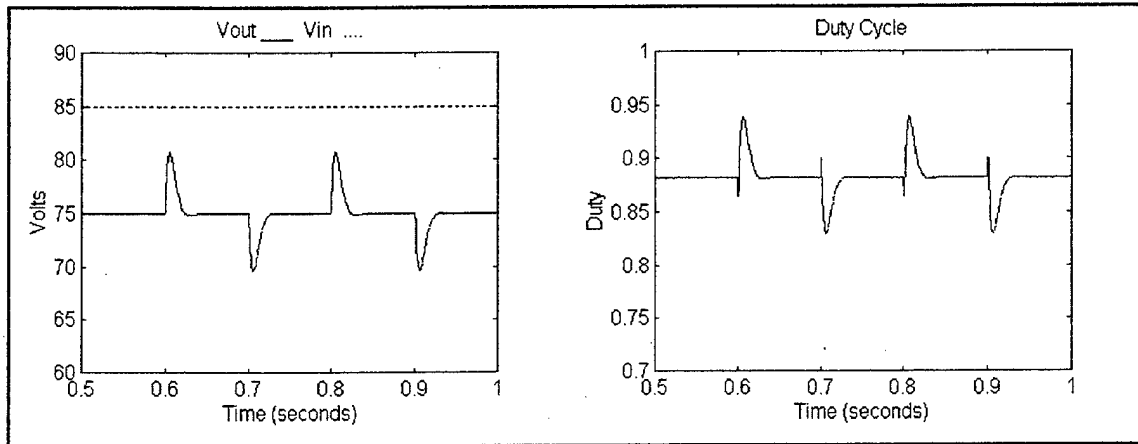


Figure 4.13. Multiloop Feedback with Resistive Load Change

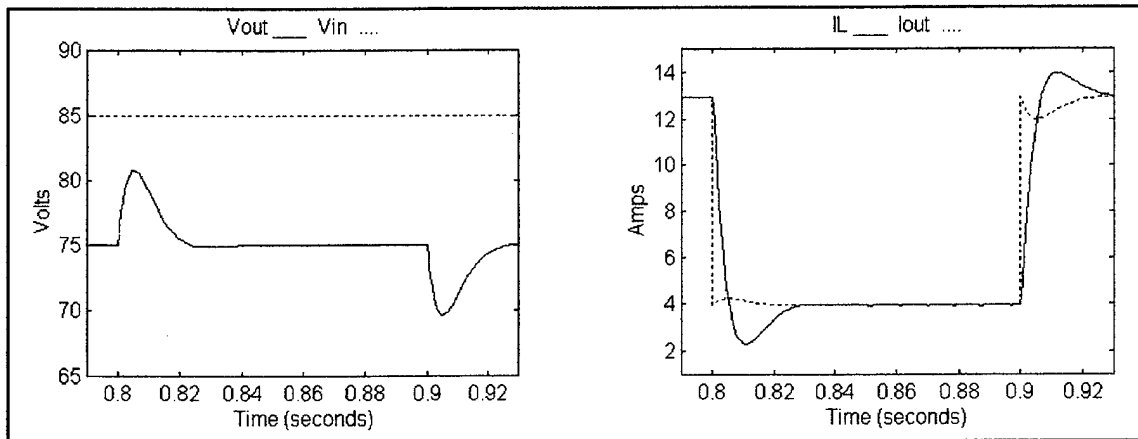


Figure 4.14. Response of Output Voltage and Inductor Current to Load Change of Multiloop Control

output current. The output voltage is supported by the charge in the output capacitor which changes at a rate proportional to the difference in the inductor and output currents. Therefore, the output voltage does not experience an abrupt change. Since it is the average voltage differential across the inductor which changes the inductor current, it too is delayed from the event. In order to quickly turn power in order to reduce the transient excursion, this controller must be sensitive to minute changes in the measured parameters. Therefore, minimizing the transient peaks requires extremely high gains which makes the circuit highly susceptible to noise and not practical.

4. State Difference

The state difference method offers improved transient response over the multiloop. To achieve the improved transient response, the output current was included into the control algorithm (Figure 4.15). The use of the output current in the feedback has been documented in the power control methods of Ref. 12 and Ref. 13. While the multiloop control was driven by a voltage error signal and variations in the inductor current, both voltage error and current error signals are generated with the state difference control. The specific error signals are $(v_{out} - v_{ref})$ and $(i_L - i_{out})$. The duty cycle now responds immediately to any mismatch between the inductor current and the output current. In addition, the duty cycle is driven to minimize the difference between the two signals.

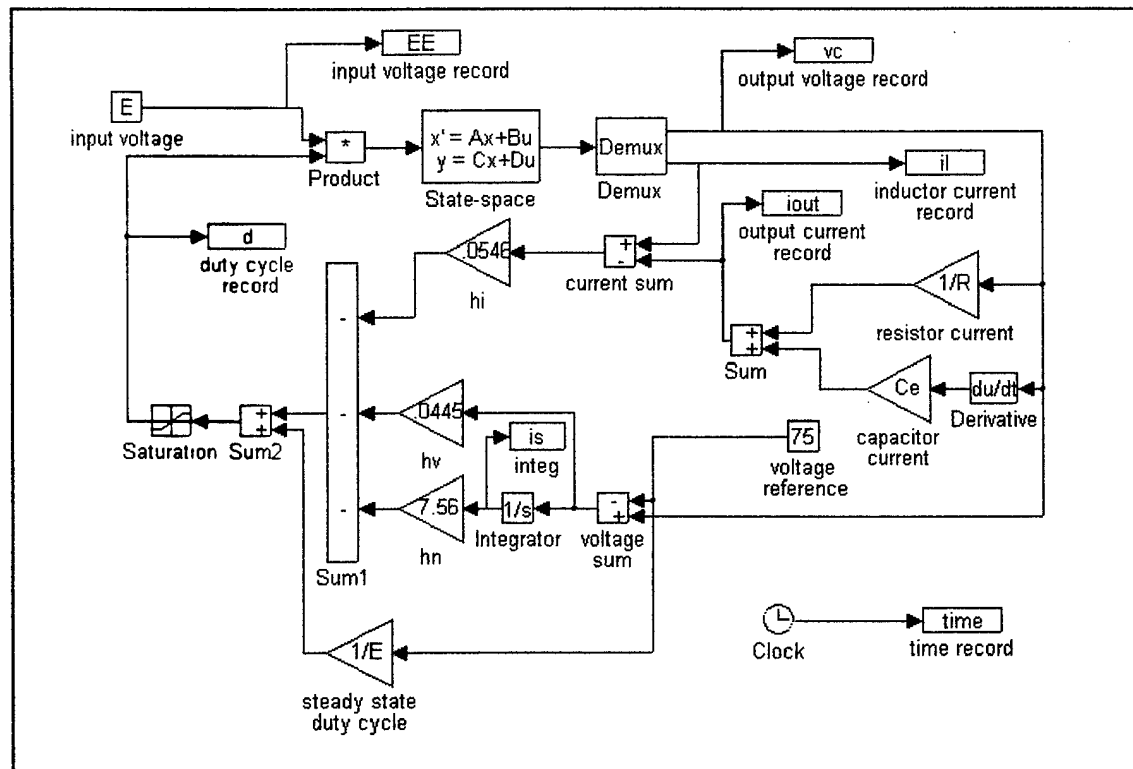


Figure 4.15. State Difference feedback Simulation

The specific control law implemented in the state difference control is:

(4.13)

$$d = -h_I (i_L - i_{out}) - h_V (v_{out} - v_{ref}) - h_N \int (v_{out} - v_{ref})$$

The A matrix is similar to Equation 4.9 with the bottom row modified as follows.

The derivative of the small-signal duty cycle is found from Equation 4.13.

(4.14)

$$\frac{\partial \hat{d}}{\partial t} = -\left(h_I \frac{\partial \hat{i}_L}{\partial t} - \frac{h_I}{R} \frac{\partial \hat{v}_{out}}{\partial t} + h_V \frac{\partial \hat{v}_{out}}{\partial t} + h_N \hat{v}_{out}\right)$$

Substituting Equation 4.6 into 4.14 yields

(4.15)

$$\frac{\partial \hat{d}}{\partial t} = \left(\frac{h_I}{RC} - \frac{h_V}{C}\right) \hat{i}_L + \left(\frac{h_I}{L} - \frac{h_I}{R^2 C} + \frac{h_V}{RC} - h_N\right) \hat{v}_{out} - \frac{h_I E}{L} \hat{d} - \frac{h_I D}{L} \hat{e}$$

From Equations 4.6 and 4.15 the A matrix is

(4.16)

$$A = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{E}{L} \\ \frac{1}{C} & -\frac{1}{RC} & 0 \\ \left(\frac{h_I}{RC} - \frac{h_V}{C}\right) & \left(\frac{h_I}{L} - \frac{h_I}{R^2 C} + \frac{h_V}{RC} - h_N\right) & -\frac{h_I E}{L} \end{bmatrix}$$

Which yields the characteristic equation of

(4.17)

$$s^3 + \left(\frac{1}{RC} + \frac{h_I E}{L} \right) s^2 + \left(\frac{h_V E}{LC} + \frac{1}{LC} \right) s + \frac{h_N E}{LC} = 0$$

The coefficients of the characteristic equation are of such as to allow independent calculation of the required gains for pole placement. Each gain is based on the value of a single coefficient which allows a greater degree of freedom for pole placement. The specific equations for determining the gains are found from Equation 4.17.

(4.18)

$$h_I = \frac{L}{E} K(2) - \frac{L}{RCE}$$

$$h_V = \frac{LC}{E} K(3) - \frac{1}{E}$$

$$h_N = \frac{LC}{E} K(4)$$

where $K(x)$ is the value of the coefficient term that is x from the left in Equation 4.17.

The dependance of Equation 4.18 on the input voltage indicates that when the controllers are integrated into the 100kW SSCMs, the gains must be changed from the NPS values to reflect the higher input voltage.

Pole placement for state feedback simulation is identical to the system poles of the multiloop. Specifically, the system poles are at $[-3141.6+0.0i, -150.0-140.0i, -150.0+140.0i]$. Again, the gains are based on the minimum load or maximum resistance of 114 ohms. The gains are calculated to be

(4.19)

$$h_I = 0.0546$$

$$h_V = 0.0445$$

$$h_N = 7.5622$$

These gains are very similar to the gains used in the multiloop control (Equation 4.12), but the transient response is extremely improved (Figure 4.16). This is due to the prompt feedback of the output current, a concept which is not uncovered in the small-signal analysis. The duty cycle quickly responds to the difference between the inductor and output current with a signal that approximates an impulse (Figure 4.17). It is this feature that allows the state difference feedback to outperform the transient response of the multiloop, although the system poles are comparable. The control also incorporates the feed forward that decouples the input voltage from the output voltage. The excellent regulation and transient performance of this design makes it the desirable choice for SSCM control.

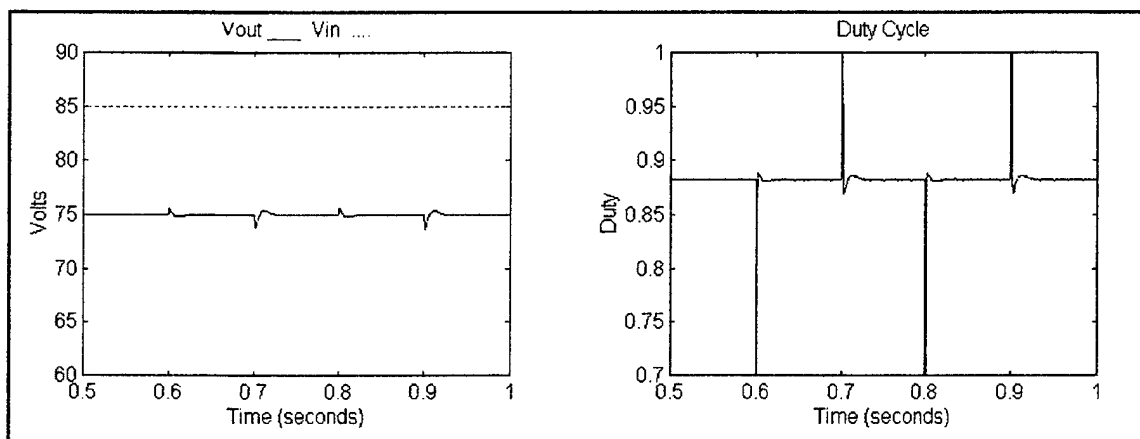


Figure 4.16. State Difference Feedback with Resistive Load Change

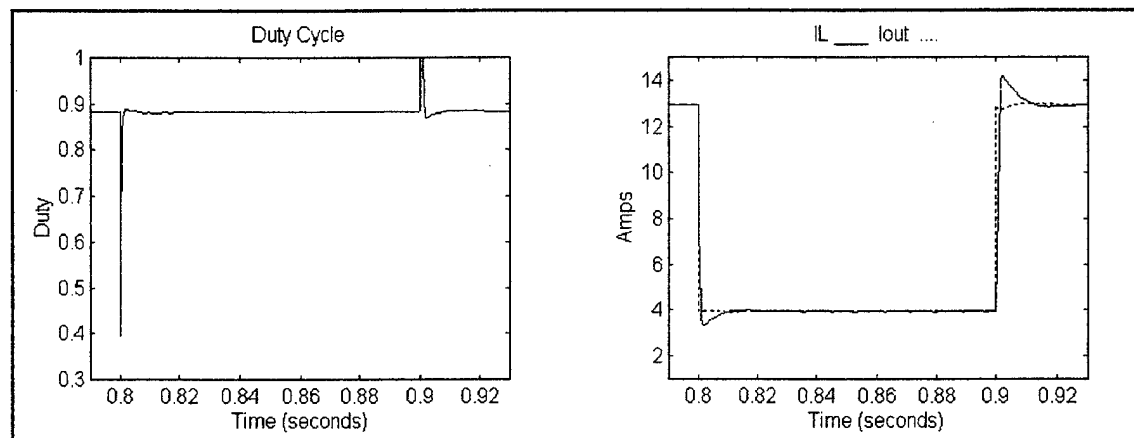


Figure 4.17. Duty Cycle Response for State Feedback

5. Modeling Actual Implementation

a. Resistive Loads

The actual implementation of the state difference control required the modification of the gains and the incorporation of a voltage droop or "house curve" for load sharing among parallel units. These changes are reflected in the system of Figure 4.18. The house curve subtracts a bias to the reference voltage which is proportional to the output current. It is responsible for a 0.1 V/A droop on the output voltage. This reduces the quality of the voltage regulation from zero-voltage to a significant programmed output impedance but does little to undermine the transient response. The transient response is well within the requirements of ± 2.5 volts for a 50% load change (Figure 4.19).

The digital implementation suffered from process delays which prevented it from responding immediately to a change in the output current. Specifics on the delays are covered in Chapter V. Figure 4.20 illustrates the addition of the delay elements to the model. The delays result in increased transient peaks that are not predicted in the model without the delays (Figure 4.21). These peaks are present in the measurements of the actual controllers performance in the lab.

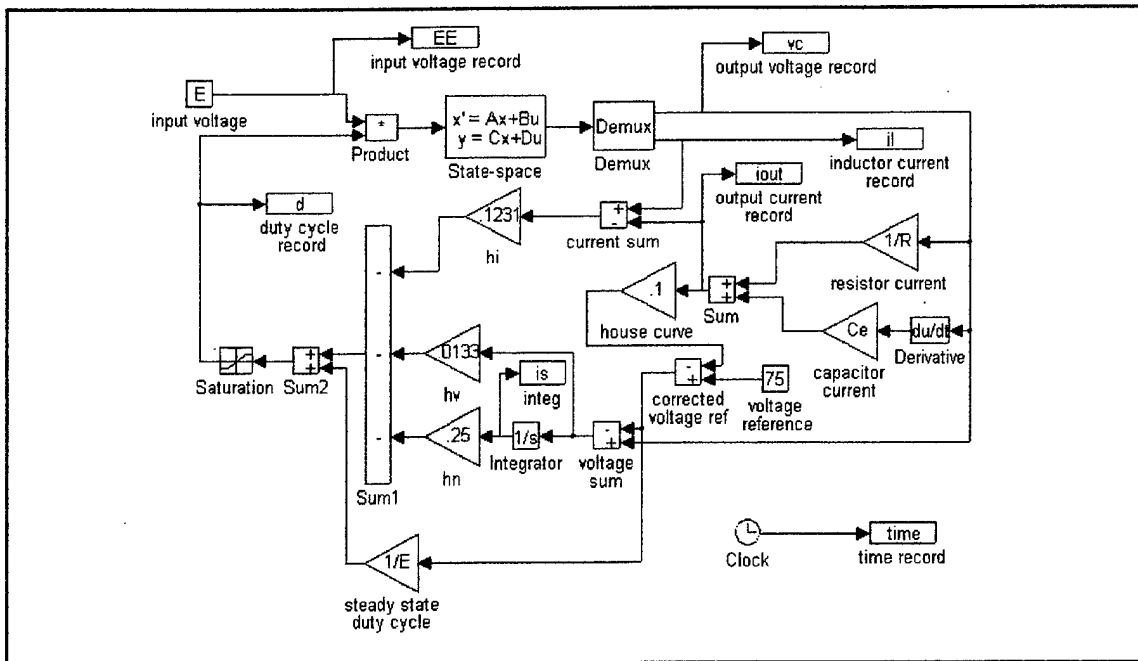


Figure 4.18. State Feedback with Voltage Droop and Actual Gains Simulation

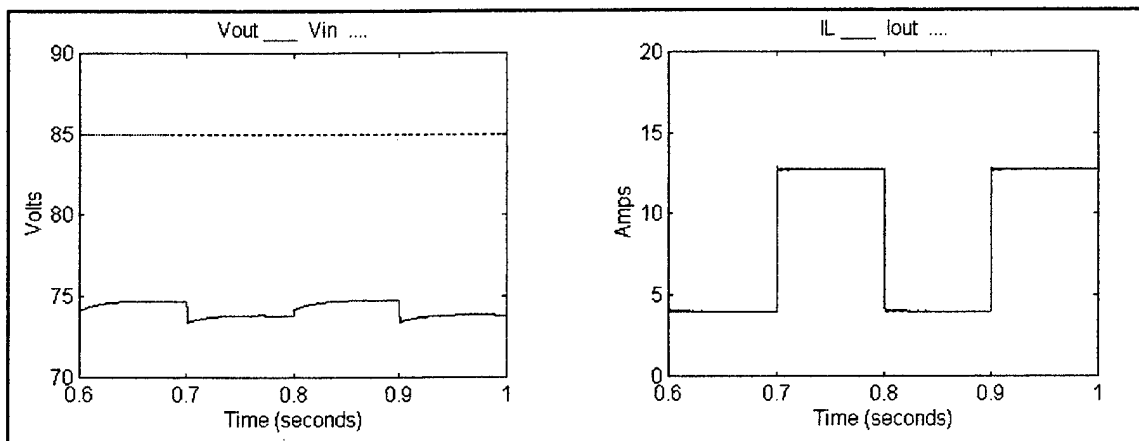


Figure 4.19. Transient Response of State feedback with Voltage Droop

b. Capacitive Loads

Loads that receive power from the SSCM will often have capacitance associated with them. The models include this capacitance in both the state space representation of the output filter and the calculation of the output current. the simulations demonstrate that the additional capacitance does not adversely affect the peak of the transient, but does effect the duration. It is important to note that with 2400 μ F of external capacitance the transient behavior differs little from the transient behavior of the case with no external capacitance (Figure 4.22). With an extremely large amount of external capacitance the peaks began to smooth out (Figure 4.23). This demonstrates that the large load capacitance does not adversely effect the performance of this control.

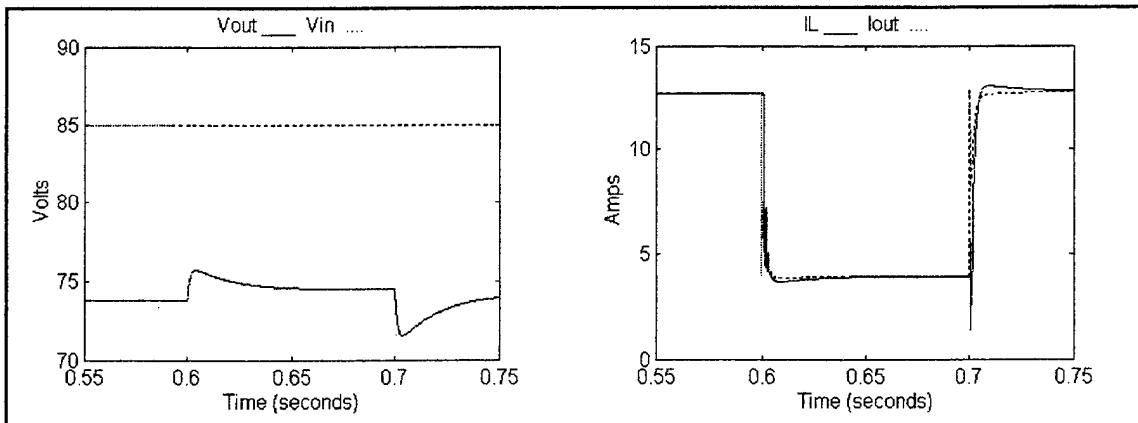


Figure 4.22. Actual Control with Resistive Load and External 2400 μ F Capacitor

D. DISCRETE COMPONENT MODELING

A typical shipboard zone incorporates SSCMs supplying power to SSIMs which supply power to AC loads. The SSIMs are designed to deliver a constant voltage output regardless of the input voltage variances. Therefore, the SSIMs will appear as a constant power load to the SSCM which differs from the resistive load explored in simulations thus far. A constant power load means that if the output voltage of the SSCM increases, the load current will decrease. The equations that the state space representations were

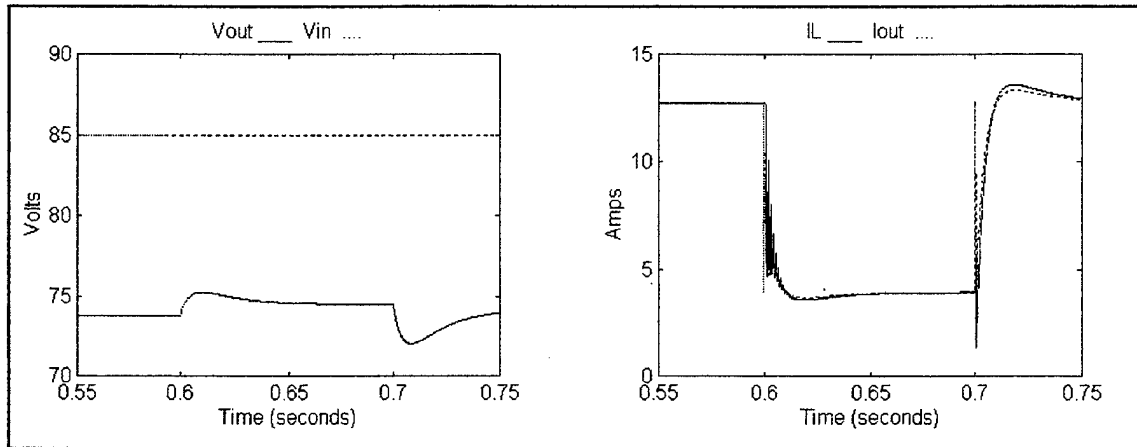


Figure 4.23. Actual Control with Resistive Load and External 10,000 μ F Capacitor

based on no longer hold. The output current expression becomes

(4.20)

$$i_{out} = \frac{p_{out}}{v_{out}}$$

where p_{out} is the output power. The averaged equations (Equation 4.5) become

(4.21)

$$\frac{\partial v_{out}}{\partial t} = \frac{1}{C} \left[i_L - \frac{p_{out}}{v_{out}} \right]$$

$$\frac{\partial i_L}{\partial t} = \frac{1}{L} (de - v_{out})$$

Since the output voltage is now in the numerator of the governing equations, the system defined by the equations is no longer linear. A nonlinear control could be applied to linearize the entire system as in Ref. 14, but it is more desirable to prove stability with the present control scheme through simulation.

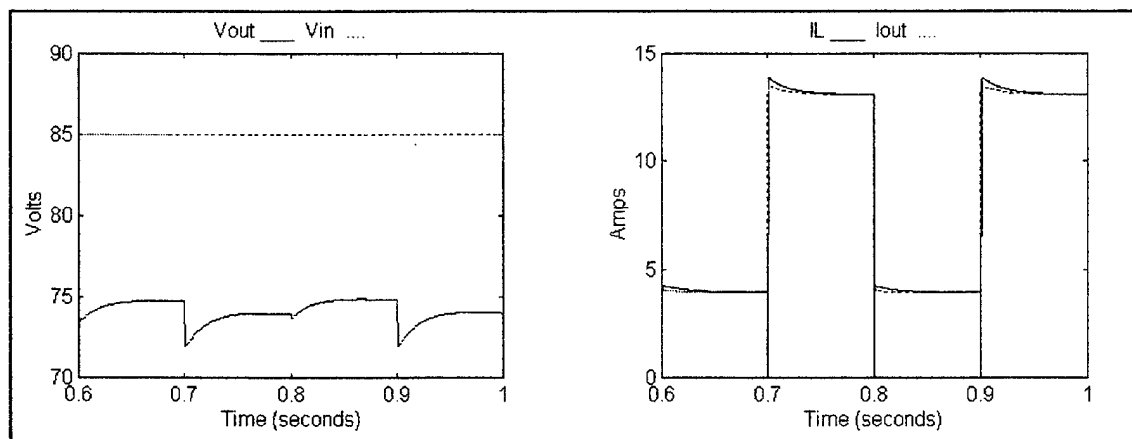


Figure 4.25. Constant Power Load Changes

V. DIGITAL CONTROLLER IMPLEMENTATION

A. REQUIREMENTS

The digital control is accomplished with an Innovative Integrations Digital Signal Processor (DSP) protocard based on the Texas Instrument 320C31 32-bit floating-point DSP. The NPS controller is displayed in Figure 5.1 with both the digital and analog portions identified. The protocard (SBC31) performed a number of base functions in support of the controller:

- 1) Sample input voltage, output voltage, inductor current, and output current.
- 2) Provide a 5kHz synchronization pulse to the analog PWM.
- 3) Sample the fine and course adjust potentials for local voltage control.
- 4) Calculate and output the analog value of V_{ref} .
- 5) Sample the power portion 24 V control voltage.
- 6) Calculate and output the analog value of duty (0-10V).
- 7) Sense the position of the mode switches and enter the correct mode.
- 8) Send the reset to the analog trip circuit.
- 9) Sense the status of the analog trip circuit.

B. HARDWARE DESCRIPTION

1. Overview

The SBC31 is a stand-alone processor card with both analog and digital peripheral devices. The board is suitable for data collection, control, and digital signal processing [Ref. 15]. The processor, a Texas Instrument 320C31, is capable of sustaining .5 instructions per clock cycle. The current version in use has a 50 MHz clock and can sustain 25 million instructions per second. The card has 128K of on-board Programmable Read Only Memory (PROM) and 32K of static random access memory for programs.

All peripherals on the SBC31 are memory mapped. The 320C31 can communicate with fast internal and external peripherals in zero wait states, but all external, off chip peripherals present on the SBC31 are slow devices requiring numerous wait states (the default is seven wait states). This does not effect the performance of the SBC31 in this application. The response requirements of the controller are well below the switching frequency of 5 KHz and sampling of the controller parameters is

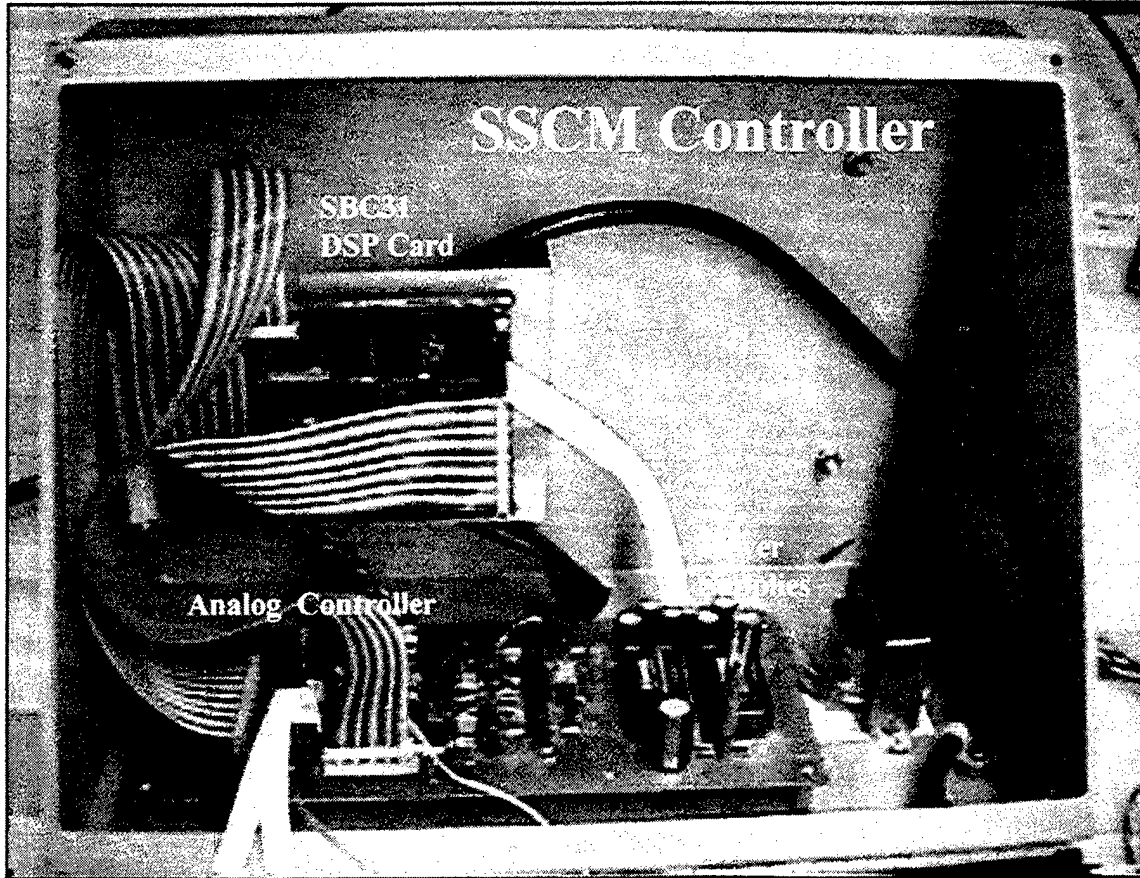


Figure 5.1. NPS Controller

accomplished at 5 KHz (with the exception of output current which is sampled at 15kHz to help eliminate the switching noise).

2. SBC31 Analog Circuits

The analog circuits on the SBC31 include two channels of 16-bit, 200 KHz analog to digital (A/D) input and four channels of 16-bit, 200 KHz digital to analog (D/A) output. Each input channel is configured with independent gain control and a multiplexer (MAX DG528) that allows eight single-ended inputs (16 total) to be sampled.

a. Modifications

Modification of both input channels have been made at NPS to enable the SBC31 to meet its design specifications of +10V to -10V. The buffer amplifier on each

SBC31 to meet its design specifications of +10V to -10V. The buffer amplifier on each channel required replacement of the manufacturer's incorrect 3 K Ω resistor with a 2.74 K Ω resistor. Likewise the buffer amplifiers on the digital to analog output channels required replacement of an incorrect 30 K Ω resistor with a 33.2 K Ω resistor in order to obtain the proper gains and meet the manufacturer's output specifications of +10V to -10V output.

b. A/D Conversion

The A/D converter (Burr - Brown DSP102) has two 16-bit conversion channels that are simultaneously triggered by a conversion signal from one of four jumper selected sources. Three of the sources use clocked interrupt conversions based on the SBC31 timers. The fourth source, and the method used for the NPS controller, triggers from a memory write to address 0xfff940. A single convert trigger both 1) starts a conversion cycle by employing the DSP102's on-chip sample and hold circuitry to acquire a snapshot of the analog signal, and 2) initiates a transmission of the last sampled value via the SBC31's synchronous serial bus to the processor. Both the DSP102 and the receive registers of the synchronous bus are double buffered. Therefore, two conversion cycles are required before the sampled data is available for computation in the processor.

Each channel of the A/D converter is driven by a PGA203 programmable gain amplifier. The amplifier can provide gains of 1,2,4 or 8 to the signal from the DG528 by writing the value of 0,1,2 or 3 respectfully to the appropriate control address.

The parameters directly used for the control of the buck; v_{out} , v_{in} , i_{out} and i_L , are measured using channel A of the A/D converter. The other signals; 24 Volt, coarse adjust and fine adjust, are measured on channel B. All unused inputs on the multiplexers are grounded to minimize noise (Table 5.1). The use of one channel and a multiplexer means that only one of the control parameters can be measured at a time. This causes a different delay for the measurement of each value used in the control. The delays experienced by the state variables v_{out} and i_L are not significant enough to introduce any degree of error due to the relatively slow change in these variables in the designed region of operation. Specifics concerning the delays can be found in the software discussion.

Table 5.1. Multiplexer Channel Assignments

Multiplexer Channel	Signal MUX A	Signal MUX B
0	v_{out}	24 Volts Control Pwr
1	none	none
2	v_{in}	Coarse Adjust
3	none	none
4	i_{out}	none
5	none	none
6	i_L	Fine Adjust
7	none	none

c. D/A Conversion

The D/A converters (Burr - Brown DSP202) provide the analog output capability of the SBC31. The D/As are multiplexed onto the same synchronous serial bus with the A/Ds. The conversion trigger can be timer driven or initiated by writing to the address for the specific D/A converter (method used in the controller). The specific conversion trigger source is determined by jumper settings. The D/As and the transmit registers of the synchronous serial bus are doubled buffered. Two conversion cycles are required before the data sent to the D/A converter is actually present on the output. Each channel of D/A is buffered with an inverting amplifier set to the gain of 3.33 V/V resulting in a potential output swing of $\pm 10V$.

3. SBC31 Digital Circuits

a. The Processor Circuit

The central processing unit, a 320C31 processor, is an industry standard 32-bit DSP with a floating-point unit. It includes two 1K x 32 blocks of internal dual access RAM and a 64 x 32 program cache. It supports single cycle execution of parallel multiply and arithmetic logic unit operations on integer or floating-point data. It has an

data transfer between the processor and the D/A and A/D circuits. An internal direct memory access (DMA) controller allows the SBC31 to communicate with slower external peripherals and memory. The floating point capabilities of the 320C31 were not used in the controller. This allows the adaptation of the design to non-floating-point microcontroller based circuits.

The processor circuit generates 4 control bits that can directly control off-board circuits via the analog port. These analog bits can be independently set and cleared and provide standard 5 volt logic levels. The most significant bit is used for generating a 5kHz, 20 percent duty cycle reference waveform. The analog circuit uses this waveform to synchronize the switching of the PWM. The least significant bit generates an active low signal that controls the reset of the safety trip circuits on the analog circuit. The second least significant bit controls the operation status of the PWM. When asserted high it will secure the PWM regardless of the safety trip status. When asserted low it allows the safety trip circuit to determine the PWM status. The remaining analog bit is not used.

b. Serial Communications

The SBC31 is equipped with two serial ports configured for RS232. The ports are based on the Zilog 85C30 and can support full duplex and asynchronous transmission rates up to 115 kBaud. The final design requires the use of RS422. This standard will be implemented with an aftermarket RS232 to RS422 converter. At present a remote PC is connected via one RS232 serial link to the SBC31. The other RS232 connection is not used.

c. Timers and Counters

An 82C54 integrated circuit provides three 16-bit counters to supplement the two 32-bit counters internal to the processor. The controller only uses one of the 82C54 counters as the timebase for the sampling interrupt. The only other timed interrupt is provided by an on-chip timer. It provides the timing interval for the external communications with the remote PC. A Dallas Semiconductor DS1248 real-time clock is also available but not used.

d. Parallel Communications

Parallel I/O are provided by two eight-bit 82C55 CMOS peripheral controllers. Each controller has three eight-bit data ports and a control port. Each data port can be individually configured as input, output, or bidirectional bits. Port A of the second controller is configured as an input and is used to monitor the status of the local/remote switch, the parallel/single switch and the three protective trips. No other parallel ports are used.

C. SOFTWARE DESCRIPTION

1. General Background

The SBC31 software development was based in ANSI C as implemented by the Texas Instrument Floating Point Optimizing C Compiler toolset. Included in the toolset are peripheral libraries with functions specific to the SBC31. These functions are highly capitalized upon for the A/D and D/A operations required in the controller implementation.

The SBC31 has multiple boot options. In the development phase, the SBC31 boots up with a talker program resident in its memory. The software compiled on the PC is then downloaded via the serial connection into the memory of the SBC31 and executed. The serial connection is then used for monitoring. Later in development and once the program code has been finalized, the SBC31 can boot up and load programs from on board PROM.

2. Program Description

The program code is divided into three regions: initialization, monitoring routine, and interrupt. Flow charts for all three regions are included as Appendix B and source code is included as Appendix C. The initialization of the SBC31 configures the external peripherals and communication ports of the SBC31 for controller operation. It also initializes all data structures used by the program. All variables and constants used are of global scope. This is desired since the majority of the code is located inside the interrupt. Call by value is not used in order to minimize the overhead associated with the required memory management. The largest portion of code in the main function performs

initialization; the remainder of the code is devoted to the monitoring routine.

The monitoring routine is based on a keyboard terminated while loop. As currently designed it serves to send information about the controller parameters to a remote PC for display. The loop speed is based on a call to an SBC31 special time function driven by the interrupt of one of the processor's on-chip timers. The function effectively halts the processor except for interrupt and DMA activity. This allows the controller algorithm located in the interrupt to continue to function while waiting between the updates of the monitoring routine. Currently the monitoring is accomplished with a remote PC running the Terminal program which comes with the C software development kit.

A digital approximation of the following analog algorithm was implemented on the SBC31:

(5.1)

$$d = d_{ss} - h_n \int (v_{out} - v_{ref} + i_{out}/g) - h_v (v_{out} - v_{ref} + i_{out}/g) - h_i (i_{out} - i_l)$$

where

(5.2)

$$d_{ss} = \frac{v_{ref} - i_{out}/g + i_{out} R_{comp}}{v_{in}}$$

In addition to the programmed voltage droop, $-i_{out}/g$, a compensating term, $i_{out} R_{comp}$, was included in the sum of the modified reference voltage. The compensating term was required in order to account for the real voltage droop already present in the buck chopper. The value of the compensating resistance, R_{comp} , was determined by removing the programmed droop, voltage difference, and integration terms from the controller algorithm and adjusting R_{comp} until zero-voltage regulation was achieved during a change from partial to full load (Figure 5.2). The value of R_{comp} for the NPS buck choppers is 1/9 ohm.

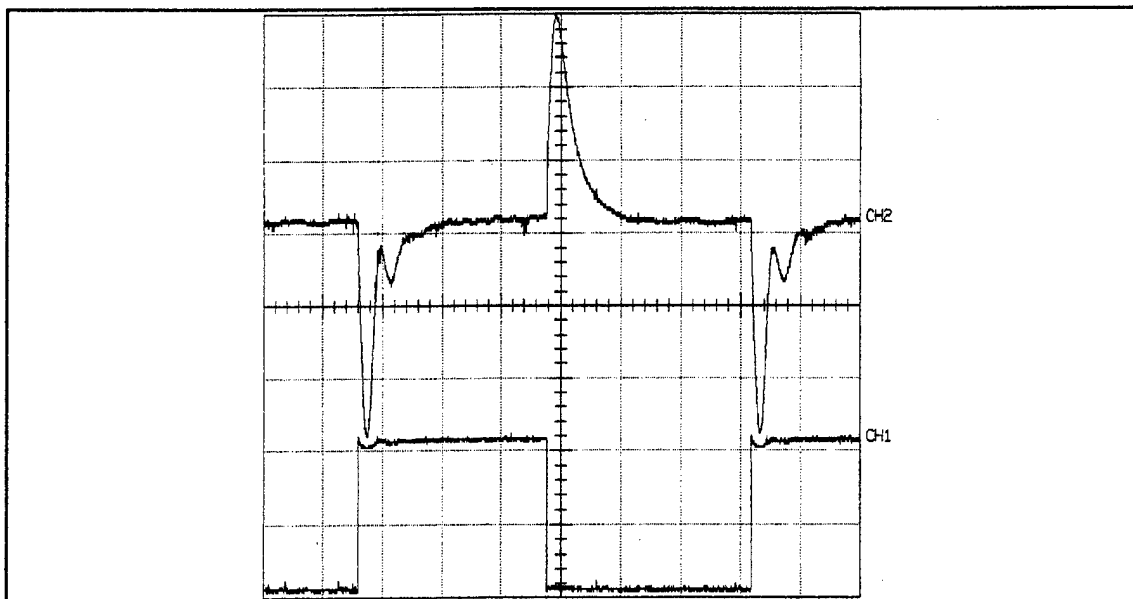


Figure 5.2. Compensating for Inherent Droop of Buck Chopper
 CH2 (v_{out}) 1.0V/Division CH1(i_{out}) 5.0A/Division

The SBC31 performs the controller algorithm driven by a single 30kHz interrupt from one of the three 16-bit timers on the 82C54. The body of the interrupt routine is split into common areas and count specific areas. The common areas are the portions of code which execute on every interrupt. The count specific areas execute only on interrupts that occur in conjunction with a specific state of a software based six-state counter. The counter increments to the next state on each interrupt. The counter returns to the first state on the next interrupt following the sixth state. The count specific areas perform functions that are required to be different at each interrupt for correct controller operation. These functions include multiplexer channel selection and the assignment of A/D sample values to specific variables (Table 5.2). Additionally, much of the computation for the control algorithm of Equation 5.1 is divided among the count specific areas to minimize the total amount of calculations that must be done during any one interrupt (Table 5.3). The final summation of all the terms in the duty cycle calculation is performed in the common areas each interrupt.

Table 5.2. Multiplexer Channel Selection and Value Assignments at Each Count

COUNT	0	1	2	3	4	5
MUX A	i_{out}	v_{out}	i_{out}	i_L	i_{out}	v_{in}
MUX B	24 volts control pwr	coarse adjust	fine adjust	none	none	none
Variable(s) Updated	i_{out}	v_{in}	i_{out} , 24 volt control pwr	v_{out} , coarse adjust	i_{out} , fine adjust	i_L

Table 5.3. Division of Computation

Calculation	d_{ss}	$(v_{out} - v_{ref} + i_{out}/g)$	$\int (v_{out} - v_{ref} + i_{out}/g)$	$(i_{out} - i_L)$
COUNT	2	4	3	0

3. Delays

Significant delays occur between the time the control parameters are sampled and the time the analog output based on those parameters are made available for the PWM. Both A/D and D/A are double buffered at both ends of the synchronous bus. As demonstrated in Table 5.2, when MUX A is configured for v_{out} at count '1', the variable is actually updated two interrupts later at count '3'. Likewise, the duty cycle sent to the D/A will require two interrupts before it is seen as an analog value.

The output current is sampled at three points during the switching period and the average of the three samples is used in the calculations. This process minimizes the effect of any downstream switching converters (a phenomenon discussed with the analog control in Chapter 6) but also introduces up to T delay for the parameter that is most time critical. The change in output current is the controller's first indication of a change in load. It is the controllers response to change in the load current that allows the controller to quickly return the voltage to its nominal value and minimize the transient extremes.

The worst case delay occurs if the output current changes value after the A/D conversion at the end of the interrupt that started with count equal to '2'. The captured signal does not represent the new current value and is therefore not seen in the assigned value until two interrupts later, $(2t_{int} - t_{ADconv})$. The averaged value of output current calculated during the count specific area of count '5' does not reflect the change and remains unchanged until it is calculated again after T delay. The new averaged value is not used until count '0' and therefore experiences an additional interrupt delay, t_{int} . For an analog output on the D/A, two additional interrupt delays and the D/A conversion time are required. Since the instructions for starting both D/A and A/D conversions are sequential in the program, the delays for program execution are extremely small and can be ignored.

(5.3)

$$t_{dmax} = (2t_{int_{2,4}} - t_{ADconv}) + t_{int_{4,5}} + T + t_{int_{5,0}} + (2t_{int_{0,2}} + t_{DAconv})$$

With $t_{ADconv} = t_{DAconv} = 5.0 \mu s$ and an interrupt at 30kHz Equation 5.3 becomes

(5.4)

$$t_{dmax} = 6t_{int} + T = .4 \text{ milliseconds}$$

This delay is responsible for the larger transients experienced with the digital controller compared to the analog control and simulations. The maximum delay can account for a 10 degrees shift in a sinusoid at the resonant frequency of the buck choppers output filter. To compensate for the differences, the gains were adjusted to minimize the transient peeks and therefore differ from the gains used in the analog controller. The gains used for the digital control are as follows:

$$h_i = 0.123$$

$$h_v = 0.0133$$

$$h_n = 0.25$$

$$1/g = 9.0$$

4. Status Detection and Mode Control

Controller status and mode control is performed in the common area of code. The contents of the parallel port A are read and conditioned to a 5-bit number. The number represents the status of the controller's switches and protective trips (Table 5.4). Based on the status word, the interrupt routine makes three decisions which establish the mode of the controller. The decisions are the source of the reference voltage, the state of the controller reset integer, and the state of the controller enable integer.

Table 5.4. Status Word Control Bits Table

Control Bit	4	3	2	1	0
Switch or Trip Sensed	Local* / Remote Switch	Over Current Time-out	24 Volt Control Power Trip	Over Temp Trip	Parallel* / Single Switch
Active / Tripped State	*high	high	high	low	*high

VI. ANALOG CONTROLLER

A. REQUIREMENTS

The analog controller provides all of the auxiliary functions required for a successful controller that are not implemented on the SBC31. These specifically include the following:

- 1) Interface the SBC31 with the buck chopper.
- 2) Convert the ordered duty cycle to a PWM signal.
- 3) Generate the pulses for the IGBT driver circuit.
- 4) Filter and buffer measured parameters for the control loop.
- 5) Provide protective trips and limit pulse-by-pulse current.
- 6) Interface the local controls with the SBC31.
- 7) Provide power for both SBC31 and analog control.

In addition it offers a backup analog control loop that can replace the duty cycle control of the SBC31 should a partial failure of the SBC31 occur. These failures would be limited to the data acquisition hardware of the SBC31. The reference voltage for the analog control loop originates on the SBC31 and would still be required. Either analog or digital control can be the source of the duty cycle. The choice is made by positioning a mutually exclusive digital/analog jumper located on the analog control board.

B. HARDWARE DESCRIPTION

1. Analog Controller

The analog controller receives the analog signals of input voltage, output voltage, output current, and inductor current from which it calculates the required duty cycle (Figure 6.1). It provides a duty cycle signal to the pulse width modulator via a mutually exclusive digital/analog jumper switch. The analog controller implements the same control algorithm as the digital controller with the exception of the sampling and computation delays which occur in the digital controller:

(6.1)

$$d = d_{ss} - h_n \{ (v_{out} - v_{ref} + i_{out}/g) - h_v (v_{out} - v_{ref} + i_{out}/g) - h_i (i_{out} - i_L) \}$$

An AD534 multiplier receives v_{ref} from the SBC31 and v_{in} from the measured parameters and calculates d_{ss} :

(6.2)

$$d_{ss} = \frac{v_{ref}}{v_{in}}$$

Absent from the steady state duty cycle is the house curve bias and the compensation for the inherent voltage droop of the buck chopper. These two terms are equal in magnitude and contribute to the reference voltage in opposite fashions as shown in the discussion of the software for the SBC31. Therefore, it was possible to eliminate the additional bias circuitry required to include the two terms in the d_{ss} calculation. If the final integration of the controller into the 100kW SSCMs requires modifications to account for any difference in the magnitude of the two terms, it can be easily incorporated into the software of the SBC31 which generates the v_{ref} signal.

The subsequent terms of the duty cycle computation of Equation 6.1 are implemented with summing circuits and a bounded integrator based on a single LM324 quad op amp integrated circuit. The sums of $(i_{out} - i_L)$ and $(v_{out} - v_{ref} + i_{out}/g)$ are formed by their respective summing circuits each based on a single op amp of the LM324. The gain for the voltage droop, $1/g$, is determined from the value of a single bias resistor and can be easily changed to support different droops. During development at the Naval Postgraduate School, the gain was set with a 1 M Ω resistor to provide the droop of 0.1 V/A.

The integrator compensates for any variations in the circuits and real-world factors not accounted for in the simulations. It also makes possible the steady-state voltage control of the buck chopper in the nonlinear region of discontinuous operation during maintenance. It accomplishes these functions by providing additional bias to the duty cycle in order to drive the difference in the output voltage and the droop compensated reference voltage to zero. The integrator uses a 10 k Ω resistor and 1 μ F

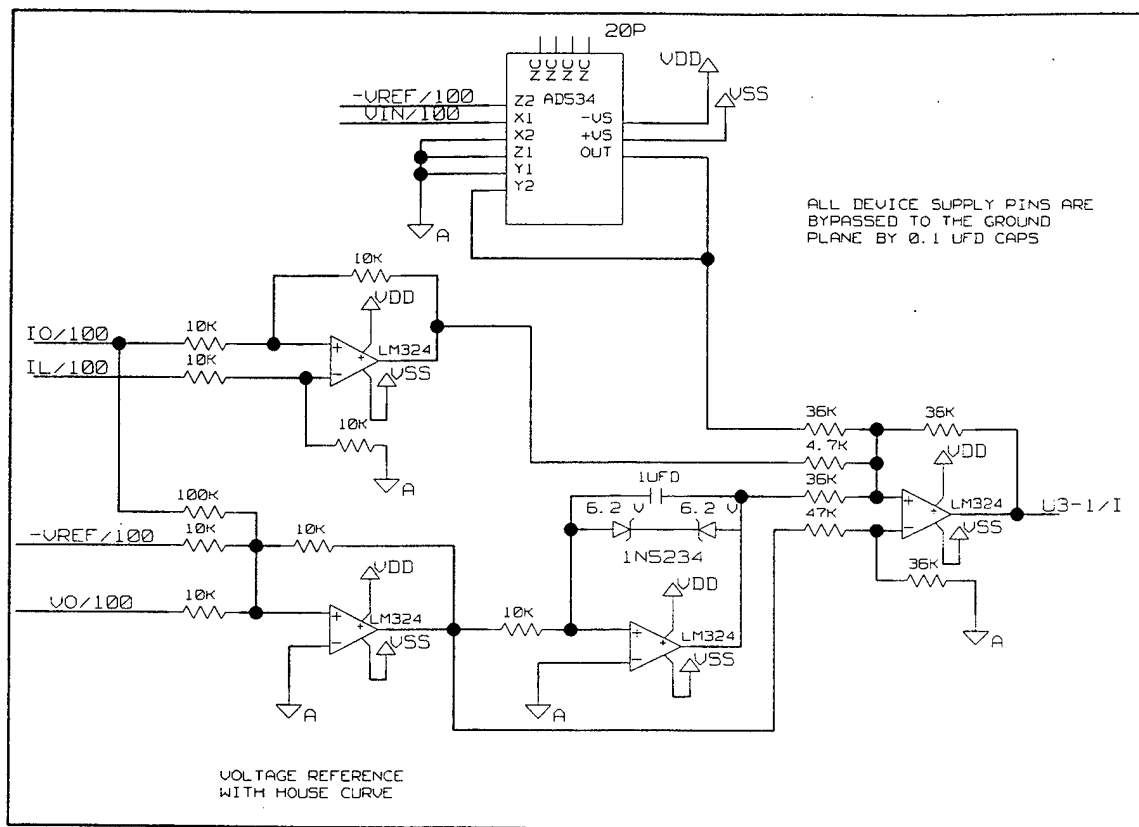


Figure 6.1. Analog Controller Schematic

capacitor to provide a slow 0.01 V/s response. The output of the integrator is bounded by two 1N5234 zener diodes placed back to back in the feedback loop. The diodes limit the output to ± 6.6 volts.

The combination and scaling of the terms in Equation 6.1 is implemented by employing the fourth operational amplifier of the LM324 in a weighted summing configuration. All gains are mutually independent except h_v , which is dependent on the bias resistors of all the other gain terms. Therefore, in order to modify any of the channel bias without changing h_v , both the channel bias resistor and the bias resistor for h_v channel must be altered. To make a change to only h_v requires only changing the bias resistor for h_v . The gains for the analog controller as used in the development at NPS are as follows:

$$h_i = 0.07659$$

$$h_v = 0.004623$$

$$h_n = 0.1$$

$$1/g = 0.1$$

2. Pulse Width Modulator

The duty cycle signal from either the analog controller or the SBC31 is ported to the pulse width modulator (PWM) via a mutually exclusive digital/analog jumper switch, a low pass RC filter and a zener voltage limiter (Figure 6.2). The zener limiter protects the input of the pulse width modulator from voltages in excess of 10 volts and below ground. The pulse width modulator is based on the UC1637 integrated circuit. The monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with output stages capable of sourcing 100 milliamps. Additional protective circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5 V temperature compensated threshold. All protective circuits act to disable the output stages. The pulse-by-pulse current limit is the only latched protective circuit. It does not immediately remove its disable signal from the output stage when the condition that caused the protective action is removed. The pulse-by-pulse current limit latch is reset at the beginning of the next cycle of the sawtooth generator.

The sawtooth oscillator sets up a reference waveform whose amplitude extremes fall between two threshold voltages. The lower threshold, $-V_{th}$, is connected to ground and the higher threshold, $+V_{th}$, is established by a zener diode reference at 10 volts. The rise and fall rate of the waveform is based on the charge and discharge of an external capacitor fed by a current source, I_s , internal to the UC1637. A control port allows the value of this current to be externally controlled, and this value, when coupled with the value of the capacitance, C_s , and the difference between the threshold voltages, determines the frequency, f , of the reference waveform.

(6.3)

$$f = \frac{Is}{2 C_t [(+V_{th}) - (-V_{th})]}$$

The duty cycle signal is compared to the reference waveform. When the reference waveform is less than the duty signal the output is driven to the low supply potential of -15 volts. When the reference waveform is greater than the duty signal, the output is driven to the high supply potential of +15 volts. The result is a pulse train whose pulse duration at the positive potential, t_{pos} , compared to the period, T , is proportional to the value of the duty cycle signal, d_{sig} , compared to the difference in the threshold potentials.

(6.4)

$$\frac{d_{sig}}{(+V_{th}) - (-V_{th})} = \frac{t_{pos}}{T}$$

A second comparator and driver combination is configured to provide the inverse of the pulse train, but this output is not used.

3. Pulse Generation

The IGBT driver circuit for the 100 kW SSCM requires two PWM signals that are driven by a low impedance source. The signals must be the inverse of each other. These requirements are met by using the TC4425 dual high-speed MOSFET driver (Figure 6.2). The TC4425 incorporates both an inverting and noninverting driver each capable of a peak output current of 3 amps. The PWM signal from the UC1637 is first applied to a resistor-diode voltage limiter to prevent the occurrence of any negative voltages that would cause damage to the TC4425. The signal is then applied to both inverting and noninverting inputs of the TC4425 and the outputs are sent to the IGBT gate driver located in the buck chopper of the SSCM. During development the PWM signal is taken before the limiter and sent directly to the prototype's IGBT gate driver.

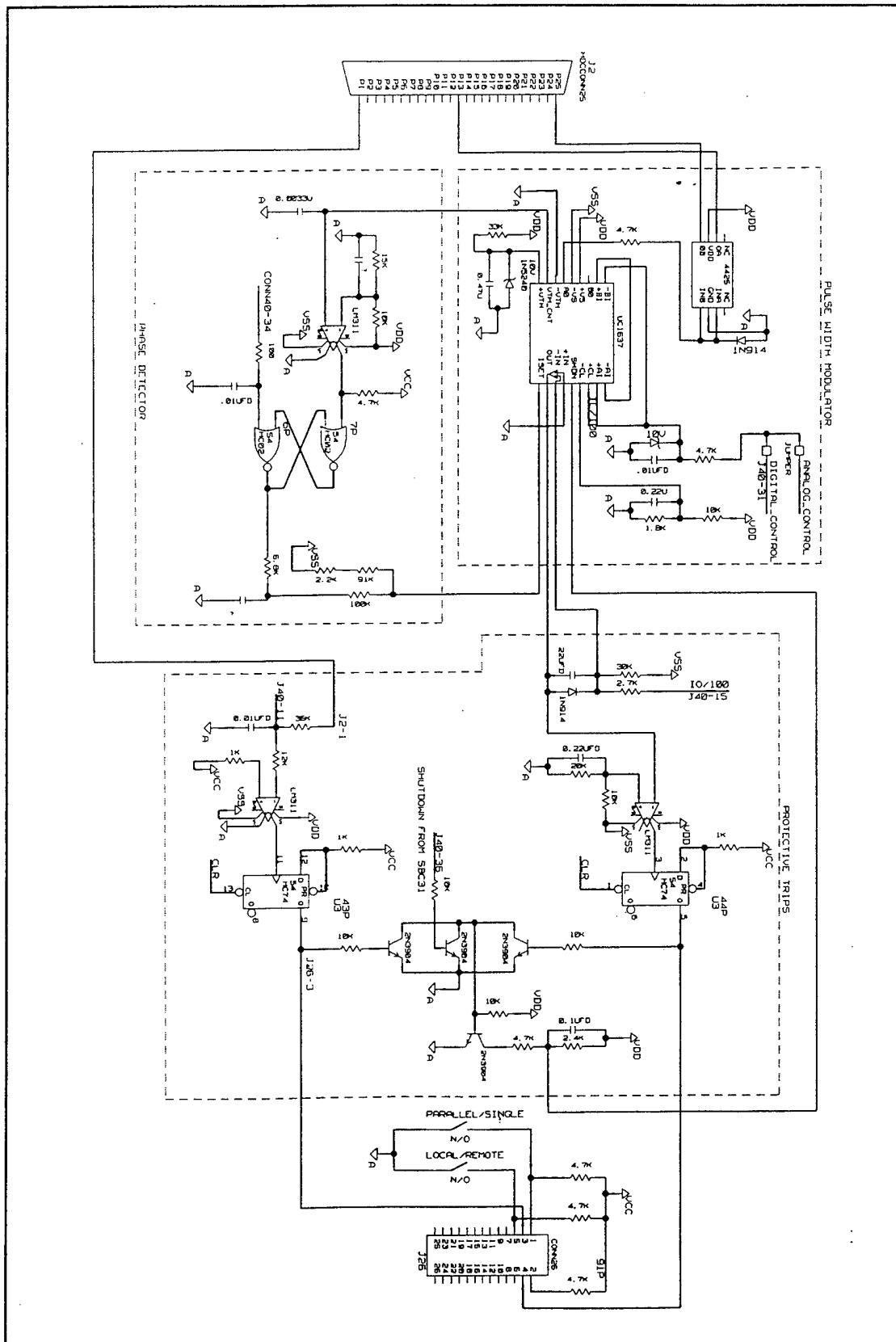


Figure 6.2. Pulse Width Modulator, Phase Detector, and Protection Circuit Schematic

4. Phase Locked Loop

The switching frequency of the analog circuit is synchronized to the SBC31 via a phase locked loop (PLL) circuit. This eliminates any variation in the measured parameters due to the beat frequency between the PWM circuit and the SBC31. Through synchronization each control value is measured at the same point in the converter cycle providing a consistent bias from the average value. This bias is corrected for, along with the many other variation in the circuits, by the integrator of the controller. The average value and variations in this average value can then be measured. A similar method has been used to uncover the inductor's average voltage in a zero-voltage buck chopper control scheme of Ref. 16.

The PLL circuitry consists of a pulse generator, a phase detector, filter circuits, and the UC1637 PWM integrated circuit (Figure 6.2). The pulse generator generates a 10 percent duty cycle pulse train from the PWM reference triangle wave of the UC1637 by comparing the reference wave against a constant nine volt potential. The pulse train is applied to one input of the phase detector comprised of a dual nor gate configured into a bistable latching circuit. A 5 kHz 20 percent reference pulse train from the SBC31 is applied through a filter circuit to the other input of the phase detector. The filter circuit prevents any noise from generating a false trigger in the high-speed logic of the nor gates. The close placement of the phase detector to the pulse generator removes any requirement for filtering on that input. The phase detectors output latches high upon the receipt of a pulse from the pulse generator. It remains in that state until a pulse is received from the SBC31. Therefore, the output duty cycle is proportional to the phase difference between the two pulse trains. An RC filter on the output recovers the average value of the output which is used to provide additional bias to the capacitor charge current circuitry of the UC1637. This change in bias alters the charge and discharge rates of the capacitor used in the time base for the UC1637 and ultimately locks the UC1637 frequency with the SBC31.

The range of operation of the PLL is ± 250 Hz from the free-running frequency of the PWM oscillator. If the oscillator is farther than 250 Hz from the 5 kHz reference of

the SBC31, the phase detector will not create enough bias to bring the signals into synchronization.

5. Protection And Shutdown Circuits

Three shutdowns are implemented on the analog control. The shutdowns include timed-over current trip, 24 volt control power trip, and a commanded shutdown from the SBC31 (Figure 6.2). Both the timed-over current trip and the 24 volt control power trip when activated, latch D-type flip-flops and require an external reset signal from the SBC31 before PWM operation can continue. As an additional protection measure, the pulse-by-pulse current limit feature of the UC1637 is implemented at 200 percent of maximum current. All protection and shutdown circuits can operate whether the analog or digital control is selected.

The timed-over current shutdown is implemented with an op amp-based precision rectifier and integrator circuit followed by a comparator and a D-type flip flop. The output current signal is weighted and summed with -15 volts such that the precision rectifier is forward biased when the current exceeds 100%. Once forward biased, the capacitor of the integrator begins to charge at a rate proportional to the excess bias and the integrator's output voltage decreases. If the integrator's output falls below the reference voltage of the comparator, the comparator's output rises causing the flip flop to latch in the shutdown state. The input resistors and integrator capacitance were selected to provide a one second timeout at 150 percent of maximum current and a two second timeout at 125 percent of maximum current.

The 24 volt control power signal is first reduced with a 4:1 voltage divider. The signal is then sent both to the analog trip circuitry and the analog to digital circuitry of the SBC31. The 24 volt control power trip is accomplished using a comparator and D-type flip flop. The reduced signal is compared with a 5 volt reference. When the signal falls below the 5 volt reference, indicating that the 24 volt control power has decreased below 20 volts, the comparator's output rises and latches the flip flop in the shutdown state.

All three shutdowns; the timed-over current trip, 24 volt control power trip, and a

commanded shutdown from the SBC31, are logically ORed with a gate constructed with discrete components. The output of the gate is biased to interface with the 2.5 volt temperature compensated shutdown port of the UC1637.

6. Signal Filters

The filtering of the measured parameters for the controllers is accomplished by first order low pass RC filters (Figure 6.3). The filtering removed the very high frequency noise that was a result of ringing during the switching. The filter for the output current measurement also aids with uncovering the average value of the output current. It was found during development that high-frequency variations in the current caused by the switching of downstream converters or inverters could cause erroneous output current readings. The erroneous readings would prevent the controller from correctly maintaining the voltage level on the output of the buck chopper. The controller recognized the output current change as a transient change to a new load level. This loss of control occurred at the beat frequency between the source and load converter's switching frequencies. Since both prototypes used in development switched at 5 kHz and both were governed by highly accurate crystal oscillators, the error only occurred at approximately 2 minute intervals. The corner frequency for all measurement filters except the output current were set at 4.2 kHz. The corner frequency for the output current filter was set at 477.5 Hz, below the switching frequency of the converter and above the resonance of the buck chopper's output filter.

7. Buffers

Buffering of the four filtered parameters was performed by elements of an LM324 configured as voltage followers (Figure 6.3). The buffering provided low impedance outputs to drive both the analog control circuit and the analog to digital circuits of the SBC31. The performance of the multiplexer circuits on the SBC31 are extremely susceptible to the impedance of the source that is driving the channels. The buffering also prevented the change in the corner frequencies of the parameter filters by the effects of additional circuits.

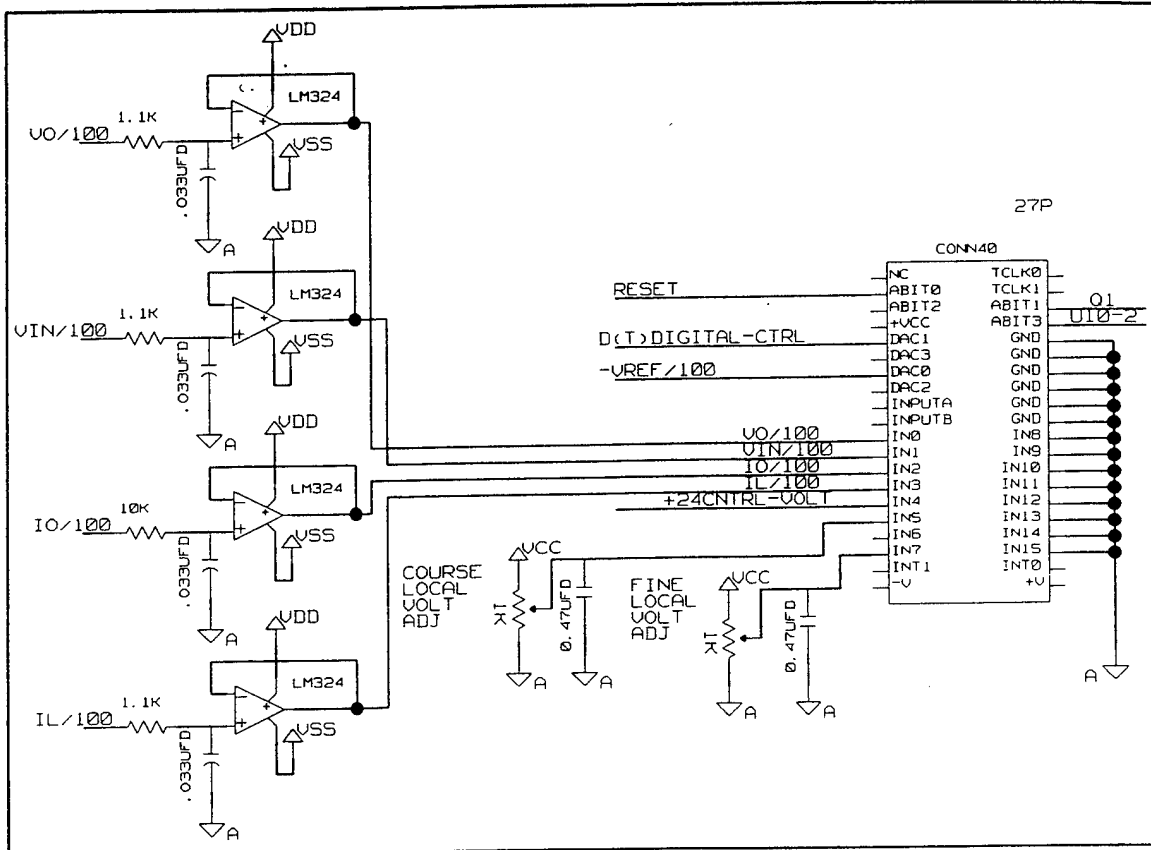


Figure 6.3. Signal Filters and Buffers Schematic

8. Supporting Elements

Power for all the circuits on the analog control board is provided by a Datel TWR-5/100 15/200 D12 converter module. The module is a small package self contained switching power supply that provides both +/- 15 and 5 Vdc from a 9 to 18 Vdc source. An additional Datel module provides power to the SBC31. The ground for the SBC31 power system was separate and distinct from the ground of the analog control board to minimize the potential for ground loops.

A 12 volt power supply provides power to the Datels. The power supply is comprised of a 120:12.6 Vac isolation transformer, a full wave bridge rectifier made of discrete diodes, and a single filter capacitor. With the exception of the transformer, these components and the Datels are mounted on the circuit board of the analog control.

The analog controller interfaces with the SBC31 through 40-pin and 26-pin ribbon cables. The ribbon cables connect to the corresponding 100 mil headers on the analog controller board. Interface to the power converter section is through an industry standard DB25 connector also mounted on the board. A four-post power connector provides power from the analog controller to the SBC31.

The analog control was built on a single circuit board milled at NPS with standard Gerber file commands. The board has double-sided copper clad, with all excess cladding on both sides used as ground planes. The ground planes of the circuit board are isolated at the four chassis mount holes making the two grounds independent.

The board layout was designed using the EasyTrax software by Protel, Incorporated. The freeware programs include a graphical-based design editor and a PCB plotter. The plotter can drive printers, plotters, or generate Gerber or postscript files.

VII. NPS SCALED SSCM TESTING AND EVALUATION

The testing and evaluation of the controller is divided into two areas. The first area encompasses the evaluation of the dynamic performance of the control algorithm as implemented by both digital and analog controllers, and the measurement of the delay imposed on the algorithm by the use of the SBC31. The second area includes the operability tests that verify the correct function of auxiliary features. These features include the protection, shutdown, and mode control. In addition, the efficiency of the prototype SSCM was measured at various levels of loading.

A. DYNAMIC PERFORMANCE

1. General Description

The dynamic performance tests include measurements with both resistive loads and constant power loads. The tests attempt to imitate the abrupt load changes of the simulations to create conditions under which comparisons between the two results can be made. DC power for the buck chopper originated from a full wave rectification of the three phase power from a high-voltage variac (Figure 7.1). A 10,000 μ F capacitor was used to filter the output of the rectifiers and prevent the high frequency current surges of the buck chopper from creating undesirable noise on the laboratory power lines.

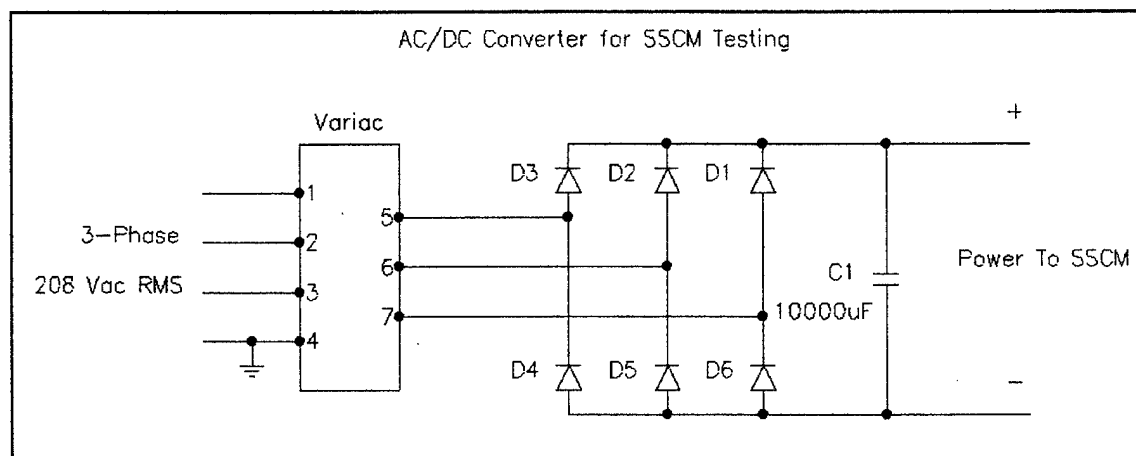


Figure 7.1. DC Power for NPS Tests

2. Resistive Loads

a. Test Description

The resistive load tests were conducted with a high-power resistor load bank of five 29 Ω resistors (Figure 7.2). The load bank is split in two parts. The first part is a single 29 Ω resistor that is used for the startup load for the buck chopper and the low value of load during the transients. The second part is a group of four resistors in parallel that are combined with the first part through the IGBT switch. The switch is gated on and off to create the abrupt changes in load.

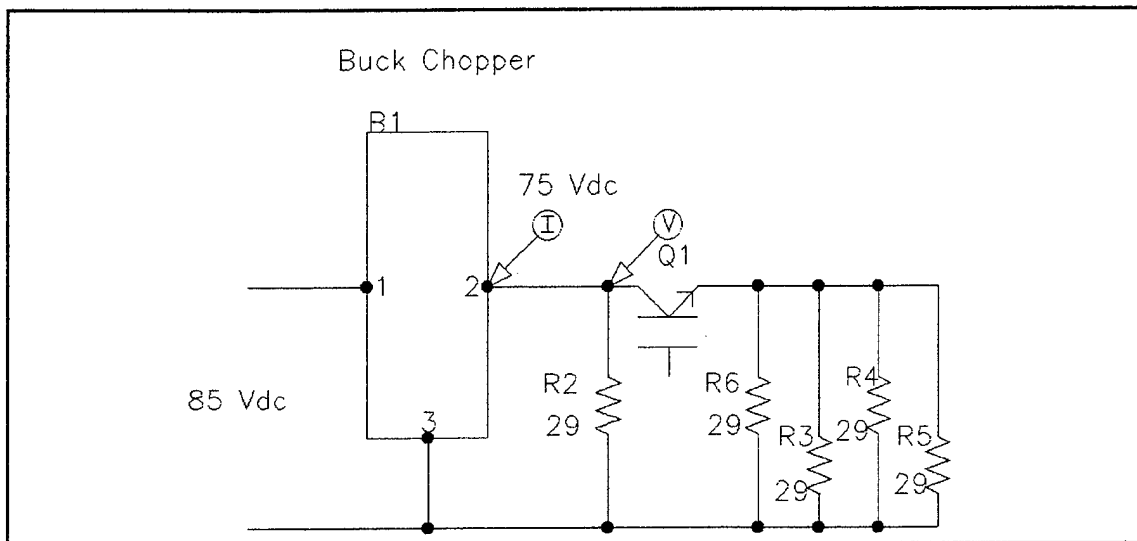


Figure 7.2. Resistive Load Test Circuit

The transient tests were conducted in the parallel and local mode of operation. In this mode the output voltage is based on a fixed reference value generated internal to the SBC31 program. This reference value establishes a no-load output voltage of 75.5 Vdc. The input voltage of the buck chopper was adjusted so the nominal voltage was 85 Vdc.

b. Test Results

The digital control transient response is shown in Figures 7.3 and 7.4. The resistance change is from 29 Ω to 5.8 Ω which corresponds to a load change from 19 percent to 97 percent of the rated maximum current for the prototype SSCM. The peak-to-peak measurement of 4.9 volts which occurred at a 78 percent change in load

demonstrates that the controller will meet the specification of ± 2.5 volts at a more conservative 50 percent change in load. The transient takes approximately 12ms to reach steady state. The difference in the steady state levels is 1.1 volts and is within 10 percent of the 1.0 volts that the 1 A/V droop programmed into the controller predicts. The waveform of the output voltage shares the same characteristics as the simulations modeling the state difference controller which incorporates the delays (Figure 7.5); specifically, the short duration peak, followed by a quick return to the regulated value.

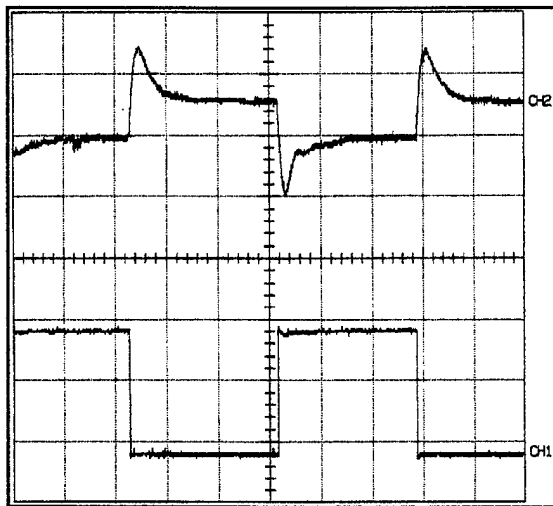


Figure 7.3. Output Voltage and Current for Digital Control and Resistive Loads
10ms/div CH2 (v_{out}) 2V/div
CH1 (i_{out}) 5A/div

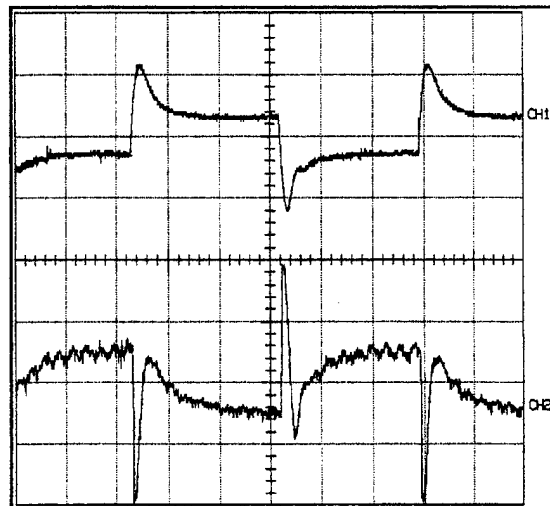


Figure 7.4. Output Voltage and Duty Cycle for Digital Control and Resistive Loads
10ms/div CH1 (v_{out}) 2V/div
CH2 (duty) 0.5V/div

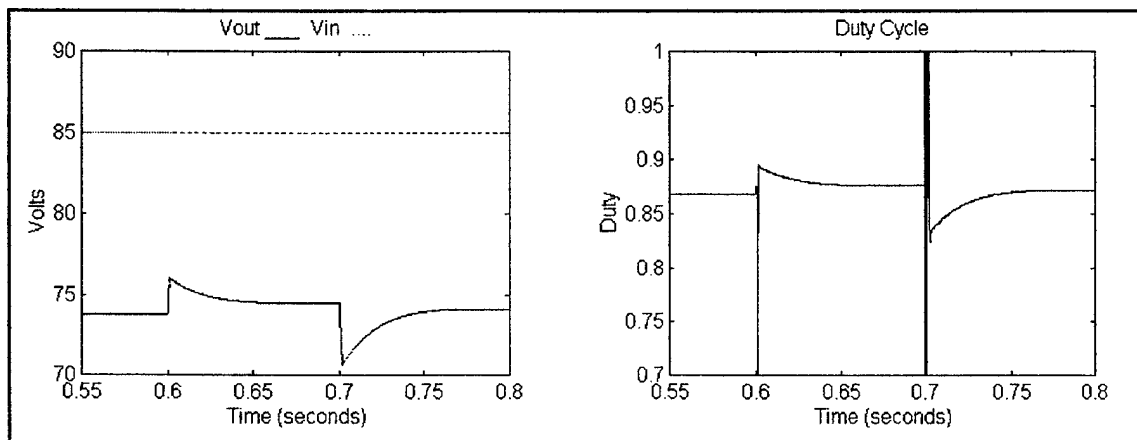


Figure 7.5. Digital Control and Resistive Loads Simulation

The duty cycle waveform differed from the predicted modeled waveform because it also was burdened with the task of compensating for droop in the power supply for the buck chopper while the simulations used an ideal voltage source with no droop. Also present on the duty cycle signal is a 360 Hz ripple from the rectified power supply for the chopper. The quick impulse that the duty cycle experiences in the model manifests itself as a broader pulse in the actual operation.

The controller does eliminate the oscillations of the output filter of the buck chopper. With a fixed duty cycle, the output voltage experiences oscillations during a transient (Figure 7.6) which are similar to those in the simulations (Figure 7.7). The oscillations are not as severe as predicted, but this can be attributed to the non-ideal characteristics of the circuit, the dynamic source voltage and the significant output impedance of the buck chopper.

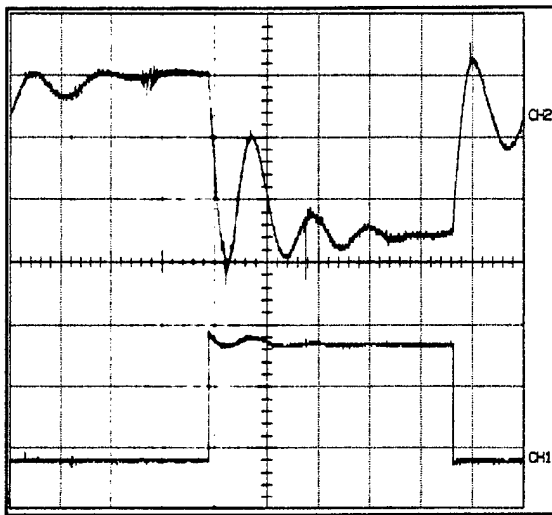


Figure 7.6. NPS Buck Chopper with Fixed Duty Cycle and Resistive Loads
10ms/div CH2 (v_{out}) 2V/div
CH1 (i_{out}) 5A/div

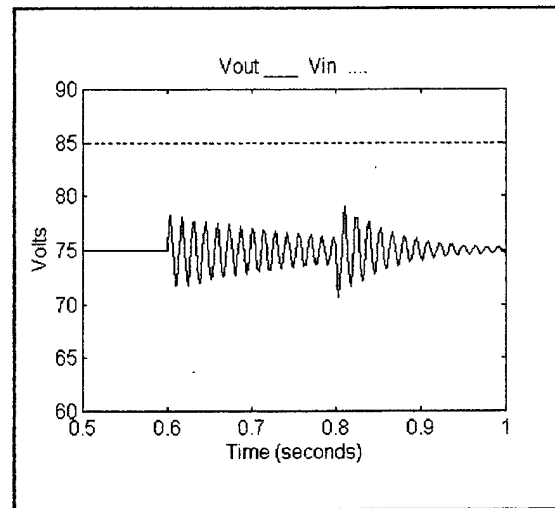


Figure 7.7. Fixed Duty Cycle Simulation

The analog control demonstrated a greater reduction in the peak values of output voltage during a transient than those which occurred with the digital control (Figure 7.8). This difference can be attributed to the delays found in the digital implementation that were not present in the analog version. The system with the analog

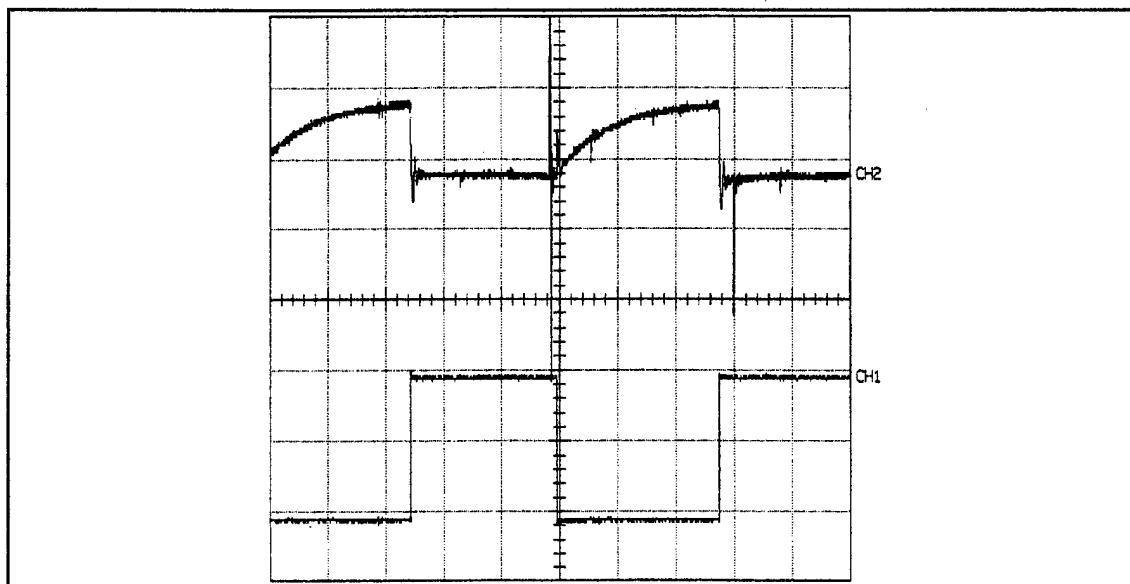


Figure 7.8. Output Voltage and Current for Analog Control with Resistive Loads
 10ms/division CH2 (v_{out}) 1V/division CH1 (i_{out}) 5A/division

controller also responded slower to the transients and took 50 milliseconds to reach the steady-state value after a prompt drop in the load. The slower response can be attributed to the difference between the gains of the digital and the analog controls. The flat response of the output voltage following an increase in load is due to the relatively small change in the duty cycle when attempting to support the falling voltage. The steady-state duty cycle is 0.88. The impulse from the error signal ($i_L - i_{out}$) can only create an impulse of height 0.12 to support the voltage, while an impulse of the 0.88 is available to prevent an excessive voltage. If the analog controller is placed in single and local mode, and the voltage is reduced to that of a 0.5 duty cycle, the up and down transients display slopes of the same magnitude but opposite directions.

3. Constant Power Loads

a. Test Description

The constant power load was created by using another prototype SSCM as a load (Figure 7.9). The output of the second SSCM was connected to a switched load bank used in the resistive load testing. An additional 29 Ω resistor was placed on the output of the first SSCM to offer it some resistive load when the second SSCM was not

operating. This prevented the first SSCM from operating with a discontinuous inductor current, a condition in which voltage control is not ensured. In addition, a 2400 μF capacitor was used as an input filter for the second SSCM. The capacitor minimizes the effect of current surges from the switching of the second buck chopper on the output current of the first buck chopper as illustrated in the differences between Figure 7.10 and Figure 7.11.

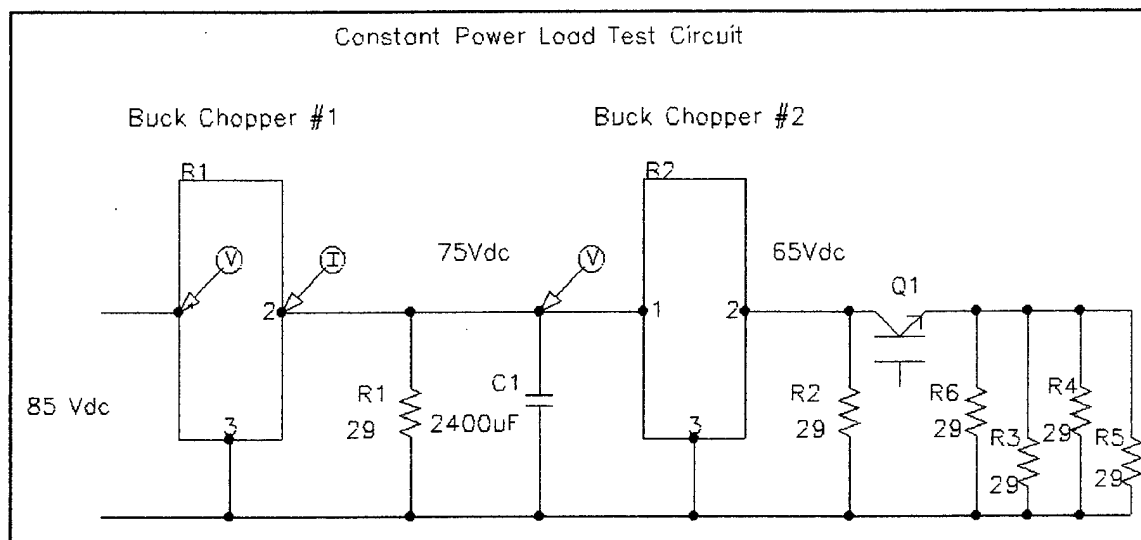


Figure 7.9. Constant Power Load Test Circuit

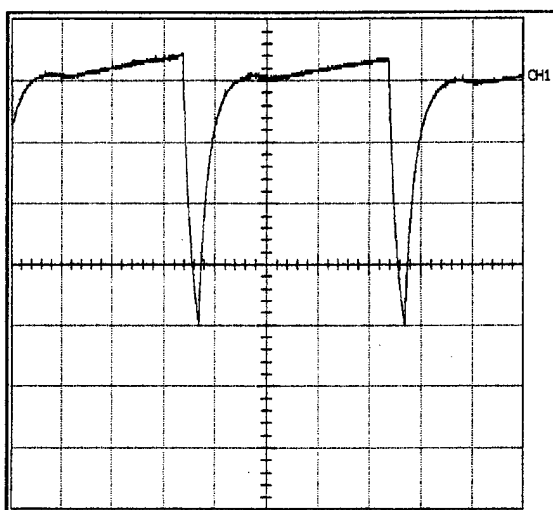


Figure 7.10. Output Current with Buck Chopper Load without 2400 μF Capacitor
CH1 (i_{out}) 2A/div

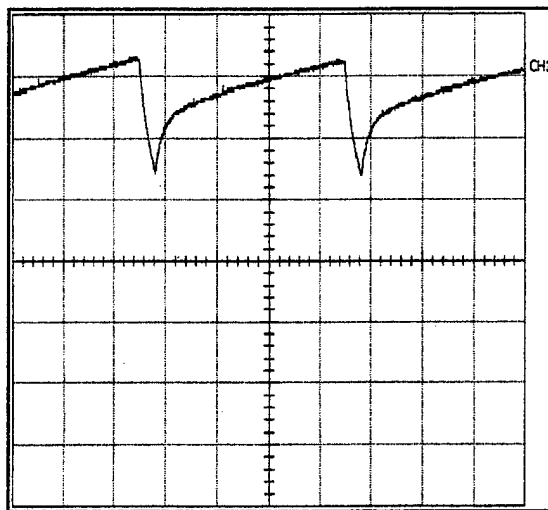


Figure 7.11. Output Current with Buck Chopper Load and 2400 μF Capacitor
CH1 (i_{out}) 2A/div

Both SSCMs were operated in the single and local mode. This mode allows the output voltage to be adjusted from the potentiometer on the front of the controller enclosure. The output voltage of the second buck chopper was set to a nominal value of 65 Vdc. The output voltage of the first buck chopper was set to a nominal value of 75 Vdc. The switch in the load bank is gated on and off to create load changes on the output of the second buck chopper that are passed on to the first buck chopper as changes in the constant power load.

b. Test Results

Only the digital controller was tested for its ability to handle constant power loads. The system was extremely stable. The voltage transient experienced with the change in a constant power load were not as severe as with the resistive load (Figure 7.12). This can be attributed to the less prompt nature of the transient and the reduction in the amount the load is changed. The delays of the second buck chopper combined with the additional 2400 μ F of capacitance prevents the load change from reaching the output of the first buck chopper as a prompt increase in power demand. In addition, the load changes only 7.8 amps or 58 percent vice the 78 percent load change of the resistive tests (Figure 7.13). The output current waveform of the first buck chopper also includes significant switching noise from the operation of the second buck chopper.

The severity of the droop with the non-ideal power supply used in the testing is illustrated in Figure 7.14. The 7.8 amp load change of the first buck chopper corresponds to approximately 6.9 amp change at the supply. This creates an almost 4 volt drop in input voltage. Also present in the waveform is the voltage ripple associated with the rectification of the three-phase power.

3. SBC31 Delay Measurement

The SBC31 introduces significant delays in the way it performs A/D and D/A conversions and the way the average output current is computed. These delays prevent the rapid response required to further reduce the transient voltages. The maximum delay is illustrated in Figure 7.15. The duty cycle rises to its maximum value in approximately 0.4 milliseconds. This agrees with the calculation of the maximum delay in Chapter V.

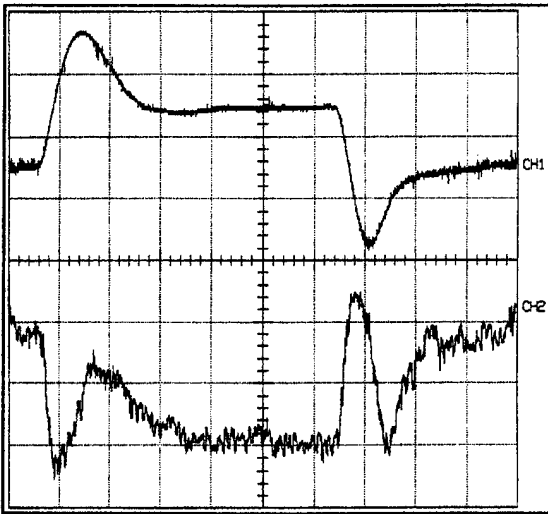


Figure 7.12. Output Voltage and Duty Cycle for Digital Control with Constant Power Load 5ms/div CH1 (v_{out}) 1V/div CH2 (duty) .2V/div

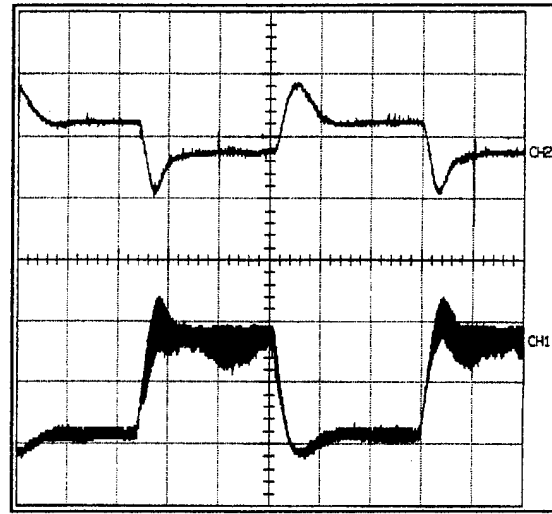


Figure 7.13. Output Voltage and Current for Digital Control with Constant Power Load 10ms/div CH2 (v_{out}) 2V/div CH1 (i_{out}) 5A/div

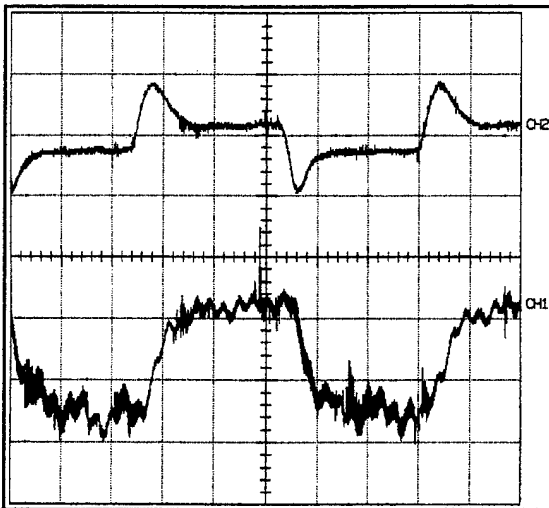


Figure 7.14. Output Voltage and Input Voltage for Digital Control with Constant Power Load 10ms/div CH2 (v_{out}) 2V/div CH1 (v_{in}) 2V/div

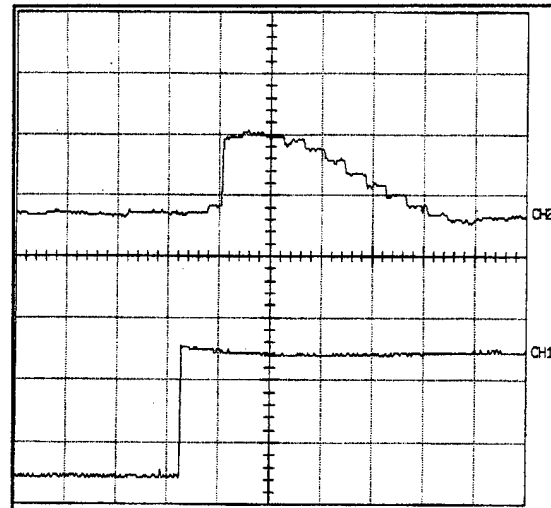


Figure 7.15. Digital Controller Delay 5μs/div CH2 (duty) 1V/div CH1 (i_{out}) 5A/div

4. Dynamic Performance Evaluation

The dynamic performance of the controller in the scaled environment predicts adequate control of the transients in the 100 kW units. The gains in the control algorithms must be altered for the higher voltages of the 100 kW SSCMs (see Equation

4.18). The output voltage appears stable and regulated for both resistive and constant power loads.

B. OPERABILITY TESTS

1. Protection Tests

Over-current timeout trip was tested for pass or fail. The trip was tested with a bank of six 29 Ω resistors in parallel. The trip was biased below the correct trip point and, as a result, it trips at lower currents and at faster speeds than it should. It does pass functionality and adjustments prior to installation will correct the setpoint.

The pulse-by-pulse current limit was tested with the circuit of Figure 7.16. The excessive load was switched in and out at 10 Hz. This prevented the over-current timeout trip from occurring. The limit does not prevent excessive inductor currents as designed (Figure 7.17). This failing can be traced to the filtering of the inductor current measurement prior to the trip. The delay from the filter allows the actual inductor current to exceed the 20 amp trip point and prevents recovery of the trip until approximately four switching periods later. This fault can be corrected by removing the inductor current filter.

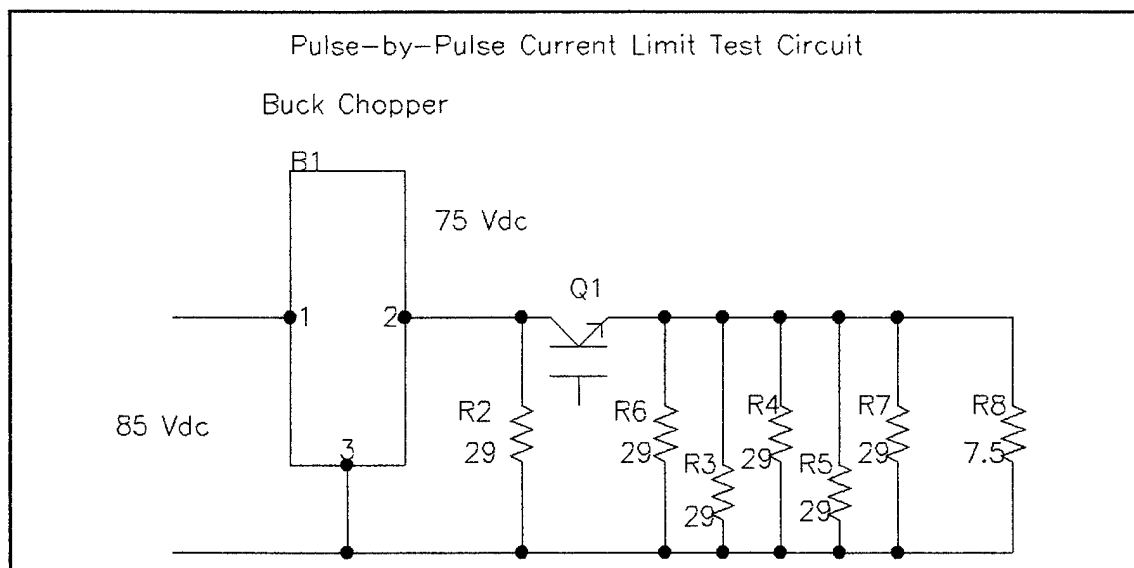


Figure 7.16. Pulse-by-Pulse Current Limit Test Circuit

Both the over-temperature trip and 24 volt supply power trips operated correctly. The 24 volt supply power trip actuated below 21.3 volts as implemented with the SBC31 and below 21.2 volts as implemented on the analog controller.

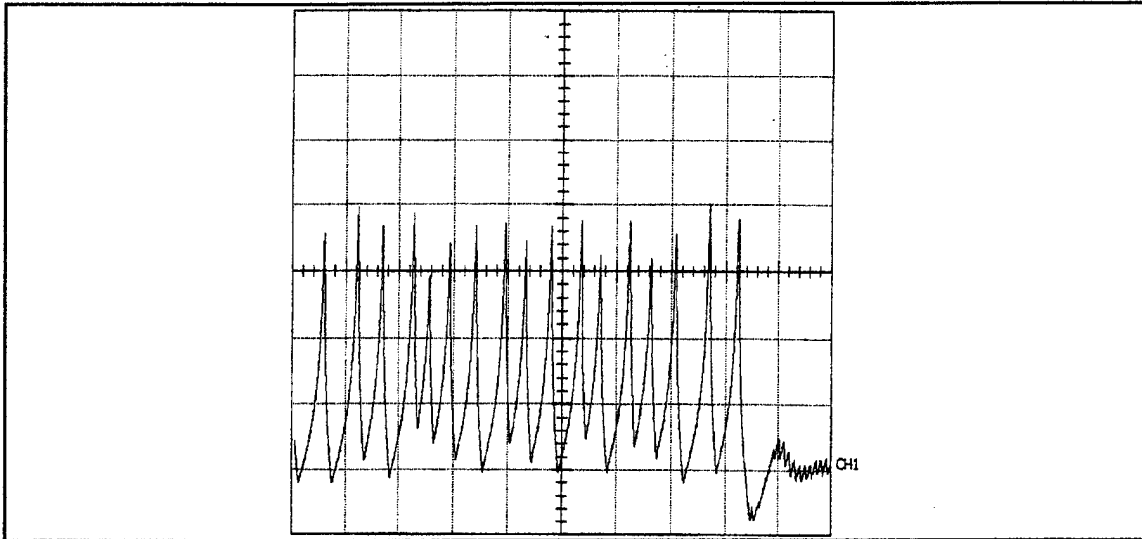


Figure 7.17. Failure of Pulse-by-Pulse Current Limit
2ms/division CH1 (i_L) 5A/division

2. Shutdowns

Both the analog and digital controllers performed all required shutdowns correctly. Shutdown was required for any mode other than local or when any protective trip occurred. The controller remained shutdown until the condition causing the shutdown was removed and the local/remote switch was cycled first to remote and then back to local.

3. Mode Control

Mode control was tested only in local operation. Presently, remote operation will shutdown the controller. The local and single mode tested satisfactory. The voltage could be adjusted with the fine and coarse adjust potentiometers from zero to two volts below the level of the supply voltage. The local and parallel correctly fixed the reference voltage to 75 volts.

4. Efficiency

The efficiency of the prototype SSCM was based on measurements of input and output voltage, input current, and load resistance (Table 7.1). The prototype SSCM was placed in the local and single mode while the load was incremental increased and measurements taken. The buck chopper maintained efficiencies above 97.5 percent throughout the test. These values are of interest for support of the claim in Chapter II that the SSCM would provide high-efficiency conversion. They do not reflect the efficiencies of the 100 kW SSCMs. The 100 kW SSCMs have switching losses and internal resistor losses which are a smaller proportion of its rated power and therefore should have even higher efficiencies than the NPS buck chopper.

Table 7.1. Prototype SSCM Efficiency

I_{in} (Amps)	V_{in} (Volts)	V_{out} (Volts)	R_{load} (Ohms)	P_{in} (Watts)	P_{out} (Watts)	Efficiency %
2.46	85.87	75.94	28.00	211.2	206.0	97.5
4.85	85.2	75.7	14.19	413.2	403.8	97.7
7.20	85.4	75.35	9.46	614.9	600.2	97.6
9.55	85.1	75.1	7.10	812.7	794.4	97.7
11.79	85.5	74.8	5.68	1008.1	985.0	97.7
14.12	85.1	74.5	4.73	1201.6	1173.4	97.7

VIII. CONCLUSIONS AND RECOMMENDATIONS

The SSCM controllers built at NPS provide the foundation for further development of the SSCMs and DC ZEDS at NSWC, Annapolis. The controllers offer basic functionality which can be expanded upon during the follow-on joint engineering effort between PPI, NSWC and NPS. The integration of the controllers with the 100 kW SSCMs will require modifications to the hardware and the software. In addition, testing at NPS has both uncovered design issues which must be addressed prior to integration and, provided great insight into the controller design that is source for many recommendations.

A. PRE-INTEGRATION DESIGN ISSUES

The pulse-by-pulse current limit must be modified by removing any filtering of the i_L signal prior to the protection circuit in the PWM integrated circuit. This will allow it to function as designed and limit the peak current of any pulse to 200 amps. In addition, the bias levels for the hardware protective trips must be adjusted to the correct trip points. This is accomplished with resistor replacement in the bias circuit for the respective trip. All protective trips should be retested to verify the correct trip points and proper operation prior to integration.

B. 100kW SSCM INTEGRATION

Integration of the controllers requires that the gains of the controllers be changed in both the software and the hardware to reflect the higher input voltage of the 100kW SSCMs. Specifically, the gains must be reduced by a factor of 10 based on Equation 4.18. The hardware gain changes require replacement of resistors in the appropriate amplifier circuits. The software changes are made in code which is then recompiled and downloaded to the SBC31. The expected refinement to the software during the integration and testing of the 100 kW SSCMs dictates that the code remain free of the SBC31 ROM.

Additional modifications must be made to account for the higher signal levels from the control parameter sensors and the 50 A/V vice 10 A/V scaling of the current

sensors. This requires software changes in the initialization portion of the code which changes the gains of MUX A to unity and modification of the current retrieval loops in the interrupt routine to account for the new scaling. The analog controller can compensate for the scaling by further adjustments to the gains in the amplifier circuits. The higher signal levels do not exceed the limits of the analog control and requires no modification.

Differences between the non-ideal parameters of the NPS buck chopper and the 100 kW buck chopper will require adjustments to hardware and software. The compensation term for the output impedance of the NPS buck chopper must be changed in the software to reflect the correct value for the 100 kW SSCM. An additional biasing resistor must be inserted to add bias to the reference voltage signal before the AD534 hardware multiplier for the analog control.

C. RECOMMENDATIONS

The engineering effort of developing the SSCM controllers provided a great amount of insight into the actual functional requirements of such controllers. Recommendations from these insights may provide direction for future development.

A better choice than the SBC31 for the digital implementation of the controller would be a microcontroller. The floating point capabilities of the SBC31 were not required and the delays associated with the A/D and D/A severely restricted the performance of the control algorithm. A microcontroller such as the Microchip PIC16C74 includes all that is required for the completion of the control algorithm in a single integrated chip. Specifically, it contains both A/D and PWM capabilities along with on-board program and data memory. The A/D data is immediately available to the processor once an A/D conversion is complete. The reductions in the delays offered by such a microcontroller would greatly benefit the performance and reduce the cost, while still allowing upgrades with minimal hardware replacement.

A recommended approach to the controller design would be to divide the labor between a microcontroller dedicated to the specific control algorithm and an additional processor to handle the auxiliary functions. The auxiliary functions would include

monitoring, external communications, mode control, and protective trips. This would allow the microcontroller to perform the control algorithm without the burden or interruption of the auxiliary functions.

The use of active high-order Butterworth filters vice the passive first-order low-pass filters and buffers would greatly enhance the ability to uncover the average components and reject the high-frequency switching components of the control parameter signals. A microcontroller with sufficiently high sampling frequency could implement the filtering completely in the digital domain, allowing even greater flexibility with field changes to the controller.

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APPENDIX A. STATE DIFFERENCE FEEDBACK SIMULATION M-FILES

The process of simulating state difference feedback using the following m-files is illustrated by the process flow chart of Figure 4.3.

% **Denoini.m** Initializes all variables to begin a simulation run.
%

% Set component parameters.

E=85;

L=.00135;

Ce=.000;

C=.0036;

R=5.625;

% Set the initial run period for .6 seconds to achieve steady state.

tt=.6;

% Initialize all data variables to 0.

tstart=0;

tstop=0;

vc=0;

il=0;

ilt=0;

vct=0;

time=0;

timet=0;

dt=0;

d=1;

EE=0;

Et=0;

ioutt=0;

iout=0;

is=0;

iso=0;

ioo=0;

```
% Denosta.m re-initializes the simulation for a run continuation.
% It updates the initial parameters to the last value when the
% simulation stops. It also maintains the arrays for the plots.
%
```

```
% Establish the state space parameters.
A=[-1/(R*(Ce+C)) 1/(Ce+C); -1/L 0];
B=[0;1/L];
CB=[1 0;0 1];
DB=[0;0];
```

```
% Set the start and stop time for the simulation.
tstart=tstop;
tstop=tstop+tt;
```

```
% Update the initial parameters.
vco=vc(length(time));
ilo=il(length(time));
iso=is(length(time));
ioo=iout(length(time));
ddo=d(length(time));
```

```
% Maintain the data arrays for plotting.
timet=[timet;time];
ilt=[ilt;il];
vct=[vct;vc];
dt=[dt;d];
Et=[Et;EE];
ioutt=[ioutt;iout];
```

```

% Denplot.m performs the final update of the data arrays by calling
% "denosta" and then plots the data. The run may be continued after
% the plotting by starting the simulation.
%
% Caution must be taken not to run "denosta" again prior to the
% continuation of the simulation following "denplot".
%

% Call "denosta" for final update of array data.
denosta;

% Plot data, title and comment plots.
subplot(2,2,1), plot(timet,vct,'r-',timet,ioutt,'b:')
axis([.6,1,0,80])
xlabel('Time (seconds)')
ylabel('Volts or Amps')
title('Vout ____ Iout ....')
subplot(2,2,2), plot(timet,dt,'r-')
axis([.6,1,0,1])
xlabel('Time (seconds)')
ylabel('Duty')
title('Duty Cycle')
subplot(2,2,4), plot(timet,dt,'r-')
axis([.6,1,.7,1])
xlabel('Time (seconds)')
ylabel('Duty')
title('Duty Cycle')
subplot(2,2,3), plot(timet,vct,'r-',timet,Et,'b:')
axis([.6,1,70,90])
xlabel('Time (seconds)')
ylabel('Volts')
title('Vout ____ Vin ....')

```

```

function [ret,x0,str,ts,xts]=dend(t,x,u,flag);
%Dend.m contains the code to support the graphical simulation of
%   the State Difference feedback of Figure 4.15. This code
%   is generated by the SIMULINK.
%
%DEND      is the M-file description of the SIMULINK system named DEND.
%   The block-diagram can be displayed by typing: DEND.
%
%   SYS=DEND(T,X,U,FLAG) returns depending on FLAG certain
%   system values given time point, T, current state vector, X,
%   and input vector, U.
%   FLAG is used to indicate the type of output to be returned in SYS.
%
%   Setting FLAG=1 causes DEND to return state derivatives, FLAG=2
%   discrete states, FLAG=3 system outputs and FLAG=4 next sample
%   time. For more information and other options see SFUNC.
%
%   Calling DEND with a FLAG of zero:
%   [SIZES]=DEND([],[],[],0), returns a vector, SIZES, which
%   contains the sizes of the state vector and other parameters.
%       SIZES(1) number of states
%       SIZES(2) number of discrete states
%       SIZES(3) number of outputs
%       SIZES(4) number of inputs
%       SIZES(5) number of roots (currently unsupported)
%       SIZES(6) direct feedthrough flag
%       SIZES(7) number of sample times
%
%   For the definition of other parameters in SIZES, see SFUNC.
%   See also, TRIM, LINMOD, LINSIM, EULER, RK23, RK45, ADAMS, GEAR.

% Note: This M-file is only used for saving graphical information;
%   after the model is loaded into memory an internal model
%   representation is used.

% the system will take on the name of this mfile:
sys = mfilename;
new_system(sys)
simver(1.3)
if (0 == (nargin + nargout))
    set_param(sys,'Location',[143,44,848,518])
    open_system(sys)
end;

```

```

set_param(sys,'algorithm', 'RK-45')
set_param(sys,'Start time', 'tstart')
set_param(sys,'Stop time', 'tstop')
set_param(sys,'Min step size', '0.000002')
set_param(sys,'Max step size', '0.002')
set_param(sys,'Relative error','1e-3')
set_param(sys,'Return vars', '')

add_block('built-in/Demux',[sys,/, 'Demux'])
set_param([sys,/, 'Demux'],...
    'outputs','2',...
    'position',[365,67,410,103])

add_block('built-in/Product',[sys,/, 'Product'])
set_param([sys,/, 'Product'],...
    'position',[195,75,220,95])

add_block('built-in/Constant',[sys,/, 'input voltage'])
set_param([sys,/, 'input voltage'],...
    'Value','E',...
    'position',[60,50,80,70])

add_block('built-in/Gain',[sys,/, 'hi'])
set_param([sys,/, 'hi'],...
    'orientation',2,...
    'Gain','.1231',...
    'position',[270,129,310,171])

add_block('built-in/Sum',[sys,/, 'Sum2'])
set_param([sys,/, 'Sum2'],...
    'orientation',2,...
    'position',[140,245,160,265])

add_block('built-in/Saturation',[sys,/, 'Saturation'])
set_param([sys,/, 'Saturation'],...
    'orientation',2,...
    'Lower Limit','0',...
    'Upper Limit','1',...
    'position',[85,245,110,265])

add_block('built-in/State-Space',[sys,/, 'State-space'])
set_param([sys,/, 'State-space'],...
    'A','A',...

```

```

        'B','B',...
        'C','CB',...
        'D','DB',...
        'X0','[vco;ilo]',...
        'position',[255,62,330,108])

add_block('built-in/To Workspace',[sys,/, 'input voltage record'])
set_param([sys,/, 'input voltage record'],...
    'mat-name','EE',...
    'buffer','10000',...
    'position',[230,12,280,28])

add_block('built-in/To Workspace',[sys,/, 'output voltage record'])
set_param([sys,/, 'output voltage record'],...
    'mat-name','vc',...
    'buffer','10000',...
    'position',[490,17,540,33])

add_block('built-in/Sum',[sys,/, 'current sum'])
set_param([sys,/, 'current sum'],...
    'orientation',2,...
    'inputs','+-',...
    'position',[370,140,390,160])

add_block('built-in/Gain',[sys,/, 'house curve'])
set_param([sys,/, 'house curve'],...
    'orientation',2,...
    'Gain','.1',...
    'position',[385,184,425,226])

add_block('built-in/To Workspace',[sys,/, ['duty cycle',13,' record']])
set_param([sys,/, ['duty cycle',13,' record']],...
    'mat-name','d',...
    'buffer','10000',...
    'position',[120,132,170,148])

add_block('built-in/Gain',[sys,/, ['steady state',13,' duty cycle']])
set_param([sys,/, ['steady state',13,' duty cycle']],...
    'orientation',2,...
    'Gain','1/E',...
    'position',[195,379,235,421])

add_block('built-in/Sum',[sys,/, 'Sum1'])

```

```

set_param([sys,'/','Sum1'],...
          'orientation',2,...
          'inputs','---',...
          'position',[195,156,215,344])

add_block('built-in/Gain',[sys,'/','hv'])
set_param([sys,'/','hv'],...
          'orientation',2,...
          'Gain','.0133',...
          'position',[240,229,280,271])

add_block('built-in/Gain',[sys,'/','hn'])
set_param([sys,'/','hn'],...
          'orientation',2,...
          'Gain','.25',...
          'position',[240,289,280,331])

add_block('built-in/Integrator',[sys,'/','Integrator'])
set_param([sys,'/','Integrator'],...
          'orientation',2,...
          'Initial','iso',...
          'position',[305,300,325,320])

add_block('built-in/Sum',[sys,'/',['corrected',13,'voltage ref']])
set_param([sys,'/',['corrected',13,'voltage ref']],...
          'orientation',2,...
          'inputs','-+',...
          'position',[425,255,445,275])

add_block('built-in/To Workspace',[sys,'/','time record'])
set_param([sys,'/','time record'],...
          'mat-name','time',...
          'buffer','10000',...
          'position',[570,372,620,388])

add_block('built-in/Clock',[sys,'/','Clock'])
set_param([sys,'/','Clock'],...
          'position',[470,370,490,390])

add_block('built-in/Sum',[sys,'/',['voltage',13,'sum']])
set_param([sys,'/',['voltage',13,'sum']],...
          'orientation',2,...
          'inputs','-+',...

```

```

        'position',[365,300,385,320])

add_block('built-in/To Workspace',[sys,/, 'integ'])
set_param([sys,/, 'integ'],...
        'mat-name','is',...
        'buffer','10000',...
        'position',[310,256,345,274])

add_block('built-in/Gain',[sys,/, 'resistor current'])
set_param([sys,/, 'resistor current'],...
        'orientation',2,...
        'Gain','1/R',...
        'position',[565,149,605,191])

add_block('built-in/Sum',[sys,/, 'Sum'])
set_param([sys,/, 'Sum'],...
        'orientation',2,...
        'position',[450,195,470,215])

add_block('built-in/To Workspace',[sys,/, ['inductor current',13,'record']])
set_param([sys,/, ['inductor current',13,'record']],...
        'mat-name','il',...
        'buffer','10000',...
        'position',[560,87,610,103])

add_block('built-in/To Workspace',[sys,/, ['output current',13,'record']])
set_param([sys,/, ['output current',13,'record']],...
        'mat-name','iout',...
        'buffer','10000',...
        'position',[470,112,520,128])

add_block('built-in/Constant',[sys,/, ['voltage',13,' reference']])
set_param([sys,/, ['voltage',13,' reference']],...
        'orientation',2,...
        'Value','75',...
        'position',[490,260,510,280])

add_block('built-in/Derivative',[sys,/, 'Derivative'])
set_param([sys,/, 'Derivative'],...
        'orientation',2,...
        'position',[600,225,630,245])

add_block('built-in/Gain',[sys,/, ['capacitor',13,'current']])

```

```

set_param([sys,'/','capacitor',13,'current'],...
          'orientation',2,...
          'Gain','Ce',...
          'position',[535,214,575,256])
add_line(sys,[335,85;360,85])
add_line(sys,[415,75;445,75;445,25;485,25])
add_line(sys,[225,85;250,85])
add_line(sys,[235,250;220,250])
add_line(sys,[85,60;180,60;190,80])
add_line(sys,[415,95;555,95])
add_line(sys,[80,255;70,255;70,90;190,90])
add_line(sys,[135,255;115,255])
add_line(sys,[85,60;170,60;170,20;225,20])
add_line(sys,[415,95;430,95;430,145;395,145])
add_line(sys,[365,150;315,150])
add_line(sys,[265,150;250,150;250,190;220,190])
add_line(sys,[235,310;220,310])
add_line(sys,[300,310;285,310])
add_line(sys,[190,250;165,250])
add_line(sys,[415,75;645,75;645,170;610,170])
add_line(sys,[190,400;180,400;180,260;165,260])
add_line(sys,[70,140;115,140])
add_line(sys,[360,310;330,310])
add_line(sys,[485,270;450,270])
add_line(sys,[380,205;360,205;360,245;460,245;450,260])
add_line(sys,[420,265;400,265;400,400;240,400])
add_line(sys,[400,305;390,305])
add_line(sys,[495,380;565,380])
add_line(sys,[300,310;295,310;305,265])
add_line(sys,[350,310;350,250;285,250])
add_line(sys,[645,170;645,315;390,315])
add_line(sys,[445,205;430,205])
add_line(sys,[445,205;445,155;395,155])
add_line(sys,[445,155;445,120;465,120])
add_line(sys,[560,170;500,170;500,200;475,200])
add_line(sys,[595,235;580,235])
add_line(sys,[530,235;505,235;505,210;475,210])
add_line(sys,[645,235;635,235])

```

drawnow

% Return any arguments.

if (nargin | nargout)

```

% Must use feval here to access system in memory
if (nargin > 3)
    if (flag == 0)
        eval(['ret,x0,str,ts,xts']=sys,'(t,x,u,flag);'])
    else
        eval(['ret =', sys,'(t,x,u,flag);'])
    end
else
    [ret,x0,str,ts,xts] = feval(sys);
end
drawnow % Flash up the model and execute load callback
end

```

APPENDIX B. SBC31 SOFTWARE FLOW CHARTS

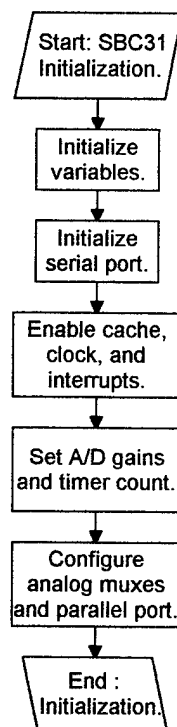


Figure B.1. SBC31 Initialization.

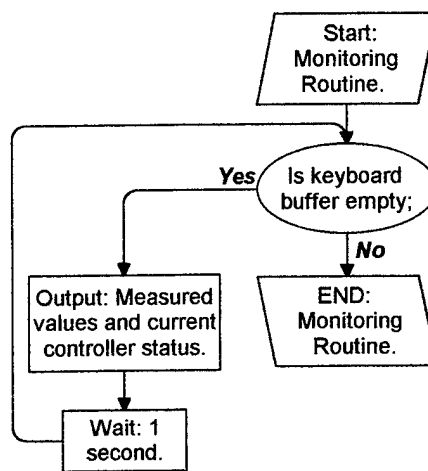


Figure B.2. Monitoring Routine

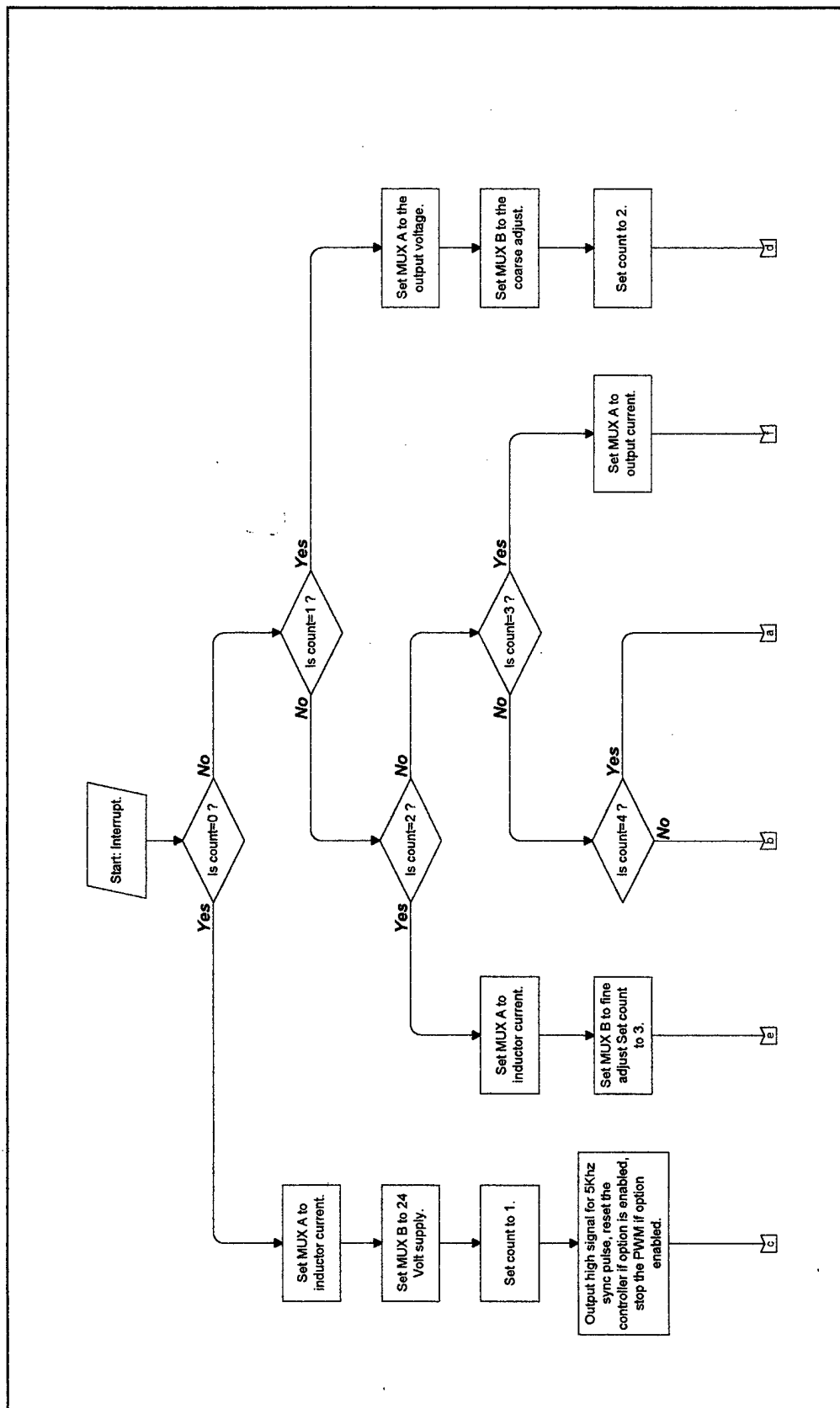
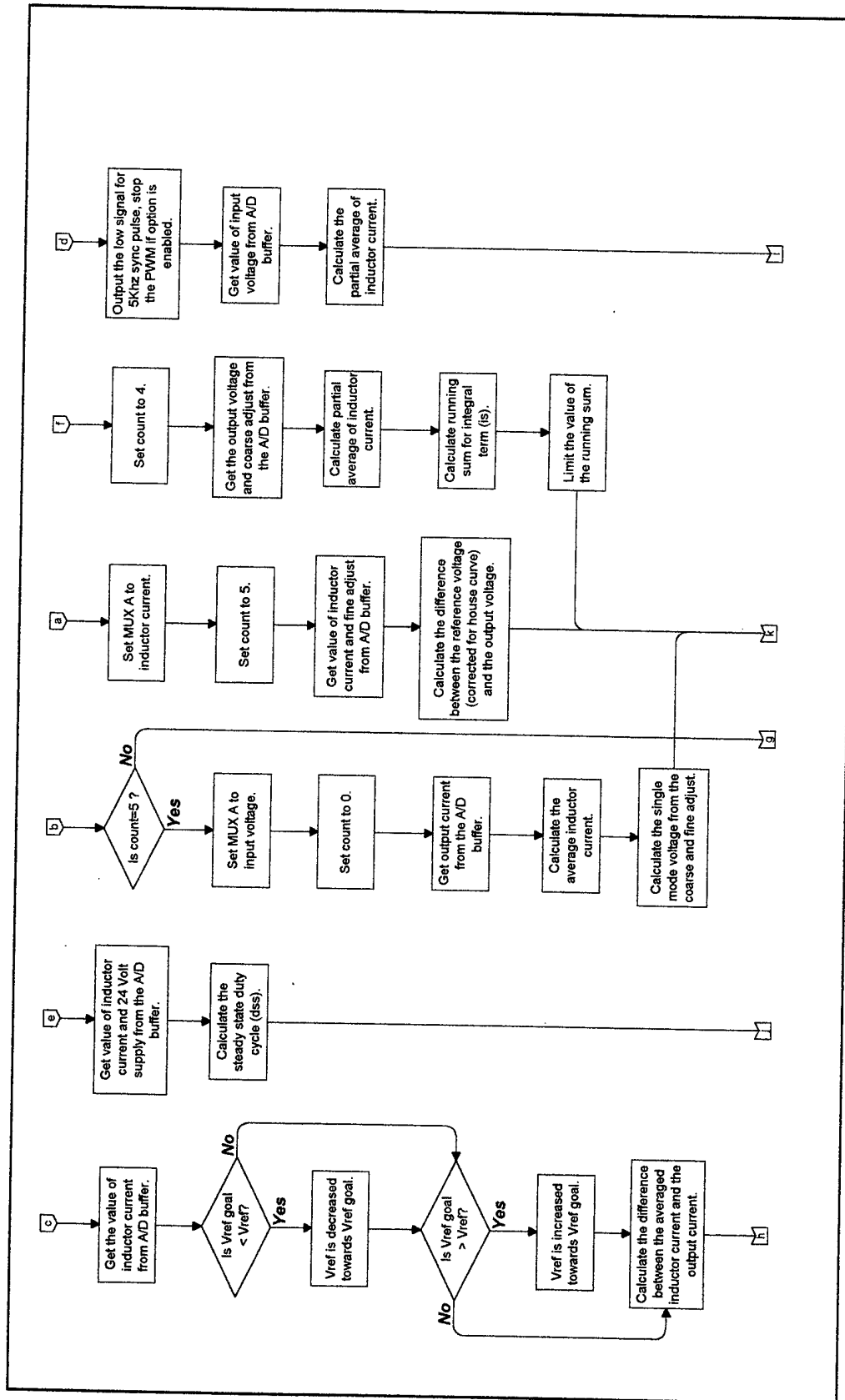


Figure B.3. Interrupt Routine (1 of 5)



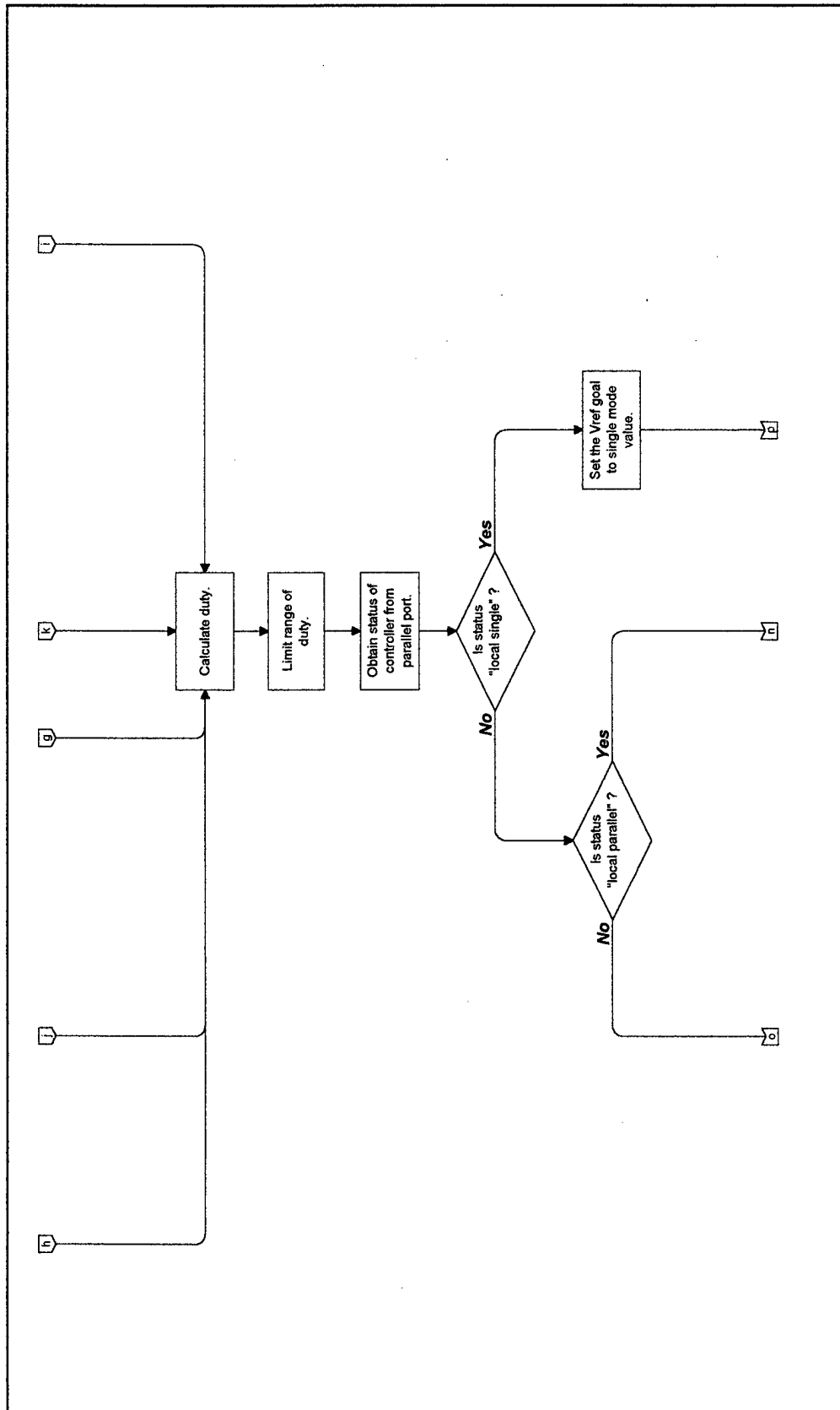


Figure B.5. Interrupt Routine (3 of 5)

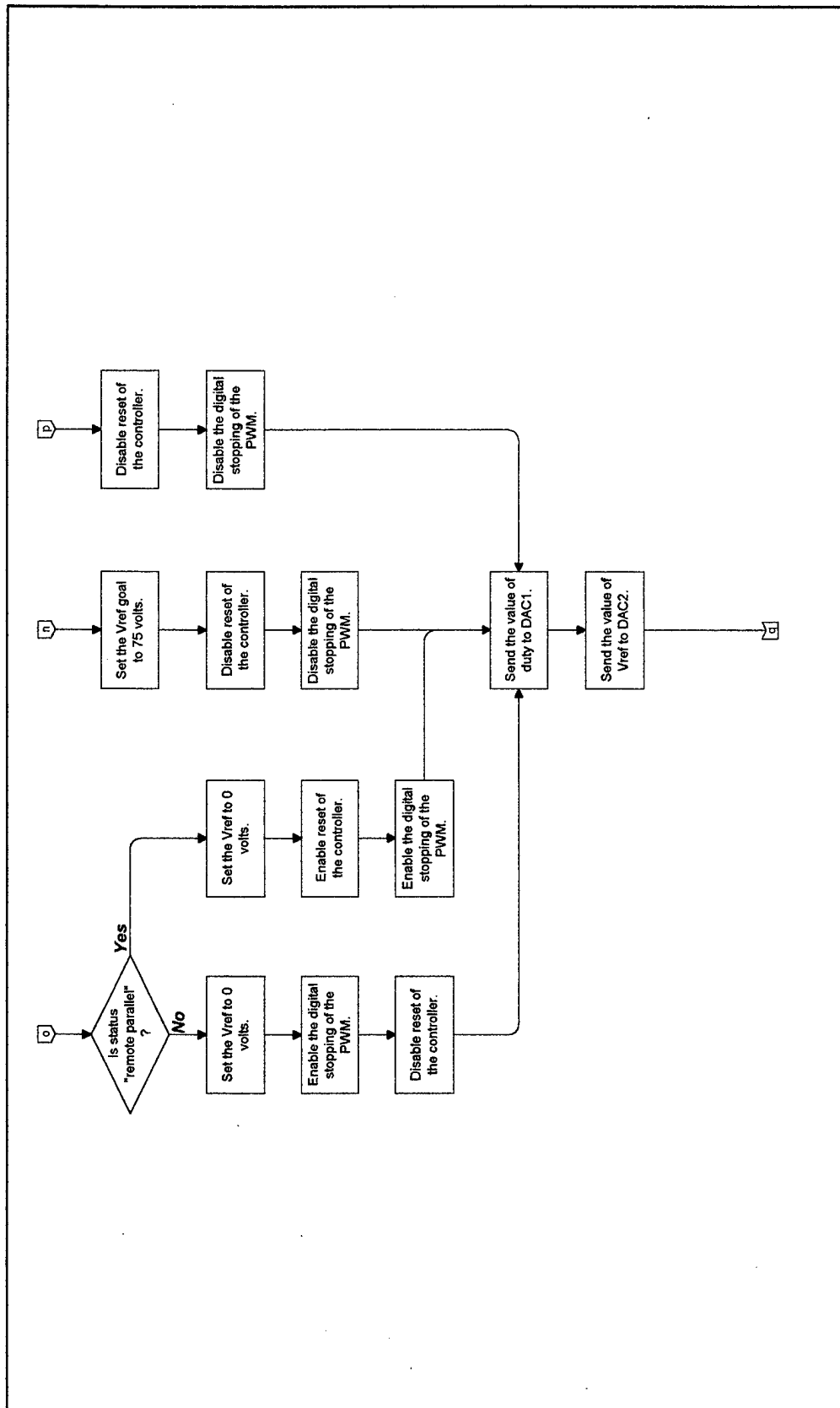


Figure B.6. Interrupt Routine (4 of 5)

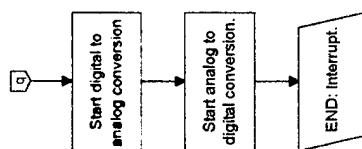


Figure B.7. Interrupt Routine (5 of 5)

APPENDIX C. SBC31 SSCM CONTROLLER SOURCE CODE

```
/*
* File: cont.c
* Name: Benjamin D. Salerno
* Project: Buck Control on SBC31
* Operating Environment: SBC31 w/ Talker
* Compiler: TMS320C3x/4x C Compiler by Texas Instruments under MSDOS 5.0
*
* Description: This program implements a control for the 1KW buck
* converter at Naval Postgraduate School. Modification to the gains
* (HI, HV, and HN of Equation 5.1) is made by direct modification to
* the final duty cycle summation as marked in the source code. This
* will allow the control to be used with the 100KW SSCM of NSW. The
* program also controls operating modes, and monitors and reports the
* status of the SSCM.
*
* Inputs:      The values of vout, il, vin, and iout
*              The values of the coarse and fine adjust potentiometers
*              The value of the 24 volt supply
*              The status bits for analog control trips
*
* Constants:   The steady state reference voltage
*
* Outputs:     PWM Disable signal
*              Duty cycle
*              Trip Reset signal
*              5 Khz reference waveform
*              Reference voltage
*/

#include "periph.h"
#include "stdio.h"

/* Prototypes */
void c_int04();

/* Constants */
const int VREF_SS = 9965; /* reference parameter for parallel mode*/

/* Variables */
int di=0,dv=0; /* current difference and voltage difference*/
int duty=0,count=0; /* duty cycle and interrupt counter*/
```

```

int vout=0,vin=0,vt=0;
int il=0,is=0,io=0;
int dss=0,ca=0,fa=0, psa=0;/* steady state duty cycle and volateg adjusts and status*/
int it=0,cv=0,vset=0;/* average current, 24V control power and reference set term*/
int vref=0,vsep=0;
int col,row;
int abc=2,abr=0;/* control and reset words*/
int psd=0,itt=0;/* status and current summation*/

main()
{
/* declare variables and constants*/

MHZ=50;

/* Initialize SBC31*/

enable_cache();
init_serial();
enable_clock();
enable_interrupts();
install_int_vector(c_int04,4);
enable_analog();
set_mux_a(1);
set_mux_b(0);
set_gain_a(4);
set_gain_b(1);
*PIA_d=156;
enable_interrupt(3);
timer(2,30000);
wherexy(&col,&row);

/* Start monitoring routine*/
while (!kbd_hit()){
    printf("\n                ");
    gotoxy(col,row);
    printf("\n IS=%d VIN=%d VOUT=%d io=%d di=%d IL=%d", is, vin,
        vout, io, di, il);
    gotoxy(col,row);
    ms(1000);
}
}/* end main*/

```

/* Interrupt from timer */

void c_int04()

```
{
  if (count==0)
  {
    set_mux_a(4);
    set_mux_b(0);
    count=1;
    set_abits(8+abc+abr);
    io=-adc(0);
    if (vref>vset)
      vref=vref-1;
    if (vref<vset)
      vref=vref+1;
    di=(il-it)*8;
    itt=it;
  }
  else if (count==1)
  {
    set_mux_a(0);
    set_mux_b(2);
    count=2;
    set_abits(abc+1);
    vin=-adc(0);
    it=io;
  }
  else if (count==2)
  {
    set_mux_a(4);
    set_mux_b(6);
    count=3;
    io=-adc(0);
    cv=-adc(1);
    dss=((vref+itt/90-itt/90)*32767)/vin;
  }
  else if (count==3)
  {
    set_mux_a(6);
    count=4;
    vout=-adc(0);
  }
}
```

```

        ca=-adc(1);
        it=io+it;
        is=is+dv;
        if (is>13000000)
            is=13000000;
        if (is<-13000000)
            is=-13000000;
    }
else if (count==4)
{
    set_mux_a(4);
    count=5;
    io=-adc(0);
    fa=-adc(1);
    dv=(vout-vref+itt/90);
}
else if (count==5)
{
    set_mux_a(2);
    count=0;
    il=-adc(0);
    it=(io+it)/3;
    vsep=(fa>>5)+ca*2/3;
}
duty=-dss+is/800+(dv/3+di/26);/*MODIFY THIS CODE FOR GAIN ADJUST*/
if (duty>0)
    duty=0;
if (duty<-32767)
    duty=-32767;
psd=*PIA_a;
psd=psd+(~(psd|31));
psa=(psd<<31)>>31;
if (psd== -30)
{
    abc=0;
    abr=1;
    vset=vsep;
}
else if (psd== -14)
{
    vset=VREF_SS;
    abc=0;
    abr=1;

```

```

    }
else if (psa== -1)
    {
        vref=0;
        abr=0;
        abc=2;
    }
else
    {
        abc=2;
        vref=0;
        abr=1;
    }
dac(1,duty);
dac(0,(vref/4));
*DAC0 = 0;
*ADC = 0;
}/* end interrupt*/

```


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