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The primary motivation of this work has been to investigate the growth, fabrication, and device physics of Silicon-based Heterostructure Devices. The goal is to extend performance limitations of existing devices and to develop silicon-based heterojunction technology for the fabrication of new types of transistors (e.g. quantum devices). The basic device structures investigated in this work are the Si/SiGe Heterojunction Bipolar Transistor (HBT) and the Strained-Si n-MOSFET. Epitaxial layers are grown by the

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LIMITED REACTION PROCESSING: HETEROSTRUCTURE AND NOVEL DEVICE FABRICATION

FINAL REPORT

May, 1996

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LIMITED REACTION PROCESSING: HETEROSTRUCTURE AND NOVEL
DEVICE FABRICATION

FINAL REPORT

J.L. Hoyt

May, 1996

.FOREWORD

This document is the final report for U.S. Army Research Office contract number DAAL03-91-C-0026 which corresponds to the proposal entitled "Limited Reaction Processing: Heterostructure and Novel Device Fabrication" (ARO proposal number 28729-EL). The original proposal covered the period from June 1, 1991 - December 31, 1994. In late 1994, the scope of work was expanded and the contract was extended to cover the period from September 1, 1994 - March 31, 1996. The above contract also served as the parent agreement for the ARO-supported AASERT fellowship entitled "Electron Device Applications of Strained-Si Epitaxial Layers" (contract DAAL03-92-G-0055). This report describes research performed under the original contract and the contract extension, as well as highlights from the AASERT project.

The primary motivation of this work has been to investigate the growth, fabrication, and device physics of Silicon-based Heterostructure Devices. The goal is to extend performance limitations of existing devices and to develop silicon-based heterojunction technology for the fabrication of new types of transistors (e.g. quantum devices). The basic device structures investigated in this work are the Si/SiGe Heterojunction Bipolar Transistor (HBT) and the Strained-Si n-MOSFET. Epitaxial layers are grown by the rapid thermal, low pressure chemical vapor deposition technique known as limited reaction processing. The research involves materials characterization and semiconductor processing, with an emphasis on obtaining a fundamental understanding of electronic properties and device physics. The specific problems studied in this research include characterizing minority carrier transport and heavy doping effects in Si/SiGe/Si HBTs, investigation of boron diffusion in SiGe, fabrication and analysis of the first high mobility, strained-Si MOSFETs, and preliminary study of the feasibility of adding carbon to SiGe layers to expand the opportunities for Column IV heterostructures. The HBT research was carried out in collaboration with Hewlett-Packard (Palo Alto, CA), and Motorola (Mesa, AZ) has maintained a strong interest in our work on the strained-Si MOSFET.

TABLE OF CONTENTS

STATEMENT OF THE PROBLEMS STUDIED

Silicon is the material of choice for high density integrated circuits. Metal-oxide-semiconductor field-effect transistors (MOSFETs) and/or bipolar junction transistors are the basic building blocks of these circuits. To a large extent, the performance of these devices has improved over the years by scaling both lateral and vertical dimensions. However, both practical and fundamental limits to this scaling, and to the resulting performance advantages, are being reached. These performance limits can be extended by introducing other silicon-compatible materials, such as SiGe, into the device structure to form heterojunctions. The use of Si/SiGe heterojuctions provides a powerful combination of the performance advantage usually associated with III-V semiconductor devices, with the well-developed manufacturing technology of silicon. The n-Si/p-SiGe/n-Si HBT is the most advanced Si-based heterojunction device to date, and is one of the most promising devices for manufacturing silicon-based high performance circuits. Significant speed enhancements have been demonstrated at both the device and circuit level, and very high performance systems incorporating Si/SiGe HBTs are currently going into production in a joint Hughes/IBM project.

In this work, we study two key problems in the device and processing physics for Si/SiGe HBTs, and obtain information which is essential to modeling, optimization and fabrication of these devices. The first project concerns the characterization of the effects of heavy doping on electron transport in p-type strained SiGe. Despite the high-speed performance demonstrated with Si/SiGe HBTs, most of the electron transport parameters in strained p-SiGe, which control HBT performance, are unknown. Characterization and understanding of the transport parameters in heavily doped p-SiGe alloys is essential for accurate modeling of Si/SiGe HBTs.

The second HBT-related project involves a detailed study of the diffusion of boron, the p-type dopant in npn HBTs, in SiGe. Dopant diffusion is reasonably well characterized and understood in silicon. However, data for dopant diffusion in SiGe is lacking. In particular, for HBT design and optimization, it is important to have an understanding of boron diffusion in SiGe. A detailed study of boron diffusion in SiGe was undertaken in this project.

In addition to the work in the area of Si/SiGe HBT technology, we also performed a study of the application of strained Si grown on relaxed SiGe layers to MOS technology

(AASERT project). The strained Si device area is much less developed than the Si/SiGe HBT. The devices fabricated in this project were the first strained Si MOSFETs. The goal of this work was to determine what enhancements in device performance can be achieved, and at what cost in increased fabrication complexity. A broad range of experiments were performed to learn as much as possible about the growth of the material, the effect of various fabrication processes, and the electronic properties of the resulting structures. In addition to clearly demonstrating enhanced device performance in long-channel MOSFETs, several important physical characteristics of the strained-Si material itself were also measured.

Finally, the problem of the extension of silicon-based heterojunctions to include alloys of Si, Ge, and C is explored in a preliminary feasibility study of the growth and basic electronic materials properties of SiGeC alloys. The goal of this project was to perform a preliminary investigation of the growth and materials properties of these alloys, by simply adding a carbon-containing precursor to the gas stream during growth of SiGe. The basic materials properties (strain compensation, carbon substitutionality, etc.) were studied, and preliminary measurements of the band offsets and electronic properties were performed. The objective was to study the feasibility of using Si/SiGeC heterojunctions as a means of expanding the application of silicon-based heterojunctions, particularly with respect to obtaining band offsets suitable for quantum devices.

SUMMARY OF IMPORTANT RESULTS

In this section, the important results for each of the focus areas studied under this contract (SiGe HBTs, strained Si MOSFETs, and SiGeC materials) are summarized.

(A) Si/SiGe Heterojunction Bipolar Transistors -- Heavy Doping Effects

The main objective of the HBT device project is to measure the transport parameters, such as dopant-induced bandgap narrowing in heavily doped, strained p-SiGe. High base doping is key to obtaining low base resistance and high frequency performance in these devices. The understanding of the doping dependence of the transport parameters obtained in this work is important for the design and optimization of Si/SiGe HBTs.

Outdiffusion of the boron from SiGe into the adjacent p-type Si regions must be avoided during device growth and processing. In order to achieve this, undoped SiGe spacer

layers are grown on each side of the p^+ SiGe base region (see section B below for a detailed study of boron diffusion in SiGe). Device and process simulations were used to study various factors which impact the choice of SiGe spacer layer thickness in heavily doped Si/SiGe HBTs. One of the key conclusions derived from this analysis is that the insertion of SiGe spacer layers dramatically increases the sensitivity of base current to lifetime in SiGe alloys. This constraint imposes an upper limit on the SiGe spacer layer thickness.

Boron outdiffusion is found to be dramatically enhanced by implant-associated defects during 850C, 10 sec. rapid thermal annealing following arsenic emitter contact implantation. Two techniques which dramatically reduce this defect-enhanced diffusion were studied. These include (1) reducing the post-emitter-implant-anneal to 600C, 2 min. and (2) using a pulsed laser anneal to activate the emitter contact implant. HBTs fabricated using these techniques show good device performance. In addition, high oxygen content ($\sim 10^{20}$ cm^{-3}) in p-SiGe is found to dramatically reduce implant-damage-enhanced boron diffusion in Si/SiGe HBTs, though it also reduces the electron lifetime and is thus a less practical solution [1].

The device and design issues specific to the fabrication of n-Si/p^+-SiGe/n-Si HBTs were investigated in this work. Mesa-isloated test transistors suitable for extraction of minority carrier diffusivity D_n and bandgap narrowing were fabricated and analyzed. The measured $D_n n_i^2$ product, extracted from DC measurements of the collector current in Si/SiGe HBTs, indicates that heavy doping effects are prominent in p-type SiGe alloys. In this study, a combination of DC and AC measurements are performed on Si/SiGe HBTs to *independently* extract the doping dependence of the apparent bandgap narrowing and D_n in p-SiGe. In other studies of bandgap narrowing, assumptions about the values of D_n have been made in order to attempt to measure bandgap narrowing. The minority electron diffusivity in p-SiGe is extracted by performing s-parameter measurements on small-geometry Si/SiGe HBTs. The doping dependence of D_n in p-SiGe is observed to be similar to that in Si, remaining relatively constant for doping above 4 x 10^{18} cm^{-3}. However, the measured values of D_n in p-SiGe are consistently below those for Si at all dopings.

The values for apparent bandgap narrowing extracted for SiGe in this study are simliar to those in Si, for doping below 10^{19} cm^{-3}. However, at higher doping concentrations, the increase in the apparent bandgap narrowing is less pronounced in p-SiGe, relative to Si.

This is attributed to the lower valence band density of states in p-SiGe, which makes the impact of Fermi-Dirac statistics more prominent at lower doping in p-SiGe relative to p-Si.

The apparent bandgap narrowing values in p-SiGe are corrected for the impact of Fermi-Dirac statistics to extract the *actual* dopant induced bandgap narrowing in SiGe. As shown in Fig. 1, these results indicate that bandgap narrowing values in SiGe exceed those in Si for doping above 10^{19} cm^{-3}, in agreement with theoretically predicted values for SiGe [2]. These are the first experimental results to fully test the published theory for doping induced bandgap narrowing in SiGe. The higher bandgap narrowing values observed in heavily doped p-SiGe relative to Si are also attributed to the smaller valence band density of states. The lower valence band density of states in p-SiGe is less effective in screening the negatively charged acceptors, thereby increasing the contribution of the bandgap narrowing component due to the impurity-carrier interaction. Finally, we use our heavy-doping parameters to simulate the collector current of several HBTs published in the literature [3] and find very good agreement for SiGe HBTs with Ge contents up to 30% (Fig. 2).
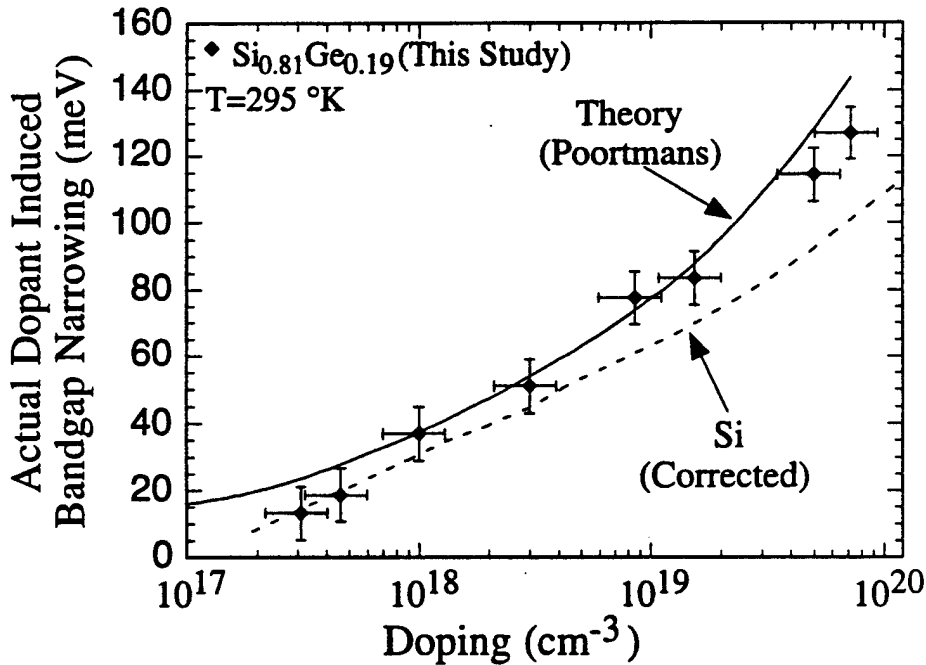

Fig. 1: Doping dependence of the corrected dopant induced bandgap narrowing in SiGe and Si obtained by correcting the apparent bandgap narrowing data extracted in this work, by using Fermi-Dirac statistics and taking into account the effect of non-parabolicity of the valence bands. This work shows that the theory of Poortmans is in reasonable agreement with our experimental results.
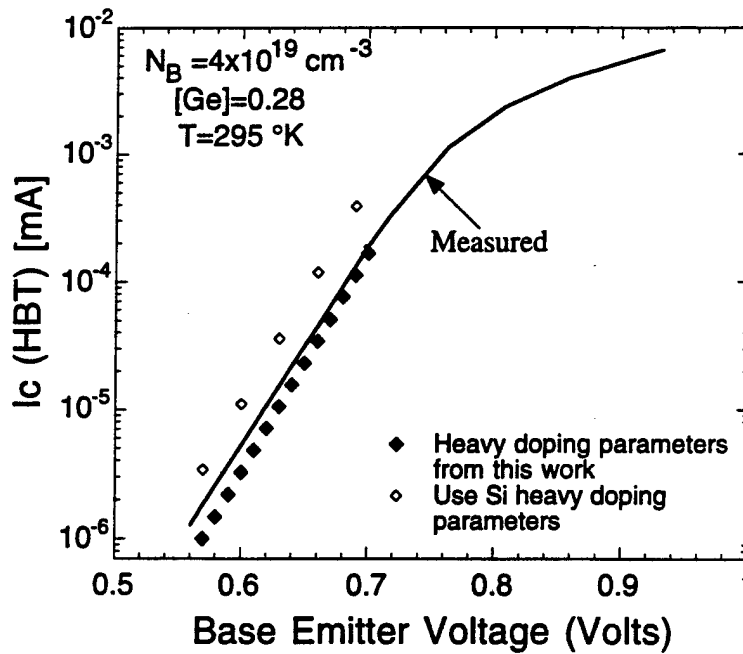
8

Fig. 2: Comparison of the calculated collector current using heavy doping parameters from this work (solid symbols) with experimentally measured values reported by Daimler-Benz (line) [3]. The HBT has a Ge composition of 28% and a base doping of 4 x 10^{19} cm^{-3}. The open symbols represent the collector current calculated by using the heavy doping parameters in p-Si. Clearly, much better agreement is obtained using the parameter values for SiGe extracted in this work, compared to the values for p-type Si.

(B) Si/SiGe HBTs -- Boron diffusion in SiGe

For optimal HBT device and fabrication process design, it is important to have an understanding of boron diffusion in Si/Si$_{1-x}$Ge$_x$ heterostructures. Dopant diffusion is reasonably well characterized and understood in silicon; however, data for dopant diffusion in Si$_{1-x}$Ge$_x$ is lacking. Boron is the dopant of choice for the Si$_{1-x}$Ge$_x$ base layers in HBTs; therefore, the objectives of this work are experimental characterization and modeling of boron diffusion in Si/Si$_{1-x}$Ge$_x$ heterostructures. In addition to its importance for silicon heterostructures, studying boron diffusion in SiGe influences our understanding of diffusion in silicon in general, and thus can impact silicon homojunction device technology as well.

In this work we characterized boron diffusion in silicon and Si$_{1-x}$Ge$_x$ using SIMS (secondary ion mass spectrometry) and SUPREM IV, a silicon process simulation program. In this project, we reported the first observation of slower boron diffusion in strained SiGe than in Si [4]. As shown in Fig. 3, the boron diffusivity decreases dramatically with increasing Ge content. This turns out to be quite beneficial to HBT fabrication, where boron diffusion must be minimized. In addition, the slower diffusivity of boron in SiGe alloys indicates that it is possible to use thin SiGe "barrier layers" to reduce boron diffusion in conventional silicon devices (e.g. in the region under gate in an

n-MOSFET, to provide a steeper retrograde boron profile). The major findings of this work are summarized as follows:

- systematic characterization of boron diffusion in strained $Si_{1-x}Ge_x$ as a function of germanium content ($0 < x < 0.20$), annealing temperature (750 to 850 °C), and boron concentration (1×10^{17} to 1×10^{20} cm^{-3}) shows that
  - boron diffusivity shows enhancement with boron concentration in both silicon and $Si_{1-x}Ge_x$,
  - boron diffusivity decreases with increasing germanium content,
  - the activation energy for intrinsic boron diffusivity increases with germanium content.
- using relaxed $Si_{1-y}Ge_y$ buffer layers as "substrates" for the $Si_{1-x}Ge_x$ diffusion structures, we showed that boron diffusion in $Si_{1-x}Ge_x$ is primarily a function of germanium content x and does not appear to depend strongly on macroscopic biaxial strain, contrary to theoretical prediction based on total energy calculations.
- $Si_{1-x}Ge_x$ does not appear to be a strong sink for silicon interstitials injected from the top via a silicon surface thermal oxidation process.
- as in silicon, the mechanism for boron diffusion in $Si_{1-x}Ge_x$ ($x < 0.20$) involves mostly silicon interstitials.
- the $Si_{1-x}Ge_x$/Si segregation coefficient for boron as it diffuses across the heterointerface increases with increasing germanium content.
- a pairing interaction between boron and germanium could be responsible for the slower boron diffusion in low-germanium-content $Si_{1-x}Ge_x$. A model incorporating this mechanism was developed and provides a good fit to the measured boron diffusivity as a function of Ge content.

In addition to the work on boron diffusion in SiGe, we also studied several samples of boron diffusion in strained silicon grown on relaxed SiGe, and found that the measured boron diffusivity is not a strong function of macroscopic strain in silicon.
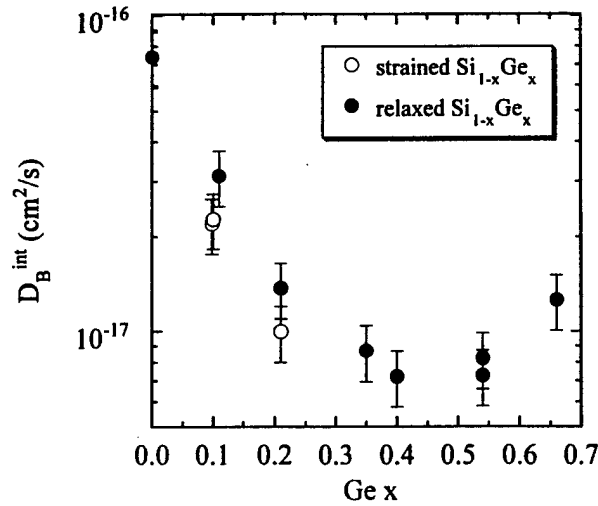
Fig. 3: Measured intrinsic boron diffusivity, $D_B{}^{int}$ in both strained and relaxed SiGe alloys (T=800C). The boron diffusivity decreases dramatically with increasing Ge content, and is only weakly dependent upon the macroscopic strain in the alloy layer.

(C) Strained-Si MOSFETs

Enhancing the electron mobility in the channel of a MOSFET has the potential to extend the performance limits of existing MOS technology. Inducing biaxial tension in Si will split the normally degenerate conduction and valence band minima. One method of producing this strain is to grow thin layer of silicon pseudomorphic to a substrate with a larger in-plane lattice constant, such as relaxed SiGe. Theoretical predictions indicate that the band splitting can improve the mobility of both holes and electrons, and cause conduction and valence band offsets between the strained silicon material and the relaxed SiGe. To investigate some of these predictions experimentally, *n*-MOSFETs with strained-Si channels were fabricated (Fig. 4) in this project.
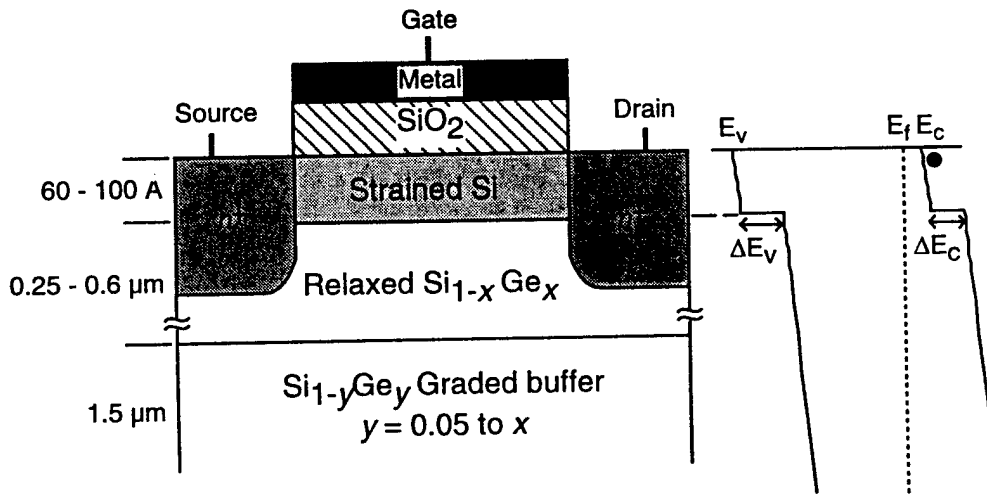

Fig. 4: Device structure and band diagram for the surface-channel strained Si MOSFET. Band diagrams are computed for n-MOSFETs on $Si_{0.7}Ge_{0.3}$ relaxed buffer layer with 0V on the gate.

11

In the work on strained Si, the following contributions were made:

- Demonstrated the first n- and p-MOSFET devices utilizing strained-Si channels.

- Characterized the growth of thermal oxides on strained-Si layers, illustrating that the strain in the layer is maintained, and that the growth rate and oxide quality are similar to that of oxides grown on bulk Si.

- Observed the effect of self-heating on device performance, as witnessed by a negative output conductance at high power densities. A first order heading model was used to extract the thermal resistivity of the SiGe layers, which was found to be higher than that of silicon.

- Verified for the first time experimentally the band offsets between strained-Si and relaxed-SiGe using the "split C-V" technique and one-dimensional device simulations.

- Demonstrated clear enhancement in the low-field effective mobility of strained-Si n-MOSFETs as compared to devices fabricated in CZ silicon, and observed the highest mobility in a Si MOS inversion layer at room temperature reported to date.

- Measured the strain dependence of the mobility enhancement in surface-channel strained-Si n-MOSFETs down to 10K. At room temperature, the theoretical model [5] for the bulk mobility enhancement ratio was corroborated. This strain dependence is shown in Fig. 5 below.

- Created a empirical model for the mobility enhancement ratio in surface-channel strained-Si n-MOSFETs which fits the observed mobility enhancement behavior over the entire temperature range. The model and data suggest that, as expected, the mobility enhancement is primarily due to strain splitting in the conduction band, and not to deformation of the energy valleys.
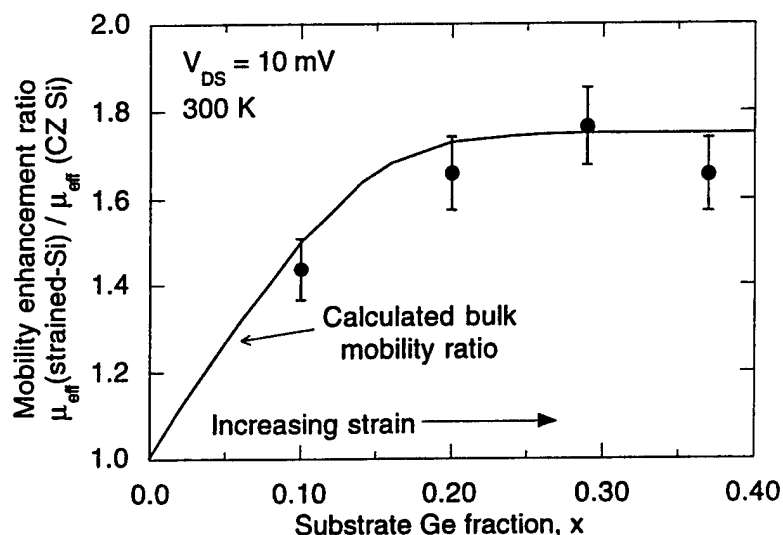
Fig. 5: Peak electron mobility enhancement ratio at room temperature as a function of the apparent Ge fraction in the relaxed SiGe buffer layer (and hence the strain in the Si channel). The measured values (bullets) compare very well to the theoretical predictions of Vogelsang and Hoffman [5].

(D) SiGeC Feasibility Study

In late 1994 the scope of work of this contract was expanded to include a feasibility study of the growth and electronic properties of SiGeC alloys. The addition of C to SiGe alloys has the potential to expand the opportunities for silicon-based bandgap engineering by offering strain compensation, the possibility of a conduction band offset, and the opportunity for obtaining layers strained in biaxial tension, which may have important electronic properties by analogy to those of strained silicon grown on relaxed SiGe. During this preliminary study, we investigated both SiGeC and SiC growth processes using two different carbon precursors (ethylene and methylsilane), and performed preliminary analysis of the bandgap shift and the band offsets. The focus of previous reports in the literature had been on materials studies, while we have emphasized the electronic properties of SiGeC. The highlights of the SiGeC work performed in this period are listed below:

- Developed a growth process for SiGeC and SiC alloys using both ethylene and methylsilane as the carbon precursors

- Demonstrated growth of lattice-matched, epitaxial SiGeC layers on Si, with Ge content of roughly 11% and C content of 1.1%

- Using a combination of high resolution XRD, SIMS, and FTIR, found that C in SiGeC is essentially fully substitutional for C concentrations

13

up to roughly 1.1% for an ethylene source and 1.5% for a methylsilane source. A number of other groups have reported higher *total* carbon concentrations (which we have obtained as well), but have failed to note that at these higher carbon concentrations, the carbon is not fully substitutional and the resulting electronic properties are significantly degraded.

- Demonstration of the first devices fabricated in the Si/SiGeC system (MOS capacitors) [6].
- Fabrication of well behaved *n*- and *p*-type Si/SiGeC MOS capacitors with C contents up to roughly 1%. For higher C concentrations, there is evidence of deep level formation and Fermi level pinning.
- Performed the first measurements of the band offsets between Si and SiGeC, and found:

   - no evidence of a conduction band offset for [C] < 1%

   - the valence band offset is reduced as C is added. Fig. 6 shows the measured characteristics of p-type Si/SiGeC MOS capacitors. With increasing C concentration in the SiGeC layers, we see that the capacitance plateau disappears and the extracted valence band offset decreases.

- Demonstration of photoluminescence in SiGeC layers (Fig. 7).
- Both PL and CV analysis indicate that the bandgap increases as C is added to SiGe. CV analysis shows that the primary effect is a lowering of the valence band energy rather than a change in the conduction band energy.

The preliminary results on SiGeC are encouraging in that we have demonstrated that with the addition of C, it is possible to grow thicker layers with higher Ge contents without misfit dislocation formation. There is also evidence that the valence band offset is slightly larger for a SiGeC alloy than for a SiGe alloy with the same lattice mismatch to Si. More work needs to be done to clarify the offsets, to study the deep level behavior of C in SiGeC alloys, to understand the difference between $Si_{1-y}C_y$ and SiGeC alloys, and to obtain higher quality films with higher *substitutional* carbon contents. These areas are the subject of some of our present work under a new contract.
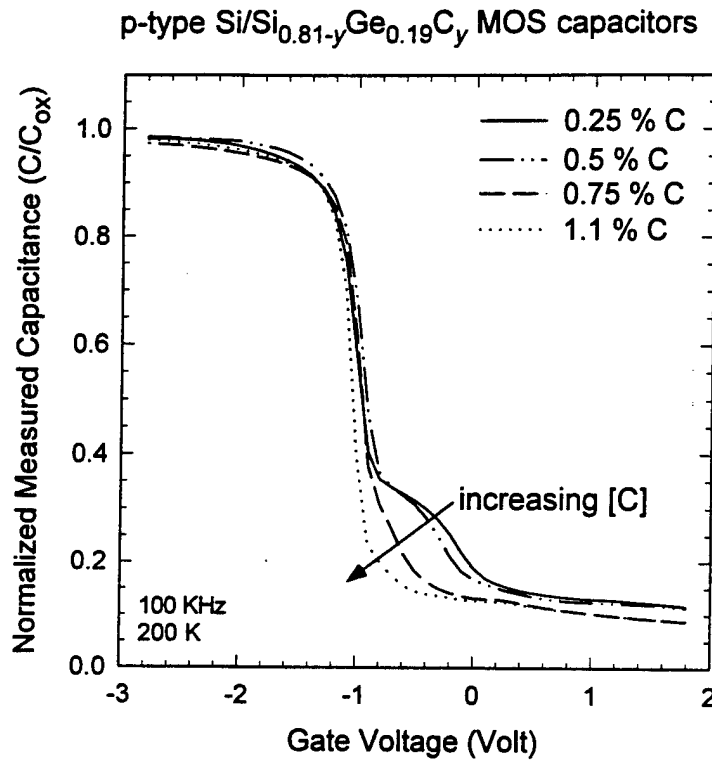
14

p-type Si/Si$_{0.81-y}$Ge$_{0.19}$C$_y$ MOS capacitors

Fig. 6: Normalized measured capacitance versus gate voltage for p-type Si/Si$_{0.81-y}$Ge$_{0.19}$C$_y$ MOS capacitors as a function of C content. As the carbon content increases, the measured capacitance plateau decreases, indicating that the valence band offset is decreasing.
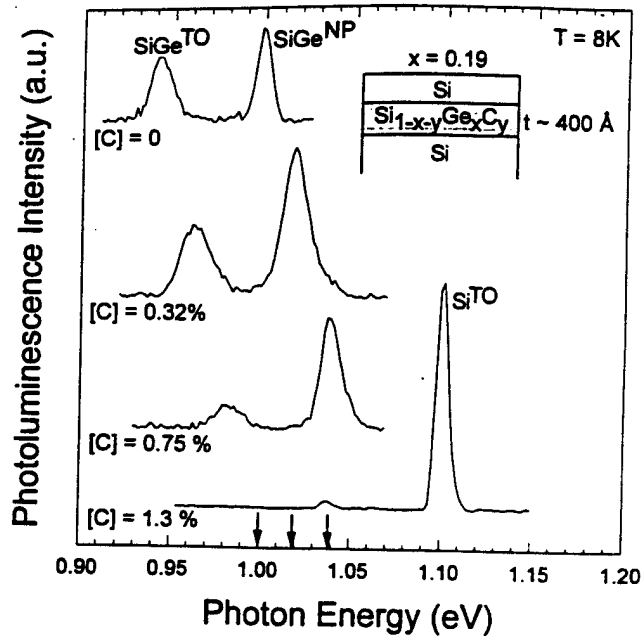

Fig. 7: Measured photoluminescence spectra for SiGeC layers indicating that the SiGeC bandgap increases as the C content increases (roughly 40 meV per atomic percent C).

15

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2. "Electrical and Structural Properites of Diodes Fabricated in Thick, Selectively Deposited $Si/Si_{1-x}Ge_x$ Epitaxial Layers," T. I. Kamis, K.Nauka, R. D. Jacowitz, J. L. Hoyt, D. B. Noble and J. F. Gibbons, *IEEE Elect. Dev Lett.* 13, pp. 177-179, April 1992.

3. "Rapid Thermal Processing-Based Epitaxy," J. L. Hoyt, *Rapid Thermal Processing Science and Technology*, Chapter 2, Richard Fair, Editor, pp. 13-43, 1993.

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5. "Comparison of boron diffusion in Si and strainded $Si_{1-x}Ge_x$ epitaxial layers," P. Kuo, J. L. Hoyt and J. F. Gibbons, J. E. Turner, R. D. Jacowitz, and T. I. Kamins, *Appl. Phys. Lett.* 62 (6), 8 Feburary 1993, p. 612.

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14. "The Application of Strained-Silicon/Relaxed Silicon-Germanium heterostructures to Metal-Oxide-Semiconductor Field-Effect Transistors", J. Welser, Ph.D. Thesis, Stanford University, December, 1994.

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LIST OF INVENTIONS

No invention disclosures were filed during this contract period.

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