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Attention: Dr. Francis J. Kub
Subject: Monthly Progress Report - January 1997
Reference: SiGe Power HBT

Gentlemen:

1.0 Introduction

The objective of this program is the development and demonstration of a viable SiGe power HBT device design and associated processes that will demonstrate >1 Watt of output power at 6 and 8 GHz.

2.0 Objectives for the Reporting Period

2.1 The new MNM capacitors will be used at PHO to further evaluate the power performance and load-pull parameters of SiGe2 and BUR50 devices at 6 GHz.

2.2 Measurements will be made at BSO to determine the MNM capacitor Q-value at frequencies to 8 GHz.

2.3 The new MNM capacitors will be used at CR&D to further evaluate the power performance and load-pull parameters of SiGe2 and BUR50 devices at 6 GHz.

2.4 Testing will resume at CR&D to compare the RF performance of the poly-emitter and poly-all processes at 1.88 GHz.

2.5 The design of the emitter ballasting resistors will be completed at BSO and the appropriate mask levels purchased.

3.0 Progress During the Reporting Period

3.1 The new MNM capacitors were used in packaged test devices at PHO to further evaluate the performance of the BUR50 devices at 6 GHz. The MNM capacitors allowed an increase in packaged device gain of about 3 dB when compared to the previously used MOS capacitors.

The packaged BUR50 devices were measured at 6 GHz with 20 mA of Class-AB bias. BVceo of these devices ranged from 5.6 to 6.2 V, and most measurements were made at 6V or less. Instabilities are evident in some of the devices tested due likely to parastic elements in the packaged device. Some of the measured test results are shown in Table 3.1.1.

Sample	Vcc (V)	P1dB (dBm)	G@P1dB (dB)	Efficiency (%)
Y2609 #1	6	23	14.8	25
Y2609 #2	6	23	13.4	20
Y2609 #3		(bad Zin)		
Y2609A #1	6	23	13.3	20
Y2609A #2	6	(no 6GHz power)		
Y2609A #3	6	(no 6GHz power, but will oscillate at 5.6GHz,>23dBm)		
Y2609A #1	7	23	17.7	17
Y2609A #1	8	23	20 (unstable at low drive)	14
Y2609A #1	9	(unstable)		

Table 3.1.1 Measured BUR50 Device Performance with MNM Capacitors at 6 GHz

The calculated thermal impedance of a single BUR50 cell is 55° C/W and with all four cells connected it is 14.3° C/W.

3.2 Two wafers of the new design capacitors were retained at BSO for RF PCM measurements to determine the capacitor Q at frequency. These measurements are performed on capacitive test structures located at PCM (Process Control Monitors) sites on the wafers.

The On-Wafer Q data is measured using an Alessi On-Wafer probe station and an HP8510 network analyzer measuring one port data. The resulting S-parameter file is converted into a conductance and admittance form from which the high frequency Q can be calculated using the following formulas at discrete frequencies.

$Y=G+jB$ (Y obtained from s-parameter measurement)

$B=2\pi fC$

$Q=B/G$

These PCM measurements resulted in the following Q vs Frequency Table:

DEVICE Rp Cs	Q1	Q2	Q3	Q4	Q5
(ohms) (pF)	(1 GHz)	(2 GHz)	(3 GHz)	(6 GHz)	(10GHz)
CP0104.DEM 23056.50 0.7875	141.32	101.36	53.51	30.68	13.57
CP0106.DEM 28457.82 0.6545	157.97	102.94	55.98	33.02	14.57
CP0108.DEM 30070.46 0.6322	127.39	108.46	58.07	32.86	14.28
CP0302.DEM 26034.58 0.7314	114.9	98.01	53.13	30.88	13.67
CP0304.DEM 28906.65 0.6345	100.98	102.15	54.82	32.08	14.42
CP0306.DEM 31708.78 0.6049	118.33	106.66	57.99	32.83	14.57
CP0308.DEM 31821.26 0.5980	165.24	105.74	55.37	31.89	14.01
CP0310.DEM 32105.12 0.6341	120.1	105.3	57.76	33.42	14.72
CP0502.DEM 27608.61 0.6974	135.03	101.63	53.13	30.74	13.53
CP0504.DEM 34891.22 0.6135	112.54	109.53	57.6	32.67	14.73
CP0506.DEM 31427.82 0.6062	122.91	110.35	55.76	32.93	14.52
CP0508.DEM 31269.38 0.6169	120.51	101.66	55.53	31.87	13.92
CP0510.DEM 28121.85 0.6638	143.03	99.6	55.3	31.59	13.84
CP0702.DEM 25406.18 0.7142	122.01	95.26	52.08	30.35	13.3
CP0704.DEM 32089.08 0.6007	107.3	106.09	55.88	31.35	13.83
CP0706.DEM 36223.86 0.5608	148.93	104.03	55.31	31.61	13.82
CP0708.DEM 32382.85 0.5731	116.31	104.08	56.35	33.1	14.75
CP0710.DEM 24788.00 0.6429	94.83	93.37	51.3	29.78	13.2
CP0904.DEM 29255.01 0.6467	118.22	95.1	51.76	29.11	12.75
CP0906.DEM 27.23 0.5272	0.09	0.19	0.28	0.57	0.9
CP0908.DEM 31225.37 0.5659	111.21	101.37	53.74	31.5	14.04

3.3 The new MNM capacitors were incorporated into new test fixture configurations at CR&D for load-pull power measurements at 6 GHz. A diagram of the new 6 GHz test fixture is shown in Figure 3.3.1. The test fixture equivalent circuit is shown in Figure 3.3.2. Tests were performed on SiGe2 devices at Vc = 5 volts and the power sweep test data can be seen in Figure 3.3.3. Initial testing indicated an output power of 25 dBm with 6 dB of gain and 15% power-added efficiency. Improvements are expected with increased practice in tuning the fixture elements. The load-pull circles for power added efficiency is shown in Figure 3.3.4 and load-pull circles for maximum output power is shown in Figure 3.3.5. Tuning of the test fixture involves a three step process for base tuning, emitter tuning, and tuning of the collector output circuit. Continued improvements in the tuning technique is expected to yield improved performance at 6 GHz and will aid in subsequently achieving 8 GHz test results. The SiGe2 devices do not have ballast resistors and as expected, attempts to operate the devices at 10 volts results in device burn-out.

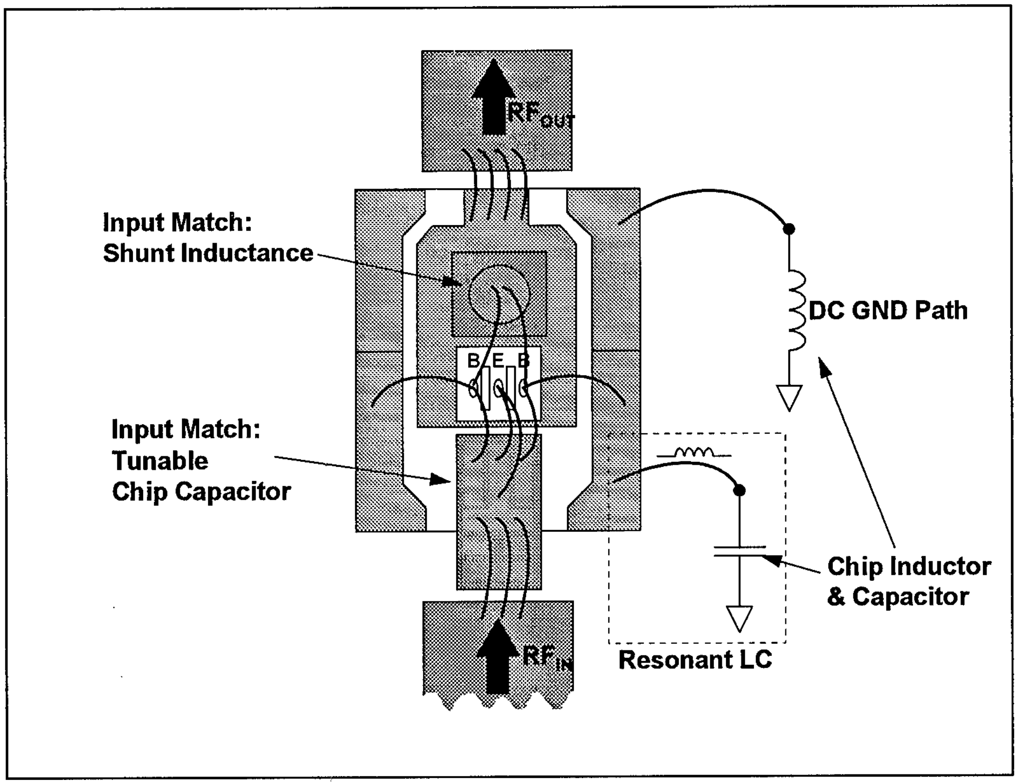

Figure 3.3.1 6 GHz Test Fixture with MNM Capacitors (CR&D)

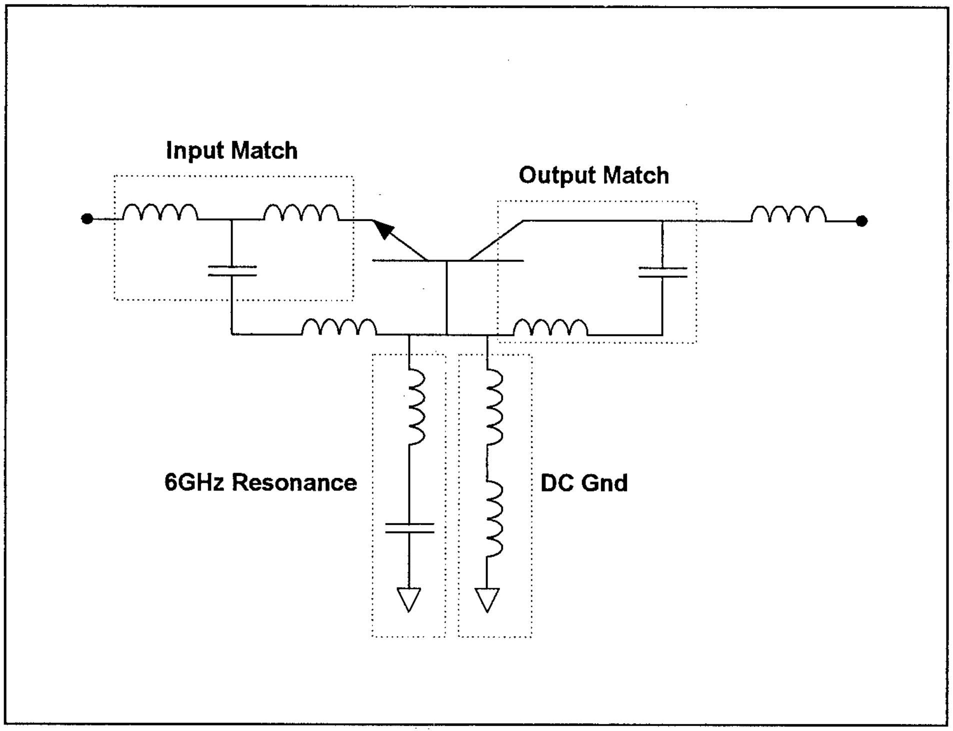

Figure 3.3.2 Equivalent Circuit of 6 GHz Test Fixture at CR&D

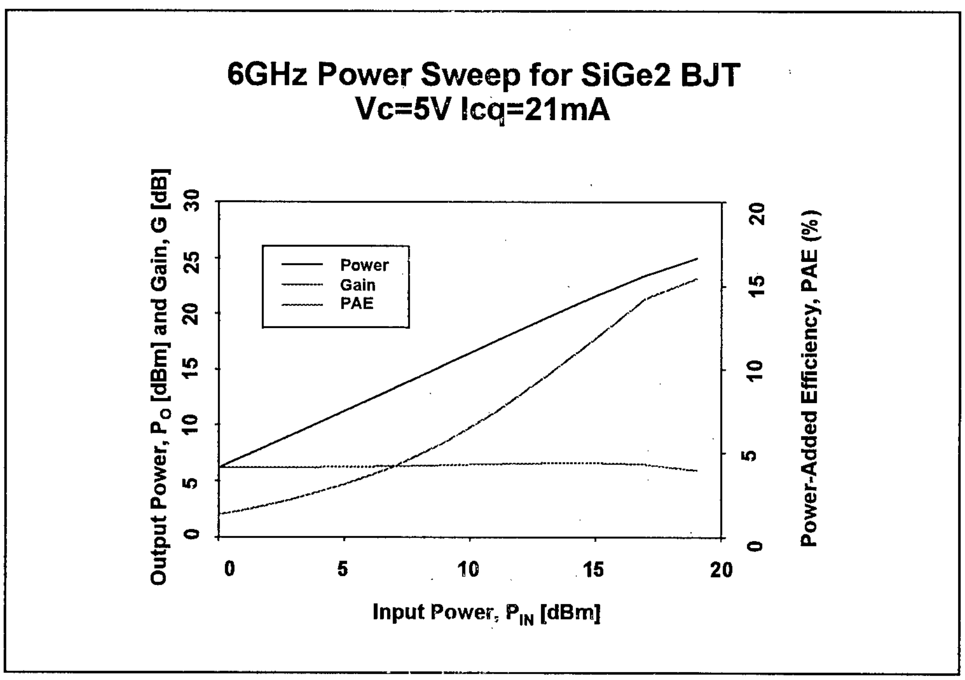

Figure 3.3.3 Power Sweep Performance of SiGe2 Device at 6 GHz

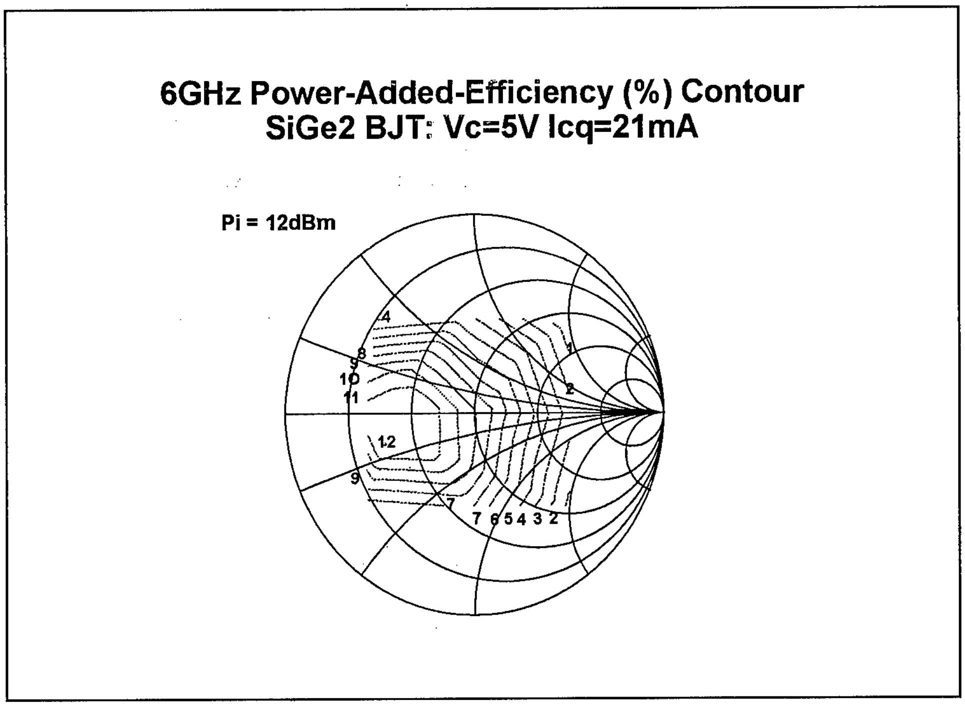

Figure 3.3.4 Measured PAE Contour Plots of SiGe2 Device at 6 GHz

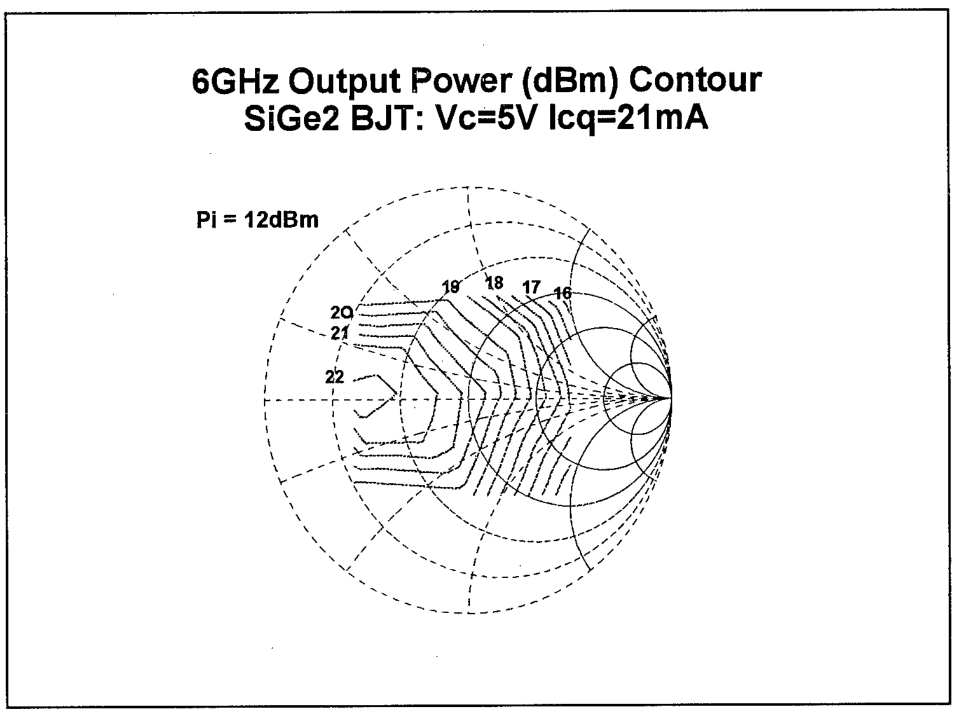

Figure 3.3.5 Measured Output Power Contours for SiGe2 Device at 6 GHz

3.4 1.88 GHz testing was performed on the polysilicon emitter SiGe2 device from lot 15. The devices showed non-uniform turn-on characteristics with early compression. At this point, it is not clear if the problems are due to the poly-emitter process. Further tests will be run on the BUR50 devices.

3.5 Design and layout to incorporate thin film NiCr ballast resistors into both the SiGe2 and BUR50 designs has been completed and the masks have been ordered. The scheduled delivery date for these masks is 2/5/97. A new run start of both the SiGe2 and BUR50 design was started utilizing the NRL collector epitaxial design anticipating receipt of these thin film metal ballast masks. These runs have progressed through Mesa etch and are awaiting LTO Deposition prior to EBC Photo.

Design and layout for the alternate approach to adding ballasting to the SiGe2 design involving initially forming the resistors out of polycrystalline silicon at very high temperatures and followed by the selective growth of the SiGe base is close to completing design and mask layout. It is anticipated that masks will be ordered by 2/11/97.

4.0 Problems and Proposed Solutions

No new issues during this period.

5.0 Objectives for the Next Reporting Period

5.1 Continued 6 GHz testing of unballasted BUR50 and SiGe2 devices at PHO using the new MNM capacitors.

5.2 Continued 6 GHz testing of unballasted SiGe2 devices at CR&D using the new MNM capacitors and begin testing of the BUR50 devices.

5.3 Begin processing run of SiGe2 and BUR50 lots using the new thin film ballasting mask sets.

5.4 Place order for polycrystalline silicon ballasting mask set for the SiGe2 device.

5.5 Perform additional testing at 1.88 GHz of the poly-emitter BUR50 devices in order to assess uniformity of DC and RF characteristics.

Respectfully,

M/A-COM Inc.

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