High Speed Circuits and Packaging Technology for Advanced Laser Altimeter Systems

Contract No. N00014-94-C-0112

Progress Report & Documentation for the 800 Ms/s Data Acquisition System

Prepared for:

Warner Miller (NASA Goddard SFC),

Alvin Goodman (ONR),

Yoon Soo Park (ONR)

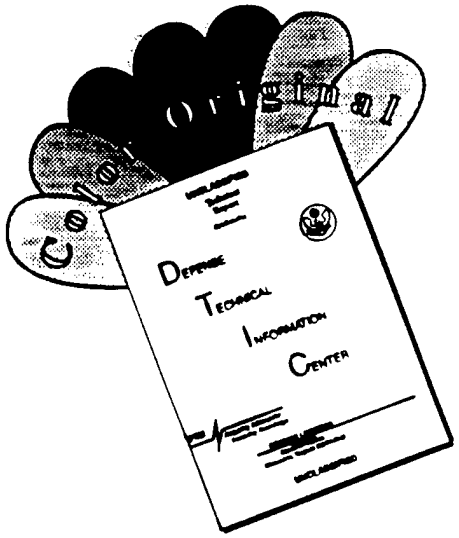
Prepared By

Charles Chang, Dharmesh Jani,

Alfred Yen, and K.C. Wang,

Rockwell International Science Center

DISCLAIMER NOTICE



THIS DOCUMENT IS BEST QUALITY AVAILABLE. THE COPY FURNISHED TO DTIC CONTAINED A SIGNIFICANT NUMBER OF COLOR PAGES WHICH DO NOT REPRODUCE LEGIBLY ON BLACK AND WHITE MICROFICHE.

High Speed Circuits and Packaging Technology for Advanced Laser Altimeter Systems Program Status Report

7/1/96 through 12/30/96

To

Warner Miller (NASA Goddard SFC)

and Alvin Goodman (ONR)

By

Charles Chang, Dharmesh Jani, Alfred Yen, and K.C. Wang,

Rockwell International Science Center

1.0 Introduction and Summary

During this period, significant progress has been made towards the demonstration of the advanced laser altimeter data acquisition unit. Our package design efforts have resulted in a fully functional GaAs chip set for the altimeter system that exceeds the requirement of the 800 Ms/s system and should be able to be used in the 3000 Ms/s system with little or no modifications. The 800 Ms/s data acquisition system design was finalized and committed to hardware. Extensive development efforts were applied to the software development needed to verify the performance of the complicated data acquisition system on the test bench. These effort have resulted in the successful demonstration of the 800 Ms/s data acquisition unit. The unit is tentatively scheduled for hand-delivery and demonstration at NASA Goddard in January, 1997. Although progress was made by Rockwell with the TELOS packaging effort and by UCSB for the design of the GaAs FIFO, this report is dedicated to the 800 Ms/s demonstration vehicle and serves as both the progress report and documentation for the unit.

2.0 ADC, DEMUX, and TIU IC Fabrication and Testing

For the 800 Ms/s demonstration, ADCs from 40029 were tested on-wafer and diced. Extensive on-wafer characterization of the ADC, DEMUX, and TIU was carried out on lot 40047. From the many wafers tested, ADCs, DEMUXs, and TIUs were diced out from wafer 40047-1-11 and TIUs from 40047-1-1. On-wafer characterization primarily focused on functionality and speed. The test results are documented in previous progress reports. The on-wafer performance of the DEMUX and TIU significantly exceed the requirements of the 3000 Ms/s system. Due to equipment limitations, the ADC has been tested up to a maximum sampling rate of 2000 Ms/s.

Originally, the ADC package was designed to accommodate ADCs that were diced with a dicing saw. However, since higher chip yields were seen with the scribe-and-break dicing technique the dicing saw was replaced as the standard dicing technique at Rockwell. This resulted in a slightly larger chip that did not fit the package cavity (too large by one mil in the short direction). The cavity size of the packaged was designed to minimize the length of the performance robbing bond-wire. As a result, the scribe-and-break chips were sent to a saw dicing firm to trim the ADC chips to fit the package. This approach was successful, however, the yield was low.

Under a separate APRA program, the ADCs have been modified for higher bandwidth and linearity. An improved DEMUX with the reset feature has also been designed. Both the new ADC and DEMUX have been fabricated, tested, and shown to be functional with improved performance. We propose to further improve the ADC for use in the 3000 Ms/s data acquisition system demonstration. Several versions of the TIU with improved output buffers and interface logic type have been fabricated or are in fabrication and await testing.

2.1 ADC, DEMUX, ADC Packaging Design

2.1.0 ADC Package Effort

A full custom ADC packaged was designed by Rockwell and fabricated by Stratedge and is shown in figure 2.1-1. This packaged was tested up to 2000

Ms/s which was the limitation of the test setup. We expect this package to work past 3000 Ms/s so the same package can be used for both the 800 and 3000 Ms/s demonstration. The package was designed to accommodate both the current and new versions of the ADC. The details of this package can be found in previous reports.

2.1.1 DEMUX Package Effort

For the DEMUX package, the packaging approach consists of a large commercial 196 pin package in conjunction with a custom designed interconnect substrate. The Rockwell designed interconnect substrate allows for controlled impedance lines connecting the small IC to the large chip cavity of the package. A figure of this packaging approach is shown in fig. 2.1-2 and a close up of the substrate is shown in figure 2.1-3. On-wafer tests have shown that the output of this chip is very sensitive to inductance which can cause ringing and oscillations if all of the outputs are switching at once. As a result, the controlled impedance substrate was carefully designed with high-speed coupled microstrip lines to minimize inductance. Furthermore, design attention was also placed at minimizing the inductance in both power and ground lines as well as extensive use of by-pass capacitors for clean DC power. The substrate design does challenge the lithography limits used by most substrate vendors and fig. 2.1-4 shows the fine lines of the substrate as well as the numerous bondwires. The packaged chip was tested with a test fixture sold by the package manufacture. As figure 2.1-5 shows, the output does not excessively ring or oscillate as all of the outputs are changing with a 3 GHz input clock. Speed tests show that this part is functional up to 3.2 GHz. Both the package and the substrate were designed to accommodate both the current non-resetable and the future resetable DEMUX versions. This packaging approach satisfies the performance requirements of both the 800 and 3000 Ms/s demonstration vehicle.

2.1.2 TIU Package Effort

Due to the small size of the TIU and low number of I/O's, a commercial package was used. The initial TIU package pin-out and wire bonding configuration was modified to work with the non-optimized output stage of the TIU as shown in fig. 2.1-6. The changes result in using the package floor as a ground plane and all chip ground connects are made from that plane. This prevents potentially destructive ground loops that may damage the chip as was seen with the previous approach. This package was tested in a custom designed test fixture to well over 5 GHz. The functionality of the TIU is shown in fig. 2.1-7 showing the launch pulse leave, launch pulse return, launch pulse gating signal, memory write enable, and 9 of the 27 bits in the coarse counter. The figure shows that the TIU functions as designed. The coarse counter properly starts and stops with the control signal. Furthermore, proper operation of the memory enable signal is shown which is used to start and sync. the ADC operation with the coarse counter for high accuracy.

2.1.3 Packages for the 800 Ms/s System Demonstration

In each case, several TIUs, DEMUXs, and ADC were packaged and tested for use in the 800 Ms/s system deliverable. Of the 6 packaged and tested TIUs in the new configuration, 4 were lost in the development of the 800 Ms/s system. Of the first 3 packaged DEMUXs, two were fully functional. Of the two fully functional parts, one was lost in the system development phase. Three more additional DEMUXs were packaged but not tested. For the ADC, 6 ADC were packaged. After testing, only two were of similar high-performance in terms of the number of effective bits. Four more ADC were packaged as a backup but have not yet been tested.

2.1.4 Packages for the 3000 Ms/s System Demonstration

As a cost saving measure, the packages used for the 800 Ms/s system was designed for use in the 3000 Ms/s system. We believe that this goal has been meet and the TIU and DEMUX packaging approach has been shown to

work above 3000 Ms/s and the ADC design is expected to work at 3000 Ms/s. For improved yield, the ADC package may be modified with a larger cavity to incorporate the scribe and break ADC chips; however, the cost is quite minimal since much of the package benefits from the original NRE.

2.2 800 Ms/s Data Acquisition System integration: Hardware

2.2.0 Overview

The 800 Ms/s data acquisition system (DAS800) was integrated into a large EIA rack mount case as shown in fig. 2.2-1 to ease development and testing. During the prototype phase, the DAS800 was interfaced to a 80486 PC through a National Instruments AT-DIO-32F data acquisition card. The controlling software was written in VISUAL Basic Pro. The PC is responsible for initializing the DAS800, resetting the DAS800, acquiring the 64 K samples from the FIFOs, displaying the data, and optionally, signal processing/filtering. For NASA's intended use, the PC can be omitted and the microprocessor based hardware can be directly interfaced to the FIFOs for a maximum data read rate. A system level schematic of the DAS800 is shown in fig. 2.2-2 while the corresponding sections in the DAS800 chassis are pointed out in fig 2.2-3. The primary sections of the DAS800 is the data acquisition PCB, the power supply regulator PCB, and the ISA interface PCB.

2.2.1 Power Supply Distribution

Fig. 2.2-4 shows a schematic of the power supply and distribution. This unit uses two 50W 12V isolated switching power supplies and one 15W 5V isolated switching power supply to generate the primary +12 V, -12 V, and +5 V. The +12V & -12V primary supplies are used to feed the power supply regulator PCB which can individually switch (controlled by the PC) the various voltages required by each IC for minimal power dissipation. For demonstration purposes, linear regulators are used instead of the more efficient custom DC-DC converters to provide the require chip level voltages (ig. +5 V, -5.2 V, -2 V, 0 V); however, the linear regulators do dissipate a significant amount of power as heat. For

example, if the IC draws -5.2V @ 1A (5.2W), the regulator will dissipate 6.8 W as heat. Although two fans are used in the design, only one is necessary for cooling. The two fans were used if it became necessary to employ a bisecting shield to separate the power supply and power supply regulator PCB from the ISA interface PCB and data acquisition PCB.

2.2.2 Data Acquisition PCB

The heart of the DAS800 is the data acquisition PCB which contains the high-speed ADC, TIU, DEMUX, and FIFO memories. Fig. 2.2-5 through 2.2-9 show the final schematic of the main data acquisition PCB. The schematics are broken into the overall board, ADC details, DEMUX details, TIU details, and FIFO details. Fig. 2.2-10 shows a photo of the main data acquisition board. This board is a five layer board and the top layer is RO3006 (10 mils thick) DURIOD. The high-speed DURIOD layer is use to house the high-speed transmission lines for the analog input and high-speed digital signals of the ADC, TIU, and DEMUX. The ADC package fits into a slot cut into the PCB. This mounting approach was used 1) to minimize the microstrip transmission line discontinuity between the PCB and IC, 2) provide access for the machined aluminum heatsink that connects to the CuW heatspreader under the IC, 3) to avoid purchasing an expensive custom designed lead bender or the ADC package. This approach does however complicate the board layout since routing area is lost. In anticipation of the 3000 Ms/s design, the transmission lines connecting the ADC to the DEMUX are matched to 1/10 inch to minimize the phase delays between the different signals. Since the DEMUX package was designed to complement the ADC package, a cutout in the PCB is also need for the DEMUX package heat spreader to minimize the high-speed line crossovers. Both the ADC and DEMUX heatsinks are attached on the back of the PCB. High-speed SMA connectors are provided for I/O. Through SMA coaxial cable jumpers, the ECL/CML level converters for the LPR and LPL can be configured as needed.

Although the PCB passed LVS (layout vs. schematic), due to software errors in the routing program, several key signals were shorted out and key

traces were missing during fabrication. Furthermore, a schematic error on the DEMUX and a footprint error on the ECL 2:1 MUX also contribute to the overall error. As a result, this board took a considerable time to debug; however, it was possible to make this board fully functional. Future board will be hand checked before release to the fabrication house.

The pseudo random generator does not work for this design. For it to work, the DEMUX inputs can not be load and as designed, it is loaded with the output of the ADC. Since the DEMUX input clock is derived from the ADC, this condition can not be meet even if the ADC was powered down. For our purposes, the gray-to-binary conversion was shifted to software for better performance. Tests have shown that the TIU can function up to 5 GHz with this PCB approach; thus, the DUROID/Glass Epoxy PCB approach should be able to be employed for the high-speed 3000 Ms/s system demonstration.

A summary timing diagram of the DAS800 is illustrated in figure 2.2-11. The DAS800 was initially designed to accommodate four possible timing scenarios in order to take into account the variation of the max. & min. setup and hold times of the slower ECL conversion chips (as documented in the previous report). The system was designed for case one and the final design used case one.

2.2.3 Power Supply Regulator PCB

Regulated and switched power to the individual chips on the Data Acquisition PCB is provided through the Power Supply Regulator PCB. A photograph of the power-supply board is shown in figure 2.2-12 and its schematic shown in fig. 2.2-13 and 2.2-14 This board is a 4 layer board with a separate ground and power plane for low inductance returns. A PCB software error shorting the ground plane to several key components was corrected quite easily. A logic error forces the change of some NPN transistors to PNP in order for the power shutdown to work correctly when more that one regulator is tied to a single control input. As configured, the software through the ISA interface PCB controls the different voltage regulators for minimum power dissipation. Although

software control of the power is demonstrated, the power dissipation is not optimized in the test software. Due to the need to convert 12 V to the numerous required lower voltages, this power supply dissipates quite a bit of power as heat since linear regulators are used.

2.2.4 ISA Interface PCB

The ISA Interface PCB provides the necessary bridge between the National Instruments ISA bus card in the PC and the Data Acquisition PCB and Power Supply Regulator PCB in the DAS800. The schematic of the board is shown in figure 2.2-15 and 2.2-16. A photo of the board is shown in figure 2.2-17. This board was designed with standard TTL parts and is used to control the different setting of the data acquisition board as well as to interface to the FIFOs. This board is a standard 3 layer board and was designed to operate at the maximum rate of 330 KW/s. However, due to either our slower 66 MHz 80486 PC or National Instruments interface limits, the actual achievable read rate is much slower. For NASA's altimeter prototype, the microprocessor based hardware should directly interface to the FIFO for a maximum read rate of 100 MWord/sec. There are no known problems with this board.

2.3 800 Ms/s data acquisition system integration: PC to DAS800 Interface

Testing and development of the DAS800 is complicated by the numerous tasks and functions of the hardware. The required information is the vast quantity of sampled data (64Kb), TIU coarse count, FIFO initialization, and general hardware control. To accomplish this efficiently, control of the DAS800 is delegated to a PC where the development of high-level user-friendly software is straight forward. As a result, a general purpose I/O board from National Instruments was used as the go-between from the PC to the DAS800. The following section documents the software/hardware interface between the PC and the DAS800.

2.3.0 National Instruments AT-DIO-32F Hardware Setup and Description

The AT-DIO-32F was designed as a multipurpose ISA interface card by National Instruments. As a result, the operation of the card is quite complex and the following information is required to configure and understand the operation of the AT-DIO board. Table 2.3-1 maps the AT-DIO pin assignments to the names on the ISA PCB schematic. Tables 2.3-2a and 2.3-2b detail and discuss the hardware configuration used to read and write data to the ISA Interface PCB. For further information, please consult both the printed and on-line manuals provided by National Instruments.

Table 2.3-1: AT-DIO to ISA Interface Board Hardware Assignment

Schematic Name	ATDIO Name	Function
PCA0-PCA7	A0-A7	Data Write Address Bus (WA)
PCB0-PCB7	B0-B7	Data Write Data Bus (WD)
PCC0-PCC15	C0-C7, D0-D7	Data Read Bus (RD)
WREQ1	REQ1	Handshaking Write Request
RREQ2	REQ2	Handshaking Read Request
DLATCH	ACK1	Write Data Latch
RACK1	ACK2	Read Acknowledge
OUT1	OUT1	WREQ1 Generation
OUT2	OUT2	WREQ1 Generation

Table 2.3-2a: AT-DIO Data Read Hardware Setup

Read FIFO Data: (Mode 1: With handshaking)
a) RREQ2 and RACK2 in leading Edge Mode, Positive Logic
b) TDelay=0, LPULSE=1, Single Buffered Data Input
c) 16 bit word Read (RD)
Read TIU Data: (Mode 0: No Handshaking)
a) 16 bit port word Read

Table 2.3-2b: AT-DIO Data Write Hardware Setup

Method 2: Out1 & Out2 generate WREQ1, ACK1 generates DLATCH to latch data
a) 16 bit write (WA+WD)
b) REQ and ACK in leading Edge Mode, Positive Logic, LPULSE=0
c) Single Buffered Output Mode

2.3.1 NASA ISA Interface Board Setup and Description

The NASA ISA interface PCB was designed to control both the data acquisition PCB and the power supply regulation PCB. To simplify programming,

data is written to the ISA interface PCB and stored in its hardware latches. The address of the latch is determined by the Write Address Bus (WA) and the content of the data is determined by the Write Data Bus (WD). Both WA and WD are present at the same time. On board hardware decodes the address bus so the contents of the WD is written to the proper storage location. The following details the functions of the different latches.

ISA Register Write Address & Data Allocation:

WA: WD: Function

00h: x Deselect all latches

01h: Power Control #1 Latch (PCtrl1)

Bit	Function	High	Low
0	FIFO Memory Cells	On	Off
1	FIFO ECL-CML Converters	On	Off
2	TIU Chip	On	Off
3	DEMUX Core	On	Off
4	DEMUX Output Drivers	On	Off
5	ADC Core	On	Off
6	ADC Output Drivers	On	Off
7	VGA	On	Off

02h: Power Control #2 Latch (PCtrl2)

Bit	Function	High	Low
0	EXT1: Aux. 1 Power Ctrl	On	Off
1	EXT1: Aux. 2 Power Ctrl	On	Off
2	EXT1: Aux. 3 Power Ctrl	On	Off
3	VGA Gain ctrl LSB	H	L
4	VGA Gain ctrl	H	L
5	VGA Gain ctrl	H	L
6	VGA Gain ctrl MSB	H	L
7	Demux PNgen Reset	Rst	Run

04h: FIFO Control Latch (FIFOCtr)

Bit	Function	High	Low
0	PEN' (Parity Byte Latch En.)	Z	OE0
1	FEN' (Flag Latch En.)	Z	OE0
2	SEN' (Sequence Enable)	Stop	Run
3	CEN' (Clock Enable)	Dis	Ena
4	REN' (FIFO Read Enable)	Dis	Rd
5	FS1 (Clock Freq. Sel.) LSB	H	L
6	FS2 (Clock Freq. Sel.)	H	L
7	FS3 (Clock Freq. Sel.) MSB	H	L

08h: TIU Control Latch (TIUCtr)

Bit	Function	High	Low
0	MRS' (FIFO Master Reset)	Nor	Rst
1	PRS' (FIFO Standard Reset)	Nor	Rst
2	TRS' (TIU Reset)	Nor	Rst
3	TIUS0 (Byte Sel) LSB	H	L
4	TIUS1 (Byte Sel) LSB	H	L
5	GateT: accept/block LPR	Acp	Blk
6	TCLKP (FIFO Clock Polarity)	0	180
7	DOVRS (Demux OF Reset)	Nor	Rst

10h: LED Status Latch (LEDCtr)

Bit	Function	High	Low
0	Acquire Pulse	On	Off
1	Standby	On	Off
2	Data Read	On	Off
3	FIFO Read	On	Off
4	TIU Read	On	Off
5	Reset System	On	Off
6	Initialize System	On	Off
7	DAS800 On-line	On	Off

20h: x Expansion #1 (Expan1)
40h: x Expansion #2 (Expan2)
80h: x Expansion #3 (Expan3)

2.3.2 DAS800 Control and Operation Procedure

The following summarizes the control sequence our software uses to control the hardware. For proper operation, there are several key operations which are power up initialization, master reset, partial reset, reading the TIU, and reading the FIFOs.

"Power up initialization" involves latching the correct setting to the power supply regulator board to turn on the chips, resetting the TIU and FIFO, resetting the FIFO read counter, and placing all of the Read bus users in the high Z state.

"Master reset" and "partial reset" are use to reset the data acquisition board for a new measurement. Both reset the TIU and place the TIU in the high Z state. The "master reset" is used with the "power up initialization" phase to set the FIFO into the proper mode. Afterwards, all subsequent measurements uses

the "partial reset" option in the FIFO to clear its contents without changing the FIFO mode of operation.

"Reading the TIU" involves transferring the coarse count in the TIU to the PC. The 27 bit TIU data is read in three nine bit words. A two bit address bus is used to select the proper word or the high Z state.

"Reading the FIFO" is quite complicated since in invokes the counter chips which generate the proper sequences to clock the FIFOs, read the 16 bit data and two bit parity from each of the four FIFO chips in the most efficient manner. The read sequence is detailed in table 2.3-3. Table 2.3-4 show the different read rates selectable with the 5 MHz crystal. At present, it is believed that a 80486 running at 66 MHz is not capable of reading the data anywhere near the maximum rate of 330 KWord/Sec running in the DMA mode. The overhead involved in running Windows 3.1.1, NIDAQ drivers, and Visual Basic prevents the maximum rate from being achieved.

The different latch settings to control the hardware is summarized in table 2.3-5.

Table 2.3-3: FIFO Read Sequence

1) Clock (f) generated by a TTL based Crystal Oscillator (U34)
   a) Freq. selection changed with different oscillators
2) f/2 and f/4 generated with JK FF 'LS73 (U20)
3) f/8, f/16, f/32, f/64, and f/32 generated with 4 bit counter 'LS163 (U24)
4) Clock Frequency Selection with 8:1 mux 'LS151 (U23)
   a) FS1, FS2, FS3, CEN' latched with FIFOCtr Latch
   b) CEN'=L send clock to read, CEN'=H stop clock when not reading
   c) FS1, FS2, FS3 = 000 for f, 111 for f/128
   d) Testpoint 1 (TP1) is selected clock
5) FIFO read sequence: 4 bit counter 'LS163 (U32) and 3:8 Demux 'LS138 (U32)
   a) Counter Clear
      1) Clear generated by SEN' nor Output decode (U18B)
      2) SEN'=H, counter and D-FF is cleared and paused
      3) SEN'=L, FIFO read sequence begins (REN'=L before SEN'=L)
      4) Output decode count 1001 (U21A) clear counter (TP3)
   b) QA output generates clock (TP2)
   c) QB-QD output is demux to select FIFO chips & parity
5a) FIFO read sequence
   1) Counter Count: 0000 QA=L OE0=L
      a) OE0 enables transparent data latch 'LS373 (U26, U22) in trans. mode

1) Latched parity bits (P0-P7) on data bus (PCC0-7)
2) FIFO Flag Status (EF', HF', FF', DOVR) on (PCC8-PCC11)

2) Counter Count: 0001 QA=H OE0=L
   a) OE0=L or (U13D) QA generate rising edge of RCLK to clock FIFO
   b) Generates rising edge of RReq2 for AT-DIO read (Hold for 225 ns)
   c) Maximum read rate 2.2 MHz
   d) Parity and FIFO flag data read into AT-DIO
3) Counter Count: 0010 QA=L OE1=L
   a) OE1 selects FIFO #1, Valid FIFO data: 7ns after OE1
   b) OE1 prepares FF to latch parity (U11A, U11B)
4) Counter Count: 0011 QA=H OE1=L
   a) With SEN'=L, QA L to H generates rising pulse to latch D-FF (U14)
   b) D-FF data is not visible on bus since OE0=H so t-latch is in high Z
   c) QA L to H generates another read cycle for the AT-DIO
   d) FIFO #1 DA0-7, DA9-16 is placed on PCC0-15
5) Counter Count: 0100 QA=L OE2=L
   a) OE2 selects FIFO #2, Valid FIFO data: 7ns after OE2
   b) OE2 prepares FF to latch parity (U11A, U11B)
6) Counter Count: 0101 QA=H OE2=L
   a) With SEN'=L, QA L to H generates rising pulse to latch D-FF (U15)
   b) QA L to H generates another read cycle for the AT-DIO
   c) FIFO #2 DA0-7, DA9-16 is placed on PCC0-15
7) Counter Count: 0110 QA=L OE3=L
   a) OE3 selects FIFO #3, Valid FIFO data: 7ns after OE3
   b) OE3 prepares FF to latch parity (U12A, U12B)
8) Counter Count: 0111 QA=H OE3=L
   a) With SEN'=L, QA L to H generates rising pulse to latch D-FF (U16)
   b) QA L to H generates another read cycle for the AT-DIO
   c) FIFO #3 DA0-7, DA9-16 is placed on PCC0-15
9) Counter Count: 1000 QA=L OE4=L
   a) OE3 selects FIFO #3, Valid FIFO data: 7ns after OE3
   b) OE3 prepares FF to latch parity (U12A, U12B)
10) Counter Count: 1001 QA=H OE4=L
   a) With SEN'=L, QA L to H generates rising pulse to latch D-FF (U17)
   b) QA L to H generates another read cycle for the AT-DIO
   c) FIFO #4 DA0-7, DA9-16 is placed on PCC0-15
   d) Decode 1001 sets clear=L so next clock cycle, Counter-0000
12) Cycle repeats to step 0 and ends after n-reads or when FIFO is empty by checking the FIFO flags during to count 0001
11) When cycle starts, first read is parity bits which should be all zeros.

Table 2.3-4:Read FIFO Clock Frequency

FS1	FS2	FS3	f RCLK	f=4 MHz	f=5 MHz	f=18.432
0	0	0	f/2	2.000	2.500	9.216
1	0	0	f/4	1.000	1.250	4.608
0	1	0	f/8	0.500	0.625	2.304
1	1	0	f/16	0.250	0.313	1.152
0	0	1	f/32	0.125	0.156	0.576
1	0	1	f/64	0.062	0.078	0.288
0	1	1	f/128	0.031	0.039	0.144

CEN'=L to enable the clock

Table 2.3-5: Latch sequence for proper operation

Function	MRS'	PRS'	TRS'	TIUSO	TIUS1	PEN'	FEN'	SEN'	CEN'	REN'	FS1	FS2	FS3	Gate	TClkP	DOvers
Master Reset	0	1	0	1	1	1	1	1	0	1	X	X	X	0	0	1
Partial Reset	1	0	0	1	1	1	1	1	0	1	X	X	X	0	0	1
Power Up	1	1	0	1	1	1	1	1	1	1	X	X	X	0	0	1
TIU Reset	1	1	0	1	1						X	X	X	0	0	1
TIU set	1	1	1	1	1						X	X	X	0	0	1
FIFO Read						1	1	0	0	0	X	X	X	0	0	1
FIFO status						1	X	1	0	1	X	X	X	0	0	1
TIU read	1	1	1	X	X						X	X	X	0	0	1
Parity Read						X	X	1	0	X	X	X	X	0	0	1

X denotes software selection

2.4 Rockwell DAS800 Verification and Test Software

2.4.0 Introduction

In order to develop and test a complicated system like the DAS800, custom software is developed to control the instrument as well as to handle the large volume (64 Kb + parity) of data read from the FIFO. This software was implement with Microsoft Visual Basic Professional. Interface with the National Instruments AT-DIO ISA card is accomplished with Visual Basic drivers provided by National Instruments. Both the control software and the AT-DIO interface card operated from a 66 MHz 80486 based PC running Windows 3.1.1. To complicate matters, both the software and the DAS800 hardware were developed and debugged at the same time. The Windows 3.1.1 based software is titled "DAS800.exe" and is run from Windows by clicking the Icon which should in turn display the Main Control Panel.

2.4.2 Main Control Panel

The Rockwell DAS800 Verification and Test Software (SOFTWARE) was designed at the onset to be easily used. Although the software was designed for Rockwell to develop and test the unit, the SOFTWARE can be used by NASA to verify several key functions of the DAS800 Hardware. The Windows based main control panel is shown in figure 2.3-1. The program is divided into a display section on top and several control groups on the bottom.

The measurement group contains three buttons and two display boxes. The "AUTO" button starts, configures, resets, and completes one measurement cycle of the DAS800. The measurement cycle consists of data acquisition of the TIU coarse count and FIFO contents, FIFO data sorting, gray-to-binary conversion, plotting the raw data, and filter and smoothing the data for display. The "Gray-to-Binary" button selects the data pass through mode (off) or the software gray-to-binary conversion of the data (on). The default is software Gray-to-Binary conversion. Hardware Gray-to-Binary conversion can be selected with a jumper on the data acquisition PCB. After completion of the measurement, the TIU binary coarse count is displayed in the TIU length box. Based on the input clock frequency, the corresponding Time-Of-Flight is displayed in the TIU Time box. The "M" button selects some of the development features that will be discussed latter.

The input clock frequency is determined in the Sampling Frequency group. The frequency unit and frequency can be selected with the mouse. Alternatively, the frequency can be directly typed into the box when selected. This frequency is used to determine the TIU time as well as the time scale of the acquired waveform displayed at the top.

The Display group manages the display of the acquired waveform. The "C" Button clears the display. The "Raw Data" button displays the as measured data. The "Filtered Data" button displays the filtered and smoothed version of the measured data. The Start and Stop position of the graph is determined by

keyboard or mouse at the bottom of the group. Due to the limited computing power of our PC as well as the large data set, this display is quite slow.

During our development, several problems were encountered with reading the FIFOs using the PC. It is believe that the problem lies in the handshaking routine between the AT-DIO-32 and the ISA Interface PCB where the ISA Interface initializes a read that may be missed by the AT-DIO-32. At present, we believe this may be due to the fact that our PC is slow and may be running some overhead software. As a result of a misplace or skipped read, the data sequence (FIFO 1, FIFO 2, FIFO 3, FIFO 4, parity) is corrupt and the parity data is mistaken for valid FIFO data resulting in a huge jump in the read data. A coarse and fine filter algorithm is used to correct this type of error. The data is organized into an array that consists of the low and high byte (DL_i, DH_i). The coarse filter first uses knowledge of the empty and full flags in the high byte to determine that that the low byte is parity. Afterwards, full scale and zero scale data is filtered out (typically associated with parity errors). Then the fine filter is applied by assuming that DL_i is a valid point, the software first compares the absolute difference between the high and low byte of the next data ($|DL_{i+1} - DH_{i+1}|$) to a threshold value, C. C is a user entered number in the Filter group (default is 8). If it is smaller than C, then the points should be valid, if not, there is a possible error and both DL_{i+1} and DH_{i+1} are set to DL_i. Afterwards, the High byte (DH_i) of the previous sample is compared to the Low byte of the next sample (DL_{i+1}). If the absolute difference is greater than C, a possible error has occurred so both DL_{i+1} and DL_{i+1} is set to DL_i. This algorithm proved to be quite useful for removing the parity bit from the main data stream. Afterwards, a smoothing function is applied to the data to clean up the high-frequency noise. The filter is based on the following function:

$$D(i) = \frac{\sum_{i-N/2}^{i+N/2} \left(\frac{1}{0.37\sqrt{2\pi}} \exp\left(\frac{-\left(\frac{i-j}{b}\right)^2}{2(0.37)^2} \right) \right) D(i)}{\sum_{i-N/2}^{i+N/2} \left(\frac{1}{0.37\sqrt{2\pi}} \exp\left(\frac{-\left(\frac{i-j}{b}\right)^2}{2(0.37)^2} \right) \right)}$$

N is the window depth (default=8). A larger N will increase the runtime of the smoothing function. B is a filter parameter whose default value is 4.

Lastly, the System Group is used to control the DAS800 system. The "On" Button configures the power supply regulator PCB and brings the ISA Interface PCB on-line. The "SAVE" button saves the displayed data to a text file for off-line processing. The "Exit" Button exits the SOFTWARE.

For proper operation, upon running the SOFTWARE, click "ON" to initialize the system. Change any of the options (filter, sampling frequency, gray-to-binary, etc.) if needed. Click "Auto" to make the measurement. Click "C" to clear the display. Click either or both "Raw Data" or "Filtered Data" to display the waveform. Use the Start and End position to zoom in on the region of interest.

2.4.3 Advanced Control Panel

Upon clicking the "M" button from the main control panel, the advanced control panel is added to the bottom of the main panel as shown in fig. 2.4-2. In this mode, the individual functions required to operate of the DAS800 can be individually accessed with the Measurement Group of buttons in the Manual Override. Furthermore, the display can display the High and/or Low byte of each FIFO individually as well as the parity and FIFO status flags with the Display Group in the Manual Override. The unit also displays the TIU count as three nine bit words which from the 27 bit coarse count. The FIFO flag status and parity bit is shown in the FIFO Info group. For further register level tests, the "Interface Test switch can be pressed.

2.4.4 Interface Test Panel

With the "Interface Test" button in the Advanced Control Panel, the screen shown in figure 2.4-3 is displayed. Here the individual ISA Interface PCB registers can be accessed. The "Initialize" Button sets the DAS800 to the default state. To change any of the registers, click on the desired signals and a X will appear to show that the selected function is active. Upon clicking the "SET" button in the desired registers, the contents of the register is updated. For the TIU and FIFO, it is also possible to read the current contents of the Data Read Bus corresponding to the TIU or FIFO. The "Frequency Select" group allows one to select the AT-DIO read rate. The "DAS800" button returns to the Main Control Panel" and "Exit" terminates the program.

2.5 800 Ms/s Data Acquisition System: Test Results

2.5.1 Test Setup

On the test bench, the DAS800 data acquisition system data acquisition cycle is triggered by sending in a voltage pulse similar to the laser launch pulse. This starts the TIU's coarse counter. On receiving another voltage pulse corresponding to the laser return, the timing interface unit stops and sends the acknowledge signal to ADC, DEMUX and FIFO memory. This starts the digitizing phase which samples the returned laser pulse. The returned laser pulse is simulated by feeding an analog waveform into the DAS800. Up to 65536 8-bit samples and the 27 bit coarse count is subsequently displayed on the PC through the DAS800 Test and Verification software.

Figure 2.5-1 shows the schematic of the test setup used. An HP data generator (HP8180A) is used to generate the laser launch and the laser return signals. Signal levels are adjusted to the expected ECL signal levels from the laser detector. The Data Acquisition PCB is configured to use the on-chip ECL-to-CML level converters. The gating signal is also generated from HP8180A and adjusted to overlap the return laser pulse. Synthesized signal generator (HP8665B) is used for providing the system clock. Clock levels are adjusted to

1Vpp at 800MHz. A power splitter is used to generate a differential clock from a single ended source. Due to the differential nature of the ADC clock, the DC offset level of the clock is adjusted to 0V. The analog input is fully differential and is generated from a two channel synthesizer (HP3326A) which has a maximum frequency of 20 MHz. The modulated input waveforms are generated by feeding one of the HP8180A data channels into external AM or PM ports of HP3326A. A Tektronix oscilloscope (TEK7104) is used to observe the waveforms sent into the acquisition system. This feature allows one to verify that the captured waveform displayed on the PC is the same as the input waveform displayed on the oscilloscope. All the signals fed to the data acquisition box are fully differential. Figure 2.5-2 illustrates the photograph of the test setup while figure 2.5-3 shows the DAS800 under test.

2.5.2 Data Acquisition PCB Configuration

The Data Acquisition PCB has a myriad of adjustable resistors and jumpers to adjust and select the many different features. As part of the development procedure, proper jumper setting and potentiometer adjustment were made to obtain the proper threshold voltage values. ECL to CML level converter pots R104 and R89 were adjusted to obtain -1.85V at the pins 6 and 9 of Q4 and Q5, pin 9 of Q3 and Q2 and pin 6 of Q1. CML to ECL level converter (R87) was adjusted to obtain -1.7V at pin 2 of Q1. ADC adjustment included R115 and R116 to obtain FLIA to -3.4V. All the voltage regulators on power supply regulator PCB were also adjusted to the proper voltage levels before connection to the data acquisition PCB. Fine tuning the power supply consists of measuring and adjusting the supply voltage at every IC on the data acquisition PCB. This was done to account for voltage drop in the connecting ribbon. The DEMUX VCO2 supply was adjusted at -0.3V to optimize the performance of the package part. The data acquisition PCB jumper settings are summarized below.

Jumper information on data acquisition board:

A. DEMUX Jumpers

1. JP1 Jumper position: Open

   Overflow reset select disable.

2. JP2 Jumper position: P1 to 2

   Normal parity select.

3. JP3 Jumper position: P1 to 2

   Disable the PN generator.

4. JP4 Jumper position: P3 to 4

   Disable the PN generator.

5. JP5 Jumper position: P1 to 2

   Gray-to-binary adjusted to pass data from ADC undisturbed. Data errors are introduced during hardware conversion. Hence it was decided to perform conversion through software.

B. ADC Jumpers

1. JP9 Jumper position: P 3 to 4

   Delay select adjusted to tap7. Delay of 7x20ps between falling edge of sample clock and falling of latching clock.

2. JP11 Jumper position: P1 to 2 and P3 to 4

   Provide FLIA voltage to ADC. This jumper should be a short.

3. JP12 Jumper position: GND

   Output clock select. Always ADC clock as this is shorted to GND.

C. TIU Jumper

4. JP7 Jumper position: P3 to 4

   TIU stop clock select. DEMUX clock is selected.

2.5.3 DAS800 Test Results

The DAS800 system was tested and verified to function beyond the target design frequency of 800 MHz. It is believed that the system is limited by the commercial FIFOs as well as the commercial ECL/TTL and ECL/CML level converters. For the 3000 MHz design, custom FIFO will be designed and the commercial level converters will not be needed.

TIU testing was done to evaluate the speed limitation of the system since packaged TIU has been tested to operate up to 5GHz. The main system clock speed was increased up to 3GHz for testing purposes while the HP8180A used to generate the control signals were triggered externally from 10MHz reference generated by the clock source (HP8665B). Thus the laser launch and the return pulse are synchronized to the input clock. This is required to accurately count the number of clock periods of the 3GHz clock between laser launch and laser return pulse. The coarse count (distance) between laser launch pulse was varied by changing the return bit position in the memory of 8180A. Change in one memory location changes the TIU count by 300 as expected. (as there are 300 periods of 3GHz clock in every 10MHz clock period). The acknowledge selection option (The TIU acknowledge signal used to start the digitizing hardware can be generated from either the high-speed ADC clock or the slower DEMUX clock) is selected by JP7 functions as expected. Since the TIU can stop on either the ADC clock or DEMUX output clock edges, the observed difference in count register has an expected maximum difference of 8. This is expected because the ADC clock is 8 times faster than DEMUX clock thus the edge difference between stopping on DEMUX clock and stopping on ADC clock should be no more than 8. The interface bus signals between AT-DIO 32 board and ISA interface board is shown on logic analyzer photograph in Figure 2.5-4. Input voltage specifications are tabulated below for the DAS800 system. The right SMA connectors on the front panel of DAS800 are defined to be the positive signal in the differential inputs.

Signal	Voltage	Signal	Voltage	Fin	Vout
LPL High	-0.9V	Gate High	0V	25.6MHz	0.8V
LPL Low	-1.8V	Gate Low	-0.6V	51.2MHz	0.75V
LPR High	-0.9V	System Clock	0.8V	100MHz	0.7V
LPR Low	-1.8V		0.8V	200MHz	0.6V

Functionality testing was done with clock frequency at 800MHz. Analog input waveforms with different modulations were sent in and captured on laser return acknowledgment. Figure 2.5-5 and Figure 2.5-6 shows the amplitude modulated waveform as seen on oscilloscope screen and as captured by DAS800 on PC. Figures 2.5-7 through 2.5-9 illustrate the DAS800 acquiring a wide variety of input waveforms. Frequency response of DAS800 is in figure 2.5-10 using a full scale (0.8Vpp) input sinewave. In summary, the test results show that the DAS800 functions as expected with respect to the coarse count and the digitized signal.

3.0 Summary of Financial Status

Month	Expenditure this month cost+fees	Cum. Expenditure to data cost+fees
July	$50,513	$1,349,441
Aug	$47,858	$1,397,300
Sept	$48,486	$1,455,787
Oct	$43,098	$1,488,884
Nov	$39,756	$1,528,640
Dec	$28,578	$1,557,218

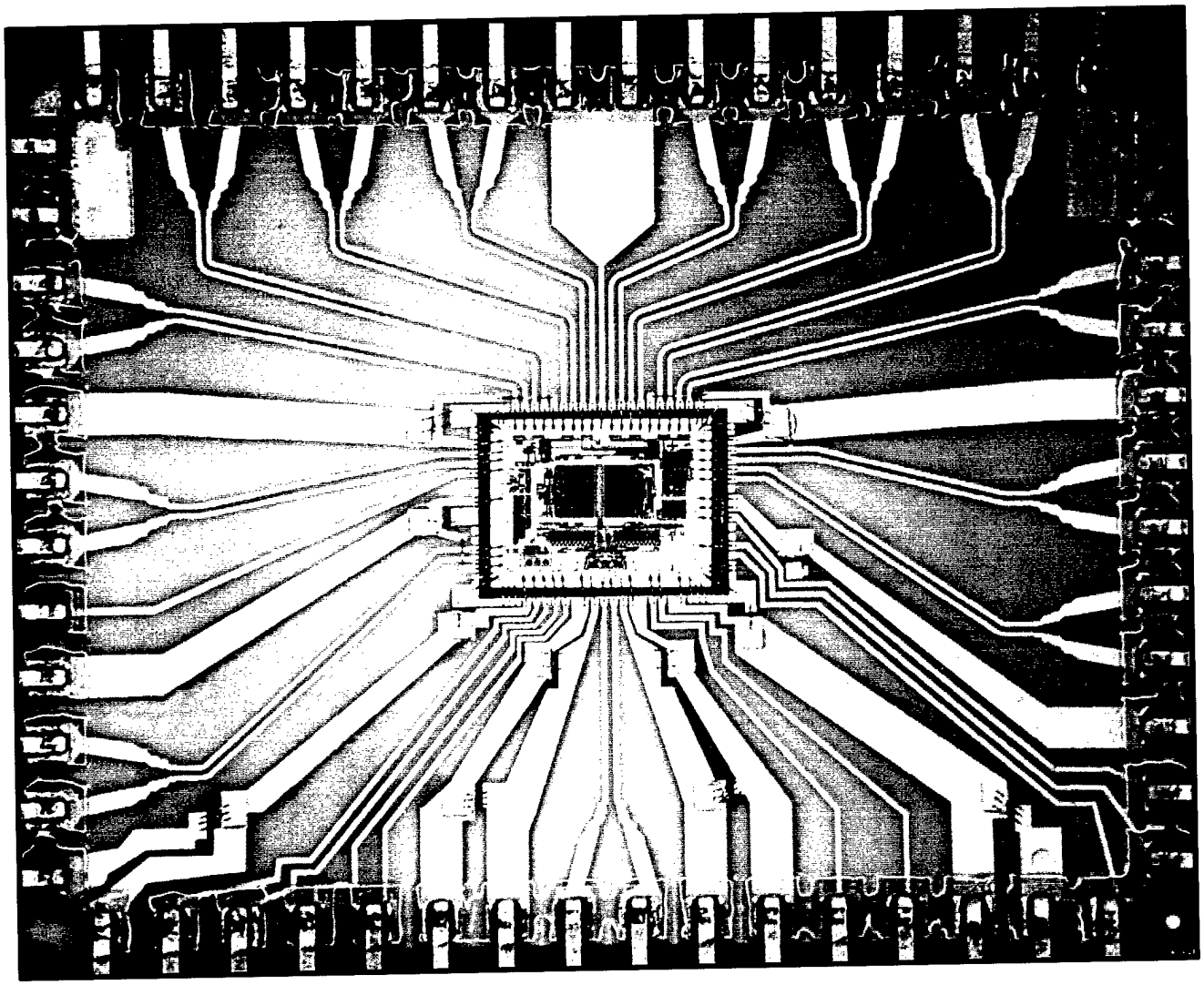


Figure 2.1-1: A photograph of a packaged ADC with the protective epoxy cap removed.

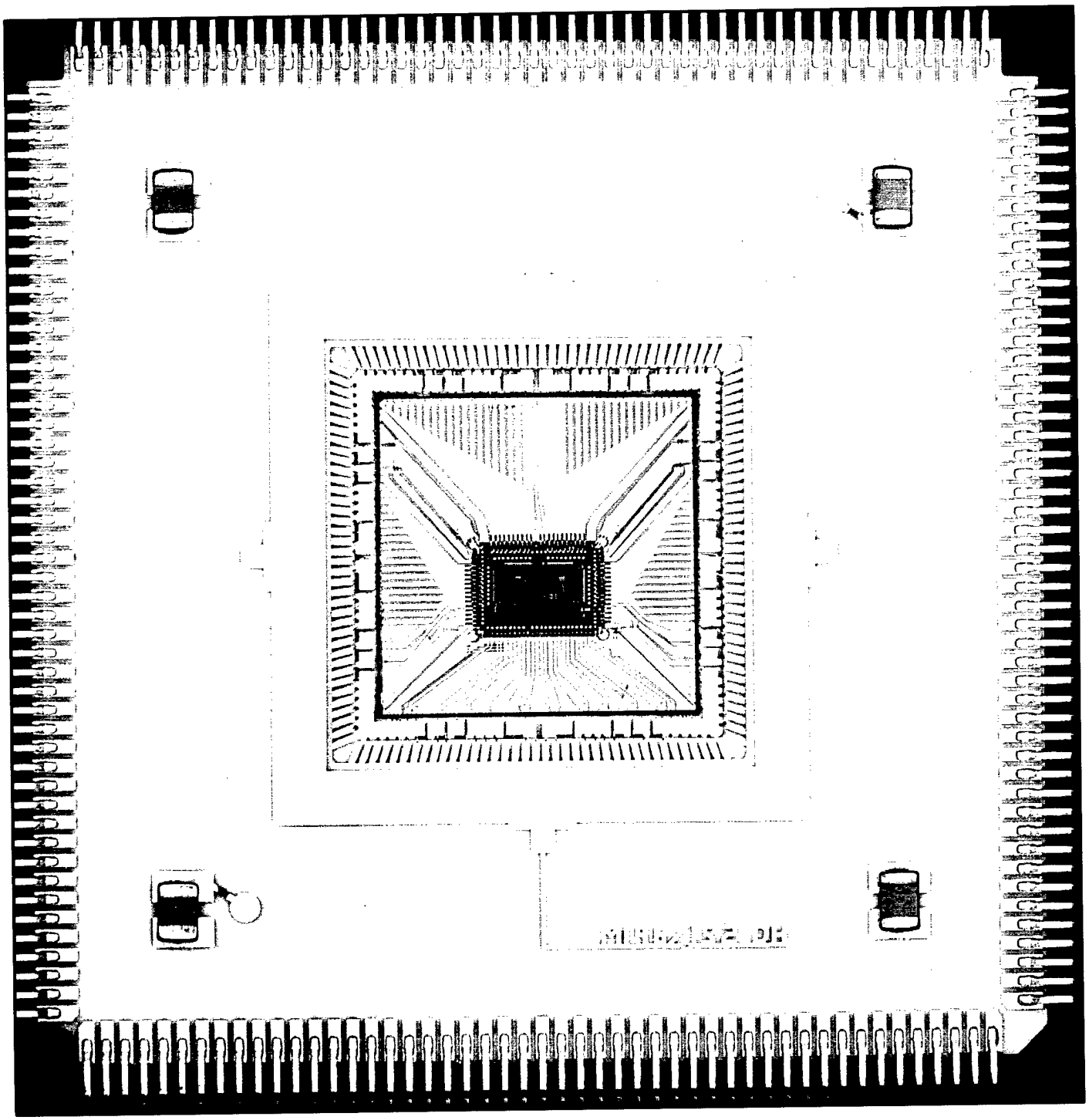


Figure 2.1-2: A photograph of the entire DEMUX package without the protective lid.

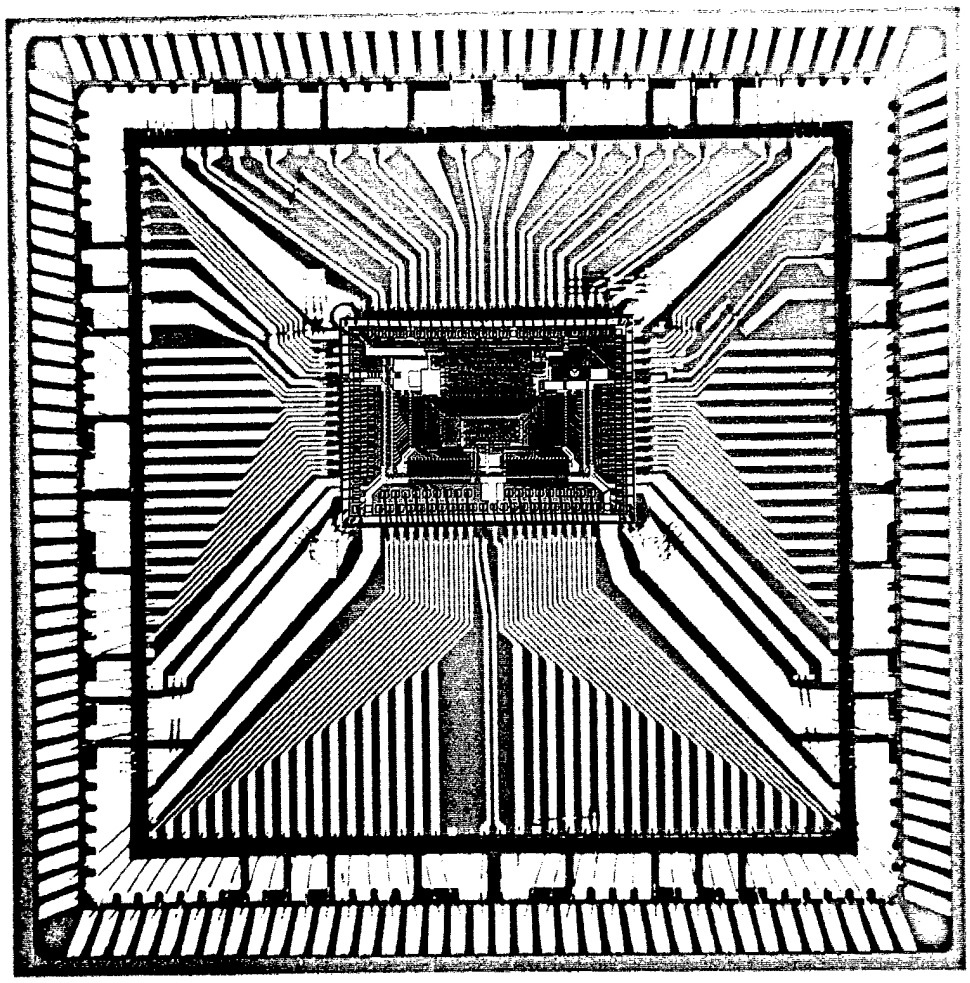


Figure 2.1-3: Enlarged DEMUX package showing details of the alumina controlled impedance substrate.

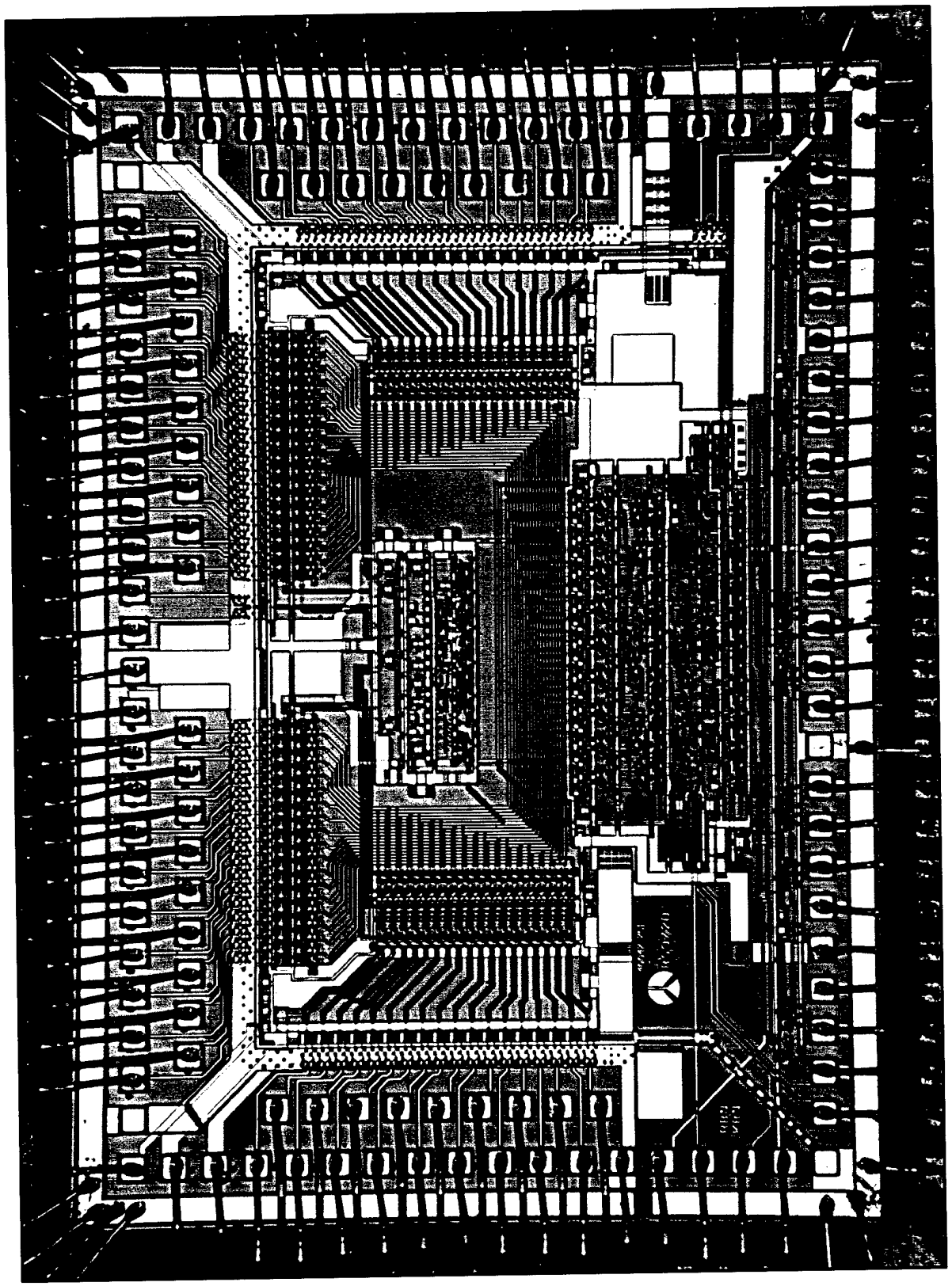


Figure 2.1-4: Extreme close up of the DEMUX Package showing the fine line lithography of the substrate and the numerous bondwires to the DEMUX IC.

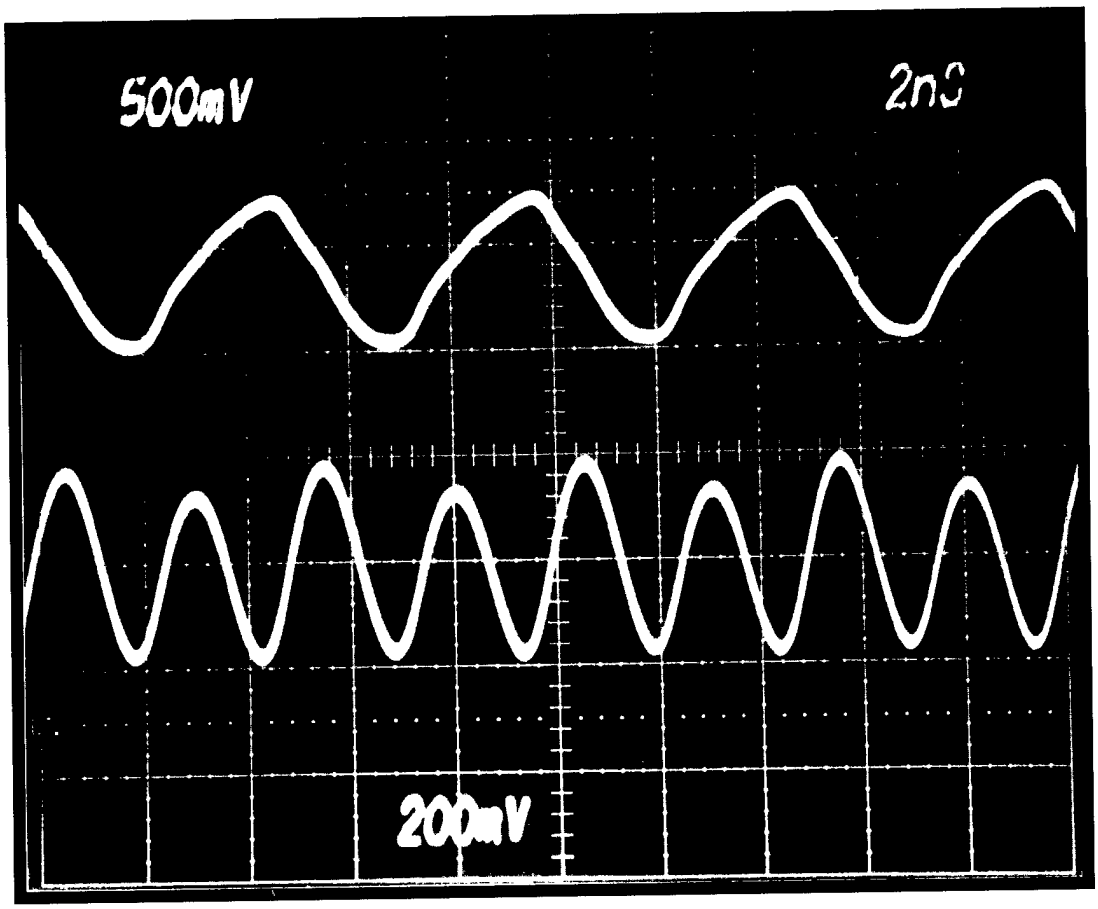


Figure 2.1-5: High-speed out put waveform of the packaged DEMUX showing the absence of oscillations and ringing when all 72 outputs are simultaneously changing states.

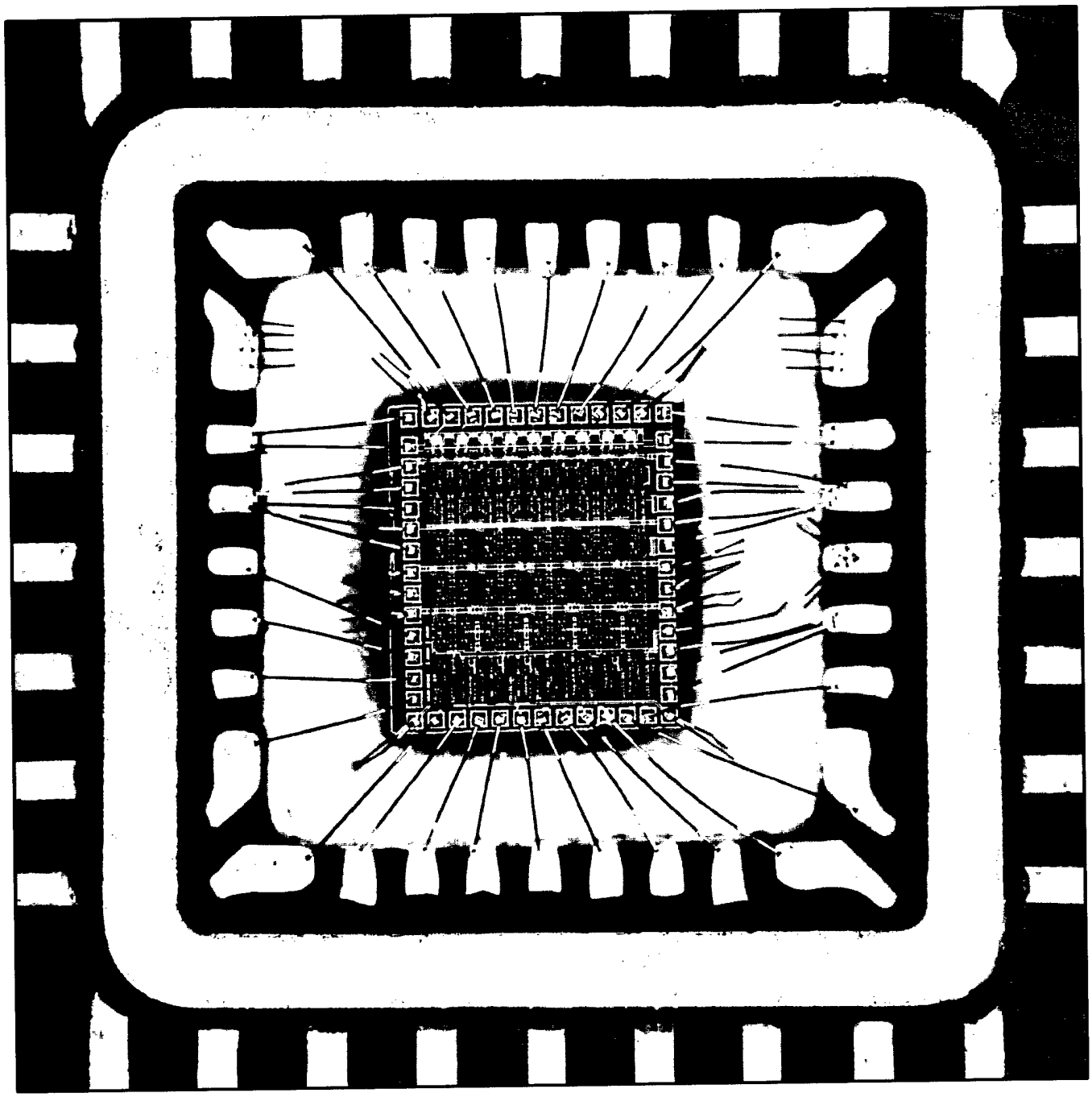


Figure 2.1-6: TIU package photograph.

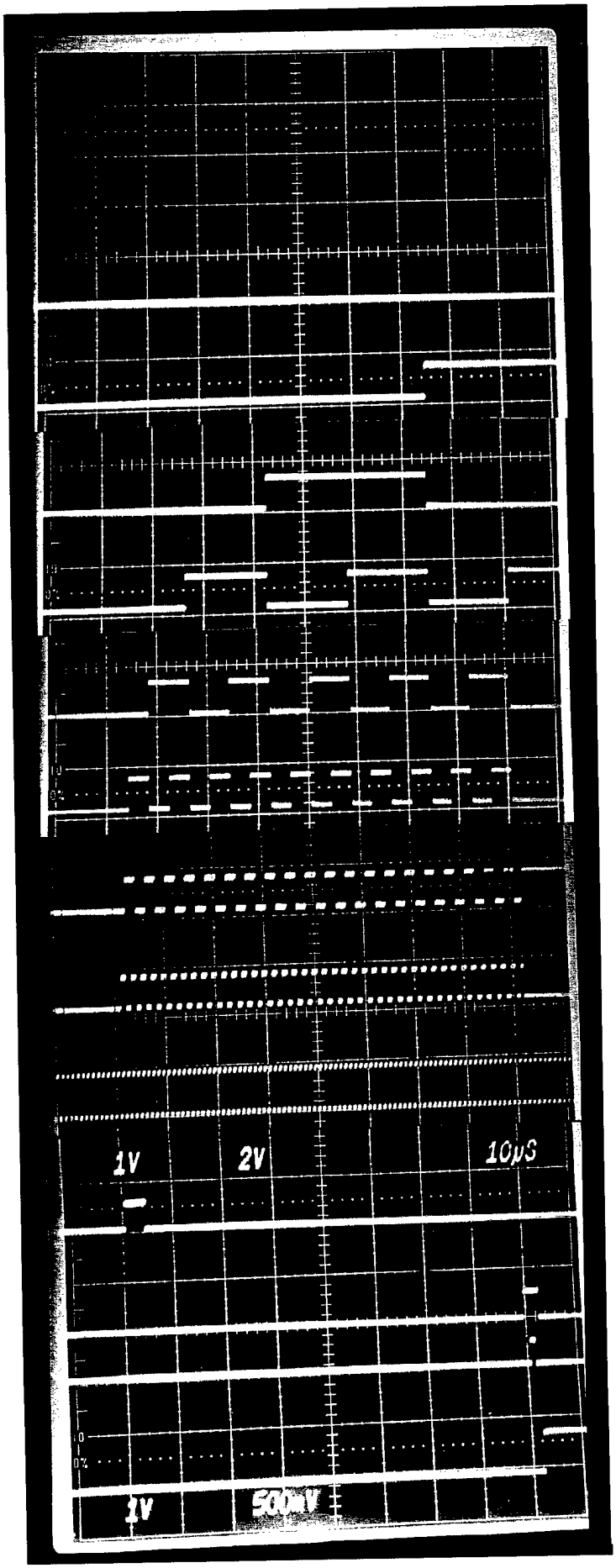


Figure 2.1-7: Functionality test of the packaged TIU showing proper operation.

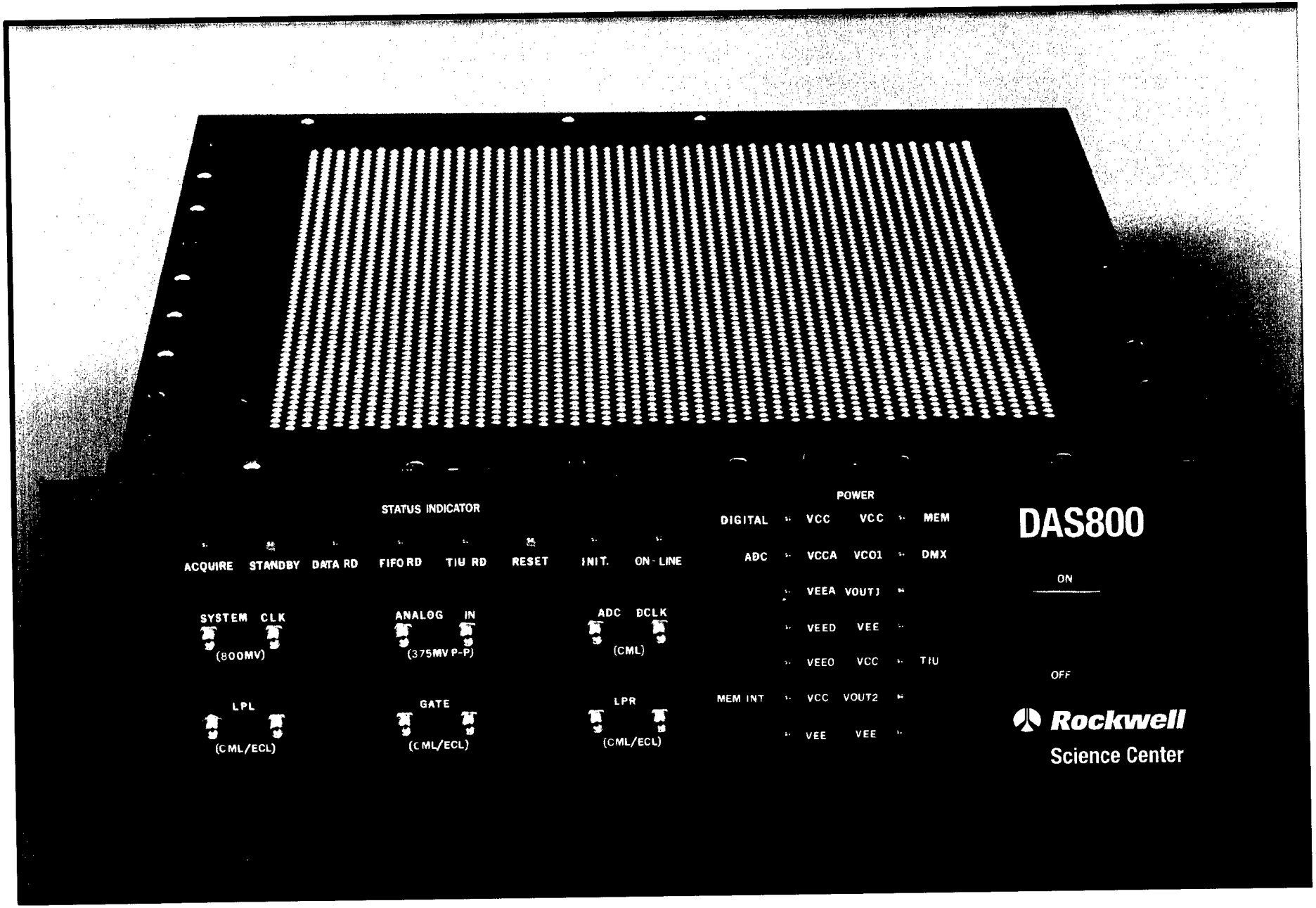


Figure 2.2-1: Front view of the 800Ms/s data acquisition system chassis.

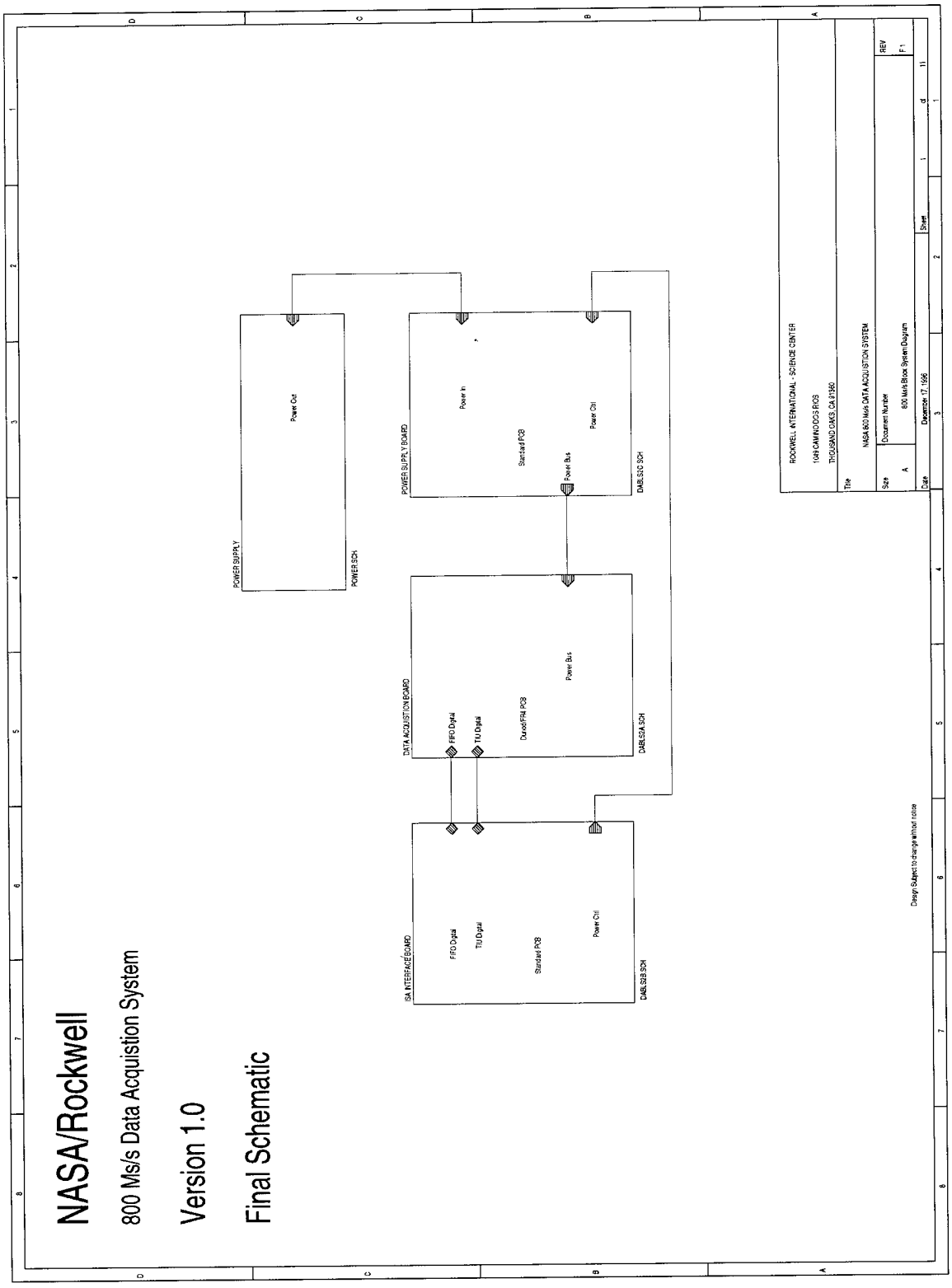


Figure 2.2-2: Block level schematic showing the interrelationship between the three PCB and power supplies.

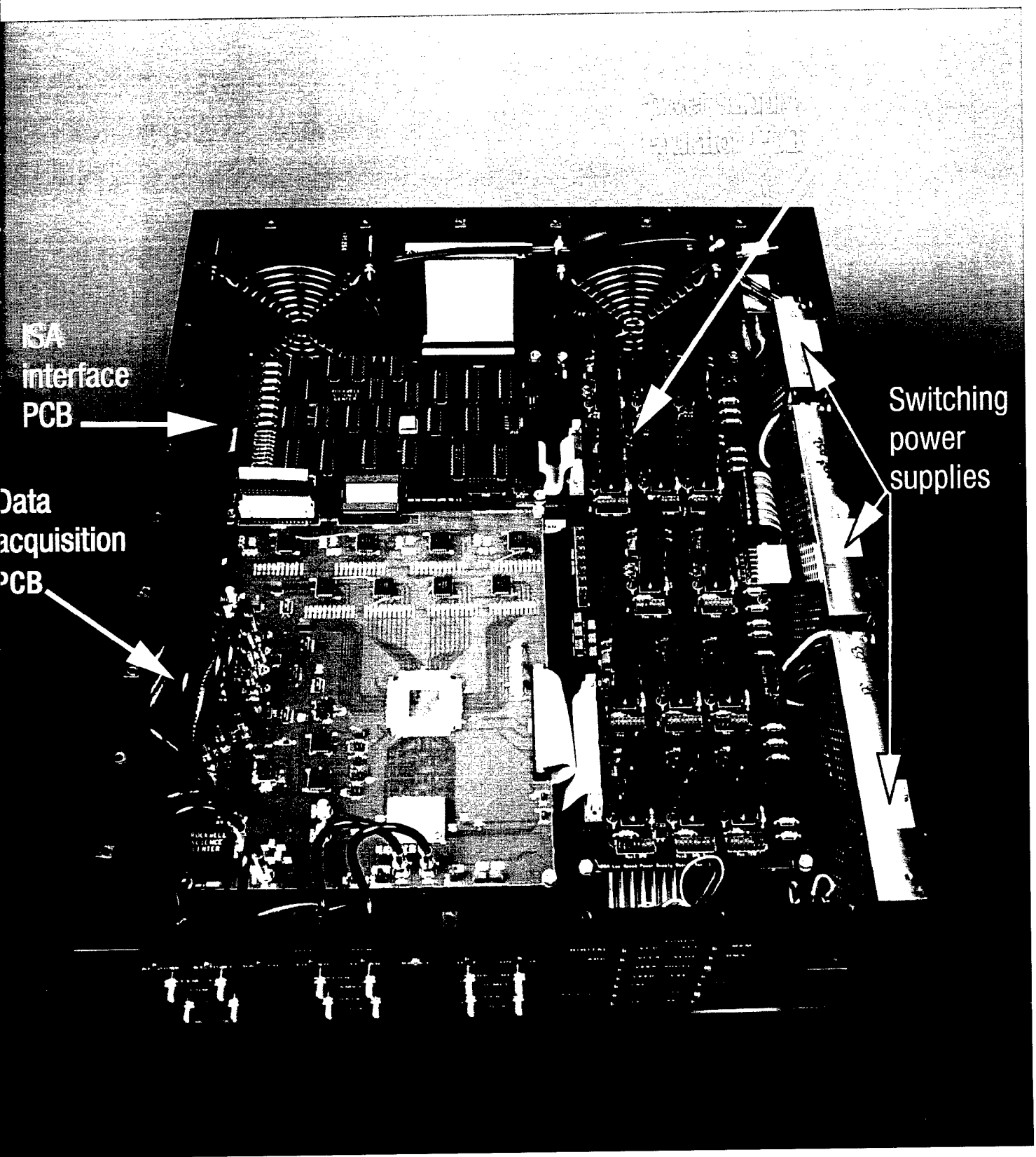


Figure 2.2-3: Top down view of the 800DAS showing the three main PCBs and the power supplies.

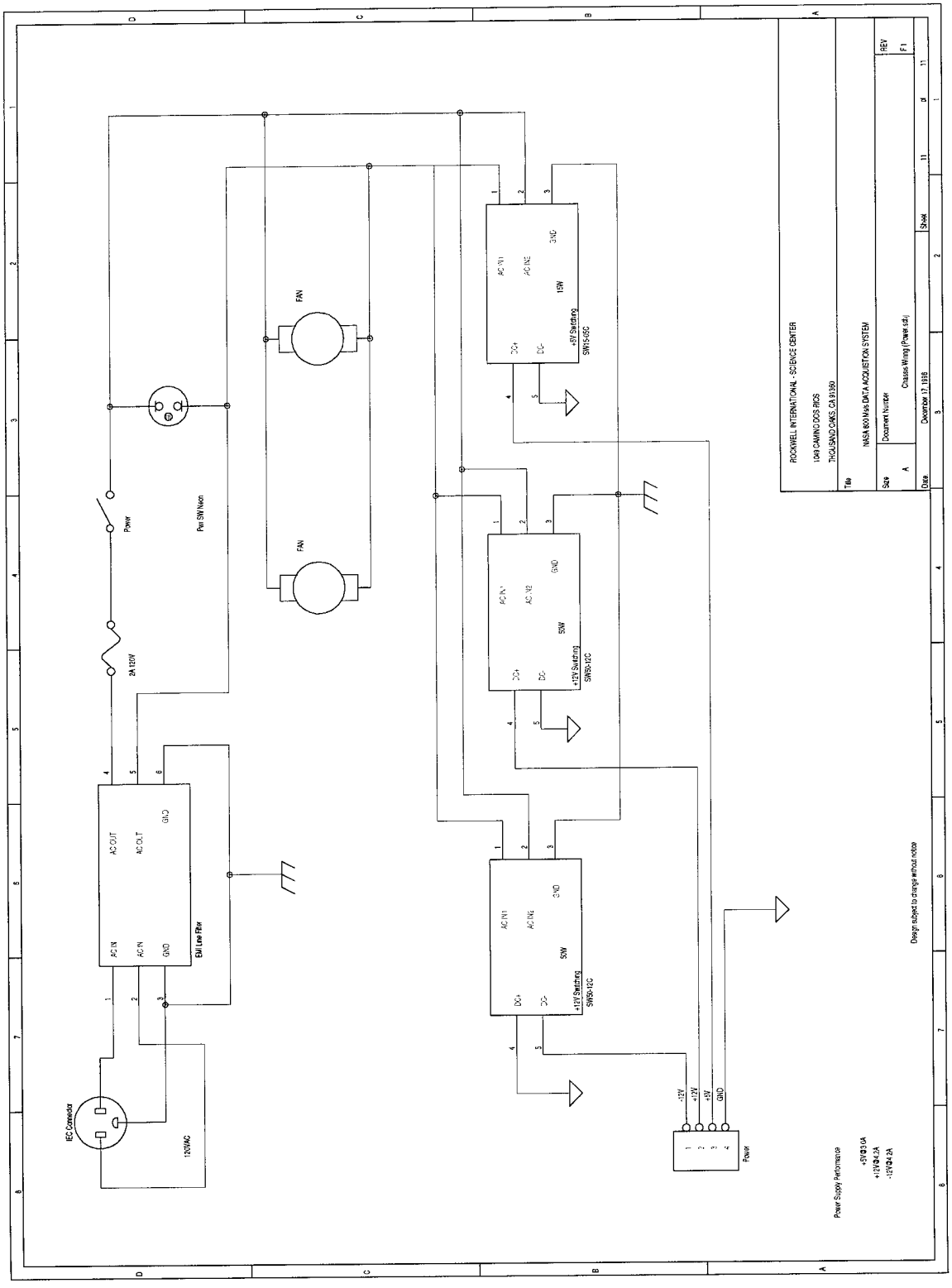


Figure 2.2-4: Power supply schematic

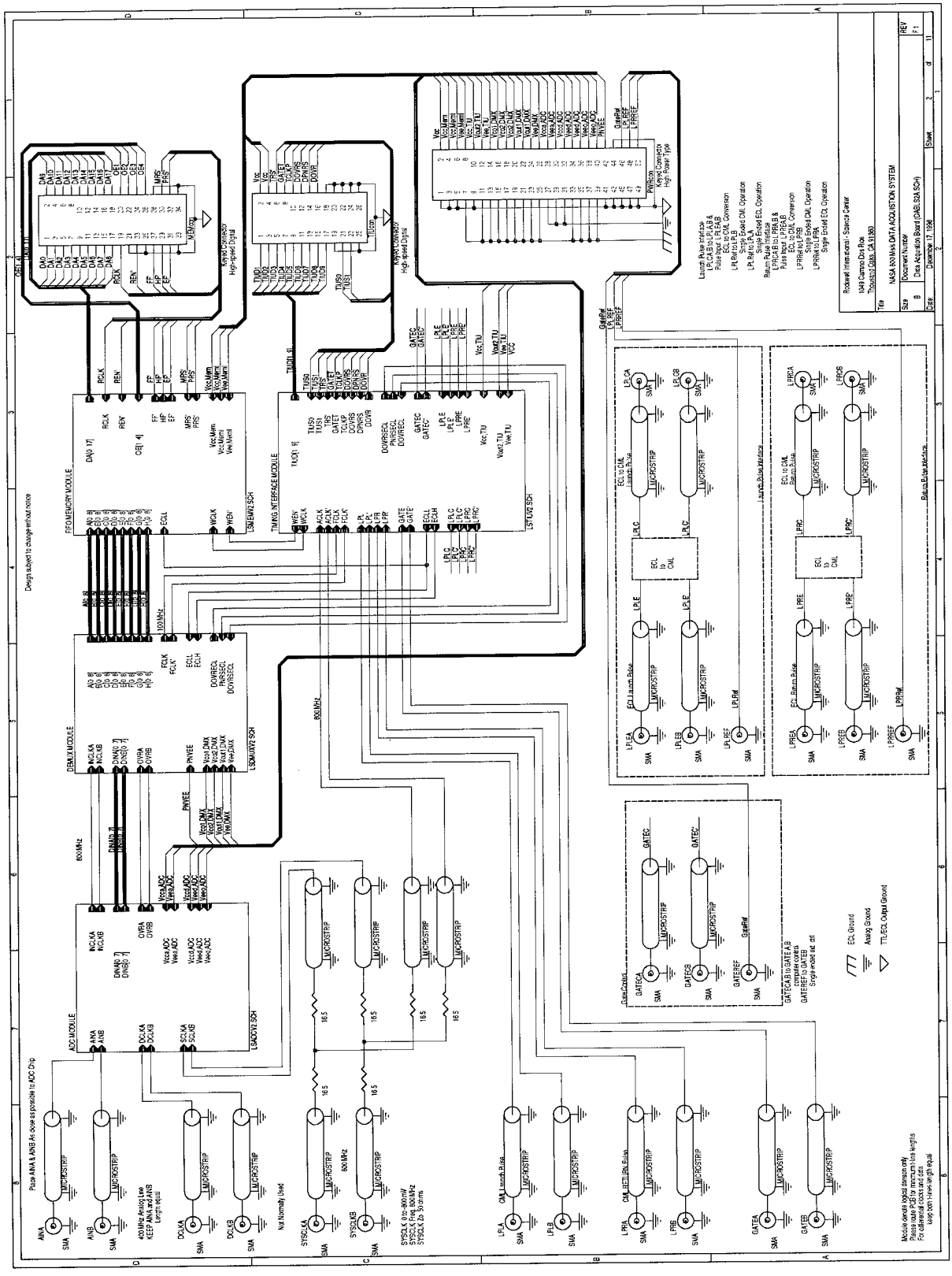


Figure 2.2-5: Data acquisition board overview schematic

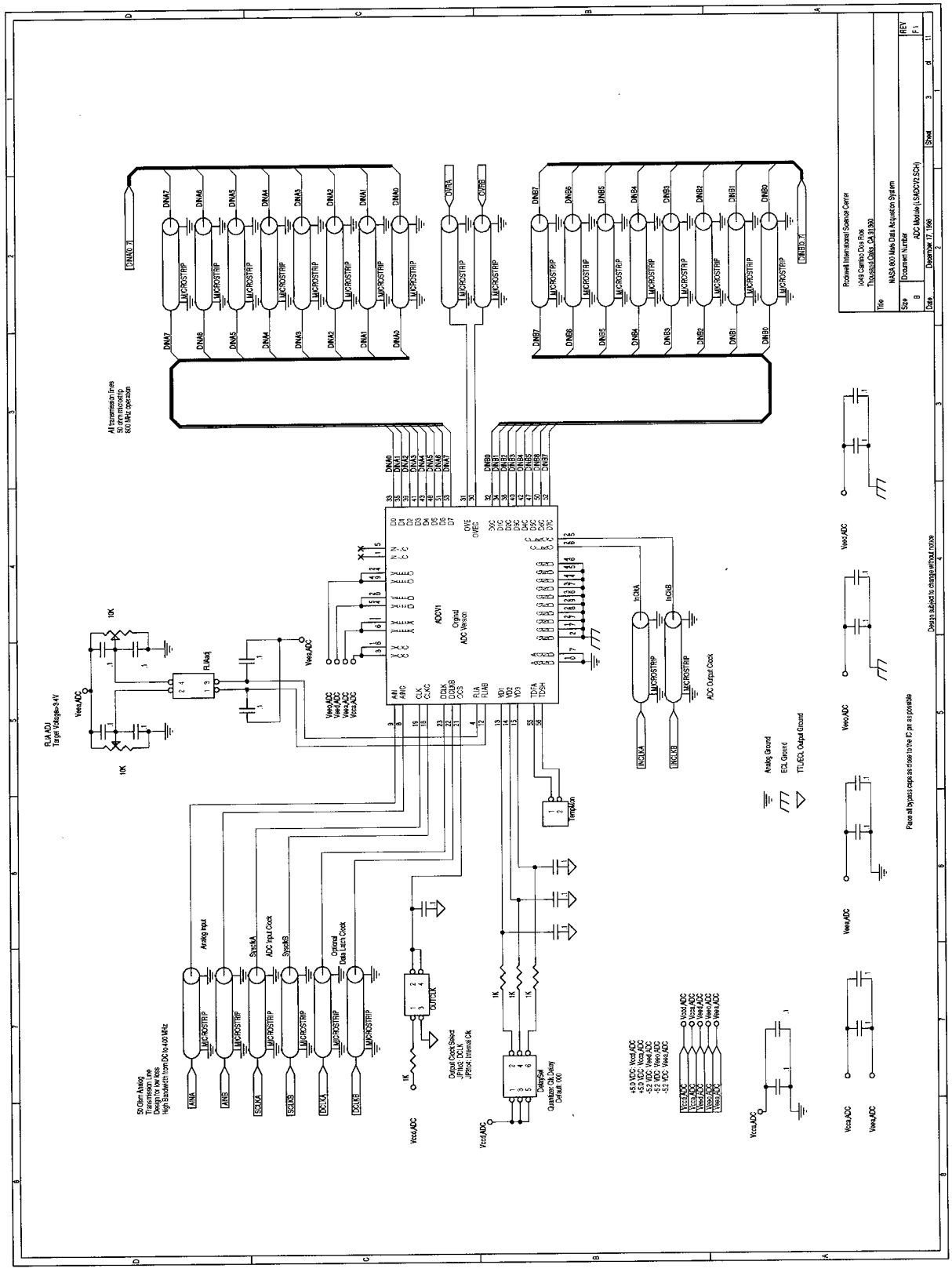


Figure 2.2-6: ADC sub-circuit schematic

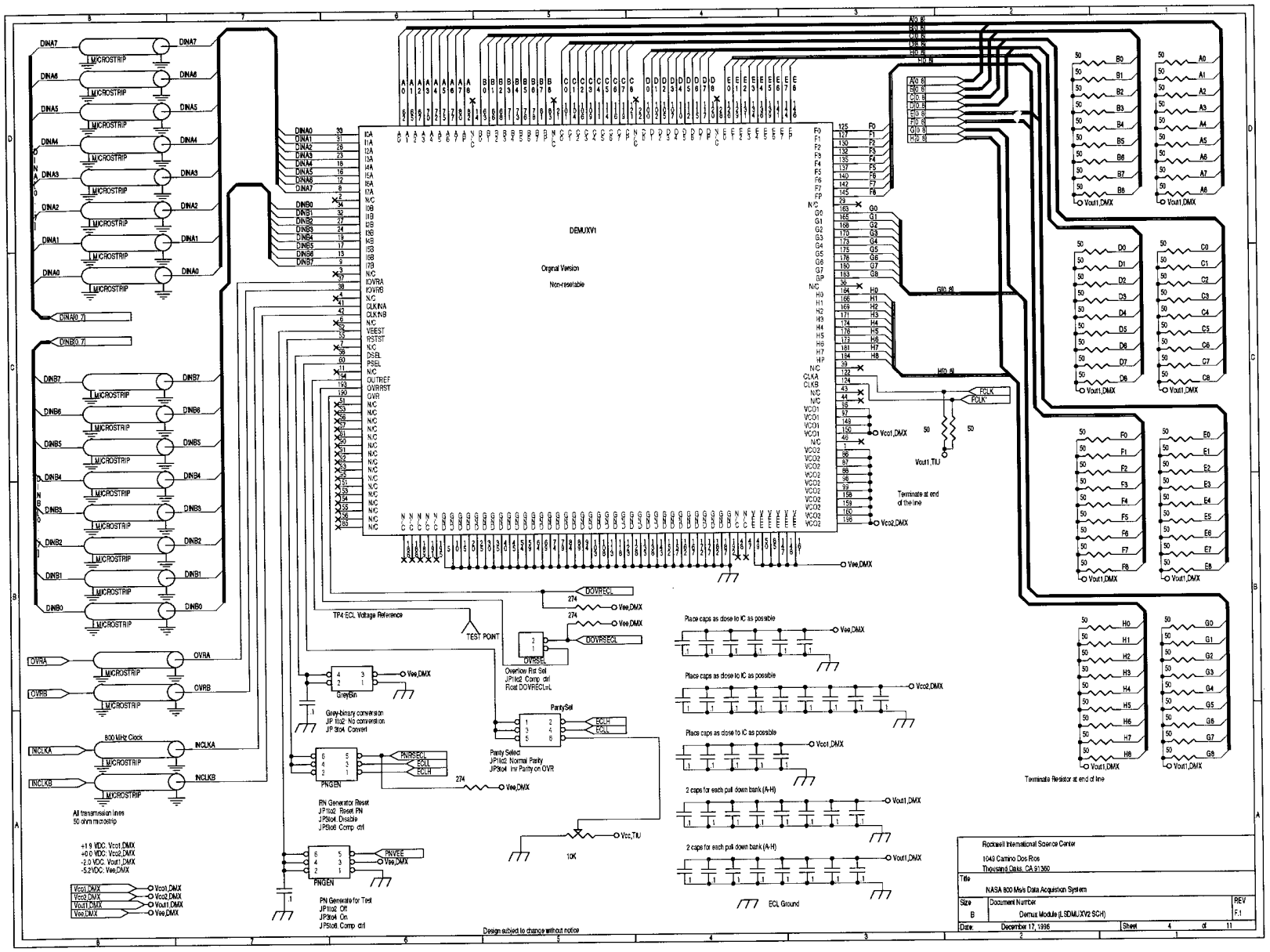


Figure 2.2-7: DEMUX sub-circuit schematic

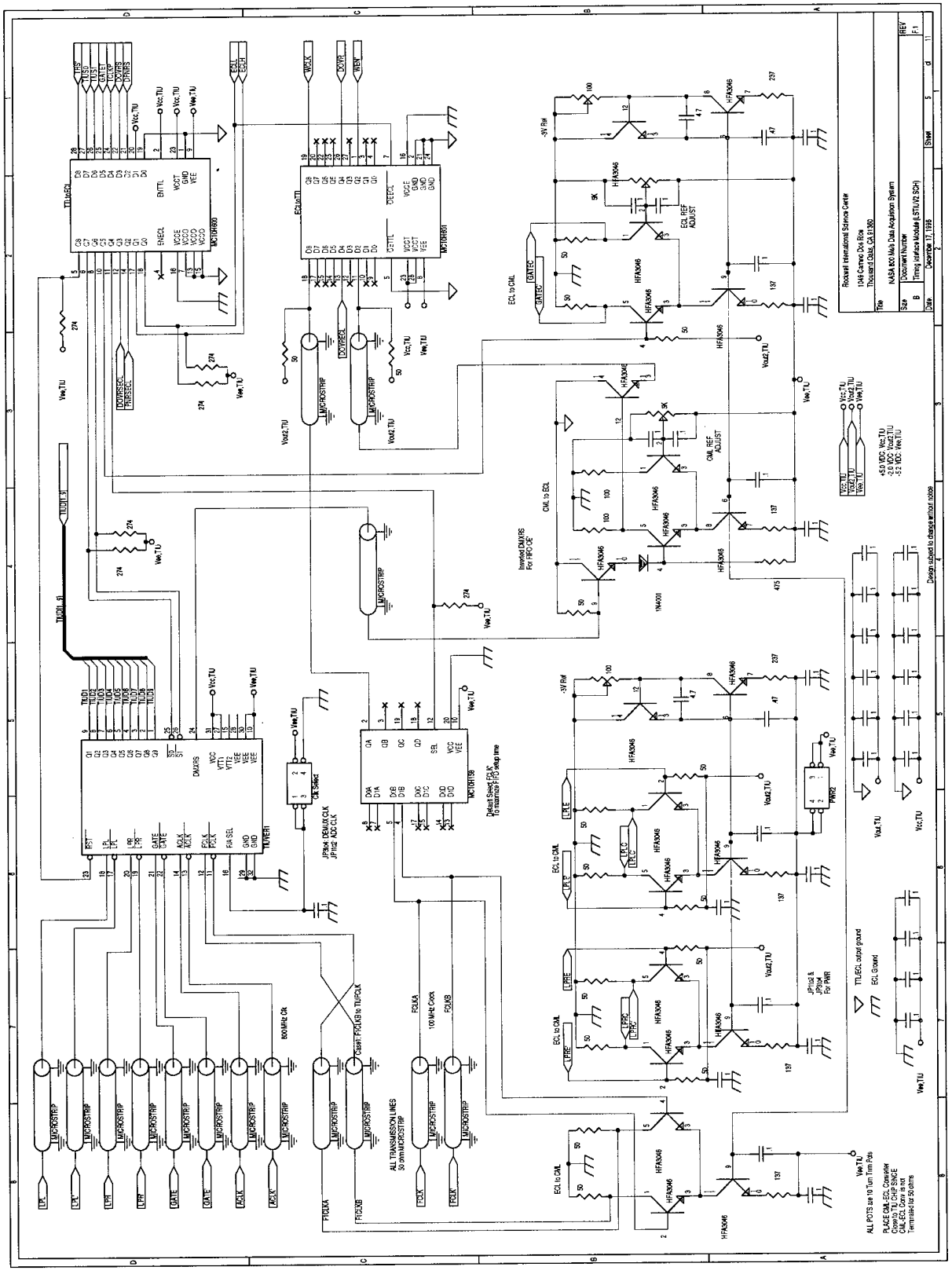


Figure 2.2-8: TIU sub-circuit schematic

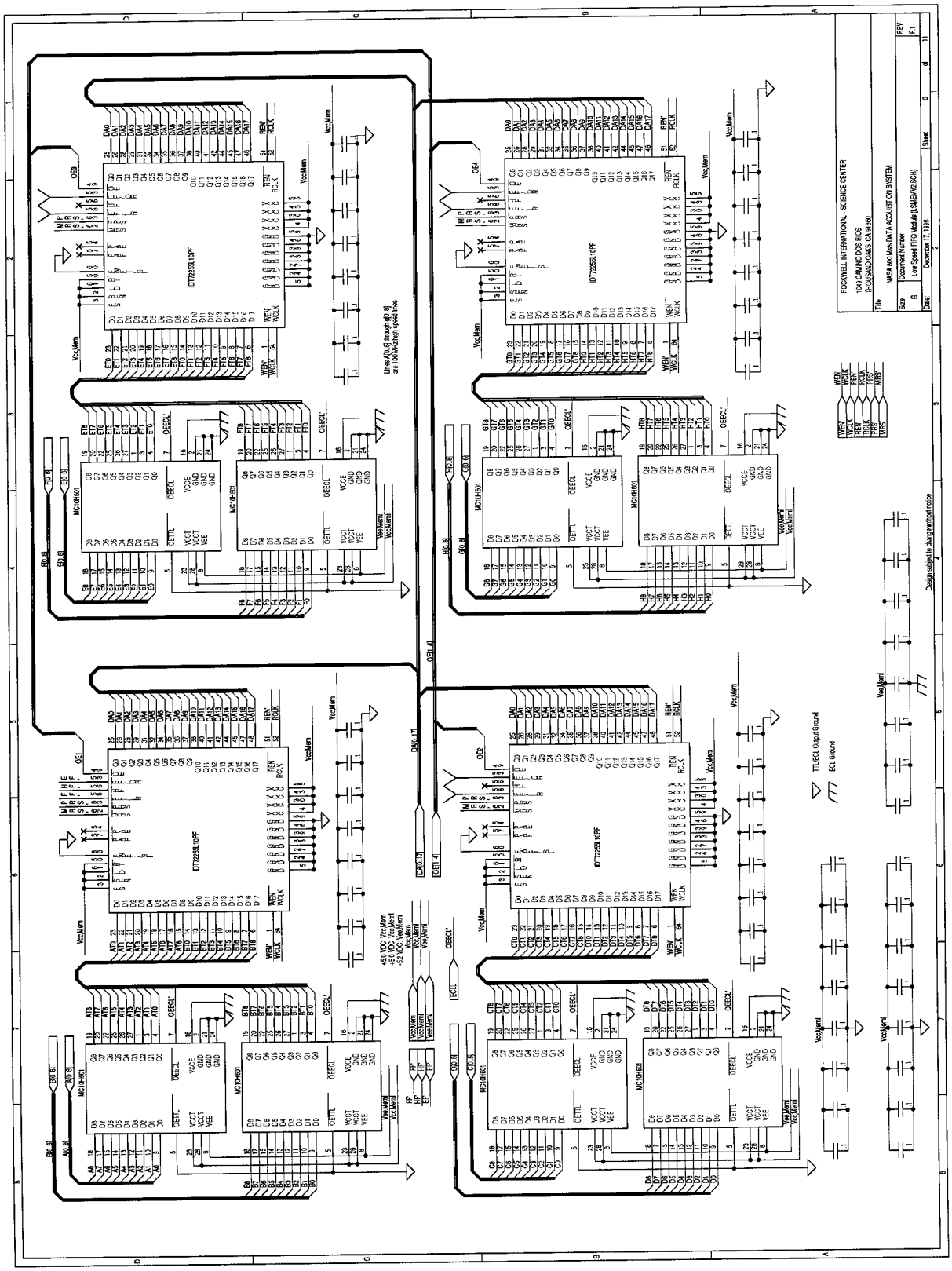


Figure 2.2-9: FIFO sub-circuit schematic

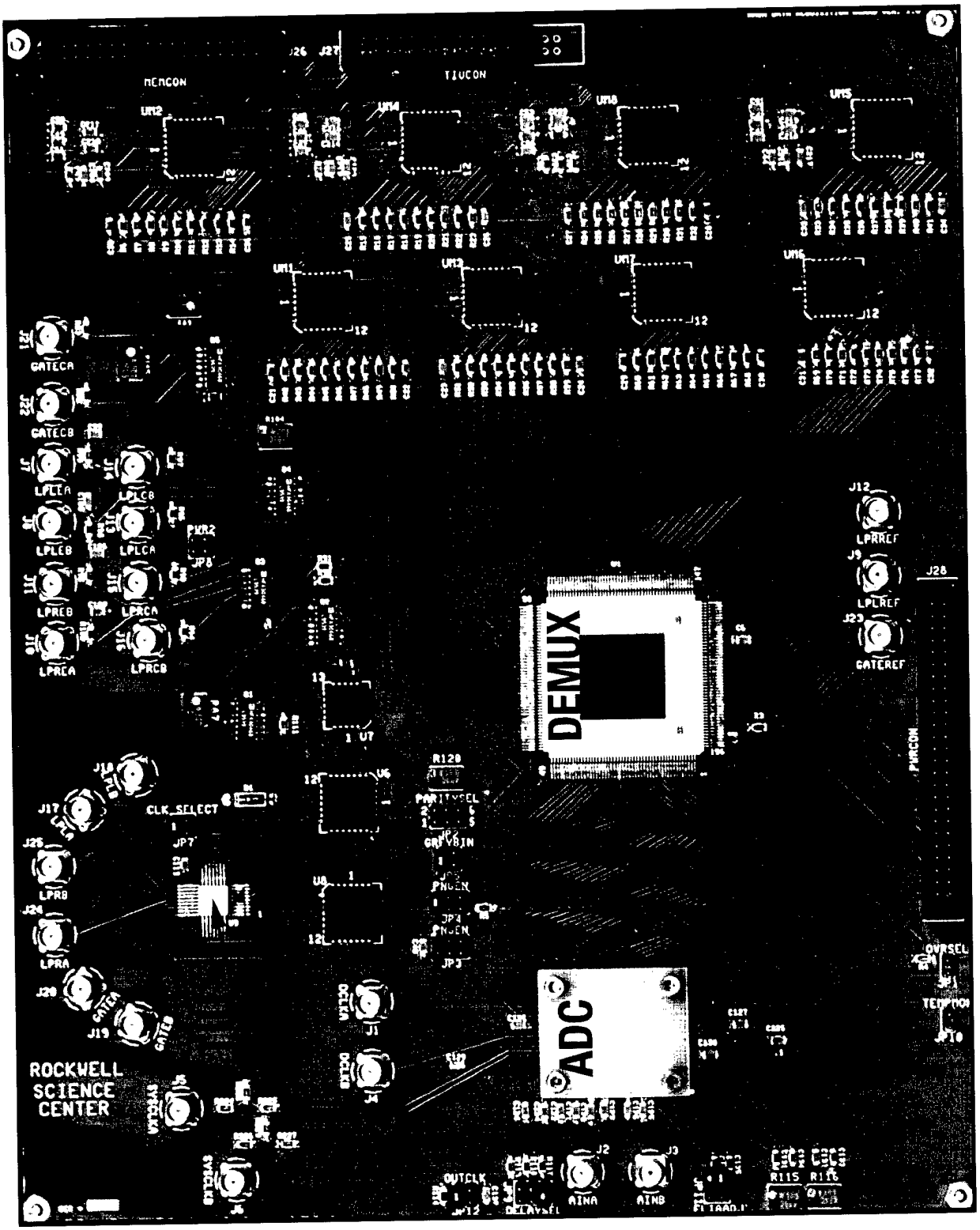


Figure 2.2-10: Data Acquisition system PCB photo.

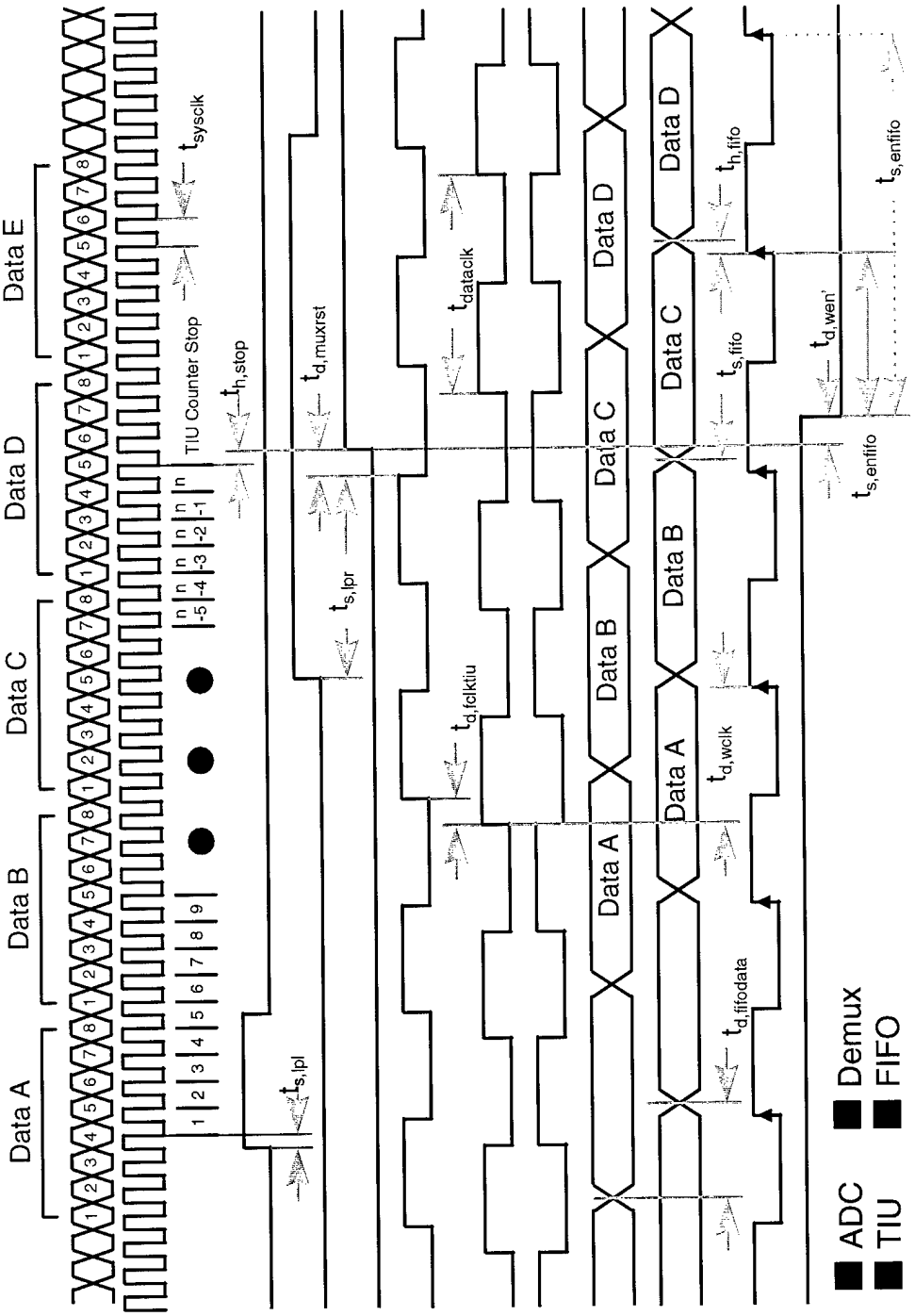


Figure 2.2-11: Timing analysis for the DAS800

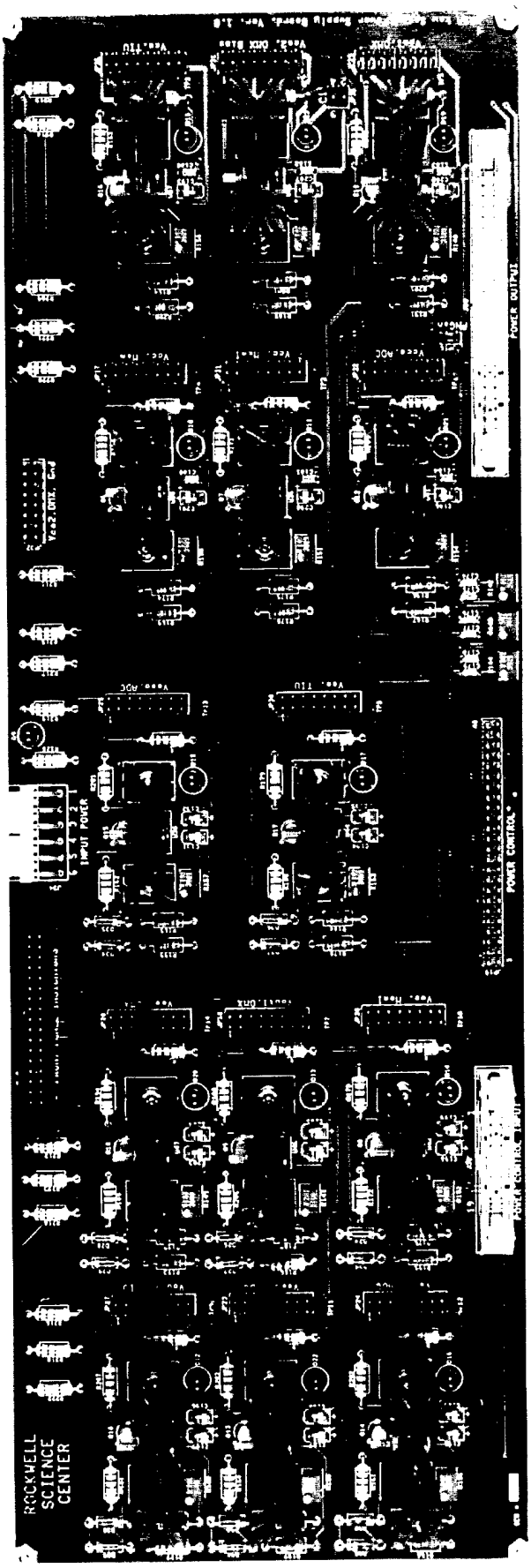


Figure 2.2-12: Power supply board photo.

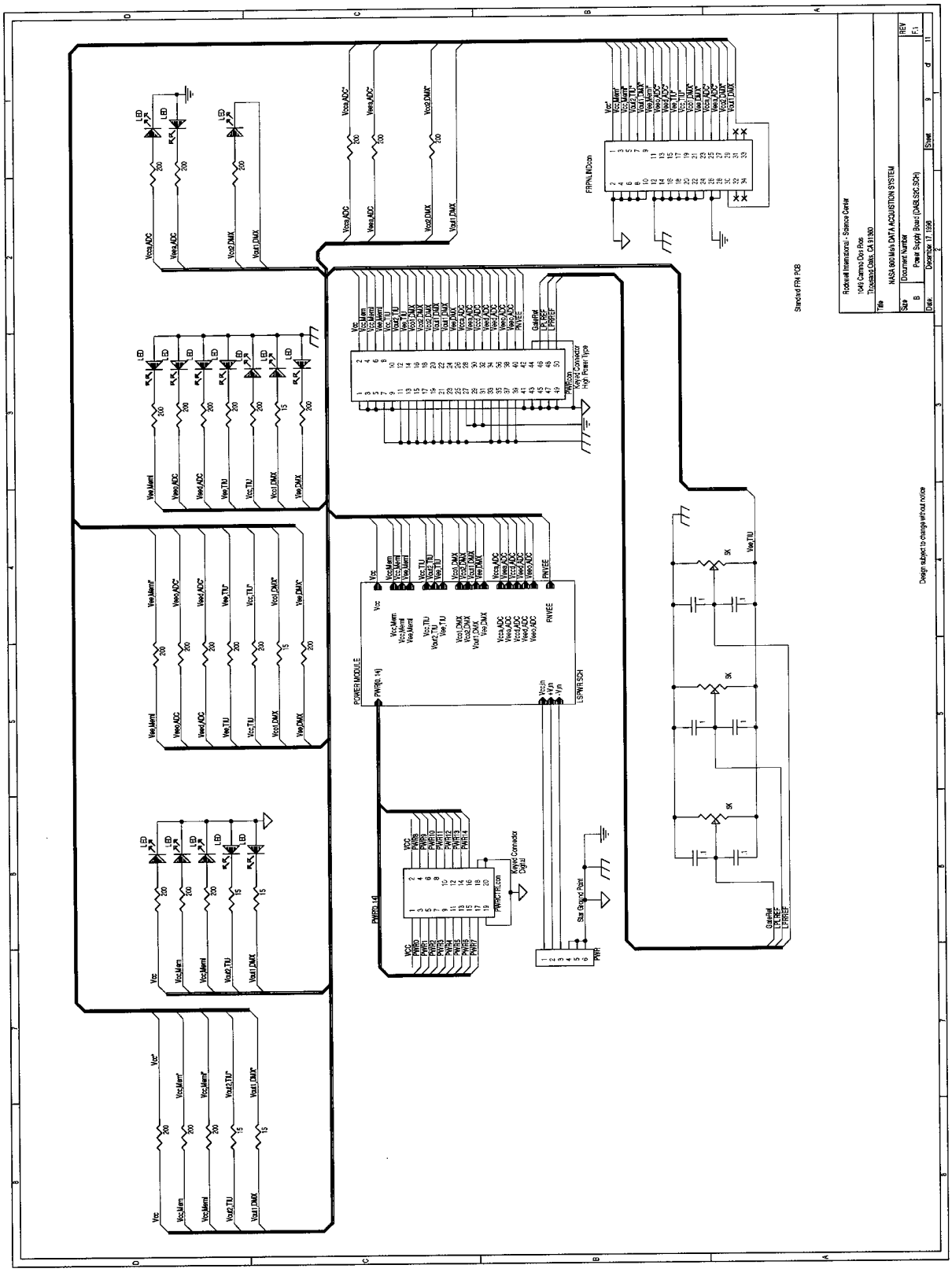


Figure 2.2-13: Power supply schematic I

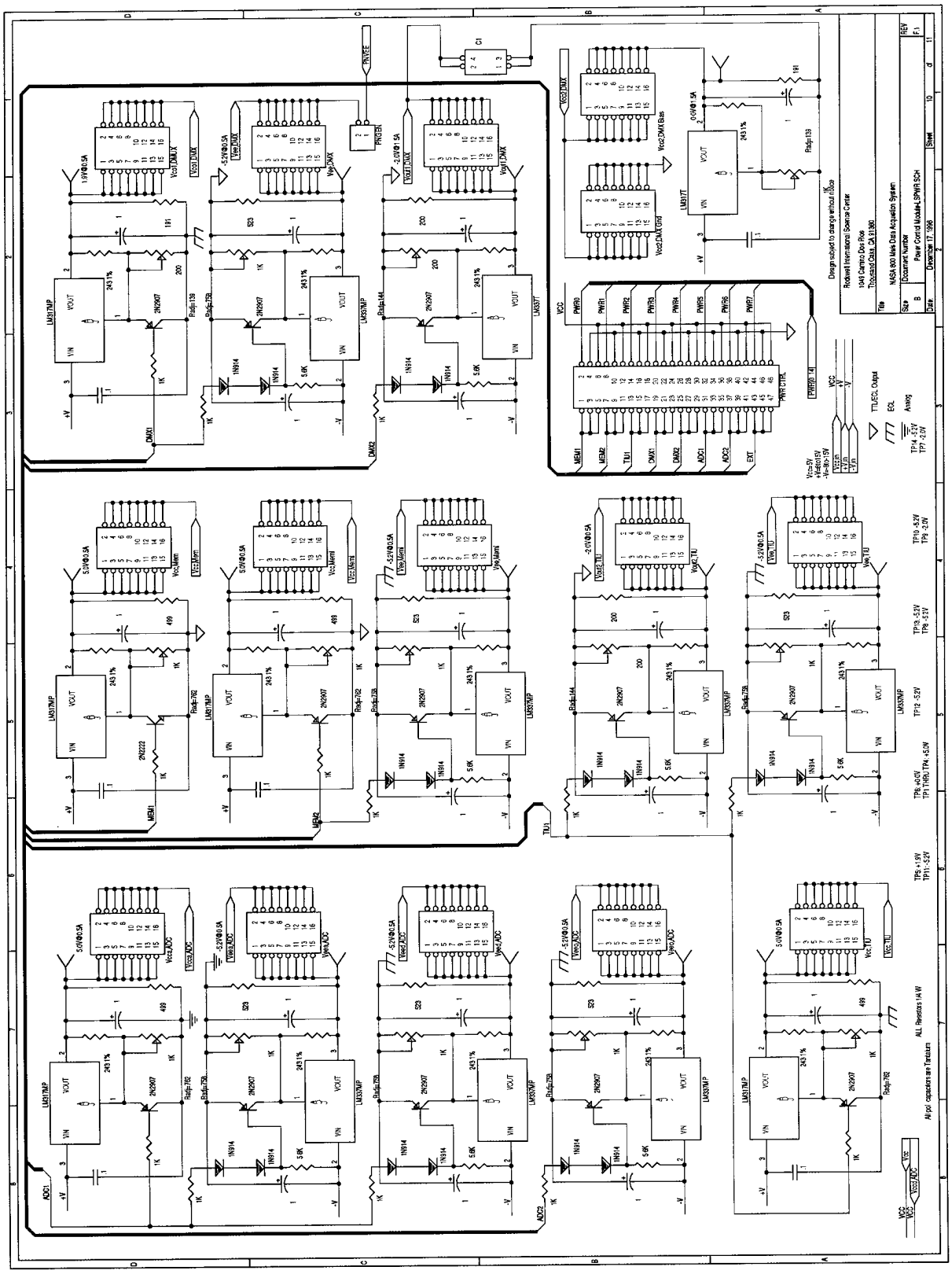


Figure 2.2-14: Power supply schematic II

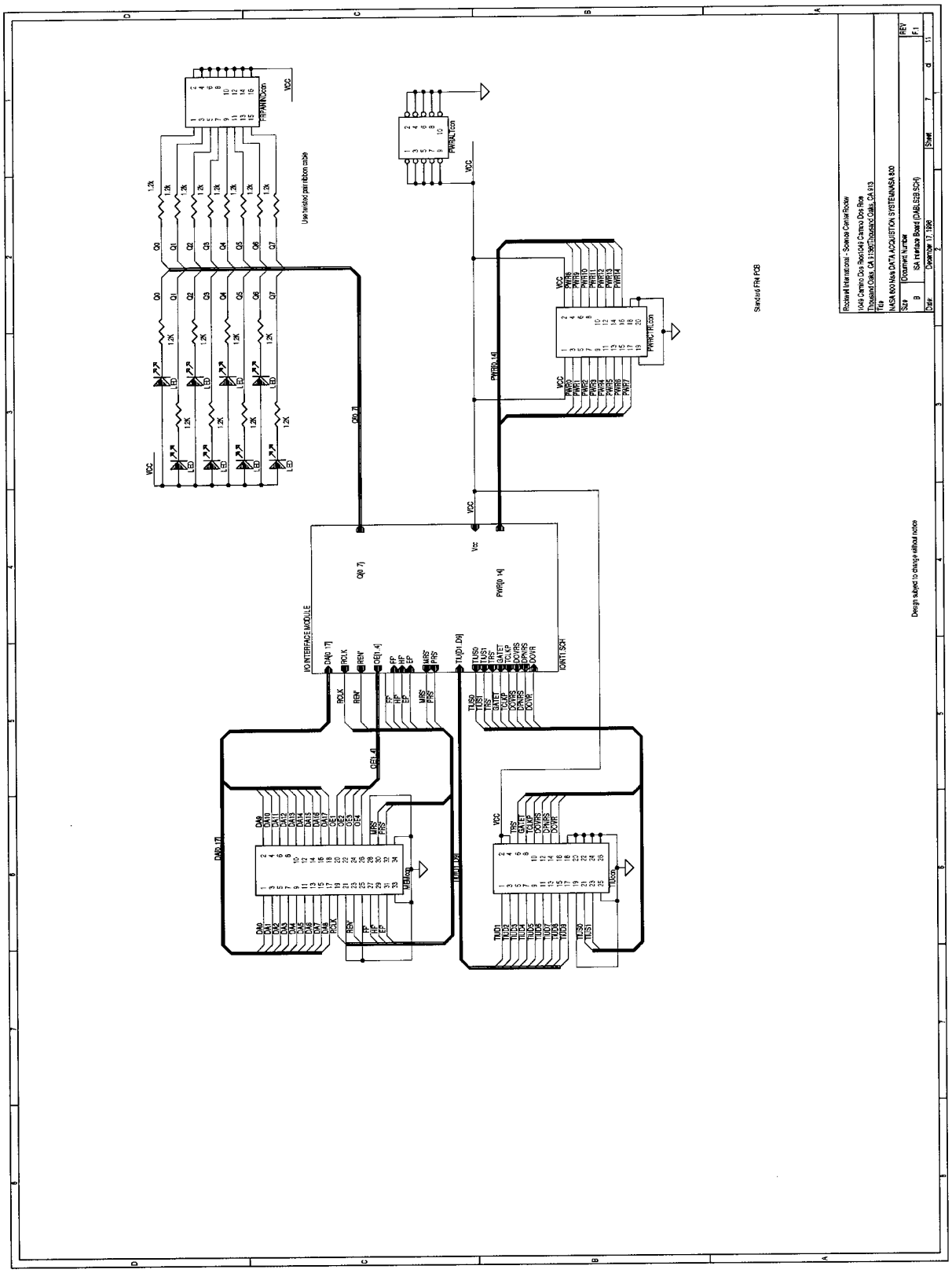


Figure 2.2-15: ISA Interface schematic I

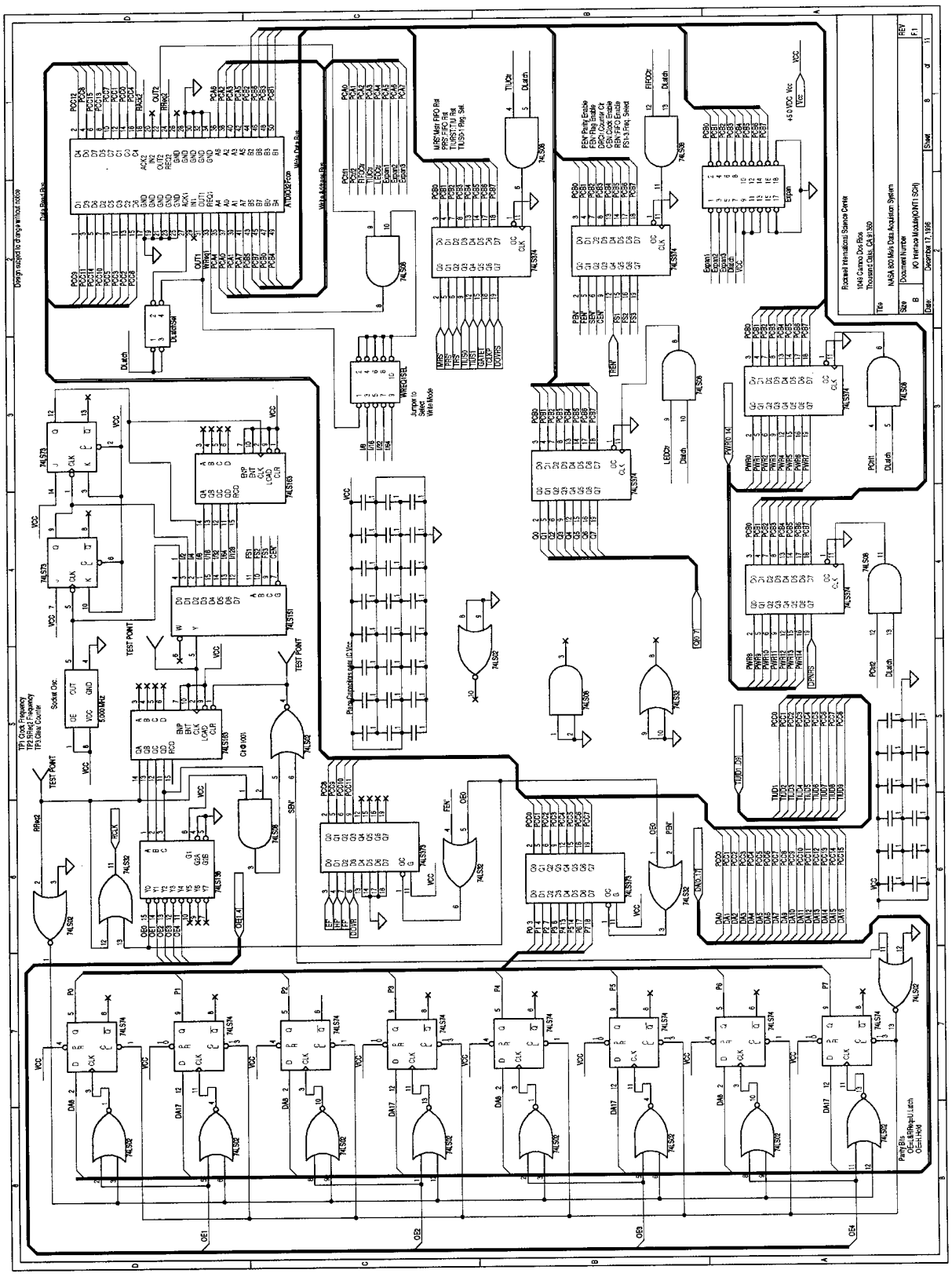


Figure 2.2-16: ISA Interface schematic II

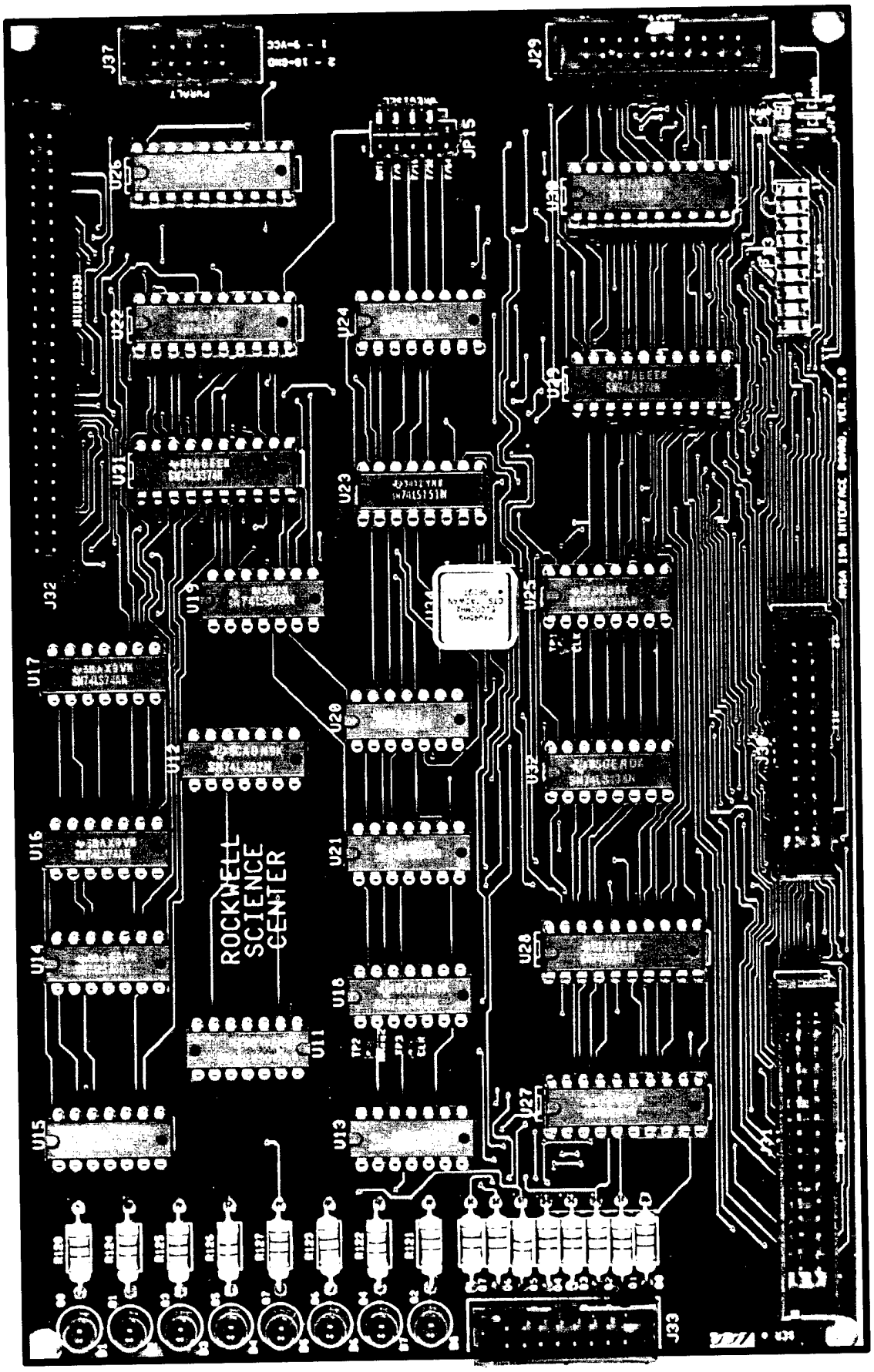


Figure 2.2-17: ISA Interface board photo.

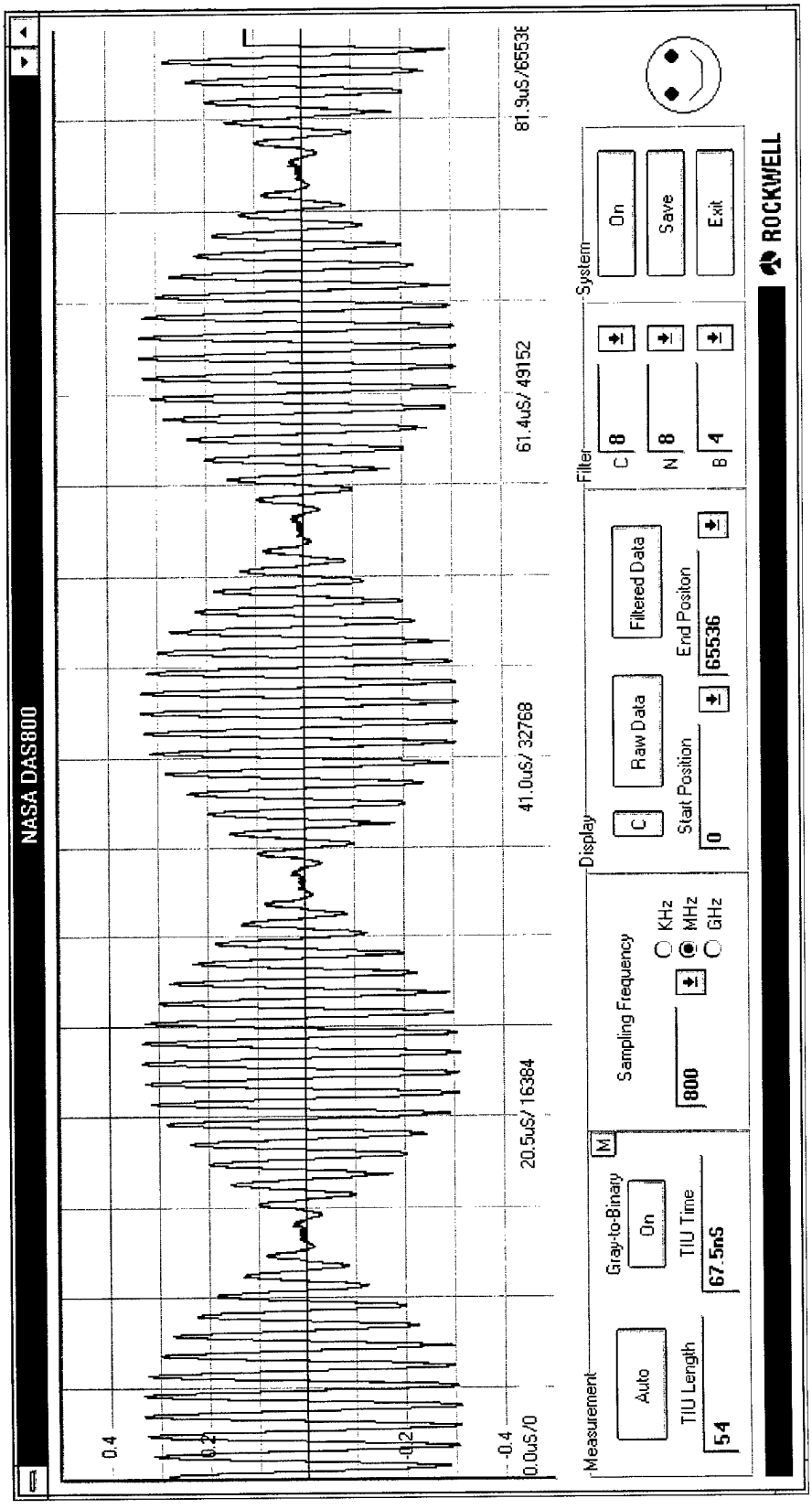


Figure 2.4-1: The main control panel of the Rockwell DAS800 Verification and Test Program.

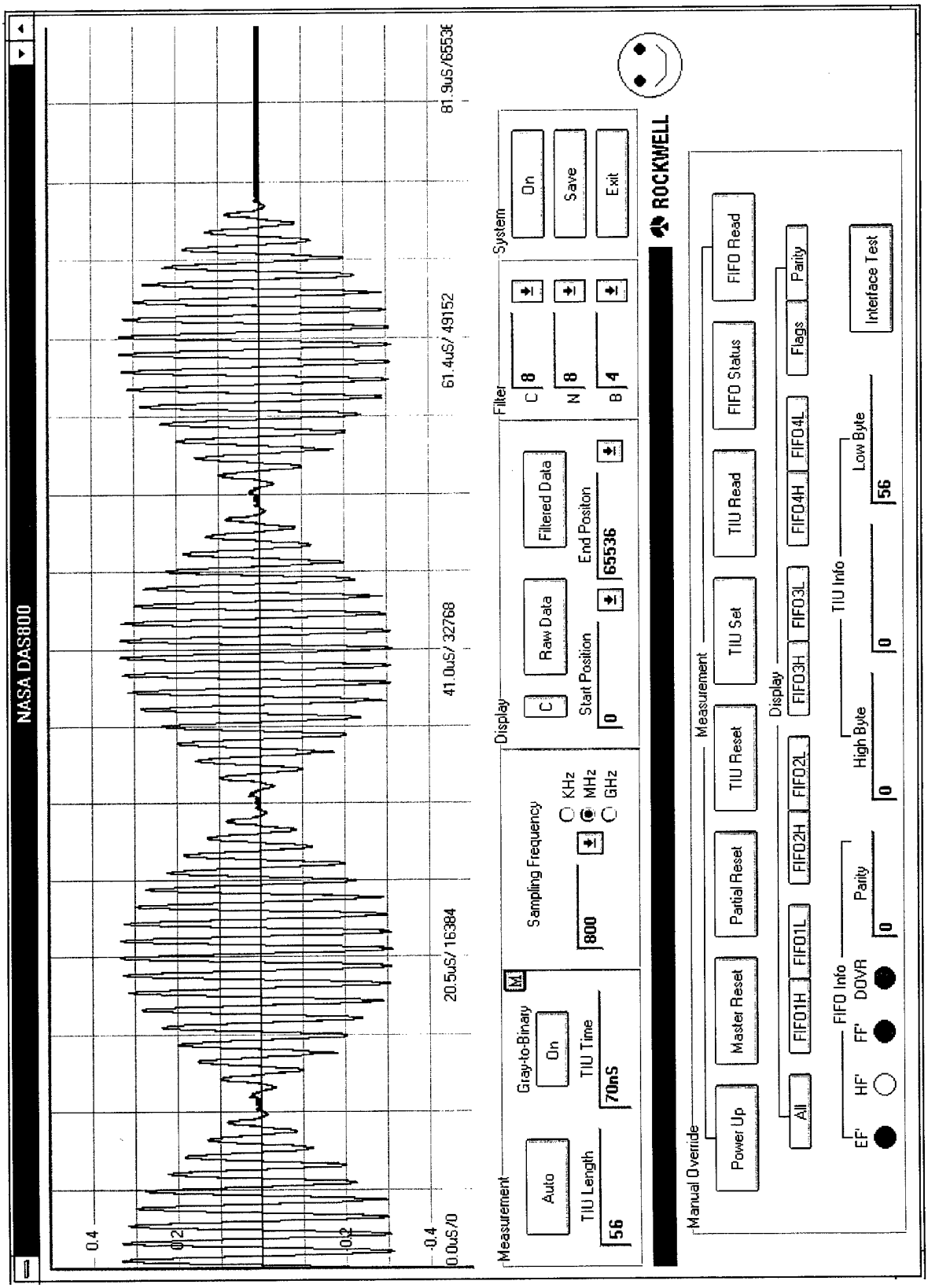


Figure 2.4-2: Advance Control Panel added to the Main Control Panel with the click of the "M" button in the measurement group.

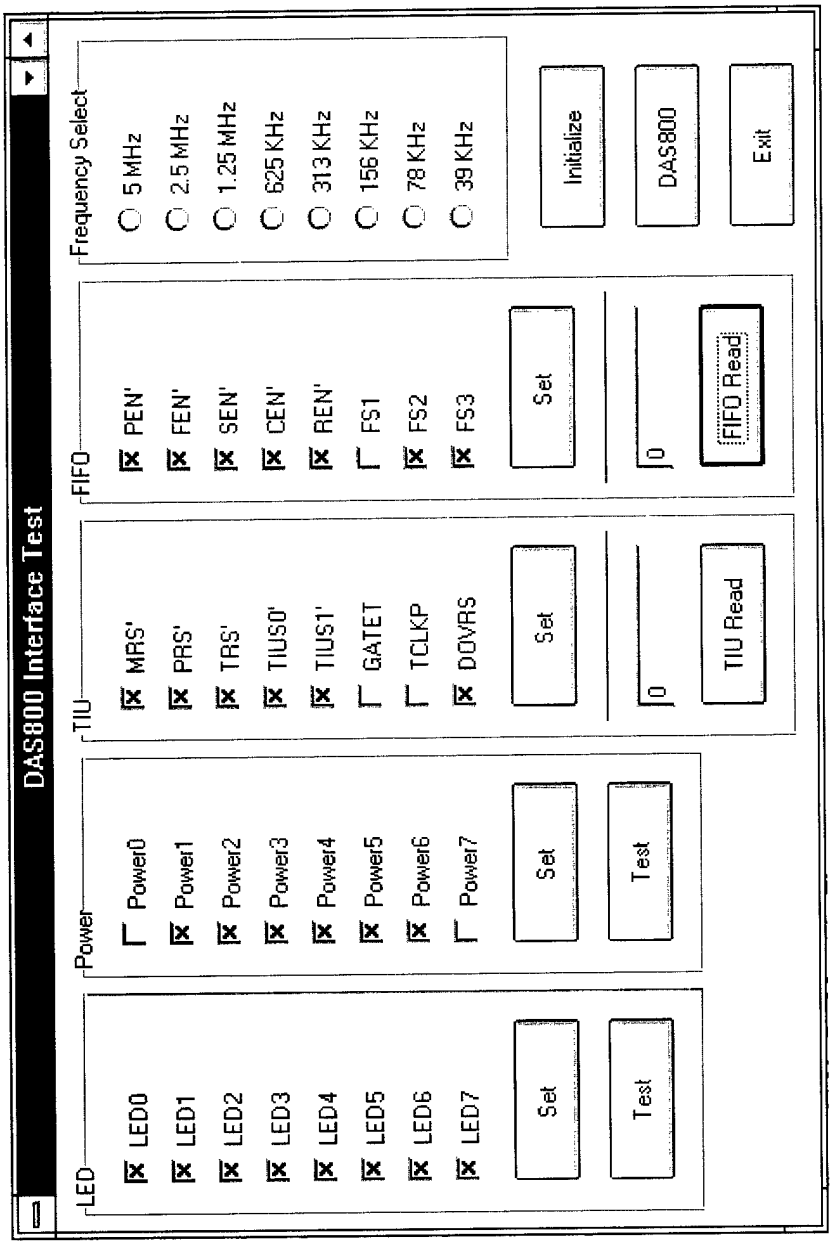


Figure 2.4-3: The Interface Test Panel selected from the Advance Control Panel by clicking the "Interface Test" button.

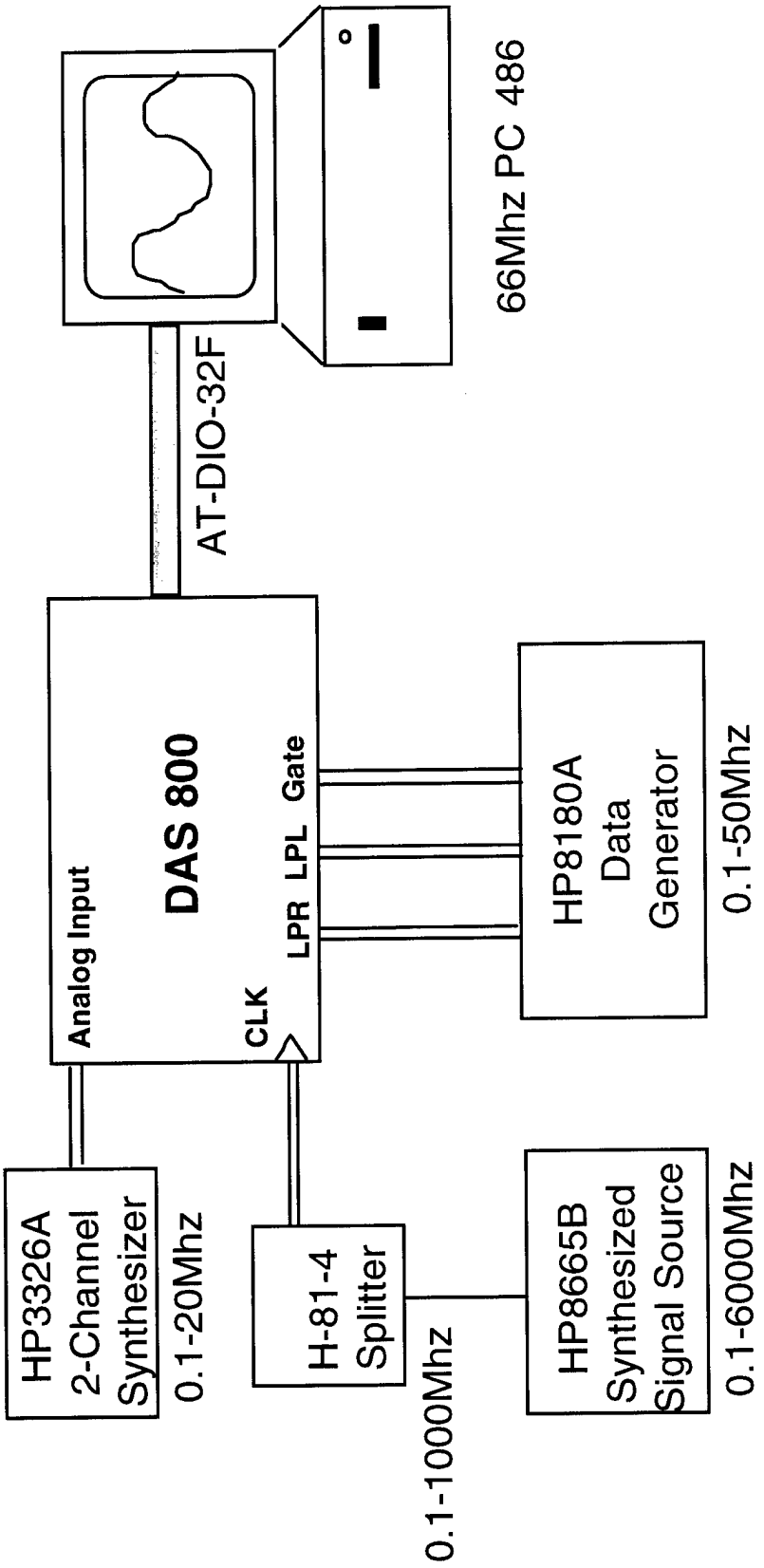


Figure 2.5.1: DAS 800 Test Setup

Figure 2.5-2: NASA DAS800 setup.

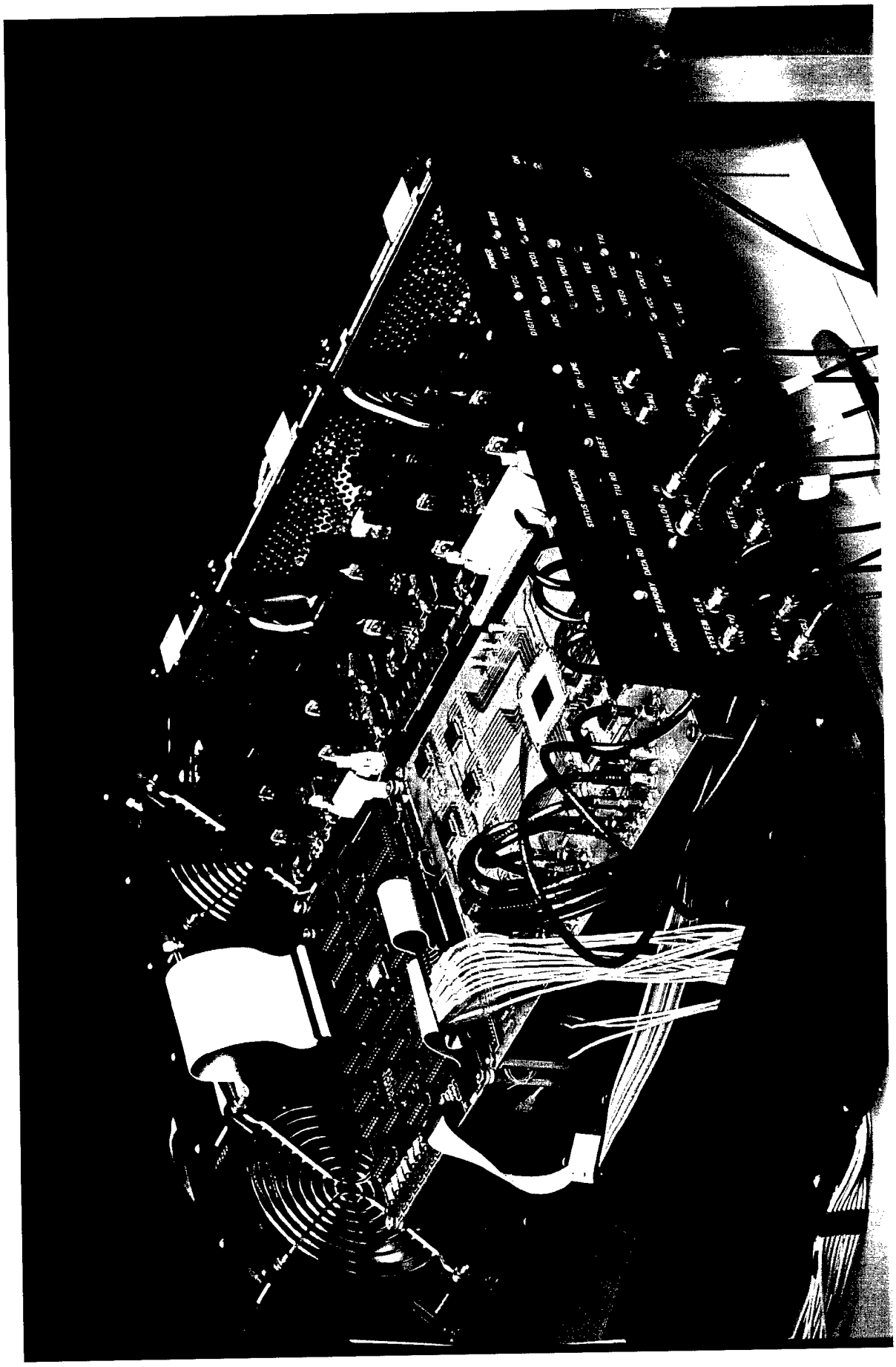


Figure 2.5-3: Diagnostic test of the NASA DAS800 close-up.

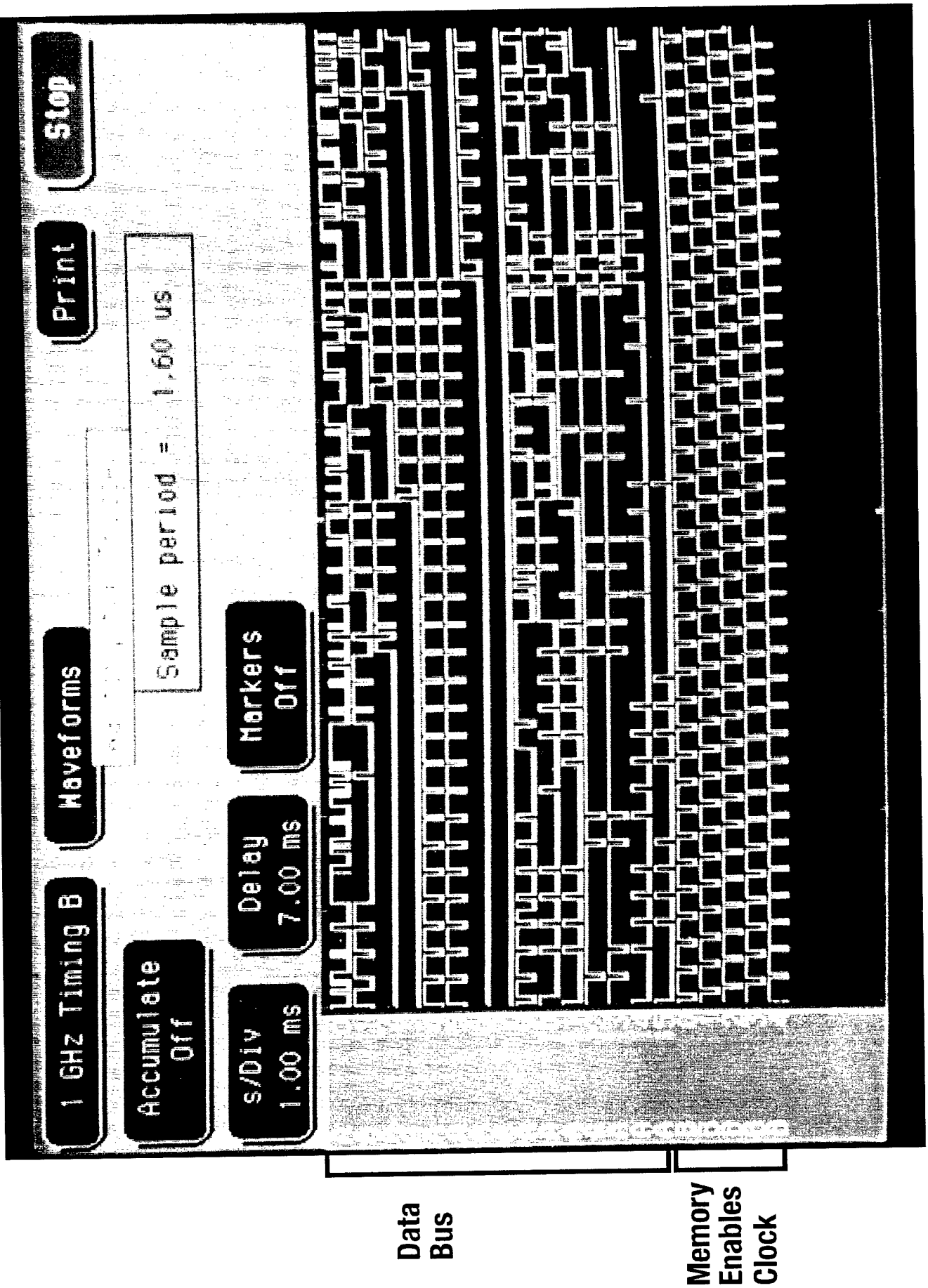


Figure 2.5-4: Clocks and data bus.

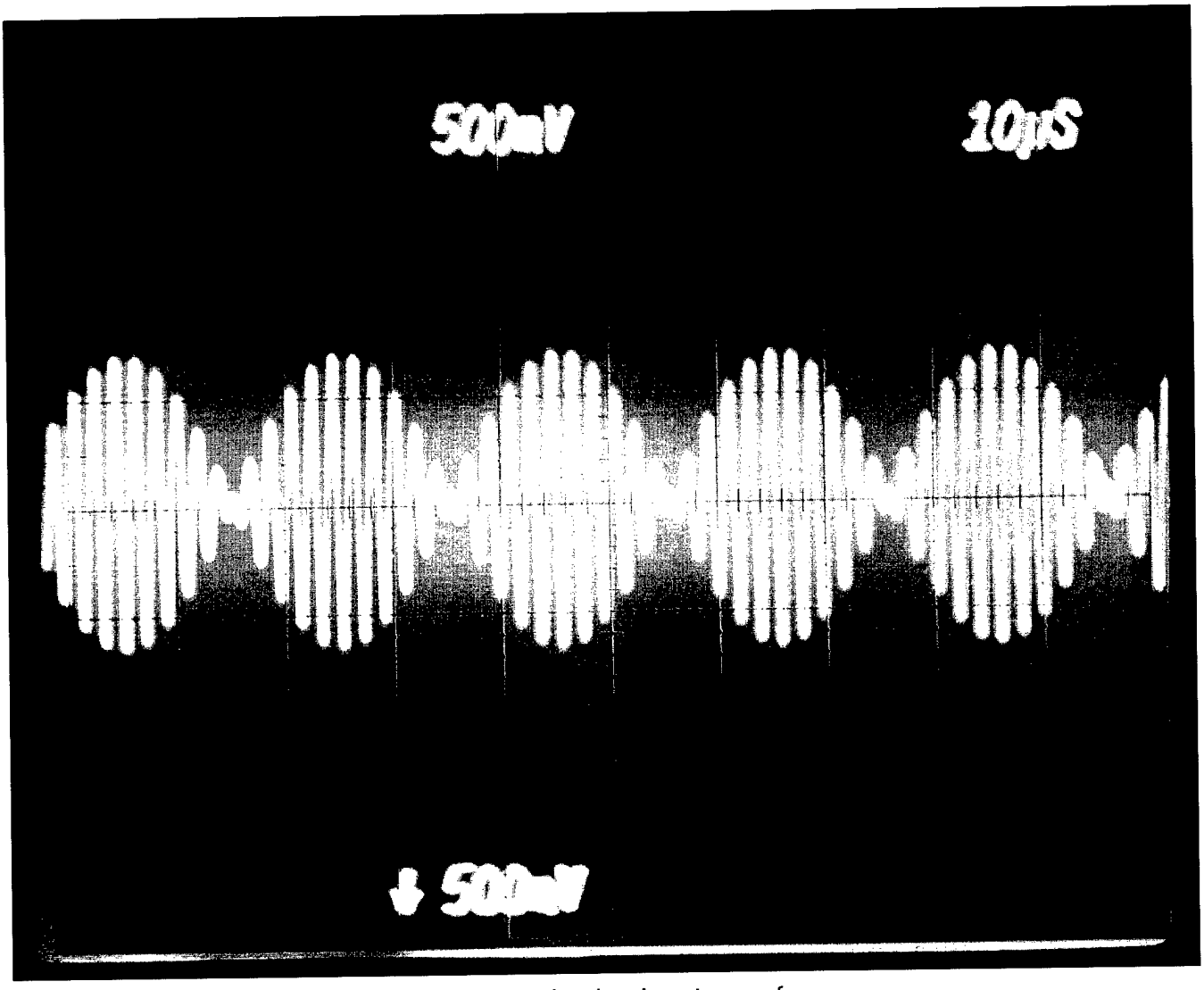


Figure 2.5-5: Analog input waveform.

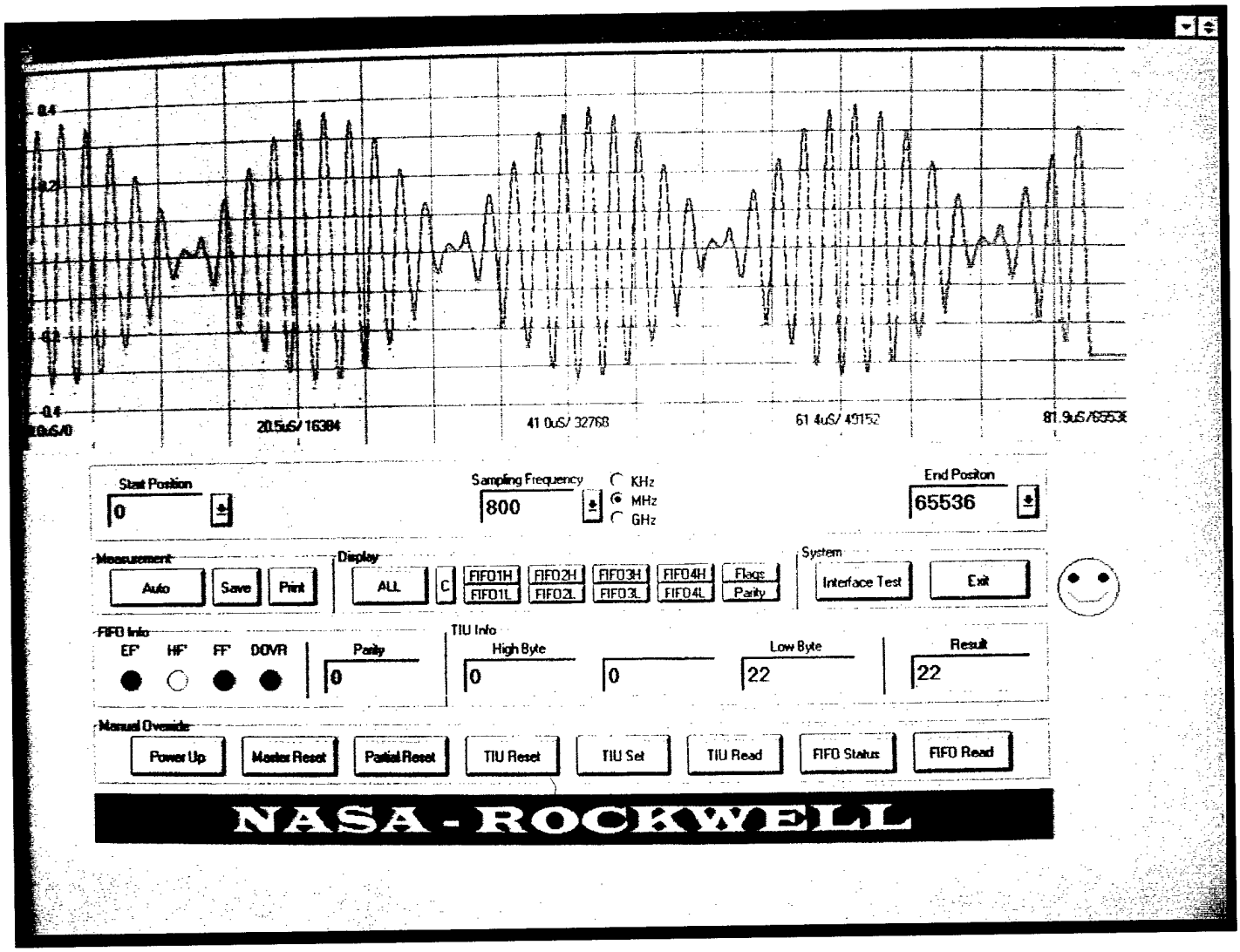


Figure 2.5-6: Captured analog input waveform

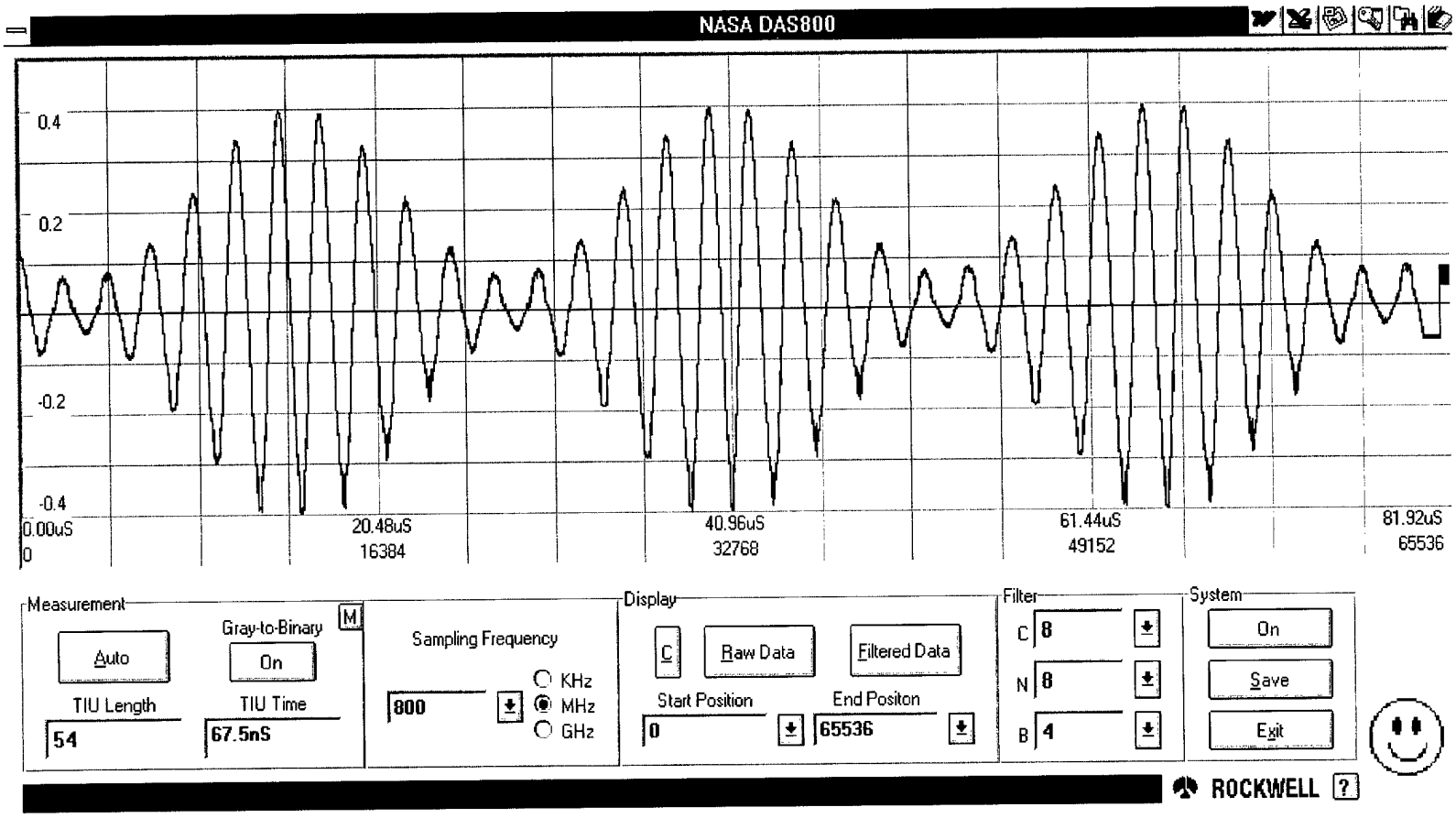


Fig.2.5.7 Captured Amplitude Modulated Waveform

Amplitude Modulation

F_{signal} = 40kHz Vpp=400mV $F_{carrier}$=400kHz Vpp=0.5V

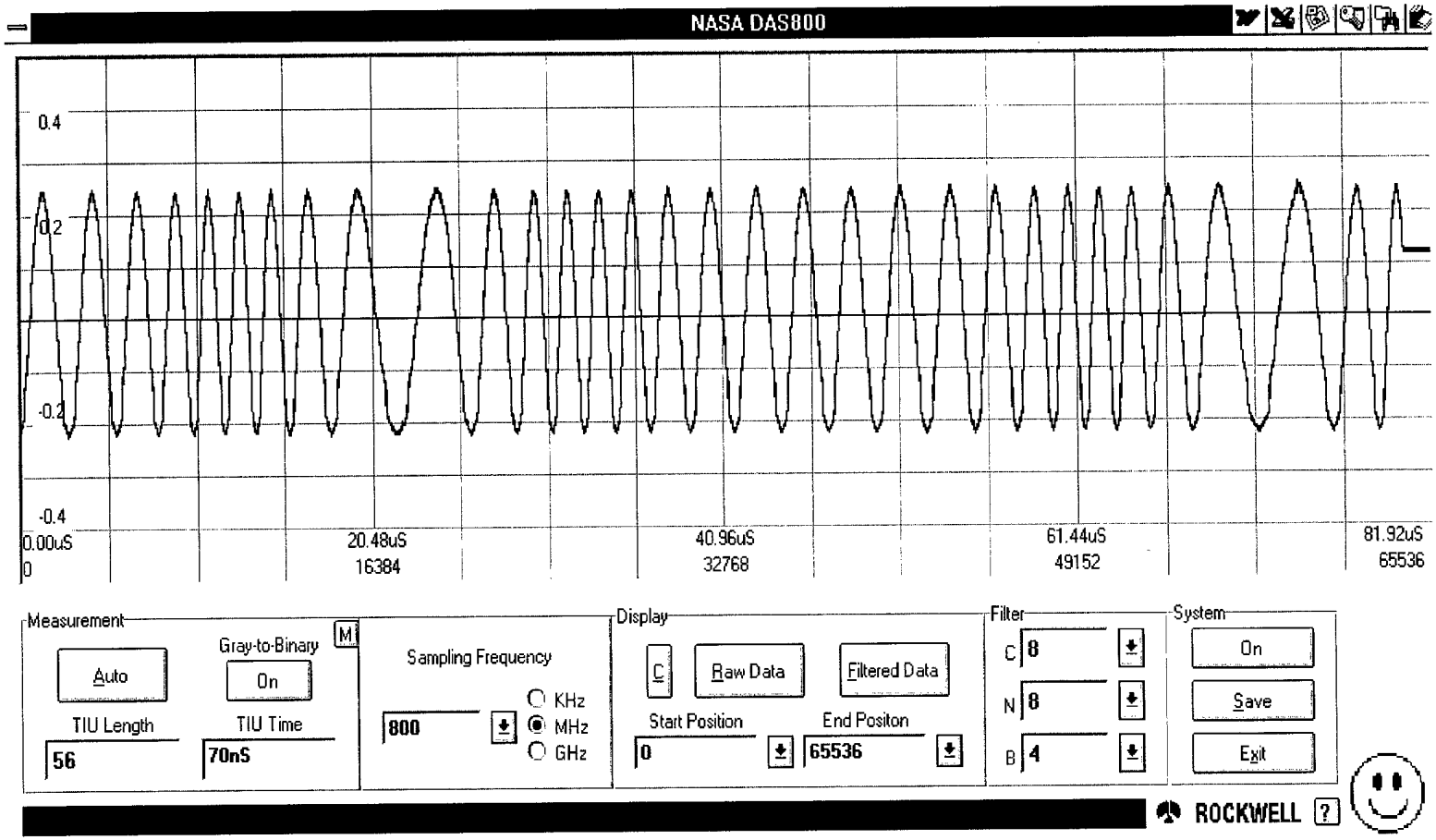


Fig.2.5.8 Captured Phase Modulated Waveform

Phase Modulation

F_{signal} = 40kHz Vpp=400mV $F_{carrier}$=400kHz Vpp=450mV

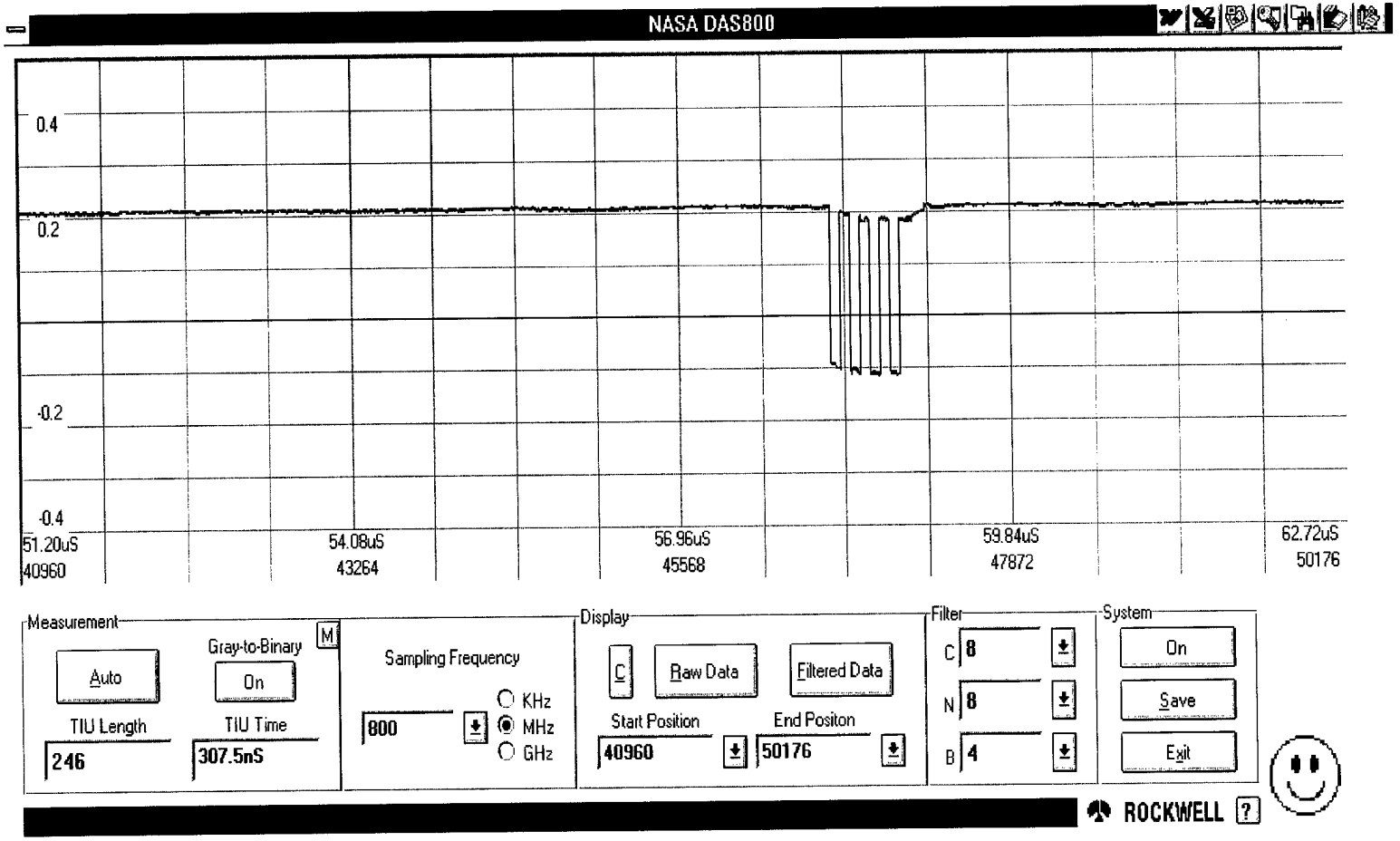


Fig.2.5.9 Captured Pulsed Square Wave

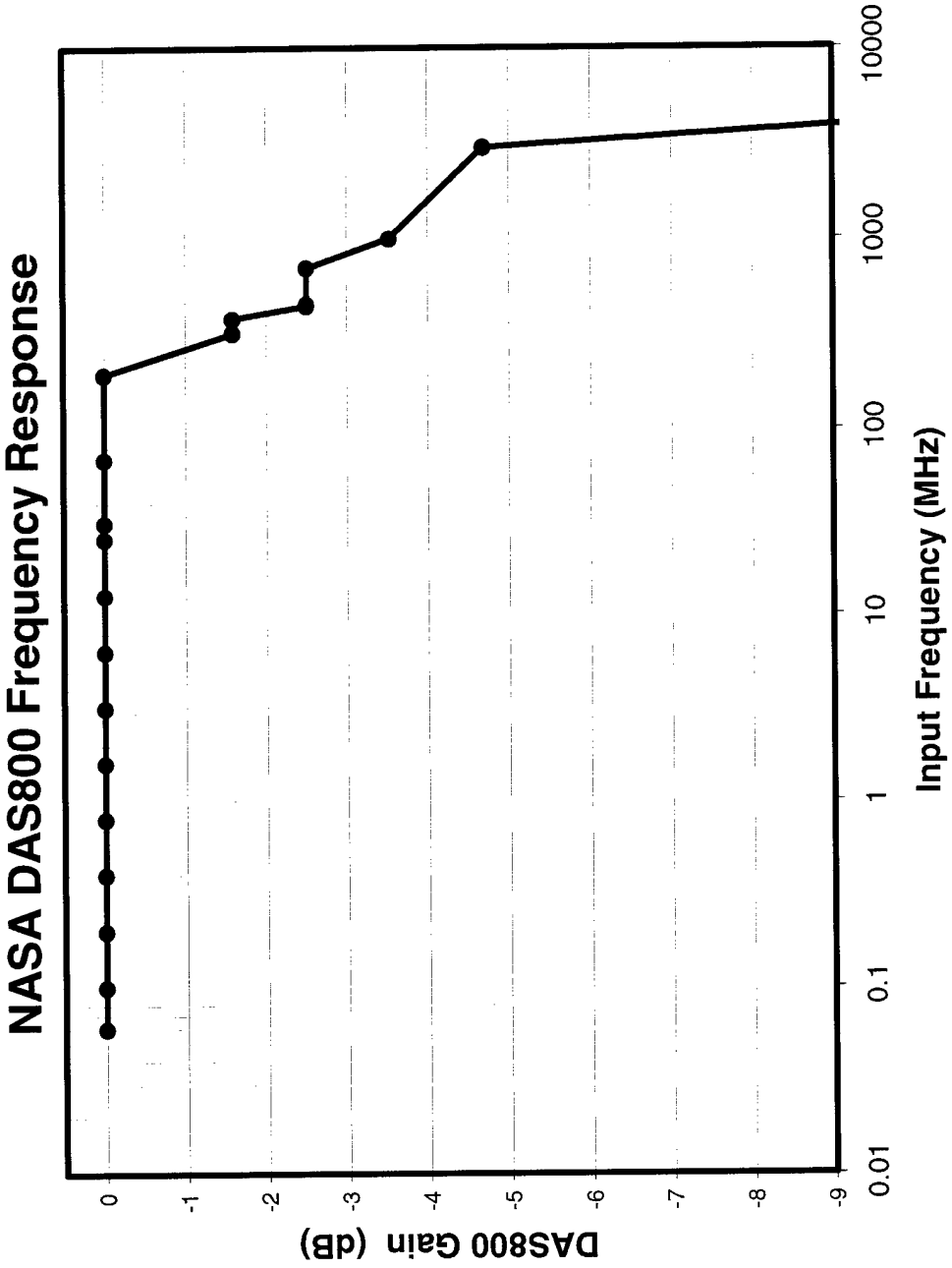


Figure 2.5-10: Full scale frequency response of the DAS800. The low frequency is limited by the test generator with a minimum frequency of 0.1 MHz. For this test, the sampling frequency is 800 MHz.