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Attention: Dr. Francis J. Kub
Subject: Monthly Progress Report - February 1997
Reference: SiGe Power HBT

Gentlemen:

1.0 Introduction

The objective of this program is the development and demonstration of a viable SiGe power HBT device design and associated processes that will demonstrate >1 Watt of output power at 6 and 8 GHz.

2.0 Objectives for the Reporting Period

2.1 Continued 6 GHz testing of unballasted BUR50 and SiGe2 devices at PHO using the new MNM capacitors.

2.2 Continued 6 GHz testing of unballasted SiGe2 devices at CR&D using the new MNM capacitors and begin testing of the BUR50 devices.

2.3 Begin processing run of SiGe2 and BUR50 lots using the new thin film ballasting mask sets.

2.4 Place order for polycrystalline silicon ballasting mask set for the SiGe2 device.

2.5 Perform additional testing at 1.88 GHz of the poly-emitter BUR50 devices in order to assess uniformity of DC and RF characteristics.

3.0 Progress During the Reporting Period

3.1 Additional testing was performed at PHO using the new MNM capacitors for internal package impedance matching. The Class-A device performance at VC = 5V is shown in Figure 1.

3.2 The SiGe2 devices continued to be evaluated at CR&D through February. Through improved impedance matching techniques, excellent results were achieved at 6 GHz. In

Class-A common-base operation, the device achieved 12 dB of gain with a peak output power of 28 dBm and a PAE = 21% at Vc = 6 volts; reference Figure 2.

3.3 All photo-masks which will enable the incorporation of thin film NiCr ballast resistors into both the SiGe2 and BUR50 designs were received on schedule in early February.

A new run start of both the SiGe2 and BUR50 design was started utilizing the NRL collector epitaxial design anticipating receipt of these thin film metal ballast masks. These runs have progressed through LTO Deposition, EBC Photo & Etch, Polysilicon Emitter Deposition, Phosphorus Implant, Polysilicon Photo & Etch, Base Contact Photo, Base Contact Implant and are awaiting Final Emitter Activation and Base Width Adjustment. To date all in process key breakdown and PCM measurements are well within anticipated tolerances.

3.4 The design and layout for the alternate approach to adding ballasting to the SiGe2 design by forming the resistors out of polycrystalline silicon at very high temperatures and followed by the selective growth of the SiGe base was completed. Photo-masks for this design approach were ordered and delivery is expected by 3/10/97.

A process run in anticipation of the receipt of these masks has been initiated into the wafer fabrication line at BSO. This wafer run has completed Initial Oxidation and LPCVD Nitride Deposition and is awaiting masks for LOCOS Photo & Etch.

3.5 More of the SiGe2 devices were assembled at CR&D for 1.88 GHz common-emitter power measurements. Tuned for power output (Vc = 7 volts, Class-AB), the device performance shown in Figure 4 achieves Gp = 13 dB peak gain, P1dB = 29 dBm, and PAE (P1dB) = 40%; tuned for efficiency, the device achieves PAE = 52% at Po = 28 dBm. The PAE in this case is limited by the device gain; the collector efficiency being > 60%. More importantly, due to the high collector efficiency, under two-tone operation, the device performance shown in Figure 3 achieves a PAE = 37% at a peak-envelope-power (PEP) of 29 dBm (Po=29 dBm) and IM3 = 30 dBc which is a significant improvement over Si BJTs which achieve ~25% PAE at IM3 = 30 dBc. Current efforts are directed towards improving the common-emitter match to enhance the device gain and PAE.

5.0 Problems and Proposed Solutions

5.1 In order to try to improve the consistency of the contact resistance associated with the formation of the polysilicon emitter, a SiGe2 design wafer run has been initiated into the BSO fabrication line. This run utilizes the UHVCVD epitaxial system to deposit the

polysilicon layer. This run has completed all process steps up through Base Contact Implant and is awaiting Final Emitter Drive-in.

5.2 The design of SiGe3, which is a pizza mask approach aimed at establishing a design Library for SiGe power transistor structures has been initiated. It is anticipated that this device design and mask layout will be completed by the end of March 1997.

5.0 Objectives for the Next Reporting Period

5.1 Continuation of 6 GHz testing of unballasted BUR50 and/or SiGe2 devices at PHO.

5.2 Perform load-pull testing at CR&D of selected BUR50 and/or SiGe2 devices in PHO test fixture.

5.3 Perform common-emitter testing of SiGe2 devices at 1.88 GHz using improved impedance matching techniques for improved device gain and efficiency.

5.4 Continue processing of SiGe2 and BUR50 wafers for inclusion of thin film ballast resistors.

5.5 Continue processing of SiGe2 wafers for inclusion of polycrystalline silicon ballast resistors.

Respectfully,

M/A-COM Inc.

B.A. Ziegner
Sr. Principal Engineer

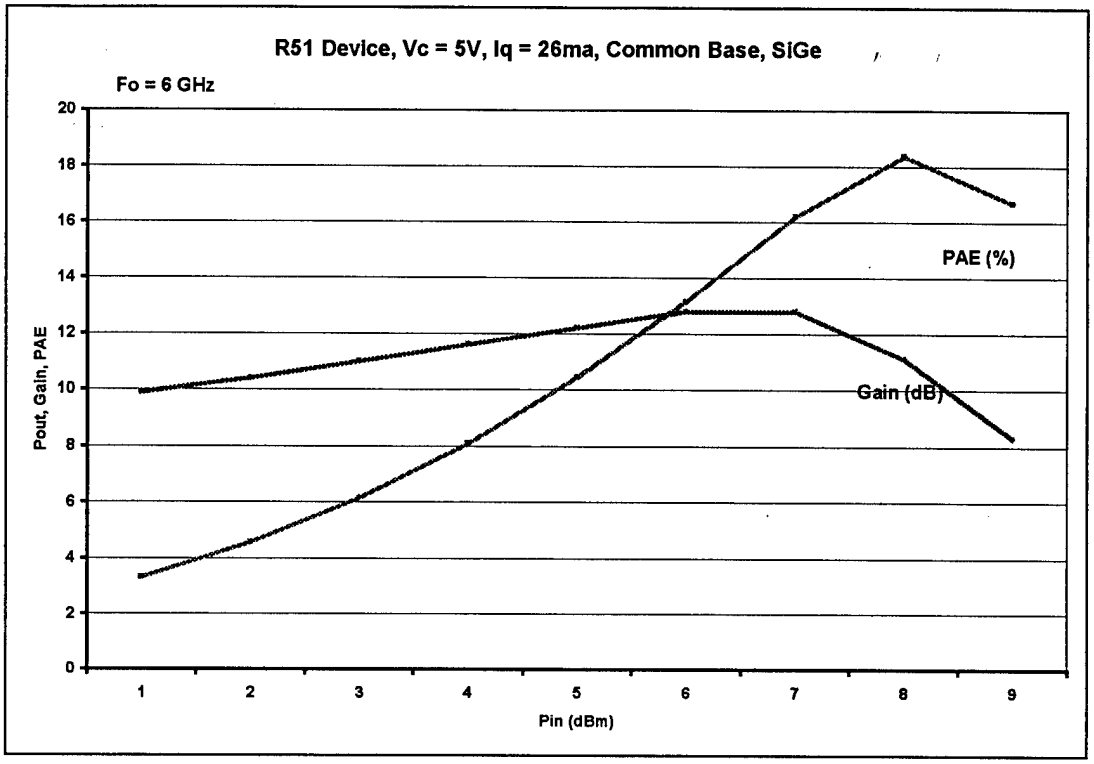

Figure 1 R51B Device Performance at Vc = 5V, Fo = 6 GHz

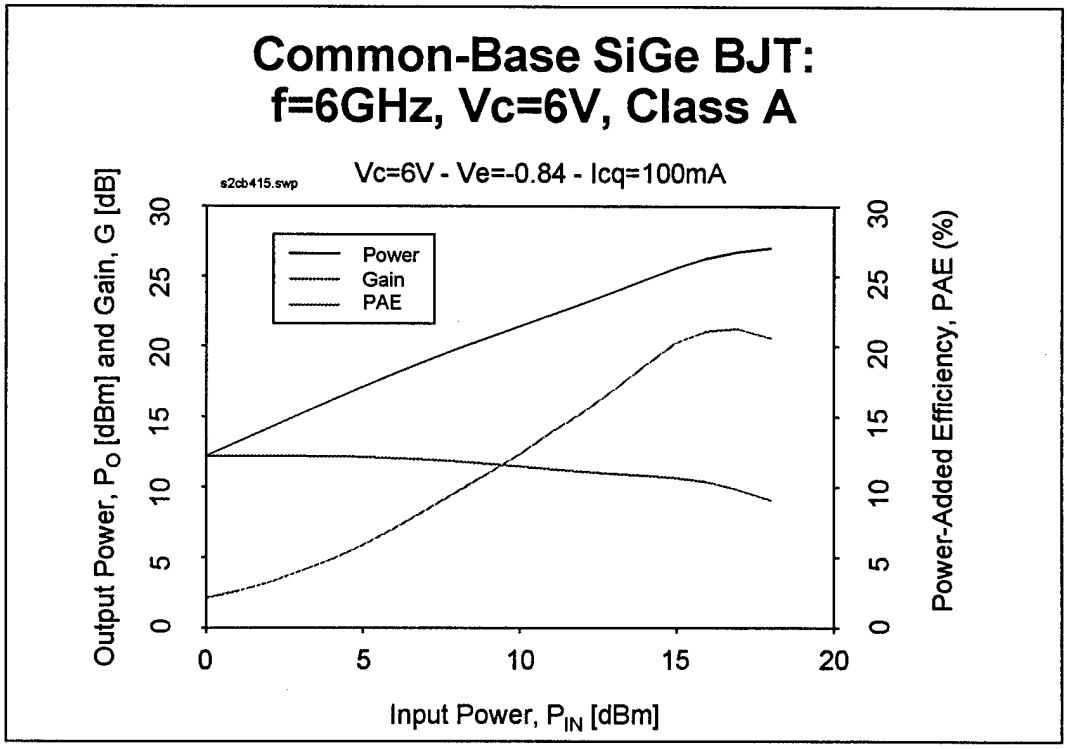

Figure 2 Sige2 Device Performance at Vc = 6V, Fo = 6 GHz

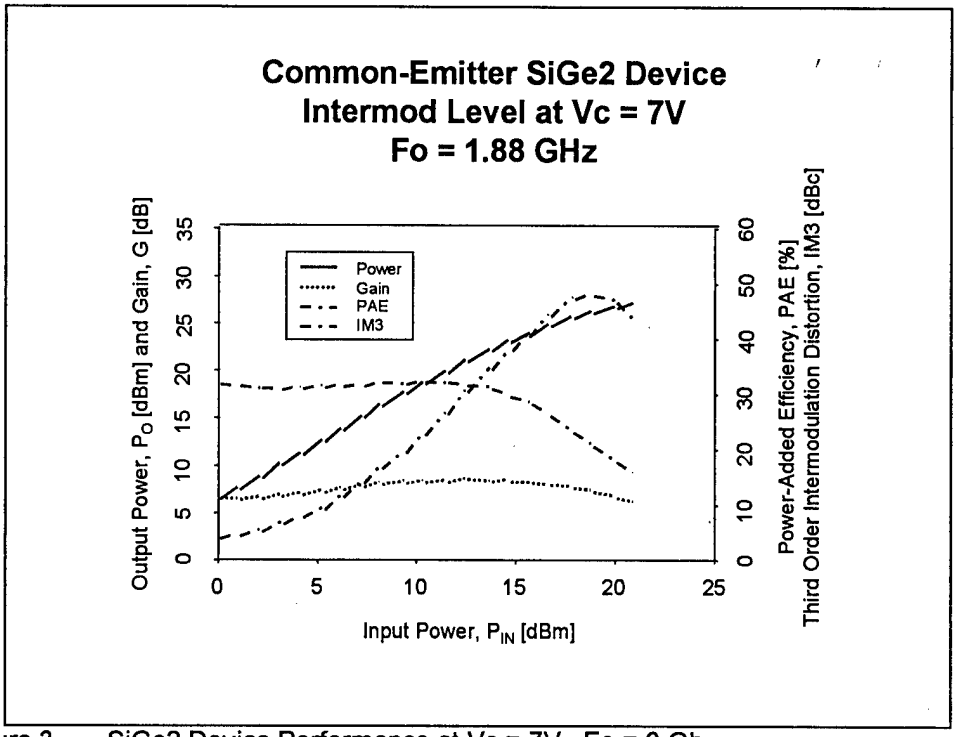

Figure 3 SiGe2 Device Performance at Vc = 7V, Fo = 6 Ghz

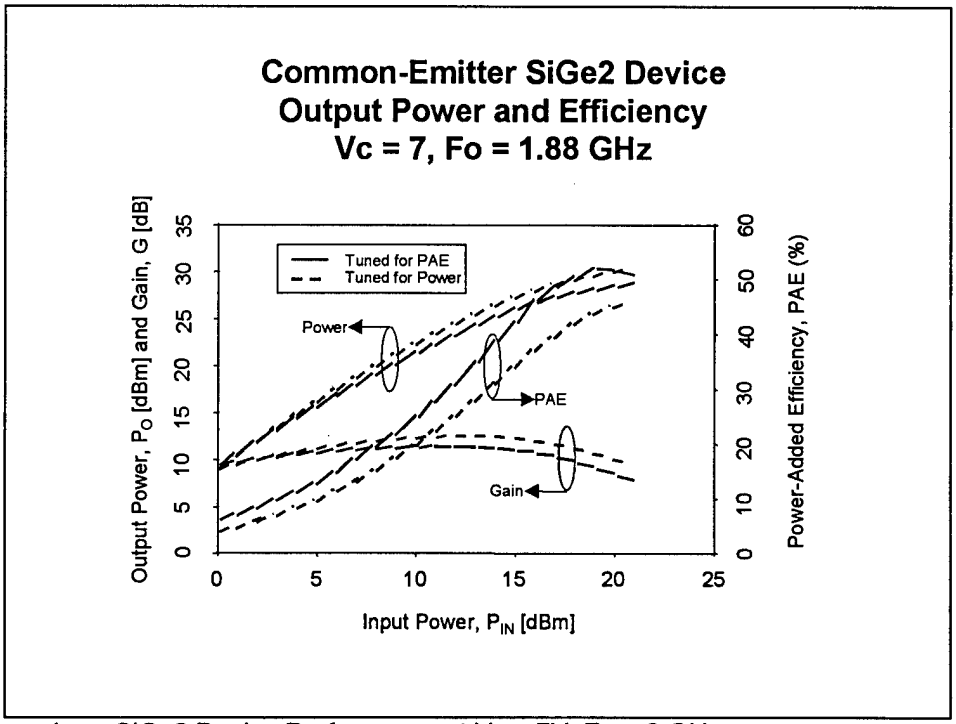

Figure 4 SiGe2 Device Performance at Vc = 7V, Fo = 6 GHz