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for an Industrial Phase-Locked Loop

by

Ryan J. Welch

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Chapter 1 Introduction

As the electronics industry aims for newer and better products, designers are pushing technology limits--smaller device sizes, lower supply voltages, and higher digital/analog integration -- while ensuring functionality. Many parasitic effects that were previously ignored can have dramatic effects on circuit operation. The problem of substrate coupling has become a significant consideration in advanced mixed-signal design[1][2]. Current injected into the common chip substrate from fast-switching digital circuits creates a less than optimal environment for precision analog circuits. Substrate current can cause latch-up leaving a circuit useless and causes device threshold voltages to rise which reduces the precision of analog circuitry.

Due to the time and monetary constraints of fabrication, detailed simulations are a must to ensure functionality and will help reduce the design life cycle. Many programs are available that can extract designed electrical elements from a layout and place them in a netlist. Such a netlist, with the proper device models, has been sufficient in the past to predict the circuit operation. In mixed-A/D design, this is no longer true. The major drawbacks to "device-extracted" simulations are that all substrate connections are at ideal voltages, resistance in interconnects is zero, and noise guarding strategies (guard bands, and physical separation) are not modeled, since the netlist provides only a list of devices and how they are connected.

Noise guarding strategies--low-impedance substrate guard structures, minority-carrier guard structures, and physical separation--do exist in physical layout. Data, via device simulations and silicon results, has shown the effectiveness of these different guard structures[3]. The problem is that these results are specific to one technology and one configuration. Noise reduction effectiveness depends on specific technology information (doping concentrations, junction depths, substrate type, etc.) and the physical location of layout features. Experiments on different guarding techniques have lead to general mixed-A/D design guidelines. Some of these common strategies include:

- use both low-impedance and minority carrier guard structures around analog devices.
- use substrate contacts liberally.
- physically separate digital circuitry from analog circuitry.

These guidelines usually are effective but conservative which can be costly in chip area.

As device sizes shrink allowing higher chip integration, the substrate coupling problem will only get worse. Analog precision becomes a difficult challenge when sensitive analog devices are placed on the same chip with many fast-switching digital devices. In order to manage substrate coupling effects, an accurate and efficient tool to predict these effects is desired by the mixed-A/D design community. Such a tool will allow designers to more accurately predict circuit performance, optimize circuit functionality within given constrains, and develop new and better guarding techniques. Without such a tool, it will be difficult for monolithic mixed signal designs to be aggressive in a business that is demanding better and faster products.

One class of mixed-A/D circuits whose performance would benefit from a substrate modeling tool is Phase-Locked Loops (PLLs). They are susceptible to substrate cross-talk due to sensitive analog circuits, many digital circuits, and high frequency oscillation. A case study on a PLL provided by National Semiconductor will be used as the subject to study substrate coupling. The most sensitive block of a PLL is the Voltage Controlled Oscillator (VCO) [1][4]which requires a quite substrate to produce low-jitter oscillation. Jitter refers to how much each cycle deviates from the ideal. Realistically, the VCO will be operating in a non-ideal substrate where small changes in the substrate bias can dramatically increase circuit jitter. The PLL to be analyzed in this work is used for clock generation. To maximize system speed, jitter should be accounted for to avoid timing errors. Thus, in aggressive designs, accurate PLL jitter must be determined before fabrication to determine system speed, which can only be done with the non-ideal substrate modeled in the circuit simulation.

1.1 Substrate Modeling Technique

1.1.1 Constraints

A tool that can accurately model the non-ideal substrate using reasonable memory and CPU requirements is not a trivial task. To accurately model a substrate, many different process features such as doping variations, well boundaries, ohmic contacts, buried layers, etc., must be considered. This problem becomes even more complex when the substrate is modeled in three dimensions. The challenge is to be able to model as large a substrate as possible while keeping the model accurate and not exceeding CPU or memory limitations. The earliest reported attempt at substrate modeling descretized the substrate into 3-D blocks that could all be stacked together to form a substrate mesh[5]. These blocks quickly added up giving hundreds of thousands of descretized elements. This was way beyond the capacity of any circuit simulator. Even though computer capabilities have increased dramatically, integrated circuit features have shrunk requiring a smaller descretized section, thus the need for simplified modeling techniques. Besides hardware limitations, a useful modeling tool must be compatible with the existing design framework. The model generation must come from existing design structures and the model must be consistent with simulator specifications. These constraints set the guidelines to create a useful tool for the CAD community.

1.1.2 SNAPPLE Approach

Many different techniques have been used to model the non-ideal substrate. Finite difference methods, such as [5] [6], have shown to discretize the mesh but the models become unrealistically large since mesh density does not correlate to device density. An elegant technique in [7] uses the boundary element method. This approach is good at keeping the model small, but it assumes that each substrate layer has the same conductivity, meaning device wells cannot be modeled. Other simplification techniques as shown in [3][8] create models through semi-empirical expressions from layout data and device simulations. These models become impractical as circuit sizes become large. All of the described techniques so far are not accurate and efficient for large circuits.

SNAPPLE (Substrate Noise Analysis Program with Post Layout Extraction) is a substrate coupling analysis tool that is accurate, efficient, and compatible with standard spice-like simulators. The non-ideal mesh is represented with discrete resistors and capacitors created through Voronoi Tessellation[9]. This is a finite difference technique that localizes the substrate discretization points(nodes) to relevant layout features such as MOSFETS, well edges, and ohmic contacts. Localizing substrate nodes dramatically decreases the substrate model size. Since nodes are smartly chosen at relevant layout features and not by some sort of gridding technique, nodes are not placed in unnecessary locations so a small shift in the layout geometry will not change the number of nodes chosen. One example in [9] compares a uniform grid technique and the Voronoi Tessellation technique for a 7 transistor circuit. Both techniques achieved the same accuracy while the uniform gridding technique had over thirty thousand RC elements and the Voronoi Tessellation technique had under three thousand elements. Unlike the boundary element and semi-empirical methods, this technique can accurately model a non-ideal substrate since all substrate features are included. Eventhough the Voronoi Tessellation method is a vast improvement over previous schemes, the size of the substrate model can get excessive as circuit sizes increase.

In order to make circuit simulation possible, SNAPPLE uses a RC reduction program on the substrate macromodel. Pole Analysis via Congruence Transform(PACT) [10]is a well conditioned algorithm that creates an approximation for the substrate model within a specified error tolerance and accurate up to a specified frequency. The resulting model is dramatically smaller than the original model while maintaining the circuit behavior at the ports. Unlike the Asymptotic Waveform Evaluation (AWE)[11] and Matrix Pade Via Lanczos (MPVL)[12], PACT is well conditioned and ensures stability. PACT was designed specifically for the reduction of substrate macromodels which consist of only resistors and capacitors. Once the reduction is completed, the circuit simulations using the substrate model will be possible without running out of memory.

With the development of accurate and efficient substrate model extraction and well-conditioned and passive RC reduction, substrate coupling analysis can be performed on much larger circuits than before (approximately 1000 transistors). Since RC reduction memory requirements scales super-linearly, the elegance of the model generation scheme determines the maximum circuit size. Eventhough SNAPPLE cannot handle state-of-the-art mixed A/D designs which can have 3-4 orders of magnitude more transistors than the maximum for this system, substrate coupling analysis simulations can be performed on sub-circuits that are suspected to contribute to substrate coupling. Additionally, small circuits can be studied to develope substrate coupling reduction techniques specific to a technology and layout style. Thus guarding strategies can be developed that move away from traditional heuristic guidelines.

1.1.3 SNAPPLE Architecture.

The entire SNAPPLE system is shown in Figure 1.1. The system requires two inputs, the GDSII layout data file and a technology file. The technology file is the heart of the SNAPPLE system. It contains all the information necessary to do the device and parasitic substrate extraction including: steam layer numbers, geometric directives to create the ideal netlist, doping concentrations, junction depths, ohmic contact definition, and substrate type. Each technology file is specific to a circuit's design and fabrication parameters. Without the proper technology file, the entire process does not work.

The program *str2edge* translates the GDSII file format into layer files that are used to create the netlist and substrate model. The resulting edge files are used by *topex* to create the ideal netlist. This is the spice-like netlist including all ideal circuit elements such as MOSFETS, diodes, resistors, BJTs, etc. The unique aspect of topex is that each node connection made to the substrate is assigned a unique node name. Circuit simulation could be done at this point without the substrate model by connecting the substrate nodes to the appropriate ideal bias. *Meshgen* is then called to create the non-ideal substrate model. This software uses edge files created from topex needed to create the substrate model. It creates a detailed, three-dimensional, RC model that attaches to the ideal substrate. Each unique substrate node in the netlist is matched up with the correct node

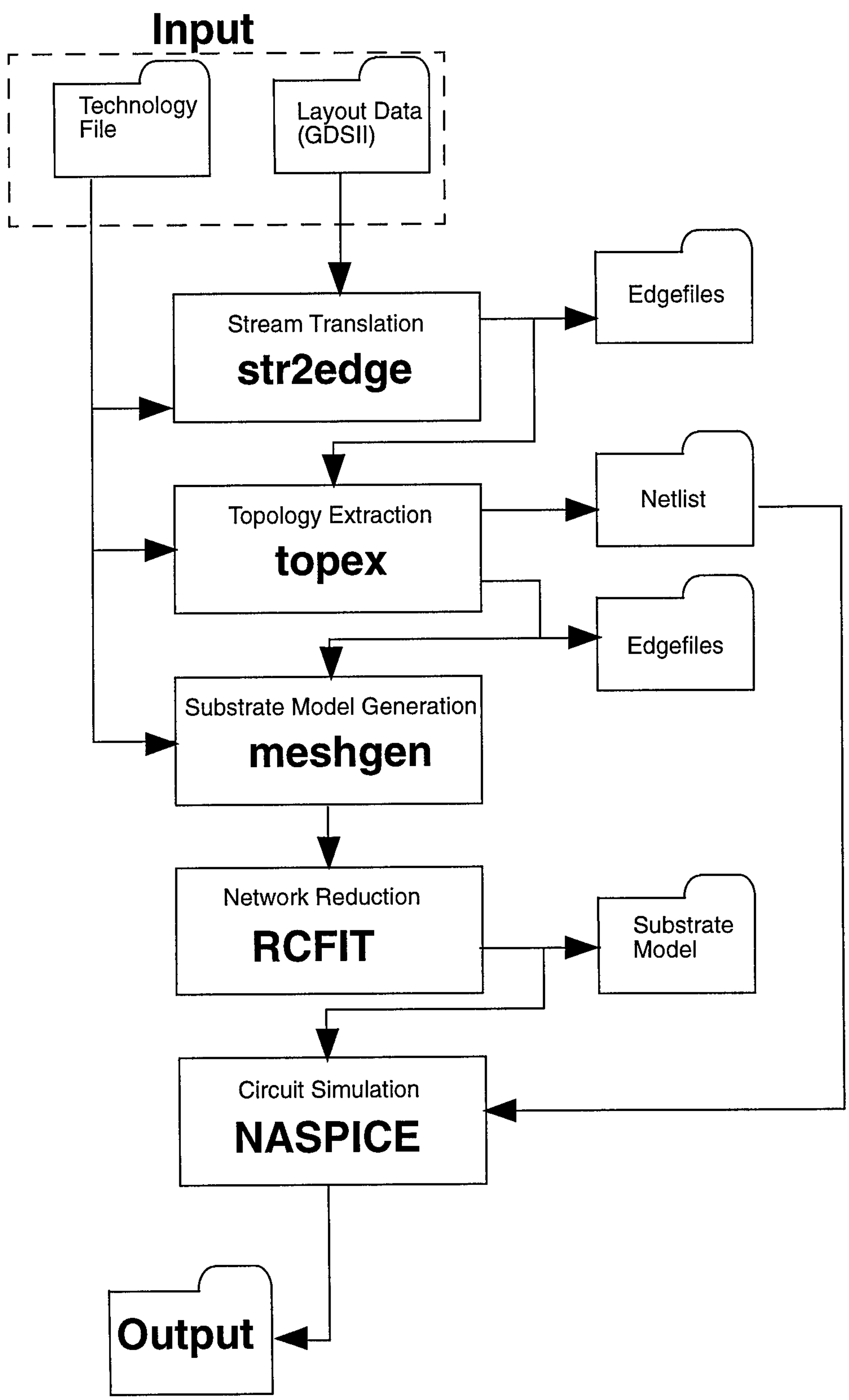


Figure 1.1 SNAPPLE System Flow

in the substrate model. Once the RC mesh has been created, it is reduced using *RCFIT.* Finally, the simplified substrate model is attached to the ideal netlist which is now ready for simulation. *NASPICE* is used as the simulator in order to support the device models from National Semiconductor, Inc.

When the entire process is done, only two files are necessary to run the substrate coupling analysis simulations, the device netlist and the non-ideal substrate model. The system is capable of producing many intermediate files used for debugging and information on each step in the system. Several small programs have resulted from the development of this system, but they are not significant in the entire system architecture.

1.1.4 SNAPPLE Example

The first silicon tests to verify the SNAPPLE system were conducted on simple experimental structures[13].The testing done preformed DC tests, to verify the modeling of the substrate resistivity, and AC tests, to verify the coupling effects through the substrate. The DC test cases tested the resistance along a stretch of bulk substrate and well implant material. For the well case, an average resistance of 3.614k was measured com-

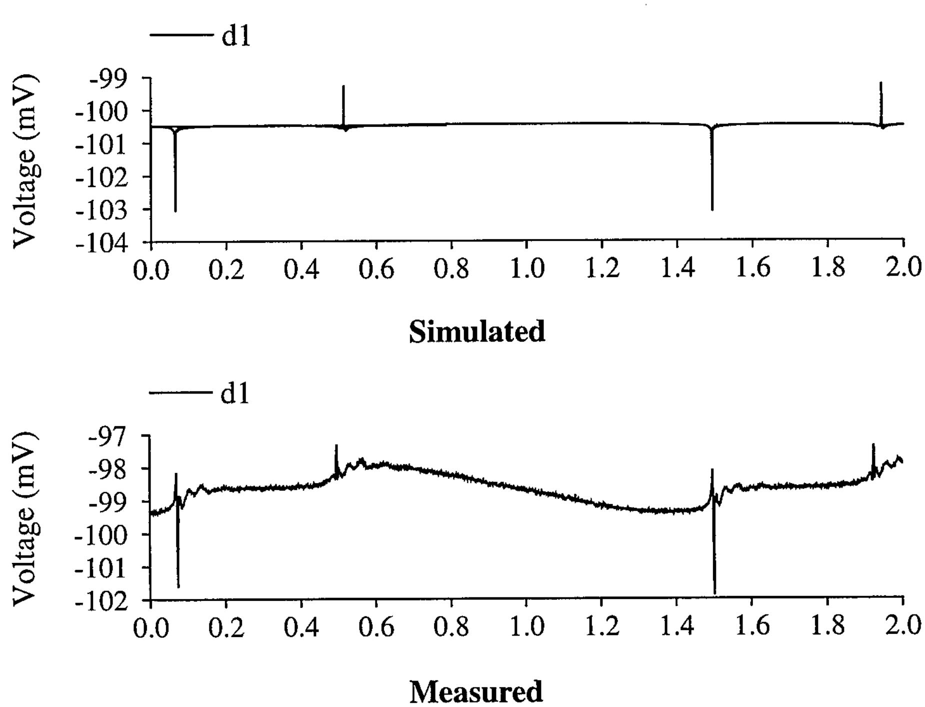


Figure 1.2 Simulated and Measured Results from a Simple Test Case

pared to 3.405k simulated. For the bulk case, an average resistance of 11.344k was measured compared to 9.5k simulated. The 5.8 and 16.3 percent error are not unreasonable since the simulation models depend on exact physical properties, such as doping concentrations and junction depth, which can easily vary in fabrication.

The AC test case consisted of a large inverter (noise injector) near a simple NMOS device (noise receptor). The NMOS device was externally configured to be a current source and its output voltage was monitored. Figure 1.2 shows that the transient simulation and measurement are reasonably close. Unlike the DC test cases, the AC test case has many interconnect parasitics to consider which are difficult to accurately and completely model. Eventhough all possible parasitics may not be modeled, the simulation results closely match the measured results.

Chapter 2 Substrate Coupling

2.1 Substrate Coupling Mechanisms

Since the common chip substrate in integrated circuit designs has a finite resistivity, any current flowing through the substrate will produce voltage fluctuations in device substrate connections. These connections are ideally held at the bias voltage. Substrate current is the mechanism for substrate coupling and the resulting voltage difference alters the operation of circuit devices. Current is injected into the substrate across parasitic capacitance according to equation (2.1) by switching voltage transients. The possible

$$I = C\frac{dv}{dt} \tag{2.1}$$

parasitic capacitances to the bulk substrate for MOS transistors are shown in Figure 2.1.

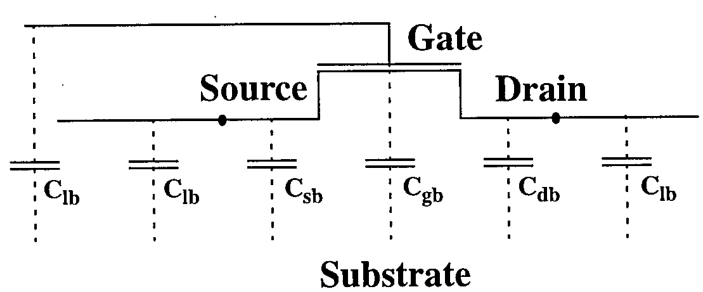


Figure 2.1 Parasitic Capacitance to the Substrate for a MOS Transistor

C_{gb} is the capacitance from the gate to the bulk from the gate oxide separating the gate and the channel of the device. C_{sb} and C_{db} are the capacitance from the source/drain diffusion regions to the bulk. These capacitance terms arise from the depletion region in a reverse biased diode. C_{lb} is the capacitance from the interconnect lines to the bulk since interconnect lines are separated from the substrate by a thick field oxide. Once the current is injected into the substrate, it leaves through low impedance ohmic contacts.

Since the substrate modeling system used does not model interconnect capacitance (C_{lb}), injected current will refer to only current injected across p-n junctions and gate capacitance (C_{sb}, C_{db}, C_{gb}). The capacitance from the gate to the bulk (C_{gb}) is identical to a parallel plate capacitor, given by (2.2). For a MOS device, A is the area of the gate

$$C_{pp} = \frac{A\varepsilon}{d} \tag{2.2}$$

area, e is the permittivity between the two plates which is the permittivity of silicon dioxide if built in silicon, and d is the separation of the plates which is the thickness of the silicon dioxide.

The capacitance from the source/drain diffusion areas to the substrate (C_{sb} and C_{db}) can be modeled as diodes. A generalized expression for reverse biased p-n junction capacitance is given by (2.3) where V_A is the bias across the p-n junction, V_{bi} is the built-

$$C_J = \frac{C_{J0}}{\left[1 - \frac{V_A}{V_{bi}}\right]^m} \tag{2.3}$$

in potential from the depletion region, m is a constant depending on the characteristics of the junction with typical values ranging from 0.3 (graded junction) to 0.5 (abrupt junction), and C_{J0} is the zero bias capacitance given by (2.4). K_s is the dielectric constant for silicon, ε_0 is the permittivity of free space, A is the area of the junction, q is the charge of

$$C_{J0} = \frac{k_s \varepsilon_0 A}{\left[\frac{2k_s\varepsilon_0}{q}(V_{bi})\frac{(N_A - N_D)}{N_A N_D}\right]^{0.5}} \tag{2.4}$$

an electron, N_A is the acceptor doping level, and N_D is the donor doping level. Many times this junction capacitance is expressed by (2.5) where A is the area of junction, P is the perimeter of the junction, C_{ja} is the junction capacitance per unit area of the bottom of

$$C_d = C_{ja} \times A + C_{jp} \times P \tag{2.5}$$

the junction, and C_{jp} is the junction capacitance per unit length of the periphery of the junction. This allows the bottom and sidewall capacitances of a diffusion region to be modeled as separate terms.

The current path, from injection across p-n junctions and gate capacitance to ohmic contacts, results in a potential difference in the common chip substrate. Substrate voltage fluctuation affects transistor operation by changing the threshold voltage(Vt) through the body effect. Vt, given by equation (2.6), describes the mode of operation (cut off, saturation, non-saturation) and is in the current equation for each of these regions for

$$V_t = V_{to} + \gamma\left(\sqrt{2\phi_b + |V_{sb}|} - \sqrt{2\phi_b}\right) \tag{2.6}$$

MOS devices. Thus a changing substrate bias ($|V_{sb}| > 0$) will have a significant effect on the operation of the devices built in that substrate.

This phenomenon becomes ever-so important in mixed signal designs. Fast switching digital devices inject substrate current that can be received by sensitive analog devices. Figure 2.2 shows a very simple situation where substrate coupling occurs. Note that the figure is **not** drawn to scale but more importantly shows generally how devices are built a substrate. The digital device is an inverter. Figure 2.2 only shows the NMOS device where Vinv would be some sort of switching signal to produce a switching signal at the drain. The analog device is a single NMOS current source which, in an ideal substrate, should provide a DC current as long as Vg is greater than the threshold voltage of the device. Figure 2.3 shows the effect on the output voltage (node between the resistor and the analog NMOS device) from a fast-switching input to the digital device.The fast-switching input to the inverter causes a fast-switching output at the drain of the NMOS device. The switching signal and the capacitance of the drain diffusion region inject current into the substrate. This current causes a voltage fluctuation at the substrate connection (Vb) of the analog device which causes the output to fluctuate from the body-bias effect. The shown example is a very simple case but hopefully shows what can happen in any

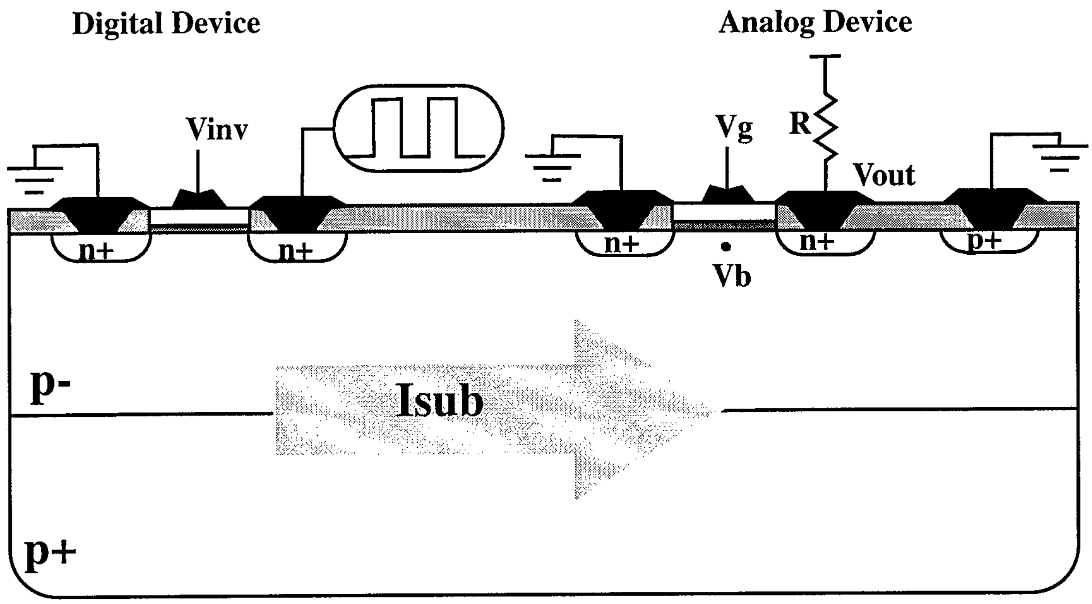


Figure 2.2. Simple Substrate Coupling Example

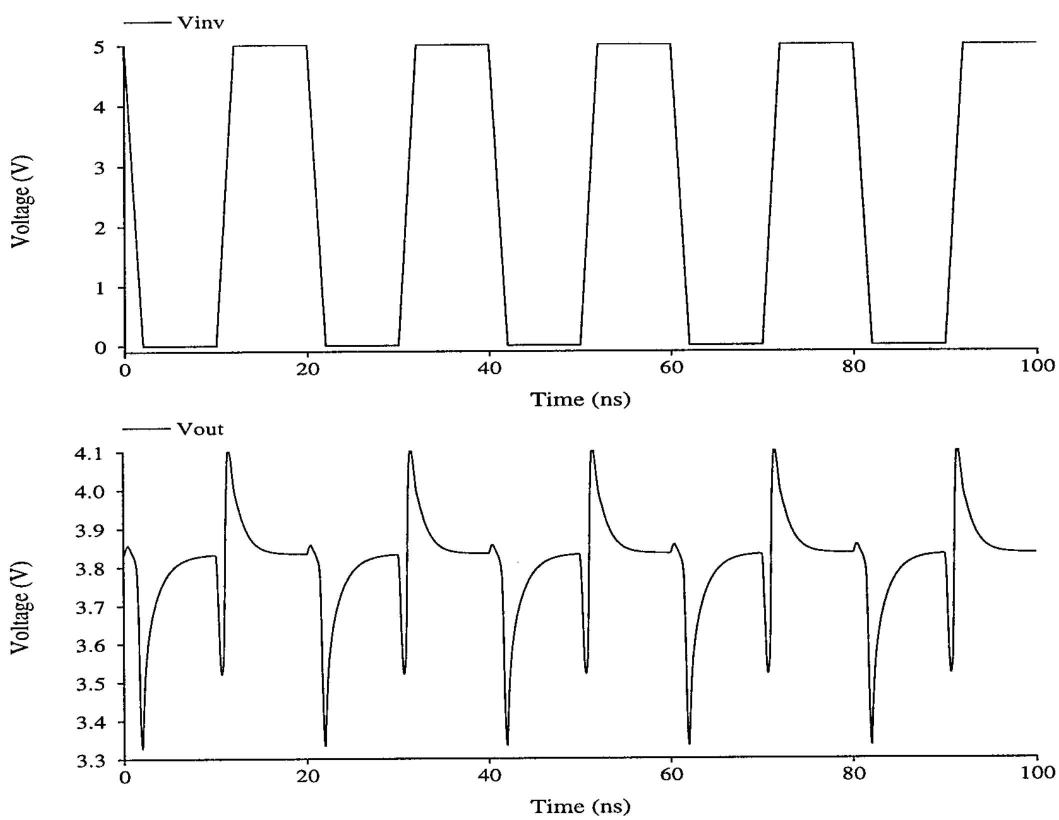


Figure 2.3. Noisy Digital Input and Sensitive Analog Output

design where digital and analog devices are fabricated on the same die.

2.2 General Substrate Coupling Reduction Techniques

The adverse effects of integrating digital and analog devices on the same die are common knowledge in the mixed signal design industry. Strategies to reduce parasitic interaction are commonly used today and are a must in aggressive designs. For example, ground bounce is a common problem in mixed signal designs. Fast switching digital devices draw large amounts of current which deteriorate the power supply biases to analog devices due to a finite resistance and pin inductance in the power lines. To minimize this effect, designers utilize separate power rails for digital and analog devices, filters to reduce ground bounce, and power-line insensitive analog designs. Ground bounce is a common problem with common fixes. It will be assumed from here that ground bounce reduction strategies are used in all instances in order to focus on substrate coupling.

The effectiveness of guarding techniques varies for the type of technology used, such as uniformly lightly-doped, heavily-doped epitaxial, or Silicon-On-Insulator(SOI) substrates. The results presented within are based on an epitaxial process, so substrate cross-talk reduction effectiveness will be based on such. Uniformly lightly-doped processes are much more common and are the basis for many guarding heuristics. Therefore, the differences between epitaxial and uniform substrates will be made clear in the guarding technique explanation.

Once the technology parameters have been fixed, designers have several techniques to help reduce the effects of substrate coupling including: substrate bias insensitive designs, physical separation, and guarding structures. Substrate bias insensitive designs are not trivial to create. This work does not present any new design techniques, but just acknowledges that it may be possible to implement a design style that is insensitive to substrate fluctuations. Changing a design style is not desirable to many people especially in mixed signal designs since this will be costly. Additionally, other simple yet effective coupling reduction techniques do exist that depend only on the physical layout of the circuit.

The first layout dependent substrate coupling reduction technique is physical separation. By placing the analog circuits as far away as possible from the digital circuits, substrate coupling can be reduced. In an epitaxial process, this technique has limited effectiveness. Figure 2.4 shows a simplified resistive model of what is happening in the substrate. For now, the assumption is made that the bulk substrate (p+) is modeled as one node. This assumption will be addressed later. FSN is the Fast Switching Node that injects current at V_i. All the shown examples will only show current injected at the source/drain region of a device. Repi is the resistance from an active diffusion to the bottom of the epitaxial layer which is dependent on the doping and the thickness of the epitaxial layer. R1, R2, and R3 all depend on the doping of the epitaxial layer as well as the physical separation in the layout. By varying d (R1), this effectively varies the distance between the analog and digital devices. As d gets large with respect to the epitaxial thickness (R1 >> Repi), substrate current will only couple from node Vi to node Vb through the bulk substrate(Repi) and not the epitaxial layer (R1). So when d gets large enough, the coupling from Vi to Vb will be independent of the physical separation between the devices since the coupling occurs through the bulk substrate (p+) and not the epitaxial layer (p-). [3] suggests that when the separation is 4 times the epitaxial thickness, the separation no longer is a factor.

For a uniform lightly-doped process, this is not the case as was again verified by [3]. Figure 2.5 shows how physical separation affects substrate coupling in this process Since the substrate now has a uniform doping, the resistive model simplifies. As d (R1)

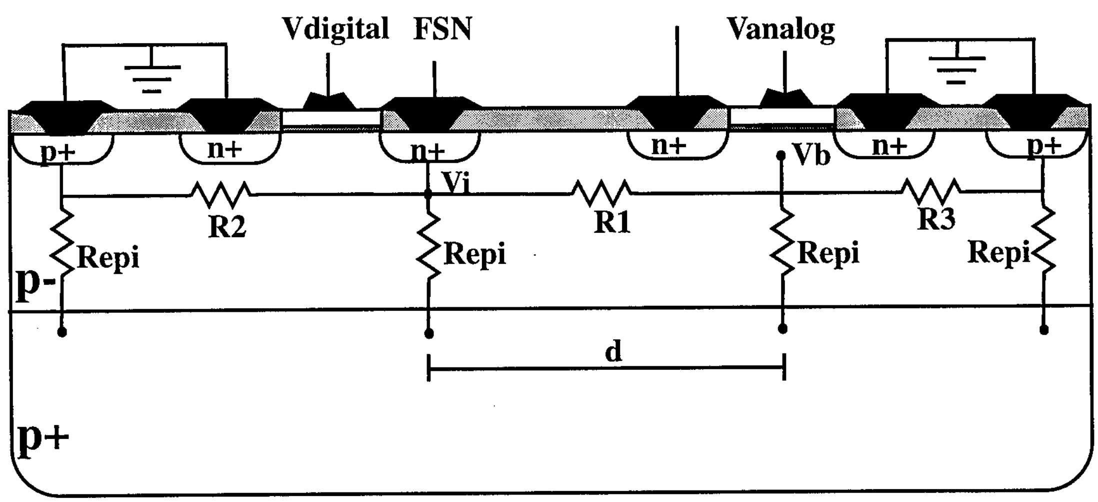


Figure 2.4. Proximity Effect in an Epitaxial Process

changes the substrate current does not have an alternate path and so a simple current divider is created. Since R2 and R3 do not change, as R1 gets larger, less current flows from node Vi to Vb and thus the voltage at Vb will decrease This reduction in the voltage at Vb will continue as d is increased to any value. As d gets larger, there are other lower impedance paths to ground that the current will follow and so the substrate fluctuation under the analog device will be lower.

The second layout dependent substrate coupling reduction technique is the use of guard structures placed between sensitive and noisy devices. These include low impedance ohmic guard structures (same type as the substrate) and minority carrier well guard structures (opposite type as the substrate). Their purpose is to prevent substrate current from reaching the sensitive devices. Since these two guarding structures are many times applied heuristically resulting from studies on uniformly doped substrates, it would be logical to discuss how they apply in this substrate and then contrast their effectiveness in an epitaxial substrate.

The ohmic guard structure gives substrate current a lower impedance path to the substrate bias with respect to the analog device. This is shown in Figure 2.6a. If the guard structure is placed in the path of the substrate current, the low impedance path is out through the ohmic guard ring (R2) rather that through the substrate to the analog device ohmic contact(R1 + R2 + R3). Please note that this resistive model is a very simplified view of a three dimensional resistive material.

The effect of a minority carrier guard well is to increase the impedance seen by the substrate current to the sensitive devices, Figure 2.6b. The well increases the substrate

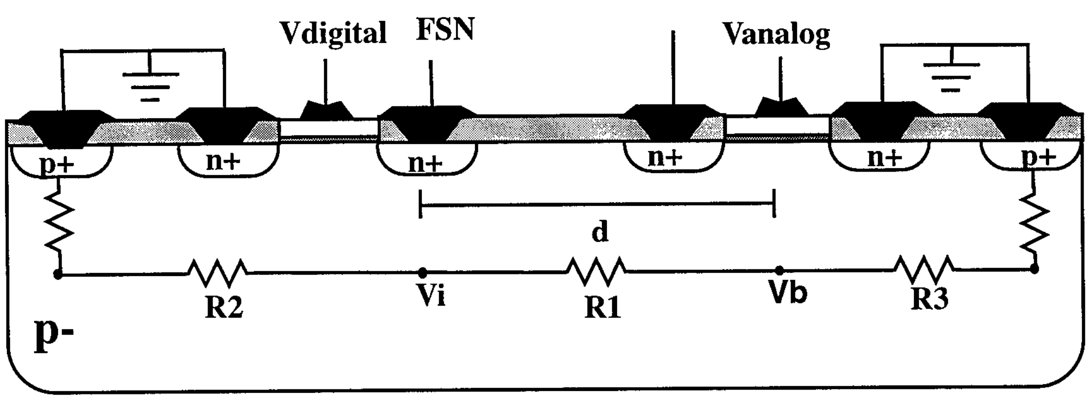


Figure 2.5. Proximity Effect in a Uniformly Doped Process

resistance by cutting a hole in any low impedance channel stop layer at the top of the substrate. This forces the current to flow underneath the well structure which is a longer path through the resistive substrate material. Comparing Figure 2.6a and Figure 2.6b, (R2' + Rwell + R1' + R3) is much greater than (R2 + R1 +R3). The well bias is arbitrary. If the well is biased opposite the substrate, the depletion region is larger causing current flow even deeper in the substrate. The drawback is that as the substrate fluctuates, there is a change in potential across the well depletion region which couples current across this junction. The junction will take away a small amount of current compared to ohmic con-

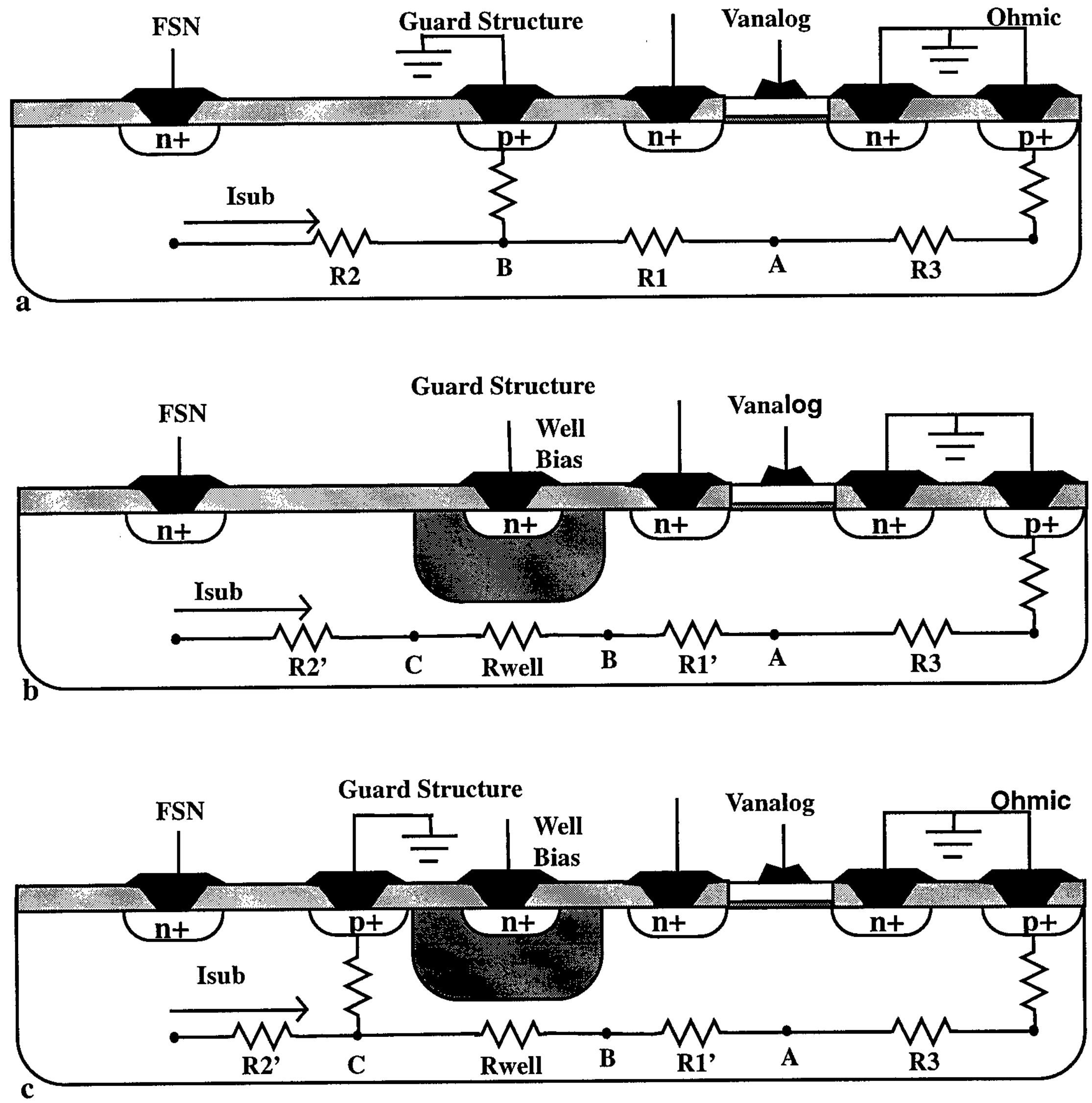


Figure 2.6a,b,c. Guard Structures in a Uniformly Doped Substrate

tacts which could potentially worsen any problem of ground bounce. Some designers leave the well unbiased so no current can couple through it. The current may not be pushed quite as far into the substrate, but no current will leave through the well diffusion.

When both of these structures are used together, they enhance the reduction of substrate coupling. Figure 2.6c shows how this happens. The ohmic guard structure acts to collect the substrate current while the guard well increases the resistance to the sensitive device. Now, the resistance to the analog circuitry is the same with just the well Figure 2.6b, but the ohmic contact gives the current a low impedance path to exit the substrate. The ohmic and the well guard structures both help to reduce substrate coupling but are more effective when used together. This is not the case with an epitaxial process.

When current is injected into the substrate in an epitaxial process, the current can flow through the highly resistive epitaxial layer or the less resistive bulk substrate. Since the bulk substrate is usually several orders of magnitude less resistive than the epitaxial layer, current is quickly drawn to the bulk substrate. The use of a well guard structure does very little in this process. The purpose of the well in a uniformly doped substrate was to push the current beneath the well. Due to the nature of the different resistive layers in an epitaxial substrate, current is already drawn to bulk substrate. Substrate current spreads easily once it reaches the bulk substrate layer so it is desirable to keep current out of the bulk substrate. The well guard structure only helps the current into the bulk and so is ineffectual in reducing substrate coupling in this process. This will be proven later with circuit simulations. Ohmic guard rings do help substrate coupling but there effect is highly layout dependent.

The effects of ohmic guard structures can be viewed from two stages: injection and reception. Injection describes how much current reaches the bulk substrate from capacitively coupling across fast switching nodes. Reception describes how the injected substrate noise affects the bulk voltage of sensitive devices.

When current is injected across a p-n junction, it effectively has two paths it can take as shown in Figure 2.7. It can flow through the epitaxial layer to a nearby ohmic contact (through R1) or it can flow down through the epitaxial layer to many other ohmic contacts (through R1 and Reff). Repi is a function of the epitaxial thickness while R1 is a function on the physical separation between the digital device and the ohmic contact. Reff is the parallel combination of all the Repi's in the layout determined by the number of ohmic contacts. When R1 >> Repi + Reff, the majority of current inject at node Vi will travel to the bulk substrate where the current can easily spread through out the entire chip. In order to reduce the amount of substrate coupling, current must be kept out of the bulk substrate. When R1 is small, meaning the ohmic contact is close to the digital device, more current will exit the substrate at node A through the epitaxial layer. Since current flowing in the epitaxial layer will only be for short distances, it will not couple into analog devices. Thus, the proximity of the ohmic contacts or guard structure should be as close as possible to the noisy digital devices to collect current before it gets dispersed through the bulk substrate.

One important phenomenon to recognize from this diagram is that as the number of ohmic contacts increases (Reff decreases) more current will be drawn into the bulk. The substrate current can flow through R1 or Repi + Reff. As Reff reduces, this produces a lower impedance path to the substrate bias than before. For example, with only one ohmic contact, Reff is Repi, but with 10 ohmic contacts, Reff is Repi/10. So an increased number of ohmic contacts will not help with the amount of current that reaches the bulk substrate.

It is impossible to keep all substrate current from entering the bulk, so there are two ways in which to reduce the amount of current that is coupled into the sensitive analog devices; reduce the resistance from the bulk to the substrate bias (Reff) or locally decouple

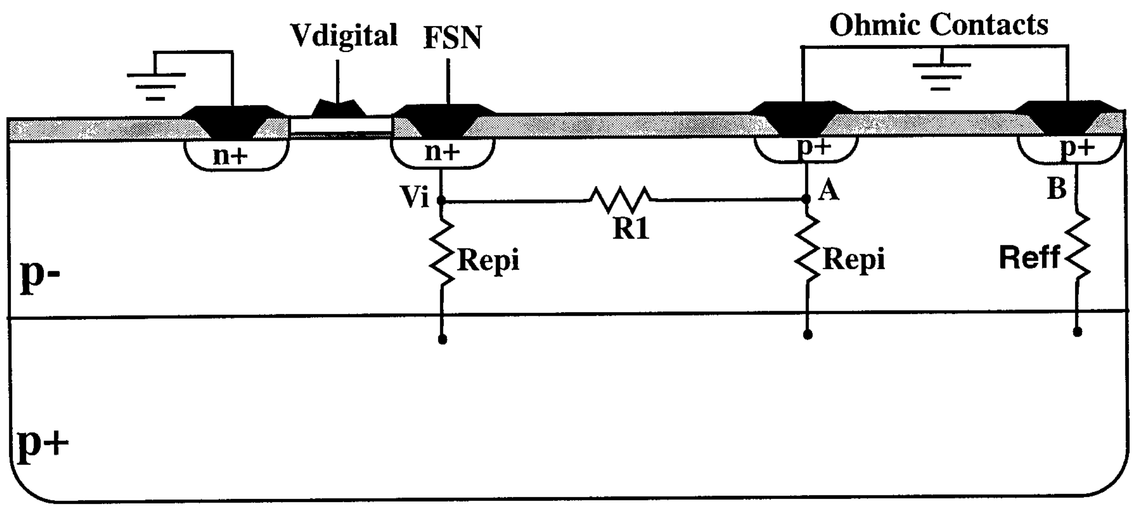


Figure 2.7. Epitaxial Substrate Noise Injection

the sensitive device from the bulk fluctuation, Figure 2.8. Lowering Reff will help the substrate coupling problem in the reception area, yet it was seen to be deleterious in the injection area. So what is better? It is in a designers best interest to keep Reff as low as possible to help in reducing noise reception but also to eliminate other adverse effects such as latch-up. If Reff were to approach zero, the current divider for the injected current in Figure 2.7 would be between R1 and Repi showing that some current would still leave through the epitaxial layer, but Vbulk in Figure 2.8 would be held at the substrate bias independent of the amount of current flowing in the substrate.

Reff is reduced by placing more ohmic contacts as described above. This gives the current more paths to leave the substrate, thus reducing the effective resistance from the bulk to the bulk bias. Reducing Reff reduces the amount of voltage fluctuation in the bulk substrate(Vbulk). The voltage fluctuation at the 4th node of a MOS device (node Vb) is a voltage divider between the Vbulk and near by ohmic contacts.So by reducing Reff, the amount of substrate current that can couple into the sensitive devices reduces.

Now, assuming Reff is fixed, there is another technique to reduce the amount of voltage fluctuation at node Vb. Again Repi is fixed by the epitaxial thickness, but R1 depends on the proximity of the ohmic contact to the sensitive devices. The voltage at node Vb is a simple voltage divider between Vbulk and the substrate bias through Repi and R1. By placing the ohmic contact as close as possible to the device, node Vb will be held closer to the substrate bias which locally de-couples the device from the bulk fluctua-

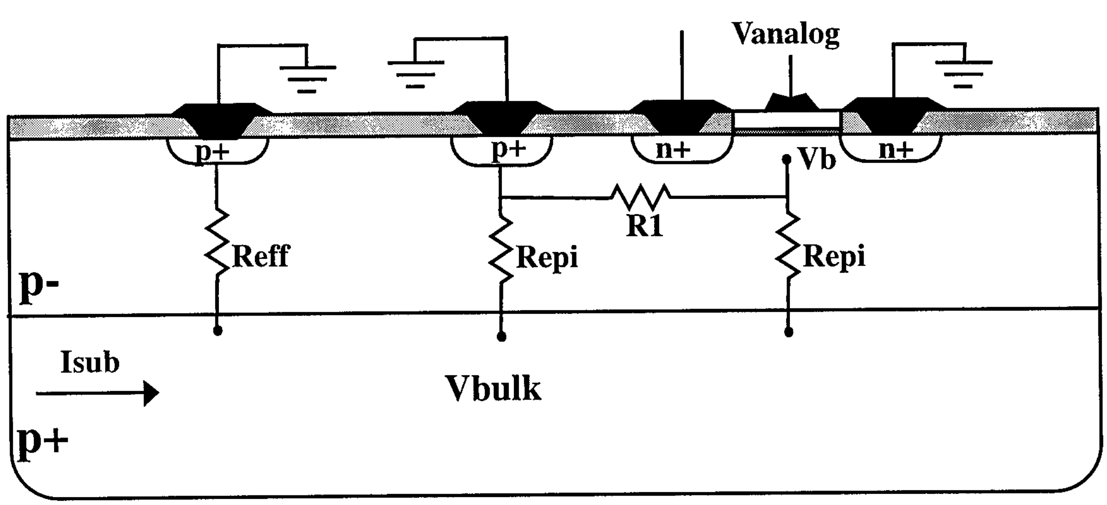


Figure 2.8. Epitaxial Substrate Noise Reception

tion. It is not possible to eliminate substrate current from coupling to analog devices since Reff and R1 will never be zero. By being liberal with ohmic contacts and paying special attention to the location of ohmic guard structures near analog devices, noise reception can be minimized.

2.3 Simulation Verification of Epitaxial Guarding Strategies

It has been shown in theory that several physical parameters--physical separation, proximity of ohmic guard structures, and number of ohmic contacts--can reduce the effects of substrate coupling. Before the actual PLL circuit is analyzed, a test circuit with different guarding configurations will be analyzed to show the effects of these different techniques. The test circuit used, Figure 2.9, is an inverter and a simple NMOS current source. This circuit was created with the same technology parameters as the industrial PLL. The inverter is left unloaded so the output waveform will be faster resulting in more noise injected into the substrate. It is driven by a 50 MHz square wave with 2ns rise and fall times. The analog NMOS device is driven with a DC voltage so that the device is turned on but not saturated so that the source of the device is not near zero potential. For these test simulations, Vin was set to 1.2 volts so the node between the NMOS device and the 1k resistor should be around 3.75 in a 5 volt process. Additionally, each device has one ohmic contact placed away from the center of the design (right of the digital device, left of the analog device). The measure of merit in these simulations is the peak-to-peak voltage fluctuation on the output of the analog device. For example, Figure 2.3 shows this output,

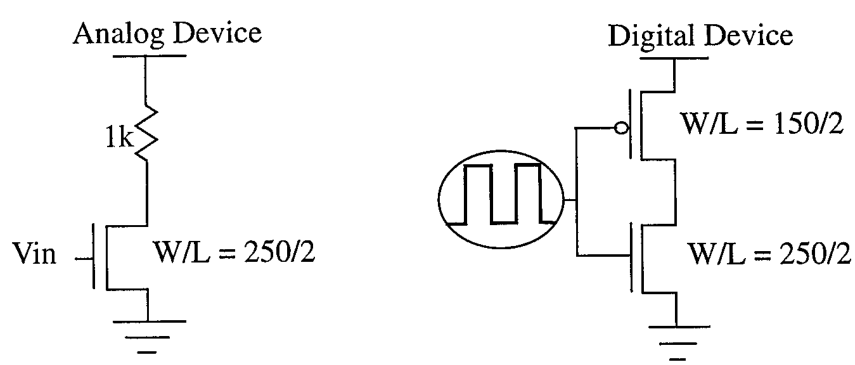


Figure 2.9. Simple Test Circuit to Test Epitaxial Guarding Strategies

resulting in approximately 800 mV fluctuation.

The first test simulation was to show the effects of the physical separation of the analog and digital circuits. This was tested by sweeping the analog device from the digital device (D=0) out to a distance of 100 microns. Figure 2.10 shows the results of these simulations. As the analog device gets further away from the digital device, the amount of coupling to the analog device levels off. The process used in this experiment has an epitaxial thickness of approximately six microns, so the physical separation of the devices becomes a factor in the amount of substrate coupling if the distance is less than four to five times the epitaxial thickness. This result is consistent with the findings in [3]. Figure 2.4 is an exact representation of what is happening in the silicon. As d (R1) gets large, a majority of the current that reaches the analog device couples through the bulk substrate, not the epitaxial layer. Thus beyond about 4 times the epitaxial thickness, the amount of substrate coupling is independent of the physical separation. Figure 2.10 is not a smooth curve as a result of the substrate discretization and the RC reduction approximation.

The next simulation was to show the effects of proximity of an ohmic guard structure to an analog and digital circuit. For these simulations, the analog and digital devices were set at 110 microns apart and an ohmic guard structure was swept from the analog device (D=0) to the digital device (D=110). Figure 2.11 shows the results of these simulations. When the guard band is near the analog device the substrate under the analog device is locally decoupled from the bulk substrate. Figure 2.12a shows the , percent sen-

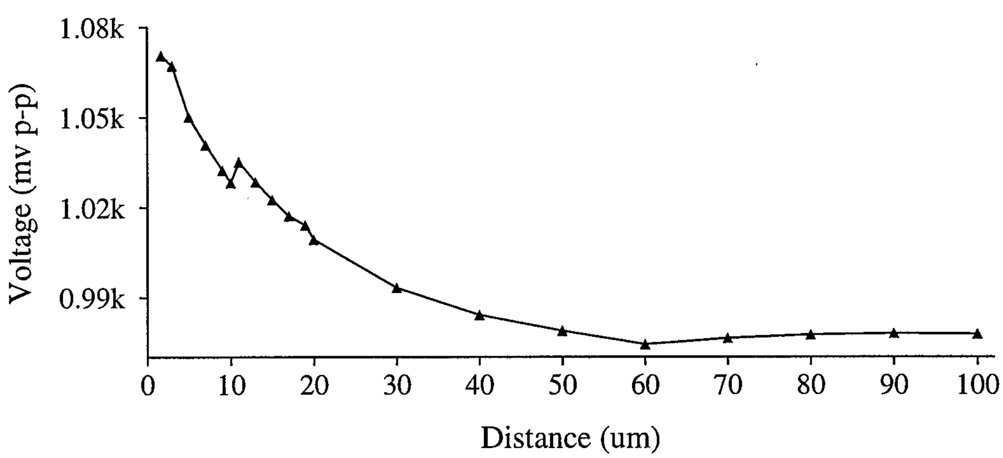


Figure 2.10. Effects of Physical Separation in an Epitaxial Process

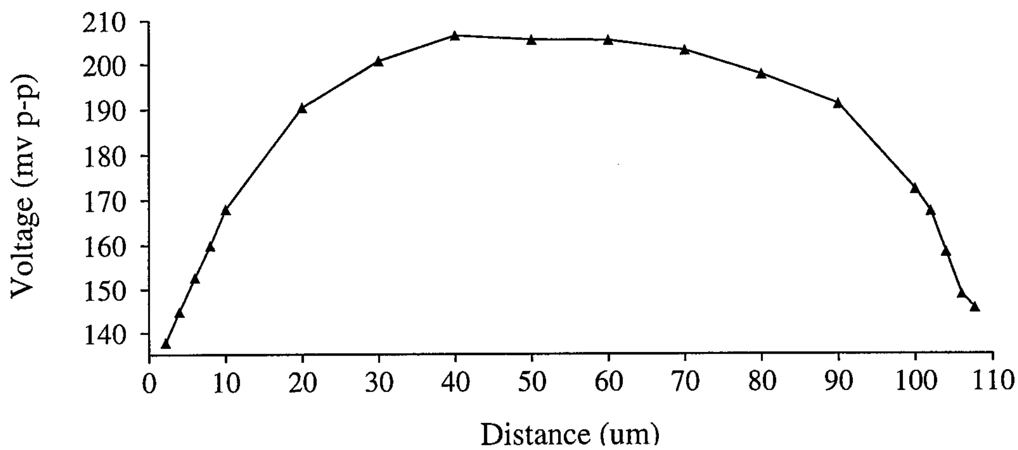


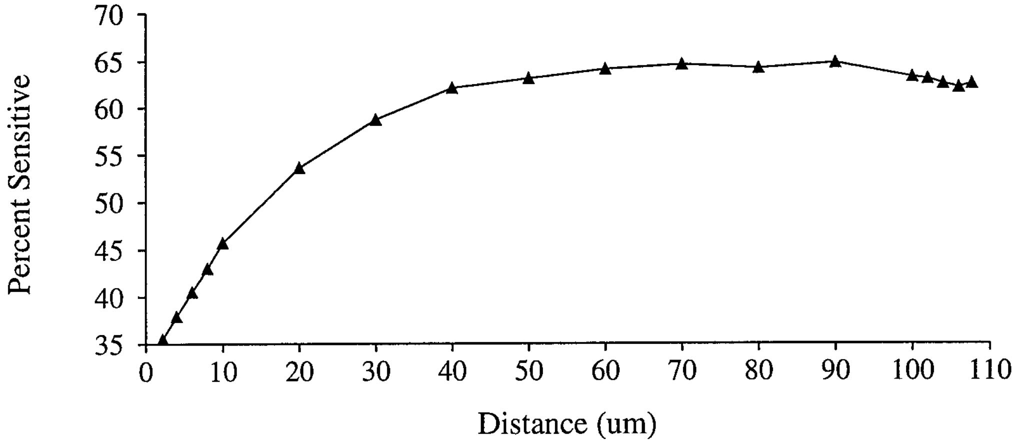
Figure 2.11. Effects of Guard Band Proximity in an Epitaxial Process

sitive of the analog device as given by equation (2.7).When the guard band is near the

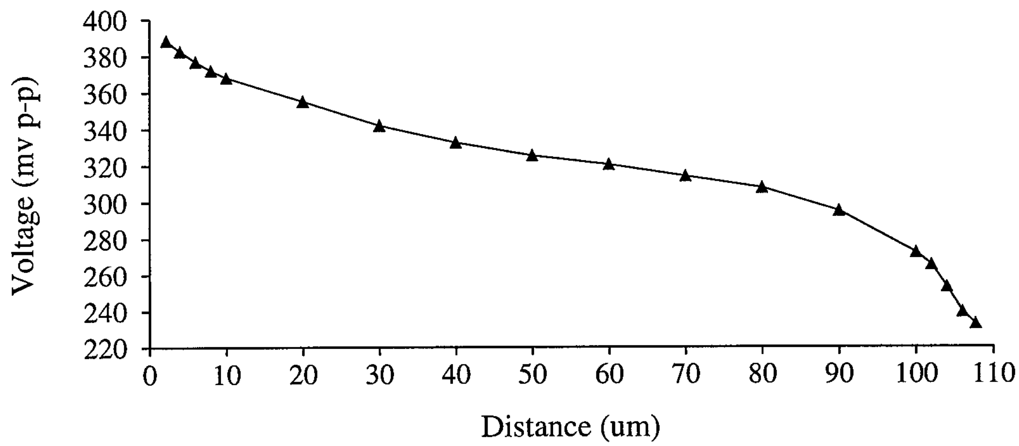
$$\text{Percent Sensitve} = \left[\frac{\text{Sensitive Device Substrate Fluctuation}}{\text{Bulk Substrate Fluctuation}}\right] \times 100\% \qquad (2.7)$$

analog device, the device substrate is held close to the substrate bias. As the guard band is swept away from the analog device, it becomes more strongly coupled to the bulk substrate. Figure 2.12b shows what is happening to the bulk substrate as the guard band is swept along. When the guard band is near the noisy device, current leaves through the epitaxial layer resulting in less current in the bulk substrate, so the bulk fluctuation is low. When the resistance through the epitaxial layer gets large, a majority of the injected current flows through the bulk substrate resulting in higher fluctuation. Figure 2.12b appears to be growing again at D=0 but this is not what physically happens. There is some small error incurred from the substrate discretization and the RC reduction. To ensure that this is not the case, the guard band was placed at -100 microns and the bulk fluctuation was around 400 mv. Thus the bulk voltage levels off as the guard band moves further away from the noisy device. The up-side down U shape in Figure 2.11 shows that ohmic guard structures should be placed as close as possible to the noisy digital or sensitive analog devices in the design.

Finally, the effects of the number of ohmic contacts were simulated. The two devices were place 110 microns apart. Then additional ohmic contacts, in groups of ten, were placed approximately 120 microns from the digital device. They were placed this far



a



b

Figure 2.12a,b. Percent Sensitive and Bulk Fluctuation with the Swept Guard Band

so there would be no noise current flowing through the epitaxial layer. The results from these simulations are shown in Figure 2.13. As the number of ohmic contacts increase, the bulk fluctuation decreases since there are more current paths to ground. Another way of looking at it is that the effective resistance to the bulk substrate is reduced as more ohmic contacts are included.

Now that a brief background on substrate coupling, especially in an epitaxial process, has been discussed, the analysis can switch to the industrial PLL. The explanation of substrate coupling will be important in further sections since different guarding techniques will be tried based on what is happening in these simple test cases.

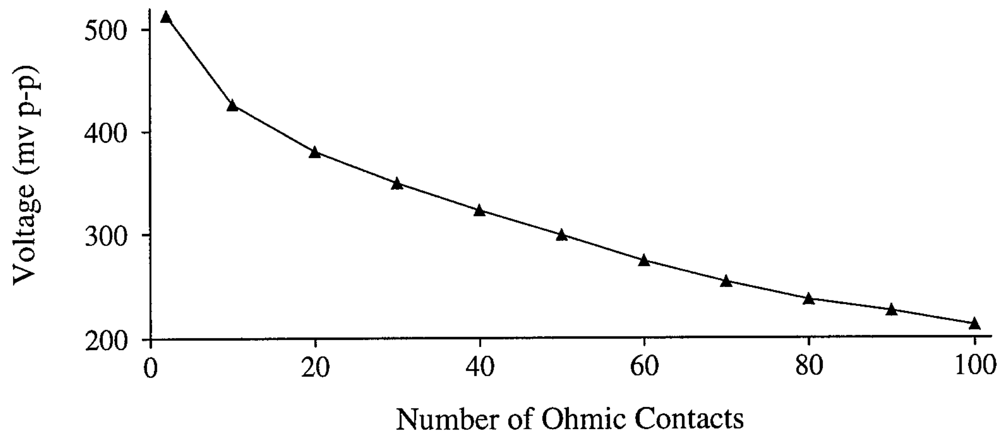


Figure 2.13. Effects of Ohmic Contact Number in an Epitaxial Process

2.4 Jitter Measurement Techniques

A quick discussion on jitter and how it is measured will be helpful in the next sections. Jitter is defined as the deviation in a signal's output transitions from their ideal positions. There are three categories of jitter: cycle-to-cycle, period and long-term. Long term jitter measures the maximum change in the output signal's position over many cycles. This will not be discussed further since measured results are not in this format and very lengthy simulations would be required to get these results. Cycle-to-cycle jitter measures the maximum difference between cycle periods and is always measured from the same voltage as shown in Figure 2.14. The jitter is then the maximum period minus the minimum period. This type of jitter is simple to get from simulation results since the simulator can give the period of each cycle easily. It is not easily seen from measured results

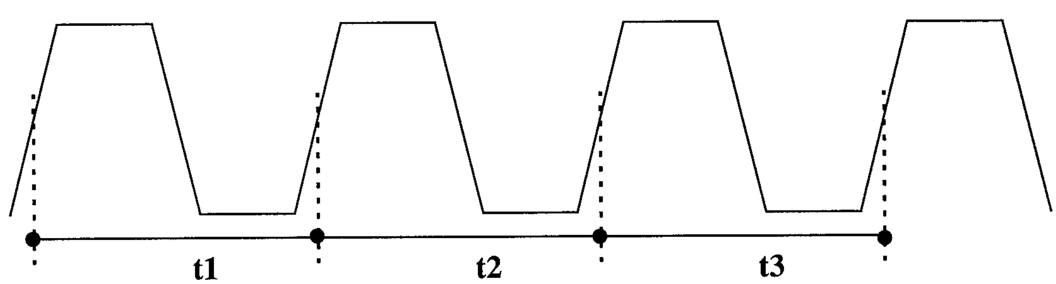


Figure 2.14 Cycle-To-Cycle Jitter Measurement

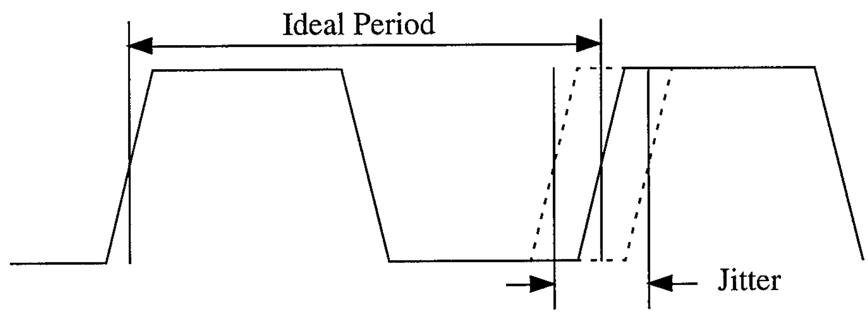


Figure 2.15 Period Jitter Measurements

since a scope likes a trigger point and shows overlapping waveforms, not each cycle. Period jitter is very easily seen from measured results since it measures the maximum change in the signal's transition from the ideal transition as shown in Figure 2.15. This can easily be seen on an oscilloscope if it triggers off of the falling edge of the signal. These results are difficult to get from simulation without some lengthy post-processing. Since National Semiconductor is providing the measured results, the simulations will be measuring cycle-to-cycle jitter. Every effort will be made to compare the same type of jitter when referring to measured results. When not comparing to measured results, only cycle-to-cycle jitter will be used. Since it will be used a majority of the time cycle-to-cycle jitter will be referred to as jitter from now on unless otherwise specified.

Chapter 3 System Simplifications

3.1 Why are simplifications needed?

National Semiconductor, Inc. provided the Phase-Locked Loop to be analyzed for substrate coupling. The PLL is used in industry to create clock signals for integrated circuit systems. They had previously fabricated the circuit and measured the effects of substrate noise on this circuit's performance. The design includes the PLL and a large buffer to create the substrate noise. No I/O pads were included in the simulated design. The circuit is built in a twin-well, epitaxial, dual-metal, silicon gate CMOS process. The minimum dimension is 1.0 micron that is shrunk to 0.72 microns for fabrication. A total of 1810 transistors are in the design. The objective of this research is twofold.

- Correlate measured results with simulation results.
- Develope aggressive guarding techniques for this circuit in this process.

Unfortunately, due to limited computer memory and time, these results cannot be achieved by simply attaching a substrate model (referred to as a mesh) to the entire circuit.

It was realized early in the research that simplifications would have to be done to the circuit and/or the system to perform substrate coupling simulations. The large transistor count and the small device features equate to a substrate modeling problem that is beyond the limits of the software used in SNAPPLE on the Sun Sparc20 processor with 160 Megabytes of memory. Successful substrate coupling analysis has been performed on a design with 1524 transistors in under 4 hours on a Sun Sparc20 workstation[14]. Even though the device count may be similar, the substrate features are dramatically different. The National PLL has large guarding structures and many odd shaped wells that require large numbers of RC branches to properly model. The constraint is not just transistor number but also how they are arranged and the placement of "non-device" substrate features. Additionally, the 1524 transistor case study performed a sensitivity analysis to determine the noisy and sensitive circuits. This dramatically reduced the size of the substrate model resulting since not all circuit devices were attached to the substrate mesh. The sensitivity analysis previously done has been found to be inaccurate so that analysis has been omitted from the system.

The first piece of limiting software is the RC reduction tool. This software's memory requirements scale super-linearly with the number of ports and the number of internal nodes in the mesh. Ports in the SNAPPLE system refer to the number of transistors and substrate or well biases in the design. Simulations were done to predict the amount of memory that would be required to reduce the mesh for the entire PLL. These simulations used a mesh that assumed the bulk substrate can be modeled as one node. This assumption has been used in previous work [3] and will be addressed later. Figure 3.1 shows a logarithmic graph of the number of nodes vs. the memory required to reduce the mesh. The

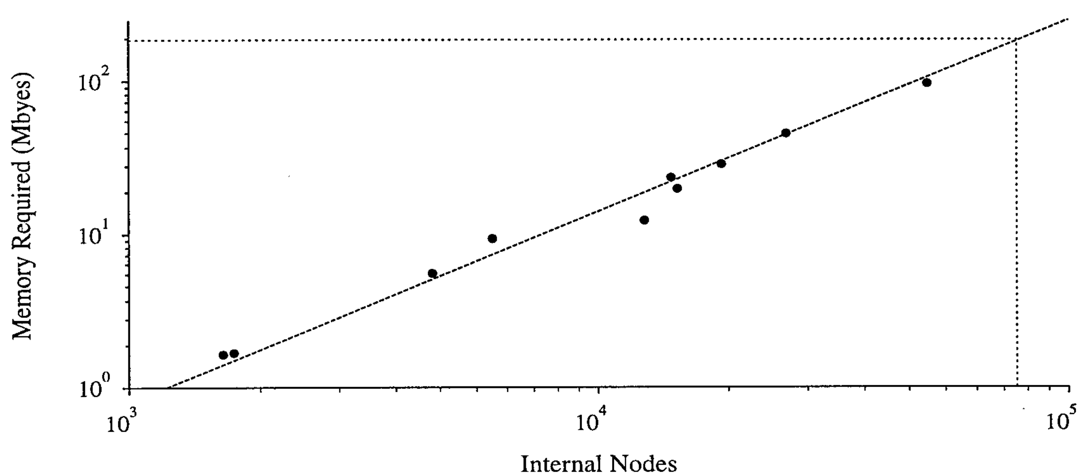


Figure 3.1 Internal Nodes vs. RC Reduction Memory Requirement

dotted horizontal and vertical lines show the projection of memory for the entire PLL which is approximately 190 Megabytes. The current memory on the system used is 160 Megabytes. A different projection based on an attempt to reduce a substrate mesh for the entire PLL showed that approximately 275 Megabytes of memory would be required. Although these predictions are not similar, due to memory being dependent on both the number of nodes and the number or ports, both show that additional simplifications have to be done in order to create a reduced substrate model with the current system beyond the single bulk node assumption.

The second limiting software package is the circuit simulator with respect to time. Simulations done on just the VCO and the noise generating circuit with a substrate mesh take approximately 3 days to simulate for 100 ns on a Sun Sparc20 workstation. Simulations without a substrate model have shown that the simulation must last for at least 1μs to get lock in the PLL. Just the VCO and the noise generators for 1 μs would take 30 days to simulate. If the rest of the circuit transistors were added with ideal substrate connections, the number of transistors in the simulation would over double but the substrate model would remain the same. Assuming that circuit simulator has a linear time complexity, which is not the case, the simulation time becomes approximately 60 days to get results. The point is that the simulation time required quickly becomes unreasonable. A 2 month simulation time is not reasonable in industry. Now, even if a reduced substrate model existed, the simulation time for the entire PLL is unreasonable.

In order to analyze jitter in the National Semiconductor PLL, simplifications are a must. The assumptions need to simplify the PLL can come from the circuit components used and also how the substrate is modeled. Three major assumptions will be applied to the PLL to reduce the RC reduction memory required and the simulation time.

- Simulate just the VCO and the noise generator.
- Model the bulk substrate as one node.
- Include only well regions containing MOS devices in the substrate mesh generation.

These simplification will be shown to be advantageous to the SNAPPLE memory and time limitations while still ensuring accurate results.

3.2 Simplifications

3.2.1 VCO and the Noise Generator.

The PLL from National Semiconductor is built as shown in Figure 3.2. The Divider, VCO, and Phase_Pump/Filter blocks compose the PLL. The noise generator

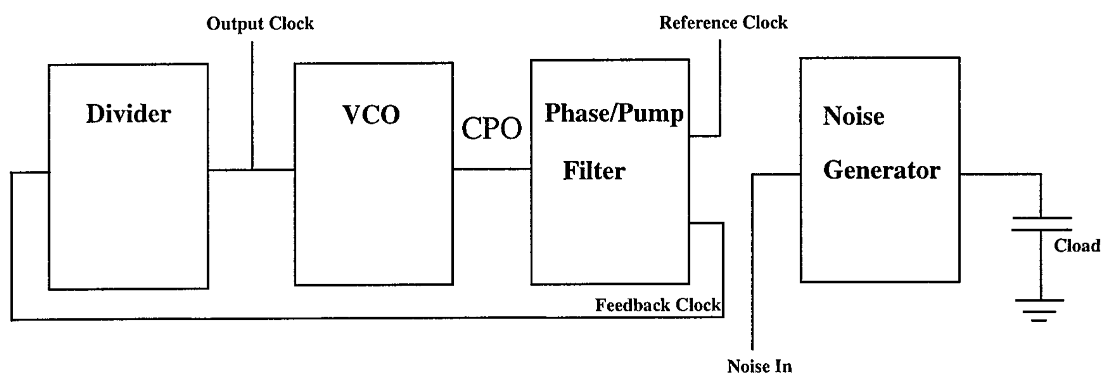


Figure 3.2 Block Diagram of Phase-Locked Loop

block is used to create a noisy substrate. The digital devices in the noise generator circuits are built from output pads. This gives realistic buffer sizes and switching characteristics since they are capacitively loaded. In order to reduce the time to simulate this circuit, it is desirable to include only two of these blocks in the simulation. The reduction in circuit size will also dramatically reduce the size of the mesh required to model the substrate.

The two obvious choices are the noise generator and the VCO. The noise generator was specifically placed in the design to create a noisy substrate. The noise generator consists of five output pads in series. Each output pad consists of four inverters in series with each stage getting increasingly bigger as is done in most digital output pads. The large inverters on the last stage are by far the largest digital devices in the circuit which produce a large capacitive region to the substrate. When driven to produce a fast switching signal at the output, these devices will inject substantial current into the substrate. This block is a must to create the noisy substrate.

The VCO was the obvious choice for the block to be included with the noise generator. Previous research has shown the VCO is the most sensitive block of circuitry in a PLL. National Semiconductor does not allow detailed description of this circuit's design. In very basic terms, the VCO consists of a current-starved ring oscillator. MOS devices control how much current flows through the ring oscillator components. The current control devices' input voltages are determined by the input voltage to the VCO. Since the I-V relationship of a MOS device is non-linear, additional circuitry is required to bias the control devices. In this circuit, two groups of transistors are very sensitive to the substrate bias, the devices that determine the input voltage to the current controlling devices and the actual devices that control the current. Small fluctuations in these devices substrate bias can dramatically effect the amount of current flowing through the ring oscillator components changing the output frequency.

Besides its sensitivity, the VCO was chosen since the structure is relatively easily to separate from the entire design. The output of the VCO is an oscillating signal that is the same output of the entire PLL. Additionally, the VCO has only one input required to control the output frequency. The small number of I/O for this block of circuitry makes the simulation setup very simple. Since the resulting circuit to analyze for substrate coupling is dramatically smaller, the substrate model will also be dramatically smaller. Subsequent simulation time will drastically decrease since the circuit will not have to lock, unlike the entire PLL, and the transistor number has decreased.

One issue that arises with this dissection of the PLL is the input to the VCO. In the PLL, every attempt is made to make the VCO input a constant value. This is very difficult to achieve since devices in the Phase Detector and the Charge Pump (called the Phase_Pump in this design) have non-ideal delays. Device switching time as well as any parasitic interaction like substrate coupling, causes the VCO input to have some fluctuation around a DC value. In order to get accurate results, this fluctuation into the VCO must be modeled. Again the entire PLL can be broken into just the noise generator and the Phase/Pump and Filter block of the design. The output from this block can be mapped into the VCO to hopefully give an accurate jitter value.

Now that the circuit has been simplified to only the VCO and the noise generator, the substrate model and the simulation time will decrease. The number of transistors in the design decreases from 1810 to 718. To compare the simulation time between the entire PLL and just the VCO and noise generator, both were simulated for 2 us without a substrate model. The entire PLL took 36 hours while the VCO and noise generator only took 14 hours. More importantly, it took the entire PLL about 1 us to get into a locked state which took about 20 hours. The PLL must be locked before jitter analysis can begin. Since the VCO and noise generator do not have to lock, the simulation only takes about 45 minutes to get the useful information. Finally, the substrate models can be compared for the two designs. Table 3.1 shows how reducing the analyzed circuit to just the VCO and the

Table 3.1 Substrate Branch and Node Comparison

Circuit	Nodes	% Reduction	Branches	% Reduction
PLL	268304	0	948781	0
VCO/Noise generator	232178	13.5	787818	17.0

noise source affects the resulting substrate model. This simplification provides a decent job at reducing the pre-reduction substrate model but a signification reduction in mesh size is still required before RC reduction can take place.

3.2.2 Modeling the Bulk Substrate as One Node.

Epitaxial substrate processes are created with the majority of the substrate highly doped, resulting in a low resistivity. A very thin layer on the top of the substrate, the epitaxial layer, is lightly doped. The epitaxial layer is doped this way to allow devices to be easily created in the substrate. The combination of the vastly different resistive materials allows good control over device construction and a low resistive substrate. The layered substrate structure allows the substrate model to only include the epitaxial layer with all connections to the bulk substrate connected to one node. This modeling technique has been used in previous epitaxial modeling techniques[3]. This assumption will drastically cut down on the size of the substrate model. Now only the three or four node planes needed to model the epitaxial layer are sufficient to model the entire substrate. If the epitaxial layer and the bulk substrate are both modeled, approximately eight or nine node planes are required. Since the substrate model is completed in three dimensions by stacking layers with similar amounts of nodes, cutting the number of node planes in half should reduce the substrate mesh by the same amount. The issue then becomes how accurate this simplifying assumption is.

A simple cross section of silicon as shown in Figure 3.3 will be used to show how

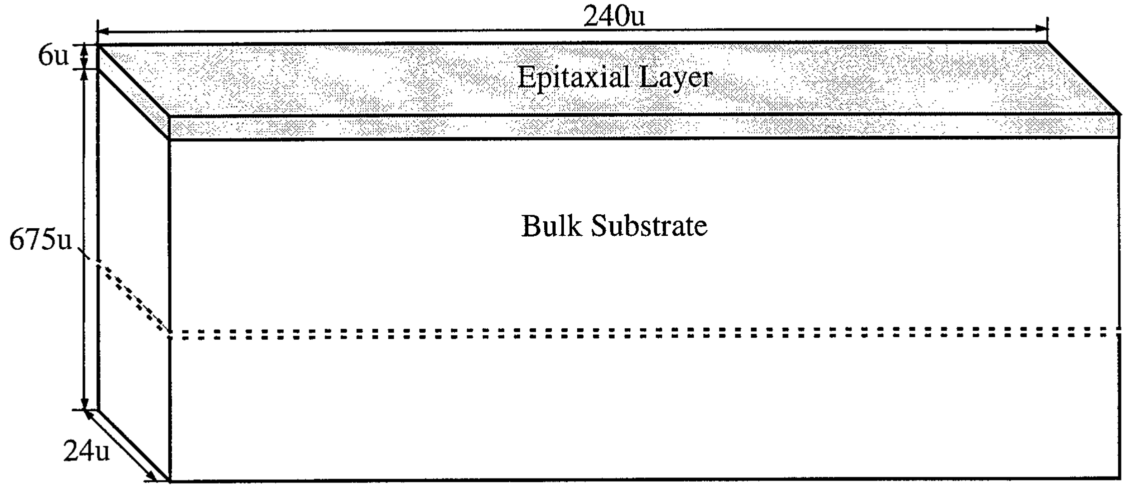


Figure 3.3 Simple Silicon Cross-Section for an Epitaxial Substrate

little accuracy is lost using this assumption by calculating the resistance of each type of material. From the National Semiconductor technical information, the epitaxial layer is p-type and doped at 3.5 x 10^{14} sites/cm^3 and the bulk substrate is p-type and doped at 2.8 x 10^{18} sites/cm^3. From a standard table of silicon resistivity verses impurity concentrations at room temperature [15], the resistivities of the two layers are 36 Ω-cm and 0.02 Ω-cm. The four order of magnitude difference in doping concentrations results in three orders of magnitude difference in resistivity. From the dimensions of the scaled drawing in Figure 3.3 and the resistivity values, a value of resistance can be calculated for each layer from equation (3.1). ρ is the resistivity, l is the length (240u), w is the width (24u), and t is the

$$R = \frac{\rho \times l}{w \times t} \tag{3.1}$$

thickness (6u for the epitaxial layer and 675u for the bulk substrate). This is the same equation that is used to create the resistance values for the substrate model. For this process and the give dimensions, the epitaxial layer has a resistance of 600 kilohms while the bulk substrate has a resistance of approximately 3 ohms which is a difference of five orders of magnitude.

Since current injected into the substrate is drawn to the bulk substrate, it must travel through at least 6 microns of epitaxial silicon. Assuming that this current only flows through a 1 μm x 1 μm rectangle piece, the resistance to the bulk substrate is 216 megohms. The distance the current would have to flow through a piece of bulk substrate with the same width to give a similar resistance is over seven meters. The layout in question has a maximum length of 3 millimeters from corner to corner, so the maximum value of a bulk substrate resistance is approximately 90 kilohms which is still three orders of magnitude less than the resistance through the epitaxial layer. What all these numbers show is that it is unnecessary to model the bulk substrate. If it were modeled, there would be many resistive branches with such small values compared to the epitaxial values that their effect would not be seen.

The software to create the substrate mesh can be tricked to achieve the single node bulk substrate. The problem is set up such that the substrate thickness is only 6 microns (the epitaxial thickness) with a backplane contact. This will create a detailed model for the epitaxial layer and hook every connection to the bulk substrate to the same node. When all this is done, the substrate model is significantly smaller than when the bulk substrate is modeled. Table 3.2 shows a comparison of the mesh nodes and branches from the entire

Table 3.2 Updated Substrate Branch and Node Comparison

Circuit	Nodes	% Reduction	Branches	% Reduction
PLL	268304	0	948781	0
VCO/Noise	232178	13.5	787818	17.0
VCO/Noise, bulk as 1 node	82231	69.4	289147	69.5

circuit down to just including the VCO and noise generator and modeling the bulk substrate as one node. The resulting models are almost 70 percent reduced in size from two simple steps. Despite the good results, further simplifications are desired as long as the accuracy of the model is not compromised.

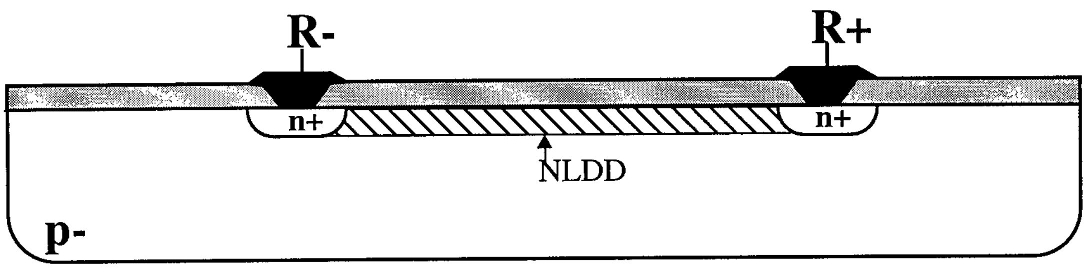
3.2.3 Model Only Device Wells

The SNAPPLE system accounts for regions of substrate that are doped of the opposite type as the substrate. These well regions are used to create different types of circuit devices and used as mixed signal guarding structures. The depletion regions formed between well boundaries and the substrate are modeled as capacitance in the substrate model. The number of capacitors in a substrate model add up quickly since all area of these depletion regions are modeled with discrete components. Thus, if certain well regions in the layout can be ignored, then the substrate model will be simplified. It was decided to only include the wells that have MOS devices built in them. This is necessary to isolate the bulk node connection in devices built in wells from the native substrate. By only including these wells, there are wells used for three purposes that are omitted including:

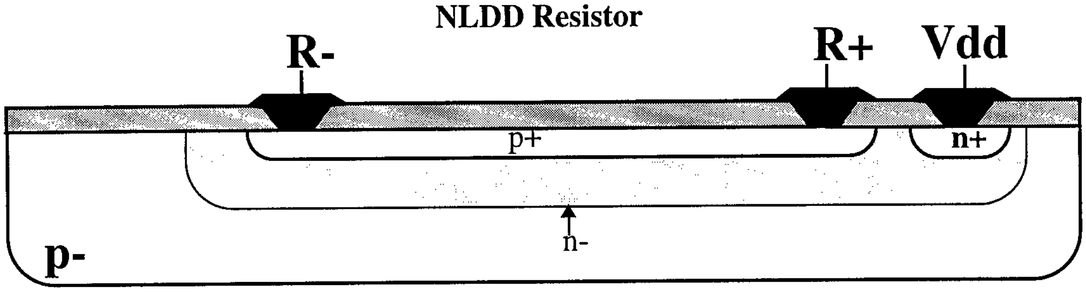
- Resistor wells.
- Zener diode wells.
- Minority carrier guard structure wells.

The effect of omitting each of these will be discussed separately.

Many IC designs build resistors in the silicon. The substrate mesh could be used to for these resistors by hooking the ideal circuit straight into the mesh. For the resistors in this design, SNAPPLE was used to find the connectivity of these resistances and the values were placed in by hand. The two types of resistors, the NLDD resistor and the p+ resistor, have cross section views shown in Figure 3.4. Note that the figures are only showing the epitaxial layer to simplify diagram. The NLDD layer is a special n-type doping layer used by National Semiconductor. Since the value of resistance that is created depends solely on the doping concentrations, the substrate bias is of little concern. The only possible parasitic effect is that current could couple across a junction into one of the resistances from the bulk substrate or current could be injected into the substrate. Because the size of these resistors are not large, the capacitance to the bulk substrate is not very large. Additionally, the current that would couple across the junction would be small compared to the current designed to flow through the devices. To show an example of this, a small section of the design that uses p+ resistors was simulated with a crude model for a



NLDD Resistor



p+ Resistor

Figure 3.4 Resistor Cross-Sectional Diagrams

connection from this resistor to the substrate. Figure 3.5 shows the resulting current flowing through this resistor with a substrate connection modeled and with no connection modeled. As is shown in the figure, the current through the resistor changes only slightly when the substrate connection is modeled. This shows that the noise received from transistors in this design will dominate any noise received in the resistors.

Since some of these resistors are used in switching circuits, they could possibly

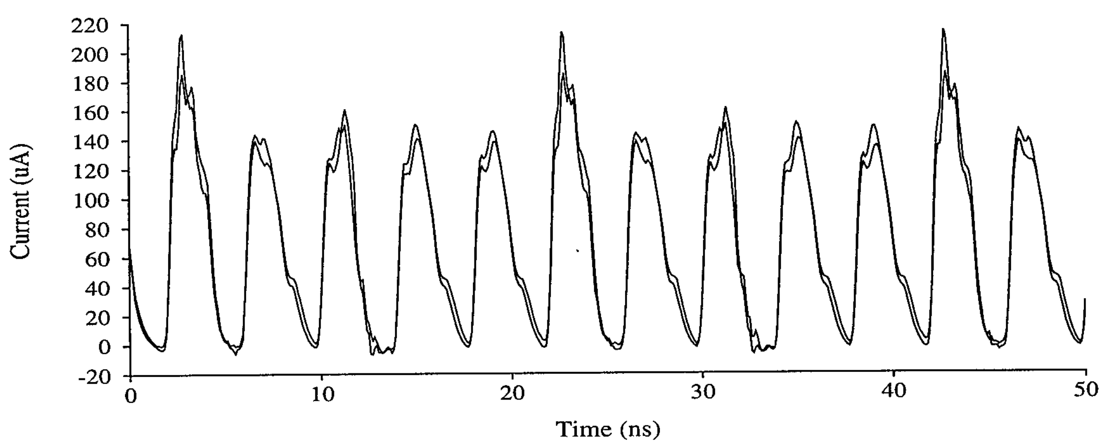


Figure 3.5 Resistor Current Comparison

inject current into the substrate. The NLDD resistor in this design has switching signals on each end but the signals switch slower than some of the large digital devices. Since the switching signals and the capacitance for this resistor are much smaller than the noise generator devices, their noise injection will not be significant. For the p+ resistor, the area is about the same as the NLDD resistor, but the signals switch at the same speed as the digital devices. Still a substantial amount of current will not be injected into the bulk substrate since this noise must couple across two reverse biased p-n junctions.

The next group of well regions that are omitted by just modeling the device wells are the wells used to create zener diodes in the output pads in the noise generator portion of the circuit. The zener diode is used to protect the sensitive devices on the silicon from static charge from the outside world. Figure 3.6 shows how the zener diode is built in silicon. The junction of interest is from the NLDD layer to the p+ implant. Since the p+ region is grounded, this diode is reverse biased. There is also a parasitic diode from the n-well region to the p- epitaxial layer. The n+ connection is the cathode of the zener diode but also acts like a low impedance ohmic contact to the zener diode well. Since there are no other ohmic connections to the well, the voltage in the well will be the same as the cathode of the zener diode. Since the n+ region sits at the output node of the pad, this node will be switching rail to rail.

Since the well bias is swinging rapidly and the size of the well is enormous, it cannot be assumed away. It cannot be modeled with the SNAPPLE system due to the way p-n junctions from well implants are modeled. SNAPPLE assumes that the well bias is constant which allows reverse biased p-n junctions to be modeled as a parallel plate capaci-

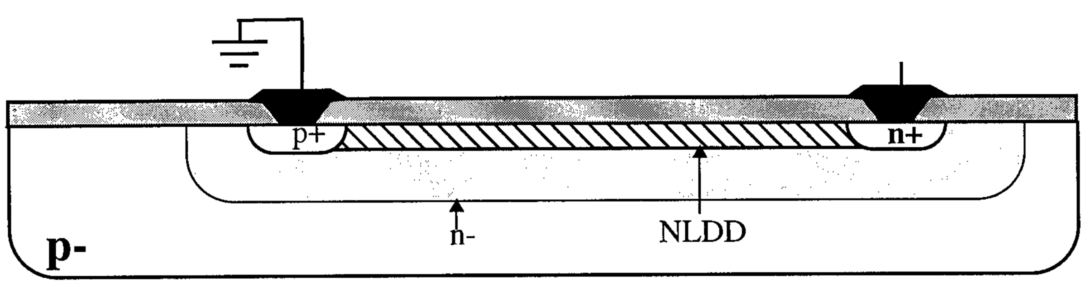


Figure 3.6 Zener Diode Cross-Sectional Diagram

tance. Since the well bias is fluctuating from rail-to-rail, the well cannot be accurately modeled with the SNAPPLE system. Due to the large size of the well, it could potentially inject a significant amount of noise into the substrate. The fix to this problem is to model the entire well as a single diode with the cathode hooked to the output of the noise generator and the anode hooked to the single node bulk substrate. With this well modeled as a diode, SNAPPLE does not have to discretize this large area of diffusion region and so thousands of linear devices are replaced with one non-linear device.

An issue that arises is concerning connecting the anode of the device directly to the bulk substrate node. By making this connection, it is assumed that all current injected across this diode goes directly to the bulk substrate. This connection is justified by three factors. First, the junction depth of the n- well is only 4.6 microns from the bulk substrate layer. Any current injected on the bottom of the diode can go directly down to the bulk through 4.6 microns or back up to the top of the epitaxial layer which is 1.4 microns, but it must exit through an ohmic contact. Second, the nearest ohmic contact to this well is over fifty microns away. So even if current is injected from the side wall of the well closest to the ohmic contact, the low impedance path will be to the bulk substrate, 4.6 microns verses 50 microns. Finally, the well region is 150 by 130 microns. Even if ohmic contacts surrounded the well, any current injected from the center of well region would see a much larger resistance through the epitaxial layer than down to the bulk substrate. It is relatively easy to see that this modeling simplification will work and still be accurate.

The final concern is wether or not the diodes are even necessary. It is possible that the current they inject can be insignificant to the current injected at the source/drain or gate areas of MOS devices. To test the amount of current that these diodes will inject, a simple test circuit was created. This circuit is identical to Figure 2.9 except the digital device was replaced with one output pad since this is where the zener diode well is located. There was no guard structure around the analog NMOS device. The voltage fluctuations in the bulk substrate with and with out the zener diode modeled as a well diode are shown in Figure 3.7 The peak-to-peak fluctuation without the diode is 400 mv and the fluctuation with the well is 790 mV. This clearly shows that the zener diode wells will inject a substantial amount of substrate current. This will be important since one of the

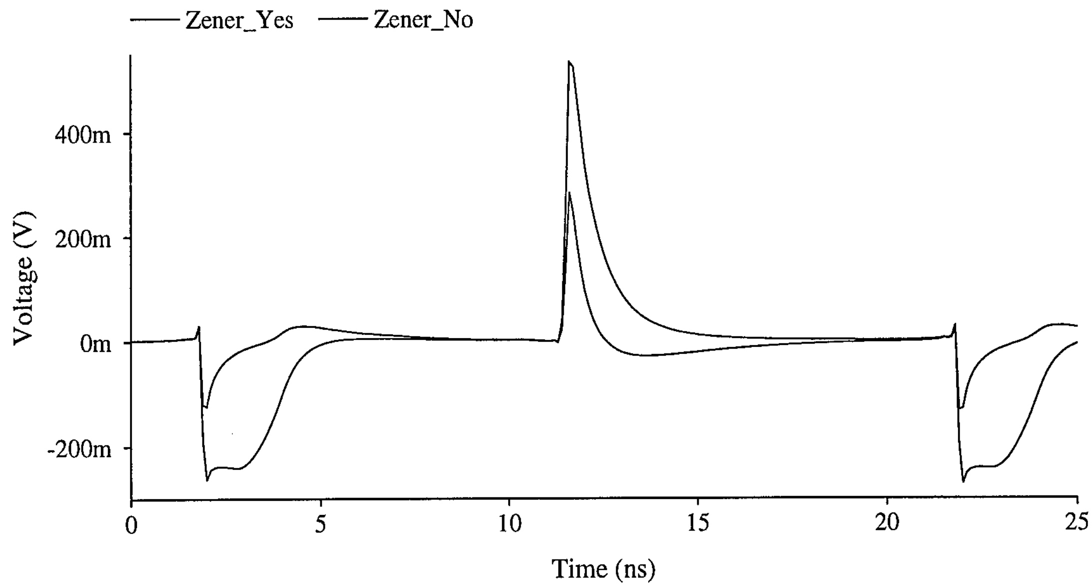


Figure 3.7 Comparing Current Injection with Zener Diodes

goals of the research is to correlate silicon measurements to simulation results. Without these diodes, the injected noise would not be accurate.

The final group of well regions that are omitted with using only device wells are the minority carrier well guarding structures. Chapter 2 discussed the theory why these guard structures are not effective in an epitaxial process. Now simulations will be used to prove the same point. The same test structure from the zener diode test case is used. The only parameters that were varied were the type of guard structures placed around the analog device. The different guard structures used in this test are shown in Figure 3.8. This view shows how the device and guard structure are created in a layout. Figure 3.9 shows the cross-sectional diagram of case D in Figure 3.8. Since case D has both the low impedance ohmic and the minority carrier well guard structures, the remaining structures (A-C) cross-sectional views are seen by removing the appropriate guard structure.

The simulation set up is identical to those in section 2.3 and the voltage fluctuation at the substrate connection of the device is monitored. The SNAPPLE system is configured for these simulations to include the guard wells but not the resistor and zener diode wells. The single zener diode is modeled as a diode as discussed earlier.

The results of the six test simulations are shown in Figure 3.10. There are only four

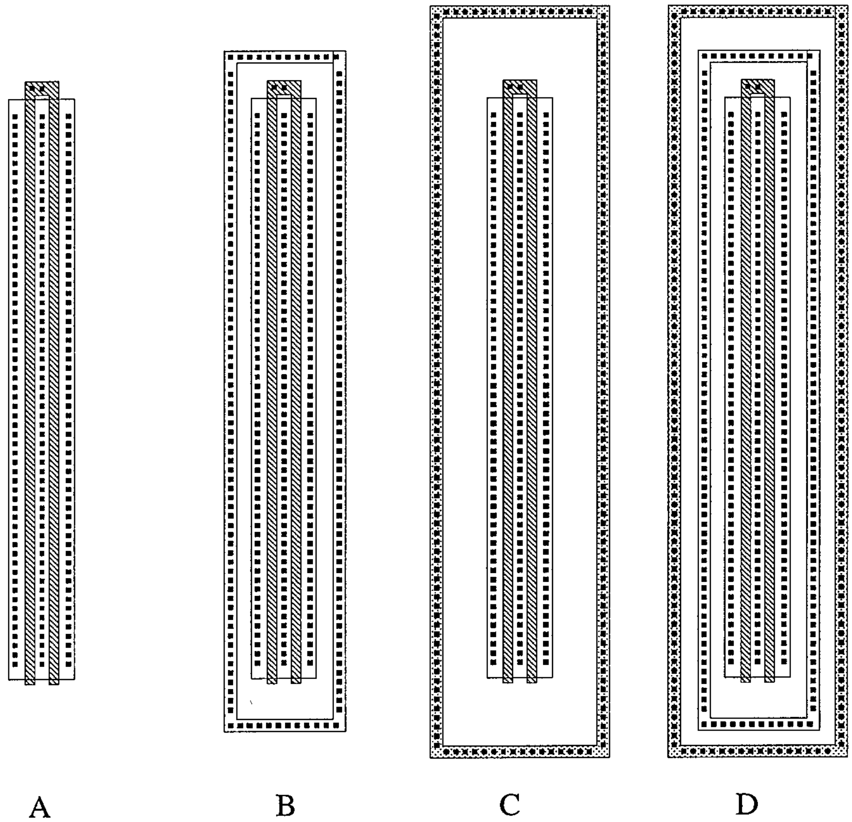


Figure 3.8 Four Different Guard Structures for an NMOS Device. A--No Guard Structure, B--Ohmic Guard Structure, C--Well Guard Structure, D Both Ohmic and Well Guard Structure.

test structures, but the well bias is arbitrary. Both structures with well guard rings were simulated twice, once with the well floating and once with the well tied to Vdd. As the results show, the well guarding structure was ineffective. It is obvious that guarding strategies A-C are similar and D-F are also similar. The difference between these two sets of results is the inclusion of the p+ ohmic guard ring around the sensitive device. The well guard structure does have a slight impact on the noise shielding of the sensitive device but its effectiveness is minor compared to the ohmic guard ring.

Since it has been proven that well guard structures can be ignored with only a slight cost in accuracy, they can be omitted from the substrate model creation. The results from these simulations not only verify an assumption, they also lead to an important realization for mixed signal designers. Well guarding structures have little effect in an epitax-

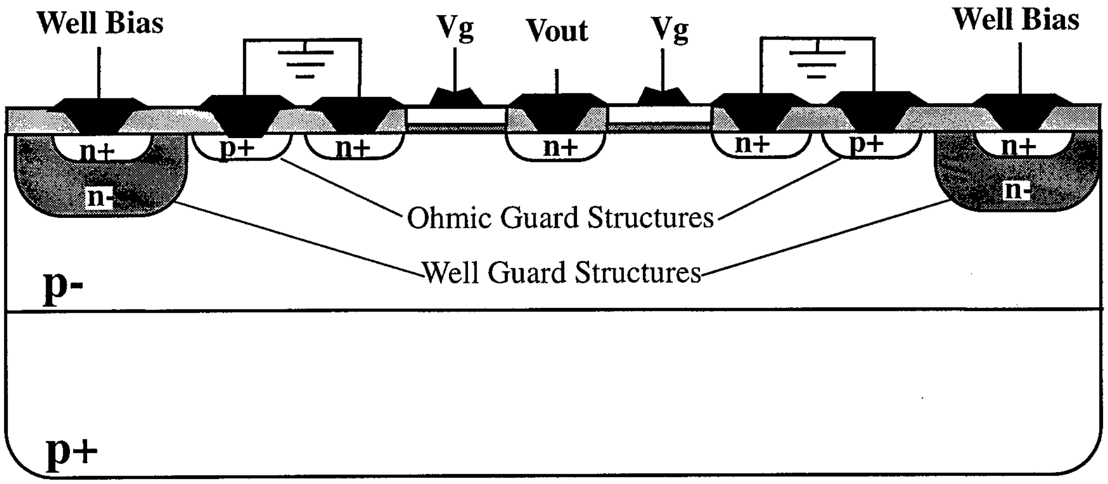


Figure 3.9 Test Structure Cross-Section

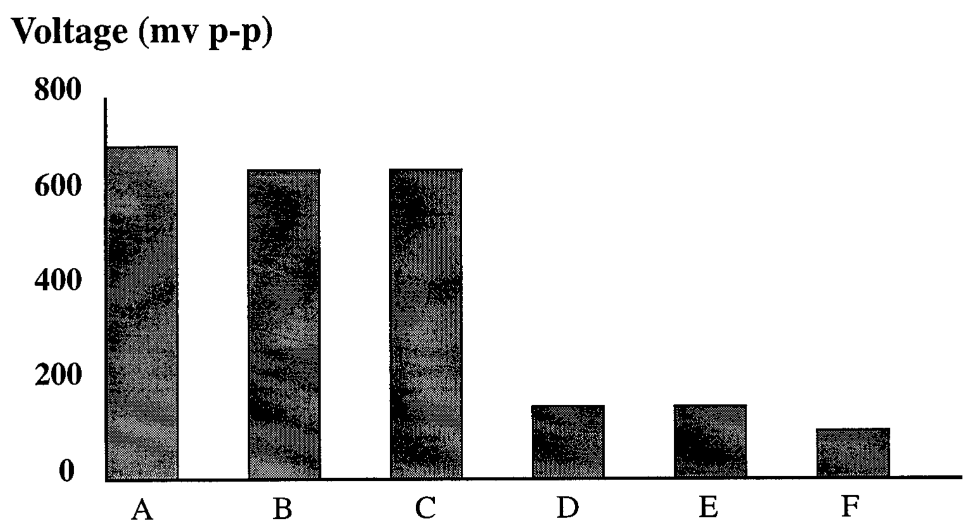


Figure 3.10 Simulation results for Well Guard Structures. A--No Guard Structure, B,C--Well Guard Structure, unbiased and biased, D,E, Well and Ohmic Guard Structures, well unbiased and biased, F--Ohmic Guard Structure.

ial process. When designers use heuristic guarding measures, which usually include both ohmic and well guard structures, they are wasting silicon area which is costly when the chip is fabricated. It was found in the PLL design from National Semiconductor, that over

$70{,}000\ \mu^2$ or approximately 3.2 percent could be saved if the well guarding structures

Table 3.3 Updated Substrate Branch and Node Comparison

Circuit	Nodes	% Reduction	Branches	% Reduction
PLL	268304	0	948781	0
VCO/Noise	232178	13.5	787818	17.0
VCO/Noise bulk as 1 node	82231	69.4	289147	69.5
VCO/Noise bulk as 1 node ignore 3 well types	55626	79.3	192672	79.7
VCO/Noise bulk as 1 node ignore 3 well types RC-Reduction	729	99.7	8569	99.1

were removed from the design.

Now that two well regions, the resistor wells and the well guard structures, can be omitted and the zener diode well can be modeled as a single diode, the substrate model is simplified even further when used with all the assumptions. Table 3.3 is an expansion of Table 3.2 showing how much of a reduction is achieved with the well omission assumption. This table also shows the reduction in the mesh size after it is processed with the RC-reduction software. The reduction could only take place after all of these assumptions were used when modeling the substrate.

3.2.4 Additional Assumptions

It was stated in Chapter 2 that the parasitic capacitance from the interconnect lines to the bulk substrate is not modeled. An example from the circuit at hand should show that a majority of injected substrate current will come from device capacitance and not the interconnect capacitance. In order to simplify this comparison, it will be assumed that all capacitances have the same switching signal on them in order to just compare capacitance values. The block of the circuit from Figure 3.2 to be analyzed is the noise generator. The noise generator has the majority of the fast switching devices and the largest area of metal in the layout so it should provide a good comparison.

The large area of metal in the noise generator is on the second layer of metal. It has an approximate area of 97,000 μ^2. From the technical data provided by National Semiconductor, this metal has a capacitance per area of 21 aF/μm^2, resulting in a capacitance of 2.04 pF. A discussion of all the capacitance from devices in this block of circuitry would be tedious, so only several of the contributors will be looked at including all the NMOS gate capacitance and the zener diode well capacitance.

The output pads in the noise generator consist of a four stage buffer with each successive buffer increasing in size by about a factor of three. For one buffer, there is a total NMOS gate area of 554 square microns. The capacitance per area for polysilicon over gate oxide is 2878 aF/μm^2, producing a capacitance of 1.59 pF. Since there are five output pads, this capacitance grows to 7.95 pF. Each output buffer also has a large zener diode well. Each well has an area of 20415 square microns and a perimeter of 572 microns. The technical data shows that the capacitance per unit area for these diode is 120 aF/μm^2 and the capacitance per length is 359 aF/μm. From equation (2.5), the capacitance from this well diffusion is 2.66 pF. Again there are five wells so the total capacitance to the bulk from the zener well diodes is 13.3 pF. So the total capacitance from the NMOS gate areas and the zener diode wells is 21.25 pF. The capacitance from only these two regions omits quite a bit. There is capacitance from all the NMOS source/drain regions, the PMOS gate area and the PMOS source/drain regions. The PMOS capacitance to the bulk substrate is difficult to predict since current must first couple into the well and then couple across the well boundary. One noteworthy PMOS device, used to load the output of the output buffers, has a width of 492.9 microns and a length of 57.1 microns. Thus the capacitance to the bulk of this device is 81 pF. This device injects quite a bit of current into that device well that then couples into the bulk substrate.

From just these two parasitic capacitances to bulk, it is obvious that the capacitance modeled in the SNAPPLE system greatly outweighs the capacitance from the interconnects. Therefore, the amount of substrate current in this circuit should be accurate as predicted from SNAPPLE. By using this system and the discussed simplifications, it should be possible to get accurate simulation results in a reasonable amount of time. The only last issue is what to do about the parasitic effects of the package. National Semiconductor has provided data on measured parasitics from the package pins. The pin parasitics will be modeled differently for certain simulations and so each pin parasitic configuration will be discussed for each group of simulations.

Chapter 4 VCO Jitter Results

Now that simplifications have been made to the circuit and the substrate modeling technique, simulations can occur to analyze the effects of substrate coupling on the National Semiconductor Phase-Locked Loop. The objectives of this research were touched upon lightly in the previous section. The first and most important objective is to correlate simulation results from SNAPPLE to measured silicon results, provided by National Semiconductor. Such a correlation will establish the accuracy and the usefulness of the SNAPPLE system. The second objective is to show the effects of different guarding structures on the PLL's performance. Both traditional guarding techniques--using both an ohmic guard ring and a well guard ring--and new guard techniques-- using ohmic guarding--will be explored. Ohmic guarding refers to placing ohmic guard bands as close as possible to each sensitive device as opposed to placing an ohmic guard ring around large groups of sensitive devices. Hopefully, the research will show aggressive ways to guard against the adverse interactions present in monolithic mixed signal design.

4.1 Measured Results Vs. Simulated Results.

4.1.1 Simulation Set-up.

In order to be as accurate as possible for this group of simulations, not just the

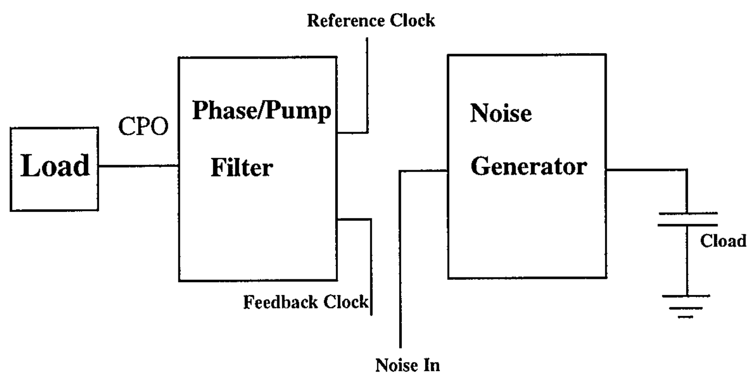
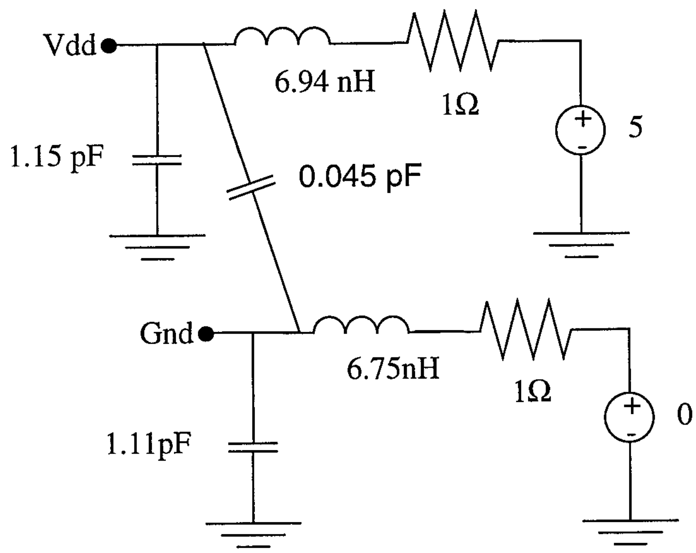


Figure 4.1 Phase/Pump Filter Block Diagram

VCO and the noise source were considered. In order to model the non-ideal input to the VCO, the Phase/Pump Filter block of the design in Figure 3.2 was simulated with the noise generator as shown in Figure 4.1. The noise generator was loaded with a large PMOS device. All ohmic contacts to the substrate remained in the layout from the circuit blocks removed to keep the resistance from the bulk substrate to ground as accurate as possible. Since the loop of the PLL is not connected, two inputs were required to the Phase/Pump Filter circuit, the reference clock and the feedback clock. Both of these signals are identical.to simulate a locked PLL state. With identical input clocks, the charge pump will not change the charge in the filter, so this voltage must be initialized. This initial voltage was determined by simulating the VCO to get the correct VCO frequency. Finally, all the transistors hooked to the CPO node of the layout were included in this setup to account for the loading of the VCO. Both the reference clock and the feedback clock were set to 50 MHz square waves with 2ns rise and fall times. The noise generator was turned off for the first half of the simulation and then driven by a 50 MHz square wave with 2ns rise and fall times for the second half of the simulation. The output of the Phase/Pump Filter circuit was initialized to 1.58 volts. Accurate pin parasitics were included only on the power and ground lines since they are the only pins drawing a substantial amount of current. A schematic of these parasitics is shown in Figure 4.2. The simulation lasted for 40ns

The results from the Phase/Pump Filter block output were then mapped to the



K value for mutual inductance is 0.35

Figure 4.2 Accurate Pin Parasitic Diagram

input of the VCO. The block diagram for the VCO simulation is shown in Figure 4.3. Again, all ohmic contacts in removed blocks remained in the layout. The only input is the CPO which was determined by the Phase/Pump Filter simulation. The output pad is added to try to recreate the exact measurement since the signal had to exit out of a pad. All of the pads were not included due to a large increase in transistor number and mesh size. The pad used was the same one used in the noise generator since the given design did not include the actual pads used in this circuit. The only difference is that the noise generator has five

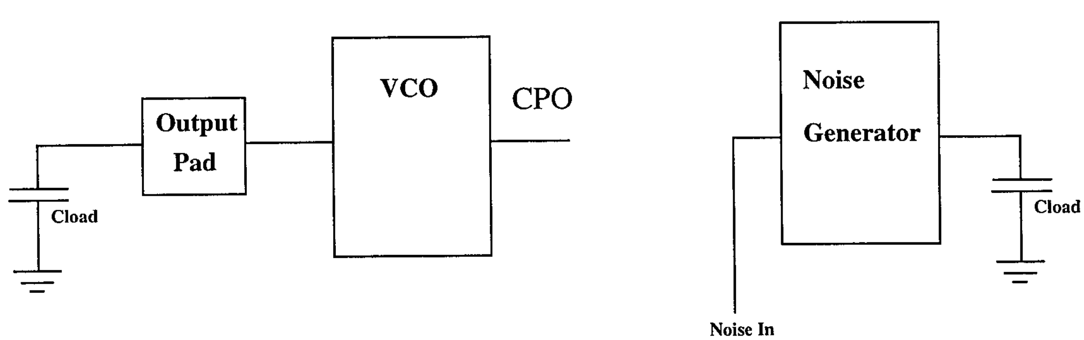


Figure 4.3 VCO Block Diagram

pads in series while the output pad for the VCO only has one pad. One internal node in the oscillator in the VCO had to be initialized to speed up convergence in the simulation. The pin parasitics are those described in Figure 4.2.The signal monitored for jitter is the signal coming out of the output pad. This simulation lasted for 100ns in order to get a good number of cycles to measure jitter in a reasonable amount of time.

4.1.2 Simulation Results.

For the first stage of simulation, the output from the Phase/Pump Filter circuitry with the noise generator both off and on is shown in Figure 4.4. The noise generator was turned off for 20 ns and then turned on. Without a noisy substrate, this node should stay at a constant value and then fluctuate when the noise is turned on. This circuit, consisting of 764 MOSFETs, required 76.8 Mbytes of memory and 2.5 hours to reduce. The 40ns simulation length required 20.6 hours. This work was done on a Sun Sparc20 workstation.

This waveform was then mapped into the VCO simulation using a piece-wise linear approximation. Simulations were run with the noise turned off and the noise turned on. Figure 4.5 shows the output waveform which is the output of the pad.The fluctuations on the constant regions of the square wave are caused by the power rail fluctuation that occurs when current flows through the power supply lines. Some of the current in these lines is used by the transistors and some is injected into the substrate causing the bulk substrate to fluctuate. Just to give an idea of how the substrate is behaving, Figure 4.6 shows

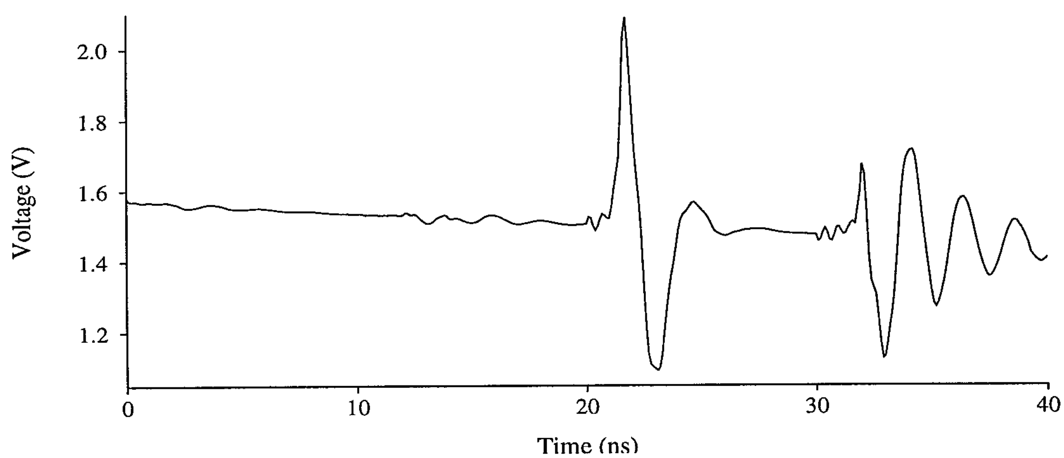


Figure 4.4 Phase/Pump Filter Output

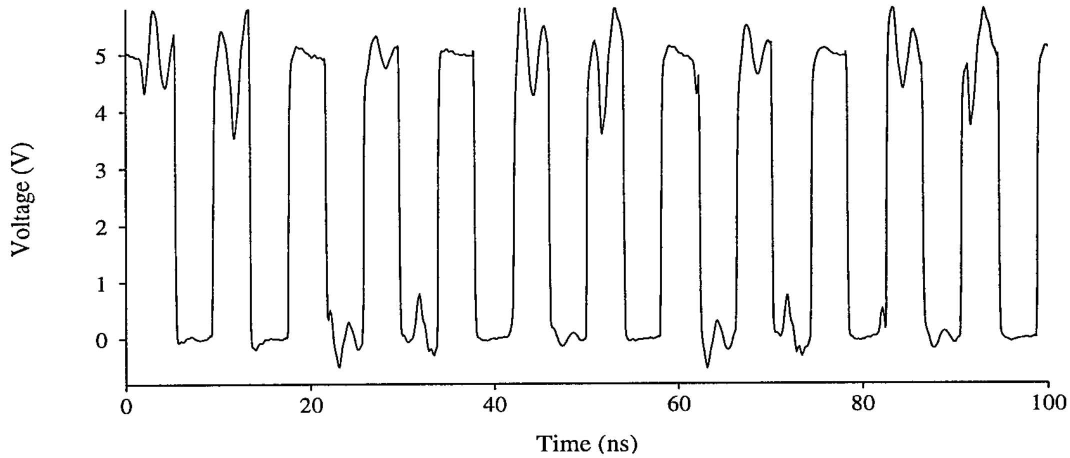


Figure 4.5 VCO Output Waveform

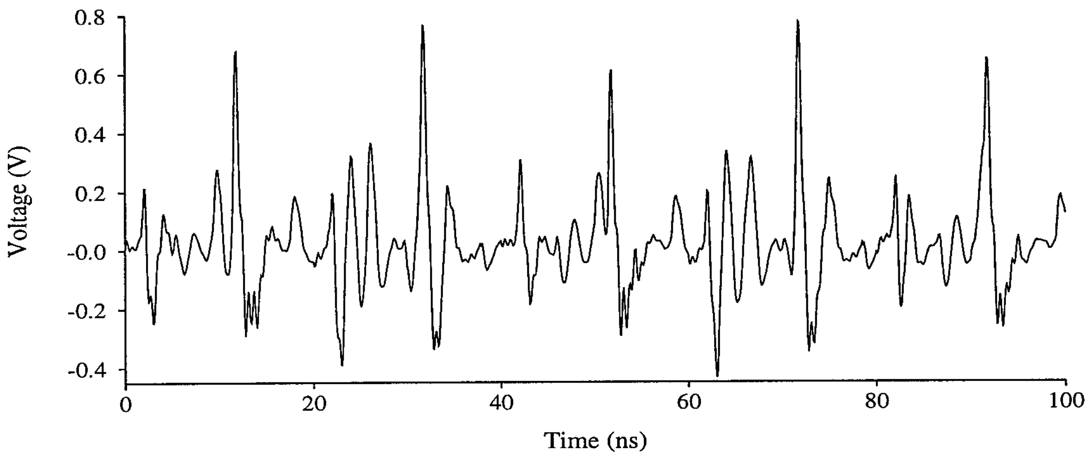


Figure 4.6 Bulk Substrate Voltage Waveform

the node voltage at the bulk substrate node when the noise generator is turned on.

In order to compare the simulated jitter results, the measured jitter results must be shown. Figure 4.7 shows the measured jitter results with the noise generator turned off (quiet substrate) and the noise generator turned on (noisy substrate). These measurements were provided before the research began from National Semiconductor. Each minor tick mark is 200 ps so the PLL jitter with the noise generator turned off is below 100 ps while the jitter with the noise generator turned on is approximately 500ps. Note that this type of jitter is period jitter since the scope is triggered at the falling edge and then the varying

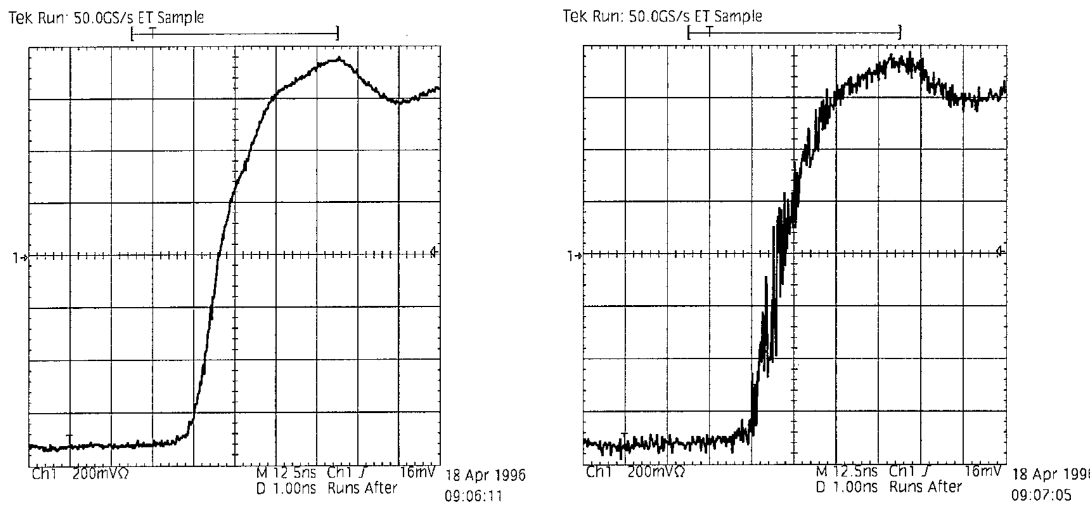


Figure 4.7 Measured Jitter Results with the Noisy and Quite Substrate

rising edges show the jitter.

From the simulations, cycle-to-cycle jitter was measured. Figure 4.8 and Figure 4.9 show the data used to calculate the jitter for the quite substrate and noisy substrate respectively. These figures show the portion of the simulation output file that measures the period of each cycle. The maximum value from the right column is subtracted from the minimum value in the right column to get the jitter. From this data, the jitter with a quite

```
V(0:237) 2.500E+00 2(R) 1.790E-08 V(0:237) 2.500E+00 3(R) 2.613E-08 TRR= 8.23466E-09
V(0:237) 2.500E+00 3(R) 2.613E-08 V(0:237) 2.500E+00 4(R) 3.435E-08 TRR= 8.21898E-09
V(0:237) 2.500E+00 4(R) 3.435E-08 V(0:237) 2.500E+00 5(R) 4.257E-08 TRR= 8.21602E-09
V(0:237) 2.500E+00 5(R) 4.257E-08 V(0:237) 2.500E+00 6(R) 5.080E-08 TRR= 8.23375E-09
V(0:237) 2.500E+00 6(R) 5.080E-08 V(0:237) 2.500E+00 7(R) 5.901E-08 TRR= 8.20728E-09
V(0:237) 2.500E+00 7(R) 5.901E-08 V(0:237) 2.500E+00 8(R) 6.723E-08 TRR= 8.22286E-09
V(0:237) 2.500E+00 8(R) 6.723E-08 V(0:237) 2.500E+00 9(R) 7.545E-08 TRR= 8.21717E-09
V(0:237) 2.500E+00 9(R) 7.545E-08 V(0:237) 2.500E+00 10(R) 8.366E-08 TRR= 8.21230E-09
V(0:237) 2.500E+00 10(R) 8.366E-08 V(0:237) 2.500E+00 11(R) 9.189E-08 TRR= 8.22609E-09
```

Figure 4.8 Jitter Numbers with a Quite Substrate

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V(0:237) 2.500E+00 2(R) 1.762E-08 V(0:237) 2.500E+00 3(R) 2.577E-08 TRR= 8.15022E-09
V(0:237) 2.500E+00 3(R) 2.577E-08 V(0:237) 2.500E+00 4(R) 3.387E-08 TRR= 8.09764E-09
V(0:237) 2.500E+00 4(R) 3.387E-08 V(0:237) 2.500E+00 5(R) 4.213E-08 TRR= 8.26081E-09
V(0:237) 2.500E+00 5(R) 4.213E-08 V(0:237) 2.500E+00 6(R) 5.005E-08 TRR= 7.92228E-09
V(0:237) 2.500E+00 6(R) 5.005E-08 V(0:237) 2.500E+00 7(R) 5.814E-08 TRR= 8.09481E-09
V(0:237) 2.500E+00 7(R) 5.814E-08 V(0:237) 2.500E+00 8(R) 6.637E-08 TRR= 8.22514E-09
V(0:237) 2.500E+00 8(R) 6.637E-08 V(0:237) 2.500E+00 9(R) 7.445E-08 TRR= 8.08533E-09
V(0:237) 2.500E+00 9(R) 7.445E-08 V(0:237) 2.500E+00 10(R) 8.259E-08 TRR= 8.13631E-09
V(0:237) 2.500E+00 10(R) 8.259E-08 V(0:237) 2.500E+00 11(R) 9.066E-08 TRR= 8.07129E-09
V(0:237) 2.500E+00 11(R) 9.066E-08 V(0:237) 2.500E+00 12(R) 9.887E-08 TRR= 8.20957E-09
```

Figure 4.9 Jitter Numbers with a Noisy Substrate

substrate is 27ps and the jitter with a noisy substrate is 338ps. These numbers are reasonably close to the National Semiconductor measured results. It is difficult to compare these two results since two different techniques are being used to measure jitter and the jitter results from National are being visually determined from a scope printout. Additionally, there will be some error in the modeling system since all parasitic interactions are not modeled and simplifications were made to the entire process.

To compare the same type of jitter, post processing was done on the file containing the VCO output waveform. The waveform was cut so that each cycle becomes its own waveform and then the cycle waveforms are plotted on top of one another. This will show the jitter in the same manner as the measured data does. Figure 4.10 shows these results for both the quiet and noisy substrate. The voltage of 2.5 volts was chosen as the measuring location. The jitter with the noise turned off and turned on is 100 ps and 282 ps respectively. These results need to be taken for what they are worth. The process of cutting each cycle is not entirely accurate. The smallest time division in the waveform file is 100 ps. So the maximum error in each cycle is 100ps since the cycles were separated after the simulation was complete. It would be possible to have more time points placed in the

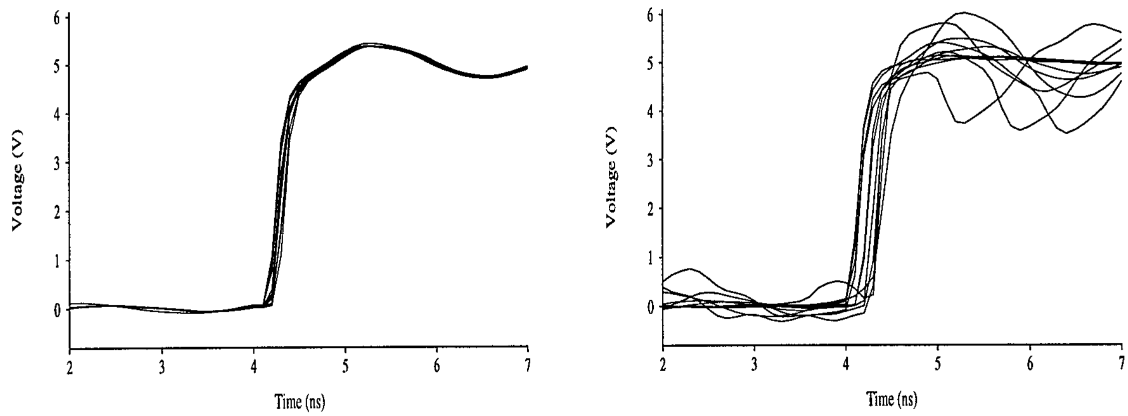

Figure 4.10 Period Jitter from Simulation Results.

output file, say 1ps steps, but this could slow the simulation dramatically. So the data in Figure 4.10 give a visual understanding of the jitter from the noisy and the quiet substrate, but their method of calculation is not particularly accurate.

The computer resources required to get these results were substantially higher than the Phase/Pump Filter circuit. The 802 transistor design required 128 Mbytes of memory and 5.1 hours to complete the RC reduction. Both simulations used the same reduced mesh. The simulation times for the noisy and quite circuits were 131.5 hours and 113.4 hours respectively. There is a large difference in times because when the input to the noise generator is not switching, all of that block's nodes converge faster than when the input is switching. Again, these results were accomplished by a Sun Sparc20 workstation.

From all the careful simplifications techniques and trying to model exactly how the measurements were taken, the simulated jitter results are reasonably close to the measured values. The period jitter pictures give a nice physical appearance to what is happening in the simulations, but their results are not as accurate as the cycle-to-cycle jitter measurements since the data comes from the simulator. There are two areas where the simulations do not exactly model the measured system. First is the measurement loading. This could possibly alter the measured jitter values. Second is the fact that the feedback loop from the PLL was cut to get these results. When this loop is intact, the input to the VCO will have some fluctuation due to the nature of a charge pump in a PLL. There would be bit more fluctuation on the input of the VCO which could potentially cause more jitter. This phenomenon was ignored since the peak-to-peak fluctuation from the feedback is significantly less than the fluctuation seen from substrate coupling. These results are very promising considering all the different parasitic interactions that are possible in a circuit this size. From these results, it is obvious that substrate current does have a dramatic effect on the operation of the circuit. Additionally, SNAPPLE has shown to be able to accurately model the non-ideal substrate in IC design. The next step is to evaluate the effectiveness of different guarding techniques.

4.2 Guard Structure Effectiveness.

4.2.1 Simulation Set-up

The simulations to test different guarding strategies can be simplified a bit from the previous simulations since jitter results will be compared to other simulation results, not measured data. The first simplification was to not include the effects of the Phase/Pump Filter at the input to the VCO. A DC voltage replaced the previous piece-wise linear approximation to a transient waveform. This allowed the simulations to monitor jitter incurred only in the VCO and allowed the effectiveness of guarding strategies in the VCO to be more accurately determined. The second simplification was to not include the additional output pad show in Figure 4.3. This added more transistors to the design which slowed down the simulation. Substrate coupling effects can still be seen without this pad and thus simulations could be sped up. The final simplification was to only keep the ohmic contacts in the blocks simulated. This made the process of creating the circuits easier and requires less memory in the reduction. These simulations were done with and with out pin parasitics. If pin parasitics were used, they are the same as Figure 4.2 .

For these simulations, three different guarding techniques will be evaluated including:

- A backplane contact to the bulk substrate
- A p+ ohmic contact guard ring around the analog circuitry.

- p+ ohmic guard structures around NMOS devices in the analog circuitry.

The effects of well guarding structures were not simulated since they have been proven to have almost no effect in an epitaxial process. Ohmic guarding was done on one particular section of the VCO, the V-I converters. These devices should deliver a DC value to a current-starved ring delay which controls the oscillation frequency. The outputs of this section are the nodes bias_n and bias_p. Ohmic guarding was also be done on all NMOS devices in the VCO.

Even though it may be difficult to create a backplane contact in chip fabrication, the simulations with the backplane contact modeled an ideal (not including pin parasitics) connection to the bulk substrate. In an epitaxial substrate process, there is no low impedance contact to the bulk substrate. This contact to the bulk substrate gives the substrate current a new path to exit the substrate holding the bulk substrate closer to the ideal potential. Since the substrate current does not have to exit through the epitaxial layer, the amount of substrate coupling should be dramatically reduced. Pin parasitics limit the effectiveness of a backplane contact since fast switching current leaving the backplane will cause a voltage fluctuation across the pin inductance.

In order to explain the difference between the p+ guard ring and the p+ ohmic guard structures, see Figure 4.11. The p+ guard ring structure is one large ohmic contact surrounding the analog devices. This guard ring adds many paths for current to exit the substrate and is thought to collect current before it reaches the analog devices. The ohmic guard structures, on the other hand, are placed as close as possible to individual devices to locally decouple these devices from the bulk substrate. The effectiveness of these different guarding structures will be shown in the next few sections.

There are eight different guarding configurations that were used. They included: A--no guard structures, B--no guard structures with a backplane contact, C--p+ guard ring, D--p+ guard ring with a backplane contact, E--ohmic guarding on the NMOS V-I converters in the VCO, F--ohmic guarding on the NMOS V-I converters in the VCO with a p+ guard ring, G--ohmic guarding on all the NMOS devices in the VCO, H--and ohmic guarding on all the NMOS devices in the VCO with a p+ guard ring. The noise signal for all of these simulations was a 50 Mhz square wave with 2ns rise and fall times. The DC

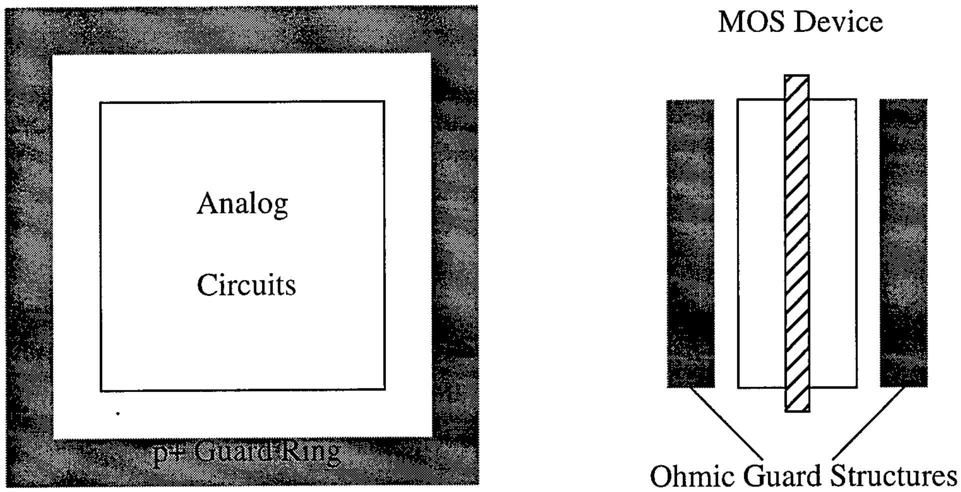

Figure 4.11 p+ Guard Ring and p+ Ohmic Guard Structure

input to the VCO was set to 1.58 volts as previously determined. Each simulation lasted for 100ns and jitter was measured on the output waveform.

4.2.2 Results with No Pin Parasitics

There are several basic differences from these simulations results compared to the previous results that included an output pad and accurate pin parasitics. The major differences are the shape of the output waveform, Figure 4.12, and the voltage fluctuation in the

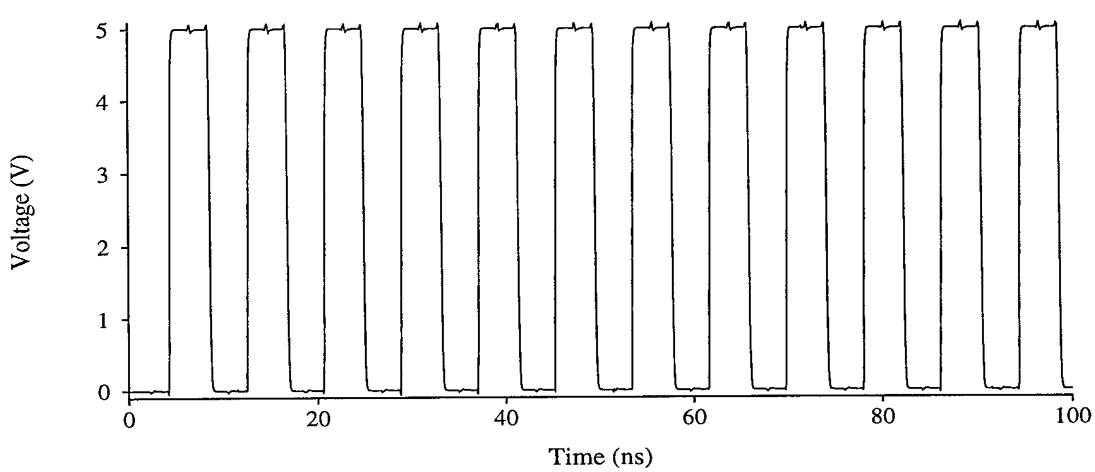

Figure 4.12 VCO Output Waveform with No Load and No Pin Parasitics

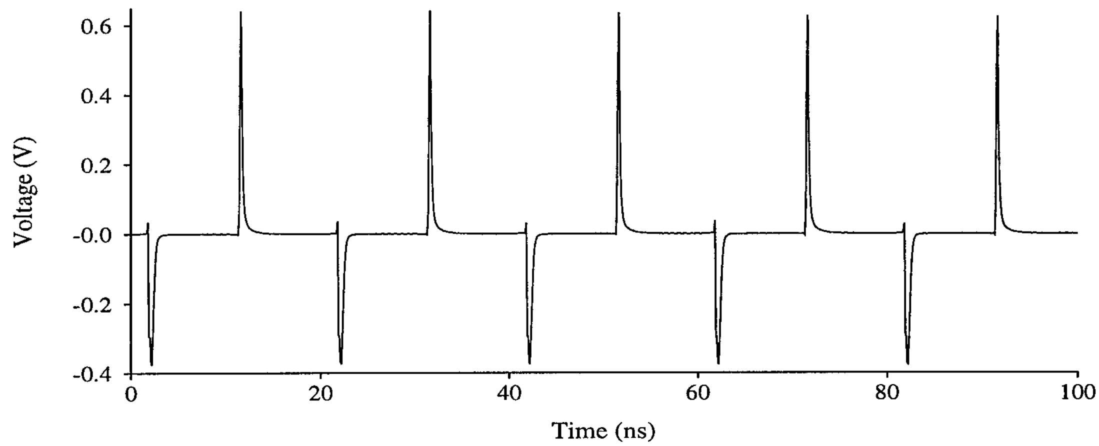

Figure 4.13 Bulk Substrate Waveform with No Load and No Pin Parasitics

bulk substrate, Figure 4.13. These waveforms are dramatically different from those in Figure 4.5 and Figure 4.6. The output waveform is quieter on in the constant regions of the waveform since now there are no pin parasitics that alter the power bias voltages. The backplane waveforms have about the same amplitude but different shapes. The smoothness of the curve in Figure 4.6 comes from the pin parasitics. There is some ringing in the substrate due to the inductance and capacitance on the pins. When these are not present, the bulk substrate waveform has sharp peaks and valleys. On average the reduction for these circuits required 2.5 hours and 86 Mbytes of memory on a Sun Sparc20 workstation. The simulation times ranged from 3 to 7 days since the simulations were done on both Sun Sparc20 and Sun Sparc10 machines.

Figure 4.14 shows the jitter results for the different guarding strategies discussed above. This bar graph shows that each guarding structure has its own unique effectiveness. Before a discussion on guarding effectiveness begins, there are other details of this circuit that can be analyzed to see what effect each guarding structure had. There are five other aspects that will be considered besides the jitter, including: the backplane voltage fluctuation, the voltage fluctuation under a sensitive NMOS device in the V-I converter section of the VCO, the fluctuation of the two outputs of the V-I converter section, called bias_n and bias_p, and the resistance from the bulk substrate to the analog ground node. All fluctuations are peak-to-peak. The digital ground resistance does not change since no new ohmic.

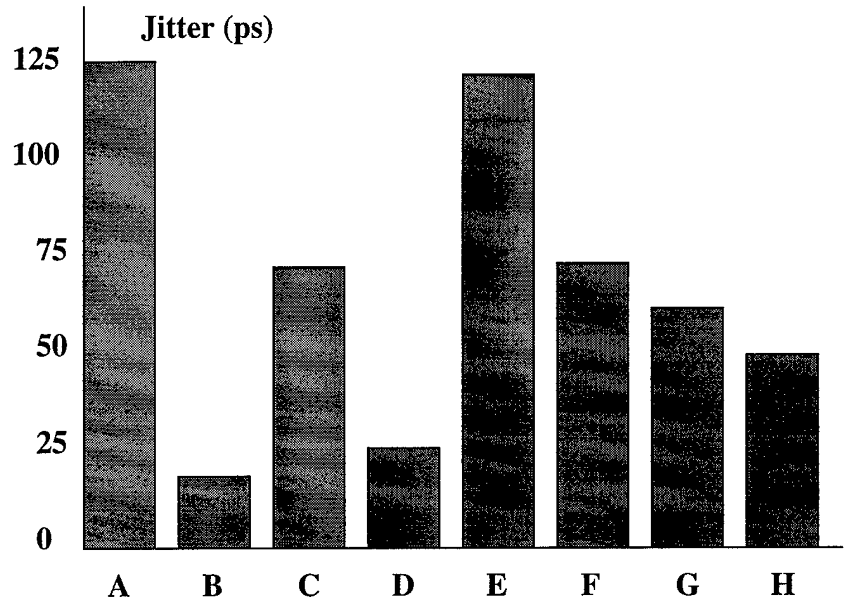

Figure 4.14 VCO Jitter Results from Circuits Described in the Text

Table 4.1 No Pin Parasitic VCO Simulation Results

Circuit	Bulk Substrate (Volts)	Sensitive Device (Volts)	Bias_n (millivolts)	Bias p (millivolts)	R to Clean Ground (Ohms)
A	1.026	0.632	72	59	22.8
B	0	10 m	1	1	22.8
C	0.671	0.431	49	40	8.9
D	0	10m	1	1	8.9
E	0.988	0.216	34	27	20.8
F	0.744	0.162	28	20	8.9
G	1.006	0.209	22	21	17.1
H	0.719	0.157	17	18	8.2

contacts were connected to it. This information is provided inTable 4.1. The first guarding technique, the backplane contact, greatly reduces the jitter in the case where no pin parasitics are included. Cases B and D are much better than all the other cases with respect to all performance categories. This is because any current that reaches the bulk substrate leaves through the backplane contact and so does not couple into the analog circuitry. There still is a tiny amount of jitter which comes from the operation of the VCO itself and any current that does not reach the bulk substrate.

The second guarding technique, the p+ guard ring, does not come close to the backplane contact's effectiveness, but it does help reduce jitter. It does this by reducing the resistance to the bulk substrate to the substrate bias and thus the voltage fluctuation at the bulk will decrease. Circuits C, F, and H all have p+ guard rings with other ohmic guard structures. All three of these test cases have similar jitter values, bulk substrate voltage fluctuations, and resistance to the backplane from the ground node. So, when the p+ guard ring is included, the injected current causes a lower voltage fluctuation in the bulk substrate from the lower resistance to ground causing lower jitter. Another simple example of this is comparing circuits A and C. The only difference is the p+ guard ring. The guard ring causes a 34 percent reduction in the bulk substrate, a 32 percent reduction in the sensitive NMOS substrate connection, and a 32 percent reduction in the bias_n and bias-p outputs. They all have the same percent reduction showing that the reduction of the bulk substrate fluctuation causes all other fluctuations to reduce the same amount. The reduction in resistance cannot be compared since there are other paths that the current can use to leave the substrate.

The third guarding technique, the p+ ohmic guard structures, also prove to be useful in reducing substrate coupling. Remember that these results are from simulations without pin parasitics. The best example of this is to look at simulations A and E. Here, the bulk fluctuation drops only 4 percent, yet the sensitive device fluctuation drops 66 percent and the bias_n and bias_p fluctuations drop approximately 53 percent. So some mechanism besides lowering the bulk fluctuation cased these fluctuations to drop. Case E has the NMOS devices in the V-I converters guarded. The sensitive device that is compared is in this section. An interesting observation is that even though these fluctuations dramatically decreased, the jitter did not. It is not clear if this is from the jitter not strongly dependent on the bias_n and bias_p, which are the outputs of the V-I converter, or the fluctuations did not occur at the proper times to effect jitter. Because there are no pin parasitics, the voltage fluctuations decay very fast and show now ringing so it is possible that these fast spikes on the outputs of the V-I converters occurred at the wrong time to effect jitter. All of the other ohmic guarding cases, F-H, show improvements over their counterparts without ohmic guarding. So it appears that ohmic guarding is very effective, especially since all of the ohmic guarding cases simulated added no extra circuit area to create.

All of these simulations show that the three different guarding techniques are effective with the backplane contact being the most effective and the full ohmic guarding with a p+ guard ring the next most effective. Additionally, the jitter with ohmic guarding around all NMOS devices reduces jitter more than the p+ guard ring which requires a substantial amount of chip area. These results hold true to the theory behind reducing substrate coupling effects as discussed in Chapter 2. The pin parasitics will have a dramatic effect since there is a substantial amount of fast switching current flowing through this substrate and circuit devices, thus the di/dt term that determines voltage drop over an inductor could alter the guarding strategies effectiveness.

4.2.3 Results with Pin Parasitics.

All of the same circuits were used as in the last section. The only difference is that now pin parasitics were included on the power and ground rails. The parasitics used are the same as shown in Figure 4.2. Additionally, if a backplane contact was used, it was given the pin values of just the ground line. There was no cross capacitance or mutual inductance included on the backplane contact. When these parasitics are included, the

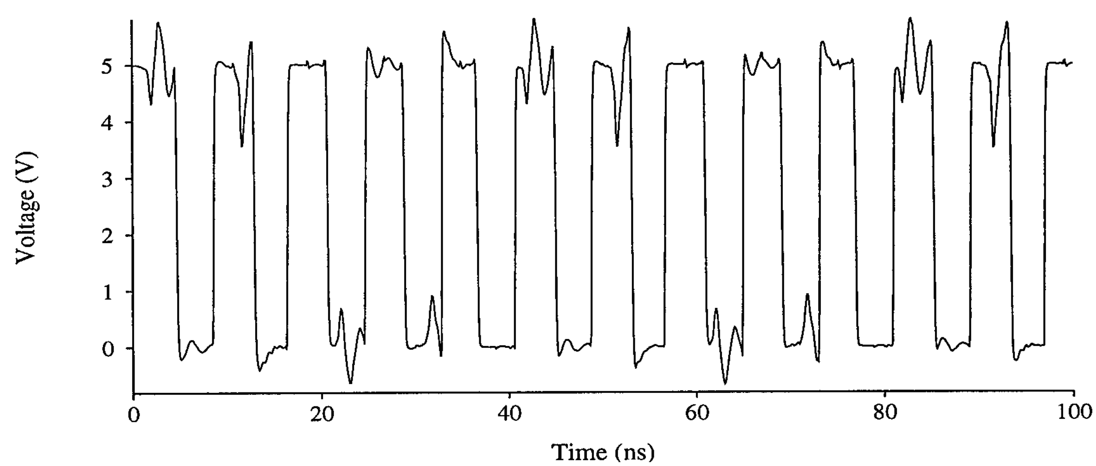

Figure 4.15 VCO Output Waveform with No Load and Pin Parasitics

backplane voltage fluctuation is similar to that shown in Figure 4.6. The effect of the parasitics can be easily seen on the output waveform Figure 4.15. The rise and fall times are very fast since the output is unloaded, but the pin parasitics cause spikes in the flat areas of the signal.

Figure 4.16 shows the jitter results when the pin inductances are included. These results are contrary to the results seen in the last section. Additional circuit nodes can be examined, Table 4.2, to help explain what is happening and more importantly why some structures seemed to worsen jitter when they improved it when no pin parasitics were included. The resistance is not included in this table since the same substrate models are used. The sensitive device is not included due to a lack of data.

A major effect of including the pin parasitics is the value of jitter increases dramatically. The previous maximum value was approximately 125 ps and the new maximum value is around 525 ps. Additionally, the voltage fluctuation on the bias_n and bias_p nodes are now measured in hundreds of millivolts as compared to tens of millivolts in the no parasitics simulations. Besides these basic differences for all the simulations, there are some very interesting jitter results that vastly differ from the no pin parasitic simulations.

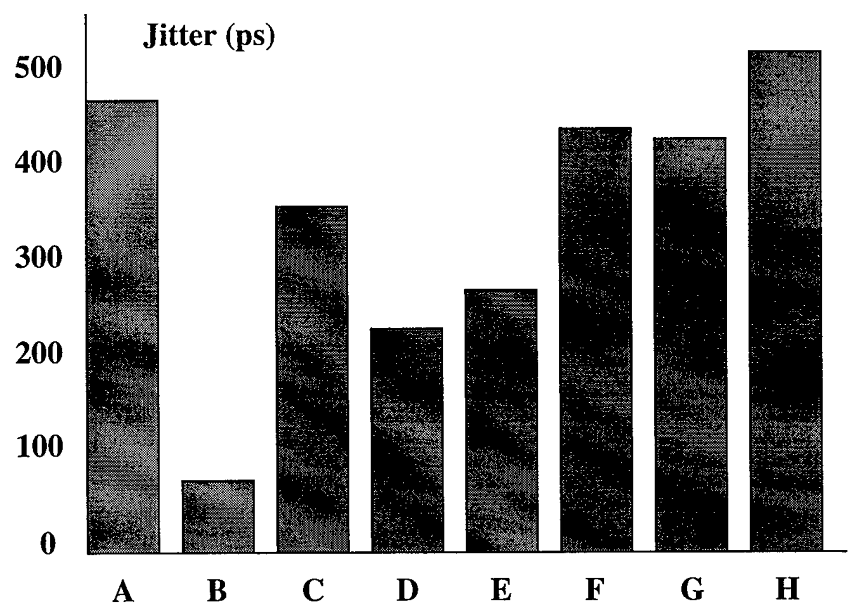

Figure 4.16 Jitter Results with Pin Parasitics Included

Table 4.2 Pin Parasitic VCO Simulation Results

Circuit	Bulk Substrate (Volts)	Bias_n (millivolts)	Bias_p (millivolts)
A	1.3	920	580
B	0.846	590	410
C	1.12	960	580
D	0.81	670	400
E	1.296	890	580
F	1.16	1020	660
G	1.239	920	670
H	1.17	1020	660

Each guarding technique alone, the backplane contact, the p+ guard ring, and the ohmic guarding, reduce the jitter by, 83 percent, 24 percent, and 43 percent respectively. The interesting results occur when combinations of guard structures were used. It would seem reasonable that the jitter performance should reduce if two guard structures are used instead just one. This is obviously not happening from these simulation results. One obvious case is comparing case D with case B. Circuit B has no guard structures but a backplane contact. D only differs in the inclusion of a p+ ohmic guard ring. Both of these circuits have similar fluctuations on the backplane, but a substantial difference in jitter, 80ps for case B and 240 ps for case D. Additionally, both the bias_n and bias_p fluctuations increase with the inclusion of the p+ guard structure. This trend is consistent throughout these simulations. When any guard structure is used with the p+ guard ring, the circuit performance deteriorates.

The data shows that circuit performance is deteriorating as the p+ guard ring is used with other techniques. So why is this guard structure, which is used to help reduce substrate coupling, increasing its effects? An explanation of what is occurring is helped by Figure 4.17. Rclean is the resistance from the bulk to the clean ground supply and Rdirty is the same resistance to the dirty power supply. The problem comes from the p+ guard

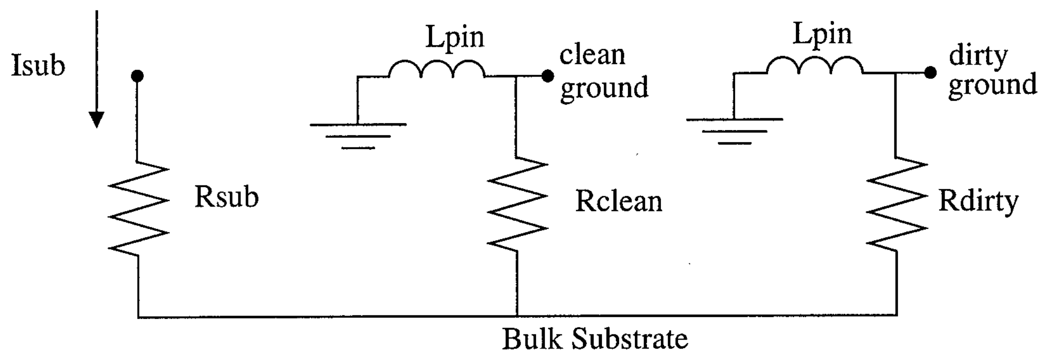

Figure 4.17 Simplified Diagram of Substrate Interactions

ring being biased by the clean ground line. This is the line that connects to all analog circuitry. So when the guard ring is not included, Rclean is about the same value as Rdirty. From the reduced mesh with no guarding structures, the Rclean is 23 ohms and Rdirty is 24 ohms. When the p+ guard ring is included, Rdirty stays the same, but Rclean reduces to 9 ohms. The reduction of Rclean has two effects on the circuit. First, the bulk substrate voltage fluctuation reduces since the impedance to ground has been reduced from the case with no guard structures. Second, the majority of substrate current leaves through Rclean since the impedance from the bulk substrate is less through this branch than through Rdirty. Without the guard ring, equal amounts of current leave through each. Now the transient current through Lpin for the clean ground signal has a higher current level causing a higher voltage drop across the pin inductance. This causes a higher voltage fluctuation at the ground node for the analog devices.

So by including the p+ guard ring biased by the clean ground node, the voltage fluctuation under sensitive devices will decrease, but the ground bounce will increase. Since ground bounce is a first order effect and a changing substrate bias is a second order effect, the increased ground bounce deteriorates jitter performance even though there is less voltage coupled into the sensitive devices' substrate connections. The vast majority of the substrate current injected into the substrate comes from the digital (or dirty) positive power supply. Since the p+ guard ring is connected to analog (or clean) ground, a majority of the substrate current leaves through the clean ground causing significant ground bounce. There are two obvious solutions to this problem. The first is to reduce the amount of pin parasitics by having more than one pin for each bias. The extreme case of this, when there are no pin parasitics, is shown in the no pin parasitic simulations. The second solution is to hook the p+ ring to a different ground node. This should collect a majority of the substrate current without causing ground bounce for the analog circuits.

4.2.4 Effects of Guard Ring Bias Node.

In order to test the effects of the guard ring bias when parasitic pin values are included in the simulations, a simple test circuit was simulated before the VCO and noise generator to save time. The circuit used is the same as Figure 2.9 with a simple inverter as the noise generator and an NMOS current source as the analog device. The parasitics on the pins were simplified to be 6nH inductors on each pin. The simulation set up is identical to the simulations done in section 2.3 except for the inclusion of the pin inductance.

The four different circuits to be compared are A--no guard structure, B--p+ guard ring hooked to clean ground, C--p+ guard ring hooked to dirty ground, and D--p+ guard ring hooked to a separate ground. The primary measure of goodness is how much peak-to-peak fluctuation there is on the output of the analog current source. The voltage fluctuations on the backplane, and the two ground nodes before the parasitic pins can also be used to gain insight into what is happening in these simulations. The voltage fluctuation on the output is compared in Figure 4.18 and the additional fluctuations are shown in Table 4.3.

The results from these simple simulations show some very interesting results. The first important results shows what was discussed previously about the guard ring being hooked to the clean power supply. When this is the case, the voltage fluctuation in the bulk decreases, but the voltage fluctuation on the clean ground node increases since more transient current is flowing through the inductor hooked to that ground node

It was previously thought that hooking the guard ring up to the dirty ground node would help this problem. These results show that this is not the case, but the fluctuation got a little bit worse than when hooked to the clean ground. By comparing the statistics from the dirty ground case to the clean ground case, the reason for this can be explained. The major difference is that the voltage fluctuation on the backplane dramatically

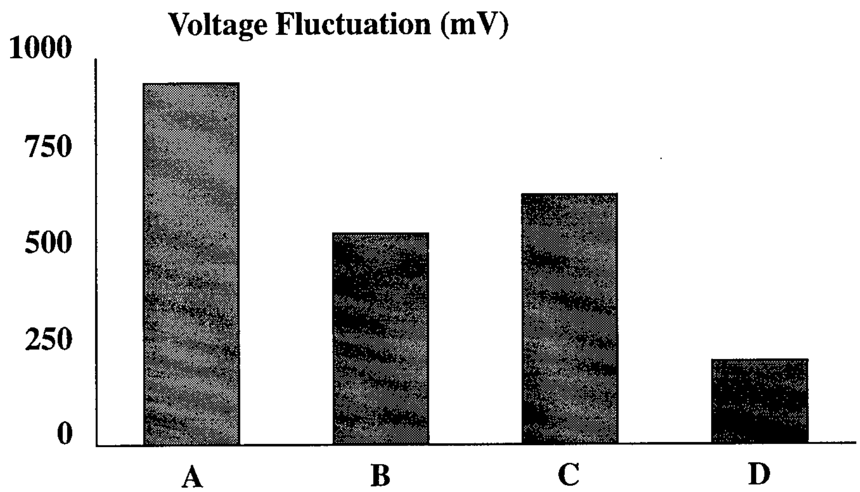

Figure 4.18 Results from p+ Bias Simulations

Table 4.3 p+ Ring Bias Simulation Results

Circuit	Output (millivolts)	Bulk Substrate (millivolts)	Clean Ground (millivolts)	Dirty Ground (millivolts)
No Guard Structures	930	556	85.2	506.6
p+ Ring Clean	547.7	227.2	151	514.8
p+ Ring Dirty	679.1	412.9	100.4	452.3
p+ Ring Separate	214.7	224	40.9	515

increased and the fluctuation on the clean ground dropped. The rising of the devices substrate connection and dropping of the ground node cased the voltage fluctuation to increase slightly. The reason for the ground fluctuation decrease is less current is flowing through the clean pin inductance. The reason for the backplane fluctuation increase is a not quite as obvious. The explanation again uses the simple diagram located in Figure 4.17. When the p+ ring is hooked to the clean or dirty ground node, the resistance from that node to the bulk substrate will be small compared to the other resistance. This effectively couples the bulk substrate to the node biasing the guard ring. When this guard ring is hooked to the dirty ground node, the bulk substrate is strongly coupled to it. The dirty ground node will fluctuate due to substrate current leaving the substrate and, more importantly, transient current drawn through fast switching digital devices. The fluctuation on the dirty ground is significantly greater than the clean ground and so the bulk substrate's fluctuation rises when hooked to dirty ground. To further show how the ring bias effects circuit operation, the waveforms from these simulations will be shown. Figure 4.19 shows the waveforms for the guard ring hooked to the clean ground node and Figure 4.20 shows the waveforms for the guard ring hooked to the dirty ground node. Both figures show the clean ground node, the dirty ground node, and the backplane fluctuation. When the guard ring is hooked to clean ground, the bulk substrate's behavior is very close to the clean ground nodes behavior. The same is true when the ring is biased by dirty ground.

The case where the guard ring was biased by a separate ground node gave the best results. Now, less current is leaving the analog ground node reducing the effects of ground bounce on the analog circuits. Also, the bulk substrate is not strongly coupled to the dirty ground node since the low resistance path is to the separate ground node. The only drawback is that an additional pin must be used to bias the guard ring.

Now that the bias fundamentals have been worked out on a small example, the same guarding strategies were used to examine the same effects on the VCO and the noise generator. Figure 4.21 shows the jitter results for all four of these cases. Table 4.3 shows additional results from these simulations. The trends from these results are identical to the simple simulation results. The jitter performance is not much different from when the ring is biased by either the clean or dirty ground node. Also, the bulk substrate fluctuation increases when the bias is switched from the clean to dirty ground node. These simulations did not monitor the fluctuation on the ground nodes, but the Bias_n node can tell the same story. When the bias was switched to the dirty node, the fluctuation of Bias_n dropped a small amount even though the bulk substrate increased. This means that the fluctuation on the clean ground node must have dropped. This is consistent with the findings from the smaller test cases. Additionally, the case where the p+ ring had a separate bias was easily the best performer.

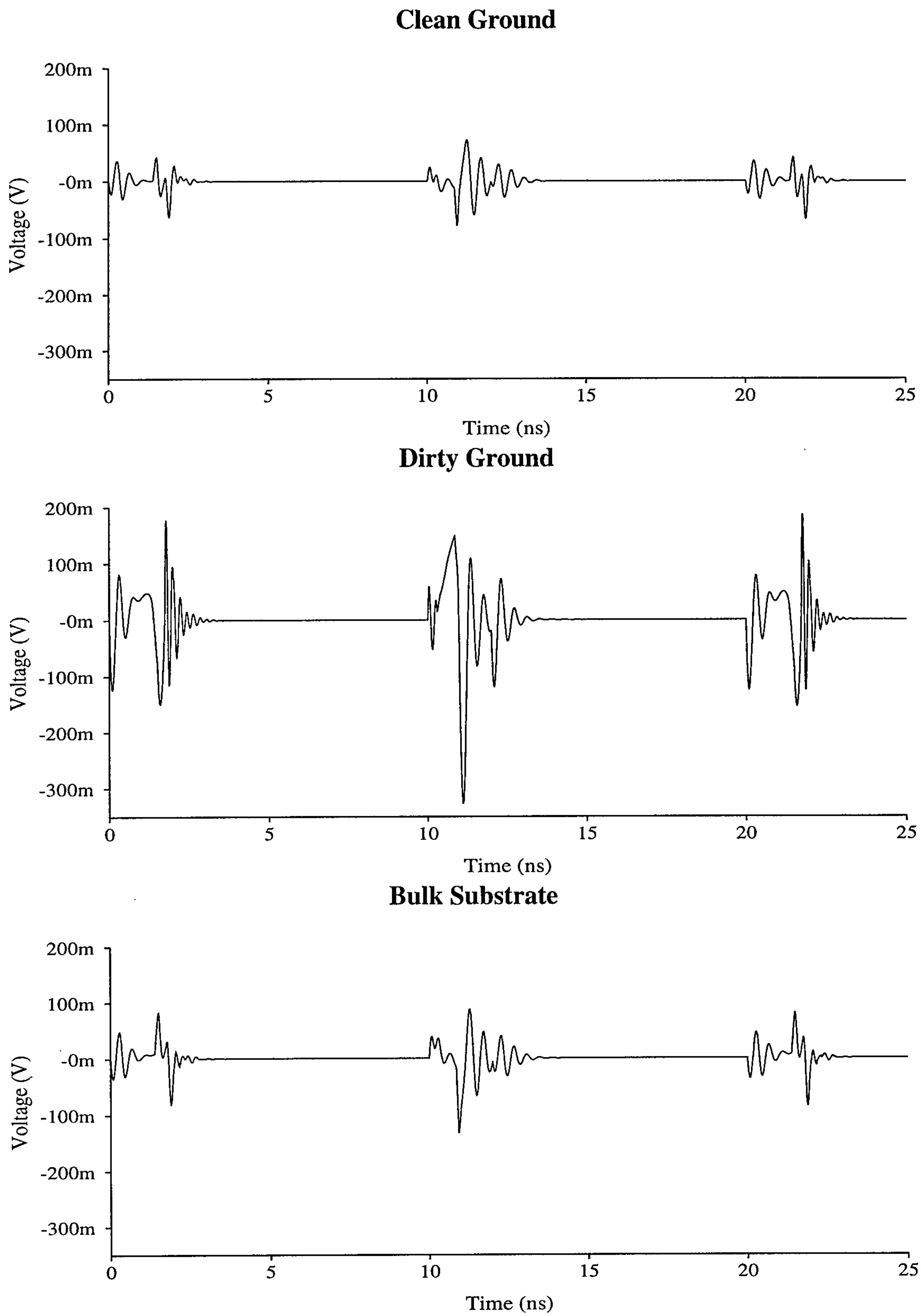

Figure 4.19 Voltage Waveforms for Clean Bias on p+ Guard Ring

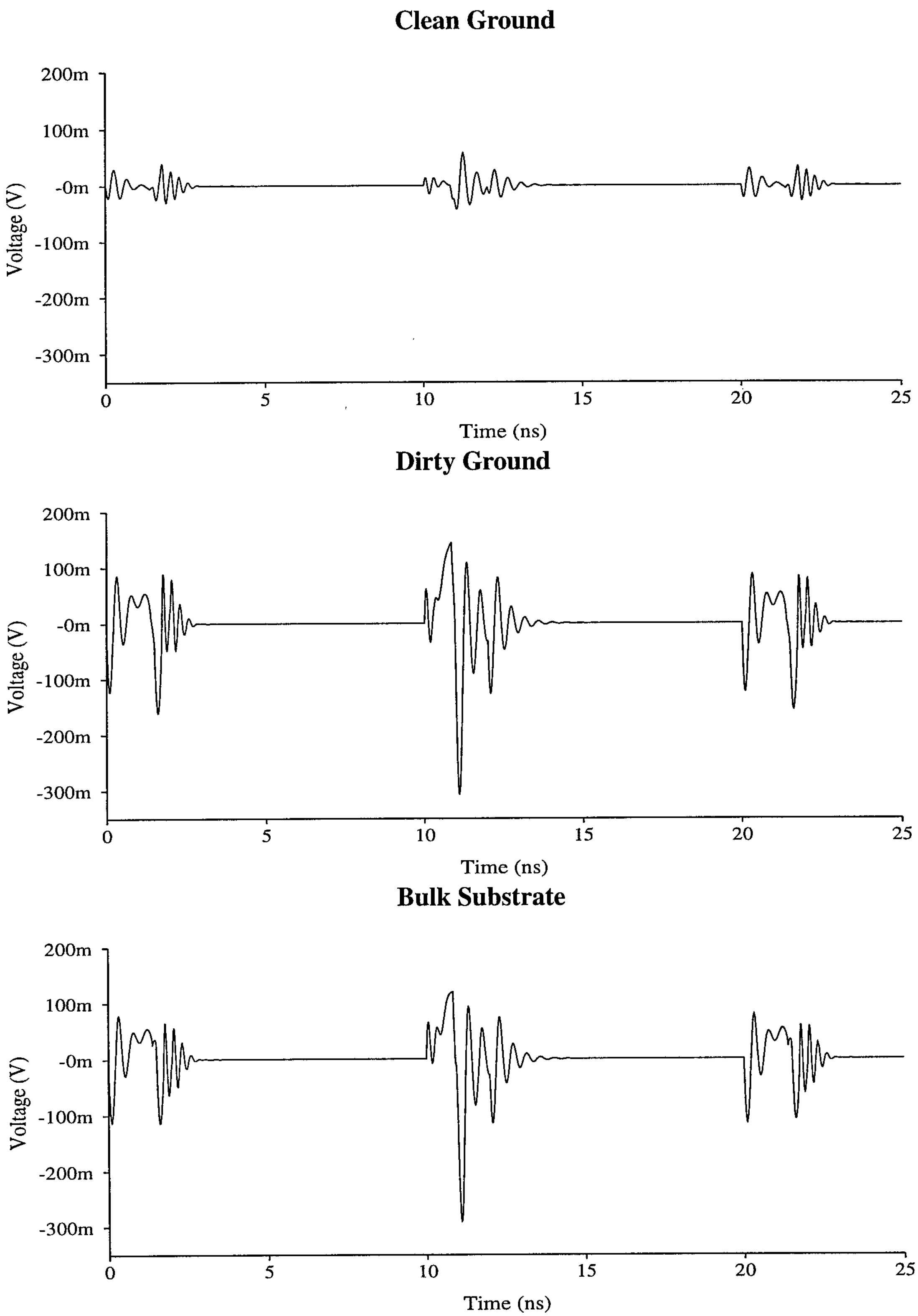

Figure 4.20 Voltage Waveforms for Dirty Bias on p+ Guard Ring

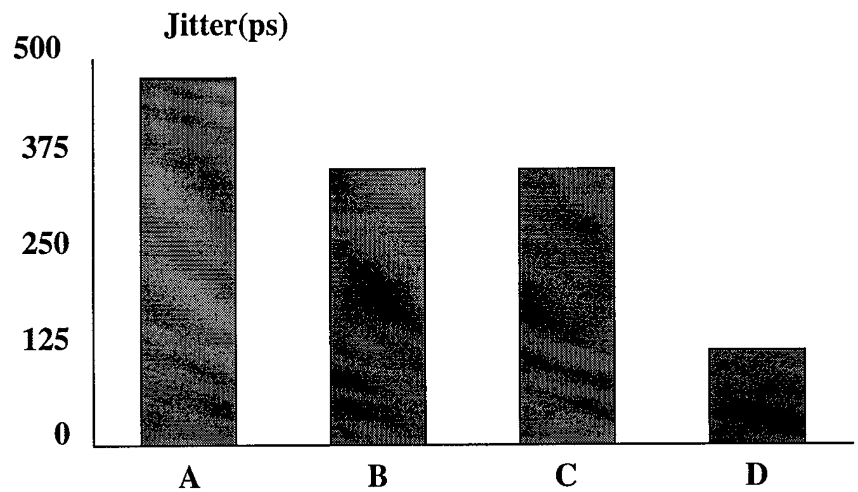

Figure 4.21 Jitter Results with 3 Different p+ Biases

Table 4.4 VCO p+ Ring Bias Simulation Results

Circuit	Bulk Substrate (millivolts)	Bias_n (millivolts)	Bias_p (millivolts)
No Guard Structures	1300	920	580
p+ Ring Clean	1120	960	580
p+ Ring Dirty	1391	930	596
p+ Ring Separate	899	619	406

The simulations with the parasitic pin values included have shown some valuable information on the effectiveness of different guarding strategies for mixed analog/digital designs. On a more general note, they have shown the importance of using the parasitic pin values in circuit simulation. In these simulations, guarding strategies that were effective without pin parasitics were proven to be ineffective when they were include. Getting accurate models for package pins is not a trivial task. Every effort to get a detailed pin package model should be taken when doing detailed circuit simulations, especially when the substrate is modeled.

The effects of pin parasitics will not magically disappear and so designers must do what they can to eliminate their effects. The obvious solution to reducing the effects of pin parasitics is to provide more than one pin for each power and ground node. This puts the pin inductances in parallel thus reducing their effects. An alternate way which may be more effective if the number of pins is limited is to have three separate bias systems, one for the analog devices, one for the digital devices, and one for the guarding structures. Of course, this is only possible if extra pins are available in the package.

4.2.5 General Mixed Signal Guarding Guidelines.

From the simulations with and without the pin parasitics, much information has been gathered on how to reduce the effects of substrate coupling in mixed signal designs built in an epitaxial substrate. A backplane contact is very helpful but it may not be practical in designs today. There are still effective techniques that can be employed from the physical layout. From this research, several guidelines can be established for an epitaxial process.

- 1. Include ohmic guard structures near noisy devices to prevent substrate current from reaching the bulk substrate.
- 2. Include as many ohmic contacts hooked to a separate power supply to reduce the bulk substrate voltage, to draw current away from the analog power bias system, and keep the bulk substrate from being coupled to the dirty ground node.
- 3. Include ohmic guard structures near sensitive devices that are not built in wells to decouple these devices from the bulk fluctuation.
- 4. Take every effort to reduce the effects of the pin inductance on the power buses by either giving multiple pins to each node, or breaking up the bias system in smaller systems with their own pin or pins.

If design parameters allow for these guard strategies, then it should be possible to significantly reduce the effects of substrate coupling in mixed signal designs built in an epitaxial process. These are not guidelines that are a must but each one will help if biased correctly. This gives the designer new possibilities on how to design for substrate coupling and should allow aggressive protection strategies to go along with aggressive designs. None of these results would have been possible if it had not been for the accuracy and efficiency of the software used in the SNAPPLE system.

Chapter 5 Capacitor Example

During the research on the PLL, National expressed interest in ways to make a capacitor immune to substrate coupling. Even though the PLL study did not focus on the capacitors built in the design, their response to substrate coupling is of interest. The filter block of this circuit consists almost entirely of capacitors built in the substrate. A technique to make these capacitors immune to substrate noise would only help the performance of this circuit. This provides a great opportunity to show the usefulness of SNAPPLE on a very small aspect of an entire design.

The capacitor in question is built using a PMOS device. Capacitors built from devices are commonly called MOSCAPs. Figure 5.1 shows how this capacitor is built.

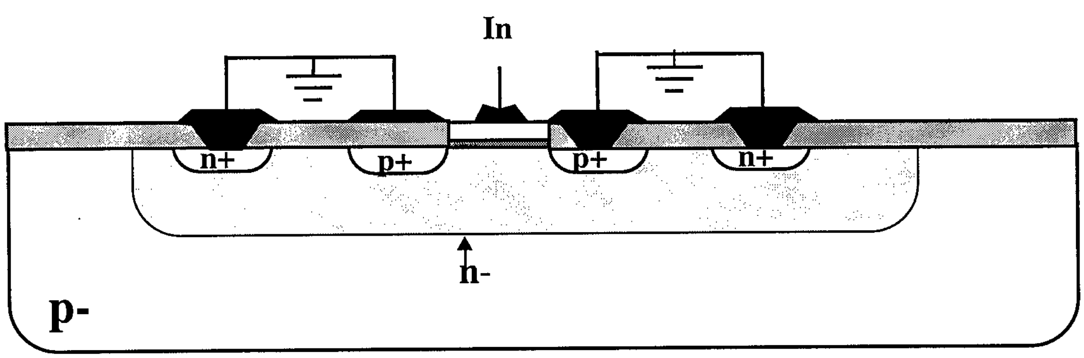

Figure 5.1 MOSCAP Cross-Section

The capacitor is again built in an epitaxial process and only the epitaxial layer is shown in Figure 5.1. Since the ohmic contacts, source, and drain are at ground potential, there is zero current flowing through this device. The majority of capacitance is from the gate to the bulk of the device which in this case is the device well. In order to test capacitor designs for noise immunity different device configurations will be used.

5.1 Capacitor Simulations

There are four different capacitor configurations that were simulated. Each simulation had the same design, as shown in Figure 5.2. The only difference between simulations was how the capacitor is built. The inverter is included to drive the capacitor. It was given an input of zero volts so that the voltage sitting on the capacitor was five volts. The noise generator is one output pad loaded with a capacitor. This was driven with a 50 MHz square wave with 2ns rise and fall times. The voltage fluctuation on the capacitor and the bulk substrate are the measures of goodness for these simulations.

The first capacitor configuration, A, is a single PMOS device with the gate having the dimension of 105μ by 87μ. n+ ohmic contacts are included around the devices in the well. A p+ guard ring is included around the outside of the device well. The second configuration, B, is four PMOS devices with the dimension of 53μ by 43μ built in the same well. n+ ohmic guard rings are included around each device and a p+ guard ring is included around their well. The third configuration, C, is identical to the second except that each of the devices are built in separate wells. A n+ guard ring is placed around each device and a p+ guard ring is placed around each well. The fourth capacitor configuration, D, is identical to the second except that now the capacitor is broken into sixteen blocks

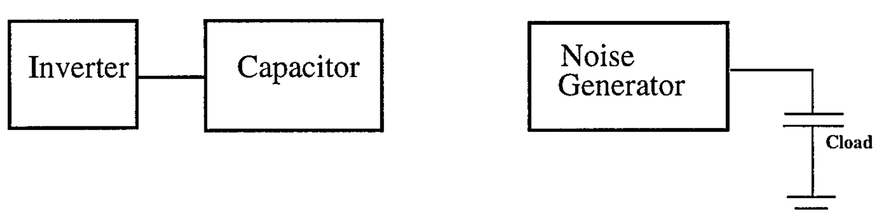

Figure 5.2 Capacitor Simulation Block Diagram

with the dimension of 30μ by 19μ.

The first set of simulations was to ensure that the equivalent capacitance of these test cases are identical. This was done by hooking a 1 ohm resistor to the gate of the devices used for the capacitor and doing an AC sweep. Since the resistance of this low-pass filter configuration is 1 ohm, the 3dB frequency of this filter simplifies to that in equation (5.1). Since the AC amplitude in the simulations is one, the frequency where the

$$C = \frac{1}{2\pi f_{3dB}} \tag{5.1}$$

transfer function drops to 0.7071 is the 3dB frequency. Table 5.1 shows that the four different capacitance configurations have approximately the same value.

Table 5.1 Equivalent Capacitance Values

Circuit	3dB Frequency (GHz)	Capacitance (pF)
A	12.64	12.59
B	12.66	12.57
C	12.66	12.57
D	12.56	12.67

The second set of simulations was to see how much noise couples through the capacitor. This is done with a transient analysis of the circuits with the substrate model included. It is not good enough to just compare how much the voltage fluctuation on the capacitor decreases since the number of ohmic contacts in each set-up is different. A good improvement comparison can only be done by comparing the voltage fluctuation reduction on the capacitor compared to the reduction of the bulk node of the device. This data is shown in Table 5.2. The reduction software required 26 minutes and 55 Mbytes to finish. The average simulation time was approximately 7 minutes. This was achieved on a Sun Sparc20 workstation.

The data shows that by breaking up the capacitor into smaller pieces but keeping the same gate area, its performance in a noisy substrate improves. Physically when a capacitor is broken up into smaller units, each piece is further decoupled from the bulk substrate. In these examples, the substrate current must first couple through a well deple-

Table 5.2 Substrate Coupling Statistics

Circuit	Bulk Substrate (millivolts)	Reduction (Percent)	Capacitor (millivolts)	Reduction (Percent	Area (μm^2)
A	657	0	88	0	13280.4
B	625	4.9	30.9	64.9	17242.2
C	603	8.2	31.1	64.7	19577.2
D	590	10.1	14.5	83.5	24004.7

tion region and then into the device. Once current is injected into the device well from the bulk substrate, the smaller the device, the less distance this current must travel to an ohmic contact causing less voltage fluctuation under that device. The drawback is the substantial increase in circuit area. It is recommended to keep the broken capacitor devices in the same well. For the case C where there were four segments with individual wells, the performance was no better than case B where there was only one well, but the area of the circuit is 13.5 percent larger. Thus, if a capacitor is broken into multiple devices, there is no advantage over placing each device in a separate well.

This simple test case for the performance of MOSCAPs in a noisy substrate prove two important points. First, there is a design trade-off between noise immunity and circuit area for capacitors. It is up to the designer to determine the how good of a capacitor is needed and then fit it into the smallest area possible. Capacitors do not have to be designed to be immune to noise if other techniques are used to prevent a large bulk substrate fluctuation. Such techniques include close ohmic guard rings around noisy devices to keep noise from reaching the bulk substrate, and many ohmic contacts connected to a separate ground supply to reduce the resistance to the bulk substrate.

The second important point has to do with the usefulness of SNAPPLE. The results from these four circuits were achieved in approximately four hours. This is much more realistic than the VCO and noise generator example in Chapter 4. It took approximately 12 days to get the results from four different configurations of that circuit. The SNAPPLE system may be designed to handle designs of over 1000 devices, but the time required to get meaningful results may be too lengthy to be useful in a circuit's design lifecycle. Work on just one circuit element has show how to achieve aggressive noise reduction strategies with out needing to simulate the entire circuit. SNAPPLE has been used to shown how guard structures can reduce substrate coupling in both large and small circuit blocks. Each has their own advantages so it is up to the designer to decide what is necessary. Small circuit examples can show how circuit components will react to substrate noise, but many times larger systems must be simulated to get an overall circuit performance prediction.

Chapter 6 Conclusion

The National Semiconductor Phase-Locked Loop has been an excellent case study for substrate coupling. The design includes both sensitive analog circuits and large, noisy digital circuits on the same die. Despite the efficiency of the SNAPPLE system, a substantial amount of the research and engineering effort was involved in simplifying the circuit and the substrate model so that simulations could occur. Once the simulations were feasible, modeling the non-ideal substrate provided a vast amount of knowledge. Not only were VCO jitter results correlated to silicon measured jitter results, but the effectiveness of many different guarding structures was evaluated.

The usefulness of the SNAPPLE tool has been demonstrated for aggressive mixed analog/digital designs. The time for aggressive designs and heuristic guarding techniques has past. In this case study, several very important improvements were discovered that can dramatically decrease substrate coupling and minimize the circuit area. Well guarding structures should not be included in an epitaxial process. A p+ ohmic guard ring should be included and biased by a separate ground line, not the clean nor the dirty ground. Also, ohmic contacts should be placed as close as possible to noisy and sensitive circuits to collect current before it enters the bulk substrate and decouple devices from the bulk substrate. These different techniques seem to make sense now that the work has been done, but for designers who do not have access to a tool like SNAPPLE, these guarding techniques may not be obvious.

The reality of substrate coupling analysis tools is that computer resources will probably never catch up to the requirements for state-of-the-art designs unless dramatic improvements are made to the tools. Computers will get faster and have more memory, but VLSI designs are getting smaller with more getting packed into each chip. Despite this no-win situation, substrate coupling tools are still a valuable tool in mixed signal designs. Large systems can be smartly separated into pieces and simulated separately. Designs today are becoming more complicated and so even breaking a circuit into a single block may exceed the limitations of computer systems. SNAPPLE can be used on very small circuits, consisting of just several devices, to determine the effects of different guarding techniques. Then the useful guarding strategies found from simple test cases can be used in the creation of the larger systems. SNAPPLE has shown valuable results in the National Semiconductor circuit, and will be valuable in the future for mixed signal designers to predict the effects of substrate coupling and substrate coupling reduction techniques.

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