Microlithographic Mask Development (MMD)

CDRL H007: Option 1 Contract Summary Report
CDRL H004: Contractor Progress, Status, Management Report

14 March 1997

Contract Number N00019-94-C-0035

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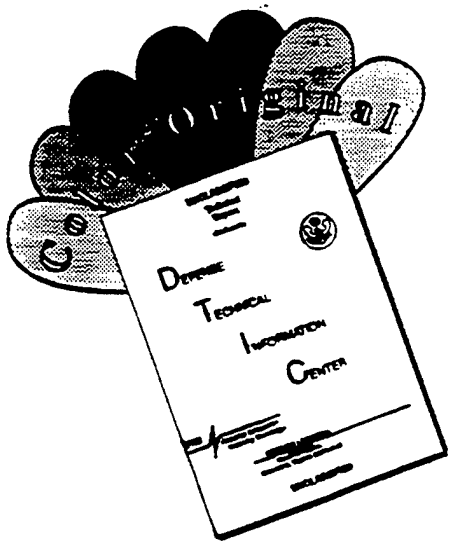

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14 March 1997

ENCLOSURE NO: 97-MMD-LMFS-00026

Prepared for:

Naval Air Systems Command
1421 Jefferson Davis Highway
Arlington, VA 22243-5120

Contract Number N00019-94-C-0035
Lockheed Martin Federal Systems
Manassas, Virginia

Lockheed Martin Federal Systems, Manassas, Virginia

Certification of Technical Data Conformity

The Contractor, Lockheed Martin Federal Systems, hereby certifies that to the best of its knowledge and belief, the technical data delivered herewith under Contract Number N00019-94-C-0035 is complete, accurate, and complies with all requirements of the contract.

3/13/97
Date

D.V. Jamba for S.G. Schnur
S.G. Schnur, Program Manager

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1.0 Introduction

This document provides the data required under contract N00019-94-C-0035 in accordance with CDRL H007, Option 1 Contract Summary reporting on the period from 25 January 1996 through 25 January 1997, and CDRL H004, Contractor Progress, Status, Management Report, 4Q96, covering the period from 25 November 1996 through 28 February 1997.

Program Summary

During this reporting period, manufacturing focus has been on both building gold customer masks and developing the refractory mask process. Ongoing research projects are shown in Table 1 and Table 2. Completed projects are highlighted in the tables.

Table 1 provides a concise, aggressive schedule to meet tighter specifications for x-ray mask performance. Each column lists by quarter the specifications for product and the beginning of projects to meet the improvements. Table 2 contains MMD objectives for the refractory metal process. The technology path by quarter comprises the goals and the learning initiated by quarter that must be met to reach these goals for the year. The learning activities are dependent upon each other. This report focuses in detail on the status of these activities.

Status reports from IBM Yorktown Research and SVGL are included as Appendix A and Appendix B, respectively.

Table 1. 1996 MMD Objectives, Baseline Technology				
	1Q96	2Q96	3Q96	4Q96
Line Monitor	*0.25μ product mask 10 defects @ 120 5 starts/wk, 0.25μ IP=35, CD=20nm*	*0.25μ product mask 10 defects @ 120 5 starts/wk IP=35, CD=20nm*	*0.18μ product mask 10 defects @ 90 5 starts/wk IP=35, CD=20nm*	*0.18μ product mask 10 defects @ 90 5 starts/wk IP=35, CD=20nm*
Product Applications	**Polaris Plutus** *BQM* **Nighteagle**	**LTM5 LTM4**	*LMFS*	*PXLA product masks* **Phoenix/1Gb test site**
MMD Contract Deliveries	**0.25μ/0.18μ masks**	**0.25μ/0.18μ masks**	**0.25μ/0.18μmasks**	*0.25μ/0.18μ/0.13μm masks*
Technology Learning				
	High MW PMMA Evaluation	**Adv E-beam RFI for 0.13μ/0.10μ**	*Multipass writing with offsets (XE-P0)*	*Insitu develop station*
	Suss mfg resist coater	*** Define single wafer membrane etch**	*PSE reduction via modeling*	**IP sub-25nm (Au) Nighteagle pattern**
	Conductive poly-analine coating evaluation		*Edge slope optimized for 0.13μ*	**Final mask clean implementation**
	Leica 2020		*XE-P0: upgraded laser*	**XE-P0: Beam heated apertures P5 data path**
	XE-P0: Ferrite hole AIX 4		**New proximity correction software (dose 6) started**	

* Capital delayed until 1997

Phoenix - IBM 1Gb DRAM test site
Plutus - IBM 0.1μm development test site
NIGHTEAGLE - 64Mb SRAM 0.18μm test vehicle
LTM4 - High resolution ALF line monitor
LTM5 - 0.15μm resolution ALF line monitor

Table 2. 1996 MMD Objectives, Refractory Metal Process				
	1Q96	2Q96	3Q96	4Q96
Technology Path	*PXLA/Hoya TaX Evaluations SiC qualifications*	*PXLA/Hoya TaX Evaluations SiC qualifications*	*BTV TaX etch/Hoya SiC plus TaX blanks*	*BTV 100% prototype capability for refractory metal with Hoya substrates*
Deliveries	*N/A*	*1st mask manufactured (random walk)*	*0.25μ mask, BTV early learning*	*0.25μ prototype mask, 0.18μ and below demonstrations*
Checkpoint for Mfg Insertion	*3/31/96: absorber stack specification*	*6/30/96: stack etch bias = 50 BEOL IPD = 50 CD = 30*	*9/30/96: IP = 60, CD = 30 Defects = 100@120 0.25μ NIGHTHAWK*	*12/1-15/96: IP = 35, CD = 25 (0.25μ & 0.18μ) Defects = 10@120 16% yield(20 masks)*
Technology Learning				
	SiC Rad damage assessment	**Hoya/SiC qualification**	**Hoya stack qualified**	**SNR200 proximity defined**
	NTT-AT stress tool evaluation started	**1st Ta XE-P0 mask written**	*Verify mask performance on SVGL started*	*Checkpt for MMD line conversion*
	Order Ta RIE tool PXLA process defined	**Moto etch process optimized**	*Ta etch process transferred to MMD started*	*Radiation study completed*
	New back etch process defined	**SNR200 resist/ process optimized**	*Order new back-side etch tooling started*	*Mask cleaning/KLA inspection process defined - started*
	SNR200 resist/ process defined			*2.1mm wafer conversion started*
				Evaluate thick SiC
NIGHTHAWK - 64Mb SRAM 0.25μm test vehicle				

Highlights

- Contract deliverables through November, 1996 for prototypes have been filled (Figure 1).
- Transitioned from 0.25μm NIGHTHAWK line monitor to 0.18μm NIGHTEAGLE.
- Evaluation of conductive topcoat polyaniline has been completed, and the coating capability is currently being qualified in Burlington.
- Image size 3σ has improved on the line monitor. Both e-beam tools average below 20nm, with EL-4 P0 obtaining 13nm on a NIGHTHAWK with the regular process and 11nm with polyaniline.
- SNR 200 negative resist process has been qualified for both gold absorber negative masks and refractory absorber positive masks.
- Hot plate bake of membranes for both SNR 200 and UVIII has been implemented.
- Defect sensitivity on KLA has been reduced from 120nm to 90nm for all line monitors.

- Defect-free Plutus P1 masks (0.13μm) and defect-free Phoenix DT masks (0.18μm) were fabricated and shipped during 1996.
- The High Molecular Weight PMMA Blanket Pre-exposure project is completed (reference CDRL G004, 96-MMD-LFSC-00073).
- The manufacturing Karl Suss coater process qualification for PMMA resist was completed on 15 April 1996 and the product qualification was completed on 28 May 1996.
- The Leica 2020 factory acceptance and site acceptance were completed and the tool was installed in the MMD.
- A defect-free silicon carbide mask was built during 1996. Hoya was conditionally qualified for SiC deposition.
- Short and long-term membrane etch strategies for refractory masks were defined. Immersive Compact etch will be used in the short term, with Fountain Cup the long-term solution.
- Absorber etch system was received from Plasmatherm. Qualification is complete and process optimization is ongoing.
- The Plasmatherm plating base removal system was modified to act as an SiON etch station.
- A low-stress nitride deposition system was ordered.
- Proximity algorithm optimization for refractory masks was completed (reference CDRL G004, 97-MMD-LFSC-00002).
- Initial evaluation of DOSE6 proximity algorithm for both PMMA and SNR was completed.
- Refractory metal film material, TaSiNx, and hard mask material, SiON were chosen.
- The first refractory 0.18μm NIGHTEAGLE masks were shipped to ALF.
- Initial refractory mask benchmarking using the 0.18μm NIGHTEAGLE pattern was completed. Results were comparable to gold masks for image size and image placement.

0.25u VALIDATED

- defect free, I/P = 36 (goal is 30), I/S = 24 (goal is 20), NIGHTHAWK, Qty = 2

	F	M	A	M	J	J	A	S	O	N	D	J
Schedule	2											
Actual	2											

0.25u PROTOTYPE

- not defect free, I/P =60 (goal is 36), I/S = 40 (goal is 24), TALON or NIGHTHAWK, Qty = 66

	F	M	A	M	J	J	A	S	O	N	D	J
Schedule	9	9	9	0	0	0	3	4	5	9	9	9
Actual	9	9	9	0	0	0	3	4	5	9	4	

0.18u PROTOTYPE

- defect free, I/P = 44 (goal = 20), I/S = 30 (goal is 18), NIGHTEAGLE 180nm test area, Qty = 5

	F	M	A	M	J	J	A	S	O	N	D	J
Schedule								1	1	1	1	1
Actual								1	1	1	1	1

0.13u PROTOTYPE

- early learning / no spec, Qty = 1, Yorktown VS5

	F	M	A	M	J	J	A	S	O	N	D	J
Schedule												1
Actual												1

Figure 1. MMD Contract Deliverables, 1996

2.0 Validation Study (Task 1)

Task Objective: Develop a pilot line validation study for the production of masks with test and/or circuit patterns that use 0.25μm and 0.18μm design rules.

2.1 Validation Plan Update: CDRL G001

The Validation Plan was updated in February, 1997. Reference CDRL G001, 97-MMD-LFSC-00018

2.2 NIGHTHAWK Manufacturing Measurement Vehicle

2.2.1 NIGHTHAWK/NIGHTEAGLE Writes per Plan

The number of NIGHTHAWK and NIGHTEAGLE writes per plan are shown in Figure 2. The goal for 1996 was to write five line monitors per week with the emphasis on NIGHTEAGLE, the 0.18μm pattern, in the fourth quarter. Generally, until the fourth quarter, line writes were to plan.

A charging problem referenced in 3Q96 on EL-4 P0 was found to exist on the fourth aperture. While this problem was found in July of 1996, it was not resolved until late January, 1997 in order to keep the tool available for refractory development and the shipment of other customer masks that were less affected by the problem. Line monitors written in 1Q96 were, therefore, below plan. Since the aperture was replaced, work is ongoing to return to normal line monitor starts.

2.2.2 NIGHTHAWK/NIGHTEAGLE Yields

NIGHTHAWK and NIGHTEAGLE yields were measured throughout 1996 for overall yield and for the individual yields of image size, image placement and defects. Figure 3 shows all of the yields. The targets for each yield are 80%, 80%, and 25% for image size, image placement and defects, respectively. The overall yield target is 16%.

2.2.3 Image Size

Image size results for 1996 are shown in Figure 4. Image size control improved throughout the year as image size "bow" was reduced by reducing fogging at EL-4 P0, and with the introduction of better quality coatings from the Karl Suss coater. Yield to 20nm 3σ improved from 10% to 50%. NIGHTHAWK masks were fabricated with 13nm 3σ with the normal process, and 11nm 3σ with a conductive topcoat. Similar results were obtained from both e-beam tools.

The charging problems mentioned in section 2.2.1 adversely affected image size performance this quarter, especially for the normal multipass process. Excessive charging causes poor overlay of the respective passes which increases image size variation across the mask. By exposing line monitors with a single pass exposure, charge problems are reduced but image placement performance is sacrificed. Image size 3σ averaged 22nm during 1Q97 with the single pass line monitor.

The emphasis for 1997 is to convert from Au to refractory masks with SNR 200 and UVIII resists. These lower dose resists, along with the resolution of the charging problem at EL-4 P0, should improve yield performance to the target of 80%. Also, polyaniline conductive topcoat will be implemented to improve image size performance.

2.2.4 Image Placement

Image placement performance for 1996 is seen in Figure 5. Due to the charging problems on EL-4 P0 mentioned in section 2.1.1, image placement yield was not as good as seen in the last quarter of 1995. A NIGHTHAWK mask was fabricated with 22nm 3σ image placement, with the charging condition masked with a +22 volt bias placed on the center tube. Because charging conditions change over time, this was only a short-term fix. Also, EL-3 #6 gave excellent results with 80% yield to 60nm and the fabrication of a NIGHTHAWK mask at 40nm.

As mentioned above, image placement performance on the line monitor degraded during 1Q97 due to the return to the single pass exposure. With the replacement of the fourth aperture, image placement improved in January, 1997 and the PSE (Product Specific Emulation) is currently being corrected to improve even further to below 35nm.

The plan to improve yield for image size also applies to image placement. With the EL-4 P0 showing less charging and the use of lower dose resists, the yield to the 36nm specification will improve. Also, with the determination that a polyaniline topcoat improves repeatability, work will continue in 1997 to implement polyaniline into product manufacturing.

2.2.5 Defect Learning

The defect learning is shown in Figure 6. Again, charging at EL-4 P0 resulted in a high number of clear defects. Parts written that did not have the excessive number of clears showed normal defect density numbers, <30 defects/cm^2. Also, gold bubbles were resolved with an adjustment at the resist coat tool and opaque spots were eliminated from the rework process. Defect-free masks shipped to the customer during 1996 included NIGHTHAWK, Plutus and Phoenix. Emphasis on defect density is now shifting from the current gold process to the new refractory process; work in this area is ongoing.

The emphasis in 1997 will be to transfer all refractory processes to the MMD to improve defect performance to the 25% yield. Initial results from Au masks built with SNR 200 show a reduction in expose/process clear defects seen with PMMA in the last half of 1996. Also, new inspection tools will be installed in 1997 to help improve substrate build quality.

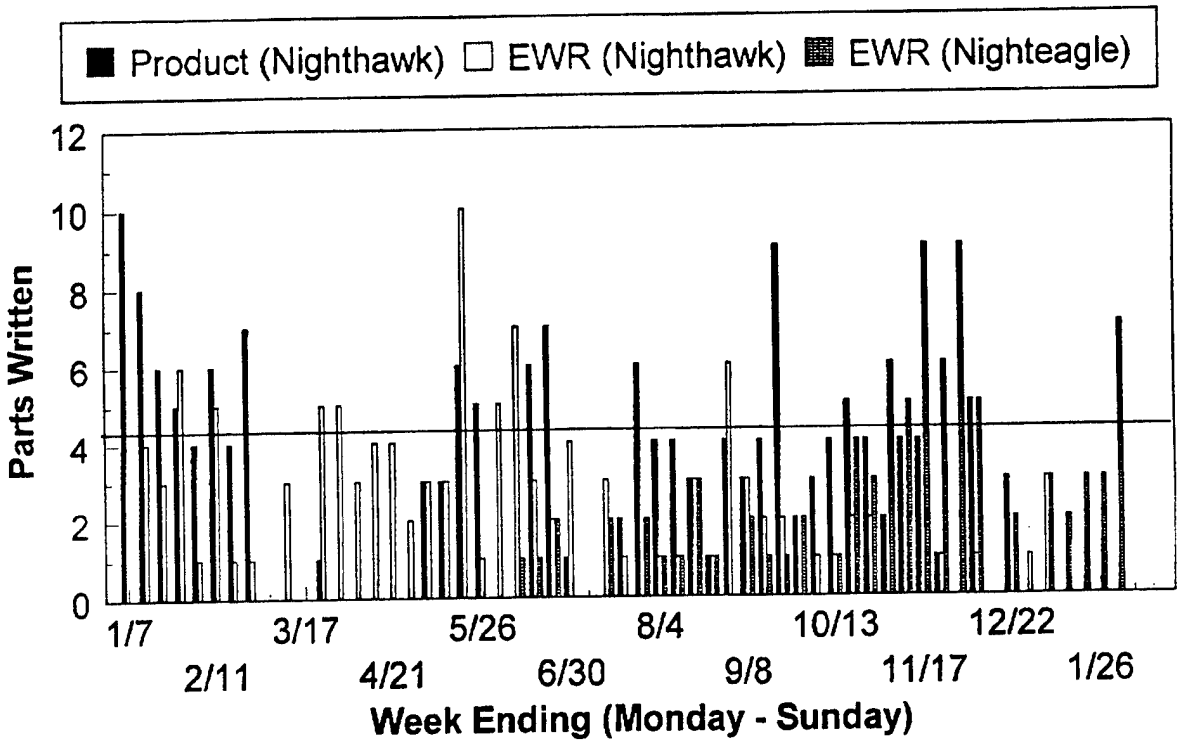


Figure 2. Line Monitor Writes per Week

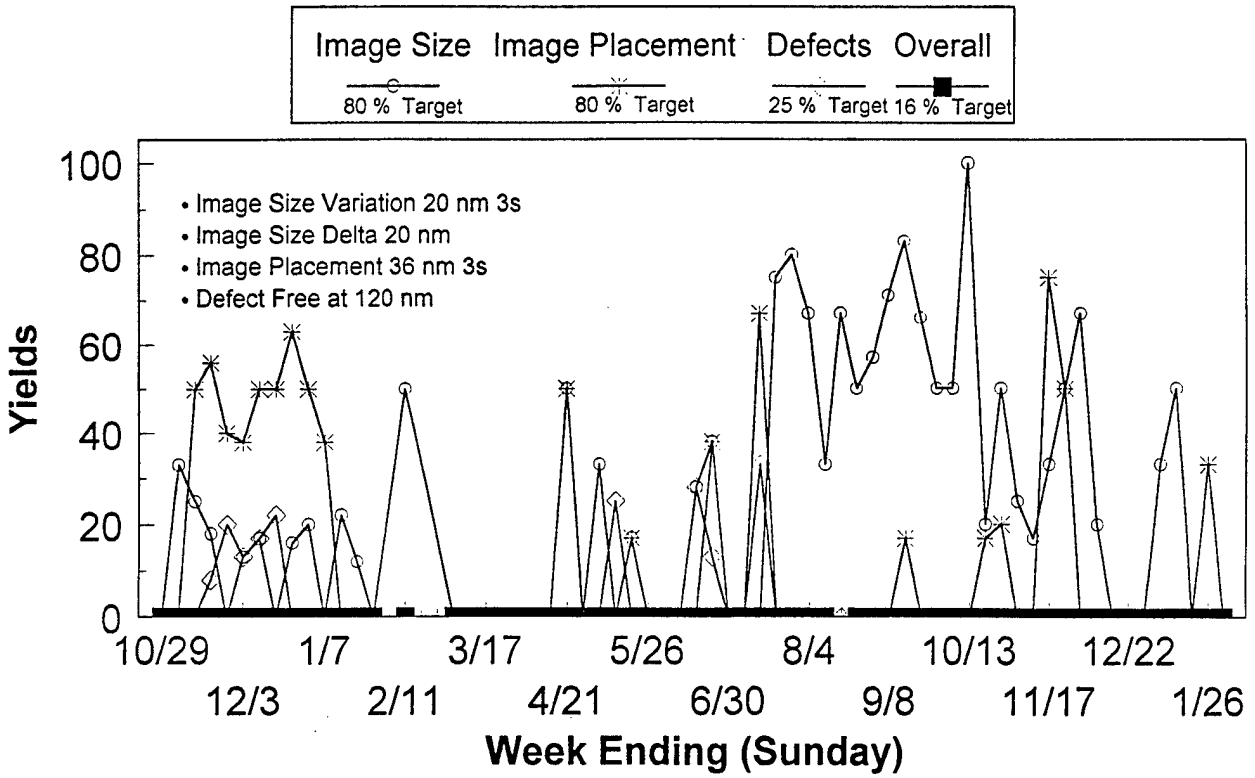


Figure 3. Line Monitor Yield

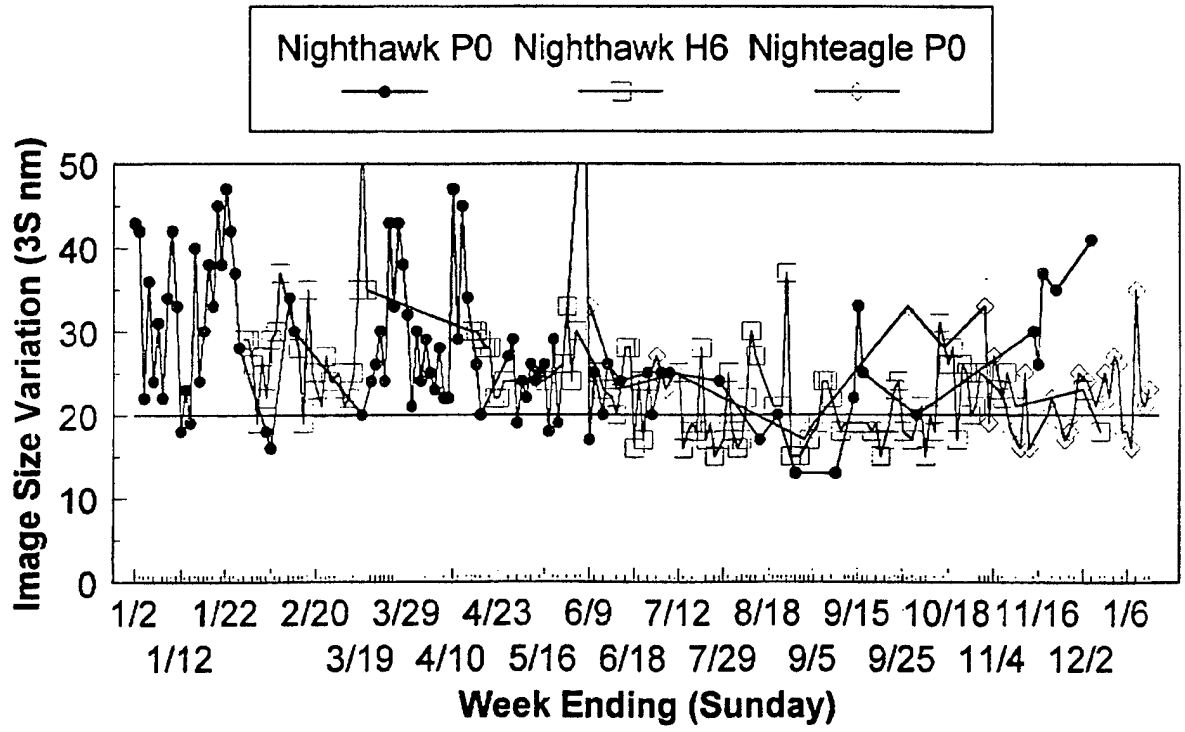


Figure 4. Image Size Variation (Line Monitor)

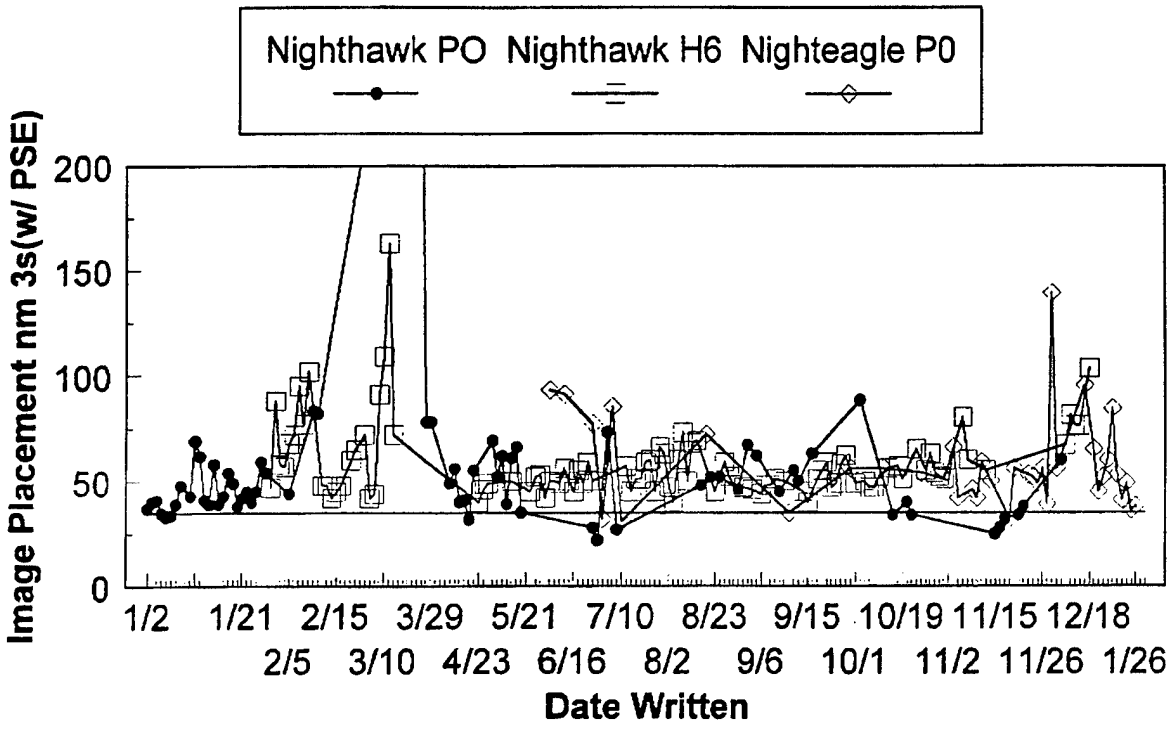


Figure 5. Image Placement (Line Monitor)

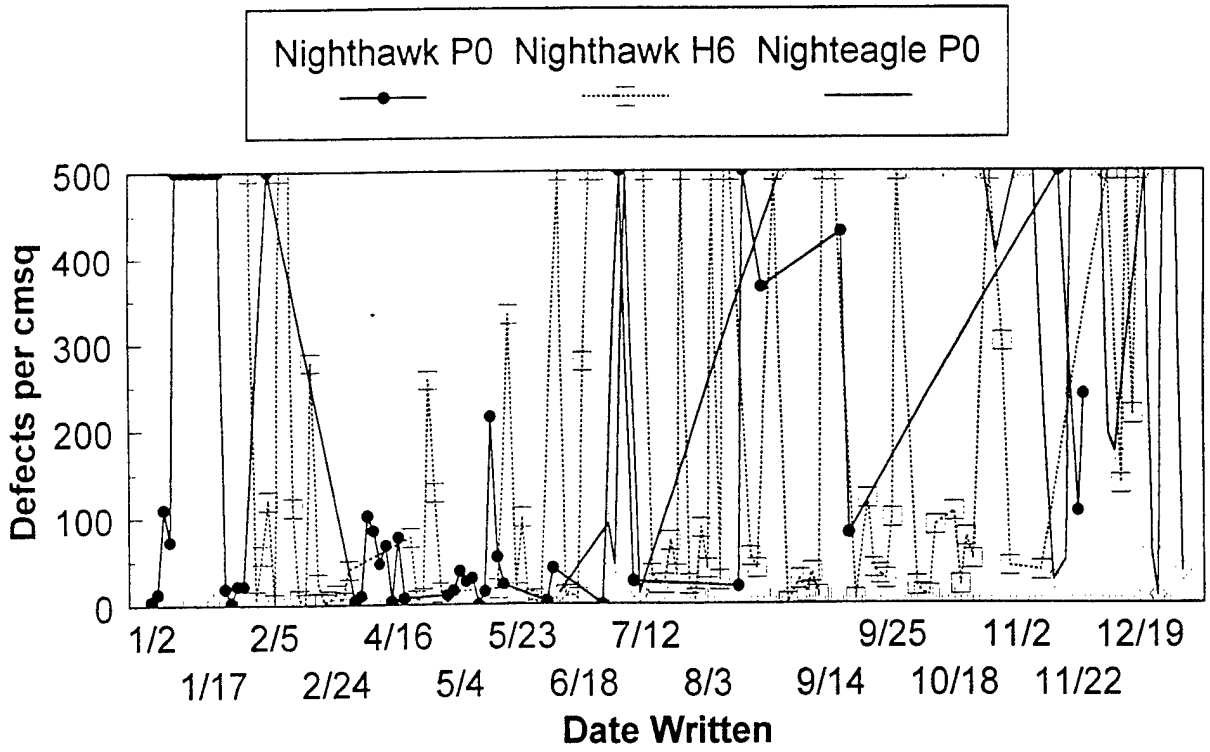


Figure 6. Defect Density (Line Monitor)

3.0 Roadmap Activities (Task 1)

Task Objective: Devise a comprehensive MMD technology roadmap.

3.1 Technology Roadmap

The Technology Roadmap was updated in February, 1997. Reference CDRL G002, 97-MMD-LFSC-00019.

3.2 Metrology and Inspection

3.2.1 Tencor Surface Inspection System

The Tencor surface inspection system project plan is shown in Figure 7. The order for the wafer/wafer-membrane tool has been placed. Acceptance is planned for 20 March 1997.

There is an x-ray mask substrate tool issue with the software mapping the wafer edge and the laser scattering off of the Pyrex ring. The scattered light causes the detector to saturate which causes the system to see false defects. Discussions with the vendor failed to identify a solution to either problem. The mask substrate tool will not be ordered. We are currently looking for a new substrate surface inspection system (see Figure 7).

3.2.2 Leica LMS 2020 Trade-in

The LMS 2020 tool has been moved and reinstalled. There was a delay in starting the qualification due to installation problems with the critical dimension precision. The tool is currently being qualified. (See Figure 8.)

3.2.3 AutoSEM

The Amray AutoSEM software upgrade has been completed. The added function facilitates the creation of job set-ups and automates the system calibration procedure. Future plans include moving the tool to a new location next to the LMS 2020 in March of 1997.

3.2.4 KLA SEMSpec

A study is underway to determine if the refractory stack should include a chrome etch stop. The KLA SEMSpec will be evaluated for its capability to handle a chrome etch stop, which acts as a discharge layer for the e-beam (see section 6.2.).

3.3 Process Equipment

3.3.1 Suss Automated Resist Coating System

The robotics cable, which was replaced for the fourth time in August, has been reliable. The new cable is a more robust, braided type cable more suitable for the range of travel required for the Suss tool.

A replacement robot end-effector has been manufactured by Suss and installation is scheduled for mid-February. (The current end-effector is corroding, possibly due to acid exposure at the Suss factory.)

A proposed agenda for the maintenance training is being reviewed with the internal maintenance group. Training will be scheduled in March.

A sizing to install two additional Millipore pumps on the tool was completed by Karl Suss in February. Installation of the pumps will be scheduled for next quarter. The new pumps will be used for the FEOL resist and EV3 positive resist.

3.3.2 New Develop Tool

An automated bake/develop tool specification was sent to six suppliers for quotations. Only three of the suppliers responded: SSI, Suss and Fairchild. SSI was chosen since they have the best reliability results and superior technical capability on develop equipment. Originally, SSI would not provide SMIF handling due to lack of space in the tool footprint for multi-substrate PODS. They later agreed to provide SMIF handling for single PODS. Suss has no experience with develop equipment and Fairchild's quote failed to address critical x-ray handling issues.

A purchase requisition has been submitted to Purchasing, along with the quotation and cost of ownership form. Purchasing will complete final negotiations with the vendor regarding warranty and price, and the order will be placed. The vendor agreed to shorten the lead time from 10 months to seven months. The new target date for receipt of the tool is September, 1997.

3.3.3 New Hot Plate

The first of two hot plates was received on 16 January 1997. This hot plate has a vacuum hold-down of the membrane pedestal, as opposed to the current screw-on type. New pedestals are being ordered for the new style base hot plate. The tool will be tested, with implementation targeted for May, 1997.

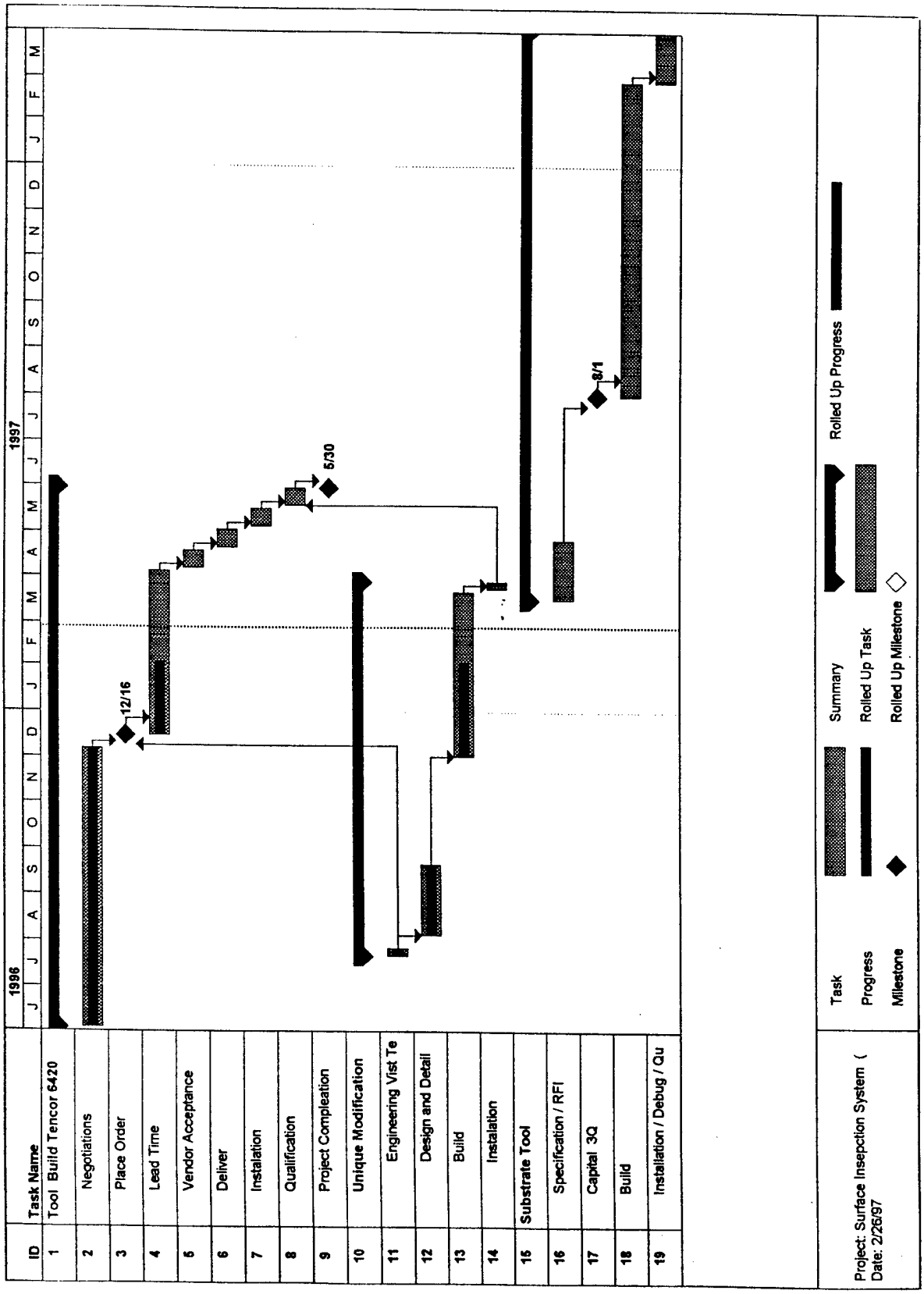


Figure 7. Tencor Surface Inspection System

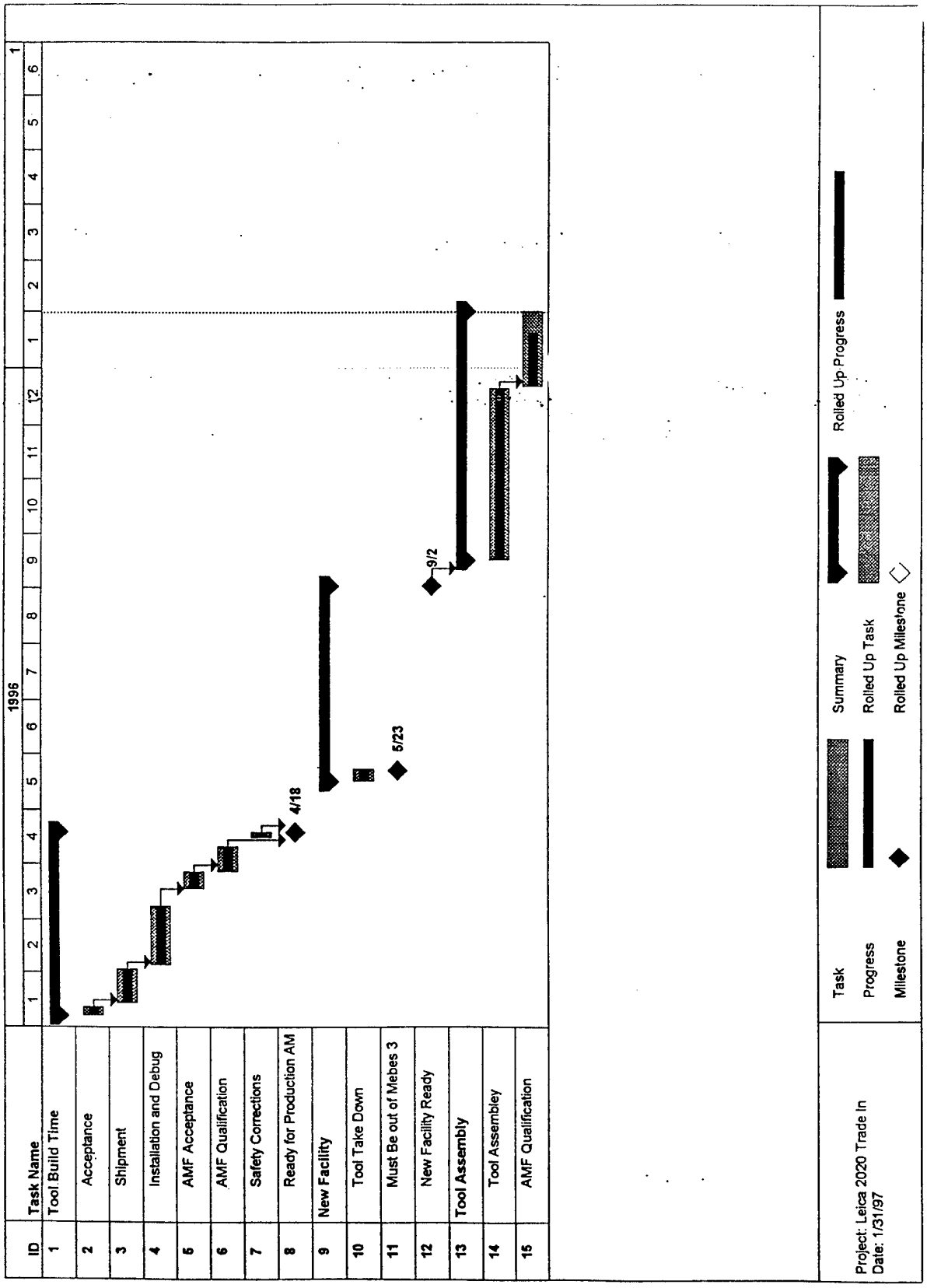


Figure 8. Leica 2020 Trade-In

4.0 Develop 0.25μm Mask Fabrication Capability (Task 3)

4.1 0.25μm Prototype Mask Fabrication (Task 3.1)

Task Objective: Establish and maintain a pilot production facility capable of on-premises x-ray mask production, and demonstrate 0.25μm mask fabrication capability by fabricating prototype masks of increasing complexity.

4.1.1 Line Status

The emphasis for the line in 1996 was the shipment of gold customer masks and shift to inserting the capacity to build refractory masks. Because these goals were sometimes contradictory, decisions had to be made that affected the ability to complete these tasks. While charging at EL-4 P0 restricted the ability to fabricate gold masks to meet contract specifications, it was decided to keep the tool available for refractory exposures for process learning.

MMD was able, however, to ship NIGHTHAWK masks to meet commitments through November. Also, three levels of defect-free Plutus masks and several defect-free Phoenix masks (two that met product specifications) were shipped to IBM customers, while Motorola received the F54P (Motorola 0.25μm SRAM test site), LTM4 and LTM5 levels. The first NIGHTEAGLE masks were also fabricated with both gold and refractory substrates. The current line monitor is the 0.18μm test site, NIGHTEAGLE.

Many new tools were qualified in the MMD in 1996. The Karl Suss resist coater was both process- and product-qualified. A significant improvement was seen in both uniformity and defect levels. This was a contributor to an image size variation reduction seen in 1996. Factory acceptance was completed on the Leica 2020 and the tool is currently undergoing product qualification in Burlington. This image placement measurement tool will give better repeatability, drift performance and improved scan linearity. Also, a new tantalum RIE etch tool arrived and is currently being qualified for the Motorola process. Other new tools expected in 1997 include two Tencor Surfscan particle detection tools and a new resist develop tool.

EL-4 P0 experienced charging problems from July, 1996 and received several upgrades. A hole was drilled through the ferrite table to reduce fogging on the backside of the membrane. This allowed electrons that travel through the membrane a path away from the substrate, contributing to improved image size control in 1996. Also, to reduce contamination on the third aperture, an electrically heated (250°C) third aperture assembly was designed, tested and installed. This has resulted in longer aperture life and is currently in test for the fourth aperture. Also tested in 1996 was a RISC 6000 P5 parallel processing system that will allow local post-processing of tool data. This cost-saving processor will be implemented in the first quarter of 1997. EI-3+ #6 was a backup tool for EL-4 throughout 1996 and several shipments were exposed on this tool.

In the area of defect control, several final mask cleaning strategies were evaluated during 1996. An FSI Aries ICE mask cleaning system was chosen over a Radiance laser system. The FSI Aries provides better cleaning efficiency, and implementation will proceed in 1997. (See CDRL G004, 97-MMD-LFSC-00011.) A final mask wet cleaning station has been tested and was very effective on organic foreign material (FM). Analysis and use of this system will continue in 1997.

The collaboration with the University of Wisconsin to study the benefits of modeling techniques continued in 1996. It was shown that the model use effectively matched the results of membrane movement during the exposure with the technique currently used. However, results from the alternative writing techniques that the model suggested would minimize this movement, a spiral pattern, and did not match the model. It is believed that the model underestimated some factor, such as resist heating or resist charging, that would need adjustment. Further work in this area will concentrate on BEOL movement for refractory stacks.

Two problems were reported in 3Q96 as affecting line performance. The charging at EL-4 persisted through most of the quarter while rough gold was not seen during the quarter. Emphasis during this period was on integrating the refractory process to replace gold (see Section 6.2) and on shipping select gold customer masks.

A perfect Plutus M1 mask was shipped in 1Q97, along with several engineering quality Phoenix DT masks with good image size results, and with defect issues that are presently being handled. Excessive FM and sand-dollar defects have been found on finished parts. Initially, the BEOL process steps were investigated. A gold flaking problem at plating was identified and resolved by refinishing the cathode surface. FM counts at the remaining BEOL stations were within specification. Next, the FEOL was investigated and high, bright light counts were seen after CVC sputter. Further analysis indicated that the primary FM causes are sand-dollars (diffusion) and bond marks at the edges of the bulk silicon. Substrates are being inspected and sorted for diffusion defects and inspected after every FEOL process step. The cleanest substrates were selected for the Phoenix DT product mask. The target date for completion of this order was mid-February, 1997, and three product masks were shipped on 7 February.

4.1.2 Equipment Engineering Changes and Facilities Activities

Suss Resist Coat Tools

A NOWPAK resist dispense system was installed for the conductive polyaniline qualification on the small Suss coater. The polyaniline can now also be filtered.

A digital scale was installed for the resist bottle to indicate proper replacement cycles. This eliminates air bubbles in the line caused by an under-filled NOWPAK. This modification has resolved the gold bubble problem.

Plasmatherm Tools

New bearings, turbopump and o-rings were installed on the Plasmatherm AM36 tool. Fiber-optics were installed for a new end-point detect. The Ardel cover was modified for the new oxynitride etch process.

Microwave power levels and sensors were calibrated for the new refractory etch tool.

AMRAY Auto-SEM

Antistatic mats were installed to eliminate operator static affecting the tool's electronics. The reliability of tool is now improved.

Hot Plate Tools

A custom hot plate was designed and built for 100mm wafers.

A new style temperature controller was installed for the mask hot plate tool. The temperature is now very stable ($\pm$0.1°C) which improves the tool's process performance and reliability.

Thermtec Diffusion Furnace

A new heating jacket, cable and thermocouple were installed to improve tool performance.

Nomenclature Tool

A 100mm fixture for this tool was designed for experimental use. This will photo-expose alphanumeric characters onto wafers, improving defect control.

SMIF Pod Cleaner Tool

Design work has begun on this tool for modifications to clean the new single SMIF Pod format. The design will be universal so that all SMIF pod sizes will be accommodated.

APT Develop Tool

A custom chemical dispense system was installed to eliminate air infiltration into chemicals. This will improve chemical life and operator ergonomics.

Resistivity Monitor

A resistivity monitor was designed and built to spot-check DI water baths on the MMD line. This monitor will confirm proper operation of the station's built-in sensors.

Tropel Flatmaster Tool

The chuck was modified to hold new 2.1mm thick wafers. A Teflon seal was added to ensure proper vacuum.

Etch System Tools

Improvements to the reaction vessel system included temperature control, heat transfer media, condenser, and Teflon PFA rinse tank.

KOH system improvements included Teflon fixturing for wafer-compact design, process and rinse tank upgrades, and a vent system for compacts. A tool was designed and built to remove the compact etch fixture from the KOH.

MMD Microscopes

A microscope chuck was designed and built to hold an x-ray mask in the inverse position for backside membrane FM inspection. The chuck assembly includes 3-point leveling control, notch location, and bottom illumination port.

4.1.3 Miscellaneous Image Placement Experiments

4.1.3.1 University of Wisconsin Modeling Verification

Coordinated projects are currently being defined based on student goals and industry requirements. One project which will be included is a continuation of the process-induced distortion modeling with an extension to look at more localized distortions. In addition, they will be switching models over to the refractory stack (most were completed with the gold process). Additional modeling of the resist bake chuck currently in use in the MMD will also be completed.

4.1.3.2 Small Subfield Evaluation on EL-3+ #6

EL-3+ #6 was down for a majority of 1Q97 due to a clamping problem (see Section 4.2.5) that hampered progress on this project. Before the tool went down, exposures made with reduced bias, small subfields, and normal field sizes produced very promising results. Image size was in specification and clear defects, a signal of resolution limitations, were minimal. When the tool becomes available, work will continue on the optimization of small subfields with a negative resist for the refractory process.

4.1.4 Substrate Fabrication (FEOL)

During 1Q97, 52 substrates were manufactured. As seen in Figure 9, 52 category A, 0 category B and 0 category C substrates were built during the quarter:

- December: 12 category A, 0 category B and 0 category C.
- January: 34 category A, 0 category B and 0 category C.
- February: 6 category A, 0 category B and 0 category C.

No polyimide substrates were in the MMD during 1Q97 (polyimide substrates are no longer built in the MMD). The reworked substrates can be seen in Figure 10. For December, there were 13 category A, 1 category B and 0 category C. The rework process was halted because only virgin substrates were used to analyze a defect problem.

4.1.5 FEOL Foreign Material Reduction

4.1.5.1 Tencor Calibration

The Tencor 4500 defect measurement system was recalibrated using standards comprised of known diameter latex spheres on bare silicon wafers. The tool was optimized for a size distribution around 1.0μm, but acceptable results were obtained for the 0.3μm size distribution as well.

4.1.6 Membrane Haze (Surface Roughness)

The diffusion furnace studies reported in 3Q96 were continued with the goal of improving diffusion disk life and reducing membrane haze. An engineering tube was established for these studies and evaluation runs were made by varying oxygen and argon gas flow and wafer position in the tube. Results of experiments using center-of-tube position with three liters argon and one percent oxygen produced no haze, and lifetime was extended on disks previously considered spent (5-6 runs). This tube is now being qualified for product with new diffusion disks to confirm haze elimination and determine maximum run life.

4.1.7 BEOL Defect Reduction/Inspection

The overall defect reduction project schedule is shown in Figure 11.

4.1.7.1 Defect Reduction

A benchmark of the defect level for the refractory mask (TaSiNx) process is currently being run. A lot consisting of 24 refractory masks is currently being produced using the current process-of-record. These masks will be characterized for defect levels by mid-March, 1997. At this time, key defect reduction projects will be developed.

4.1.7.2 AutoSEM

The SMIF loader/unloader for the AutoSEM was installed in January, 1997.

4.1.7.3 New Mask Boats

The new NIST-compatible x-ray mask boat mold is being designed and built by Fluoroware. Completion is scheduled for the end of March, 1997.

4.1.7.4 Sacrificial Layer Study

During the current boron-doped silicon membrane process, the parts have a sacrificial layer to protect the front surface of the mask from damage during the back surface lithography (defines the membrane size and shape). For the refractory program, the addition of a sacrificial layer would add two process steps (a chrome top layer and a nitride layer). To keep the process as simple as possible, we are investigating the need for the sacrificial layer. Twenty-four refractory masks are currently being run through the process without a sacrificial layer. The masks will then be evaluated for defect levels.

4.1.8 Final Mask Clean

Evaluations of the FSI Aries (ICE) system and the Radiance Laser clean system have been completed. The FSI Aries system, overall, demonstrated better cleaning efficiencies (80% vs 43%) over the Radiance system. The MMD has decided to pursue funding to support the purchase and installation of an FSI Aries system. The overall Final Mask Clean project schedule is shown in Figure 12.

4.1.8.1 FSI Aries Final Mask Clean Evaluation

The system design concept and costing of the FSI Aries system have been completed. The total cost of the system will be approximately $2.3M for a fully automated (SMIF-to-SMIF) system.

4.1.8.2 Laser Clean

A second evaluation of the Radiance clean system was completed. Four masks containing a number of non-repairable foreign material were cleaned. An overall cleaning efficiency of 43% was demonstrated (Figure 13). The study also looked at whether the system would damage refractory masks. One refractory mask was cleaned and re-inspected and no damage to the mask was seen. This project will be closed out since the decision has been made to pursue the FSI Aries system; the laser cleaning activity has been transferred to ALF.

4.1.9 Substrate Flatness/SiC 2.1mm Wafers

4.1.9.1 2.1mm Thick Wafers/5μm Flat Substrates

The delivery of two hundred, 2.1mm wafers has been completed. These wafers will be used to start the evaluation of 2.1mm conversion (see Figure 14). The MMD has not yet received the 2.1mm pre-mesa wafer.

4.1.9.2 Tooling Upgrade to Support 2.1mm Thick Wafer Conversion

- Plasmatherm Hardmask and Protective Overcoat PECVD Nitride tool: Tool is on order.
- Upgrade to the Perkin Elmer 500 for the back side lithography: The vendor was on-site in early February to size up the conversion task.
- P0 e-beam system wafer chuck: No new status.
- Plasmatherm Refractory etch tool upgrade: No new status.
- Thick wafer boats: The mold has been completed.

4.1.9.3 Etch Chemistry

The final key decision to be made was that of which etch hardware to use with the KOH. Evaluations of the compact system and the fountain etch system have been completed. The compact system will be used in the interim, however, for the manufacturing solution the purchase of a fountain etch system is being pursued. See Figure 13 for the etch station plans. A statement-of-work is being prepared and IBM funding is being pursued.

4.2 Develop 0.25μm Validation Mask Fabrication Capability (Task 3.2)

Task Objective: Establish and maintain a pilot production facility capable of on-premises x-ray mask production, and demonstrate 0.25μm mask fabrication capability by fabricating validation masks.

4.2.1 PMMA Resist Status for EL4 P0

The intermittent rough gold problem observed on PMMA product in 3Q96 has not recurred.

The gold bubble problem resurfaced. Initially, the results correlated with the bottom of the NOWPAK, yet for the first time bubbles were still seen with a full resist NOWPAK. The resist filter was replaced in mid-December and the KLA defect reports for several NIGHTHAWK line monitors indicate that the problem has been corrected. The Millipore (pump/filter) field service representatives recommended a filter change every six months. This has been included in the new Suss procedure.

4.2.2 SNR 200 Resist Status

Resist scumming has been observed on several refractory-metal masks with the SiON hardmask. An oxygen descum before resist application appears to reduce the tendency for scumming. Five of seven reworked parts descummed prior to coating did NOT have scumming. (This is part of Motorola's rework process and was also discussed in an SPIE '96 paper [1] to avoid acid contamination of SiN substrates when using chemically-amplified resists

All of the DOE and experiments for SNR were completed on Cr substrates; therefore, some additional testing on SiON substrates is warranted. An experiment has been designed to verify the effectiveness of the descum on both SiC and Boron-doped silicon. In addition to the change from Cr hardmask to SiON hardmask, a difference in the bake was noticed between the boron-doped silicon and the SiC membranes. The boron-doped silicon membranes "bow" during the first 15 to 20 seconds of the bake cycle, then relax to a flat position. The stiffer silicon carbide remains flat for the entire bake cycle. This experiment will clarify the bake and substrate surface contributions to the residue problem.

Resist lot aging was ruled out as a cause of the scumming by three separate tests completed to compare the old lot with the new resist lot: chemical analysis did not indicate any changes in resist chemistry, bare Si wafers had the same image size and image quality results for both resist lots, and refractory substrates exposed with the LTM5 (Motorola mask pattern) had the same amount of scumming and similar image size results for both lots. Meanwhile, we used up the remainder of the old lot and changed the resist filter and installed the new lot.

4.2.3 UV III Resist Status

UV III is a positive chemically amplified resist which is currently being evaluated as a positive resist complement to the SNR 200 negative resist. A positive resist will be required for contact levels on refractory absorber masks.

A Design of Experiments (DOE) matrix has been designed to optimize the post-apply bake (PAB) and post-expose bake (PEB) for UV3 on refractory membranes. The design was based on pipecleaner wafers completed in 3Q96. Bake temperatures of 135 to 145°C will be evaluated for resolution, exposure latitude, and sensitivity. A dose range of 8 to 44μC/cm^2 at 75keV will be completed on EL-4. The benchmark test pattern which includes nested and isolated arrays of varying linewidths has been post-processed at the required doses using the proximity parameters which were optimized for SNR on Ta absorber. SiC substrates with the Ta absorber are presently being prepared for this DOE.

[1] S. Mori, T. Watanabe, K. Adachi, T. Fukushima, K. Uda, Y. Sato, "Investigation of substrate-effect in chemically amplified resists," Proc. SPIE 2724, pp. 131-138.

4.2.4 Status of EL-4 P0

Emphasis at EL-4 P0 has shifted to support of the refractory effort and to the manufacture of PHOENIX masks. Downtime in the fourth quarter was contained to 15% (168 hours/week). Several system problems have been addressed in the past few months. A new electron gun assembly was installed at the end of November. This was in response to unstable beam current and vacuum bursts. There has been a persistent image placement problem in the Phoenix masks. The within-field measurement in the *X* axis (measuring a vertical line) has been roughly twice the error of the *Y* axis. This was due to a shifting of the spot placement during the exposure of the line. The same phenomena was noticed in an electrostatic position test pattern. This was traced back to a settling issue that resulted in the first spot of each subfield being shifted about 30nm in the *X* axis. After several weeks of testing, the *X* axis electrostatic position dither circuitry was repaired and analysis of this problem continues. Due to the poor image quality of the second aperture and charging at the fourth aperture, all apertures in the system were replaced in January. This was the first test of the new electrically heated third aperture. Previous aperture life was six to eight weeks. This new style heated aperture was installed in August. Inspection of the aperture showed little signs of contamination that limited its lifetime previously. This was deemed a successful test of the third aperture heater design, and a duplicate replacement was installed.

Software enhancement at EL-4 P0 is continuing, with more automation of the daily data collection being implemented. Work is continuing on the P5 post-processor system. The software was fully tested on a RISC system and has been successfully migrated to the permanent SP machine. Currently work is proceeding on schedule, with full implementation of the P5 parallel post-processor planned for the end of March, 1997.

Plans are also being made to schedule time on EL-4 P0 for the Naval Research Labs during first quarter of 1997. This will be a second series of the "through the membrane" beam registration technique.

4.2.5 Status of EL-3+ #6

EL-3+ #6 clamping performance degraded during December, and the tool was taken down to repair this problem. It was decided that during this maintenance, the stage would be re-calibrated to attempt to improve image placement performance. Initial exposures were made in mid-February.

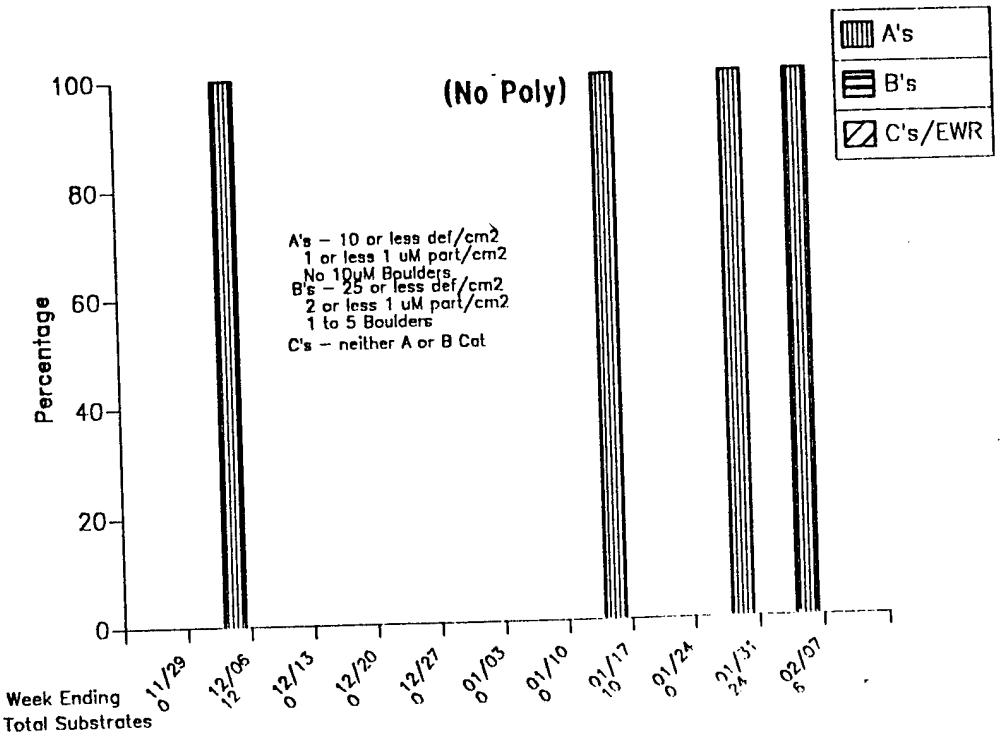


Figure 9. FEOL Substrate Category Yield

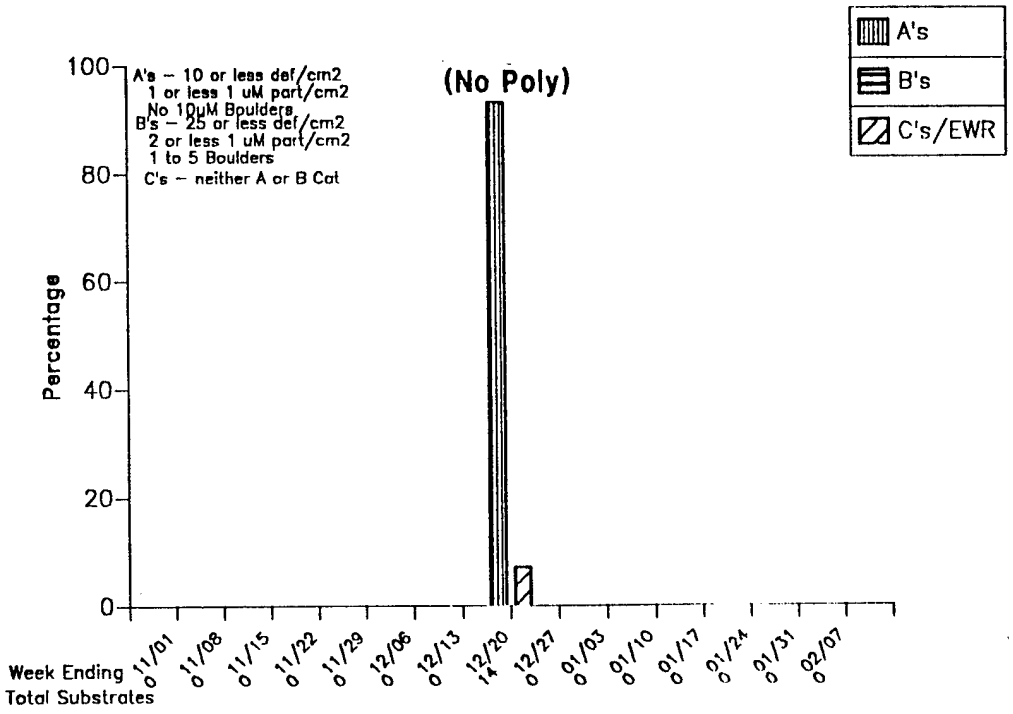


Figure 10. FEOL Reworked Substrate Category Yield

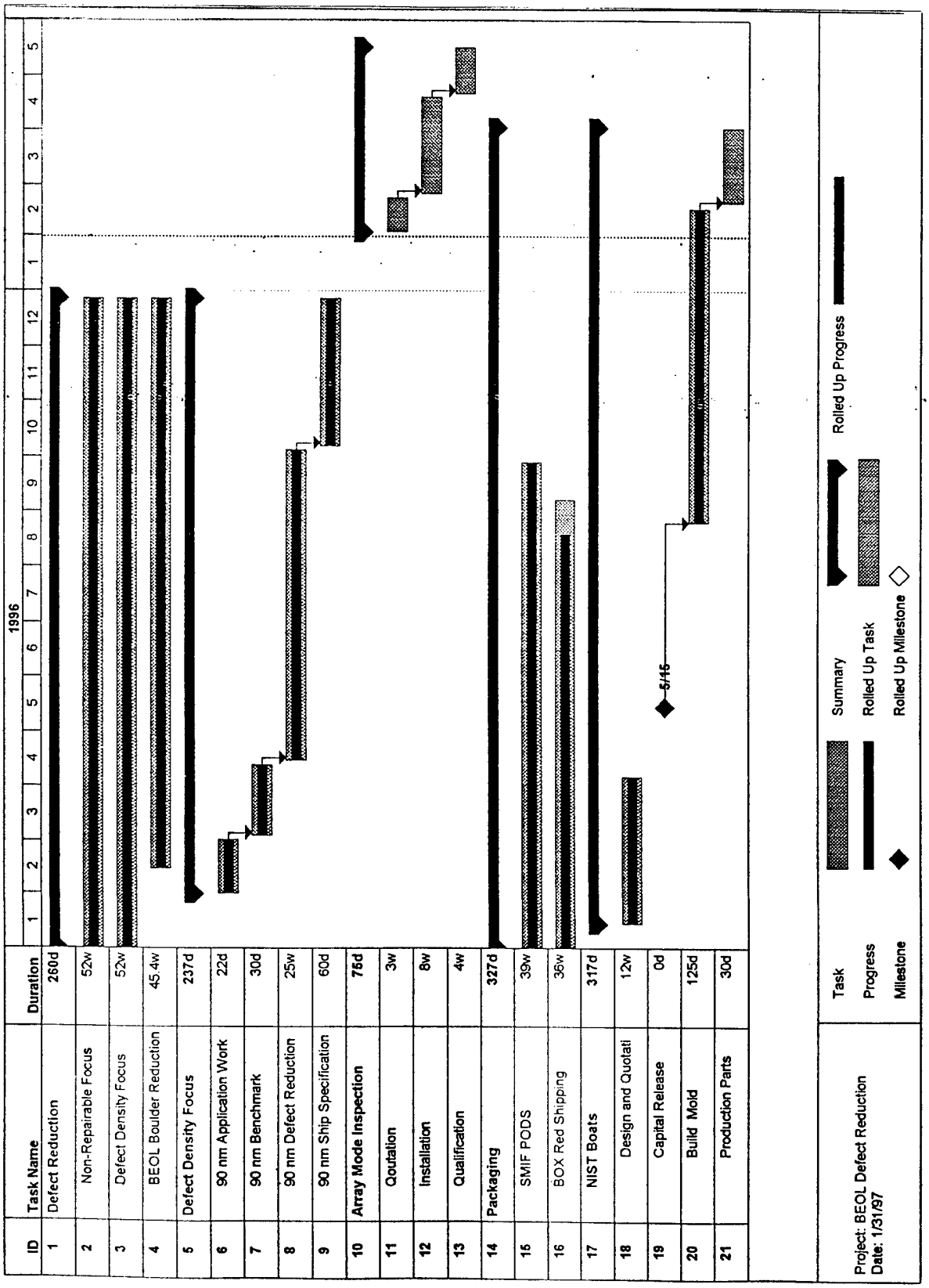


Figure 11 (Part 1 of 2). BEOL Defect Reduction Schedule

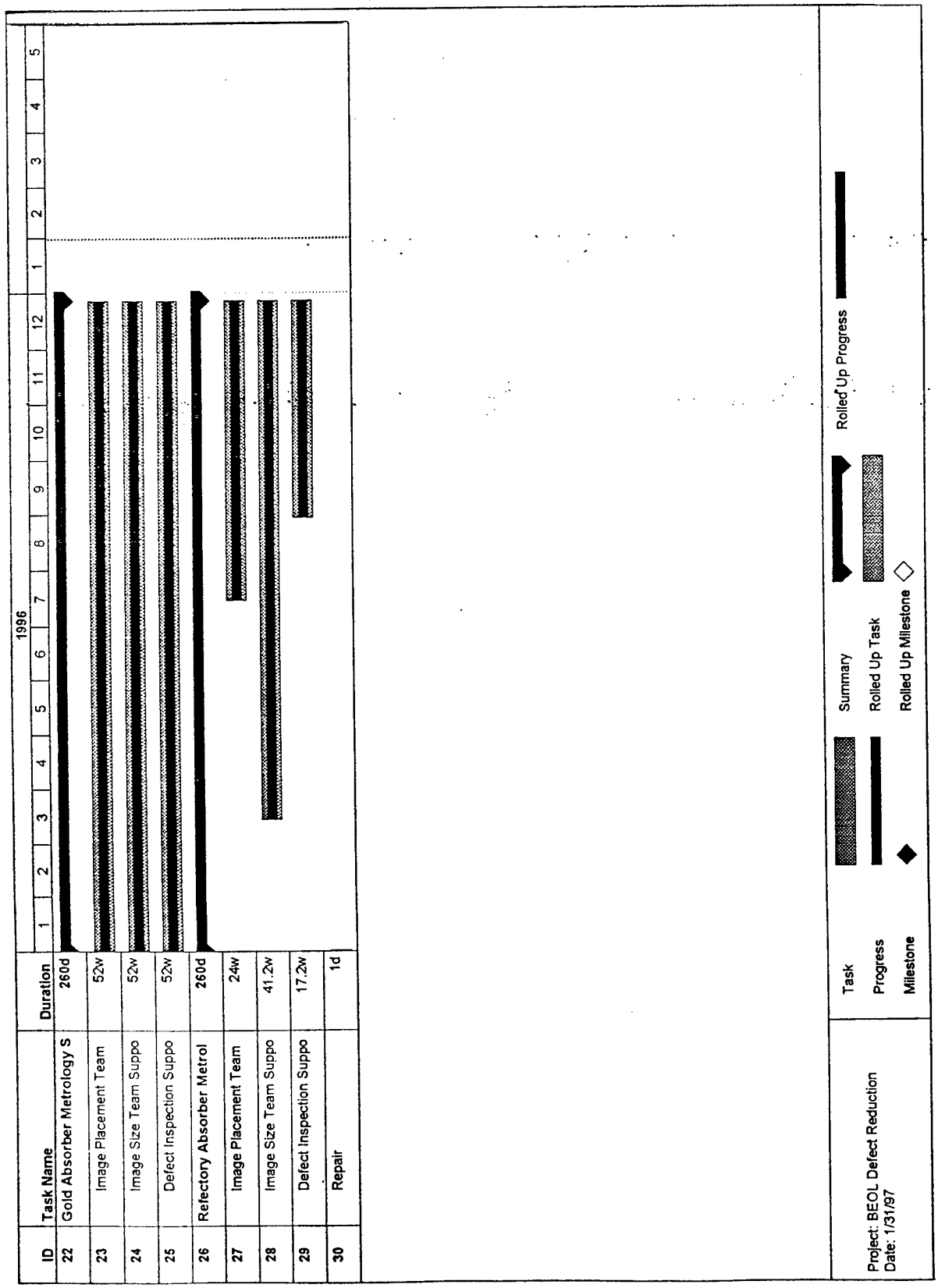


Figure 11 (Part 2 of 2). BEOL Defect Reduction Schedule

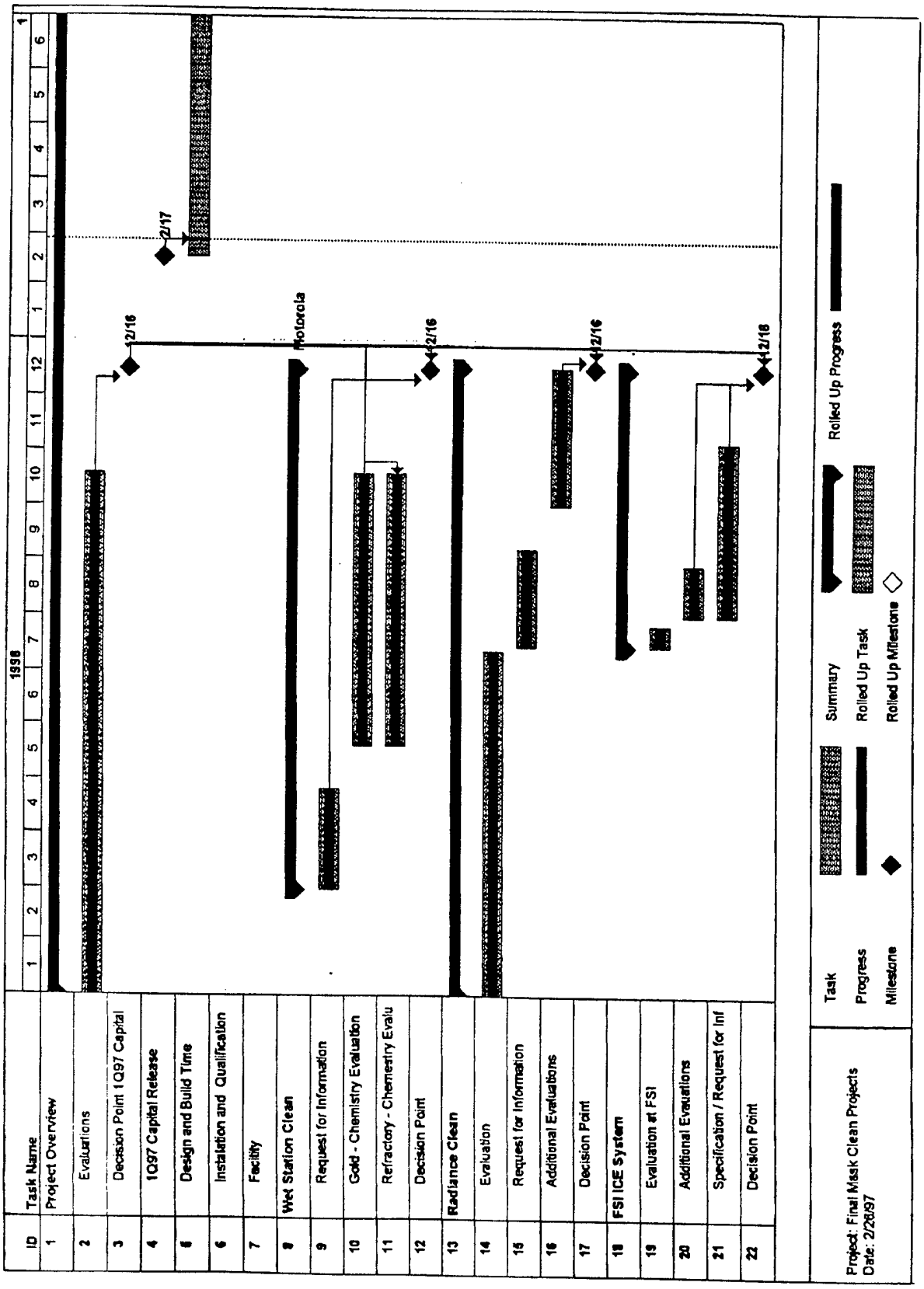


Figure 12 (Part 1 of 2). Final Mask Clean Projects

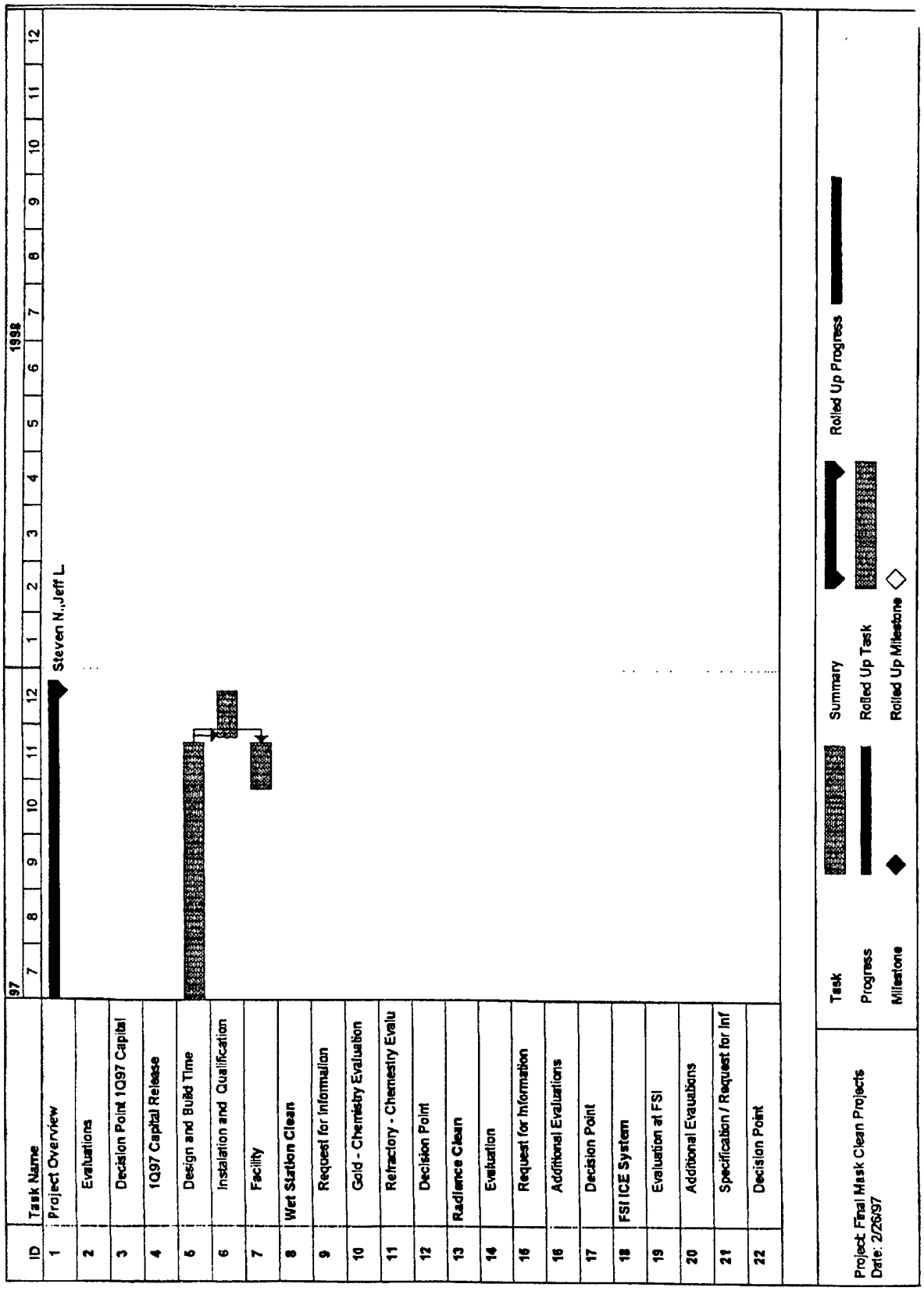


Figure 12 (Part 2 of 2). Final Mask Clean Projects

	0803B	0925B	1001H	0922A	Overall
Pre Cleaning	1	4	3	4	12
Removed	1	0	2	2	5
Repairable	0	0	0	0	0
Remaining	0	4	1	2	7
Efficiency (%)	100	0	66	50	43%

KLA SEMSpec Inspection System

- **Saw no Damage on the Refractory Mask**

Figure 13. Radiance Laser Clean System. Non-repairable foreign material cleaning efficiencies

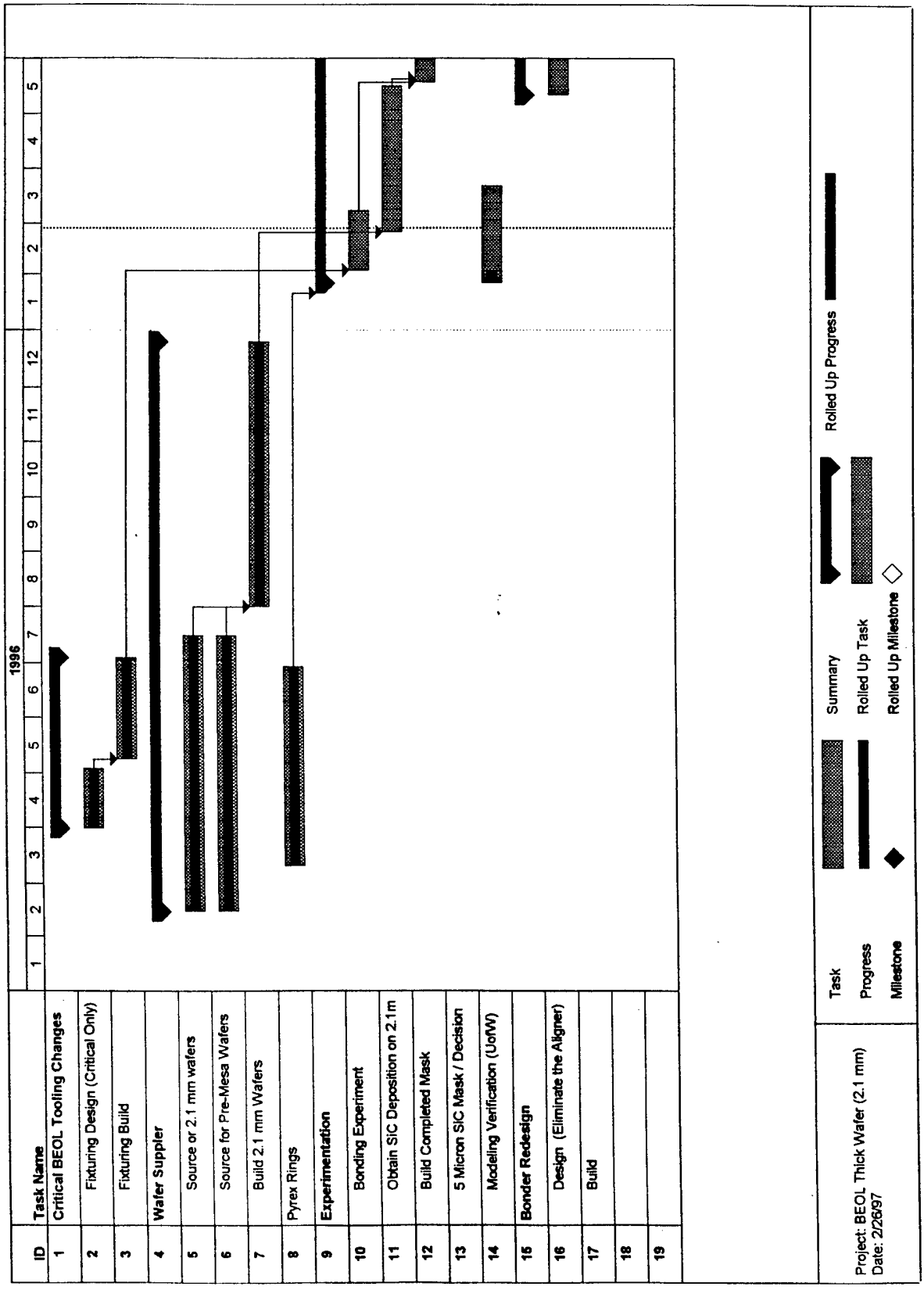


Figure 14 (Part 1 of 5). BEOL Thick Wafer (2.1mm)

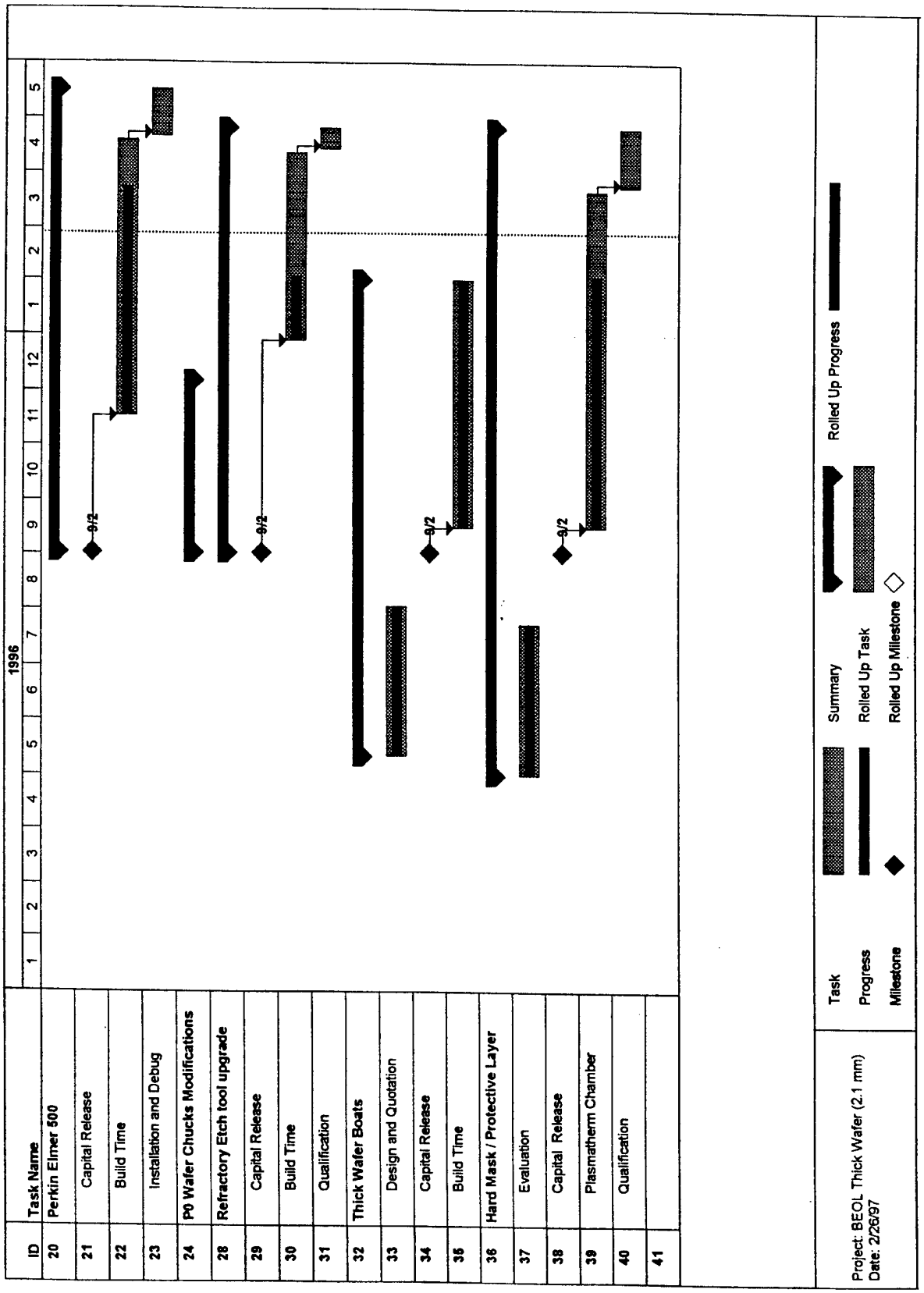


Figure 14 (Part 2 of 5). BEOL Thick Wafer (2.1mm)

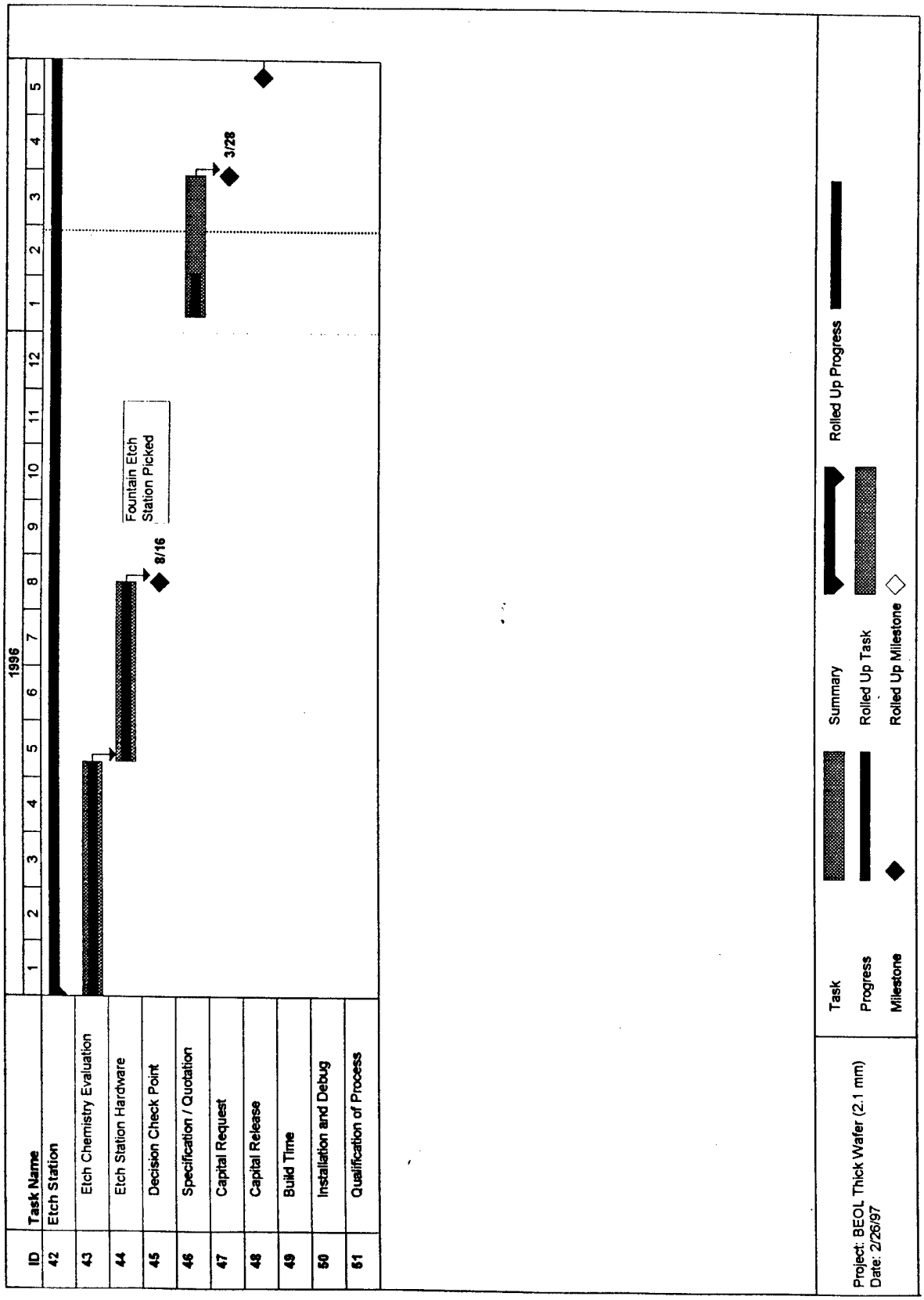


Figure 14 (Part 3 of 5). BEOL Thick Wafer (2.1mm)

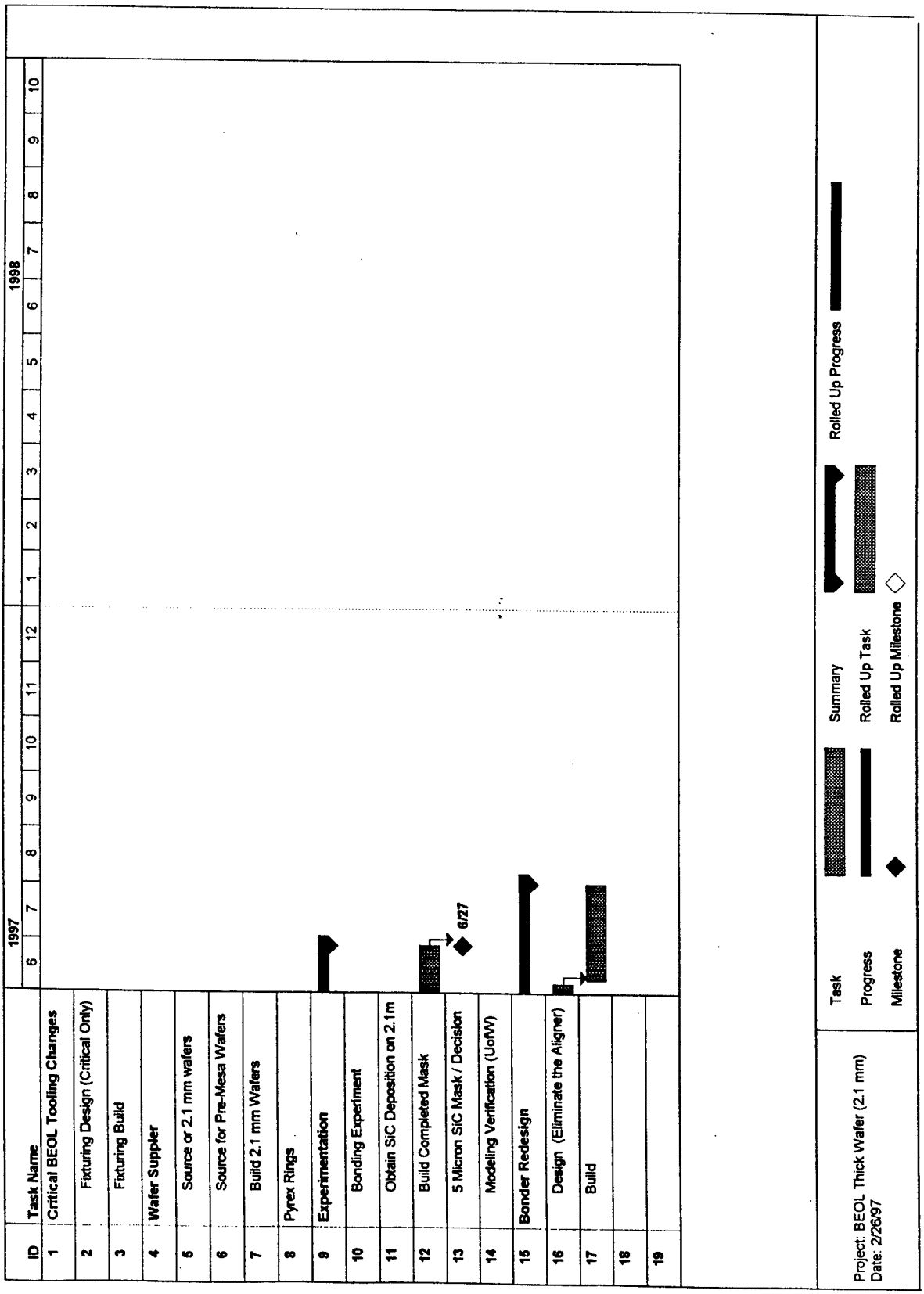


Figure 14 (Part 4 of 5). BEOL Thick Wafer (2.1mm)

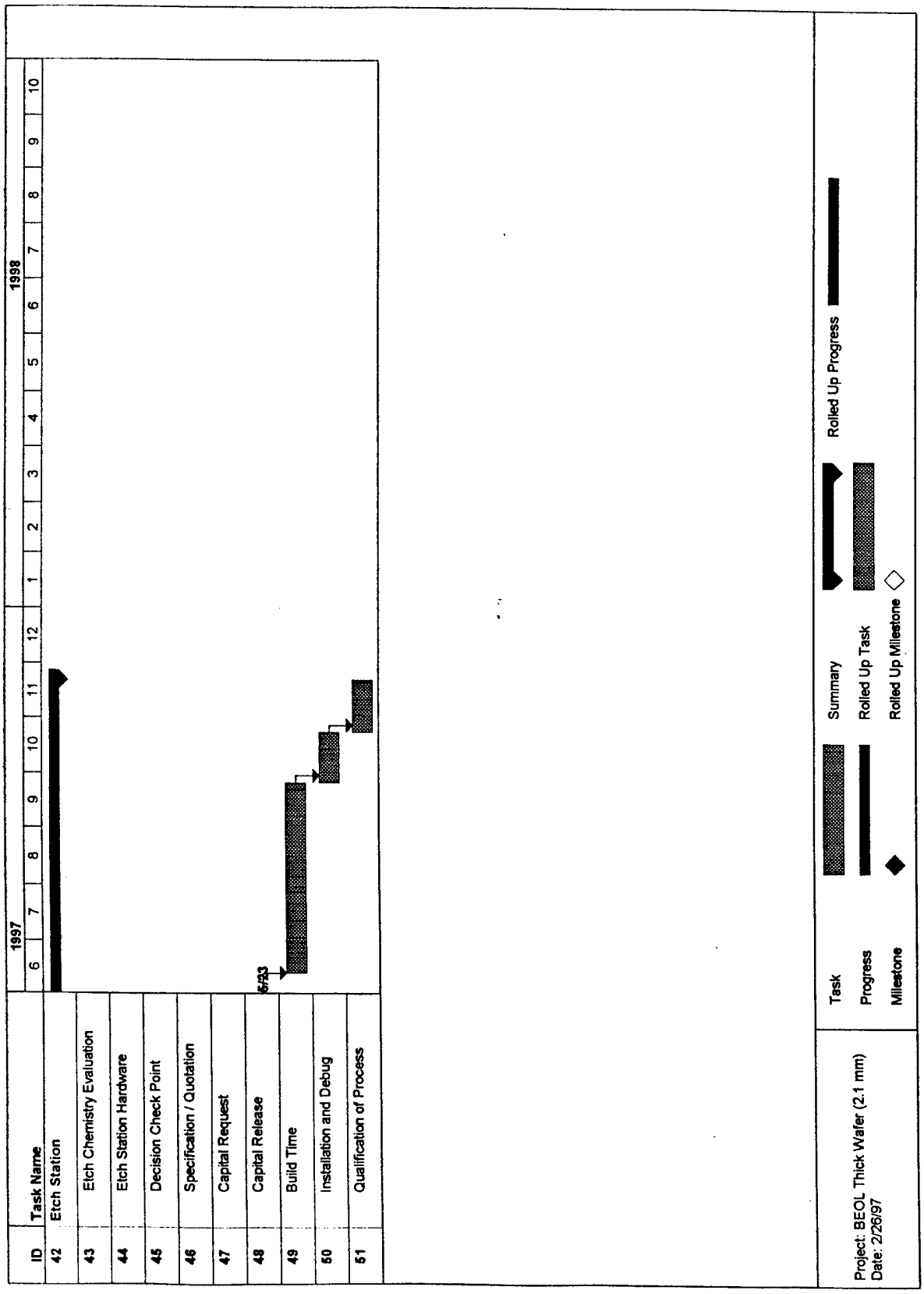


Figure 14 (Part 5 of 5). BEOL Thick Wafer (2.1mm)

5.0 Advanced Lithography Defect Verification

Several major changes were made in ALF during 1996. The x-ray source was shut-down for an extended period for repair and upgrade and came back on-line at about 2× the average beam current prior to the shutdown. The SVGL stepper passed BETA test and has been put into application use on a regular basis. The last planned 5-inch wafer lots were processed and ALF is being reconfigured for 8-inch wafer operations only. The operating schedules have been modified to permit more days per month for source studies to further capitalize on the storage ring upgrade.

5.1 Tooling

5.1.1 Suss Stepper

With the new SVGL DALP aligner becoming available for application use part time during this period, the usage of the two Suss steppers dropped significantly. Consequently, Suss 1 was retired from service and removed from the cleanroom. Its class 1 chamber has been converted to a clean wafer processing center. With the usage of Suss 2 also decreasing, the service plan was converted to a lower cost version. Suss 2 has been exposing mainly 5-inch wafers, but with our last 5-inch customer now converting to 8-inch, it will serve as an 8-inch backup.

5.1.2 Overlay/Metrology Tools

The Conquest overlay measurement tool was replaced with a prototype Biorad Q2 tool. This prototype tool proved too unreliable for routine use and was also removed. The KLA 5015 is now used as the primary ALF overlay measurement tool. It is not located in the cleanroom at this time, but plans are in place to move it to the cleanroom or to equip it with a clean mini-environment in the next reporting period. This tool has also been upgraded for more automatic cassette-to-cassette operation. The SEM room was modified and an Opal automated cassette/cassette critical dimension (CD) SEM was installed and accepted. It is now being used regularly to support several programs including XRL CD measurements.

5.1.3 ALF 3 Beamline and Mirror

The original scanning mirror in the ALF 3 beamline on which the SVGL DALP aligner is installed was found to have very poor performance due to a large amount of scattered light. This scatter also had an adverse effect on the printing of horizontal features due to the apparent divergence of the beam. These effects made it difficult, if not impossible, to perform good print verifications on the SVGL aligner. For these reasons a new scanning mirror was purchased and installed. The original mirror was a single piece of aluminum. The new mirror is made of four planar glass segments. These segments need to be aligned to better than 2% non-uniformity at the segment joints. Characterization of the mirror indicated that the desired result was only

obtained at the center joint. The other two joints have a measured non-uniformity of about 8%. The flux at the joints is also quite low. Otherwise the new mirror meets its design goals. The delivered flux increased by a factor of about three compared to the original mirror. In addition the spectrum of the reflected light appears to be softer giving a resist sensitivity improvement of about 30%. Wafer thruput increased by a factor of about three. In addition, the lack of scattering gives excellent printing results. With the new mirror, the process latitude for horizontal and vertical features is the same (Figure 15). Over several months of operation, the flux from the new mirror decreased by about 15%. This was attributed to a build-up of carbonaceous matter on the flat new mirror in areas struck by the x-ray beam. It is felt that the source of the contamination was a leaky bellows because the decrease in flux seems to have remained constant since the bellows was replaced. Additional vacuum pumping will be installed at the mirror chamber and an off-line mirror cleaning apparatus will be constructed. There are no plans to clean the mirror at this time. To solve the problems from the mirror joints, a new single segment mirror has been ordered; delivery is expected early in the next reporting period. A beamline software upgrade using LABVIEW is being tested and is expected to be installed during the next reporting period. This new software version improves the velocity scan control of the mirror scanning motors, permitting more accurate exposure compensation for mirror and other non-uniformities by variable scanning rates.

5.1.3.1 SVGL DALP Aligner Installation

Overlay problems observed during the BETA test of the stepper were traced to changes in the temperature of the jacket cooling water (JCW) supplied to the stepper. A secondary chiller was added to the JCW circuit to give better temperature control of the stepper's environmental chamber. Smaller effects observed after this modification were traced to air leaks in the stepper environmental chamber which caused excessive amounts of make-up air to be used. Correction of these has brought stepper operations into specification.

5.1.3.2 Other Beamline Activities

The parabolic collimating mirror from ALF-1 beamline was installed into RD-1 beamline, replacing the original flat mirror. This resulted in a 5.7× flux increase which greatly reduced the exposure time required for radiation damage and other experiments.

5.1.4 ESR Repair and Upgrade

Studies had shown that the beam current in the ESR was limited due to synchrotron light hitting cold surfaces within one of the two superconducting dipole vessels (D2). Two problems were identified: If the beam was steered upwards by a few millimeters it hit some cooling tube retaining clips that had become dislodged and if it were steered downwards by a similar amount, the light would hit the liquid nitrogen cooled collimators near the beam exit. Tests on the other dipole (D1) showed that it did not have the retaining clip problem, but did have the exit collimator problem. This

problem had been understood for some time, but until the installation of the faster SVGL aligner there was little reason to attempt the repair and upgrade. The decision was made to perform the work in the summer of 1996. The plan required warming the dipoles to room temperature, venting the ring, disassembling the straights connecting the two dipoles and modifying the affected components. The system would then require reassembly, bakeout, leak checking, cooldown, magnet training, commissioning and conditioning. The system was down for six weeks since leak-checking detected three weld leaks in D-1 that required welding and a second bakeout. The system was back in operation with normal peak currents and beam lifetimes greater than 10 hours by the end of June.

Subsequent beam studies showed that the modifications were successful. Substantial beam steering was now possible in both dipole magnets. Beam heating of the cryogenic system was substantially reduced from the levels prior to the upgrade and consistent with normal operations. Initial beam lifetimes were short, the recommissioning program of around-the-clock stored beam achieved acceptable beam properties, beam currents >200mA, and lifetime near 20 hours by early July. During this period of downtime several more changes were made to the system and the normal six month maintenance activities were performed. Some of these permitted unattended overnight running of the synchrotron by mid-July. This has since become our normal mode of operation.

After the acceptance of the SVGL aligner, one day per week was devoted to source studies and maintenance. Much of this time was spent on studies to increase the peak current and to then improve the lifetimes of large current beams. Figure 16 shows that beam lifetime recovered to pre-shutdown levels of about 30 hours in about three months. This trend is similar to the lifetime improvement during the first months of normal operation. Improved efficiencies of the energy ramp resulted in a peak stored beam current of 454mA. A highly efficient repeatable ramp for high peak currents has been developed, but presently the peak current is limited to 300mA due to beamline issues.

Figure 17 illustrates the greater usage of the light source after the upgrade compared to the month before. Due to the operating conditions at ALF, the tracked period is from 6:00 a.m. Monday to 6:00 p.m. Friday (108 hours). After the upgrade, the increased usage came with no additional manpower requirements due to the implementation of fully automated running overnight. The category of PM and studies has been larger after the upgrade in order to study larger current operations; this should be scaled back in 1997. The decision to make overnight running the default was made during the week ending 03 November 1996. Typically, the night-time running is for radiation damage automated exposures. The short week ending 01 December was Thanksgiving week. Before the upgrade, extended running would have required additional staffing. It is particularly noteworthy that the greater usage has not come at the expense of greater Helios downtime and, furthermore, the refills during the week are dependably short.

Since running with large currents, it was observed that a significant difference in RF system setpoint and readback was occurring due to beam loading. This was a concern for even larger beam current operations. An RF expert from Oxford Instruments in England made modifications to the RF system control board during the holiday shutdown period. In order to ensure source operations, the modifications were only made to the spare board so that operations could be restored by returning to the original board if necessary. Indications are that the modified feedback works very well. Testing continues in study sessions with the goal of converting to the modified card early in 1997.

5.2 SVGL Stepper

The actual installation and acceptance of the stepper was reported under DALP contract N00019-91-C-0207. Since the acceptance of the stepper, performance optimization activities have continued and scheduled application lots were begun.

5.2.1 Performance Improvement and Optimization

Signal-to-noise at mask alignment was improved by a factor of three by modifying the XRIS detector to improve its signal-to-noise ratio. The system's thermal stability was also improved, as previously reported. These improvements led to the aligner consistently achieving its design objective of 20nm 3σ grid repeatability. Grid accuracy was confirmed. Software modifications were made to allow multiple virtual masks per wafer and to correct for rotation and the $+x$ and $-y$ framing blades were adjusted. This was in preparation for a detailed Beta acceptance test.

5.2.2 BETA Acceptance Test

A detailed acceptance test including throughput, contamination and reliability was performed.

5.2.2.1 Overlay

The aligner contribution to overlay error was characterized by two level exposures using two masks on 13 wafer types with the same overlay offsets for all types. The systematic mask and beamline signature was removed. The data revealed additional "systematic" errors caused by wafer stage rotations. X-mean offset fluctuations caused by misalignment of the wafer stage rotation detection laser interferometer were corrected. Metal and CMP wafers had a process-induced offset analogous to optical steppers. The aligner overlay performance met or was near the pre-production tool specification. The alignment to absolute grid measurement was near specification and limited by the accuracy of the measurement tool. The aligner-to-itself overlay performance was near to and in many cases exceeded the prototype specification of mean plus 3σ $<$50nm for most process levels. Figure 18 shows the overlay data

histograms for the test with the mask contribution removed. The best case after software correction was 41nm for *X* and 34nm for *Y* absolute plus 3σ.

5.2.2.2 Reliability

Reliability was measured for the entire system, including the track, SMIF/load and unload station, and hot plates, by recording any run failure which forced ejection of one or more wafers. Ninety-four percent of the wafers completed processing. Twelve failure incidents were recorded, five of which were from a known software problem for which there is now a "work-around."

5.2.2.3 Contamination

Contamination was tested by cycling wafers through the system and measuring their contamination levels before and after the runs. Two test ranges were used: 12μ and greater and 0.3 to 12μ. No particles greater than 12μ were found. Typically, five to seven smaller particles are added each pass. The source of these is being investigated.

5.2.2.4 Throughput

Aligner throughput during the BETA test was about 12 wafers per hour under the standard conditions. The main detractors were mask alignment and XRIS calibration on each wafer. The software is also not optimized for throughput. An 83% throughput improvement has been achieved (22WPH) by improving the system stability to allow the exposure of multiple wafers between mask alignment and XRIS cal, by increasing wafer stage stepping speed from 50 to 125mm/second, and by reducing software delays. This aligner throughput improvement was achieved without overlay performance degradation. Work is continuing on refinement of software control and additional aligner operations optimization for throughput improvement. Figure 19 shows the target specifications for the stepper and the present status of each.

5.3 SVGL Stepper Applications Support

Good resist processes are required to perform mask verification printing. In addition to APEX-E, our process-of-record, other resist systems have been explored to determine if they might provide even better performance.

5.3.1 APEX-E

Studies have shown that across wafer linewidth variation (AWLV) with APEX-E resist does not vary significantly with feature sizes from 350nm to 175nm. APEX-E has also been characterized for printing 100nm features. The dose latitude at a 25μ mask-to-wafer gap is about 20% better than at a 40μ gap. The AWLV CD control is about 8-10nm. The Apex-E process was reoptimized early in this reporting period with

about a 20% gain in sensitivity, with no observable deleterious effects on contrast or biases.

5.3.2 Other Resists

A sample of TDUR resist was obtained from Tokyo Ohka Kogyo Co. No mask contamination growth was found on a test series in the Suss 2 stepper, but other tests did not warrant further investigation. Two commercial formulations of ESCAP resist (UV2-HS and UV3HS) did not show good performance for x-rays because of low sensitivity and small over-exposure linewidth budget for isolated lines. Special high and low contrast lots were formulated by IBM Almaden. Development and chemical contrasts of the two formulations were studied. Dissolution inhibition properties of the formulation's components are thought to play a dominant role in the resist contrast and linewidth performance (see 3Q96 report). It was shown that proper blends of components with different dissolution inhibition properties may result in optimal lithographic performance.

5.3.3 New IBM Resist

A new IBM resist, UV-4, is being evaluated for x-ray exposures. This resist has better isolated line performance compared to UVII-HS resist. Similar to UVII-HS, it has very low sensitivity in the range of 240-270mJ/cm^2 for nested and isolated 175nm lines. An experimental sample of UV-4 resist without base additive has been prepared to increase its sensitivity. Sensitivity for isolated lines was increased to 230mJ/cm^2 compared to 270 for the standard UV4 but at the expense of the linewidth over-exposure budget. The process development for UV-4HS is continuing. Figure 20 shows the linearity of UV-4HS under a standard set of conditions for both nested and isolated lines. Figure 21 shows well-resolved 125 and 175nm images with UV-4 resist. Figure 22 shows the process latitude of UV-4HS for both exposure and post expose bake. Both resists are acceptable for the 1Gb (175nm) application with UV-4HS being preferable for the more complex levels. The photospeed of this resist (170-300mJ/cm^2 depending on feature type) is the main limit to stepper throughput. Improved across chip linewidth variation (ACLV) performance is expected when the beamline scannong mirror is upgraded early in the next reporting period.

5.4 Contamination Control

5.4.1 Shipping and Handling

In this reporting period the mask shipping container has advanced from an interim white box to a single mask SMIF pod with a special liner. The goal is to ship and handle all critical masks in the dedicated SMIF pods. Also in this period, the ALF cleanroom was upgraded with additional tool mini-environments, the conversion of ALF 1 stepper chamber to a clean wafer processing area, an increased level of garmenting and additional point-of-use filtration for the process DI water. Figure 23

shows the decrease in airborne particle count before and after the introduction of the new garments.

5.4.2 Protective Covers

The feasibility of a protective mask cover pellicle was previously demonstrated on the Suss stepper. During this period, work continued on protective covers for the x-ray masks. Several types of PMMA and polyimide covers were tested but all failed radiation resistance tests. It was also determined that a different type of mounting ring would be required for the SVGL stepper versus the one developed for the Suss stepper. Material and technique development are continuing.

5.4.3 Mask Cleaning

It was decided that ALF would concentrate on laser cleaning of masks and that the work on wet chemical cleaning would be done at the MMD in Burlington, Vermont. An existing 193nm laser ablation tool in ALF has been modified with an upgraded stage and control system to handle masks and wafers. This is a dry class 1 laser ablation cleaning tool for masks and wafers up to eight inches. New software is being planned to take KLA SEMspec or mask Inspex coordinates and drive to the appropriate location for cleaning. Figure 24 shows how the laser was able to clean a dirty sample. An IBM European-patented technique called laser steam cleaning is also being investigated. Here a thin layer of liquid is condensed on the mask or wafer surface. Then a 248nm laser pulse causes the liquid to explosively vaporize and the expanding vapor carries 0.1 to 2μ and larger particles away from the surface. A test system is currently being installed in ALF. It should be on-line early in the next reporting period. Mask lifetime work is continuing in the SVGL stepper. One mask was used for 10534 fields with no added defects at a total x-ray dose of 2043J. There was also no change in image placement as measured on the wafers and no growths on the mask. The mask was stored in a SMIF pod with minimum handling. This work is planned to be continued to 100,000 fields.

5.4.4 Defect Modeling

5.4.4.1 Defect Printability Modeling Summary

An extensive study of x-ray mask defect printability using simulation was completed in 3Q96 by a University of Wisconsin summer student working with Motorola engineers at ALF.

Isolated defects on the x-ray membrane and isolated defects on protective covers mounted behind the x-ray membrane were modeled. Defects in proximity to x-ray absorber features and absorber fabrication defects were also considered (absorber linewidths ranged from 100-175nm). Spheres and parallelepiped defect shapes composed of PMMA, ammonium sulfate and stainless steel were modeled at gaps in the range of 10-50μm. Spheres printed more readily than parallelepipeds. Increasing the

gap reduced defect printability only slightly. In summary, spheres as small as 0.2μm in diameter, regardless of material composition, must be detected and removed from mask membranes. Also, organic defects and ammonium sulfate must be at least 1μm in size to print, but metallic defects $>0.3\mu$m are likely to print.

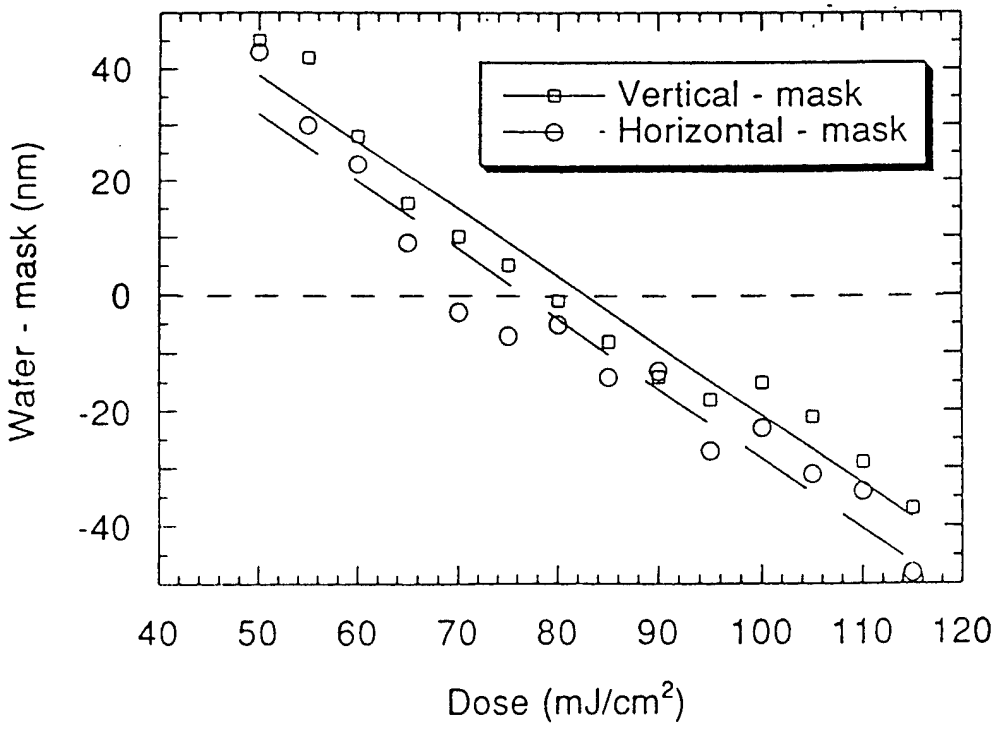


Figure 15. New Beamline Mirror (Horizontal versus Vertical)

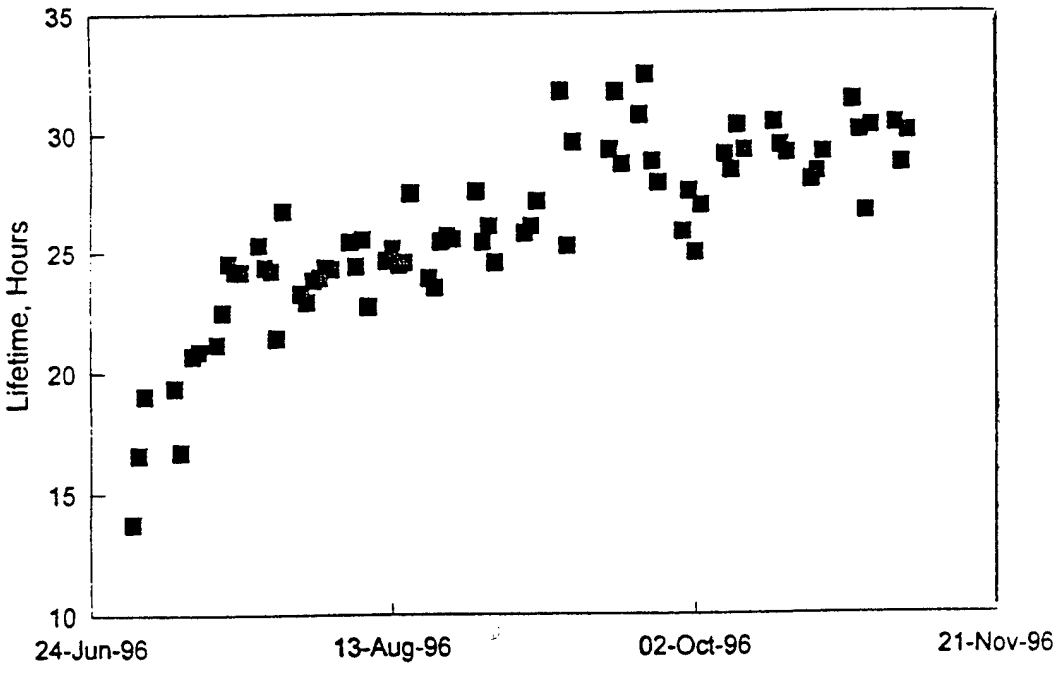


Figure 16. Lifetime at 200ma

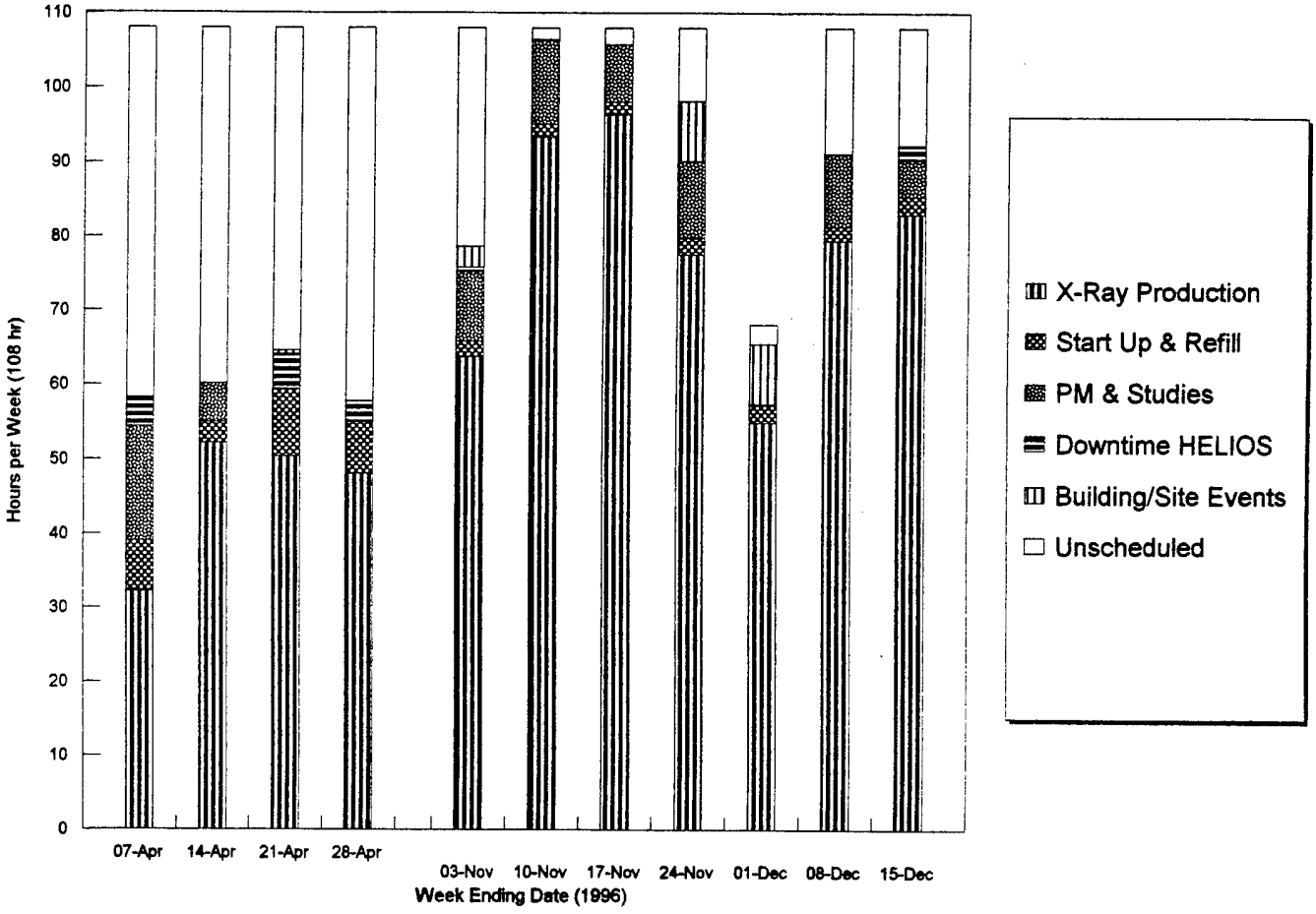
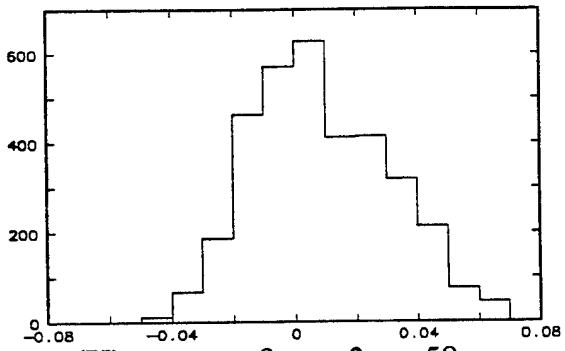
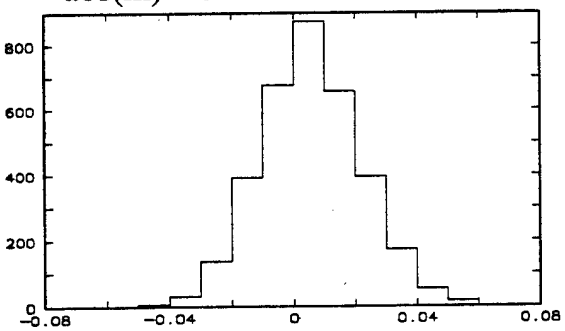


Figure 17. Typical Usage of Synchrotron Before and After Upgrade

(etched Si wafers, depth = 100 nm)
(before S/W correction)

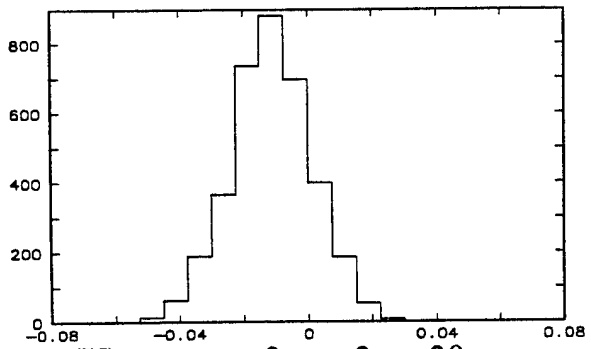


(X): mean = 9 nm, 3σ = 58 nm
abs(m) + 3σ = 67 nm

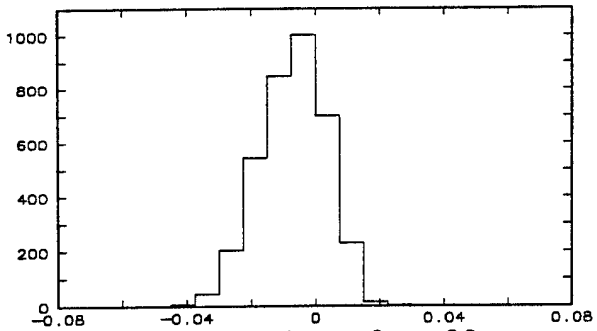


(Y): mean = 6 nm, 3σ = 37 nm
abs(m) + 3σ = 43 nm

(same wafers reworked and
after S/W correction)



(X): mean = -2 nm, 3σ = 39 nm
abs(m) + 3σ = 41 nm



(Y): mean = -1 nm, 3σ = 33 nm
abs(m) + 3σ = 34 nm

Figure 18. Overlay Data Histogram (Mask Signature Removed)

Aligner Requirements	Preproduction Requirement	Verified Performance	Production Requirement
Resolution	250nm	150nm	150nm ✓
Line Width Control (3σ)	12nm	10nm (Inclusive of Beamline, processing and metrology; data taken over 37 fields on a wafer)	12nm ✓
Overlay (Mean + 3σ) (nm)			
Stepper-to-Stepper	70	Not Yet Measured	50
Stepper-to-Self	50 ✓	50	33
Stepper-to-Absolute Grid	20	20	20 ✓
Mask-to-Wafer Gap (μm) (Gap must be continuous within the range specified)	10 - 50	Testing Limited To 20	5 - 50
Gap Accuracy/Precision (μm)	±1.0 / ±0.5	±1.1 + 1.5 offset / ±1.1 Recalibration Req	±1.0 / ±0.5

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Figure 19 (Part 1 of 3). Stepper Specifications

Aligner Requirements	Preproduction Requirement	Verified Performance	Production Requirement
Alignment Systems	Off-Axis	Requirement Met	Off-Axis ✓
	Through the Mask	Not Yet Tested	Through the Mask
Alignment Modes	N site Global where N ≥ 3	Requirement Met	N site Global where N ≥ 3 ✓
	Field-by-Field	Supported Upon Software Debug	Field-by-Field
TV Wafer Microscope	Required	Requirement Met	Required ✓
X-Ray Image Sensor	Required	Requirement Met	Required ✓
Alignment Mark Size (μm) Marks shall fit into the kerf area between chips	100 max width	Requirement Met	100 max width ✓
Alignment Mark characteristic feature size (μm)	≤ 0.5	Requirement Met	≤ 0.5 ✓

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Figure 19 (Part 2 of 3). Stepper Specifications

Aligner Requirements	Preproduction Requirement	Verified Performance	Production Requirement
Throughput (Wafers/Hour with 20 overlaid fields in Global Alignment Mode) (1-sec exposure; 100mW/cm^2 power density; 100mJ/cm^2 resist sensitivity.)	≥ 40	≥ 16 (Cal per 1-Wafers @ 50nm Overlay) ≥ 25 (Cal per 6-Wafers @ 80nm Overlay)	≥ 60
Wafer Size (mm) (flats or notches)	200 Baseline 100, 125, 150 (optional)	200 Supported 100, 125, 150 (Supported upon planned retrofit of compatible SMIF)	200 Baseline ✓ 100, 125, 150 (optional)
Batch Size (Conform to SEMI standard Carriers and provide dual input/output cassettes.)	25	Requirement Met	25 ✓
Wafer Input/Output	SMIF	Requirement Met	SMIF ✓
Mask Envelope	ARPA / NIST per SVGL Dwg #868-1001-001	Requirement Met	ARPA / NIST per SVGL Dwg #868-1001-001 ✓
Field Size (mm)	50 x 50	Requirement Met	50 x 50 ✓

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1196TWG.PPT

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Figure 19 (Part 3 of 3). Stepper Specifications

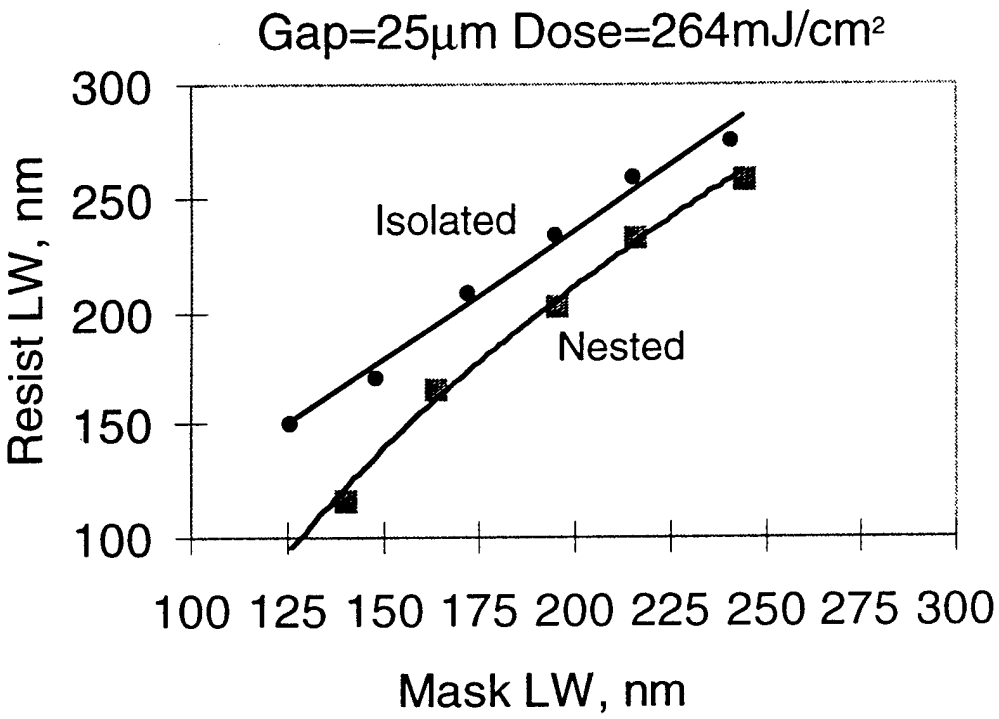


Figure 20. UV-4 Linearity

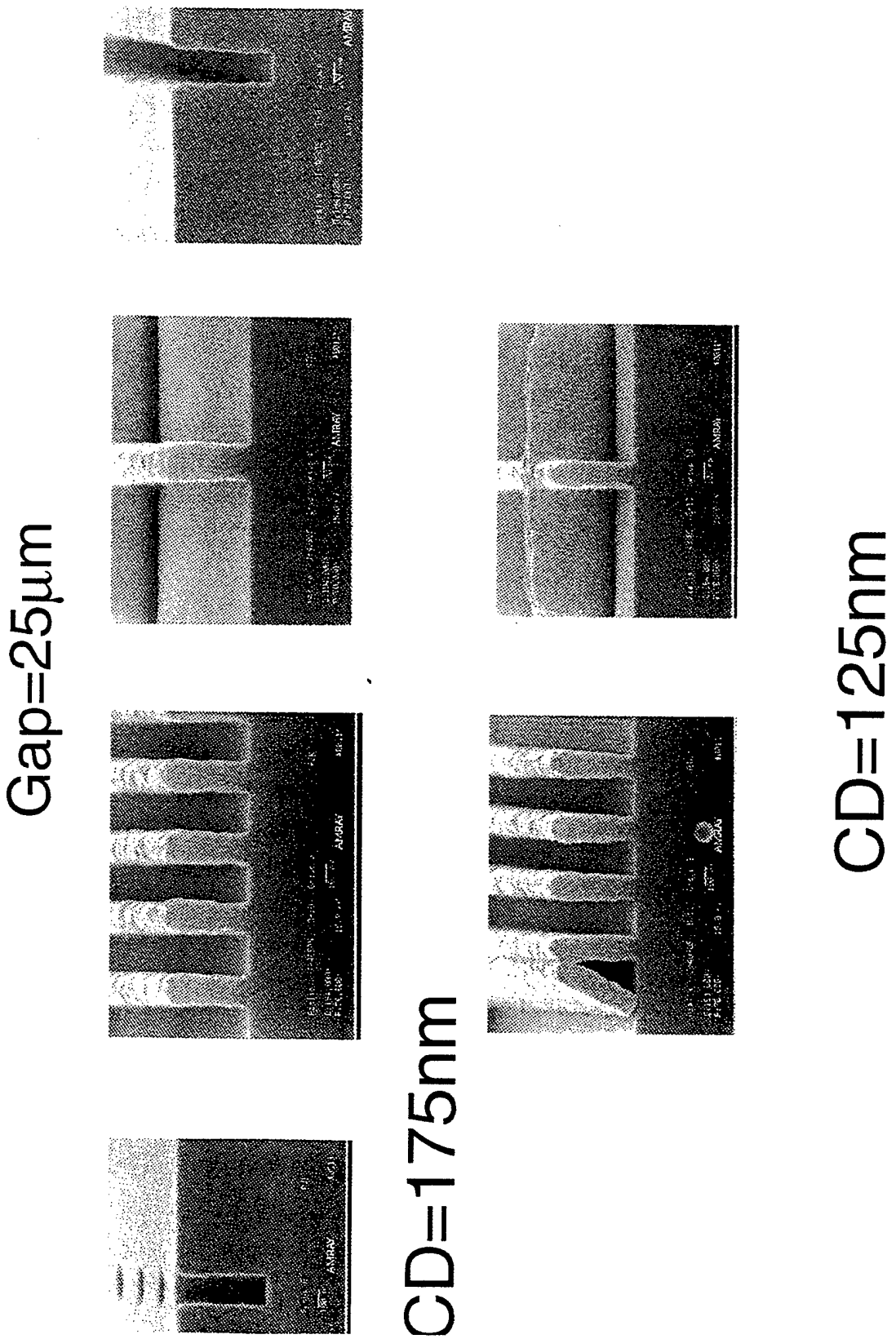
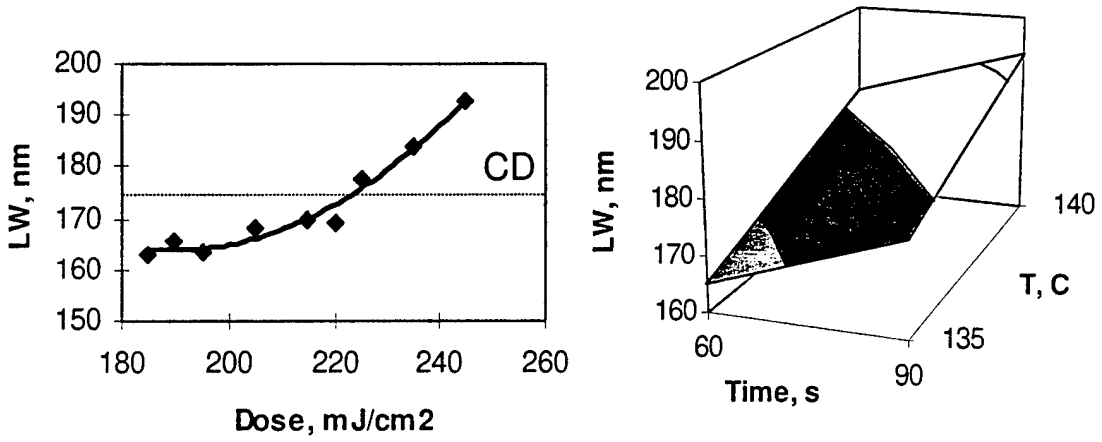


Figure 21. UV-4 Resolution Capabilities



Exposure Latitude:

+/- 10% (Gap=25μm)

PEB: T=140C, t=90s

PEB latitude

0.5nm/1sec; 3.2nm/1C

Gap=25μm, Dose=245mJ/cm²

Figure 22. Process Latitudes for UV-4HS (Trench Level)

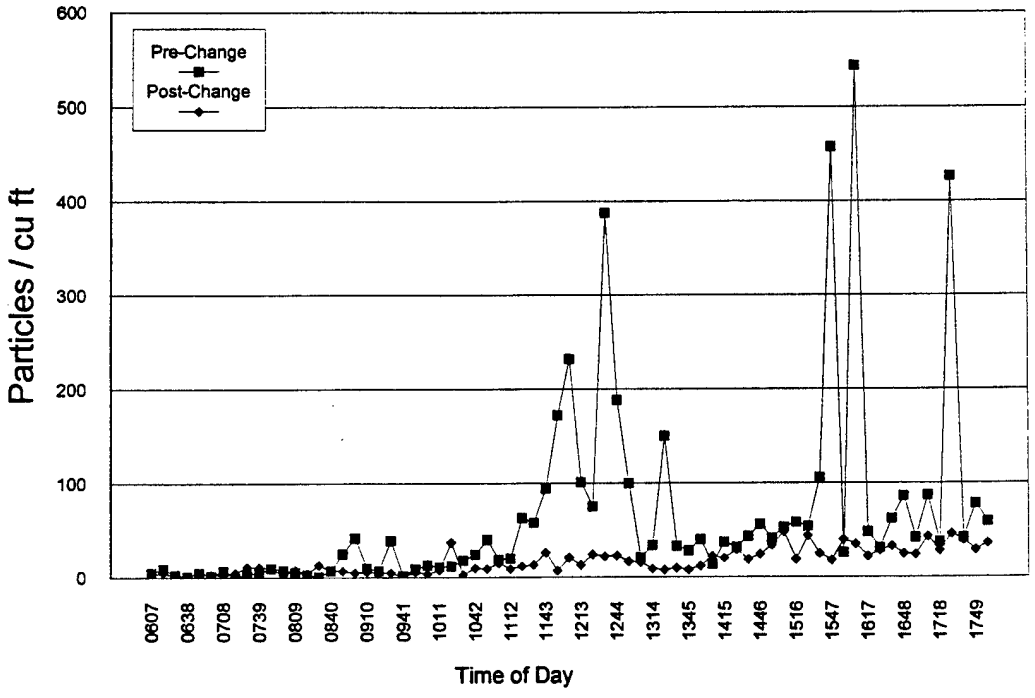


Figure 23. Pre- and Post-Garment Change Particle Count.. ALF cleanroom - particles >0.3μm.

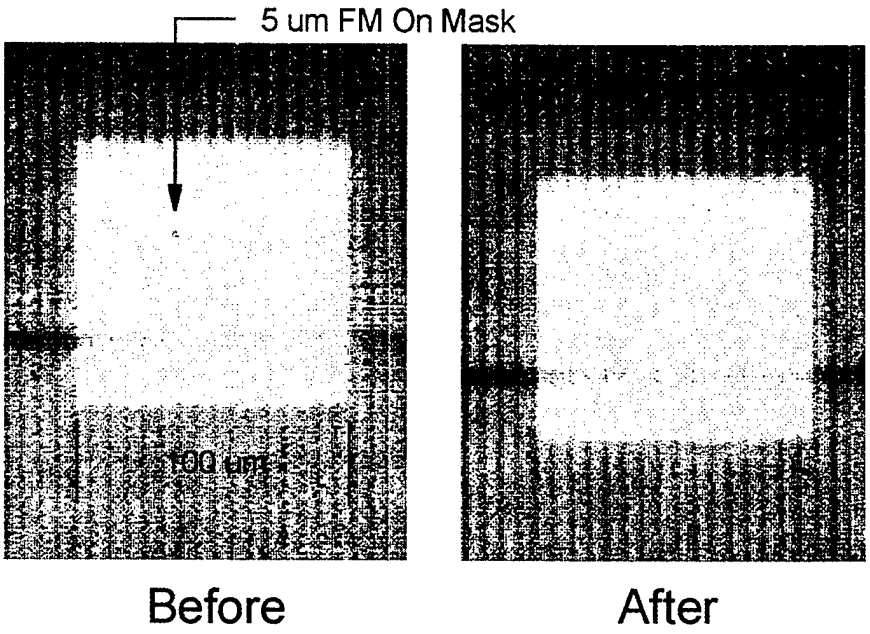


Figure 24. Talon Gold Mask Cleaned with ALF ASAT

6.0 Technology Acquisition (Task 8)

Task Objective: Evaluate the applicability and utility of new technology and tools to use in the MMD pilot production lines with the objective of improving production efficiency, quality, and profitability, and achieving progressively smaller mask feature sizes.

The major focus in the area of Technology Acquisition this year was the beginning of the MMD commitment to transfer from boron-doped silicon gold masks to silicon carbide refractory masks.

At the beginning of 1996, both Hoya and Fujitsu shipped silicon carbide substrates to the MMD for evaluation. The quality of the films from Hoya were superior and they became a conditionally qualified supplier in the third quarter. The Hoya in-house polishing and defect control improved throughout 1996 and the MMD was able to fabricate a defect-free NIGHTHAWK with a silicon carbide substrate.

A study of suitable refractory wet membrane etch chemistry was completed this year and a KOH chemistry was chosen due to superior quality and etch times. It was also determined that the Fountain Cup etch process will be used in the long term and these fixtures are now in fabrication. In the short term, a Full Immersion Compact etch will be used.

SNR 200, a chemically amplified negative resist, was qualified for product use. This resist will be used for positive level refractory masks and was used to ship negative level gold masks during 1996. A new hot plate bake was also qualified and resolution of 150nm×250nm was seen on membranes. Also this year, qualification began on UVIII, a chemically amplified positive resist. Full qualification is scheduled for 1997.

To achieve better image placement and image size control, work was started on the use of a conductive topcoat, polyaniline, during e-beam exposure. It was found that raw image placement, image placement repeatability and image size variation with multiple pass exposure improved with this topcoat. It was determined that polyaniline will be a key contributor to reaching 0.13μm groundrule specifications. Therefore, coating capabilities have been transferred to the MMD.

Work was also completed on blanket e-beam pre-exposure to relieve resist stress. It was concluded that while raw image placement improved, repeatability was slightly worse, and this technique will not be pursued.

In the area of improving image size variation, other alternative Proximity Correction Algorithms were evaluated this year. The current algorithm, DOSE5X, was compared to DOSE5XE and DOSE6X using both PMMA and SNR. Since the MMD will be using snr with positive level refractory masks in the future, its results were the most interesting. While it was found the DOSE6X had code that was not complete which gave

negative dose assignment to critical shapes, DOSE5XE experimental results were superior to DOSE5X and is now being used.

6.1 Silicon Carbide Status

Two aspects of the film quality of the 125mm SiC wafers received from HOYA seen in Table 3 are defects and thickness uniformity.

The defect levels as-received and post-incoming megasonics clean (strong acid cleans) can be seen in Figure 25. This data was collected from a Tencor 4500 tool at a sensitivity of 0.05, based on a calibration wafer of 1.0μm. The circles represent the pre- and post- quantities in defects per centimeter squared of the defects approximately 0.5μm and larger. The "X" represents the total defects from 0.2μm and larger. There was a forty-two percent decrease in the total defects with a megasonics clean and a forty-four percent decrease in the larger 0.5μm defects with a megasonics clean. The January, 1997 shipment consisted of 20 pieces cleaned to specification for both large and small defects. The cleaning information will be given to HOYA to aid them in improving the silicon carbide storage and shipping procedures.

The same wafer films were measured in nine points interferometrically in the NIGHTHAWK membrane area. Figure 26 represents a total of 1125 measurements averaged per wafer and plotted with the lot mean and high wafer average and low wafer average. The within-wafer uniformity is very good, as seen in Table 3, with the first November shipment having the highest range of 0.03μm. The remaining shipments were all below 0.015μm.

To further quantify the number of "pin hole" defects in the silicon carbide films, two wafers from the first November shipment were "decorated" by immersing the wafers in the 107°C KOH (potassium hydroxide). KOH will etch silicon in the pin hole areas. These wafers were then microscope-inspected for defects. Approximately 10 to 15 defects, not pin holes but "globs" of silicon carbide, were found. These silicon carbide defects are more prevalent than pin holes and were analyzed by EDX for composition (Figure 27). Characterization information regarding this defect has been given to HOYA to assist them in eliminating it. One membrane of the 125 received was found to have a large pin hole.

Table 3 (Page 1 of 2). Hoya Silicon Carbide Evaluation Summary

Month Year	Samples sent/ received	Incoming FM	Transmission optical HI MEAN LO	flatness: overall, membrane	thickness and uniformity	Image size	Image placement final	KLA	Comments
units	*number*	*defx/cm²*	*%@=600nm*	*(μm)*	*(μm)*	*(nm 3σ)*	*(nm 3σ)*	*(defx/cm²)*	
Target/ Spec		*<1 of .5μ <5 of .2μ>*	*>50*	*<1.0*	*2.0±0.1 0.05*	*250,20*	*<50 X,Y*	*10 rprbl 0 non*	
April 1996	*25/10*	*245*		*7.7 2.9*	*2.66 0.03*	*188 20 301 47 193 17 302 29*	*56,47 40,40*	*68.2 4.16*	*lower sens.tencor lab result=res. slurry 1.32defx/cm² substrate related*
May 1996	*5*	*7.5*	*50*	*5.4 4.3*	*1.8 0.04*				*1 lost etch/alignment 1 lost bond*
H10A						*334 30 499 29 249 26*			*SVGL2NEW V052196D Shipped*
H16A						*171 26 276 27*	*58,68(R) 41,45(F)*	*336(W/O repair)*	*NHWK V052296B(PSE)*
H13A						*164 20 235 23*	*50,45(F)*	*7.1defx/cm² (0 W/repair)*	*NHWK V061296C(PSE) Shipped H30A H38A H39A received this time*
June 1996									
July 1996	*H4B H9B H11B*	*(3.8)3.1 (4.6)3.1 (4.9)3.6*		*7.7 6.2 11.0*	*1.8 .015 1.7 .036 1.8 .012*	*170 20*	*99,95*	*6.04*	*Broke in Bond NEAGLE*
August 1996	*75unscrb/0 H16rwk*					*261 37 153 21*	*52,39(F)*	*437.9*	*rwk FM*
Sept 1996	*150unscrib/0*								
	H30A					*224 15 133 5*	*47,42(F)*	*>500 non substr*	*older vintage*
	H39A					*231 17 133 6*	*46,39(F)*	*1.5*	*Shipped*
	H38A					*242 18 147 15*	*51,45(F)*	*5.478 @0.09*	*Shipped*
Oct 1996									

Table 3 (Page 2 of 2). Hoya Silicon Carbide Evaluation Summary

Month Year	Samples sent/ received	Incoming FM	Transmission optical HI MEAN LO	flatness: overall, membrane	thickness and uniformity	Image size	Image placement final	KLA	Comments
Nov 1996	*100unscrib/ 25SiC*	*(4.2)4.1 (51.2)51.6*		*8.6*	*2.02 .015*				*backside/frontside issue..no scribe*
	25SiC	*(6.7)6.6 (9.3)8.7*		*8.6*	*1.99 .03*				
Dec 1996	*200unscrib/ 25SiC*	*(3.4).84 (14.2)17.8*		*7.8*	*2.05 .0108*				*begins to meet FM spec*
	15SiC(A)	*(3.8)1.4 (33.7)18.2*		*8.7*	*2.07 .014*				
	15SiC(B)	*(14.8)2.3 (115.2)17.9*		*7.8*	*2.08 .014*				
Jan 1997	*250unscrib/ 20SiC*	*(3.2) 2.3 (28.2) 4.1*		*10.6*	*2.01 .011*				*All meet .2μ spec*

6.1.1 HOYA

During the last quarter of 1996 IBM received 105 product quality silicon carbide wafers with Hoya reporting a yield of 65%. This is an improvement of 15% over the last quarter. A decision was made to cancel all orders for refractory metal deposition from Hoya. Deposition will be completed at Motorola's PCRL facility, with additional work also to be done at IBM Yorktown Research, until a system is ordered and received at MMD, at which time all depositions will be processed in-house. This allowed Hoya to increase its output of silicon carbide to 100 wafers/month for the remainder of the current purchase order. Negotiations are underway to improve wafer yield, identify and reduce defects and reduce per-wafer cost. Hoya will be reporting on these activities at a 05 March 1997 meeting at IBM.

Data for September through December 1996 and January of 1997 can be seen in Table 3. Although incoming foreign material levels are still higher than specifications, Megasonics clean reduced them to nearly target levels.

A benchmarking was completed with the Hoya-deposited refractory metal (Ta_4B) using the NIGHTEAGLE pattern. Two masks were built and used to build a coarse PSE. The image size and image placement results are shown in Figure 28 and Figure 29. There is some variability in the numbers, but the median values are very close to the averages seen with gold during the same timeframe.

6.2 Refractory Metal

The refractory metal process is being transferred from Motorola's Phoenix Corporate Research Lab to the MMD. The current refractory stack includes a 5000Å layer of tantalum silicide (TaSi) as the absorber, and a 2000Å layer of silicon oxynitride (SiON) as the hard mask. Some initial work was done using a 300Å layer of chromium as the hard mask; it was decided however, that the oxynitride film would be a better choice because of the film stress requirements (reference CDRL G004, 97-MMD-LFSC-00020).

For the current process flow, both the absorber and hard mask layers are deposited at Motorola onto the Hoya SiC-coated wafers before membranes are formed. The parts are then shipped to the MMD after which the front end of the line process continues. Membranes are formed and the wafers are bonded to NIST rings. The parts are then coated with resist, exposed by the EL-4 P0 electron-beam tool, and developed. At this stage the masks are usually shipped back to Motorola for etch of the hard mask and refractory stack. They are then shipped to MMD for metrology, inspection and repair.

6.2.1 Refractory Metal Deposition

As mentioned in Section 6.1, a decision was made to purchase a deposition system for MMD rather than continue to attempt to purchase wafers with metal stacks from Hoya. This decision was based on capacity demands and cost issues. Tantalum silicide deposition will continue at Motorola in Phoenix with increased output. IBM Yorktown has completed installation of a laboratory sputter deposition system which will be used to develop a low stress tantalum silicide process as a backup for Motorola. Sputtered Films Inc. has ordered a Ta_5Si_3 target which will be used to produce tantalum silicide films to evaluate their deposition system for potential purchase by IBM. On-site review of the SFI tool by IBM and Motorola personnel during December of 1996 indicated that this system is of excellent design and construction. Capital justification, tool specification, requests for quotation and tool evaluations will be completed during first and second quarter with tool purchase planned for June, 1997 and installation at IBM by year-end.

Defect density in refractory films is currently being tracked. The silicon carbide films were inspected at a 0.05 sensitivity with a 1.0μm calibration wafer, and the average defects per wafer was 8.7 defects/cm^2. These same pieces, when inspected after refractory absorber stack deposition and reduced to 1.0 sensitivity, were found to have 116.5 defects/cm^2. Reduced sensitivity is used when inspecting films with rough surfaces such as the silicon oxynitride hard mask. These wafers had a defect density of 104 defects/cm^2 after a megasonics clean with a strong acid. After front-end-of-line processing, they were found to have 33.5 defects/cm^2. Inspections will continue and the sources of the defects are being investigated by Motorola. Also, a series of cleans are being implemented during the film deposition processes at Motorola (see Section 6.2.5).

6.2.2 Silicon Oxynitride Hard Mask Etch

The capability is currently being developed to perform both hard mask and absorber etches in the MMD. This process transfer should be complete by the end of February, 1997. After this time, the entire back end of the line process will be done at the MMD.

A Plasmatherm parallel plate dry etch system in MMD was reconfigured to perform the etch of the silicon oxynitride hard mask layer. The process involves a fluorinated etch chemistry as developed by Motorola. Since there are certain differences between the tool used by Motorola and the one in MMD, significant process adjustments were necessary. Initial work to transfer the oxynitride etch process into MMD was started in December of 1996. Significant progress has been made in a relatively short time with a limited number of samples.

A typical set of process conditions are as follows: 1sccm O_2, 7sccm CHF_3, and 20sccm Ar flowing at a pressure of 20mT, substrate temperature of 20°C and incident RF power of 350 watts. An overetch of 40% was used to ensure that the smaller features

were clear. This set of conditions gives an average linewidth bias of 10nm. The linewidth bias ranges from -2 to 18nm and tends to increase with feature size as shown in Table 4 The selectivity of the oxynitride to negative resist was found to be approximately 4:1. The current process conditions tend to degrade the profile of the resist during etch resulting in some faceting especially on the smaller features. This faceting does not seem to transfer to the TaSi profiles during absorber etch; however, it may be contributing to the negative biases seen there. Work to further improve upon these results is in progress.

Table 4. Linewidth Data from SiOn Etch Optimization

Feature Size Nominal	Before SiON Etch	After SiON Etch	Linewidth Change
175x200nm	*167nm*	*165nm*	*-2nm*
250x250nm	*239nm*	*245nm*	*6nm*
250x500nm	*226nm*	*244nm*	*18nm*
500x500nm	*468nm*	*484nm*	*16nm*

6.2.3 Tantalum Silicide Absorber Etch

The tantalum silicide etch process in the MMD is performed on the new Plasmatherm etch tool. The initial etch development work was done on masks with a chromium hard mask. The set of process conditions that seemed to work best for this etch were as follows: 20sccm Cl_2 flowing at 2mT pressure, 120 watts RF power, and a substrate electrode temperature of 10°C. An overetch of 25% was used to clear the smaller features. This gave an etch bias of -20 to -35nm.

Since silicon oxynitride was chosen to replace chromium as the hard mask, the etch development is now being done on parts with SiON hard mask. The etch process was first developed at Motorola, and is now being transferred to the MMD, much like the silicon oxynitride etch process. This work was also started in December of 1996, and progress continues. The process conditions have not shifted significantly from the conditions with the chromium hard mask. A set of typical etch results is shown in Table 5. This data was collected on a part etched at 120 watts rf, 20°C substrate temperature, and the rest of the conditions as given above. The profile after this etch is good with straight sidewalls, and the etch bias in this case is around -17 nm. Work is currently underway to improve upon these results in conjunction with the oxynitride etch. The selectivity of the tantalum silicide to silicon oxynitride is approximately 4:1 during the tantalum etch.

Table 5. Linewidth Data from TaSiNx Etch Optimization

Feature Size Nominal	Before TaSiNx Etch	After TaSiNx Etch	Linewidth Change
175x200nm	*165nm*	*148nm*	*-17nm*
250x250nm	*245nm*	*228nm*	*-17nm*
250x500nm	*244nm*	*228nm*	*-16nm*
500x500nm	*484nm*	*467nm*	*-17nm*

Even though the negative e-beam resist is still present on the masks after oxynitride etch, the resist disappears halfway through the tantalum etch process. Therefore, a resist strip is not needed after this etch. The oxynitride hard mask can be stripped in a dilute mixture of buffered hydrofluoric acid.

6.2.4 Refractory Substrate Membrane Etch Process

6.2.4.1 Immersive Compact Etch

New modified compact fixtures for fabricating SiC membranes have been qualified and are being used in the process. All necessary set-up requirements (heated KOH tanks, hot DI rinse, etc.) for the etch process have been completed. The complete process has been qualified and is being routinely used to fabricate SiC membranes. The yield is 87% from the limited number of substrates etched using the new set-up.

A compact fixture for NIST ring bonded wafers was fabricated at Motorola's Sensor Division in Phoenix. Some additional design modifications are needed, however, in order to implement the process for etching bonded substrates.

6.2.4.2 Fountain Cup Etch

This process involves continuous wetting of the wafer back side using a fountain of KOH while recirculating and filtering the etchant throughout the etch. The demo etching experiments using the fountain cup process were performed by modifying an existing Au plating system at Motorola's PCRL. This process could be used to fabricate SiC membranes on substrates bonded to NIST rings as well as unbonded wafers.

Demonstration experiments showed 100% yield on both bonded and unbonded wafers. The etch was performed on wafers with refractory stack on several different membrane sizes from 25mm×25mm to 50mm×50mm. The main highlights of these experiments are:

- No leakage was observed during the 8 hour etch. The long etch was required because of a temperature limitation of the current system and the KOH concentration used.
- No degradation of the refractory stack or substrate edges or NIST rings was observed.
- No defect source was identified
- Substrates were loaded/unloaded efficiently

In summary, the Fountain cup method is the final choice for a manufacturing etch station. The immersive compact etch method will be used during the transition period until the etch station is delivered, then as a back-up strategy. A comparison of the two techniques is included in Table 6.

Table 6. Comparison of Membrane Etch Process Techniques		
Parameter	**Compact etch**	**Fountain Cup**
Typical chemical capacity	*4 gallons*	*16-24 gallons (6-8 cup)*
Operator safety/handling	*Operator in touch with some KOH fumes/solution*	*No contact with fumes or solution*
Throughput (6 compacts or cups)	*12/shift*	*12/shift*
Throughput (8 compacts or cups)	*16/shift*	*16/shift*
Estimated yield (based on demo experiments)	*90%*	*Greater than 95%*
Extendibility to various sizes	*Compact/design changes with substrate specification change*	*Two locking caps needed (wafers & NIST rings)*
Automation	*Robotic handling possible, always manual mounting/unmounting*	*automation possible*
Process induced defects	*Greater probability (more manual handling)*	*Low Probability*
Estimated cost (First Phase)	*120K Manual loading*	*170-200K Manual loading*
Maximum membrane size	*50×50mm (untested)*	*50×50mm demonstrated*
Unbonded wafer fixturing	*O-ring contact with wafer edges*	*Four point wafer contact*
Bonded wafer fixturing	*O-ring contact on NIST ring*	*Four point clamps on NIST ring*
Leakage	*Degrades wafer surface*	*Might not degrade the surface or rings*
Loading/unloading time(6)	*30-45 min.*	*5-10 min.*
KOH Filtration	*Required*	*Required*
Recirculation	*Not essential*	*Required*
AutoFill	*Essential*	*Essential*
End point Detection	*Visual*	*Timed Etches*

6.2.5 Refractory Wet Chemical Cleaning

The chemical cleaning process for the refractory parts using megasonic power has been implemented. The parts are cleaned at various stages of the membrane fabrication process. The cleaning recipe is a modified RCA clean using piranha (H_2SO_4:H_2O_2) at 120°C and NH_4OH:H_2O_2:H_2O at 55°C.

In addition, wet chemical cleans have also been extended to the final mask clean both for refractory masks as well as gold masks. The process has demonstrated 100% removal of foreign material on the final masks. The role of megasonic power on the image characteristics is also currently being investigated.

6.3 Proximity Correction Algorithm Evaluation and Optimization

A Technology Assessment report was submitted to document the results of comparisons of the DOSE5X, DOSE5XE and DOSE6 for PMMA/gold. (CDRL G004, 97-MMD-LMFS-00002).

Benchmarking results reported in section 4.2.2 included the optimized proximity corrections for SNR. Additional optimization will be completed with the TaSiNx stack with silicon oxynitride on SiC when the final etch processes are implemented at MMD.

An initial DOSE6 algorithm evaluation was completed. A matrix was completed for the PMMA proximity correction values which resulted in negative doses for very small images. Investigation of this problem found that DOSE6 cannot be used to post-process shapes with a size much smaller than alpha. The PMMA-required alpha of 0.1 could not be used with 0.075μm images (required for 0.175μm lithography with a 0.1μm bias process bias with PMMA). A test of smaller alphas with DOSE6 did not give acceptable results. Consequently, DOSE6 will not be implemented for PMMA/gold.

However, the SNR alpha of 0.06 can be used. This, combined with the 0 bias process with SNR/refractory, makes DOSE6 an option. An initial comparison of DOSE5XE vs. DOSE6 for the same set of proximity corrections shows only small differences, as expected (Figure 30). DOSE6's real improvements will come when the software is completed to include more than two Gaussians for approximation of the dose distribution. This software is expected in 1997. In the meantime, the optimization of SNR/refractory proximity corrections for final etched images will be completed with both DOSE5XE and DOSE6 to see which gives the best results.

6.4 Conductive Polymer

A new polyanaline sample prepared at Monsanto based upon the IBM Research patent was evaluated in October. The coatings were still grainy but not streaky. NIGHTHAWK membranes were coated and processed to evaluate the image placement results. The results on EL-4 P0 were excellent: two parts had image placement of 30nm, while a third mask had a 40nm IP. Image size 3σ's were 25 to 30nm which is comparable to product without conductive polymer during the same timeframe. Based on the image size and placement results obtained to date, a decision was made to implement the process into manufacturing. To accomplish this, a NOWPAK of polymer was installed on the small Suss tool with a 0.1μm resist filter. The filter plugged as soon as the polymer was introduced to the system.

Several filter types and pore sizes were evaluated in an effort to find a suitable filter for the polymer. Both Teflon and nylon filters with 0.2μm membranes plugged as soon as the polymer was introduced. IBM Yorktown research worked with Monsanto

and prepared a thinner solution of the polymer (2.5% versus 5.0%). Monsanto was able to filter this material to 0.2μm using a nylon filter at 100psi.

Experiments were completed in the MMD with IBM Yorktown research to determine if the pre-filtered, 2.5% polymer could be filtered with the NOWPAK. An assortment of nylon filters was ordered for the evaluations from pore sizes of 0.2 to 4.5μm. The pre-filtered material passed through the 1.2μm filter at 6psi; however, the 0.2μm filter did not provide an adequate flow at 20psi. At 25psi, the pressure burst seal broke. The 0.45μm filter was tested and provided an acceptable flow of the polymer at 10psi.

A new burst seal which will allow the dispenser to run at higher pressures was received in mid-February. The 0.2μm filter will be evaluated at pressures up to 30psi. (The vendor does not recommend using the NOWPAK at pressures greater than 30psi.) Meanwhile, IBM Yorktown is investigating the cause of the filtration issue.

The thinner polymer provides uniform coatings at 2000rpm with a thickness of 900Å. The original material was coated to a thickness of 2000Å. An evaluation is presently underway to determine the effectiveness of the thinner film as a conductive layer and to obtain defect results with the 0.45μm filter.

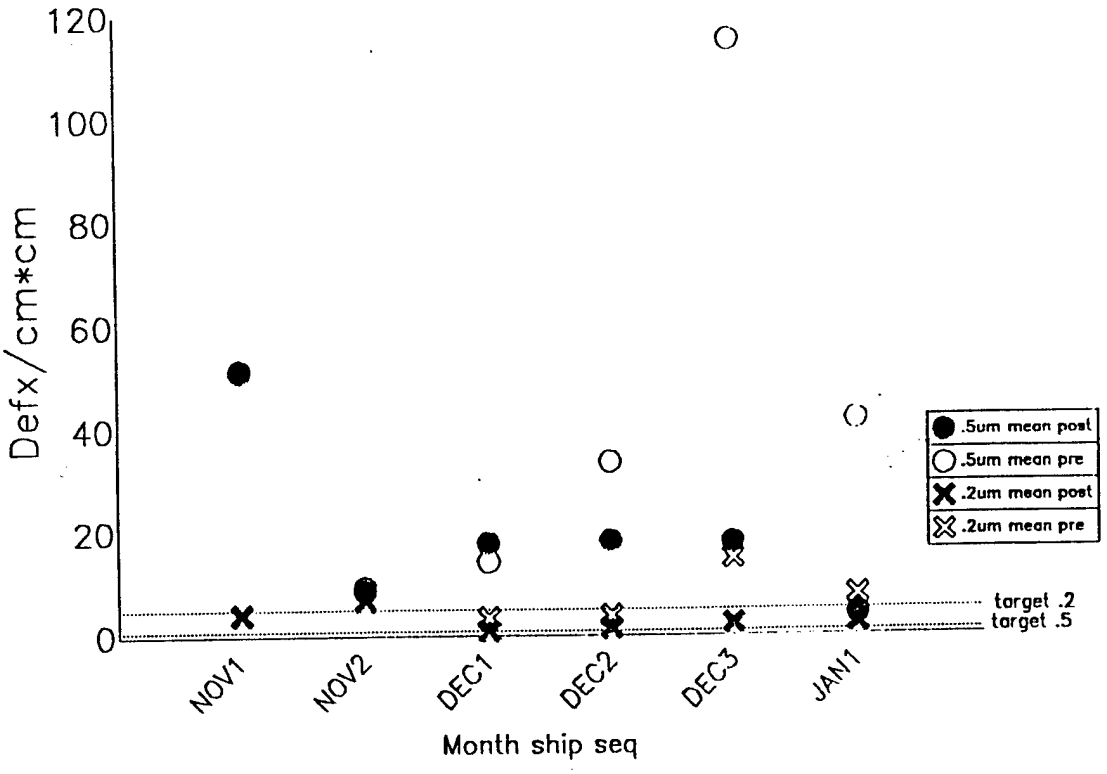


Figure 25. SiC Foreign Material Lot Averages, Pre- and Post-Megasonics

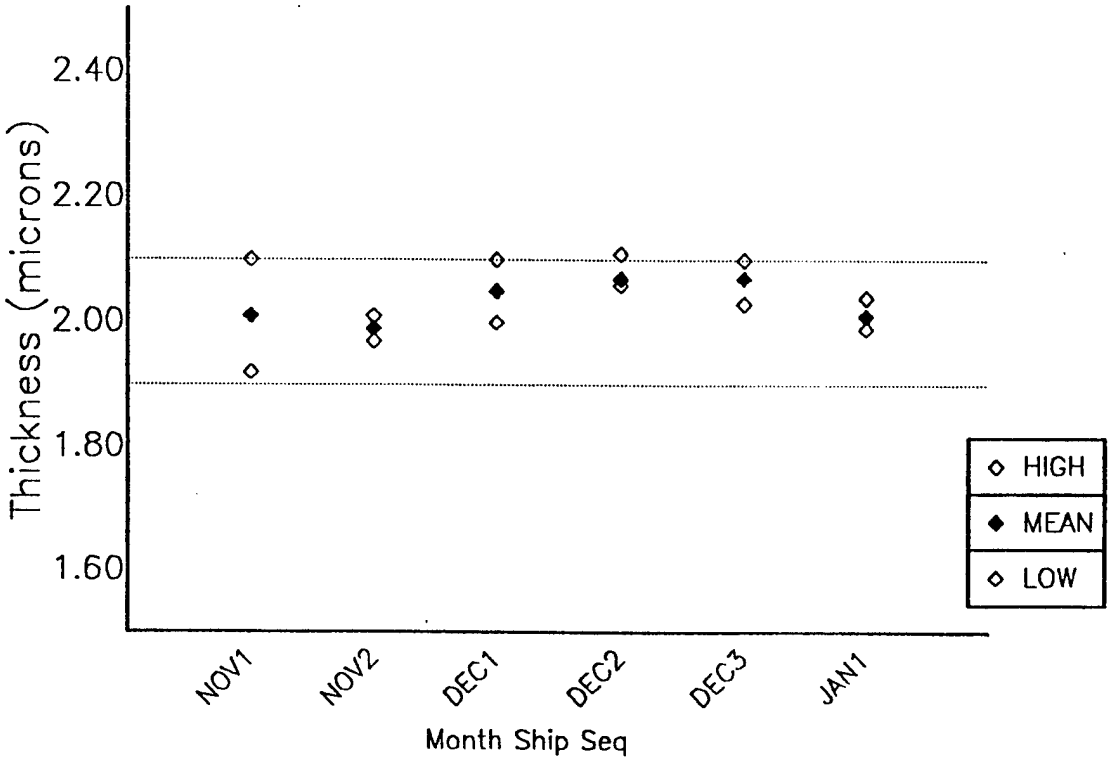
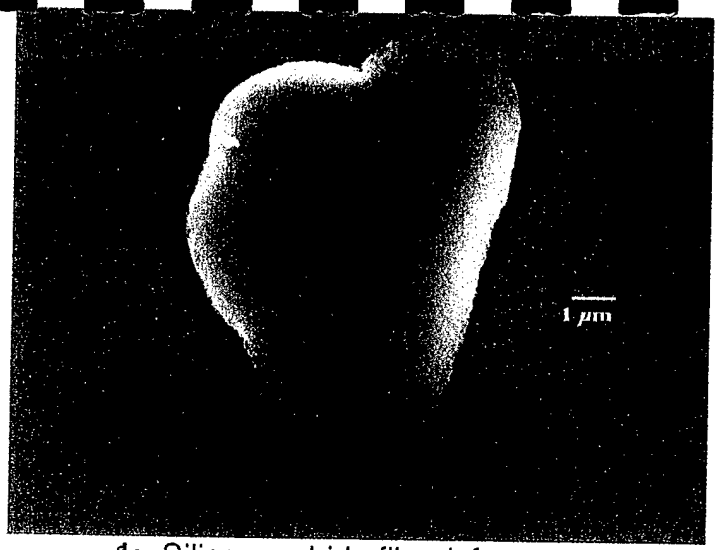
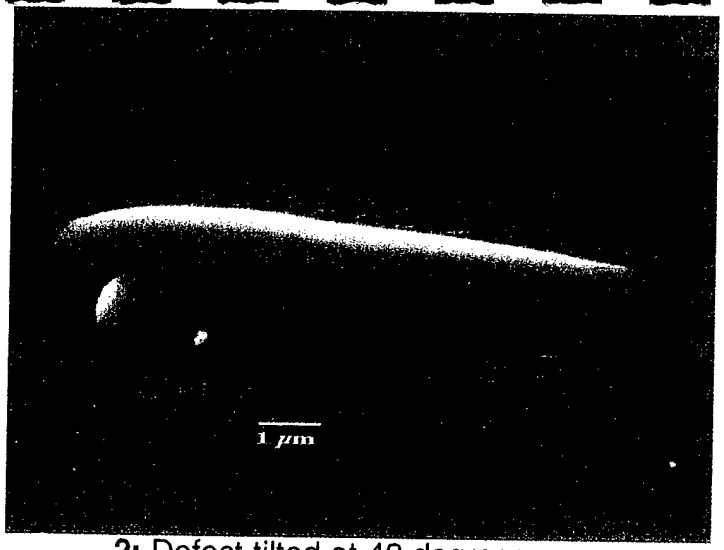


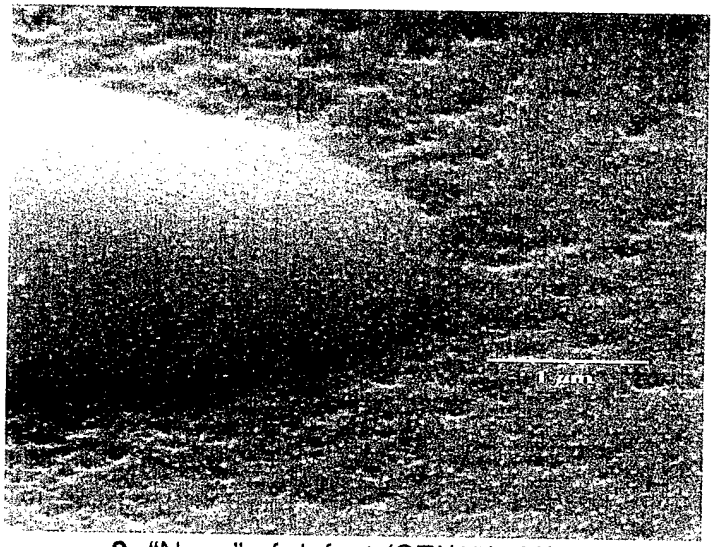
Figure 26. SiC Thickness and Uniformity



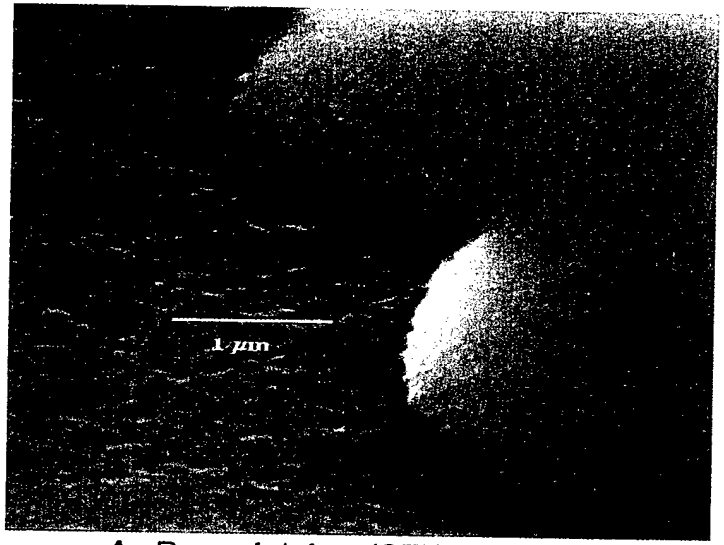
1: Silicon carbide film defect (SEI/15keV/6.5kX). EDX spectra indicated no significant elemental differences between defect and background.



2: Defect tilted at 48 degrees (SEI/15keV/6kX) .



3: "Nose" of defect (SEI/15keV/25kX/48 deg tilt) .



4: Rear of defect (SEI/15keV/25kX/48 deg. tilt) .

Figure 27. Silicon Carbide Film Defect

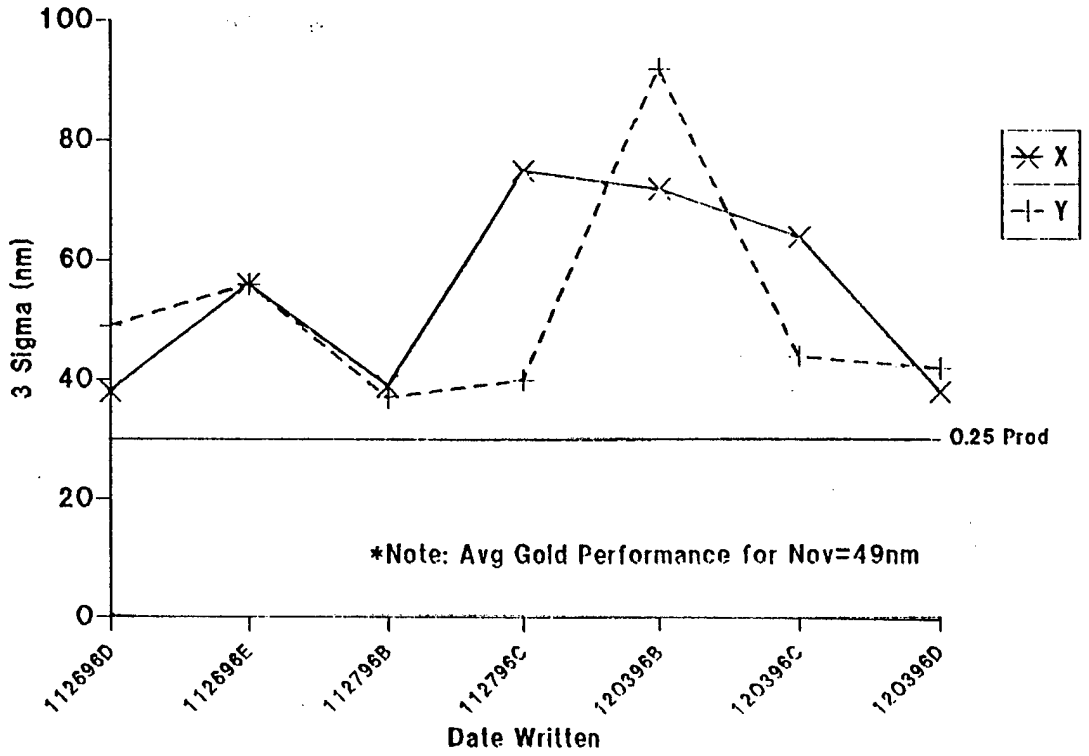


Figure 28. Refractory Mask Image Placement. First results using PSE from two parts. 64Mb SRAM line monitor.

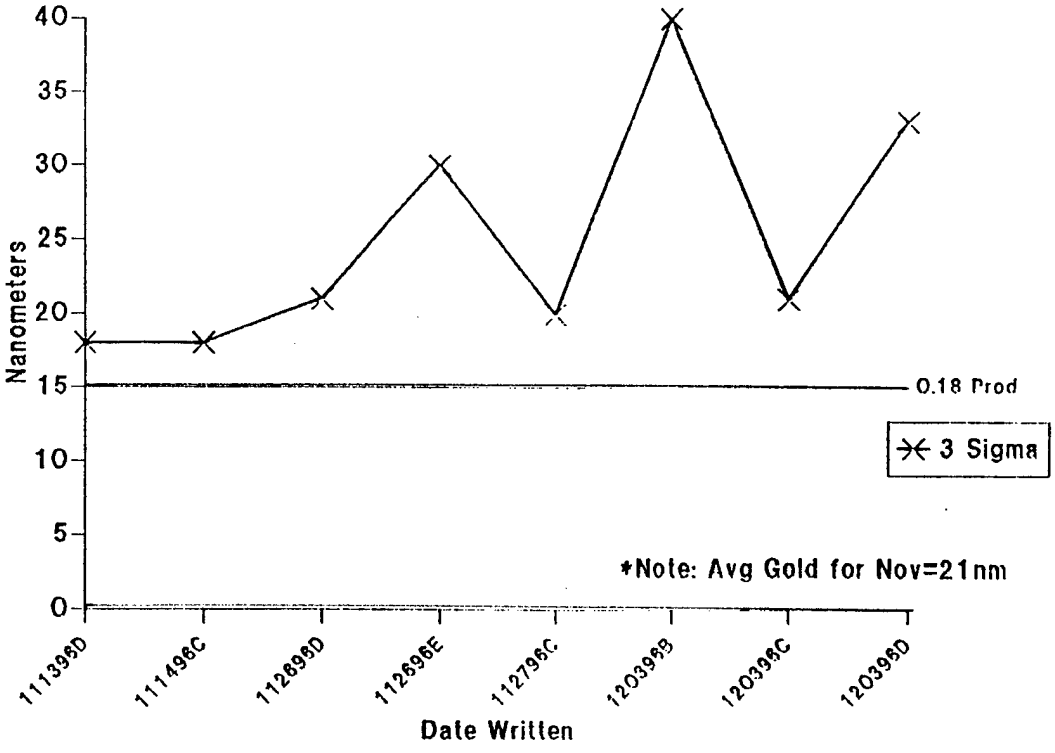


Figure 29. Refractory Mask Image Size. First results.

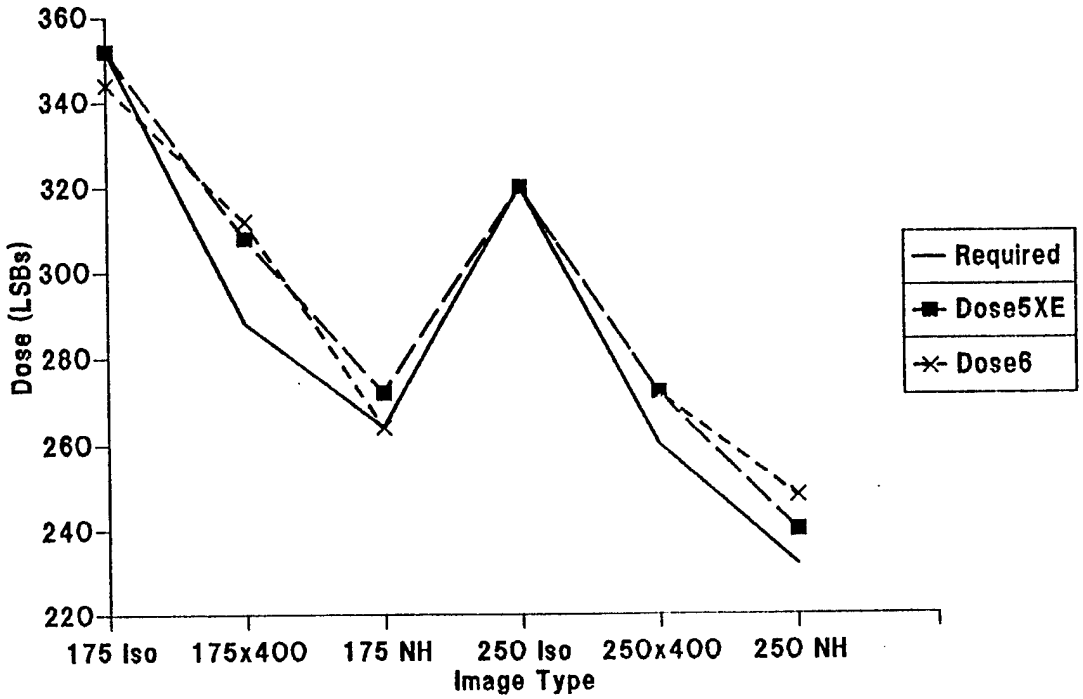


Figure 30. Proximity Algorithm/Alpha Comparison

7.0 Technical Interchange Meetings (Task 10)

Task Objective: Conduct Technical Interchange Meetings (TIM) for industry and the government on a bimonthly basis.

The following Technical Interchange Meetings were held during this period.

- A TIM for 0.13-0.10μm e-beam mask writer was held 19-20 March 1996. The objective of the meeting was to finalize the specification for the 0.13-0.10μm x-ray and optical e-beam writer tool. It was attended by AT&T, IBM, Loral (Lockheed Martin) and Motorola and is documented in CDRL H002, reference 96-MMD-LFSC-00029 dated 02 April 1996.

- A TIM was held on 15-17 April in Japan and was a follow-up to the U.S./Japan X-ray Technology Workshop held in Gotenba, Japan in November, 1995. The emphasis of this TIM was to develop common materials, specifications, and mask formats and parameters to leverage and unify the world-wide x-ray community. A full report was submitted in accordance with CDRL H002, 96-MMD-LFSC-00033).

- A TIM was held on 08 May 1996 at the Lockheed Martin facility in Manassas, Virginia. Attendees included government, industry and academia representatives. All presentation materials were distributed at the meeting. The meeting minutes were published and distributed in accordance with CDRL H002, reference 96-MMD-LMFS-00041.

  This half-day TIM began with a Program Office review of program-specific changes, followed by a review of the program financial structure. The remainder of the review addressed the technical plans and schedules of both the Microlithographic Mask Development facility in Burlington and the Advanced Lithography Facility in East Fishkill. IBM Yorktown advanced mask plans were also presented, as well as e-beam activities.

- The first Executive Review of MMD "Option Year One" was conducted by Lockheed Martin at the IBM Burlington, Vermont facility on 26 June 1996. Attendees included representatives from the government, industry and academia. All presentation materials were distributed at the meeting. The meeting minutes were published and distributed in accordance with CDRL H002, reference 96-MMD-LMFS-00052.

  The feedback session resulted in no action items, but highlighted perceived strengths and weaknesses in the program. Specifically, the feedback indicated that the P0 work was encouraging. Sematech expressed concern about the current 120nm defect inspection sensitivity, which should be at 50nm for groundrules.

  The refractory absorber work to date was good but more pressure needs to be applied in this area; for example, pursuing HOYA or seeking alternatives to HOYA's Ta_4B. Sanders, a Lockheed Martin company, also expressed surprise that

more had not been done on refractory etch in that more support is needed from resist manufacturers in order to get to resists for sub-100nm.

Sematech expressed concern that the protective covers do not act like pellicles and take particles out of printing focal plane. Without this ability, there is no assurance in a day-to-day production environment that the mask remains defect-free. If this is to be implemented, a complete system, including inspection and cleaning, must be developed.

- A Technical Interchange Meeting on "Advanced Mask Cost of Ownership" was held in Chicago on 22-23 August, 1996. The meeting was hosted by Lockheed Martin Federal Systems and IBM. Minutes of the meeting were documented and submitted under CDRL D002, reference 96-MMD-LFSC-00064.

  The objective of this meeting was to establish consensus on the cost methodology and base assumptions that can be used for cost-per-mask calculation projections within the advanced mask technology community.

  A methodology is required to collect data and estimate final mask costs, yields and resources required for non-optical mask technologies. Agreement on the base assumptions and cost formulas are required for accurate comparisons and future business investment decisions.

  Representatives from the advanced mask community were invited to attend a Technology Interchange Meeting held in Chicago on August 22, 1996. This is the second technical exchange on the subject of mask costs. The initial meeting was held in November 1995.

- A Technical Interchange Meeting on "Inspection Technology Requirements and Capabilities of IBM and Orbot Instruments" was held at the IBM facility in Essex Junction, Vermont on 20 August 1996. The meeting was documented and submitted under CDRL H002, reference 96-MMD-LFSC-00066.

  The objective of this meeting was to review current roadmaps and industry requirements for x-ray mask inspection with ORBOT Instruments, Inc.

  Lockheed Martin presented the x-ray program objective, which included the history of x-ray technology, its current program, and technology insertion into future manufacturing.

  IBM presented the chrome-on-glass and phase shift mask requirements which included transmission error detection, inspection area, image size and inspection time.

  The meeting was turned over to ORBOT Industries and company president, Eylan Pick, gave a verbal overview and history of ORBOT. Following this overview Meir Aloni gave the company technical presentation.

- A Technical Interchange Meeting was held in Smuggler's Notch, Vermont on 26-28 September 1996. The meeting is referred to as the Green Mountain Workshop.

The meeting minutes were documented and distributed in accordance with CDRL H002, reference 96-MMD-LFSC-00077.

This meeting was a follow-on to the 05 November 1995 meeting hosted by NTT in Gotenba, Japan. The intent was to continue with the initial topics of standardization of x-ray mask fabrication and potential international collaboration in development of x-ray technology.

- An Executive Review Meeting was held at Lockheed Martin, Manassas, Virginia on 10 December 1996. This TIM was the final Executive Review of the MMD "Option Year One" contract. The minutes of the meeting were submitted in accordance with CDRL H002, reference 96-MMD-LMFS-00092.
- An Advanced Cost of Ownership TIM was held on 22 January, 1997 in Fort Lauderdale, Florida. The objective of this meeting, which was a follow-up to the 22 August 1996 TIM held in Chicago, was to assess the current status of the cost-per-mask calculations being generated by the advanced mask technology community. The minutes of this TIM were submitted in accordance with CDRL H002, reference 97-MMD-LMFS-00022.

Appendix A - IBM Yorktown Research

IBM Yorktown Research Report, 1Q97

E-Beam Post Processing

Introduction

Historically, all post-processing of mask patterns for the e-beam mask writer has been done on large mainframe computers in central data centers. However, this approach has several practical drawbacks, which have become increasingly significant as data sets become larger and more complex:

- Only a fraction of the mainframe's CPU time is available, and the actual elapsed time to process a large data set can be unpredictable, as well as long.
- The amount of data storage is also limited, which has prevented processing of the larger data sets without breaking them up into pieces.
- The recurring costs of processing data in the data center are growing increasingly large.
- The outlook for commercialization of e-beam systems requires that post-processing capability be delivered with the tool, which virtually requires a stand-alone post-processing system.

To deal with these issues, a project was initiated to port the post-processor code from the mainframe to an IBM RISC computer platform with parallel processing. Such a porting would have a number of advantages:

- Post-processing could be done on a dedicated system, eliminating the dependency on and costs of the data center. A dedicated system makes it easy to provide commercialization, and the cost savings are expected to cover the capital cost of the system in a relatively short time.
- The storage capacity can be increased almost arbitrarily by adding storage modules, as required.
- The computational speed can be enhanced by increasing the number of parallel processors, as required.

The new post-processor is known as P5 (**P**ractically **P**erfect **P**arallel **P**ost-**P**rocessor).

It should be noted that the P5 post-processor can be used for the Hontas 6 and P0 variable shaped beam e-beam tools, even though their respective data paths are totally different. However, it is not applicable to vector scan tools such as VS-5, which has a completely separate post-processor.

Project Strategy

The first phase of the project consisted of porting the existing code off of the Main-Frame and onto the IBM RISC platform. There are several programming languages employed by the Post-Processor. Most had counterparts on the RISC. Those that did not had to be rewritten. In addition, the I/O service software and all interfaces to the Sorting Program Product had to be replaced.

After thoroughly testing the 'Serial' version of the RISC based Post-Processor, the Parallel code, which was developed during the port phase, was integrated and tested on the IBM SP computer. There is a total of 250 KLOCs of source code in the entire software system. About 40% of this code had to be modified for the project.

The SP is currently configured with six nodes and has expansion capability to 512.

Remaining work is as follows:

- Final software reconciliation with the Host version
- Define and execute the qualification test with the customer
- Tune the system for optimal performance
- Freeze and release the software to the customer

Port Code to RISC Computer Platform

This phase of the project called for the redesign, where required, and the recompilation of all Source Code for subsequent execution on the IBM RISC Computer Platform.

In some cases, entire programs had to be re-written because of machine language incompatibilities. Interfaces to system services required redesign and software development. Compensation for the differences in the functionality of the available software services was also required.

All work proceeded on schedule. The final test for this work was the serial post-processing of a very small design. The data from the RISC processed design and from the Host processed design were analyzed for area coverage. The agreement in the results constituted completion of this phase of the project.

Processed Standard Patterns Serially

This phase of the project called for the Post-Processing of several current designs in a serial fashion. That is, the Parallel architectural changes were not included so that a less complicated picture of the software system would exist while we were debugging platform changes.

The following designs were processed for this test:

- Plutus
- Polaris
- Nighthawk
- Nighteagle
- Equinox
- F54 P06

Visual and KLA inspections of the designs exposed in resist on wafers were used to compare the Host versus RISC processed patterns.

Processed Standard Patterns in Parallel

Now, the SP computer was configured and the required System Software installed. The Parallel software was then integrated into the Post-Processor Software System and testing continued.

Major redesign was required, necessitated by the incompatibilities between the Sort/Merge system software and the Parallel Operating Environment System Software. In addition, because of file size limitations of the Unix environment, design enhancements were added to break up large files into smaller sizes and process them in a parallel fashion. The same tests were repeated as above.

Qualification, Tune, and Release

We are now in the final stage of the project. The system is being tuned for performance and a qualification plan is being developed. It must be noted that an additional stress test was completed successfully, i.e., the entire Nighthawk 64Mb pattern was posted as one entity using the P5 software. This is not achievable on the Host version of this software.

Schedule and Status

Table 1 indicates that the project is on schedule and that the delivery of 3/31/97 will be met.

Table 1. E-Beam Post-Processing Schedule and Status

Checkpoint	Date	Status
All Code Ported to RISC	*2Q96*	√
Standard Patterns Processed Serially	*3Q96*	√
Standard Patterns Processed in Parallel	*4Q96*	√
Qualification and Release	*1Q97*	

Enhanced Shape Processor (ESP)

Introduction

The data path on P0 began as a high speed, custom ECL based design intended for direct write applications and dependent upon a 4381 mainframe as the tool control computer. The so-called Phase 3 hardware currently installed on the tool in Burlington consists of

- A RISC System 6000 computer for pattern library storage
- SCSI RAID for pattern buffer storage
- Shape Processor for custom pattern processing

The Phase 3 hardware replaced the 4381, 2 Gbytes of silicon pattern buffer and a number of the custom ECL units.

The Enhanced Shape Processor is intended to complete the job of replacing the custom logic boxes in the data path with single cards plugged into a VME backplane. The overall benefit of this task will be:

- Enhanced reliability through reduced component count
- Reduced cost
- Reduced footprint
- Reduced power consumption
- Easy to upgrade through use of FPGA's (Field Programmable Gate Arrays)

By simply replacing the interface cards in the Enhanced Shape Processor, the unit may be used as an upgrade to P0 or incorporated as the data path on EL-5.

Description of the individual ESP cards

- FPGA Shape Divider

  One or more Xilinx FPGA based VME cards which replace the current Shape Divider unit installed on P0.

- FPGA Shape Generator

  One or more Xilinx FPGA based VME cards which replace the current Shape Generator unit installed on P0.

- FPGA SPAT

  One or more Xilinx FPGA based VME cards which replace the current SPAT (Subfield Position And Timing) unit installed on P0. Several functions may be implemented on DSP cards for speed considerations.

- FPGA Digital Feedback

  One or more Xilinx FPGA based VME cards which replace the current Digital Feedback unit installed on P0.

- FPGA Interface Cards

  Two sets of interface cards, and XEP0 upgrade version and a EL-5 version.

- XTC Workstation Card

  A VME card replacement for the existing model 95 IBM PS/2 tool control computer.

XEP0 Characterization and Learning for 0.18μm Ground Rules

Image Placement

Factors with a negative impact on image placement vary with the process. With a slow resist such as PMMA, charging and drift over the duration of the exposure tend to be the dominant error. With comparatively fast resists such as SNR, noise, and settling errors tend to become more important. In both cases, diagnostic tests have been designed and implemented which resulted in the identification system changes leading to improved tool performance. Achievements include:

- BEST 1996 Placement 21,22nm 3σ (X,Y)
- 2 masks @ 25nm 3σ or less (1 req'd in 96)
- 17 masks @ 35nm 3σ or less (nominal 96 spec)
- 63 masks @ 50nm 3σ or less
- Writing masks with SNR/Au, SNR/Ta and PMMA/Au processes.
- Polyanaline conductive topcoat shown to significantly reduce placement errors on PMMA.

Image Quality

A long outstanding problem in the electron beam fabrication of x-ray masks has been the 100 nm process bias required by the PMMA/Au process. This required the e-beam tool to image 80 nm spots to produce 180 nm features. With the introduction of the SNR/Ta process, the bias has been reduced to near zero, with the favorable consequence that the e-beam system is no longer working close to its limits of resolution. Early results with the SNR/Ta process looked encouraging and routine production at 0.18μm ground rules should commence during the 1997 time frame. Achievements include:

- 7 masks @0.18 μm GR CD spec
- 0.10 μm features printed on SNR/Ta masks.
- Beam dump installed to reduce fogging contribution to CD variation.

VS-5 Data Handling Upgrades

Due to the relocation of the MVS systems from Yorktown to Poughkeepsie, the method of moving design data sets from the MVS system to the IBM Series 1 (S/1) control computer for the VS-5 e-beam mask writer would no longer work. A new solution was therefore required. A solution was proposed by ISSC; however, it was deemed to be sufficiently risky that a backup plan was put in place. This backup plan involved using the IBM LAN to move the data sets from MVS POK, to a local PC in Yorktown, and then using a IEEE 4888 interface to move the data from the PC to the S/1. This required software to be written for both the PC and the S/1.

As it turned out, the ISSC approach never worked successfully. However, the work on the backup approach was successfully concluded in October. The new software was installed and tested. Not only did it provide a solution that worked, but it was also found to allow much higher data transfer rates (by approximately a factor of 50) than were available using the original method when the MVS system was located in Yorktown. As a result, VS-5 remains available for writing new high resolution mask patterns.

Origin of Stress Changes in PMMA Resist upon Exposure

Introduction

It was previously demonstrated that some of the errors in image placement are due to the change in stress that PMMA experiences upon exposure. This knowledge led to study the effect of the writing sequence and an improved writing strategy was derived. It is known that the exposure mechanism for PMMA is bond breaking, and it had been speculated that the stress change is due to a lowered molecular weight (MW). In this period we investigated the origin of the stress change.

Results.

It was found that unexposed PMMA films of various MW's in the range 25k to 980k, all have the same stress, within the accuracy of the measurement. This appeared somewhat contradictory, since the stress is very strongly affected by small doses of radiation. Films of 495k MW PMMA were exposed to various doses of radiation. Subsequently the films were dissolved and their molecular weight was determined using gel permeation chromatography. From these results we conclude that it is not the change in average MW that strongly influences the stress of the films, but rather the presence of a (relatively) small fraction of very low MW entities. The presence of the latter probably facilitates the disentanglement and relaxation of the remaining high MW matrix.

Publications.

"Image Placement Errors in X-ray Masks Induced by Changes in Resist Stress During e-Beam Writing". R. E. Acosta and Denise Puisto, J. Vac. Sci. Technol. B14(6) pp 4354-8 (1996).

"Predicting In-Plane Distortion from Electron-Beam Lithography on X-ray Mask Membranes" D. L. Laird, et al. J. Vac. Sci. Technol. B14(6) pp 4308-13(1996).

Magnetron Deposition of Mask Materials

To support the AMF in its transition from gold to refractory absorber, a magnetron deposition system is being set up in Yorktown to deposit materials required in the x-ray lithography mask. These materials include the absorber material, a hard mask, and the etch stop layer. An existing pumping system with a cryopump and a 20″ diameter chamber was used. The MRC magnetron sputtering source was selected because of its size and the uniformity requirements. It is also the same source used at the Motorola Research Center. Also, some of the cathode materials are available in our lab. Due to the precise stress and film thickness and uniformity requirements, a planetary substrate was built. Three 4″ diameter wafers simultaneous rotate both about the center of the system and about the center of each substrate. A load lock chamber has been set up, but not installed on the deposition system yet. Work on sputter deposition has been started while the final details of the system are being completed.

The initial depositions are being done with Cr films. These films can be used both as a hard mask on top of the absorber material and as an etch stop layer under the absorber material. As expected from a substrate holder with planetary motion, the thickness uniformity is excellent. Table 2 shows the thickness deviation from a 397 nm thick Cr film deposited at 12 mTorr using 1.0 kW of dc power. Thicknesses are for 2 orthogonal directions across the wafer. A profilometer was used and a step was chemically etched in the Cr film.

Table 2. Thickness uniformity - deviation in nm from the 397 nm average

Location	First position	Orthogonal position
edge	*- 2.*	*- 7.*
0.5 radius	*13.*	*- 2.*
center	*- 7.*	*- 7.*
0.5 radius	*8.*	*8.*
edge	*3.*	*3.*

These deviations represent an average uniformity of 1.4%. Most of this thickness error is due the profilometer measurement.

The dependence of the Cr film stress on the deposition is being characterized. This work is being done while the construction of the sputtering system is continuing. Table 3 shows the stress in 100 nm thick films for varying sputtering conditions. During these depositions, there was a nitrogen gas leak of the order of a few percent that varied with the argon gas flow. The dc sputtering power was 1.0 kW.

Table 3. Cr film stress and resistivity for different sputtering conditions			
Pressure (mTorr)	Ar flow (sccm)	Resistivity ($\mu\Omega$-cm)	Stress (dynes/ cm^2)
10.	*104.*	*145.*	$4.X10^9$
25.	*98.*	*480.*	$2.X10^9$
50.	*104.*	*890.*	$-1.X10^9$
75.	*178.*	*1422.*	$-1.X10^9$

The film resistivity variation indicates the film purity is varying with deposition conditions. This is consistent with the uncontrolled nitrogen leak and the change in pumping speed with different pressures. However, these results indicate the stress can be tuned through zero.

Refractory Metal Etching

To support the AMF in its transition from gold to refractory absorber, Research Division work started in September 1996 with a focus on (i) exploring etch selectivity of TaX, e.g., Ta_4B, over Cr (mask) and SiC (substrate), for multi-step etching of refractive x-ray mask stacks, and (ii) helping BTV on etch issues related with etch technology (silicon nitride mask opening and TaX etching) transfer from Motorola.

An inductively coupled high density etching system was set up in Yorktown to etch x-ray lithography mask materials. To do this, chlorine etching capability was added to the system. Diagnostics include a differentially pumped mass spectrometer, an optical multichannel analyzer, rf diagnostics, and a full wafer interferometer. These capabilities are used for both monitoring the etching process and end point detection.

Etch selectivity

An initial evaluation of the selectivity of Ta_4B to SiC and Cr was done using an inductively coupled, high density plasma tool in Yorktown (which is similar to the PlasmaTherm etch tool in Burlington). With appropriate process parameters, a good etch selectivity of Ta_4B over Cr or SiC was achieved. The etch results of Ta_4B, SiC and Cr using Cl_2 chemistry are summarized in Figure 1.

The etch selectivity of Cr over Ta_4B without rf power on lower electrode is around 50:1.

With the selectivity we have now, we believe that multi-step etch of Cr/Ta_4B/SiC stacks can be explored further to address the key issue, i.e., balancing RIE bias, profile control and minimizing loss of SiC membrane. However, this work has been discontinued due to the decision to switch from Ta_4B to $TaSiN_x$ absorber.

SiON hard mask etching

I. Summary:

Collaborative work with personnel from Burlington, Motorola, and Yorktown was done in Burlington with the objective of providing any needed help for the transferring of SiON hard mask opening etch process from Motorola to Burlington. Initial attempts to use the standard Motorola Phoenix etch conditions were unsuccessful (poor selectivity to resist, etc.) due to significant tool differences between Burlington and Motorola. A significant effort was therefore needed on the SiON hard mask opening process transfer. An experimental survey of etch selectivity (SiON:$TaSiN_x$resist) was conducted over a range of process conditions. Using this process learning, a new process window was established which matched the process performance in Phoenix (etch bias $\sim$ 1 to 20 nm on selected features). Addition of helium gas was found to potentially improve etch bias ($\sim$ -8 to 3 nm on selected features).

The preliminary data obtained showed promising results, e.g., from the data Burlington measured so far, the CD variation for 0.175/0.25 μm, 0.25/0.25 μm, 0.25/0.5 μm, and 0.5/0.5 μm test features were the same or better than Motorola's results. Once all the measurement results from Burlington are available, a new set of matrices should be run and more test features (e.g., from 0.15 up to 1 μm, on test benchmark mask) should be measured at Burlington to first confirm the process results and then further define process window.

II. Brief Summary of the Results

1. Samples: Samples used for the process transfer were stacks of SiON(200 nm)/TaSiN(~500 nm)/Si(heavily B-doped)/Si (4″ substrate) provided by Motorola. Si(B) membrane, photo resist and test masks were then processed on the stacks by Burlington.

2. Etch tool: The etch tool Burlington has is a Plasma-Therm system VII, capacitively coupled parallel plate plasma source, which has a maximum distance of approximately 2.5″ between two electrode plates.

3. Etch chemistry: The Motorola recipe is: O_2(2sccm)/CHF_3(7sccm)/Ar(20sccm), 350 W rf power (RIE mode, i.e., wafer is mounted on a powered electrode), 20 mTorr, and 4.5″ gap (between two plates). Oxygen is for reducing fluorocarbon, i.e., CF_x film, deposited on sidewall of SiON, which results CD variation, e.g., CD growth. CHF_3 provides all the etchants, such as, F and CF_x. ($x=1,2$) ions or radicals. Ar acts as a diluting gas which helps control the etch rate, while sputtering by Ar ions enhances the formation of etch products, thus enhancing the SiON etch rate. Twenty mTorr is a relatively low pressure for capacitive coupling plasma, but lower pressure, in general, helps to reduce aspect ratio dependent etch (ARDE). Motorola's recipe requires 40% of overetch, which indicates clearly ARDE. The 4.5″ space between plates increases energetic electron travel distance to increase plasma density.

4. Results:

a. A new endpoint detection: After replacing the EG&G OES unit with a unit from the IBM ASTC, the whole optical emission spectra were reviewed and a CN peak at about 387 nm was determined as the endpoint trace because of nitrogen contents in SiON layer. The OES peak at about 486 nm, which was used by Motorola, was not used in this work.

b. Initial results: The original plan was to first use Motorola's recipe to etch samples at different spaces to determine the effect from gap between plates then run a matrix to define the process window. The results obtained from 2″ and 2.5″ (maximum gap for this tool) spaces showed a significant decrease of etch rate for SiON, e.g., from approximately 80 - 100 nm/min (Motorola) to 20 - 30 nm/min. By increasing pressure (increasing density of etchant), SiON etch rates were up to 80 nm/min, but etch selectivity of photo resist over SiON was down to approximately 2-3:1, instead of 1:2

(Motorola). By eliminating oxygen from the recipe, etch selectivity went up to about 1:4.

c. Results: Using a new recipe (based on Motorola's recipe), O_2(1sccm)/CHF_3(7sccm)/Ar(20sccm), a few samples were etched at different pressures, 20 mTorr (etch rate approximately 30 nm/min) and 50 mTorr (etch rate approximately 80 nm/min). Results from SEM and CD variation from auto-SEM indicated that the photo resist masks were almost intact and the CD variation for 0.175/0.25 μm, 0.25/0.25 μm, 0.25/0.5 μm, and 0.5/0.5 μm test features were the same or less compared to Motorola's results (Motorola measured from 0.15 μm to 1 μm).

III. Discussions and Remarks

1. Differences between Burlington and Motorola

The etch results were believed to be different from Motorola for several reasons. First, there were a few things different from Motorola's etch tool: (i) Gap between two plates (2.5″ instead of 4.5″ for Motorola's tool), (ii) chamber volume (75% of Motorola's tool), and (iii) the chamber materials (aluminum instead of stainless steel for Motorola's tool). Among these, the gap, which might affect etchant density, and the inner surface, especially the upper electrode material of the chamber which might affect plasma gas chemistry (even though fluorine, in general, does not etch aluminum or aluminum oxide well), might be important. These effects should be possibly corrected by varying other parameters. The difficulty is to increase etch rate of SiON without reducing etch selectivity of photo resist over SiON or enhancing ARDE. Since CD variation is the number one concern, the low etch rate, 30 nm/min. of SiON may not be a show stopper.

2. Potential improvements

a. The best results in terms of minimum CD variation so far were obtained at a condition of 20 mTorr, O_2(1sccm)/CHF_3(7sccm)/Ar(20sccm) with a approximately 7 sccm He leaked from wafer backside cooling into the chamber. The etch rate of SiON was only about 30 nm/min, which is less than half from Motorola's rate. This result might indicate that further diluting the plasma to reduce CD variation (e.g., CD growth) by controlling fluorocarbon film deposition on sidewall might be worthy of further exploration. Using HeO_2) gas, as is widely used in Si technology, can be one of the choices.

b. Since x-ray masks should address lithography issues for small feature size, e.g., less than 0.1 μm, the aspect ratio will be increased up to 5:1 from currently around 3:1. Aspect ratio dependent etch (ARDE) will be more severe. Besides further increasing overetch time, one method to reduce ARDE is to develop a low pressure (e.g., a few mTorr) and high flow rate etch process. This might be require different etch tool, e.g., an ECR tool.

3. Outlook

Based on this work, it should be possible to transfer Motorola's etch processes to Burlington with a certain amount of effort, despite the differences of etch tools.

TaSiNx etching

Joint efforts with personnel from Burlington and Motorola have begun to transfer the Phoenix etch process to Burlington. The primary effort is currently focused on obtaining minimal etch bias (primarily through the addition of a small amount of O_2, which increases line width, to the ECR Cl plasma) in the absorber etch. The Phoenix process is also being modified as a result of a recent change in the $TaSiN_x$ formulation (less nitrogen). In addition, the role of the resist in controlling line width is also being examined.

Evaluation of NTT Stress Measurement Tool

Description

An absorber with uniform stress or with small stress variations across the membrane is necessary to meet the image placement requirements of x-ray masks. Sputter deposition of refractory metals with uniform stress is a major technical challenge, particularly when the deposition is carried out on membranes. Even when the deposition is carried on wafers, obtaining uniform stress has required a major development effort. This effort has been hampered by the difficulty in reliably measuring stress uniformity on thick (500 - 600 μm) substrates.

NTT-AT has a stress measurement apparatus which is believed to be available for purchase. NTT-AT claims that the apparatus is capable of measuring local film stresses, with a good spatial resolution, when the films are deposited on substrates with a thickness on the order of 600 μm. The technique used relies on measuring the deflection (bow) of the substrate wafer, with and without the film of interest, using a laser reflection method. Local mapping of the bow is achieved by x-y movement of the substrate using an accurate stage. The stress is calculated from the local bow using Stoney's equation. The claimed accuracy and sensitivity of the apparatus is on the order of a 0.2 to 0.3 x 10^7 dyne/cm^2

Given the stiffness of a 600 μm silicon wafer, the low magnitude of the film stresses of interest, and the technique used to determine stress, it is justified to question the ability of the apparatus to meet the claims. On the other hand, if the apparatus were to meet the claims, it would constitute a very valuable development tool for characterization of absorber stacks. The problem so far had been to devise a methodology for testing the apparatus, i.e., for providing samples with well-defined areas of known varying stress.

Four samples, prepared as described below, were sent to NTT-AT. The small number of samples was dictated by the high cost per sample charged to perform the measurements; promising results would justify a thorough evaluation using more samples.

Test Methodology

The four samples submitted, on 2-side polished Si wafers, approximately 500 μm thick, consisted of two PMMA and two gold films.

The PMMA films were spun from "standard" PMMA solution (490k mol. wt. in diglyme), spun and baked at 170 °C. The thickness of these films was 700 nm, and the nominal (unexposed) stress was 1 x 10^8 dyne/cm^2. Based on work done last year, areas of different stress values were produced in these films by exposing selected areas to different doses of UV radiation from a mercury lamp. Both large and small areas of reduced stress were created to test the spatial resolution of the tool.

The gold films were obtained using the POR electrodeposited gold. In this case the different "effective stress" areas were achieved by producing areas of different thickness. Because the NTT apparatus uses Stoney's equation to calculate stress, areas of different thickness will appear as areas of different stress when the calculation assumes a film with uniform thickness. Both large and small areas of thicker gold were created to test spatial resolution.

Specifically, the four samples were:

- 1a) A 4" silicon wafer coated with PMMA as described above. Large areas with stress of of 0.5, 0.2, and 0.1 times the nominal (shown as the vertical rectangles in the upper part of the wafer in Figure 2) were created through exposure. Smaller areas (1x1 to 3x3 mm^2) of the same reduced stress values were similarly created in the areas shown in Figure 2 as horizontal rectangles in the lower part of the wafer; these areas had the pattern shown in the inset of the Figure.
- 1b) Identical to Sample #1a.
- 2) A 4" silicon wafer coated with 330 nm of gold (having a stress of 1 x 10^8 dyne/cm^2), except in the patterned areas shown in Figure 3, where the gold thickness was 1030 nm (for a stress of approximately 3 x 10^8 dyne/cm^2).
- 3) Identical to Sample #2, except that the thicker gold was only 730 nm thick (for a stress of approximately 2 x 10^8 dyne/cm^2), as shown in Figure 4.

Note that Figure 2 through Figure 4 show the patterns as seen from the backside of the wafer, which is how the NTT apparatus looks at the wafer.

Results

Figure 5, Figure 6, Figure 7, and Figure 8 are the stress maps produced by NTT, corresponding to the wafers of the numbers.

If one disregards the *absolute* value of the stress, comparison of Figure 2 and Figure 5 indicates that Figure 5 appears to give a fairly good indication of the stress distribution of the PMMA film, but *only* within the square areas indicated. Outside of these square areas the stress distribution given in Figure 5 appears to bear *no correlation at all* to the stress of the film supplied. Notice also that the spatial resolution is poor: the large areas of different stress were bound by fairly sharp, straight, edges, but they appear fairly diffuse in the stress map. Furthermore, the small patterned squares do not show up in the plot, not even the larger ones which measure 3x3 mm.

Comparison of Figure 2 with Figure 6, Figure 3 with Figure 7, and Figure 4 with Figure 8 shows that the stress maps produced by the NTT apparatus bear no relationship to the stress distribution in the samples submitted for measurement, even when one disregards the absolute value of the stress in question.

In the case of Figure 8, there *may* be some resemblance to the stress distribution indicated in Figure 4 if one assumes that the patterned area and the measurement area are displaced relative to each other in the vertical direction. Even with this allowance, one is hard put to justify the small area of high stress that appears in the NTT map at the 8 o'clock position. Furthermore, notice that the stress values indicated for Figure 7 and Figure 8 relative to each other are the reverse of the relative stress values of the samples submitted; this gives one reason to suspect that the apparent resemblance may just be a fluke.

In summary, from the small number of samples measured it appears safe to conclude that the NTT apparatus *does not* have the stress mapping capability claimed. Further expense and effort in evaluating this apparatus is not considered justifiable.

Radiation Hardness of SiC and Refractory Absorbers

Description

The radiation hardness of future mask absorber materials (Ta_4B, $TaSiN_x$) is being tested. Irradiation is conducted using the DEL beamline at ALF. This beamline has a spectrum harder than that of the lithography lines, but it allows continuous unattended irradiation of the samples in a parasitic manner. The absorber material in the form of a blanket film deposited on top of a SiC membrane is irradiated by an x-ray beam in the shape of a slit. Changes in the stress or mechanical properties of the absorber film, exaggerated by the uneven exposure, should result in membrane distortion. The latter is checked periodically using a metrology tool (Nikon 3i, Leica).

Results

Various Ta_4B samples have been irradiated to between 170 kJ/cm^2 and 450 kJ/cm^2 without evidence of distortion. The underlaying SiC material had previously been tested to be radiation hard to a dose of 420 kJ/cm^2. Evaluation of $TaSiN_x$ samples is planned pending availability.

Advanced X-ray Mask Fabrication below 130 nm Using VS-5

SNR negative resist process development for refractory absorber

In early 1996, an attempt was made to implement an SNR resist process on the VS-5 100 kV gaussian beam electron beam mask writer in Yorktown, using process parameters provided by Motorola. However, the use of oven baking for post-apply bake (PAB) and post-expose bake (PEB) did not yield good results. Subsequently a hot plate was used for PAB and PEB. The primary focus was to find optimized bake conditions to resolve equal line/space patterns. Equal line and space patterns were achieved for patterns down to 150 nm. However micro-bridging problems were encountered at dimensions below 150 nm. An array of SEM micrographs are shown in Figure 9 illustrating the characteristics of the resist. A graph showing the linewidth dependency on dose is illustrated in Figure 10.

Based on these results, it appears that a better resist system and process may be required to extend the patterning resolution below 150 nm. We are now in the process of evaluating alternative resist systems.

Sub-130 nm mask fabrication

Several x-ray masks with minimum features below 130 nm have been fabricated. VS-5 was primarily used to pattern high resolution features, while the XEP0 e-beam writer in the AMF was used to pattern large features on these masks. A diagram illustrating the process flow for these masks is illustrated in Figure 11. Briefly the patterning process consists of exposing high resolution patterns at 100 kV beam energy using a beam size of 300 Å. PMMA resist with a resist thickness of 4700 Å was used with a base dose of 600 $\mu C/cm^2$. Appropriate proximity correction (forward and back scattered correction and bias) was applied for these patterns. The patterned masks were electroplated with gold in the VS-5 process lab in Yorktown. Some of the finished masks were characterized at AMF, which is responsible for providing the characterization packages. The characterization and qualification includes CD measurements, accuracy measurements, mask inspection, and mask repair. A SEM micrograph of a high resolution gold absorber pattern is shown in Figure 12.

Included among the masks fabricated on VS-5 were:

- 3 gate level masks with 75 nm minimum feature size for IBM advanced logic development
- 2 gate level masks with nominal 125 nm minimum feature size (but also including some features at 100 and 75 nm) for high frequency RF circuits and devices (for a project under a Navy contract)
- 3 masks with lithography characterization patterns for the University of Wisconsin

Optimization of vertical memory x-ray mask fabrication

We have begun work on a mask for a new, vertical memory structure under development in IBM. The mask consists of large arrays of pillars in the mask absorber ranging in size from 50 nm to several microns and in pitch from 150 nm to several microns. There are several tens of millions of shapes, which were possible to process only through the use of a matrix command in the digital pattern generator of VS-5. Otherwise the pattern data file size would exceed available disk storage.

We have optimized the exposure dose of the PMMA resist at 100 kV to ensure complete development of the fine holes in the thick resist. We compared two developers: IPA(70%):H_2O(30%) for 60 seconds and 1:2 MIBK:IPA for 90 seconds. At present the minimum hole size developed in 420 nm thick PMMA is 75 nm in diameter. It is limited by electron scattering in the resist, which makes it difficult to develop the holes straight through the resist to the plating base (which is essential for the subsequent gold absorber plating). To compensate for the forward scattering effects in the resist, we found that the small holes need to be exposed with a 12 times higher dose than the large area dose on the silicon membrane. With less exposure dose the holes do not develop all the way to the bottom and consequently no gold is plated.

The resist descum etch after development, and before the gold absorber plating, has been changed to minimize the possibility of membrane breakage after striking the He plasma. It appears that some membranes were broken in the reactive ion etching system as the result of electrical discharge between the powered electrode and the membrane. To minimize the possibility of electrical discharge, a quartz plate has been introduced in the space between the powered aluminum electrode and the membrane with very good results: no membranes have been broken since. Also, to ensure better effectiveness of the descum etch, the gas mixture was changed from 100% He to 90% He/10% O_2 with no significant increase in the resist etch rate. The resist thickness loss during the descum etch was approximately 20 nm. Figure 13 shows 75 nm diameter pillars plated 350 nm thick.

Lithography test mask (LTM-4) fabrication

During 2Q and 3Q 1996, second generation high resolution test patterns were laid out for a lithography test mask (LTM-4) using GL/1 CAD system. These patterns included isolated lines, nested lines with a 1:1 through 1:3 line:space ratio, contact holes and islands at 75 to 250 nm feature sizes. Sections of SRAM and DRAM device layouts were scaled to ground rules of 75 nm to 400 nm and included in the LTM-4 data. Additionally, electrical linewidth measurement structures with linewidths ranging from 75 to 1000 nm were prepared. The patterns were then post-processed and proximity corrected at Yorktown.

For the x-ray mask fabrication, the AMF prepared 2.2 μm thickness boron-doped silicon membranes with gold plating base and 470 nm of PMMA resist. The AMF also exposed alignment marks and a border frame with SVGL x-ray aligner mask interme-

diate alignment marks. These patterns were plated to 100 nm thickness. Two LTM-4 mask patterns (Revision 0 and Revision 1) have been fabricated successfully using VS-5 to expose the high resolution LTM-4 patterns. The Revision 0 pattern was a subset of the full mask pattern written at a dose of 580 through 630 $\mu C/cm^2$ in increments of 10 $\mu C/cm^2$. Limited top-down SEM metrology at ALF of these patterns revealed a 0.5 - 0.7 nm/$\mu C/cm^2$ change in linewidth as a function of dose for 125 nm features. The Revision 0 SEM data was used to determine the dose for Revision 1 pattern, which was written on one mask. The final resist strip and limited top-down SEM metrology was then performed at AMF on the Revision 1 mask. Measurements of the same 75 to 250 nm features on ALF SEM indicated that the ALF SEM linewidth measurements were consistently $\simeq$ 10 nm smaller than the AMF data, and the AMF measurements suffered from a $\simeq$10 nm horizontal versus vertical bias. Additionally, using another test sample, top-down SEM metrology at ALF was compared to linewidth measurements made from tilted SEM micrographs obtained at MIT with Prof. Henry Smith's Carl Zeiss Gemini SEM. The linewidths measured by the ALF SEM were $\simeq$ 15nm larger than the tilted SEM measurements. Tilted SEM measurements of 75 and 100 nm isolated and nested lines are shown in Figure 14 through Figure 17. Top-down SEM photographs of 75 and 100 nm ground rule SRAM like gate structures taken at ALF are shown in Figure 18 and Figure 19.

A third version (Revision 2) mask is now being prepared for writing in the next few weeks. The Revision 2 data includes isolated and nested lines exposed at several doses to study linewidth print biasing, and it includes SRAM and DRAM device patterns without proximity correction not only to correct errors in the proximity correction but also to study mask biasing in the absence of proximity correction.

Mask Distortion Studies

In a general manner pattern placement errors in X-ray masks arise from two sources: e-beam writing and membrane distortion. The former errors are the result of having to write the pattern in a blind or semi-blind mode. Membrane distortion arises from the interplay of membrane and absorber characteristics. Presently masks are written in a semi-blind mode: because reference marks are not allowed in the patterned area of the mask, they must be located far from the area to be written, which precludes frequent correction of the e-beam writer position and requires a long travel (with correspondingly increased positional uncertainties) when they are measured. The membrane distortion is to a first order directly proportional to membrane size. Because future chips will be even larger than present ones, both the e-beam writing problem and the membrane distortion will be aggravated.

A new mask structure concept that potentially eliminates the need for PSE and improves placement accuracy is being studied. The concept here relies on using narrow "printing slits" to significantly reduce or eliminate problems associated with large area masks. The printing membrane slits are alternated with support struts of the same width. Printing of the wafer would use the interleaved exposure method, in a manner similar to that used for image formation in television. Accurate stitching of the pattern is required, which in turn requires good alignment of two exposures in a stepper.

In this proposed structure advantage can be taken of the support areas to provide position reference marks for each window. These marks can be used to allow continual reckoning and correction of position of the e-beam writer. Since the windows are relatively small, these marks can be placed within a relatively short distance of any part of the pattern, allowing for frequent corrections with short travel, which should also improve the accuracy of the corrections.

Because the distortion of narrow windows is dominated by the smallest dimension, this new structure is also expected to show in-plane distortion (IPD) on the order of one order of magnitude smaller than that observed in present day masks (e.g. the IPD of a 3 x 30 mm window is, to a first approximation, 1/10 the IPD of a 30 x 30 mm window).

These two factors may eliminate the need for Product Specific Emulation (PSE). The small windows give wider tolerance in the magnitude and uniformity of the allowed stress of the absorber. They may also allow patterning of the absorber on a wafer, with membrane formation as one of the last steps in mask fabrication.

Work has been initiated to assess the performance improvements of such a mask structure and to demonstrate its feasibility. The following studies are under way:

- Experimental determination of the reduction in IPD when going from chip dimension (L1 x L2) membrane masks to narrow windows (l x L2) where l/L1 $\simeq$ 1/10 using thin (625 μm) wafers.
- Several schemes for fabrication of a mask structure with narrow windows interleaved with a sturdy support structure, e.g. separate fabrication of the strut structure and membrane carrier to be subsequently bonded.
- Schemes for formation of an accurate grid of reference markers on the support members separating the various narrow windows.
- Feasibility of stitching the patterns in the various narrow windows with small errors: schemes of pattern splicing to minimize stitching errors, and issues related to framing of the spliced pattern to prevent formation of ghost images.

At present, these activities are in an early stage; results are expected later this year.

Investigation of Non-Chemically Amplified Resist

As indicated in previous reports, we have begun evaluation of a series of non-chemically amplified resists, referred to as Spar, under development in IBM. These materials are potentially well suited for use in x-ray mask patterning and wafer patterning since there are no post-exposure bake requirements. We have tested these materials by both x-ray exposure and e-beam exposure (see earlier reports) and found lithographic activity comparable to chemically amplified materials. However, these materials did not have sufficient etch resistance for some applications. Therefore the matrix to determine process latitude on this material was deferred.

More recently, variations of the Spar material chemistry have become available that promise better etch resistance. For example, several other derivatives have been tested for etch resistance using an aggressive Cl etch process at MIT-Lincoln labs. This is the same etch process that is used for testing of IBM's 193nm resists. A comparison of relative etch rates for various resist systems is shown in Table 4, using a novolak resist as the standard (etch rate = 1 by definition). Note that a lower number for etch rate indicates better etch resistance.

Table 4. Relative Etch Rates

Resist	Relative etch rate
Novolak 1.0	
IBM 193nm resist V1 (non-etch resistant)	*2.4*
IBM 193nm resist V2 (etch resistant)	*1.6*
Apex (DUV resist)	*1.35*
Spar-XP1196	*1.5*
Spar-XP1196b	*1.45*
Spar-XP696	*1.45*

As can be seen, the relative etch rate of the newer versions of Spar are more in line with conventional DUV and experimental 193 nm resists, and we believe that the demonstrated etch resistance is adequate for device application and x-ray mask fabrication. It remained to be seen if similar chemistry would also have good lithographic sensitivity.

Preliminary lithographic evaluations conducted with a DUV source suggest that newer versions of this material do indeed have good sensitivity and contrast. SparXP-1296 has demonstrated 2X improvement and SparXP-197 shows a 10X improvement in sensitivity over the versions of Spar reported on earlier. It should be noted that those versions of Spar had x-ray sensitivities in the 100 mJ/cm^2 range. If the improvement in speed mentioned here translates in x-ray exposures, these materials would meet the 50 mJ/cm^2 sensitivity requirements for wafer printing. In addition, they are

expected to be etch resistant due to the results of similar chemistries as described above. Etch resistance verification tests are in progress, and x-ray exposure characterization is planned.

Figures

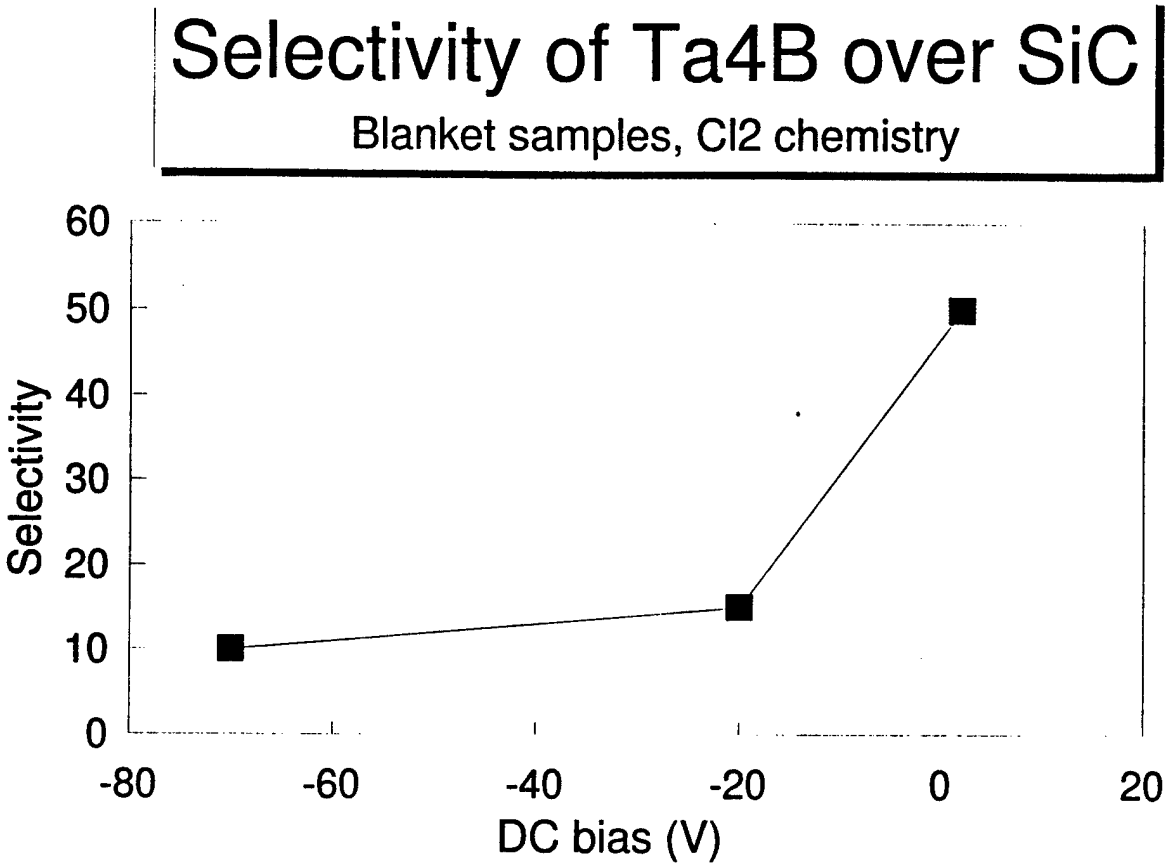


Figure 1. Etch Selectivity

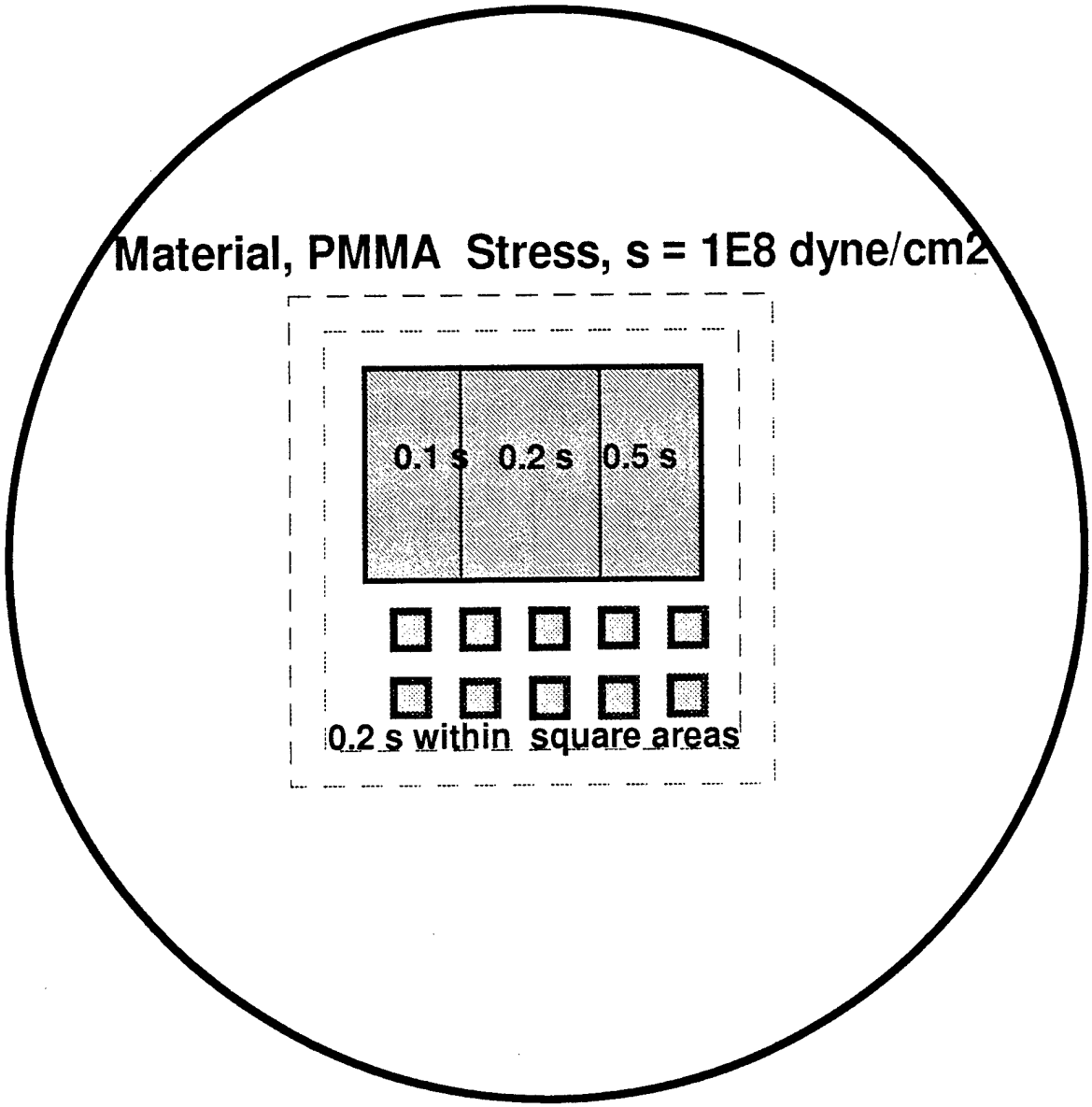


Figure 2. Layout of Wafer Type 1 Used in Evaluation of NTT Stress Measurement Tool

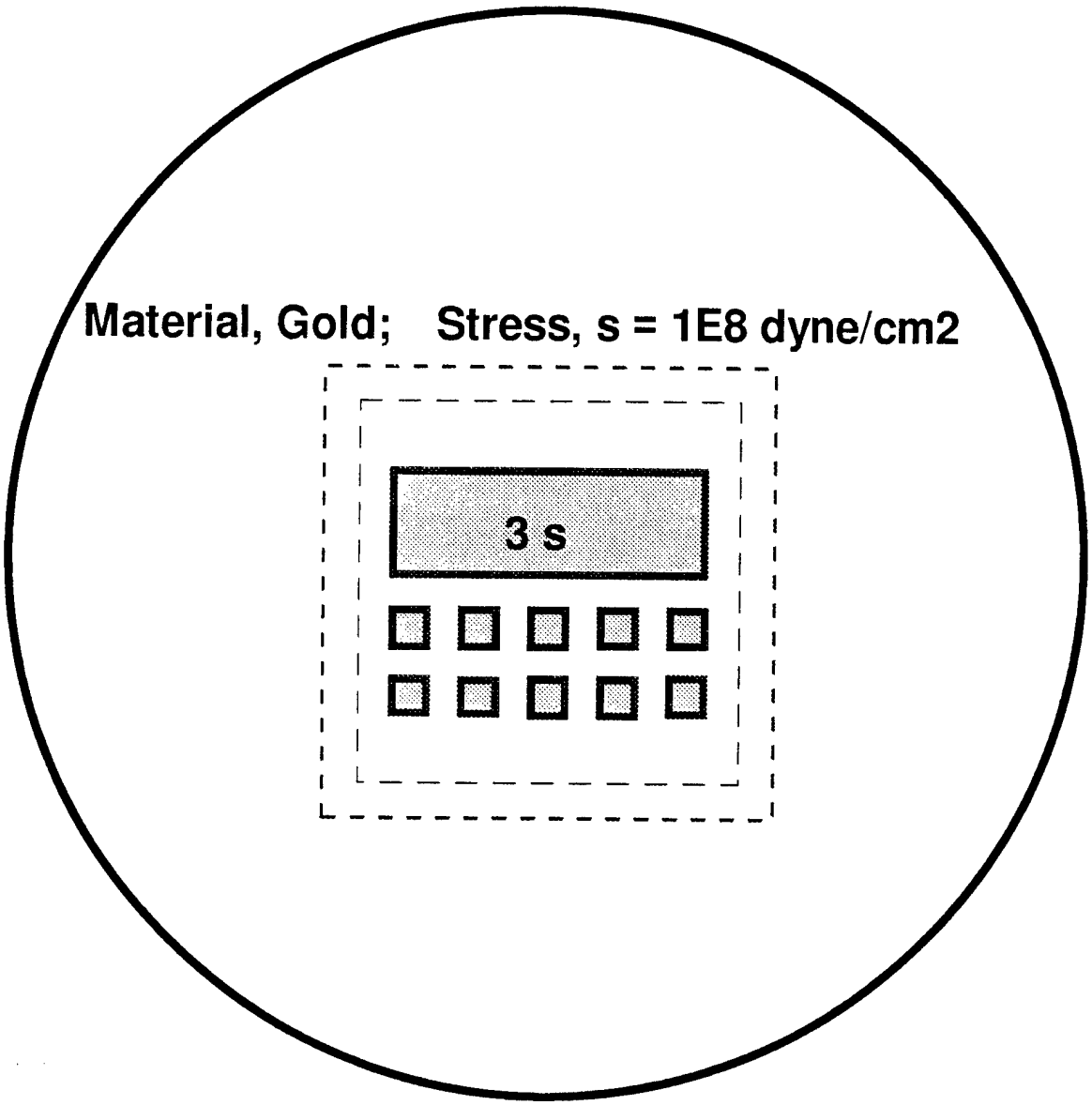


Figure 3. Layout of Wafer Type 2 Used in Evaluation of NTT Stress Measurement Tool

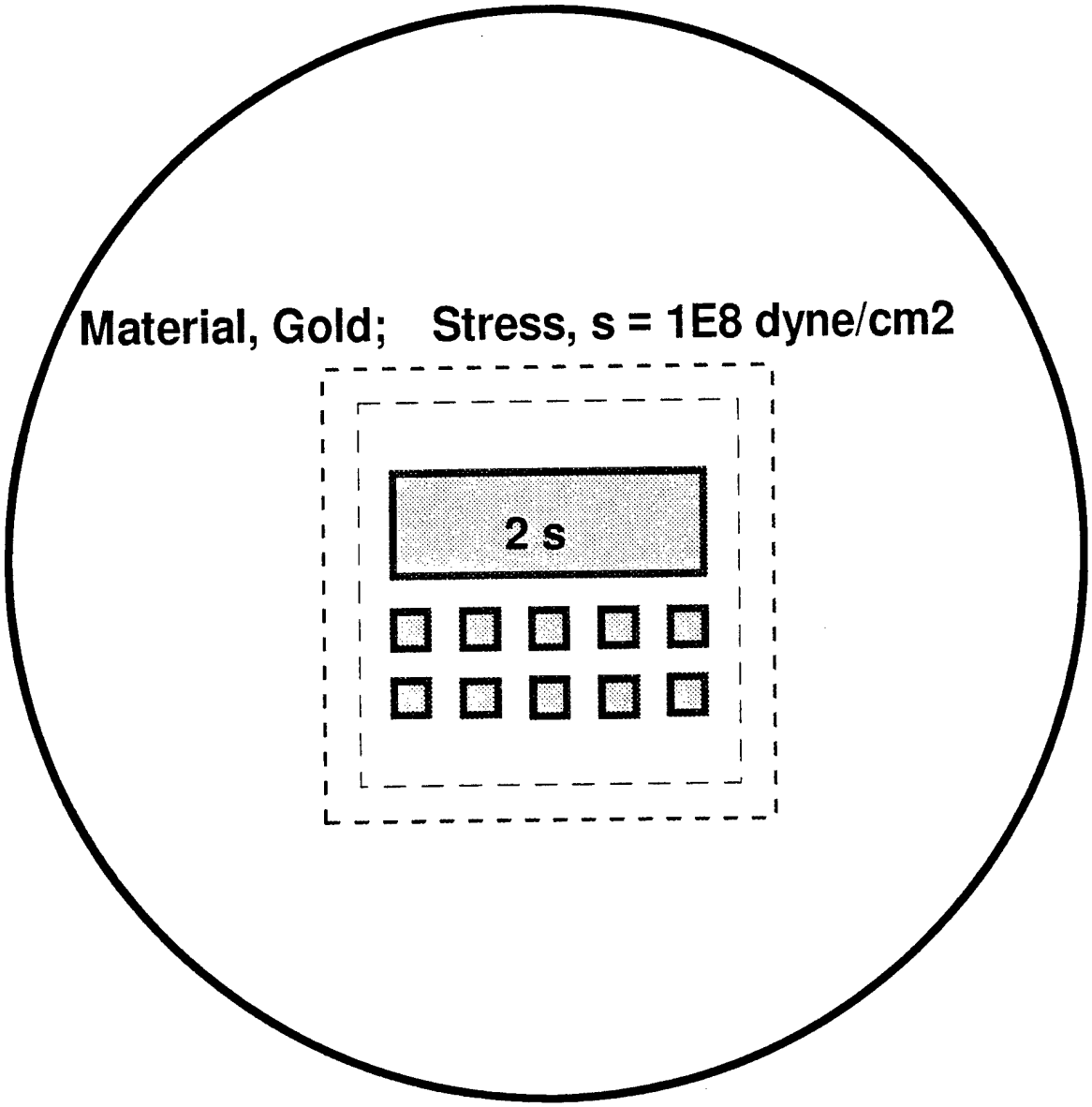


Figure 4. Layout of Wafer Type 3 Used in Evaluation of NTT Stress Measurement Tool

1AIBM Stress (dyn/cm2)

Mean Stress (75mmø) 9.990E+07
Max. 2.124E+08(112.6%)
Min. 7.228E+05(99.3%)

Mean Stress (30mm□) 9.488E+07
Max. 1.671E+08(76.2%)
Min. 5.910E+07(37.7%)

Mean Stress (25mm□) 8.986E+07
Max. 1.461E+08(62.6%)
Min. 5.910E+07(34.7%)

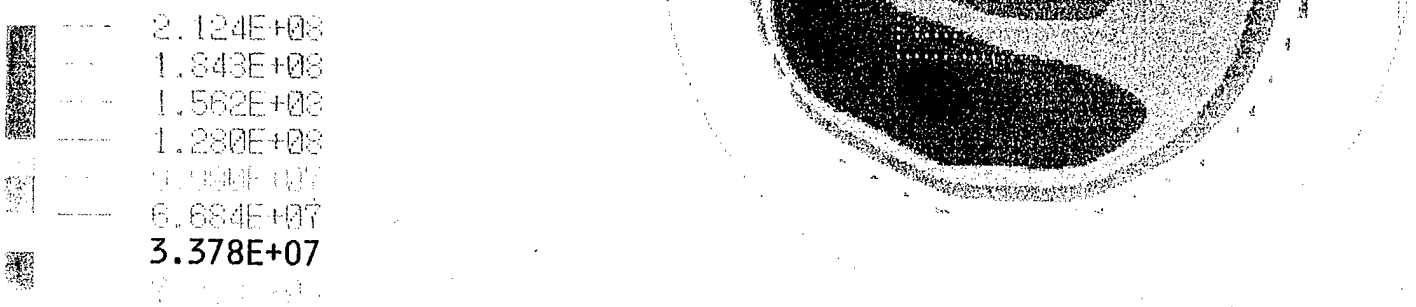


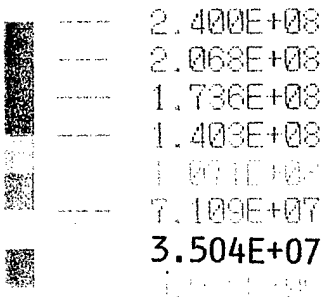
Figure 5. Stress Map of Wafer 1a as Reported by NTT Stress Measurement Tool

2AIBM Stress (dyn/cm2)

Mean Stress (75mmø) 1.071E+08
Max. 2.400E+08(124.0%)
Min. -9.986E+05(100.9%)

Mean Stress (30mm□) 1.358E+08
Max. 2.236E+08(64.7%)
Min. 5.714E+07(57.9%)

Mean Stress (25mm□) 1.377E+08
Max. 2.153E+08(56.3%)
Min. 6.427E+07(53.3%)



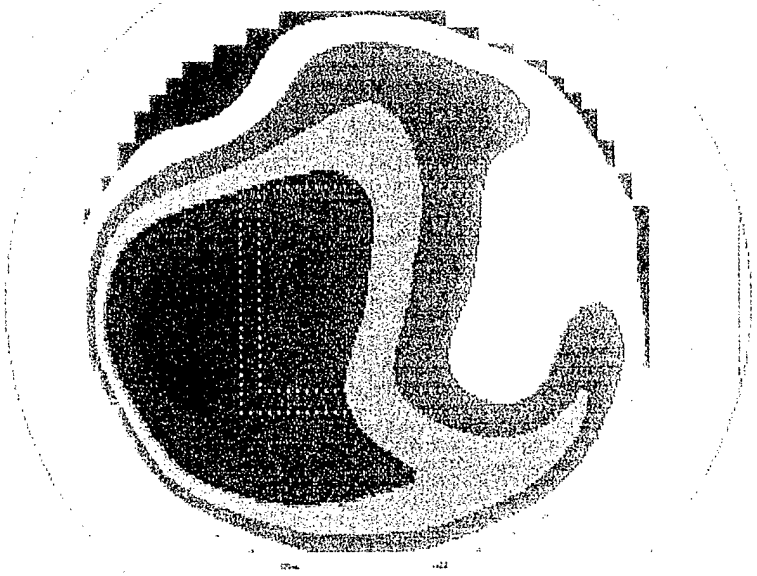


Figure 6. Stress Map of Wafer 1b as Reported by NTT Stress Measurement Tool

3AIBM Stress (dyn/cm2)

Mean Stress (75mmø)		1.098E+08
Max.	1.685E+08(	53.5%)
Min.	1.381E+07(	87.4%)
Mean Stress (30mm□)		1.547E+08
Max.	1.685E+08(	8.9%)
Min.	1.132E+08(	26.8%)
Mean Stress (25mm□)		1.547E+08
Max.	1.685E+08(	7.1%)
Min.	1.273E+08(	19.1%)

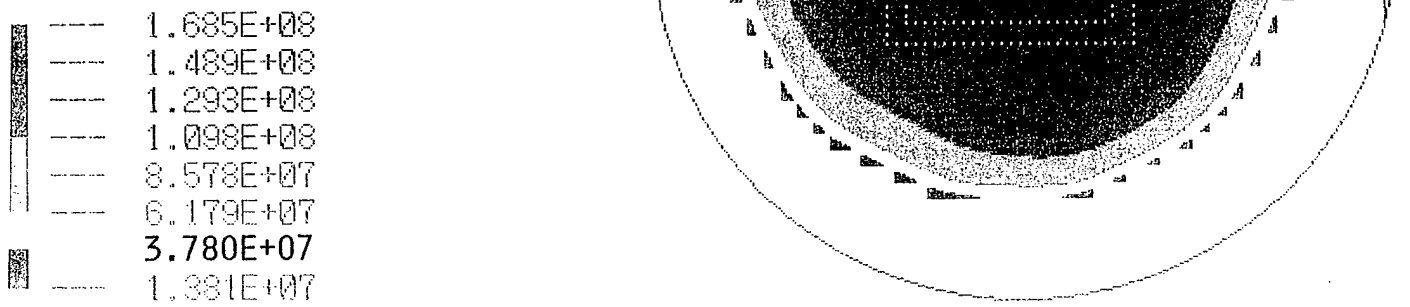


Figure 7. Stress Map of Wafer 2 as Reported by NTT Stress Measurement Tool

4AIBM Stress (dyn/cm2)

Mean Stress (75mmø) 2.042E+08
Max. 4.459E+08(118.4%)
Min. -1.126E+08(155.1%)

Mean Stress (30mm□) 2.179E+08
Max. 4.459E+08(104.6%)
Min. 1.016E+08(53.4%)

Mean Stress (25mm□) 2.000E+08
Max. 4.437E+08(121.9%)
Min. 1.016E+08(49.2%)

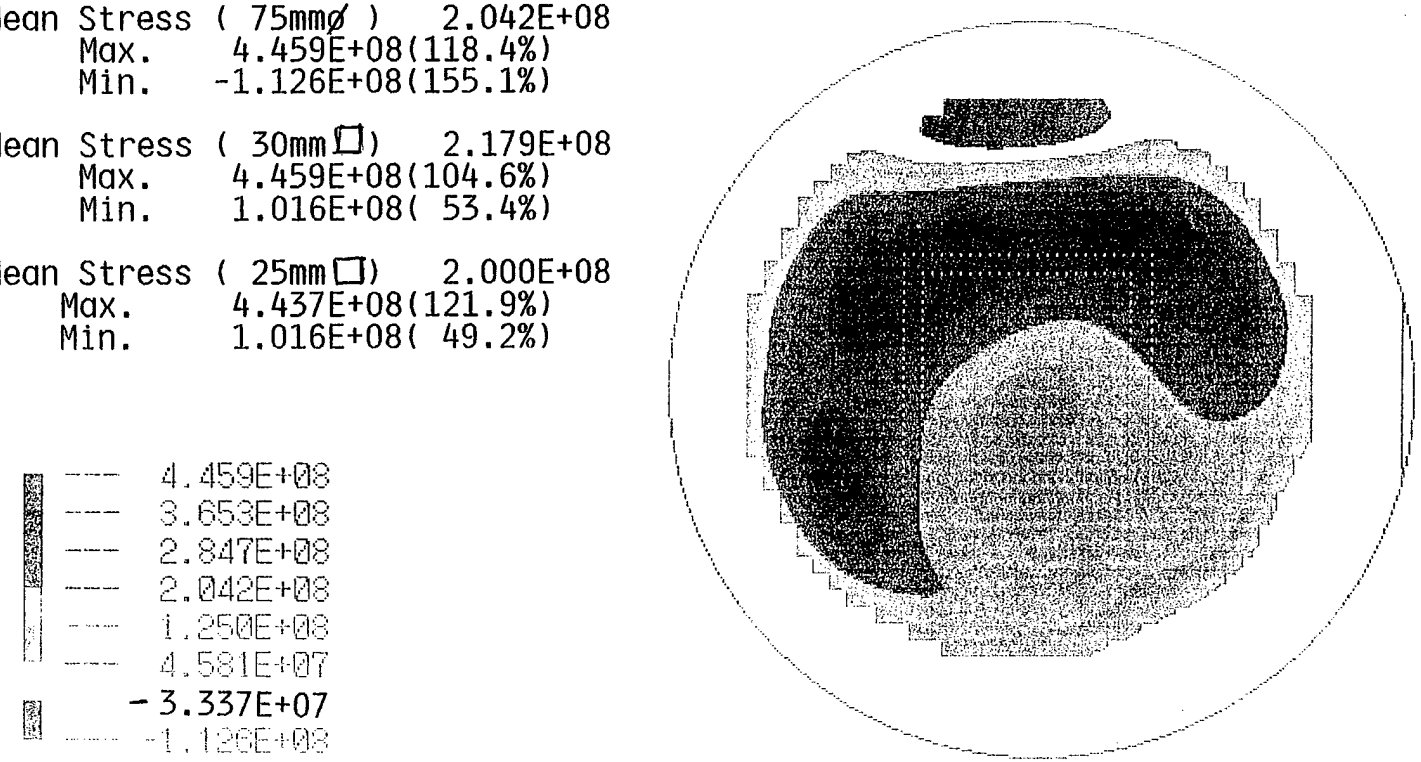
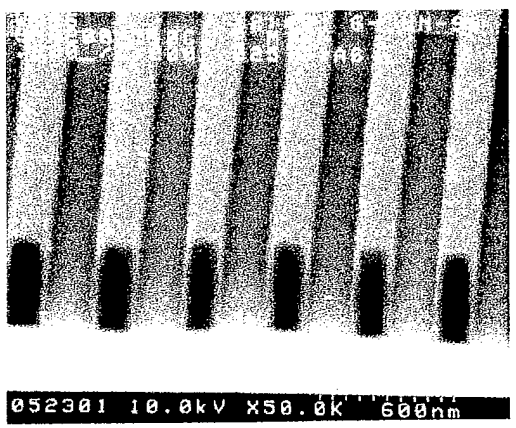
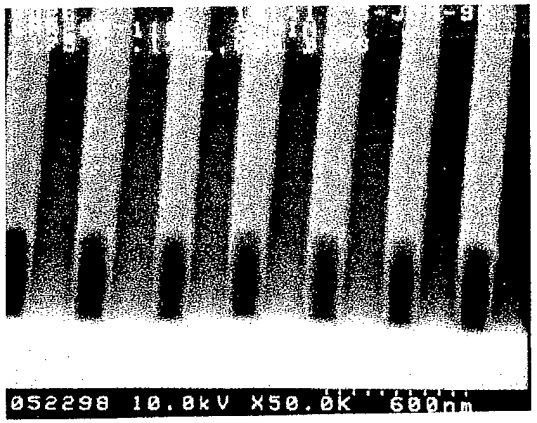


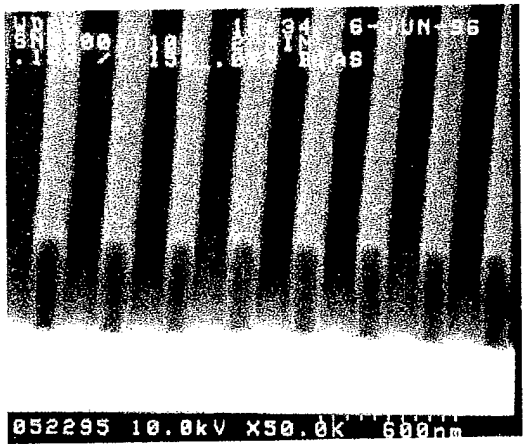
Figure 8. Stress Map of Wafer 3 as Reported by NTT Stress Measurement Tool



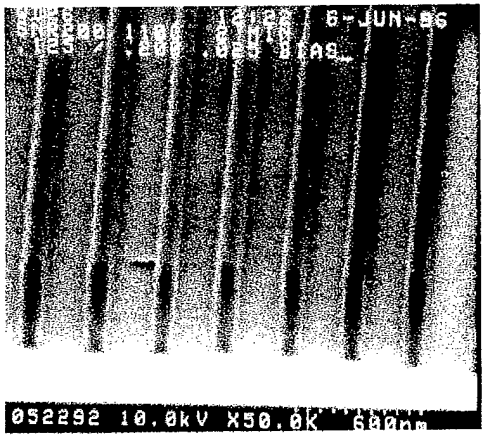
200/200 nm



175/175 nm



150/150 nm



125/200 nm

125/125 nm

Figure 9. SNR-200 Patterned on VS-5

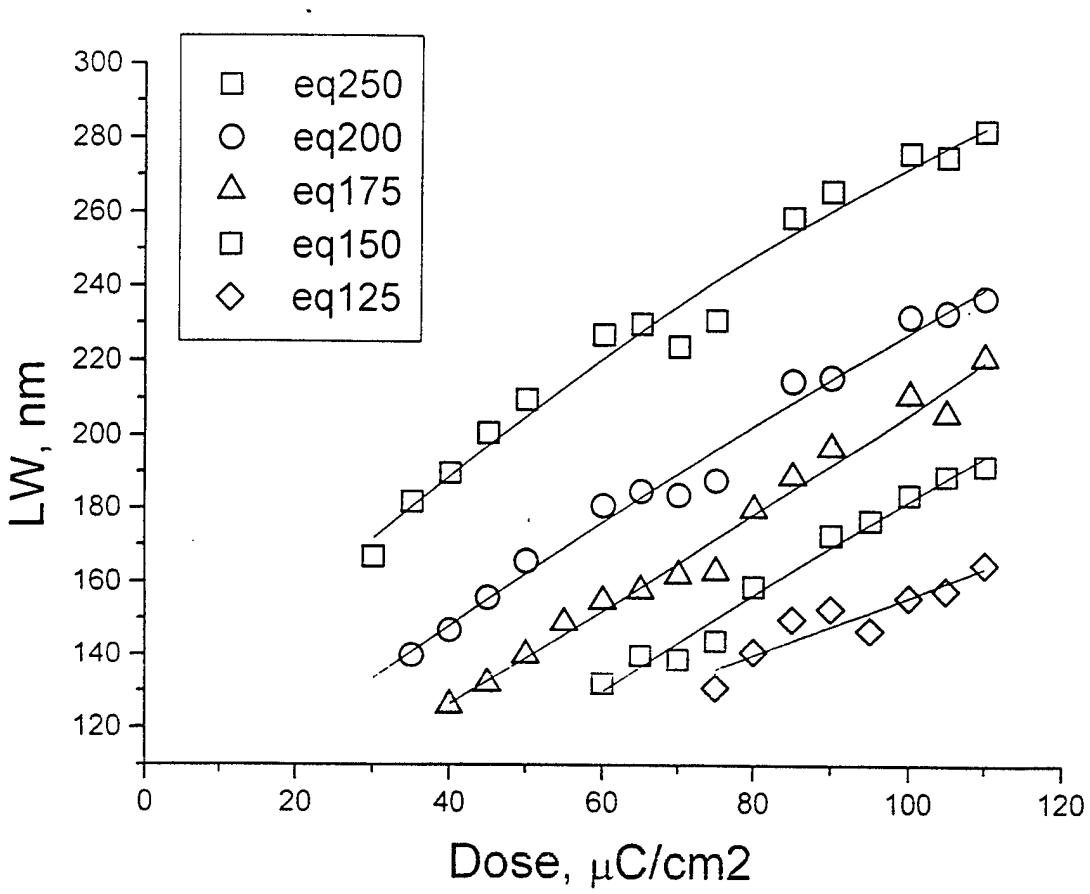


Figure 10. SNR 200:LW(Dose) Dependence for Nominally Equal Lines and Spaces

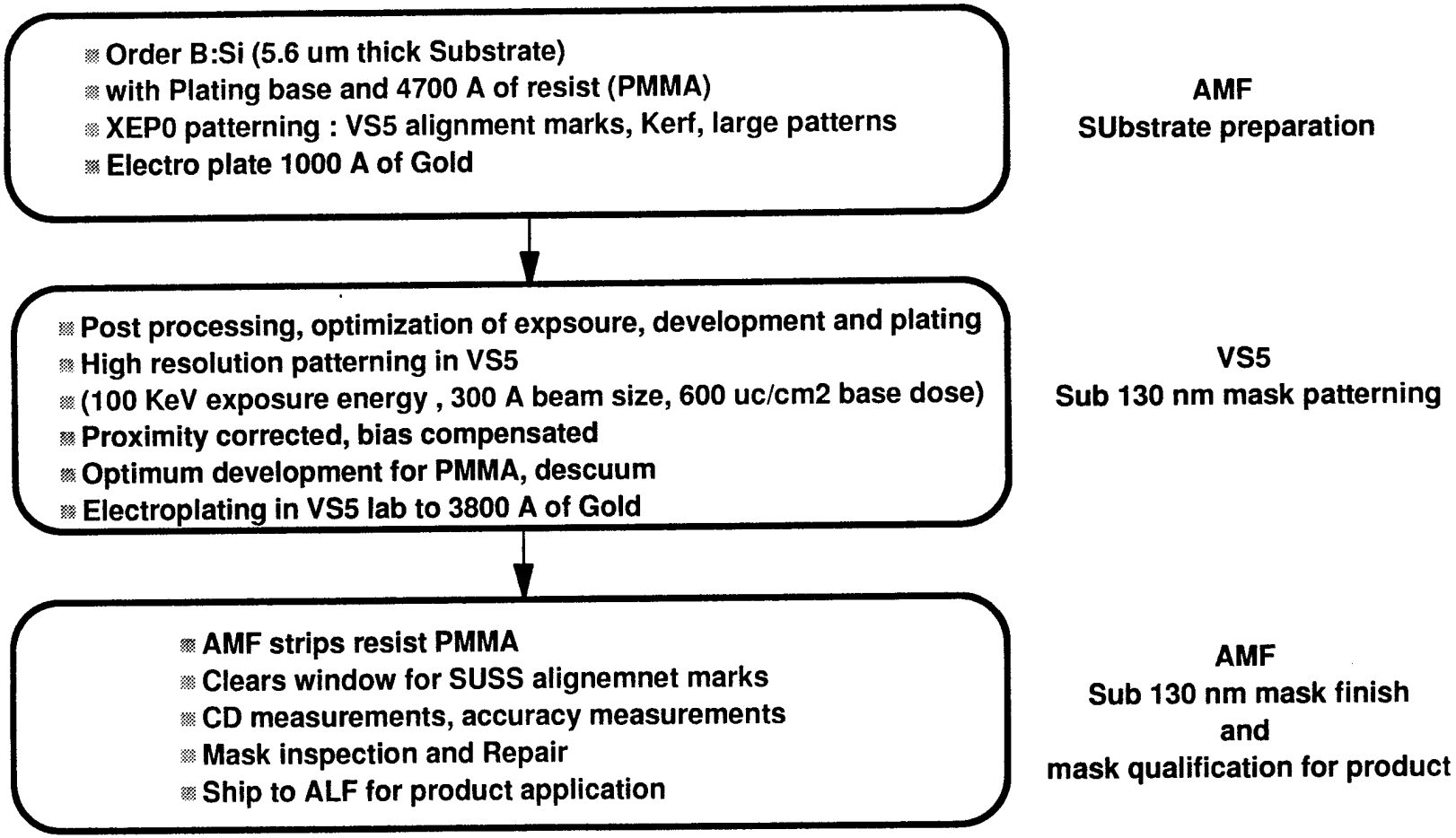


Figure 11. Sub-130nm X-ray Mask Fabrication Process Flow Using VS5 E-beam

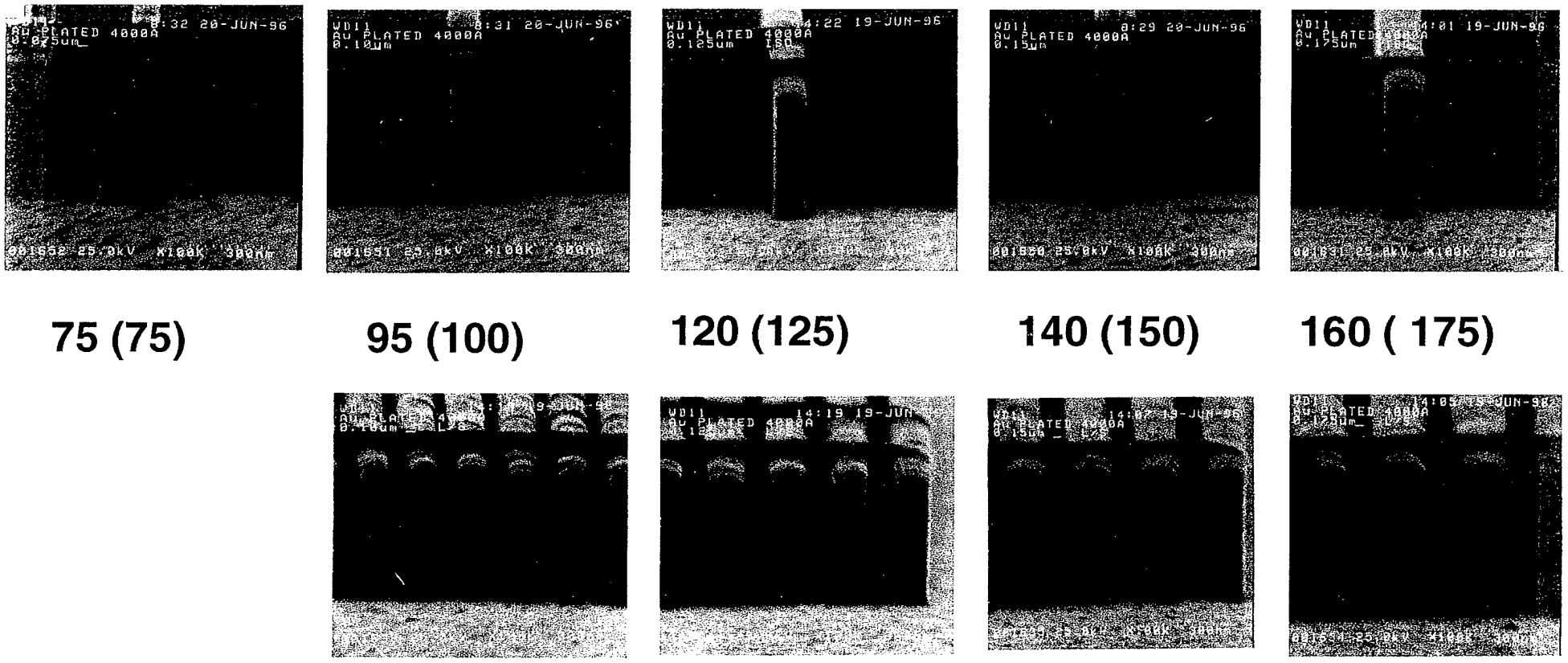
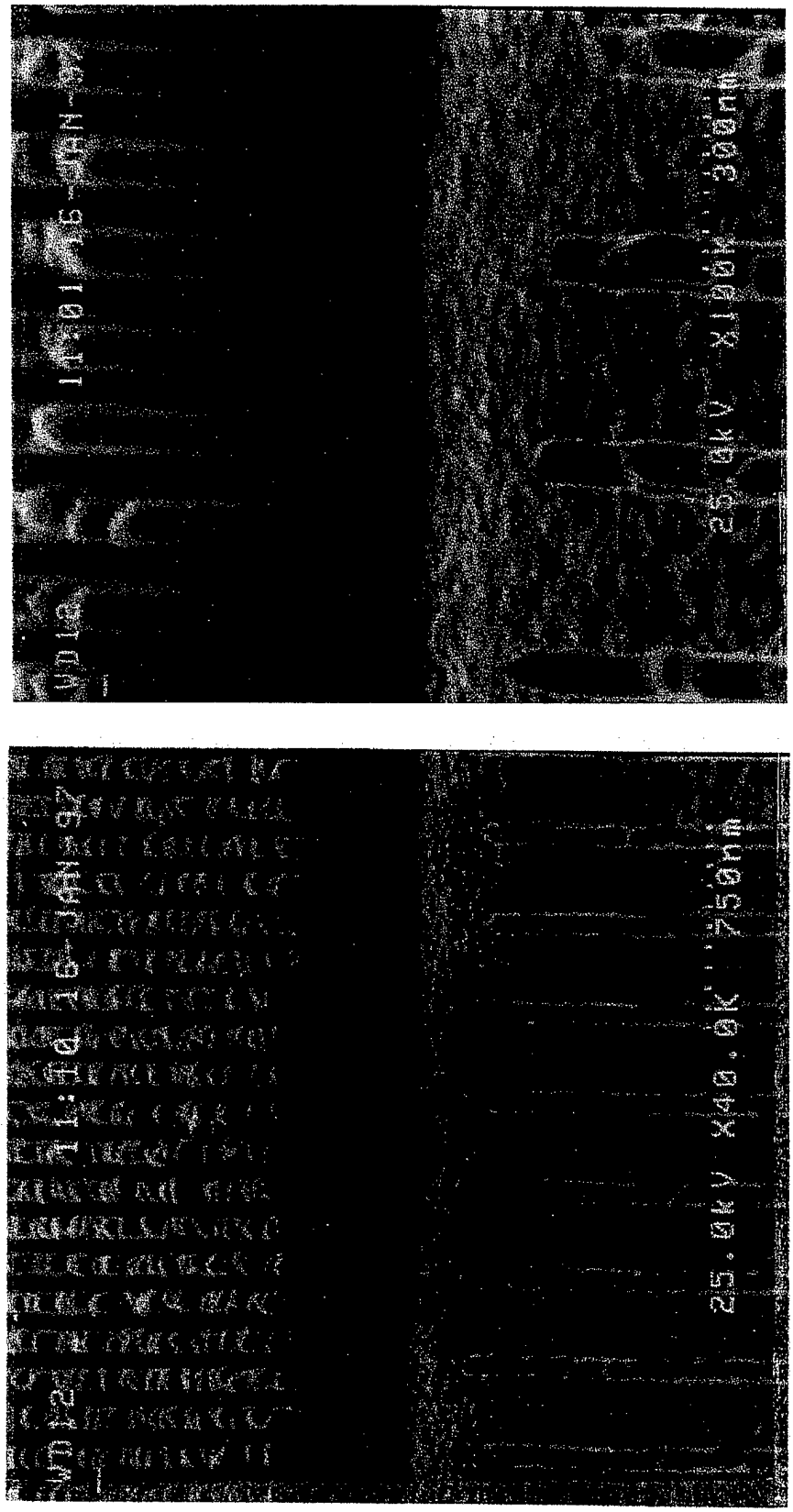


Figure 12. Gold Absorber for Advanced CMOS Technology Devices



Arrays of 75 nm Pillars with 75 nm space
Gold absorber thickness 350 nm
Exposure energy 100kV
Resist PMMA

Figure 13. Advanced X-ray Mask Fabrication Using VS5 4Gb Patterns

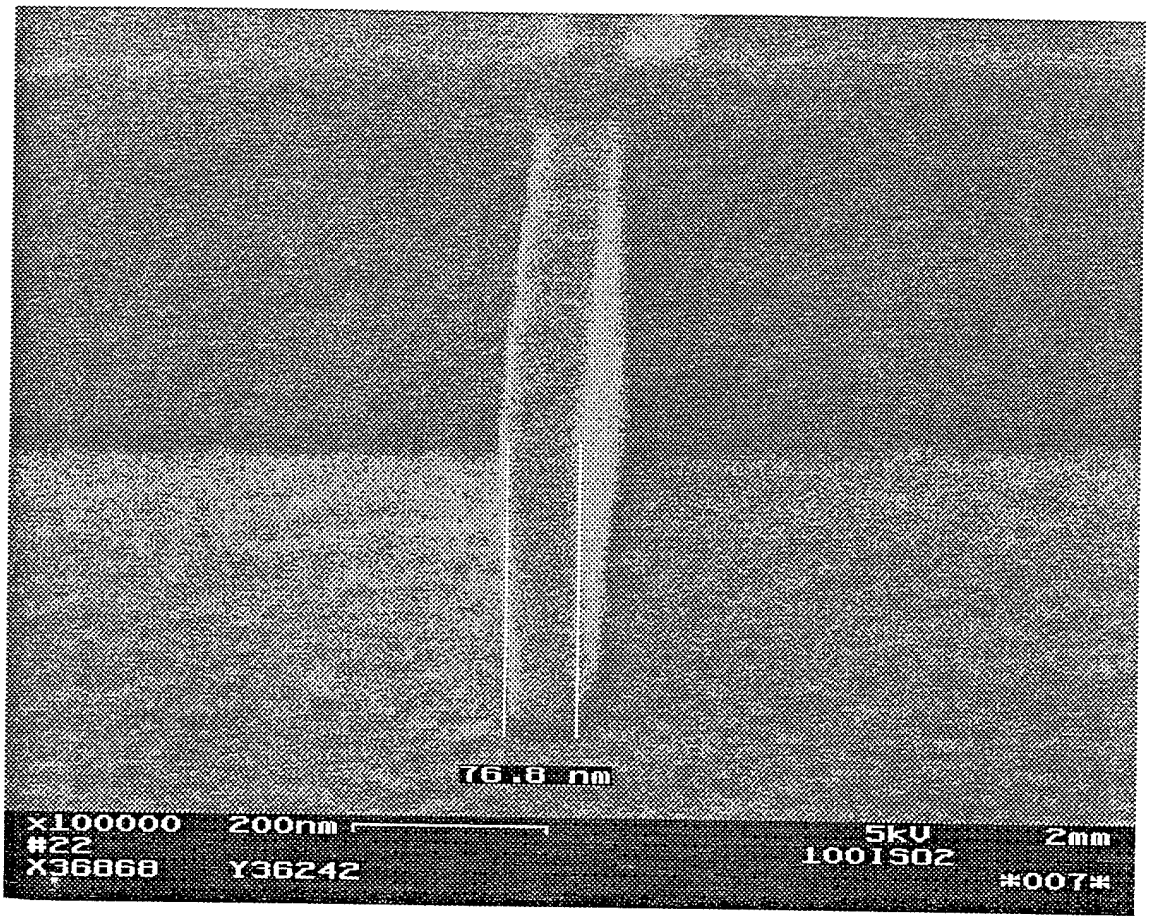


Figure 14. Coded 100nm Isolated Lines in Plated Gold

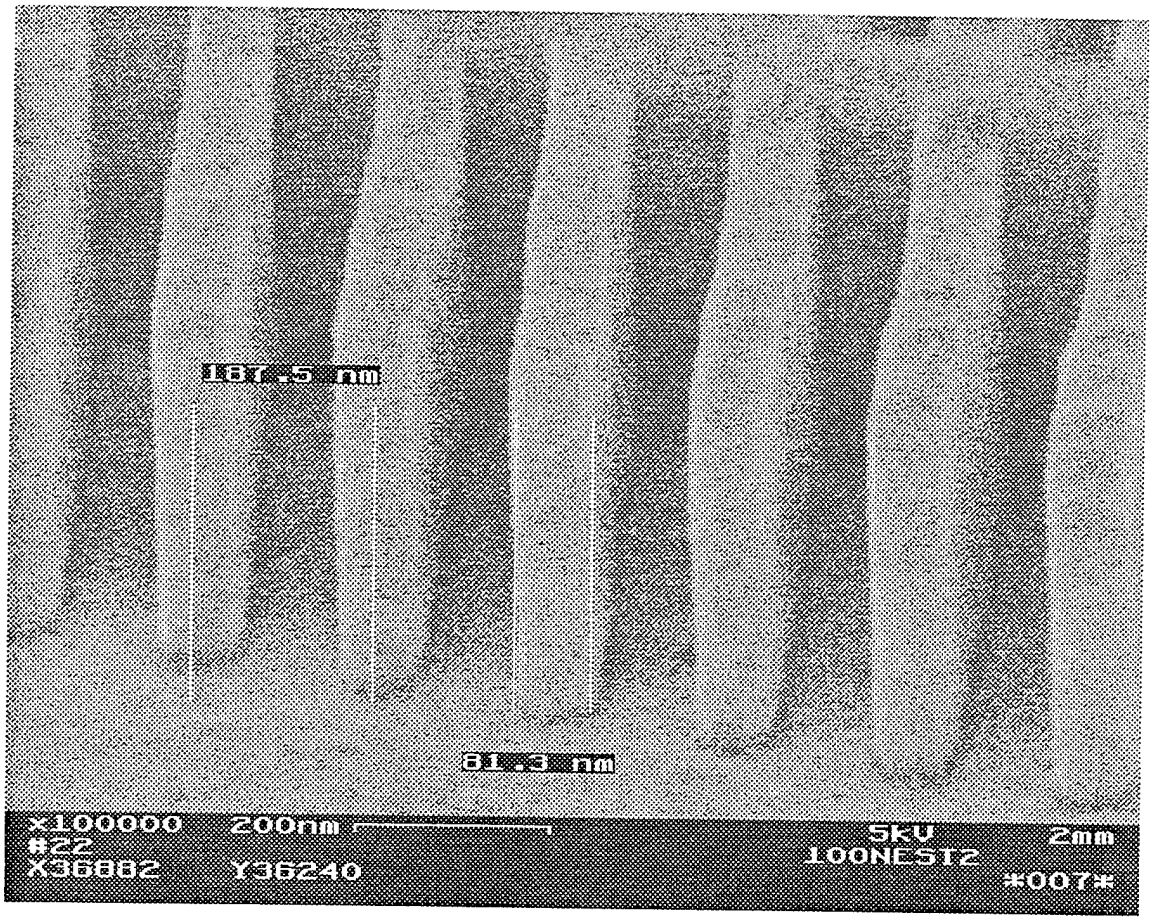


Figure 15. Coded 100nm Equal Lines and Spaces in Plated Gold

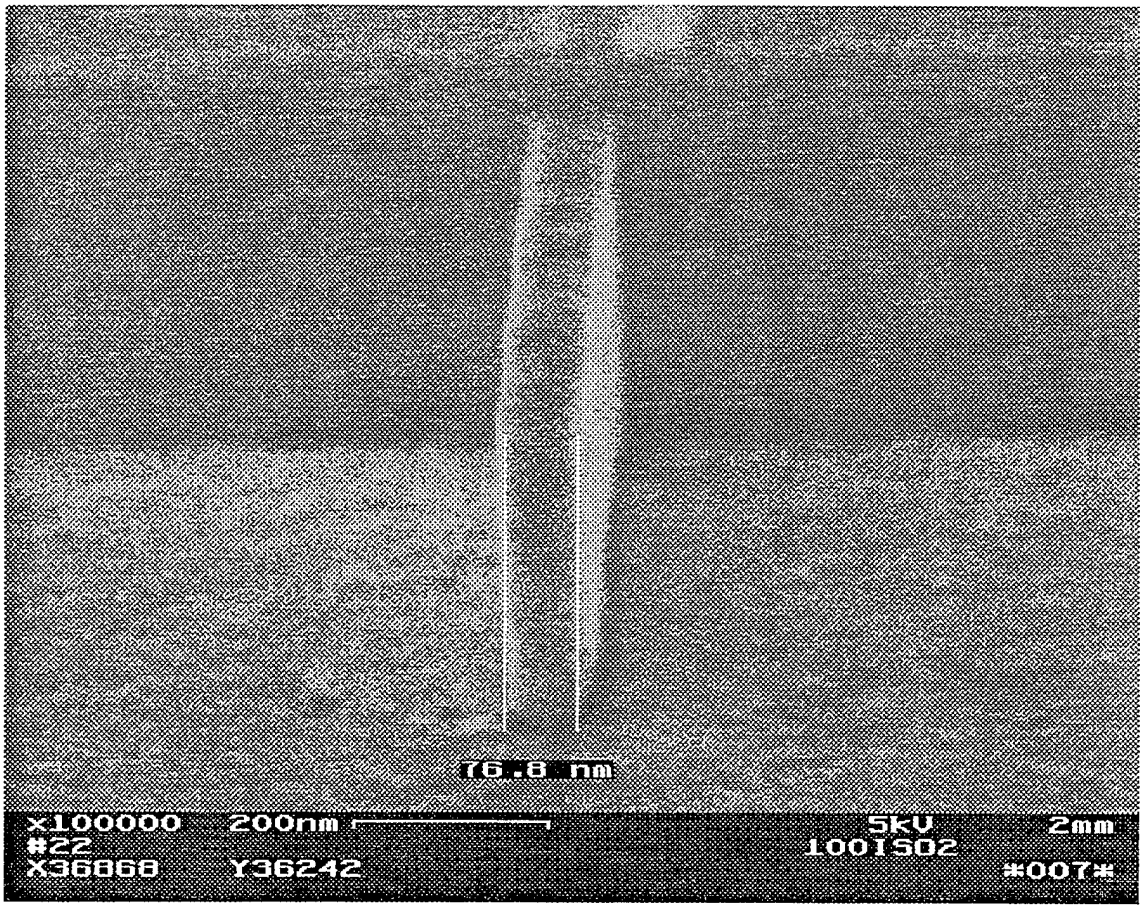


Figure 16. Coded 75nm Isolated Lines in Plated Gold

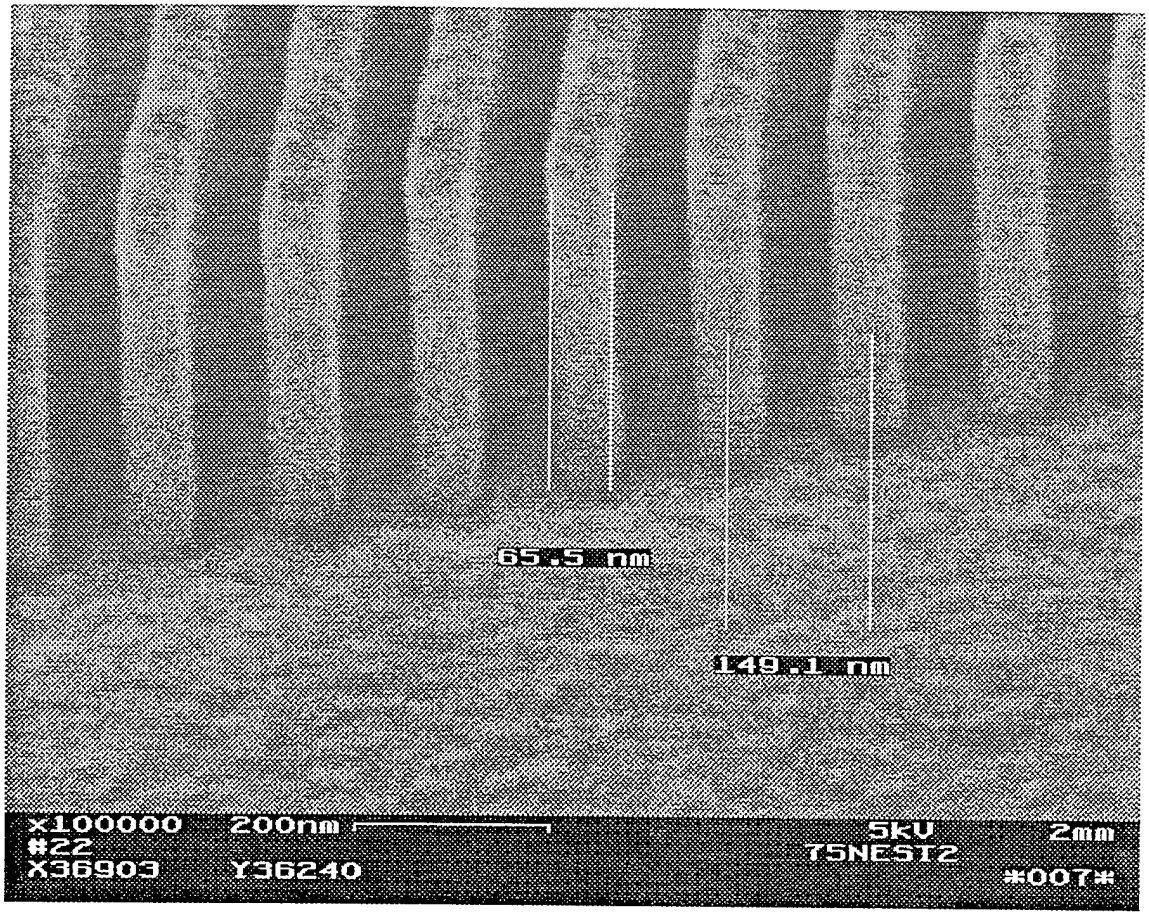


Figure 17. Coded 75nm Equal Lines and Spaces in Plated Gold

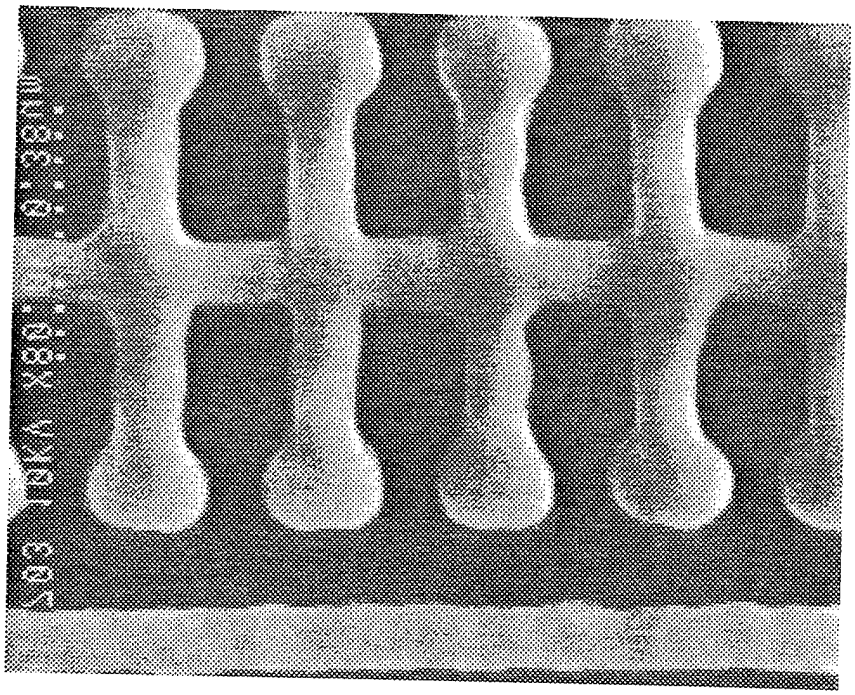


Figure 18. Top Down SEM View of 100nm Groundrule Pattern

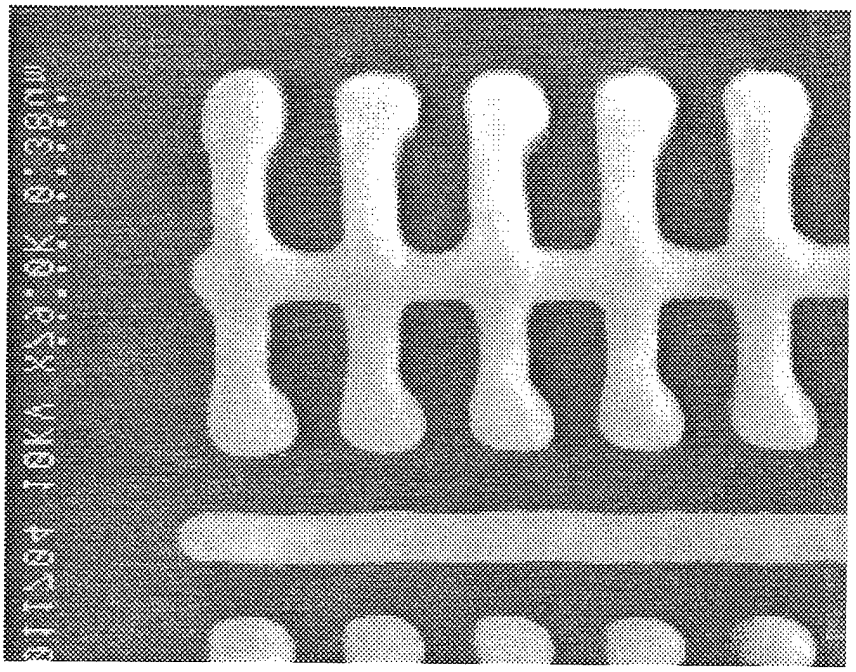


Figure 19. Top Down SEM View of 75nm Groundrule Pattern

Appendix B - SVGL

DALP X-Ray Aligner
Monthly Progress Report

SDRL A001

Period: November 23, 1996 through December 27, 1996

Reference Contract Number N00019-94-C-0035

Table of Contents

1.0 Executive Summary

Program Status:

The major emphasis in this period continued to be the improvement of the Aligner's throughput performance while maintaining the Aligner's overlay at specification levels. The Particle Detection System (PDS) mechanical assembly, Mask Handler Improvements, and Mask Cassette task continued to receive emphasis. Support of application exposures was also a priority as many exposures were completed during this period.

Highlights for this period include:

- Completion of throughput and overlay incremental performance improvement resulting in throughput at 22 Wafers per hour (actual time adjusted for 1 sec exposures) and overlay at < 50nm (mean + 3 sigma).
- Near completion of the mechanical assembly process for PDS.
- Support of customer Application exposures.
- Preparations for 10 micron gap exposures.
- Completion of technical evaluation for computer-aided finite element analysis of software and hardware on the Magnification Control task.

2.0 Beta Site Activities

2.1 Phase 1 Performance Improvements

2.1.1 Mask Damage

Mask Handler improvements designed to reduce the possibility of Mask damage were continued in this period. Progress on this task included completing a final concept review as well as engineering design changes. Planned activities for the next reporting period include the completion of any residual design issues, and placing orders for materials necessary to upgrade the Mask Handler Elevator.

2.2 Phase 2 Performance Improvements

2.2.1 Throughput Improvements

Throughput improvements have continued in this period. Analysis of overlay data showed that the overlay errors appear to be a repeatable systematic effect, with the largest errors seen on the first three wafers in the lot. Further analysis showed that by stepping the Wafer Stage for 5 minutes prior to the start of a Run, the magnitude of the overlay errors were reduced by at least a factor of two. A strategy was developed and implemented in Run software that would step the Wafer stage prior to the start of a run with wafer calibration cycles reduced from once per wafer to 7 per 25 wafers. The Aligner was characterized for throughput and overlay performance under these conditions, with the throughput at 22 Wafers per hour (actual time adjusted for 1 sec exposures) and overlay at < 50nm (mean + 3 sigma).

Throughput improvements in Mask fine alignment (MFA) were also implemented in this period. A strategy was developed and implemented in software that would calculate the initial Framing Blade positions required during MFA and move the Framing blades during a non critical wafer load sequence. This improvement was verified to reduce MFA time by 10 seconds.

Software improvements implemented in this period included upgrading the Run software to reduce the number of wafer calibration cycles, step the Wafer stage prior to Run and implement look ahead Framing blade moves for MFA.

Continued testing of systematic overlay affects as well as more throughput software improvements are planned in the next reporting period.

2.2.2 Backup XRIS

An issue with the backup XRIS was discovered during the mounting process. It was determined that the XRIS mount was unusable and it was decided that a new mount should be ordered. The mount was not ordered during this period due to a minor issue with processing engineering changes. The mount will be ordered during the next reporting period.

2.3 Particle Detection System

Progress on the Particle Detection System (PDS) was focused on the mechanical assembly. Several minor design were identified and corrected during the assembly process. Some mechanical rework is still ongoing with the assembly completion anticipated in the next reporting period.

An issue with threading the wire used to detect particles was identified. The wire was found to be extremely difficult to assemble due to its material (Aluminum) and small diameter (0.0006 inches). Samples of various wire materials and diameters will be tested in the next reporting period.

Plans for the next reporting period include hiring of an Electrical Engineer to work full time on the electrical control hardware and harnessing. Additional staffing within SVGL will be assigned on an as needed basis to assist with Engineering, Assembly and Design requirements. Software activities will also start in the next reporting period.

2.4 Mask Cassette

The design work for a second Mask cassette was completed during the last reporting period. Procurement of the necessary parts is anticipated to start in the next reporting period.

2.5 Aligner Maintenance & Support

A Mask charging issue identified last month which manifests itself during exposures of Masks that are mostly gold continued to receive attention. This issue was under investigation with another set of experiments completed in this period. A successful containment of this problem which includes Mask grounding, half chip mask exposures and lowering the Wafer stage velocity enabled several Application exposures to be completed in this period. Plans to investigate this issue include measuring Mask & Wafer stage forces in the Aligner and measuring the differential pressure across the Mask.

Mask to Wafer Gapping calibration to support 10 micron gap exposures was initiated in this Period. Tasks completed include optimization of sensor positions during Mask and Wafer leveling and Capacitance gauge calibration with updated spline fit tables. Completion of this task is anticipated in the next reporting period.

A communication issue was identified in this period that would cause intermittent errors between the Operator Interface and the Single node computers. A Run software patch was implemented to contain this error with hardware investigations planned for the coming weeks.

Support of many Application exposures was prioritized in this period with approximately 2/5ths of the system time allocated for exposures.

2.6 Plans

Plans for January include:

- Continue Mask Charging Investigation.
- Continue Particle Detection System design and mechanical assembly.
- Continue to Optimize and Characterize Throughput and Overlay utilizing Second-Level exposures.
- Support of Application Exposures.
- Initiation of Mask Cassette procurement.
- Completion of Mask Cassette Docking design changes.
- Place Backup XRIS mount on order.

3.0 Magnification Control Activities

3.1 Status

The Advanced Programs group technical evaluation of computer-aided finite element analysis software and hardware was completed. A capital appropriation request for purchasing this equipment from Structural Dynamics Research Corporation (SDRC) was finalized, and it is presently being approved. The baseline analysis for the Mask Distortion Modeling task was started, using computer-aided finite element analysis tools made available from within other engineering groups at SVGL. Dedicated use of this equipment by these groups necessitated the additional software and hardware purchase, but temporary timesharing allowed the modeling effort to begin.

System level requirements have begun to be reestablished with the emphasis on updating and refining present DALP X-Ray Aligner specifications as related to the addition of the Magnification Control Option feature. Talks were somewhat limited this month on mask process and design issues, but a dialog was initiated and a meeting is scheduled in early January to continue this pivotal discussion.

3.2 Plans

Plans for January include:

- The step up of discussions with the customer on issues regarding present and anticipated x-ray mask design processes, ring geometry design and materials, as well as Aligner system level requirements and specifications.

- The start of systems level modeling on overlay, throughput, mask distortion and gapping, and algorithm development.
- Completion of a first case, baseline analysis model using an SVGL/NIST standard mask.

4.0 Program Office

4.1 Funding

To date, SVGL has received $500,000 of contract authorized funding against CLIN 200 (Extended Support) and $263,000 against CLIN 201 (Magnification Control Option). $391,846 has been expended against the contract through 27 December 1996.

4.2 Key activities in this reporting period

The Program Office continues to maintain focus on software and hardware integration activities that support the effort to achieve a demonstration of throughput and overlay performance at the Beta site. An updated plan of Beta site activities is being used to track day-to-day activities.

Working reviews are being held at the Beta site on a weekly basis in lieu of the more formal monthly reviews at SVGL. This approach reduces preparation time and serves to maintain focus on day-to-day progress against plans.

4.3 Staffing Status

Addition staffing levels are being actively pursued by way of Purchased Technical Services. An offer package is being prepared for an electrical engineer to work on the Particle Detection System. This person will begin work in January.

Additional staffing within SVGL will be assigned on an as needed basis to assist with Engineering, Design and Assembly requirements, primarily for the Particle Detection System.

4.4 Plans

Within the limits of available funding the Program office will, in conjunction with Lockheed Martin/IBM, continue to work to execute the updated Beta Site plan, and to assure coordination of Aligner, Beam line, and Process related integration activities. In so doing, we hope to achieve a successful integration of the Particle Detection System and throughput at 40 wafers per hour while maintaining specification level overlay performance.

DALP X-Ray Aligner
Monthly Progress Report

SDRL A001

Period: December 28, 1996 through January 24, 1997

Reference Contract Number N00019-94-C-0035

Table of Contents

1.0 Executive Summary

Program Status:

Beta Site Activities:

The major emphasis in this period continued to be the improvement of the Aligner's throughput performance while maintaining the Aligner's overlay at specification levels. Additional emphasis was put toward progress in the Particle Detection System (PDS) electrical design, Mask Handler Improvements, and on the Mask Cassette task. Procurement of parts is being held back until additional funding is received. There was also continued support of application exposures as many exposures were completed during this period.

Highlights for this period include:

- Identification of Wafer Handling sequence improvements for throughput.
- Initiation of Particle Detection System (PDS) electrical design including circuit board and harnessing details.
- Completion of 10 micron gap exposures under manual control.

Magnification Control:

A preliminary mask distortion analysis comparable to previous predictions of force-to-displacement behavior has been performed. This preliminary analysis will become the baseline for optimizing placement of force actuators in regard to the magnification adjustment capability of various mask membrane sizes.

2.0 Beta Site Activities

2.1 Phase 1 Performance Improvements

2.1.1 Mask Damage

Mask Handler improvements designed to reduce the possibility of Mask damage were continued in this period. The resolution of some residual mechanical design issues form the prior period was deferred as efforts were shifted to the PDS task. The placing of orders for materials necessary to upgrade the Mask Handler Elevator has been put on hold due to funding limitations.

2.2 Phase 2 Performance Improvements

2.2.1 Throughput Improvements

Throughput improvements have continued in this period. Tasks completed include the qualification of a RUN version to be used for application exposures, and Identification of a wafer handling Robot sequence change which could reduce the Wafer Handling time by at least 3 seconds.

Plans for the next reporting period include continued characterization of throughput timing as well as implementation of the improved Robot sequencing.

2.2.2 Backup XRIS

The XRIS mount was ordered during this period.

2.3 Particle Detection System

Progress on the Particle Detection System (PDS) focused on the electrical design. An Electrical Engineer was hired during this period to work full time on the electrical control hardware and harnessing. Design of the detection electronics, positioning servo amplifier and cap gauge rectifier were started in this period. Harnessing design was also initiated in this period.

An issue with an interference of the PDS mechanical assembly was identified during this period. A fit test in the Aligner at ALF identified an interference with the Off Axis alignment sensor. An initial investigation has begun for a final design solution. Mechanical rework scheduled for this period was not completed because of this interference issue.

Plans for the next reporting period include completion of a wire test fixture to facilitate functional testing of the PDS detection electronics, design completion of the positioning servo amplifier and cap gauge rectifier PC Boards and the investigation of a design solution for the mechanical inference.

Software activities did not begin in this period due higher priorities but are anticipated to begin within the next two months.

2.4 Mask Cassette

The design work for a second Mask cassette has been completed. Procurement of the necessary parts is on hold due to funding limitations.

2.5 Aligner Maintenance & Support

Mask to Wafer Gapping calibration to support 10 micron gap exposures was continued in this Period and resulted in wafer exposures at 10um gap. The exposures were completed in a manual mode of operation to prohibit the Xray Image Sensor (XRIS) from going in front of the mask at small gaps due to large particles (>10um) on the XRIS. Remaining issues include investigation of a 2.5um position offset from the Wafer to XRIS and a 13urad Tx angular Wafer offset after leveling.

An Mask charging issue had been identified that manifested itself during exposures of Masks that were mostly gold. The effect on the Aligner resulted in a Mask to wafer collision and Wafer Stage servo errors. A successful containment of this problem which includes Mask grounding, half chip mask exposures and lowering the Wafer stage velocity enabled several application exposures to be completed in this period. Measurement of the Mask stage forces and monitoring of the differential pressure across the Mask was also implemented in this period.

Hardware investigations to fix a communication issue identified in the prior period should be initiated in February.

2.6 Plans

Plans for February include:

- Continue Particle Detection System electrical design, perform bench testing of the detection electronics, complete the design changes identified during the initial mechanical assembly process, and investigate a design solution for the mechanical interference.
- Continue to Optimize and Characterize Throughput and Overlay utilizing Second-Level exposures.
- Continue Mask Charging Investigation.

3.0 Magnification Control Activities

3.1 Status

The SDRC-Ideas workstation and software code has been approved and ordered. This system will be dedicated primarily for the MCO tasks. The baseline analysis for the Mask Distortion Modeling task continued, using finite element analysis tools from other engineering groups within SVGL. A first case, preliminary analysis using an NIST Standard Mask was run, and yielded X-mag and Y-mag displacements within the range of original predictions.

Discussions with the mask manufacturer and customer were stepped up with regard to mask design and process issues, and will be examined further at a February technical review. The format of the mask will be necessary for final design of the MCO.

The effort to further update and refine the present DALP X-Ray Aligner specifications as they relate to the Magnification Control Option is ongoing. No progress has been currently made in the area of systems level modeling on overlay, throughput, mask distortion, gapping, or algorithm development.

A revised plan that omits installation and implementation of the MCO on the present DALP X-Ray Aligner is under discussion. A review of the present statement of work is needed to address a change of scope. Some present tasks will be modified or eliminated, with the following tasks being the primary focus of the project:

1. Completion of the compliance assessment modeling of a mask for analytical demonstration and understanding of magnification displacement potential.
2. Fabrication of a breadboard model for empirical testing and comparison to modeled results.
3. Feasibility study of differential mask and wafer scanning techniques.
4. Feasibility study of beamline optics magnification control.
5. Feasibility of wafer magnification adjustment.

3.2 Plans

Plans for February include:

- Further discussions on mask format standard concerning ring geometry, substrate thickness, and Aligner system level requirements for gapping.
- Conduct a technical review meeting and interactive discussion with the customer to discuss preliminary results of the compliance assessment modeling.
- Complete a modified statement of work for the projected change of scope.

4.0 Program Office

4.1 Funding

To date, SVGL has received $500,000 of contract authorized funding against CLIN 200 (Extended Support) and $263,000 against CLIN 201 (Magnification Control Option). As of 24 January 1997, $450,164 has been expended against CLIN 200 and #35,140 has been expended against CLIN 201.

4.2 Key activities in this reporting period

The Program Office continues to maintain focus on software and hardware improvement activities that support the effort to achieve a demonstration of throughput and overlay performance at the Beta site. An updated plan of Beta site activities is being used to track day-to-day activities.

Working reviews are being held at the Beta site on a weekly basis in lieu of the more formal monthly reviews at SVGL. This approach reduces preparation time and serves to maintain focus on day-to-day progress against plans.

4.3 Staffing Status

An electrical engineer was hired in this period. Additional staffing from within SVGL will be assigned on an as needed basis to assist with Engineering, Assembly and Design requirements, primarily for the Particle Detection System.

4.4 Plans

Within the limits of available funding the Program office will, in conjunction with Lockheed Martin/IBM, continue to work to execute the updated Beta Site plan, and to assure coordination of Aligner, Beam line, and Process related integration activities. In so doing, we hope to achieve a successful integration of the Particle Detection System and throughput at 40 wafers per hour while maintaining specification level overlay performance.