NORTHROP GRUMMAN

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May 28, 1997

Letter No. CYRO-RADAR-CDRL-A0017

Office of Naval Research, ONR-31
Attn: BAA-ACI, Room 720
800 North Quincy Street
Arlington, VA 22217-5660

Attention: Glynis Fisher, ONR 251, Contract Negotiator

Subject: Monthly Status Report, CDRL 0001, Data Item A001, CRYORADAR ADC Feasibility Demonstration Program

References: (A) Contract No. N00014-95-C-0195
(B) Westinghouse G.O. 47862

Enclosure: Monthly Status Report, CDRL 0001, Data Item A001, CRYORADAR ADC Feasibility Demonstration Program, one (1) copy

Dear Ms. Fisher:

We are pleased to submit the Monthly Program Status Report, CDRL 0001AA, Data Item A001 in accordance with the Referenced (A) contract requirements. This report covers the period ending 30 April 1997. The Program Funding Status Report is attached as well.

Please contact the undersigned with any questions. Technical questions may be directed to the Program Manager, Mr. Hal Ball (410) 765-0410.

Sincerely,

NORTHROP GRUMMAN CORPORATION

Helen Panagiotopoulos

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NRL, Director, Code N00173, one (1) copy
Defense Tech. Info. Center, Code S47031, two (2) copies

CRYORADAR™ ADC Feasibility Demonstration Program
Contract No. N00014-95-C-0195
Status Report for Period Ending 30 April 1997

Meetings and telephone conference calls were held in April with STC, Conductus, Oregon State University, and UCLA. M. Fitelson and A. Davidson visited UCLA on 1 April 1997. Two separate trips involving H. Ball, J. Colgan, A. Pershall, and G. Kolnowski were made to STC in preparation of and during Demo 1. Demo 1 was done on 23 April at STC with Dr. VanVechten present. Mr. R. Fagaly of Conductus-San Diego visited J. Donovon in Baltimore on 17 April to discuss the final plans for the dual stage package. As a related synergistic activity, H. Ball attended a planning meeting with Drs. Nisenoff and VanVechten at TRW with TRW, Loral, Hughes, and JPL to lay preliminary ground work for a new thrust in digital communications for satellites. Also, several contractor personnel will support the HTS Collaboration meeting with the government sponsors on 12 and 13 May in Washington D.C.

As of 14 May, 1997, the CRYORADAR™ ADC Feasibility Demonstration Program has invoiced $2,045,866. Total estimated spending as of 27 April, 1997, is $2,032,000. Program Spending Status and Program Funding Status charts are attached.

The Program Schedule Status is attached and reflects progress and task activity on the program. The program is approximately one month behind the original schedule due to the 1996 stop work period. Demo 1 was completed on 23 April.

Recently, Program Management has focused on the re-evaluation of the program scope with the ONR Program Manager. Tasks and associated costs of the baseline program plan are being reviewed in the context of a potential funding reduction and optimum approaches are being explored to complete this phase of the program in mid 1998 in preparation of the next Option Phase which is part of the current contract. Preliminary correspondence with the customer has occurred to exchange background information and put forth potential scenarios.

System Engineering

An analysis tool to investigate ADC dynamic range impact on receiver non-linearities is complete. This tool will be used to define the receiver requirements to support the high dynamic ranges afforded by the HTS sigma-delta analog-to-digital converters.

HTS Component Fab & Test - Conductus

This program's support of the development of HTS JJ technology at Conductus has lapsed due to a reduction in funding.

Superconducting Modulator/Demux

Testing of chips has continued. Two types of differential output circuits have been tested at low speed. One type, based on magnetic coupling has been tested with some success. The second type, based on three junction interferometers, has been subject to undesired flux storage and has been less successful. High speed testing is now underway.

Modifications to the Demo 1 modulator are currently being simulated to improve dynamic range.

A software modification, which is nearly complete, will allow the collection of up to 1 Mbit of raw data from the Demo 1 test setup, permitting a more precise determination of the signal to noise performance of the modulator.

Digital Filter - OSU

Work on the Digital Filter task has continued at Oregon State University. A. Pershall of Northrop Grumman has had ongoing dialog with the OSU technical folks. The following input was provided by OSU:

Current estimate on the decimation filter size and power (unchanged from last report): 2 chips (HP 0.5 um fab), power<5W.

1. A 2nd test chip was taped out - Another test chip was sent to fabrication this month. The chip has a ECL-CMOS input&output interface and some CMOS adders inside. The power supply for the CMOS circuit is -3v to 0v. The purpose of the chip is to test those adders and the ECL input & output pads.

2. System level work finalized - The filter has been simulated down to the bit-true level. All the coefficients have been finalized. Simulation programs, data files, schematics and documents are now all available. (Implementation or layout considerations may result in revisions to these items.)

3. Dr. Lu will take over the layout work in the summer - As the architectural work is essentially complete. The layout work is all that remains. Shih-Lien will do the first stage decimator this summer. Low-speed testing will be done at OSU, but we expect that at-speed testing will be done at Northrop-Grumman.

4. Dr. Schreier will leave OSU this summer - Richard intends to take a "leave of absence" in lieu of a sabbatical. He has accepted a position with Analog Devices and will depart OSU shortly after June 13. Since the architectural work is mostly done, his leaving should not affect the progress of the project too much. We fully expect that Northrop-Grumman will be satisfied with the deliverables which result from this sub-contract.

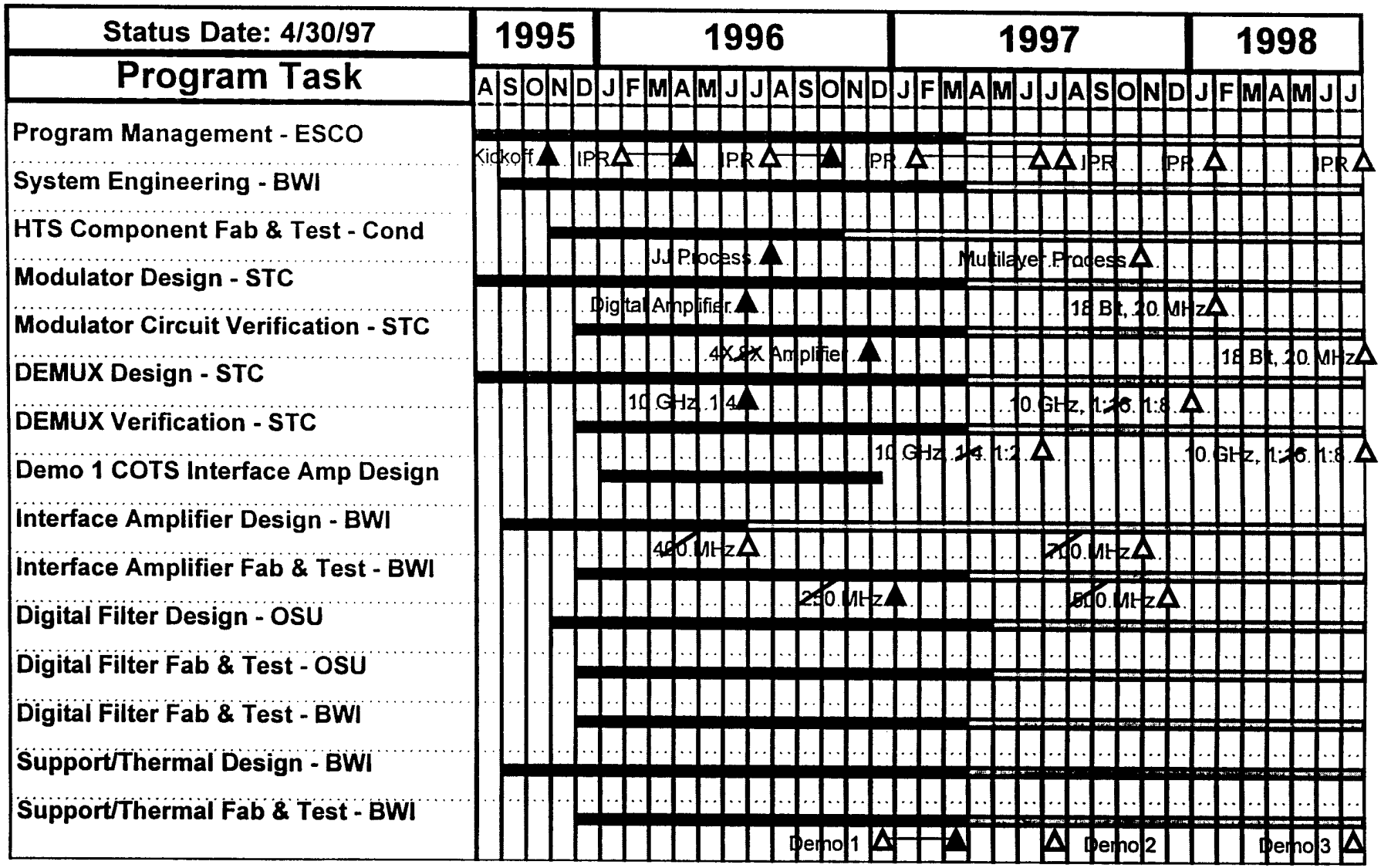
Interface Amplifier / Support Electronics, Packaging, & Thermal

The focus of this task in April was to support Demo 1 at STC in Pittsburgh. Two separate trips involving J. Colgan, A. Pershall, and G. Kolnowski were made to STC in preparation of and during the demonstration. All of the elements of Demo 1 that were included in this task area were provided and supported. The Interface Amplifier, threshold detector, demultiplexor, buffer memory, frequency reference, and PC with digital filter software simulator were included and functioned as planned.

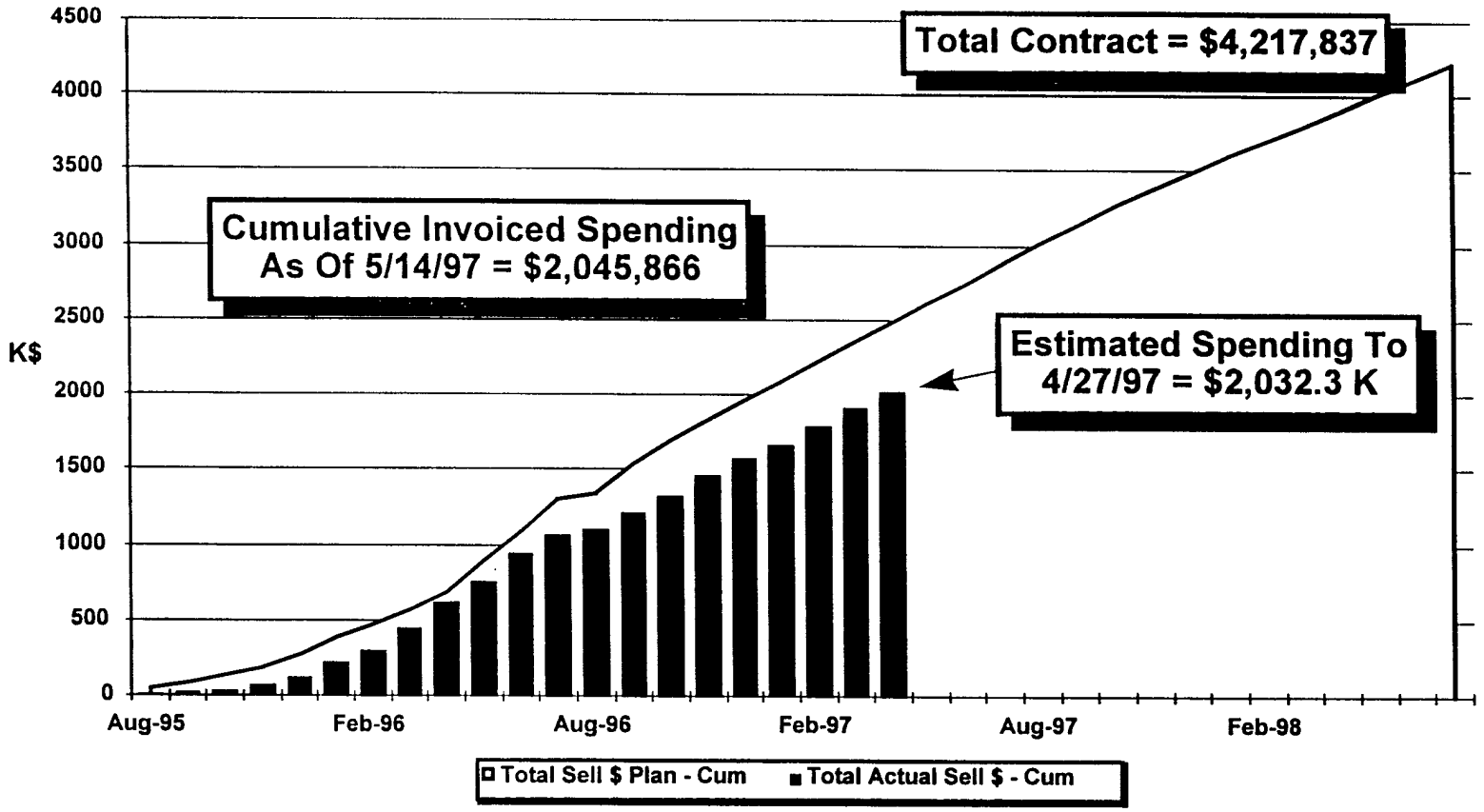
Subsequent activity has focused on the re-evaluation of the program scope with program management. Tasks and associated costs of the baseline program plan are being reviewed in the context of a potential funding reduction and optimum approaches are being explored to complete this phase of the program in mid 1998. Communication with Oregon State University has taken place to develop alternate, but evolutionary, applications of their digital filter, and advice has been sought concerning the delta-sigma performance impacts associated with the potential changes. We have

Conductus on hold with respect to the purchase of their modified dual stage package which was planned originally for Demo 3. We have also pursued some additional software work on the digital filter simulator to provide additional capabilities that were identified during Demo 1.

Program Schedule Status



Program Spending Status - 4/27/97



Program Funding Status - 4/27/97