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ADVANCED APPLICATIONS OF LASERS IN MATERIALS AND PROCESSING

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ADVANCED APPLICATIONS OF LASERS IN MATERIALS PROCESSING

Monday, August 5, 1996

Sessions:

MA: Fabrication

MB: Analysis

8:30am - 9:15am (Invited)
MA1

Pulsed Laser Deposition of Dielectric and Superconducting Materials : Mechanisms and Applications

Tomoji KAWAI,
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1. Advantages of laser ablation method for the synthesis of metal oxide thin films.

Laser ablation method is suitable for the formation of metal oxide thin films, such as dielectric materials and high Tc superconductors. This is because laser beam comes from outside of the film formation chamber and therefore oxygen pressure can be chosen as a desired value for the growth of thin films. Fig.1 shows a schematic diagram of laser ablation system used for the experiment. Emission of atoms and ions only from the irradiated targets gives a non-contaminated pure thin films on the substrate which are suitable for the device application. Internal excess energy and kinetic energy ranging from 10 to 100eV of emitted atoms and ions by laser ablation also assist the migration of atoms on the substrate surface leading to the low temperature formation of thin films.

2. High dielectric constant thin films

Fig.2 shows D-E hysteresis curve of $PbTiO_3$ thin films formed by laser ablation. Clear hysteresis is observed, and the value of remanent polarization is 80 μC which is almost the ideal value of $PbTiO_3$. This high quality c-axis oriented film is obtained by rapid cooling of the film after

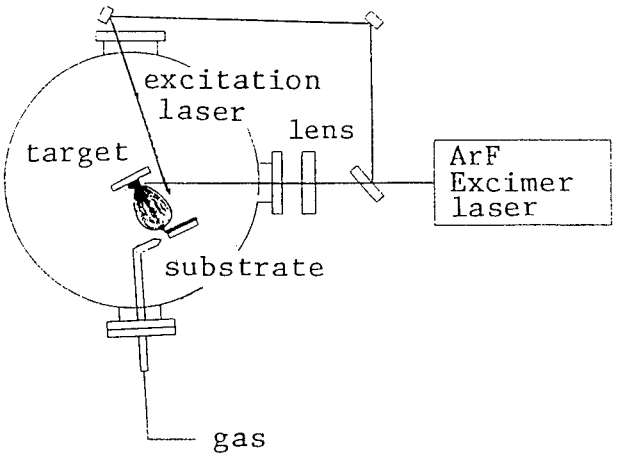
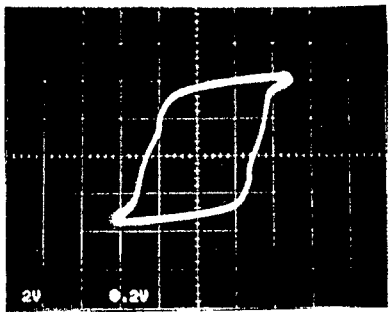


Fig.1 Laser ablation system



$PbTiO_3$ film

46 μ C/cm^{2}div

190kV/cmdiv

Fig.2 D-E hysteresis curve of the $PbTiO_3$ thin film

deposition utilizing the lattice mismatch between the substrate and the film to enhance the c axis orientation. Second laser irradiation during the film formation with delay time of 6 μ sec also enhances the crystallinity and assists the low temperature formation of the films.

3. Molecular layer control of dielectric strained superlattices

As shown in Fig.3, the strained superlattice is formed by the stacking of SrTiO3 and BaTiO3 layers which have different lattice constants. This superlattice shows high dielectric constant at the short stacking periodicity of each layer. It is noticeable that the $(Sr_{0.3}Ba_{0.7})TiO_3/(Ca_{0.3}Sr_{0.7})TiO_3$ strained superlattice exhibits the dielectric constant of 900 even for the film thickness of 500A. This result indicates that the strained superlattice approach is one of the promising ways for the fabrication of ultra-high density DRAM.

4. Atomic layer control of high Tc oxide thin films

High Tc superconductors have been fabricated by atomic layer deposition method to create new superconductors using the laser MBE method shown in Fig.4. RHEED and STM are used for the control of the growth of atomic layers, and superconducting Ba-Ca-Cu-O as well as Au-Ba-Cu-O artificial superlattices have been synthesized for the first time.

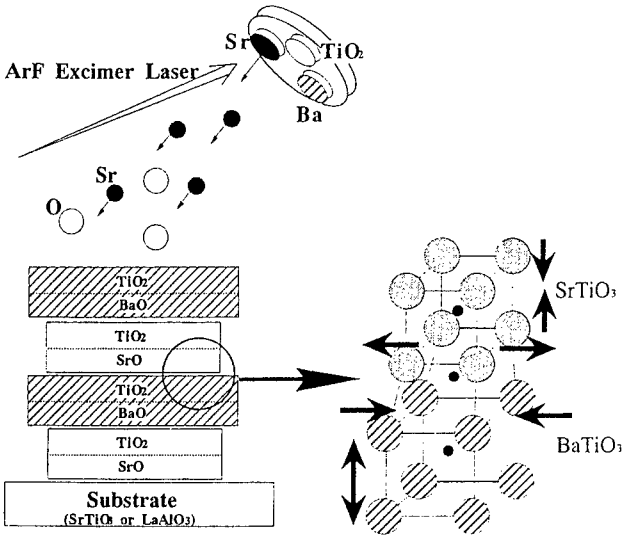


Fig.3 Schematic diagram for the formation of $SrTiO_3/BaTiO_3$ strained superlattices

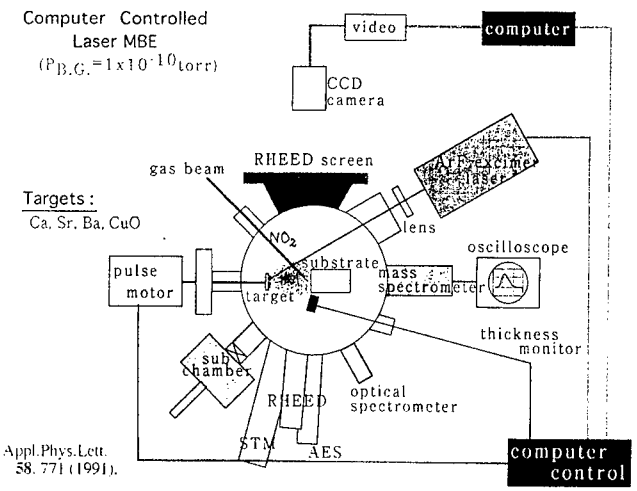


Fig.4 Laser MBE apparatus

9:15am - 9:45am
MA2

Epitaxial growing of refractory metal films by laser ablation deposition

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Thin films of refractory metals have been widely acknowledged as a prospective material for "traditional" microelectronics. Recently new exciting area for applications of metallic films has arisen in the field of mesoscopic physics. The development of the fabrication of ballistic metallic mesoscopic device needs one to grow thin films with high electron mobility. This application requires thin films of advanced properties. First, the films should be of high purity and perfect crystalline and surface structure to provide long electron mean free path. Second, they should have low electromigration rate up to high current densities. Such structures should also have perfect interfaces, since their composition significantly affects the electron transport properties. In this report we present the results of investigation of electrical properties, as well as structure of thin Tungsten and Niobium films, grown under ultra high vacuum (UHV) by laser ablation deposition on R-plane sapphire substrate and, for comparison, on (100) plane of GaAs and InP, the latter having been treated by H-ECR plasma to achieve atomic clean near stoihiometric surface, followed by metallic film deposition without cutting of high vacuum.

Experimental setup. The optical system consists of the pulse Q-switch solid-state ($AY:Nd^{3+}$) laser with the pulse duration of 15 ns, the repetition of 20 Hz, with the wavelength of 1.079 μm. It also includes the photometers to measure the mean laser radiation power and the energy per laser pulse, the light filters and the focusing lens. The target is placed on the rotating holder in the UHV backing chamber. The temperature of the specimen table in the range of 20-900 °C is controlled by thermocouple. The films were deposited onto [$\bar{1}$012] sapphire single crystal substrate at mean deposition rate of 10 nm/min. Conventional electrical measurements from room- to He-temperatures as well as RHEED measurements are ex situ carried out for investigation of grown films with thickness of 10-150 nm.

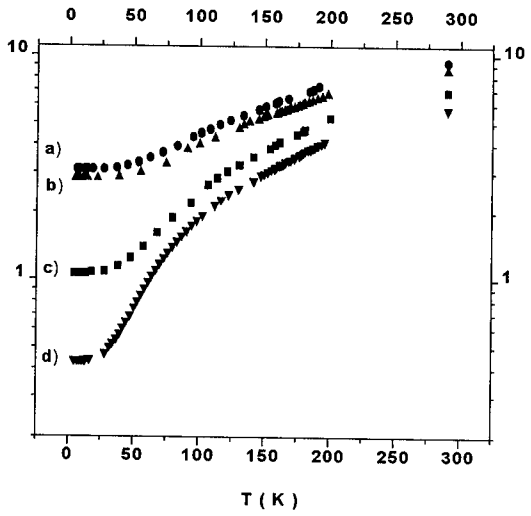


Fig. 1

Temperature dependence of film resistivity. The temperature dependence of electrical resistivity (μΩ cm) of Tungsten films, deposed at substrate temperature T_s=300°C on (100) plane of GaAs (a) and InP (b), and on sapphire R-plane - (c), T_s=300°C and (d), T_s=700°C are shown in Fig.1. The thickness of the films is in 60-70 nm range. Also room temperature film resistivities coincide each other within 50%, the residual ones differ drastically. It is defined by concentrationof "static" defects and depends on film quality. RHEED measurements show that film (d) corresponds to high quality monocrystalline epitaxial film. The films (a,b) have lower structural and electrical properties, as expected, since (001) plane of GaAs and InP has not suitable lattice parameters for epitaxial growth of Tungsten.

Temperature range of epitaxial growth. Fig. 2 shows the dependence of residual resistance ratio (RRR), which is used as film quality parameter, versus substrate temperature, at which the films are grown for Tungsten (a) and Niobium (b) films on R-plane of sapphire substrate.

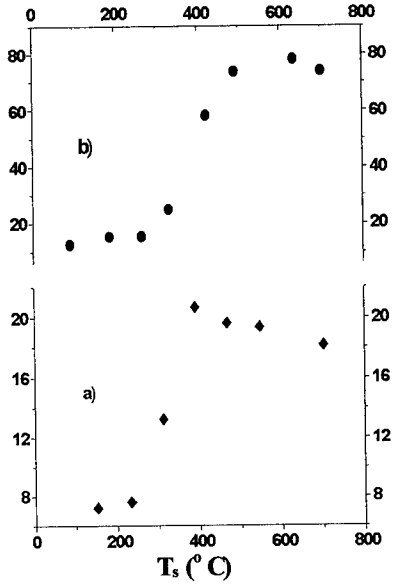


Fig. 2

This dependence has sharp inflection at T_s=350°C and 400°C respectively for W and Nb, with increasing of RRR values in 3-4 times. It is accomplishing with magnifying of intensities of monocrystalline streaks, as well as Kikuchi lines on RHEED patterns. Since room temperature resistivity of the films varies slowly and coincides the bulk monocrystal value within experimental accuracy, such dependence of RRR is defined by conducting electron scattering on "static" defects. At higher film growth temperature the concentration of the defects diminishes, resulting to the growth of high quality epitaxial films with [001] axis perpendicular to R-plane and [111] axis parallel to C-axis of substrate. At lower growth temperatures both perfect epitaxial and imperfect "bulk" phase are exist. Nevertheless the monocrystalline phase survives up to T_s=100°C.

Classical size effect. The dependence of RRR on film thickness is presented in Fig. 3 for Tungsten (a) and Niobium (b) films. It shows classical size effect dependence, according to Fuchs's theory. The fitting curves are also presented in Fig. 3. The bulk residual electron mean free paths defined by fitting of experimental results are equal to about 2 μm for Nb and 100 μm for W and significantly exceeds the film thickness. The main channel of conducting electron scattering, as have been found, is defined by surface scattering. The electron transport in these films is ballistic one at liquid He-temperatures. The found RRR values for the refractory metal films, grown at high substrate temperature, correspond to record meanings in investigated film range.

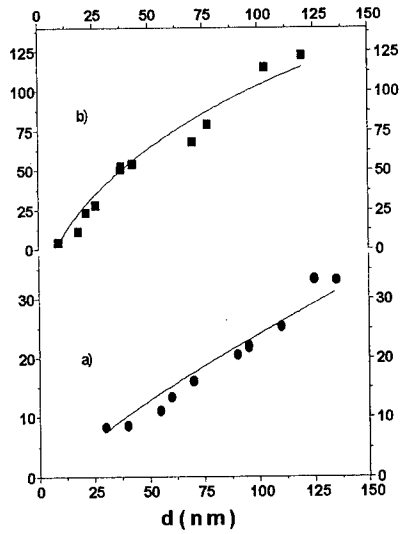


Fig. 3

Conclusion. High quality epitaxial films, grown by laser ablation deposition on R-plane of sapphire substrate under UHV condition possess high electrical properties, as well as we know, exceeding those of the films, grown by other conventional methods in investigated thickness and growth temperature ranges, due to, we believe, application more energetic metallic particles during film deposition.

9:45am - 10:15am
MA3

Fabrication of Silicon Solar Cells by Laser Processing

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Solar cells became important as the alternative energy source recently. In the present work we fabricated silicon solar cells using a laser processing technique. The goal here was to examine how laser processing can possibly be used for such an application. As the first attempt we tried to fabricate solar cells by the simplest method possible.

Among a variety of laser processing techniques that are available for the preset application, we chose pulsed laser deposition (PLD). Using PLD, we deposited thin n-Si layers on p-Si wafers, and successfully formed the p-n junction that is essential for the photovoltaic effect. Indeed, this was the simplest way to fabricate Si solar cells by any laser processing technique.

PLD is currently under intense investigations to deposit such interesting films as high-temperature superconductor films and dielectric films. PLD becomes particularly useful for deposition of the complex multicomponent materials owing to the compositional fidelity between target materials and deposited films. However, at the same time we succeeded to produce interesting single-component films such as diamond-like carbon films[1] and amorphous Si films.[2]

To deposit crystalline Si films, we kept the p-Si wafer at 800℃ during the

deposition of n-Si films. The crystalline state of the n-Si films was examined by reflection high energy electron diffraction (RHEED). A close relation existed between the RHEED pattern of the deposited n-Si layers and the photovoltaic power generated by the solar cells.

The target used for PLD was P-doped Si. The electrical resistivity of the films reproduced that of the target. Therefore, the compositional fidelity worked favorably in the present PLD work. In order to suppress the particles mixed into the films, we used a short-wavelength ArF laser (193 nm). The oxidation of the films was troublesome in Si PLD. Therefore, we set the base pressure of the deposition chamber in a range of 10^{-9} Torr. The low level of oxygen in the films was confirmed by secondary ion mass spectroscope (SIMS). The comb-type Ti electrode was fabricated on n-Si surfaces, while the back side of the cell was coated with Al layers. The detail of the present experiment will be published elsewhere.

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10:45am - 11:15am
MA4

Laser Desorption of NO and CO from Sodium Nitrate and Calcium Carbonate Crystals

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Summary: Pulsed laser irradiation of solid samples produces plumes of gaseous material suitable for mass or chemical analysis. The combination of laser desorption with various mass spectrometry techniques offers a method by which solid micro samples may be analyzed for elemental and chemical composition. Such techniques are being developed to characterize a variety of solid samples including soil, and hazardous mixed wastes. It is clear that the laser desorption analysis of mixed wastes involving molecular ionic compounds requires a detailed knowledge of the desorption properties of these components [1]. Sodium nitrate ($NaNO_3$) and Calcium carbonate ($CaCO_3$) are of particular interest since each is a component in waste storage tanks at the Hanford nuclear reservation and a constituent of the earth's subsurface. In an attempt to develop laser desorption as an analysis tool, we have studied pulsed UV laser desorption from crystalline $NaNO_3$ and the calcite form of $CaCO_3$.

Sample crystals were cleaved and mounted in an ultra high vacuum (UHV) chamber (base pressure 10^{-10} torr) equipped with quadrupole (QMS) and time-of-flight (TOF) mass spectrometers. The cleaved crystals were excited using 5-ns pulses of the 213-nm Nd:YAG fifth harmonic or 193 nm excimer laser radiation incident on the sample at 40° to the crystal face at laser irradiances of < 2 MW/cm^2. In this low irradiance regime, desorption yields are small and secondary interactions of desorbed particles are rare. A more complete description of the sample preparation and experimental apparatus can be found in reference [2]. Following excitation, neutral NO or CO fragments were detected by either (1+1) or (2+1) resonance enhanced multiphoton ionization (REMPI), respectively, which employs a delayed probe laser aligned parallel to the crystal surface and directed within the desorption plume. The positive ions produced via REMPI are detected using the TOF mass spectrometer to determine the relative NO and CO product state populations. For laser desorption from $NaNO_3$, the relative NO rotational and vibrational populations were determined from the intensity of the NO P_{12} bandhead of the (0, 0), (1, 1), (2, 2), (2, 3), and (3, 4) vibronic A $\leftarrow$ X transitions. For the detection of CO we used a (2+1) REMPI scheme involving two-photon excitation of the $B^1\Sigma \leftarrow\leftarrow X^1\Sigma$ transition followed by one photon ionization from the B-state to the ion ground electronic state [3]. The (2+1) spectrum is characterized by a strong Q-band obtained over a relatively narrow frequency range ~ 20 cm^{-1}. Subsequent analysis of the rotational Q-branch then affords insight into the product state distribution and mechanisms of the photochemical processes [4]. We have recently recorded the partially resolved Q-band of the neutral CO products desorbed from $CaCO_3$ following pulsed UV excitation using REMPI through the B-state.

Figure 1 displays the neutral NO rotational distribution obtained using resonance enhanced multiphoton ionization following 213-nm irradiation of $NaNO_3$. State distributions obtained from this and other data (not shown) indicate that the NO rotational distributions are in thermal equilibrium with the sample, while the vibrational state distribution is hyperthermal. The relative vibrational distribution for the v_0:v_1:v_2:v_3:v_4 levels is 1:0.43:0.28:0.32:0.15 respectively, which is not consistent with a Boltzmann distribution, but rather with a non-thermal and highly excited vibrational distribution. The NO velocity distribution is well fit by a half-range Maxwell-Boltzmann distribution function [5] yielding a translational temperature of 250 ± 40 K, in thermal equilibrium with the surface. A similar analysis of the NO rotational spectrum yields a rotational temperature of 270 ± 50 K. Data obtained at higher surface temperatures indicates that the rotational temperature of the desorbing NO tracks with the surface temperature.

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(b) Associated Western Universities Postdoctoral Fellow
(b) Associated Western Universities Senior Research Fellow

Figure 2 displays the neutral CO rotational distribution obtained using (2+1) REMPI following 193-nm irradiation of $CaCO_3$. Preliminary analysis indicates that the CO rotational distributions are again in thermal equilibrium with the sample, while the vibrational state distribution is somewhat hyperthermal. The relative vibrational distribution for the v_0:v_1 levels is 1.0:0.05 which is consistent with a vibrational temperature of approximately 1000K. A Boltzmann analysis of the CO rotational spectrum displayed in Figure 2 yields a rotational temperature of 300±30 K. We are presently completing detailed studies of the CO product state distributions following UV excitation of calcite.

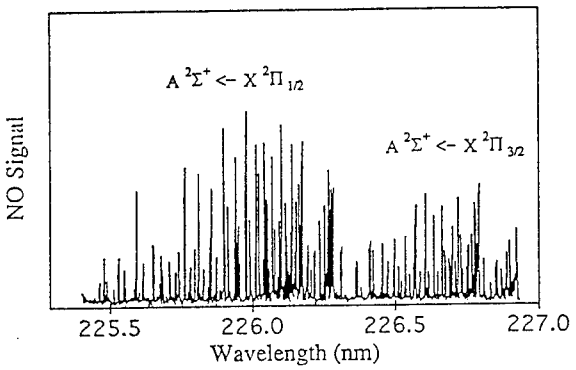


Figure 1. The NO rotational spectra obtained using REMPI following 213-nm excitation of $NaNO_3$. Spectrum (a) displays the full rotational distribution of the (0,0) $A\,^2\Sigma^+ \leftarrow X\,^2\Pi_{3/2,1/2}$ transition. Boltzmann analysis of yields a rotational temperature of 270 ± 50 K.

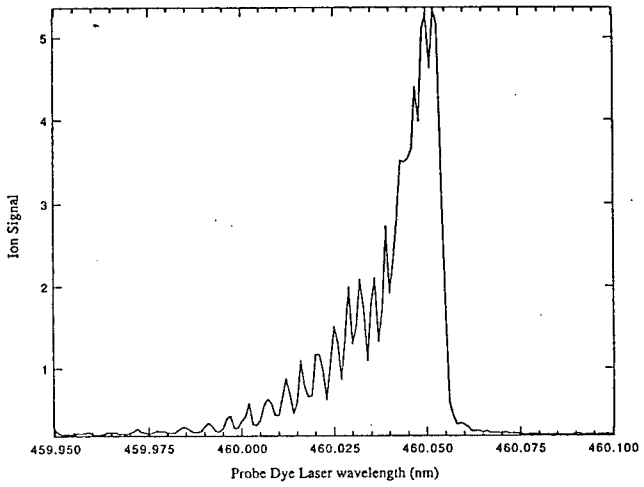


Figure 2. Partially resolved Q-branch B←←X spectrum of desorbed CO following 193 nm laser excitation of calcium carbonate. The (2+1) REMPI scheme contains the entire Q-branch within a narrow frequency range of only 20 cm^{-1}. Wavelengths shown are of the dye fundamental which is subsequently doubled to ~ 230 nm.

Acknowledgment:
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11:15am - 11:45am
MA5

LASER ASSISTED DEPOSITION OF MERCURY CHALCOGENIDES THIN FILMS IN CHEMICALLY REACTIVE ENVIRONMENT

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The results of the experimental study of major physico-technological considerations of formation of the thin films structure and elemental composition at laser vaporization and deposition of thin CdHgTe and MnHgTe films on the substrate in chemically reactive environment are presented in this paper.

The laser vaporization and condensation took place in the mercury vapour ($P = 10^{-1} - 10^{3}$ Torr). The presynthesized CdTe-Te(MnTe-Te) or Te plates were used as targets. The laser with τ=50-100 ns generation pulse duration, density of vaporization pulse power $q = 10^{8} - 10^{9}$ W/cm^2 was used for vaporization of the target material.

The experimental data obtained testified to the mercury atoms ionisation by highly energetic Te ions. When the ionisation multiplicity increased the atom luminance time ecreased with the simultaneous displacement of its intensity maximum towards the evaporation pulse origin. The maximum displacement was, perhaps, due to the increase of the ionised atoms velocity, when ionisation multiplicity increased. The duration and intensity of the Te atoms radiation in the mercury vapour increased considerably, when the mercury vapour pressure increased, reaching the maximum at P ~10 Torr.

The increase of the mercury vapour pressure (P >10 Torr) caused the deceleration of the plasma of the luminance intensity growth at the instant of the laser pulse action end stimulated by absorption of laser radiation by a shock wave. The subsequent increase of the mercury vapour pressure (P >100 Torr) caused the avalanche optic breakdown in the neighbourhood of a target.

As a result of the above, the mercury vapour luminance intensity increased abruptly with simultaneous decrease of the target evaporated substance luminance intensity. The mercury vapour pressure increase in the volume causes the decrease of the length of the particle free run and, respectively, the decrease of their kinetic energy. Besides, the atoms and ions of more light Cd and Te meet with the most distinctive retardation.

The observed particle velocity increase at the (l ~1 cm) distance from the target surface can be caused by the character of gas-dynamic substrate spread under the conditions of a plasma shock wave and redistribution of the particle energy because of their intensive collision. The study of the synthesis process and film structure formation, deposited in reactive space in the volatile component vapour revealed the increased reactivity of laser plasma. Besides, when the target evaporated from a pure chalcogene (Se,Te) the films of HgSe, HgTe, respectively, always form on the orienting substrates KBr, KCl, NaCl already at $P > 5 \cdot 10^{-3}$ Torr in the mercury vapour. And when CdTe-Te (MnTe -Te) evaporate the CdHgTe (MnHgTe) homogeneous films of the corresponding composition form.

Excitation and ionisation of the mercury vapour by highly energetic ions of the target material make the major consideration, determining the high reactivity of laser plasma. This stimulates formation of molecular complex in reactive space, influencing the formation of the condensate elemental composition.

On the other hand, the intrusion ofthe mercury ions in the nearsurface layer of a plate at a depth up to 0,5-1 μm takes place at irradiation of the CdTe plate by laser radiation pulses in the mercury vapour with light flux density, sufficient for the surface melting. Since the process of laser vaporization of the absorbing targets is realised, as a rule, through a liquid phase, then the target vaporization in the mercury vapour takes place from a layer saturated by Hg to a certain degree. This also can determine the relation of the condensate components.

Hence, the mechanism of formation of the films of binary and triple Hg compounds at the target vaporization in the vapour of a lacking or fully absent component (Hg) is of a complex nature. Depending on the Hg vapour pressure in the chamber the radiation of the compound formation can take place (or is dominating) at the target surface ($P > 10^{-1}$ Torr) or during the process of transition and condensation of vapour on the substrate ($P < 10^{-1}$ Torr). Ionisation and excitation of Te and Hg atoms, besides, the Hg implantation in the irradiated target are defining here.

4:30pm - 5:15pm (Invited)
MB1

Dynamics of Pulsed Laser Ablation for Thin Film Growth

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Fast imaging and sensitive spectroscopic investigations of laser ablation plume propagation reveal fundamental collisional phenomena relevant to film growth by pulsed laser deposition and optimized cluster growth via laser vaporization. Two phenomena will be described. The first involves the splitting of the ablation plume into distinct high and low energy components as a weak shock front forms during ablation into a low-density background gas. The second involves the dynamics of graphite ablation for vacuum deposition of tetrahedrally coordinated amorphous diamond films.

Spatially- and temporally-resolved (~0.1 mm, ~5 ns) plasma diagnostic techniques of optical emission spectroscopy, optical absorption spectroscopy, fast Langmuir probe analysis, and gated-ICCD fast photography are combined to provide a more complete picture of the laser ablation plume initiation and propagation. Spectroscopic imaging was performed using a tunable liquid crystal filter with 5 nm bandwidth across a 400–720 nm wavelength range. Gated photon counting spectroscopy was employed to explore extremely weak plasma luminescence following the propagation of the initial ablation plume in vacuum and during the 'rebound' of the plume with a substrate during pulsed laser deposition of amorphous diamond.

Ex situ film analyses have shown that ArF-laser (193-nm) irradiation produces higher quality amorphous diamond films than does KrF (248-nm) laser irradiation of pyrolytic graphite in vacuum. Three principal regions of plume emission have been characterized: (1) a bright luminescent ball (v ~3–5 cm/μs) displaying nearly entirely C^+ emission which appears to result from laser interaction with the initial ejecta, (2) a spherical ball of emission (v ~1 cm/μs) displaying neutral carbon atomic emission lines and, at early times, jets of excited C_2, and (3) a well-defined region of broadband emission (v ~0.3 cm/μs) near the target surface first containing emission bands from C_2, then weak continuum emission from C_3 and possibly higher clusters and/or blackbody emission from hot clusters or nanoparticles. The evolution of these three regions is shown in Fig. 1. Diamond-like film quality correlates directly with the presence of the high-velocity ion ball and minimization of the cluster emission at the target surface.

Addition of background gases strongly enhances the third (cluster) component, in accordance with plume-splitting phenomena, a general effect which will be described for several materials. As shown in Fig. 2, during expansion into low-pressure background gases the ion flux in laser ablation plasma plumes is generally observed to split into distinct "fast" and "slow" components. The fast component is target material which penetrates the background gas in accordance with a scattering model, while the slow component is material which has undergone momentum-changing collisions with the background gas, or with other plume atoms. When the multicomponent graphite plume of Fig. 1 encounters low-pressure argon several collisional overlap regions between plume atoms are created, as shown in Fig. 2(b), which leads to additional clustering near the target surface.

The combination of sensitive imaging and photon-counting diagnostic techniques permit an understanding of the importance of gas dynamic effects on the time-of-flight distributions of species arriving during the deposition of thin films in both vacuum and background gases.

This research was sponsored by the Oak Ridge National Laboratory, managed by Lockheed Martin Energy Research Corp. for the U.S. Department of Energy under contract number DE-AC05-96OR22464

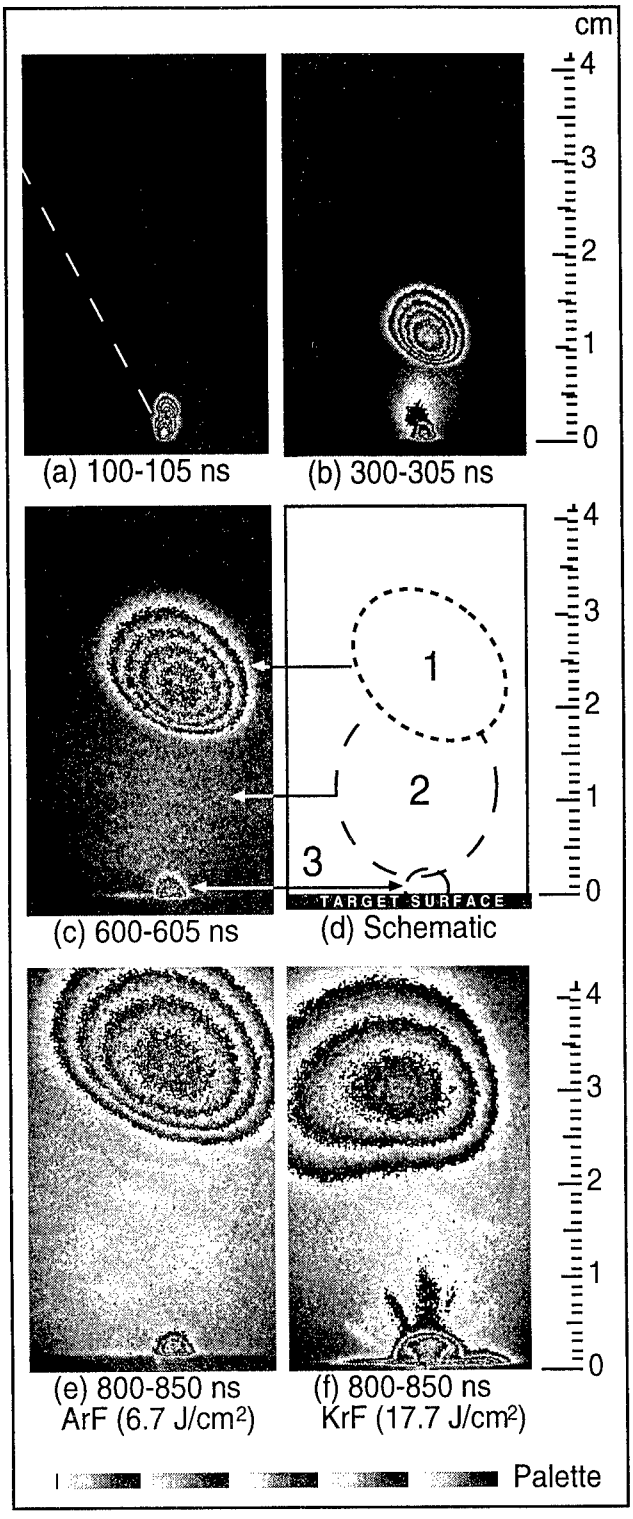


Fig. 1. Gated-ICCD photographs of the total visible luminescence at the indicated times following ablation of pyrolytic graphite in vacuum using (a), (b), (c), (e) ArF-laser (6.7 J/cm^2) and (f) KrF-laser (17.7 J/cm^2) irradiation (incident angle 30° from the left). The 5-grayscale palette (bottom) is normalized to the maximum numbers of counts for each image. (d) Schematic indicating the different luminescent plume components discovered by ICCD-imaging (see text).

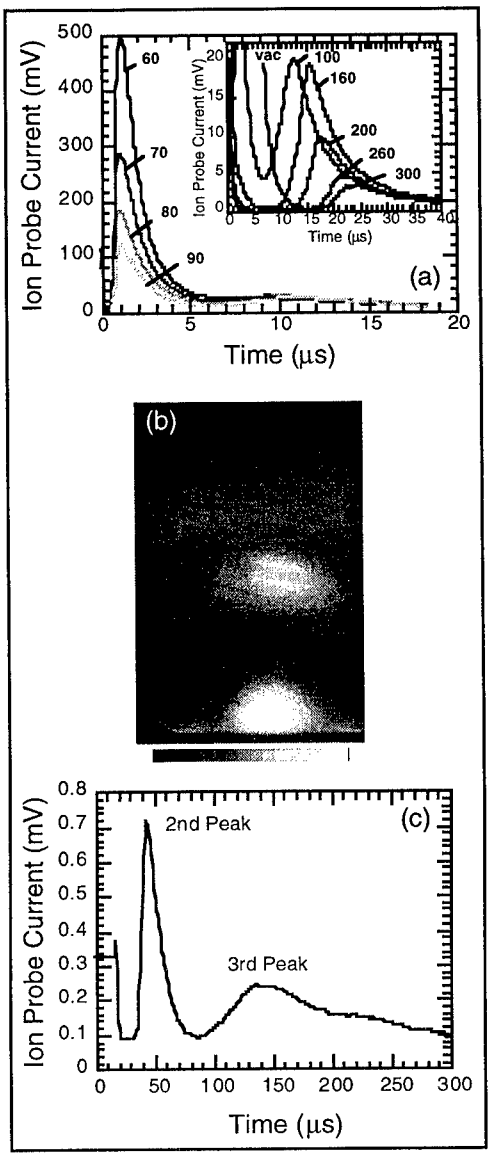


Fig. 2 (a) Ion probe current (mV into 50 Ω) induced by the ArF-laser (6.7 J/cm^2) generated plasma at d = 5 cm along the normal to the graphite target into 60, 70, 80 and 90 mTorr of Ar. In addition to the dominant fast component of the ion flux, a second component is observable at delays of ~10 μs. The insert shows the disappearance of the fast component and the evolution of the second component for vacuum (7×10^{-7} Torr) and argon pressures of 100, 160, 200, 260, and 300 mTorr. (b) ICCD image of luminescence (unfiltered) from the ArF-laser (6.0 J/cm^2) generated carbon plasma propagating into 70 mTorr of argon (2.1 μs delay, 0.2 μs exposure). The grayscale palette used is shown. (c) Ion current versus time after laser pulse in 350 mTorr of Ar.

5:15pm - 5:45pm
MB2

DIAGNOSTICS OF GROWTH AND FILM PROPERTIES OF AMORPHOUS SILICON

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High quality amorphous hydrogenated silicon (a-Si:H) films were deposited by pulsed VUV F_2 laser CVD (157nm) allowing the digital control of the deposition process. The photodeposition was performed in a parallel configuration with an average power of 4W at a repetition rate of 50Hz. The source gas was disilane. Nucleation and growth on native oxide-covered Si(100) and on hydrogen-terminated Si(111) surfaces were studied *in situ* by FTIR transmission spectroscopy with submonolayer sensitivity. The film thickness was monitored simultaneously using a quartz crystal microbalance with comparable resolution in the case of the oxide-covered silicon surface.

The *in situ* spectra reveal that the nature of the substrate surface significantly influences the hydrogen bonding configuration in the interface region. For both surfaces the assumed cluster growth during the initial stage is characterized by a band around 2100cm^{-1}, which is assigned to SiH_x (x=1-3) surface modes. This band broadens until the clusters coalesce and band saturation occurs. At this time a second band starts to grow at 2000cm^{-1}, which is attributed to bulk SiH bonds. Difference spectra calculated for layers at different depths with definite thickness and deconvolution of the broad feature observed during the very first stage of film growth indicate the existence of a hydrogen rich layer at the substrate surface, whose composition and thickness depends on the nature of the substrate surface. The IR spectra reveal that the hydrogen is mainly bonded as dihydride within the first 20Å of growth on the smoother H-terminated surface, whereas on the rougher oxidized surface also trihydride species can be observed.

The growth of a-Si:H can be divided into three phases.The first is nucleation with growth of clusters, which may be disk shaped on the H-terminated surface. A hydrogen content of up to 50 at-% may be reached in the about 20Å thick transition layer. The point of coalescence strongly depends on the nature of the substrate surface. The second stage is bulk growth, with decreasing hydrogen content. The substrate is still affecting the bonding configuration. Finally, homogeneous film formation with 8-10 at-% hydrogen takes place.

The material obtained by laser CVD is comparable to high quality plasma CVD films deposited under similar conditions. This is demonstrated by the values measured for the electronic properties such as the Urbach energy, Tauc gap, defect density, photoconductivity and dark conductivity. For the first time the density and elastic constants have been determined for such films.

The mechanical and elastic properties of the a-Si:H films were measured by broadband surface acoustic wave spectroscopy (SAWS). In this technique ns-ps Nd:YAG laser pulses (355nm) are used to excite broadband surface acoustic wave pulses, and a cw Nd:YAG laser (532nm) or piezoelectric foil detector is employed for time resolved detection of the resulting surface displacements. Fourier transformation of the resulting oscillatory signal detected at distances of several millimeters to centimeters from the source yields the dispersion of the phase velocity.

In the frequency range achieved in these experiments, the SAW dispersion curves extend to 300MHz, which allowed the density, Young's modulus, and Poison's ratio to be determined for the films grown by laser CVD with different hydrogen concentrations. The films had the best mechanical and elastic properties at a hydrogen concentration of about 10 at-%, where also the best electronic properties are found. For this material, a density of 2300kg/m^3 (silicon: 2329kg/m^3) and a Young's modulus of 134GPa (average value for crystalline silicon: 160GPa) was obtained. The mean coordination number of the amorphous network structures has been estimated by applying the constraint-counting model. The mean coordination numbers determined from the Young's moduli approach those calculated for an ideal hydrogenated silicon network near the hydrogen content of 10 at-%.

Ion-implanted silicon wafers were examined by SAW, Rutherford backscattering spectrometry (RBS), and TRIM (Transport of ions in matter) simulations. If the topmost layer is completely amorphized, ist thickness can be determined by all three methods. The SAW technique allows furthermore the determination of the density and two elastic constants from the strong nonlinear dispersion. The thickness measurements by SAWs, as compared to RBS, lead to about ten per cent higher values. We found that the Young's modulus in the amorphized region cannot be reduced below about 120GPa with argon ions. The Poisson's ratio possesses nearly crystalline values and the density is a few per cent lower than the crystalline counterpart.

6:00pm - 6:30pm
MB3

ACOUSTIC WAVE MONITORING IN PULSED LASER INTERACTION WITH MATERIALS

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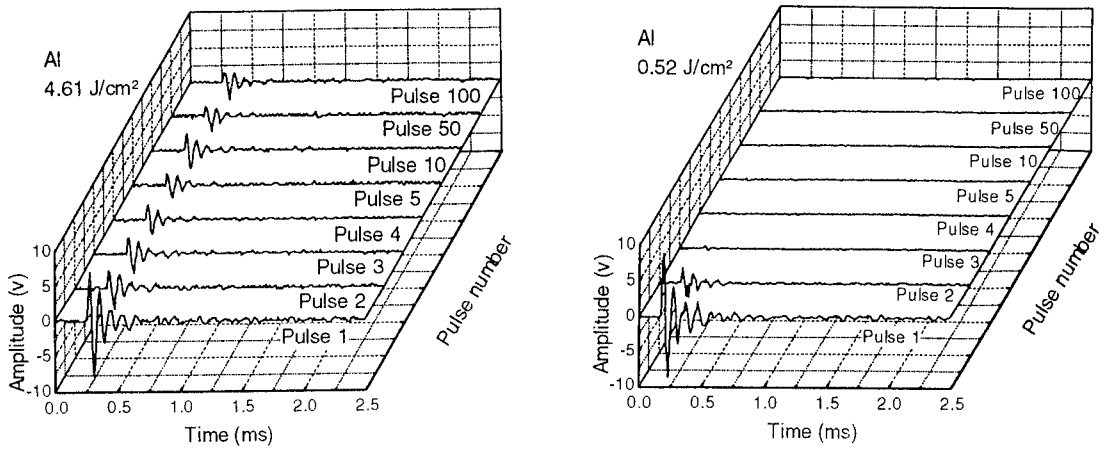
Pulsed excimer lasers have been proven very useful in material processing, such as laser ablation of materials and the cleaning of material surfaces. It is desirable to introduce a suitable real-time monitoring probe to control the laser processing. The optoacoustic effect, the generation of acoustic waves by the absorption of laser radiation, has been widely applied as a monitoring method in laser applications. However, these efforts are concentrated on the detection of the ultrasonic waves which requires expensive equipment. In this article, audible acoustic waves generated during laser interaction with materials will be studied, to monitor the interaction and to reflect the nature of interaction such as laser ablation and surface cleaning. The spectral analysis method, fast Fourier transform (FFT), was used to study the acoustic wave generation and to establish relationship between the acoustic waves and laser ablation rate or cleaning efficiency.

A KrF excimer laser (Lambda Physik LPX100) is used as the light source. The laser beam has a wavelength of 248 nm and a pulse duration of around 20 ns. The laser fluence applied in the experiment is set in a range of 0.1 to 20 J/cm^2. The sample to be processed is placed in air with its surface perpendicular to the incident laser beam. A wide-band microphone Sony ECM-23F3, with a bandwidth from 20 to 20 kHz, is used to detect the acoustic wave generated. The position of the microphone can be adjusted to investigate the acoustic wave spectra change. The synchronous output of the laser controller is sent into a digital oscilloscope as a trigger signal for the acoustic wave detection. The acoustic wave spectra recorded are displayed, digitized by the oscilloscope and sent to a PC through an IEEE-488 interface card for data storage and further processing.

Figures 1a and 1b show the acoustic waveforms generated during laser irradiation on Al surface at laser fluences of 0.52 and 4.61 J/cm^2 respectively. The waveforms are recorded at the 1st, 2nd, 3rd, 4th, 5th, 10th, 50th and 100th pulse of laser irradiation. Since the ablation threshold of Al under KrF excimer laser irradiation is around 1.3 J/cm^2, Fig. 1a corresponds to laser surface cleaning without ablation while Fig. 1b corresponds to the case of laser ablation. It can be observed from Fig. 1a that as the pulse number increases, the acoustic waves gradually reduce and finally disappear. This represents the Al surface being cleaned by excimer laser. Only 10 pulses of laser irradiation are enough to clean the surface completely. In our previous study, the variation of acoustic waves has been proven to be related to the change of contamination level on the surfaces. Therefore, this detection can be used to monitor the cleaning process in real-time. When the laser fluence increases up to the Al ablation threshold, material removal begins to occur on Al surface under laser irradiation. In Fig. 1b, as the pulse number increasing, the acoustic wave gradually decreases to a stable waveform after about 10 pulses of laser irradiation. This is due to simultaneous laser cleaning and ablation. After about 10 pulses, the contaminants on the surface have been completely

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cleaned and only laser ablation exists on the Al substrate surface. Therefore, the waveform becomes stable and does not change with further pulses. It is obvious that the acoustic wave detected at a high pulse number, such as 100th pulse of laser irradiation, can be used to represent the laser ablation. Therefore, acoustic wave can also be used to monitor the laser ablation in real-time.



(a) (b)

Fig. 1 Acoustic waveforms generated during excimer laser irradiation on Al surfaces at fluences of (a) 0.52 and (b) 4.61 J/cm^2

The first peak-to-peak amplitudes in the waveforms have been observed as a function of pulse number at two laser fluences of 0.52 and 4.61 J/cm^2 irradiating on Al surfaces. In both cases, the amplitude drops drastically at the first a few pulses and reaches a constant level within ten pulses. When the fluence is of 0.52 J/cm^2 below the ablation threshold, the constant level is zero. When the fluence increases to a value of 4.61 J/cm^2 above the ablation threshold, the constant level is larger than zero. We name this constant level as bulk response because it does not depend on surface condition. Obviously, the bulk response can be a clear criteria of laser ablation.

In a laser-based manufacturing process, the complete analysis of the whole waveform is inefficient due to time constraint. Therefore, characteristic parameters, such as first peak-to-peak amplitude, must be extracted from the signal. The variation of the parameters can be used as a feedback signal to control the process in real-time. According to the variation of the amplitude Y with laser pulse number N, a model can be established as:

$$Y = P1 + P2 \times Exp(-N \times P3) \qquad (1)$$

where $P1$, $P2$ and $P3$ are three characteristic parameters. $P1$ is defined as bulk response as discussed above. P2 and P3 have the physical meanings of surface response and pulse dependence. A few examples are listed in Table 1 for different laser parameters.

There are five important mechanisms responsible for the acoustic wave generation: dielectric breakdown, electrostriction, radiation pressure, thermoelastic process, and material ablation. Their attribution is related to the laser parameters, material optical and thermal characteristics. From the results of analyses, the generation of audible acoustic waves is only attributed to laser ablation.

6:30pm - 7:00pm
MB4

PHOTOLUMINESCENCE AND X-RAY ANALYSIS OF LASER DEPOSITED II-VI THIN FILMS AND MULTILAYERED STRUCTURES

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V. Capozzi, G.Perna, G.Lorusso - Dipartimento di Fisica and Unita' INFM dell'Università di Bari via Amendola173, I-70100 Bari (Italy)
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Summary

Highly structured buffer layers are of fundamental importance in multilayer depositions if superlattices or quantum wells are to be grown on a substrate. Nowadays, MBE and MOCVD are the conventional technique for growing multilayers but very recently pulsed laser ablation and deposition (PLAD) was shown to be an up to date method for depositing heterostructures[1]. Among the others, II-VI materials are promising for producing films showing high luminescence efficiency[2]. This work aims to determine the best buffer layer for the deposition of II-VI heterostructures on silicon. Here the results obtained from laser ablated films (1μm thick) of CdSe, CdS and CdTe at different substrate temperatures are presented. A Nd:Yag laser (λ=532nm) was used to ablate and deposit II-VI compounds in a vacuum chamber pumped down to 10^{-6} Torr.

X-ray spectra were collected by a conventional θ–2θ diffractometer and grain dimensions were calculated accordingly to Debye Sherrer formula.

Photoluminescence (PL) experiments were carried out to study radiative transition and emission efficiency of laser ablated films of CdSe, CdS and CdTe.

PL spectra were measured from 10 to 300K at low photoexcitation intensity, (about 10 Wcm^{-1}) by using the 514 nm and 458 nm lines of an Ar-ion laser.

PL efficiency of CdSe ablated films is strongly dependent on the substrate temperature. Best results were obtained for CdS and CdSe films deposited on Si(111) at 400 °C . Exciton line of type χ_A are resolved either in CdTe or in CdSe films. A detailed study of linewidth and spectral position of the exciton line versus temperature T was studied . Broad PL bands due to extrinsic luminescence are present both in CdS and CdSe films. This PL feature is related to impurity levels localized in the energy gaps of the films. Recombination of donor acceptor pairs are present and they are studied as fuction of T and laser power. Preliminary results of CdTe/CdSe multilayers deposited on Si(111) also by PLAD will be shown.

References.

[1] A. Giardini, M. Ambrico, D. Smaldone, R. Martino, V. Capozzi, G. Perna, G.F. Lorusso in press on Appl. Surf. Sci.

[2] W. Shen and H.S. Kwok: Appl. Phys. Lett. 65, p.2162 (1994)

ADVANCED APPLICATIONS OF LASERS IN MATERIALS AND PROCESSING

Tuesday, August 6, 1996

SESSIONS:

TuA: Processing

TuB: Fabrication

8:30am - 9:15am (Invited)
TuA1

ADVANCED LASER PROCESSING OF METALS

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Abstract

The application of lasers span the entire commercial and industrial scene starting from the CD player at home to welding in automobile and aircraft plants. The CD player uses tiny ($\approx$ mm) diode lasers, whereas 5 kW to 45 kW CO_2 laser used in industrial welding application have footprints of tens of square meters. Processes such as welding and cutting of components in order of meters, drilling dimensions of mm to μms are widely accepted in manufacturing floor. Heat treatment is closely behind. The future application in manufacturing include: nano-meter size powder generation by laser ablation; Angstrom to micron size deposition by Laser Chemical Vapor Deposition (LCVD); mm scale coating by laser cladding; and surface modification and meter scale components by direct metal deposition. The laser is a tool which can provide energy density varying from 10^{-3} watts/cm^2 to 10^{12} watts/cm^2. They have a wavelength range varying from UV ($\approx$193 nm) to far infrared (10.6 μm). Recently, high brightness lasers has created new excitement for laser processing community. This inertialess tool of optical energy has the potential of starting a new era the way steam energy started the industrial revolution in the 19th century

The preferred approach for successful process development is to apply "atomic level understanding to applications". This paper discusses the science base for many of the important laser processing techniques. Emission, absorption and Laser Induced Fluorescence(LIF) spectroscopy have been applied for studying interaction physics whereas transport models are used for quantitative understanding of effects of process parameters on the materials. Electron optical techniques are applied to characterize the processed materials and whenever possible effort has been made to establish structure-property-process-parameters relationship.

PAPER SUMMARY

Laser processing covers a wide range of power (-up to 10^{12} watts/cm^2), interaction time (seconds to picosecond) and process materials with lengthscale nano-meters to meters. Therefore, developing a science base is challenging. Although, often research is application driven, basic understanding of the process often requires in depth knowledge in mathematical modeling of the process and on-line process diagnostics.

Process modeling is rather challenging since several transport phenomena occur simultaneously in laser processing, depending on the intensity of the incident laser beam and the laser-materials interaction time, as shown in Fig. 1. For example, in laser surface hardening where the power density level is on the order of 10^3 to 10^4 W/cm^2, heat transfer plays the most important role with mass transfer, determining the limits of dwell time required for phase transformation. In surface melting (or melt quenching) and welding where the power density level is on the order of 10^5 to 10^7 W/cm^2, momentum transfer or convection is significant. Convection also dominates the process of laser surface alloying and cladding (power density is on the order of 10^5 and 10^6 W/cm^2) along with mass transport, which determines the nonequilibrium microstructure and composition of the solidified materials. Vaporization and plasma formation also are important in determining the surface contour, energy partitioning, and deep penetration in welding. However, vaporization and gas dynamical effect become predominant in laser processing when the power density is achievable with high brightness lasers, such as face-pumped YAG laser. Figure 1 summarizes the associated transport phenomena in various laser processes. It is evident that convection affects a large number of laser processes, and thus attention to the unsteady flow in melt dynamics is important for an understanding of laser processing. Also, the effects of high brightness lasers during materials processing, and the interaction between the laser beam and plasma are essential to gain a complete understanding of the laser-materials interactions. It is especially important now that a national team lead by TRW will design and build high brightness YAG laser for manufacturing application.

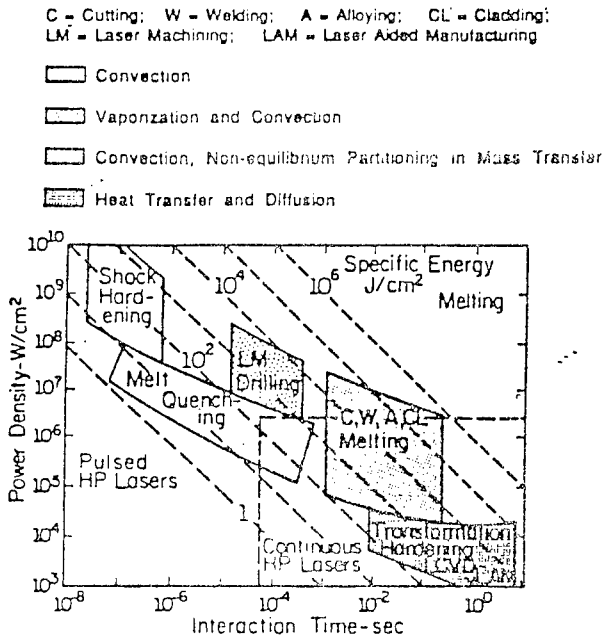


Figure 1 Operational regimes and associated transport phenomena for various processing techniques

When a high brightness laser, such as face-pumped YAG laser, is focused on the surface of a solid target, a fraction of the laser energy is absorbed by the target material. This heats up the material to produce liquid and vapor. During rapid vaporization, the temperature, density, and pressure become discontinuous across a narrow region of thickness with a few mean free paths, called Knudsen layer where the continuum hypothesis is not valid.

Development of real-time optical, acoustic, and electronic sensors for on-line process monitoring is key to the development of advanced processing techniques. The development of control strategies that couple on-line sensor measurements with sophisticated computer models of the laser aided material processing technique is especially promising. Several techniques to monitor the laser beam have been reported by Beyer and Abels (Industrial Laser Review, Dec. 1993).

Optical techniques are promising both in terms of diagnostics for fundamental studies of the laser-material interaction and as the basis of sensors for real-time process control. Potential optical diagnostic techniques include emission spectroscopy, laser-absorption spectroscopy, laser-induced fluorescence (LIF) spectroscopy, coherent anti-Stokes Raman scattering (CARS) spectroscopy, degenerate four-wave mixing (DFWM) spectroscopy and Rayleigh scattering. In emission spectroscopy, the radiation emitted by excited state species present in the gas or plasma in the laser-material interaction zone is detected in a spectrally resolved manner. The intensity of the light detected at a characteristic frequency for a particular molecule or atom is a qualitative indication of its total number density. In a laser absorption measurement, a tunable laser beam is passed through the gas or plasma. The laser frequency is tuned over a molecular resonance and the integrated absorption is a measure of the path-integrated total number density for the species of interest. Laser-induced fluorescence is a spatially resolved technique where molecules are driven from the ground state to an excited state by laser absorption, and fluorescent emission from the laser-excited states is detected as a measure of total number density. Both laser absorption and LIF can also be used to measure temperature. Coherent wave-mixing detection techniques, where the signal is emitted as a laser-like beam, include CARS for temperature and major species concentration measurement, and DFWM for minor species concentration measurement. Rayleigh Scattering produces a signal that is non-resonant and strongly (4th power) and dependent on the size of the scattering particles and could thus be used to monitor the abundance of clusters in the cooling vapor/plasma.

Many of these optical techniques have been developed and applied successfully in the field of combustion. Application of these same types of techniques in laser-aided materials processing will enhance significantly our fundamental understanding of the laser-material interaction. While the species of interest for laser-material interactions will differ in general from those of interest in a combustion medium, the experience gained from applying these techniques in a hostile combustion environment is invaluable for diagnostic studies of laser-aided materials processing.

Acoustic diagnostics offer the potential of providing real-time sensing of defect formation during laser-aided material processing. Acoustic emission signals are stress waves generated defects as they occur in the material.

Advanced optical diagnostics will provide spatially and temporally resolved measurements of surface and gas-phase properties in laser-material interaction zone. The application of advanced optical diagnostics should be closely coupled with the laser-material interaction modeling. The increased fundamental understanding of the key process variables that results from the coupled modeling-diagnostic effort can be used to guide the development of real-time sensors for process control. This paper describes some of the recent advances in modeling and measurement techniques for laser processing of metals.

9:15am - 9:45am
TuA2

High Speed Ablation of Glass Using TEA-CO_2 Laser

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Introduction. Glass is characterized by high transmission from the UV to the IR and outstanding thermal, electrical, and chemical properties. It is one of the most important materials in fields like optoelctronics, flat panel display, UV-optics, and fiber technology. Microfabrication of glass substrates has been required in these fields more and more. One of the promising technique for the fabrication is laser ablation which has been used for direct etching of various polymers[1]. Our group has recently developed a TEA-CO_2 laser of good performance, which shows maximum repetition-rate of 1000 pps, average power per pulse of 500 W, and long running time[2]. In this study, laser ablation has been applied to glass using the TEA-CO_2 laser for maskless high speed etching.

Experimental. The glasses used in this study are synthetic quartz and BK-7. The TEA-CO_2 laser beam with a 10.6 μm wavelength and 80 ns pulse duration was focused by a ZnSe lens (focus length = 20 cm) down to a spot diameter of about 400 μm (at 1/e intensity) on the sample surface. The repetition-rates of laser were varied from 1 pps to 1000 pps to investigate the dependence of ablation rate on the repetition-rate. The ablation was performed at the atmosphere and a vacuum of 4.2×10^{-5} Torr. Ablated profiles including depth and width are observed by a surface profiler (alpha-step 200) and optical microscope. The chemical compositions of the ablated bottoms were measured by electron prove micro-analyser (EPMA).

Results and Discussion. The threshold fluence of laser ablation is 3.47 and 1.63 J/cm^2 for quartz and BK-7, respectively. When laser fluence over this threshold is irradiated on the sample surface, debris are produced and scattered. The profile of ablated cross-section presents a Gaussian distribution of laser power. This result shows that the etching of glass with TEA-CO_2 laser occurs by photothermal ablation. Figure 1 shows ablated groove depth and width as a function of laser pulse count at laser fluence of 30 J/cm^2, repetition-rate of 1 pps, and the atmosphere. The depth of groove increases almost linearly with increasing pulse count, but the width of groove is saturated. Therefore, spatial micro-fabrication and control of a groove profile on glass are possible with a condition of this laser processing. These results can be applied in fabrication of micro optical device[3,4]. Figure 2 shows a cross-sectional profile of the ablated region for the synthetic quartz and BK-7 substrate measured by a surface profiler. The cross-section of ablated groove on the synthetic quartz is smooth at the edge as shown in Fig.2 (a). On the other hand, the edge of ablated groove on the BK-7 substrate has

rise and roughness as Fig.2 (b). It is suspected that this difference of the ablated profile between synthetic quartz and BK-7 substrate is caused by the difference of temperature rising and melting point between two samples. The maximum etching rate of 400 μm/s was obtained by a laser fluence of 30 J/cm^2. It is about five orders of magnitude greater than that (0.06 μm/s) obtained by common wet etching[5] with HF solution. Dependence of the ablated depth on repetition-rate and chemical compositions of the ablated bottoms will be also discussed.

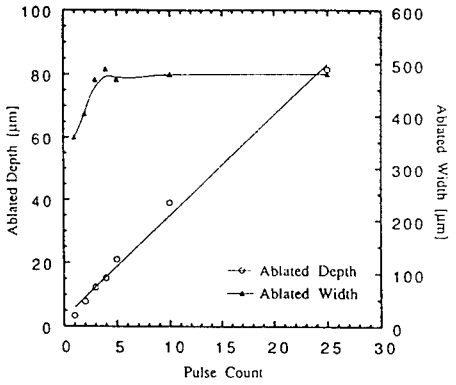


Fig. 1 Groove depth and width as a function of laser pulse count at laser fluence of 30 J/cm^2, repetition-rate of 1 pps, and the atmosphere.

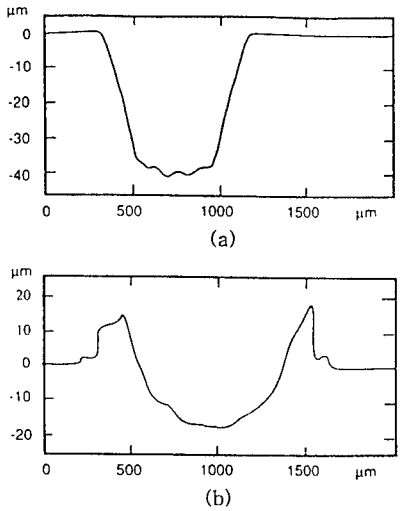


Fig. 2 Cross-sectional profiles obtained by a laser fluence of 30 J/cm^2, repetition-rate of 1 kpps, and 10 pulses at the atmosphere for a synthetic quartz (a) and BK-7 (b).

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9:45am - 10:30am (Invited)
TuA3

Excimer Lasers as Tools for Material Processing in Manufacturing

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Summary

Since their initial demonstration 20 years ago, excimer lasers have developed from physicists´ ´´toys´´ to powerful tools, offering unique benefits to a wide range of applications. Nearly all technical (plastics, ceramics, glasses, metals, semiconductors, composites) and biological/medical materials can be structured by the intense ultraviolet (UV) laser lights. Drilling of microholes for ink jet nozzle heads and for MCM microelectronic packaging, stripping of very tiny wires, annealing of TFT´s for flat panel displays and high quality marking are well-known industrial introduced examples of this technique.

Recently two very important breakthroughs were achieved. The first is in regard to the performance of the excimer laser itself. The second one is a much more advanced way of using UV photons more efficiently.

New Quality in Excimer Laser Performance

Excimer lasers are expanding their importance as the most powerful and reliable industrial tools in the UV region. Recently, technical developments by laser manufacturers have resulted in remarkable improvements in excimer laser performance and reliability, as well as cost of ownership. With gas and optics lifetimes in excess of 10^8 laser pulses together with integration of internal halogen generators, a breakthrough towards quasi-sealed off excimer lasers with handsfree operation was accomplished.
For example, for a line-narrowed KrF excimer for microlithography, the actual cost of ownership is already close to the goal of less than $20K per 10^9 laser pulses. This is one of the reasons why the development of the current market for this high-end application (256MB DRAM production) develops very promising. The first commercial 1 kHz line-narrowed KrF laser became available at the middle of 1995. For the next generation (1 GB DRAM) already corresponding ArF lasers are under development. High repetition rate excimer lasers are also an advantage for a wide range of other scanning applications. In some cases this is combined with the request for a higher pulse energy. For industrial excimer lasers the available laser power is actually between 100W (ArF) and 200W (KrF, XeCl). Lasers with higher output are under development, but the dominant parameters are the industrial reliability and components lifetime. The most important cost item for industrial use of excimer

lasers, especially in high duty cycle applications (e.g. 24 hours/3 shifts with 300 Hz), is the laser discharge tube lifetime. Today, high power excimer laser tube lifetimes are between some 10^8 (ArF) and more than 10^9 (XeCl) pulses. With the introduction of the NovaTube™ technology, gas consumption costs were reduced to a minor part, which makes the running costs of an excimer laser more economical than using a flash-lamp pumped solid state laser.

Advanced UV Optical Systems

With the development of spatial averaging multi-lens beam homogenizer techniques, the application itself can be isolated from laser influences, which further increases the reliability of the total process. The combination of special homogenizer and illumination design with the following imaging optics allows an optimum beam use. So the approx. 30x10mm output of a high power XeCl laser (670mJ, 300 Hz) can be converted into a very homogeneous (better than 5 % rms) line, about 200-500 mm long and 500 µm wide. Efficiency is about 55 to 60 %. These line beam optics are the key component for excimer laser annealing of Active Matrix Liquid Crystal Displays (AMLCD's). Only excimer laser technology enables low temperature (below 400°C) silicon recrystalization and allows the use of low cost, plain glass substrates which reduces the AMLCD's cost by almost two orders of magnitude. Such excimer laser annealing systems are already used in larger numbers in manufacturing especially in Japan and Korea. Customers in the US and Europe are becoming more and more interested in this new technology as well.

The next example only becomes possible on the basis of a high performance optical system. One of the most recently commercialized productions uses excimer lasers is precision drilling of ink-jet printer heads. In high volume manufacturing, 50 to 200 or more nozzles can be drilled in parallel over a field of about 10-20 mm, with hole diameters of between 20 to 100 µm and tolerances in the sub-micron range. Also, a precisely defined hole shape (including wall angle control) and telecentricity of all hole axes (within 0.5 degree) are required. The excimer laser ablation replaces conventional hole production methods, which have many more steps, smaller yield and finally much more cost. The same technology is used for drilling of ceramic nozzles with applications from automotive industry to medical device manufacturing.

Generally, the availibility of the new generation of industrial excimer lasers together with high-end UV optics systems opens more and more doors for microprocessing and advanced surface treatment industrial applications.

Laser Processing to Improve Residual Surface Stress of Metal Components

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Laser processing of water-immersed material has been developed to improve the residual surface stress of metal components. The process changes the stress field from tensile to compressive through irradiation by a frequency-doubled YAG laser or copper vapor laser (CVL).

Principle of Residual Stress Improvement

When a focused laser pulse impinges on a metal surface, a high-pressure plasma forms through the ablative interaction between the laser pulse and the metal surface, as shown in Fig.1. The presence of water significantly enhances the plasma pressure, causing it to exceed the yield stress of most metals. A shock wave is generated on the metal surface by the impulse of this high-pressure plasma, and as it propagates energy is lost and a permanent strain is caused in the metal. A residual compressive stress could be introduced in the metal surface by scanning the laser pulse over the surface.

Results of Basic Experiment

Figure 2 shows a typical compressive stress invested in the surface layer of austenitic stainless steel (SUS304). A frequency-doubled YAG laser was focused with a spot diameter of 0.75 mmϕ on a water-immersed test piece with a peak power density of 50 TW/m^2.

A cross-sectional micrograph of the SUS304 test piece after underwater laser irradiation is shown in Fig.3. No sensitized nor re-solidified layer can be observed, which suggests the test piece was processed with minimal thermal effects.

Figure 4 shows the result for inconel 600 processed with the frequency-doubled YAG laser.

Copper Vapor Laser Processing

Processing with a CVL was also studied. The main feature of CVLs is their high-repetition rate of about 5×10^3 pulses per second, together with the high-average power of several hundred watts. The time required for processing would be drastically reduced if a CVL could be used. Preliminary experiments on residual surface stress improvement with a 500 W class CVL showed that an area of 0.3 to 3 m^2 could be processed every hour.

Concluding Remarks

A significant residual compressive stress (>100 MPa) was successfully added to the surface layer of SUS304 and inconel 600 to an adequate depth (>100 μm) by focusing a pulsed laser on submerged test pieces. This effect could be exploited to extend the fatigue life and prevent the stress corrosion cracking (SCC) of metal components.

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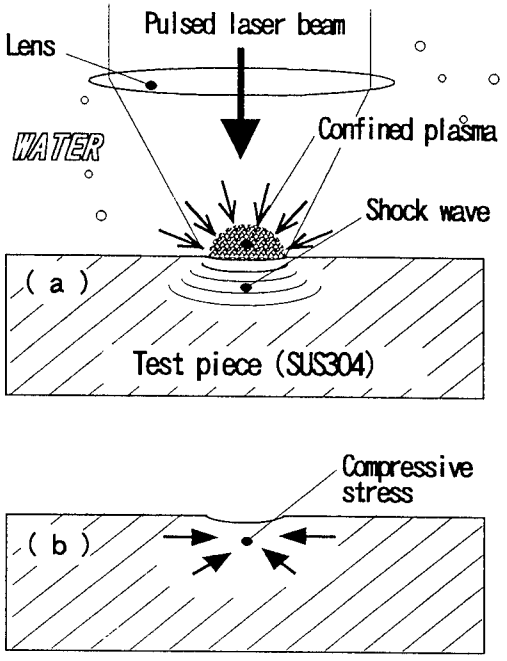


Fig.1 Principle of stress improvement by underwater laser irradiation
(a) during irradiation
(b) after irradiation

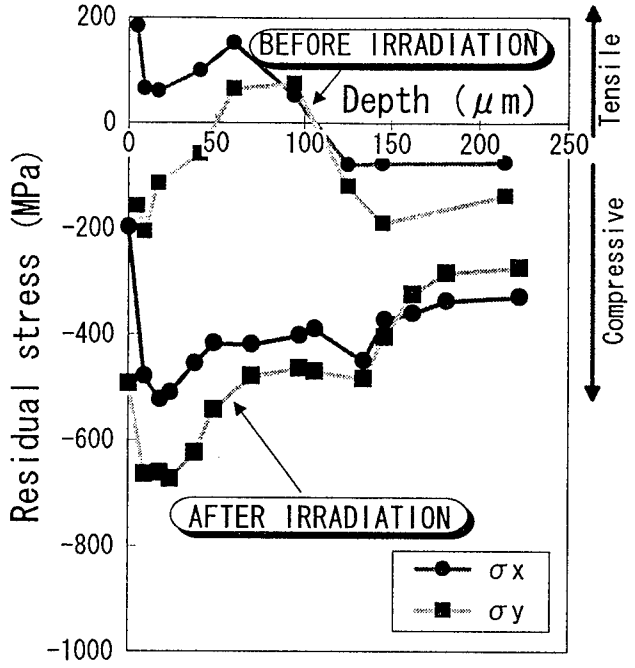


Fig.2 Stress improvement of SUS304 with frequency-doubled YAG laser

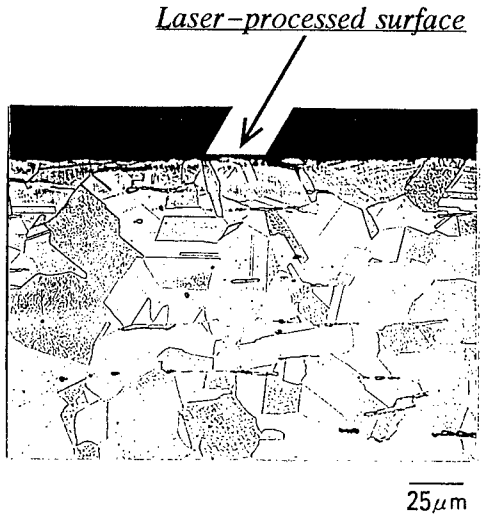


Fig.3 Cross-sectional view of laser-processed SUS304 test piece

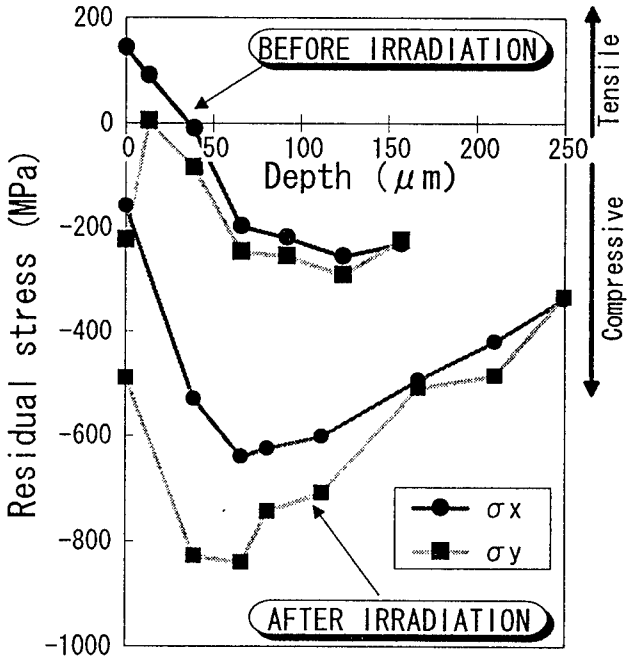


Fig.4 Stress improvement of inconel 600 with frequency-doubled YAG laser

Terawatt Lasers: Probing Unique Material Properties with Novel Diagnostic Source

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University of Michigan, Ann Arbor, MI

Short pulse and high intensity lasers can produce bright ultrashort-pulse-duration x-rays, electrons and ions. They also make highly nonequilibrium plasmas that can be used to deposit thin films with unique material properties. We present new experimental results all of these topics.

We first report results on the characterization, control, and applications of ultrashort x rays emitted from laser plasmas. It is demonstrated experimentally that the pulse duration may be controlled by adjusting the incident ultrashort-pulse laser flux.[1]. Figure 1 shows streaked gold x-ray emission using high-contrast conditions for three different laser intensities.

The results are found to be in qualitative agreement with the predictions of both a code-independent model of radiation from a collisionally dominated two-level ion and a hydrodynamics code coupled to a detailed-configuration atomic physics package. Applications of such sources include: (1) diagnostics of solid-density and non-LTE plasma conditions, (2) a tool for the study of opacity and radiation hydrodynamics in a parameter regime that is otherwise inaccessible, and (3) a source for time-resolved diffraction, spectroscopy, or microscopy studies of transient chemical, biological or physical phenomena. Preliminary results of an ultrafast time-resolved x-ray absorption spectroscopy of ultrashort-laser-produced shock propagation will also be presented

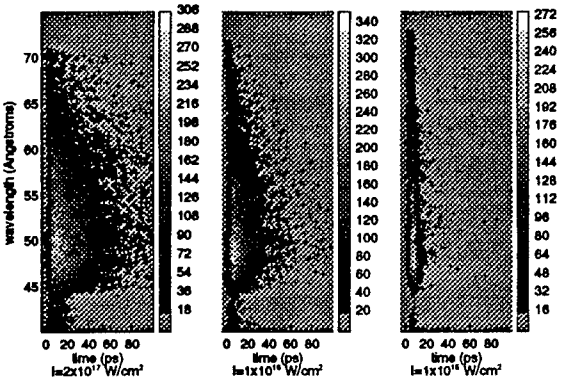


Figure 1: Streaked gold x-ray emission using high-contrast conditions for three different laser intensities ranging from I = 2.0×10^{17} W/cm^2 down to I = 2.0×10^{15} W/cm^2.

The field at the focus of one of these short pulse, high power lasers is so high that electrons are oscillate at nearly the speed of light, giving rise to several interesting, and previously unstudied, effects. For instance, it produces extremely high laser pressure (called the ponderomotive force), which can drive a high-amplitude plasma "wake-field plasma wave," the basis for what is called the laser wake-field accelerator (LWFA). Essentially, the laser pulse pushes the electrons out of its way, but the ions—because of their much heavier mass—pull them back, setting up a plasma wave oscillation. In this way, the plasma wave effectively rectifies the laser electromagnetic field so that it becomes an electrostatic field propagating in the direction of the light pulse at nearly the speed of light. This can continuously accelerate electrons to GeV energies in a centimeter distance.

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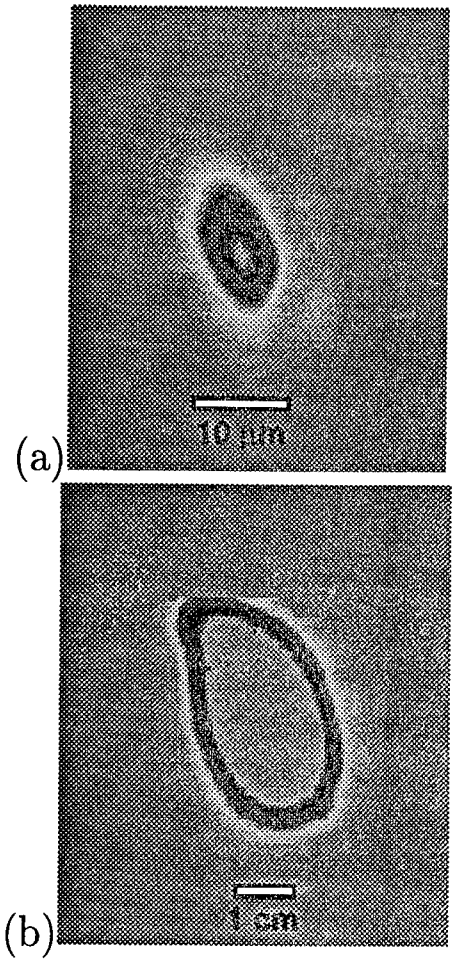


Figure 2: Images of: (a) the laser spotsize at the beam waist, obtained with equivalent plane imaging and a CCD camera, (b) the electron beam 8 cm away, obtained with filtered photographic film.

We have recently demonstrated that a laser wake field can produce a collimated beam of MeV electrons and that the laser may have been guided by relativistic self-focusing and electron cavitation. The experiment is remarkably simple. A high-power laser is focused into a molecular beam produced by a gas jet. The laser used in the experiment has a pulse duration of $\tau = 400$ fs, and an energy up to 10 J, corresponding to a peak power of 25 TW. When focused in vacuum with an f/5 off-axis parabolic mirror, the laser can reach an intensity of up to 10^{19} W/cm^2. In order to create the plasma, the gas from a pulsed valve is tunnel-ionized by the laser pulse itself, reaching a peak electron density on axis of 10^{19} cm^{-3}. In this case, the laser pulse width is much greater than a plasma period, $\tau >> 2\pi/\omega_p$, where ω_p is the plasma frequency. This is usually described as the self-modulated laser wake field since, in this case, the laser pulse becomes modulated by the plasma wave with a periodicity of a plasma period. Basically, the density rarefactions of the plasma wave modifies the index of refraction periodically along the axis of the pulse, breaking the pulse into a sequence of shorter pulses. It is related to the stimulated Raman scattering instability. Greater than 10^8 electrons were observed to be accelerated. The electron source size is estimated to be 10 μm and the electron pulse duration, a few picoseconds. Fig. 2 shows a photograph of the electron beam (all electrons with energies above an MeV) at a distance of 15 cm from the jet.

4:15pm - 5:00pm (Invited)
TuB1

PULSED LASER DEPOSITION OF DOPED EPITAXIAL COMPOUND SEMICONDUCTOR FILMS

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The past decade has seen rapid growth in fundamental studies of the pulsed laser ablation (PLA) process and its application for pulsed laser deposition (PLD) [1]. However, there has been relatively little use of PLD to grow *doped, epitaxial* compound (or elemental) semiconductor films. Nevertheless, it is clear that some of the advantages of the ablation process also should apply for exploratory semiconductor materials research, especially for complex multi-element materials. Several groups recently have carried out experiments to determine whether PLA can grow structurally high quality and highly doped epitaxial compound semiconductor films [4–9]. We initiated a systematic study using closely related II-VI and I-III-VI materials.

Experiments with ZnSe and ZnTe show that use of high-density, hot-pressed ablation targets reduces the areal density of particulates to a level that is negligible for exploratory materials research. RBS measurements, though limited by ~1% precision, show that stoichiometric epitaxial films can be grown by ablation of a stoichiometric target; however, congruent transfer does appear to be sensitive to ambient gas pressure and pulsed laser energy density.

Highly *p*-type ZnTe:N films were grown by ablating a ZnTe target through molecular N_2 [4,5]. The highest hole concentrations, $p \sim 10^{20}$ cm^{-3}, are approximately equal to the largest obtained by any growth method in a wide band gap II-VI semiconductor. These experiments demonstrate the general feasibility of doping compound semiconductors from the gas phase during PLA. The heavy hole doping of ZnTe:N is accompanied by a uniform lattice contraction, consistent with nitrogen incorporation on substitutional lattice sites and the resulting *p*-type conductivity. However, atomic nitrogen is not observed in the laser-generated plasma. The high nitrogen doping apparently occurs by a new mechanism, believed to be direct kinetic energy-enhanced reactions of Zn with N_2, either adsorbed on the growing surface or in the gas phase. Earlier experiments showed that the composition of $ZnSe_{1-x}S_x$ films produced by ablating a pure ZnSe target also could be controlled via the partial pressure of ambient H_2S gas [3].

A combination of RHEED, ion probe, and TEM measurements revealed a succession of transitions, controlled by N_2 pressure, between distinctive growth regimes in which different species dominate the incident ablation flux [10,11]. Clearly 2D (streaky) RHEED patterns were obtained for N_2 (Ar) pressures of <30 (<40) mtorr, with spotty (3D) patterns for pressures ≥50 mtorr [10]. Time-resolved ion current measurements have been deconvoluted to reveal three distinct peaks in the ion (and presumably the atomic) flux as a function of N_2 pressure. The fast peak (mode 1), dominant for N_2 pressures ≤15 mtorr, is due to unscattered ions having kinetic energies sufficient to do lattice displacement damage to the growing film. Mode 2, dominant for pressures up to ~70 mtorr, consists of ions and atoms with kinetic energies of only a few eV or less, which seem ideal for energetic beam-assisted film growth and near-surface chemical reactions. The peak in hole mobility for *p*-ZnTe:N films is reached near 50 mtorr N_2 pressure, where mode 2 is dominant, though cross-section TEM images reveal an increasing density of extended defects (microtwins) from vacuum up to 50 mtorr. At higher N_2 pressures, TEM, ion probe, and electrical properties measurements all reveal a transition to a new growth regime, which is believed to be the onset of significant cluster deposition, near 70 mtorr N_2 pressure. Films exhibit a columnar microstructure and decreasing hole mobility in this regime. The broadening found in high resolution XRD rocking curves is consistent with the microstructural changes observed by TEM.

Both *n*- and *p*-type doping of II–VI films have been demonstrated by Shen and Kwok [8,9] by incorporating column-I (Li) or column-III (In) dopant atoms directly in ablation targets. However,

quite high (~10 mole %) Li and In concentrations were required in the targets to obtain films with low enough resistivity to make ohmic contacts and carry out Hall effect measurements. Thermopower measurements also suggested p-type doping of ZnS, ZnSe, and CdSe, but Hall measurements were not made because of difficulties in making ohmic contacts. The fact that the dopant atom concentrations in ablation targets were so much larger than the carrier concentrations in films suggests either that dopants were not incorporated efficiently in the films or that they were electrically inactive. Direct measurements of dopant incorporation and carrier concentrations in films are needed to resolve this question.

We also have grown fully epitaxial n-type films of $CuInSe_2$ at 350°C [11]. This temperature is ~175°C below typical growth temperatures for polycrystalline $CuInSe_2$ films used for photovoltaic energy conversion. Thus, it may be possible to grow and dope epitaxial I-III-VI films at low temperatures in order to study their intrinsic properties and doping mechanisms.

Unintentionally doped GaN and InN films recently were grown on sapphire(0001) by PLA at ~500°C without the use of a buffer layer [6,7]. This temperature is significantly lower than those at which most epitaxial nitride films have been grown by MOCVD or MBE. The PLA films were grown at a target-substrate separation of only 3 cm and were immersed in the excited laser ablation plasma. These conditions produced GaN films whose crystallinity and electrical properties rival those of films grown at much higher temperatures by other methods. The implication is that growth in the ablation plume, with both kinetic and internal internal energies available, must be an important factor in forming high quality GaN at low temperatures. The growth of strongly p-type InN films also suggests distinctly different growth conditions and doping behavior during PLD than with conventional growth methods [6]. The occurrence in the GaN experiments of accidental doping by impurities in the ablation target or in an ambient gas is promising for future applications of PLA to grow and dope these materials.

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5:00pm - 5:30pm
TuB2

MULTILAYER MULTICOMPONENT SEMICONDUCTOR STRUCTURES FOR MICROELECTRONICS FORMED USING LASER AND THIN FILM TECHNOLOGY

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The present-day technological processes enable to obtain the smallest thicknesses of doped layers ≈300-500 nm. The use of laser as a technological tool makes it possible to reduce the thickness of modificated layers to ≈10 nm and to build the full-automatic low-temperature technology for shallow p-n junctions and devices needed in future.

Solid-phase laser-induced doping of semiconductors uses radiation with the wavelength for which the semiconductor is transparent. Therefore, absorption takes place mainly in the dopant film covering the semiconductor surface. During laser light absorption the impurity film heats up to give way to solid-phase diffusion into the semiconductor. This process can be characterised as a cold diffusion, or a diffusion at the temperature gradient Due to low temperature laser processing gives especially good result for compound and easy dissociating materials, such as: InAs, InP, GaAs, InGaAs, InGaAsP, ets.

We used 0,5 mm thick wafers of Si, InP, GaAs and CdS mechanically and chemically polished on both faces and vacuum-coated with a thin film (100-1000 Å) of dopant elements (P, Al for Si; Zn, Au-Au:Ge-Ni for InP; Zn, Au-Au:Ge for GaAs and Cu for CdS). The irradiation was performed in a vacuum chamber ($p=10^{-6}$ Torr) with a 1 kW CW CO_2 laser source (λ = 10,6 μm) during ≈1s uniformly over the whole sample surface. The dopant depth distribution in laser-implanted wafers was studied by secondary ion mass spectroscopy (SIMS) and by Auger electron spectroscopy (AES)

In the process of laser solid-phase doping of semiconductors impurities display electrical activity at their top equilibrium solubility and do not need supplementary activation as, for example, after ion implantation. The zero-bias resistance of GaAs diodes is 10^{10} Ω and leakage current does not exceed 1 nA under a reverse bias of 8 V.

The characteristics of diodes formed on the basis of Si and InP correspond to an average level of analogous structures, traditionally obtained on these materials by the methods of diffusion and ion implantation. At 10 V inverse voltage, the dark current is = 1 nA and the breakdown = 100 V and = 40 V for Si and InP diodes, respectively. Since the laser solid-phase doping ensures also a high degree of reproducibility of p-n junction parameters, it can be effectively used for device fabrication.

The current-voltage characteristics of the contacts with GaAs and InP, obtained before and after laser irradiation, shown that the initially non-linear characteristic of the contacts transforms into a straight line as a result of diffusion of the contact group of elements into the semiconductor. A typical contact resistance with GaAs and InP after laser treatment decreases to $\approx 5 \cdot 10^{-7}\ \Omega \cdot cm^2$ and $\approx 5 \cdot 10^{-5}\ \Omega \cdot cm^2$ that is the desired value for nonrectifying contacts with these semiconductors.

The improvement in the electrical characteristics of the contacts is, in our opinion, due to the specifics of laser solid-phase doping of semiconductors. Brief but intensive laser interaction with semiconductors does not result in mutual penetration of the elements of main material and of the elements of contact group as well.

The method of laser solid-phase diffusion can be applied efficiently not only for laser-induced doping of semiconductors, but for synthesis of compound materials and heterojunction formation as well. It is known that in the process of CdS doping such impurity as Cu do not replace Cd but react chemically with S forming usually Cu_2S.It was determined that laser action on the CdS single crystals with the Cu thin film covering the surface of the crystal, results in synthesis of Cu_2S compound layers and CdS-Cu_2S heterojunction formation.

Besides the ion implantation technique used at present, laser solid-source out diffusion may become a cheap but effective self-aliyned doping technology for shallow p-n junctions needed in future. The unique possibilities of laser application in microelectronics lie in formation of perfect doped layers of submicron thickness with reproducible parameters and given picture of location of active elements.

A number of applications of solid-phase processes stimulated by laser radiation is suitable for microelectronics, for IC and device fabrication: involving formation of submicron doped layers, cleaning of dielectric coatings, making of Ohmic contacts, p-n and heterojunctions.

5:45pm - 6:30pm (Invited)
TuB3

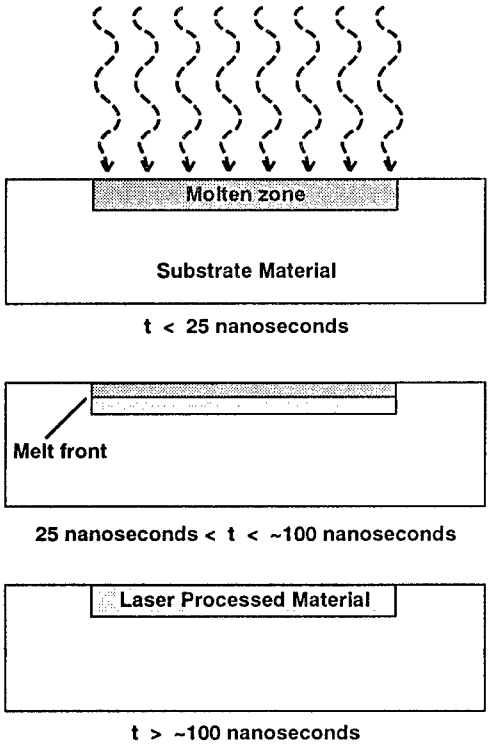
ADVANCES IN EXCIMER LASER SURFACE PROCESSING OF MATERIALS

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The use of pulsed excimer lasers to surface processing of materials hinges on an understanding of the nature of the interaction between the laser energy and the material. One of the advantages of excimer laser processing is the relative uniformity of that interaction across diverse materials. The short wavelength, (200–400 nm depending on the laser gas) and the short pulse length (~ 30 ns) mean that for most materials, the energy is absorbed in a region of the surface that is shallow (~10 nm) relative to the thermal diffusion length (~100 nm) in the material. These conditions mean that the details of the absorption process do not affect the temperature distribution below the surface[1] and the thermal effect is that of an instantaneous heat pulse incident on the surface. The large size of a typical excimer beam spot for fluences in the 1–3 J-cm^{-2} range ensures that the heat flow is essentially one-dimensional. The net effect of an incident excimer laser pulse is therefore to rapidly heat the surface of the material with cooling occurring at a rate determined by the 1-D heat flow to the back of the sample. The process is also highly efficient, due to the low reflectivity of most materials in the ultra-violet. Typical cooling rates for surface-melted materials are of the order of 10^9 K-s^{-1} with a typical melt–solidification–cooling cycle back to ambient temperature taking less than 10^{-2} s. The short duration of the liquid state and the thin melt layer eliminate any chance for convection. These aspects of the laser-materials interaction mean that surface effects, whether through thermal transformation or melting and resolidification, are dependent entirely to the incident fluence, the thermal properties of the material, and the number of incident pulses.



The application of this understanding of the laser materials interaction to surface modification must also recognize the existence of thermodynamic driving forces and kinetic limitations in light of the short duration of a single pulse event. Single pulse processing can result in amorphization[2], recrystallization[3], or martensitic transformation[4]. For modifications that require substantial migration of individual species, either mixing or segregation, multiple pulse processing is necessary. For typical liquid state diffusion parameters and a melt duration of the order of 100 ns, diffusion lengths of the order of 50 nm per pulse can be obtained and net effects can be related directly to the number of incident pulses[5]. Metastable microstructures often result from rapid solidification from the melt[6].

For species that have higher solubility in the liquid than in the solid phase, segregation by "zone refinement" from multiple passes by a solidification front to the surface results in surface enrichment of those species[7]. Mixing of alloying elements can occur when there is an appropriate driving force[8]. The most straightforward case is for mixing at a solid-solid interface that is melted by the laser energy, but the use of a gas or liquid atmosphere can lead to alloying directly from the fluid phase[9, 10]. Additions that alter the chemical or mechanical properties of the surface

region can be incorporated with a graded interface that is not prone to delamination. The high temperatures reached during laser processing facilitate mixing in some systems that cannot be mixed with ion beams due to kinetic constraints[11]. The short duration of individual pulse events means that multiple pulse processing, even at rates at high as 100 Hz, can be thought of as a series of independent events, allowing for very rapid processing.

The most obvious applications for surface processing occur where the bulk properties of a component are not commensurate with the needed surface properties. Excimer laser processing has been shown to increase the resistance to pitting of AISI 304 SS due to an increase in the surface Cr and the formation of a thicker layer of the stable Cr oxide. Enhancement of Cr results from zone refinement. Mixing of Si layers into Nb surfaces has also provided increased corrosion resistance in Nb through formation of stable surface compounds[12]. In an inverse process, WSi_2 was formed by mixing of W layers on Si substrates[13].

Improvements in surface mechanical properties have been observed in a number of metal[14, 15, 16] and ceramic alloys[17, 18, 19]. In tribological applications, improvements are related variously to changes in the surface hardness, finer-grained or amorphous microstructure, and the formation of high-lubricity transfer films on the surface. Fundamental changes in the wear mechanism have typically been observed. Excimer laser surface processing has also been used to increase the bulk fracture strength of ceramic materials, which often fail due to surface defects[20, 21].

In the microelectronics industry, apart from micromachining or material removal applications, the same features of the laser-materials interaction that are used to modify the mechanical or electrochemical properties of a surface can be used to advantage. Single-shot recrystallization of large areas of amorphous Si to poly-Si for production of active-matrix liquid crystal displays has been demonstrated, as has multiple-pulse annealing[22]. Exploiting the low viscosity of liquid metals, laser melting and resolidification has been demonstrated for planarization of Al[23] and other metal layers.

The fundamentals of excimer laser surface modification have largely been established. As in many "boutique materials" developments, process optimization is required for particular applications. Further advances, such as those demonstrated in microelectronics, await these application-specific developments.

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Wednesday, August 7, 1996

SESSIONS:

WA: Analysis

WB: Processing

8:30am - 9:15am (Invited)
WA1

Applications of fs lasers to nonlinear spectroscopy and process control of Si(001) interfaces

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(512)-471-6054

Si(001) interfaces are among the most technologically important for nonlinear optical analysis, yet their exceptionally weak interfacial second harmonic susceptibility $\chi^{(2)}_s$ has strongly inhibited quantitative interface-specific second harmonic (SH) spectroscopy and related nonlinear optical process control applications. The advent of widely tunable, unamplified femtosecond (fs) solid-state lasers has overcome this barrier by enabling unprecedented SH generation efficiency (~ 10^6 photons/s) with minimal interface heating (<20 K).[1] We have exploited these capabilities to characterize technologically important characteristics of buried SiO_2/Si(001) interfaces, including microroughness,[2] band-bending,[3] strain,[4] and interface oxidation stoichiometry[5] by SH spectroscopy with a single unamplified Ti: sapphire fs laser beam. Here, as an example, we highlight an interface-specific SH electro-modulation spectroscopy[3] study of a Cr/SiO_2/Si(001) MOS structure, and its extension to a fs-time-resolved SH pump-probe study of carrier dynamics in the space-charge region (SCR). In addition we illustrate real-time (< 0.1 s kinetic resolution) SH monitoring of hydrogen (H) coverage of $Si_{1-x}Ge_x$(001) epitaxial growth surfaces during UHV chemical vapor deposition.

The three SH spectra plotted in Fig. 1a were obtained by Fourier analysis of *p*-fundamental/*p*-SH $I_{pp}(2\omega,\psi)$ signals from a Cr/SiO_2/Si(001) MOS structure while sample azimuthal angle ψ, the applied bias φ, and the incident Ti:S frequency ω were systematically modulated. From the ψ-dependence, we extracted the isotropic (a_0), four-fold (a_4), and eight-fold (a_8) Fourier coefficients (FC) at each ω and φ, where a_0 consists of a field-dependent term $a_0^{FD}(\varphi)$ and a field-independent term a_0^{FI}. Fig. 1a shows the spectra of a_0^{FI}, a_0^{FD}, and a_4 near the two-photon resonantly enhanced E_1 critical point. These contributions are proportional, respectively, to a) the electric-dipole signal from the strained interfacial region (~ 10 Å depth); b) the bulk electric-field-induced signal from the space charge region (~ 100 Å depth); c) the bulk quadrupole signal (~ 1000 Å depth), and are here *fully* deconvolved for the first time. The main result is the strong tensile-strain-induced red-shift (ΔE = 0.11 eV) of the interfacial resonance from the bulk E_1 resonance (3.37 eV) exhibited by the two bulk contributions. These spectra should be contrasted with the convolved spectrum $a_0(2\omega)$ obtained from an unbiased SiO_2/Si(001) interface without φ-modulation, shown in Fig. 1b along with the measured phase $\phi_4(2\omega)$ of the 4-fold azimuthal FC. In this case $a_0(2\omega)$, an unresolved convolution of the bulk $a_0^{FD}(\omega)$ and red-shifted interface $a_0^{FI}(\omega)$ E_1 spectra, peaks at the intermediate energy 3.33 eV. Here, the importance of the fs laser was to provide SH signal rates high enough to enable multi-parameter (ψ,φ,ω) modulation, which in turn greatly improved the accuracy of buried interface strain characterization compared to the simpler measurement (Fig. 1b).

Fig. 1c shows the results of extending the previous experiment to a pump-probe measurement using 100fs, λ=710nm Ti:S pulses. In this case, pump-generated carriers modulate the interface SCR instead of an external bias φ, and the effect on the ψ-dependence of probe-generated SH is monitored. At time delay $\Delta t = 0$, the phase ϕ_4 shifts by 180° from the phase observed at $\Delta t < 0$, and a_0 becomes maximum. These changes are consistent with rapid, complete screening of the field-induced SH contribution. At Δt = 170 fs, a_0 is minimum while the SH signal becomes 8-peaked. This occurs as the field-induced SH contribution a_0^{FD} recovers partially to the same magnitude, but opposite sign, as the field-independent contribution a_0^{FI}, leaving $I_{pp} \sim |a_4 \cos 4\psi|^2$. Note also the strong modulation depth of the SH signal due to its interface specificity. Finally after ~ 500 fs the signal has recovered to its unpumped magnitude and phase. The spectral dependence, underlying physics, and diagnostic potential of this ultrafast interfacial recovery will be discussed.

Finally, we show that fs-Ti:S-laser-generated SH provides *real-time*, in-situ monitoring of surface chemical kinetics during epitaxial growth. Such monitoring is increasingly necessary in chemical deposition growth technologies because of the sensitivity of surface chemical kinetic rate constants (precursor adsorption, H-desorption), and therefore growth rate and alloy composition, to growth conditions (temperature, composition, doping). Fig. 2a shows the variation of the *p*-in/*p*-out SH spectrum near the two-photon E_1 feature as an initially 2x1-reconstructed Si(001) surface in UHV is exposed to increasing atomic hydrogen doses (calibrated by temperature programmed desorption) up to 1.5 monolayers. Such spectra, modelled (solid curves) in terms of the combined effect of relaxation of reconstruction-induced strain and the optical interference of resonant and nonresonant background contributions, provide a quantitative basis for selecting strategic laser frequencies at which SH intensity is proportional to H coverage over significant ranges. Fig. 2b then shows real-time variation of SH, and therefore H-coverage, at one such frequency as the gas precursor (Si_2H_6) inlet valve is successively opened and closed at several different substrate temperatures. The temperature-dependence of the H-desorption rate and steady-state H-coverage is immediately evident. From such measurements, kinetic rate constants for precursor adsorption and H-desorption can be extracted. Fig. 2c plots preliminary SH-based measurements of H-desorption rate constants $k_D = A \exp(-E_{activation}/RT)$ for several different $Si_{1-x}Ge_x$ substrate alloy and precursor gas mixtures, which, despite the need for further quantitative calibration, illustrate the flexibility of real-time, fs-laser-generated-SH for kinetic measurements under a widely varying growth conditions.

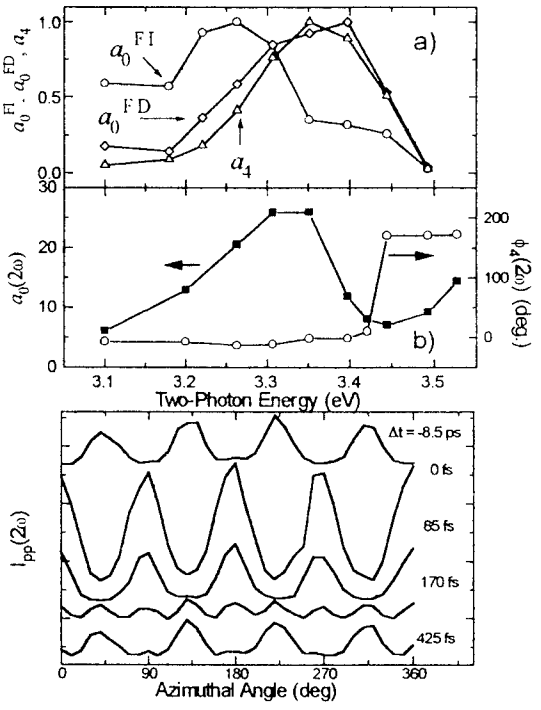


Fig. 1. Spectral dependence SH Fourier coefficients a) $Cr/SiO_2/Si(001)$ MOS structure; b) unbiased $SiO_2/Si(001)$ interface; c) fs-time-resolved rotational anisotropy.

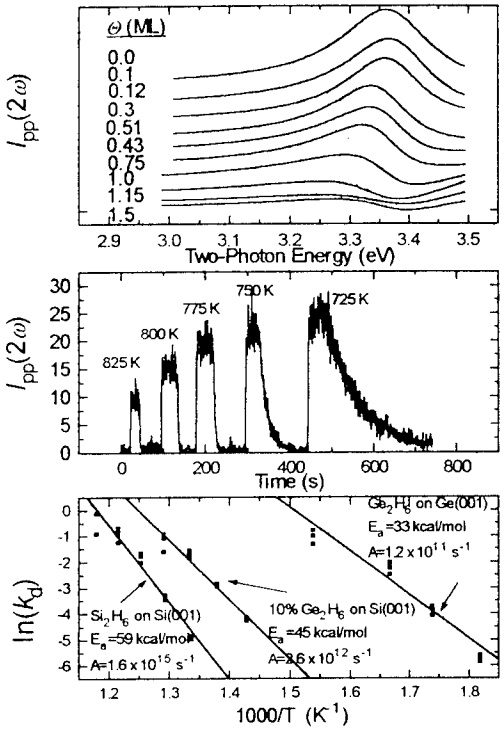


Fig. 2 a) SH spectra of H-dosed surfaces; b) real time SH monitoring of H-coverage with periodic growth interruption at several substrate temperatures. c) H-desorption rate constants.

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9:15am - 9:45am
WA2

Application of ArF Excimer Laser in MOCVD Growth and in situ Characterisation of Gallium Nitride

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1. Introduction

Laser-induced chemical vapour deposition (LCVD) is an attractive technology for the growth of films on fragile and thermally sensitive substrates at low temperature. The laser may simultaneously be used as a probe, both in excitation of semiconductors for in situ photoluminescence measurements and for spectroscopic analysis of MOCVD precursor dissociation paths. We here describe application of an ArF excimer laser (193 nm, 6.4 eV) to growth and characterisation of gallium nitride.

Significant progress has been achieved in GaN crystal growth in recent years, Metalorganic Chemical Vapour Deposition (MOCVD) growth of GaN films on (0001) sapphire , for example, has been reported by Nakamura and co-workers[1] to yield the best quality material. However, the high temperatures required for conventional MOCVD (about 1100^{o}C) are unsuitable for growth on conventional but more temperature sensitive substrates such as GaAs, and especially on lattice-matched but readily dissociated compounds such as the lithinates. Microwave plasma assisted LCVD growth of III-Nitrides is a recently developed technique with the potential to realise low-temperature MOCVD of GaN and is principally intended to provide the reactive radicals Ga and N by photolyic and plasma fragmentation of their precursors over substrates at lower temperature. An ammonia microwave plasma supplies a high flux of activated nitrogen supporting the growth of films in a nitrogen-rich environment. The laser beam dissociates precursors adjacent to the growth surface and enhances growth rate, especially at low growth temperature, by up to one order of magnitude.

2. Material Growth

Our growth chamber consists of a 6-way stainless steel cross with both the pulsed laser and injected microwave plasma beams set in the horizontal plane and meeting at 90^{o} over the substrate. The principal precursors trimethylgallium (TMGa) and NH_3 are introduced into the chamber from above, and perpendicular to, the substrate. The laser beam is set coplanar with, and 5 mm above, the substrate where it photodissociates both group III and group V source gases.

Before growth, sapphire substrates are pre-cleaned below 10^{-6} Torr followed by a NH_3 plasma at a flow rate of 100 ml/min injected downstream into the chamber to clean the sapphire and convert a few surface monolayers to AlN. NH_3 and trimethylaluminium (TMAl) are next introduced into the chamber at flow rates of 100 ml/min and 30 μ mol/min respectively via mass flow controllers and photodissociated by the ArF laser. An AlN buffer layer is thus grown by LCVD with remote NH_3 microwave plasma assistance, to a thickness of 500-1000Å. The GaN film is grown by switching TMAl to TMGa at a flow rate of 40 μmol/min to the thickness of approximately 2 μm. Buffer and film are grown at the same temperature.

R-plane sapphire is the preferred substrate, and at 600^{o}C the total growth time averages 4 hours. Film thicknesses are determined ex-situ by stylus profilemeter along with Hall-mobility, carrier concentration and resistivity data. Room temperature electron concentration and Hall mobility lie in the ranges 10^{15}-10^{16} cm^{-3} and 200-400 cm^{2}/Vs, respectively. Reaction process can be studied by in situ dissociation luminescence, while beam adjustment allows film characteristation either post-growth or at growth interrupts. Photoluminescence (PL) and photoconductive decay measurements use the ArF excimer laser, boxcar integrator, monochromator and photomultiplier.

To investigate the photolysis of precursors in the LCVD process, the ArF excimer laser-induced fluorescence (LIF) spectra of TMGa, NH_3 and TMGa+NH_3 have been measured. Figure 1 shows

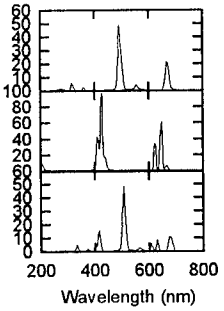


Fig.1 Laser-induced fluorescence spectra of (a) TMGa, (b) NH_3, and (c) TMGa+NH_3.

the LIFs of TMGa (a), NH_3 (b) and TMGa+NH_3 (c). The fluorescence peaks at 492-515 nm and 649-663 nm shown in Fig 1(a) are associated with the emission lines from NH_3 at 492 and 649 nm and from NH_2 at 515 and 663 nm. A strong emission

from NH at 336 nm due to the $A^3\Pi \rightarrow X^3\Sigma^-$ transition indicates its presence with appreciable population. Two groups of peaks at 405, 423 and 440 nm, and at 610, 627 and 647 nm are characteristic of the TMGa fragments $Ga(CH_3)_n$ (n=1-3) and shown in Fig 1(b). The two groups can be identified with the emission of neutral gallium, shifted according to the different chemical co-ordination provided by the number of CH_3 radicals π-bonded to it. Fig 1(c) shows the fluorescence from TMGa+NH_3 under actual growth conditions. The spectrum of Fig. 1(c) is the sum of the spectra of laser activated TMGa (a) and NH_3 (b) indicating that no new detectableradicals are formed during the photolysis of the TMGa+NH_3 mixture.

Hence, GaN is most probably formed directly by reaction of the populous and active radicals $GaCH_3$ and NH on the growing surface rather than from the laser activated radicals $Ga(CH_3)_2$, $Ga(CH_3)_3$, NH_2 and NH_3, that is

$$[Ga\text{-}CH_3] + [NH] \Longrightarrow GaN + CH_4. \quad \text{------(1)}$$

Film growth rate in the temperature range 350-650^{0}C at constant total pressure and NH_3/TMGa ratio decreases exponentially with substrate reciprocal temperature as shown in the Arrhenius plot of Fig. 2. The activation energy is 0.2 eV, which agrees well with other LCVD [2] work, and describes a process in which only the final reaction (1) and surface mobilities are thermally moderated [3] and much smaller than the 1.1 eV found in conventional chemical vapour deposition [3] where all precursor deposition is thermally activated.

3. Film Characterisation

Photoluminescence (PL) measurements use 10 ns laser pulses at 10 Hz repetition with a pulse energy of 80 mJ and light intensity of 2 MW/cm^2. The 300 K PL spectrum shown in Fig.3 has a strong peak located at 3.3 eV (376 nm) with about 10 nm FWHM associated with GaN band to band emission.

Photoconductive decay is measured post-growth with anular evaported aluminium electrodes irradiated by laser pluses under a 1mA constant bias current. Photoconductive decay signals are acquired by sweeping the time between laser excitation pulses and boxcar gate delay. Figure 4 shows a typical photoconductive decay signal including two time constants, an initial rapid decay with time constant $\tau_1 \approx 0.8$ μs associated with the band-to-band radiative process,followed by a slower component with $\tau_2=6$ μ s related to trapping.

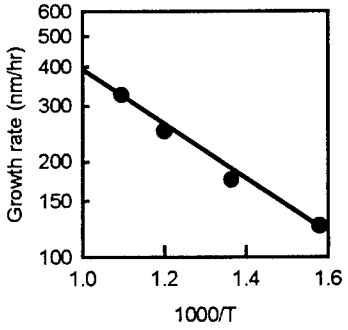


Fig. 2 GaN growth rate as a function of the substrate temperature.

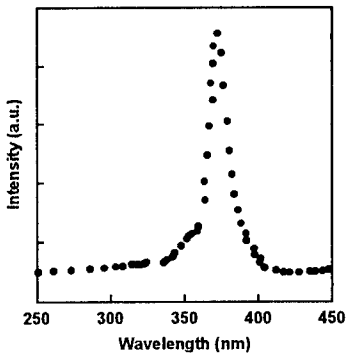


Fig.3 Photoluminescence spectrum of a typical GaN sample, measured at room temperature.

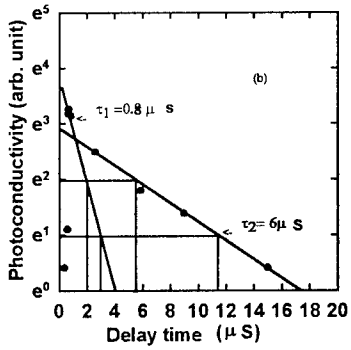


Fig.4 Photoconductive decay of GaN.

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9:45am - 10:15
WA3

Diagnostics of Laser-Induced Germanium Growth by In Situ Spectroscopic Ellipsometry

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Nucleation and growth of high quality amorphous hydrogenated germanium (a-Ge:H) films was initiated by ArF laser-induced CVD and monitored in situ by real time spectroscopic ellipsometry. The UV-laser power was varied between 3W and 10W. The depositions were carried out at low partial pressures of digermane from 0.05μbar to 6μbar, chamber pressures between 0.5mbar and 12mbar and substrate temperatures between 250°C and 310°C. The influence of the deposition parameters such as substrate temperature, laser power, digermane partial pressure and total pressure in the deposition chamber on the growth rate and the film properties was investigated in detail. Typical deposition rates were in the nanometer per minute range.

The quality of the Ge films was studied by several ex situ diagnostic techniques such as FTIR spectroscopy to determine the hydrogen content and bonding configuration, photothermal deflection spectroscopy (PDS) to obtain the Urbach energy and band gap, scanning force microscopy (SFM) to monitor the surface topography, surface acoustic wave spectroscopy (SAWS) to measure the mechanical and elastic constants and conductivity experiments to determine the photo- and dark conductivity. The best electronic properties were found for a hydrogen content between 1-2at.% hydrogen. Under these conditions the Urbach energy was between 50-60meV, the Tauc gap 0.96eV, the photoconductivity 1.2×10^{-6}S/cm and the dark conductivity 5×10^{-7}S/cm.

The ellipsometer (SOPRA) used for in situ monitoring was a rotating polarizer setup with a high pressure xenon arc lamp as light source and a usable energy range between 1.2-4.7eV. As detector we used an optical multichannel analyzer (OMA), which was calibrated against the spectrum of a mercury lamp. With 512 points per spectrum less than two seconds are required to process a spectrum. The spectra collected during film deposition are interpreted by taking as substrate index the pseudo refractive index obtained from the previous spectrum and modeling the difference as a layer consisting of bulk film material and voids using the effective medium approximation (EMA).

To explore the influence of the nature of the substrate surface on the initial growth and the bulk film properties we deposited films on natural silicon single crystal surfaces with the native oxide layer and onto atomically smooth hydrogen-terminated silicon (111) surfaces. The latter samples were prepared by wet chemical processing and inspected ellipsometrically. A comparison of the growth rates for the two surfaces yields a much higher initial deposition rate on the native oxide covered silicon. With increasing film thickness the growth rates approach each other and finally become identical for the same deposition conditions at a film thickness of about 35nm.

A spectrum recorded after about 10s of film deposition corresponds to a thickness of four angstroms or two monolayers. It shows a shift of the $E_0'+E_1$ peak in the real part of the refractive index to lower energy. This peak is attributed to localized interband transitions and therefore, the shift indicates a change in the band structure of the substrate material rather than long range changes in the film. This effect cannot be modeled using an a-Ge:H overlayer with voids, since these layers tend to decrease and flatten the peak heights rather than shift the peak positions. A model which can describe the observed effect is the formation of a $Si_{1-x}Ge_x$ ($x=0.12$) alloy at the surface, where the germanium atoms smooth out the remaining defects. The presence of a native oxide layer seems to prevent the formation of an alloy by separating the silicon surface from the reactive germanium species in the initial stage of the deposition process.

As we can see from the significant differences in the bulk film properties between films grown on native oxide covered and H-terminated surfaces, the different surface conditions not only affect the nucleation stage but have also an observable effect on the morphology of the entire film. Coalescence and growth of uniform film material starts at 1.6nm on H-terminated Si (111) substrates and at 3.5nm on native oxide covered silicon. For the H-terminated surface we find improved electronic, elastic and mechanical properties. The SFM measurements show that the surface roughness of the film depends not only on the growth rate, but also on the nature of the substrate surface and reaches ist smallest value of 1.8nm rms for the smoother H-covered silicon surface.

10:45am - 11:15am
WA4

Analysis of Stearic Acid Adsorbed on Silver Surfaces Using Optical Spectroscopic Techniques

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Silver (Ag)-filled conductive polymer adhesives have been widely used in a variety of microelectronic packages due to lower temperature processing and lower stress than inorganic eutectics. The particles in these adhesives, termed "Ag flake", are not pure Ag, but materials that contain various additives which are required during the processing stage and designed to improve the conductivity of the resultant epoxy adhesive. Lubricants such as stearic acid are used in the flake processing which leaves an insulative coating on the surface of the material. Interestingly, little attention has been focused on the chemical nature of the lubricant/flake interface, despite its role in developing conductivity in the cured polymer adhesive.

This study involves the vibrational analysis of a lubricant/flake system which is routinely used in Ag-filled adhesives. The investigation focused on the interaction between the lubricant, in this case stearic acid, and a silver surface using temperatures that are employed in the curing of the polymer adhesive. The chemical nature of the stearic acid/Ag surface was probed with two vibrational spectroscopies: (1) surface enhanced Raman scattering (SERS), and (2) IR-visible sum-frequency generation (SFG). In addition to chemical specificity, numerous studies have shown that both techniques exhibit surface sensitivity to interfacial processes such as adsorption and decomposition [1-3].

Ag particles were milled in a stearic acid/solvent system to generate flake samples of ellipsoidal geometry with dimensions ~ 1 μm by 10 μm and having a residual lubricant adlayer coverage of ~ 1.5 monolayers. SERS was used in the investigation since previous Raman studies of ellipsoidal and spherical shaped Ag particles have demonstrated a significant improvement in the surface scattering efficiency via the electromagnetic enhancing nature of the this geometry [4]. A standard Raman optical experimental arrangement was utilized in the measurements including a cw argon ion laser (488nm output) as the excitation source and a double grating monochromator for spectral analysis. The powder-like Ag flake was mounted in an optical cell that provided for sample heating.

The Raman spectra shown in Figure 1 were found to be typical of this particular flake/lubricant system. The vibrational features marked by the arrows (1) and (2) in Figure 1 represent modes in the scattered intensity that were not observed in the Raman spectrum of bulk stearic acid. The position of mode (1) was attributed to the Ag-O stretch, while mode (2) at 1392cm^{-1} was consistent with the symmetric stretch of an adsorbed carboxylate species (OCO). The presence of these two modes suggested the breaking of the O-H bond in the carboxylic acid end of the stearic acid molecule upon adsorption with the subsequent formation of a carboxylate species, which is consistent with earlier Raman studies of anhydride adsorption on Ag(111) [5].

The carboxylate group was unperturbed as the flake temperature was increased from 22°C to 130°C. Temperature increases above this point introduced broad and intense vibrational bands at 1405 and 1597 cm^{-1} which were assigned to amorphous carbon. Unfortunately, it was not possible to determine whether decomposition or the large Raman cross-section for the amorphous carbon was responsible for the loss of the carboxylate mode. However, the presence of the amorphous carbon indicated some degree of decomposition of the carboxylate species at the surface. Similar results were obtained with commercially available Ag-filled adhesives except that the amorphous carbon bands appeared at much lower temperatures. Although not shown, measurements in the C-H stretching region showed that the methylene chain in the surface species

was not strongly perturbed in this temperature range which implied that this part of the molecule was not involved in the decomposition.

The vibrational characteristics of stearic acid adsorbed on a smooth Ag surface were also examined using nonlinear optical SFG. The attributes and experimental requirements of this optical technique for surface investigations has been discussed in the literature [2,3]. Measurements involved the generation of an optical signal via nonlinear mixing of a high intensity, pulsed visible and IR laser beam at the stearic acid/Ag interface. The SFG signal, which had a photon energy equal to the sum of the two input sources, was resonantly enhanced when the frequency of the IR beam was tuned through a Raman and infrared active vibrational mode in the surface adsorbate. Figure 2 shows the SFG spectra versus the IR frequency for the room temperature stearic acid/Ag surface system. The features observed in the spectrum were associated with the C-H stretches in the terminal methyl (2,3) and adjacent methylene group (1) of the molecule. Similar to the SERS results, the vibrational features in the SFG spectrum were unperturbed until ~ 150°C. Above this temperature, a marked, irreversible decrease was observed in the vibrational intensity of the C-H stretches. The C-H features, however, were still observed in the SFG signal which indicated that a portion of the stearic acid layer was still adsorbed on the surface.

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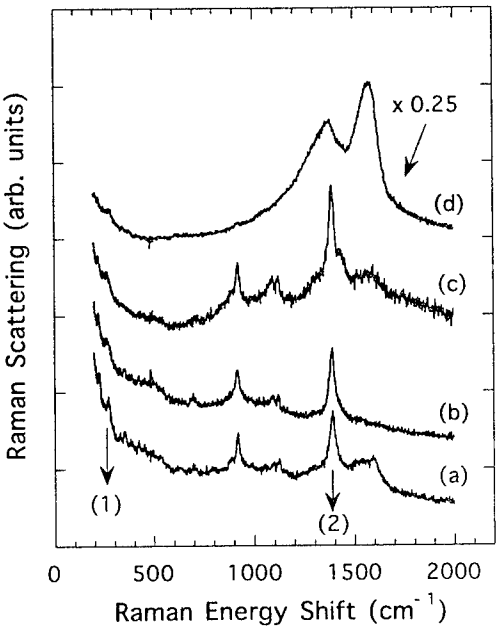


Figure 1. SERS spectra from a lubricant/Ag flake system recorded at (a) 22, (b) 60, (c) 130, and (d) 150°C. Modes (1) and (2) are associated with a surface carboxylate species.

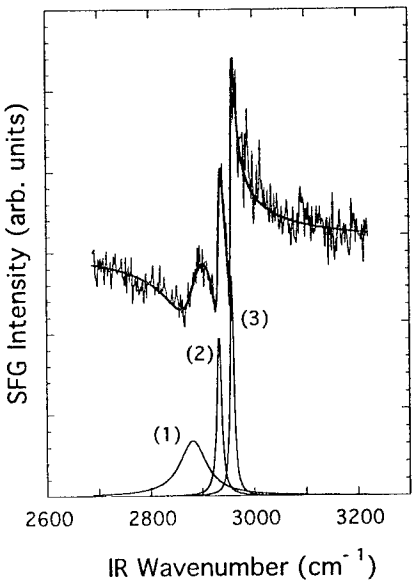


Figure 2. SFG spectrum and fit (solid line) for stearic acid adsorbed on a Ag film. Modes (1), (2), and (3) are associated with the terminal methyl and adjacent methylene groups in the surface species.

11:15am - 12 noon (Invited)

WA5 # Digital etching of GaAs - the mechanism and the application-

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Recent progress of nano-meter devices and ULSI requires us development of etching and epitaxy technology with atomic scale controllability. Since etching depth is basically a function of etching time, etchant gas flow, temperature and etching product etc, the precise control of those parameters are indispensable for achieving the atomic scale controllability. Recently, new technology of etching in which self-limiting mechanism is included has been developed[1], namely digital etching. In this technology, the etching rate is exactly controlled in atomic scale without any precise control of etching parameters. The etching rate is independent of etching time and etchant gas flow rate due to the self-limiting mechanism of etching.

In this paper, photo assisted digital etching using tunable DUV laser[2] is introduced and the mechanism of the digital etching is discussed.

Figure 1 shows schematic diagram of digital etching procedure. In our experiment of Ga As, etchant of Cl gas is fed onto the substrate as the first step. To realize monolayer adsorption of the etchant and to purge out residual etchant in a reactor, a purging time is set up as the second step. We can expect that after monolayer adsorption of the etchant on the substrate, the back bond of the surface atom is weakened due to the charge transfer from the surface of the substrate to an etchant molecule. As the third step, energetic beam like photon is introduced to attack and break the back bond and to form a vaporizable product. And as the 4th step, the product is purge out to complete one etching cycle to realize one monolayer etching identically. In this experiment a tunable DUV laser is used as an energetic beam to understand the mechanism of the etching.

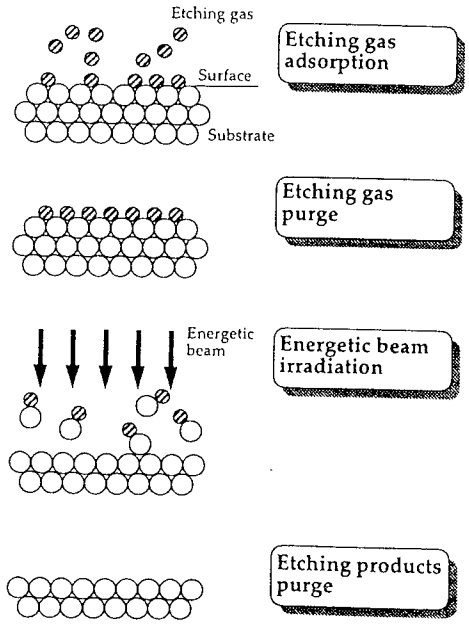


Fig. 1. Schematic diagram of digital etching.

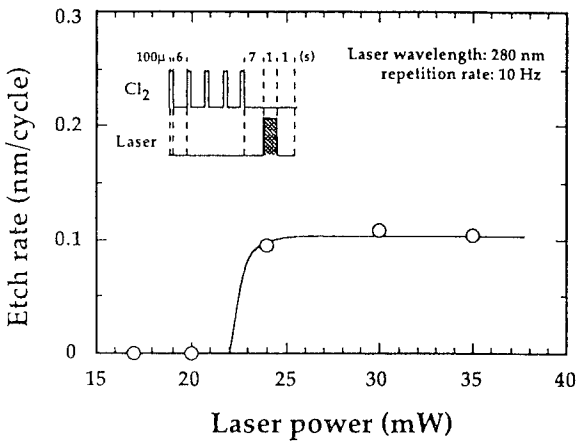


Fig. 2. Light intensity dependence of the etching rate.

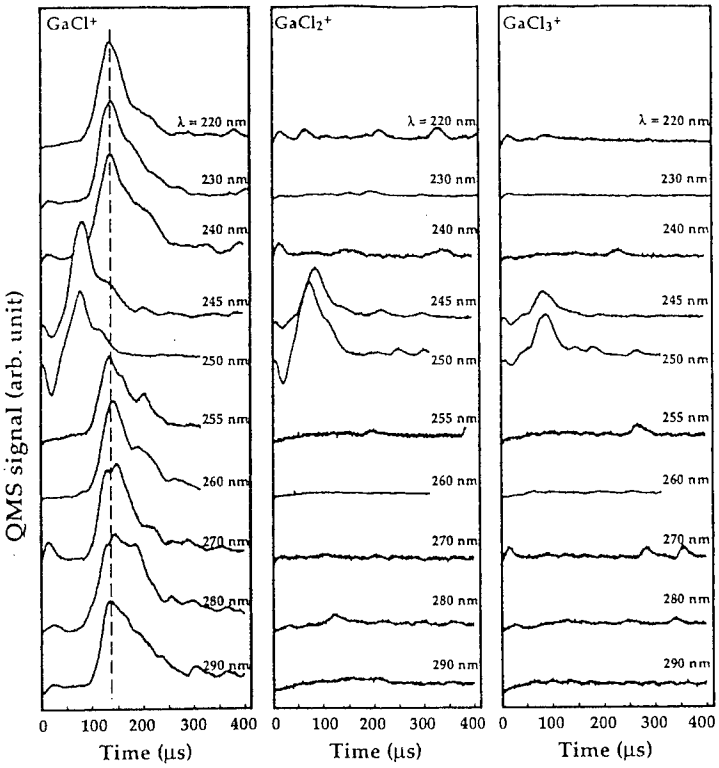


Fig. 3. Wavelength dependence of etching products.

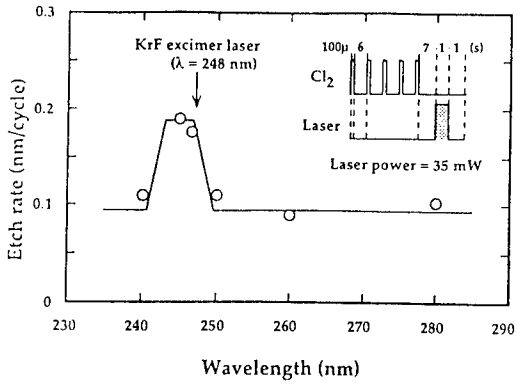


Fig. 4. Wavelength dependence of the etching rate.

Figure 2 shows the etching rate of GaAs as a function of light intensity at a wavelength of 280 nm. The etching rate saturates clearly at 1/3 monolayer /cycle. Feeding rate dependence of etchant gas on the etching rate shows us that the etching rate also saturates at 1/3 monolayer /cycle independent of the feeding rate.

Figure 3 shows the etching rate of the GaAs as a function of the wavelength of incident laser. As shown in this figure, etching rate depends on the wavelength. Near the 245 nm the etching rate is 2/3 monolayer /cycle but in other region the etching rate is 1/3 monolayer per cycle.

Figure 4 shows the wavelength dependence of the etching product observed using quadrapole mass analyzer. In the wavelength region around 245 nm the product related Ga is $GaCl_3$ but in other region the product is GaCl. This wavelength dependence of the product seems to related to the wavelength dependence of the etching rate. These etching characteristics also depend on the substrate type and the crystallographic orientation. In addition to those, the etching characteristics also depend on the beam used, that is, photon beam[3], electron beam[4],or ion beam[5] .
Details of the mechanism will be discussed in the conference.

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5:15pm - 6:00pm (Invited)
WB2

Tailoring of Chemical, Morphological, and Mechanical Surface Properties of Materials with Laser Radiation

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Microelectronics is largely based on metal-oxide-semiconductor field effect transistor technology. For example, complementary metal oxide semiconductor applications are the mainstream of current microelectronics markets with a 75 % market share. The continuous decrease of transistor channel lengths results in improved performance of transistor parameters (cut-off frequency and transconductance) and increases the packaging density for integrated circuits. Feature sizes down to the 200- or even 100-nm range will be necessary for 1-to-4-Gbit devices [1]. The reduction of critical dimensions, however, imposes strict requirements on lithography, etching and other process equipment. Techniques capable of lateral resolution down to tens of nanometers such as electron beam lithography and scanning tunneling microscopy are still not cost-effective and lack the output capacity for industrial applications. Thus, the disparity between the mask layout dimensions and the final device geometry is a problem for processes used for ultralarge-scale integration. Consequently, new processes must be found to overcome these problems.

The situation in microsystem technology, which has been the subject of intensive research since the 1980s, is similar to microelectronics. Various approaches have been followed in its development, such as sophisticated semiconductor technology using silicon, the LIGA (German acronym for Lithography (lithography), Galvanoformung (electro-forming), Abformung (moulding)) technique applied to a wide range of working materials, or interconnection of functional components to a combined hybrid integrated component on a common substrate base. The dimensions of the generated microsystems are ranging from the nm to the mm scale depending on the method of manufacturing and on the type of application [2].

The continuing increase in levels of integration in microsystems and in operational speeds will demand more compact and higher density packaging and interconnection schemes even during the 1990s and beyond. Consequently, the overall trend is towards integrated packaging of the functional components. Three-dimensional stacking of packaging onto a larger substrate mother board most likely will become a reality. All of these trends pose a challenge to develop new materials and processing techniques [3].

Another big challenge will come with the growing introduction of optical technology. This introduction is expected to be gradual, with a mixture of electronic and optical components. There will be a need for interconnection between optical fibers and devi-

ce packages, which may include optoelectronic components, electrooptic devices and optical waveguides, as well as verly large-scale integrated chips, capacitors, resistors, and conductors [3].

In the last several years there is a very fast development of microsystem technology, which is characterized by specific features such as the high density of integration of the single elements, 3D integration of the elements in the hybrid system, the use of new materials having specific properties, and overall miniaturization of the system as well. Particularly, the development of new processes for microprocessing of technical materials is the basis for an increasing integration and therefore miniaturization of structural, optical, and electrical components. Most important is the reduction of the number of production steps and a faultless production. During the past few years, besides integration and miniaturization, also a tendency towards high precision processing of surfacess is observed [4].

Particle and photon beams have begun to take over important roles in the fabrication of microsystems [5, 6]. This is natural, because as the demands of microfabrication escalate, the need for greater spatial and temporal control of the processing environment increases: i. e. by directed processing in a manner not possible by immersion of a material in a conventional isotropic liquid or plasma. Processing of materials with directed energy beams can be used to generate spatially confined, anisotropic features. Especially, the use of chemically specific energy beams within microelectronic and optoelectronic application has matured significantly within the last years.

Several of the recent advances of laser processing such as the removal of matter by thermal and non-thermal processes including etching, the production of vias, the deposition of multilayer thin films, and the photoresistless pattering by direct and indirect processing techniques are illustrated for tailoring the chemical, morphological, and mechanical surface properties of materials.

For example, the four primary techniques currently used to form vias are wet etch, reactive ion etching, photosensitive polymer lithography, and laser ablation, which have been used within the microelectronics industry. Laser ablation involes the fewest steps (application of the polymer, curing, ablation, and plasma treatment for debris removal) and is, therefore, the quickest method of via formation [7]. Furthermore, laser ablation is the only dry process of the four. Both reactive ion etching and wet-etch are process-intensive and expensive when compared to the laser alternative. Photosensitive polymer lithography technique is probably the next best option, after laser ablation, for forming vias, although the limited choices and high cost together with the half-barrel shape of the vias so formed limit the usefulness of the technique.

Following the requirements for present microsystems the necessary resolutions are restricted to about 100 Å in vertical direction and to higher than 10 µm in lateral direction, respectively. It appears that laser radiation has now found confirmed applications in the prototyping stages of device engineering and is now on the edge of also becoming a cornerstone technology in manufacturing of leading-edge devices.

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6:15pm - 7:00pm
WB3

Tissue Ablation as a Function of Laser Pulsewidth

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Laser ablation of optically transparent materials begins with laser-induced breakdown (LIB). Ablation of material occurs when the incident laser irradiance is greater than the LIB threshold, where rapid vaporization takes place. LIB has been studied extensively since it imposes a fundamental limit of power output from a laser system due to its ability to damage laser components [1]. However, LIB can be used in applications such as laser eye surgery, where tissues targeted for treatment are transparent and accessible to wavelengths of the visible spectrum [2].

For any given material, the laser fluence threshold for LIB depends on the pulsewidth. Major efforts have focused on determining the LIB threshold as a function of the laser pulsewidth [1]. Previously, for pulsewidths from nanosecond down to ~ 10 ps, the fluence threshold for the material has been shown to be proportional to the square root of the pulsewidth [3]. These findings suggested that ablation with shorter pulsewidths would require progressively less energy and generate correspondingly smaller acoustic shock waves that are believed to create collateral damage. Recent reports have challenged this scaling law relationship [4], however femtosecond laser ablation in absorbing materials still suggest that such limitation of collateral effects may indeed by possible [5].

We used a titanium:sapphire ultrafast laser system to produce ablation of human and mouse tissue. Specimens were exposed to increasing fluences at pulse widths from 100 femtoseconds (fs) to 7 nanoseconds (ns). Laser-induced breakdown fluence thresholds at each pulsewidth were determined by monitoring plasma emission due to individual pulses. Ablation of excised tissue was then performed using multiple shots and the ablation threshold and cutting depth at each pulsewidth were determined histologically. Threshold parameters for histologically observable ablations were then used to create incisions in live animals, which were followed up to three weeks to assess wound healing.

Laser-induced breakdown fluence thresholds for tissue decrease by the square root of the pulse width, as the pulsewidth is reduced from 7 ns to approximately 10 picoseconds. Fluence thresholds vary little as pulse width is further reduced below 10 picoseconds. However, breakdown for pulse widths below 10 picoseconds show little intershot variability, resulting in precise fluence thresholds. When examined histologically, tissue ablations using multiple shots

showed similar fluence thresholds over the entire range of pulsewidths examined. The highest cutting efficiency measured histologically occurred at pulse widths with the lowest and most precise ablation thresholds, at near threshold fluences. Histologic and biochemical measures of wound healing revealed significantly less collateral tissue damage associated with ultrashort pulsewidths.

We conclude that ablation of biological tissue shows pulsewidth dependence. At pulse widths less than 10 picoseconds and with fluences near the breakdown threshold, tissue ablations are maximally precise and efficient, resulting in limited collateral tissue damage when compared to longer pulsewidths.

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ADVANCED APPLICATIONS OF LASERS IN MATERIALS AND PROCESSING

Thursday, August 8, 1996

SESSIONS:

ThA: Fabrication

ThB: Processing

Laser Induced Formation of Adherent Interfaces

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There has been a considerable effort in recent years to develop adherent coatings especially in high thermal expansion coefficient mismatched systems[1]. One of the technologically significant thermal expansion coefficient mismatched systems constitute diamond coatings on substrates like steel, WC with (≥ 10%) cobalt. Diamond coatings on these materials are expected to have widespread applications as cutting tools and corrosion and erosion resistant coatings. Although a wide variety of techniques have been applied to improve adhesion, the growth of diamond thin films on these substrates, especially on steel substrates have at best met with very limited success. The main problem for the deposition of diamond thin films on these materials stresses is the high thermal stresses generated during the deposition process. The magnitude of the thermal stresses σ_{th} scales with the difference in coefficient of thermal expansion given by

$$\sigma = E(1-\nu)\int_{T_\infty}^{T_s}(\alpha_f-\alpha_s)\,dT$$

where, E is the Young's Modulus of the coating, ν is the Poision's ratio, and $(\alpha_f - \alpha_s)$ corresponds to the difference in thermal expansion coefficients of substrate and coating. The integral represents the thermal expansion mismatch between the diamond film and the substrate Based on linear strain of ~ 0.25 % for WC and~ 0.8 % for steel, and taking typical values of E(1-ν) for diamond to be approximately 1000 GPa , the magnitude of the stresses in these systems can range from 2.5 GPa to as high as 8.0 GPa . Thus, high bonding strength is necessary for obtaining adherent coatings.

Methods to increase the adhesion strength in diamond coatings particularly on steel substrates have not been particularly successful. One of most common methods to enhance adhesion is to apply interlayers possessing intermediate thermal expansion coefficients. Some of the interlayers which have been explored for diamond films on steel substrates are tungsten, molybdenum, silicon, tantalum, silver etc. However these methods have only been partially successful chiefly because the residual stresses are still high enough to debond from the film.

In this paper we report a novel laser-based method to increase the adherence of coatings on high thermal expansion mismatched substrates[2,3]. This method is based on morphological surface modification of the substrate, which results in the creation of a three-dimensional thermal and composition graded interface. The laser induced microrough structures (LIMS) possess surface

areas which are up to an order of magnitude higher than the original surface. The second phase is deposited on the surface using thin or thick film deposition methods. The increase in interfacial area, and the modification of interfacial stress significantly improves the interfacial adherence of the film. Results of diamond films grown on 418 steel and tungsten carbide (with 10% Co) substrates have been presented. Scratch and indentation tests on diamond coated samles on steel and tungsten carbide donot exhibit film fracture at the interface and concomitant catastrophic propagation of the interfacial crack. The critical load for indentation based facture was found to exceed 150 Kg for diamond films deposited on steel and WC substrates. These results are in sharp contrast with indentation tests conducted on diamond films coated on un-modified surfaces.

Laser induced surface modification has also been applied to develop a new class of materials termed as "*surface composites*". In this engineered material, the second phase is spatially distributed in the near surface regions, whereas the phase composition is linearly graded as a function of distance from the surface. Surface composites are different from existing engineered materials such as "bulk composites" and "functionally graded materials" (FGM). Unlike bulk composites, the surface phase in surface composites is present only at the near surface regions. In contrast to FGM, the graded properties of surface composites are achieved by unique morphological surface modification of the bulk phase. To fabricate surface composites, the initial surface of the bulk material is transformed using a novel multiple pulse irradiation technique into truncated cone-like structures. The laser induced microrough structures (LIMS) possess surface areas which are up to an order of magnitude higher than the original surface. The second phase is deposited on the surface using thin or thick film deposition methods. Example of various types of surface composites such W/Mo, alumina/SiC, silica/silicon carbide and diamond/WC(Co) are presented in this paper.

Finally, this paper will deal with the mechanisms for creation of LIMS structures . LIMS are also a by product of laser ablation process and are created during multiple pulse irradiation on the surface of the material. Experiments were conducted on a wide variety of materials to understand the mechanisms for generation of the microrough structures. The LIMS structures were found to have the following characteristics : (a) the structures pointed in the direction of the laser beam, (ii) were formed in a certain energy window near the threshold for ablation process (iii) optimum number of pulses were required for the evolution of these structures (iv) periodicity of the structures was related with the gain size variation in the thin films. Based on these experimental observations, a model based on non- spatially uniform etching of the surface was developed.

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9:15am - 9:45am
ThA2

Excimer Laser Assisted Deposition of Metal Films on Aluminum Nitride

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Lexington, KY 40506-0046

Aluminum nitride (AlN) is a high thermal conductivity ceramic substrate for microelectronics with a better thermal coefficient of expansion match to silicon than traditional aluminum oxide substrates. Metallization techniques are needed to increase the ease of use of AlN as a substrate for high power circuits, high frequency devices, and multichip modules. Excimer laser assisted deposition of copper and aluminum addresses the need for repair and customization of interconnects, as well as a patterning technique for defining circuit features without photolithography. A KrF (248 nm) laser system with motion control stages, vacuum chamber, and heated stage, is used to decompose AlN to an aluminum rich metallic seed layer for laser induced chemical vapor deposition and electroless copper plating.

The laser modified surface has a sheet resistance of 20-30 Ω/□ (1-1.5 kΩ for a 100 μm X 5 mm line) when processed in vacuum and the resistance increases with increasing scan speed and decreasing laser fluence. Preliminary XPS data for the decomposed surface shows that the laser has depleted nitrogen from the substrate. Laser assisted CVD has been accomplished by two processing sequences. In a two step sequence, the seed line is produced in vacuum followed by a second laser pass with trimethylaluminum (TMA). The substrate temperature during the deposition pass is less than the thermal decomposition temperature of TMA to prevent deposition on other areas of the substrate, thereby promoting selective area deposition. Table I summarizes resistance values for a seed pass in vacuum, seed pass and deposition pass in vacuum, and seed pass in vacuum followed by a deposition pass with TMA. The decrease in resistance with the addition of TMA shows that deposition is occurring. A single laser pass with TMA produces a line with similar resistance values by direct writing aluminum. Figure 1 shows sheet resistance values for laser decomposed seed lines versus direct write lines for several scan speeds. Both sets of lines were produced with 2.1 mJ/pulse at 5 Hz and a substrate temperature of 120°C. The seed lines were processed in 10^{-4} Torr vacuum and the direct writing was done in 2 Torr TMA.

Electroless copper films are plated on the laser decomposed AlN using Shipley Cuposit 328 plating system. Laser processing involves four passes at 5 μm/sec with a 100 μm square beam in 3 X 10^{-3} Torr vacuum. The laser fluence was approximately 15 J/cm^2 at 10 Hz. Contact pads were patterned at the ends of the test lines by rastering the beam. The seed line has a resistance of ~1 kΩ for a 100 μm X 5 mm line. After immersion in the plating bath, copper particles were observed within ten minutes and a continuous line was formed in two hours with a resistance of ~1Ω (0.2 Ω/□). Several line widths were produced by overlapping the 100 μm wide beam and the growth rate was approximately 1.5 μm/hour in each case. The line width also increased with increased deposition time, as shown in Figure 2. Lateral growth is an important consideration for designing precise pattern dimensions. Complex shapes, such as microwave devices have also been produced by laser patterning the desired outline and rastering the interior.

Table I. Line resistance values for laser assisted chemical vapor deposition of Al on AlN.

Laser Pass	Scan Speed (μm/sec)	Pulse Energy (mJ/pulse)	Substrate Temp. (°C)	Pressure (Torr)	Resistance (Ω)	Sheet Res. (Ω/□)
Seed Line	750	2.85	25	10^{-4}	1600	32
Seed Line + Dep. Pass without TMA	750 10	2.85 0.2	25 120	10^{-4} 10^{-4}	890	18
Seed Line + Dep. Pass with TMA	750 10	2.85 0.2	25 120	10^{-4} 2	460	9

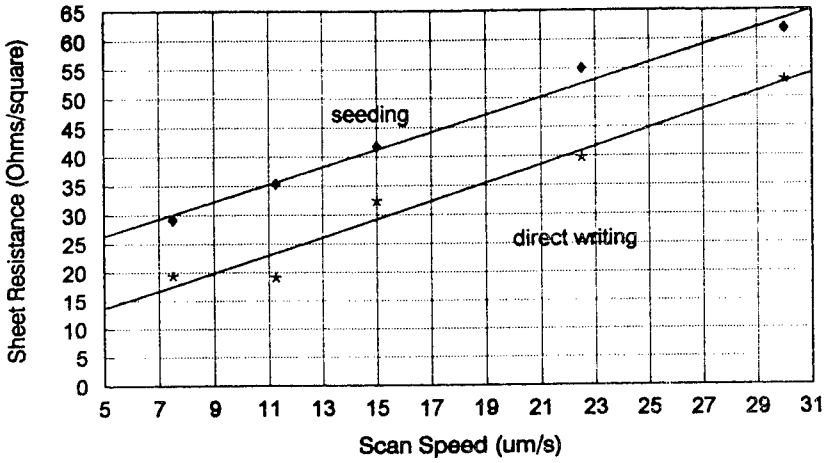


Figure 1. Sheet resistance versus scan speed for KrF laser decomposed seed lines and direct write deposited lines on aluminum nitride.

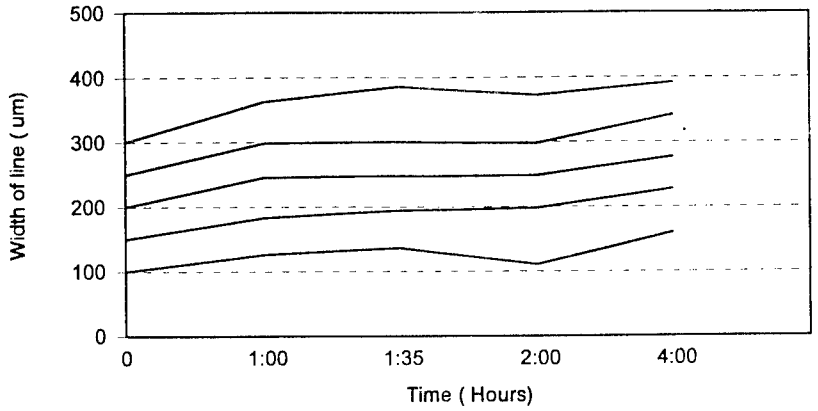


Figure 2. Increasing line width with increasing deposition time for KrF laser decomposed AlN immersed in electroless copper plating solution.

Deposition of Copper-Phthalocyanine Thin Films by Laser Ablation and Its Application for an Organic Electroluminescence Device

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Various functions of organic materials in electronics and optics have been received much attentions. Because of the excellent controllability offered for laser ablation deposition technique in thin film fabrication processes and its applicability for a wide range of materials, laser ablation processes are suitable for fabricating new material structures of different types of materials with nanometer-size resolution, such as complex systems consisting of organic and inorganic components. We experimentally studied the fabrication of copper-phthalocyanine (CuPc) thin films via KrF laser ablation. In contrast to organic polymer thin film formation[1)-3)], where the monomer generation through unzipping processes in the target followed by the repolymerization on the substrate results in the successful film production, reconstruction of original molecular structure through surface chemical reactions from various types of small fragments generated in the laser ablation does not work for non-polymer materials. In fact, none of original structure is observed in FTIR spectroscopy, when a CuPc target is ablated at relatively high laser fluences (>10x laser ablation threshold fluence of ~20 mJ/cm^2 with KrF laser). Successful fabrication is obtainable for CuPc at laser fluences near the ablation threshold, although a slight reduction in nitrogen is still observed[4)].

The CuPc thin films fabricated via KrF laser ablation exhibit a poor crystallinity. We tried to improve the crystallinity with two different techniques. One is elevation of the substrate temperature. It is noteworthy that presumably due to the higher kinetic energies of fragments in the laser ablation, significant improvement was observed only at 325 K. Further increase in the substrate temperature resulted in extremely low film deposition rates. Second method is irradiation of the substrate with a weak HeNe laser beam, of which wavelength of 633nm corresponds to the absorption band of CuPc. Clear improvement in the crystallinity was obtained at HeNe laser power ranging 25-500 μW/cm^2. A comparison in the XRD spectra obtained with and without the HeNe laser irradiation at the substrate temperature of 300 K is shown in Fig. 1. Electrical excitation may enhance surface chemical reactions and migration for constructing the uniform film structure. This secondary excitation scheme with a weak cw laser beam will enable one to obtain a selective growth of the crystalline films at a specific position excited by the laser with a submicrometer resolution.

We applied this organic thin film fabrication technique via laser ablation for constructing a Schottky diode, and a double-layer electroluminescence (EL) cells consisting of a CuPc layer and an aluminum tris-8-hydroxyquinline (Alq_3) layer as a hole-transport and a luminescent layer, respectively, as shown in Fig. 2. During the fabrication of EL cells, neither of the methods for improving the crystallinity was used, since the crystallinity is not necessarily required for a hole-transport layers. Compared with those fabricated via vacuum evaporation technique, characteristics of these devices proved that the organic thin films fabricated via the laser ablation can maintain its electrical properties.

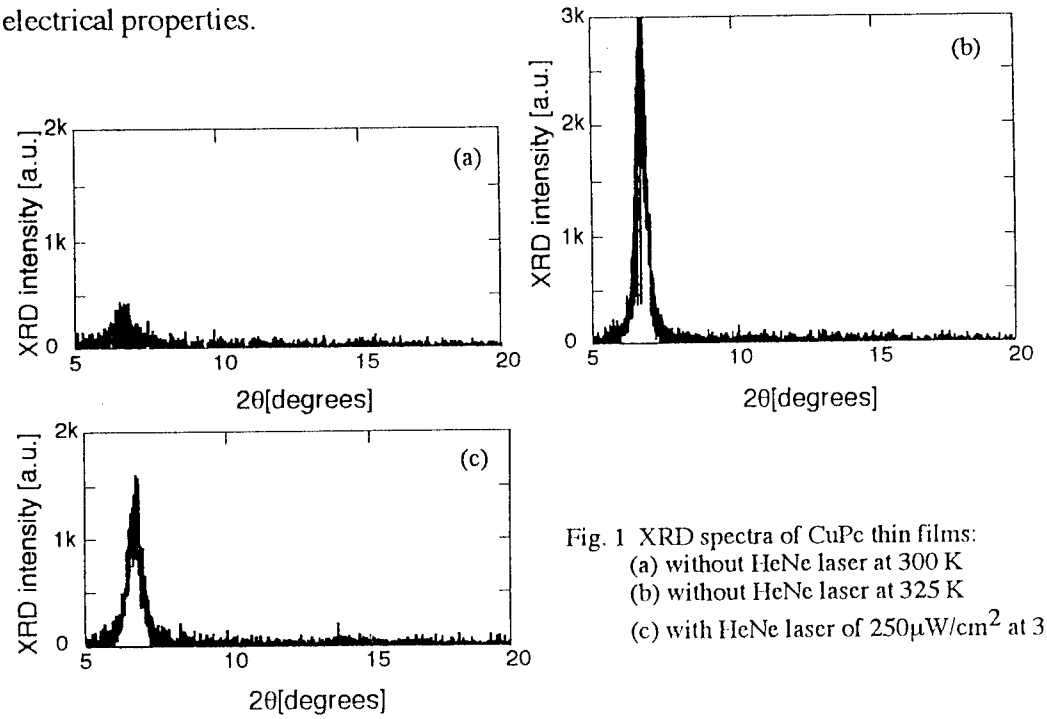


Fig. 1 XRD spectra of CuPc thin films:
(a) without HeNe laser at 300 K
(b) without HeNe laser at 325 K
(c) with HeNe laser of 250μW/cm^2 at 300 K

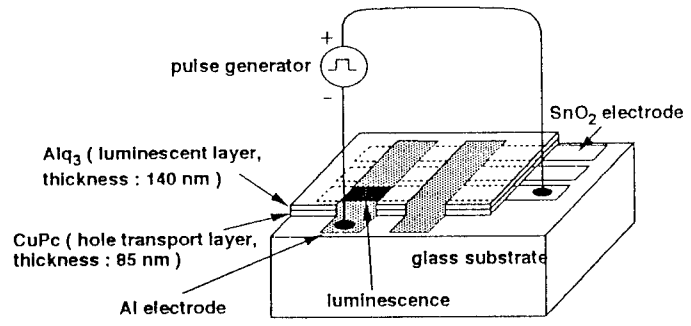


Fig. 2 The structure of CuPc/Alq_3 double layer EL cell.

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10:45am - 11:15am
ThA4

Aluminium Nitride Film Fabrication: Reaction and Diagnostics of Laser Evaporated Al in NH_3 Atmosphere.

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Hard coating materials are becoming increasingly important for many engineering applications. These materials range from diamond like carbon DLC to refractory compounds such as carbides and nitrides. Nitrides of high melting transition metals are referred to as refractory hard metals. The non-metallic compounds are corrosion and heat resistant ceramic type materials with semiconductor properties. Pulsed laser ablation has been applied successfully to deposit thin film from nitride target of various elements [1-4]. A method to prepare nitrides by adding gaseus ammonia to laser evaporated elements has been developed in our laboratory. This method is at present applied in our laboratory to prepare III-IV group nitrides [5].
The intermediate steps in nitride production have been examined by optical emission measurements and by mass spectrometry of the gas phase [6]. Optical imaging of the plume expansion in vacuum and in the presence of added ammonia was studied by a fast quartz window equipped ICCD camera. The plume emission spectroscopy was studied by an optical multichannnel analyzer. The mass spectra of the pure element target plume in vacuum and in presence of NH_3 reacting gas were measured by KrF or frequency doubled Nd-YAG laser ablation in combination with supersonic expansion and laser photoionization [7]. The thin films obtained from the element target plume in the presence of NH_3 were examined by conventional tecniques. It is reported in the present summary the results obtained by diagnostics of the reaction of laser evaporated Al with NH_3.
Typically the plume imaging from a bare Al target in vacuum shows distinctive features which appear at early stage after the laser pulse. The analysis of the plume expansion by means of band pass filters shows a faster component (8 10^6 cm/sec) and a slower one which stays back (1.6 10^6 cm/sec) The OMA spectroscopy analysis shows that the fast part of the plume is formed by Al

positive ions and the slow plume component by Al neutrals. Plume imaging has been carried out also in the presence of added NH_3.In the presence of NH_3 the aluminium plume is constrained in a small volume and the maximum of the emission intensity goes to the front [5]. This suggest that the density of the excited species at the front edge increases owing to the increased number of collisions. It would be tempting to confirm that this may be related to the reaction of Al with NH_3. A spectroscopic analysis is in progress to answer this important question.

Reaction of the Al plume with NH_3, examined with a Smalley type vaporization source followed by laser ionization, in the case of Al and NH_3 mixture, leads to the formation of $Al_n(NH_3)_m$ clusters. Similar experiments of laser-induced fluorescence (LIF) have been used to detect AlN diatomics [8]. Other systems such as B, In, Si, and Ge with NH_3 have been studied.

The films fabricated by this method have been characterized by Auger, EDX, Scanning Electron Microscopy (SEM), and X-ray Diffraction spectra. Highly oriented films of nitrides of these elements on several substrates have been identified as a function of laser fluence and substrate temperature. The effective mechanism which leads to thin film deposition through III-IV group elements and ammonia nitridation is not yet clear. A gas phase process or a gas-solid reaction on the substrate surface are discussed in terms of the gas phase composition and of the process parameters affecting the film growth. EDX and IR analysis of films confirm the formation of AlN. A fairly dense homogeneous texture with a columnar microstructure of AlN films grown on Si (100) is observed from SEM pictures. X-ray diffraction patterns of AlN films on Si (100) show AlN (100) with a high degree of preferential orientation with no other contributions [5].

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11:15am - 11:45am
ThA5

LITHIUM CHARGING CAPACITIES OF VANADIUM OXIDE THIN FILMS GROWN BY PULSED LASER DEPOSITION FOR RECHARGEABLE Li BATTERY APPLICATIONS

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This research was supported by the Advance Battery Project, Chemical Sciences Division, USDOE.

INTRODUCTION

Vanadium oxide has significant potential as the Li storage electrode in high energy density rechargeable Li batteries. We present results of the charge capacity and stability of vanadium oxide thin films deposited at various temperatures and ambient atmospheres by pulsed laser deposition from a sintered target of V_6O_{13}. The charging capacity of the films was measured by cycling the films in an electrochemical cell. The PLD films showed a capacity loss of as little as 2% after 100 cycles far exceeding films deposited by other methods.[1,2]

EXPERIMENTAL

The chamber consists of a 12" spherical cross with Neocera 6-target rastering carousel and a 2" diameter resistance heater. The ablating laser is a Lambda Physik EMG 103 excimer laser (KrF, 248 nm) and laser fluence was held between 340 - 420 mJ/pulse at a repetition rate of 20 Hz. The focused beam hit the target with ~12 J/cm^2 at a 45° angle of incidence. The substrates, SnO_2 on glass, were mounted onto the heater with silver paint and were ~10 cm directly in front of the target.

There are two sets of films. In the first set, all films were deposited in vacuum at temperatures ranging from 25-400°C. In the second set, the deposition temperature was 200°C and ambient atmospheres were O_2/Ar mixes.

Films were characterized for crystallinity by x-ray diffraction (XRD), for stoichiometry by x-ray photoelectron spectroscopy (XPS), and for charging capacity by electrochemical measurements. The vanadium oxide films were cycled between 4.1 - 2.0 volts and 4.1 - 1.5 volts in an electrochemical cell using 1 M $LiClO_4$ in propylene carbonate as the electrolyte. Lithium metal was used as the reference and counter electrodes.

RESULTS

Films deposited in vacuum or pure Ar were dark brown in color and adhered well to the substrate. Conversely, films deposited in O_2 or an O_2/Ar mix were yellow in color and very soft and powdery and did not adhere well to the substrate. Thickness measurements were difficult due to the stylus of the DekTak profilometer grooving the film. X-ray diffraction measurements showed that the films were amorphous with the exception of some crystallinity appearing in films which were post-annealed in O_2. The oxygen:vanadium ratio of the as-deposited films ranged from 0.95-2.62. The charge capacity and O:V ratio results of the films deposited in vacuum at various temperatures are listed in Table 1. Between 200-300°C, all of the films had roughly the same capacity when cycled between 4.1-1.5 volts; therefore, the optimum deposition temperature for these films was taken as 200°C. The second set of films were grown at 200°C in O_2/Ar atmospheres.

Table 2 tabulates the results of the films grown at 200°C in O_2/Ar atmospheres. The deposition rates varied widely with chamber pressure. V9 was deposited onto a substrate which had been sputtered with a 100Å layer of Cr in an attempt to increase the deposition rate. It did not appear to affect the deposition rate or the charge capacity. Figure 2 shows the voltammograms of the cycled vanadium oxide films. Film V10's crystallinity was maintained throughout the charging cycle as indicated by the abrupt shoulders.[3] Film V8 was initially crystalline and became

Table 1: Charge capacity and O:V ratio of films deposited in vacuum at various temperatures by PLD.

Film	Dep. Temp (°C)	Charge Capacity (mC/cm^2/1000Å thick film)	O:V Ratio
V1	25	0.001	0.95
V2	100	0.003	2.0
V3	150	15.2	n/a
V4	200	31.2	1.6
V5	225	26	n/a
V6	300	25	1.53
V7	400	1.7	1.7

Figure 1: Charge Capacity vs. Deposition Temperature.

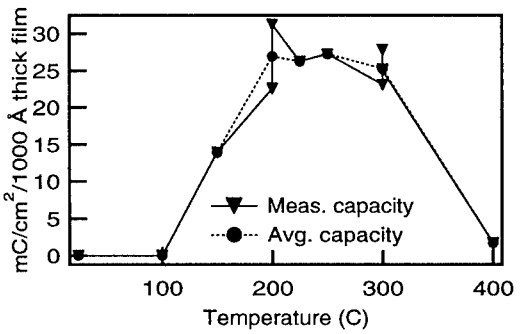


Table 2: Charge capacity, degradation rate, and O:V ratio of films deposited at 200°C in various O_2/Ar atmospheres. The degradation rate/cycle was calculated after 100 cycles.

Film	Chamb Pres mTorr	%Ar	$\%O_2$	Film Thick Å	Charge Capacity ($mC/cm^2/1000Å$) 4.1-2.0V	Charge Capacity ($mC/cm^2/1000Å$) 4.1-1.5V	Degradation Rate (%/cycle) 4.1-2.0V	Degradation Rate (%/cycle) 4.1-1.5V	O:V Ratio	Other treatment
V4	vac	0	0	3100		31.2		0.02	1.6	
V8	100	100	0	900		15.6		0.6	2.62	
V9	50	100	0	800	27.6	11.4	0.26	5	2.33	100Å Cr on substrate
V10	100	90	10	1000	26.1	15.8	0.2	5	2.13	
V11	20	0	100	1500	31.0	23.5	0.15	0.43	2.25	1.6 sccm O_2
V12	vac	0	0	1800	25.0	25.1	0.39	0.4		Annealed in 20 Torr O_2 at 350°C, 3 hr

amorphous over the course of 100 cycles. Film V9 was amorphous throughout the cycling as indicated by the smooth curves lacking abrupt shoulders. Figure 3 plots Charging Capacity vs. Number of Cycles for V10 and V12. Both films were crystalline before and after cycling. V12 shows similar curves for the 4.1-2.0 V and 4.0-1.5 V cycles; however, V10 exhibits significantly different behavior for the two tests.

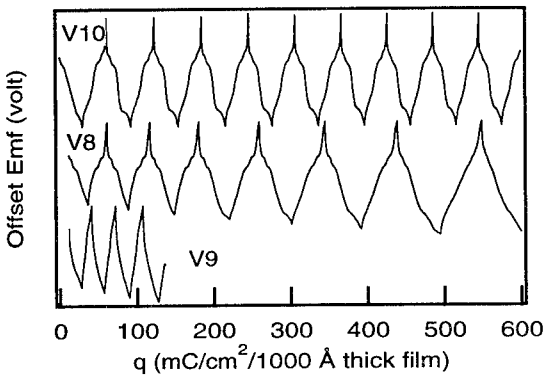


Figure 2: Voltammograms of the cycled vanadium oxide films. Abrupt shoulders indicate crystallinity as seen throughout cycling in V10.

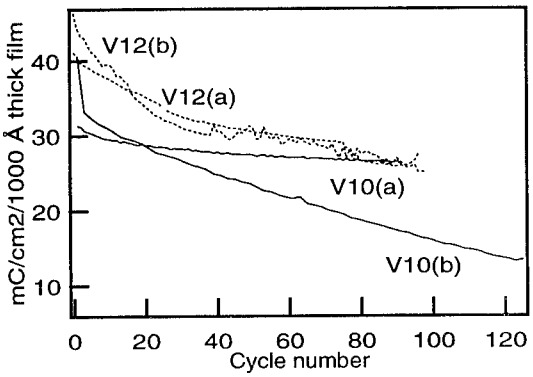


Figure 3: Charge Capacity vs. Number of Cycles for V10 (1000Å) and V12 (3100Å). (a) 4.1-2.0V, (b) 4.1-1.5V. Both films retained crystallinity after 100 cycles.

CONCLUSIONS

We have demonstrated the pulsed laser deposition of vanadium oxide thin films with significant charge capacities and excellent stability. The charge capacity is most heavily dependent on the substrate deposition temperature and chamber pressure and not on the stoichiometric ratio of oxygen to vanadium. Films deposited by PLD were superior to other deposition methods. The best film in this paper lost only 2% capacity compared to 10% or more for films deposited by other methods. The degradation of the PLD films can most likely be attributed to loose particles being removed from the film surface for the soft, powdery films and the destruction of the initial crystallinity of the films during the charge/discharge cycling.

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11:45am - 12:15pm
ThA6

Theoretical and experimental investigation on laser dry cleaning of particles from substrate surfaces

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I. Introduction

In order to develop laser cleaning technology to meet the need of industry, it is very important to investigate the cleaning efficiency and mechanism of this cleaning technology. Theoretical and experimental investigation on laser dry cleaning of particles from substrate surfaces will be discussed in this paper.

II. Experimental Results

A KrF excimer laser is used as a light source for laser cleaning. The laser beam after passing through an aperture is directed by a mirror and focused by a quartz lens on substrate surfaces. The substrate surface before and after laser irradiation was observed by an optical microscope and a scanning electron microscope (SEM).

It was found that there is a similar trend for the dependence of laser cleaning efficiency on laser parameters for removing different types of particles. Laser cleaning efficiency increases with increasing laser fluence or pulse number, but does not depend on repetition rate up to 30 Hz which is the limit of excimer laser used in this study.

III. Mechanism and Discussion

Since the predominant adhesion force for tiny particles on a dry surface is Van der Waals force, this interaction can be simulated by a "spring" between the particle and the surface. When a laser beam irradiates on the substrate and particle surface, the substrate surface and particles absorb excimer laser energy and causes fast thermal expansion, laser also induces a transient light pressure to particles, which all result in depressing the "spring" and leads to an increase of the particle potential energy which transfers into particle kinetic energy by releasing the potential energy after laser irradiation. The particles obtaining large kinetic energy can be ejected from the surface. Fig.1 shows an illustration of three mechanisms in laser dry cleaning of particles.

The temperature rise ΔT in the top surface supporting particles or in particles is approximately given by

$$\Delta T = (1-R)\, I / \rho c \mu \qquad (1)$$

where R , ρ, μ, and c are the reflectivity, density, thermal diffusion length during the laser pulse and specific heat of the substrate material or particle, respectively. I is laser fluence on the substrate or particle surface.

The normal expansion ΔL of the top surface supporting particles or particles due to the above temperature rise ΔT is given by

$$\Delta L = \gamma \mu \Delta T = (1-R) \gamma I / \rho c \qquad (2)$$

where γ is the thermal expansion coefficient of the substrate material or particle.

The average pressure on the particle surface during laser pulse can be estimated by

$$P = (2R + \alpha) I / \tau C_0 \qquad (3)$$

where P is the light pressure under laser irradiation, C_0 is the velocity of light, and α is the absorptance.

According to above discussions, the experimental results can be explained. With increasing laser fluence, the normal expansion ΔL of the top surface supporting particles or particles due to absorbing excimer laser energy and the average light pressure on the particle surface during laser pulse increase, so that it is easier to remove particles and to result in higher cleaning efficiency. When the pulse number increases, the number of laser-induced depressing the "spring" increases, which results in higher cleaning efficiency. For the fixed laser fluence and pulse number, changing the repetition rate does not change the normal expansion ΔL and the average light pressure on the particle surface or the number of laser-induced depressing the "spring", so that laser cleaning efficiency is almost the same for different repetition rate.

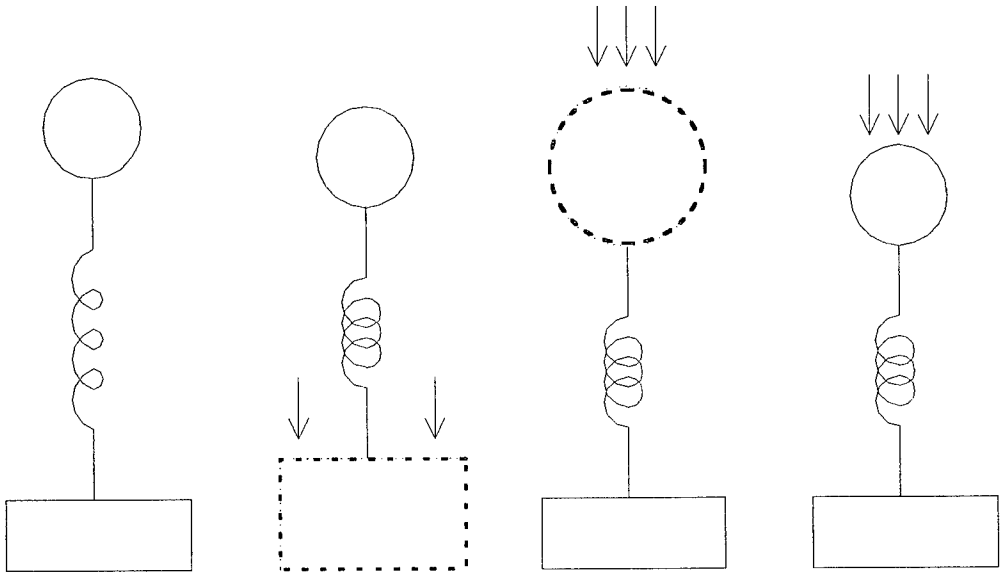


Fig.1 Illustration of three mechanisms in laser dry cleaning of particles: (a) "spring" in equilibrium, (b) depressed "spring" due to thermal expansion of the substrate surface, (c) depressed "spring" due to thermal expansion of the particle, (d) depressed "spring" due to a transient light pressure.

4:45pm - 5:15pm
ThB2

LASER INDUCED PHASE TRANSFORMATIONS IN VANADIUM OXIDES

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Extreme thermodinamic conditins in the effected zone of the powerful laser radiation make it an effective instrument for the material processing. In the base of the photo-chemical influence of laser radiation on the semiconductors is the appearance of strong positive inverse connectin between an optical absorption of the one hand and the carriers concentration, the material heating and the velocity of the thermo-chemical processes on the other hand. Crystals of the higher vanadium oxides (V_2O_5) were under local effect of the powerful (40-150 J/cm ^{2}) radiation pulse of the Ruby laser in the vacuum 10^{-5} Torr. The X-ray analysis of the irradiated samples defined the existence in these of the phase VO_2. In additin, on the curve of the temperature dependence of crystals microhardness in the zone of the laser influence with T=340 K the fracture is observed which is characteristic or the vanadium dioxide and is due to the activation energy reduction of the dislocation motion at the phase transition of the semiconductor-metal type (PTSM). At the same temperature takes place a crystal conductivity jump on 3-4 orders and, in addition, changes in spectra of absorption and electroreflectivity. Structural and phase transformation $V_2O_5 \rightarrow VO_2$ are connected with recreational processes, stimulated by laser radiation in the volume of crystal V_2O_5 . In the structure of the vanadium pentaoxide there are channals in the direction [001] and [010] with effective diameter of the 2 Å order. Along these channals and defect clusters takes place stimulated by the laser radiation the oxygen diffusion to the crystal surface. In oxygen poor crystal under the respective thermodynamical conditions in the laser influence zone takes place the rearrangement of the crystal structure with a phase formation VO_2.It is shown, that the threshold switch of the conductivity in artificial created structures V_2O_5-VO_2 can be the initiated by the laser pulse. The dominant role of the electro-thermal switch mechanism of the conductivity by a combined influence on the crystal of laser radiation and electrical current is esteblished. The state of the low ohmic memory in the system V_2O_5-VO_2 is determined by he width of thermal histeresis of the channal VO_2 conductivity at the PTSM. The reinforced effect of the single crystal matrix V_2O_5 and the absence of the considerable overheating of switch channal above the temperature of the phase transition comtributes to the stability characteristics of the forming structures.

5:30pm - 6:00pm
ThB3

Application of Laser Cutting and Linking Technology for Restructuring Interconnections in Microelectronic Devices

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The ever-increasing complexity and rapid pace of change in current VLSI technology has led to a demand for some sort of rapid prototyping capability. Circuit designers are working on increasingly more complex chips and thus the possibilities for errors in the design phase has increased. From the receipt of a given design, the typical CMOS fabrication process takes weeks to months to complete. Thus, if any design problems are discovered after chip fabrication, an iterative debugging procedure is costly and time-consuming. Thus, the need for a rapid prototyping capability is apparent. One implementation of this concept is the laser programmable gate array (LPGA), in which a generic gate array is customized into a particular design by laser linking and cutting of the metallization lines. A 'mask equivalent' design can be rapidly produced once the laser customized prototype has been tested, enabling the fabrication of large numbers of chips. Since there is no programming wiring or high-voltage switching on the chip, the LPGA has the potential for higher density than other schemes, such as the electrical field programmable gate array. Laser-customized prototypes can be produced in a matter of hours; this offers a significant rapid prototyping capability.

In the present research, the laser linking and cutting of the metallization lines has been studied both numerically and experimentally. The laser cutting of metal lines proceeds by an ablation/melting process. The metal typically has a high reflectivity, so much of the incident laser energy is lost. The remaining energy is absorbed in the first few hundred Angstroms, with the metal acting as a surface heat source. This energy quickly diffuses through the rest of the metal line, causing either vaporization or melting of the line, depending on the amount of energy absorbed. Two typical metal lines are considered: aluminum with 0.5% Si and with 1% Cu.

Normally, LPGA's are produced using either electro-optically shuttered argon lasers (μs pulses) or Q-switched solid-state lasers (ns pulses). An argon laser with 1-W power at 1 μs pulse is typically used. For a Q-switched YLF laser, the energy is typical in 1 mJ at 10 ns pulse. Based on the spot size (in microns) measured and the 0.95 reflectivity of aluminum, the corresponding surface heat fluxes induced by these two types of lasers can be found between 10^{10} and 10^{11} W/m^2. The aluminum alloy lines under these high intensity and short duration heat fluxes are rapidly melted (or even evaporated) and, subsequently, rapidly solidified. As a result, non-equilibrium solidified structures are formed. The associated heat transfer phenomenon is further complicated by the accompanying phase changes with moving solid/liquid interfaces, as well as a significant amount of melt undercooling caused by rapid solidification.

In the numerical effort, a general model of heat and mass transfer during pulsed laser melting with planar interface has been developed. The strong interaction among heat transfer, mass diffusion, and non-equilibrium melting and solidification kinetics has been taken into consideration [1,2]. The governing equations of heat and mass transfers can be, respectively, described by:

$$\partial T_j/\partial t = \partial (\alpha_j \partial T_j/\partial x)/\partial x \quad \text{and} \quad \partial C_j/\partial t = \partial (D_j \partial C_j/\partial x)/\partial x \qquad (1)$$

where T is the temperature, C is the solute concentration, t is the time, α is the thermal diffusivity, and D is the solute diffusivity. The subscript j denotes either solid or liquid phase. The corresponding boundary conditions are:

$$-k_j \partial T_j/\partial x = q, \text{ where } t \le Dt \quad \text{and} \quad -k_j \partial T_j/\partial x = 0, \text{ where } t > Dt \qquad (2)$$

where k is the thermal conductivity, Dt is the pulse duration, and q is the laser surface heat flux.

Typical model predictions are given in Fig. 1 for the interface velocity during melting (positive values) and solidification (negative values) at various interface locations for both Al-0.5%Si (solid curves) and Al-1.0%Cu (broken curves) for three laser exposure times: Dt = 20, 50, and 100 ns. A relatively minor effect of the solute element on the melting and solidification characteristics is found by the comparisons between the two alloys considered, except when the exposure time is very short, such as in the case of Dt = 20 ns, as shown in the insert. The little

effect of the solute element on melting and solidification for long laser exposure might stem from the dilute alloy conditions considered here. When the exposure time is short, however, the non-equilibrium kinetics play an important role, as demonstrated by the high melting speed (larger than 80 m/s) and solidification rate (about 36 m/s). The effect of the solute element on phase transformation also becomes important, probably because of different effects of solute element on solidification kinetics. Figure 1 also shows that the longer the laser exposure time, the higher the average melting speed and solidification rate. For example, the average solidification rate for the case Dt=20 ns, at about 36 m/s, decreases to about 6 m/s, and finally decreases to about 3 m/s for Dt=100 ns. The effect of the non-equilibrium kinetics on melting and solidification also deceases.

Experimentally, the laser is focused down to a small spot (microns) by a microscope objective and the sample is positioned by an interferometrically controlled x-y table with submicron positioning capability. The testing specimen is a standard 2-level metal CMOS process line operated by National Semiconductor. The vertical line of Metal 1 is connected to a horizontal line of Metal 2 with a via and can be connected to a Metal 2 line by forming a link at a crossing. The link region consisted of a 4x4 μm square of Metal 1 and Metal 2, with a 2-mm square hole in the center of Metal 2. Figure 2 is a scanning electron micrograph depicting both line cuts and interlevel links induced by laser pulses. The experimental investigation of laser cutting and linking of aluminum lines is being conducted at Lincoln Laboratory at Lexington, Massachusetts. The laser spot size, molten zone, and final microstructures for various laser power and pulse durations have been recorded and measured. In general, the experimental results agree very well with the numerical predictions.

In conclusion, for current metallization dimensions, thermal issues become very important, since the thermal diffusion lengths in typical aluminum lines are of the order of the line sizes (about 1 micron). For the purposes of designing an efficient wiring channel and determining the maximum packing density of these wires, a understanding of the heat and mass transfers in these structures in critical. Such a modeling effort would also assist in determining the laser parameters for the very high yield cutting required in LPGA's, and would also address the issue of future scalability of these devices.

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2. Wang G.-X., "Experimental and Numerical Study of Heat Tansfer and Solidification for Molten Metal in Contact with a Cold Substrate", Ph.D. Thesis, University. of California, Santa Barbara, CA, 1995.

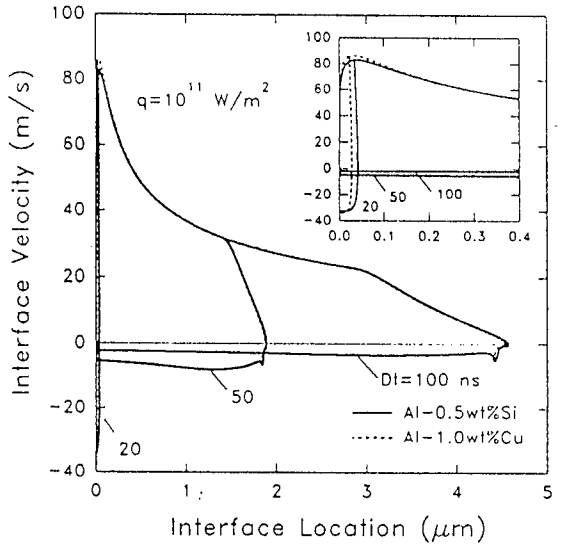


Fig. 1 Interface velocity during melting and solidification

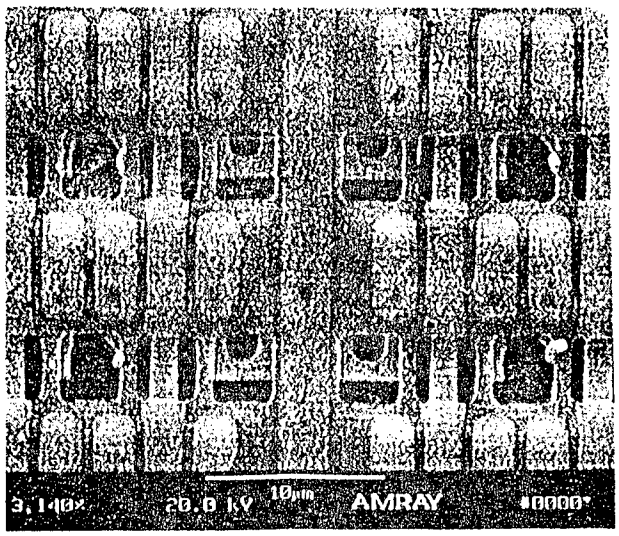


Fig. 2 Laser-induced line cuts and intermetal links

6:00pm - 6:30pm
ThB4

Surface-Related Phase Changes and Structure Modifications in Silicon with Ultrafast Laser Pulses

P. A. VanRompay, X. Liu, R. K. Singh*, and P. P. Pronko

Center for Ultrafast Optical Science; Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109

This paper presents an overview of experiments and modeling calculations on the energy absorption mechanisms and the near-surface thermodynamic phase changes and structure modifications in silicon as a result of exposure to femtosecond and picosecond laser pulses in the wavelength range of 760 to 800 nm. It is found that these short pulses produce sufficiently high electric field intensities to cause avalanche dielectric breakdown in the near-surface region, and that the free electrons so generated act as the dominant absorbing centers for the incoming radiation. For sufficiently short pulses, the energy resides entirely in this electronic medium during the pulse duration and is transferred to the ions, over time, in a controlled fashion that is described by a well-defined coupling formulation. Based on time-resolved melting and vaporization as determined through reflectivity and imaging, one can obtain specific calibration of the coupling coefficient in this formulation. It is found that the coupling process depends on a number of factors, including the phase state of the material and the state of the electrons during the incoming pulse. A complex interplay of average electron temperature and lattice structural condition appears to be involved in describing the process. These complexities are observed to lead to an interesting crystalline and amorphous composite layer in the final state of the material as observed by cross-sectional TEM. Experimental determination of melt thicknesses is used to confirm the modeling calculations which in turn is used to help explain the origin of the structural composite layer of crystalline and amorphous silicon that is observed to form.

In a recent paper [1] on laser-induced avalanche ionization and electron-lattice heating of silicon, we showed that in order to explain the absorption depths of the laser radiation and to properly account for the average electric field intensities associated with surface damage due to vaporization, it was necessary to invoke a dielectric breakdown mechanism during the pulse absorption process. It is further demonstrated [2] that the ionization coefficient for the process can be described by the well-known Thornber equation [3] derived for DC electric field conditions. This implies that the electron collision rates occur on a sub-femtosecond time scale during the period of the pulse duration. The high field limit for this equation may be expressed as: $\alpha(\varepsilon) = \{q\varepsilon/E_I\}\exp[\varepsilon_I/\varepsilon]$, where ε is the laser electric field, q the electron charge, E_I the ionization energy at high field, and ε_I the breakdown field strength. The instantaneous electric field during the laser pulse (normalized to full-width, half-max) is shown in Fig. 1 for those pulse durations at which threshold for vaporization was measured. It is seen that for all these cases the fields are greater than the dielectric strength of the material. The temporal build-up of charge carriers due to the avalanche process can be determined by integrating the fields of Fig. 1 over the pulse time and using the avalanche equation: $N/N_O = \exp[\alpha(\varepsilon)V_d t]$, where N is the number of carriers produced over time t with ionization coefficient α under saturation drift velocity V_d.

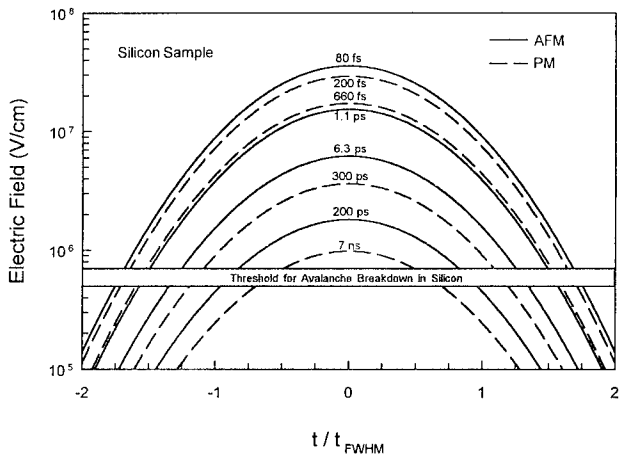


Figure 1. Instantaneous electric field for measured threshold of vaporization. Note that for all pulse durations, the field is above the threshold for avalanche breakdown in silicon. (AFM=atomic force microscope, PM=photomultiplier)

* Department of Materials Science and Engineering, University of Florida, Gainesville, FL 32611

The results of the above calculation provide justification for using an absorption depth of 75 nm in our two-temperature thermodynamic modeling calculations that are used to describe the melting and vaporization process [1]. Fig. 2 shows the results of that simulation where the electron-lattice coupling coefficient is given by the Kaganov equation in terms of $D_4(T_{e,i})$, 4th order Debye integrals [4] :

$$G(T_e,T_i) = G_0 \frac{T_e}{T_D}\left\{D_4(T_e) - \frac{T_i}{T_e} D_4(T_i)\right\}$$

In this equation, T_e, T_i and T_D are the electron, lattice, and Debye temperatures, respectively. G_0 requires calibration from experiment and is determined from time-resolved melting and vaporization [5]. It is found, when doing that calibration, that a unique value of G_0 may be assigned to the solid state in order to obtain a specific time for melting under a given set of laser conditions, but that a different and unique value needs to be assigned to the melt state in order to properly account for the time taken to achieve the onset of vaporization. The difference between using one or two values of G_0 is further shown in Fig. 2. It is seen there that the vaporization onset time is changed by more than a factor of 4 based on the phase state value of G_0. Data from time-resolved melting and vaporization measurements require that a phase state change in G_0 be used. In so doing it is observed that an unusual inversion in the heating rates for the solid versus liquid states is invoked. The simulation code clearly monitors this process and shows how a cool surface can exist in the presence of a very hot subsurface.

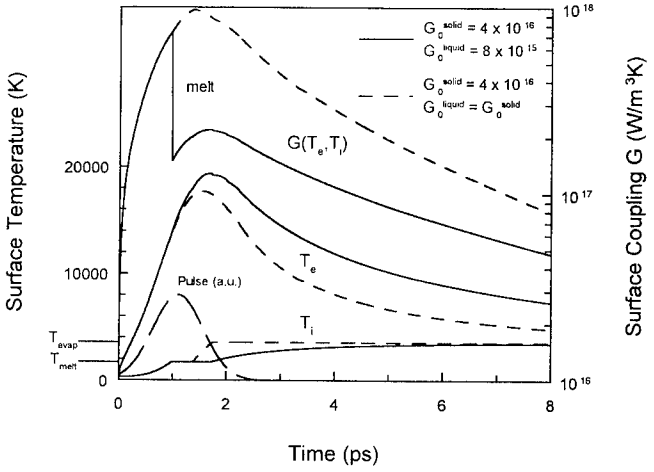


Figure 2. Results of simulation using a single G_0 and a phase-dependent G_0. Shown are the electron and lattice temperatures, the coupling coefficient and the laser pulse. Results are for a 1.1 ps, 0.37 J/cm² pulse on a silicon sample.

Cross-sectional TEM measurements of laser-irradiated silicon at just below the vapor threshold shows a phenomena that supports the predictions of the simulation code. This is seen in Fig. 3 where one observes a thin crystalline (xtl-Si) overlayer on top of a deeper amorphous (α-Si) zone. The disordered material is considered to be formed by rapid resolidification of the liquid state, with the crystalline material above being the result of radiation and electron emission from a cool surface preventing the complete liquid state from being attained. The deep material below the amorphous layer is original silicon that had not melted. A more detailed explanation of this process will be provided in the presentation of this work.

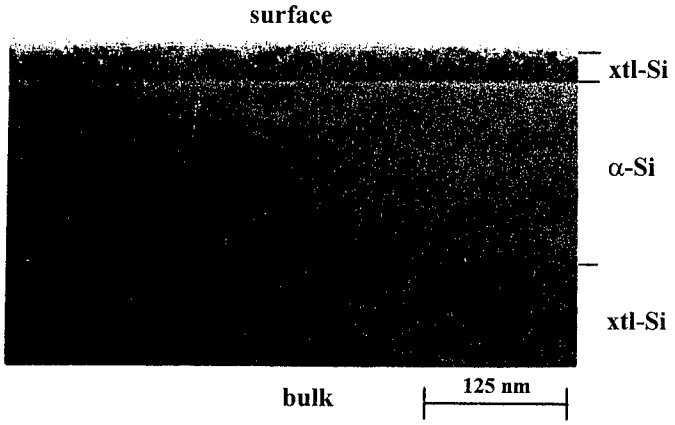


Figure 3. Cross-sectional TEM of silicon sample irradiated with a 1.1 ps, 0.37 J/cm² laser pulse. Note the ~300 Å crystalline layer at the surface, on top of a ~1500 Å amorphous layer.

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ADVANCED APPLICATIONS OF LASERS IN MATERIALS AND PROCESSING

PAPERS NOT AVAILABLE FOR THE FOLLOWING

6:60pm - 7:00pm
TuB4: Epitaxial Growth of Oxide Superconductors Using Pulsed-Laser Deposition, D.P. Norton, *Oak Ridge National Laboratory, Oak Ridge, TN*
The use of pulsed-laser deposition in the growth of high-temperature superconducting films will be addressed, focusing on developing a viable YBCO-based deposited conductor for long-length, high current applications at 77 K.

4:30pm - 5:15pm (Invited)
WB1: Laser Processing of Coatings and Surfaces, M. Donley, *Wright Patterson Air Force Base, OH*
Research and development activities in laser processing of material for aerospace applications undertaken at the Air Force Wright Laboratory, Materials Directorate (WL/ML) will be discussed. Researchers at WL/ML have been involved in the research and development of using lasers for a wide variety of materials processing since 1981.

4:00pm - 4:45pm (Invited)
ThB1: 3D Micromachining by Stero-Lithography, Koji Ikuat' Nagoya University, Nagoya, JAPAN
Real three dimensional micro fabrication named "IH Process" based on stereo lithography is developed. 3D resolution is better than 5 micro integrated fluid system are fabricatioated successfully.

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DIGEST
IEEE/LEOS
1996 Summer Topical Meetings

Broadband Optical Networks
Enabling Technologies and Applications

at

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Monday, August 5, 1996

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8:30am - 9:15am
Plen1

THE POTENTIAL & PROMISE OF WDM NETWORKS

Peter Cochrane

BT Laboratories, Martlesham Heath, Ipswich, IP5 7RE, England

Prologue

Much of the telecommunications industry is strongly conditioned by established practices and trends. It appears difficult to shake off the notion of bandwidth constrained by copper cables, radio and satellite systems, and high distance related costs. Software too appears to invoke an acceptance of massive complexity to realise relatively simple tasks. Network management, signalling, control and billing now dwarf bit switching and transport! What are we doing? People talk of the bandwidth efficiency of ATM and packet systems whilst sending a single line e-mail message with a 25 line header! They then go on to suggest that real time services can be accommodated by reserving packets and routings, whilst actually wasting bandwidth to control delay. This has all become steeped in political and corporate correctness through massive investment programmes that perpetuate a dubious trajectory. How come the obvious solution - WDM has been yet to be implemented on any scale?

History shows us that every few decades technological progress across disconnected areas presents opportunities for radical change. The great benefit of these epochs is that they effectively change the nature of the problem and allow new solutions to be engineered. Such an opportunity is with us now at the conjunction of very low cost computing and telecommunications. The prospects go far beyond multi-media, poor teleconferencing quality and co-operative working environments. But to grasp the opportunities requires new mind sets. It also means taking a few bold steps - and WDM is like the everlasting match - it is a technology that means much more for much less! More bandwidth, connectivity and reliability with less electronics and hardware, lower operating costs, lower prices, a smaller industry and fewer people employed.

WDM can transform the telecommunications industry by effectively making bandwidth free and distance irrelevant. This would negate billing and relegate network management to a minor spectator sport. In its ultimate realisation we can envisage a zero switching network with most of the system intelligence at the periphery. All of this is difficult for the industry to subsume and comprehend, but it is inevitable. No doubt PDH, SDH and ATM will continue to be deployed, but for a future GII they are fundamentally flawed and limited.

What Are We trying to do?

Integrated electronics has effectively made information processing and storage limitless and effectively free, whilst software has introduced the potential for unexplained system and network failures on a grand scale. What should we do, or be doing? There would appear to be only a few key actions required to take the next major step. Fundamentally we need to start thinking and engineering ***systems*** and not hardware, software, networks and applications as if they were in some way disconnected. We need to think and engineer the whole, not just the individual building blocks. Even chaotic systems need a light hand of control to be successful.

New Networks

The longer transmission distances afforded by optical fibre systems is predicating a reduction in the number of switching nodes and repeater stations. When augmented by optical amplifiers and network transparency even greater opportunities are realised with, reduced component counts, improved reliability, reduced power and raw material usage, increased capacity and utility. A further logical development would see the concentration of traffic onto single rather than several fibres in parallel. WDM makes such a proposal the more reliable option as the time to repair one fibre is far shorter than for multiple fibres!

Today we access < 0.01% of the fibre bandwidth available, and we may be able to approach 1% with currently available technologies. But everything we have realised so far may be totally eclipsed by moving from the linear to the non-linear regime where there are likely to be hidden properties and benefits that we have yet to discover.

As the cost of transmission continues to go down we have to question the balance between transmission, switching and software. Reductions in the number of network nodes, management and repeaters, consolidated switches, and the constraints imposed by software look to be good targets. We may also have to move away from a local call spanning just a city area, to the whole country and planet.

Economics of Analogue and Digital

During the 1970s numerous economic studies established digital transmission and switching as the best option for a global network. Programme decisions made at that time are now seeing their full realisation with the near 100% digitalisation of networks. With the fixed assets of a Telco measured in $Bns, and any major network changes take ~ 10 years to complete - a move back to analogue is not good news. Before fibre technology the ratio for long lines was ~ 50% transmission and switching. With optical fibre the transmission asset base may now be as little as 10% with some 50% of all resources residing in the local loop. This has changed the economic balance away from digital towards WDM and analogue. With WDM and photonic amplification, an all-analogue system for national and international wideband services looks far more attractive.

Software

The biggest single problem with software science and engineering is the almost total lack of any science and engineering. Whilst we might use the excuse that it is a very young field, this does not give the full story. Indeed, should we even expect to achieve as mature an understanding as that enjoyed in mathematics and the physical sciences? In truth software is a further level of abstraction beyond mathematics and may well defy real understanding for some time.

By any comparison, software is becoming a cause for significant concern in terms of sheer scale. For example; the complete works of William Shakespeare take up about 450m of paper; the line code for a small telephone switch is about 1km and a central office is ~10km. A full stop in the wrong place and the spacecraft misses the planet! In the software domain very minor things pose a considerable risk, which appears to be growing exponentially as we look to the future. We have to find new ways of solving this increasing burden of risk as the present trajectory looks unsustainable in the long term. Quite perversely the unreliability of hardware is coming down rapidly. From any engineering perspective this growing imbalance needs to be addressed. If it is not, we can expect to suffer an increasing number of ever more dramatic failures.

Technology

In some respects we currently suffer from technological indigestion, and it is likely to worsen as we approach the new millennium. We now have so much "ripe technology" (and more is coming) that we are spoilt for choice. What is required is a new approach that breaks the bonds with the "copper" past and reaches out for the new. WDM is one of the vital components!

Further Reading & Background

Visit = http://www.labs.bt.com/people/cochrap

10:30am - 11:00am (Invited)

MA1

The National Transparent Optical Network (NTON): moving key WDM technologies off the lab bench into public and private networks

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The National Transparent Optical Network Consortium (NTONC) and the Defense Advanced Projects Research Agency (DARPA) are jointly funding a full scale wavelength-routed regional optical demonstration network featuring live traffic to investigate strategies for commercial deployment. The NTONC comprises world leaders in many areas of optical data transmission technology. They are Pacific Bell, Sprint, Northern Telecom, Uniphase Telecommunications Photonics, Hughes Aircraft, Rockwell International, Lawrence Livermore National Laboratory (LLNL), University of California at San Diego and Columbia University. Northern Telecom is leading the overall effort and in particular the development of new optical technology. LLNL is leading the network integration, deployment of demonstration applications and operation of the prototype network and testbed.

There are two thrusts for the three year project. First, establish a prototype network over which high bandwidth applications can illustrate new optical technologies. Second, build an open testbed with 'real traffic' to test new ARPA sponsored, optical technologies. A transparent "backbone" will encircle San Francisco Bay with optical (i.e. data independent) routing nodes at LLNL, Pacific Bell (San Ramon), UC Berkeley and Sprint (Burlingame). The ring will carry four $\geq$ 2.5 Gb/s channels (each using a different wavelength) except for the Livermore to San Ramon Link which will carry eight channels. Sprint engineering fiber and Pacific Bell installed fiber will connect additional high data volume as well as high visibility application sites. Initial feeder sites will include Stanford, LBNL, SNL, SRI , other "Silicon Valley" participants and the Moscone and San Jose Convention Centers.

We started the project January 1 1995 and unveiled the operating network at the Optical Fiber Communications (OFC) conference in the San Jose Convention Center (2/27-29/96). A number of demonstrations showed connectivity to the four backbone sites and two additional application sites, SRI and LBNL. We demonstrated the initial technology under test: optical (format free) switching, wavelength translation and optical multicasting.

Numerous tecnological advances have occurred recently that enable the realization of transparent optical networks. Currently we are evaluating wavelength flattened optical amplifiers developed for WDM applications in the network. Multi-wavelength signals carrying digital and analog signals simultaneously across optical amplifier chains have been characterized. The signals are routed within the network using optical switches based on acousto optic tunable filter technology. We also demonstrated the application of a highly integrated WDM transceiver with add/drop, wavelength translation, and multicasting capabilities during our initial demonstration at OFC.

We have just begun recruiting applications users and potential technology demonstrations.

11:00am - 11:15am
MA2

Scaling WDM Networks: Two Options for 100 Gb/s

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In future wavelength-division multiplexed (WDM) optical networks provisioning, restoration and, possibly, fast switching may be implemented at the optical level, on a per-wavelength basis [1]. Increasing the number of channels for a constant total capacity increases the *granularity* of the network. A WDM network with a larger number of lower bit-rate channels is more flexible from a provisioning and from a restoration point of view. Increasing the granularity also shifts part of the terminal cost from electronics to optical components. Furthermore, granularity has an impact on the system performance in terms of bit-error rate (BER). The interplay among the above three factors: network performance, cost and transmission performance will ultimately determine the optimum granularity for each WDM network.

In this paper the issue of granularity is addressed from a transmission point of view. The linear and nonlinear effects that determine the BER of a WDM point-to-point transmission system with intensity modulation and direct detection are compared for two systems with different granularity and same total capacity of 100 Gb/s, S_1 with ten channels at 10-Gb/s, and S_2 with twenty channels at 5 Gb/s. It is found that the impact of optical fiber nonlinearities is lower in the second system.

The two systems are assumed to have the same length and amplifier spacing and to use the same optical amplifiers, so total output power, total bandwidth and noise figure are the same, hence power per channel P and channel spacing Δf in S_2 are half the one in S_1. The fibers used in the two systems are assumed to be the same except for chromatic dispersion. Therefore fiber loss, effective length, effective area, and gain coefficients for nonlinear effects are the same in the two systems. Both systems are assumed to take advantage of dispersion management [2] to balance the degradation introduced by chromatic dispersion and nonlinear effects.

The key element in this comparison is the choice of the dispersion map for the two systems. It is assumed here that S_1 utilizes the best possible dispersion map, the one that yields the lowest BER for the given system parameters (length, power, channel plan, amplifiers). Since the relation between the optimum dispersion map of S_1 and S_2 is in general unknown, it will be arbitrarily assumed here that the map for S_2 corresponds to the map for S_1 with a chromatic dispersion four times larger at any point. This choice of the dispersion map for S_2 is justified, at least from a linear point of view, by the fact that linear distortions due to chromatic dispersion are inversely proportional to the square of the bit rate R [3]. Clearly the choice of the dispersion map for S_2 could be suboptimal, therefore it is expected that the performance of S_2 might improve with a more careful selection of its dispersion map. If S_2 can be proved to perform better than S_1 even with the above suboptimal choice, all the more reason it will perform better with an optimal choice of its dispersion map.

In the absence of fiber nonlinearities, S_1 and S_2 with the above choices are equivalent. They have the same overall loss and gain, the optical signal-to-noise ratio (SNR) at the receiver is the same and the pulse evolution due to the chromatic dispersion D, determined by the product $R^2\,D$, is the same. Also the walk-off length, defined as the length of fiber over which two bits of adjacent channels completely walk through each other due to dispersion, is the same since $R\,D\,\Delta f$ is the same.

When fiber nonlinearities are considered [3], [4], one might expect that S_2 will be less affected than S_1 by the "single-channel" nonlinearities, stimulated Brillouin scattering (SBS) and self-phase modulation (SPM), since its power per channel is lower, and more affected than S_1 by the "multi-channel" nonlinearities, stimulated Raman scattering (SRS), cross-phase modulation (XPM) and four-wave mixing (FWM), since its number of channels is larger.

For SBS, the requirement is that the power on each channel at the output of each amplifier be below threshold to avoid SBS induced depletion [4]. The SBS threshold is the same in the two systems, however the power per channel is smaller in S_2, therefore S_2 is more robust to SBS than S_1. The effect of SPM can be estimated by looking at the spectral broadening ΔB induced on each signal, proportional to the product $P\,R$ [3]. The degradation introduced by spectral broadening on each fiber span is proportional to $R\,\Delta B\,D$ [5], and is lower for S_2. Therefore, in agreement with the above intuitive argument, S_2 is less affected than S_1 by "single-channel" nonlinearities.

As for XPM, the spectrum of each channel is mostly broadened only by its immediate neighbouring channels, since pulses belonging to channels that are widely separated walk-off through each other very rapidly and without affecting each other [6]. This is true provided that the dispersion is not too low, as must be the case for both S_1 and S_2 to achieve a sufficient FWM suppression [2]. Since the walk-off length of adjacent channels is the same in the two systems, the number of

This work was partially supported by ARPA through the MONET Consortium.

relevant neighbouring channels will also be the same. The XPM spectral broadening introduced by each immediate neighbouring channel is proportional to $P R$, therefore, in analogy to the SPM case, the effect of each immediate neighbouring channel is weaker in S_2. Hence S_2 is less affected than S_1 by XPM.

The impact of a FWM wave generated at a channel frequency in a WDM system depends on its power relative to the channel power at the receiver and is proportional to the square of the channels' power and to its efficiency [2]. In a WDM system with equally spaced channels, the number of mixing products that are generated on each channel grows with the square of the number of channels. However, mixing products generated by channels beyond the near neighbours have quickly decreasing efficiency, so the number of "relevant" mixing product generated on each channel is actually the same in S_1 and S_2. Hence, to compare the impact of mixing on S_1 and S_2 it is enough to compare the magnitude of the largest mixing products (and that of all the "relevant" mixing products, suitably paired). If the best dispersion map for S_1 does not include fiber with very low dispersion, as it is very likely, it can be shown that the efficiency of mixing products generated by the same set of channels in S_1 and S_2 is the same, since the increase in efficiency in S_2 due to the closer channel spacing is perfectly balanced by the reduced efficiency due to the increase in the fiber chromatic dispersion. Since the efficiency of the paired mixing product is the same in the two systems, but the power per channel is lower in S_2, the impact of FWM is smaller for S_2.

If the impact of SRS is assessed by considering the worst-case SNR degradation of the shortest wavelength channel assuming that all channels are transmitting marks and neglecting dispersion, the simple result is obtained that the effect is proportional to the product of total power and total bandwidth of the WDM system [4]. Since S_1 and S_2 have same total power and bandwidth (they use the same amplifiers) the SRS effect in this worst-case analysis is the same in the two systems. In presence of dispersion and with a large number of channels, though, several bits from different channels interact with each other, and the SNR degradation of the different bits in the same channel tends to become the same, since each bit interacts with approximately the same number of marks and spaces in the other channels. When the number of bits that interact is sufficiently large, the SRS crosstalk becomes a deterministic effect, since all bits in the same channel have essentially the same SNR variation, and the impact of SRS can be largely suppressed by channel pre-equalization [7]. For SRS crosstalk all interacting bits have the same effect. The reason is that bits from channels that are further in frequency from the channel under consideration have linearly increasing Raman gain, but their interaction length is inversely proportional to the frequency separation. For SRS crosstalk suppression, what really matters is the number of bits that interact. The larger the number of bits, the better the suppression [7]. Since the walk-off length between adjacent channels is the same in the two systems, the number of interacting bits is larger in S_2 because of the larger number of channels. So the worst-case of SRS crosstalk is the same for S_1 and S_2, but in S_2 the SRS crosstalk can be more effectively suppressed with power pre-equalization.

In conclusion, the intuition that "multi-channel" nonlinearities would affect S_2 more than S_1 because of the larger number of channels is wrong. XPM and FWM do not get worse, under the present assumptions, with an increase in the number of channels, and the lower power per channel of S_2 allows a reduction of these effects. For SRS the increase in the number of channels is actually beneficial, under the present scaling assumptions, since it facilitates SRS crosstalk suppression.

A key role in the scaling of all the nonlinear effects is played by the scaling of the dispersion map. However, as mentioned above, optimizing the dispersion map can only further improve the performance of S_2. Therefore, from a transmission point of view, twenty 5 Gb/s channels is a better choice than ten 10 Gb/s channels to achieve a 100 Gb/s aggregate capacity. The conclusion that increasing the granularity is better from a transmission point of view is quite general, but the reasoning used in this paper cannot be extended arbitrarily to, for example, compare one channel at 100 Gb/s with one hundred channels at 1 Gb/s. A fundamental assumption in this paper is indeed that the best dispersion map of S_1 does not include any segment of fiber with small dispersion. This is reasonable for a ten-channels 10-Gb/s WDM systems, but it is not for a single-channel system at 100 Gb/s. Furthermore, if the scaling factor is large, the assumed scaling of the dispersion map becomes unrealistic.

It is a pleasure to acknowledge Andy Chraplyvy, Bob Jopson and Bob Tkach for several hand-waving discussions.

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Experimental assessment of node cascadability in a reconfigurable survivableWDM ring network

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Photonic networks will not only increase the overall capacity of the transport networks but also provide higher network flexibility in terms of routing capability, reconfigurability, and protection. Following their commercial introduction, WDM point-to-point transmission systems will rapidly evolve to include wavelength add/drop, and, in the longer term, optical cross-connect functionalities [1,2].
On the other hand, ring topology is especially attractive because of the efficient self-healing protection schemes that can be adopted. The implementation of WDM ring networks is therefore regarded as the first deployment phase of photonic networking.

WDM ring network testbed
A 10-Gbit/s capacity, 4-wavelength, self-healing 2-fiber unidirectional ring network testbed has been realized with 3 pre-industrial rack-mounted OADMs assembled with commercial devices. The 3 nodes are based on the dynamically reconfigurable N-wavelength OADM architecture [3], depicted in Fig.1 with N=4. This node architecture exhibits full connectivity ("Add", "Drop") capability, "Drop & Continue" connections for multicasting along the ring, and "Trib-to-Trib" capability (simultaneous "Add" and "Drop" of a signal at a node for the interconnection of subnetworks). It has also been designed to meet protection requirements; in case of failure of the working ring, all the traffic can be routed onto the protection ring.

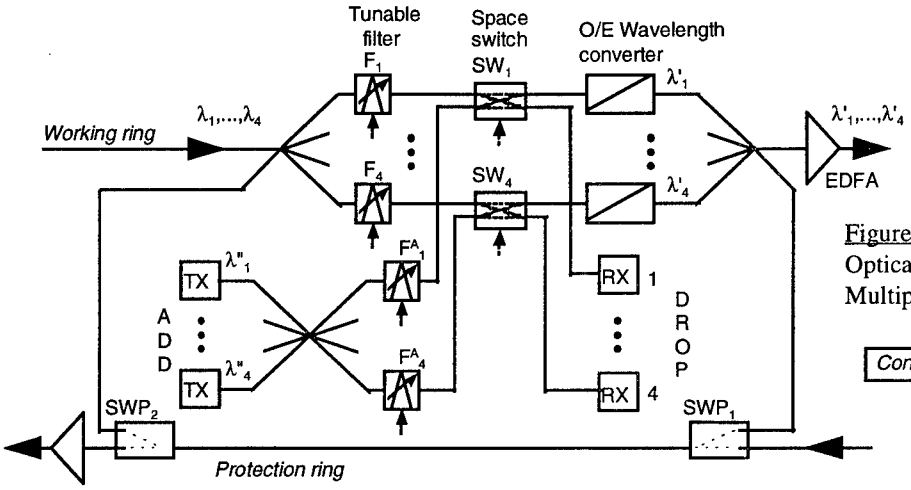


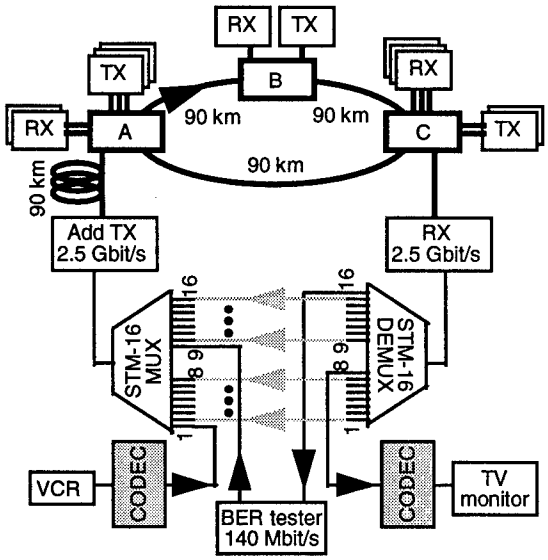
Figure 1 : flexible Optical Add/Drop Multiplexer architecture.

The nodes are linked by 90-km of G.652 pure silica core dispersive fiber, and a +13 dBm optical post-amplifier is used at the beginning of each section of the working ring. The channel frequencies are spaced 200 GHz apart, and the first channel wavelength is 1551 nm. A control PC, communicating with the 3 nodes via a parallel bus, acts as both a node and network control station. 103 different traffic configurations with various connection types were succesfully demonstrated, and the self-healing protection scheme utilizing the second fiber ring has also been validated (time to switch from the normal operating mode to the protection mode = 55 ms; primarily limited by the switching time of the protection switches SWP).

Recirculation experiments
In a first experiment, the ring is set in a loop configuration, in which a signal is added and dropped in the same node after travelling 4 times around the ring, using a different wavelength on each turn, in effect

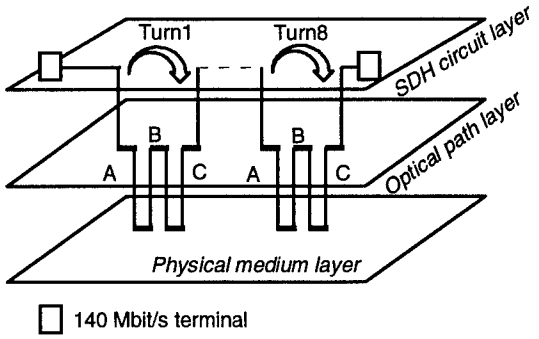
exploiting all the ring resources. The power penalty (at a 10^{-10} BER, with 2^{23}-1 PRBS) after 1080 km and a cascade of 12 nodes (i.e., 12 signal regenerations) was less than 0.3 dB. Error-free transmission was recorded over more than 112 hours, corresponding to a BER < 10^{-15}. In this configuration, both SONET OC-48 and SDH STM-16 frames were carried by the channels and a BER less than 10^{-14} was measured with non-scrambled sequences (i.e., up to 128 consecutive identical bits possible). The network performance proved to be fully compatible with the ITU G.958 recommendation for jitter tolerance and jitter transfer.

In a second experiment, an Add transmitter of node A is driven by a synchronous STM-1/STM-16 time-division multiplexer, fed by a 140 Mbit/s digital video signal on input 1 (out of 16), and by a pseudo-random bit sequence on input 9, as shown in Fig.2a. After one A to C connection over the WDM ring, the two 140 Mbit/s signals received at the output of the synchronous demultiplexer are injected on inputs 2 and 10 of the synchronous multiplexer, respectively, for a second A to C connection. This procedure is repeated until the STM-16 frame is fully loaded with the two 140 Mbit/s signal types. Thus, the synchronous demultiplexer output 8 delivers the video signal, after 8 A to C connections, to a TV set. BER measurements are carried out on the data delivered from output 16, after transport over 8x(90+180)=2160 km. In this configuration, a BER less than 10^{-14} was recorded. This path accross the network is represented in the layered network model (Fig.2b) [4] that includes the SDH circuit layer, the optical path layer and physical medium layer. This path simulates a long-distance transport through a network including optical routing and SDH electrical processing, as well as the interworking of the various layers.



a) Experimental setup

Figure 2 : 8-turn recirculation experiment



b) Equivalent path through the network model

Conclusion

The experiments carried out on the WDM ring network testbed demonstrated high node cascadability with negligible power penalty (0.3 dB after 1080 km transmission through 12 nodes). A long-distance path across a layered network was also shown, thereby simulating the iterative transport through the SDH circuit, optical path and physical medium layers.

The reported results are especially interesting for the design and short-term implementation of *flexible* survivable WDM ring networks with more than 10 nodes, which is considered a major step in the introduction of photonic networking.

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11:30am - 11:45am
MA4

Performance of a Wavelength-Routed All-Optical Network at Over 100 Gigabit/s

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Introduction: There are several network services provided by the 20 channel (50 GHz spaced) all-optical network (AON) testbed deployed in the Boston metropolitan area [1,2]. Such services include transparent optical channels capable of supporting transmission at 155 Mbps to 2.488 Gbps with local broadcast, and metropolitan-area multicast and broadcast capability. The network also supports a novel scheduled simultaneous TDM/FDM service to independently interconnect many low rate users (<155 Mbps) among several optical terminals by sharing wavelengths in time [3,4]. In this work, we report on a new metropolitan area service with 10 Gbps access rates per channel using tunable transmitters and receivers to support, for instance, SONET OC-192 users. We demonstrate operation of more than 10 independent local and metropolitan channels for a total data rate exceeding 100 Gigabit/s. This is the first time such high rates have been demonstrated in a dense WDM system utilizing all-optical wavelength routing and partitioning for wavelength and channel re-use.

Network Architecture and Testbed: The AON testbed was assembled to provide a scalable high-speed, high-capacity transparent optical network and to promote the interaction of architecture, technology and applications. The hierarchical architecture relies on wavelength partitioning to segment the network and allow for wavelength re-use (Fig. 1). This can occur at two levels within the network: within the local area (Level-0) domain and within the metro area (Level-1) domain. Of the 20 channels assigned to the network, the 10 odd-numbered channels on 100 GHz spacing remain in the local domain. The remaining 10 even numbered channels are routed to the metropolitan area hub where they can be routed or broadcast to other local hubs depending on the configuration of the hub and the chosen wavelength. Each path through the network is transparent over a wide spectral bandwidth (~30 GHz) and is thus essentially bit rate and modulation format independent over a wide range of conditions. We use that transparency in this work to demonstrate the bit-rate upgradability of the AON.

Each channel may be assigned to a single source-multiple destination set (A-Service) or multiple-source-multiple-destination sets via synchronized optical time-sharing (time-slotted B-Service). A separate out-of-band channel (not transparent) is implemented at 1310 nm for network management and control (OAM&P) and timing distribution. We have built two Level-1 hubs, six Level-0 hubs and eleven optical terminals (OTs) and implemented these in a metropolitan area testbed using over 138 km of normal dispersion duplex fiber. To support the high bit rates described here, we augment that fiber with dispersion compensating fiber modules.

10 Gigabit/s Transmitter and Receiver Configuration: The high speed transmitters use the same type of distributed Bragg reflector laser and E-0 modulator (EOM) plug-in circuit cards described in previous work [1-4]. To generate the independent 9.953 ("10") Gbps sources, four EOMs are used as shown in Fig. 2. The BERT pulse pattern generator drives the master EOM carrying the five local channels, numbered (1,3,5,7,9). The output of the master EOM is split and then injected into two separate Level-0 hubs. This generates 100 Gbps aggregate local capacity, and further demonstrates the utility of wavelength partitioning for wavelength re-use. The data for the other three plug-in transmitters is generated by either by detecting one of those five local channels after transmission through the Level-0 hub, or by detecting signals generated from it then re-broadcast over the Level-1 metro hub, thus implementing multihopped connections. In the experiments described below, as many as three hops are required for some of the BER curves. Normal dispersion fiber rapidly decorrelates the individual data streams. The outputs of the three slave EOMs are carried on three independent lasers on metro-routed channels 12, 14, and 16. These wavelengths are broadcast throughout the network and are detected in both Level-0 hubs used in this test.

The receivers, also implemented on plug-in circuit cards, use an erbium preamplifier followed by a tunable Fabry-Perot filter having 18 GHz FWHM and between 1-4 THz FSR. The filtered signal is

detected in an 18 GHz *pin* detector followed by a low noise 12 GHz 50Ω preamp. The signal is split for clock-recovery and then ac-coupled to a decision circuit having a fixed-threshold. The thresholds are adjusted for best operation near 10^{-12} BER for a 2^{23}-1 PRBS under worst case SNR conditions for normal operation of the network.

System Performance: The same plug-in receiver was installed in both local area hubs for all the BER measurements. The performance in each of the local hubs for representative local and remote channels is shown in Fig. 3 and is compared to back-back measurements using one of the five local channels directly from the master EOM. In Fig. 4 we summarize the performance as the sensitivity measured at 10^{-9} BER. It is evident that the performance is uniform across operating mode and channel number. The normal received signal power is approximately -15 dBm. The minimum spacing between operating modes was approximately 100 GHz; however, separate measurements show that closer operation at 50 GHz introduces only a 1.2 dB power penalty due to adjacent channel crosstalk.

Summary: Optical networks have long promised to provide easier migration to vastly higher transmission rates and system capacities. In this work we demonstrate the bit-rate upgradability of such networks in the All-Optical Network testbed by introducing 10 Gbps circuit cards embodying tunable transmitters and receivers and operating them over optical channels interchangeably used for data rates between 0.155 and 2.488 Gbps. To demonstrate the enormous capacity of this type of wavelength-routed network, we implemented a 130 Gigabit/s transmission experiment using four E-O modulators, 8 lasers on 13 channels with up to three spans of multihopped operation. Up to 80 Gbps was present in some of the resources. Uniform performance with -32.0 dBm average sensitivity and 4.2 dB average penalty was achieved.

Acknowledgments: This work was supported by the Consortium on Wideband All-Optical Networks and the Advanced Research Projects Agency.

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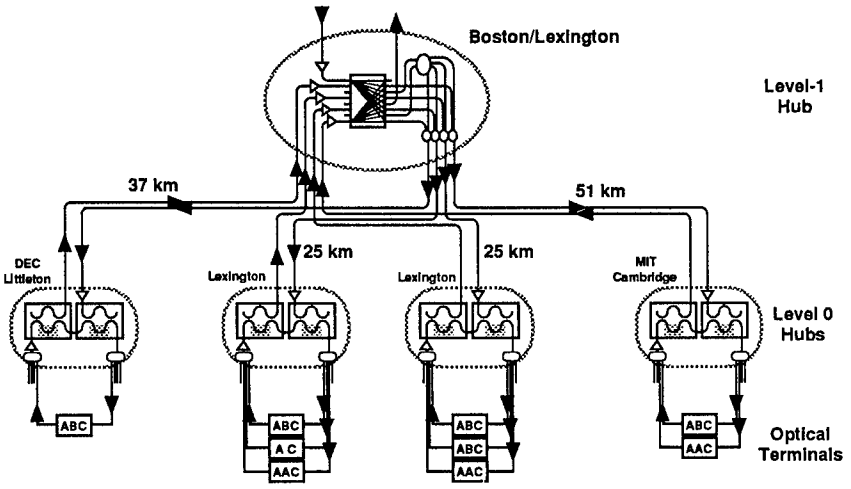


Fig.1. AON testbed hierarchical architecture. Local wavelengths, routed only within the L-0 domains, support local (LAN) connections; remote wavelengths, routed at L-1 hubs for interconnections among L-0 domains, support remote (MAN) connections.

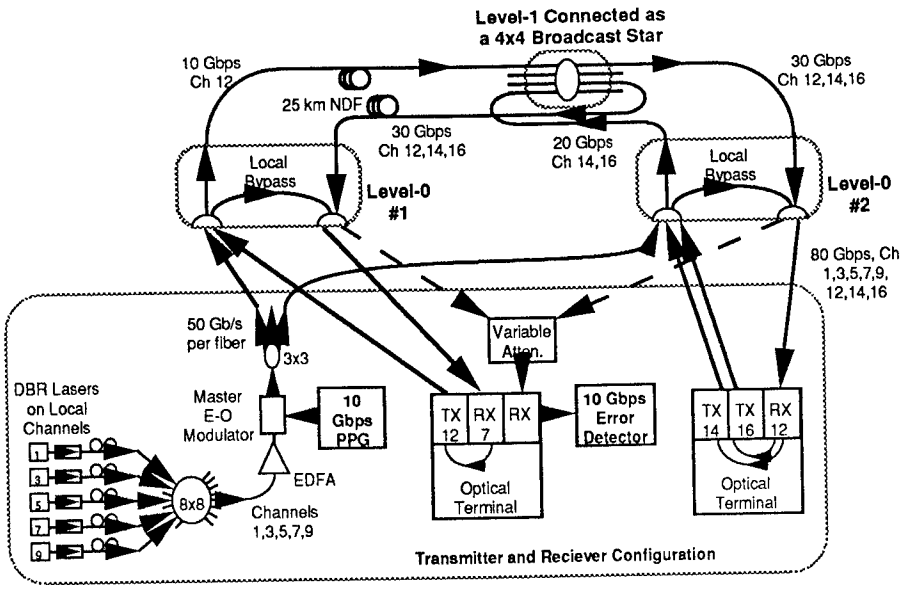


Fig. 2. Configuration of the transmitters and receivers for direct and multihopped generation of 130 Gbps optical data streams on eight wavelengths. The Level-1 hub carries a total of 30 Gbps, 10 Gbps on Ch 12 from L-0 hub #1 and 20 Gbps on channels 14 and 16 from L-0 #2. Each local L-0 hub carries 50 Gbps generated and distributed locally plus the 30 Gbps broadcast down from Level-1. The data source for transmissions on channel 12 from the optical terminal in Level-0 #1 is generated from data transmitted to it over the Level-0 #1 local bypass connection on channel 7. The data source for transmissions from the optical terminal in Level-0 #2 is generated from data broadcast to Level-0 #2 on channel 12 from the optical terminal in Level-0 #1.

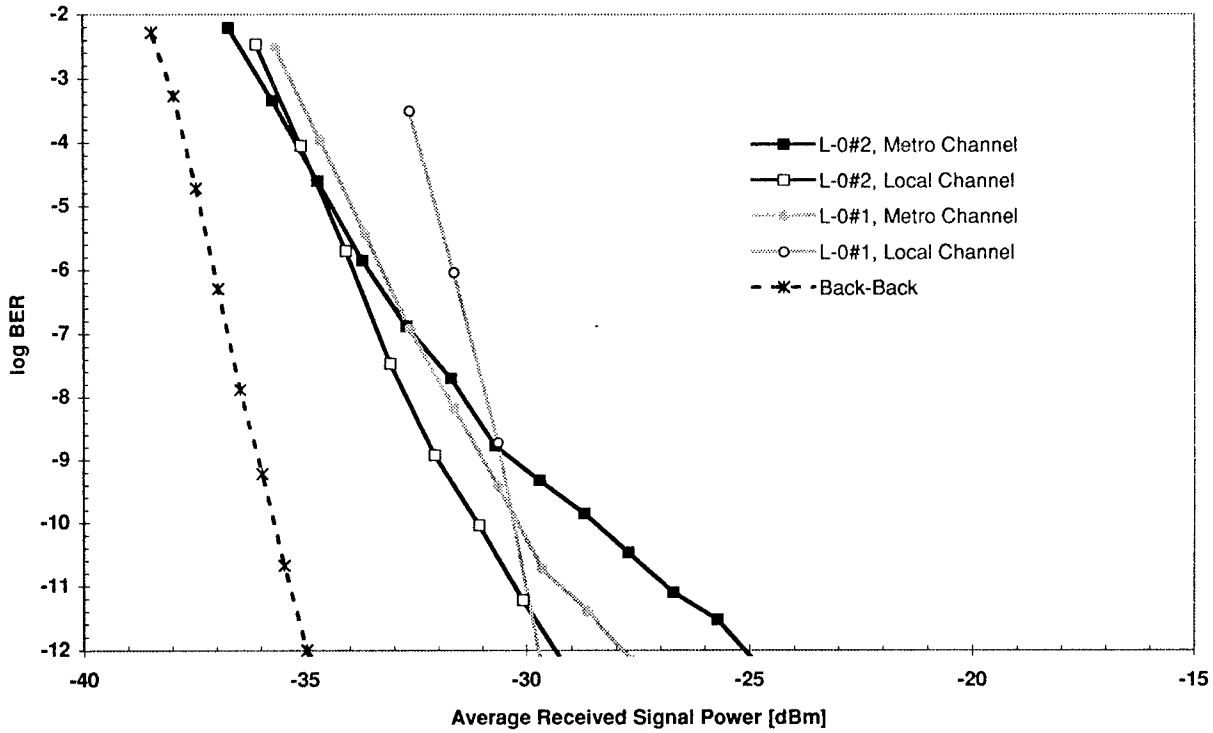


Fig. 3 Bit error rate performance for representative Level-0 local and Level-1 metro channels in both local area hubs Level-0 #1 and #2.

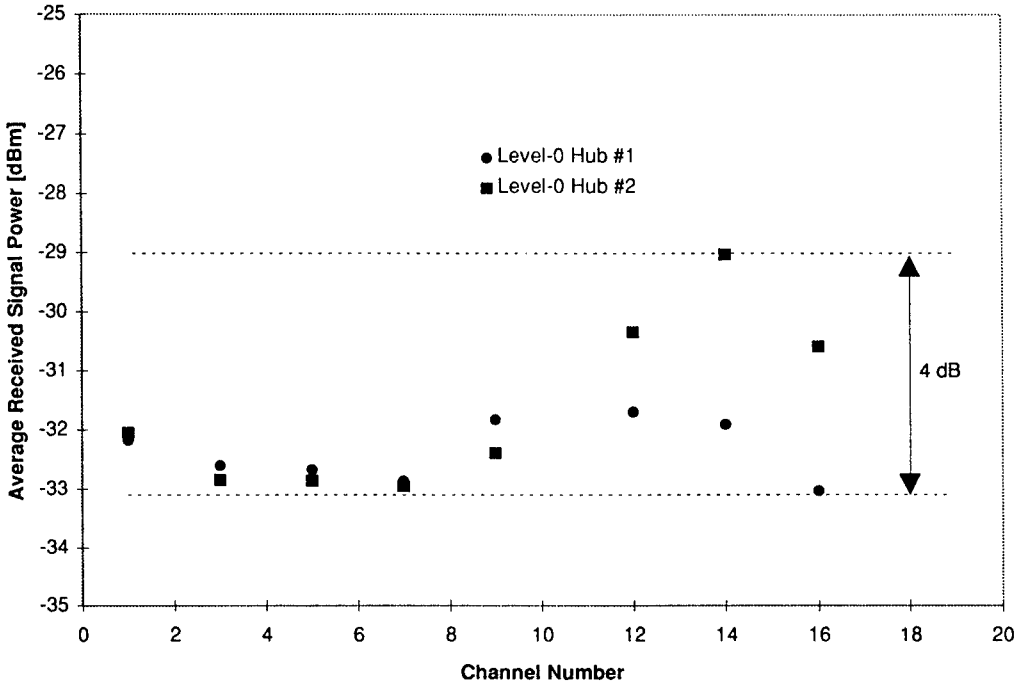


Fig. 4 Summary of bit error rate performance for all channels expressed as the receiver sensitivity for detection at 10^{-9} bit error rate for 2^{23}-1 PRBS. Circles represent Level-0 #1 operation and squares represent Level-0 #2 operation. Open data show local channels, solid data show metro-routed channels. The even numbered channels represent multihopped operation (Channel 12 two hop, and Channels 14 and 16 three hops) transmitted through the Level-1 hub and as much as 50 km of normal dispersion fiber with partial dispersion-compensation.

11:45am - 12 noon
MA5

A Wavelength-Routing Node by Using Multifunctional Semiconductor Optical Amplifiers and Multiple-Pilot-Tone-Coded Subcarrier Control Headers

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Wavelength-Division-Multiplexing (WDM) can dramatically increase the capacity of optical networks through simultaneous transmission of multiple channels on the same fiber. Furthermore, a wide-area WDM network may be composed of many local-area WDM networks, with certain wavelengths accessing the WAN and certain other wavelengths accessing each LAN. For a WDM access node at the WAN-LAN gateway, a wavelength routing function is required: if the data packets are destined for this LAN, they will be dropped and wavelength shifted to the apropriate wavelengths, otherwise, they will pass through the access node unaffected. Recent work has reported the dynamic wavelength shifting by using an 8-bit 50-Mbit/s-modulated subcarrier control header [1].

An SOA has previously been investigated as a multifunctional device, e.g., a simultaneous channel dropper and wavelength shifter [2]. We report here an experimental demonstration of dynamic wavelength routing based on multifunctional SOAs. To reduce the processing and transmission delay [3], a multiple-pilot-tone-coded subcarrier header scheme is proposed. In such a scheme for which each of n subcarrier tones have m header bits, the number of addressable nodes would be 2^{m*n}. This scheme differs from that reported in [3] since the number of required subcarriers scales logarithmically with the number of addressable nodes, not linearly. It may also be a desirable alternative to the multiple-wavelength-coded header scheme [4] because dispersion will limit the number of parallel wavelengths which can be used for addressing .

Figure 1 shows the experimental setup. The incoming packets are at 1571 nm (λ_1). The baseband is ASK modulated at 1 Gb/s preceded by a multiple-pilot-tone subcarrier header. The multiple-pilot-tone consists of three subcarriers f_1, f_2 and f_3 transmitted in parallel time slots located at 1.2, 1.4 , and 1.6 GHz, respectively. The specific routing information is determined as follows: f_1 informs the switch as to whether the packets are destined for this LAN; f_2 and f_3 inform the switch as to which of the 4 local wavelengths the packet will be shifted onto. Since the dynamic routing to a specific local wavelength has already been demonstrated [1], we focus on the packet passing through the switch unaffected or dropped at the switch and wavelength shifted for a local node destination. Passing or dropping is determined by switching "on" and "off" f_1 while keeping f_2 and f_3 always "on". The packets are programmed so that 1/3 of the traffic is destined for this access node while 2/3 is passed on to other access nodes.

Multifunctionality of the SOA is demonstrated as follows. At the beginning of each packet time slot, the pilot-tone header is detected by the reverse biased SOA1. The detected pilot-tones are demodulated by 3 subcarrier demodulators and input to the control board in parallel. When f_1 is "on", the control board emits a signal to switch SOA1 "on" while switching SOA2 "off". The incoming packets will saturate the gain of SOA1, and all data is inversely copied to a cw probe signal at 1552 nm (λ_2). When f_1 is "off", SOA1 will be switched "off" and SOA2 will be switched "on", allowing the packets to pass this access node unaffected. The real-time wavelength routing is shown in the oscilloscope traces of Fig. 2. The incoming packets are successfully routed according to the subcarrier control headers preceding it. The bit-error-rate (BER) measurements are performed for the output routed packets, with a sensitivity of -29.0 dBm for passed packets and -28.6 dBm for wavelength-shifted packets.

References

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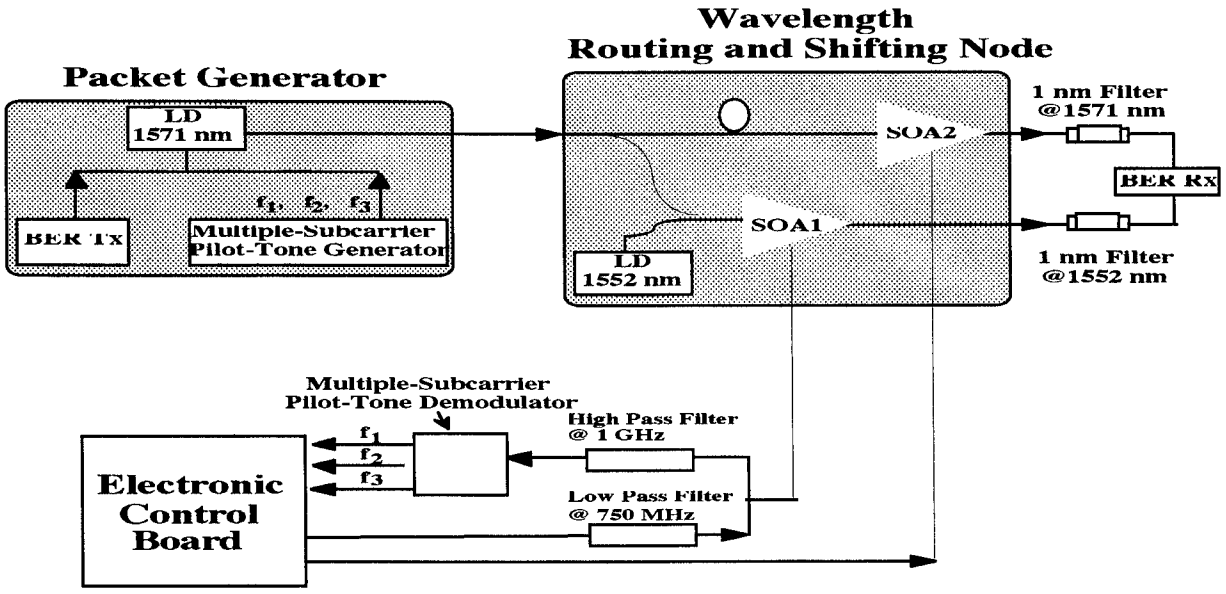


Figure 1. Experimental setup of the wavelength routing node.

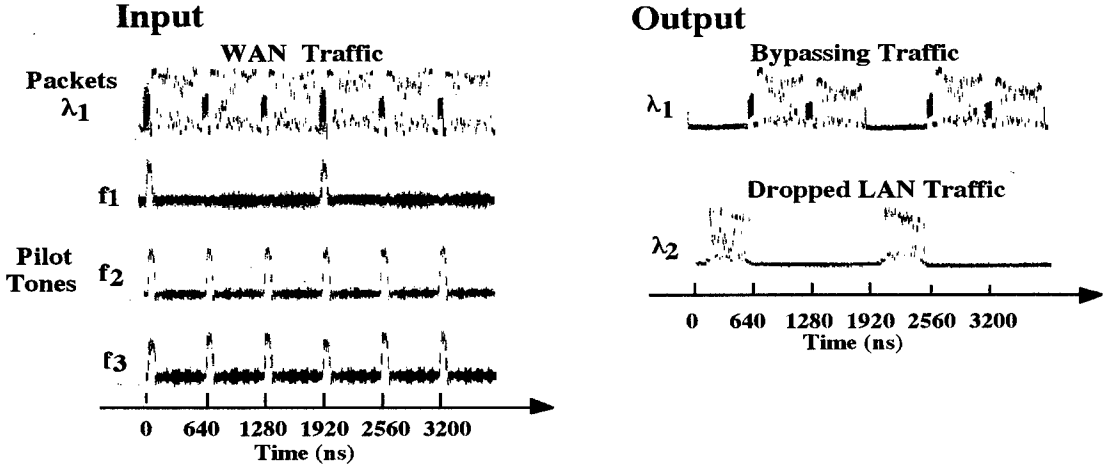


Figure 2. Oscilloscope traces of the packets at the input and output of the wavelength routing node.

2:00pm - 2:15pm
MB2

A Fiber Loop Buffer Storing Variable Length Data Packets at 18 Gb/s for 200 Circulations

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The development of system technologies for high speed, time-division-multiplexed (TDM) local area networks (LAN's) is an active area of research [1]. Because bandwidth on demand represents an important network service, and because all network users may not generate or accept data at the ultrafast data rates, optical buffers operating at the network data rate are key components. Previously, two types of optical packet buffers have been loaded and unloaded. Passive loop buffers have stored 2.5 Gb/s data packets for 30 circulations[2] and active loop buffers have stored a 1 Gb/s pattern for long periods of time[3]. Theoretically, there is no limit on the ultimate number of circulations possible in active loop buffers[4]. We present the first results for loading and unloading an active loop buffer with externally generated kbit data packets at data rates of 18 Gb/s. The data packet length in this experiment is compatible with projected packet lengths for ultra-high speed TDM networks[1]. We demonstrate long term storage (200 circulations (equaling 17.6 μs)) and investigate the effect of the patterns' "1's" density on the buffer performance. To the best of our knowledge, these are the highest data rates and largest packet lengths demonstrated for externally loaded optical loop buffers.

The schematic diagram for the active loop buffer is shown in Figure 1. The loop contains a 90/10 input/output coupler. The erbium doped fiber amplifier provides gain, the isolator forces unidirectional operation, and the $LiNbO_3$ modulator sets the data repetition rate in the loop. Energy stability is provided by nonlinear polarization rotation in conjunction with the polarizing elements in the loop. The data packets are generated by externally modulating the 18 GHz stream of 8-ps pulses generated by a modelocked external cavity laser.

Figure 2 shows 1 GHz analogue oscilloscope traces of the buffer output. In Figure 2a, a 11111100 pattern is repeated for 21.3 ns (384 bits). Because the oscilloscope bandwidth is not large enough to resolve the data bit pattern, the packet envelope is displayed. The largest amplitude packet envelope corresponds to the input packet. The subsequent 8 packets are replicas of the input packet. The time between packets is 88 ns, the cavity round trip time. The packets preceding the input packet on the oscilloscope trace correspond to the 198th, 199th and 200th circulation. Notice that the amplitude of the packet envelope has been maintained even after 200 circulations.

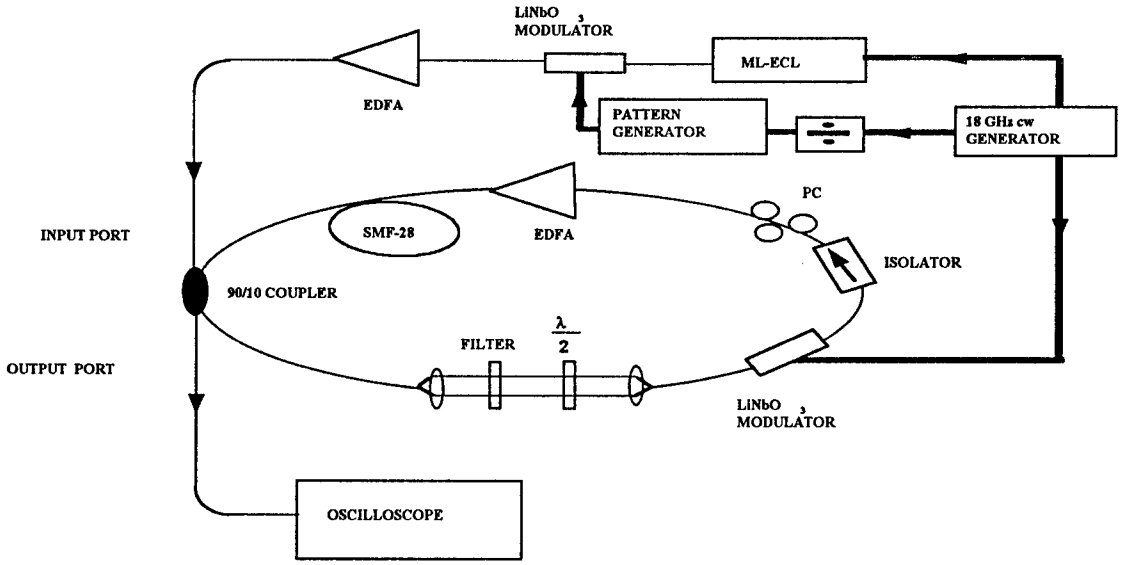
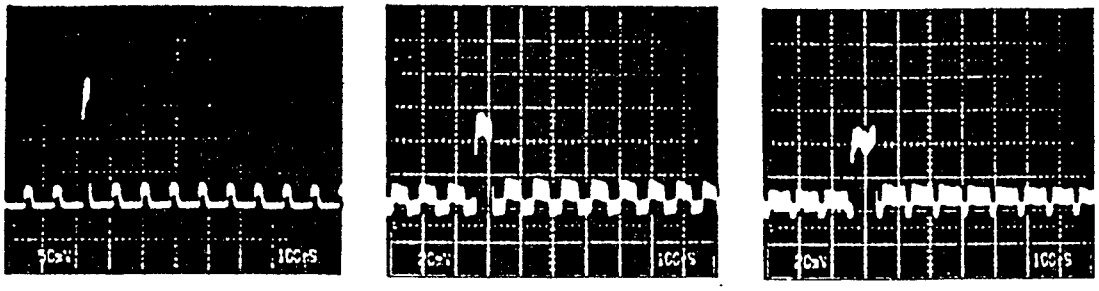


Figure 1. Experimental set-up. Dark lines indicate electrical connections and light lines indicate optical connections. ML-ECL=modelocked external cavity laser, EDFA=erbium doped fiber amplifier, SMF-28=standard single-mode fiber.

Figures 2b and 2c show the buffer output when the input packet length is changed to 54.2 ns (976 bits) and 71.1 ns (1,280 bits). Notice that the amplitude of the packet envelope is maintained in these cases as well. These results suggest that active buffers can store data packets with a wide variance in "1's" density for long periods of time without packet power fluctuations. In addition, the average power of the input packet was varied from approximately 0.5 μW to 40 μW and the buffer operation was maintained suggesting that packets with large variances in average power can be maintained in the loop.



(a) (b) (c)

Figure 2. Oscilloscope traces of data packets coupled out from the loop buffer. a) The input packet length is 384 bits, b) 976 bits and c) 1,280 bits long. In each case the packet was a repeating pattern of 11111100. The total buffer length is 1,585 bits.

Figure 3 shows a portion of the 11111100 pattern detected by a 45 GHz bandwidth photodiode and displayed on a 50 GHz digital sampling scope for the buffer operation shown in Figure 2a. The top trace shows a portion of the pattern from the input packet, the middle trace shows a portion of the packet from the first replica (circulation) and the bottom trace shows a portion of the pattern from the 200th replica. Notice how well the pulses, "1's", and the "0's", have been maintained. These initial results suggest that storage times as well as data rates can be scaled to much higher values.

In conclusion, we have demonstrated an active loop buffer storing an externally generated data packet with a data rate of 18 Gb/s for 200 circulations. Stored data packet lengths ranged from 21.3 ns (384 bits) to 71.1 ns (1,280 bits). The total capacity of the buffer was 1,585 bits. This data rate and stored packet length are the highest reported for externally loaded optical loop buffers.

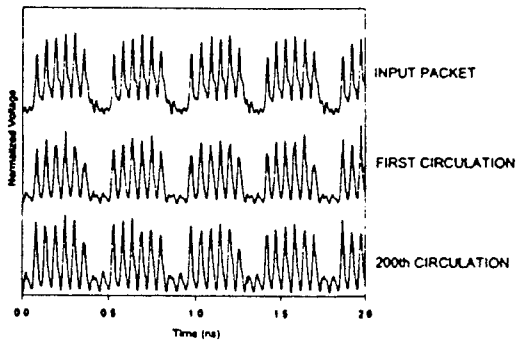


Figure 3. Portions of the data packet at the input to the buffer (top trace) and at the 1st (middle trace) and 200th (bottom trace) circulation. Several data traces have been averaged in each case.

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2:15pm - 2:30pm
MB3

High-Speed Header Processing Using Synchronized Fiber Lasers Driving All-optic Logic Gates

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We show all-optic logic gates driven by synchronized erbium-doped fiber lasers (EDFL's) to perform 100Gb/s header processing in TDM packetized networks or optical add/drop multiplexers. We experimentally demonstrate AND and XOR logic functions in low-birefringent nonlinear optical loop mirrors (Low-Bi-NOLM's) with switching energy as low as 9pJ and peak switching contrast of 8:1. We show that the Low-Bi-NOLM's satisfy decision-making capabilities in a header processor such as cascadability and Boolean-complete logic functions. [1] Our novel AOM-grating scheme of synchronization provides 30 times the length and 10 times the bandwidth as compared to the scheme using piezo-electric transducers (PZT's).[2] We have achieved synchronization of two passively mode-locked EDFL's with a timing jitter of approximately 1.3 times the pulse width. We are now integrating the synchronized EDFL's and all-optic logic gates, which are key components for packet addressing for 100 Gb/s applications.

The experimental setup is shown schematically in Fig. (1). In preliminary experiments, one passively mode-locked EDFL is used to drive the Low-Bi-NOLM. Following an optical isolator, the laser beam is split into three beams, namely, two signal and one control beams by using two polarization beam splitters (PBS's). The timing between the two signal and the control pulses are controlled by two optical delay stages. The control pulse is coupled to the 3dB coupler/splitter in the fiber loop, while the signal pulses are coupled into/out of the fiber loop by two fiber polarization combiners/splitters (FPCS's). Let O be the output of the 3dB coupler, C be the control, $S_{1,2}$ be the two signals. Then we have $O = C^*(\overline{S}_1 * S_2 + S_1 * \overline{S}_2)$, where overbars represent logic complementary. Thus, we can obtain logic functions of NOT, AND, XOR by biasing the gate according to the above formula. For example, an inverter $O = \overline{S}_1$ can be obtained by setting $S_2 = C =$ TRUE, an AND gate $O = C^* S_2$ by setting $S_1 =$ FALSE, or XOR gate $O = \overline{S}_1 * S_2 + S_1 * \overline{S}_2$ by setting C = TRUE.

The results of logic functions are shown in Fig. (2). The solid curve shows the function of an AND gate as well as the tolerance of timing jitter. The vertical axes is the switching contrast, while the horizontal axes is the optical delay between control and signal pulse. The timing window is about 1.3 times the pulse width. The dotted curve shows the function of an XOR gate with presence of both signals. When both signals are present, we have a low output, and when one of the signal is present, we have a high output. The timing between the control and one of the signal determines if both or one signal is effective. The switching energy is about 9pJ. We have also demonstrated cascaded operations of two Low-BI-NOLM's.[1] Consequently, we have demonstrated that our Low-Bi-NOLM's meet the main requirements for the all-optic logic gates needed in high speed header processors.

Designed as the driving source of the logic gates, synchronization of two passively mode-locked lasers is realized by using novel AOM-grating scheme, as shown in Fig. (1). The error signal resulted from the timing jitter between two EDFL's , by which can be obtained by differencing two fast detector outputs in an RF mixer, and is fed back to the driver of the AOM placed inside the slave laser. The non-deflected zero-order beam serves as the output, while the deflected first-order beam is reflected back by a grating. Through the AOM driver, the deflection angle and cavity length vary in proportion to the error signal. This design provides 300μm tuning range and 10 kHz bandwidth.

As a characterization of the synchronization, the cross-correlation of two EDFL's is shown in Fig. (3). The solid curve is an average of 32 sweeps in 30sec., while the dotted curve is a single sweep in 200 μs. The broadening of the averaged curve is due to low frequency residual jitter that has a period of about 40ms. Approximated with a Gaussian distribution for the jitter, the average timing jitter is about 1.3 times the pulse width(5ps), which is extracted from the full-width-at-half-maximum of the cross-correlation.

In summary, we have experimentally demonstrated two key building blocks for 100 Gb/s TDM systems that can be used for header processing in packet networks. Our Low-Bi-NOLM's can be used as an inverter, AND gate, or an XOR gate with a switching energy of 9 pJ. Synchronization of two passively mode-locked EDFL's has been achieved with an timing jitter of 1.3 pulse width. We will report experimental results from combination of these components and further cascading of logic gates.

Work at the University of Michigan is supported by the National Security Agency.

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2. M. Jiang, *et. al*, "Synchronization of two passively mode-locked Er:doped fiber lasers using an acousto-optic modulator and grating scheme", to be published, Opt. Lett. 1996.

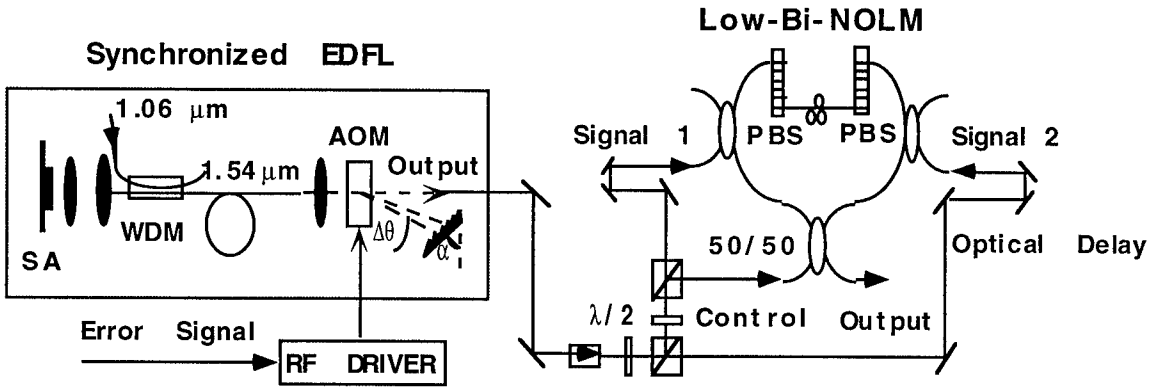


Fig. (1) Experimental setup for testing synchronized EDFL's driving Low-Bi-NOLM. (SA=saturable absorber; AOM=acousto-optic modulator; PBS=polarization beam splitter; WDM=wavelength division multiplexer).

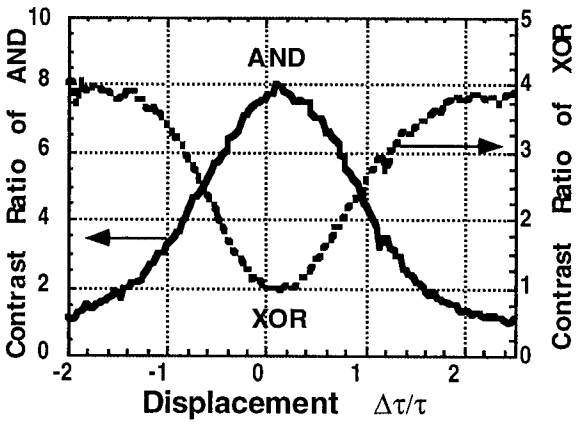


Fig. (2) Logic AND and XOR functions Low-Bi-NOLM.

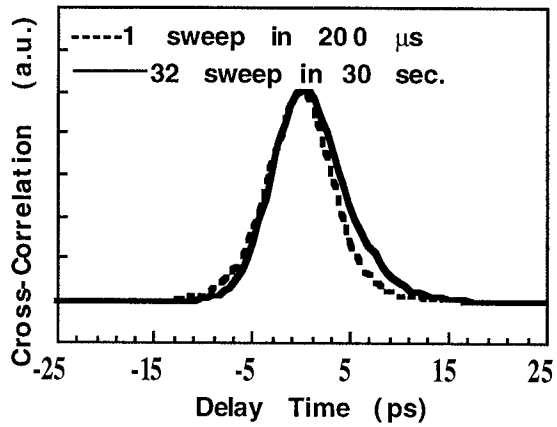


Fig. (3) Cross-correlation of two synchronized EDFL's.

2:30pm - 2:45pm
MB4

Experimental Demonstration of Bipolar Codes for Direct Detection Multi-user Optical Communication [1]

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Abstract — **We report the first experimental demonstration of a broadband spectral encoding and decoding technique using bipolar codes for optical code–division multiple access. The code-word correlations are verified and rejection of multiple-access interference is demonstrated.**

I. Introduction

The application of code-division multiple access techniques in the optical domain has not been very successful, primarily due to the unipolar nature of the direct detection optical channel. Recently we proposed an all-optical encoding and detection method that is equivalent to the use of bipolar spreading codes in the radio domain [1]. The technique uses the broad bandwidth of the optical channel to create an effective bipolar channel using longer unipolar codes. In the spectral encoding realization, a portion of the spectrum from an eribium-doped superfluorescent fiber source (SFS) [2] is encoded using a grating and amplitude mask.

II. Experiments

Fig. 1 illustrates the geometry for each encoder module in the system. A planar holographic grating of 1200 grooves/mm disperses the SFS beam, and the first–order spectrum is collected and collimated by the concave–spherical mirror 1. On the amplitude mask, the spectrum is formed to a 30 μm high horizontal stripe, where 1 nm of optical bandwidth corresponds to 1 mm of horizontal distance. The mask pattern is the concatenation of the unipolar code U and its binary complement $\overline{U}$, where U is obtained from a length-N bipolar code, by replacing each -1 with 0. Portions of the spectrum reflected off the amplitude mask are collected on mirror 1 and focused back to the grating surface. The recombined beam exits the encoder module representing the "0" symbol. The remaining portion of the spectrum, the spectral complement of the reflection, is transmitted by the amplitude mask and returned to the grating by mirror 2, forming the beam representing the "1" symbol. ON/OFF modulation of the "0" and "1" beams of the encoder forms the binary information symbol.

The geometry for each decoder module is the same as the encoder, with the transmission channel replacing the SFS beam. For the decoder, the "0" and "1" output beams are coupled to a balanced photodetector pair, where the detector current represents the true bipolar correlation of the codes at the encoder and decoder. Fig. 1 also shows the mask patterns of one length-16 and two length-32 codes (from bipolar Walsh codes of lengths 8 and 16), denoted A, B and C, respectively. The chip widths vary to compensate for the non–uniform source spectrum, so that the per-chip power is uniform as required by the coding. Mask patterns are created on glass substrates by photo-etching an evaporated aluminum coating.

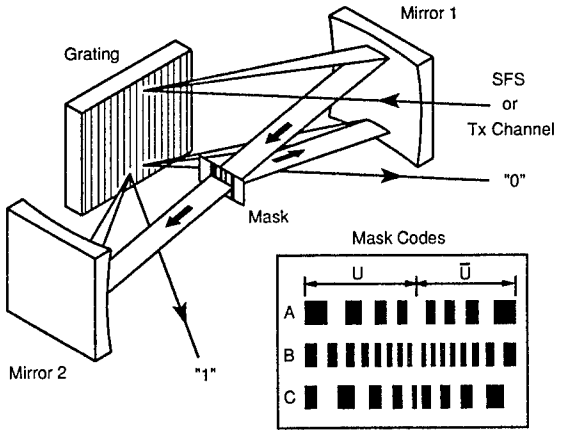


Fig. 1: Geometry for the grating based encoder/decoder modules, and the mask codes A, B, and C.

Prior to measuring the correlations and demonstrating the rejection of multiple–access interference (MAI), we made a measure of the total dispersion and resolution for the encoder–decoder system. A special mask, comprised of three 100 μm (0.1 nm bandwidth) chips spaced 2.5 mm (2.5 nm spectral separation) was fabricated for the encoder and decoder. A mask convolution was performed, whereby the mask of the decoder was moved horizontally with respect to the incident beam, while the total transmitted power through the decoder mask was recorded. Shown in Fig. 2 are three measured peaks corresponding to the alignment of all three chips, two chips, and just one chip, as viewed from right to left. Plotted with a dashed line is the theoretical convolution curve for the masks. From the shifted location of the smaller measured peaks, a distortion of 100 μm over a 5 mm field in the decoder mask plane is apparent. In addition, it is also clear from the plot that the width of the measured peaks is larger than theory predicts. Ideally, the convolution of two 100 μm chips should result in a triangular spatial distribution of power with a base of 200 μm width.

[1] This work was jointly supported by the Advanced Technology Program of the Texas Higher Education Coordinating Board, GTE, Inc., and the U.S.A.F. Phillips Laboratory.

If the linear slopes of the measured peaks are extended to the horizontal axis, the base of the largest distribution is at least 500 μm. Applying the Rayleigh criterion, the minimum chip spacing for this system, or equivalently the minimum chip size, is estimated to be 250 μm. The amplitude of the measured peaks is not proportioned as theory would predict, an effect that can be attributed to the non-uniformity of the source spectrum. Since only $\sim$ 10% of the grating surface is currently illuminated, expansion of the incident beam should result in improved resolution for future experiments.

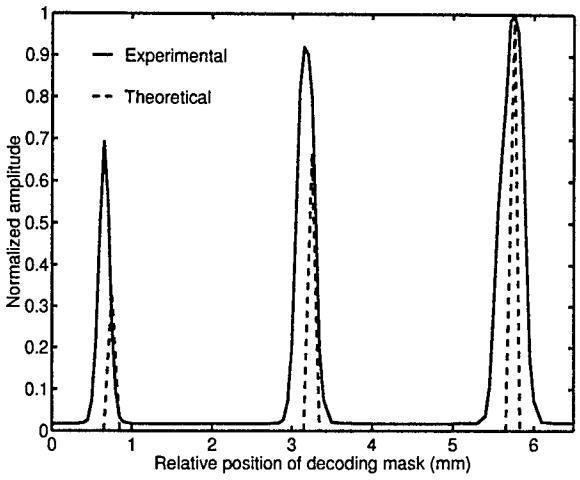


Fig. 2: The intensity pattern obtained from convolving the 100 μm chip mask to test the total resolution and dispersion of the system.

The correlation measurements were performed with a single user system, comprised of one encoder module matched to one decoder module. The results are shown in Fig. 3. Separate graphs (a,b,c) are presented for each code

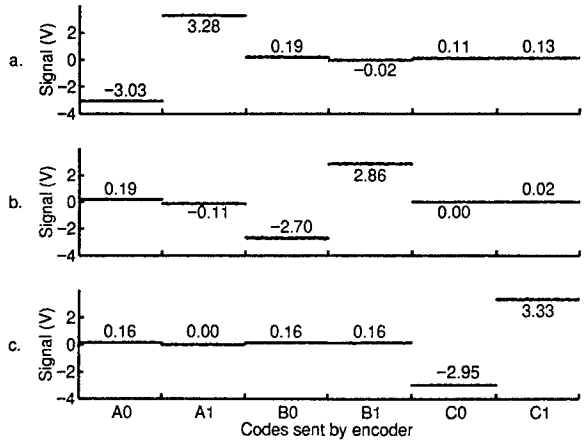


Fig. 3: Correlations of the codes seen on the oscilloscope. Plot (a) shows the correlations for user A, plot (b) for user B, and plot (c) for user C.

positioned at the decoder, plotting the balanced receiver voltage as a function of the code sent by the encoder. The DC voltage levels shown are the actual waveforms stored by the oscilloscope during each correlation. For each graph, when the encoder is matched to the decoder, a large positive or equally large negative auto-correlation is recorded. Conversely, when the encoder sends a code that does not match the decoder, a small cross-correlation value is recorded, which in all cases is measured to be less than 8% of the auto-correlations. The good contrast between the auto- and cross-correlation values shows that a binary information symbol can be recovered by an appropriate threshold operation.

The rejection of MAI was demonstrated with a two user system, comprised of two encoders coupled to one decoder. Shown in Fig. 4 are the results of matching the desired user's code to B or C while varying the interference user's code. The plots show the amount of interference detected by the desired user, obtained by subtracting the desired user's auto-correlation from the signal measured with two users. As expected, the decoder cannot make a discrimination when the interference user is matched to the desired user's code, as evidenced by the large values for the B codes of plot (a) and the C codes of plot (b). For the other codes, the interference level is equal to or less than 10% of the desired signal, demonstrating the capability of the decoder to reject MAI.

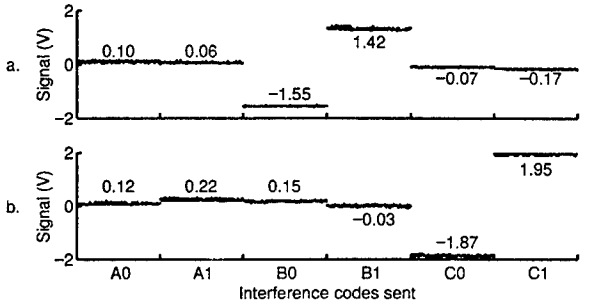


Fig. 4: Waveforms obtained from subtracting the autocorrelation value from the two-user waveform stored by the oscilloscope. Plot (a) is the measured interference for user B, plot (b) is for user C.

III. Conclusion

We have presented experimental results that demonstrate the use of bipolar codes for spectral encoding and decoding in optical code-division multiple-access. The auto- and cross-correlation measurements have shown that a binary information symbol can be recovered using an appropriate threshold operation. Multiple-access interference has been shown to be rejected in a multi-user situation. Technical improvements in the spectral encoding and decoding process are likely to lead to improved system performance and enhanced practicality for use in optical CDMA.

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2:45pm - 3:00pm
MB5

Demonstrations of All-Optical Conversions Between the RZ and NRZ Data Formats Incorporating Noninverting Wavelength Shifting Leading to Format Transparency

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All-optical wavelength-division-multiplexed (WDM) networks may be required to support a variety of modulation and data formats. Two standard data formats are the return-to-zero (RZ) and non-return-to-zero (NRZ) formats. The RZ data format is quite useful in many applications, including passive TDM, soliton generation, and the suppression of Brillouin scattering [1,2]. Also, since some optical processing operations unintentionally change the data format [3,6], fully functional WDM networks should have the capability of all-optically converting between the RZ and NRZ formats. Previous work [4] has demonstrated all-optical RZ-to-NRZ conversion using a nonlinear optical loop mirror at 10-Gb/s, but the performance of this system was shown to be highly sensitive to the loop polarization state.

In an earlier paper [5], we demonstrated an NRZ-to-RZ (NRZ→RZ) converter that uses semiconductor optical amplifier (SOA) gain modulation to convert an input NRZ signal into an output RZ signal at the same wavelength. In this paper, we demonstrate a polarization insensitive SOA-based system that converts an RZ WDM channel into the NRZ format (RZ→NRZ). Our system allows the input RZ wavelength to be either preserved *or* wavelength shifted. Additionally, we use the previous NRZ→RZ converter and our new RZ→NRZ converter to realize an all-optical NRZ→RZ→NRZ *reconverter*; such an operation may be necessary for intermediate optical processing of packets. To demonstrate the robustness of the reconverter, we incorporate 4 EDFAs and 80 km of fiber between the individual converters. These functions may significantly help to realize RZ/NRZ *data format transparency* within dynamically-reconfigurable and fully-functional WDM networks. The fundamental operations used in our system include: optical sampling, wavelength shifting using cross-gain compression [6], time multiplexing and SOA gain modulation. We demonstrate the RZ→NRZ and NRZ→RZ→NRZ functions at 1-Gb/s while incurring low power penalties (<2 dB) for both cases.

Figure 1 shows the RZ→NRZ converter which consists of two cascaded SOAs, two optical sampling pulse trains, and a CW probe signal. Cross gain compression wavelength shifting relies on an intensity-modulated pump signal and a low power CW probe signal being simultaneously coupled into an SOA. The pump signal saturates the SOA gain only when its bit pattern is "HIGH" and results in an inverse modulation of the SOA gain that is available to the probe. The cross gain compression causes the complement of the pump data to be impressed onto the probe. This principle is used to realize the RZ→NRZ converter. When an input RZ pump signal at λ_1 is coupled into SOA_1, it is optically sampled by a pair of synchronized low power RZ probe pulse trains at λ_2 and λ_3. These pulse trains can be generated by electronically recovering the input clock signal to modulate a bank of two probe lasers.

To demonstrate this converter, pulse trains are generated by modulating two probe lasers with the transmitter clock. By optically sampling the input RZ pump signal, the complement of the pump data is impressed onto each probe pulse train by SOA_1. At the output of SOA_1, both probe signals at λ_2 and λ_3 are amplified and filtered, after which the signal at λ_2 is delayed by half a bit. Both amplified and interleaved probe signals then become the pump signals for SOA_2, in which the complement of their data is **wavelength shifted** onto the input CW probe signal at λ_4 by cross gain compression. This results in an NRZ signal at λ_4 having the *same* data polarity as that of the original RZ signal at λ_1. Also, note that the wavelength of the output NRZ signal can be the ***same*** as that of the original RZ signal by setting $\lambda_4=\lambda_1$. This converter is, in principle, limited to ~20 Gb/s [7]. Figure 2 shows the 1-Gb/s oscilloscope traces; a conversion power penalty of only ~0.8 dB is measured with a PRBS 2^{15}-1 sequence.

We demonstrate an NRZ→RZ→NRZ ***reconverter*** by cascading a NRZ→RZ converter with the RZ→NRZ converter. To show system robustness, the two converters are interconnected through a cascade of four EDFAs and 80 km of dispersion shifted fiber (DSF). Figure 3 shows the oscilloscope traces from our demonstration. In this case, a 1-Gb/s NRZ 1571-nm signal is first converted into the RZ format and is then wavelength shifted and ***reconverted*** back into a *noninverted* NRZ signal at 1540-nm. Figure 4 highlights a power penalty of only ~2.0 dB incurred by the reconverter.

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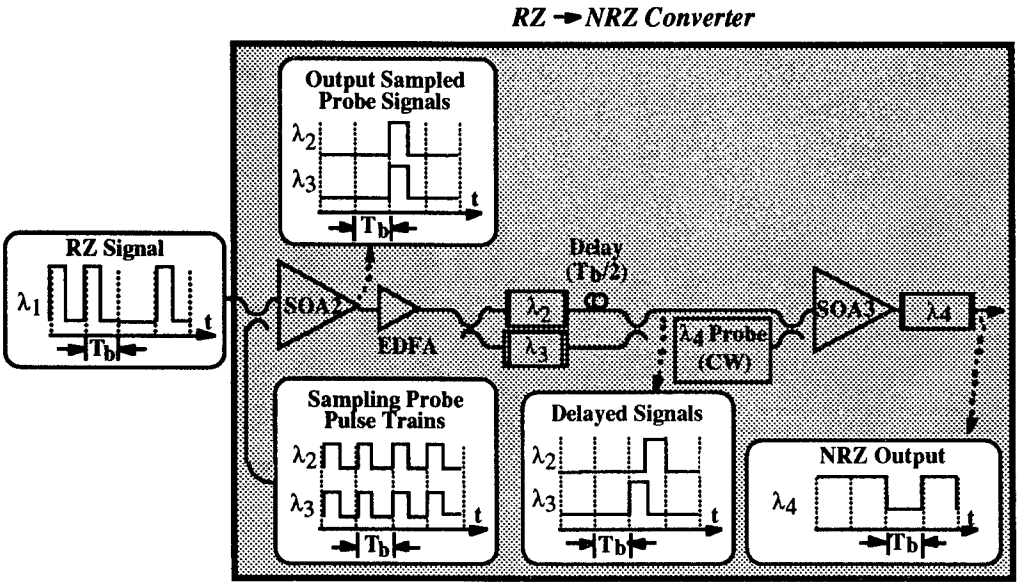


Figure 1. All-optical RZ→NRZ converter.

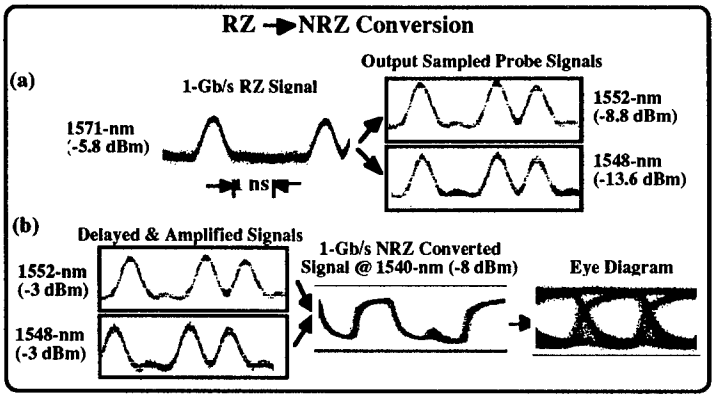


Figure 2. RZ→NRZ converter oscilloscope traces showing (a) the input 1571-nm RZ signal and the output sampled probe signals; (b) the amplified and delayed pump signals and the converted NRZ output signal.

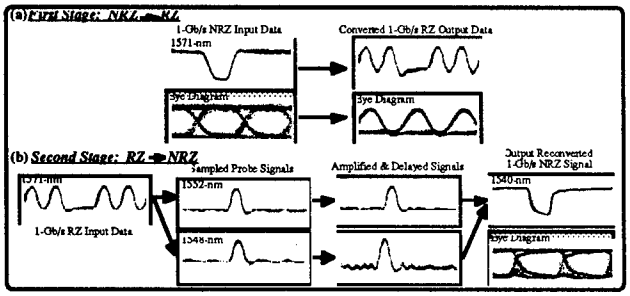


Figure 3. NRZ→RZ→NRZ scope traces showing (a) NRZ→RZ conversion; and (b) RZ→NRZ conversion recovering the original NRZ data.

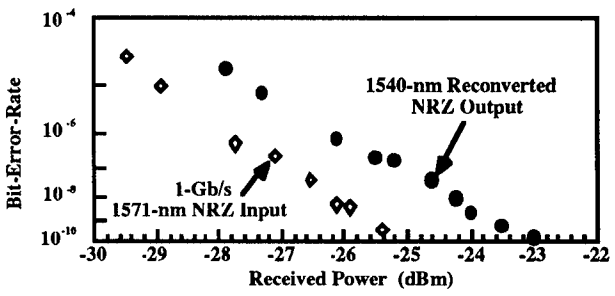


Figure 4. BER curves of the NRZ→RZ→NRZ reconversion process, showing a penalty of ~2 dB.

4:00pm - 4:15pm
MC2

External Cavity Laser Array with Monolithically Integrated Glass Waveguide and Rowland Circle Grating for WDM Applications

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Summary:

Wavelength division multiplexing (WDM) is rapidly becoming a mainstream technology for high capacity optical communications. One of the critical components needed in WDM systems is a multi-wavelength laser array. [1-4] The external cavity laser array configuration [2,3], which exhibits accurate channel spacing control, is particularly appealing for many WDM systems. Up to now all integrated external laser array processes require one or more steps of semiconductor regrowth and/or alloy disordering to produce the passive elements. These greatly limit the materials and devices which can be used. In this paper we present an integrated WDM laser array based on an external glass cavity Rowland circle spectrometer which does not require a regrowth process. The laser array process is fully compatible with the conventional ridge laser process and, thus, can be implemented in all materials systems.

Fig. 1 shows the schematic design of the WDM laser array. The external cavity is a glass waveguide Rowland circle spectrometer, formed by etching a well into the semiconductor laser material and filling with a PECVD (plasma enhanced chemical vapor deposition) SiO_2 planar waveguide. The integrated laser arrays were processed on MBE grown GaAs/AlGaAs GRINSCH single quantum well laser materials. The ridge lasers and the spectrometer well were etched by two chemically assisted ion beam etching (CAIBE) steps, a custom-made ultra high vacuum CAIBE system using Ar as the ion beam source gas and Cl_2 as the reactive gas. [5] Photoresist was used as the etching mask which was patterned by a 10x i-line projection aligner. During the p-metal (laser electrode) deposition, the grating teeth and the floor of the spectrometer were also coated to provide an optical shield. A PECVD SiO_2 film was then deposited into the well to form the Rowland circle spectrometer. The air-SiO_2-Au planar waveguide is relatively low loss and the presence of gold under the glass waveguide favors the fundamental mode operation of the laser array - a plus for WDM applications. [6] One of the critical processing steps is grating and facet etching during the formation of the spectrometer well. The following SEM photograph demonstrates the high quality etching from CAIBE system. Fig. 2 was taken at the grating region prior to the glass waveguide deposition. The grating facets were of high optical quality, limited by the graininess of the photoresist.

The nine-wavelength laser array had a Rowland circle grating radius of 10,883 μm, a grating period of 5.037 μm and a diffraction order of 12. The chip size of the laser array is 0.15 cm by 0.96 cm. This design is based on the point spread function(PSF) of the Rowland circle grating. [7] The following equation can be used to evaluate the choices of grating period, diffraction order, grating aperture(size) and Rowland circle size.

$$I=|\Sigma c \times \exp([2\pi i(PA+PA')/\lambda])|^2$$

I is the intensity. P is a point on the grating. A is the source point. A′ is any point along the Rowland circle. c is an intensity normalization constant.

Fig. 3 shows the emission spectrum of the nine-stripe laser array, the free spectral range (FSR) is ~68 nm and the wavelength spacing is 1.5 nm. The data shown are for stripes biased 60 mA or more above threshold. This additional current is needed to lock the laser to the grating feedback wavelength. This is due to a large undesired feedback from the etched facet (uncoated) and to a mismatch of gain spectrum of the laser material to the designed wavelengths of the WDM laser array. The threshold current increase due to the integrated glass waveguide is only 5 mA. We expect to lower the threshold current appreciably with a reduction of the optical feedback from the etched laser facet. This laser design offers a convenient method of fabricating integrated external cavity lasers in novel laser material where the material regrowth is difficult or unavailable. Detailed results will be discussed in the talk.

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Fig 1:Schematic illustration of the monolithically integrated WDM laser array

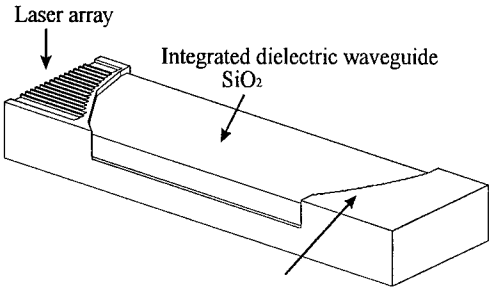


Fig 2:Rowland circle grating teeth etched by CAIBE. The surface of curved gratings is covered by Au metal to increase reflectivity.

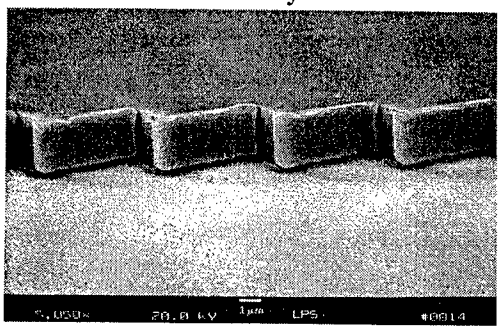
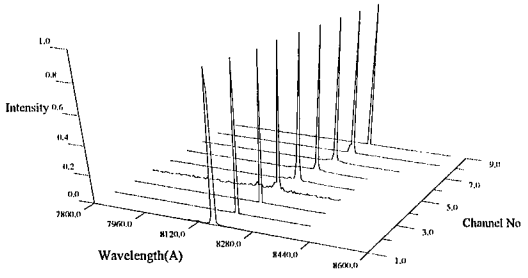


Fig 3:Normalized intensity from outputs of laser array. The channel separation is 1.5 nm



4:15pm - 4:30pm
MC3

32 Channel WDM Graphic Equalizer

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In wavelength division multiplexed (WDM) networks, multiple data channels are carried by a single fiber. As the signals propagate through the network, power losses from propagation, splitting and coupling are periodically replenished by Erbium-doped fiber amplifiers. It is important to maintain similar signals levels on all channels to avoid crosstalk and data loss. However, the amplifier gain profile tends to favor the center wavelengths, so that a WDM signal propagating through a chain of amplifiers grows increasingly nonuniform. Fixed wavelength-dependent losses can in principle be compensated by pre-emphasizing the input levels[1]. Alternatively, the amplifier gain spectrum can be flattened using a relatively simple passive in-line optical filter to attenuate the central wavelengths[2].

However, fixed attenuation or pre-emphasis can only compensate for a fixed path with fixed input power and amplification. In an active network, inputs can switch on and off. Each time this happens, the available amplifier gain changes. In a passive ("transparent") optical network, each channel may follow a different path, with different losses and amplification. Each time a signal is routed to a new path, the levels can change. In such networks, active level compensation at each independent wavelength channel is needed. This paper describes an active 32 channel WDM equalizer using free space optics and a 1x32 array of surface-normal reflective variable attenuators. The packaged equalizer, with FC connectors to standard single mode input and output fiber, measures 7 x 4 x 2 inches.

Figure 1 is a drawing of the optomechanical system showing how the fiber input is collimated by a f=25 mm doublet lens, diffracted by a 600 line/mm blazed grating, then focused by a f=50 mm triplet lens onto the device plane. In a simple imaging system, reflected light would return to the input fiber. However, the collimation lens is shifted so that the reflected light is picked off by a fold mirror into a third lens which focuses the output into a separate output fiber. This design has no intrinsic loss. Total insertion loss measured with a gold mirror at the device plane, was 4.0 to 5.5 db (into single mode output fiber) and 3.7 to 4.9 db (into 62.5 μm core GRIN multimode output fiber) depending on input polarization. This indicates that overall efficiency is limited primarily by the grating efficiency, surface reflections and modulator insertion loss rather than optical aberrations. The spot full width at half maximum at the modulator plane was 25 μm.

The 1x32 attenuator array shown in Figure 2 was fabricated with MARS (mechanical anti-reflection switch) devices developed at AT&T Bell Labs.[3] This device uses electrostatic force to deflect a $\lambda/4$ thick layer from $3\lambda/4$ to $\lambda/2$ above the surface, effectively changing a single-layer dielectric mirror into an antireflection coating. MARS modulators typically have a switching time of less than 1 μs, a contrast ratio of > 50:1, and an insertion loss of about 2 db. The modulator array had a 35 μm pitch and an 30 μm optical window, for a total array length of 1.09 mm. This yields an operating range of 1542 - 1563 nm with a 0.68 nm (84 GHz) spacing.

Figure 3 shows the output of one channel of the equalizer with a 78 V square wave drive at 10 KHz. The lower trace shows the crosstalk which occured when this modulator was turned off and the adjacent device was driven. The contrast ratio was more than 20 db at the center wavelength, and more than 10 db over a 0.2 nm wavelength range. The response time shown was limited by the power meter. The rise and fall times of the device were measured with a fast detector to be less than 100 ns.

To summarize, we have fabricated a packaged 32 channel active intensity equalizer for WDM fiber networks using free-space optics and surface normal MARS modulators. This design could be altered to allow automatic level control by monitoring the output level with a 1% beamsplitter before the grating and a detector array adjacent to the modulators.

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3 K. Goossen, J. Walker, and S. Arney, "Silicon modulator based on mechanically-active anti-reflection layer with 1 Mbit/s capability for fiber in the loop applications," *IEEE Phot. Tech. Lett.* **6**, 1119-1121, Sept. 1994.

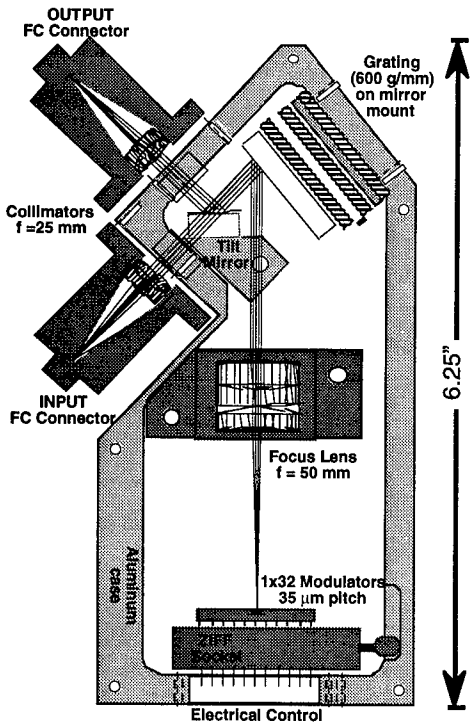


Figure 1 : Optomechanical design

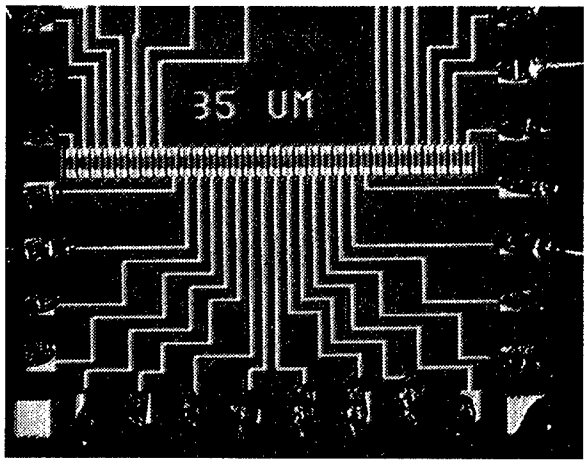


Figure 2 : 1x32 MARS attenuator array

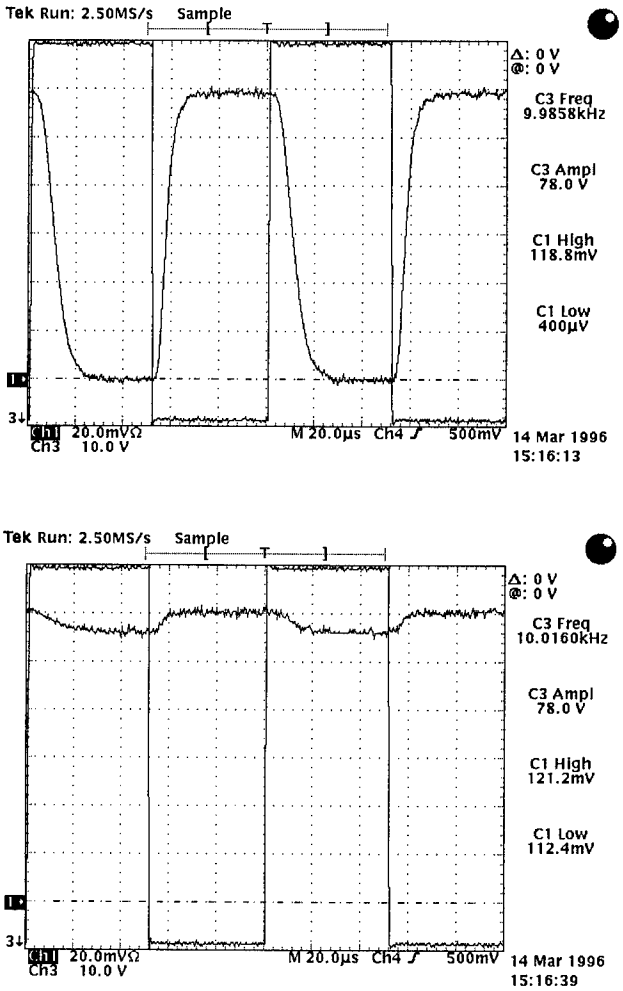


Figure 3: Output signal (top) & crosstalk

4:30pm - 4:45pm
MC4

A Very Simple Integrated Coherent Receiver with Record High Sensitivity

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SUMMARY

Coherent WDM communication systems have a great potential to be applied to local broadband access networks due to its high sensitivity and densely spaced multichannel characteristics. Unfortunately, comparing with a high-bit-rate direct detection system the installation cost of such a system is relatively high. Although the hybrid coherent system can reach almost shot noise limited sensitivity [1], the higher cost can prevent it from gaining ground in the long run. Previously, some research works on the integrated coherent receivers [2-5] have brought in a new direction to reduce the system cost of this technology. However, both the structure and fabrication processes of those devices are quite complex and yields are considerably low.

In this work, we report a high sensitivity integrated coherent receiver with very simple device structure. The fabrication process of this device is so simple that it is nearly no more than making a distributed-Bragg-reflector (DBR) laser. The device structure and its possible application as a broadband access terminal device with both receiving and transmitting functions are shown in Fig.1. The device is composed of a tunable DBR laser and an integrated detector. The incoming ASK or FSK signals are mixed in the DBR local oscillator (LO) cavity. This self-heterodyne operation has previously been reported using the laser gain section for a full duplex operation at 40 Mb/s [6]. In our work the detector and the laser are separated. More important, the laser cavity is carefully designed that only one cavity mode is allowed in the grating stop band. Such an arrangement has produced semiconductor lasers with the highest side mode suppression ratio and very narrow linewidth (800 KHz) [7] to contribute to the sensitivity. It also made possible to utilize the self-heterodyne scheme for multichannel system applications. One should notice that the self-heterodyne scheme will not work in a multiwavelength system if the incoming multiwavelength signals see more than one mode in the stop band.

As shown in Fig. 1 we can use this device as a heterodyne receiver and transmitter with either FSK or ASK format. When a pair of the devices is used for FSK, NRZ transmission and receiving, a free-space beam sensitivity of -43.4 dBm at $1x10^{-9}$ BER for an 108 Mb/s, 2^{15} - 1 pseudorandom signal was obtained. This result is 1.1 dB better than Koch's result [8], even without balanced detector operation. Fig. 2 shows the BER measurement results for signals taking from the detector section and from the gain section of the LO. Signal taking from the LO section had a 6 dB sensitivity penalty due to higher intensity noise and less detection efficiency at that section.

In conclusion, we demonstrated a high sensitivity integrated coherent receiver with very simple structure. The demonstrated device can be an ideal candidate for broadband local access terminal devices.

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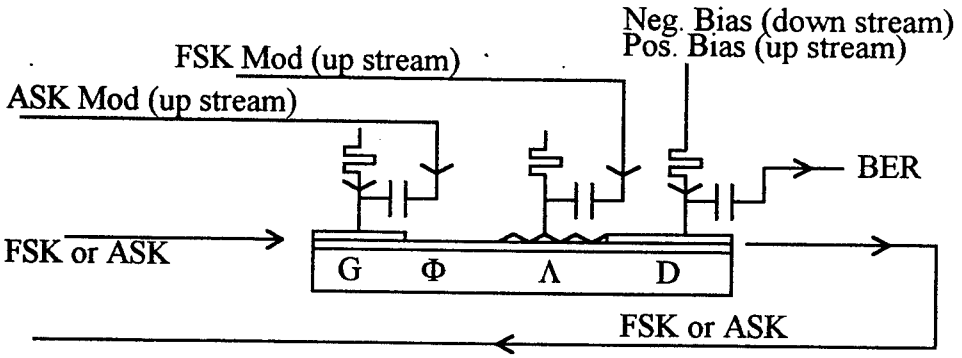


Fig. 1 Device structure and its application as a broadband terminal

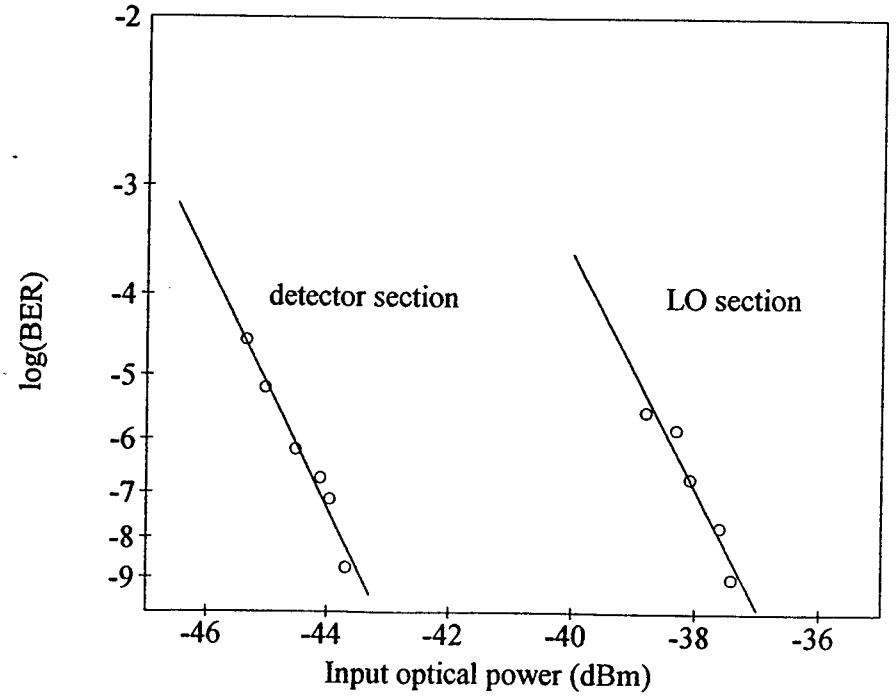


Fig. 2 Bit-error-rate measurements versus input optical power

4:45pm - 5:00pm
MC5

Broadband Fiber Optic Parametric Amplifiers and Wavelength Converters With Low-Ripple Chebyshev Gain Spectra

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Introduction. Recently we have shown that a single-pump fiber optical parametric amplifier (OPA) or wavelength converter could be operated over a 35 nm bandwidth, but with relatively poor gain flatness [1]. Here we show that two-pump OPA's operated near the fiber zero-dispersion wavelength, λ_0, can exhibit gain spectra flatter than those of EDFA's over comparable bandwidths; they can also be used as broadband wavelength converters.

Analysis. Consider strong pump fields $E_1(z)$ and $E_2(z)$ with equal powers $P_1 = P_2 = P_0/2$, and a small signal field $E_s(z)$, with respective radian frequencies ω_{p1}, ω_{p2} and ω_s, co-propagating in the z direction in a lossless fiber with nonlinear coefficient γ. Parametric gain amplifies the signal, as well as an idler $E_i(z)$ arising at $\omega_i = \omega_{p1} + \omega_{p2} - \omega_s$ [2]. The idler amplitude gain over a length L is $g_i(L) = \frac{|E_i(L)|}{|E_s(0)|} = \frac{u}{g} sinh(gL)$, where g is the parametric gain, given by $g^2 = -\frac{1}{4}[\Delta\beta^2 + 2u\Delta\beta - 3u^2]$, and $u = \gamma P_0$. $\Delta\beta$ is the linear propagation constant mismatch, i.e. $\Delta\beta = \beta_s + \beta_i - \beta_{p1} - \beta_{p2}$, where the β's are the respective propagation constants of the four waves. Maximum gain is obtained for $\Delta\beta = -u$. The gain bandwidth corresponds to g being real, i.e. to $-3u \leq \Delta\beta \leq u$. Measured in terms of $\Delta\beta$, the bandwidth is thus $4u$; what it is in terms of signal wavelength is determined by the fiber dispersion characteristics.

Let us define the central frequency as $\omega_c = \frac{(\omega_{p1}+\omega_{p2})}{2} = \frac{(\omega_s+\omega_i)}{2}$. We assume that $\Delta\beta$ can be well approximated by just the first two terms of its power series expansion in terms of $\Delta\omega_s = \omega_s - \omega_c$. Then it can be shown that

$$\Delta\beta = \beta_2[(\Delta\omega_s)^2 - (\Delta\omega_p)^2] + \frac{\beta_4}{12}[(\Delta\omega_s)^4 - (\Delta\omega_p)^4],$$

where β_k denotes the kth derivative of $\beta(\omega)$ at ω_c, and $\Delta\omega_p = \omega_{p1} - \omega_c = \frac{\omega_{p1}-\omega_{p2}}{2}$.

We can adjust ω_c and $\Delta\omega_p$ independently. Adjusting ω_c allows us to tune β_2 (while leaving β_4 essentially unchanged), because in the vicinity of ω_0 we have approximately $\beta_2(\omega_c) = \beta_3(\omega_0)(\omega_c - \omega_0)$. By adjusting $\Delta\omega_p$ we can in effect add an arbitrary bias to $\Delta\beta$.

Consider first the case where $\beta_4 \geq 0$, and $\beta_2 = 0$. In this situation, if we want to have $\Delta\beta = -u$ for $\Delta\omega_s = 0$, we need to have $\Delta\omega_p = \Delta\omega_4' = (\frac{12u}{\beta_4})^{1/4}$. The resulting gain spectrum is quite flat near $\Delta\omega_s = 0$, but it begins to drop abruptly well before reaching $\Delta\omega_p$. Let us now choose β_2 in such a way that $\Delta\beta$ oscillates symmetrically about the optimum value, $-u$, always reaching the same maximum and minimum on either side. Since $\Delta\beta$ is a fourth-order polynomial in $\Delta\omega_s$, this simple behavior must correspond to a (shifted and scaled) fourth-order Chebyshev polynomial ($T_4(x) = \cos[4\arccos(x)] = 8x^4 - 8x^2 + 1$), i.e. $\Delta\beta$ must also be of the form

$$\Delta\beta = u[-1 + \rho T_4(\frac{\Delta\omega_s}{\Delta\omega_t})].$$

ρ denotes the amplitude of the ripple in $\frac{\Delta\beta}{u}$. $\Delta\omega_t$ represents the range of $\Delta\omega_s$ (to one side of 0 only) over which the ripple remains between the Chebyshev extrema; we use it as a measure of the bandwidth of the OPA. Identifying these two forms of $\Delta\beta$ leads to

$$\Delta\omega_t = 2\Delta\omega_p \left[1 - \sqrt{\frac{1}{2}(1 + (\frac{\Delta\omega_4'}{\Delta\omega_p})^4)}\right]^{1/2} \qquad \text{and} \qquad \rho = \frac{1}{8}(\frac{\Delta\omega_t}{\Delta\omega_4'})^4.$$

As $\Delta\omega_p$ ranges from $\Delta\omega_4'$ to $2^{3/4}\Delta\omega_4'$, $\Delta\omega_t$ ranges from 0 to $\Delta\omega_p$, and ρ ranges from 0 to 1. There is a tradeoff between amplifier bandwidth and gain ripple. For small ρ, we find that

$$\frac{g}{u} = [1 - \frac{\rho^2}{4}(T_4)^2]^{1/2} = [1 - \frac{\rho^2}{8}(1 + T_8)]^{1/2} \simeq 1 - \frac{\rho^2}{16}(1 + T_8).$$

Thus we find that the ripple amplitude of g/u is $\frac{\rho^2}{16}$. As an example, a ripple amplitude for $\Delta\beta/u$ of the order of 10%, which is not very low, leads to a riple amplitude for g/u of less than 10^{-3}, which is very small. Fig. 1 shows typical graphs for $\Delta\beta/u$ and g^2/u^2 versus $\Delta\omega_s/\Delta\omega_t$, exhibiting the typical Chebyshev polynomial behavior.

Consider a dispersion-shifted fiber (DSF), operated near 1.55 μm, for which we measured $\beta_4 = 2.5 \cdot 10^{-55}$ $m^{-1}s^4$ [1]. If we assume that $\gamma = 2 \cdot 10^{-3}$ $m^{-1}W^{-1}$ and $P_0 = 7$ W, we obtain $u = 1.4 \cdot 10^{-2}$ m^{-1}. The maximum bandwidth achievable is $1.68\Delta\lambda_4' = 61.4$ nm. These numbers are quite respectable, in fact exceeding the full EDFA bandwidth. If we choose $\Delta\lambda_t = 45$ nm, we have $\rho = 29\%$; the corresponding β_2 is $-2.5 \cdot 10^{-29}$ $m^{-1}s^2$ which can easily be obtained by tuning λ_c. If we use a 200 m long fiber, we find that the OPA then has gain of about 18 dB, with peak-to-peak uniformity of better than 0.2 dB over the 45 nm bandwidth.

Discussion. The preceding analysis assumed that all dispersion terms higher than the fourth could be neglected in the region of interest. We have performed numerical simulations to test the influence of these other terms. In the same conditions as for the preceding 18 dB amplifier, we have found that β_6 of the order of 10^{-81} $m^{-1}s^4$ (with either sign) was needed to double the ripple. We used as a comparison values obtained for bulk silica from Sellmeier's equation. We found these to be at least two orders of magnitude lower than the above value, for wavelengths ranging from 1.2 μm to 1.6 μm. It thus seems unlikely that silica-based fibers would have a β_6 capable of significantly affecting the design based on T_4.

Even with ρ of the order of 30% we can still have excellent performance. With ρ in this range, variations in P_0 of a few percent will not cause severe degradation; such power stability should be easy to achieve by means of feedback control. Similar changes in β_2 would also be tolerable. Since β_2 is determined by adjusting the pump frequencies, maintaining β_2 reduces to the problem of controlling the laser frequencies. The fact the λ_0 varies with position and temperature in typical communication fibers will pose practical challenges; using highly nonlinear fibers would help reduce the length, and could thus alleviate these problems.

Summary. We have shown that the propagation constant mismatch $\Delta\beta$ for a 2-pump fiber OPA can be well approximated by a fourth-order Chebyshev polynomial, by adjusting ω_c near ω_0, and the pump spacing. Very low gain ripple can be obtained over tens of nanometers. This level of performance is not available with any other type of optical amplifier. It could make fiber OPA's and related wavelength converters attractive when multiple stages are required.

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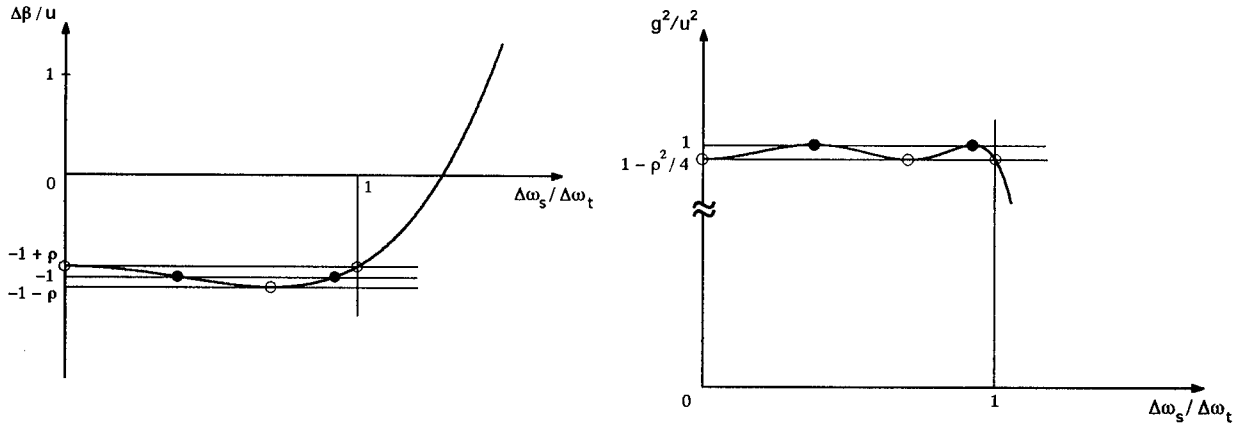


Fig.1. Graphs of $\Delta\beta/u$ and g^2/u^2, for $\rho = 0.1$. Note the expanded vertical scale for the graph of g^2/u^2.

Tuesday, August 6, 1996

SESSIONS:

TuA: Broadband Optical Access

TuB: Wave Division Network Architecture

8:30am - 9:00am (Invited)
TuA1

Broadband Access Networks - Whatever Happened to Fiber-to-the-Home?

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Although both technical feasibility and efficacy of fiber-to-the-home (FTTH) systems for delivering advanced, broadband services were established in dozens of trials in Europe, Japan, and North America in the 1980s, the cost of simply replacing copper conductors — one-for-one — with fiber proved too expensive. This was true even when allowing for high-volume production: as would be expected, the trial systems were *very* expensive. Major contributors were the dedicated optical components and high-speed electronics at each end of the fiber, not to mention the fiber itself, which at the time was more costly than either copper pairs or coax. Power dissipation of the customer's terminal equipment was high, making inexpensive standby powering difficult.

Fiber-to-the-curb (FTTC) and other approaches appeared on the scene to resolve these problems by bringing fiber *partway* to the home, then, at low power consumption, converting optical signals to electrical at enclosures serving multiple customers (thus sharing costs). The final connection to each customer was by metallic media. Cost-sharing alternatives such as FTTC were quite effective, especially in North America where attention precipitously shifted away from FTTH shortly after 1989 and somewhat later elsewhere. Japan, and to a lesser extent Europe, retained a research focus on FTTH (and fiber-to-the-building, FTTB), leading to continued progress in areas impacting costs. Two key advances have been in passive optical networks (PONs) and "loop" lasers. These, along with cost reductions in fiber, fiber components, and electronics for other applications, point to much lower costs (and prices) for FTTH than commonly believed. The bottom line is that FTTH is alive, well (or rapidly getting better), and should be an important factor in the nearer rather than longer term.

PONs offer numerous advantages for fiber loop deployment, but the most important is having a topology that shares the costs of the network-end equipment and usually most of the fiber among, typically, 16 to 32 subscribers.[1][2] A PON employs a 1:N passive optical splitter somewhere between the network facilities (e.g., switch, headend) and the residence. If the split is placed very near the customer, the topology resembles FTTC. The splitters themselves can be fused-fiber, silica-on-silicon, or $LiNbO_3$ planar components, or new polymer waveguide devices.

Loop lasers, unlike high-performance devices for transmission, achieved initial economies in the 1980s by using Fabry-Perot chips in low-cost, alignment-tolerant packages and eliminating thermoelectric cooling. Performance was adequate for short-distance (few km) applications and prices were as low as $50 in quantity. During the last three years, there has been remarkable new progress. At the chip level, SL-MQW lasers can be engineered to have low thresholds over a wide temperature range, and beam shaping (e.g., adiabatic beam expanders) has been integrated into several designs.[3][4][5][6]

Better matching of the fiber and laser mode-field diameters results in high (50%) yet alignment-tolerant coupling efficiencies. Furthermore, even over temperature ranges as wide as -40°C to +85°C, these lasers can be operated without bias current (eliminating the need for internal power monitoring and feedback control, thereby reducing costs)[7] as well as demonstrate high reliability (> 10^5 hours MTTF @ 60°C, 10 mW).[8] Most recently, all-plastic packaging and all-passive alignment have also been demonstrated, again contributing to low costs.[9][10]

In addition, advances in analog lasers [11], fiber amplifiers, analog receivers, and planar hybrid WDM modules[12] suggest that an overlay of analog television channels may be achievable and economical, especially if the number of analog channels is kept low. This offers an option for

smoothly transitioning from analog to fully digital television delivery, while the cost of digital converters continues to fall. Progress in MPEG compression[13] of video also assists FTTH in that numerous digital channels can be "broadcast" to all customers over a reasonable digital bandwidth. The MPEG-2 standard currently permits "off-air" quality video to be transmitted at 3 to 4 Mbit/s, and "studio quality" is attainable at 4 to 6 Mbit/s.

Providing reliable, low-cost electrical power to the O/E interface at each home can be accomplished either by applying established FTTC powering options, or by designing energy-efficient systems and powering locally from the residence. The latter, which is most cost-effective, will be substantially helped by new battery technologies which promise long life and low cost.[14][15]

By combining the latest technologies and architectures, FTTH can come close to or even match the installed cost of other alternatives depending on the application. Additionally, FTTH offers operational economies during its installed life (e.g., related to powering, maintenance, provisioning, and upgrading), making it ultimately the most economical means to deliver broadband services. Clearly, FTTH should be considered for an important, near-term role in many broadband infrastructures.

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Hybrid WDM Digital Trunking System for Both HFC and FTTC Access Networks

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Wavelength-division-multiplexed (WDM) systems can utilize the vast bandwidth provided by single-mode fiber (SMF) [1]-[4]. Most WDM systems distribute homogeneous traffic, for example, all channels transmit OC-48 (2.5 Gb/s) signal [1] or OC-192 (10 Gb/s) signal [2]. Hybrid WDM systems have been proposed for transmitting both FM-TV and 622 Mb/s baseband digital video [4], AM-TV and uncompressed (PCM) video [5], or AM-TV and 622 Mb/s B-ISDN signal [6] (WDM in 1310 nm and 1550 nm). Here, we demonstrate a hybrid WDM system that can distribute QAM-modulated multichannel digital video, baseband PCM video signal [7], and SONET OC-192 signal that can serve both hybrid fiber/coax (HFC) and fiber-to-the-curb (FTTC) broadband access networks.

Figs. 1(a) and 2(b) show the schematic diagram of a digital trunking system using hybrid WDM technology demonstrated for spans of 50 km and 100 km over standard SMF, respectively. The wavelength of the externally modulated QAM-SCM channel and the external modulated 10 Gb/s SONET channel are 1552 and 1548.5 nm, respectively. The wavelength of directly modulated 2.5 Gb/s PCM-video channels are 1544 and 1546 nm. The wavelength separation of the 10-Gb/s to 2.5-Gb/s channel is larger to reduce the crosstalk due to insufficient rejection of optical filter in the receiver. For the 50 km system, both the QAM-SCM channel and the 10 Gb/s channel are first amplified using erbium-doped fiber amplifiers (EDFAs). The transmitted power of the QAM-SCM channel is 12 dBm and that of the 10 Gb/s channel is 7 dBm. The optical power of the 10 Gb/s channel is lower to reduce the crosstalk to the 2.5 Gb/s channel at 1546 nm. The transmitted power of the two 2.5 Gb/s channels is -1 dBm. Because of higher required optical power at the receiver, the transmitted power of both QAM-SCM and 10 Gb/s channels are 8 dB and 13 dB higher than that of the 2.5 Gb/s channels. The loss of the WDM multiplexer is about 7 dB and the loss of 50 km of SMF is 11 dB.

For 100 km of transmission in standard SMF, the 10 Gb/s SONET channel is limited by fiber dispersion [8]. In Fig. 2(b), the transmitted power is first amplified through an EDFA, followed by 15 km of dispersion compensation fiber (DCF), another EDFA to boost the optical power, and an optical filter with FWHM bandwidth of 1.5 nm to reduce amplified spontaneous emission (ASE) noise. The DCF has dispersion of -45 ps/km/nm and the standard SMF has dispersion of 17 ps/km/nm.

In practice, a wavelength demultiplexer needs to be employed at the receiver. For this demonstration, an optical filter with a FWHM bandwidth of 0.25 nm is employed to separate each channel for the testing. The optical filter induces crosstalk to the system, especially for the two 2.5 Gb/s channels that have lower optical power. For the QAM-SCM channel, the crosstalk from other channels is less than -30 dB. For the 10 Gb/s channel, the crosstalk from other channels is less than -13 dB. For the 2.5 Gb/s channel at 1546 nm, the crosstalk from other channels is less than -10 dB. For the 2.5 Gb/s channel at 1544 nm, the crosstalk from other channels is less than -20 dB.

Fig. 3 shows the BER as a function of received optical power for both 50 km and 100 km of fiber span. Fig. 3(a) shows the sensitivity of QAM-SCM channel with 84 64-QAM subchannels. The first 80 subchannels are single-frequency tones to simulate QAM subcarrier and are assigned according to NTSC frequency allocation from 53 MHz to 550 MHz to take advantage of tuners designed for NTSC frequencies. The last four subchannels carry PRBS 64-QAM traffic with center frequencies at 553.25, 613.50, 660.75, and 701 MHz. Each channel occupies 6 MHz of bandwidth and transmits at a data rate of 30 Mb/s. All tones and QAM channels have a modulation index of 3%. Fig. 3(a) shows that the sensitivity of 100 km transmission is about 1.5 dB worse than that of 50 km transmission for BER of 10^{-9}. The 1.5 dB power penalty may be induced by the nonlinearity of the fiber and the ASE noise of the in-line amplifier.

Fig. 3(b) shows the BER of the 10 Gb/s SONET OC-192 signal at wavelength of 1548.5 nm. Transmission over 50 km and 100 km shows a sensitivity difference of less than 0.2 dB. The sensitivity at a BER of 10^{-9} is -18.5 dBm.

Fig. 3(c) shows the BER of the two 2.5 Gb/s channels at wavelengths of 1544 nm and 1546 nm, respectively. The difference between 50 km and 100 km transmission is negligeable. The optical channel at 1544 nm yields a sensitivity of -30.2 dBm while the channel at wavelength of 1546 nm yields a sensitivity of -29.2 dB. The 1 dB difference is attributed to the crosstalk from other channels, mainly from the 10 Gb/s SONET channel because of its larger optical power. While the 1544-nm channel has crosstalk less than -20 dB, the 1546-nm channel see a larger crosstalk of about -10 dB.

In conclusion, a hybrid WDM system is demonstrated for digital trunking applications. Supporting heterogeneous traffics, such a hybrid WDM trunking system can serve both HFC and FTTC broadband access networks. The system can carry a multichannel 64-QAM SCM signal, a 10-Gb/s OC-192 signal, and 2.5 Gb/s PCM video signals.

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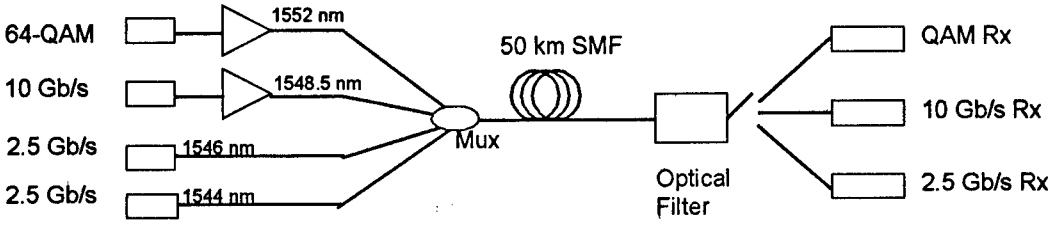
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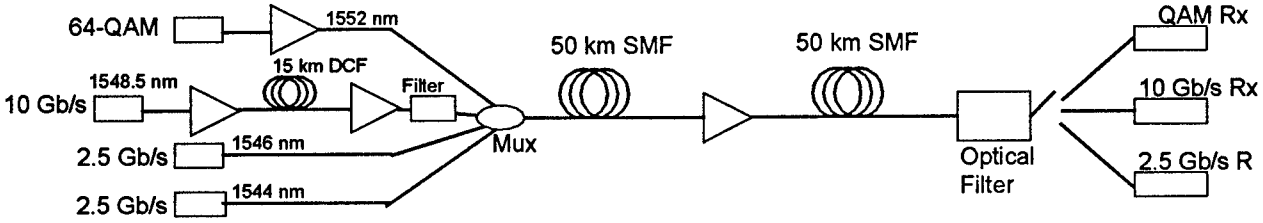
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(a) 50 km



(b) 100 km

Fig. 1. Demonstration of hybrid WDM system to support QAM subcarrier multiplexing, 10 Gb/s SONET, and 2 × 2.5 Gb/s PCM video for a span of (a) 50 km and (b) 100 km. (DCF: Dispersion compensation fiber, SMF: single mode fiber, ▷ : erbium doped fiber amplifier.)

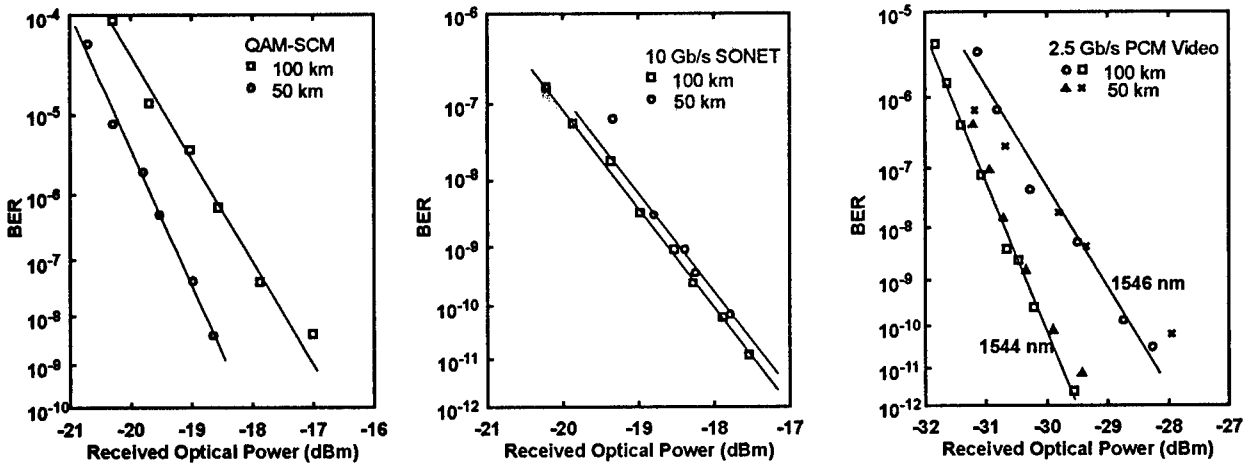


Fig. 2. The dependency of BER on received optical power of (a) QAM subcarrier multiplexing, (b) 10 Gb/s SONET, and (c) 2.5 Gb/s PCM video signal.

Optical Networking for Local Access

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SUMMARY

Passive Optical Networks (PONs) have been proposed as a telecommunications distribution method for the local loop, both in power-dividing broadcast [1] and in Wavelength-Division Multiplexing [2] forms. Implicit advantages of these PONs are the limitless bandwidth of the optical fiber connecting the Central Office or Headend to the subscriber and the opportunities for optical network connections. However, the promise of broadband optical networking in access networks remains unrealized, nearly a decade after these proposals.

The most common broadband service today is entertainment video, primarily delivered over coaxial cable in CATV systems. In hybrid fiber/coax networks that have been proposed recently, the expense of high quality fiber optic links capable of carrying AM-VSB television channels has necessitated extensive sharing (up to 500 subscribers on a coax tree and branch network) of a single optical link. Consequently, the potential of this architecture for broadband optical networking is limited to a shared coaxial bus by the economics of television delivery over optical links. On the other hand, conventional PON proposals, in order to share optical plant, are restricted to optical bus architectures, whose effective bandwidth scales inversely with the square of the number of subscribers. Thus, the potential of this approach is limited by the initial choice of the optical bus. In both cases, the drive for low cost access solutions results in a sub-optimal network for future broadband services.

We review recent research [3-8] on representative optical architectures that are intended to be cost-effective at installation and yet can be upgraded to very high levels of performance in the future. Recognizing that there are many dimensions to network opportunities, we examine several recent optical network architectures and their abilities to: provide low cost entry for low level services; utilize components that are in or near commercial viability; deliver non-segmented bandwidth; deliver broadcast entertainment video at low cost; provide operations and maintenance advantages for the netork administrator cost effectively; permit individual, subscriber supported

service upgrades; permit immediate high bit rate upgrades; and provide a platform that is resistant to competitive bypass.

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AM/OFDM versus AM/QAM for Mixed Analog/Digital Subcarrier Multiplexed Lightwave Transmission

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Introduction

Hybrid multichannel AM/QAM subcarrier multiplexed (SCM) lightwave systems are attractive for mixed analog/digital video-data transport over hybrid fiber/coax (HFC) networks. It is well known, however, that the "clipping" impulse noise generated by the laser diode threshold in a multichannel SCM system can significantly degrades the performance of the QAM signals [1]-[3]. Especially, for higher order QAM, bit-error-rate (BER) "floor" has been observed [1]-[2]. Furthermore, the performance degradation limits the total system capacity (the total number of channels that can be accommodated) [3].

As an alternative to QAM, OFDM (orthogonal frequency division multiplexing) has also been attractive for digital video transmission due to its advantages against multipath and impulse noise [4]. OFDM involves a multiplexing of multiple low data rate carriers, each being independently modulated with a conventional QAM. Since OFDM is built upon a number of conventional QAM subchannels, it would be expected that an OFDM-QAM signal in a mixed AM/OFDM lightwave system may also suffer the clipping degradation. However, as will be shown here, because of the concurrent transmission of many narrowband carriers in OFDM, the symbol duration of an OFDM signal is much larger than that of the single carrier system. While an impulse noise may completely destroy one or several symbols of a single carrier QAM, it may only affect a small fraction of an OFDM symbol. Hence, OFDM has an advantage over QAM against impulse noise. Our results herein presented indeed support the claims. In particular, we show that significant BER improvements can be obtained using AM/OFDM vis-à-vis AM/QAM, when corrupted by both the clipping-impulse and Gaussian noise. It is shown that the clipping effect on the BER of an OFDM signal can be negligible for a large range of laser optical modulation depths, and therefore, virtually no limit is imposed on the channel capacity. It is further shown that OFDM introduces little effect on the analog AM channels, as opposed to use of QAM systems.

BER Comparisons for AM/OFDM and AM/QAM Lightwave Systems

The analytic model of an OFDM signal embedded in the clipping and Gaussian noise is illustrated in Fig. 1, where the OFDM system assumes FFT configuration [4]. Since the OFDM signal can be modeled as Gaussian distributed [4], the same statistical properties of the clipping noise in an AM/OFDM SCM system as that of [3] can be applied. Thus, following the same approach as given in [3], the BER of OFDM can be obtained by

$$p_e = \frac{1 - 1/\sqrt{M}}{\log_2 M}\left[\operatorname{erfc}(\Delta/\sqrt{2}) - \frac{5}{2\gamma}\left(\frac{1}{1+G}\right)^2\Phi_3(\Delta) - \frac{1}{\gamma^2}\left(\frac{1}{1+G}\right)^3\left(\frac{35}{3}\Phi_5(\Delta) + \frac{25}{16}\Phi_7(\Delta)\right)\right] \quad (1)$$

where M is the QAM level, γ is the clipping index per OFDM symbol interval, G is the variance ratio of the Gaussian noise to the clipping noise, i.e., $G=\sigma_g^2/\sigma_c^2$, $\Delta = \sqrt{[3\cdot SNR/(M-1)]}$, SNR being the total signal to noise ratio, and $\Phi_k(x) = d^k[\exp(-x^2/2)/\sqrt{(2\pi)}]/dx^k$. The variance of the clipping noise is given by [3] $\sigma_c^2 = 4\bar{\tau}\,(\pi)^{-3/2}\mu^5\exp(-1/\mu^2)P_o/3$, where $\bar{\tau}$ is the average impulse duration, μ is the total RMS optical modulation index (OMI) of the hybrid analog/digital signal, and P_o is the received signal power. From (1), it follows that as $\gamma \rightarrow \infty$, the OFDM BER p_e approaches the Gaussian BER model. Similar BER expression for QAM is given in [3].

The BER performances of AM/OFDM and AM/QAM lightwave systems under various conditions are shown in Figs. 2-5. In all cases, 70 AM channels are used. The OMI used is the per channel OMI. For comparison purpose, each OFDM subchannel uses the same level of QAM as that of the conventional single carrier QAM. The Figs.2-5 clearly indicate the improvements obtained when OFDM is used instead of conventional QAM. The improvements include lower BER, larger operating OMI range (or equivalently higher capacity), higher tolerance to AM interference, and lower interference onto AM. Other results, including the comparisons on the employment of error correction coding, will also be presented.

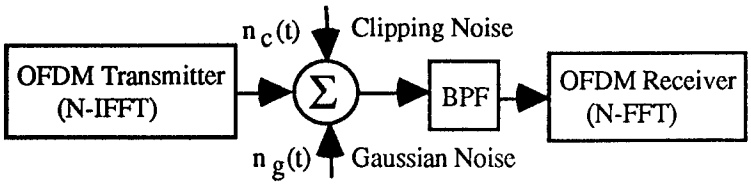


Fig. 1 Analytic Model of OFDM in the Presence of Clipping and Gaussian Noise.

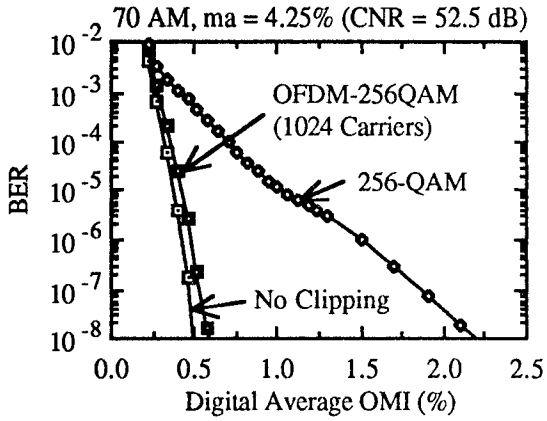


Fig. 2 BERs of Single Digital Channel.

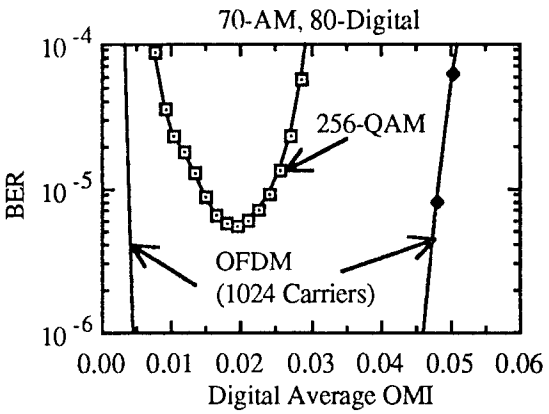


Fig. 3 BERs of Multple Digital Channels

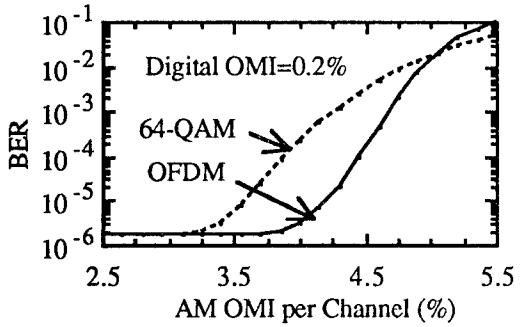


Fig. 4 BER of Digital Signal vs. OMI of AM.

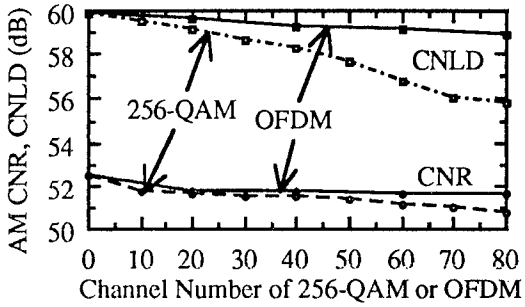


Fig. 5 Effect of Digital Channel on AM.

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Effects of Wavelength Routing and Selection Algorithms on Wavelength Conversion Gain in WDM Optical Networks [1]

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Abstract

We propose two k shortest path algorithms for selecting the route-wavelength pair in WDM networks with and without wavelength converters with orders of magnitude larger conversion gains as compared to conventional routing. We state a conclusion on the use of wavelength converters in long-distance networks.

1 Introduction

In this paper, we address the problem of quantifying the benefits of wavelength conversion for different routing and wavelength selection algorithms. We use two metrics to measure the merits of wavelength conversion. The utilization gain G_u is the ratio of maximum offered loads for wavelength interchangeable (WI) and wavelength selective (WS) networks for achieving a given blocking probability. The blocking probability gain G_p is the ratio of blocking probabilities for WS and WI for a given traffic load.

The model presented in [1] and developed later in [2, 3] provides equations which can be used to study the qualitative behavior of G_u as a function of the network topology, number of wavelengths, and routing algorithm for the random wavelength selection algorithm. The utilization gain is upper bounded as:

$$G_u \leq \left(\frac{H}{L}\right)^{\frac{1}{M}}, \tag{1}$$

where H is the average number of links per path, L is the average number of links shared by two link sharing paths (interference length), and M is the number of fibers per link [2].

2 Maximum H/L Routing (MHLR)

The shortest path routing algorithm does not produce large G_u and G_p since it decreases H and increases L. As suggested by (1), a routing algorithm that maximizes H/L may maximize G_u. Obviously, an algorithm that maximizes H only also generates a large G_u, but very high blocking probabilities achieved by this technique can be unacceptable. We thus restrict the path set to the set of k shortest paths between all node pairs. Shortest path routing is equivalent to $k = 1$. For WS, the wavelength with the smallest index number is selected among available wavelengths (First-Fit rule).

In Figure 1, the blocking probabilities for WS and WI with $k = 1$ and 7 are plotted versus the traffic load. The performance of WS deteriorates as k increases since longer paths create more wavelength conflicts. On the other hand, the blocking probability for WI decreases at low utilization since maximizing H/L over a larger path set distributes the traffic over less used parts of the network. As the utilization increases, the blocking probability for WI also worsens with increasing k since extra bandwidth used by longer paths become very critical.

3 Least Loaded Routing (LLR)

The path and wavelength selection technique for the LLR algorithm is as follows: Let $U_l = \sum_{j=1}^{K} A_{lj}$ be the total number of wavelengths utilized on link l, where A_{lj} is the number of fibers for which wavelength j is utilized. The path set contains the set of k shortest paths between all node pairs. The least loaded path

[1]Work supported by DARPA under the Multiwavelength Optical Networking (MONET) consortium of Lucent Technologies, Bellcore, AT&T, Bell Atlantic, Bell South, Pacific Bell, and Southwestern Bell.

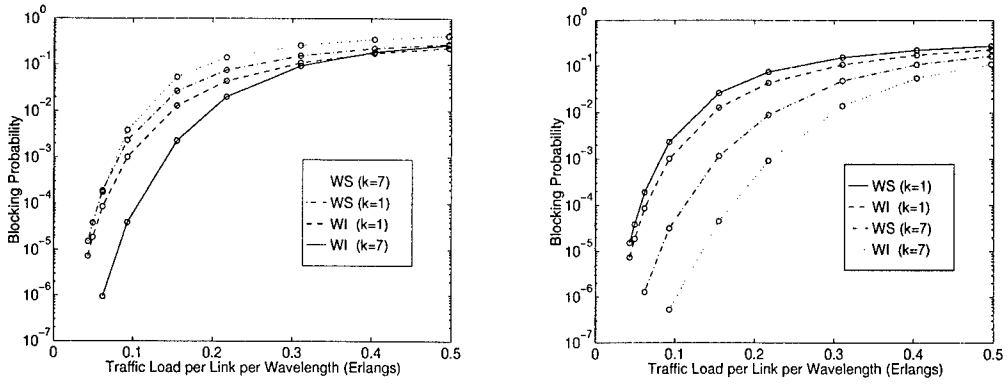


Figure 1: Blocking probability versus network load for $k = 1, 7$ with MHLR (left) and LLR (right).

within the path set is selected according to the following criteria: For each connection request with WI, LLR chooses the path p that maximizes

$$\max_{p} \min_{l \in p} K M_l - U_l \tag{2}$$

and with WS LLR chooses the path p and wavelength j that maximize

$$\max_{p,j} \min_{l \in p} M_l - A_{lj}. \tag{3}$$

In Figure 1, the blocking probabilities for WS and WI with $k = 1$ and 7 are plotted versus the traffic load with a single fiber network. As k increases, the blocking probability for both WS and WI decreases, while the improvement gets smaller with k.

4 Conclusions

Shortest path routing algorithms used in conjunction with a packing wavelength selection algorithm, such as First-Fit, produces a small conversion gain in our simulations with a 30-node, 47-link (each link has a single fiber) network: $G_p < 2$ and $G_u < 1.2$. On the other hand, the MHLR algorithm which maximizes H/L achieves much larger gains: $G_p < 200$ and $G_u < 2$, while part of these increases are obtained at the expense of worsening the performance of WS. The LLR algorithm tries to select the path and wavelength with the minimum load, and achieves much better blocking performances for both WS and WI. Conversion gains for LLR are also comparable to the MHLR algorithm: $G_p < 100$ and $G_u < 1.7$. Although these conversion gain figures seem to favor WI networks over WS networks, these gains are obtained at very low loads which are not likely to be the case for future optical networks. Finally, as the traffic demand increases, links will have multiple fibers, and G_u decreases exponentially with the number of fibers per link, substantially reducing the gain by WI: $G_p < 30$ and $G_u < 1.15$.

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Wavelength Reservation Under Distributed Control[1]

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1 Introduction

Distributed control is a key to feasible implementation of wide-area wavelength-routing networks. It also requires re-examination of two issues. One is how wavelengths are *reserved* (as opposed to *assigned* under centralized control) and the other is how effective wavelength conversion can be.

In this study, we design and evaluate efficient *wavelength reservation* policies that specifically address the *signaling overhead* in distributed control. Our discussions will focus on the application of these policies to two representative approaches called *Path Multiplexing* (PM) and *Link Multiplexing* (LM) applicable to either TDM or WDM networks [1]. In WDM networks, PM requires *wavelength-continuity* paths while LM does not but requires *wavelength conversion* at each switching node *instead.*

2 Distributed Control

Existing distributed circuit-switching schemes for non-optical networks may be applicable to LM at their best, but not to PM [2]. On the other hand, centralized control was assumed (or implied) by the wavelength assignment schemes proposed so far, e.g. in [3]. Most of the studies comparing LM and PM in terms of blocking probability assumed (or implied) centralized control and ignored signaling overhead.

Under distributed control, signaling is done by exchanging control packets between the nodes (or routers). These control packets are processed at each node based on local information, thus eliminating the potential performance bottleneck caused by the central controller, and increasing the reliability of the system. However, signaling overhead resulted from processing and exchanging control packets becomes an important factor. Distributed control also leads to *simultaneous contention* for resources (e.g. wavelengths) among several control packets. These factors render the existing centralized schemes and the results obtained under these schemes on the effect of wavelength conversion unappealing to distributed control environments.

3 Wavelength Reservation

A basic distributed scheme is as follows. A reservation packet (RESV) is sent by a source node to its destination node. It visits each intermediate node and reserves a *suitable* wavelength available on each link along the way[2]. Upon receiving RESV, the destination node sends a positive acknowledgement (ACK) back to the source following the reverse of the route that RESV took, triggering switch reconfigurations needed to establish the connection. The source will send a release packet (RELS) to the destination to tear down the connection.

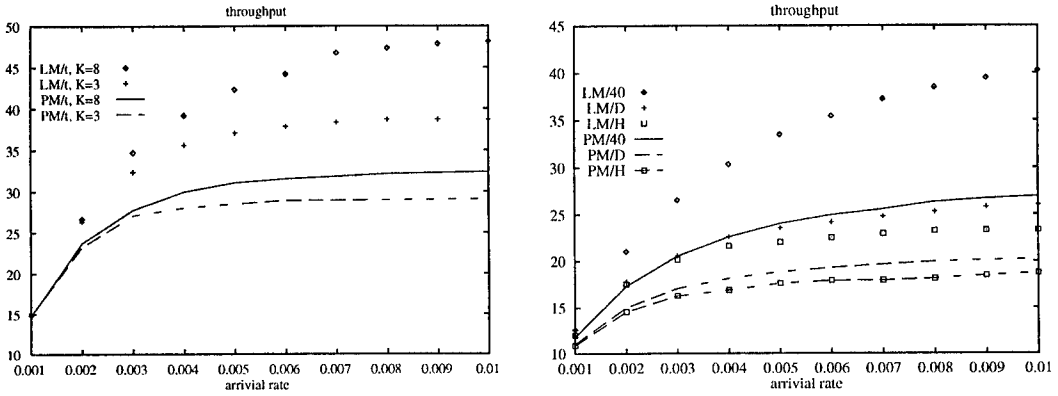
If no suitable wavelength is available for reservation at an intermediate node, two policies may be considered. One is called "*Drop*" under which an negative acknowledgement (NACK) is sent back to the source immediately, releasing the (wavelengths on the) partially reserved path. This (or an analogous) policy is adopted by existing centralized schemes, along with the assumption that a blocked request never comes back. Often, a request is resubmitted until it is satisfied, in which case, the second policy called "*Hold*" may be adopted in order not to incur the signaling overhead in releasing a partial path and then reserving it again. Under the *Hold* policy, a blocked RESV is buffered at the intermediate node until either a suitable wavelength is available, in which case it proceeds, or a timer expires, in which case the partially reserved path is released. *Deadlock* may occur due to limited buffer space at each node as in worm-hole routed networks [4].

[1]This research is supported in part by NSF under contract MIP-9409864

[2]In LM, any wavelength is suitable but in PM, only the same wavelength as the one reserved in the previous links is.

4 Performance Evaluation

We have implemented the following distributed schemes: LM and PM employing Drop (LM/D and PM/D), LM and PM employing Hold without time-out (LM/H and PM/H), and LM and PM with a time-out value $0 < t < \infty$ (LM/t and PM/t). Some of the simulation results for an 8×8 mesh are shown below. A Poisson arrival of the connection requests and an exponential distribution of the connection durations are assumed. Note that it is more appropriate to compare various schemes, and to contrast LM and PM, based on *throughput* than blocking probability under distributed control.



We have found that the performance advantage that LM gains over PM increases with the number of wavelengths (K). In addition, this advantage is significant, more so than under centralized control, such that the use of wavelength converters in LM may be justified. We have also found that the Hold schemes with a time-out value are better than the Drop schemes, which in turn are better than the Hold schemes without time-out. However, the time-out value, t, has relatively insignificant effect on the performance, and can assume any reasonable value (e.g., the round-trip propagation delay in the network).

5 Concluding Remarks

The wavelength reservation schemes and the effectiveness of wavelength conversion need to be re-examined under distributed control. Applying the *Drop* and *Hold* policies to LM and PM is just one way to address the signaling overhead. Another way currently under evaluation is *parallel* reservation, which is unique to PM under distributed control [5]. Its main idea is to temporarily reserve *all* suitable wavelengths on a link instead of just one at a time as in centralized schemes. This way, it is likely that a connection can be established on a common wavelength without incurring signaling overhead as many times as in its *sequential* counterpart.

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Wavelength conversion in future WDM optical transport networks

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Abstract

This paper describes the advantages introduced by wavelength conversion in the design, implementation and management of future WDM optical networks and nodes.

Introduction

The introduction of Wavelength-Division-Multiplexing (WDM) in the telecommunication networks is now becoming a world-wide concern. WDM is envisioned to be implemented soon as a flexible and straightforward way to enhance network traffic capacity [1] by using more efficiently and cost effectively the available bandwidth of existing optical fibre transmission link infrastructure. In a medium term, a WDM optical layer [2-3] could be the enabling factor to build high capacity transport networks, allowing flexible and cost-effective routing of high-speed highways directly in the wavelength domain. Different strategies can be adopted to implement WDM all-optical transport networks based either on wavelength routing or on wavelength translation. In this paper, we will describe the routing and wavelength assignment process in a WDM network and then we will demonstrate the major advantages introduced by wavelength conversion, mainly regarding the dimensioning aspects but also including considerations on the physical and management issues.

Dimensioning of the WDM optical layer

The main goal is to dimension optical nodes and links in terms of needed optical channels according to the network topology, traffic matrix and protection/restoration schemes. The network topology is defined by the number N and the location of the optical nodes and of the number M and the location of the optical interconnection links. The traffic matrix is expressed in end-to-end connections between pairs of nodes. We define the optical channel as a WDM optical carrier in a specific fibre : therefore one optical path is characterized by one optical channel in each link used by a given end-to-end connection. In the wavelength routing scheme, an optical path is established by concatenation of optical channels using the same wavelength from end to end. In wavelength translating networks, an optical path is made by a concatenation of optical channels with possibly different wavelengths.

Two problems have to be tackled : to establish the path for each end-to-end connection (routing problem) and to allocate the transport resources to each path (resources assignment problem). The routing solution is the initial step of the resource assignment problem : therefore they are linked, but they could be resolved separately and iteratively. The routing and wavelength assignment process establishes optical paths, performing channel reservation, wavelength and fibre allocation, and comparison with constraints (physical and logical). It is an optimization process based on rerouting of optical paths according to well defined citeria (available resources, cost, ...), which translate into assignment constraints.

1 : Copenhagen
2 : Berlin
3 : Vienna
4 : Milan
5 : Paris
6 : London
7 : Amsterdam
8 : Prague
9 : Zurich
10 : Luxemburgh
11 : Brussels

- Number of major optical nodes N = 11
- Number of uni-directional links M = 50
- Number of connections C = 150 (symmetric traffic matrix)

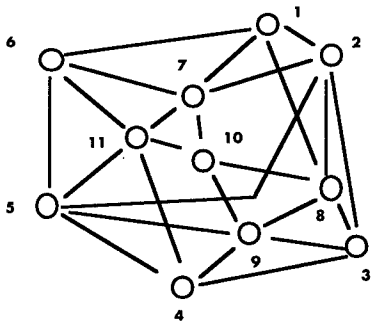


Fig. 1 - An European optical network model

Wavelength conversion within the nodes resolves blocking due to wavelength conflicts, whereas nodes/networks without wavelength conversion shift the blocking into another point of the WDM optical network layer. Indeed, wavelength conversion reduces always the number of used fibres from 10% to 30% [3], depending on the operating conditions and constraints and also the size of the used optical crossconnects. Figure 1 illustrates the core (only the major nodes) of the COST model for an European optical network [4]. Figures 2 and 3 show the mentioned results obtained on this network without path protection, for the fibre length and the node size, respectively.In the case of 4 wavelengths per fibre, the total network fibre length is reduced by 5280 km (13.5%) whereas the reduction of the number of used fibres is 11.5%. The same benefits exist for the node size, expressed in optical ports (number of I/O fibres x number of wavelengths per fibre). For instance, assuming a maximum node size of 32 ports, only two nodes (Luxemburgh and Brussels) cannot fit in this limit when using wavelength conversion, whereas the nodes are six (Berlin, Amsterdam, Prague, Zurich, Luxemburgh and Brussels) in the case without wavelength conversion. Indeed, these differences are amplified when also resources are reserved to implement protection schemes (at the path or link level). Figure 4 shows the total length of fibre with path protection : the difference is much higher (36%) even for 16 wavelengths per fibre. Finally, it is worth noting that better results can be obtained with low-meshed topologies.

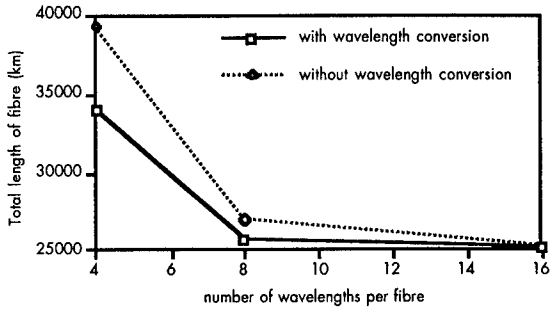


Fig. 2 - Total length of fibres in the network (without path protection)

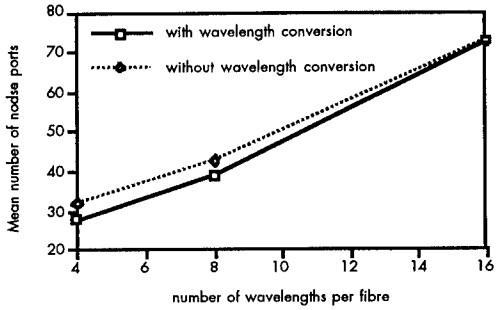


Fig. 3 - Mean number of optical node ports (without path protection)

Discussion

Wavelength conversion would give the following advantages :

- Given the limited number of wavelengths that can be physically used, due to the imposed optical amplification window (1530-1560 nm), and minimum channel spacing, the wavelength will have to be reused to increase the network capacity beyond this limit. In that case, wavelength conversion will be welcome to eliminate efficiently wavelength blocking situations and simplify path allocation, as shown in the previous section. This translates into both significant savings of fibres and reduction of nodes size and implementation of a more flexible and upgradable network.

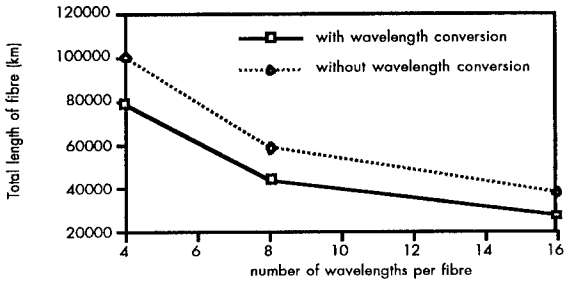


Fig. 4 - Total length of fibres in the network with path protection

- At the network management level, the planning and management aspects of a large, public network have to be extended to cover the specific properties of WDM transmission and routing resources [5]. Therefore, configuration and re-configuration of the optical network layer, especially if performed via TMN-compatible software applications, are affected by the same constraints mentioned for the dimensioning process, moreover to be performed within a maximum recovery time. In this case, wavelength conversion can simplify the channel reservation and resource allocation : as a matter of example, the related computing time is reduced by a factor of ten.

- From the transmission viewpoint, wavelength conversion allows to cope with physical limitations. When considering a network with connections spanning over some thousands kilometers, the signal degradation coming from noise accumulation, transmission impairments and crosstalk issues in the routing nodes might raise severe limitations to network extension and node cascadeability. Therefore signal regeneration will be required within every or well-identified nodes of the network. Full regeneration is currently performed by means of optoelectronic, non bit-rate transparent regenerators. Partial signal regeneration and reshaping can be accomplished by means of transparent wavelength converters : short term solution is the use of opto-electronic converters; state-of-art results indicate that in the near future all-optical wavelength converters could also perform some signal regeneration (output power regeneration, extinction ratio enhancement, signal-to-noise ratio enhancement, spectral cleaning) [6].

Conclusions

The multiple benefits of wavelength conversion in a WDM optical network layer have been described. For this reason, Alcatel is developing fully reconfigurable optical nodes [7-8] exploiting wavelength conversion to implement strictly non-blocking architectures, transparency to the transported signals and to perform signal regeneration and reshaping at multi-Gbit/s speed directly in the optical domain, thus simplifying the design, implementation and management tasks. In particular, work on all-optical wavelength conversion techniques has been initiated in the RACE ATMOS project and is currently being continued within the ACTS projects OPEN and KEOPS.

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Optimal Design of WDM Ring Networks Via Resource-Balance[1]

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1 Introduction

Performance and *cost* are two most important factors that affect the scalability of a WDM network. To achieve optimal performance with minimal cost, the resources (e.g. the number of wavelengths and tunable transceivers) in a network have to be *balanced*. That is, none of them should cause performance bottleneck while the others are underutilized. This study addresses two issues. One is to determine what is the best possible performance, and more importantly, how to achieve it with the given resources. The second is to determine which resource is insufficient, which is excessive, and how to balance them.

We illustrate the principle by focusing on the problem of establishing complete connections, also known as all-to-all personalized communications, in a WDM ring. We show that there is an optimal value of the number of wavelengths for a given number of tunable transceivers per node and vice versa. In particular, the latter does not need to exceed 12 in an arbitrarily large ring.

2 TWDM Scheduling in Rings

The complete connections (CC) in a network of N nodes consist of one connection from each node to every other $N-1$ nodes for a total of $N(N-1)$ connections. We consider a WDM ring in which two adjacent nodes are linked with a full-duplex fiber (or two simplex fibers) multiplexed with K wavelengths. Assume that each node has T fully-tunable transmitters and receivers, and is interfaced to the ring through a wavelength-routing device similar to an add-drop multiplexor [1]. A connection is established along its shortest path having $S \leq N/2$ strides (also known as hops) by using the same wavelength on each hop.

Since one *cannot* establish all the connections in CC at the same time with a limited T and K, one may schedule several *rounds* (or time slots), during each of which a subset of the required $N(N-1)$ connections is established. An optimal schedule is the one that results in best possible performance, i.e. a minimum number of rounds, for a given T and K.

3 Theoretic Lower Bound and Resource-Balance

The theoretic lower bound (TLB) on the number of rounds needed to establish CC is determined as follows. First, assuming an infinite number of wavelengths, a TLB imposed by T is $TLB(T,-) = \lceil (N-1)/T \rceil$. This is because there are $N-1$ connections originating from a node each requiring a transmitter. Second, assuming an infinite number of transceivers per node, a TLB imposed by K is $TLB(-,K) = \lceil N^2/8K \rceil$ if N is even. This is because the total number of channels required to provide the bandwidth needed to establish CC is $2 \cdot N \cdot \sum_{S=1}^{N/2-1} S + N \cdot N/2 = N^3/4$, but only $2NK$ channels are available in one round[2]. Accordingly, the TLB when both T and K are finite is $max\{TLB(T,-), TLB(-,K)\}$.

For a given T and K, it is possible that $TLB(T,-) > TLB(-,K)$. In this case, the performance bottleneck is caused by an insufficient number of transceivers while the bandwidth provided by K wavelengths is underutilized. Hence, more transceivers should be used to increase the performance (or fewer wavelengths should be used to achieve the same performance at a lower cost). Similarly, it is also possible that $TLB(-,K) > TLB(T,-)$, in which case, the bandwidth is the performance bottleneck while the transceivers are underutilized, necessitating resource-balance to achieve better cost-performance ratio.

The above theoretical analysis can guide not only the search for an optimal scheduling algorithm (as to be discussed next), but also the design of cost-effective systems. For example, since the performance is limited by bandwidth when $T > 8K(N-1)/N^2$, and it is reasonable to assume $K \leq N$, it is likely that no more than 8 transceivers per node is necessary with an ideal scheduling.

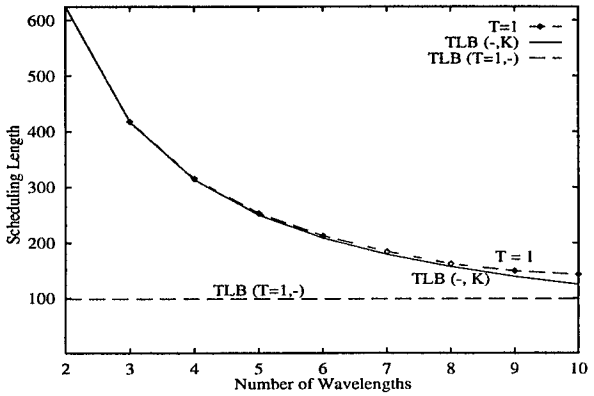
[1] This research is supported in part by a grant from NSF under contract MIP-9409864.

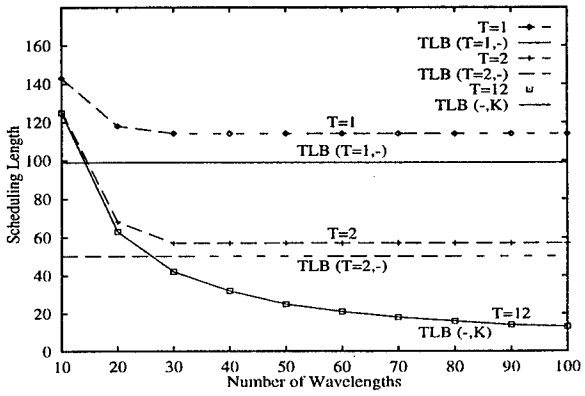
[2] when N is odd, $TLB(-,K) = \lceil (N^2-1)/8K \rceil$ for a similar reason.

4 Optimal Scheduling Based on CADS

The idea of the proposed *Complementary Assembly with Dual Strides* (CADS) method is to establish up to four connections having stride S and its complementary stride $N/2-S$, $(0 \leq S \leq N/4)$[3], which form a *circle* of N links. For example, if $K = 1$ (i.e. no wavelength multiplexing), the following four connections $(0, S)$, $(S, N/2)$, $(N/2, N/2+S)$ and $(N/2+S, 0)$ form a circle and are established in one round. It has been found that CADS guarantees an optimal schedule, *but* a naive method that tries to "pack" in one round as many connections having the *same* stride first as possible does not. Specifically, when $K = 1$, the performance is limited by the bandwidth, and the TLB can be achieved with $T = 1$ transceiver per node based on CADS scheduling.

When $K > 1$, a round can accommodate several circles which may be *heterogeneous*. That is, one circle can be formed based on strides S_1 and its complement, and the other can be formed based on S_2 and its complement, where $S_1 \neq S_2$ and $S_1 \neq N/2 - S_2$. The number of circles that can be scheduled in one round is limited not only by K (at most one per wavelength), but also by a function of T because a node can only be active in at most T circles. A heuristic scheduling algorithm based on CADS has been implemented, and the results for a 100-node ring[4] are shown in the two figures below for $2 \leq K \leq 10$ and $10 \leq K \leq 100$, respectively.





We have found that when $K < 10$, having one(1) transceiver per node is sufficient to achieve near-optimal performance. When $10 \leq K \leq 20$, two(2) transceivers per node are needed in a balanced system. Finally, at most 12 transceivers per node are needed. Our analysis have shown that in general, a balanced design will use between $NT/12$ and $NT/8$ wavelengths for a given T, or equivalently, $8K/N$ to $12K/N$ transceivers per node for a given K if scheduling is based on CADS. Since $K \leq N$, no more than 12 transceivers per node are needed independent of the size of a ring. Note that these results have also shown that much better performance (i.e. a shorter scheduling length) can be achieved in a ring than in a WDM Star with the same number of wavelengths and transceivers (usually one per node) [2].

5 Concluding Remarks

This study has, for the first time, applied the resource-balance principle to the optimal design of WDM rings for supporting all-to-all personalized communications. The proposed principle can be applied to balance many other resources such as physical connectivity, memory space, switching and processing power for general networks and applications.

References

[1] M. Chawki et al., "Wavelength reuse scheme in a WDM unidirectional ring network using a proper fiber grating add/drop multiplexer," *ELectronics Letters*, vol. 31, no. 6, pp. 476–477, 1995.

[2] G. Pieris and G. Sasaki, "Scheduling transmissions in WDM broadcast-and-select networks," *IEEE/ACM Transactions on Networking*, vol. 2, no. 2, pp. 105–110, 1994.

[3] when $S = 0$, only two connections having the same stride of $N/2$ are actually established.

[4] this is rather ambitious with current technology (see Willner & Hwang in IEEE PTL, 6:760-763, 1994), but is assumed to show how dramatic the following results can be.

Wednesday, August 7, 1996

SESSIONS:

WA: WDM System Technologies

WB: WDM Network II

9:00am - 9:15am
WA2

Digitally Tunable WDM Source

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Introduction: WDM technologies will play an important role in future broadband optical networks. Thus there is a demand for tunable components which can be tuned quickly, precisely and reliably to any desired wavelength within a tight tolerance [1]. In this paper we present the results of a digitally tunable WDM source which can fulfill all these requirements.

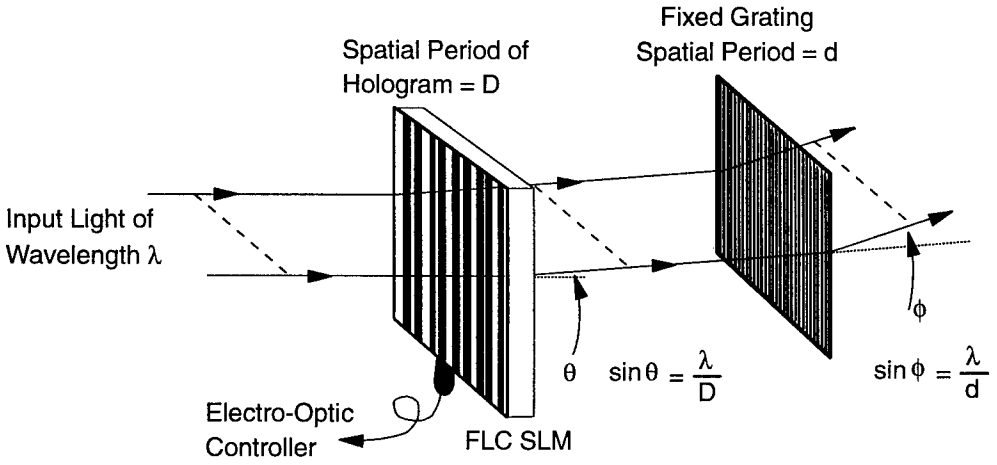


Figure 1: Holographic filter tuning mechanism

Design and Operation of Tunable Filter: The filter is based on a pixellated 2D ferroelectric liquid crystal (FLC) spatial light modulator (SLM), where each pixel can be electro-optically configured to give either 0 or π phase modulation of the light passing through. Digital control of the pixels gives rise to a digital 2D binary phase hologram or grating. Such a spatial grating is inherently wavelength dispersive and this effect can be enhanced by an additional fixed high spatial frequency binary phase grating. The fixed grating causes high wavelength dispersion, while the hologram displayed on the FLC SLM gives a controllable finer wavelength dispersion (see figure 1). Tuning is achieved by varying the fundamental spatial period of the displayed hologram, to change the degree of dispersion. Holograms are designed with iterative algorithms, such as simulated annealing, and may be tailored so that simultaneous wavelengths can be tuned to, and the relative strength of each tuned wavelength controlled. The fibre ring laser is constructed by connecting an erbium doped fibre amplifier (EDFA) with the tunable filter into a feedback loop. Spontaneous emission from the EDFA is filtered by the tuning element [2] which only allows a particular gaussian spread of wavelengths of FWHM 2.0nm to pass through. A 3dB coupler is inserted into the fibre loop to allow monitoring of the output power.

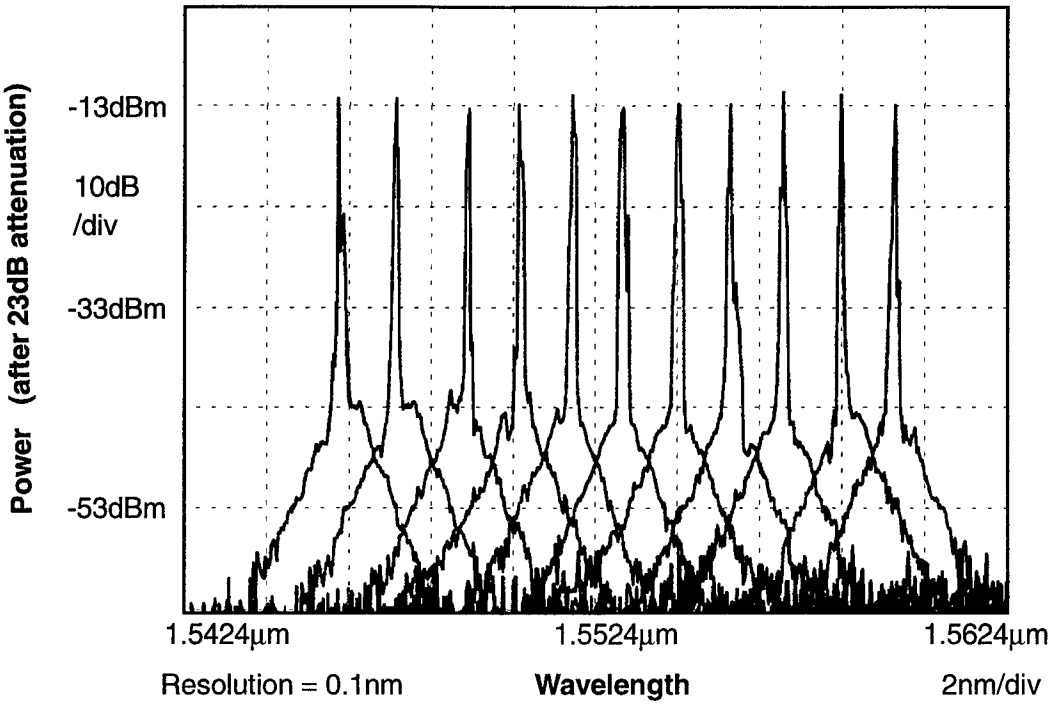


Figure 2: Eleven successively tuned lasing wavelengths

Results: The wavelength filter is tunable over a range of 82nm, but the spectral gain characteristics of the EDFA limited lasing to the range 1528.6-1567.1nm. Figure 2 shows an arbitrary group of 11 individual neighbouring lasing modes which the laser was successively tuned to. Uniform output powers for each wavelength of up to 10mW were achieved. The unequal spacing between the 11 lasing modes is due to fine differences in the spatial frequencies of the displayed holograms. When holograms are designed there are many solutions which should ostensibly tune to the same wavelength, but the solutions all have slight variations in their fundamental spatial frequencies which cause different lasing frequencies. This provides a possible mechanism for fine-tuning of the fibre laser. The short term linewidth of laser was measured to be < 40kHz, and the long term stability (over 4 hours) was ≈ 0.1nm. The frame update of the FLC SLM is 5ms, which determines the retuning time of the fibre laser. It should be possible to reduce this to about 10μs with a custom-designed SLM.

This digital holographic technology also has applications in space-wavelength switching and dynamic gain equalization of EDFAs. These will be further discussed.

References:

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9:15am - 9:30am
WA3

Fast nematic liquid crystal Fabry-Perot filter for WDM all-optical networks

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Optoelectronic Computing Systems Center, Campus Box 525, University of Colorado at Boulder, Boulder, Colorado 80309-0525

The recent developments in Wavelength-Division Multiplexing (WDM) systems in telecommunication networks have given rise to the need for fast tunable optical filters for dynamic tuning of the received or transmitted wavelengths in these systems. Recently demonstrated liquid crystal Fabry-Perot (LCFP) filters have achieved tunable wavelength ranges of 60 nm [1] to 75 nm with required tuning times "on the order of milliseconds, limited by the time required to reorient the [liquid crystal] molecules" [2]. Some nematic LCFP filters have exhibited slow response times, up to 50 s [3]. These earlier devices were constrained to relatively narrow wavelength ranges and slow tuning times due to the low birefringence of most nematic liquid crystal materials in the infrared region. The lower birefringence of the material within the Fabry-Perot etalon cavity implies that a thicker liquid crystal layer is required to obtain high transmission efficiency, thus resulting in a narrower tunable wavelength range and slower response times [4].

In this paper, we report a LCFP filter which utilizes a high birefringence nematic liquid crystal mixture PTTP-24/36 [5]. This material has $\Delta n \approx 0.35$ in the infrared region. The high material birefringence allows wide-range tunability and fast filter response times because only a thin layer of liquid crystal is needed to induce the required change in optical pathlength seen by light traversing through the filter.

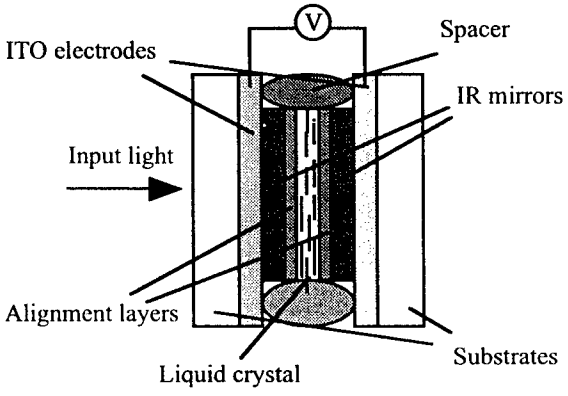


FIG. 1. Structure of a liquid crystal Fabry-Perot filter

The structure of the nematic LCFP filter is shown in figure 1. Two silica substrates, each of which has been coated with a transparent indium-tin-oxide (ITO) conductive layer and an infrared-reflective mirror, are spin-coated with a commercially available polyimide solution [6], then buffed mechanically. The buffed polyimide layer acts to align the nematic liquid crystal along the buffing direction parallel to the plane of the substrates. A Fabry-Perot etalon is assembled using the treated substrates separated by silica rod spacers suspended in UV epoxy. The resulting cavity is filled with the nematic liquid crystal by capillary action under low vacuum. The thickness of the liquid crystal layer is approximately 2 μm. The reflectivity of the IR mirrors is 98% for the wavelength range of 1530 nm to 1580 nm, but the reflectivity outside of this range is still quite high, thus resonance phenomenon is still expected outside of the mirror specification range.

When an electric field is applied across the cell via the ITO layers, the nematic liquid crystal molecules tend to align with the applied field, thus tilting out of the plane of the substrates. This tilting of the molecules results in a modulation of the birefringence and the optical pathlength seen by the incoming light. The net result is a tuning of the transmission peaks of the Fabry-Perot etalon.

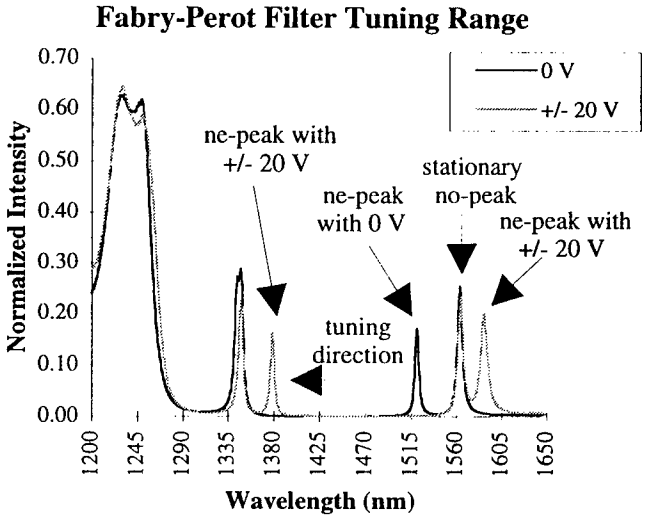


FIG. 2. Output of the liquid crystal Fabry-Perot filter with 0 V/μm and with $\pm$ 10 V/μm applied electric field

The device constructed as above was tested using a broadband light source and an optical spectrum analyzer [7] at room temperature. Variable square-wave AC voltage at 2 kHz was applied across the cell using a function generator equipped with an amplifier [8]. The tuning of the Fabry-Perot peak corresponding to the extraordinary ray is shown in fugure 2. The total tuning range

achieved with the electric field application of 0 V/μm to $\pm$ 10 V/μm was 142.2 nm.

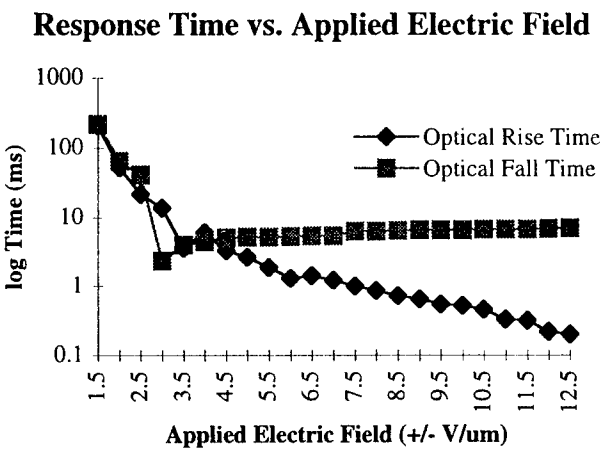


FIG. 3. The response times of homogeneously aligned PTTP-24/36, measured within the LCFP configuration.

The wavelength tune-on and tune-off times of the LCFP filter are directly related to the response times of the liquid crystal molecules within the etalon cavity to applied field. The response times of the liquid crystal molecules can be measured directly in the LCFP configuration by using a He-Ne laser light source operating at λ = 632.8 nm (outside of the IR mirror reflectivity range). The LCFP filter was placed between crossed polarizers, then variable AC voltage was applied to modulate the phase retardance of the nematic liquid crystal layer. The He-Ne laser beam was directed through the polarizer/LCFP filter combination. The throughput was detected using an avalanche-cascade detector, then monitored on a digital oscilloscope [9]. The rise and fall times of the throughput signal intensity, which correspond directly to the liquid crystal response times, are measured using a built-in function of the oscilloscope.

The results of the liquid crystal response time measurements are shown in figure 3. The full-range tune-on time, corresponding to the optical rise time with application of $\pm$ 10 V/μm, is determined to be 520 μs, and the full-range tune-off time, corresponding to the relaxation time of the liquid crystal molecules, is measured to be 6.6 ms. The tuning time could be improved further by using a slightly more complicated voltage-driving scheme to take advantage of the transient nematic effect [10].

In summary, a tunable liquid crystal Fabry-Perot filter utilizing a novel high birefringence nematic liquid crystal has been demonstrated. The filter has a wide tuning range of 142.2 nm around λ =1450 nm, with a full range tune-on time of 520 μs and tune-off time of 6.6 ms.

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[9] LeCroy 9310 AM Dual 400 MHz Oscilloscope.

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9:30am - 9:45am
WA4

Wavelength Demultiplexer for Sub-nm Channel Optical Amplifier WDM System

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Introduction

To obtain the higher capacity in an optical amplifier wavelength division multiplexing (WDM) system, each signal must be located at the narrow channel spacing [1,2] because the optical bandwidth of the system with cascaded Er^{3+} doped fiber amplifiers (EDFA) is restricted by their wavelength dependent gain. As the number of channels is increasing, the loss of optical devices for the wavelength demultiplexer becomes so large that optical amplifiers may be required. And as the accumulated chromatic dispersion is different from each channel, the dispersion must be separately equalized to be zero for the minimum penalty [3].

From these points of view, we proposed the practical wavelength demultiplexer using cascaded fiber gratings and optical circulators. Our proposed method can achieve the small excess loss and effective allocation of dispersion compensating for each channel, and introduce new channels without affecting other existing channels.

Proposed wavelength demultiplexer

The configuration of our proposed wavelength demultiplexer, for example, in the case of 4WDM system is depicted in fig. 1(a). 4WDM signal is dropped next by next with each fiber grating through each circulator. Only the shortest wavelength signal is not reflected by any fiber gratings and directly received. If other sets of fiber grating and circulator are added to the end of this demultiplexer, it would be able to be used for more channels. Moreover the accumulated chromatic dispersion is compensated by the common equalization fiber which is enough to be equalized at the longest wavelength signal and the individual equalization fibers locating after each fiber grating. As the individual equalization fibers are used for the signals dropped by the downstream fiber grating, the total length of equalization fiber can be saved. For the comparison to our method, the conventional demultiplexer such as 3dB couplers, the equalization fibers and the concatenation of 4 optical bandpass filters with a 1nm bandwidth is constructed like Fig. 1(b). Since the excess loss of our configuration for per one demultiplexing is about 5dB smaller than that of the compared one, our configuration would save the additional amplifiers for compensating excess loss as much as possible even in more densely WDM systems.

Demultiplexing results

To confirm the performance of the wavelength demultiplexer, 4WDM signal was transmitted through 2,500km system with 33km repeater spacing. The transmitted spectrum is shown in fig. 2. The each signal was externally modulated by the $LiNbO_3$. The nominal output power of repeater is +3dBm and the average noise figure is below 5.5dB. The average loss and zero dispersion wavelength of the fiber is about 0.21dB and around 1561nm. 20dB reflection bandwidth of the used fiber gratings is about 0.4nm and concatenated bandpass filter rejects the next channel signals with about 25dB loss. The Q factors of 4 channels after 2500km transmission are shown in fig. 3. Solid line shows the results of Q factor demultiplexed by our method with only common compensation. As

there remains about 400ps/nm to equalize at the shortest wavelength signal, the Q value of this channel degrades about 3dB than that of the longest channel. 2 types of dashed lines denote the separately equalized results obtained from the different demultiplexers. The accumulated dispersion of each channel is equalized with the appropriate length through the common and 3 different equalization fibers. The Q value of the shorter wavelengths recover up to 18dB and the channel deviation becomes within about 1.5dB from 4dB. The result of our configuration is almost same as that of the compared type, and no remarkable degradation was not observed due to using fiber gratings and circulators. In addition, our proposed configuration needed no additional amplifier up to 4WDM signal, though another amplifier for compensating the loss of the demultiplexer was inserted to the compared configuration.

Conclusion

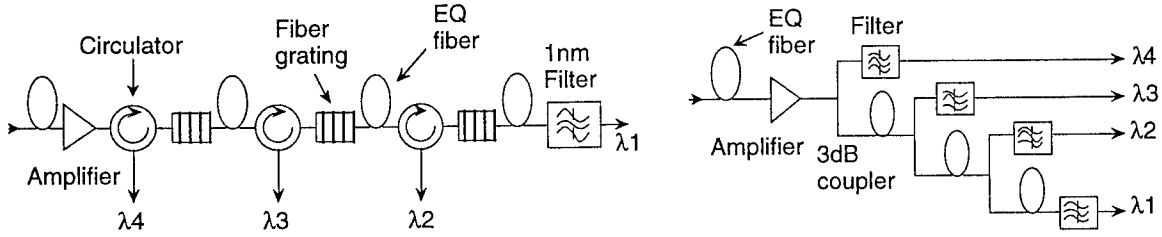
We proposed the wavelength demultiplexer using cascaded fiber gratings and optical circulators. And we have successfully demonstrated the wavelength demultiplexer with the small excess loss and the effective allocation of dispersion compensator for each channel.

Acknowledgement

We thank Mr. A. Yamamoto, Mr. H. Yamamoto and Mr. M. Tanaka for their support of this presentation and Dr. S. Akiba of KDD R&D Laboratories for helpful discussions.

Reference

[1] H. Onaka, et al, OFC '96, PD19, 1996. [2] N. S. Bergano, et al, OFC '96, PD23, 1996.
[3] H. Taga, et al, IEEE JLT, Vol. 12, No. 6, pp. 1042-1045, June, 1994.



(a) Our proposed configuration (b) Compared configuration

Fig. 1 Wavelength demultiplexer configuration

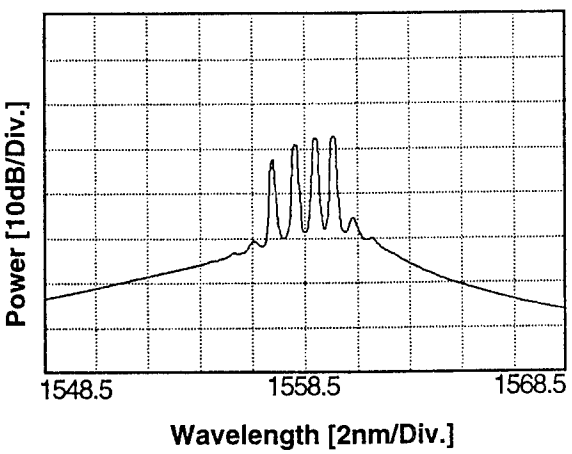


Fig. 2 Transmitted spectrum of 4WDM signal after 2,500km

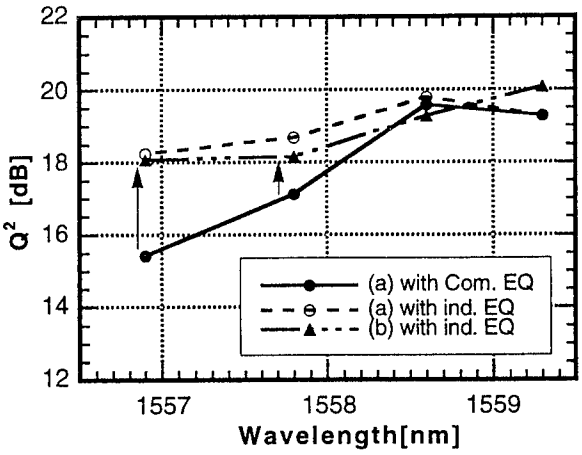


Fig. 3 Received performance of demultiplexed signals

9:45am - 10:00am
WA5

WDM Laser Tracking of an Uncontrolled, Remote Router Suitable for Local Loop Applications

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Introduction: Dense Wavelength Division Multiplexing (WDM) requires precise spectral alignment between the optical source and the passive WDM components. Recent demonstrations either require a reference wavelength, one or two channels for locking, and hold a WDM under local control [1] or require a pilot tone [2]. We demonstrate a new and robust digital method to *remotely* track rapid (1 C/min) uncontrolled environmental changes in a WDM device. Our method requires no RF circuitry, wavelength standard, or analog dithering. Our method enables a multi-wavelength source to track a multi-channel WDM component in the field within a local loop environment which is characterized by large temperature and received power variations, hardware limitations, and power fluctuations.

Principle of Operation: Our method shifts the wavelength comb of a multi-wavelength laser by temperature tuning the laser and comparing the transmission of the wavelength comb at the current laser temperature to that of the previous temperature. The algorithm compares the received optical power at the current DBR temperature, T, and the power at the DBR temperature $T+\Delta T$. If the returned power increases after the DBR temperature step ΔT, the DBR temperature is maintained at the new value and the cycle begins again. If returned power drops after the temperature step, the algorithm assumes that the misalignment has been made worse and the direction of the temperature stepping is reversed: i.e. ΔT goes to $-\Delta T$. The simplicity of the algorithm is expected to help meet the harsh slew rates and stringent cost requirements associated with local loop hardware. An impairment to the method is the noise associated with each power measurement.

Experimental Setup: The experimental setup is shown in Figure 1. A tunable DBR [3] with 100 GHz mode spacing was modulated with data and stepped in wavelength to match the four modes of a remote wavelength grating router (WGR) [4]. The router output was returned through an optical loopback that simulates upstream data in the Rite-Net architecture [5] and to an HP optical spectrum analyzer used as a proxy for a receiver circuit which would in practice be located at the central office (CO). Our tracking method is not restricted to a single architecture; in alternate architectures, power readings could be made at the ONU and telemetered upstream to the CO.

Experimental Results: The effect of wavelength tracking is shown in Figure 2. The router temperature profile was ramped at the maximum 1 C/min rate as defined by the ETSI specifications for temperature slew rates [6]. The algorithm was implemented with a step size of 0.03 nm and a step period of 2.0 seconds; widely different parameter values potentially lead to insufficient tracking slew rate, excessive power loss, or random walk-off, as will be discussed. Due to the thermal response of the router (0.011 nm/C), a 20.0 C variation in router temperature corresponds to a 0.22 nm shift in the router passbands potentially resulting in a power loss of 1.3 dB. Figure 2a shows the source wavelength tracks the passband shift caused by thermal stress on the router (Fig. 2b). The small deviations from the optimal DBR wavelength are the result of decisions to step the laser temperature in the wrong direction. The likelihood of step errors is dictated by the power measurement accuracy or SNR, and the consequence is loss penalty or walk-off. We have seen these step errors experimentally and through simulation.

The power penalty corresponding to spectral misalignment while tracking, under the same conditions as above, is shown in Figure 2b. The existence of power fluctuations is evident as is the algorithm's ability to track in the presence of fluctuations. Since thermally tuning the DBR tunes the entire comb of optical modes, the other three modes also track the passband shift.

Conclusion: In summary, we have proposed and demonstrated a digital technique for tracking thermally-induced spectral drifts in remote WDM devices by controlling the source wavelength comb with a single degree of freedom. Our method uses no pilot tone, sacrifices no channels, and tracks at near optimal slew rates. Differential measurements enable tracking in the presence of extraneous power fluctuations. We have performed experiments and simulations, with slew rate constraints, to understand the impact of temperature step size, length of time between steps, and

SNR on figures of merit such as algorithm-induced loss and tracking walk-off probability. Experimental and simulation results demonstrate that wavelength tracking reduces RMS power penalties from 1.3 dB to less than 0.11 dB for a 20 C variation in router temperature.

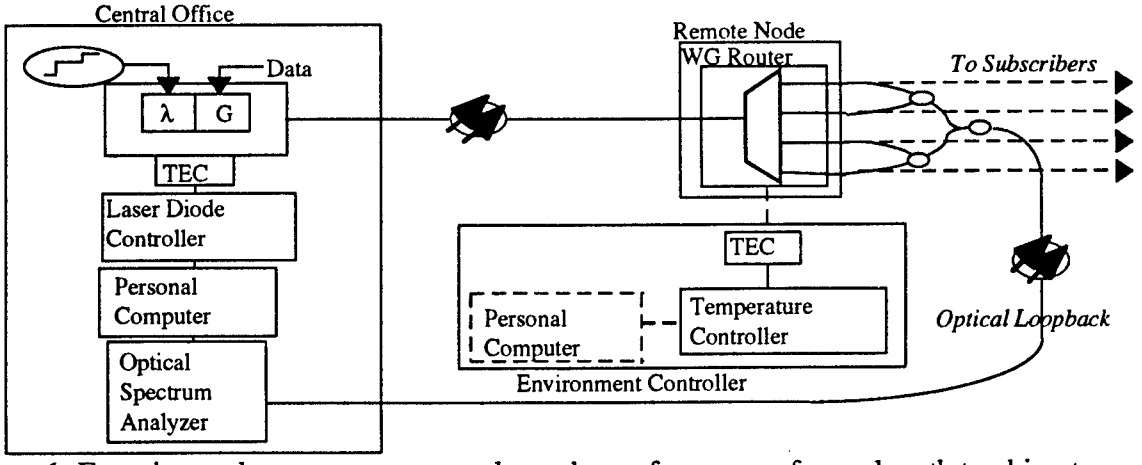


Figure 1. Experimental arrangement to evaluate the performance of wavelength tracking to compensate for spectral shifts due to external thermal drifts.

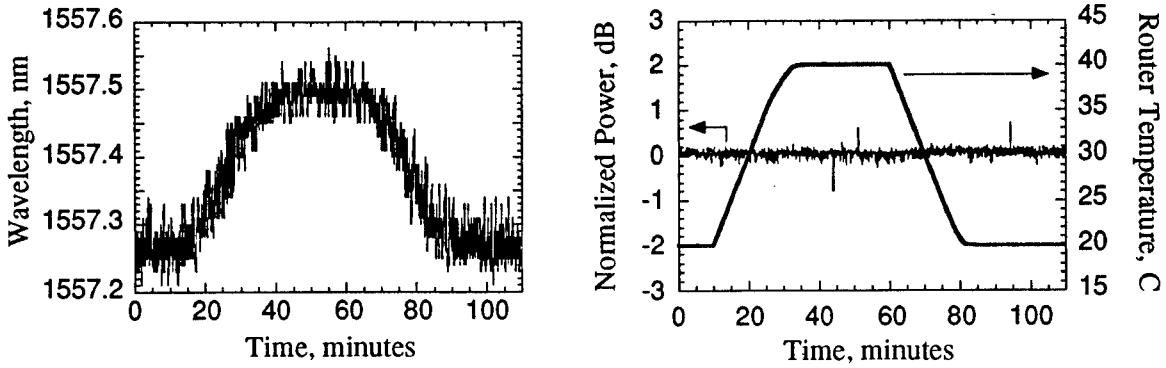


Figure 2: (a) Experimental DBR temperature profile with wavelength tracking implemented. (b) In the presence of 20 C router temperature variations (0.2 nm shift), the RMS variation in received power after the router filtering (0.3 nm passband FWHM) remains within 0.11 dB.

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10:30 am - 11:00am (Invited)
WB1

Metropolita n Optical Network

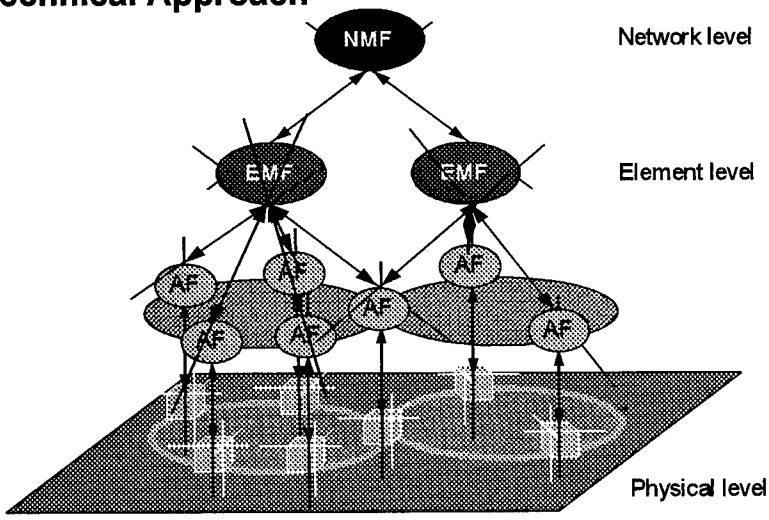
Sonny Johansson
Ericsson Telecom AB
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Email: etxsojo@kk.ericsson.se

ABSTRACT
Optical WDM networks would be attractive in the metropolitan area, but differ in demands and requirements must be met to compared to applications within long distance networks. The ACTS- METON consortium is developing a rearrangeble optical network for use in the metropolitan area.

Introduction

METON will stage a demonstration, in the Stockholm Gigabit Network, that will display various services/applications over an ATM switched network, interworking with an optical network. The optical layer will be developed by METON, together with a management system from where the demonstrator will be operated. Component technologies that enable realisation of a WDM network will also be developed and integrated into the demonstrator. The demonstrator and individual components will be evaluated against defined network requirements.
The goal is to develop an optical transport layer to support an ATM/SDH network to provide an effective transport in the metropolitan area. Network requirement will be identified by considering a future demand of a multi-services metropolitan network.

Technical Approach



PARTNERS:

LM Ericsson
Thomson
Telia
CNET
CSELT
Ericsson - Telecomunicazioni
Deutsche Telecom
Royal Institute of Tecnology
Technical Univ. of Denmark
HHI

Sub-contracted:

National Micro-electronics Research Center

Management Functional Architecture
A demonstrator is up and running in the Stockholm Gigabit Network, using equipment already available from RACE-MWTN. The demonstrator will then continuously be upgraded as new sub-systems are completed, tested and delivered, or when new software is developed. All new developments are focused to the optical transport layer and its functionality.
The optical layer will be formed by one Optical Cross-Connect (OXCs) and five Optical Add/ Drop Multiplexers (OADMs). The OXC fabric will be developed by refining an existing set-up, whereas the OADMs will be newly developed using different technology fabricated by METON.
The technology development will primarily be focused to the wavelength add/drop function exploiting fibre grating, silica-on-silicon, indium phosphide, and OEIC technologies.

For the purpose of demonstration the wavelength allocation has been specified to the 400 GHz frequency scheme that has been discussed in the standardisation body, ITU. Four channel have been selected from this frequency plan, which the transmitted channels must be locked to.
To guarantee that the optical channels are locked to the specified frequency grid, that the signal levels are kept within a determined range, and to ensure the transport quality in general, supervision with in the optical layer will be necessary. Appropriate monitoring points are implemented to provide

sufficient supervisory information for the management system.

The management system has earlier been developed to operate OXCs and OADMs focusing on element management. Focus will now be put on network management; to extend the functionality by considering future network requirements.

An Optical Control Cannel (OCC) enables transfer of management information and control signals over the network through the optical medium. Thus, enabling connection to remote optical nodes via integrated control paths.

Key Issues

- Network requirements that meet future capacity demands and desired functionality.
- Transmission characteristics of optical networks and their capability to meet requirement on dimension in different network topologies.
- Network management and control issues when operating an optical network, and also taking into account interoperatability with other networks.
- Information exchange within an optical network and means to establish communication channels between nodes by employing OCCs.
- Wavelength referencing and methods for monitoring and supervision in optical networks.
- Technology choice that enable a cost effective and robust realisation.

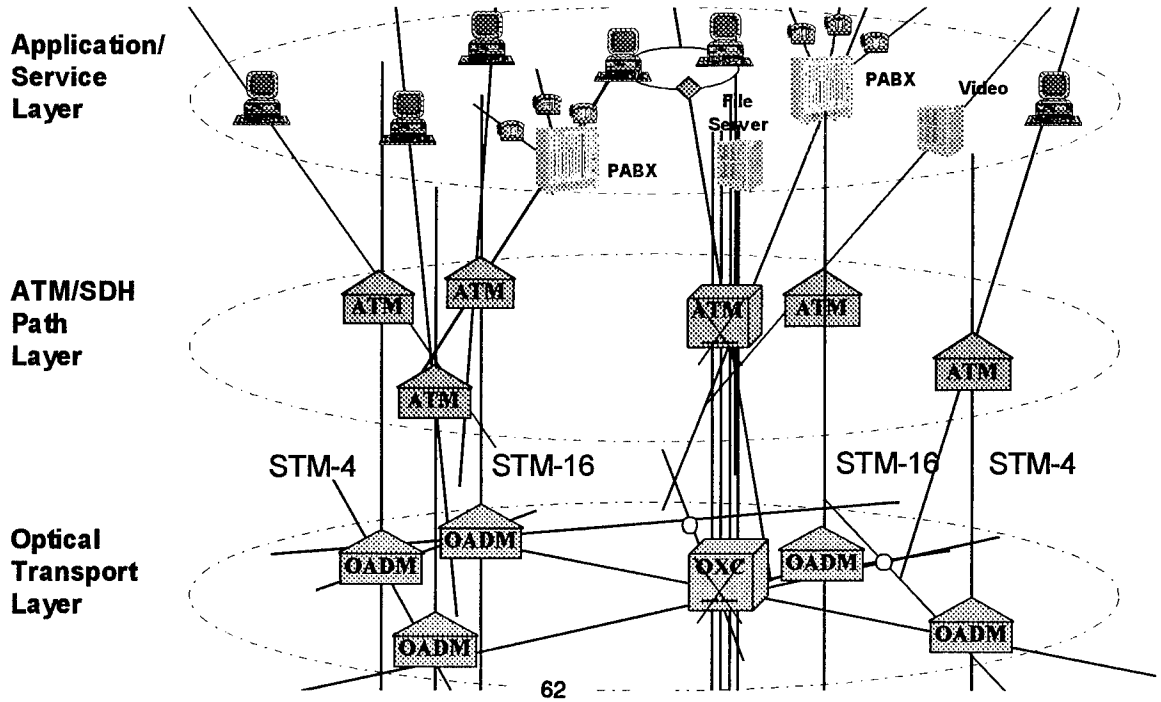
Demonstration

The demonstration is under development in the Stockholm Gigabit Network divided into a service/application layer, an ATM layer, and an optical transport layer. The network topology is two rings connected to each other through a centralised node. Five cites, distributed over the network as remote units, will be equipped with ATM multiplexers that provide access to the users. Various services will be available over the network and switched by an ATM switch located in the central node. An OXC, co-located with the ATM switch, serves for desired routing of the different optical channels over the network, whereas OADMs select and drop dedicated optical channels at each ATM multiplexers.

Expected Impact

Demonstrator outline

Results are expected to validate the use of an optical network layer as a compliment to ATM and SDH to achieve a cost effective, robust and flexible transport. Most Telecom operators are planning for an evolution of their networks before the end of this decade. Harmonisation and realistic planning will define the interfaces and requirements for the network components involved as well as for the management system. This is a prerequisite for standardisation and productification of these network components.



11:00am - 11:15am
WB2

The Optical Pan-European Network (ACTS Project OPEN)

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The OPEN project deals with an Optical Pan-European overlay Network (OPEN), interconnecting major European cities by means of a mesh of high-capacity optical fiber links crossconnected through transparent photonic nodes.

OPEN is the concept of a bearer network (Fig.1), built upon existing optical fibre infrastructure, offering a long distance transparent transport service for traditional and global network operators. This transparency pertains to the bit-rate and to the frame format. The capacity of each fibre link will be upgradable so as to offer a potential capacity of at least 40 Gbit/s , each channel with at least a capacity of supporting STM-16 SDH service. The proposed approach relies on the extensive use of Wavelength Division Multiplexing (WDM) for both transmission and routing purposes, but the interfacing with high-speed trunks carrying Time Division Multiplexed channels is considered as well. The aim of the project is to assess by modelling, laboratory experiments and field implementation of an optical crossconnect prototype, the feasibility of the OPEN concept.

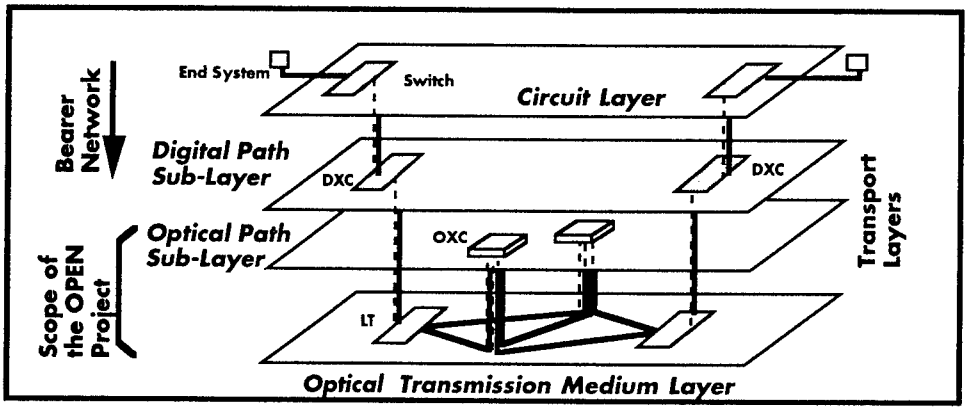


Figure 1: Layered transport network concept

In terms of network analysis, the project will establish the full description of the network, including the overall dimensioning, the evolutionary path from the existing infrastructures, the operation and management aspects and the protection schemes, so as to propose a sound vision of the various steps leading to the implementation of the OPEN network in a medium-term and in a longer-term perspectives.

The laboratory experiments in OPEN are geared toward the system validation of the OPEN concept and to demonstrate the upgradability of such a network to rates of Nx10 Gb/s as well as the feasibility of the OTDM/WDM interface.

Furthermore, one of the goals of the project is to assess the feasibility of the system concept under real operating conditions, by field implementation of an elementary three-node network. To this end, prototype photonic functional modules will be built and tested. The consortium has planned two cross-border field trials (see Fig.2), representing two different cases of implementation of OPEN over existing fiber routes: one will link Oslo in Norway (N) with Hjørring and Thisted in Denmark (DK), via a mix of terrestrial and submarine types of fiber cables; the second will link Paris in France (F) with Brussels in Belgium (B), via a terrestrial standard fiber cable to be installed in the near future. One transparent multiwavelength optical cross-connect (MOXC) built by the consortium will be installed successively in these two trials, along with appropriate commercial SDH terminal equipment. In the N-DK field trial, the MOXC will be located in Arendal (N), while in the F-B infrastructure, it will be located in Lille (F). Several experiments are planned on each trial, including protection, restoration, and cascadability of MOXCs.

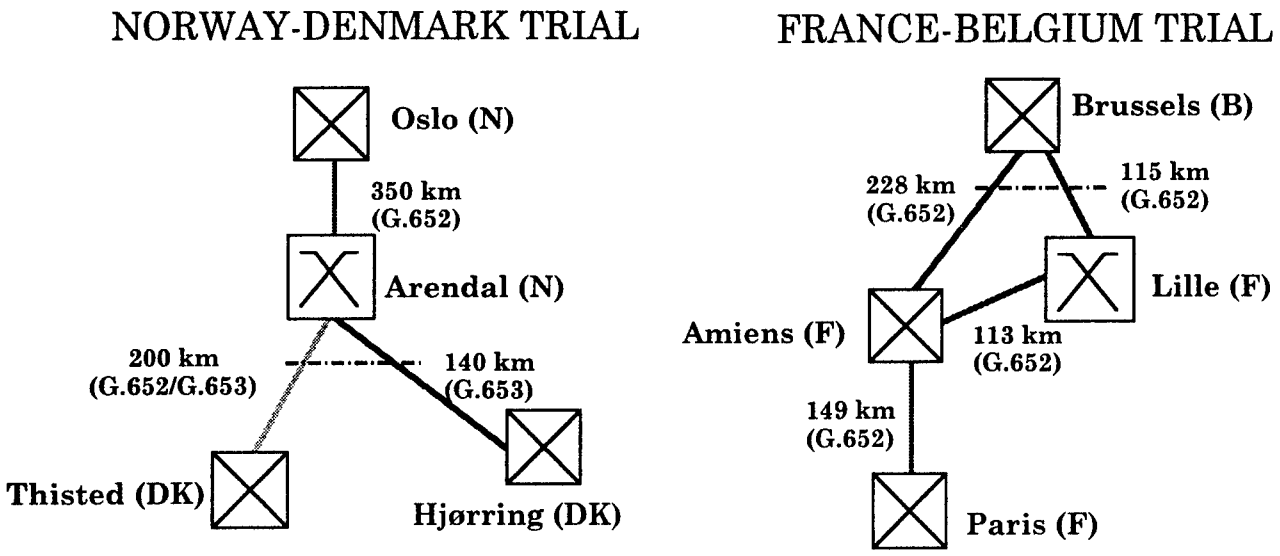


Figure 2: OPEN cross-border field trials

The OPEN MOXC has a 4x4 connectivity, and includes all-optical space routing by means of arrays of gain-clamped semiconductor optical amplifiers, channel selection through tunable optical filters, and wavelength translation using Mach-Zehnder-type interferometric wavelength converters. The routing is performed without any electrical regeneration, and alleviates wavelength blocking constraints. The node features full reconfigurability in terms of interconnection pattern and wavelength allocation.

In the presentation, we will give an overview of the project (project structure, participants, ...) and will pay a particular attention to the OPEN concept and the advantages that are brought by the use of WDM all-optical technologies (wavelength translation, WDM amplification, WDM dispersion compensation, ...) in a wide-scale pan-European network. We will also present the current status of the project, including the latest achievements in network analysis, fabrication and packaging of functional modules, system validation through laboratory experiments, and the field trial preparation.

11:15am - 11:30am
WB3

Parallel-Optical-Interconnecting Multiwavelength Star Network (POIMS Net) for the ultimate in high-capacity switching

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Abstract -- POIMS Net is a passive optical network that combines time-, space-, and wavelength-division techniques to yield network capacities far beyond 100 Gb/s. We describe its concept, practical implementation with an arrayed-waveguide-grating router, and application to the ATM switching fabric.

Introduction

Recent high-capacity local area networks (LANs) employ the physical star topology and centralized switch fabric for flexible cable wiring and dedicated bandwidth allocation. Serial optical interconnection to the switch fabric assures node bandwidths wider than 1 Gb/s whereas a centralized switch, such as the Fiber Channel fabric or ATM switch, provides network capacity of several tens of Gb/s by using space- and/or time-division electrical switching.

To cope with future increases in processor-performance, we will need to realize switching capacities over 100 Gb/s and node bandwidths over 10 Gb/s. The electrical switch fabric [1,2] will encounter serious limitations such as power consumption in time- and space-division switching and for electrical interconnections. Another problem will be its poor survivability; switch fabric failure interrupts all communications.

An interesting alternative for the high-capacity LAN is the optical wavelength-division-multiplexed (WDM) network [3]. It has a broadcast star topology with a passive star coupler at the center; each node has a fixed-tuned laser transmitter and a wavelength-tunable receiver. The WDM network has better survivability since switching is carried out in each node and hence requires no centralized switch. Another advantage is its low power consumption achieved by optical switching; no electrical switching nor intermediate O/E and E/O interfaces are required. Feasibility of the WDM network is, however, hard to confirm since 1) wavelength tunable optics and their operation are expensive, and 2) star-coupler loss and noisy burst-mode receivers restrict the possible network capacity far below 100 Gb/s; e. g. a 16-node system suffers from at least 12-dB broadcasting loss and may allow at most 2.5 Gb/s node bandwidth and 40 Gb/s total capacity.

POIMS Net described in this paper is another alternative for the high-capacity star network that employs distributed optical switching to provide better survivability and lower power consumption. It comprises time-, space-, and wavelength-division techniques to yield network capacity beyond 100 Gb/s. It requires no wavelength-tunable optics nor serial high-speed receivers, and is hence expected to be a viable candidate for future high-capacity star networks.

POIMS Net Architecture

POIMS Net is a broadcast-and-select passive star network [3]; the switching is carried out in each node at the receiver end. Its main feature is the dynamic establishment of *parallel* optical links between multiple node pairs. Fig. 1 shows the diagram of a 4 node POIMS Net. Each node transmits parallel optical signals on 4 wavelength channels λ_1, λ_2, λ_3, and λ_4 to its private star coupler at the center. Each star coupler multiplexes and broadcasts them to all nodes by its dedicated fibers. At the receiver end, a 4×1 optical switch selects the source node whose WDM signals are demultiplexed and received by the receiver array. This network provides non-blocking 4×4 space-division switching for 4-bit parallel optical links. Assuming a 16-node system where each node has a 16-channel WDM transmitter and receiver arrays with a 16×1 optical switch, the combination of all transmitter-receiver pairs carrying 2.5 Gb/s serial data stream yields 40 Gb/s node bandwidth and 640 Gb/s aggregate network capacity.

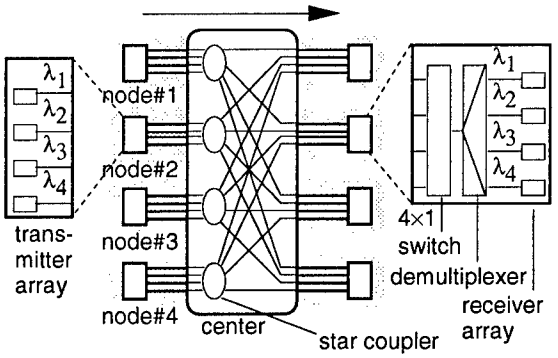


Fig. 1 POIMS Net configuration

POIMS Net employs three types of division techniques to achieve the ultimate in network capacity. Non-blocking space-division switching enables up to N simultaneous connections where N is the number of nodes. Parallel optical interconnection [4] is another space-division technique employed; it avoids power-consuming, noisy high-speed serial electronics as well as offering the benefit to burst-mode optical detection that is inevitable in optical switching.

The wavelength-division-multiplexing technique reduces the number of optical fibers and switches. It is

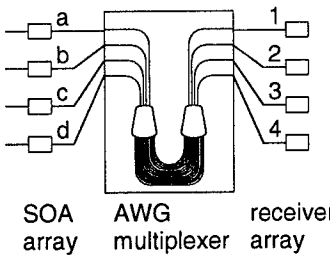
also indispensable for practical implementation with an arrayed-waveguide-grating (AWG) router and optical gate switches as is discussed later.

The time division multiple access (TDMA) technique is used for resolving receiver contention [5] and enables the flexible sharing of transmitter array, receiver array, and related electronics. It also provides modularity since all nodes consist of identical optics and electronics; neither wavelength tunable nor presetable optical devices are required.

Implementation with AWG Devices

One of the key functions of POIMS Net is $N\times1$ optical switching at the receiver end; sub-microsecond switching time, crosstalk less than 30 dB, and low insertion loss are required for efficient TDMA, to avoid beat-noise crosstalk influence [6], and to cope with the broadcasting loss at the center, respectively.

Fig. 2 shows the practical implementation of 4×1 optical switching and 4-wavelength demultiplexing functions. The semiconductor optical amplifier (SOA) array is used for gate switching whereas the arrayed-waveguide-grating (AWG) router [7,8] provides periodic characteristics as shown in the right part of Fig. 2. This configuration provides sensitive optical detection since 1) the SOA provides gain and 2) the periodic router avoids the combiner loss that is inevitable when a 4×1 switch is constructed with 4 gate switches [9]. It also relaxes the requirement for switch crosstalk since the following AWG router avoids the crosstalk causing beat noise. Note that all the devices shown in Fig. 2 will be integrated monolithically [10]. Faster switching will require semiconductor electro-absorption modulators (EAM's) instead of the SOA's assuming that their insertion loss is tolerable.



AWG multiplexer routing table

	1	2	3	4
a	λ_4	λ_3	λ_2	λ_1
b	λ_3	λ_2	λ_1	λ_4
c	λ_2	λ_1	λ_4	λ_3
d	λ_1	λ_4	λ_3	λ_2

Fig. 2 Receiver end for 4-node POIMS Net

Fig. 3 shows the results of a preliminary experiment using 1.5-μm InGaAsP EAM's with an AWG multiplexer fabricated by silica waveguide technology [8]. The 4-channel WDM signals from two different transmitter arrays were selected by turns every 43 ns where each channel was spaced by 0.8 nm and modulated at 2.5 Gb/s. The switching response was restricted by the EAM drivers to 100 ps. Burst-mode receiver operation has not been examined yet; it may require rapid phase acquisition and DC restoration [11].

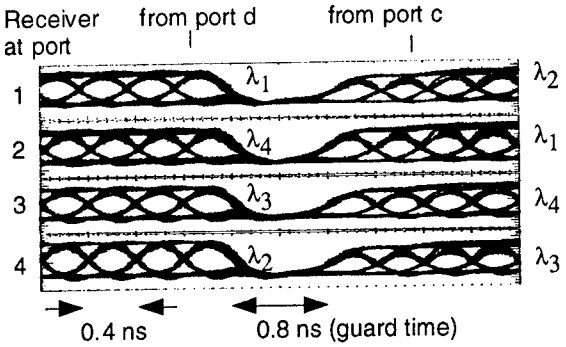


Fig. 3 Preliminary experimental results; receiver-array output for 2.5 Gb/s 4-ch parallel signals from 2 different input

POIMS Net Application

One of the POIMS Net applications is the switch core for a high-performance ATM switch [9]. Electrical switch core hubbing satellite switches with 10 to 20 Gb/s capacity indeed have realized 160 Gb/s aggregate capacity [1,2], but its huge power consumption, physical size, and difficulty in inter-cabinet cabling require further innovations. POIMS Net will be a viable candidate for the switch core because of its lower power consumption and higher modularity due to its distributed switching nature.

Future Work

POIMS Net indeed provides the ultimate in switching capacity by the optimum use of time-, space-, and wavelength-division techniques. Further innovations are needed in integrated opto-electronics, in burst-mode parallel optical transmitter/receivers, and in protocols suitable for distributed switching.

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11:30am - 11:45am
WB4

Increasing the capacity in real WDM network requirements: dispersion management and wide-band flat-gain optical amplifiers in Nx10 Gb/s transmission systems

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Making the best out of terrestrial transmission over installed standard single-mode fiber (SMF) is a cost-effective approach to future telecommunication systems. The challenge is to achieve a large throughput over a long distance with minimal added components to existing embedded fiber infrastructures. Wavelength-division multiplexing (WDM) seems to be the most promising approach to achieve large throughput transmission over terrestrial distances of several hundred kilometers [1,2]. The design of such high-capacity transmission systems establishes a duality between the number of WDM channels and the bit-rate-per-channel. The limitation on the former aspect arises from the available bandwidth which, in turn, reflects on the single optical amplifier bandwidth and the number of cascaded amplifiers, i.e., the amplifier span and the total transmission distance. The limitation on the latter aspect stems from the transmission line polarization-mode dispersion (PMD) [3], through which the achievable distance decreases as the square of the individual channel rate. On the other hand, the stability of optical components used in WDM transmission systems, such as sources, multi- and demulti- plexers, and filters, sets a lower bound on the channel spacing, and therefore on the total number of channels for a given optical bandwidth. From all these considerations, it seems that the most viable solution is the use of a large bandwidth (~ 25 nm) by means of a large channel spacing (~ 200 GHz) and wide-band flat-gain fiber amplifiers [4], along with relatively low individual channel-rates, which are favorable for transmission over several hundred kilometers in regard to the fiber PMD.

In this presentation, we will study the system design aspects of high-capacity, large wavelength span, and long distance transmission links based on conventional single-mode fiber. A particular attention will be brought to the dispersion map architecture. Indeed, a careful design of this map in terms of choice, position, and length of the dispersion-compensating fiber will reveal it to be a critical parameter for a reliable transmission in view of the interplay between the accumulated chromatic dispersion and the nonlinear effects. We will show that limitations brought by modulational instability and the accumulated dispersion per amplifier span rule out the propagation of the channels in a predominantly-positive total dispersion regime. Figure 1 shows numerical simulation on the propagation of 8 channels at 10 Gb/s spanning 25 nm in a dispersion-managed transmission over 510 km of SMF. As seen in Fig.1a three dispersion maps are considere: the dashed line represents a dispersion map in which the channels propagate predominantly in the positive total dispersion regime, the dot-dashed line represents a propagation predominantly in the negative total dspersion, and the solid line represents an almost symmetrical dispersion map with respect to zero dispersion. Figure 1b shows the corresponding receiver sensitivities. The impact of the dispersion map design on the system performance is clear, since a minimum of almost 3 dB additional penalty is brought by the positive-dispersion map. In addition to numerical and theoretical considerations based on a realistic analysis of the transmission link, recent experimental results based on this study and obtained for 8x10 Gb/s and 16x10 Gb/s [5] transmission over several hundred kilometers of conventional dispersive fiber and with a large bandwidth (≥ 24 nm) will be mentioned. In Fig.2, we show the measured total dispersion in a 16x10 Gb/s transmission over 531 km of SMF with a total span of 24 nm, using only 7 in-line fluoride-

based EDFAs. Here, all chanels propagate mostly in the negative total dispersion regime. Figure 3 shows the corresponding bit-error-rate curves for all 16 channels, featuring only 3.1 dB of sensitivity variation for all 16 channels along with the eye pattern of the most penalized channels.

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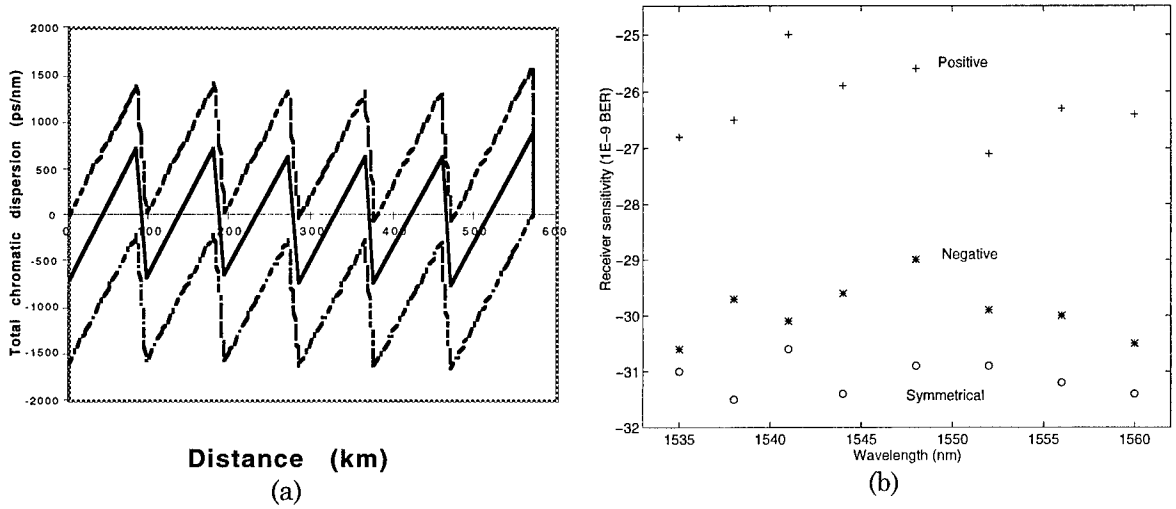


Figure 1: (a) Dispersion maps in the three cases of postive total dispersion (dashed line), negative total dispersion (dot-dashed line), and a symmetrical map (solid line). (b) Corresponding receiver sensitivities for all 8 channels.

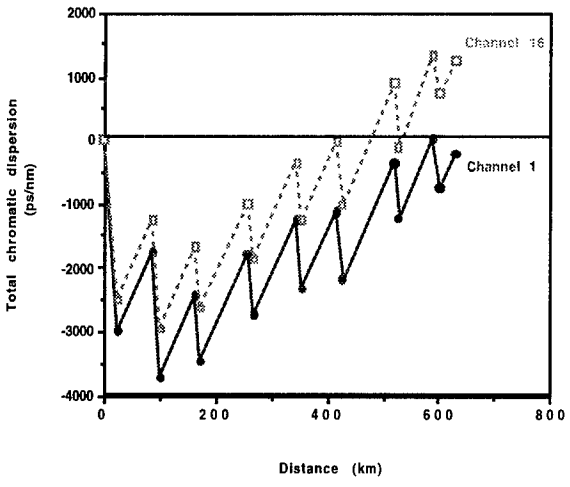


Figure 2: Measured dispersion map for channels 1 (shortest wavelength) and 16 (longest wavelength)

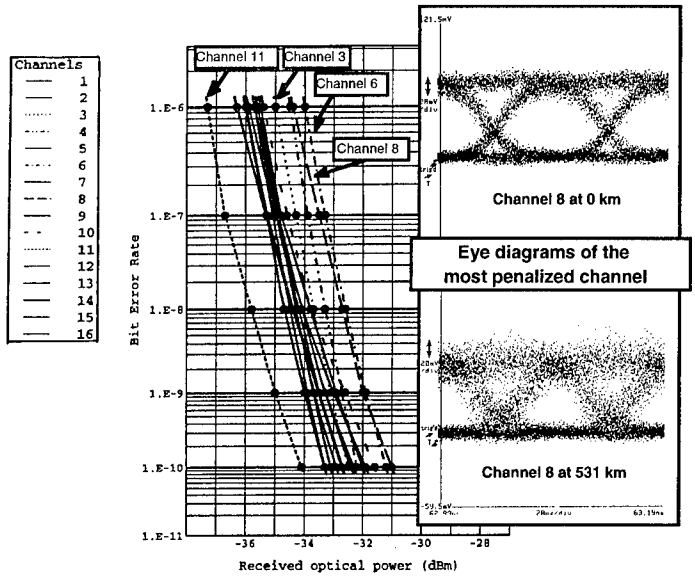


Figure 3: BER curves for all 16 channels and eye diagrams for channel 8

11:45am - 12 noon
WB5

Technical and economic comparison of full-service access network architectures

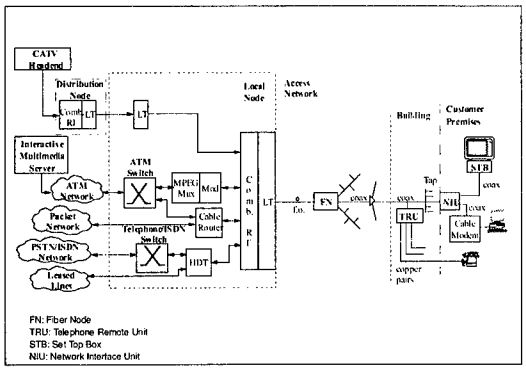
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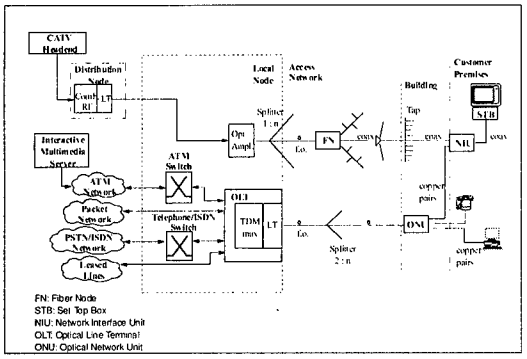
Summary

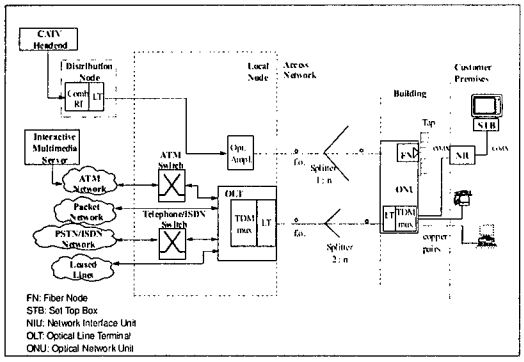
Nowadays technology improvement makes it possible to efficiently supply attractive services that imply the joined provision of voice, data and video, as video on demand, Internet broadband access, interactive video games, home shopping and tele-working. In order to support these new classes of services, new access network architectures are arising. In this scenario, the main purpose of this paper is to identify the most promising architectures able to provide residential and small business customers with traditional and multimedia services. After a short description of these access network architectures, a technical analysis and an economic comparison will be presented and discussed.

1 Description of the architectures

Among the several network options, the most interesting three architectures are:







Integrated HFC architecture

In this architecture, the network infrastructure is similar to that of traditional CATV networks already installed in several countries. About some hundreds of living units have been considered in a Fiber Node area. In order to set-up a full-service network several equipment have to be used like digital modulators and MPEG multiplexes for IMM services, or HDT and remote units, located for example at multi-flat block level, for POTS and ISDN, or cable router and single-user cable modems for Internet broadband access.

HFTTB architecture

The HFTTB solution consists of two overlaid networks: a FTTB based ATM-PON network for traditional telecommunication and multimedia services and a fiber and coaxial network for the provision of only video broadcasting services. A total splitting ratio equal to 1:16 in one stage and the Optical Network Units shared among few tens of living units have been considered for PON network. Although setting up and maintaining two separated networks are required, some synergies can be exploited for example in civil works and network infrastructures.

FTTB architecture

This solution involves the co-existence of two overlaid networks both FTTB based. An ATM-PON network for traditional telecommunication and multimedia services, almost identical to that in the HFTTB architecture, is combined to a SCM-PON network for CATV services. This network only for diffusive services roughly corresponds to the fiber segment of present CATV network with fiber node moved at customer buildings. In order to maximize the implementation of synergies and simplify network layout, the two PONs must have the same total splitting ratio.

2 Techno-economic comparison

Even if all the presented network architectures could be considered full-services architectures, their capabilities and functionalities are rather different.

The bandwidth, 622 Mbit/s downstream and 155 Mbit/s upstream, typically available on an ATM-PON network, is widely sufficient to transport all the services required by some hundreds of users. Therefore HFTTB and FTTB architectures are able to support a growing demand of bandwidth and service mix. On the contrary, the upstream bandwidth available on the coaxial section of the integrated HFC solution is limited. Therefore the band distribution among different services must be carefully defined and some concentration functions have to be introduced when the penetration of bi-directional services increases. Moreover, the provision of multimedia and telecommunication services on an integrated HFC network involves a large amount of "ad hoc" equipment: the higher is the service penetration, the bigger is the amount. In comparison ATM-PON networks are more flexible, since it is sufficient to plug the relative user-card in the ONU.

ATM-PON networks intrinsically support ATM functionalities, platform for the provision of every kind of service. Besides that, it enables a simplified end-to-end management of a connection and a dynamic bandwidth allocation on the basis of customer needs. Although ATM functionalities support cannot be excluded, in the integrated HFC solution the ATM protocol is usually terminated in the local node preventing the chance to extend ATM functionalities in the access network up to the customer.

The architectures are different with regard to environmental impact, too. In the integrated HFC network, a lot of electronic equipment is outside located while the FTTB architecture have no electronics in the external plant: this safer environment could make it possible to save costs for the equipment maintenance possible.

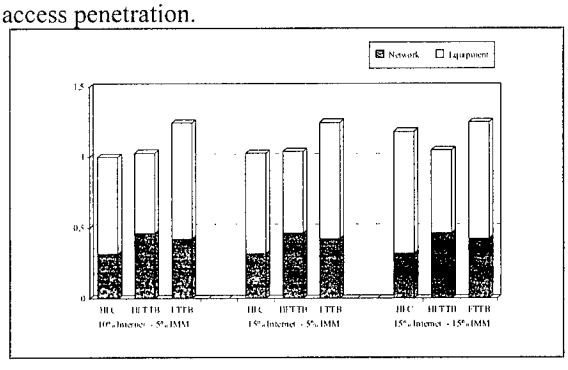
Besides the technical considerations, the economic impacts must be carefully evaluated, too. That is mandatory in the access network due to the high investments required. In order to evaluate this impact a cost analysis has been carried out by means of the software tool TITAN developed in RACE 2087 project.

It has been supposed to provide diffusive CATV, POTS/ISDN basic rate, 2 Mbit/s symmetric data connections, asymmetric interactive multimedia services (IMM) and Internet broadband access, the last two with a different percentage of penetration in order to make a sensitivity analysis.

Service	Year	Final %
CATV	1997	30
POTS/ISDN	1999	100
IMM	1999	5-15
Internet access	1999	10-15
Symmetric data	1999	4

The aim is to compare the three full-service architectures taking into account all the costs for setting up the network and the gradual service introduction during a 10 year period. In the table, the start of the provision and the penetration at the end of the studied period, for each service, are summarized.

The results of the analysis are shown in the figure. The graph highlights the influence of the penetration of IMM services and Internet broadband access with a 100% penetration of POTS/ISDN and an user density equal to 10000 l.u./km^2 and 16 l.u./building. The integrated HFC architecture shows a significant sensitivity to the IMM services penetration, due to the specific equipment that must be added to the network to support these services. However it does not reveal an important sensitivity to the Internet broadband access penetration.



The other two architectures do not show indeed a significant sensitivity to the multimedia services (IMM and Internet access).

It can be noted that the HFC architecture compares with the HFTTB architecture for low penetration of the interactive multimedia services, whereas the HFC cost increases sharply for higher penetration. The HFC architecture would have the lowest cost if penetrations lower than those ones used in this analysis were considered. The HFFTB architecture indeed is more advantageous for high service penetration. The FTTB cost is always higher than the HFTTB cost but the incremental cost is not so big, taking into account the FTTB strategic feature.

3 Conclusions

Some of the most promising multimedia network architectures have been presented and technically discussed. Then a sensitivity life cycle cost analysis has been performed.

The HFTTB and especially the FTTB prove to be the strategic solutions, because the ATM functionalities and the fiber can be extended closer to the user. In particular, the HFTTB architecture seems to be the best compromise between costs and implementation issues.

On the other hand, the integrated HFC architecture could be a good cost-effective choice for low bi-directional service penetration.

BROADBAND OPTICAL NETWORKS
Enabling Technologies and Applications

PAPERS NOT AVAILABLE FOR THE FOLLOWING

9:15am - 10:00am
Plen2: Broadband Network Strategies—A CATV Industry, A. Best, C*ox Communications, Atlanta, GA*
Most large cable operators have been aggressively upgrading their networks during the last five years by adding fiber and capacity. This "Fiber Serving Area" network topology will soon be used to provide a multiplicity of new services including wireline and wireless voice, high-speed data services, and digital video. This presentation will discuss Cox Communications' plan to provide these services in the market we serve. As part of this discussion, I will talk about the new Telecommunications Bill and how the cable operators, regional Bell companies, and the long-distance carriers are all preparing for the competitive landscape that lies ahead.

1:30pm - 2:30pm (Invited)
MB1: Very High Sped TDM Fiber Optic, J. Bowers, *University of California at Santa Barbara, Santa Barbara, CA*
Abstract Not Available

3:30pm - 4:00pm (Invited)
MC1: Advances in Sources for Wavelength Division Multiplexing, T. Koch, *SDL, San Jose, CA*
WDM has already begun to revolutionize point-to-point transmission systems, offering higher-capacity, graceful and cost-effective upgrades, and the potential for a natural evolution to new networking and routing architectures. While binned, temperature-stabilized DFB lasers provide a reliable source technology, pressure continues for advanced WDM sources that will relieve cost, inventory, and provisioning problems. This talk will survey the advances taking place in source technology that provide higher functionality, and may enable the widespread deployment of WDM into more cost-sensitive applications.

10:30am - 11:00am
TuB1: An Overview of the MONET Project, C.A. Brackett, *Bellcore, Red Bank, NJ*
This talk will be an overview of the MONET (Multiwavelength Optical Networking) project, describing the networking vision, the architecture and network elements, the technologies, and the overall project plan and objectives and recent results.

8:30am - 9:00am (Invited)
WA1: Terabit/Sec WDM Systems Technologies, H. Onaka, *Fujitsu Lab, Kawaski, JAPAN.*
We achieved 1.1 Tb/s (55-wavelength x 20 Gb/s) WDM transmission over 150 km of standard single-mode fiber using pre-emphasis, wideband EDFAs, and dispersion Compensating fiber with a negative dispersion slope. There was no noticeable BER degradation in any of the channels with no channel-by-channel dispersion adjustment.

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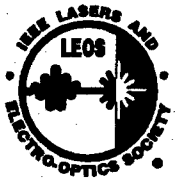
Smart Pixels

at

Keystone Resort

KEYSTONE, COLORADO







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SMART PIXELS

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Wednesday, August 7, 1996

SESSIONS:

WA: Devices for Smart Pixels, Single Smart Pixels

WB: Smart Pixel Integration Technologies

8:45am - 9:15am (Invited)
WA1

VCSEL-Based Smart Pixels

Shinji MATSUO and Takashi KUROKAWA
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3-1, Morinosato Wakamiya, Atsugi, Kanagawa, Japan
e-mail : mash@aecl.ntt.jp

Smart pixels incorporating vertical-cavity surface-emitting lasers (VCSELs) have shown great potential for use in optical computing systems and photonic switching networks because the integration of the VCSEL makes optical circuits easy to construct. Furthermore, a VCSEL is a good match for electronic circuits because it operates at a low voltage and a low current. Consequently, many smart pixels have been demonstrated that use VCSELs (Table 1). A vertical-to-surface transition electro-photonic device (VSTEP), which has a pnpn structure in the cavity, acts as an optical thyristor with small switching energy [1]. However, to get smarter and faster performance, heterojunction bipolar transistor (HBT) or metal-semiconductor field effect transistor (MESFET) circuits must be included in the pixel. A smart pixel consisting of VCSELs, HBTs, and pin-photodiodes has been demonstrated [2]. We have also developed integration with a VCSEL, MESFETs, and a metal-semiconductor-metal (MSM) photodetector, as shown in Fig. 1 [3]. In this device, both NOR- and OR-types of operation can be performed with the same circuit. The device operated at a high contrast ratio of more than 30 dB with optical gain. It also showed the 3-dB bandwidth of 220 MHz with 300-μW input power.

Hybrid integration with a silicon CMOS circuit is expected to make the function of the pixel much smarter. Flip-chip solder-bonding is one solution for fabricating this kind of device. For example, the integration of GaAs-AlGaAs multiple quantum well modulators and detectors with silicon CMOS circuits has been demonstrated in hybrid-SEED technology [6]. However, two flip-chip bonding steps are needed to fabricate a VCSEL-based smart pixel because the photodetectors should be on the same chip. We recently proposed a novel structure that uses three-dimensional integration of the compound semiconductor thin-film and a silicon circuit, as shown in Fig. 2 [7]. The VCSEL and photodetector layers are bonded onto a silicon circuit using polyimide. This method does not require any alignment before wafer bonding. The fabrication process for the photonic circuit is the same technology that is used in our monolithic integrated smart pixel, so it facilitates a wafer-scale fabrication process. To demonstrate this technology, we fabricated an MSM photodetector on a silicon substrate, as shown in Fig. 3. Each photodetector on the polyimide layer is electrically connected to the electrode on the silicon substrate. The electrical interconnection between the photodetector and the electrode on the silicon substrate consists of electroplated gold through the through-hole. The photoresponsivity of the photodetector was 0.3 A/W.

Finally, we discuss the feasibility of smart pixels, taking account of the packing density dependence on the operation frequency [7]. Figure 4 shows the maximum number of pixels as a function of operation frequency. We assume that one pixel has 25 gates in a 0.5-μm CMOS circuit, two VCSELs, and two detectors, and the cooling rate of the heat sink is 10 W/cm^2. The maximum number of pixels for an area of 1 x 1 cm^2 does not change when the operation frequency is less than 100 MHz because the power consumption of a smart pixel is limited by the peak current to the VCSEL. The maximum number of pixels then decreases with increasing operation frequency. At these frequencies, the bias current to the VCSEL must be increased with the operation frequency to decrease the lasing delay time. Furthermore, the power consumption of the CMOS circuit is proportional to the operation frequency and strongly depends on the bias voltage. Therefore, the power consumption of the CMOS circuit is not negligible at higher operation frequencies. However, in (ii), the maximum number of pixels is more than 1000 when the operation frequency is 1 GHz. This shows that both a reduced

threshold current, while maintaining the wall-plug efficiency of the VCSEL, and a reduced supply voltage to the CMOS circuit are necessary to obtain a high density array.

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[6] K.W. Goossen et al., *IEEE Photon. Technol. Lett.*, vol. 7, no. 4, pp 360-362, 1995.
[7] S. Matsuo et al., Technical Digest of International Conference on Optical Computing (OC'96), SENDAI, 1996, JWA 2, pp. 76-79.

Table 1. VCSEL-based smart pixel

	Detector	Electronics	Fabrication	Ref.
Kasahara et al. (NEC)	VCSEL	Thyristor	Monolithic integration	[1]
Alduino et al. (Univ. New Mexico & Sandia National Labs.)	pin-PD	HBT	Discrete device	[2]
Matsuo et al. (NTT)	MSM-PD	MESFET	Monolithic integration	[3]
Jin et al. (UCSD)	———	Si-CMOS	Hybrid integration	[4]
Stanko et al. (Colorado State Univ .)	Si-PD	Si-CMOS	Discrete device	[5]

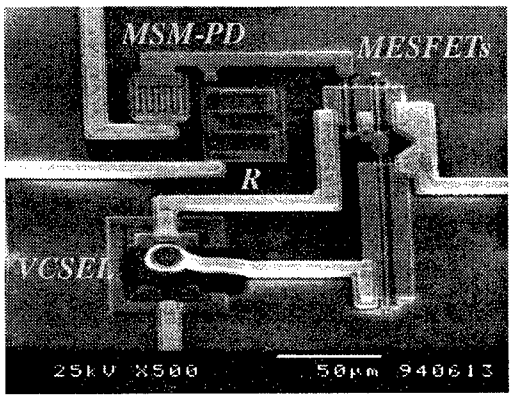


Fig. 1. SEM image of monolithically integrated device.

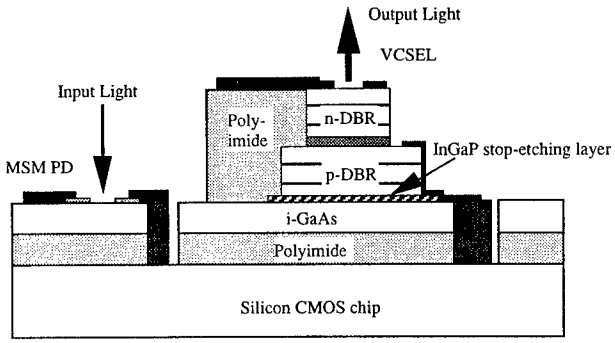


Fig. 2. Schematic cross-section of three-dimensional integrated smart pixel.

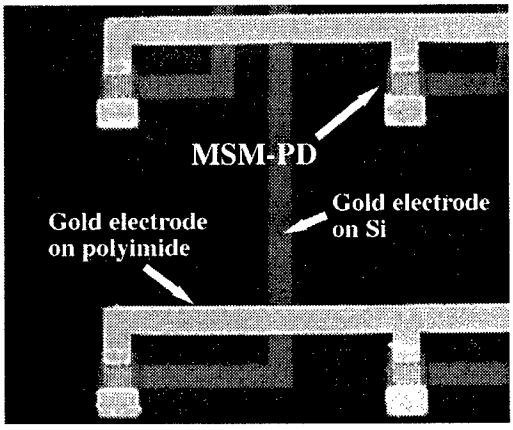


Fig. 3. SEM image of the hybrid-integrated device. MSM photodetectors are fabricated on the silicon substrate.

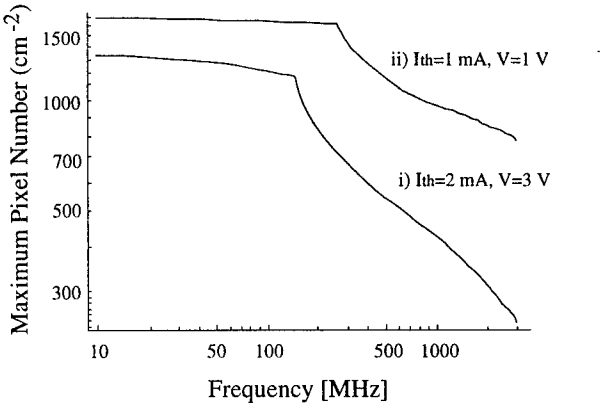


Fig. 4. Maximum number of pixels as a function of operation frequency.

9:15am - 9:45am (Invited)
WA2

Ultralow Threshold VCSEL's for Application to Smart Pixels

P. Daniel Dapkus, Michael MacDougal, Gye Mo Yang, and Yong Cheng
Center for Photonic Technology
University of Southern California
Los Angeles, CA 90089-0271

Recent technology developments in which the oxides of AlGaAs are employed as current apertures and in Bragg reflectors has created dramatic improvements in vertical cavity laser performance. The opportunities for extending these advances to produce submicroamp threshold VCSEL's will be discussed.

Summary

Vertical cavity surface emitting lasers (VCSEL's) are ideal components to incorporate into smart pixel arrays as active emitting devices. In addition to their obvious geometrical compatibility with 3D optical systems and full wafer integration, VCSEL's offer a unique opportunity to scale a photonic device to similar dimensions as electronic devices with a concomitant scaling of the electronic and optical characteristics of the device. The recent introduction of an integral oxide insulator technology in the form of the native oxide of AlGaAs[1-6] provides a clear path to scaling the lateral dimensions of VCSEL's to near 1μm dimensions while retaining high performance. Recent demonstrations of ultralow threshold laser operation (~9.0 μA)[4] and high wall plug efficiency[3] (>50%) in VCSEL's through the use of an Al_xO_y current an optical aperture suggest that integrable lasers with sub-μA thresholds may be possible with appropriate device design.

In this talk we will describe a design approach for low threshold VCSEL's that relies on the reduction of optical loss in the device structure to define an optimum operating regime in which both low threshold and high efficiency are achieved[3]. Using this approach we have been able to achieve threshold current densities as low as 140 A/cm^2 in VCSEL's. Based on these results and recent assessments of the efficacy of small oxide apertures to confine current and carrier injection in these structures, we will describe a technology path to achieving threshold currents less than 1 μA in optimized VCSEL structures.

We will also describe the use of the native oxide as a component of Bragg mirrors[5,6] that produce high reflectance, electrically isolated device structures that are suitable for electrical integration with electronic devices. The integrability of these devices arises from the relatively thin epitaxial structures that can be employed with the high contrast Al_xO_y/semiconductor DBR components while still achieving the necessary high reflectivity and from the use of intracavity contacted design that is isolated from the substrate by oxide used in the Bragg mirrors. The device design concept is shown in Fig. 1. The upper and lower mirrors consist of a few Al_xO_y / GaAs pairs with indices of refraction of 1.55 and 3.5, respectively. The electrical contact to the device is achieved by directly contacting the confining layers of the active region of the device and an Al_xO_y aperture is used to channel the current into the center of the reflectors and to confine the optical mode to the center of the mesa. Devices such as this have recently been demonstrated with 140μA threshold currents for 8x8 μm^2 apertures. The

characteristics of these devices are shown in Fig. 2 where the light output vs. current characteristics of devices with various top mirror reflectivities as indicated by the number of Bragg pairs in the mirror. With a mirror configuration optimized for maximum output power, differential efficiencies as high as 55% with threshold currents as low as 290 μA were demonstrated. In the talk we will describe how this device design can be utilized to increase the functionality of smart pixels based on VCSEL structures.

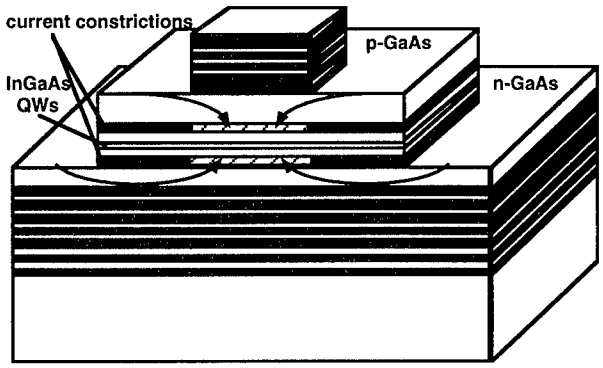


Figure 1 Schematic picture of oxide / semiconductor DBR VCSEL structure. the upper and lower Bragg mirrors are fabricated from AlAs/GaAs epitaxial structures in which the AlAs is selectively oxidized to Al_xO_y to form high contrast mirror pairs. Electrical contacts are made by directly contacting the n and p cladding layers. The current is channeled into the center of the mesa by the use of Al_xO_y current constriction layers.

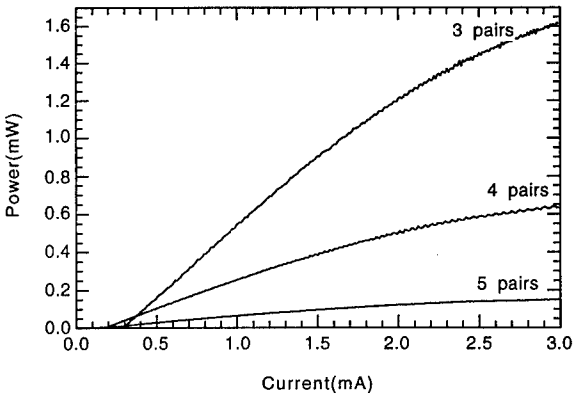


Figure 2. L-I characteristics of VCSEL's with a 7 pair Al_xO_y / GaAs lower mirror and upper mirrors with three different numbers of upper mirror pairs.

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9:45am - 10:00am

WA3 **Modeling of Low-Threshold Vertical Cavity Surface Emitting Lasers for Optical Interconnects**

H. Bissessur, T. Mukaihara, M. Abe, F. Koyama and K. Iga
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Recently, the threshold of 980 nm VCSELs with an oxide confinement structure has been reduced below 100 μA [1, 2]. We model their ultimate threshold performance as well as secondary mode discrimination, and estimate the carrier diffusion length in our devices.

The self-consistent model takes into account carrier diffusion as well as various optical processes like scattering or diffraction, and uses a logarithmic gain model for quantum wells. We assume uniform current injection into the active layer. The DBR mirrors are described in terms of effective reflectivities and effective propagation length. In order to calculate the VCSEL threshold, the optical field is propagated through the cavity until the steady-state is reached. The laser structure consists of a single 80Å thick quantum well centered in a one wavelength cavity, with an oxidised AlAs layer for current confinement. An effective length of 0.34 μm is calculated for each DBR mirror and effective reflectivities of 99.9% and 99.96% are assumed.

Due to the strong guiding properties of the oxide, light is well confined to the non-oxidised region, resulting in an improved overlap between the optical field and the pumped region. For small diameters, however, the threshold current density increases, because of diffraction losses, scattering losses at the oxide interface and carrier diffusion which reduces the available gain (see Fig. 1). The scattering losses can actually be reduced by using a thinner oxide layer. However, this also decreases the desired guiding by the oxide. From our calculations in Fig. 2, the optimum thickness seems to be around 40 nm in this structure.

The guiding properties of the oxide also affect the single transverse condition. The mode suppression ratio directly depends on the loss difference between the main and the secondary mode and on the spontaneous emission factor. As the diameter of the aperture is reduced, the loss difference increases since the secondary mode's diffraction and scattering losses become more important (see Fig. 3). Single-mode behaviour at threshold can thus be expected for small diameters. However, one should keep in mind that the secondary mode may lase even at threshold if the current injection in non-uniform.

Although carrier diffusion can hardly be reduced, since it depends mainly on the material parameters such as carrier mobility and lifetime, it is important to estimate the diffusion length in oxide-confined VCSELs. One method is to measure the spontaneous emission profile in stripe lasers with a continuous active layer, where local current injection is achieved by an oxidised AlAs layer. Since light emission from the laser facet usually includes both stimulated and spontaneous emission, we measure the spontaneous emission profile from the substrate side. The measured profile is then fitted to the theoretical curve. The stripe lasers were grown by low-pressure MOCVD. The active layer consists of three 80 Å thick InGaAs strained quantum wells separated by 100 Å GaAs barriers (see Fig. 4). After definition of 50 μm wide mesas by wet etching, the AlAs layer is oxidised by nitrogen gas bubbled through 80°C water, leaving $W \approx 8$ μm wide current flow apertures. The mesas are subsequently buried in polyimide and electrode contacts are deposited, leaving an opening on the n-side for measurement. The diffusion length, measured on 3 devices, varies between 1.0 and 1.4 μm; an example is given in Fig. 5. This would result in a minimum threshold of about 20 μA in the previously modeled device.

H. Bissessur thanks the Japan Society for the Promotion of Science for its financial support.

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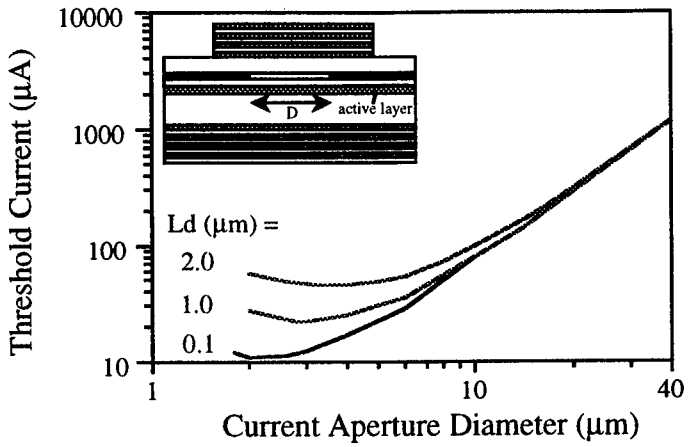


Fig. 1 : Modeled threshold current of oxidised and proton implanted VCSELs with a diffusion length Ld=0.1, 1 or 2 μm. D is the diameter of the current aperture (see insert).

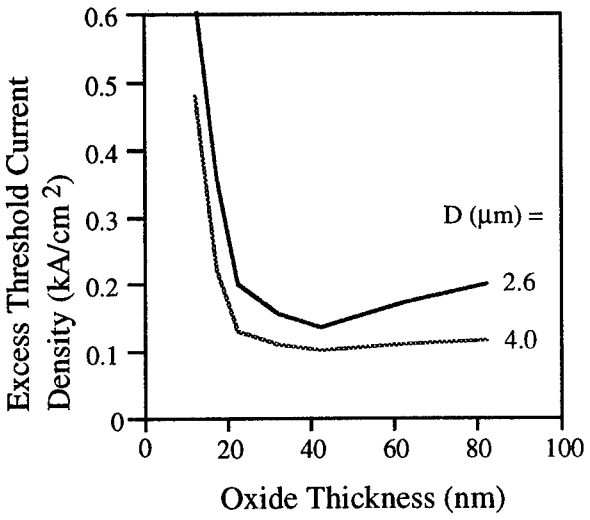


Fig. 2 : Calculated excess threshold current density (i.e., without the mirror losses) for Ld=0.1 μm and current apertures of 2.6 and 4 μm.

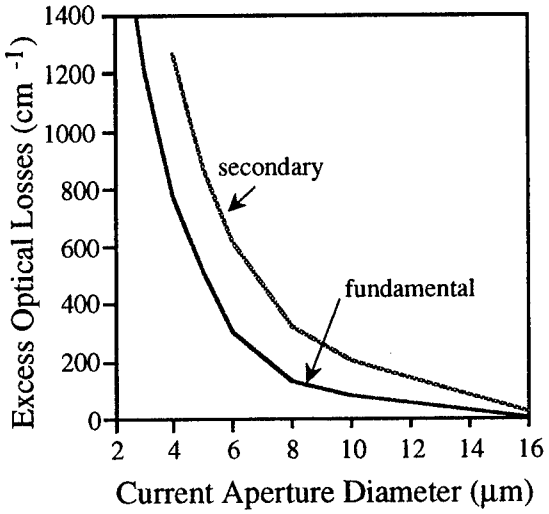


Fig. 3 : Modeled excess losses (other than mirror losses) of the fundamental and secondary modes

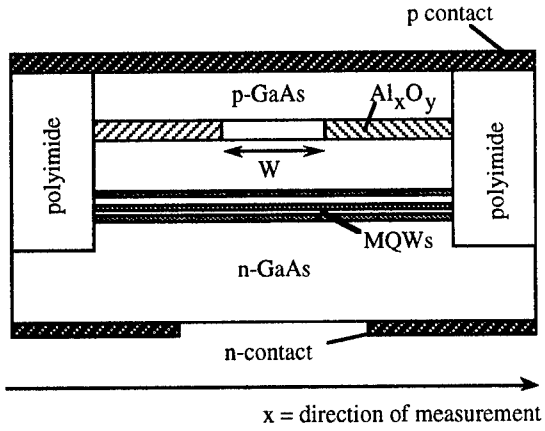


Fig. 4 : Schematic cross-section of the stripe laser with partially oxidised AlAs layer for current confinement.

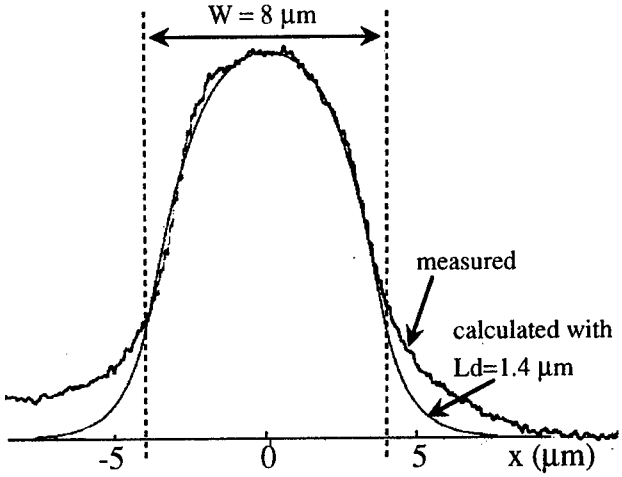


Fig. 5 : Spontaneous emission profile for W=8 μm and fitting function.

10:30am - 10:45am
WA4

Neuron Devices based on Point Contact Phototransistors

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ABSTRACT

We propose neuron devices that perform subtraction and nonlinear function with two-input and one-output optical signals. The device based on a pair of point-contact phototransistors and a LED can easily integrated with several hundred pixels.

1. Introduction

Neural network systems using optical parallel interconnections have shown advantages of light. Especially, optical neural networks based on two-dimensional (2-D) structure are useful to achieve the system that can treat 2-D images directly[1,2]. In the system that we developed, multiple images are generated by a Selfoc microlens array from input images. We have used a CRT or a liquid crystal device (LCD) as the devices that display input images. The synaptic weights that are changed according to learning algorithms are displayed on a Pockels readout optical modulator (PROM) or another LCD. The superposed images of multiplied input images and weights are detected by a CCD camera. Local accumulations and nonlinear operations are done in a computer. The calculated results are displayed on the CRT again and next layers operations are iterated. Usually synaptic weights have plus and minus values, however in the optical systems, weights are represented by intensities or transmittances of light. We prepared two (plus and minus) parts in synaptic weights. After the each calculations of vector-matrix multiplication the results of a plus part are subtracted by that of a minus part[3,4].

To realize large scale and fast optical neural networks, we need 2-D neuron device array with several hundred pixels. Multiple imaging and local accumulations of 1,000 neurons are already possible by using lenslet arrays. And liquid crystal (LC) spatial light modulators that can display one million synaptic weights are implemented. Moreover, silicon and LC based smart pixel technology implemented learning capability in the devices[5].

In this paper, we propose a new neuron device that can achieve subtract and nonlinear function with optical 2-inputs and 1-output.

2. Structure

The point contact phototransistor (PCPT) that we developed[6] has simple structure and can be easily integrated with a light emitted diode (LED) or a laser diode (LD) in vertical direction. The PCPT array has enough gain and can drive a LED or a LD without amplifiers. From this feature, the neuron devices based on PCPTs do not have complicated structure and need not difficult fabrication technology.

The neuron devices consist of 2 PCPTs and a LED (Fig.1). The current through a PCPT is controlled by input light intensity to the point. Therefore, the current according to the difference

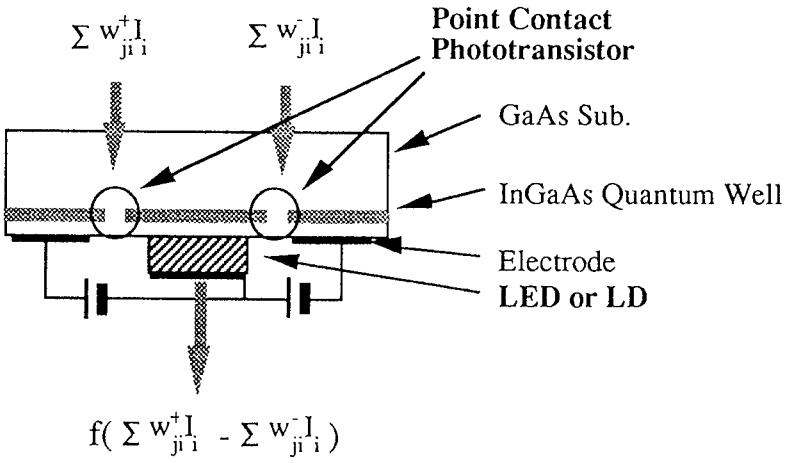


Fig.1 The neuron device structure with point contact phototransistors and a LED (or a LD).

of 2-input light power is injected to the LED. It means that the pair of the PCPTs realize the subtraction of a minus part from a plus part of the calculated results from input neuron and weight matrices. The LED emits according to injected current. The nonlinearity of the PCPTs and the bias current make Sigmoid-like input-output characteristics in the device.

3. Experiments

The basic structure of the PCPT we developed is a 10nm thickness InGaAs quantum well with GaAs barrier layers grown by molecular beam epitaxy (MBE). 200nm drains are etched out from the quantum well remaining a 200nm width bridge (see Fig.2). By MBE re-growth fill the drain by GaAs and n-doped GaAs layer covers the drain and the quantum well structure. Electrodes are deposited on the n-GaAs layers to connect with electric circuits. The single PCPT had sensitivity of 10,000 A/W at the range of several pW input light.

Outputs with a pair of the PCPTs are shown in Fig.2. Subtraction operation from 2 input lights were succeeded.

To get enough current to drive a LED, we made a PCPT array with 20,000 point contacts. The sensitivity of the array was 200 A/W. The reason of the gain deference between a single PCPT and the array is due to high resistance of electrodes and/or defects of the point contact structures. We connected the array and a LED. The light output-input characteristics are shown in Fig.3 with various bias voltages. With 5V bias voltage, the gain of 20 is obtained.

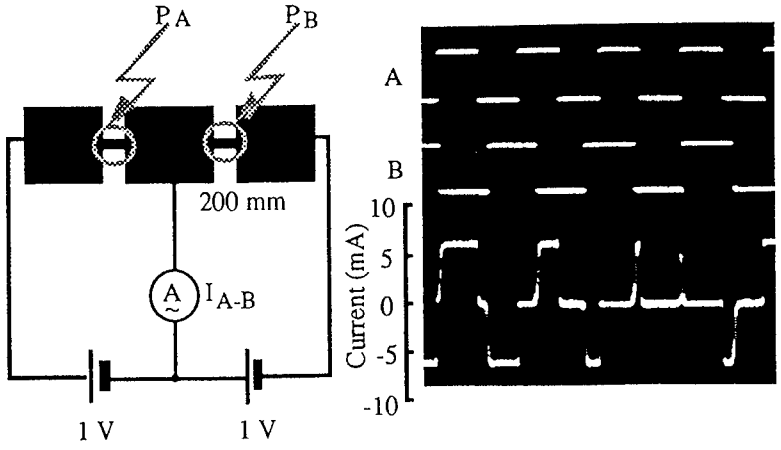


Fig.2 The subtract operation of the point contact phototransistors.

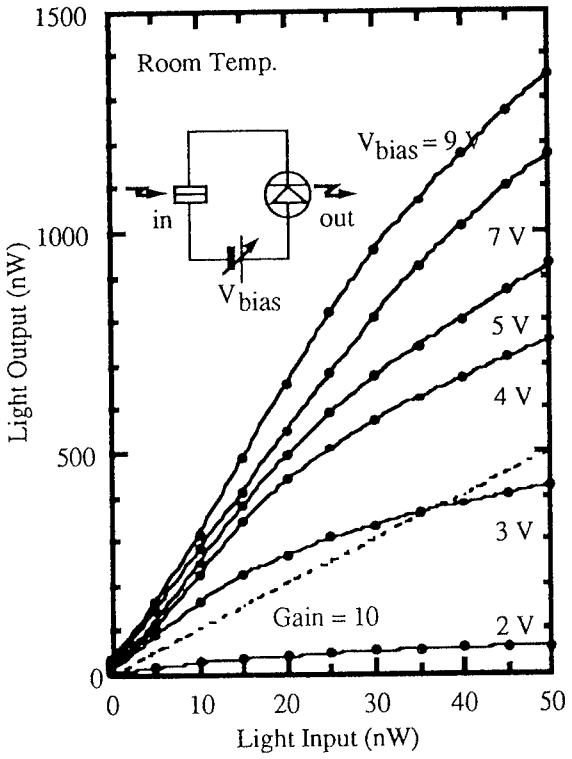


Fig.3 Light output-input characteristics of the circuit conbined a LED with a point contact phototransistor array with 20,000 contact points.

4. Conclusion

We propose the semiconductor neuron device that can be easily integrated with several hundred pixels in two-dimensional array. The device based on a pair of point contact phototransistors and a LED performs subtraction and nonlinear function with 2-input and 1-output optical signals.

We demonstrated the subtraction with 2-input light. Additionally we showed the large gain (more than 20) with a array of point phototransistors and a LED.

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Smart Pixel LCOS devices for Projection Display Systems

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Abstract

We are constructing a Head Up Display for an automotive application based on a Smart Pixel Liquid Crystal on Silicon microdisplay. We shall describe the application driving the device development, the display device and the technology enhancements implemented for this application.

Introduction

Liquid Crystal on Silicon (LCOS) spatial light modulators (SLM's) and microdisplays are made by placing a thin layer of liquid crystal directly on top of a silicon chip. We have constructed a high speed 256 by 256 binary SLM which uses a ferroelectric liquid crystal as the light modulating layer [1]. We have also recently constructed a high speed distorted helix effect analog 128 by 128 SLM [2] and a high voltage 128 by 128 analog SLM using the electroclinic effect in BDH764E [3]. This work has been motivated by the performance requirements of coherent applications which typically include high frame rate, small pixel pitch and good diffraction efficiency into a single (zeroth) diffracted order. These devices have been sucessfully used in optical correlators and holographic interconnect systems [4].

Liquid Crystal on Silicon Microdisplays

The requirements for a projection display system emphasise different aspects of the device design. For example, in the automotive Head Up Display (HUD) application which is motivating our current device development, we illuminate the liquid crystal on silicon device with over two orders of magnitude more optical power than in an optical correlator. This difference is important for the device design since photogenerated charges in the silicon substrate cause leakage currents which in turn lead to loss of image contrast. On our binary 256 by 256 device, which was optimized for single–order diffraction efficiency rather than optical power handling, the image begins to degrade at $\approx 30\text{mW/cm}^2$ of visible light illumination at 25,000 frames per second electronic refresh rate.

In other respects, Smart Pixel LCOS technology is well suited to display applications. The small size of the device can lead to a compact image engine for systems with packaging constraints and the high frame rates (kHz) available lend themselves for use in time–sequential color and/or grey–scale schemes. At the meeting we will present results from a 640 by 480 color microdisplay designed for this HUD application.

Optical System Design

An automotive head-up display (HUD) projects a virtual image in front of the vehicle, near the driver's direct line-of-sight. Information displayed by a HUD might include navigation

Key Optical Design Specifications

Virtual image size	9 x 6.5 square-inches
Virtual image brightness	3000 cd/m^2
Virtual image position	2 meters from driver 8-10 degrees below horizontal
Stage 1 package size	6 x 8 x 2 cubic-inches
Combiner element	Unaltered windshield

Table 1: Key optical design specifications.

and route guidance information, traditional instrument cluster gauges, and other human-machine interface data. By placing such information closer to the driver's line-of-sight, we can reduce driver strain and improve driving reaction times. Table 1 lists some of the critical automotive HUD specifications.

We are currently constructing a driver information HUD which utilizes a LCOS microdisplay as the image source. The automotive HUD consists of two optical stages. The first stage magnifies the the image generated by the microdisplay into a larger, intermediate real image. The second stage of the optical system further magnifies the intermediate real image into the 9 x 6.5 square-inch virtual image viewed by the driver. Key components of the optical system design include a 640 x 480 LCOS microdisplay device, a C-mount objective lens, a multi-exposure HOE field lens, and a dashmounted HOE.

The overhead HUD configuration is low in volume, non-invasive to the instrument panel, and easily adapted to different vehicle models. The system's most important feature, a compact package size, is enabled by the use of a microdisplay.

Acknowledgements

This work is supported by the National Science Foundation and Ford Motor Company through the Optoelectronic Computing Systems Center at the University of Colorado at Boulder.

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11:00am - 11:15am
WA6

Advances in pixel design and wafer fabrication for liquid crystal over silicon SLMs

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Mike W G Snook[B], Antony O'Hara[B], David G Vass[B]

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INTRODUCTION

In the past few years, a shift in emphasis has occurred in the field of liquid crystal over silicon (LCOS) SLMs from the development of general purpose / proof of principle type devices to application oriented (if not application specific) devices [1]. The primary uses for LCOS technology currently appear to centre around the following non-coherent applications -displays for head mounting, projection etc - and the following coherent applications - dynamic holograms and correlators.

While a growing number of specialist smart-pixel LCOS SLMs are being reported, the majority of applications oriented smart-pixel LCOS devices designed to date are still electronically addressed and are based upon pixel circuits which are the direct equivalent of, or a variation on, their electronic memory counterpart [2]

- single transistor dynamic random access memory (1T DRAM)
- six transistor static random access memory (6T SRAM)

OBJECT

In this paper we will discuss advances in silicon fabrication technology which have allowed the production of LCOS SLMs with enhanced specification and performance. We will discuss advances in pixel circuit design and VLSI layout, for both DRAM and SRAM based pixels, which have resulted in higher pixel packing density and improved pixel performance. We will illustrate these advances using examples of our most recent SLM designs. The discussion will be based around the topics listed below.

Scaling of silicon technology

The availability of commercial fabrication processes with smaller minimum device dimensions and larger die sizes has allowed the design and production of devices with larger and larger pixel counts. This will continue into the future.

Increased Complexity Available from Silicon Technology

As the number of layers available on the silicon increases, it is possible to stack more of the pixel circuit vertically, thus decreasing the pixel area. For smart

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[B] Department of Physics, The University of Edinburgh

pixels, this is particularly true of the increasing number of interconnect layers which can take on further roles in addition to that of interconnect. Such roles include those of light blocking and acting as a ground plane to add shunt capacitance (see below).

Custom Post Processing

This allows the addition of further layers of interconnect, the planarization of top layers for an optically flat finish and the deposition of a final mirror layer which is optimised for optical quality rather than the usual current carrying capacity [3,4]. It further allows the deposition, pattern and etch of layers for liquid crystal alignment and liquid crystal layer spacing.

DRAM Circuit Design

Optimization of the performance of the single transitor pixel circuit requires that the full 3-D nature of the pixel be taken into detailed consideration. Liquid crystal switching speed and contrast ratio are enhanced by the maximization of the shunt capacitance (which is used to drive the liquid crystal) and by minimization of charge leakage from the shunt capacitor.

SRAM and SRAM-XOR Circuit Design

We previously reported on a 10T SRAM-XOR pixel ciruit which has significant performance advantages over the 6T SRAM [5] for driving LC layers. We report here on a new SRAM-XOR circuit design which comprises as few as 8 transistors, allowing smaller area and reduced power dissipation in comparison with the 10T design.

SUMMARY

In summary we will consider firstly the requirements of the various applications and how they are best met by the available technology and secondly the prospects for continued advances in the medium term future.

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11:15am - 11:30am
WA7

A 155 Mbps Digital Transmitter Using GaAs Thin Film LEDs Bonded to Silicon Driver Circuits

Olivier Vendier, Scott T. Wilkinson, Steven W. Bond, Myunghee Lee, Zhuang Hou, Abelardo Lopez-Lagunas, Phil May, Martin Brooke, Nan Marie Jokerst, Scott Wills and Richard P. Leavitt
Georgia Institute Of Technology
College of Electrical Engineering
Atlanta, Ga 30332-0269

Systems which merge silicon circuitry and GaAs optoelectronic devices can produce smart pixel systems that take advantage of the complexity of Si circuitry while accessing optoelectronic functions. Integrated transmitter circuits optimally combine high complexity Si circuitry (VLSI) with optoelectronic devices such as surface light emitting diodes for low cost, short distance optical communication. Growth techniques for GaAs LEDs on bipolar Si [1] and GaAs [1, 2] circuits have been investigated to build integrated transmitters. However, to access digital circuitry, which comprises the majority of signal processing systems today, digital Si CMOS must be used for high yield. In this paper, high quality GaAs-based thin film surface light emitting diodes (SLEDs) have been integrated with a low cost, high yield standard foundry digital Si CMOS transmitter driver circuit. Hybrid integration of GaAs-based SLEDs with Si driver circuitry has been briefly reported [3,4], however, no speed data on the performance was reported on these integrated drivers. We report in this paper the fabrication and characterization of an integrated digital transmitter operating at 155 Mbps.

The foundry Si digital CMOS SLED driver circuit consists of two tapered inverters, a current switch, and a current mirror, as illustrated in Figure 1. The tapered buffer starts with a minimum geometry inverter and is used to drive a current switch. To avoid large voltage spikes, a current switch was not used in the final stage, however, the output stage does contain a current source. Node N2 has a large capacitance, since M1 and M2 are large transistors designed to deliver high current to the SLED. Switch SW1 is normally on and SW2 is normally off. When SW1 is closed and SW2 is open, the drive current turns the SLED on. When SW1 is open and SW2 is closed, then the capacitance charge of node N2 is discharged quickly through SW2, which provides a fast rise and fall time. To achieve current carrying capacities on the order of 40 mA, careful layout was necessary to minimize series resistance in the output power transistors.

The SLEDs were MBE grown and consists of GaAs (100 A, $p=10^{19}$ cm^{-3}) / $Al_{0.28}Ga_{0.72}As$ (2.349 μm, $p=10^{17}$ cm^{-3}) / GaAs (0.2 μm, $p=1.2x10^{19}$ cm^{-3}) / $Al_{0.28}Ga_{0.72}$ As (2.349 μm, $n=10^{18}$ cm^{-3}) / GaAs (100 A, $n=2x10^{18}$ cm^{-3}) with an AlAs sacrificial etch layer grown between the epitaxial layers of interest and the lattice matched growth substrate. After metal deposition for an ohmic contact and separation from the substrate, the thin film emitters were bonded to the circuits [5]. Polyimide was used for contact isolation, followed by polyimide via dry etching and metal deposition to contact the top of the device to the circuit. The broad area metal contact on the bottom of the device serves as a mirror, and,

combined with the Fresnel reflectivity of the top of the device, the integrated thin film SLED becomes a resonant cavity enhanced LED (RCELED) [6].

The thin film devices were dc characterized on the circuit, followed by full testing of the integrated transmitter. To characterize the integrated transmitter system we used a Tektronix CSA907T pattern generator which directly sent a digital 2^7-1 NRZ pseudorandom bit stream to the input of the transmitter. The outcoming optical data stream, shown in Figure 2, was focused onto a New Focus receiver using a two lens collimated mount. The optical eye diagram at 155 Mbps, after optical to electrical conversion at the receiver, was open, and was not filtered. Most of the jitter observed was due to the receiver noise. The average current to the RCELED was 20 mA with a 50 % duty cycle.

In summary, a low cost, low power digital silicon transmitter integrated with a GaAs-based RCELED has been fabricated and characterized. Operation at 155 Mbps has been demonstrated with a digital input, resulting in a transmitter which is integrable with digital Si circuitry, and is suitable for short haul optical communication.

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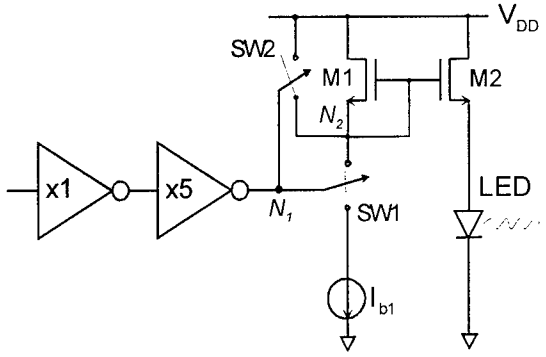


Figure 1 : Circuit diagram

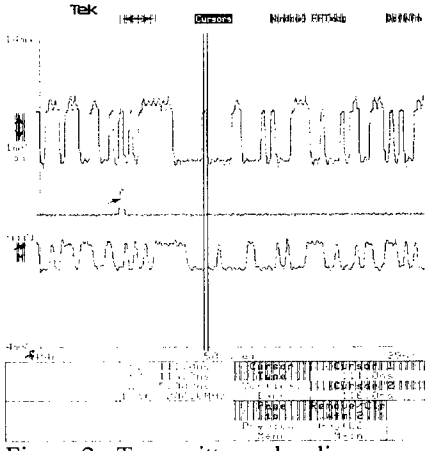


Figure 2 : Transmitter pulse diagram. From top to bottom : digital input, trigger, and optical digital output.

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WA8

CMOS Optical Receiver with Integrated InGaAs Thin-Film Inverted MSM Detector Operating up to 250 Mbps

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Standard digital CMOS receivers are desirable for their low-cost and low-power dissipation. In addition, tele-communication applications require long-wavelength (1.3 μm /1.55 μm) optoelectronic devices, which is possible only with compound materials. Because of material mismatch, implementing a monolithic optical receiver requires exotic process techonologies [1] or hybrid integration. Digital CMOS amplifiers with external photodetectors have been reported [2,3]. We have previously demonstrated an optical receiver in which GaAs photodetectors are integrated onto standard digital CMOS amplifiers [4-7] by using a thin-film epilayer device separation and bonding technology [6]. We now report that an amplifier has been fabricated in a 0.6 μm digital CMOS foundry, and integrated with an InGaAs inverted Metal-Semiconductor-Metal (I-MSM) photodetector sensitive to 1.3 μm/1.5 μm light, and characterized up to 250 Mbps.

Fig. 1 shows a single-stage amplifier circuit. The overall amplifier consists of 5 identical stages and is fabricated through a 0.6 μm standard digital CMOS process through MOSIS foundry. Each stage has a current gain of 3. The total transimpedance gain is about 12 KΩ with a 50 Ω load. To get a wide bandwidth, a multi-stage, low-gain-per-stage configuration is employed. Detailed operation of circuit in Fig. 1 has been reported [5,6]. To achieve stability, an open-loop approach over feedback-type is selected since an open-loop usually provides stability. Another important feature is the current-mode design. It gives wide-bandwidth capability due to low impedance nodes on the signal path. In addition, a diode-connected transistor at the front of an optical receiver replaces a bias resistor and minimizes parasitics.

A metal-semiconductor-metal (MSM) photodetector was selected since low capacitance per unit area is of vital importance in the design of high speed, low power and alignment tolerant optical receivers. The I-MSM detector, with the electrodes defined on the bottom of the device, overcomes the low responsivity problem of conventional MSM detectors with fingers on the top by eliminating the shadowing effect of the electrodes. The I-MSMs demonstrated up to 0.7 A/W responsivity and the leakage current is less than 10 nA at 10 V bias [7]. The bandwidth is up to 6 GHz. Because the I-MSM photodetector is fabricated separately, it is not compromized by CMOS process constraints. The detector structure has 3 μm metal finger width with 3 μm spacing between fingers. The detector size is 50 μm x 50 μm, resulting in 70 fF of capacitance. The detector is integrated onto the CMOS amplifier by using a thin-film epilayer device separation and bonding technology [6].

Fig. 2 shows a microphotograph of the completed receiver front-end after integration of the I-MSM photodetector. Two small pads at left side of the figure have overglass cuts for integration of the thin film detector in post processing.

The eye diagrams and pulse waveform at 250 Mbps has been measured for 2^7 -1 NRZ pseudorandom bit stream (PRBS) and are shown in Fig. 3. +/- 2.5 V power supplies are used for the amplifier. Total power dissipation is less than 20 mW. However, more than half of the power consumption is used for the offset control. Therefore, the 5-stage amplifier itself dissipates less than 10 mW and its size is about 150 μm x 50 μm. 50 Ω output impedance is used to measure the data in Fig. 3.

In conclusion, a quasi-monolithic digital CMOS amplifier integrated with 1.3 μm wavelength, InGaAs I-MSM is reported. The power dissipation is less than 20 mW. The sensitivity for 10^{-10} BER measured at 2^7-1, 155 Mbps PRBS is about 8 μA. To our knowledge, we have demonstrated a quasi-monolithic digital CMOS amplifier with 1.3 μm photodetector for the first time. This integration shows the possibility to make low-cost, low-power, and small-size digital CMOS amplifiers for tele-communication applications such as SONET and FDDI.

Acknowledgments: The authors would like to acknowledge the Army Missile Command under contract number DAAH01-92-D-R005 and National Science Foundation for financial support, Tektronix for an equipment donation, DuPont for a polyimide donation and Georgia Tech Microelectronics Research Center staff for their technical assistance.

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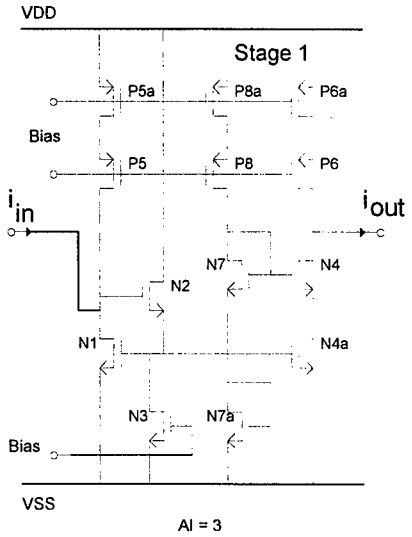


Figure 1. A single-stage circuit diagram of the standard digital CMOS amplifier.

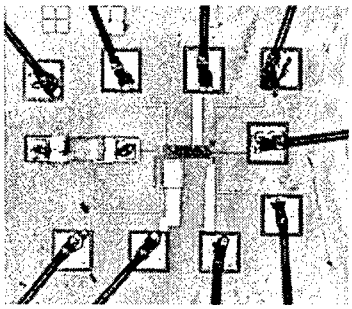


Figure 2. The microphotograph of the integrated amplifier.

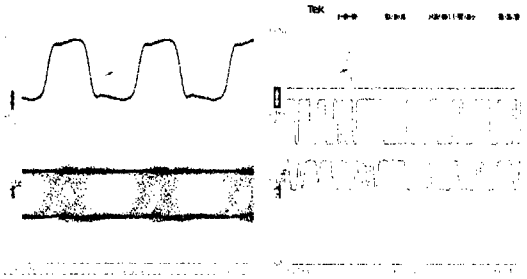


Figure 3. The eye diagram and pulse waveform of the integrated optical receiver at 250 Mbps.

Analysis of Pulse Width Distortion within an Optoelectronic Switching System Demonstrator

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Summary

Smart pixels[1] consisting of photodetectors, electronic circuitry, and electrical to optical (E/O) converters utilizing free-space optical interconnections show promise to relieve the interconnection bottleneck in computing and switching systems.[2] An experimental optoelectronic switching network[3] has been constructed using a new device technology,[4] optical system, and opto-mechanical system. Error free operation of a 2 x 2 section of the array has been confirmed experimentally at 155 Mbps, and operation as a time multiplexed switch has been demonstrated. Digital video, encoded into ATM cells, has been transported through the network, both in the lab and at a conference trade show, using multi-media adapters. In order to link with these adapters, the optoelectronic switching network interface had to conform to the ATM Forum User Network Interface Specification (ATM-UNI).[5]

The ATM-UNI describes the interface between ATM user devices and public ATM network equipment, and includes a physical layer specification. To ensure reliable data transmission, two specified physical layer parameters had to be met, namely bit-error rate (BER) and jitter. BER is a measure of probable errors, and is specified to be 10^{-10}, or less than one bit in every 10 billion bits sent. This parameter is generally associated with amplitude variations on the desired digital signal level, caused by added noise, that impede the receiver's ability to make a correct decision as to weather a logical '1' or '0' was sent. Jitter is the variation in the arrival time of the digital pulse edges, and may also impair the receiver's ability to make correct decisions, leading to bit errors. As the pulse rising and falling edges deviate from their intended location in time, the pulse shape is altered and is termed pulse width distortion (PWD). To meet the ATM-UNI specification, the total PWD must be kept less than 0.3 unit intervals (UI), where a UI is equal to the bit period. Thus, for our 155Mbps system, the total PWD must be kept less than +-2ns from the ideal pulse width of 6.4ns.

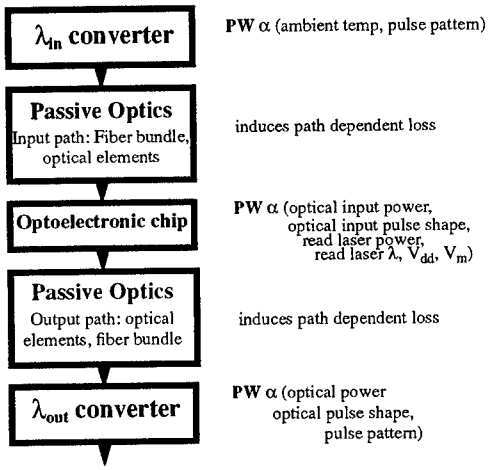


Figure 1. Simplified system block diagram depicting major PWD contributors

This talk focuses on the sources of PWD within our asynchronous optoelectronic switching system. A block diagram depicting the data path of this system is shown in Figure 1, with the signal originating at the input wavelength conversion boards and terminating at the output wavelength conversion boards. Wavelength conversion is necessary, since the ATM-UNI specifies 1300nm, and our optoelectronic chip operates at 850nm. The data pulses are regenerated, but not re-timed, in three locations, each of which may contribute to the total PWD. The first is the input wavelength converter, the second is the optoelectronic chip, and the third is the output wavelength converter. The passive optics on input and output paths shown in the diagram contribute a path dependent loss, which may induce PWD in downstream elements.

The input wavelength converter was found to contribute a pulse pattern dependant jitter of +0 up to -200ps. This asymmetric jitter is primarily influenced by the turn-on delay of the high power 850nm input lasers that were biased at threshold to ensure a high extinction ratio.

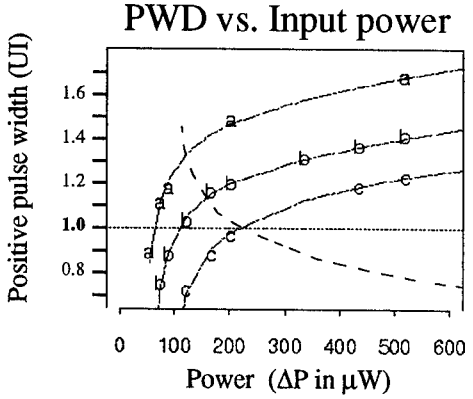


Figure 2. Optoelectronic switching chip positive PWD dependance on optical input power & V_{dd} bias (a=3.75V, b=4.0V, c=4.5V). Dashed line is -PWD for V_{dd}=4.5V.

The optoelectronic chip[6] was found to introduce path dependent PWD (i.e. the output pulse shape depended on which input was selected), primarily due to variation in optical input power levels to the receivers, caused by a non-uniform path dependant loss in the passive optics. Figure 2 shows the measured PWD as a function of applied optical input power (ΔP_{in}) for 3 different bias voltages on the optoelectronic switching node (shown as letters a, b, c) fitted to an empirically derived formula:.

$$PW = T - \Delta t + c$$

where
$$\Delta t = -\tau \ln\left(\frac{P_{peak}\left(P_{th} - \Delta P_{in}\right)}{\Delta P_{in}\left(P_{th} - P_{peak}\right)}\right)$$

$$c = y\left(\Delta P_{in} - \Delta P_{peak}\right)$$

where P_{peak} is the peak applied power for the desired pulse width value of T, P_{th} is the equivalent measured optical threshold power (31μW, 51μW, 78μW for V_{dd}=3.75, 4.00, 4.50), and ΔP_{in} is the applied optical input power. The values of τ and (y) were set to 3.8ns (1.8), 2.2ns (1.7), and 2.1ns (1.4) for V_{dd}=3.75V, 4.0V, 4.5V respectively.

The exponential term involving τ, accounts for the exponential rise time of the input signal to reach threshold, and includes the optical rise time of the source laser. The linear term c, accounts for the saturation effect of the clamping diode on the fall time.

The sensitivity of the optical input threshold power to V_{dd} bias was observed to shift at a rate of +54μW/V at a nominal V_{dd} = 4.25V, which agrees well with initial spice simulations. From Figure 2, it may also be seen that there is a trade-off between receiver sensitivity, and dynamic range for a given amount of PWD. The receiver PWD was calculated by allowing the following tolerances: P_{th}(+-5%), V_{dd}(+-2%), and 6.5dB dynamic range with a -3dB margin, and resulted in approximately +-800ps worst case PWD.

Besides the receiver contribution, there were two other possible sources of PWD within the optoelectronic chip. These were the logic and the output optical modulators. The logic was found to contribute negligible PWD. The output modulator PWD was dependent on readout laser wavelength, modulator bias voltage, and chip temperature. The global temperature of the chip may be controlled by conditioned air or a TEC, so a negligible temperature induced PWD was assumed.[7] A PWD sensitivity of 240ps/V and 190ps/nm was measured at nominal values λ=852.2nm and modulator bias (V_{mod}) of 5V. Allowing a tolerance of +-5% to V_{mod}, and λ+-1nm, resulted in modulator induced PWDs of +-60ps and +-190ps respectively.

The output wavelength converter had a maximum pulse pattern dependant PWD of +-400ps for a 45%/65% duty cycle data stream.

When all contributors are combined, the total worst case and RMS PWD for our system was +-1.6ns and +-1ns respectively. Since some of the sources are correlated, due to the pattern dependency, the RMS value would underestimate the total, while the worst case would tend to be over-conservative.

After allowing the system to operate for two weeks, a maximum eye closure of 1.2ns (~0.19 UIs) of PWD was measured on a sample of four paths. Thus, our system was found to meet the ATM-UNI physical layer requirement of less than +-2ns or 0.3UIs of PWD.

Acknowledgments

This work was partially sponsored by ARPA under Air Force Rome Laboratories contract No. F30602-93-C-0166. We also thank the authors of Ref [6] for providing the switching chip, and the authors of Ref[3] for construction of the system prototype.

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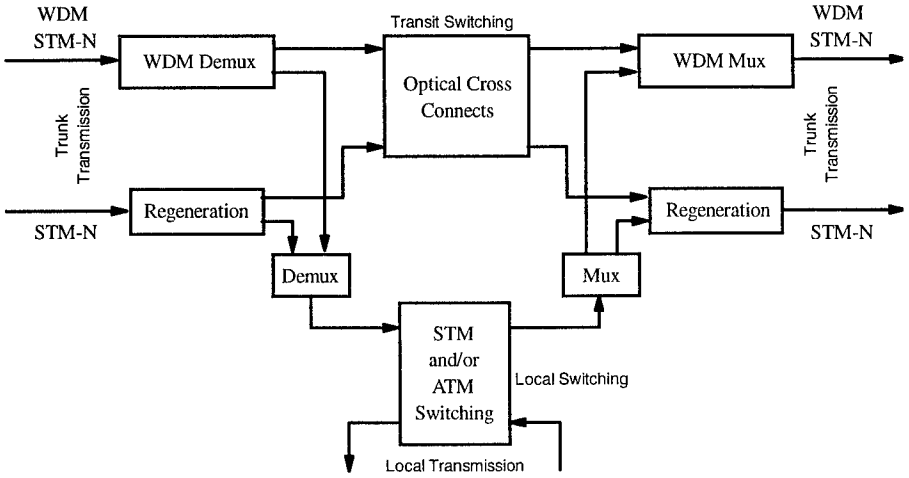
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OPTICALLY TRANSPARENT SWITCHING IN TELECOMMUNICATIONS USING FERROELECTRIC LIQUID CRYSTALS OVER SILICON VLSI CIRCUITS.

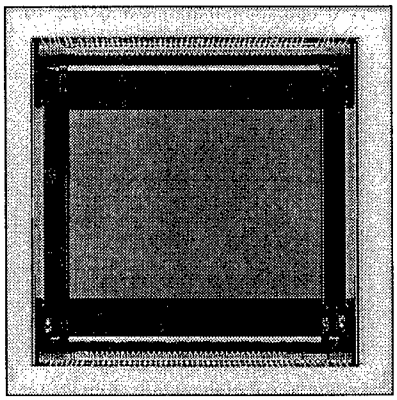
W. A Crossland (Nortel Professor of Photonics) and T. D. Wilkinson

Fibre optic communications is the basis of long haul telecommunications transmission. Fibre to fibre optical switching can avoid detecting, regenerating, demultiplexing and multiplexing these high capacity optical signals. A more general requirement is that indicated by the optical crossconnect in the upper part of the figure below. which represents a generalized network node. The transport layer is envisaged employing multiwavelength techniques (wavelength division multiplexing, WDM) based on the principle of wavelength routing[1]. The optical crossconnect should ideally have the capability to route any wavelength channel to any output port in an 'optically transparent' manner. Free space optics could make space and wavelength switches more scaleable than is possible with guided wave devices.



Optical interconnections are also used in the heart of large electronic systems, such as the STM or ATM switches that might be situated lower down in the node the above figure. Here the motivation is to avoid the bandwidth and connectivity limitations inherent in electrical connections at various levels in the structure, ultimately down to the level of the silicon integrated circuits. Optics should support the capabilities of silicon VLSI and ease the interconnection bottleneck in these large connection-intensive electronic systems. The use of free space optics in equipment backplanes[2] or in chip-to-chip interconnections[3], raises the possibility of exploiting the high parallelism and connectivity of optics, as well as the available bandwidth. This paper reviews progress with fibre to fibre optical space switches using ferroelectric liquid crystal over silicon VLSI spatial light modulators that might find application in route protection switches, optical crossconnects or routers.

FLC Over Silicon VLSI Technology.



Ferroelectric liquid crystals (FLCs) offer a method of integrating flexible light modulators into silicon VLSI circuits[4]. Such modulators can have large attenuation ratios or can be phase modulators offering full π phase shift on switching[5,6], as required for the efficient holographic steering of light beams[7]. When used as the reconfiguring element in an optical interconnect, a large electro-optic effect is needed. Under these circumstances current switching speeds are approaching 10 μsec[8], and might ultimately approach 1 μsec. Optically transparent switches can therefore handle very high data rates with modest reconfiguration times. If the light modulators are

being used to signal binary information across an interconnection path, then a more modest attenuation ratio of perhaps 10:1 might be acceptable. Smaller faster electro-optic effects could be used which have demonstrated switching speeds below 1μsec, and could perhaps ultimately achieve speeds of about an order of magnitude lower[9]. In many applications the switching speed should ideally match silicon memory access times. However, it is practical to place very large arrays of modulators on a chip (above is shown a VLSI silicon chip designed for 70,000 modulators). The high parallelism should allow a high data rate to be maintained.

Shutter Based Routing Switches.
The OCPM collaboration[8] has built a compact 64x64 single stage fibre optic crossbar that operates with single mode fibres on the input and multimode fibres on the output. It is based on the Stanford matrix vector multiplier modified to use holographic optics in a matrix-matrix configuration. The reconfiguration time is <20 μsec.

Holographic Beam Steering Switches.
Progress is reviewed with holographic beam steering switches based on writing phase holograms to arrays of FLC pixels[6,7]. These avoid the loss of power associated with fan-out. They are therefore practical for single mode to single mode fibre switches. To be effective they require radically different silicon backplane designs and major changes in the electro-optic effects compared with shutter based switches that modulate pixel intensity.

Wavelength filters and wavelength-space switches.
We will review techniques using fixed gratings in conjunction with shutter arrays[10] and reconfigurable wavelength filters[11] using grating based on reconfigurable arrays of FLC pixels. Ways in which these structures can be integrated with free space optically transparent space switches, so that any wavelength or space channel may be switched to any space channel, are of particular interest.

Reconfigurable Chip-to-chip Optical Interconnections in Large ATM Switches.
The possibility of enhancing large VLSI switch structures by using reconfigurable chip-to-chip interconnects based on FLC-VLSI technology has been investigated[12]. An attempt has been made to estimate the performance required by the free space optics and the modulators embedded in the silicon VLSI opto-electronic circuits based on a novel 3-stage switch design.

Acknowledgments: The work in this paper was collected from the Photonics and Sensors Group at Cambridge University Engineering Dept. and Electrical Engineering Dept. at Kings College London. The work is being supported by the EPSRC project Parallel Opto-Electronic Telecommunications Systems (POETS).

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2:30pm - 2:45pm
WB3

Multiple attachment GaAs-on-Si hybrid optoelectronic/VLSI chips

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For several years we have been developing an optoelectronic/VLSI (OE/VLSI) chip technology based on flip-chip bonding of GaAs optoelectronic chips onto CMOS silicon followed by substrate removal (Figs. 1,2) [1]. This work proceeded to demonstrate circuit integration [2], 3-dimensional optoelectronic-over-VLSI integration [3], LSI optically-interconnected switching circuits at clock speeds of 700 Mbits/sec [4], and 1 Gbit/sec receiver circuits in 45x25 μm areas [5]. Our optoelectronic devices are currently surface-normal modulators, which also function as the input detectors, and their loading has been shown to be < 60 fF [6]. Finally, we have demonstrated an OE/VLSI switching chip with > 140000 CMOS gates and 4352 modulators that operated with a clock of 400 Mbit/sec [7]. Our typical modulator yield is 99.9 % and we have produced chips with 100 % yield.

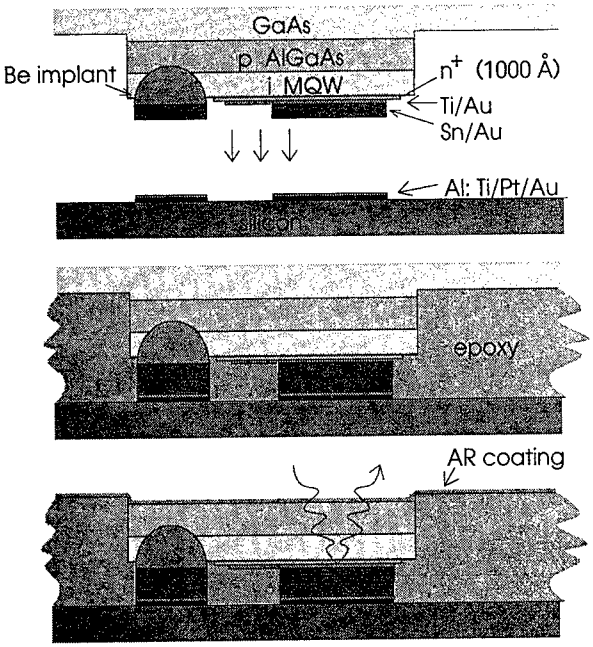


Fig. 1: Three step hybridization process: (1) Fabrication, aligning, and bonding of modulator chip on silicon chip. (2) Flowing epoxy between chips, which is allowed to harden. (3) Removal of GaAs substrate using jet etcher, and deposition of AR coating. The epoxy can be removed after substrate removal as desired.

As mentioned, we are using quantum well modulators as both the input detector and output device. It would be desirable to have different devices for the input and output, in effect a multi-attachment technology. First, within a modulator-output technology, being able to separately optimize the detector and modulator may be beneficial, and possibly necessary as the gate length and supply voltage of CMOS shrinks. Second, this would open the door to surface-emitting lasers for the output device. SEL's do not function well as a detector, and silicon detectors do not operate at the ~ GHz speeds we have already demonstrated, so it

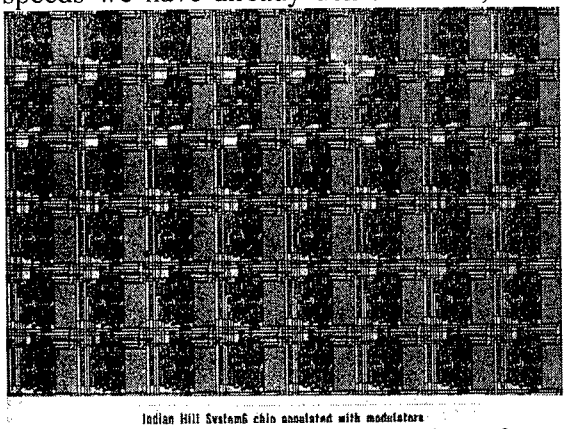


Fig. 2: Photograph of typical section of our OE/VLSI chips. The rectangular devices are the modulators. They are ~ 25x50 μm.

submitted to 1996 IEEE LEOS Smart Pixel Topical Meeting

is necessary to have this multi-attachment technology in order to use SEL's.

Ultimately, a multi-attachment technology will have the different devices interleaved on the surface of the chip in order to have the greatest flexibility of their use and to avoid long wiring traces on the chip. Here we demonstrate the first level of a multi-attachment technology, where two different arrays are attached in a non-interleaving fashion. Since we are just demonstrating the multi-attachment technology, the arrays contain the same device, our standard modulator with 15x15 μm solder pads.

The chip is shown in Fig. 3. The first array is attached using the process of Fig. 1. Since the substrate is removed, the chip can then be subsequently treated as an unhybridized chip, with no worry of mechanical contact with the first GaAs array. Since we are using a thermocompression bonding technology, the first array can withstand subsequent bonding thermal cycles. In an interleaved technology, the epoxy would have to be removed at this point, but since the second array is to the side of the first, we simply rely upon our ability to deliver the epoxy so that it just covers the first array area. So, attaching the second array is a simple matter of repeating the cycle. We apply wax to protect the first array during the removal of the second substrate.

Each array consists of 32x64 devices. Bonding the second array had no detrimental effect on the first array. Through forward biasing the arrays and observing lit diodes, we determined that only one device failed giving a yield of 99.98 %.

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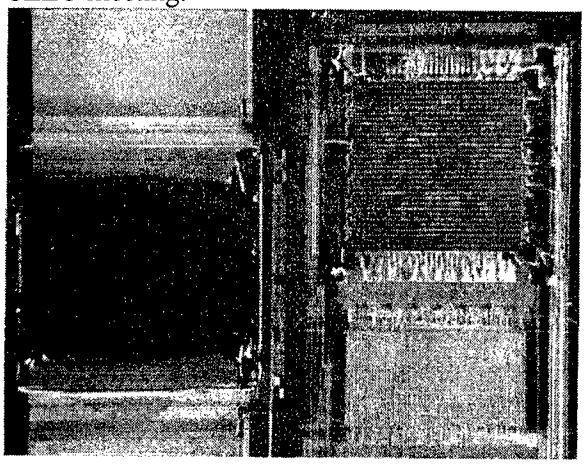


Fig. 3: Photograph of multi-attachment optoelectronic/VLSI chip. The first array is on the right. Some wrinkling of the epoxy occurred due to a process error. The devices were not affected.

2:45pm - 3:00pm
WB4

A S-SEED on CMOS Input/Output Memory Array for Optical Sorting

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1 Introduction

We present a 32×32 optical channel smart pixel array designed for use in an optical computing demonstrator system to numerically sort 1024 10-bit words. The system consists of two S-SEED on CMOS smart pixel arrays, an array of sorting nodes to compare pairs of words and a memory array to store data between comparisons and provide electrical I/O of data [1]. Optical data communication between the devices is provided by differential optical beams using flip-chip bonded InGaAs MQW modulator and receiver arrays. The CMOS memory chip described here consists of a 32×32 array of nodes, each node consisting of a 10-bit static shift register and multiplexing circuitry to select electrical or optical input and output of data. The circuitry is designed to operate at 100 Mbits/s, resulting in an overall data processing rate of 0.1 Tbits/s. Figure 1 shows a block diagram of a memory node.

2 Data I/O

Each node receives and transmits data either electrically or optically, determined by the setting of global select signals. This allows the chip to operate in three modes for different stages of the sorting cycle:

- Electrical Loading - Unsorted data in the form of 1024 10-bit words is input to the array electrically.
- Optical I/O - Optical communication between the Memory Array and the Sorting Node Array via the 32×32 channel S-SEED detectors and modulators.
- Electrical Unloading - Sorted data output electrically.

Electrical load/unload data is supplied via 16 input and 16 output pads at the top and bottom of the chip.

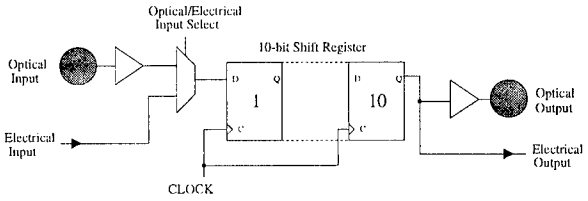


Figure 1 - Memory Node

3 Optical Receiver

The optical receiver consists of a flip-chip solder bump pad (to make electrical contact with

the S-SEED detector) and a transimpedance amplifier (TIA) to convert the analogue photocurrent from the detector into 0 to 5v logic levels [2, 3]. The receiver is optimised to work at a sensitivity of $\pm$ 1.7 μA and an optical data rate of 155Mbits/s. Detailed simulations on the receiver layout indicate a power dissipation of between 4.2 $\pm$ 1.3 mW depending on process variation during fabrication. Figure 2 shows the receiver schematic.

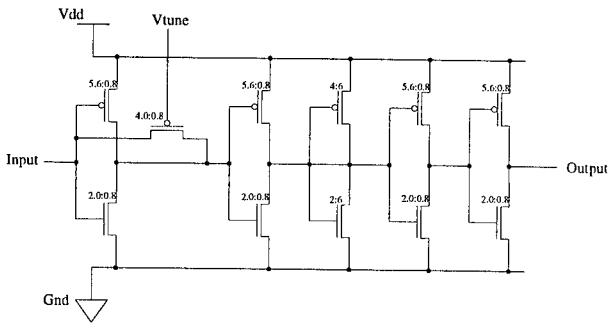


Figure 2 - Receiver Circuit Schematic

Figure 3 shows the receiver layout including clamping diodes, flip-chip solder bump pad and TIA. Approximate area is 120μm $\times$ 60μm.

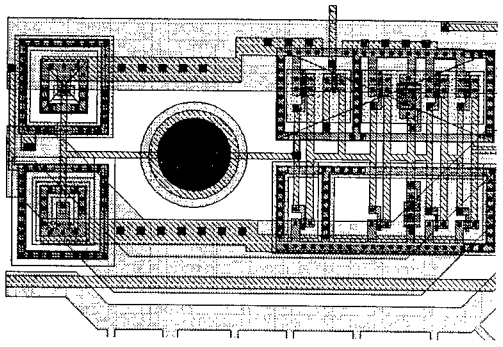


Figure 3 - Receiver Layout

4 Layout Considerations

The layout of the node is designed to isolate the sensitive analogue receiver section from the fast (100 MHz) switching of the digital shift register circuitry. The receivers are supplied with separate power rails and the nmos and pmos transistors are encased in guard rings to minimise stray currents. The clamping diodes on the TIA input are double guard ringed as a prevention against latchup. The nodes are arranged on a 180μm $\times$ 180μm pitch.

The layout of the chip includes TTL-level input pads designed to drive 100 MHz clocking signals onto the array, three sets of power supply pads (for the analogue CMOS circuitry, digital CMOS circuitry and InGaAs biasing rails) and 16 pairs of electrical I/O pads. The InGaAs modulator/detector array is biased through metal tracks at the top and bottom edges of the silicon, electrically contacted through flip-chip connections.

5 Progress

The chip has been designed in a 0.8 μm CMOS process to fit onto a 7mm $\times$ 7mm die and is currently being fabricated at AMS (Austria). We anticipate presenting the results of electrical testing results at the conference.

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3:15pm - 3:30pm
WB5

Smart Pixel Memory Buffer Array with Parallel and Serial Access

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The integration technology of silicon CMOS circuits with optical modulator and receiver based GaAs/AlGaAs MQW modulators [1] available from AT&T has allowed a new generation of smart pixels to be constructed for high speed free-space applications. One potential use is to provide serial electrical access and direct parallel optical access memory. Such devices may find application in data transfer systems as cache between high speed processors and emerging 3-D memories [2].

Fig. 1 shows the layout of the 32-element smart pixel array. The MQW Modulators transceiver array was flip-chip bonded onto a silicon CMOS circuit [1,3], which was fabricated by a part of a multiuser test chip before the CO-OP workshop. The differential optical receiver and modulator windows are approximately 10 x 15 um^2 placed on 125 um center. The circuit is designed to provide storage of 4 pages of 32-bit memory and functions of serial/parallel access at high speed. Fig. 2 shows the circuit design of a smart pixel cell. Each cell consists of a 4-bit shift register as memory unit, the stored bits are capable of recycling within the cell. Information can be written into and read from memory both in sequence electrically and in parallel optically. There is also a programmable on-chip clock to generate clock rates at 38MHz, 76MHz, 154 MHz and 277 MHz.

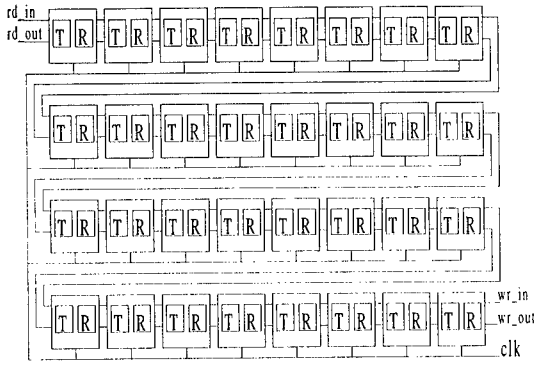


Fig. 1. Layout of 32-stage smart pixel array.

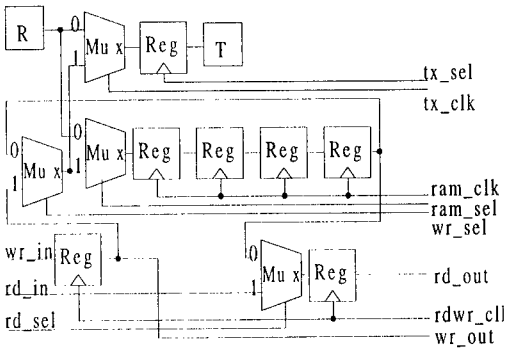


Fig. 2. Circuit design of a smart pixel cell.

A custom probe station [4] was used to enable the introduction of optical probes into the device windows. The Data, Controls and Clock were generated with a programmable pattern generator operating up to 50 MHz. In the experiment, we electrically wrote 4 pages of 32-bit data into memory and operated the chip at various speeds. We tested, both optically and electrically, the functions and performance of the chip. Fig. 3 shows the output response with optical signal modulated at 500 kHz detected by the receiver, with 12 μW optical power per pixel window. High speed testing was limited by the speed of the signal injection laser driver. We observed a modulator contrast of

approximately 2:1 when biased at 9V. To demonstrate operation of the smart pixel at high speed, we activated an on-chip clock. The stored 4-bit pattern, (1,0,1,0) is used to drive the modulator at clock rates of 38MHz, 76MHz, 154 MHz and 277 MHz. Modulator responses measured with a 1-GHz detector at clock rates of 154 MHz and 277 MHz are shown in Fig. 4a and 4b. The electrical power consumption of the chip is summarized in Table 1.

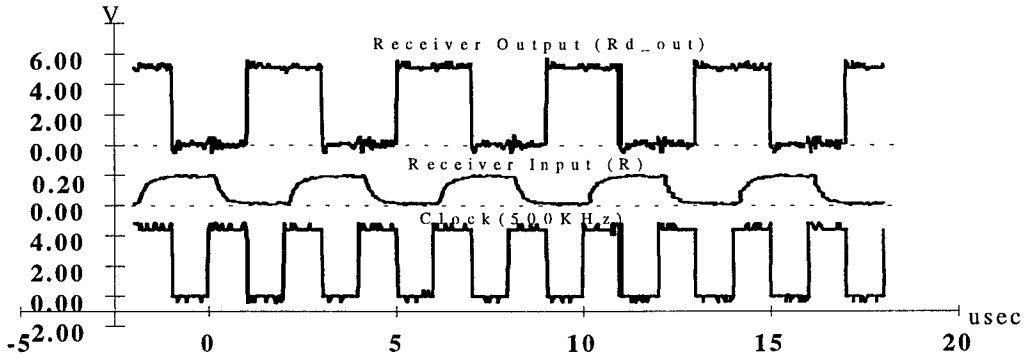


Fig. 3. Digital response of the chip with optical signal of 500 kHz at the receiver.

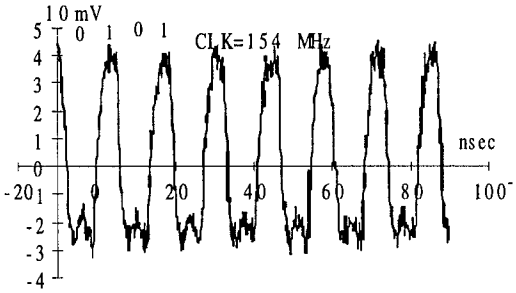


Fig. 4a. Modulator response at rate of 154 MHz.

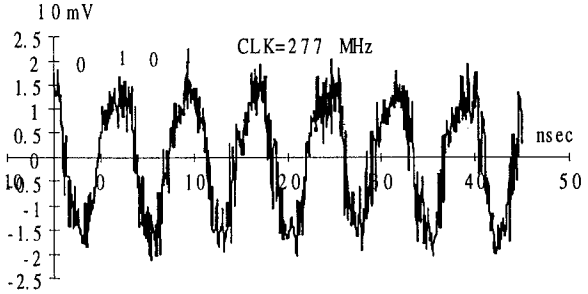


Fig. 4b. Modulator response at rate of 277 MHz.

On-Chip Clock	Power Consumption
38 MHz	0.35W
76 MHz	0.50W
154 MHz	0.65W
277 MHz	1.05W

Table 1. Test results of modulator at high speed .

In summary, an optical memory smart pixel array had been designed and fabricated. The functions and performance of this device had been tested and confirmed. We demonstrated a smart pixel capable of storing 4 pages of 32-bit memory with parallel operation of the smart pixel array at clock rates up to 277 MHz.

The Optivision portion of this research is supported by the Advanced Research Projects Agency of the Department of Defense and was monitored by the Air Force Office of Scientific Research under Contracts No. F49620-92-C-0050 and F49620-95-C-0057. The United States Government is authorized to reproduce and distribute reprints for governmental purposes notwithstanding any copyright notation hereon.

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3:30pm - 3:45pm
WB6

Design and Testing of a Smart Pixel Array for a Four-Stage Optical Backplane Demonstrator

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Introduction: Smart Pixel Arrays (SPA) can offer a large connection density at extremely high data rates for architectures such as switching fabrics and multiprocessor arrays (1). The SPA can take advantage of the surface to surface imaging capability of free space optics and the extremely low impedance loads of micron sized optoelectronics. An optical backplane could in principle provide a generic method with which these architectures could be implemented. In this paper, a dynamically reconfigurable interconnection mesh called the *Hyperplane* (2) was chosen to demonstrate the capabilities of an optical backplane system.

System Architecture: The system in which the SPAs are used constitute a representative portion of an optical backplane. Four printed circuit boards (PCB) are interconnected in a unidirectional ring via a single 4-bit wide channel using a hybrid optical relay (3). Each SPA has a 4-bit wide address associated with each PCB in the backplane and uses a "1-hot encoding" technique for the addressing scheme. This provides broadcast ability to the channel, and allows flexibility in the optical design by allowing for permutations in the bit order due to optical inversions of the relay system.

Logical Design of SPA: To allow complete testability of the initial design, the SPA is composed of only combinational logic. Each smart pixel within the array can be configured to either *inject* electrical data onto the backplane or *extract* electrical data from the backplane. In the extraction state, the smart pixel is also in an optically *transparent* state, allowing data to be retransmitted to the next stage.

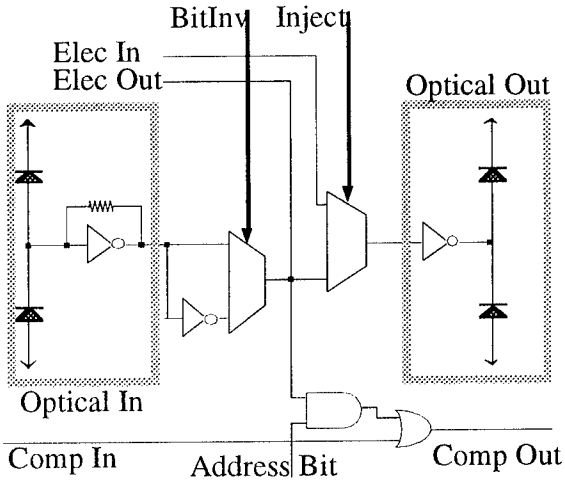


Figure 1: Logical description of Smart Pixel

The smart pixel is composed of dual-rail PiN receivers, and dual-rail MQW transmitters (4). The first multiplexer (MUX) provides a mechanism to correct for optical inversions of the dual-rail beams within the optical path (i.e.: a "high-low" pair of beams passing through a telecentric relay becoming a "low-high" pair of beams). A unique system measurement using this MUX can also be preformed. A *system level ring oscillator* can be produced by

placing all SPAs into a transparent state, and setting an odd number of inversions throughout the entire backplane using these MUXes. A sinusoidal waveform should be observed from the optical beam indicating the maximum frequency the backplane can maintain.

Because the numbers of bond pads along the perimeter of typical silicon chips is at a premium, some of the functions of the SPA have been placed into a 9-bit setup register containing the state of the MUXes, substantially reducing the number of bond pads. The photograph below shows the location of the register and the 4-bit channel of the SPA. Note that the SPA's channel has been centered about an optical axis to allow for an easier optical interconnect.

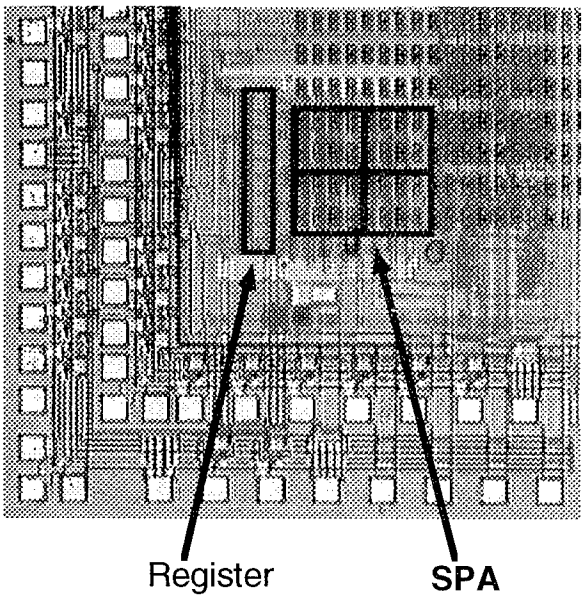


figure 2: Photograph of SPA

Electrical and Optical Testing: Before the SPA chip can be introduced into the backplane, several functional tests were carried out. The design required a set of peripheral electronics to operate the chip. A finite state machine was used to serially load the 9-bit register of the SPA, and to use the 4-bit bidirectional i/o port of the SPA chip effectively, a method of buffering the electrical i/o was implemented.

Initially, the peripheral electronics used a low bandwidth wirewrap board, and the SPA chip itself was placed in a PGA package interconnected with DIN ribbon connectors. The preliminary data using a two beam optical test rig showed that all three states of the chip worked with switching powers as low as 10μW for a bit rate of up to 2Mb/s in the extraction state (the nominal bandwidth limit of the wirewrap board).

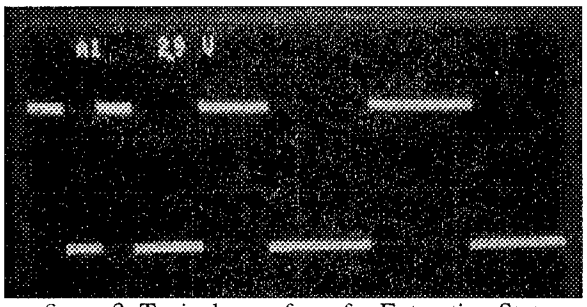


figure 3: Typical waveform for Extraction State

Custom microstrip PCBs are currently being built for both the peripheral electronics and the SPA. These boards will be integrated into the system and will allow the SPA to operate at much higher data rates. More complete measurements of the SPA will then be provided.

Conclusion: The initial characterization of a SPA for an optical backplane has been carried out. Initial measurements of the functionality and the performance have been done, and higher speed measurements will be carried out on custom PCBs. This design will then be incorporated into a four-stage optical backplane demonstrator.

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3:45pm - 4:00pm
WB7

A *HyperPlane* Smart Pixel Array for Packet Based Switching

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Abstract

The operation, simulation, and testing of a 4x2 CMOS-SEED smart pixel array is presented. The smart pixel array discussed implements a HyperPlane based ATM switch.

1. Introduction

A brief review of *HyperPlane*[1,2] packet based switching is presented. Then, details of the designed smart pixel array (SPA) are examined including smart pixel circuitry and transimpedance receiver design. Finally, the results of initial optical and electrical testing are reported and discussed.

2. A *HyperPlane* Based ATM Switch

In this switch, each user is assigned to one of the system printed circuit boards (PCBs). A corresponding SPA is located on each PCB, and each SPA is point-to-point optically connected to the SPAs on adjacent PCBs. Each SPA, and thus each user, is configured at start-up with a unique fabric address. For each node channel in the *HyperPlane*, a fixed transmitted assignment is utilized, so that only one SPA (user) may send packets on that node channel. All other SPAs (users) are configured to receive packets on that node channel.

The process for packet based communication on the *HyperPlane* is described. Following these protocols, transmitted packets traverse the backplane over the optical node channels and are extracted via address recognition at the appropriate SPA for delivery to the user.

The protocol for a sending (n+1)-bit SPA node channel:

1. Packets are injected one word (n bits) at a time.
2. The first word (n bits) of each packet transmission consists of the packet header. This header contains the destination address of the accompanying packet data.
3. Idle data (the all zero string) is sent when no packet is available for transmission.

The protocol for a receiving (n+1)-bit SPA node channel:

1. Packets are extracted one word (n bits) at a time.
2. Packet extraction is initiated when: a) the address within a received packet header matches the corresponding SPA (user) fabric address, and b) the destination user is not busy.
3. Extraction ends after the entire packet is received.
4. At all other times, the SPA node channel is transparent.

3. SPA Implementation

A SPA for implementing a *HyperPlane* based ATM switch has been designed and fabricated using AT&T's CMOS-SEED technology[3]. The 2x4 SPA is comprised of 2 node channels of 4 smart pixels each. Each smart pixel contains 51 transistors (18 logic gates). The SPA and associated control logic totals 825 transistors in an area of approximately 500μm by 1250μm. Differential SEED pairs are used for optical input and output. The SEEDs used have 18μm active areas on a 125μm pitch. Figure 1 shows a photograph of the SPA along with a template of the circuit layout.

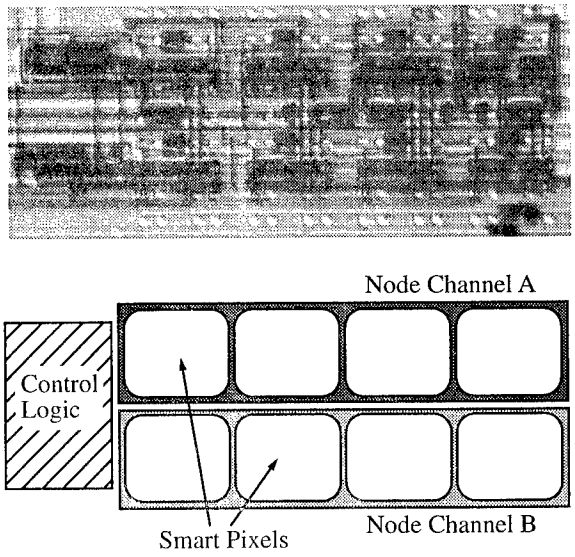


Figure 1. Photograph of SPA and layout template.

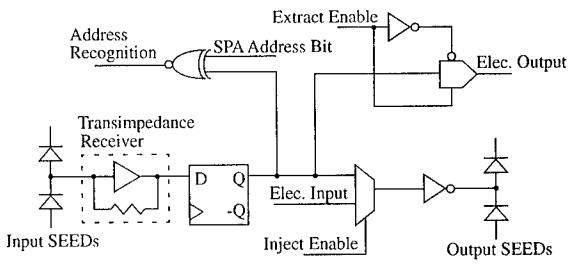


Figure 2. Smart Pixel Schematic.

4. Smart Pixel Circuit Topology

The smart pixel circuitry used in this design in shown in Figure 2. The smart pixel operation is synchronous, so that the optical input data is latched into the pixel by

a global system clock. Once latched, the bit can be operated on in several ways depending on the state of the smart pixel (or more generally, the node channel state). First, the address recognition circuitry, an XNOR gate, compares the data with the appropriate SPA address bit. The result of this comparison is used in conjunction with the address recognition results from other smart pixels in the node channel to validate packet headers and thus begin packet extraction. This validation and extraction setup is handled by the on-chip control logic. Second, once extraction has begun, extract enable will be set high and the optical input data will be extracted to the electrical output. Additionally, the input data will be optically regenerated at the output SEEDs when the smart pixel is in the transparent state. Finally, sending packet data (injection) from the electrical input is possible when inject enable is set high.

5. Transimpedance Optical Receiver

The transimpedance receiver stage used for the optical input is shown in Figure 3. The receiver was designed to operate at low input levels with minimal signal propagation delay. SPICE simulations indicate the propagation delay through the receiver to be less than 2.5ns with ±10μW of differential optical power at the input SEEDs. Additional SPICE characterization found the transimpedance gain (Z_T) to be 92 dB, the bandwidth ($f_{3\text{-}dB}$) to be 205 MHz, and the transimpedance-bandwidth product (TZBW) to be 60 Ω·GHz.

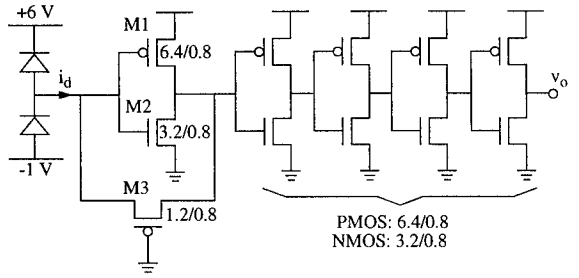


Figure 3. Transimpedance Receiver (W/L in μm).

6. Simulated SPA Performance

The full-custom layout of the chip was performed in Magic, and the subsequent layout extraction was simulated at both the circuit level in SPICE and at the switch level in IRSIM. Important digital delays to minimize for high speed operation include the transparent state delay (from the latch output Q to the output SEEDs) and the extraction delay (from the latch output Q to the electrical package pinout). These were found from IRSIM to be 0.6ns and 3.9ns, respectively. From these and other simulation values, the critical path was identified and was found to limit the system clock frequency to a maximum of 210 MHz. This is well in excess of the targeted system clock frequency of 155 MHz. In addition, the aggregate optical throughput of the SPA is found to be 1.24 Gbps (=155 Mbps per smart pixel * 8 smart pixels).

7. Measured SPA Performance

Electrical functional verification of the SPA was performed using copies of the CMOS-SEED chip which did not have SEEDs flip-chip bonded to their surface. The optical inputs of these chips were simulated by electrically probing onto the flip-chip bond pad sites. All of the functions of the SPA were verified as operating correctly, including: packet injection, address recognition, packet extraction, and transparency. Figure 4 is a photograph of the input and corresponding output trace of an individual smart pixel operating in transparency at 10 Mbps. Higher bit rates could not be demonstrated using this setup due to capacitive loading (>13pF) by the probe.

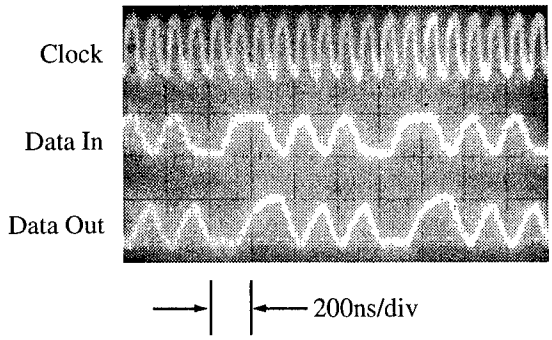


Figure 4. Smart Pixel Transparency.

Optical functional verification of the SPA was performed using a fully bonded version of the CMOS-SEED chip. Two independently adjustable optical beams at 850 nm were used to illuminate a differential SEED pair. Differential optical modulation at the smart pixel optical output was observed by clocking electrical data into the SPA, thus verifying smart pixel injection. Operation of the differential optical inputs and the transimpedance optical receiver at dc was also verified, at differential optical input powers as low as 12.5 μW.

8. Conclusion

Preliminary testing of a *HyperPlane* ATM based switch SPA has been successfully completed. Both the electrical and the optical functions of the chip have been verified. Future testing of this SPA will be focused on high speed verification in a chip-to-chip imaging setup.

9. References

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4:00pm - 4:15pm
WB8

Performance of a Silicon CMOS/VCSEL Smart Pixel for a Recirculating Sorter

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Introduction

Previously we have reported a proposed bitonic recirculating optoelectronic sorter [1]. In the 1996 international topical meeting on optical computing, Sendai Japan, we presented the demonstration of a straight pass sorter [2]. In this paper we present the performance of the smart pixels used to demonstrate the recirculating sorter. The smart pixels were implemented with CMOS circuitry fabricated through the MOSIS foundry, with integrated N Well silicon photodiodes, and wire bonded vertical cavity surface emitting lasers (VCSELs). This testbed was used to verify the functionality of the design and to determine the performance obtainable with this technology.

System Architecture and demonstration.

Similar to our previously proposed reticulating bitonic sorter, [1] the recirculating sorter we present here is comprised of two processing stages. Each stage is comprised of separately mounted chips of CMOS smart pixel and VCSEL arrays. The system functions in a bit parallel fashion, where each smart pixel (C&E module) performs a compare and exchange between the bits of two adjacent words. Each C&E module is comprised of a monolithic integrated silicon detector and receiver circuit, CMOS logic to perform the compare and exchange, and laser drivers to provide the output to the VCSELs.

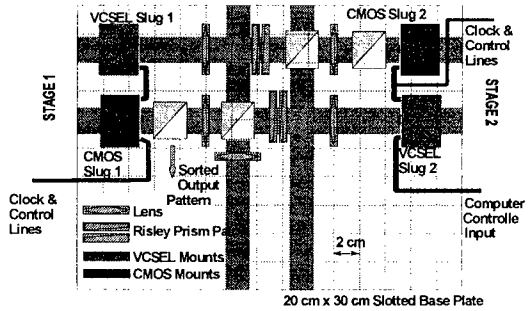


Figure 1. System layout for demonstrated sorter

The system layout is shown in Figure 1. The input to the system is loaded in word parallel, bit parallel fashion. Once the input is loaded into stage 1 then stage 1 performs word comparisons between words W_i and W_{i+1} for i = 1,2,3,..N (where N is the number of words loaded in the sorting stage). The output of stage 1 is straight passed to stage 2 by the VCSELs, and stage 2 performs comparisons between words W_{i+1} and W_{i+2}. The sorting operation is executed by passing the data back and forth between the two stages until N-1 word comparisons have been completed.

For the current demonstration of the recirculating sorter, an array of bit parallel word comparison units have been fabricated using an 0.8 μm CMOS process provided through MOSIS, with the input detectors on 250 μm pitch. A computer interface was used to provide control signals, clocking for the C&E modules and the data signals required to drive the input VCSEL array. After loading the sorter unit, the system clock was cycled manually through the N-1 word comparisons and the status of the output was observed using a video camera. Figure 2 shows the video images of both the input and output patterns for a four word sorting operation. As shown by figure 2b the most significant word has been sorted to the right with the least significant words sorted in ascending order to the left. Thus, verifying the basic functionality of the pixels and system architecture.

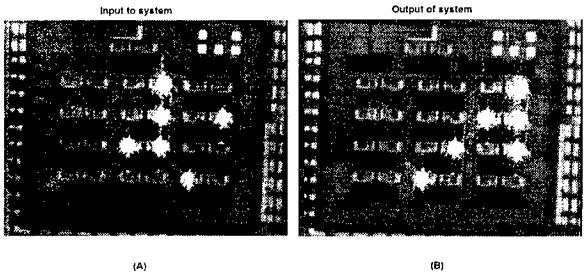


Figure 2. Infrared video images of CMOS processing array and the sorter input and output.

Performance of the smart pixels.

The performance of the demonstrator is limited by the operating speed of the C&E module which in turn depends on the speed of the silicon detector/receiver circuit (D/R circuit), latency of the CMOS circuitry, and speed of the laser drivers. The VCSELs have been shown to operated in the GHz range and thus are not a limiting factor on the operating speed of the demonstrator. Special test structures where designed into the CMOS chips to test the functionality of the design as well as to measure the performance of the detector/receiver circuit and the logic of the C&E module.

The monolithic integrated detector was fabricated using an n-well in the p-substrate to form a p-n junction photodiode with a optical window 40 X 40 μm. The responsivity of the test detector was measured to be 0.286 A/W at 835 nm which requires 130 μW of input power to produce a logic '1'. The receiver circuit is comprised of three inverters to provide the correct voltage to the logic circuit of the C&E module. The (D/R) circuit pulse response is illustrated in Figure 3. The clock rate of the input VCSEL is 200 KHz, with the duty cycle of nearly 50 %. The delay, rise and fall times of the test D/R circuit, shown in Figure 3, are 1.9 μS , 0.9 μS, and 1.24 μS. Using these values the D/R circuit can operate at approximately 250 KHz. It must be realized however that this value is a worst case due to the additional loading and capacitance present in the test circuit.

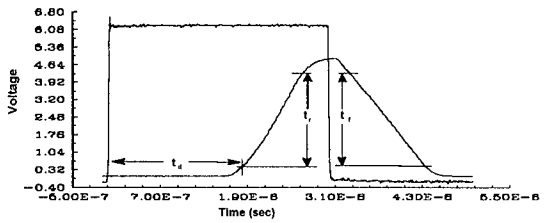


Figure 3. Detector/Receiver circuit pulse response

Also included in the design of the CMOS chip is a test C&E module with electrical inputs and outputs. This logic used for the C&E modules is discussed elsewhere [1,2]. The input to the logic is controlled by rising edge flip-flops, thus the latency of the logic consists of the time from the rising edge of the clock until the time the output is valid. In monitoring the performance of the C&E modules, the module outputs as well as the control lines that are passed between adjacent modules must be observed. The electrical latency of the C&E modules is illustrated in Figure 4. Shown at the bottom of the figure is the clock and input to the C&E module respectively, with the other input kept a constant low. From Figure 4, the rise and fall time for the output of the C&E module were 20 ns. For the control line to the next module the rise and fall time is 200 ns. This is due to the control lines passing through a greater amount of logic Using 200 ns rise and falls time the maximum speed of the electrical CMOS C&E module is 2.5 MHz.

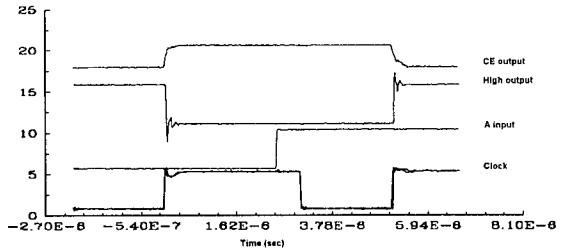


Figure 4. Response of Electrical C&E module.

The final system performance in under test. This test will measure the set up time required for the logic as well as the latency of the total smart pixel, which will include all the components from driver/receiver, CMOS logic, and laser driver.

Conclusion

From the measured performance of the test structures one can see that the speed of the system is limited by the detector/receiver circuit. The CMOS logic could operate at 2.5MHz and the VCSEL at 1GHz, thus the speed of the detector/receiver circuit is definitely limiting the speed of the system.

Acknowledgments

This work was funded partially by NSF/ERC grant EEC94085502, the Optoelectronic Computing Systems Center, the Colorado Advanced Technology Institute, and NSF grant 9408371. The authors would like to thank Sandia National Laboratory for providing the VCSEL arrays.

References

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[2] P. J. Stanko, F. R. Beyette, Jr., E. M. Hayes, R. D. Snyder, S. A. Feld, P. A. Mitkas and C. W. Wilmsen, "An Optoelectronic Recirculating Sorter Based on CMOS/VCSEL Smart Pixel Arrays; Architecture and System Demonstration" 1996 International Topical Meeting on Optical Computing; April 21-25, Sendai, Japan 1996.

4:15pm - 4:30pm
WB9

Smart Pixel Array for Optical Processing of Cervical Smears

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Introduction

The analysis of cytology specimens, particularly pap smears, is a highly repetitive and tedious task for a human operator requiring the examination of approximately 100,000 cells per slide. 90% of all slides examined are normal and in the abnormal slides there are only about 100 suspicious cells on the slide. These working parameters lead to about 20% of all slides being incorrectly diagnosed. These factors make the automation of cervical smear image processing very attractive both to improve consistency and accuracy of analysis. Optoelectronic systems provide the large scale parallel processing required to examine the approximately 8,000 images, 512×484, per pap smear slide. The suspicious cells in a cervical smear can be identified by examining the shape and size of the cell nucleus using optical morphology. A suspicious nucleus is typically circular with a diameter ranging from 12-20 μm as opposed to normal nuclei which range from 6-9 μm. We have constructed an optoelectronic system using a $4f$ correlator which can detect the suspicious nuclei by performing an optically implemented morphological hit/miss transform (HMT) on the image[1]. The hit/miss transform contains two parts, which can be computed with thresholded correlations, thereby allowing implementation of the algorithm in an optical system. First, the hit correlation finds all circular shapes 12 μm or larger, then the miss correlation identifies all circular shapes 20 μm or smaller. By thresholding each image and then ANDing the two results, we have a robust means of identifying suspicious nuclei in a pap smear.

Smart Pixel Array and System Implementation

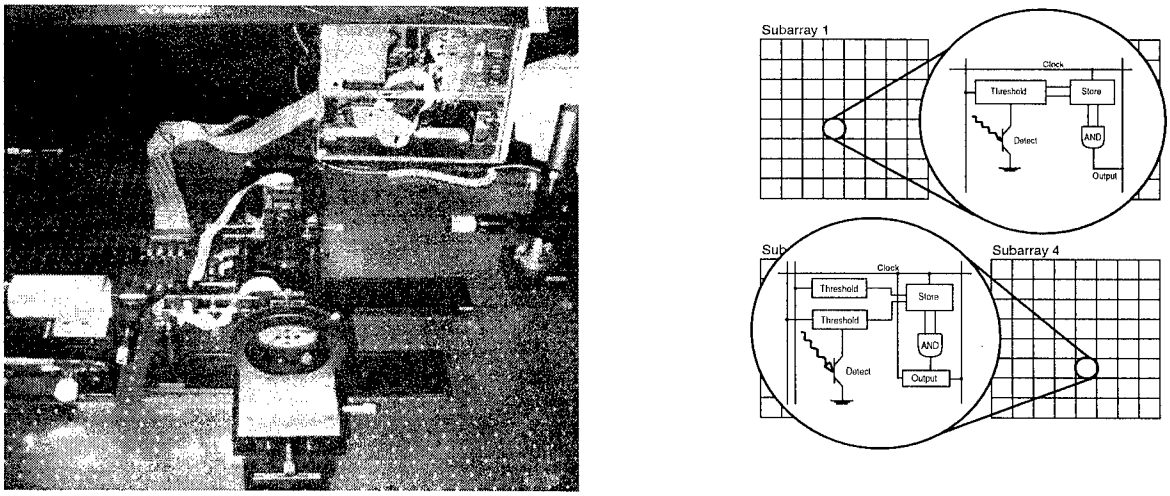
The HMT processor is a $4f$ correlator where the hit and miss convolutions are performed time-sequentially. The two results are acquired at the output, thresholded and logically ANDed to determine the presence of any suspicious cells. The current implementation shown in Figure 1(a) uses EASLMs[2] capable of 4,000 frames/second at the image and filter planes and a CCD camera at the output. This work investigates a smart pixel array to perform the two thresholds and the logical ANDing in place of the CCD camera. With the smart pixel array at the output, we can fully exploit the speed of the diagnostic system.

The first test device consisted of a detector, processing logic, and an output optical modulator. The output of the pixel was an electrode mirror used to drive a liquid crystal cell thereby allowing optical readout. Upon analysis and testing of the first device it was decided to simplify to electronic readout thereby allowing straightforward integration into a second stage electronic image processor for region of interest classification.

In performing the optical to electronic processing, each pixel within the array must threshold each of the two separate correlation images. The first thresholded image must then be stored until the second image is thresholded and then the pixel logically ANDs the results to complete the HMT. Thus the smart pixel performs a time-sequential, individually thresholded, two input AND on optically processed cervical images. The setup where we would include the smart pixel array is shown in Figure 1(a). To implement the necessary functionality, each pixel (refer to Figure 1(b)) has a vertical p-n-p transistor photodetector converting the incident image into a logic voltage by thresholding with respect to globally set values. The voltage is stored until the second image is thresholded and then the logical AND is performed. Readout of the smart pixel can be accomplished by individual pixel data lines or output summing for overall image characterization, either summing the entire chip or sub-sections as desired.

A new test chip has been designed to explore an optical-in to electronic-out scheme. The

chip consist of a 2×2 array of 8×8 sub-arrays using photodetector/logic smart pixels within a MOSIS TinyChip format. Each sub-array utilizes a different pixel type and configuration within the sub-array as well as different means of reading out the pixel data electronically. The areas of concern being investigated within the sub-arrays are: pixel pitch with minimized logic area, varying photodetector sizes, larger logic schemes within the pixel, separate thresholds per correlation image, and position sensitive readout methods. The pixel output drive scheme varies from a global data line whose current is converted into a voltage allowing overall ranking of the image to single pixel-by-pixel readout with further on-chip logic located outside the pixel structure.



(a) (b)

Figure 1: (a) Picture of diagnostic cytology system. The smart pixel array will replace the CCD camera in the lower left corner of the photo. (b) Smart pixel array block diagram and two different pixel expansions. A different pixel design is used in each sub-array of the chip to explore design limitations in pixel area and complexity of included logic. The top pixel shows a minimum geometry pixel designed for small pixel pitch and higher speed. The bottom expansion shows a pixel capable of different hit and miss thresholds.

We will describe the performance of our diagnostic cytology smart pixel array test chip as well as further issues confronting the output of an HMT optical correlator. Particularly important is the light sensitivity of the smart pixel array at 807 nm and this has implications in the design of the chip. Low light intensity operation of the chip's detector portion of the pixel will be examined in relation to reduced intensity from optical losses in the correlator. The various pixel logic implementations for this chip will be reviewed as well as the design tradeoffs associated with their use in optical-to-electronic VLSI circuits. Readout schemes which reduce the data into a more useful form will be reviewed and their performances analyzed, including region of interest position detection for faster diagnosis.

Acknowledgements

NSF Grant EEC-9015128, CATI, and the NIH

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4:30pm - 4:45pm
WB10

Design of Large-scale Photonic Page Buffer ICs

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We have developed a methodology for designing large-scale Photonic Page Buffer (PPB) integrated circuits (ICs) for parallel accessed optical bit-plane data. These ICs have numerous potential applications including photonic switching, non-volatile data storage (buffering), interfacing smart pixel systems with electronic hosts, implementing cache memory for optical memory devices, parallel processing, spatial format conversion, clock rate conversion, optical wavelength conversion, bandwidth smoothing, clock synchronization, and independent flow control for input and output channels.

As shown in figure 1, our methodology places the optical devices directly over their corresponding receiver amplifier and transmitter driver circuits. The resulting two-dimensional array structure, called the photonic interface module, is located in the center of the integrated circuit. The memory circuits are then placed around the photonic interface module as shown in figure 1. With this approach, the electronic and the photonic portions of the IC design can be optimized separately. For example, the memory structure can use existing high-density SRAM circuit layouts. On the other hand, the photonic interface array can be designed to locate the driver/receiver circuitry near the optical devices with which they communicate to achieve optimum performance.

To demonstrate our approach, a sixteen kilobit, 1,008 optical I/O channel, 32 page, 504 bits/page, photonic page buffer IC with random page access capability was designed and fabricated (see figures 2). As demonstrated by electrical testing (figure 3), the IC allows will allow operation of the page buffer at 50Mpages/sec. This 21mm^2 IC was fabricated in 0.8 micron HP26G CMOS technology and integrates 200,000 transistors. Our design is based on the hybrid CMOS-SEED technology that integrates GaAs MQW photodetectors and modulators with high-volume commodity CMOS VLSI processes [1]. It uses the optical device pitch and spacing of an existing GaAs MQW diode mask. The CMOS optical receiver amplifier and transmitter driver circuits and 3-D integration process have previously been demonstrated.

The work described in this paper builds on an earlier effort that produced a 50Mpage/sec, two-kilobit 21,000 transistor photonic page buffer IC [2]. Our approach allows one to build PPB ICs with application specific performance and functionality. Because we leverage on existing silicon memory circuit designs, our approach has excellent scalability potential. Taking into account expected reductions in the feature sizes of CMOS silicon, transistor densities will increase, allowing storage capacities of 256 megabits on a single die. This increase combined with high-bandwidth optical I/O channels, will lead to PPB ICs that have the potential for 10-100 Gbps aggregate throughput with the capability to access random pages of bit-plane data. This represents a one to two orders of magnitude increase in throughput over present state-of-the-art single-chip electronic RAM devices. Compared with commodity electronic RAMs, the PPB performance advantage increases, becoming two to three orders of magnitude higher. Although our results are based on the hybrid CMOS-SEED technology, our methodology is compatible with other emerging smart pixel technologies.

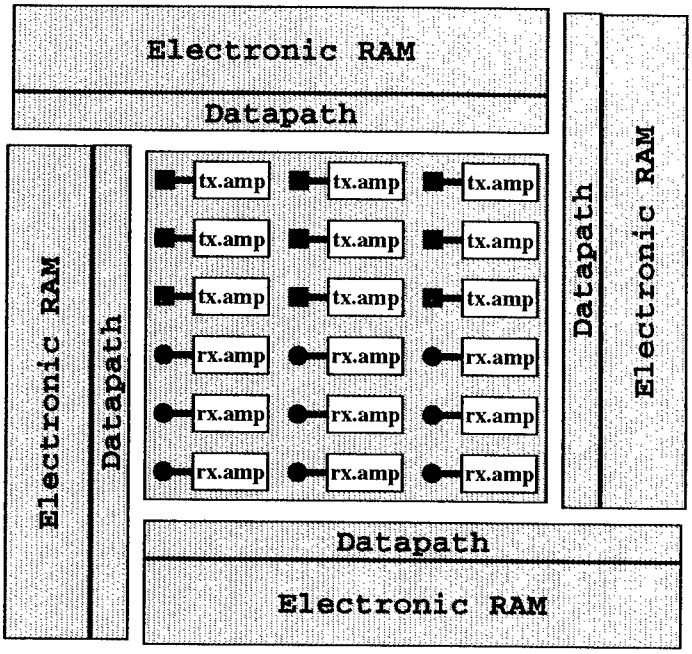


Figure 1: Proposed photonic page buffer IC layout methodology. The photonic interface module, in the center, integrates optical devices and amplifier circuits. Electronic memory and application-specific datapath circuits are placed around the photonic interface module.

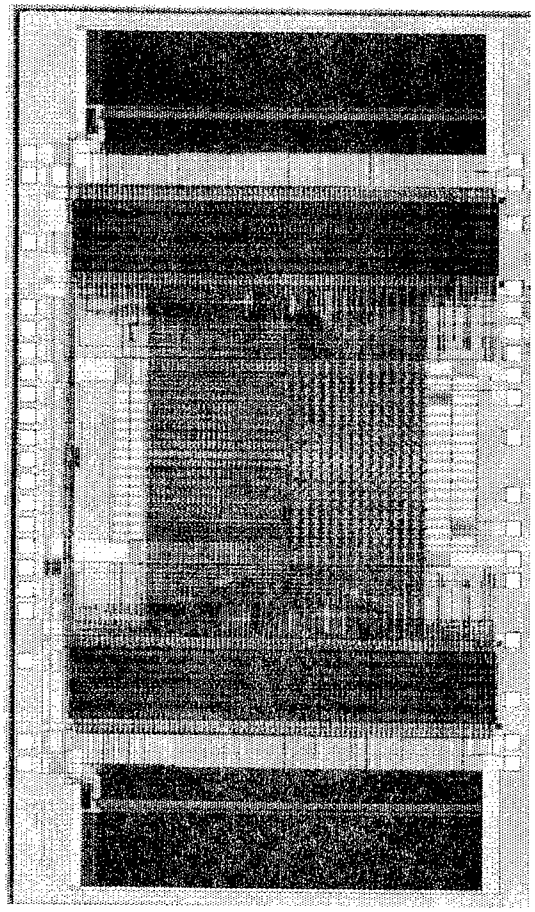


Figure 2: Photograph of 16-Kbit PPB.

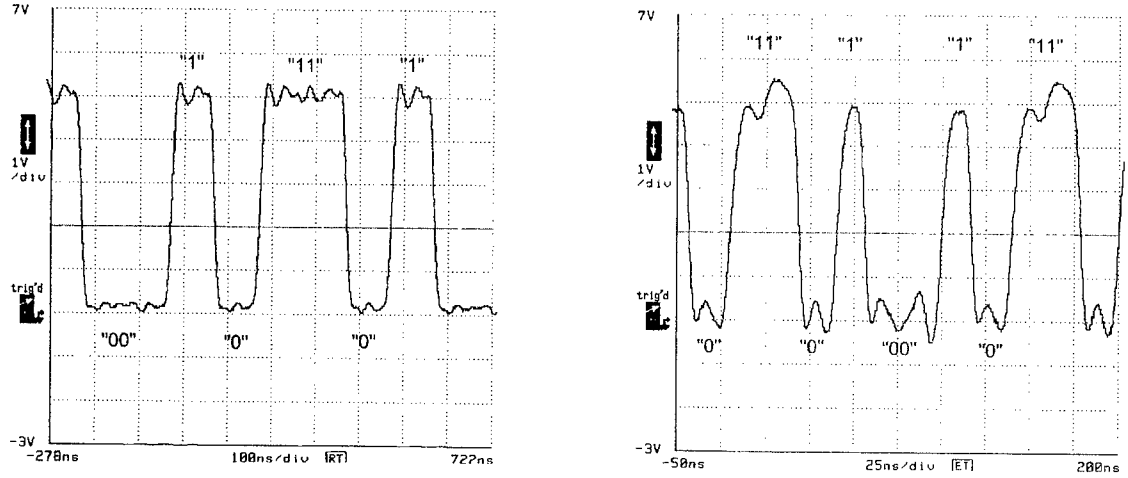


Figure 3: Experimental results showing 10Mbps (left) and 50Mbps (right) 16-Kbit PBB operation.

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4:45pm - 5:00pm

WB11 An Asynchronous Optical Token Smart-Pixel Design Based on Hybrid CMOS-SEED Integration

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Introduction

An essential operation in parallel computer systems is arbitration for mutual exclusive access to shared resources by multiple processing nodes. Often a tradeoff exists between simplicity of the arbitration scheme and its performance. Here, we describe an asynchronous optical token-based arbitration circuit designed and implemented using hybrid CMOS-SEED smart-pixel technology that is both simple and fast. Our asynchronous optical token (asynch_token) scheme is simpler than slot-based arbitration, yet potentially faster as no dedicated slots go unused. Access to a shared resource (e.g., channel or buffer) is gained simply by acquiring an optical token that circulates asynchronously in a Hamiltonian cycle through all nodes in the system. As the token propogates asynchronously with respect to each node's internal clock, high-speed arbitration is possible.

This scheme is particularly attractive in applications where arbitration simplicity is important. For example, mutual exclusive access to a shared *deadlock-free routing lane* can be implemented by our asynch_token smart-pixel circuit for fast network routers based on deadlock recovery [1]. In other work, our asynch_token scheme is applied to a round-robin reservation-based channel control protocol for scheduled (collision-free) access to spatially divided multiple free-space optical channels [2]. Distributed arbitration of the multiple optical channels connecting nodes in the system is implemented by having nodes send channel reservation packets over a shared *control channel* to update their channel reservation table. Our asynch_token scheme implements mutual exclusive access to the shared control channel.

Our circuit design is based on hybrid CMOS-SEED smart-pixel technology recently developed at AT&T [3]. This technology allows the integration of dense surface-normal optical modulators (GaAs-based quantum well optical transmitters and receivers) onto silicon VLSI circuits using flip-chip bonding techniques. Our chip is one of many fabricated under the recent AT&T/ARPA Co-Op Foundary Run. A motivation of this work is to demonstrate the potential viability and usefulness of smart-pixel technology for purposeful multiprocessor interconnect applications.

‡ *The research described in this paper was supported in part by an NFS Research Initiation Award, grant ECS - 9411587.*

Asynch_Token Smart-Pixel Design

Figure 1 is a circuit diagram of the asynch_token logic of the smart-pixel. To ensure latch-in, the optical token is assumed to have a wide pulse width (≈ 2.5 times the node clock period). With this, the token could be present in two adjacent nodes simultaneously. We therefore assume a two pulse-train token (to avoid round-trip delay) and design the circuit to block the propagation of the second pulse on the trailing edge of the first. As the second pulse can be present in at most one node at a time, a node is said to have captured the token upon receiving the second pulse.

The asynch_token logic functions as follows: If the Grab_Token line is not asserted, an Input_Token is propagated directly to the circuit output as an Output_Token for asynchronous transmission to the next node in sequence. Note that the asynchronous token suffers only two gate delays of internal propagation (i.e., < 0.5 *ns*) which is far less than the node's synchronous clock period (i.e., > 5.0 *ns*) for fast operation. When the Grab_Token line is asserted, an Input_Token is captured at this node as the circuit changes state after the first pulse to block the second pulse from propagating to the next node. At this point, the Token_Grabbed line is asserted indicating that this node now has exclusive access to the shared resource. Regeneration and propagation of the optical token occurs through the Regen_Token line. Initial electrical testing indicates that the circuit can be made to operate according to SPICE simulations shown in Figure 2.

The Input_Token line is selectable as an optical signal or an electronic signal through port-programming. Each smart-pixel optical port contains an optical detector (two SEEDs used as a dual-rail mode detector), an optical transmitter (two SEEDs used as a dual-rail modulator) and control logic. Figure 3 illustrates the operation of the optical ports and how they are connected to form an asynch_token channel. A smart-pixel port on *Chip i* detects optical signals from *Chip i-1* modulo *N* (where *N* = number of chips) which become available to *Chip i*'s asynch_token circuitry. *Chip i* uses the *select* line to control the port transmitter which, if the asynch_token logic allows it, either propagates a received optical signal or an electrical *write line* signal on to *Chip i* + 1. The smart-pixel ports of all chips operate in this daisy-chain manner to connect all nodes in a Hamiltonian cycle, forwarding an optical token to all chips in round-robin sequence. Note that this daisy-chain

smart-pixel port programming technique is applicable to broadcast and point-to-point connections as well [2].

Free-Space Optical Imaging Test System

We have developed an optical test system based on AT&T's System4 [4] which implements the daisy-chain channels described above. The optical system is modular in design so that we can replicate it to house several chips. The optical system images an array of optical transmitters on one chip onto an array of optical detectors on a neighboring chip.

Figure 4 shows the module we have designed and are constructing. An array of light beams from one chip enters from the left (polarized vertically) and passes through a patterned mirror located in the image plane of the relay lenses. The light passes through the first beam splitter (BS) and reflects down from the second BS. A Cooke triplet focuses the light beams onto the other chip's detector array. To read out the chip transmitters, a diffractive optical element generates a spot array that is focused onto the modulator windows. The reflected light travels back through the BSs and reflects off the patterned mirror. This reflected light exits the module through the BSs. The exited light is polarized vertically, compatible with the input to the next module.

We plan to cascade up to four optical modules which will interconnect four chips in an area of 23 × 9 cm^2. The optical path between two chips is 26 *cm*, resulting in a delay time of 0.9 *ns* between chips.

Conclusion

This work examines the use of smart-pixel technology to mitigate interconnect problems critical to multiprocessor systems. Our design exploits fast, global communication links offered by free-space optics while providing nontrival logic functionality required by electronic-based network operations. Thus, we show that smart-pixel technology is applicable to multiprocessor interconnection networks.

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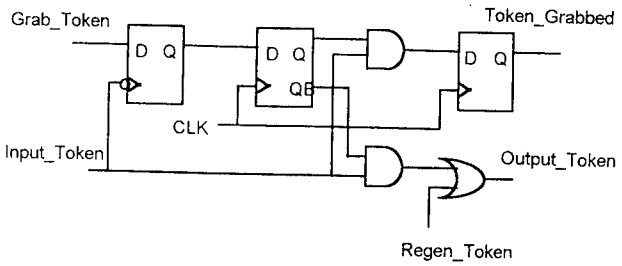


Figure 1. The asynchronous token logic.

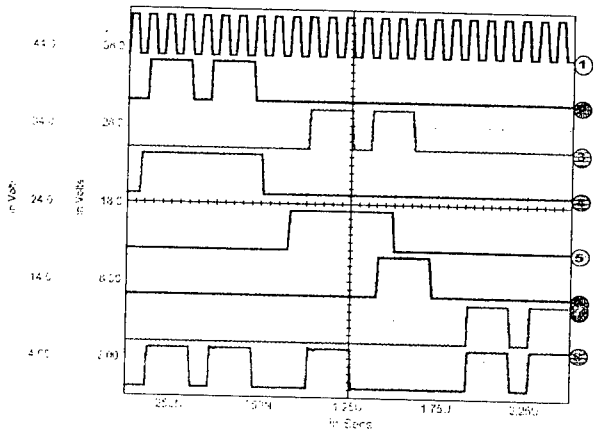


Figure 2. Waveforms from SPICE simulations.

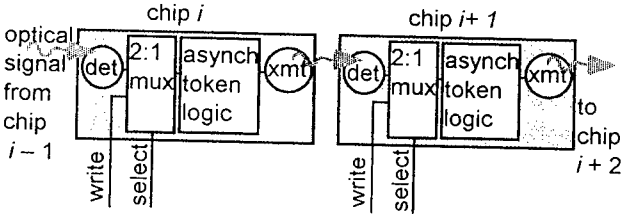


Figure 3. Operation of Smart-pixel Ports.

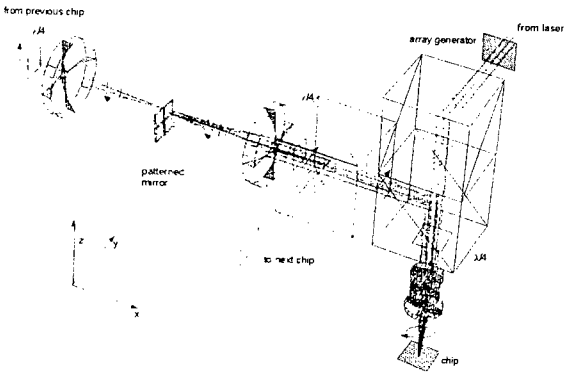


Figure 4. A single module of an optical system for imaging between nodes.

Thursday, August 8, 1996

SESSIONS:

ThA: Smart Pixels Systems Optica, Packaging and Testing

ThB: Smart Pixel Circuits

Smart Pixel Optics and Packaging

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Introduction

The realization of smart pixel optoelectronic systems requires not only high performance OE device arrays and electronic interfaces but also optical imaging or beam routing (for interconnect or image delivery) and system level packaging (for component mounting, thermal control, power delivery, etc.). Recent smart pixel systems have evolved from primitive proof-of-principle experiments to rack-mounted demonstrators with some resemblance to commercial products. However, the commercial viability of these demonstrations is less clear in terms of system performance per unit volume, and especially in terms of system cost projections. For smart pixel systems to become competitive with their all-electronic counterparts will require continued performance advancement, and dramatic reduction in system component and assembly costs. Recent progress has resulted in several OE device and electronic interface technologies approaching commodity status, and the current need for similar advancements in optics and packaging is clear. This talk will review several optical design and system packaging approaches explored in the past and currently under investigation in demonstration systems. To make the jump to a commodity-level smart pixel platform, new components and approaches will be needed and examples of potential useful techniques will be surveyed.

Packaging and Optics Progress

Smart pixel packaging is highly dependent on the choices made for the optical system design and technologies. For example, the use of many diffractive optical surfaces may enable low aberration imaging, but usually results in decreased optical power efficiency, requiring higher power optical sources and increasing the system power dissipation and thermal load. In general, these packages must integrate a variety of technologies to support high speed electrical and optical interconnections while maintaining alignment of the optical systems and high optical power efficiency. Power dissipation and thermal load handling are additional concerns. System (and sub-system) testing another critical, though often overlooked issue, both for demonstration prototypes, and for products, where testing costs can have dramatic impact. Finally, the overall cost, size, and weight of completed system must be minimized to be competitive with ever-advancing electronic technologies.

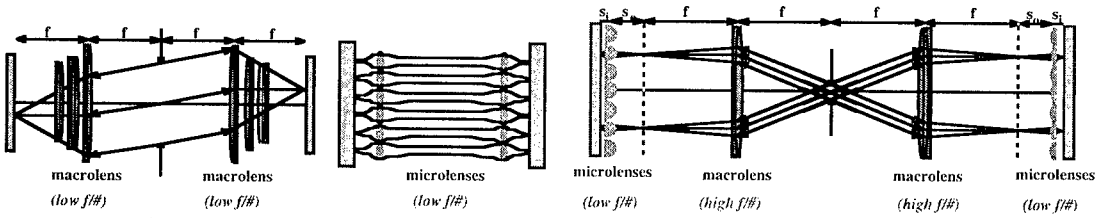


Figure 1. Optical systems: (a) macrolens (b) micro/minilens array (c) hybrid macro/micro lens.

Optical system designs for smart pixel systems[1] may be grouped into either bulk lens[2], micro/mini lens[3,4,5], or hybrid macro-microlens[6,7,8] designs (Fig. 1). These designs may implemented using refractive, diffractive, and/or reflective optics.

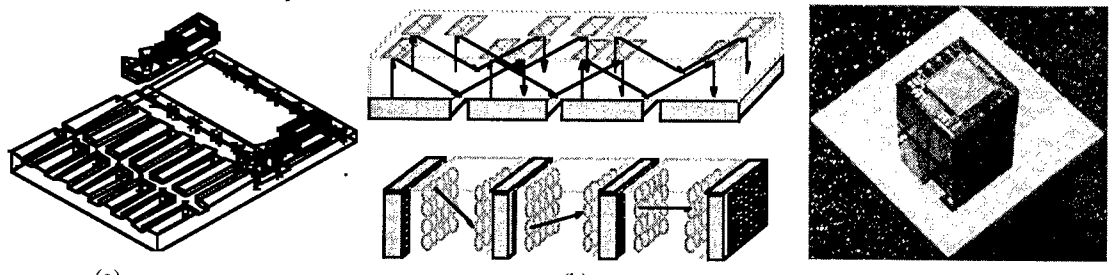


Figure 2. System packaging: (a) custom optical bench (b) stacked and coplanar monolithic optical bench (c) 3-D OE processing stack (Irvine Sensors Corp.).

Packaging for smart pixel systems[1] is commonly either on an "laboratory optical bench"[9] (generally using discrete catalogue optical components and mounts), a "custom optical bench" [10,11,12] (using custom, but still discrete optomechanics) , or a "monolithic optical bench" (in which optics, optomechanics, and optoelectronics are integrated using lithography, adhesives, solder bumps, etc.)[13,14,15] (Fig. 2a,b).

Future Critical Areas

Commodity smart pixel platforms must cost-effectively interface to high performance electronic packages (e.g.- 3-D processing chip and detector array stacking as in Fig. 2c), while maintaining low volume, weight, and power dissipation. Costs may be controlled by designing for high-yield manufacture and simple testing.[16] Promising novel optical techniques include the application of gradient index and diffractive polarization optics.[17,18] Monolithic packaging using silicon waferboard[19,20] and micromachining[21] is under investigation, and these approaches may be able to leverage mass production techniques like injection molding.[22] Standardized and cost-effective interfaces to longer distance optical and electrical interconnections[23] are also for needed successful smart pixel platforms.

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An ATM Switching System Demonstration Using a 40Gb/s Throughput Smart Pixel Optoelectronic VLSI Chip

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A 4096 optical input and 256 optical output chip was used to construct a 155 Mb/s per channel demonstration of an ATM switching fabric. Quickly reconfigurable optoelectronic VLSI permits switching at ATM cell boundaries.

Broadband switching using electronic interconnections has achieved some impressive performance goals but thorough penetration of broadband services will require more aggregate switching capacity than can be achieved economically in an electronic switch. Photonic switching technology offers an opportunity to build large, broadband switching fabrics economically.
In any broadband switching system the per channel bit rates of the signals will be on the order of 155 Mb/s to 2.5 Gb/s. Because of these high bit rates the signals communicated from the periphery of the switch must be sent optically to preserve their fidelity. If the switching fabric were electronic for this switch the signals would need to be converted from photons to electrons, switched through the fabric and converted again from electrons to photons for deliver to the periphery. In this scenario a significant part of the cost is in the O-to-E and E-to-O conversions next to the switching fabric. If the fabric were implemented with a smart pixel technology the O-to-E and E-to-O conversions would be done on the processing chip. Half of the O-to-E and E-to-O conversions of the first scenario could be eliminated in favor of a highly integrated switching chip with on-chip conversions. The construction of optoelectronic VLSI for use in this highly I/O intensive application has been achieved with the fabrication of a hybrid GaAs/GaAlAs on Silicon process used in this system [1,2].
The architecture of the fabric permits a very high level of pipelining and parallel operation. In order to calculate the routes of all potential 256 ATM input packets through the fabric, a partitioning of the fabric was needed. Partitioning (i.e., size of crossbar switches and number of switches per chip) chosen was a compromise between larger crossbars to better satisfy the needs of the architecture and the ability of the optoelectronic circuit to route the 155 Mb/s user data (210 Mb/s including encoding and reconfiguration overhead).
The technique of solder bumping Multiple Quantum Wells (MQWs) on a silicon VLSI circuit permitted the use of highly functional silicon while accessing the chip with amplitude modulated beams of light. In this case, 4352 optical I/O support 16 crossbar switches on a single chip. Each crossbar switch has 16 inputs and 16 outputs. This particular configuration was selected because of the requirements of the modified Growable Packet Switch Architecture [3]. By constructing a quickly reconfigurable distribution fabric from optical components, switch sizes of upwards of 1 Tb/s throughput are possible.

The construction of the demonstration system was achieved with minimal of optical hardware. In the past, the construction of photonic free space fabrics at AT&T relied on the multistage approach with data flowing into the system at the first chip and flowing out of the system at the Nth chip (of an N stage fabric) where intermediate interconnections were optical. In the present experiment there is only one chip. The data is input to the chip where it is switched and the output from the chip flows back into the same fiber bundle from which it was sent. By using a pupil divided system, the data from the fiber bundle was replicated 16 times and imaged onto the receivers of the chip. Thus, in principle, 256 inputs from single mode fibers are replicated 16 times requiring 4096 receivers on the chip. The data from selected receivers is routed electronically on chip to the modulator outputs. CW beams imaged onto the modulators are intensity modulated with the electronic data routed in the switch. The reflected light is imaged into multimode fibers in the fiber bundle.

Shown in Figure 1 is a schematic of the chip with the 16 crossbar switch elements indicated. Each of the switch elements has 256 receivers and 16 output modulators. 16 inputs are optically fanned out using a 16-to-1 grating to illuminate each of the 256 receivers. One of 16 receivers in a column is enabled with an on-chip control memory to send its data to the output modulator. Each output can select any of the available inputs via the control memory. Broadcast is thus possible.

This work was partially sponsored by ARPA under Air Force Rome Laboratories contract F30602-93-C-0166. We would like to thank the authors of [2] for the fabrication of the chip used in this demonstration.

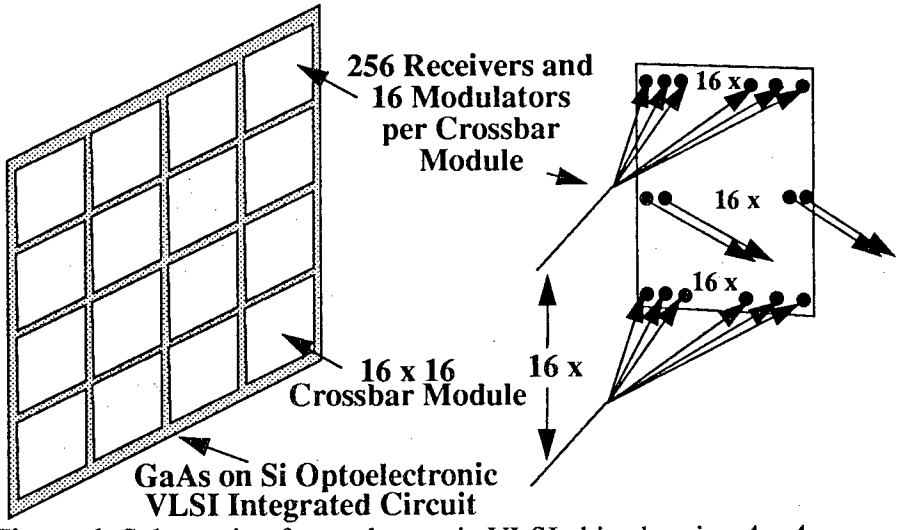


Figure 1. Schematic of optoelectronic VLSI chip showing 4 x 4 array of 16 input, 16 output crossbar switches with optical fanout and electrical fanin to the modulator outputs.

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9:30am - 9:45am
ThA3

Assembly of VCSEL Based Smart Pixel Arrays

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SYSTEM ASSEMBLY

Several applications of VCSEL-based SPA systems are being developed at the Optoelectronic Computing Systems Center (OCSC). These include a crosspoint switch, an FFT processor and an ATM switch. All of these applications are based on 8 x 8 VCSEL and detector arrays forming a bi-directional free space optical interconnect between two planes of processors. Two identical optoelectronic modules are placed at the front and back focal planes of a Fourier transform lens. Each module has 64 smart pixels with optical input (detectors) and output (VCSELs), electrical connections to nearest neighbors and a processing element.

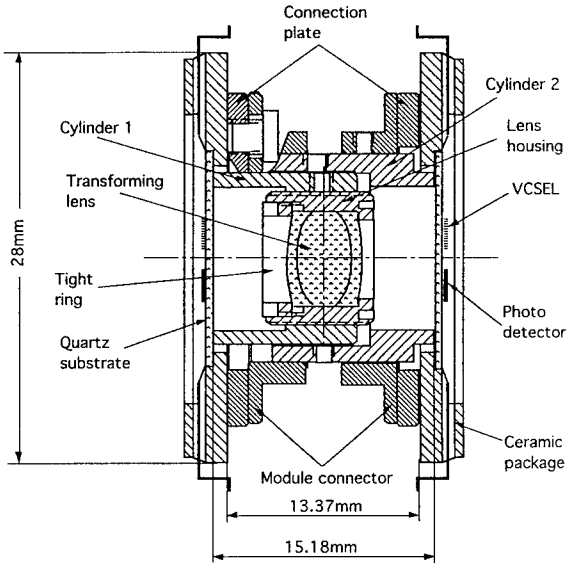


Figure 1. Cross section of Bi-directional 64 Channel Free Space Optical Interconnection Assembly

The SPA multichip module (MCM) is packaged in a conventional electronics chip carrier that has been modified to provide an optical window (see Figure 2). To dissipate the heat generated by the VCSELs, a conductive grease is applied to the back side of the chip and transfers the heat and the common electrical connection to a Silvar heat sink lid. The chip carrier is mounted to a printed circuit board.

An array of microlenses is actively aligned and glued to the glass substrate opposite the VCSEL array to collimate the output of each laser element. The thickness of the substrate is selected to position the lenses at the correct focal length. The collimated beams illuminate individual elements of a computer generated holographic (CGH) array, also actively aligned and glued. The final mechanical assembly is accomplished to align and focus the two SPAs, and the final position is locked into place. See Figure 1 and references [1,2] for additional system descriptions and information.

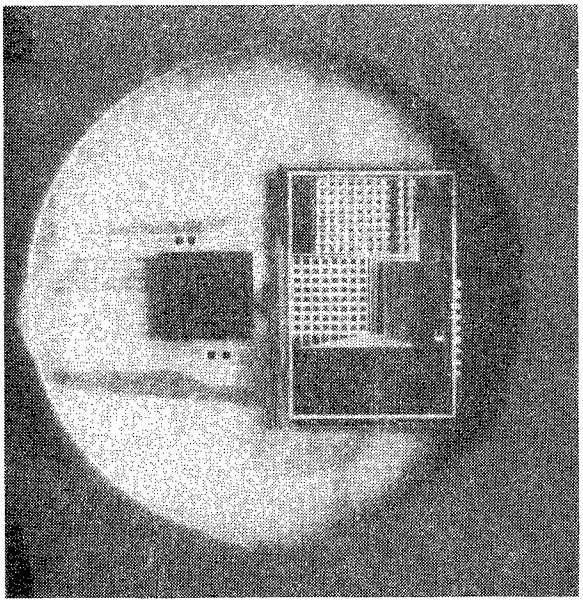


Figure 2. Photo of SPA Package Looking Through the Glass Substrate.

MCM ASSEMBLY

There are currently three methods used for flip-chip assembly of MCMs. These are: solder reflow, solid state bonding and epoxy attachment. The use of conductive epoxies is not feasible due to optical considerations, and the use of contact maintaining epoxy could have detrimental effects on the mechanical stress sensitive VCSEL structure. Soldering, the traditional flip-chip assembly method, has several disadvantages for SPA assembly at this stage of development.

Solder deposition is "dirty" and very difficult for the small contact pads used for flip-chip attachment. It is almost impossible to deposit solder on circuits once the wafer has been diced, as is the case in the prototyping and development of new SPA MCMs. Many of the chips used in prototyping activity are made using standard processes which create contact pads with aluminum metallization. These pads are easy to bond to with gold but are very difficult to solder. The VCSEL is made using a different process on GaAs which readily provides a gold surface contact pad. There is no single step solder process that can be used to solder both the gold pads on the VCSEL and the aluminum pads on the detector/VLSI to the same substrate to form the SPA MCM. A different solderable pad metallization can be specified for the VLSI chip if there is a sufficient quantity ordered, or money available for a special order.

We have chosen to develop thermosonic flip-chip bonding for assembling SPA MCMs. The principles of thermosonic flip-chip bonding are the same as those for conventional ultrasonic wire bonding, except that all of the joints on a chip must be made simultaneously. The use of ultrasonic energy for bonding allows a large reduction in the temperature and assembly force over thermocompression bonding. For flip-chip bonding, joint material must be added to the chips to form the basis for the bonds. In the case of the SPA MCMs, gold bumps (30 μm dia. by 20 μm high) are plated onto the contact pads of the VCSEL array at wafer fabrication, and bumps are formed on the detector array contacts after dicing by use of gold ball (approximately 50 μm dia.) wire bonding. Because of the ability to put the gold joint material on diced chips with a variety of contact pad metallizations and the flexibility and speed of the T/S flip-chip bonding process, this method is ideally suited for rapid prototyping of many MCM assemblies, including the SPAs.

TOLERANCE ANALYSIS

Each step of the assembly of the optical components has a tolerance associated with it. These slight misalignments all contribute to the position of the spot on a given detector. For example the X and Y misalignment between the VCSEL and detector arrays on a substrate can be partially compensated by adjustments at system assembly. However, a rotational displacement between the two chips cannot be corrected. Our initial assemblies had a maximum angular misalignment of 0.6°. System level calculations indicated that for a minimum of 80% signal on the detector, a maximum angular misalignment of 0.36° is allowed. This necessitated a modification to the assembly machine. An analysis of the impacts of the misalignments of each individual component has been presented in [1 & 2]. As additional refinements of the actual misalignments are made, a Monte Carlo analysis will be used to predicted the mislocations of the spots on the detectors.

ACKNOWLEDGMENTS

Vixel Corporation; U.S. Army contract no. DASG60-93-C-0052; NSF award no. EEC-9015128; ARPA/SAIC contract no. N00014-93-C-0185; Colorado Microcircuits; V. Morozov and H.J. Zhou, OCSC, Univ. of Colorado.

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Integrated assembly of smart pixel arrays and fabrication of associated micro-optics

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Smart pixel array (SPA) performance depends on the aggregate yield of circuit fabrication, assembly and packaging. In liquid crystal-based SPAs (e.g., [2]), liquid crystal (LC) cell assembly is the final critical processing step that directly affects the pixel array's optical and electrical characteristics, including contrast ratio and undesirable photocurrents from scattering. Present LC cell assembly techniques, such as microsphere spacer application and screen printing glue are not conducive to the assembly of miniature SPAs, as they result in occlusions and assembly difficulties. Another technique for increasing the optical performance of SPAs is the integration of microlenses. Integrating two dimensional arrays of microlenses with a SPA will reduce the amount of chip area required for individual pixel electrodes; this extra chip area can be used to increase the functionality of the pixel cell (e.g., local processing, buffering).

In this paper, we describe two SPA applications of photopolymers: integrated LC cell assembly and micro-optics fabrication. In our experiments, we utilize benzocyclobutene (BCB) organic resins (or Cyclotene^{TM}), a class of thermosetting polymers developed at the Dow Chemical Company for electronic thin film coating applications. The planarization properties, refractive index (n=1.56) and high optical transmission (>90%) of BCB resins lend themselves well to our applications. Recent display applications of BCB polymers include planarization of flatpanels [3] and miniature displays [4].

Integrated liquid crystal cell assembly

Our approach to LC-based SPA assembly is to utilize a photopolymer for LC cell definition, gapping and edge seal in lieu of microspheres or evaporated spacers and UV-curable or thermal epoxy. As shown in Figure 1(a), we first deposit a LC alignment layer on one or both substrates (depending on circuit passivation). Next, we spin coat a layer of photopolymer (e.g., photo-BCB) on either the top (shown) or bottom substrate to give the desired cell gap (d) after cure. We pattern the photopolymer using the desired cell layout and spacer grid (not shown). After patterning, we develop and post-bake the photopolymer, align and attach the top and bottom substrates, and cure the entire assembly.

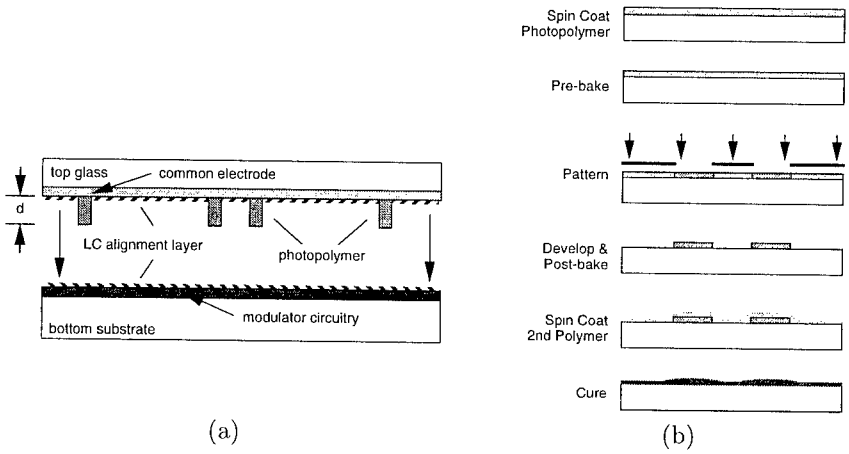


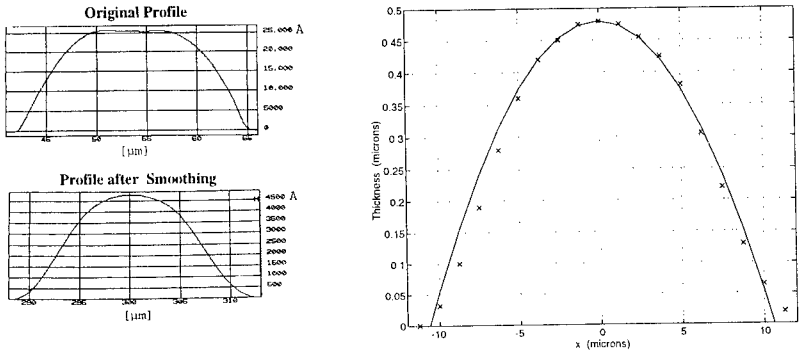
Figure 1: Photopolymer applications for SPAs: (a) photo-definable liquid crystal cell, gap control and edge seal; (b) single-mask etchless micro-optics fabrication.

We have demonstrated our approach using photo-BCB with a .7" diameter cell filled with a nematic LC (E7) and gapped to .9 μm. For a LC alignment layer, we obliquely evaporated 200 Å of SiO_x at 30° to provide LC anchoring with zero pretilt [1]. The test cell demonstrates excellent compatibility between the SiO_x alignment layer and photo-BCB chemical and thermal processing ($T_{cure} \approx 200 - 250°C$). The contrast ratio of the test cell was 30:1 with an optical throughput of 85% and a LC relaxation time of 800 μsec.

[1] http://www-ocs.colorado.edu/~pkazlas/Home.html

Micro-optics fabrication

Figure 1(b) depicts a simple etchless single-mask micro-optics fabrication process using spin coated photopolymers. We first spin coat a photopolymer (e.g., photo-BCB) and define a binary pattern using a single lithographic mask. The resulting pattern is then developed and post-baked in the traditional way. However, we then spin coat a second polymer layer (e.g. non-photodefinable BCB or simply BCB) directly on top of the existing binary structure. Unlike the fabrication of microlenses by melting photoresist, here we rely on the planarization properties of the spin coated film to provide us with smooth continuous profiles. By adjusting the relative thickness of the second "smoothing" layer with respect to the height of the first layer, we can tune the range of coating from conformal mapping to complete planarization; thinner films conform to structures, while thicker films tend to planarize structures. Note that our approach can also be used to fabricate or to enhance the efficiency of diffraction gratings and general aspheres.



(a) (b)

Figure 2: Micro-optics fabrication: (a) original and resulting profiles after smoothing; (b) a comparison between the actual resulting profile in (a) with an ideal spherical profile (x : measured data; – : ideal spherical profile).

As an experiment, we patterned a Newport RES-1 resolution target on a 2.5 μm thick layer of photo-BCB (before cure). We then deposited a 1 μm layer of BCB on top of the patterned structure. The entire sample was then cured at 225°C for two hours in a nitrogen atmosphere. As an example, the top portion of Figure 2(a) depicts the original binary structure patterned from a single resolution bar ($\approx$ 12 μm width), while the bottom portion depicts the resulting profile after applying a second thin coat of polymer (note the change in scales). To analyze this result, we fitted a spherical surface to our profilometer data. The focal length of a thin plano-convex lens is given by $f \approx R/(n-1)$, where R is the radius of curvature and n=1.56 (refractive index of BCB). From Figure 2(b), we approximate R=118 μm and from Figure 2(a), the diameter equal to 21 μm. This results in a lens with a focal length of 210 μm and an f-number of 10. The RMS thickness error within a diameter of 21 μm is 0.019 μm.

Conclusions

We have presented two applications of photopolymers that will potentially increase the yield and performance of SPAs. Integrated assembly of liquid crystal cells will improve both manufacturing and optical throughput of LC-based SPAs, while single-mask fabrication of micro-optics will simplify fabrication and enhance the performance of emitter-based SPAs. In LC cell assembly, we are presently verifying the compatibility of our LC cell assembly process with various alignment and LC materials. In micro-optics fabrication, we are modeling the planarization behavior for various optical-grade polymers to optimize our design methodology and enhance fabrication yield.

We acknowledge Miller Schuck and Yoriko Morita for their assistance in initial polymer experiments and SiO_x evaporation, respectively. We also acknowledge Mike Radler for his suggestions on BCB processing.

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10:30am - 10:45am
ThA5

Packaging of two-dimensional smart pixel arrays

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Introduction

The optomechanical and electronic packaging of two-dimensional smart pixel arrays present a series of constraints that complicate the application of standard electrical packaging approaches in system applications. Through the construction of demonstrator systems, we have designed, fabricated, and implemented smart pixel packaging which uniquely addresses the critical issues associated with successfully integrating two-dimensional optoelectronic device arrays into systems. In order to take full advantage of this class of optoelectronics, aggressive packaging solutions which use both existing and new microelectronic packaging technologies have been employed. Key system design considerations such as electrical bandwidth and connectivity, thermal management, and optical alignability have played a role in the choice of packaging solution. In this paper, we will describe smart pixel packaging designed, modelled, fabricated and demonstrated for board-to-board optical interconnect applications.

Standard packaging techniques

A standard approach to electronic packaging of a smart pixel array could include the use of a chip carrier mounted on a printed circuit board that is interfaced to support electronics. This chip carrier can be either a through-hole carrier or a surface mount device (SMD) carrier.

Through-hole carriers include pin grid arrays (PGAs) and dual in-line packages (DIPs). These are flexible and reusable carriers that are socketable, thus allowing for testability and modularity.

The SMDs include leaded chip carriers, leadless chip carriers, ball-grid arrays, land grid arrays and quad flat packs. These are all fast carriers with relatively high I/O connectivity (for example, a BGA or LGA package could support up to 600 I/O at 3–5 GHz [1]).

For smart-pixel arrays, however, an alternate approach may be attempted, such that the use of an explicit chip-carrier in the system becomes unnecessary or impossible. When the optical system has I/O counts and volume constraints that prohibit the use of standard packages, the smart pixel array may be mounted directly on the board, employing the alternative approach of chip-on-board or MCM-L mounting [2].

Chip-on-board packaging

In the system demonstrator to be completed by the McGill Photonic Systems Group, a four-stage Hybrid-CMOS modulator-based free-space optical link is the objective [3].

To accomplish the packaging task, the following packaging hierarchy and constraints were proposed:

1. The Hybrid-CMOS smart pixel arrays should reside on a small daughterboard to prevent interference with the rest of the optomechanics. The small daughterboard should preserve the system's bandwidth and be highly maneuverable for optical alignment. The chip's mount should be low profile so as not to interfere with closely-spaced lenslet arrays.
2. This daughterboard should be connected to the next level of hierarchy by a high-speed connector that provides a large number of I/O pins and can mechanically isolate the daughterboard from other electrical components.
3. A motherboard should hold the support electronics for the smart pixel, as well as connectivity to the outside world and any application-specific electronics.

The resulting daughterboard (Fig. 1) follows an impedance controlled microstrip design with 4 layers of copper interspersed with FR-4. The two inner layers are planes of copper to support ground and power, while the outer layers contain traces for signal interconnec-

Figure 1: Daughterboard

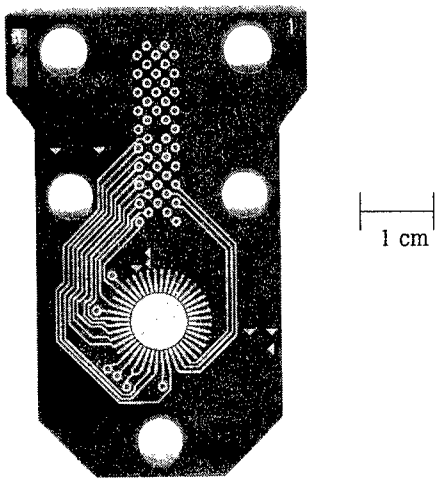
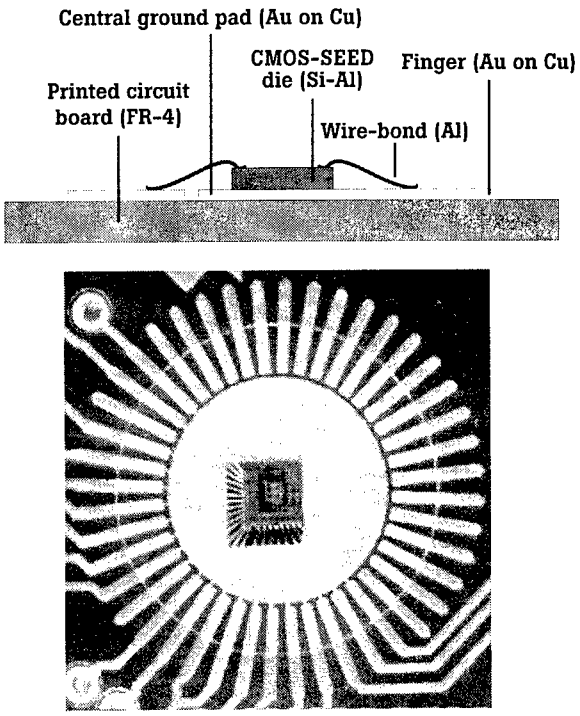


Figure 2: Chip-on-board mounting



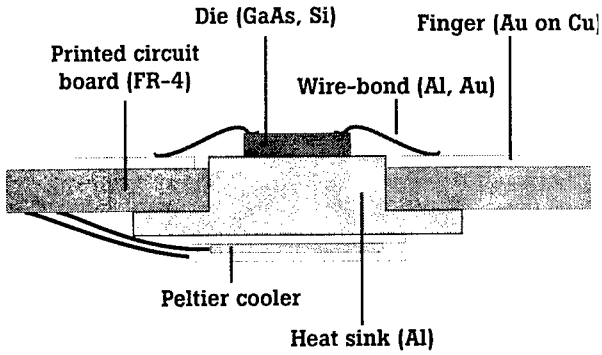
tion. By fixing the thickness of the dielectric (FR-4) between signal and ground planes, as well as the thickness of the outer signal traces and their width, we have designed a microstrip transmission line with a nominal characteristic impedance of 50 Ω.

A prototype of the daughterboard was fabricated to verify the system design, and the measured -3 dB bandwidth was found to be greater than 1.5 GHz. In addition to providing a first and second level package for the chip, this daughterboard supports a single high-speed AMP™ microstrip connector for connection to the motherboard via a flexible, impedance-controlled (50 Ω) ribbon. In this way, optical alignment of the photonic interconnect fabric is decoupled from the support electronics, while a reasonably high number of interconnects (40) is maintained at a bandwidth of more than 1 GHz per connection [4].

Due to space and connectivity constraints imposed by our optical design, we found it impossible to exploit any of the standard chip carriers described previously. With this in mind we chose to mount the Hybrid-CMOS chip directly on the daughterboard using a MCM-L arrangement (chip-on-board) [2].

The daughterboard provides for chip-on-board mounting with a central, round die-attachment pad surrounded by 44 bond fingers. All exposed copper is plated with immersion gold to allow for direct wirebonding.

Figure 3: Future packaging



One of the constraints imposed by the system was the positional tolerance of the chip. With this in mind, we have devised an alignment, bonding and gluing rig ("puck") for the chip attachment to daughterboard [5]. The daughterboard is first attached to the circular aluminum "puck" by means of mounting screws. A Teflon™ spacer is then located on the daughterboard by means of two mounting rods. This L-shaped spacer is designed to provide a stop to chip-travel during placement of the chip die, thereby providing an effective alignment mechanism. The entire "puck" can be moved to a heating unit to set the epoxy and then wirebonded on a height-adjustable, stable base. The anticipated die to daughterboard positional accuracy will be ± 100 μm.

Discussion

The packaging used in this system can be expanded and improved upon to suit future application needs. We have addressed many of the issues and concerns facing a system designer when confronted with the task of packaging a two-dimensional array of smart pixels, but others still require attention. For example, thermal management is a key system parameter which must be addressed in order to build and package large smart pixel arrays for system applications. Figure 3 shows the schematic of a package incorporating chip-on-board technology and cooling via both a passive heat-sink and a Peltier cooler. This, or other similar solutions will be required in future system applications.

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10:45am - 11:00am
ThA6

Alignment Tolerant Smart Pixels

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Summary

A Free-Space multi-board optical backplane offers a potential aggregate throughput that exceeds that of a conventional system by two orders of magnitude [1,2]. To realize this potential, a *low-cost* and *reliable* method to establish the optical connectivity is required. The optomechanics of free-space systems can position an array with micron precision and maintain this precision for months with a rigid structure [3]. In a free-space optical backplane however, the arrays must be removable for repairs. The re-insertion time needs to be short to minimize the data loss in an operating system (assuming the repairs must be done on the live backplane). These requirements make micron precision difficult (costly) if not impossible to achieve and maintain.

Fortunately, the optomechanics does not need to have micron precision for the system to operate. The alignment tolerance can be relaxed with oversized detectors and arrays used in conjunction with microlens concentrators. Oversized detectors are connected to current-mode receivers [4] the sensitivity and bandwidth of which are independent of the detector size. The alignment tolerance can approach the pixel pitch when microlens concentrators are used. To exceed this tolerance, we use an oversized smart pixel array that reroutes electrically the misaligned optical data to the correct channel. The rerouter constitutes an overhead but as we demonstrate in this paper, it can be simple and compact. With this technique the alignment tolerance can be increased to an integer number of the pixel pitch.

We use GaAs QCSE/PIN devices solder bonded onto CMOS electronic to implement a 3X3 channel array in the middle of a 5X5 array of detectors [5]. The photomicrograph of the chip is shown in Figure 1. The array can be scaled up to a NXN detectors array in a (N+2)X(N+2) oversized array. The NXN array can be in 9 different positions within the oversized array i.e. N, NW, NE, S, SW, SE, E, W misaligned and aligned position (see Figure 2). Four detectors (alignment detectors) are used to determine the position of the NXN array. We can use four detectors of the (N+2)X(N+2) array or four additional beams and detectors that are outside the oversized array. In the former option the optical data must be preceded in time by DC beams. This requires the use of a clock or control signal to delineate two distinct periods. The digital outputs of the four alignment detectors are decoded to obtain the control bits that open, for every pixel, one of nine transmission gates that exist between each pixel and its electrical output (corresponding to the align state); its N, NW, NE, S, SW, SE, E, W neighbors. Therefore the misaligned optical data are rerouted to the correct pixel and electrical pin-out. The number of control lines can be reduced to four if we use a multiplexer in each pixel that selects the proper datapaths. The four alignment detectors outputs are decoded to generate the select bits of the multiplexers.

The detectors are placed in a regular square array pitched at 250 μm. We also considered a hexagonal layout. This has the advantage that each detector has only 6 instead of 8 neighbors hence decreasing the number of rerouting lines and the number of control lines, and by the same token the number of select bits is reduced from 4 to 3 if muxes are used.

If the beams fall between the detectors, the scheme just outlined does not work. One possible solution is to use redundancy. We replicate the arrays two or three times, and layout the detectors in such a way that when beams fall between detectors of one array, the signal falls in the middle of detectors of a replicated array. A winner-take-all (WTA) circuit is used to determine which detector output is valid. Only one receiver in all arrays is powered to minimize power consumption. The size and shape of the detectors should be designed in such a way that crosstalk does not cause faulty operation. A trivial example of this to use 2 arrays: one a square array composed of 4 square

detectors with a signal beam incident, in the case of no misalignment, in the center of the square such that each detector is equally illuminated (in fact, it is likely that no light would be detected in this case since the beam would fall on inactive material); the other a cross composed of 5 square detectors with a different beam (with the same signal incident) on the center pixel in the case of no misalignment. In that case, the signal used would come from the detector in the center of the cross. If there is a misalignment: N, NE, E, SE, S, SW, W, NW, one of the other 8 detectors would be ideally placed. However, any arrangement with n=2 has a problem; there is always the remote possibility that a misalignment will occur which will cause both beams to fall between detectors. There are 4 such locations in the arrangement described above. In that circumstance, the signal from an additional array would be required.

In this talk we will present experimental results we will obtain which will demonstrate the operation of this scheme.

In conclusion, we have implemented an oversized array that has an increased alignment tolerance. We have also introduced the concept and a possible implementation of redundancy to increase the alignment tolerance of the smart pixel.

Acknowledgments

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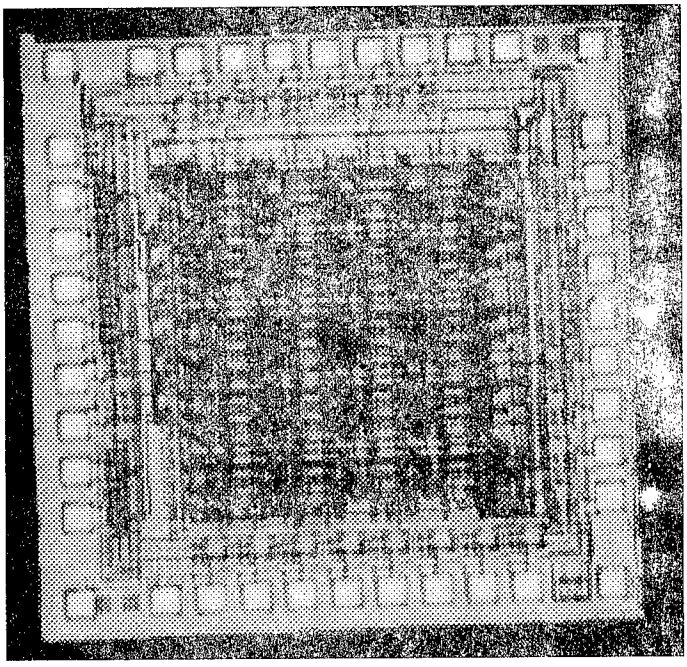


Figure 1: Photomicrograph of the alignment tolerant array

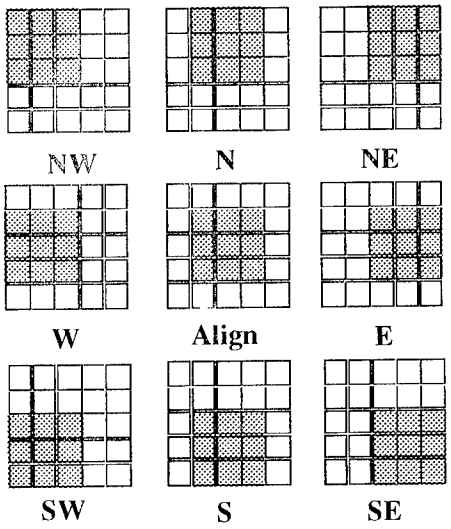


Figure 2: Alignment states.

Smart Pixel I/O Layout Constraints for a Free-Space Parallel Shuffle Module

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Abstract - A design methodology for the layout of smart pixel optical I/O, depending on physical smart pixel and optomechanical constraints, is developed. The results are utilized in several freespace optical interconnection modules under current development.

Motivation - In a multichip module (MCM) to MCM shuffle free space optical interconnection (FSOI), it is often desirable to implement many simultaneous parallel and interleaved interconnections [1]. This leads to a clustering of parallel links between chips. The area of the OEICs which are utilized for this cluster of parallel links and the spacing between these areas are constrained by the optical system. Limitations on how close two emitters can be placed are determined by the power dissipation and crosstalk of the optical system. These design constraints have a great impact on the layout of optical I/O within a smart pixel design.

Approach - A one lens per chip configuration is assumed. The opto-mechanical parameters constrain the placement of the optical I/O in the OE backplane of the FSOI module. In the OE I/O design process there are three key constraints that must be considered. They stem from geometric arguments and the density limits due to heat dissipation within an OEIC. The design constraints relate lens parameters to possible OE I/O spacing and cluster spacing in the FSOI module.

The first constraint on the placement of OE I/O in the backplane stems from the active lens aperture of the transmitting lens. The OEICs in the corner of the chip array will have OE I/O sites farthest off-axis of their transmitting lens. The I/O site farthest from this lens's center must be within the active lens aperture. In fact, the assumed square array of I/O must be completely circumscribed by the circular lens aperture as shown in Figure 1-a.

The second constraint insures that all emitters in a single cluster are captured by the *receiving* lens and that the receiving lens array spacing does not require the physical overlapping of lenses. The third constraint is the minimum spacing between I/O sites. This would come directly from the physical limitations, e.g., power density limitations on the emitter spacing. For our prototype, a typical value for minimum VCSEL spacing of 100 μm is used.

Figure 1-a depicts the first geometrical constraint. The farthest off-axis emitter of the transmitting lens must fall within the active aperture of this lens. Therefore, the distance to the edge of the active lens aperture, ($f/2f_{\#}$) must be greater than the position of the farthest emitter from the lens axis:

$$\frac{f}{2\sqrt{2}f_{\#}} \geq D_c(N_c-1)+\frac{D_e(N_e-1)}{2} \qquad (1)$$

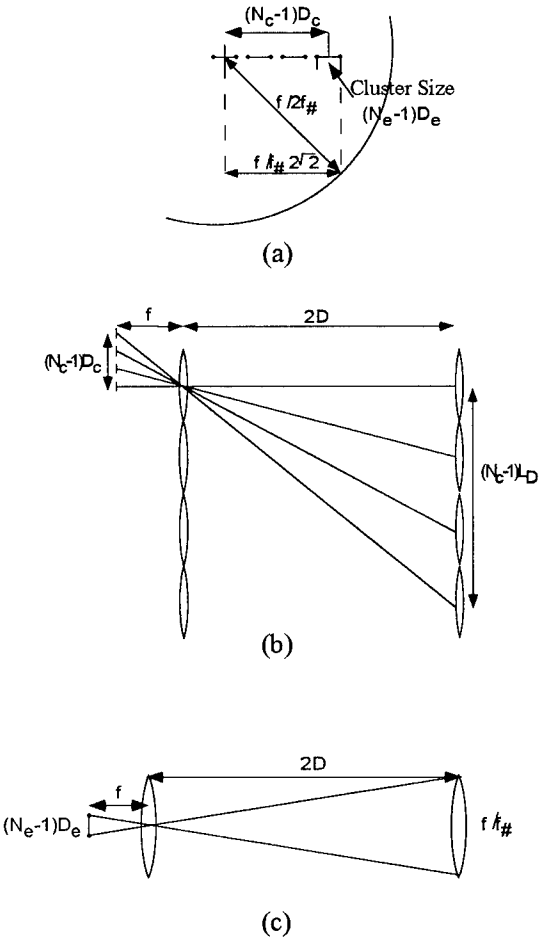


Figure 1. 1-a shows a top view of the lens and I/O geometry used in deriving the upper bound on the cluster spacing as a function of emitter spacing. 1-b and 1-c depict the geometry used to derive the lower bound on cluster spacing as a function of emitter spacing. 1-b shows that the light emitted by the individual clusters must be captured by their respective receiving lenses, which cannot overlap, and 1-c depicts the fact that the transmitted cluster must fall within the active aperture of its receiving lens.

where f is the focal length of the lens, D_c is the distance between cluster centers, N_c is the number of clusters behind one lens (i.e., on one chip) along one dimension, D_e is the distance between emitters (I/O sites) and N_e is the number of emitters in one dimension of a cluster. This leads to an *upper* bound on the cluster spacing as a function of emitter spacing:

$$D_c \leq \frac{\left(\frac{f}{2\sqrt{2}f_{\#}}-\frac{D_e(N_e-1)}{2}\right)}{(N_c-1)} \qquad (2)$$

A *lower* bound on the cluster spacing as a function of emitter spacing is found by considering the cluster spacing required to insure that the receiving lens array has no physical overlap of lenses. This places a physical lower bound on the cluster spacing as a function of the distance to the mirror, D, or equivalently the distance to the receiving array in an unfolded architecture. This relation depicted in Figure 1-b, is:

$$D_c \geq \frac{fL_D}{2D} \tag{3}$$

where L_D is the diameter of the lens barrel and D is the distance from the lens plane to the mirror in the retro-reflective architecture. This is a lower bound since the cluster spacing, D_c, can always be increased from this point. This simply separates the lenses, allowing some space between them. This equation relates the cluster spacing to the minimum system length. As the cluster spacing increases the minimum system length decreases. This is intuitively correct, as the increased cluster spacing creates larger angles in the system, thereby shortening it. This can only be exploited until the upper bound is reached. At this point the numerical aperture of the lenses is fully utilized.

To relate Equation 3 to emitter spacing requires a calculation of the maximum emitter spacing as a function of the distance to the mirror, D. This relation is depicted in Figure 1-c. The cluster size, $D_e(N_e-1)$ must be small enough to be captured by the active aperture of the receiving lens, $f/f_{\#}$. Equation 4 is the relation of distance to the mirror, D, to the cluster spacing, D_e:

$$\frac{D_e(N_e-1)}{f} \leq \frac{f}{2D\sqrt{2}f_{\#}} \tag{4}$$

Equations 3 and 4 combine to form a lower bound on the cluster spacing as a function of emitter spacing:

$$D_c \geq \frac{\sqrt{2}(N_e-1)D_e}{\beta} \tag{5}$$

where β is the ratio of the lens barrel diameter to active lens aperture. This is a line with slope proportional to $1/\beta$. Points above and to the left satisfy this constraint, while smaller cluster spacing and larger emitter spacing do not. Values of β approaching 1 are advantageous as they allow more freedom within the design constraints. This is intuitively correct, as a lens with its active aperture equal to its physical dimensions (β=1) would be ideal. Equation 5 explicitly demonstrates the self similar grid requirements [2] of the optical I/O arrangement and the lens array placement. The limit on the portion of the OE backplane used for optical I/O is a scaled version of the useable portion of the lens array.

The final constraint is the physical limit on how small the emitter spacing can be. Figure 2 shows an example of all the design constraints for an experimental FSOI module with a 4x4 array of chips (and lenses) each with a 4x4 array of clusters. Each cluster in the example system contains 4 nodes, so N_e=2 and N_c=4 in the above equations. This example system contains 1280 links in an interleaved shuffle architecture. The vertical line at 100 μm is a lower limit on emitter spacing. The nearly horizontal upper line, Equation 2, is an upper bound. The sloped line– Equation 5, represents a lower bound. The area inside the triangular region formed by the three constraints contains all possible combinations of emitter spacing and cluster spacing for the specified lens parameters.

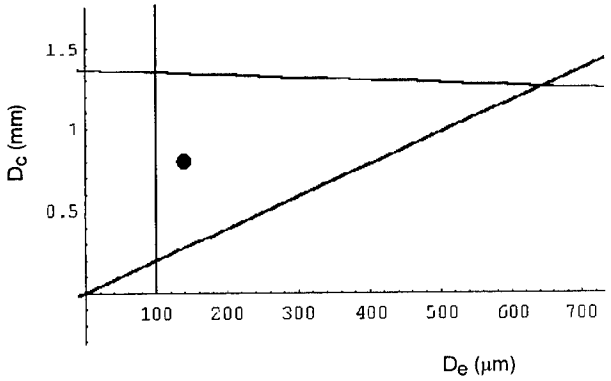


Figure 2. Example of the optical I/O layout design constraints for the SB interconnection module. The area inside the triangle represents all possible combinations of emitter spacing and cluster spacing for the experimental SB interconnection module. The dot shows the emitter spacing and cluster spacing used in the experiments.

The length of the optical interconnection module monotonically decreases with an increase in cluster spacing. So the minimum volume system would be designed to a point in the upper left corner of the design triangle in Figure 2. The design should be near this corner while avoiding both bounds, as the upper bound vignettes about half of the light of the outermost emitter at the transmitting lens and the lower bound vignettes at the receiving lens.

The point in Figure 2, inside the triangle, is representative of an experimental FSOI module designed for the Sliding Banyan architecture. The prototype was built, aligned, and evaluated. It performed the requisite shuffle pattern on all 4 parallel links, without vignetting – all interconnections were verified.

Conclusion - A design methodology for smart pixel optical I/O placement in parallel shuffle FSOI architectures is developed. This approach has proven useful in several prototype FSOI module developments and is continuing to be used for integrated smart pixel design and layout. The self similar nature of the optical interconnection is evident, and its geometric bounds are illustrated.

This research is sponsored by the Ballistic Missile Defense Organization through a grant with the Army Research Office.

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11:15am - 11:30am

ThA8

A Smart-Pixel Free-Space Interconnected Parallel Processing System

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1. Introduction

Future high-performance computing systems will use electronic and optical technologies to perform the tasks for which they are best suited. Mature electronic technologies can efficiently perform the data processing while optics can be used to provide the high-bandwidth, high connectivity and high density communication paths. The marriage of these technologies is demonstrated in smart-pixel systems.

One of the main applications for high-speed optoelectronic machines, and that which is the focus of research in our laboratory, is real-time image processing for machine vision. The architecture which we propose is based on the pipelined configuration shown in Fig. 1 [1]. In contrast to conventional parallel processing systems there are three main differences: the input and output (images) are supplied in parallel; the connections between non-local processors are by optical paths; and the interconnection topology is reconfigurable. The benefits of the first two points are well-recognised. The latter point allows the machine to use an interconnection topology that is best suited to the data-flow structure of the algorithm being performed, and is not fixed as in conventional parallel processors. This ability has the potential to provide improvements in the performance of many algorithms.

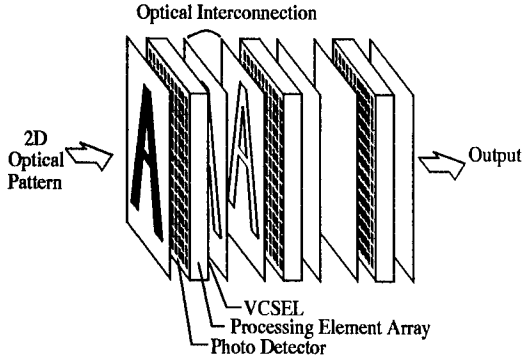


Fig. 1. Pipelined parallel processing architecture.

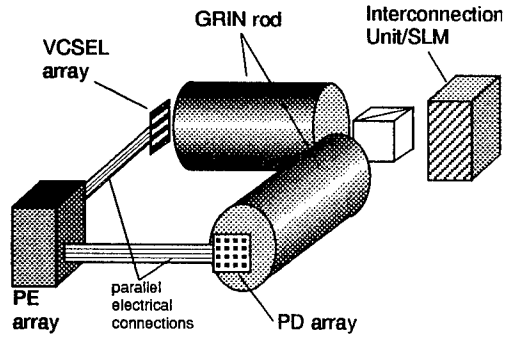


Fig. 2. Compact feedback-type implementation.

In our present demonstrator we utilise a single smart-pixel PE array to implement a feedback-type architecture as shown in Fig. 2.

2. System Description

2.1 Processing Elements (PE's)

A functional diagram of the PE design is shown in Fig. 3. Each PE has an ALU, a 24-bit local memory and can execute arbitary arithmetic and logical operations programmably, for example: addition, subtraction, and multiplication which are operated in bit serial fashion. Each PE is electrically connected to its four neighbouring PEs.

Our system can execute various applications, for example early visual processing including edge detection and smoothing. Some examples of the applications and their performance are shown below.

Application	Time
Edge detection (1bit, 4-neighbour)	0.72 μs
Edge detection (8bit, 4-neighbour)	5.6 μs
Smoothing (1bit, 4-neighbour)	1.0 μs x n (typical n=10)
Smoothing (8bit, 4-neighbour)	7.7 μs x n
Thinning (1bit, 4-neighbour)	1.9 μs
Convolution (4bit)	30 μs

A prototype version of the design is implemented in an FPGA chip [2]. This chip has 4x4 PEs and an instruction decoder. Each PE consists of 700 transistors and executes each operation in 154ns. Full-custom design with dymamic memory will allow higher density and speed, with an integrated photodetector at each pixel. The pixel pitch will be 125 μm to match the VCSEL array.

In the present demonstrator system however, the PEs, optical output and detectors are implemented by discrete units. For optical output we use an 8×8 array of vertical cavity surface emitting laser diodes (VCSEL) developed by NEC Corp. Each diode has an output power of 1 mW and a wavelength of 980 nm.

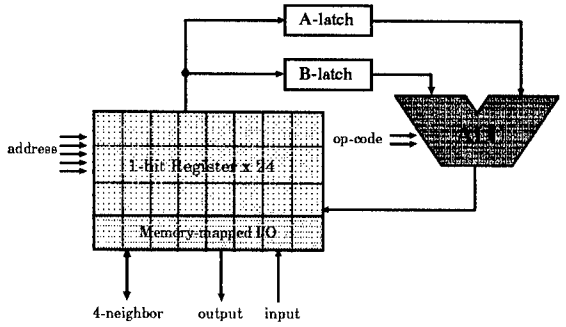


Fig. 3. A single PE.

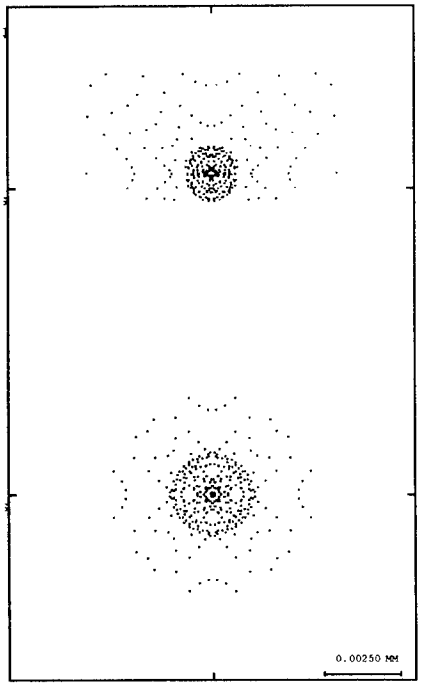


Fig. 4. Spot diagrams for on-axis (bottom) and corner (top) LD images.

The pitch is 125 μm and the LD facets are 6x6 μm^2 for the unpolarised VCSEL array, and approximately 6x9 μm^2 for the polarised VCSELs. The VCSEL array is directly driven by the output from the PE array which is implemented by custom logic chips. Since there is no integrated detector at each PE in this prototype system, we use an array of silicon photodetectors (PD) manufactured by Hamamatsu Photonics. The array contains 16x16 PDs separated by 1.1 mm but we use only 8x8 of them since that is the limit of the parallelism of our system imposed by currently available VCSEL arrays. The output from the PDs is connected to the input of the corresponding PE.

These discrete units are shown in Fig. 2 with parallel electrical connections. In near-future systems those three units will be replaced by the single-chip PE array and VCSEL array. The imaging system and interconnection described below have been designed with the single-chip PE array in mind.

2.2 Interconnection Unit

For the reconfigurable interconnection unit we use a phase-modulating spatial light modulator (SLM). The necessary phase patterns to perform the desired interconnection topology are pre-calculated (typically by simulated annealing techniques) and can be displayed on the SLM. We are currently investigating two options: (i) an optically addressed parallel aligned spatial light modulator (PAL-SLM); and (ii) electrically addressed parallel aligned liquid crystal (LC) displays.

The PAL-SLM is manufactured by Hamamatsu Photonics. It receives as input on one side an intensity pattern provided by a small liquid crystal television panel. A corresponding spatially varying phase retardation is imposed on the read beam [3]. The imaging can be performed by multi-element lenses, however more compact alternatives are a microlens array (MLA), fibre-optic plate (FOP), or a SELFOC lens array (SLA) all of which we describe. The PAL-SLM has a refresh rate of 75 Hz and a resolution of approximately 50 lp/mm, although the useful resolution is also dependent on the imaging optics.

2.3 Imaging Optics

Gradient index (GRIN) rod lenses are attractive for imaging between planes of PEs because they are low-cost and compact [4]. They are available commercially in diameters up to approximately 8 mm.

The theoretical performance of GRIN lenses is difficult to evaluate accurately with ray-tracing software unless precise data is available to model the refractive index profile. However a typical GRIN lens has sufficient performance for the imaging requirements in our system. For example we have modelled in CodeV the performance of the imaging system of Fig. 2 implemented by 0.21 pitch BG50 (Gradient Lens Corp.) lenses. They have a diameter of 5 mm and a length of 32.67 mm. The off-axis position of the corner LD in our VCSEL array is approximately 620 μm or a full field of 1.24 mm. Figure 4 shows spot diagrams for the on axis and corner field positions. The rms spot diameters are 2.98 μm and 4.75 μm respectively. Strehl ratios of 0.9869 and 0.9038 show near diffraction limited performance. A calculation of the percentage of encircled energy falling inside a circular was performed. It was found that 90% of the energy falls within a circular window of approximately 20 μm in diameter. The on axis NA of the BG50 is 0.19. Since the divergence (half-angle) of each LD is 5.5°, the NA is sufficient to collect almost all of the light from the VCSEL array. Calculations show that the energy in the image plane of the corner LD object is approximately 96% of that of the on-axis LD.

3. Discussion

We report on the progress of the construction of a smart-pixel parallel optoelectronic processing system with reconfigurable interconnections. We describe the performance of the components and limitations of the current system. System scalability issues and directions for future research will be presented.

4. References

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Optical interconnect module extensible to 10,000 parallel channels for a smart-pixel optical backplane

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1. Introduction

Free-space optical backplanes using smart pixel arrays are of interest for use in both multiprocessor and ATM switching fabrics, since they potentially offer more intelligence and greater connectivity per unit volume than do electronic backplanes[1]. A particular implementation of an optical backplane which we are constructing[2] uses hybrid-SEED[3] chips, in which differential reflection-mode optical modulators and detectors are integrated with silicon VLSI and connected using free-space optics. This requires a simple, compact repeated optical module which can deliver optical power to the modulators and then transfer the modulated beams to the detectors on the next board. We will describe the detailed design of a module suitable for optically interconnecting the smart pixel arrays on successive boards and show that it is extensible to 10,000 smart pixel channels per board. The hybrid-SEED chips and diffractive optics are presently being fabricated through ARPA CO-OP by AT&T and Honeywell, respectively.

2. Required characteristics of interconnect module

The backplane must be highly competitive with present all-electronic implementations which currently can support bisections bandwidths (number of bits / second crossing a given plane) across a backplane on the order of 10-100 Gb/s. Future optical backplanes must therefore be capable of supporting bisection bandwidths greater than 1Tb/s. There are a number of limitations which drive us to a certain physical division of this total bandwidth. The volumetric overhead of both the electrical packaging and of the optomechanics suggest that the best way to implement the 1Tb/s is to use the smallest possible number of the largest available chips. Given typical commercial CMOS speeds of around 200MHz, about 5,000 parallel channels in each direction would be needed for 1Tb/s bisection bandwidth. The largest mass-produced CMOS chips presently available are around $1cm^2$ in size. For our application, these chips need to be individually packaged. Sufficient electrical pin-outs for such a chip should be available using a package roughly 1″ on a side. A PCB in a switching system frame can reasonably have an edge of only around 10″. Therefore the optical channels could most conveniently be divided between 5 identical chips in each direction per PCB, with each chip containing 1000 smart pixels. Since each smart pixel has a differential optical input and a differential optical output, this requires a connection density of 4000 per chip (and hence 4000 SEEDs per chip). The following characteristics for the

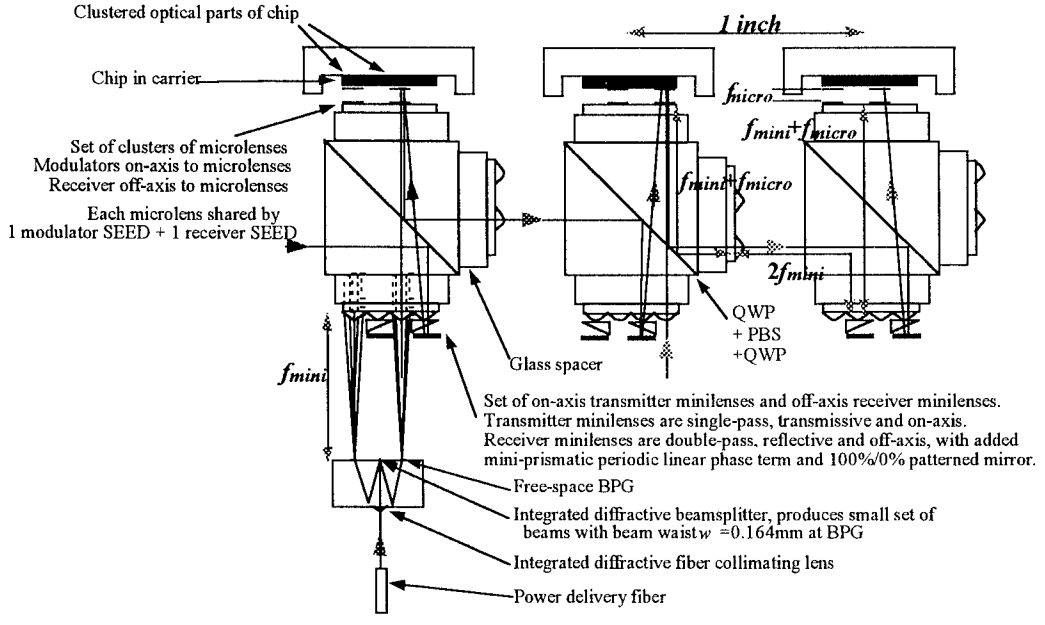


Figure 1 Optical module schematic. Electrical PCBs would be perpendicular to drawing and to chips. All lenses, miniprisms and patterned mirrors are integrated planar structures.

optical module are therefore imposed:

1. Support at least 1000 smart pixels /cm^2
2. Allow the board spacing to match electrical standards (~1″), with 1″ x 1″ x 2″ optomechanics volume per chip
3. Be extensible to a 1cm × 1cm chip size.
4. Keep the loss between the optical power supply and the detector to less than 10dB
5. Use only elements which are potentially cost-effective in mass-production.
6. Minimize the number of critical alignments

3. Description of optical module

A number of systems have been built or proposed [4,5,6,7] which address some of the targets above but most of them do not solve the issue of extensibility to 1cm chip size. In particular, SEED-based systems which use only microlenses suffer from limited throw, resulting in large microlenses and hence low channel density. Our module meets the performance criteria listed above by mixing microlenses and minilenses.

The module is sketched in Figure 1. It consists of arrays of diffractive minilenses forming a single 4f system around successive polarizing beamsplitter cubes. The minilenses between the optical power supply and the modulators are transmissive and on-axis, while those for the detectors are reflective and off-axis and emulate microprisms for beamsteering. The minilenses are augmented by microlens arrays for final focusing onto the clustered 20μm × 20μm SEED windows. Each microlens is shared by an on-axis modulator beam (passing twice through the microlens), and an off-axis detector beam. The system is entirely telecentric, apart from the last stage onto the receiver. The microlenses are used by each Gaussian beam at *f*/6.4, and the minilenses are used by each beam at *f*/21.4. The transmitter minilens as a whole is *f*/3.9. The receiver minilens is *f*/4.4 on each pass. A cheap, compact array generation scheme for the optical power supply beams is also sketched in Figure 1.

This backplane requires only simple one-to-one interconnections, thus avoiding the higher losses associated with more complex interconnects. We also choose to avoid focal-plane pixellated mirrors. Beam combination is by polarization multiplexing and a form of angular multiplexing, ensuring high power efficiency. An efficiency of -19.8dB from power supply laser to receiver, not including array generation fan-out or SEED loss, is calculated using readily available 70% efficient diffractive optics. This could be improved to -10dB using 90% efficient diffractive optics.

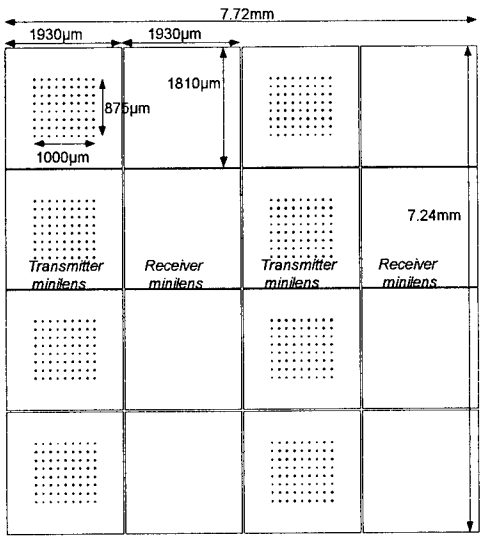


Figure 2 Clusters of modulators tiled to make large chip of 288 smart pixels (515 smart pixels/cm^2), using hybrid-SEED chip of [2] as the repeat unit. A cluster is supported by a transmitter/receiver minilens pair. Interlaced detectors are not shown.

4. Conclusion

A set of optics suitable for interconnecting and powering reflective hybrid-SEEDs in a free-space optical backplane has been presented. Detailed design has been conducted to demonstrate that the optics meet the constraints both of required performance, and of available fabrication. The design process has shown that with given hybrid-SEED design rules a smart pixel density of 515/cm^2 can be supported on a 1cm^2 chip (Figure 2). By positioning the SEEDs on a slightly different grid spacing, this can be made to rise to 1125 smart pixels /cm^2, that is 4500 windows /cm^2. For a bit-rate of 200Mb/s, using ten such 1cm^2 smart pixel chips per PCB results in a backplane with a bi-directional bisection bandwidth of 1.1Tb/s.

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11:45am - 12 noon
ThA10

A compact, low-cost, high-performance test fixture for electrical test and control of smart pixel integrated circuits.

Fouad Kiamilev, Richard Rozier and James Rieve
Dept. of Electrical Engineering, UNCC, Charlotte, NC 28223

As the complexity and speed of smart pixel integrated circuits (ICs) increases, the problem of supplying these ICs with high-speed electrical signals for electrical test and real-time control purposes becomes more difficult. The most common approaches are *ad hoc*, in which a special-purpose electrical environment is constructed around the IC to be tested. This self-contained system can be operated interactively while the user observes the state of the IC using a logic analyzer or an oscilloscope. Constructing this environment may be expensive, difficult and time-consuming. Shortcuts are taken that result in hard-wired, hard-to-modify test systems. Another approach is to use commercial IC test equipment. Although this equipment provides excellent high-speed electrical test capabilities, it is prohibitively expensive and physically large in size.

We have developed a low-cost, compact test fixture that can supply and monitor high-speed electrical signals for smart pixel ICs packaged in an 84-pin PGA chip carrier. Each of the 84 pins on the smart pixel IC can be strapped to power, ground, or configured as an I/O pin. A Xilinx FPGA chip, packaged in a 156-pin PGA chip carrier, is used to provide the test program for the smart pixel IC, with each IC pin having a dedicated connection to an FPGA signal pin. The test program resides in an EPROM chip and the system clock is derived from a 100MHZ (or slower) clock generator chip thus facilitating stand-alone operation. The fixture also includes a 7-segment display chip and several LED's that are controlled by the FPGA and can be programmed to display the operating status of the fixture. Figure 1 shows the schematic for the test fixture.

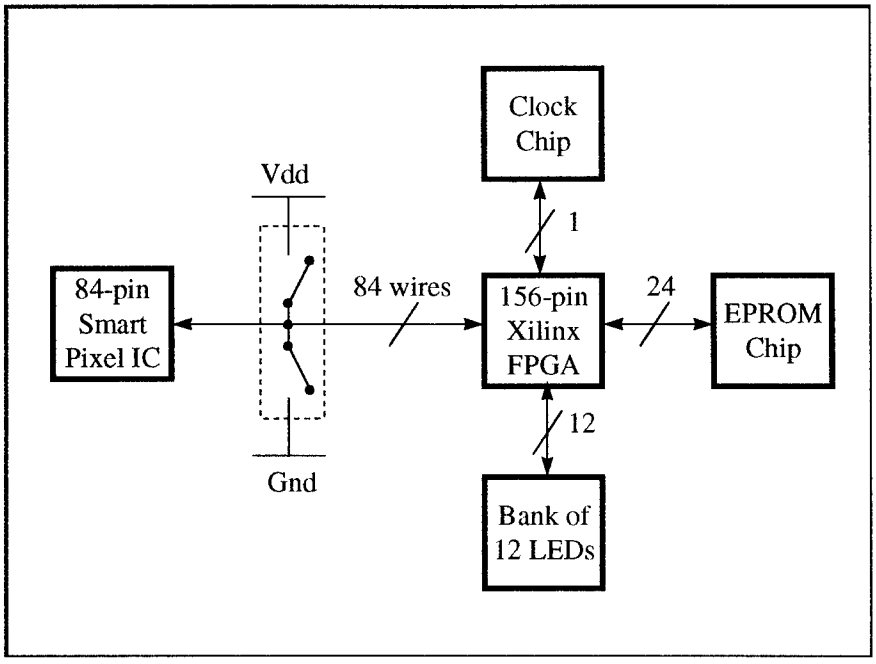


Figure 1: schematic diagram for the test fixture.

Our fixture uses a 6" x 9" 4-layer printed circuit (PC) board. The two inner wiring layers are configured as solid power and ground planes, while the two outer layers carry I/O signals. High-quality decoupling capacitors are used to ensure steady power supply voltage even in the presence of high-speed switching transients. Board component placement is optimized for high-speed operation. Zero-insertion-force (ZIF) sockets are used to achieve repeated and reliable insertion of EPROM and smart pixel chips on the PC board. The smart pixel IC socket is surrounded by a bank of 84 3-position switches allowing universal configuration for different smart pixel IC designs. Configurations are chosen by toggling the switches into one of three possible positions. Selections are VDD, Ground and digital connection to the FPGA.

For the FPGA device, we have selected the Xilinx XC4005-5PG156 [1]. This 5volt device can be reprogrammed an unlimited number of times. Using CMOS SRAM technology, it achieves ultra-low stand-by power consumption and a dynamic power consumption that is proportional to the operating speed. Its output drivers have a voltage swing of 0volts to 3.5volts, allowing it to work with either 5volt or 3.3volt smart pixel ICs. Furthermore, the output drivers are programmable for either high-speed or low-power operation. In high-speed mode, an output driver has a worst-case propagation delay of 7 nanoseconds driving a 50pF external load. The programming capacity for the 4005 FPGA is 5,000 logic gates, 616 flip-flops, and/or up to 6,272 bits of RAM. In practice, this capacity is adequate for implementing highly complex test programs. On the other hand, higher-cost FPGA devices, such as the XC4025, can be used to achieve 5X higher capacity.

Typical operation of the test fixture requires several steps. First, the test program is written on a workstation or a PC using a hardware description language such as VHDL, Verilog or ABEL-HDL [2]. Optionally, it can also be simulated to verify correct functionality. Next, the test program is synthesized to an FPGA using a synthesis tool and an EPROM bit-file is generated. An EPROM programmer is then used to write the bit-file into an EPROM chip. The EPROM chip is inserted into the ZIF socket on the PC board. Finally, when the PC board is powered on, the test program is loaded into the FPGA chip and automatically executed supplying test vectors to the smart pixel IC being tested. The operating speed can be programmed by selecting a different clock generator chip.

The component cost of our test fixture is approximately $800 (US) and it provides electrical testing and control for 84 I/O pins of a smart pixel IC at 100 MHz (or lower) speeds. We have used this fixture to perform electrical testing of several digital and mixed-signal smart pixel integrated circuits. The small size and stand-alone operating capability facilitate insertion of this test fixture in photonic demonstrator systems. Althougn our fixture is designed for smart pixel ICs packaged in the 84-pin PGA chip carrier, the design can be easily modified for other packaging schemes. Low-cost software for developing FPGA test programs is widely available from a number of EDA vendors [2]. A second generation PC board design is currently underway that will achieve 30% size reduction. We are also developing complete documentation for our design that will be made available via anonymous FTP upon completion.

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1:30pm - 2:00pm (Invited)
ThB1

VLSI-Compatible Smart-Pixel Interface Circuits and Technology

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The development of smart-pixel systems has progressed from diode-based device developments such as logic SEEDs[1] to highly-complex single-chip integrated systems containing more than 140,000 FETs.[2] Perhaps more significantly, optical input and output devices have been integrated with silicon CMOS chips.[3] These highly-complex smart-pixel chips, which could be called optoelectronic-very-large-scale integration (OE-VLSI), should scale in performance as CMOS technology advances. The advantages of OE-VLSI to system designers lie largely with the ability to provide large amounts of input and output (I/O) directly to the chip. Key elements are the receiver and transmitter circuits providing optical-to-electrical interfaces to the OE-VLSI chip. In this talk, we discuss such circuits, with a particular focus on their unique and challenging aspects.

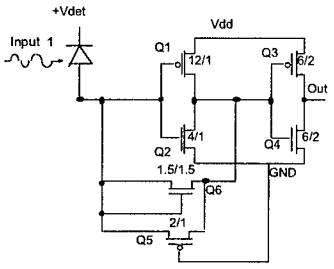


Figure 1: Schematic of a single-beam transimpedance receiver for OE-VLSI systems.

The OE-VLSI receiver is very different from a classic telecommunications-grade receiver. In the OE-VLSI case, the receiver must be particularly compact, and dissipate a minimum amount of power, since large numbers of the circuits are presumed to exist on the chip. Noise immunity and dynamic range are also important parameters. Finally, the OE-VLSI receiver must generate a logic-voltage that is presumed to be utilized on the same chip. By contrast, a telecommunications-style receiver is relatively unconstrained by power dissipation and chip area, does not necessarily generate logic-level voltages, and typically must drive a signal into 50 Ω.

In the first example of a OE-VLSI receiver, shown in Fig.1, we see a single-beam transimpedance circuit. This receiver has the advantage of being particularly small (~ 350 μm^2 in 0.8 μm CMOS), and low dissipation (~ 3.5 mW). It has a roughly constant sensitivity of -19 dBm from dc to 375 Mb/s, which arises from a built-in offset between the switching thresholds of the two stages.[4] This offset permits the receiver to operate robustly with relatively low-contrast data. In dc-coupled single-beam receivers, this offset is unavoidable, and is an important part of the design. In the second example, shown in Fig.2, we see an adaptation of the transimpedance receiver to a two-beam case. Two optical beams permit improved noise immunity, since a relative reference is provided for each signal. A version of this receiver operates to 1 Gb/s, consumed about 8 mW, and occupied 1100 μm^2 in 0.8 μm CMOS. [5]

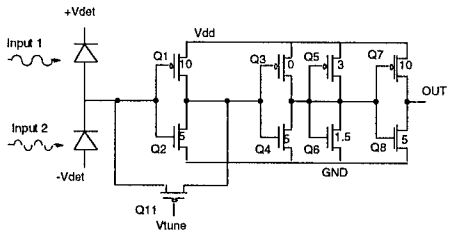


Figure 2: Schematic of a two-beam transimpedance receiver for OE-VLSI systems.

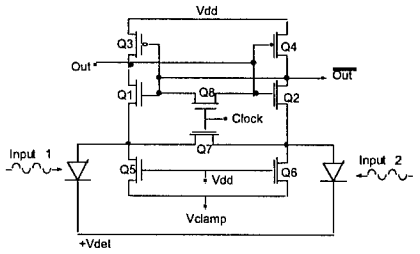


Figure 3: Schematic of two synchronous sense-amplifier-based OE-VLSI receivers.

In the final receiver example, Fig.3, we present a synchronous receiver. It has more similarity to a

comparator circuit than a linear amplifier. Indeed, this circuit was taken from a design intended for use in SRAM and DRAM bit-line amplifiers.[6] The circuit makes use of synchronization information, and so requires that reproducible timing information be available. This constraint may be acceptable, given the local nature of many smart-pixel systems. The advantage of the circuit is that it can be made with very low dissipation. The circuit will operate with one or two (illustrated) input beams. The circuit has been demonstrated at $\sim$ 1 mW dissipation and data rates of 320 Mb/s in single-beam operation, and occupied about 1000 μm^2 in 0.8 μm CMOS.

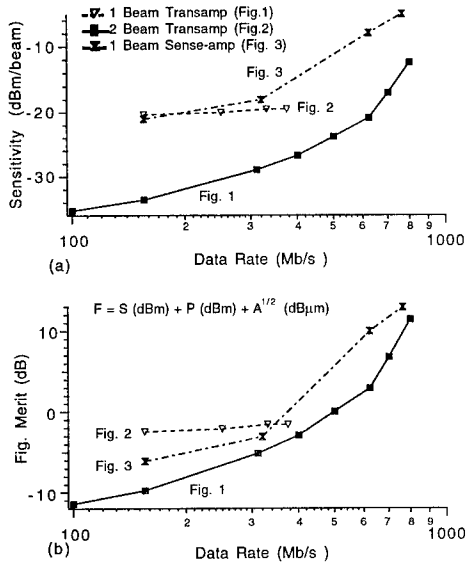


Figure 4: Sensitivity (a) and Figure of merit (b) for several different OE-VLSI receivers.

Unlike telecommunications receivers, wherein sensitivity is the primary measure of performance, any measure of OE-VLSI receiver performance must include area and power dissipation as well. To enable comparison between receivers, and to permit these factors to be presented together graphically, we propose a new composite measure of performance, or figure of merit. This measure (F) is defined by $F = S + P + A^{1/2}$, where S is the sensitivity in dBm, P is the power consumption in dBm, and $A^{1/2}$ is the square root of the area (providing a measure of linear chip dimension) defined in dBμm as $A^{1/2} = 5log(A/1\mu m)$. This is presented in Fig. 4 for the three examples described previously. F effectively imposes a sensitivity penalty that depends on area and power, and neglects dynamic range and noise immunity (which could be included analagously).

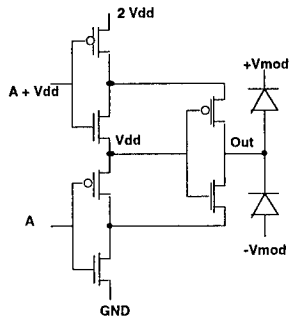


Figure 5: Schematic of voltage-doubling transmitter circuit for modulator-based smart pixel systems. Output swing is 0 to 2 Vdd.

Of course, the transmitter is at least as important as the receiver. However, less attention is paid to it since, for modulator-based systems, a simple inverter will do. As the operating voltage of CMOS circuits drops, the transmitter circuit promises to become more challenging. One particular problem for normal-incidence modulator-based smart pixels is the need for relatively high electric field. At present, this translates into operating voltages $\sim$ 5 V or so for a contrast ratio of about 3. As supply voltages decrease, these operating voltages will become more difficult to obtain. There are several options for addressing this problem. Here we consider circuit solutions. One example of a circuit that will provide a voltage swing of twice V_{dd} at the output, while maintaining no more than V_{dd} across any single FET is shown in Fig.5. The circuit does not require complementary logic, but does require an up-shifted logic voltage. Simulations indicate this circuit can operate to 622 Mb/s in 0.8 μm CMOS.[7].

I am pleased to acknowledge the work and contributions of A. V. Krishnamoorthy, A. L. Lentine, K. W. Goossen, J. A. Walker, B. Tseng, S. Hui, L. M. F. Chirovsky, R. E. Leibenguth, J. E. Cunningham, W. Y. Jan, L. M. F. Chirovsky, L. A. D'Asaro, D. Bacon, D. Dahringer, D. Kossives, and D. A. B. Miller.

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[2] A. L. Lentine, et. al. IEEE LEOS 1995 Annual Meeting, Postdeadline Paper PD2.5, 1995.

[3] K. W. Goossen, *IEEE Phot. Tech. Lett.*, **7**, p. 360, 1995.

[4] A. V. Krishnamoorthy, et. al. *IEEE Phot. Tech. Lett.*, **7**, p. 1288, 1995.

[5] T. K. Woodward, et. al. *IEEE Phot. Tech. Lett.*, **8**(3), pp. 422, 1996.

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2:00pm - 2:30pm (Invited)
ThB2

FLC/VLSI as a Smart Pixel Technology

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Abstract

Although FLC/VLSI technology is used with success in the construction of spatial light modulators it seems that few "smart pixel" systems are being progressed beyond the stage of small scale demonstrations. It is now reasonable to ask whether this materials system is well suited to the type of systems which are now described as containing smart pixels.

FLC/VLSI as a Smart Pixel Technology

Liquid crystal materials have some well–known advantages over other electro–optic materials. These include the large modulation of phase or amplitude available at relatively low voltages, a broad range of operating wavelengths, the availibility of a wide range of effects which range from bistability to analog response to controllable scattering, a high enough birefringence to allow for the construction of thin cells and therefore small pixels, and a relatively straightforward integration process allowing liquid crystals to be incorporated into a variety of device structures ranging from large flat–panel displays through liquid crystal on silicon devices [1] to WDM switches for fibers [2].

The combination of a liquid crystal layer, to modulate light, on top of a silicon backplane to control the liquid crystal is seen as, in some ways, the ideal smart pixel technology. Silicon is an appealing material because one can integrate the detection and processing of information into a single substrate which has the added benefit of being inexpensively fabricated in a commercial process (this is now also true of GaAs [3]). The perceived limiting factor is the relatively slow switching speed of the liquid crystal.

I shall discuss some of the systems which have been implemented using FLC/VLSI smart pixels and explore the advantages and disadvantages of liquid crystal on silicon technology and speculate as to its place in future smart pixel systems.

References

[1] For a recent review see K. M. Johnson et al. Smart spatial light modulators using liquid crystals on silicon. *Journal of Quantum Electronics*, 29(2):699, 1993.

[2] Anat Sneh et al. High speed wavelength tunable liquid crystal filter. *IEEE Photonics Technology Letters*, 7(4):379–381, 1995.

[3] MOSIS project, USC/Information Sciences Institute, CA 90292-6695. MOSIS recently announced that they expect to offer optoelectronic enhancements to one of their Vitesse GaAs processes. They predict that their MSM photodiodes will respond from 865nm to 600nm and have a responsivity of between 0.3 and 0.5 Amps/Watt.

2:30pm - 2:45pm
ThB3

Optimization of Smart Pixel Receivers

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Introduction

The design of the optical receiver is an integral part of any optical interconnection scheme. The performance and information handling capacity of the free-space optical link depend to a large extent on the receiver's gain, speed, power consumption, and area requirements. In general, these four parameters can be traded off against each other. We have developed a framework for modeling receivers based on digital CMOS technology, and optimizing the design to minimize either the optical power requirement or the total power requirement.

Receiver Model

The receiver designs presented here consist of simple CMOS current-source inverters, as shown in Figure 1. The analysis examines one and three-stage transimpedance amplifiers connected to cascaded voltage amplifying stages. The maximum number of stages in the voltage amplifier was limited to two, to insure that all stages would be correctly biased despite amplifier offsets. Other, more complex designs for the receiver can be envisioned, but in general they will all follow the same structure shown in Figure 2.

The model incorporates the receiver's bit-rate, as determined by the rise time of the receiver; the transimpedance, as determined from stability requirements; the transimpedance-bit rate, which is used as a figure of merit; the power dissipation; and the size. In this paper, the receiver configuration is coded as N+P, where N is the number of stages in the transimpedance amplifier, and P is the number of stages in the voltage post-amplifier.

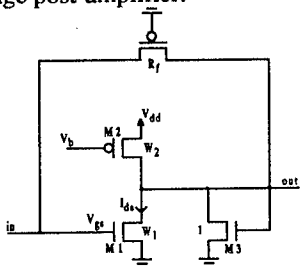


Figure 1 - CMOS amplifier with feedback

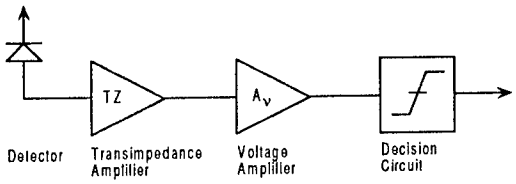


Figure 2 - Receiver block diagram

Optimization and Comparison

For a given technology (i.e. 0.8 μm CMOS), it is possible to choose values for W_1, V_{gs}, N and P that simultaneously satisfy a given bit-rate while minimizing the required power. Depending on the application, it may be desirable to minimize either the required optical power, P_o, or the total power. The total power is expressed as

$$P_{total} = P_d + \eta P_o \qquad (1)$$

P_d is the electrical power dissipation of the receiver and the constant factor η represents the electrical to optical power conversion efficiency of the optical transmitter and the optical system efficiency. Multiplying η by the optical power gives an equivalent electrical power dissipated at the transmitter. Typically, η is a function of electrical power to the transmitter. For simplicity, a constant η=10 is used in the example that follows. The configuration which minimizes the power at a given bit-rate is referred to as the optimum receiver design.

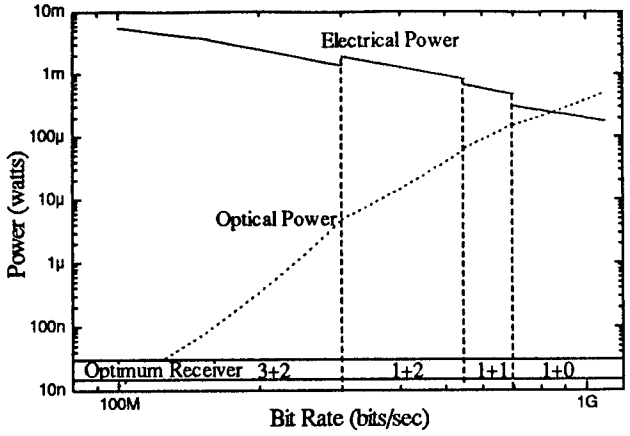


Figure 3- Electrical and optical power requirements for receivers optimized for lowest optical power.

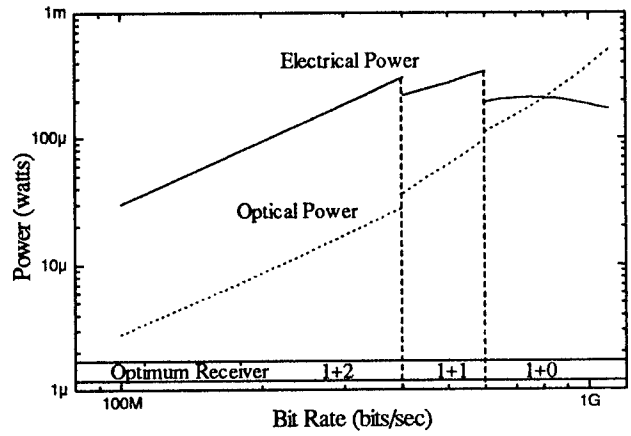


Figure 4- Electrical and optical power requirements for receivers optimized for lowest total power, with η=10.

There are four distinct bit-rate regions, as shown in Figure 3, in which different receiver configurations result in a minimum required optical power. Below 300 Mbit/s, a three stage transimpedance amplifier with a two stage voltage post-amplifier, i.e. (3+2), provides maximum gain, thereby requiring the lowest optical power. Because a receiver configuration with higher gain is used at lower bit rates, the required electrical power is high. Between 300 Mbit/s and 550 Mbit/s, (1+2) is optimum; between 550 Mbit/s and 700 Mbit/s, the optimum is (1+1). Above 700 Mbit/s only a single stage receiver (1+0) can meet the bit-rate requirement. Beyond 1 Gbit/s, a transimpedance receiver provides no additional gain compared to a simple resistor terminated photodetector.

Figure 4 plots the optical and electrical power requirements for receivers optimized for total power, using η=10. There are three bit-rate regions in this graph. In the two regions below 600 Mbit/s, the electrical power of the receiver and the electrical power required at the transmitter are optimized to be approximately equal. Above 600 Mbit/s, the electrical power at the optical transmitter dominates the total power, because the gain of the receiver is low. Notice that the (3+2) configuration is no longer optimal. Although this configuration minimizes the optical power requirement, its total power requirement is high. This is because the three-stage transimpedance amplifier dissipates more power than a one-stage transimpedance amplifier to provide the same bandwidth.

The results outlined in this summary are based on 0.8 μm CMOS technology. Smaller gate length technologies will increase the bandwidth of the receiver. However, due to short-channel effects, the gain will not increase proportionally to the decrease in gate-length.

References

1. C. Fan, B. Mansoorian, D. A. Van Blerkom, M. W. Hansen, V. H. Ozguz, S. C. Esener, and G. C. Marsden, "Digital free-space optical interconnections: a comparison of transmitter technologies," *Applied Optics*, vol. 34, no. 17, pp. 3103-3115, 1995.
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6. E. M. Cherry and D. E. Hooper, *Amplifying Devices and Low-Pass Amplifier Design*, New York: John Wiley, 1968.
7. R. G. Smith and S. D. Personick, "Receiver design for optical fiber communication systems," in *Semiconductor Devices for Optical Communication*, H. Kressel, Ed., New York: Springer Verlag, 1980.

2:45pm - 3:00pm
ThB4

Current-Mode Smart Pixel Receivers

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Summary

A smart pixel receiver must be high-speed (bit rate, B in the hundreds of Mb/s), moderately sensitive (-30 dBm to -20 dBm) and low-power (< 7 dBm). These requirements are difficult to meet simultaneously. The electrical power consumed by the smart pixel may be dominated by the receiver [1]. Our wish to minimize the receiver electrical power consumption whilst maintaining its required sensitivity and bit rate is complicated by the fact that sensitivity and electrical power consumption represent a trade-off. Typically, sensitivity is obtained by the addition of gain stages that consume area and electrical power. Furthermore the electrical power increases, and the sensitivity decreases with increasing bit rate and input capacitance, C which is dependent on detector size. The bandwidth decreases with increased input capacitance. Using small detectors is not a solution since they make the alignment impractical [2].

To solve this problem, we propose a new family of receivers which use a current-mode [3,4] front-end and a current-to-voltage converter. The concept is illustrated in Figure 1. The sensitivity and the power consumption of a current mode circuit are independent of the bit rate and input capacitance. The bandwidth is also independent of input capacitance.
Typically, the input capacitance is large (>100fF) compared to the minimum gate capacitance (a few fF). The current-mode front-end offers a potential advantage in terms of sensitivity and power if its switching current, ΔI and its static power is small (see table 1) by providing a 'buffer' between the high capacitance of detectors and the low capacitance of digital nodes.

In table 1, we summarize the comparison between power for a voltage and a current mode receiver. ΔV and ΔI are the switching voltage and current which depend on the receiver circuit. S is the responsivity of the photodetector. V_{dd} is the voltage supply. I_s is the static current.

Table 1: Power Comparison

	SWITCHING POWER		STATIC POWER
	V-mode	I-mode	
Optical Power	$\sim\Delta VBC/S$	$\sim\Delta I/S$	—
Electrical Power	$\Delta V^2 BC$	0	$I_s V_{dd}$

The current sense digital receiver [3,5] is one implementation of this concept. A layout of this receiver is shown in Figure 2. It is composed of a current-mode front-end and a sense amplifier. The sense amplifier acts as a sensitive current-to-voltage (I-V) converter. Other combinations of current mode front-ends and I-V converters are possible. In the presentation, we will also consider the current conveyor [4] for smart pixel front-end applications.

A potential limitation with this approach is that static power is dissipated when the analog front-end is biased to its switching point. To reduce the static power, we can use a dynamic approach, clocks to control the current path from V_{dd} to ground. For our current mode sense receiver, during the first part of the period, a clock signal puts the receiver in a state that consumes static power. In the second part of the period, the low-capacitance output is switched and no static power is consumed after switching. The dynamic method can also be applied to a transimpedance

receiver (TIR) by connecting the receiver in the first part of the write period and disconnecting it for the second part. This effectively reduces the static power duty cycle, and the average power.
We show in Figure 3 a power simulation of the current-mode sense receiver. The average total static and dynamic power consumed is only 0.8mW compared to 6.3mW for a TIR of similar sensitivity. We note that the receiver dissipates the same amount of power regardless of the switching activity. This leads to an uniform temperature across the array. Uniformity is important because device performance is temperature sensitive.
The sensitivity of the current mode sense receiver is -20 dBm. We will present further details of the proposed receiver designs and their simulation. It is anticipated that experimental results of the performance of the current-mode sense receiver implemented in 0.7 μm CMOS technology will be available and they will be compared with that of a multi-stage TIR.

Acknowledgments

This work is supported by the BNR-NT/NSERC Chair in Photonic Systems and UK's EPSRC(SCIOS). F. Tooley is also a member of staff of Heriot-Watt University. T. Drabik (G. Tech.) suggested charge sense amplifiers which prompted us to examine current mode circuits. J. Dines had this design fabricated for us.

References:

1) T.K. Woodward, "Optical Receivers for Smart Pixel Applications," OIPS2.1, LEOS'95, pp.67-8.
2) F.A.P. Tooley, A.Z. Shang, and B. Robertson, "Alignment Tolerant Smart Pixels," paper submitted to the Summer Topicals in Smart Pixel, August 1996, Keystone, CO, USA.
3) A.Z. Shang and F.A.P. Tooley, "A High-Sensitivity and Low-Power Smart Pixel Receiver," paper OWB5 to be presented at Optical Computing 1996 (OC'96), Sendai, Japan.
4) Analogue IC Design: The Current-Mode Approach, C. Toumazou, F.J. Lidgey, and D.G. Haigh, Eds. London: Peter Peregrinus, 1990.
5) T.K. Woodward et al, "Synchronous Sense-Amplifier-Based Optical Receivers for Smart-Pixel Applications," paper JWA3 to be presented at Optical Computing 1996 (OC'96), Sendai, Japan.

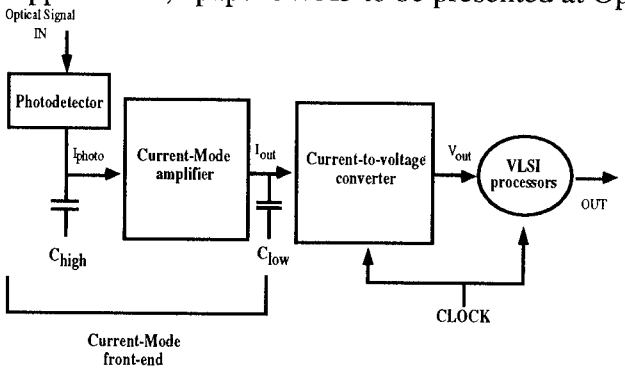


Figure 1: Current-Mode Smart Pixel

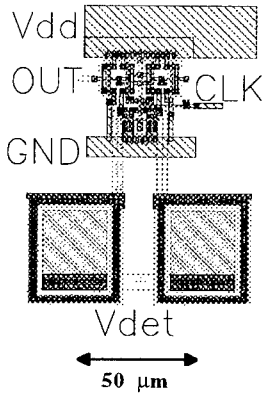


Figure 2: Current-sense receiver layout

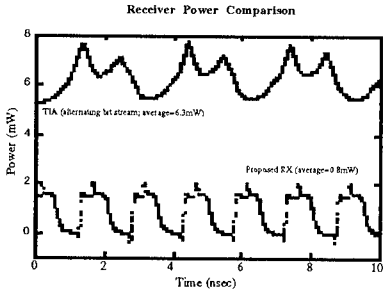


Figure 3: Power Consumption

Optimization of Transmitter and Receiver Design for Optoelectronic Computing

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Optoelectronic computing systems that combine electronic circuits with optical interconnect elements have been considered for many applications where the cost of communication is higher than that of computation. We have previously developed a method of evaluating the performance of the optoelectronic interface, referred to as a photonics layer, and examined various transmitter and receiver technologies separately.[1] In this paper, we report our recent results in the design optimization of the overall photonics layer. We examine the total electrical power dissipated in both the transmitter and the receiver modules, and optimize the receiver configurations to achieve a minimum electrical power dissipation at a given bit rate. The results indicate that, as the bit rate increases, the total power dissipation in the photonics layer increases while the interconnect channel density decreases. The actual physical size of the communication circuits is much smaller than the effective area limited by the power dissipation density. Therefore, in any parallel computing application, there is an optimal ratio between the communication and the computation circuit area that maximizes the usage of available silicon real estate.

Consider the photonics layer shown in Figure 1. The input of each channel in the layer is driven by a computational logic gate, and the output is used to drive a logic gate. The minimum optical power in each channel is determined by the input voltage requirement at the logic gate driven by the receiver. The noise-limited optical power is shown (Figure 2) to be an order of magnitude lower than the optical power required for the voltage swing. In the calculation we have assumed a 1-V voltage swing and a bit-error rate of 10^{-15}.

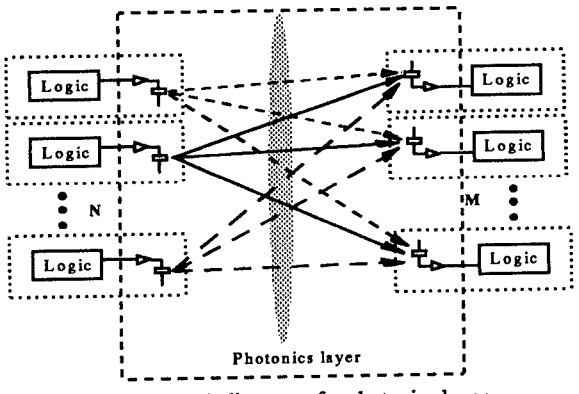


Fig. 1 Block diagram of a photonics layer

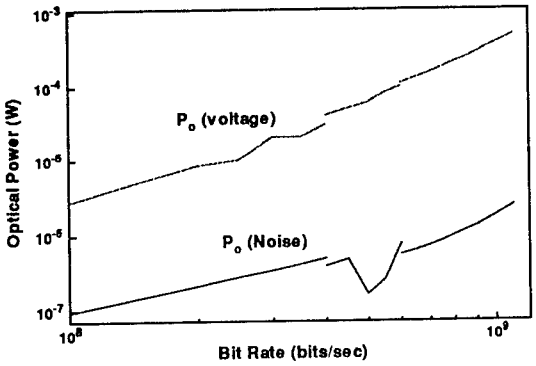


Fig. 2 The optical power required at the receiver input by the voltage swing requirement and the noise

The total electrical power dissipation in a photonics layer can be expressed as

$$P_{total} = P_{\det} + \eta P_{o\det} + P_{penalty}, \qquad (1)$$

where the first term is the electrical power dissipation in the optical receiver, and the last two terms are the electrical power dissipation in the optical transmitter, one of which is related to the optical power required at the receiver input (P_{odet}). The η factor summarizes the efficiency of the transmitter and the optical link.

The electrical power dissipated in a laser is given by

$$P_{laser} = \frac{1-\eta_{LI}/V_{th}}{\eta_{os}\eta_{LI}/V_{th}} P_{o\det} + I_{th}V_{th}, \qquad (2)$$

where η_{LI} is the slope efficiency of laser L-I curve, V_{th} and I_{th} the laser threshold voltage and current, and η_{os} the efficiency of the optical link from laser

to detector. The power penalty is due to the laser threshold power.

The electrical power dissipated in a MQW modulator is

$$P_{\text{mod}} = \frac{rV_{\text{mod}}}{\eta_{os}} P_{o\text{det}} + C_{\text{mod}} V_{\text{mod}}^2 f , \qquad (3)$$

where r is the responsivity of the modulator, V_{mod} the bias voltage of the modulator, C_{mod} the modulator capacitance, and f the operation frequency. In the modulator case the power penalty comes from driving the modulator capacitance. By using the parameters listed in Table I, the η factor in Eq. (2) is $\eta_{laser}=9.7$ for lasers, and $\eta_{mod}=8.3$ for modulators.

Table I Parameters used in the calculation

VCSEL	MQW modulator
η_{LI} = 0.45 mW/mA	V_{mod} = 5 V
I_{th} = 0.5 mA	r = 0.8 A/W
V_{th} = 2.5 V	C_{mod} = 15 fF
η_{os} = 0.47	η_{os} = 0.48

In the receiver design space, there are four dimensions, receiver gain, speed, power, and area, that can be traded off against each other. For a given transmitter technology, we optimize the receiver configuration by minimizing the total electrical power dissipated in the transmitter and the receiver. Figure 3 plots the total electrical power requirements in VCSEL and MQW systems. Also plotted are the electrical powers dissipated in the individual components. One can see that, at low bit rates, the electrical power dissipated at the MQW transmitter and the receiver are approximately equal. At high bit-rates, the electrical power dissipated in the MQW transmitter becomes dominant, because the gain of the receiver drops dramatically and, therefore, more optical power is necessary to satisfy the logic voltage requirement. In the case of VCSELs used as the transmitter, the electrical power dissipated in the VCSEL is dominant at all bit rates because of the laser threshold power penalty. In all cases, the total dissipated electrical power increases as the operation bit rate increases.

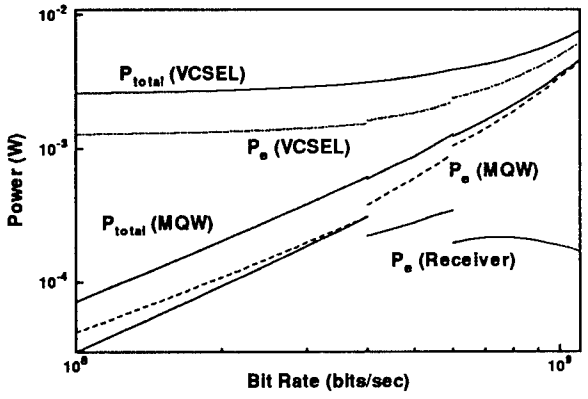


Fig. 3 Electrical and optical power required at the receiver, electrical power at transmitters, and the total electrical

The minimum combined effective area of transmitter and receiver in an individual link is determined by the total power dissipated in the link and the maximum power dissipation density; it is calculated in Figure 4 as a function of the bit rate for a 10 W/cm^2 power dissipation density. Also plotted is the physical size of the optoelectronic components per link. The figure shows the difference between the physical size and the effective area determined by the power dissipation. In the case of MQW modulators, the difference increases as the bit rate increases. Therefore, more computational complexity should be considered per I/O link at high bit rates to maximize the usage of the available silicon real estate in the link. In systems using VCSELs as transmitters, a high computational complexity should be considered for all bit rates.

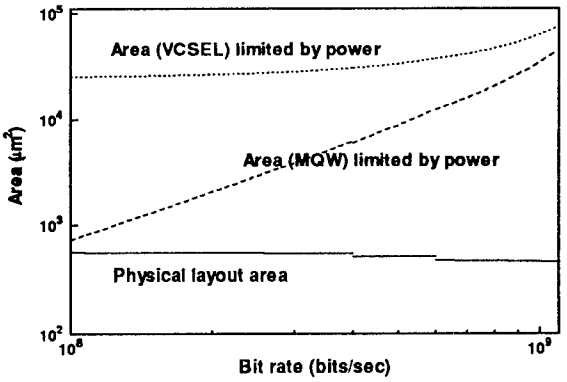


Fig. 4 Areas per link required by the physical layout and by the electrical power dissipation

References

[1] Chi Fan, Barmak Mansoorian, Daniel A. Van Blerkom, Mark W. Hansen, Volkan H. Ozguz, Sadik C. Esener, and Gary C. Marsden, "Digital free-space optical interconnections: a comparison of transmitter technologies", *Appl. Optics*, 34, pp3103-3115, 1995.

3:30pm - 3:45pm
ThB6

A Smart Pixel Bi-Directional Optical Link Using Co-Located Emitters and Detectors

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The use of highly complex digital and analog Si electronics coupled with optoelectronic devices, i.e., smart pixels, offers to systems users many options for advanced optical interconnection. Multiplexing is a popular technique to access the large data capacity of optical fiber. Multiplexed signals, however, have traditionally traveled in the same direction, although it is possible to use a single fiber for bi-directional optical communication using waveguide splitters to separate the emitters and detectors [1]-[4]. In this paper, a single fiber bi-directional link is reported that uses the integration of an emitter onto a larger detector and associated digital/analog silicon circuit to create co-located smart pixels.

The bi-directional smart pixel optical link is comprised of a thin film emitter integrated onto a silicon detector, analog optoelectronic transceiver interfaces, and digital signal processing circuitry. The thin film GaAs-based light emitting diode was separated from the growth substrate and bonded [5] into the center of a silicon CMOS bipolar junction detector, as shown in the photograph in Fig. 1. The silicon detector was a 1 mm x 1 mm array of Si phototransistors fabricated in 1.2 μm CMOS by the MOSIS foundry. The photodetector base current is controlled by the input optical signal.

In this demonstration, large core plastic optical fiber was used which was similar in size to the Si detector. To realize a fully functional smart pixel communications link, CMOS analog optoelectronic receiver and transmitter circuits which had digital input/output were fabricated adjacent to the silicon detector. Digital circuitry for multiplexing, data sampling and encoding, and microprocessor interfacing are also included in this silicon smart pixel integrated circuit.

The interface chip was fabricated using MOSIS 1.2 μm Si CMOS technology, and incorporates both digital and analog circuitry. The analog components included the detector amplifier, the emitter driver, and the analog-to-digital converter. The detector is followed by a large gain amplifier that, using an off-chip bias current, provides a binary signal corresponding to the incident light from the fiber. To drive the transmitter, inputs composed of on-chip digital and off-chip analog signals were used. The off-chip analog signal was converted to a digital signal for optical transmission using an analog-to-digital converter that utilized single-slope integration.

To tune the transmitter and receiver circuits, the emitter driver and detector amplifier contained analog bias signals. The digital circuitry was responsible for sampling, assembling, and encoding the serial data stream. External circuitry included a crystal oscillator and an HC11 microcontroller at one end of the link for decoding the received protocol. All of the circuits operated at 5 V.

After the circuits were integrated, each circuit was initially tested before packaging to verify the function of the integrated emitter, and were then subsequently packaged and tested as a link. The inputs for the experimental setup were a crystal oscillator, an 8 bit dip switch and two variable resistors. These provided the signals that the integrated smart pixel OEICs multiplexed for serial transmission. Using two XYZ stages, a 0.98 mm core plastic optical fiber (POF) was positioned above the LED and the detector, roughly centered on the emitter/detector pair. As the serial data stream was transmitted from one chip, the received signal from the detector on the other chip was decoded using a HC11 microprocessor and was then captured on an oscilloscope. Figure 2 shows the received signal, the input signal and the reference trigger for this experiment. The same procedure was used to test transmission from Chip B to Chip A, with the same result.

A single fiber bi-directional smart pixel link is reported in this paper, which uses the co-location of an emitter and detector at each end of the fiber. To realize a fully functional communications link, CMOS analog optoelectronic receiver and transmitter circuits which had digital input/output were fabricated adjacent to the silicon detector. Digital circuitry for multiplexing, data sampling and encoding, and microprocessor interfacing were also included in this silicon integrated circuit.

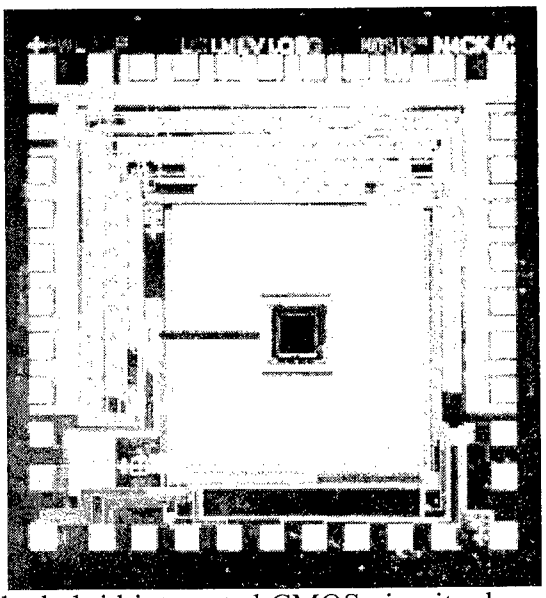
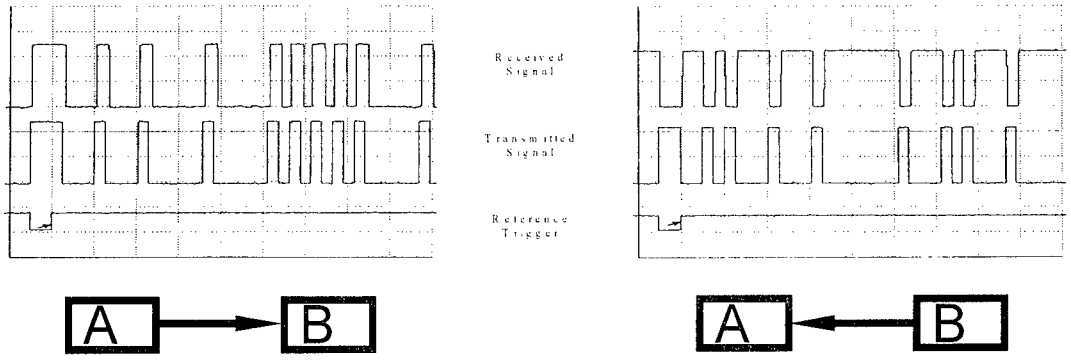


Figure 1 -- Photograph of the hybrid integrated CMOS circuit where the LED is in the center of the phototransistor detector array.



(a) (b)

Figure 2 -- Oscilloscope traces showing the received signal, the transmitted signal, and the reference trigger for transmission from one chip to another.

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3:45pm - 4:00pm
ThB7

Design and Implementation of a Field Programmable Smart Pixel Array

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Abstract

A Field Programmable Smart Pixel (FP-SP) is a smart pixel capable of having its electronic processing circuitry dynamically programmed in the field[1]. We describe the design and implementation of a 3x4 FP-SP array.

1. Introduction

The design and implementation of a 3x4 *Field Programmable Smart Pixel Array* (FP-SPA) is described. A *Smart Pixel* is an optoelectronic device that combines optical inputs and/or outputs with electronic processing circuitry, and is capable of being integrated into two-dimensional arrays. A *Field Programmable Smart Pixel* (FP-SP) is a smart pixel capable of having its electronic processing circuitry dynamically programmed in the field[1]. Hence, the optical and electrical I/Os of a FP-SP can be considered as the I/Os of an arbitrary finite state machine.

Programmable device arrays can eliminate the need for custom VLSI design, which is a lengthy and costly process. FP-SPAs can also be made compatible with standardized I/O pitches, packaging assemblies and optomechanical support structures[1]. The development of the FP-SPA described here is supported by the *Canadian Institute for Telecommunications Research* (CITR) through its project on Optical Architectures[3].

2. FP-SPA design

The described FP-SPA consists of a 3x4 array of programmable smart pixels and a control RAM. The I/O ports of a single pixel are shown in fig. 1. The pixel has four sides, *N, S, E, W*. Each side has 1-bit wide electrical I/O ports where e.g. *W.in* denotes an electrical input port on the West side. *H.B* and *V.B* denote horizontal and vertical broadcast ports respectively. *Opt.in.1* and *Opt.in.2* are two optical input windows, and *Opt.out.1* and *Opt.out.2* are two optical output windows.

As shown in fig. 2, the individual FP-SP implements an arbitrary finite state machine by using D-Flip Flops, 8-1 multiplexers (MUXs) and 2-1 MUXs. The 8-1 MUXs are used to realize arbitrary combinational logic functions. Logic variables are connected to their select lines and control RAM bits are connected to their input lines. The individual pixels can be programmed to implement different functions by changing the content of the control RAM.

3. FP-SPA technology

The FP-SPA is implemented using AT&T's CMOS-SEED Technology.[2] This technology can currently integrate dense silicon CMOS (0.8 μm CMOS) with dense GaAs optoelectronics (28,000 SEEDs/cm^2) and operate at rates greater than 500 Mb/s. To improve the device's optical detection capability, its *optical contrast ratio* is increased by using *differential optical signaling*. This requires 8 SEEDs/pixel, which is equivalent to a density of approx. 7300 SEEDs/cm^2. A single pixel (shown in fig. 3.) is implemented using approx. 670 transistors. The 2x2 mm FP-SPA (shown in fig. 4.) is implemented using approx. 10,000 transistors.

4. Simulation results

Spice simulation results are shown in figs. 5, 6. In both figs., a single pixel has an electrical input signal, simultaneously directed to one of its optical and one of its electrical output ports. In each fig., the choice of the output ports is user programmed by setting the appropriate bits in the control RAM. These simulations operate at a clock rate of 250 MHz.

5. Conclusion

The design and implementation of a CMOS-SEED FP-SPA have been described. The device has been submitted to AT&T for fabrication. Some Spice simulations operate at a clock rate of 250 MHz. Electrical and optical measurements, added to system level applications, will start once the physical device is available. A more aggressive FP-SPA design is now under development[3].

6. Acknowledgments

This research was supported by NSERC IRG OGP0121601, the CITR through Project 95-3-4 on Optical Architectures and ARPA (for the fabrication of the device).

7. References

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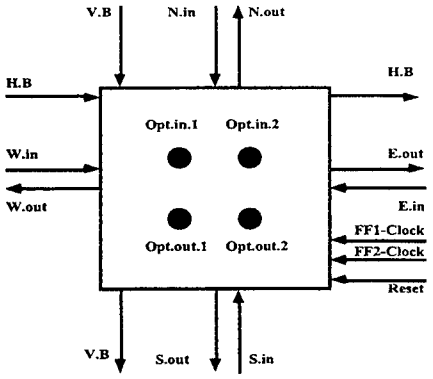


Figure 1. I/O ports of a single programmable pixel

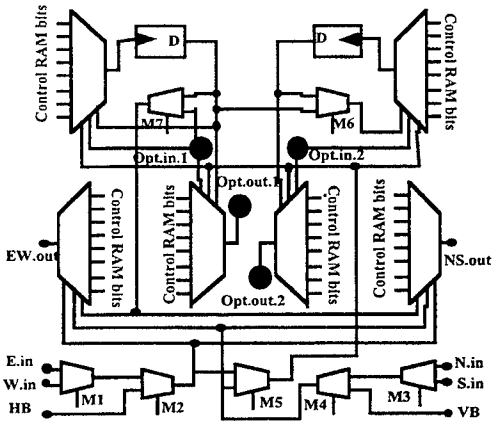


Figure 2. Schematic of a single programmable pixel

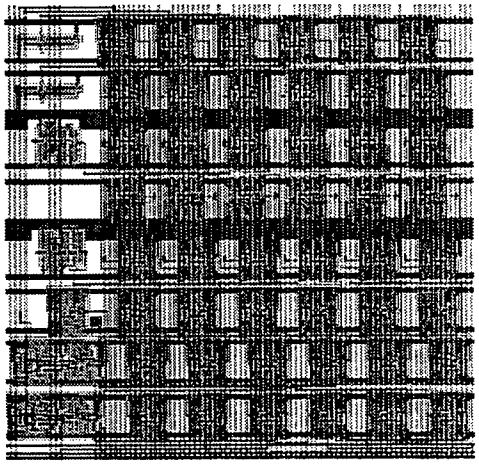


Figure 3. Implementation of a single programmable pixel (0.3x0.3 mm)

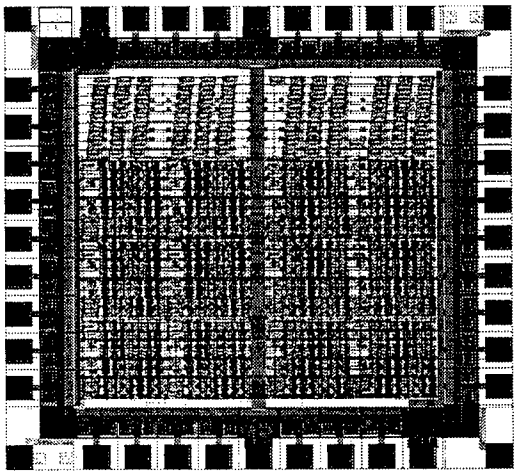


Figure 4. Implementation of the 3x4 FP-SPA (2x2 mm)

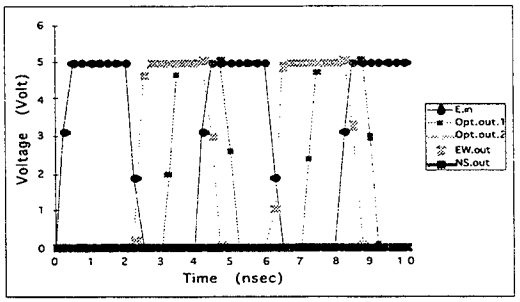


Figure 5. Spice simulation result showing E.in directed to EW.out and Opt.out.1. We note that the values of NS.out and Opt.out.2 are zero.

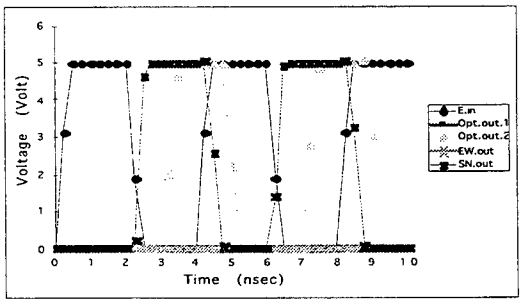


Figure. 6. Spice simulation result showing E.in (Same input in fig. 5) directed to NS.out and Opt.out.2. We note that the values of EW.out and Opt.out.1 are zero.

4:00pm - 4:15pm
ThB8

Hybrid CMOS/SEED Smart Pixel Array for 2-D Parallel Pipeline Operations

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We are developing a free-space digital optics (FSDO) system using hybrid CMOS/SEED technology to demonstrate 2-D parallel pipelining of digital computing and interconnection operations. This system optically moves 2-D arrays (frames) of digital data between chips containing mesh-connected smart pixel arrays (SPAs). The smart pixels perform electronic digital operations on the incoming data frames and/or data frames stored within the pixels. The chip design is flexible in that it can provide conversions between 1-D electrical and 2-D optical data formats, data frames manipulation and computations, optical 2-D parallel transfer of data frames and serial-parallel conversion. We have designed an optomechanical system that will house CMOS/SEED chips to construct a 2-D pipeline processor. The smart pixel design is based on the digital optical cellular image processor (DOCIP[1]) architecture which excels at performing image processing algorithms and other data-level parallel problems. We have targeted several applications in image processing and simulated the implementation of algorithm on our smart pixel chip.

The CMOS/SEED chip contains a 5 × 10 array of 250 × 125 μm^2 smart pixels. This chip is being fabricated through the ARPA/AT&T sponsored Hybrid CMOS/SEED CO-OP workshop. Each smart pixel contains 182 transistors, two MQW devices operating as a detector and two MQW devices operating as a modulator. Figure 1 shows the pixel layout with each of its functional regions. The smart pixel operation is based on binary image algebra (BIA)[2], which breaks down complex data manipulation algorithms into three basic operations: complement (logical NOT), union (logical OR) and dilation. The complement and union functions operate on bit values stored within the pixel's three-bit memory. The pixel performs the dilation function by OR'ing together one or more bits stored in its four neighboring (mesh-connected) pixels. A data bit enters the pixel either by electrically shifting from a neighboring pixel or by optical detection. Likewise, data can exit the pixel electrically through a neighboring pixel or optically through a pair of SEED modulators. The optical signals are dual-rail intensity encoded, thereby using two SEEDs for detection and two SEEDs for modulation.

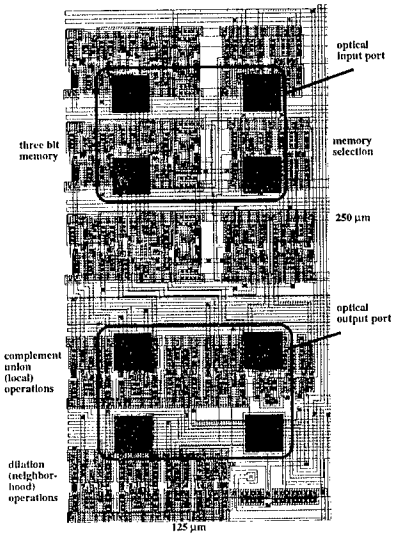


Figure 1: Layout of CMOS/SEED smart pixel. The pixel contains a three-bit memory, logic for complement, union and dilation functions; a one-bit optical input port and a one-bit optical output.

We have simulated high level image processing algorithms on the SPA. Figure 2 shows the implementation of the BIA algorithm for edge detection on our CMOS/SEED SPA. The block quantizer splits the original image into data frames of size 5 × 10 to match the size of our SPA. Each of these frames are then operated on by four BIA commands; the dilation with a reference image, two complements and a union. These four BIA commands require only three clock cycles on SPA chip to compute the edge detected image shown on the right. This is a huge reduction compared to the number of clock cycles required in a serial processor. We have also simulated efficient realization of image motion estimation and other algorithms.

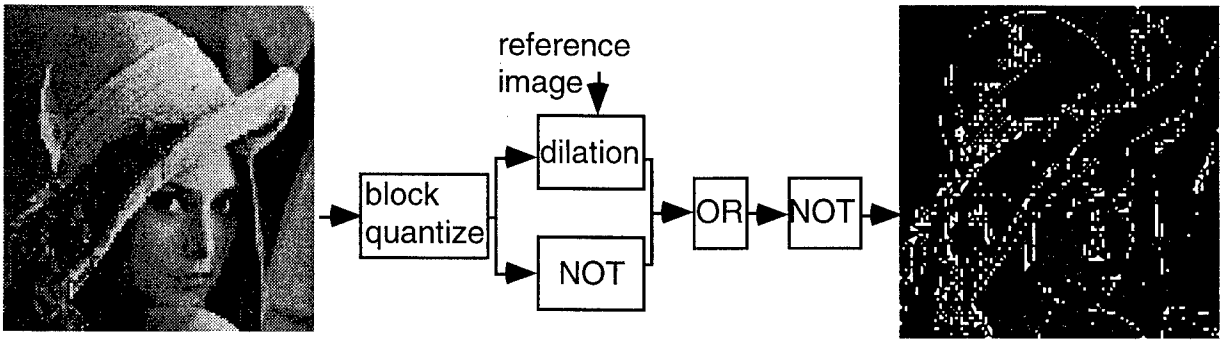


Figure 2: The image on the left is block quantized and processed in three SPA clock cycles to compute the edge-detected result on the right.

We plan use our SPA chips to create the 2-D parallel pipeline system shown in Figure 3. The first SPA formats an optical frame of data by converting incoming data from a 5-bit wide 1-D electrical format into a 5 × 10 bit 2-D optical format. Once the frame is composed, it is transferred optically in a single clock cycle to the next SPA. The intermediate SPAs perform logic operations on the frames and optically pass them along to the final SPA. The last SPA converts the 5 × 10 bit 2-D optical format back to the 5-bit wide electrical format. The pipeline architecture allows the intermediate SPAs to perform logic operations and data format conversion simultaneously. We will demonstrate the high speed implementation of the algorithms discussed above.

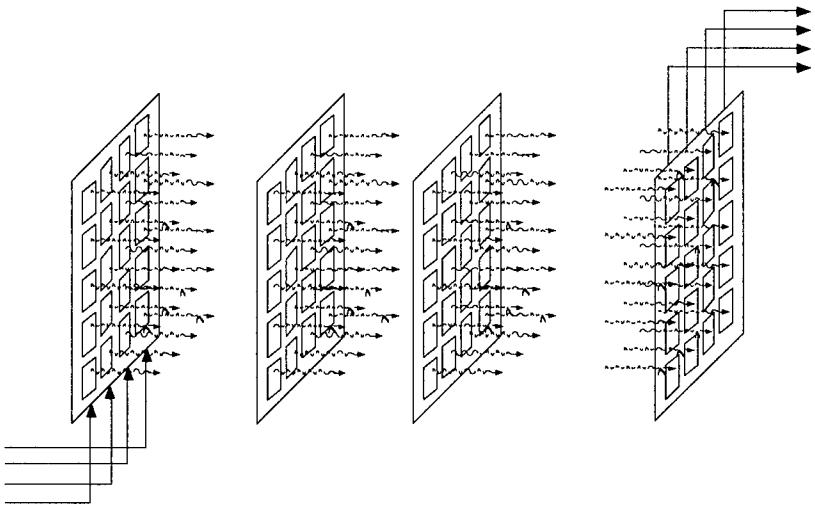


Figure 3: 2-D parallel pipeline architecture. The first SPA chip (on the left) provided electrical to optical conversion and buffering. The intermediate SPA chips perform logic operations on optical data frames. The final SPA chip converts the optical data back to electrical form.

We have also developed an optical module that images the optical modulators of one SPA onto the optical detectors of another. This module will be replicated for each SPA chip in our pipeline system. The general architecture in Fig. 3 can be adapted for many other computation intensive tasks such as photonic packet switching and page-oriented memory interfaces.

Acknowledgment - This research was supported by the National Center for Integrated Photonic Technology (NCIPT) program funded by ARPA under Contract No. MDA972-94-1-0001 and by the Joint Services Electronics Program through the Air Force Office of Scientific Research under Contract F49620-94-0022.

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4:15pm - 4:30pm
ThB9

Vizualization, extraction and simulation of smart pixel circuits in three dimensions

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Introduction

The effects of an increase in the parasitic capacitance on the performance of any electronic circuit are primarily two fold. Firstly, any such capacitances have to be charged and discharged leading to increased power dissipation. Secondly, any such capacitances between nodes lead to crosstalk and the possibility of noise (in the analog case) or bit errors (in the digital case). For VLSI circuits modern technology uitilises multiple metal interconnect layers (increasing the number of parasitic capaciors in a circuit) and operates at ever higher frequencies (increasing the value of each of the capacitors present). Thus there exists a requirement for precise capacitance extraction in order to allow the accurate modelling of circuit performance. This is particulary true for silicon based smart pixel technology.

As silicon based smart pixel technology has advanced, the three dimensional (3-D) topographic nature and complexity of the interconnect requirement has increased to the point where the technology has outstripped the capabilities of the conventional circuit extraction software. This is particularly true in at least two applications in which the authors are currently working. The first occurs where custom layers are added to a silicon wafer, as in the planarization of FLC/CMOS SLMs [1], or where different semiconductor technologies are combined, as in flip chip bonding of SEED/CMOS SLMs [2]. In each case the additional custom layers are not handled by the circuit extractor and yet can have a significant effect on circuit performance. The second occurs where "vulnerable" signals are present on nodes within a smart pixel circuit, and in particular where those nodes extend over several of the interconnect layers thus being exposed to parasitic capacitive coupling on several levels. Two extreme examples are (i) capacitive storage nodes at the output of a FLC/CMOS smart pixel [1]which, by definition extend from the bottom (active area) layer to the top (metal mirror) layer of the pixel circuit and (ii) nodes at the input of SEED/CMOS smart pixels [2] which have to conduct small, high frequency analogue signals through the layers of interconnect to the underlying high sensitivity amplifier circuit.
In this paper we briefly describe a custom software package which allows (a) the vizualization of microelectronic and micro-mechanical structures in 3-D, and (b) the accurate extraction of capacitances .We explore its initial application to a smart pixel circuit of type (i) as described in the previous paragraph.

3-D capacitance extraction

It is important in general to obtain as good an estimate as possible of the interconnect capacitances in a smart pixel. In order to achieve this, a 3-D capacitance simulator can be used, [eg, 3]. However, such software requires as input a description of the area of circuitry under consideration in a 3-D format. Furthermore, in order to achieve results which are realistic, the 3-D circuit description must be realistic. Specifically, for the process used in producing our pixel, the description of each layer should take account of the topography of underlying layers. Such a description can be acheived using software developed in-house at Edinburgh University - 3DTOP [4]. The software is designed for compatibility with a suite of industry standard device and circuit simulation software [5]. Figure 1 shows the 3D description of the circuitry up to and including layer metal 2. The circuitry is displayed without the inclusion of dielectrics for the sake of clarity. Any dielectrics used after this stage are planarised, so the effect of preceding layers on the topography of layers metal3 [M3] and metal4 [M4] is minimal - M3 and M4 are effectively flat.

Application Example

The example we use here is that of a single transistor pixel for a ferroelectric liquid crystal over silicon SLM. We choose this example because of the relatively simple nature of the circuit (if not its 3-D implementation). The circuit is shown in fig 2.

The final FLC/CMOS device has 4 metal layers. Metals 1 and 2 are used primarily for east-west and north-south bus lines respectively in the array; M4 is used for the top-level optically-flat mirror while M3 is a ground plane which complements M4 with a slight overlap in order to minimise the amount of light reaching the silicon substrate. M3 and M4 are applied in a custom post-processing technique. Conventional circuit extraction of parasitic capacitances is not available for M3 and M4 and is not sufficiently accurate for M1 and M2.

With regard to figure 2, several of the parasitic capacitances are key to the performance of the pixel and overall device. The role of Csub is well

known [1,6] as is the requirement to ensure that it stores sufficient charge in relation to the Ps of the FLC. C1 robs the mirror,M, of some of its charge as a falling edge on the row line pulls down the mirror potential at the same time as it isolates the mirror. C2 causes noise on the mirror node as the data bus line switches. C3 is a significant factor in determining the overall power dissipitation of the device [7]. A typical design goal would be to maximise Csub while minimising C1 and C2.

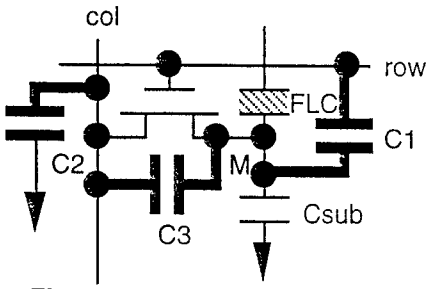


Figure 2. Pixel circuit schematic (parasitic capacitances in bold)

We carried out an analysis of a current single transistor pixel layout. We extracted the parasitic capacitances using the capacitance extraction routine available within our VLSI design suite and using 3D-TOP. The result, see Table 1, was that, in all cases 3D-TOP produced higher values of capacitance than the conventional extraction Results varied from 1% higher for essentially planar structures to 80% higher for complex topographic structures.

Name	Conv'l	3D-TOP	Diff
	fF	fF	%
ΔCsub	4.85	5.61	16
C1	2.86	2.89	1
C2	0.70	1.29	84
C3	1.36	1.68	22

Table 1. Comparison of extracted parasitics for Conventional and 3-D TOP methods.

At the conference we will present further results of the capacitance extraction and simulations detailing the effect on circuit performance.

Conclusions

Table 1 shows that, by considering planar capacitances only, conventional extraction consistently underestimates parasitics. 3D-TOP takes full account of the 3-D nature of the circuit and is thus particularly suitable for use in smart pixel design for hybrid (SEED/CMOS and FLC/CMOS) technologies.

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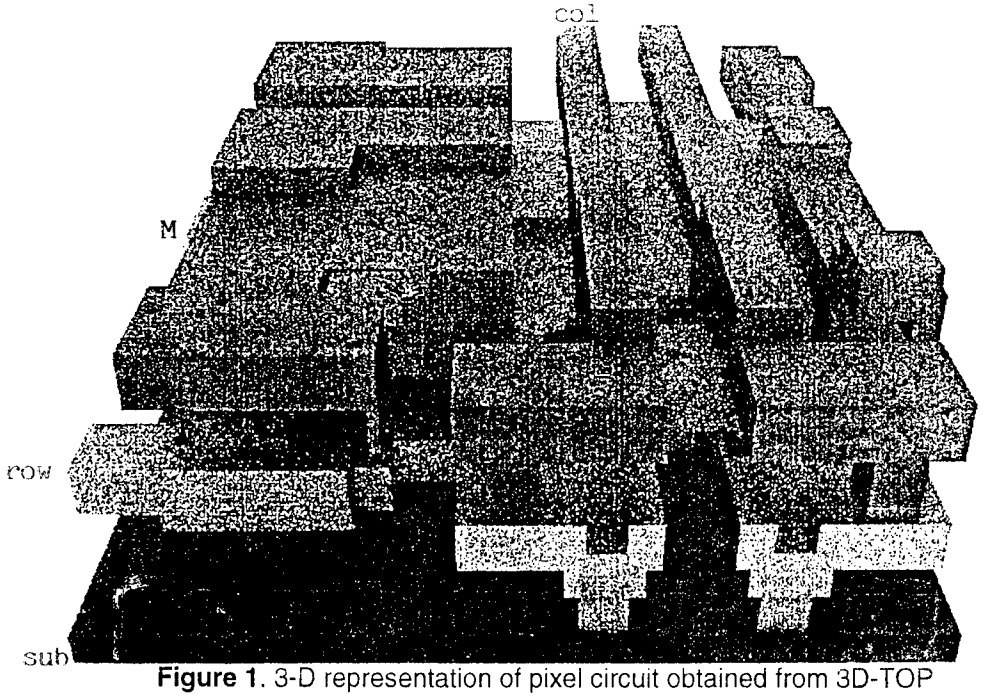


Figure 1. 3-D representation of pixel circuit obtained from 3D-TOP

4:30pm - 4:45pm
ThB10

A CMOS Chip for the 3-D Optoelectronic Computing System

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The 3-D computing system, as shown in Fig. 1, consists of two optoelectronic arrays, interconnect holograms, a host interface board, and a host computer. Using such free space optical interconnections will lead to more crosstalk-free and higher density interconnection channels, easier replacement of defective arrays, and easier multi-chip module implementation than electronic interconnects.

Each optoelectronic array includes an 8 x 8 vertical cavity surface emitting laser (VCSEL) array and a CMOS chip. Fig. 2 shows the block diagram of the CMOS chip, which is composed of an 8 x 8 photoreceiver array, an 8 x 8 signal processing array, an 8 x 8 VCSEL-driver array, and an array of connection pads which are used for flip-chip bonding. The photoreceivers detect the input optical signals emitted by VCSELs on the other photoelectronic array and then diffracted by a hologram. The detected signal is then processed by an electronic processing element (PE). The output signal from the PE is sent to a VCSEL-driver which determines the VCSEL's ON/OFF states.

The photoreceiver, as shown in Fig. 3, consists of a p-n junction photodiode, a current mirror amplifier, and two voltage comparators. The first comparator is used to convert the analog signal to a digital signal, and the voltage Vt1 can be adjusted to adapt to different incident optical powers. When the incident optical power is modulated at a frequency higher than 10 MHz, the output voltage from inverter buffer B2 may be less than 5 V for the ON state. The second comparator is used to achieve a 5 V output when the incident optical signal is modulated higher than 10 MHz. The PE, including a control logic circuit, is the most complex part of the optoelectronic array. Fig. 4 shows the block diagram of the PE. It consists of an arithmetic logic unit (ALU) which is comprised of several NAND logic units, a logic circuit which can perform 16 logic functions, a full adder, a 32-bit shift-register, 6 static registers (A, B, C, K, M, P), and some control circuits. The Global-OR signal taken from the data bus is used to monitor the calculation progress inside the PE. Due to a space limit on the chip, we did not design the RAM memory on the chip, but instead used an external RAM memory. The VCSEL driver consists of two logic inverters and a pass gate. The passing current through the gate to the VCSEL can be adjusted by adjusting the gate voltage. The advantage of this circuit is that there is no power dissipation in the OFF state.

Three test chips were fabricated using a 2-um CMOS process through MOSIS and were characterized. The test results show that the photoreceiver can respond to an incident optical power of 100 uW at 14 MHz modulation. The PE functioned as expected and can be operated at a frequency of 20 MHz. The VCSEL driver can provide a current as high as 15 mA and can work at 15 MHz. We have submitted the chip layout to MOSIS. The final test results will be presented in the conference.

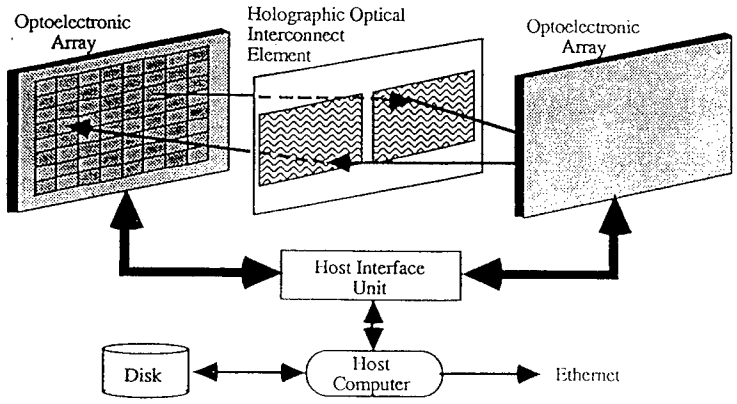


Figure 1. Conceptual illustration of the 3-D computing system.

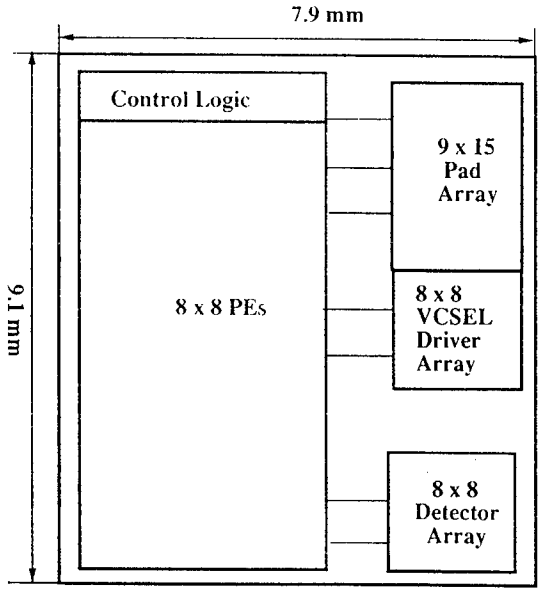


Figure 2. The CMOS chip layout diagram.

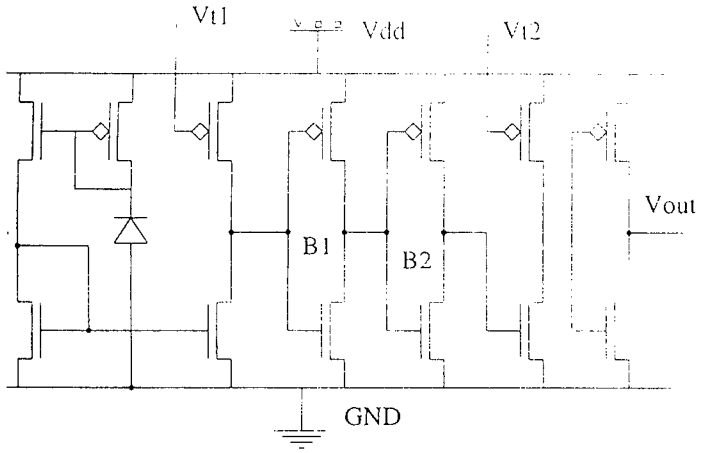


Figure 3. The photoreceiver circuit.

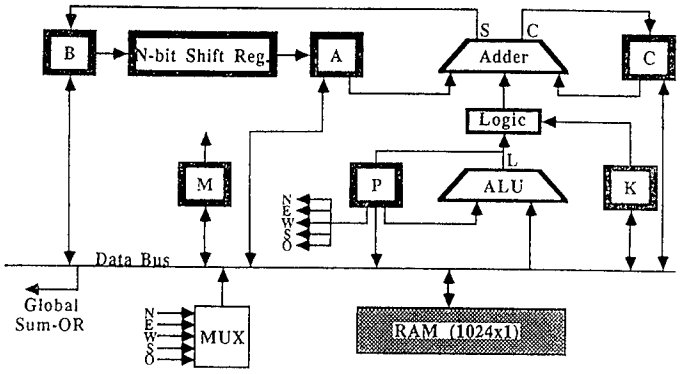


Figure 4. The function diagram of the signal processing element.

4:45pm - 5:00pm
ThB11

A NOVEL SMART PIXEL NETWORK FOR SIGNAL PROCESSING APPLICATIONS

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The growing interest in optoelectronic devices over the past five to ten years has led to significant progress in smart pixel systems based on hybrid optoelectronic architectures. Optoelectronic circuits are capable of improving the performance of computing and signal processing applications that are subject to the input/output and interconnection limitations characteristic of large scale electronic systems. Optics offers the opportunity for high-speed, parallel throughput, while complementary electronics offers information processing on a pixel-by-pixel basis. Taking advantage of the versatility of silicon integrated circuits and the developing flip chip bonding technology, we have designed a smart pixel neural network for digital image halftoning applications and implemented the electronics portion of the system in CMOS.

Digital image halftoning can be thought of as an image compression process whereby a continuous-tone, gray-scale image is printed or displayed using only binary pixels. One approach to digital halftoning involves local diffusion of error associated with a nonlinear quantization process, along with appropriate filtering to improve system performance. Classical error diffusion is a one-dimensional , serial technique in which the algorithm raster scans the image from upper left to lower right and, as a result, introduces visual artifacts. Optical implementations of such an algorithm can be two-dimensional and symmetric as multiple quantizations may occur simultaneously and in parallel. Image quality is improved as visual artifacts associated with one-dimensional error diffusion are reduced or eliminated. Key to most halftoning processes is the manner in which error is weighted and diffused throughout the image.

We have developed an optoelectronic implementation of an error diffusion algorithm that promises greatly reduced visual artifacts and overall improved image quality. This *error diffusion neural network* is based on electronic smart pixel neurons that detect and process incoming optical information, diffuse the error signals, and provide optical outputs. In contrast with most other techniques which are limited to local distribution of error, the smart pixel error diffusion neural network provides full connectivity across the entire image. Error output from the thresholding process at each pixel is distributed to neighboring pixels based on weighting factors determined by the desired functionality of the algorithm and the size of the neural network.

The integrated circuit shown in Figure 1 was implemented in 0.8 micron CMOS. The neural network is designed to compute quantization decisions in parallel and, with proper distribution of error, improve the quality of halftoned images. Optical inputs and outputs are via a 5 x 10 array of multiple quantum-well self-electro-optic-effect devices (SEEDs) flip-chip bonded to the silicon chip at the metal3 level. The pitch of the array is 250 microns. Each of the 25 cells in the 5x5 array is a smart pixel composed of a signal processing neuron and corresponding weighting and feedback interconnect circuitry. Every cell is custom designed for a particular position in the network such that the error current is properly weighted and distributed to appropriate neighbors. Although error diffusion occurs in two dimensions, wrap-around is unnecessary for the algorithm to achieve full functionality. The central smart pixel, with approximately 85 transistors, is the most complex due to the requirement to diffuse error to each of the other 24 neurons. The weighting and distribution system is the same for all other neurons, but as the pattern is shifted to the next location, a row of weights will fall off the edge, reducing the error diffusion requirement by up to five pixels. Thus, the simplest pixels can be found on the corners of the matrix where error is distributed to only the eight nearest neighbors.

The upper portion of the central pixel shown in Figure 2 contains the processing circuitry that is common to all neurons. The optical input from the SEED is converted to a current and passed through a summing node to the quantizer. The summing node adds the input signal to error signals from other neurons and feeds the result into the quantizer, which generates its own error from a comparison of input and output. The quantizer error is then transferred to other neurons via the weighting and interconnect circuitry, which occupies approximately 75% of the neuron area. The number of different weightings is fixed by the size of the array, but the distribution pattern must be custom designed for each neuron based on the location in the network.

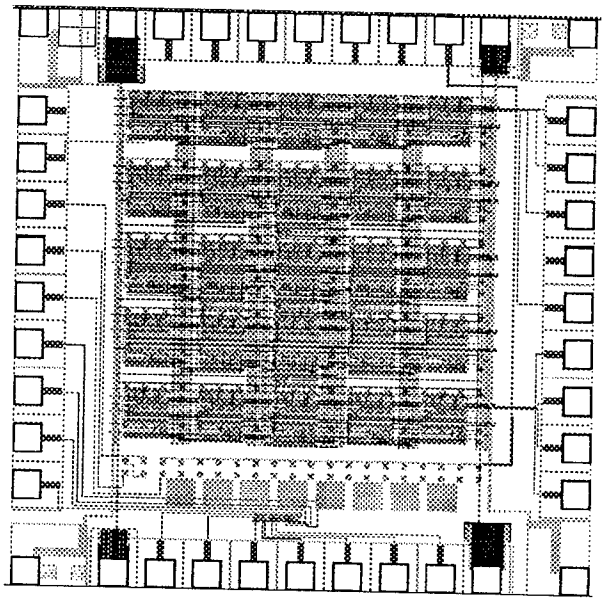


Fig. 1. Digital image hafltoning neural network.

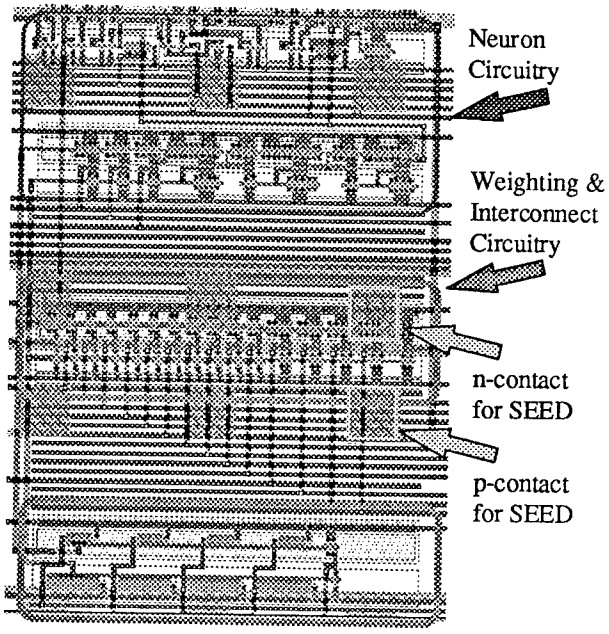


Fig. 2. Central smart pixel of 5 x 5 neural network.

The CMOS circuit in Figure 3 is an example of a weighting and distribution circuit for the most complex neuron in a 25 pixel array. Current mirrors are used to weight the error signal according to the distribution requirements derived from the image processing algorithm. In this case, a total of five different weightings are used to distribute error to 24 nodes. The weighting and number of duplicate circuits are as shown for each feedback circuit. Reasonably accurate weightings can be accomplished through careful selection of MOS device aspect ratios.

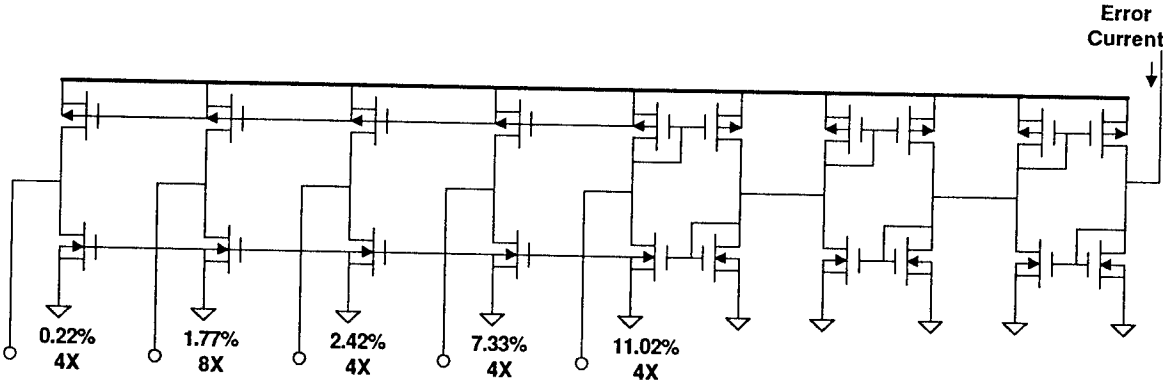


Fig. 3. CMOS error weighting and diffusion circuit.

This research work encompasses the theoretical foundations of digital image halftoning, the algorithm used as a basis for the 5x5 smart pixel array, and a full explanation of the approach taken for CMOS implementation of summing, quantization, error generation, and symmetric error diffusion. In a less rigorous manner, the operation of SEEDs as inputs and outputs in this particular application and the associated flip chip bonding issues are considered.

This research is supported by ARO, ARPA (CO-OP), and AT&T.

Friday, August 9, 1996

SESSIONS:

FA: Smart Pixels Architectures

8:30am - 9:00am (Invited)
FA1

Physical and Systems Motivations for Smart Pixels

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Holmdel, NJ 07733-3030

It is well known that systems made purely with electrical interconnections become increasingly difficult to design as the number, length, and speed of the interconnections must increase. Optics has many ways in which it can relieve these problems. Obviously, optics now dominates for all very long, high-bit-rate connections, as in the long-distance telecommunications network, and such fiber optics is likely to be increasingly used in shorter high-capacity networks. Smart pixels, however, offer a qualitatively new opportunity; they allow very large numbers of optical inputs and outputs (I/O) directly from chips. Current experimental chips have more than 2000 optical I/O channels [1]. This opportunity allows us to take advantage of yet further physical features of optics, all without sacrificing any of the benefits of digital electronic logic. As a result, smart pixels may allow new classes of systems, classes that do not suit the physics and technology of electrical interconnections.

All optical interconnections avoid the problems of distance and frequency dependent loss and cross-talk, and impedance matching and wave effects on electrical transmission lines, and provide ground isolation between different circuits. Smart pixels obviously offer two-dimensional parallel optical interconnections using "free-space" optics, allowing an "economy of scale" (e.g., one lens handles thousands of light beams), and also global interconnection topologies (e.g., perfect shuffles). Smart pixels are usually more tightly integrated than most previous optoelectronic circuits. This integration allows the less obvious benefit of reduction of power consumption for interconnections through "quantum impedance conversion" [2], a reduction that is now routinely observed in smart pixel transmitters and receivers. As a result of these various features, it now appears that we may be able to contemplate data rates in the Tb/s range on and off chips.

Another possibility in optics that has no direct counterpart in (baseband) electrical interconnections is the use of wavelength division multiplexing in which multiple wavelengths can be sent along one fiber or spatial channel. Such an approach has recently been demonstrated as an interconnection technique using smart pixels [3], allowing a linear array interconnect with one fiber, and based on the use of a short pulse laser as a multiwavelength source.

An important research question is how such new physical opportunities can be exploited in new systems, a question that is particularly timely given the recent advances in the technology (e.g., [1]). One point that has become clearer recently is that optics may allow "high-aspect-ratio" systems [4] [5]. "High aspect-ratio" means an interconnect (or even an architecture) with a high ratio of the length, ℓ, of the interconnection to the minimum cross-sectional dimension (or the square root of the cross-sectional area, A). A long thin cable or bundle of cables obviously has a very high aspect ratio, for example. Any system in which one unit (e.g., a chip, or a board) has to communicate directly with many others architecturally has a high aspect ratio because the connections must generally be long compared to the size of the unit. Examples of high aspect-ratio architectures include switching machines and multiprocessor interconnects. The problem that electrical interconnects have with high aspect ratios stems directly from the resistance of lines, and a relatively universal formula [5] gives an upper bound on the capacity of a simple electrical interconnect as $\sim 10^{15} A / \ell^2$, essentially independent of length scale. The number is

slightly better on-chip, and can be improved through use of equalization and coding techniques, though the scaling remains. (There are also various other phenomena that may prevent this limit being reached electrically.) Neither free-space nor fiber optics has any comparable "aspect ratio" limit. The existence of this electrical limit suggests that high capacity, high aspect-ratio systems are strong candidates for optics and smart pixels.

One difficulty with some smart pixel systems is that, though the smart pixel chips may have very high information I/O capacities, it is not clear either how to generate that information or to deal with it as an output, a problem reminiscent of the difficulty of drinking from a firehose. The smart pixel system, after all, must usually interface with the electrical world, with its limited I/O capacity. There are, however, several "firehose" architectures that may allow the smart pixel's capabilities to be exploited while allowing conventional input and output from and to electronics [6]. Examples include the "externally generated firehose" (as in a switching system fed from and feeding to multiple electronic input and output systems (tributaries)), the "internally generated firehose" (in which the problem is internally "fanned out" for parallel computation, with the final results being "fanned" back in), and the "internal recirculating firehose" (in which a moderate amount of input data is compared against a fixed, rapidly recirculating set of data). These classes of architectures could have various different applications.

Finally, it is worth noting that the progress of silicon technology is now "road-mapped" for many years ahead [7]. This road-map first of all allows us to see explicitly how interconnection becomes an increasingly great problem for electronics (even on-chip, where electrical interconnection works relatively well). Secondly, we can compare where smart pixel technologies (that work with silicon) may need to be if they are to allow full use of silicon technology in the future. Preliminary attempts to road-map such smart pixels are encouraging; it appears that the optical I/O may well keep up with the silicon scale and clock rate [8], and hence smart pixels may become a key technology in allowing us to exploit the future abilities of silicon electronics.

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[6] A. V. Krishnamoorthy and D. A. B. Miller, "Firehose architectures for free-space optically-interconnected VLSI circuits" (submitted to the Journal of Parallel and Distributed Computing)

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9:00am - 9:30am (Invited)
FA2

Smart Pixel Architectures for Image Processing

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Abstract

Smart pixel architectures offer important new opportunities for low cost, portable image processing systems. They offer greater I/O bandwidth and computing performance than systems based on CCD and microprocessors. However, finding a balance between performance, flexibility, efficiency, and cost depends on an evaluation of target applications. This applications-driven research combines integrated OE detectors with a high performance, flexible computing architecture to achieve a compact, efficient solution.

Summary

General purpose microprocessors offer inexpensive and versatile processing elements for a portable imaging system. Dedicated ASIC chips and chip sets offer high performance and efficiency. Unfortunately, many portable imaging applications (image enhancement, recognition, and compression) have requirements not met by either of the processors. The presented architecture is designed to provide a balance of characteristics for these applications.

	General Purpose Microprocessor	SIMPil	Dedicated ASIC
performance	low	high	high
cost	low	moderate	moderate
flexibility	high	high	very low
efficiency	moderate	high	high

Table 1: Characteristics of Microprocessors, Dedicated ASICs, and SIMPil.

This talk presents a demonstration prototype being developed at Georgia Tech to enable a new class of portable OE integrated parallel processing systems designed to efficiently process high-throughput image streams. This demonstration includes a focal plane SIMD architecture, *SIMPil*, that is currently being developed for use in videoputing systems such as high speed smart cameras. This prototype incorporates an integrated thin film detector, on-chip analog interface circuitry, and a powerful digital processor on a single Si CMOS chip. To illustrate the effectiveness of the SIMPil processing architecture, several image processing operations are demonstrated including edge detection, convolution, and image compression.

The SIMPil system combines features from both focal plane systems and image processing architectures. An integrated optoelectronic detector allows through-silicon wafer input of digital image data from a detector plane stacked above the processing plane, shown in Figure 1. By

reducing the image transfer bottleneck found in decoupled detector-processor systems, high frame rates are possible without constraining processing power. Processing area does not impact detector array fill factor.

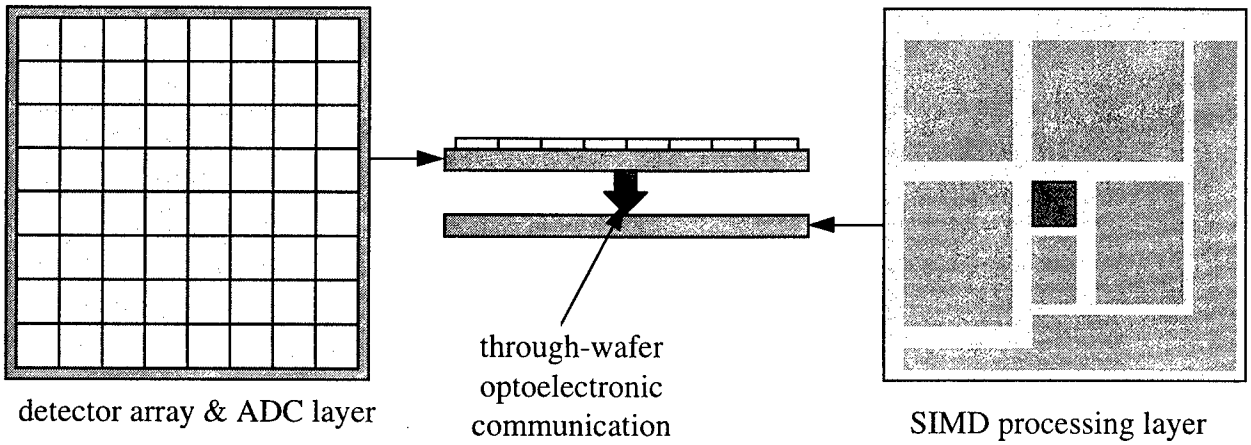


Figure 1: A Stacked Two Layer Focal Plane Processor.

Acknowledgments

This work is being supported by AFOSR, NSF Packaging Research Center (EEC-9402723), and the DARPA Low Power Electronics Program.

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9:30am - 9:45am
FA3

Fabrication and testing of AMOEBA: an opto-electronic switch for multiprocessor networking

A. V. Krishnamoorthy, J. E. Ford, K. W. Goossen, J. A. Walker, B. Tseng°, S. P. Hui°, J. E. Cunningham, W. Y. Jan, T. K. Woodward, R. G. Rozier, F. E. Kiamilev*, and D. A. B. Miller*

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*University of North Carolina, Charlotte NC

It is becoming increasingly clear that the interconnection of multiple general-purpose processors is an efficient and cost-effective means of achieving high-performance computing. In such distributed computing environments, the performance of the interconnection network typically represents a fundamental bottleneck, as electrical interconnect technologies struggle to keep pace with increasing demand for more connectivity and rapidly diminishing processor clock-cycle times. The demands made on the multiprocessor interconnection network include (i) high throughput communication (ii) low contention (iii) simple communication protocols. Additional features of low latency data transport and packet switched operation (potentially with variable-length packets or virtual circuit cut-through) may be desirable.

A number of photonic interconnect technologies are being investigated as candidates for a multiprocessor network. Performance, scalability, and cost will be critical. We are investigating the potential to build such an interconnection network based on fiber and surface-normal optical interconnects for data-transport and silicon VLSI for switching. We use an opto-electronic/VLSI technology [1] capable of supporting several thousand such optical devices with each device capable of bandwidths in excess of 1Gbit/sec. This technology enables sub-micron CMOS chips and full circuit and layout optimization typical of complex VLSI circuits, independent of the placement and bonding of the opto-electronic devices [2,3].

In this paper, we present a novel application of this technology to the AMOEBA switch: an Asynchronous Multiprocessor Opto-Electronic Bit-sliced Array switch. The AMOEBA switch is intended to function as a high-performance single-chip central switch on a data network serving multiple processors or computers in tightly coupled computing environments (single frame), loosely coupled environments (≤100m) and beyond (limited by fiber attenuation at 850nm). The purpose of the opto-electronic/VLSI chip is to provide byte-wide, switched optical interconnection at the processor clock rate (100MHz-1GHz). This switch uses multiple on-chip crossbars to connect N input channels with K bit-streams per input channel (i.e. K bits per byte) to N output channels with a corresponding K bit-streams per output channel (Figure 1). Each bit-stream is encoded as a separate optical I/O channel to the VLSI chip. We anticipate future networks comprising between 16-to-64 processors with 16-to-64-bit words operating up to 1GB/s/channel; this would imply a switch with up to 4Tbit/s throughput.

The input to the opto-electronic/VLSI multi-channel crossbar switch is composed of $N \cdot K$ beams of light that are imaged onto a two-dimensional array of $N \cdot K$ diodes that detect the incoming data bit-streams. The K bit-streams of data from each of the N input channels are then routed electronically to the corresponding output channels through an array of K NxN non-blocking crossbar switches. Each bit-stream of any one of the N given channels is fed to the input of a different one of the K crossbars. At each NxN crossbar, this bit-stream is switched to one of the N output bit-streams from that crossbar. The K bit-streams of each output channel are then collected from the corresponding K crossbars. The complete set of $N \cdot K$ output bit-streams are finally fed to a two-dimensional $N \cdot K$ array of MQW diodes that serve as output modulators. An important consequence of the architecture is that each of the crossbars can be identically configured, under the assumption that individual bit-streams of an input channel are destined to the same output channel. Hence a single controller designed for an NxN switch can be used to control the multi-channel bit-sliced crossbar switch that services $N \cdot K$ bit-streams. The controller determines the path for each input channel and configures all K crossbars to switch the bit-stream corresponding to that channel identically. Because of its reduced complexity, this controller can be incorporated onto the same chip. In addition, packet buffering (first-in, first-out buffers) and flow-control is incorporated into each channel. Thus, the data-buffers, switch-controller, and the switch can all reside on a *single* opto-electronic/VLSI chip with attached fiber arrays to deliver the input and output bit-streams to the detectors and modulators respectively. One possible implementation for the free-space-to-fiber interconnect interface is to use 2-D fiber arrays for the input and output connections [4]. Here we consider an attractive alternative that uses a combination of space-and-wavelength-division multiplexing with 1-D fiber arrays (Figure 2). The design and packaging of a novel optical interconnection system that provides an interface

to the 2-dimensional surface-normal modulators from 1-dimensional WDM fiber ribbons is described in [5]. Such a package would allow the use of each byte to be wavelength division multiplexed onto a single-mode fiber, allowing much higher bandwidth-distance products than multi-mode fiber solutions, thereby enhancing the scalability of the multiprocessor network.

We have built a 16-channel prototype of the AMOEBA switch in 0.8μm CMOS. Figure 3 presents the micro-photograph of the first-generation AMOEBA switch. The FIFO buffers, controller, crossbar switch fabric, and optical I/O circuits are shown. This chip incorporated 3-stage transimpedance receivers and transmitters with a maximum bandwidth of 550Mb/s [6]. Also provided to each input (output) channel is an optical end-of-packet signal, an optical Shift-in (Shift-out) signal, and an optical I-ready (O-ready) to control the input and output FIFOs and provide simple end-to-end flow-control. Each channel may operate completely independently of the others, at different bit-rates if necessary. The bits of a individual channel are assumed to flow through the switch in a synchronous manner. The chip incorporates an on-chip controller with serial connection set-up (estimated at 16M connections/sec) and parallel, one-step connection tear-down capability. The controller routes input channels to corresponding output channels based on a destination address contained in the first word of the data. This allows self-routing packet based switching with variable length packets. End-to-end flow control is established via FIFO interfaces at both input and output channels; each FIFO providing input-ready and output-ready signals for handshaking purposes as well as on-chip buffering of 16Bytes per channel. Initial testing have shown that optical data can be switched through the chip at 50Mbits-per-optical channel. The chip also incorporates electrically-addressed 1-D receiver and transmitter arrays that have been operated at over 100Mb/s-per-channel. These 1-D transceiver arrays are used by the processors (see Figure 2) to introduce data into the network.

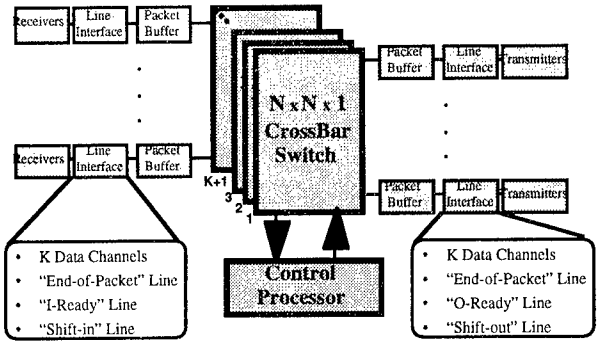


Figure 1: Architecture of the N-channel AMOEBA switch. Multiple crossbars (one-per-bit), line interfaces (FIFO-buffers), receivers, transmitters, and controller are incorporated into a single chip.

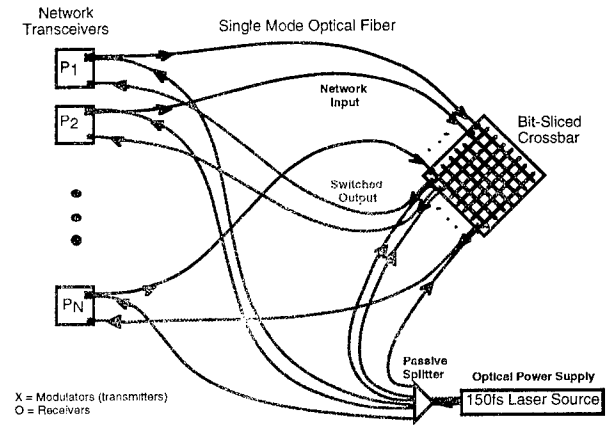
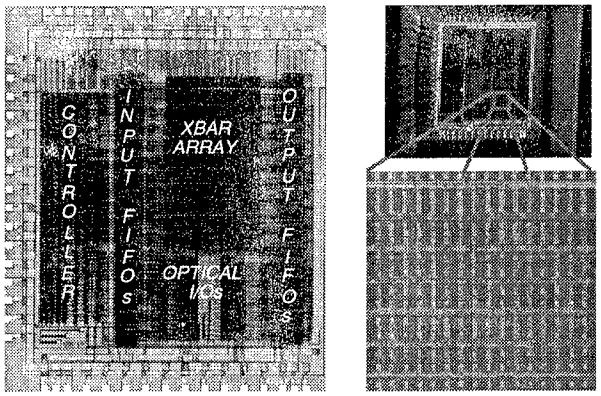


Figure 2: Architecture of a WDM/SDM multiprocessor network based on the AMOEBA switch. A short pulse laser is used as a broad-band WDM source. Processors P_X incorporate a 1-D transceiver array to transmit and receive bytes where each bit encoded on separate wavelength. Spectral bandwidth of current MQW modulators is ≈5nm (this may be increased with novel device geometries).



(a) (b)

Figure 3: (a) Microphotograph of the first generation AMOEBA switch (≈80K transistors) with 16 channels. (b) Portion of MQW device array bonded to the switch.

References:

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WDM / SDM fiber network design for the AMOEBA optoelectronic switch

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The interconnection bandwidth requirements for high performance workstations networks is constantly increasing. It will soon be cost effective to use optical fiber interconnection. Before long, it will be inescapable. The current approach to increased network throughput is to increase the data rate. But it is also possible to build a word-parallel network, where the data rate might match the processor clock speed. This avoids the high speed MUX and deMUX of data onto the network, and reduces synchronization requirements.

Most WDM networks assign one wavelength to each user. In this paper, we describe a network where each bit of a word-parallel link is carried on a different wavelength. Each processor node has an "transceiver" which can transmit and receive optical data on single mode fiber. The fibers are linked through a central switch. The transceivers and switch use CMOS/SEED technology, where MQW modulators and detectors are flip chip bonded onto the surface of silicon CMOS circuits. The center of the network is AMOEBA, an asynchronous multiprocessor optoelectronic bit-sliced array switch using K identical switches with optical input and output to route K-bit words.[1]

Figure 1 shows a WDM data transmitter using a short pulse laser as a broad spectrum source, free space optics to distribute the wavelengths, and a surface-normal modulators to apply the data signals. A 16 channel transmitter was demonstrated with FET-SEED modulators and a modelocked Ti:Sapphire laser.[2]

Figure 2 shows a WDM fiber-optic server, where the laser source and the AMOEBA switch could be housed in a single box. The network nodes are optically *passive*; with optical modulators rather than multiple wavelength-stabilized sources. A single short pulse laser to power the entire network's modulators. The output is passively split and distributed with one channel to each of the N transceivers and N channels to the switch. The output of each transmitter is connected to the switch inputs, and the switch outputs are connected to each receiver input. Each fiber carries data word-parallel using the WDM channels.

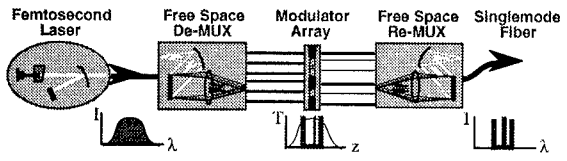


Figure 1: Short pulse WDM interconnection

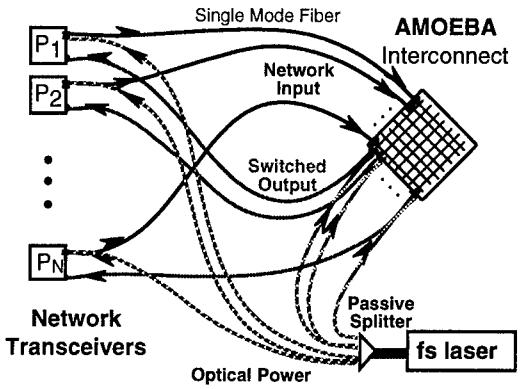


Figure 2: WDM crossbar network

Femtosecond lasers have been expensive and bulky, requiring high current water cooled pumps. Now, compact and inexpensive lasers have been demonstrated using diode pumped Cr:LiSAF with saturable Bragg reflector mode locking.[3] Such lasers should provide 100 mW of 850 nm output with 100 fs pulses at a 300 MHz repetition rate.

WDM provides access to a 1-D stripe of devices, but not the 2-D surface area of an optoelectronic chip. Figure 3 shows how 2-D access is gained using multiple SDM (space division multiplexed) fibers. For the transceiver, one fiber carries the data input signal and a second fiber carries the modulator power. The reflected output, carrying the data signals, can be collected into a separate output fiber using beamsplitting or pupil division multiplexing. The AMOEBA chip requires N inputs and N output fibers. These can be arranged in a single 1x2N array, or multiple 1-D fiber arrays (as shown) provided the separation considers the optical wavelength bandwidth.

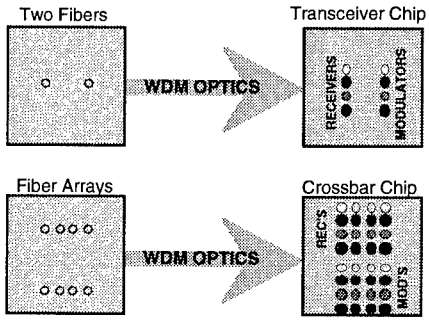


Figure 3: WDM demultiplexing geometry

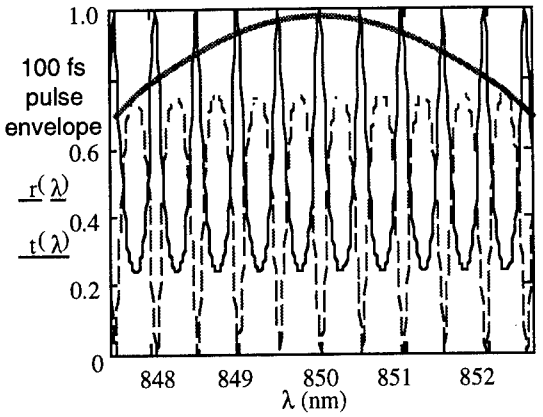


Figure 4: Spectral slicing beamsplitter

A fs source produces a continuous spectrum, but the modulators and therefore data channels are discrete. It is possible to allow the modulators to act as spatial filters, but because the substrate between the modulators has non-zero reflectivity, the wavelengths between data channels generate a DC bias which reduces SNR.

A simple technique for slicing the periodic wavelength channels out of the broadband input is to use a large-gap etalon. Figure 4 shows the transmission and reflection spectra of a 0.7 mm thick glass etalon coated with 50% reflective metal on both sides. The transmission is periodic in wavelength, with exactly the desired 0.5 nm spacing. This coating sends equal power into the reflected and transmitted beams. The approximate wavelength spectra of a 100 fs source is also shown. Increasing the etalon surface reflectivity sharpens the peaks and reduces the background level. For WDM transmission, it is possible to use a series of filters to take multiple slices from one source where each output reaches the same peak intensity

Figure 5 shows a simple optical system for the AMOEBA switching chip . The input, in the form of one or two stacked 1-D fiber arrays, is imaged onto the chip surface with a 2:1 demagnification. A 1200 lp/mm blazed grating in the Fourier plane separates the signal by angle, so that a 5 nm spectral band covers a 300 μm stripe. Demagnification helps interface CMOS/SEED modulators on a 70 μm pitch with 1-D fiber arrays fabricated using standard 850 nm 80 μm cladding diameter fiber and silicon / ceramic V-groove technology.

We have implemented a compact (7 x 4 x 2 inch) optomechanical package for the WDM transceivers (Figure 6). The optics use pupil division multiplexing to separate the input and output beams without 6 db beamsplitter power losses. The power and input signals are carried in a single 2.5 mm ceramic ferrule; the output is a FC connected fiber. Signals are distributed over a 300 μm active device area with a 1200 line/mm grating. The chip is held in a 84 pin ceramic package in a zero insertion force socket.

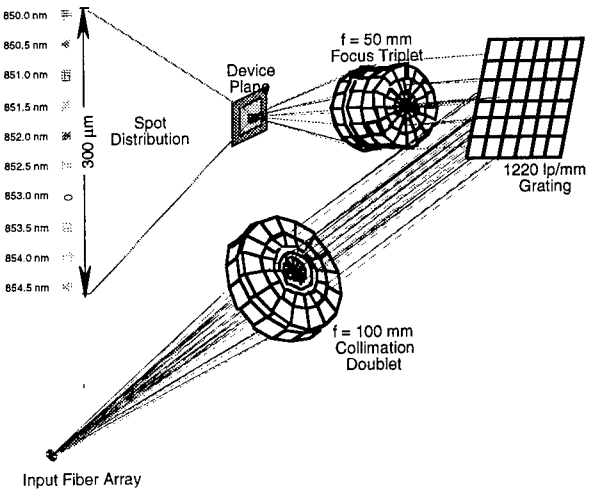


Figure 5: Crossbar optics layout

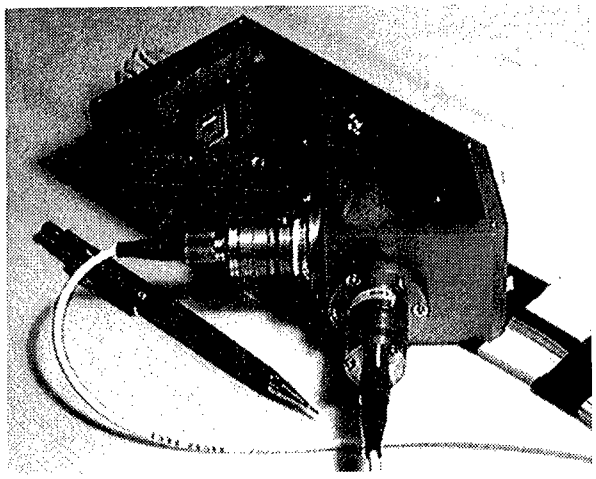


Figure 6: Packaged WDM transmitter / receiver

The transceiver package is designed to limit the number of optical adjustments. The central beam is steered to the corresponding modulator by the grating tip/tilt mount. The focus lens can be translated and locked in place. Finally the output signal is directed onto the core of the single mode output fiber using tip/tilt of the collimated fiber mount. Such a package could be engineering to mount directly onto a circuit board inside the workstation.

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2 E. De Souza, M. Nuss, W. Knox, and D. Miller, "Wavelength-division multiplexing with femto-second pulses," *Optics Letters* **20**(10) p.1166, 1995.

3 S. Tsuda, W. Knox, E. De Souza, W. Jan, and J. Cunningham, "Low-loss intracavity AlAs/AlGaAs saturable Bragg reflector for femtosecond mode locking in solid-state lasers," *Optics Letters* **20**(12) p.1406, 1995.

10:30am - 10:45am
FA5

A Buffered ATM *HyperPlane* Smart Pixel Array

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Abstract

The operation, design, and extensibility of a buffered ATM HyperPlane smart pixel array is presented. The CMOS-SEED device contains over 20,000 transistors on a 2 mm by 2 mm die.

1. Introduction

A brief motivation for the buffered ATM *HyperPlane*[1,2] smart pixel array (SPA) is presented. Details of the buffered ATM SPA architecture, operation, and implementation are then examined. Finally, the designed SPA is discussed in terms of extensibility to larger, more complex SPAs.

2. Contention in *HyperPlane* based ATM switches

In *HyperPlane* based ATM switches, many of the node channels of a given SPA operate in the extraction mode. That is, these node channels are attempting to extract ATM cells off the backplane via address recognition and to deliver them to the user. Since each node channel operates independently, it is possible that multiple ATM cells will arrive at the SPA simultaneously. Furthermore, the potential exists that two or more of these simultaneously arriving cells will have matching destination addresses. In this case, the destination SPA for these ATM cells will be required to extract multiple cells simultaneously. If the SPA is unable to do this, a collision occurs, at least one ATM cell is lost, and overall switch performance is compromised. One way to overcome this limitation is to add output queueing to the SPA. This enhanced SPA architecture allows ATM cells arriving simultaneously to be temporarily buffered before final delivery to the user. By using this strategy, the fabric cell loss probability is significantly reduced.

3. A Buffered ATM *HyperPlane* Smart Pixel Array

A CMOS-SEED SPA which includes output queueing has been designed and fabricated. Chip fabrication was provided through the CO-OP sponsored ARPA/AT&T Hybrid-SEED Workshop held in July 1995. A photograph of the chip and a corresponding layout template are shown in Figure 1.

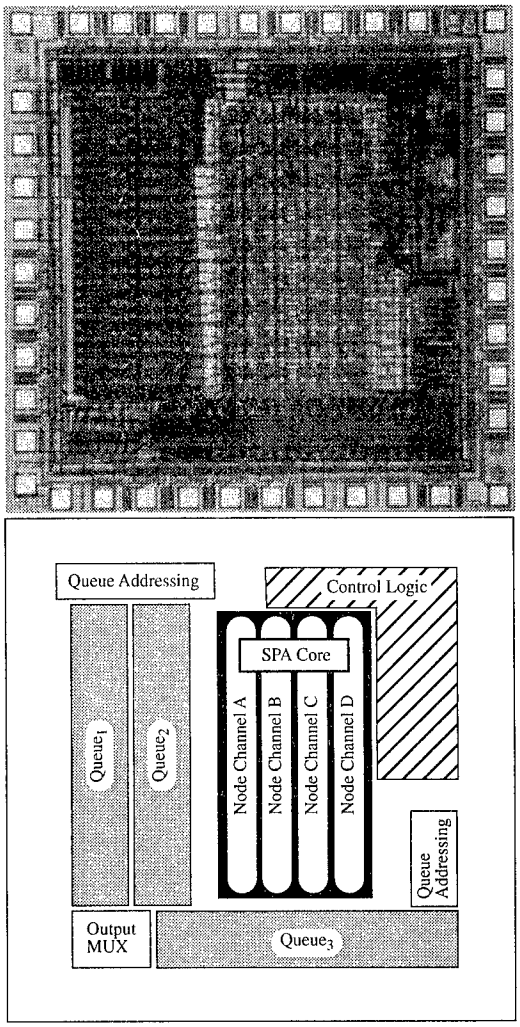


Figure 1. SPA photograph and layout template.

A brief discussion of the various SPA sub-circuits is given. The SPA core contains the individual smart pixels, each of which provides the electrical/optical interface for a single bit of data. The control logic arbitrates the flow of data into and out of the ATM cell queues. Each queue on the chip functions to buffer an entire ATM cell (53 octets of data). The queue addressing blocks are used by the control logic to place each octet of the incoming ATM cell into the queue at the appropriate location. The output multiplexer is used by the control logic to select which of the three queues writes output data to the electrical pinouts of the chip.

4. ATM Cell Loss Priority

Another feature of this Buffered ATM *HyperPlane* SPA is the utilization of the ATM standard's Cell Loss Priority (CLP) bit[3]. The CLP bit is a part of the ATM cell's 5-byte header, and identifies the cell as either high priority (CLP= 1) or low priority (CLP =0). For the cells sent on this *HyperPlane*, the CLP bit is included in the fabric header alongside the destination address of the cell. By including the CLP in the fabric header, extracting SPA node channels are able to determine not only a cell's destination address, but also the ATM cell's priority level. The CLP is then used to determine which cell(s) should be dropped in the event of a contention (e.g. when all the queues are full).

5. Control Logic Algorithms

Efficient SPA operation is dependent on the ability of the control logic to effectively arbitrate the on chip queueing. Each time a node channel receives a valid ATM cell header, it presents an extraction request to the control logic. The extraction request also contains the priority of the incoming cell. The control logic is then responsible for ensuring that the cell is queued and eventually delivered to the user. The algorithm followed by the control logic is presented.

The algorithm upon receiving an extraction request from a given SPA node channel:

1. Choose a queue for buffering.
   a) If a given queue is empty, extract the incoming cell into the empty queue.
   b) If all queues are full and the incoming cell has CLP=1, extract the incoming cell into a queue which contains a cell having CLP=0.
   c) If a suitable queue for extraction is not found from a) or b), the incoming cell cannot be extracted and is lost.
2. Mark the queue as full and note the priority of the cell being extracted.
3. Order the queue (with respect to the other full queues) for delivery to the user. A FIFO arbitration scheme is used.

The algorithm for delivering cells from the queues to the user:

1. Select the queue for cell delivery by using the FIFO ordering established during extraction.
2. Deliver the cell from the selected queue to the user.
3. Mark the queue as empty.

6. SPA Implementation

The buffered ATM *HyperPlane* SPA discussed has been fabricated in AT&T's 0.8μm CMOS-SEED technology[4]. The 4x9 SPA core is comprised of 4 node channels of 9 smart pixels each. Each smart pixel contains about 60 transistors. The state machine in the control logic has 21 latches which together determine the current state of the SPA and the three output queues. The total number of transistors on the 2mm by 2mm die is over 20,000. Differential SEED pairs are used for optical input and optical output. The SEEDs used have 18μm active areas on a 125μm by 62.5μm pitch.

Each queue is implemented as a sequentially addressed, dual-port SRAM. Each SRAM stores 424 bits (53 8-bit rows). The SRAM used is based on an 8 transistor static memory cell which occupies an area of 20.5 μm by 22.5 μm. The dual-port design of the SRAM allows for the simultaneous reading and writing of data so that latency in the queueing mechanism is significantly reduced.

The total number of transistors in the SPA core is approximately 2160 (= ~60 transistors/ smart pixel * 36 smart pixels). Thus, the number of transistors in the SPA core only comprises ~10% of the chip's transistors. Therefore, the metric of transistors per smart pixel does not accurately indicate the complexity of the buffered ATM *HyperPlane* SPA. It is useful then to define a new metric, the number of *effective* transistors per smart pixel, which more accurately expresses the complexity of this SPA. The number of effective transistors per smart pixel is defined as the total number of transistors on the die divided by the total number of smart pixels. For the buffered ATM SPA designed, this new metric gives ~550 effective transistors per smart pixel.

Extensive simulations were performed in the switch level simulator IRSIM to verify the SPA and the correctness of the control logic algorithms. In addition, the critical path was found and corresponds to a maximum clock frequency of 125 MHz. This gives an aggregate optical throughput of 4.5 Gbps (= 36 smart pixels * 125 Mbps per smart pixel) for the buffered ATM SPA.

7. SPA Extensibility

The buffered ATM *HyperPlane* SPA can also be utilized as a building block for larger, more complex SPAs. Used as such, the SPA presented here would be considered as a smart pixel cluster[5]. A 2-D array of these clusters would then comprise the new SPA. The construction of the clustered SPA is accomplished by tiling the buffered ATM *HyperPlane* SPA and then adding appropriate control logic. Also, another layer of queueing is needed, which changes the queueing characteristics of the SPA from the *KnockOut* behavior of the individual smart pixel clusters to a *CrossOut* characteristic across the clustered SPA. This change in queueing structure is accompanied by an increase in *HyperPlane* switch performance[1,2].

8. Conclusion

The design and simulation of an extensible, buffered ATM *HyperPlane* SPA has been completed. Future experimental testing will seek to verify the expected electrical and optical functionality and performance of the SPA.

9. References

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[2]. H. S. Hinton and T. H. Szymanski, "Intelligent Optical Backplanes," *MPPOI'95,* Oct. 23-24, 1995.

[3]. ATM User Network Interface Specification v. 3.1

[4]. K. W. Goossen et al, "GaAs MQW modulators integrated with silicon CMOS," IEEE Phot. Tech. Let., Vol. 7, 1995, pp. 360-362.

[5]. D. R. Rolston et al, "Analysis of a Microchannel Interconnect based on the Clustering of Smart Pixel Device Windows," To be published in Applied Optics.

10:45am - 11:00am
FA6

The Design and Interconnection of a Free-Space Photonic/Electronic ATM Switching Module

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1. Introduction

The high fan-out/fan-in capabilities of free-space optics are investigated when combined with a novel modulator/detector technology (known as opto-RAM) allowing highly parallelised optical read/write from silicon VLSI memory structures *[1]*. Such technology opens up the possibility of implementing highly connected ATM switching modules with reduced cross-office transfer rates. The technology is ferroelectric liquid crystal (FLC) light modulators embedded in standard VLSI circuitry. This enables the full capabilities of silicon VLSI electronic processing to be retained, and also to be enhanced by becoming optically accessible through highly parallel arrays of light modulators closely integrated into the silicon circuitry. This optical accessibility allows the incorporation of a degree of optical switching to assist the electronic switching. Light modulator switching speeds of the microsecond order mean that some of the available parallelism must be used to obtain the desired chip-to-chip transfer rate. Aggregate (switched) chip-to-chip bandwidths of at least several hundred Gb/s appear possible *[2]*. An optical-read opto-RAM cell, currently under development, is shown in fig. *1*.

2. Module Architecture

The module architecture (shown in fig *2* for a 16 x 16 switch) employs three stages of switching without internal queuing, and maps identically on to a three-stage Clos network *[3]*. The provision of redundant paths through the fabric enables low-blocking, high-performance ATM switching to be achieved, with all queuing taking place at the output stage. The first and third stages of switching are carried out within sectors of an opto-RAM, with the central switching stage carried out by a free-space photonic crossbar using a broadcast and select arrangement. Simulations and analysis show that an arbitrarily-low blocking performance may be achieved by the inclusion of additional memory locations on both the input and output opto-RAM planes. The purpose of the opto-RAM is three-fold: (i) to implement the first stage of switching by the selective writing of ATM cells into sectors of memory; (ii) to present a suitably parallel representation of the first-stage output to the centre-stage free-space optical crossbar; (iii) to receive a parallel representation of the data from the centre-stage crossbar and carry out the third-stage switching. The opto-RAM circuitry is almost identical to that of a standard CMOS VLSI RAM, except for the addition of liquid crystal modulators/integrated silicon photodetectors for optically reading/writing from/to memory.

3. Interconnection of Modules

To construct larger switches, we propose a novel approach based upon the interconnection of the above modules within an optical fibre harness. A simple delta network implementation of the fabric is shown in fig. *3* for a 32 x 32 switch comprising 4 component 16 x 16 output queued modules (small numbers chosen for simplicity of diagram), where each module has been drawn to explicitly show its Clos topology. ATM cells are optically routed across stage *1* of the fabric to one of the output memory sectors, where they are temporarily queued in electronic memory if contention arises for transfer to a given module in stage *2*. Following high-speed transmission from stage *1* to stage *2* by means of optical fibre, the cells are then switched by the stage *2* network. The network will be subject to loss and delay at both stages *1* & *2*. The queuing delay at stage *1* may be less than that at stage *2* since the servicing of the output buffers of the stage *1* modules (transmitting cells between the stages) is effectively equivalent to a number of single-servers operating in parallel.

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[2] *Nortel CASE award student*
[3] *Nortel Research Professor of Photonics*
[4] *Telecommunications consultant*

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[1] J.R. Collington, M.P. Dames, W.A. Crossland, R.W.A. Scarr, "Optically Accessed Electronic Memory"; to be published in a special edition of *Ferroelectrics*, 1996.
[2] M.P. Dames, J.R. Collington, W.A. Crossland, R.W.A. Scarr, "Three-stage, High-Performance Opto-electronic ATM Switch: Design and Performance"; submitted to *Optical Engineering*.
[3] J.R. Collington, M.P. Dames, W.A. Crossland, R.W.A Scarr, "Hybrid Free-Space Photonic/Electronic ATM Switching Using FLC/VLSI Technology"; *1996 International Topical Meeting on Photonics in Switching*, Sendai, Japan, 21-25 April 1996.

This work has been supported by the Engineering and Physical Sciences Research Council (EPSRC) under the Parallel Opto-electronic Telecommunications Systems (POETS) programme, grant reference GR/J44733.

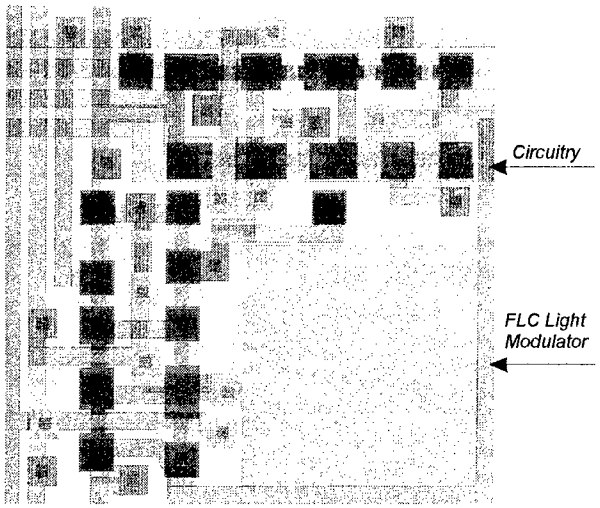


Fig.1: Opto-RAM Cell (single pixel)

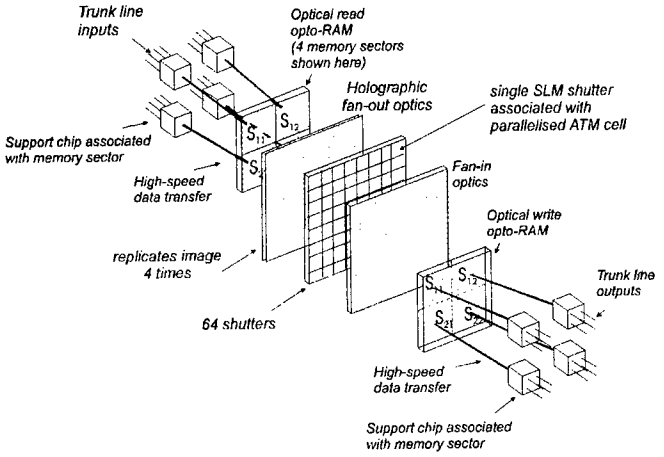


Fig.2: Three-stage output queued module (16 x 16 for clarity)

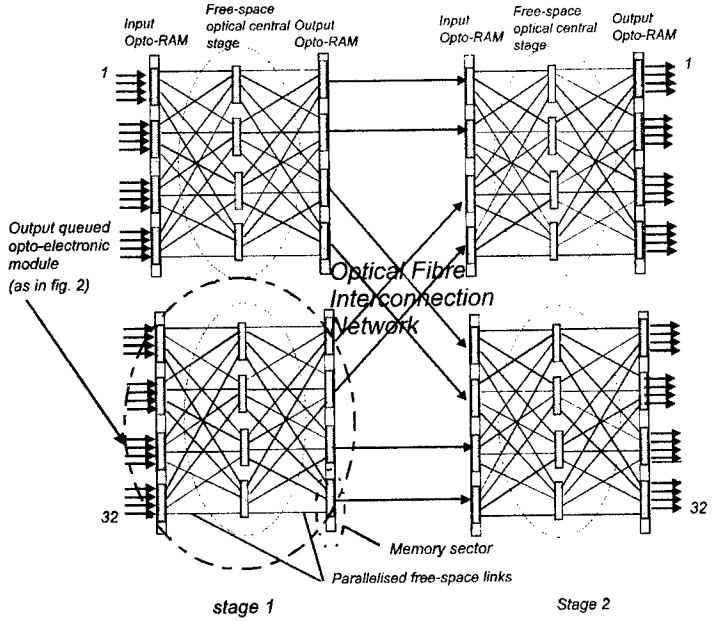


Fig 3: Optical fibre interconnection of output queued opto-electronic modules

8 X 8 Array of smart pixels fabricated through the Vitesse foundry integrating MESFET, MSM, and VCSEL elements

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Recently we have reported the successful operation of a database filter demonstrator system implemented with 4x4 hybrid arrays of vertical cavity surface emitting lasers and heterojunction phototransistors (VCSEL/HPT) configured as AND and XOR logic gates [1]. This system accepts page oriented inputs potentially provided by holographic or other massively parallel optical memory. Each logic gate array of this system is composed of two chips (an HPT array and a VCSEL array) connected together with wire bonds to traces on a ceramic submount. While this hybrid based smart pixel implementation allowed for a proof-of-principal demonstration, a device technology that provides greater pixel density, higher yield, and simpler packaging, which can be fabricated by an existing foundry is desirable for the next generation database filter demonstrator. This paper presents a new smart pixel design for the data filter which combines the four chips of the previous system into a single component chip. This eliminates many of the optical components, dramatically reduces the size of the system, and simplifies the optical alignment. The redesigned chip is being fabricated by Vitesse through the MOSIS foundry and uses MSM photodetectors and MESFETs instead of the HPTs. The VCSELs are flip-chip bump bonded to each pixel using a coplanar bonding technique similar to that developed by Goossen, et. al.[2] for the SEED devices. The paper will describe the pixel design and measured characteristics.

The 8 x 8 pixel array is monolithically integrated on a single 2.5mm x 2.5mm integrated circuit. A pixel and array layout are shown in figure 1. The pixel is made up of 3-50μm X 50μm MSM photodetectors, 2-input AND and XOR gates made up of enhancement mode MESFETs with depletion mode MESFETs as active loads, a 4 stage current step-up (width of 12μm to 360μm for a 15mA max current) to drive the VCSEL, and the VCSEL bonding pads with dimensions of 40μm X

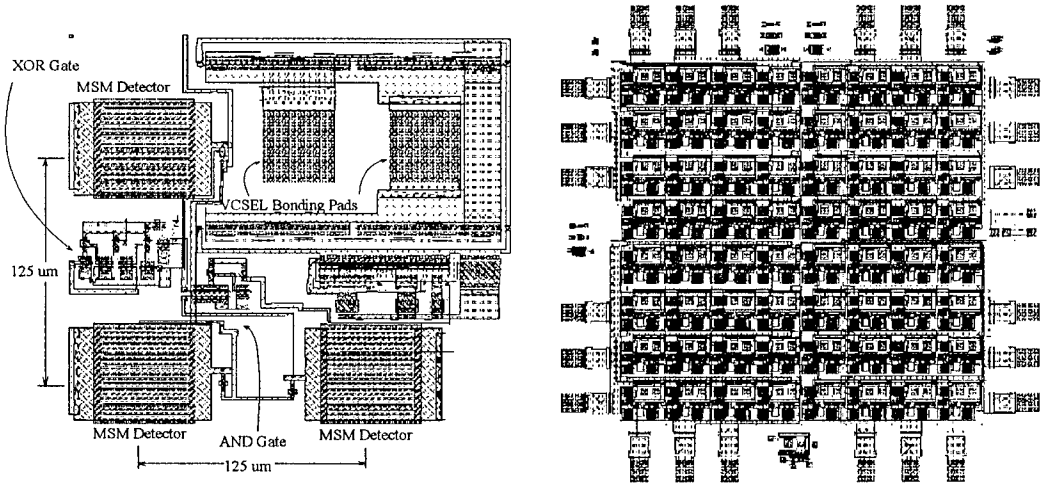


Figure 1: Pixel and 8x8 array of pixels layout

40μm with a 30μm space between pad edges, with 25μm spacing to allow the flip-chip bump bonding (all of which are being fabricated by Vitesse). Figure 2 shows a block diagram of the basic function of the pixel. The data and projection mask are the optical inputs to the XOR gate. The output of the XOR is ANDed with the selection mask optical input. The optical inputs are directed into the MSM detectors. The output of the pixel is the VCSEL which are fabricated to meet our requirements for the flip-chip bonding to the 8 X 8 array of smart pixels.

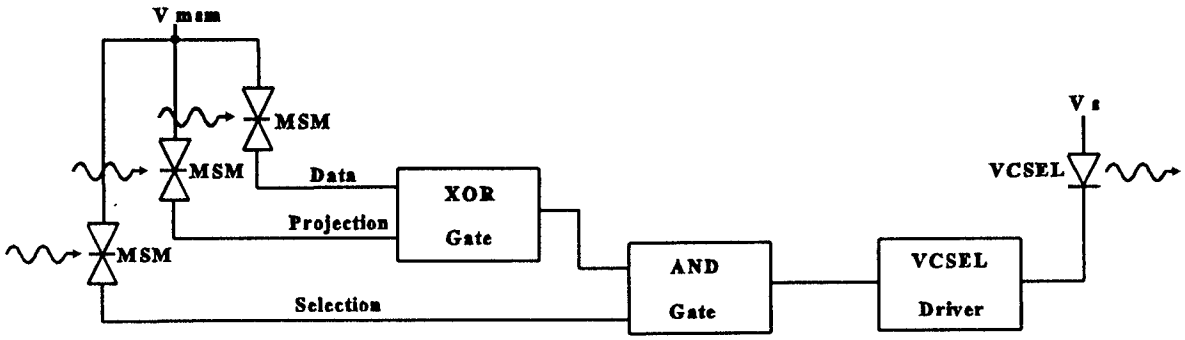
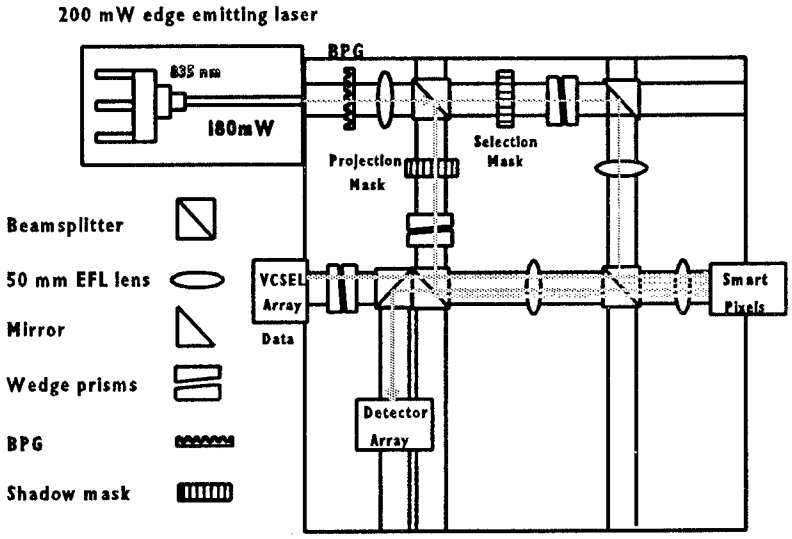


Figure 2: Database filter pixel functional block diagram.

The demonstrator design for the single chip data filter is shown in figure 3. The data inputs are simulated by an 8 X 8 array of VCSELs and the selection and projection masks are created from a 200 mW edge emitting laser that is diffracted into an array of spots through a Binary Phase Grating (BPG). The outputs from the BPG are split into two sets by a beam splitter with each array af beams directed into separate selection and projection masks. The selection and projection shadow masks produce the required input patterns to the smart pixel array. The VCSEL outputs from the smart pixels are focused onto an array of detectors.



The IC is currently in fabrication at Vitesse. Upon receiving the IC we will bond the VCSELs, test the individual devices, and verify the overall system operation. The results will be compared with the simulated results from Hspice (utilizing the Vitesse H-GaAs-III technology parameters). In the future we will be adding lenslet arrays to further reduce the demonstrator size.

Figure 3: Optical Design for Database Filter

References:

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11:15am - 11:30am
FA8

Design and evaluation of a Photonic FFT Processor

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Free-space optical interconnection (FSOI) of integrated circuits (ICs) shows great potential for the efficient implementation of high-performance parallel computing and signal processing systems [1]. The design study of a high-speed FSOI FFT processor system is the objective of this paper. The FFT is an important mathematical operation in many applications such as signal processing, telecommunications, and instrumentation, which makes it an excellent choice to incorporate in a high-speed system. The result of this work is the design of a photonic FFT system that includes the Photonic FFT (PFFT) chip and the Photonic RAM (PRAM) chip. The PRAM chip integrates over 2.5 million transistors in an estimated 1cm x 1cm die area. The PFFT chip integrates over 1.4 million transistors in an estimated 1.2cm x 1.2cm area. Each chip has 768 optical inputs and 768 optical outputs, providing a chip-to-chip bandwidth of 29 Gbytes/sec at 150mhz clock speed. This system can complete an 8,192-point (or smaller) complex FFT using one PFFT chip and two PRAM chips. Larger and faster systems can be built with additional chips. The design uses 48-bit fixed-point complex number format with 24-bit real and 24-bit imaginary parts.

The FFT algorithm, derived by Cooley and Tukey[2], is a reduction in the number of redundant calculations that is required to compute the Discrete Fourier Transform (DFT). The algorithm is a series of multiplications and additions which is performed in stages. The basic building block for the FFT is the butterfly processor (BP). The BP can also provide a graphical representation of the calculations and data flow for the FFT computation. The smallest possible BP is the radix-2 BP, which is represented by the following equations:

$$A' = A + W_N^k B \qquad B' = A - W_N^k B$$

where A and B are complex numbers and W_N^k is the twiddle factor. It can be seen that if the above equations are decomposed and solved for separate real and imaginary parts, a straightforward hardware implementation of the radix-2 BP can be obtained. The radix-2 BP is the heart of our design and is constructed from 4 multipliers and 6 adders. With the radix-2 BP as our primitive design component, a system architecture had to be developed. The choices ranged from a single BP serial design to a fully parallel system with N/2 x log2N BPs, where N is the number of points processed in the FFT. The serial design would be the smallest possible solution but would also be the slowest. The parallel design would be the largest and fastest implementation, but would be difficult to realize due to the hardwired data shuffle between stages of the FFT calculation. Given these options, a solution was chosen of 8 BPs per PFFT chip. These 8 BP's and the necessary support hardware will easily fit onto a single die. In addition, we will get eight times the performance over the single BP choice. The 8 BPs will operate in a parallel fashion, doing the calculations necessary for just a portion of one stage. Data is loaded into the processors from a separate memory chip. The results of the calculations are stored in a different memory chip.

The PRAM chip is divided into 4 banks (0 - 3) of RAM with a total capacity of 393Kbits. Data retrieval is from banks 0 and 2 in one clock cycle, and banks 1 and 3 in the next clock cycle. Data storage is to banks 0 and 1 until full, followed by banks 2 and 3 until full. This setup insures that all BPs will be able to read and write data simultaneously. It also accomplishes the required data shuffle. The PFFT and the PRAM can be combined to form a high-speed FFT system according to the system designer's needs. A low-cost solution would be one PFFT chip and two PRAMs (see figure 1a). The initial data points would be stored in one of the PRAMs. The FFT process would begin and the results would be stored in the other PRAM. This would continue for one stage, with all of the data passing through the PFFT and being stored in the second PRAM. The process would then reverse. All of the data from the second PRAM would pass through the PFFT and be stored in the first PRAM. Following this ping-pong action, the process would end when $\log_2 N$ passes had completed. The high-performance system would consist of $\log_2 N$ PFFTs and

PRAMs (see figure 1b). This is a pipelined solution that would have a separate PFFT for every stage of the calculation. Its operation would be similar to the system described previously, except that the data would move forward to the next PFFT instead of reversing at the end of every stage to be processed by the same PFFT.

Communication between the PFFT and PRAM chips is accomplished through the hybrid CMOS-SEED platform that integrates GaAs multiple quantum well (MQW) photodetectors and modulators with high-volume CMOS VLSI processes [3]. These MQW devices are bonded and electrically connected in a regular grid directly over the active silicon circuits [4]. The photodetector acts as an optical input and drives a receiver circuit. The receiver, in turn, drives the input of a CMOS logic gate. The modulator acts as an optical output and is controlled by a transmitter circuit. The transmitter is driven by the output of a CMOS logic gate. For this design, both the PFFT and the PRAM have 768 optical inputs and 768 optical outputs. A simple one-to-one optical interconnection system can be used to connect the chips.

The photonic design described in this paper provides higher chip I/O count and higher I/O bandwidth than traditional electronic implementations. Specifically, the PFFT and the PRAM chips have a total of 1,536 I/Os each. With this setup, our high-performance system can compute a 1,024-point FFT every 0.44μsec using 10 PFFT chips and 11 PRAM chips. And our low-cost system can perform the same computation every 4.3μsec with 1 PFFT chip and 2 PRAM chips.

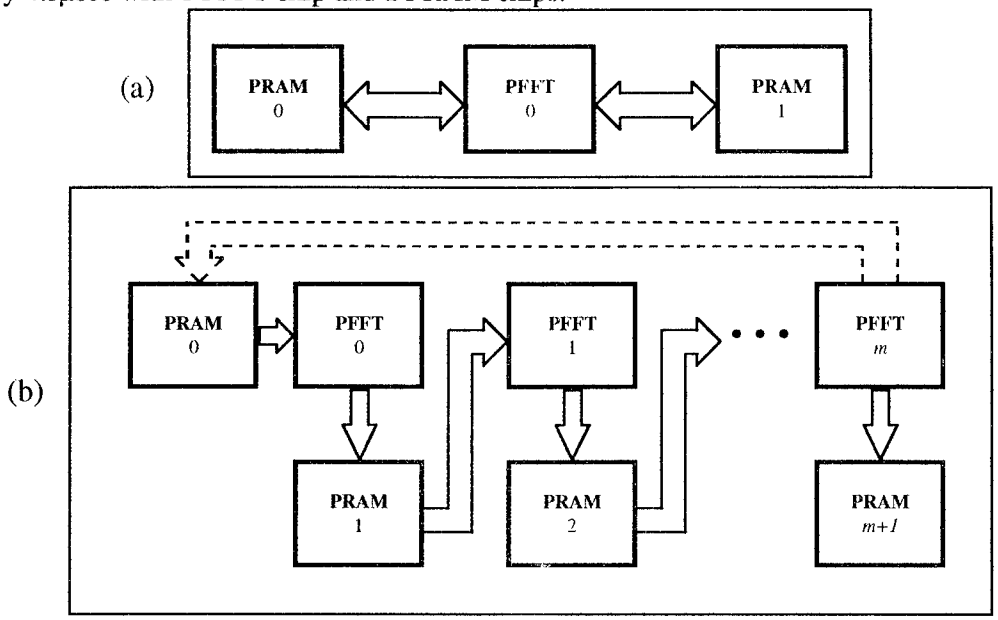


Figure 1: (a) low-cost FFT system built using 3 chips and (b) high-performance FFT system built using $\log_2 N$ PFFTs and PRAMs.

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Smart Pixel Algorithmic Tradeoffs for the Sliding Banyan Network

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Abstract

A telecommunications network modeling tool is used to evaluate smart pixel algorithmic tradeoffs for the Sliding Banyan self routing packet switching architecture. The results provide a basis for VLSI design options.

Motivation

The Sliding Banyan (SB) has been shown to achieve fundamental performance advantages due to its unique 3D optical topology, which spatially clusters nodes to reduce interconnection and control resources [1]. The SB concept is based on a deflection self-routing scheme, in which a *virtual* banyan is "slid" to accommodate each packet's routing needs. This clustering approach presents interesting smart pixel logical design tradeoffs. The tradeoffs discussed in this paper center around the control of the collocated stages of every node in the network. One approach uses a single processor for all stages of a given node. This "node" processor controls all of its stages' switches. Since the SB is a pipelined architecture and the switches are set only once for each packet, the processor needs only control one stage at a time. A different approach is to place a simpler processor at each stage of the node. There will be many more of these "stage" processors, but they will be responsible only for a single stage's routing, so they can be appropriately simpler. In order to arrive at a simplified design for the stage processor the required functionality needs to be reduced. In considering these two processor design approaches, the performance of the switching network and the logical complexity required to achieve it are the critical issues which must be examined.

Approach

The application we examined was high throughput switching of uniformly distributed traffic. A 1024 node 60 stage SB architecture was modeled [1]. Previous work has shown that this number of stages is more than adequate to successfully route all packets under a variety of stressing traffic patterns, such as area of interest traffic [2]. The OPNET™ modeling tool was used to model two local smart pixel processing schemes. The basic approach of OPNET™ is to develop an object oriented model of the switch processor, in this case an array of smart pixel processors. The smart pixel processor is represented as a finite state machine. This representation provides insight into the logical functionality of the smart pixel processors, which themselves are designed as finite state machines.

We simulated two basic SB smart pixel control functionalities – each corresponding to a variation of the pipelined routing algorithm, and the nature of the localized control. The first approach involved a node processor which employed a multiplexing strategy to associate all stages of a given node pair with the concentrated logic. The 60,000 or so VCSEL/detector pairs, distributed across a large backplane, would be serviced by relatively few (512) smart pixel processing nodes. This node processor implements pure deflection routing with a counter determining packet routing prioritization. The second approach distributed a much simpler processor to each node pair. Therefore, there are 60 times as many processors, but each processor is simpler in design. The simpler processor did not have the full functionality of the concentrated processing unit, so a variation of the routing algorithm was required.

Aspects of the node processor which are costly are the large MUXs on the I/O required to run all stages of a node from a single processor. Also, the deflection routing prioritization requires a counter at each processor. This may prove too costly for a fully distributed approach– requiring a counter at every stage of every node in the network. Clearly a different routing prioritization is required; one such scheme would be first-come-first-served. The first packet to arrive at a given stage processor would have priority over the later arriving packet. In this way, the flagging function of the counter in the previous scheme is reduced to a simple time delay on the order of one bit's transmission time. This change in functionality has two implications. The switch may become slightly less efficient since the first packet to arrive is not guaranteed to be the packet closest to its destination – which is a criterion for pure deflection routing. Secondly the bit synchronous nature of the switching fabric is removed by these randomly occurring time delays, creating a need for a mechanism to determine when a packet is present. Figure 1 is a schematic

depiction of the two smart pixel control options corresponding to may stage processors or a single node processor.

Figure 2 shows a typical simulation run of the OPNET™ model for the two smart pixel control options. As can be seen, performance is similar with both options routing all traffic in approximately 40 stages. However the pure deflection routing, as implemented by the node processor, has a slight advantage in routing efficiency. This more efficient routing is a result of the more complicated node processor design. The stage processor was able to approach the performance of the node processor but required additional overhead due to the detection of packets arrival times. Its' simpler design and fast decision process led to less overhead at each node and a commensurate reduction in the network delay. The overall latency differed by a factor of ~2 because the complexity of the node processor requires about twice as many clock cycles to route. However, both schemes seem to be within acceptable packet latencies.

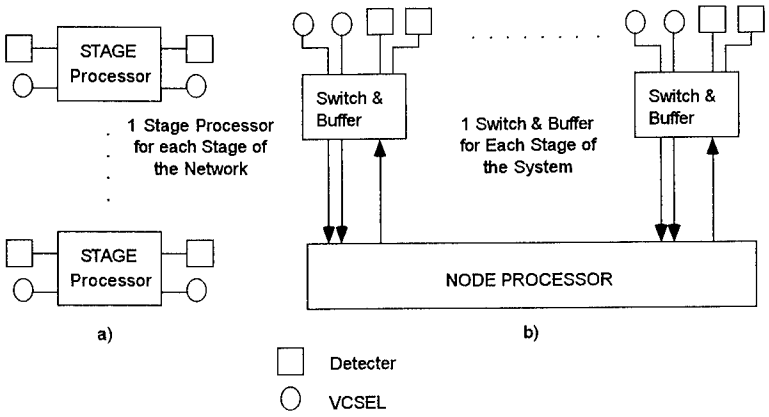


Figure 1. Schematic depiction of two smart pixel SB control options.

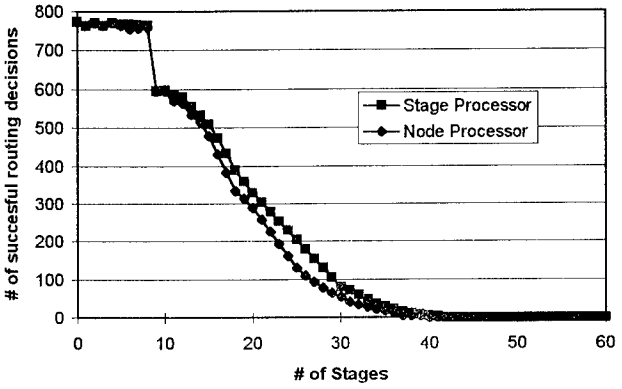


Figure 2. OPNET™ simulation performance for the two SB smart pixel control options

Discussion

Given the similar performance of the two control options, the smart pixel complexity must be examined to determine which approach is more beneficial. At each stage of each node, both smart pixel designs contain a 2×2 switch with a control line from a clocked D flip-flop, to set and hold the switch until the packet is completely through. The control line is set by the processor during the routing process at that stage. Since both designs require the same number of optical links the number of VCSEL and detector driver circuits will be the same. However there is some added complexity in the driver circuit of the stage processor, since additional functionality is required. The main simplification of the stage processor is the elimination of a counter circuit, for prioritization, and the MUXs needed for controlling multiple stages. A complete tradeoff analysis requires gate level resource analysis of the two smart pixel control options, along with further algorithmic refinements through the OPNET™ simulations.

In conclusion, the OPNET™ model was used to couple a functional smart pixel state diagram with application performance. This state diagram will be used for VLSI implementations of the SB smart pixel, and will prove useful for the real estate vs. performance tradeoff analyses. This work is sponsored by the Defense Advanced Research Projects Agency through a contract with the Air Force Office of Scientific Research.

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SMART PIXELS

PAPERS NOT AVAILABLE FOR THE FOLLOWING

2:00pm - 2:30pm (Invited)
WB2: InGaAs/CMOS Smart Pixel Arrays and Their Application to Data Sorting, A. Walker, *Heriot-Watt University, Edinburgh, UK*
InGaAs/GaAs modular/detector arrays have been developed as interfaces between CMOS ICs and free-space optical interconnection systems. Such flip-chip assembled smart pixel arrays are being used to create a fast parallel data sorter.

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Optical MEMS and Their Applications

at

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OPTICAL MEMS AND THEIR APPLICATION

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Wednesday, August 7, 1996

SESSIONS:

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WB: Reliability/Testing

WC: Scanning Applications

WD: Spectral Analysis

8:30am- - 8:45am
WA1

CHARACTERISTICS MEASUREMENTS OF THE 100 × 110 μm^2 FABRICATED MICRO MIRROR

Seok-Whan Chung, Jong-Woo Shin, Yong-Kweon Kim, Ho-Seong Kim*,
Eun-Ho Lee**, Bum-Kyoo Choi***, and Se-Jin Ahn***

School of Electrical Engineering Seoul National University
*Dept. of Electrical Engineering Chung-Ang University
**NATIONAL INSTITUTE OF TECHNOLOGY AND QUALITY
*** Samsung Electronics Co., LTD.

ABSTRACT

A 100 × 110 μm^2 aluminum micro mirror is designed and fabricated using a thick photoresist as a sacrificial layer and as a mold for nickel electroplating. The micro mirror is composed of aluminum mirror plate, two nickel support posts, two aluminum hinges, two address electrodes, and two landing electrodes. The aluminum mirror plate, which is supported by two nickel support posts, is overhung about 10 μm from the silicon substrate. The aluminum mirror plate is actuated like a seesaw by electrostatic force generated by electrostatic potential difference applied between the mirror plate and the address electrode. This paper presents some methods to measure the optical and the dynamic characteristics of the fabricated micro mirror.

INTRODUCTION

Recently, some micro actuators to use as optical instruments are designed and developed[1,2]. But it is very difficult to measure the optical and the dynamic characteristics of the micro actuators because these micro actuators are so small and invisible. In some papers, some methods for measurement of characteristics of micro actuators are presented[1,3]. In this paper, we present two methods for measurements. One method is for measurement of optical characteristics and the other method is for measurement of dynamic characteristics. Also these two method use optical instruments such as Laser, PIN lateral effect photo diode, microscope, and etc.

STRUCTURE

The micro mirror is designed like Fig. 1. The size of the mirror plate is 100 × 110 μm^2 and the height of the Ni support post is about 10 μm

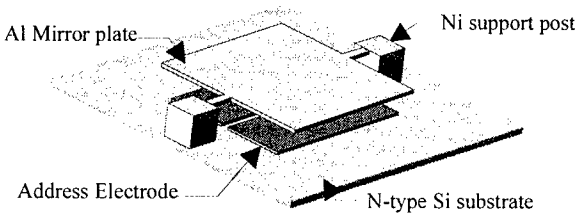


Fig. 1 Schematic diagram of Micro Mirror

FABRICATION

Fabrication process in Fig. 2 can be divided into five steps; electrode fabrication step, sacrificial layer fabrication step, nickel electroplating step, hinge and mirror plate fabrication step, and sacrificial layer removal step[4,5].

To begin the process, a <100> n-type silicon wafer is thermally oxidized. The oxide layer is patterned for backside electroplating of the nickel support posts and for electrical isolation between the support post and the addressing electrodes. In second step, in order to define the gap between the mirror plate and the electrodes, thick photoresist (PMER-P 900) is used as the sacrificial layer. At third step, nickel electroplating is performed. At fourth step, Aluminum is used as a material for mirror plate and hinge metal and Al is deposited by thermal evaporation. Finally, the thick photoresist used as a sacrificial layer is removed isotropically by plasma etching using O_2 RIE.

Fig.3 shows SEM of the fabricated micro mirror array and these four mirror are uniformly fabricated.

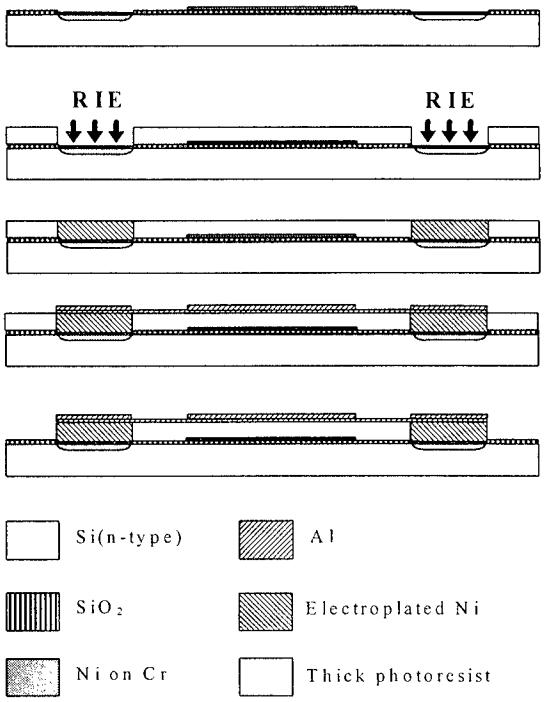


Fig. 2 Fabrication steps of the micro mirror

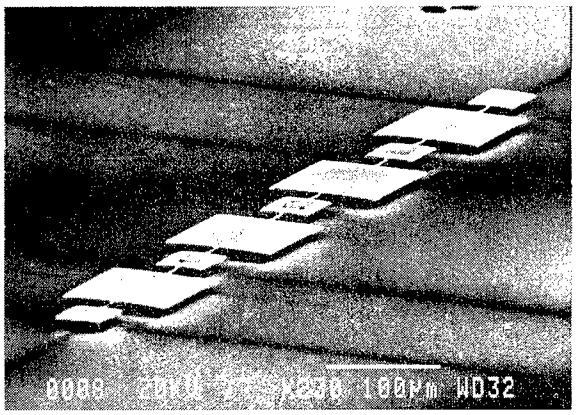


Fig. 3 SEM view of fabricated 4-bit micro mirror array

EXPERIMENTS

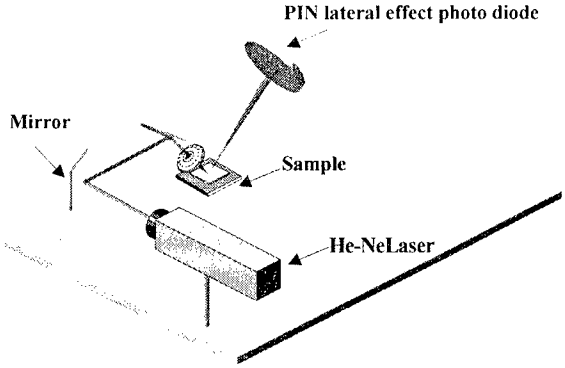


Fig. 4 Optical setup for measurements of the dynamic characteristics of the fabricated micro mirror

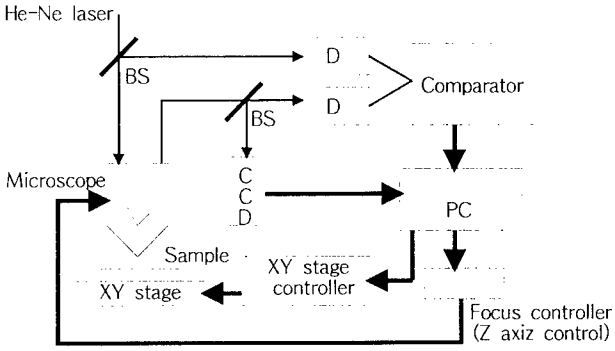


Fig. 5 Schematic diagram for measurements of the optical characteristics of the fabricated micro mirror

Fig. 4 shows the optical experimental setup for measuriments of dynamic charactristics of fabricated micro mirror. As the mirror plate is rotated, the reflected laser beam is incident on the PIN lateral effect photo diode. So we can acquire the relation between the deflection angle and the applied input voltage.

Fig. 5 shows the Schematic diagram for measurements of the optical (specially, reflectance of mirror plate) characteristics of the fabricated micro mirror. Now we are measuring these two characteristics.

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8:45am - 9:15am (Invited)
WA2

Thin-film free-space optical components micromachined in silicon

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Mixed (mechanical, optical, electrical) technologies are traditionally used for fabrication of opto-electro-mechanical components and devices [1, 2]. Introduction of an inexpensive and uniform micro-fabrication technology [3] into the field of optics facilitates a rapid progress mainly because of the reducing of the fabrication costs and the possibility of mass production. Silicon micromachining and hybrid packaging have been recently successfully applied to the fabrication of adaptive optical components [4, 5, 6] and spatial light modulators.

In present report we describe the basic technology and some applications of free-space electrically-controlled micromachined optical components. The technology is based on using stretched nitride films as a substrate for reflecting optical devices. The scheme of a basic device is shown in Fig. 1

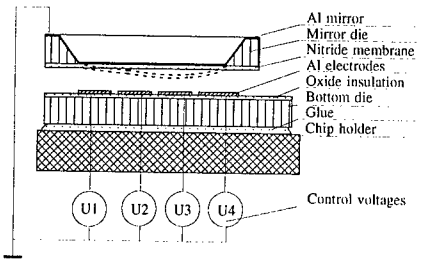


Figure 1: Scheme of the basic device.

The freely suspended deformable nitride membrane, forming a high optical quality deformable substrate is fabricated by etching through the bulk of the wafer in a water/KOH solution. Nitride is not etched in KOH, therefore the released membrane has a high optical quality. Because of the directional selectivity, the final shape of the opening, etched in standard Si wafer is normally rectangular, but special compensation methods allow for the fabrication of circular membranes. Membranes can be patterned with a precision of 0.1mm.

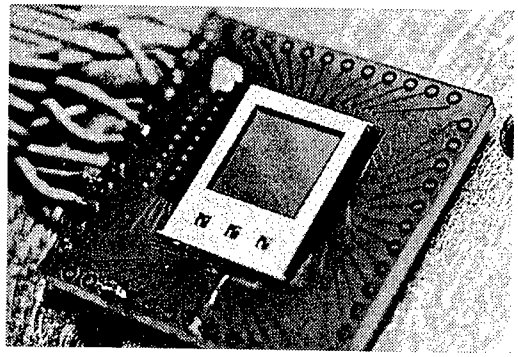


Figure 2: Assembled 9-channel silicon adaptive mirror.

Devices under development or already demonstrated include:

1. Adaptive mirror [6]. In the typical case, the surface of a rectangular 10x10mm nitride membrane is coated with *Al*. The figure of this reflecting/conducting surface is controlled by an array of electrostatic electrodes, placed under the membrane. Mirrors with rectangular and circular apertures, having up to 25 control channels have been fabricated and tested.

2. Spatial light modulators. Control of the local curvature of the mirror membrane allows for control of the near-field intensity distribution [7] with moderate resolution and contrast ratios of up to 3:1. As the modulator has a 100% fill-factor, it can be used with high illumination intensities. Laser marking is the example application of such a low-resolution modulator.

3. Defocus corrector. For correction of defocus, the deformed membrane must have a shape of paraboloid. Good approximation to the parabolic shape may be obtained by electrostatic deformation of a thin membrane, stretched on a circular frame. Rectangular membrane has cushion-like response and may not be used for correction of defocus. A special etch mask was developed to obtain

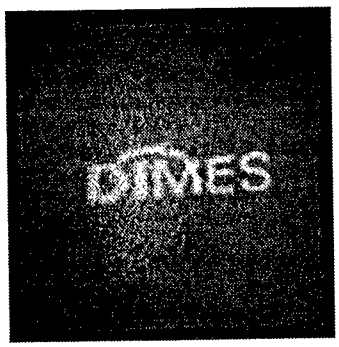


Figure 3: Low-resolution image obtained in the near field by deforming the reflective membrane.

a membrane with approximately circular aperture with standard anisotropic KOH etching, which resulted in a fabrication of "approximately circular" membrane with a diameter of $10mm$, having RMS deviation from the circular contour less then 0.1 mm. The absolute value of this error does not depend on the diameter, therefore larger circular membranes can be fabricated with relatively better approximation. The etching mask and a wafer with etched through circular openings are shown in Fig. 4.

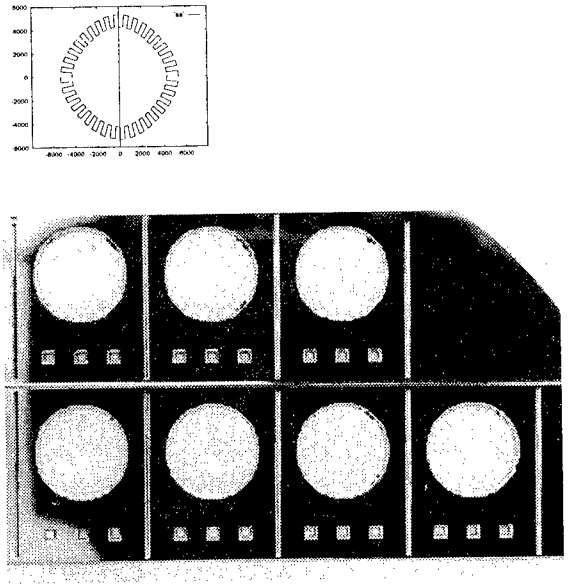


Figure 4: The etch mask used to obtain approximation to a circular contour, and Si wafer with circular openings etched with different compensation.

The assembled mirror, consisting of a 10mm-diameter membrane mounted 50μm over the single control electrode was tested in a Twyman-Green interferometer with a plane $\lambda/20$ reference. The interferograms of the initial and deformed mirror surface are shown in Fig. 5.

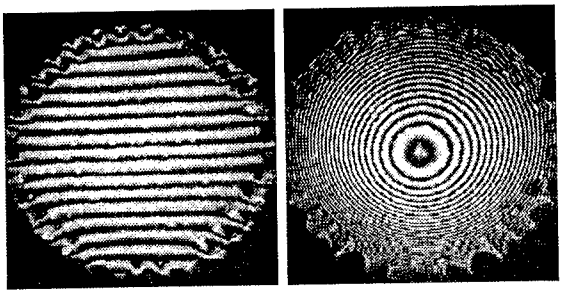


Figure 5: Interferograms of the defocus corrector - initial (left) and deformed by a control voltage of 150V (right).

The possibilities of the technology are not limited to the described devices. The technology can be used for fabrication of IC-comatible opto-electro-mechanical devices for laser adaptive optics, information processing and free-space optical switching and modulation.

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Digital Light Processing and MEMS: An Overview

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Introduction

Sights and sounds in our world are analog, yet when we electronically acquire, store, and communicate these analog phenomena, digital technology offers significant advantages. This was first evident with audio as it was transformed from a technology of analog tape and vinyl records to digital audio CDs.

Video is now making the same conversion to digital technology for acquisition, storage, and communication. Witness the development of digital CCD cameras for image acquisition, digital transmission of TV signals (DBS), and video compression techniques for more efficient transmission, higher density storage on a video CD, or video conference calls. The natural interface to digital video would be a digital display. But until recently, this possibility seemed as remote as developing a digital loudspeaker to interface with digital audio.

Now a new projection display technology called Digital Light Processing™ (DLP™) accepts digital video and transmits to the eye a burst of digital light pulses that the eye interprets as a color analog image (Figure 1). DLP is based on a microelectromechanical systems (MEMS) device known as the Digital Micromirror Device™ (DMD™) [1,2]. Invented in 1987 at Texas Instruments, the DMD is a fast, reflective digital light switch. It can be combined with image processing, memory, a light source, and optics to form a DLP system capable of projecting large, bright, seamless, high-contrast color images with better color fidelity and consistency than current displays [3].

The DMD Light Switch

The DMD light switch (Figure 2) is a MEMS structure that is fabricated by CMOS-like processes over a CMOS memory. Each light switch has an aluminum mirror that can reflect light in one of two directions depending on the state of the underlying memory cell. With the memory cell in the (1) state, the mirror rotates to +10 degrees. With the memory cell in the (0) state, the mirror rotates to –10 degrees. By combining the DMD with a suitable light source and projection optics, the mirror reflects incident light either into or out of the pupil of the projection lens. Thus, the (1) state of the mirror appears bright and the (0) state of the mirror appears dark. Gray scale is achieved by binary pulsewidth modulation of the incident light. Color is achieved by using color filters, either stationary or rotating, in combination with one, two, or three DMD chips [4].

DMD Architecture and Fabrication

The DMD light switch is a MEMS structure consisting of a mirror that is rigidly connected to an underlying yoke. The yoke in turn is connected by two thin, mechanically compliant torsion hinges to support posts that are attached

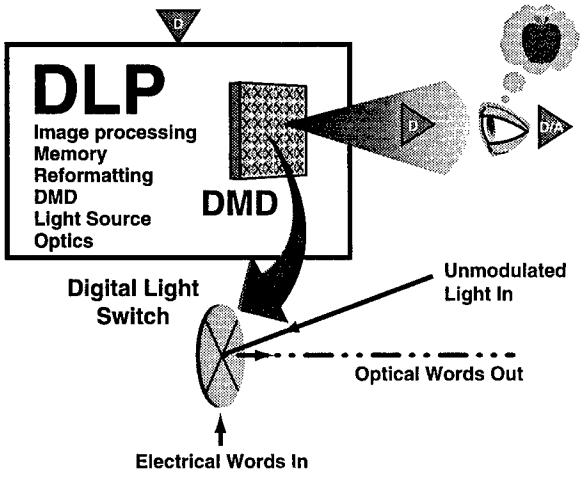


Figure 1. DLP subsystem

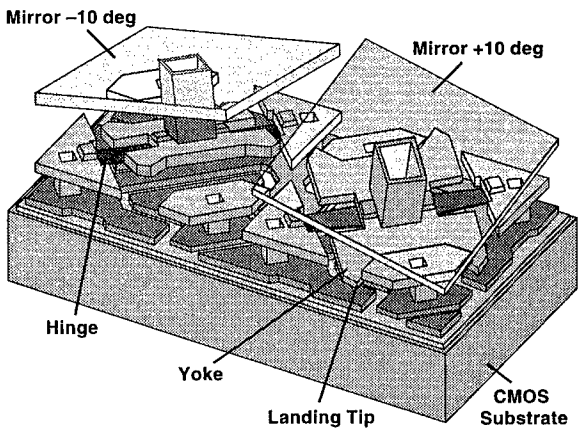


Figure 2. Two DMD pixels (mirrors shown transparent)

to the underlying substrate. Electrostatic fields developed between the underlying memory cell and the yoke and mirror cause rotation in the positive or negative rotation direction. The rotation is limited by mechanical stops to +10 or –10 degrees.

The fabrication of the DMD superstructure begins with a completed CMOS memory circuit. Through the use of six photomask layers, the superstructure is formed with alternating layers of aluminum for the address electrode, hinge, yoke, and mirror layers and hardened photoresist for the sacrificial layers that form the two air gaps. The aluminum is sputter-deposited and plasma-etched. The sacrificial layers are plasma-ashed to form the air gaps. Table 1 lists distinguishing features of this MEMS technology compared with conventional MEMS.

Table 1. Distinguishing features of DMD MEMS technology

Number of moving parts	0.5 to 1.2 million
Mechanical motion	Makes discrete contacts or landings
Lifetime requirement	450 billion contacts per moving part
Address voltage	Limited by 5-volt CMOS technology
Mechanical elements	Aluminum
Process	Low temperature, sputter deposition, plasma etch
Sacrificial layer	Organic, dry-etched, wafer-level removal
Die separation	After removal of sacrificial spacer
Package	Optical, hermetic, welded lids
Testing	High-speed electro-optical before die separation

DMD packaged parts have completed a series of reliability tests including hinge fatigue, shock and vibration failure, hinge memory, and stiction failure. For the DLP applications being considered, test results demonstrate that there is no fundamental lifetime limitation for the DMD [5].

DLP Business Opportunities

Texas Instruments is actively pursuing two broad business opportunities for DLP: projection displays and continuous-tone color printing [6]. The color printing application will be presented in a companion invited paper at this meeting. The projection display opportunity falls into three market segments [7]: professional (large audiences), business (portable), and consumer/home theater (small audiences). Texas Instruments is currently teamed with 13 market makers within these market segments [8]. TI is providing to the market makers DLP subsystems or digital display engines (DDEs). The DDE is the DLP subsystem ready for integration with a video interface, power supply, sound, controls, and a cabinet.

Currently, TI is manufacturing DDEs for the business projector segment with VGA resolution (640 × 480). Production runs of this first DLP product began in March 1996. DLP systems with SXGA resolution (1280 × 1024) have recently been demonstrated.

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10:30am - 11:00am (Invited)
WB1

Reliability and Long Term Stability of MEMS

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Although many MEMS are either commercialized or near commercialization, the long term stability and potential failure modes of these devices are not well characterized. This is of particular concern in several industries, where either safety or long term reliability are essential characteristics of the product. Safety critical applications include medical devices and sensors for actuation of devices such as airbags. Long term reliability applications include flat panel displays, optical switches, fiber optics, and integrated sensors where the warranty cost of replacing a device may exceed the cost of the device.

Particular attention to MEMS failure modes is important because failure modes that are negligible at a macroscopic scale become significant on the microscale. Potential modes of failure for MEMS structures include:

Static overload

Many MEMS operate at stress levels in the vicinity of 1 GPa. In several cases high stresses are necessary to overcome stiction in membrane geometries. These stress levels are higher by at least one order of magnitude than macroscopic structures. Small defects that act as critical cracks at these stress levels can be introduced by etching, polishing, or rough handling.

Delamination

High stresses can be associated with multilayer films, introduced by processing, thermal mismatch, or epitaxial mismatch. The adhesion between layers depends strongly on their chemical and mechanical compatibility.

Creep

High stresses and stress gradients introduce the possibility of time-dependent mass transfer through glide and diffusion mechanisms. Although the creep strains that result are negligible macroscopically, they can be enormous on the scale of MEMS. The increasing use of metal as a structural material in MEMS where room temperature creep exists should be of concern to MEMS manufacturers.

Environmental attack

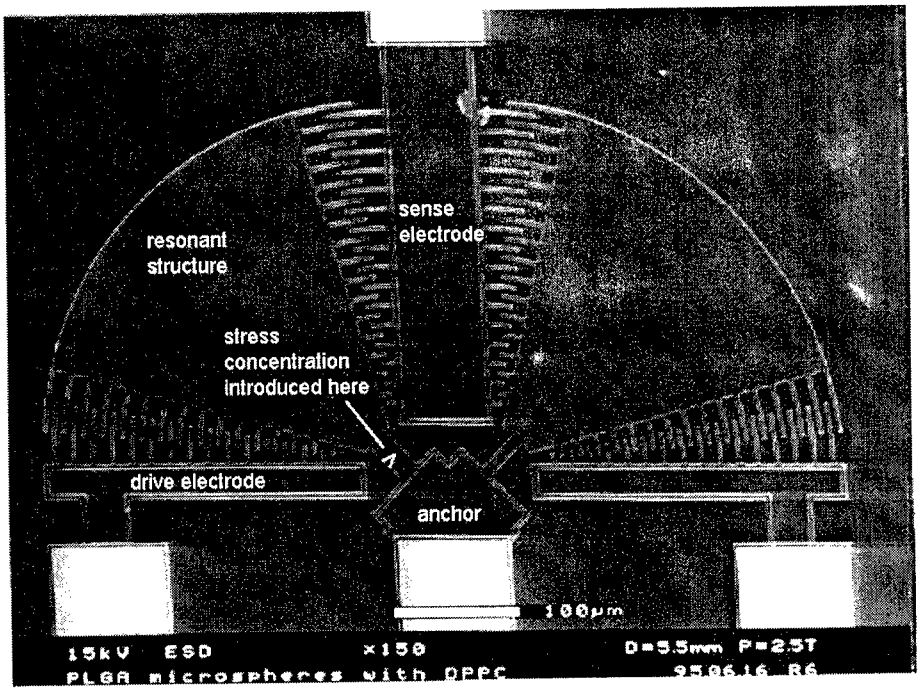
MEMS are designed for a variety of applications where environmental effects can be important. This includes valves, sensors, and pumps where the contacting fluids, including water, can be corrosive.

Fatigue

Cyclic loading of MEMS couples with the previously described mechanisms associated with static loading, creep, and environmental effects. Any process that results in an irreversible repositioning of atoms within a material can contribute to fatigue.

We have been examining long term stability through the design of MEMS for accelerated testing. These include cantilever and membrane structures for both static and cyclic loading and stiction. We have identified a potential failure mode in silicon devices that was not previously known. This failure mechanism results from the effect of water on the initiation and propagation of cracks in both single and polysilicon MEMS.

Our experiments consist of resonant fatigue testing of poly and bulk silicon test structures similar to that pictured below. We introduce either stress concentrations using the lithographic mask or a crack using a nanoindentor. Crack initiation and growth is detected by a change in the resonant frequency of the structure. We have measured crack growth in these structures as a function of time, where the growth rate is accelerated by the presence of moisture.



11:00am - 11:15am
WB2

AUTOMATIC TESTING OF THE DIGITAL MICROMIRROR DEVICE™ (DMD™)

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P.O. Box 655012, Mail Station 992, Dallas, Texas 75265

The invention of the DMD by Texas Instruments has opened the way for a new, more dramatic approach to high-performance front- and rear-projection television displays as well as the high-performance printer systems industry. If the ultimate capability of these devices is to be realized in the digital light processing industry, the device cost must be low enough when delivered to the systems producer to provide true value.

A significant contributor to any solid-state device's cost is the cost of test and evaluation including critical engineering data. The DMD is basically a special static RAM (SRAM) of a CMOS design capped with a multilevel metal process to produce the digital micromirror light modulating superstructure. Consequently, to properly test the DMD requires dc current, CMOS SRAM memory, plus specialized electro-optical testing. Figure 1 is the block diagram of the test system that performs the CMOS and optical tests. Figure 2 is a schematic of the optical test subsystem including the relationship of the DMD to the light sources and receiver optics.

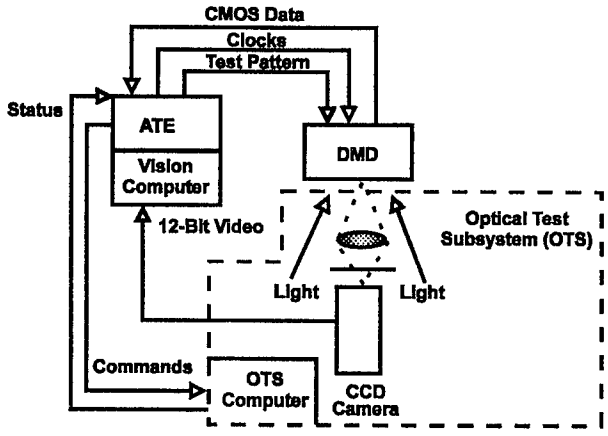


Figure 1.
DMD Test System Block Diagram

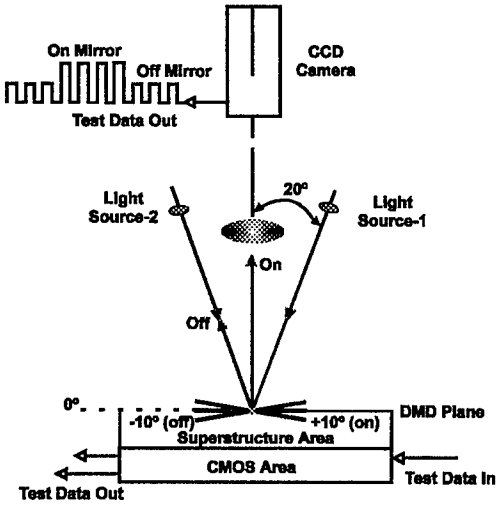


Figure 2.
DMD ATE Optical Test Subsystem

Since test costs are primarily driven by the test cycle time and the necessary test personnel coverage and expendable supplies for time periods beyond the initial equipment depreciation period, we must attain a rapid, reliable, and repeatable test for all parameters whether electrical or optical. The test process, particularly the optical process, must not be intrusive. The key technology used to perform the optical test is non-contact computer vision processing combined with effective and accurate CMOS memory methods.

The DMD performs the image formation process by responding to CMOS voltage changes that place the micromirror in either one of two states (on, off) as shown in Figure 2. However, it is possible that errors in the CMOS or superstructure production process can cause the micromirror to be in one of six states, including those representing defects, as shown in Table 1.

Table 1

Possible States	Description
1) Good	No stuck mirrors, no missing mirrors
2) S+	Stuck in the on direction
3) S–	Stuck in the off direction
4) N+	Not in the on position
5) N–	Not in the off position
6) Stuck 0	Stuck flat
7) Invalid	Conflicting logical state

It is possible to determine all six states plus invalid with the two programmable light sources, and two CCD camera exposures per light source (mirror on, mirror off).

The deflection of the light beam, as shown in figure 2, to produce the presence or absence of light in the image plane is effective and produces on-to-off ratios of the CCD camera signals well above 400-to-1. The sweeping of the light beam up to 40 degrees optical change for a +10 to –10 degree micromirror position produces a significant displacement of the beam at the lens entrance pupil. It is important that this beam be intercepted so that by the optics vignetting effects do not mask device uniformity issues. This is a particularly difficult optical design since effective f/numbers of 2.8 are typical within the projector designs for the display product.

This effective f/number is given by

$$F(\text{effective}) = F(\text{Infinity})(1 + 1/M)$$

where M is the magnification of the system.

The magnification is set by the vision process, which must place an adequate number of camera pixels on the image of the micromirror to resolve not only the mirrors and their gaps but also the subtleties of the light intensities across a mirror. Figure 3 shows the latest automatic test equipment developed for both CMOS and optical testing of the DMD.

In conclusion, Texas Instruments has maintained a rigorous test development activity during its DMD development and preproduction phase that has resulted in the ability to automatically characterize a wide range of DMD devices, including defect states, contrast ratios, and mirror array reflection efficiencies.

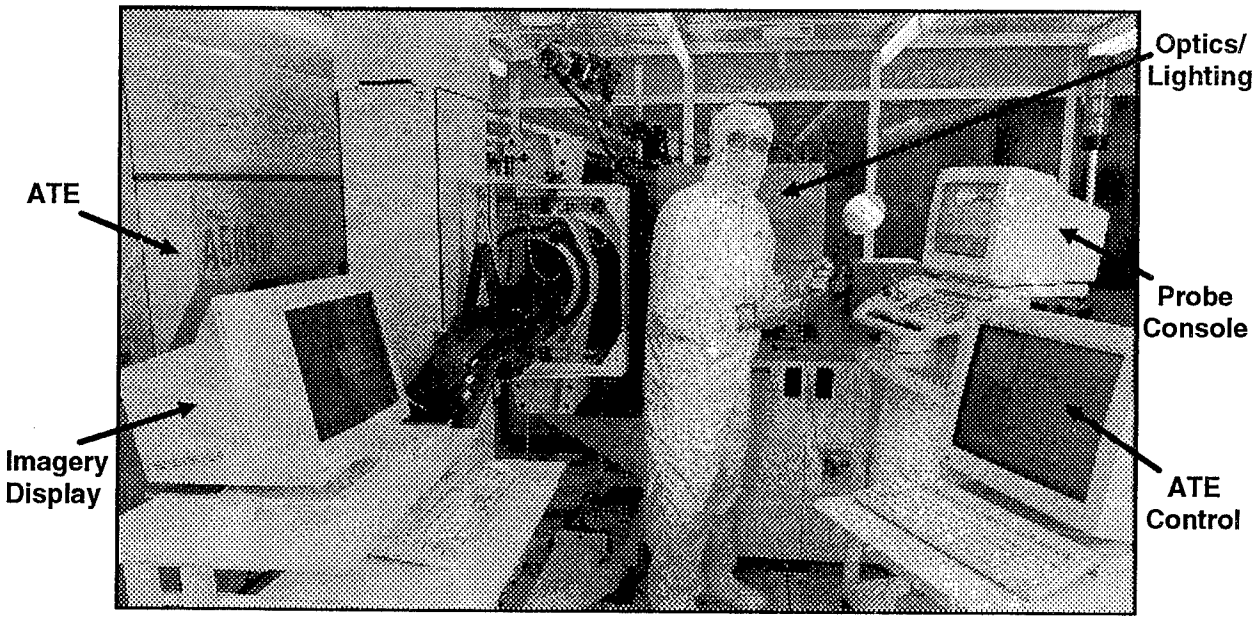


Figure 3.
DMD Automatic Tester.

11:15am - 11:45am (Invited)
WB3

Reliability studies of single crystal silicon beams for rigid micro mirrors

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Micro beams are often used to support micro mirrors. The beams behave as torsional springs or bending members when the mirrors are actuated. The mirrors themselves behave as rigid bodies. Due to deformation of the beams, they constitute the highly stressed components of the system and thus determine the systems' operational reliability.

Figure 1 shows a micro mirror supported by torsional beams. It is fabricated by the SCREAM process. The mirror is formed by filling a dense grid of frame with SiO_2. The frame is released from the SCS substrate. The oxide top is mechanically polished to form a smooth surface. Aluminum is then sputtered to form the mirror surface as well as the electrodes. The frame and the supporting beams consist of single crystal silicon (SCS) core, coated by SiO_2 and Al. The mirror is twisted or moved out of plane by applying bias between the mirror and the substrate.

In order to understand the reliability of the mirror-beam system, we study the failure mechanism of a single crystal silicon bar subjected to torsion and bending. The experimental setup is shown in Figure 2. It consists of a micro loading device and the SCS test sample at the right end. The closeup of the sample is shown in Figure 3. The minimum section of the pillar is $.5 \times .5\ \mu m^2$ at its mid height. The sample is fabricated by partially etching a SCS pillar using SF_6. The pillar is attached to a 25 μm long stiff lever arm. The loading device applies force on the lever arm at 7 μm away from the center of the pillar. The pillar is thus twisted and bent until failure. The angle of twist is measured from the relative displacements of the ends of the lever arm.

The axis of the pillar is aligned with the (100) direction of the crystal lattice. Thus, although SCS is anisotropic, the stresses due to twisting and bending are decoupled. This allows independent analysis of the stresses due to torsion and bending. From the torsion analysis, we obtain the force applied on the pillar prior to failure. The force is then used to compute the applied bending. The maximum stress is evaluated and is found to occur at the minimum cross section of the pillar. The maximum tensile stress is found to be 20 GPa and the maximum shear stress is 6 GPa. Figure 4 shows the fracture surface of the pillar. Thre failure surface coincides with the (111) plane, where the surface energy is minimum. The failure surface is smooth, indicating a brittle fracture. Note that bulk SCS fails at around .35 GPa.

The result implies that the failure strength of SCS increases by about two orders of magnitude as the size is reduced to μm scale - the scale used to support micro mirrors. It thus follows that the beams can sustain very large deformations before failure. For example, the experimental pillar twisted by 25° at failure. Most of the twisting is contributed by the deformation of about 3 μm long mid region of the pillar. If we consider a beam, 100 μm long, of similar cross section, then it could be twisted by more than 700° prior to failure.

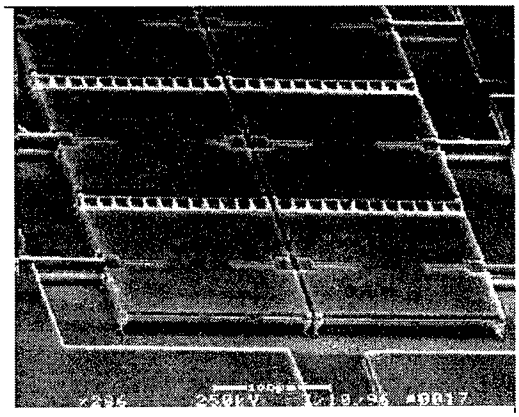


Figure 1. Torsional mirror

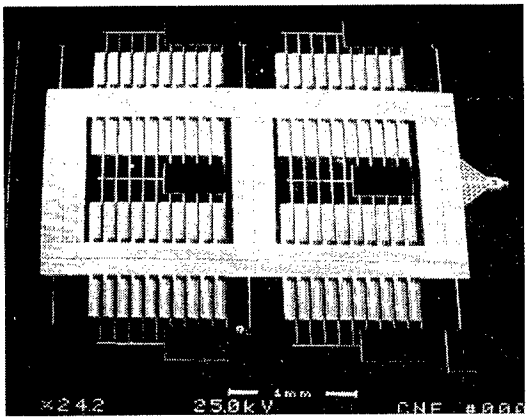


Figure 2. Loading device for reliability studies. The sample is at the right end.

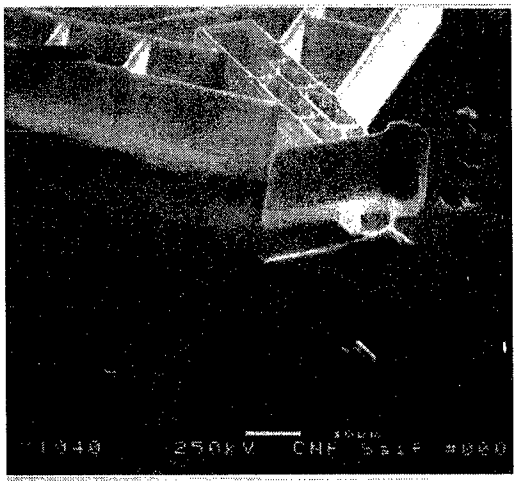


Figure 3. Close up of the test sample.



Figure 4. The fracture surface.

11:45am - 12:15 (Invited)
WB4

Breakdown Mechanisms of Electrostatic Polysilicon Actuators using as an Example the REMO-Component

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1. Introduction

The REMO (REflective MOdulator) component is a micromechanical light modulator fabricated by polysilicon surface micromachining [1]. Its operation principle is based on a Fabry-Perot consisting of two polysilicon mirrors (Figure 1).

The free standing polysilicon membrane has a nominal thickness a 464 nm. It can be actuated by electrostatic forces. To switch the Fabry-Perot from the high reflection to the low reflection state the membrane has to deform 300 nm; this results in a maximum tensile stress of 0.13 GPa (Figure 2). The electrical field necessary for the deformation is as high as 60 V/μm.

In the present paper a systematic study of the effects of these high operation stresses in combination with humid air is presented. Slow crack growth is evaluated by visual inspection of precracked structures. Electrical and mechanical drift phenomena are characterized by recording the resonance frequency in vacuum after continuos operation during several weeks.

2. Mechanical Breakdown

a. rupture strength

The maximum rupture strength was evaluated by beam bending structures [2]. Taking a sample size of 10, the average rupture strength of polysilicon is $\bar{\sigma}=3.89$ GPa with a standard deviation of $\Delta\sigma = 0.53$ GPa. Figure 3 shows a Weibull function fitted to the measured rupture values. According to the Weibull analysis the operating stress of 0.13 GPa results in a practically zero failure probability. During the fabrication process the maximum stress can be ten times larger, for example in the final rinse process the membrane may be deformed down to the underlying substrate. In this case the failure probability is still as low as 0.05 %.

b. long cycle fatigue

At room temperature polysilicon can be regarded as an ideal brittle material with no dislocation movement prior to fracture. Contrary to metallic materials where long cycle fatigue is based on dislocation pile up at a crack tip, the fatigue mechanism in polysilicon must be of a different type. It has been proposed [3] that fatigue of the native oxide layer is a possible fatigue mechanism.

The resistance of polysilicon against slow crack growth was evaluated by stress-cycling precracked microstructures. Figure 3 shows a SEM micrograph of a precracked REMO component. In a relative air humidity of 100 % stress intensities of 0.15 GPa didn't lead to an observable crack growth. The crack length was determined by visual inspection in an optical microscope. Performing tests at higher stress intensities we will be able to determine the threshold stress intensity at which slow crack growth can occur.

3. Corrosion in Humid Air

a. drift of the resonance frequency

To characterize the mechanical long term behavior the resonance frequency is measured in vacuum before and after the stress cycling. A quality factor of about 6500 can be obtained. The structures are stress cycled at atmospheric pressure under different humidity conditions.

After stress cycling in relative humidity of 84 % some test structures showed a distinct frequency increase of up to 20 % and a decrease of the quality factor down to 2000. In addition the color of these structures changed. Figure 5 shows the frequency response before and after stress cycling.

This noticeable change in the mechanical properties, which would lead to a failure of the modulator function, can be explained by the formation of a surface oxide under the high humidity and electric field conditions. Stress in the oxide stiffens the membrane and leads to the frequency increase.

b. permanent electrical polarization

Due to the nonlinear character of the Coulomb force electrostatic resonators show a strong dependence of the resonance frequency on the DC bias voltage. By recording the resonance frequency at DC bias of opposite polarity the permanent polarization of the air-gap capacitor can easily be measured. Figure 6 shows the resonance frequency as a function of the absolute value of DC bias before and after stress cycling in humid air. It can be seen, that a permanent polarization of about 2 V is present after the cycling test, i.e. for a given resonance frequency the difference between positive and negative bias DC is 4V. This polarization is probably due to trapped charges in the surface oxide.

4. Conclusions

In absence of high air humidity the mechanical properties of polysilicon meet the requirements for a highly reliable modulator, i.e. the fracture strength is well above the operation stress and slow crack growth is small. In dry air no change of the mechanical nor the electrical properties could be observed.

The combination of high electric field with humid air can lead to a noticeable change of the mechanical and electrical behavior. This is explained by the formation of a surface oxide.

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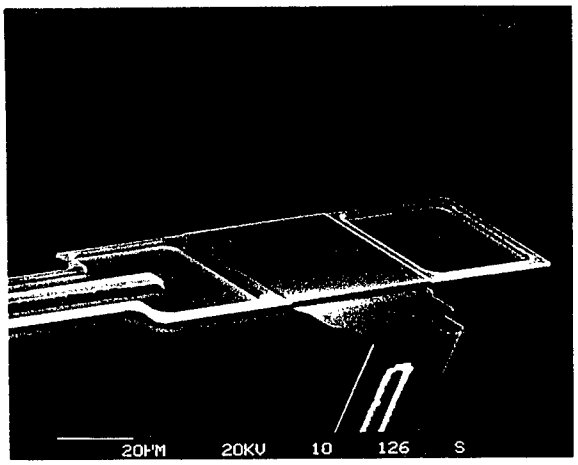


Fig. 1: SEM micrograph of the REMO component.

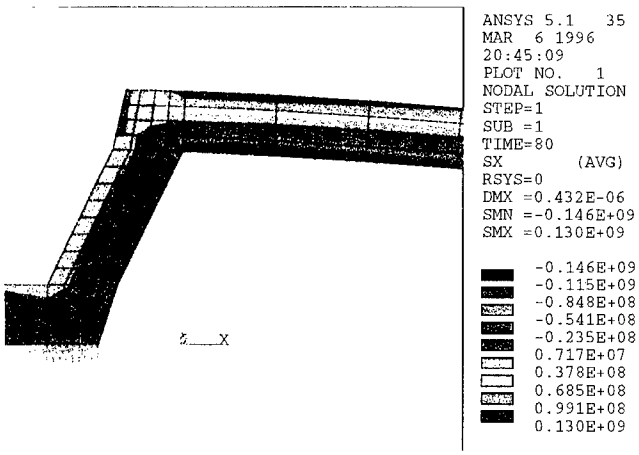


Fig. 2: FEM analysis of stress distribution in the clamped end. Maximum tensile stress is 0.13 GPa.

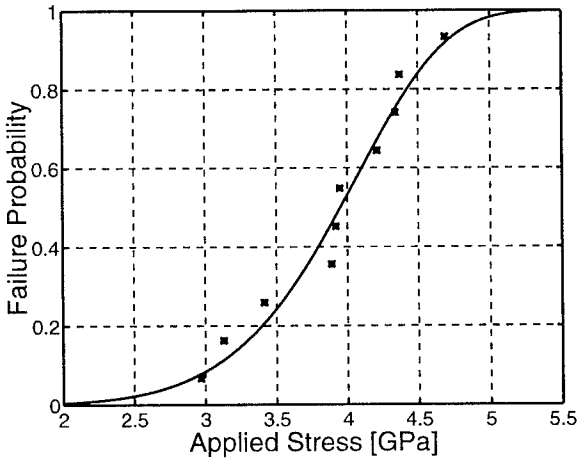


Fig. 3: Measured rupture strength of polysilicon and fitted Weibull function. Weibull parameters of rupture strength are: σ_0 = 4.15 GPa and m = 7.5.

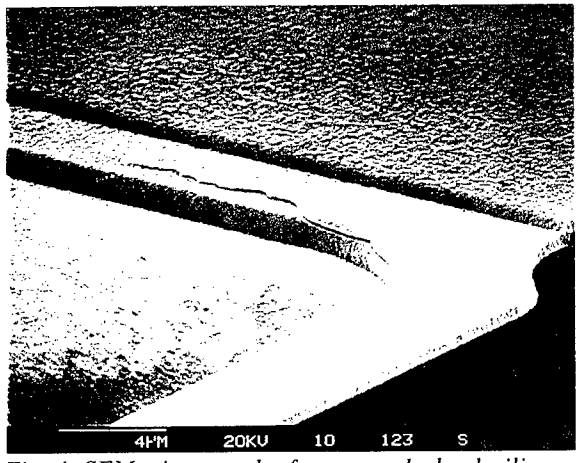


Fig. 4: SEM micrograph of a precracked polysilicon membrane for measuring the crack growth rate.

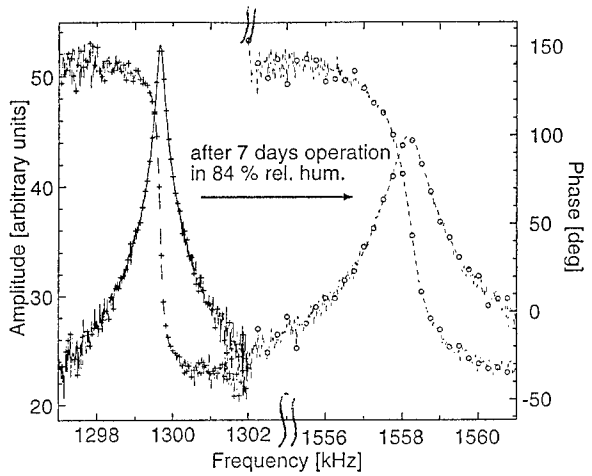


Fig. 5: Operation in humid air can lead to an increase of the resonance frequency. Operation in dry air doesn't lead to any frequency shift. Note the discontinuous frequency scale.

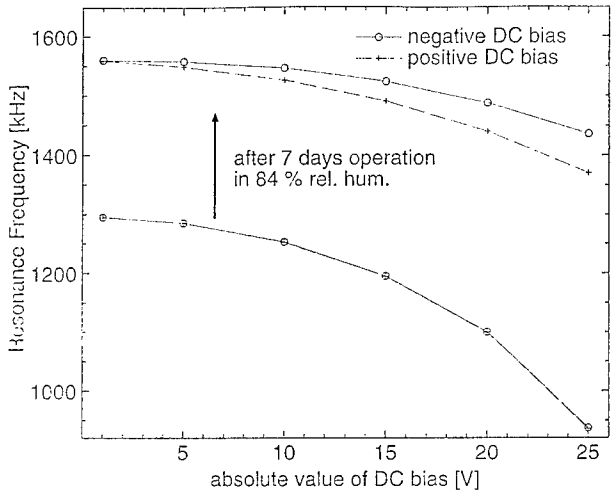


Fig. 6: Resonance Frequency as a function of DC bias. After cycling the resonance frequency has increased 250 kHz and the capacitor has a built in voltage of 2 V.

1:30pm - 2:00pm (Invited)

WC1

Si Micromachined 2D Optical Scanning Mirror and its Application to Scanning Sensors

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ABSTRACT

We have developed a two dimensional micro optical scanner integrated with a photo diode and piezoresistors in order to miniaturize scanning type of optical sensors represented to barcode reader or laser radars. The scanner with the size of 7mmx7mm is fabricated by silicon bulk-micromachining technique and capable of 2D optical scanning , photo detection and scanning position detection. A miniature 3D vision sensor for pipe inspection mobile machine has also been developed utilizing the scanner and spiral scanning detection method. This paper describes structure, operation principle and characteristics of the developed scanner and 3D sensor.

2-D OPTICAL SCANNER[1]

Figure 1 shows a structure and operation principle of 2D optical scanner. The scanner consists of a resonator with multi-degrees of freedom and a piezoelectric actuator for excitation of the resonator. The resonator which consists of a scanning mirror supported by a fine leaf spring from a flame is exited at the resonance frequencies for bending and torsional vibration mode of the scanning mirror. As the result, the scanning mirror vibrates with large amplitude in the direction of bending and/or torsional modes, and reflected optical beam on the mirror is scanned in these directions with large angle. It is possible to realize various scanning patterns as shown in Fig.2 by selecting a excitation frequency of the resonator.

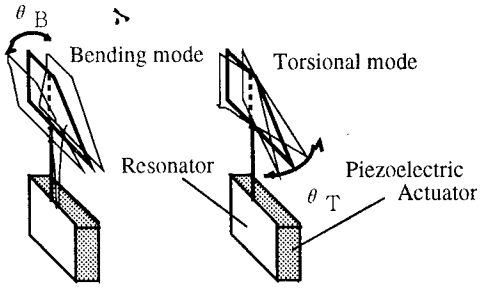


Fig.1 Structure of 2D scanner.

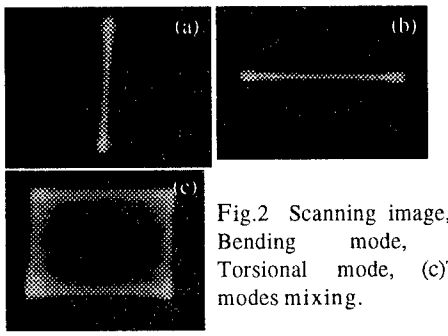


Fig.2 Scanning image, (a) Bending mode, (b) Torsional mode, (c)Two modes mixing.

DEVICE INTEGRATED 2D SCANNER[2]

Integration of a photo diode for reflected photo intensity detection from an object and piezoresistors for scanning position detection onto the scanner was performed for miniaturization of the scanning type optical sensors. The integrated scanner shown in Fig.3 is fabricated by silicon bulk-micromachining and conventional IC fabrication process and a size of 7mmx7mmx0.1mm(thick.). This scanner is capable of two dimensional optical scan, photo detection, scanning position detection and resonance frequency adjusting of the resonator with frequency adjuster and heat generation control of input current to piezoresistors for realizing a circular scanning pattern described below. Scanning characteristic and frequency adjusting performance of the

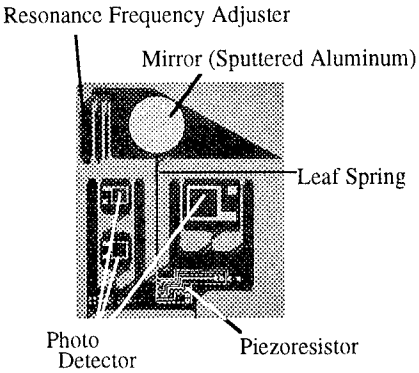


Fig.3 Integrated optical scanner.

scanner are shown in Fig.4 and Fig.5. A scanning angle of 60 degree for bending mode and 30 degree for torsional mode were obtained at only 5 micron excitation of the resonator. Resonance frequency was 57Hz for bending mode and 190Hz for torsional mode. Resonance frequency adjustment for each vibration mode was succeeded by controlling a input current to piezoresistors. Because a rate of frequency change is different each other, Lissajous's scanning pattern determined by combination of two resonance frequencies becomes variable.

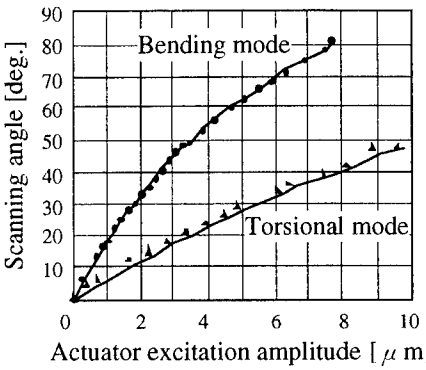


Fig.4 Scanning characteristic of the scanner.

APPLICATION OF THE SCANNER[3][4]

Applying the scanner leads to miniaturize the size of the scanning sensor and detect an object two or three dimensionally. Miniature 3D vision sensor[4] for pipe inspection mobile robot is one of useful application of the scanner. Figure 6 shows a detection principle of 3D pipe inspection. A spiral scanning method, shown in Fig.6, with continuous circular pattern of the scanner was adopted for detecting an obstacle three dimensionally in a pipe. Circular scanning was realized by adjusting two resonance frequencies to nearly equal and phase difference of 90 degree at a certain frequency between two resonance frequencies using the adjustor. A prototype sensor which consists of the integrated scanner, a laser diode with collimating lens and signal processing circuits has the size of 23mm in diameter and 18mm in length, and capability of 3D image recognition as shown in Fig.7.

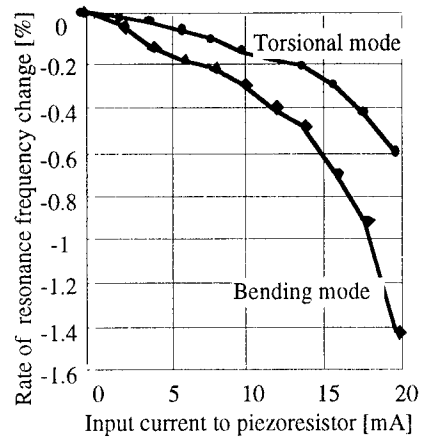


Fig.5 Performance of frequency adjuster.

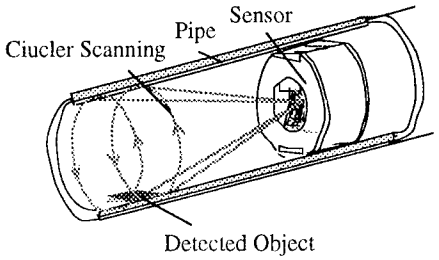
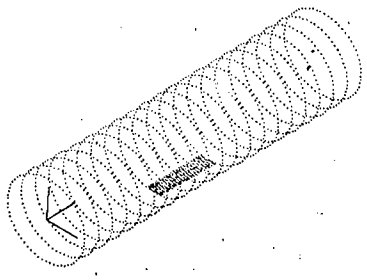


Fig.6 Circular scanning for pipe inspection.


Fig.7 Detected 3D imege of the sensor.

CONCLUSION

Si-micromachined 2D optical scanner integrated with photo detector and piezoresistor was presented. 3D vision sensor utilizing the scanner for pipe inspection was also demonstrated. The integrated 2D scanner will be useful for miniaturization and multi-dimensional detection of the scanning sensor.

This work was performed under the management of Micromachine Center as the Industrial Science and Technology Frontier Program, "Research and Development of Micromachine Technology", of MITI supported by New Energy and Industrial Technology Department Organization.

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(3)H.GOTO "High performance micro photonic devices with micro actuator", Proc. of SPIE, Vol.1992, pp.32-39(San Diego, 1993)

(4)H.TOTANI et.al."Miniature 3D optical scanning sensor for pipe-inspection robot", Proc.of SPIE, Vol.2593, pp.21-29(Philadelphia, 1995)

2:30pm - 3:00pm (Invited)
WC3

Digital Light Processing™ for Color Printing

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Introduction

The acquisition, manipulation, transmission, and storage of data and images in modern society is rapidly migrating into a digital domain. While most of the daily phenomena we encounter are analog, the advantages of digital representations are increasingly compelling in terms of costs, bandwidth, fidelity, and most significantly, convenience of use. Along with the personal computer and advancements in a host of consumer electronics, other significant trends have emerged in the last decade: the analog audio industry transitioned to the digital audio compact disk (CD), electronic color photography became pervasive, and the advantages of digital communications appear in everything from cellular phones to digital satellite TV services (DSS).

The role of semiconductors in this evolution of performance and capability is truly unique among materials and technologies. In the short course of forty years, silicon devices have expanded from transistors (1954), to integrated circuits (1958), microprocessors (1971), and high-density memories (1985). In do doing, they have grown almost seven orders of magnitude in complexity. More recently, the spectrum of semiconductor applications has encompassed high-resolution imagers and a panoply of chemical, electrical, magnetic, and process sensors, including the advent of silicon accelerometers, an early application of MEMS. The light emitting ability of semiconductors has been of considerable commercial significance, and represents an added dimension of this family of materials.

While the preponderance of focus in semiconductors has been for computing and communications, the benefits of optical sensors, imagers (CCDs), and light-emitting structures have grown since the 1970s to be virtually as important. So it is reasonable to propose a similar paradigm, where today's efforts on semiconductor-based MEMS technologies will rapidly assume comparable importance in the commercial world [1,2]. Figure 1 illustrates this evolution. A significant commercial opportunity exists for MEMS in the form of a silicon spatial light modulator (SLM) suitable for both digital display and digital printing applications. The Digital Micromirror Device™ (DMD™) SLM has been under development at Texas Instruments since 1987, and is the core component of TI's Digital Light Processing™ (DLP™) businesses [3]. A companion paper by Dr. Larry Hornbeck will cover display applications of DLP. This paper covers the benefits of DLP in digital color printers capable of producing "photorealistic" quality on plain paper, quickly and inexpensively.

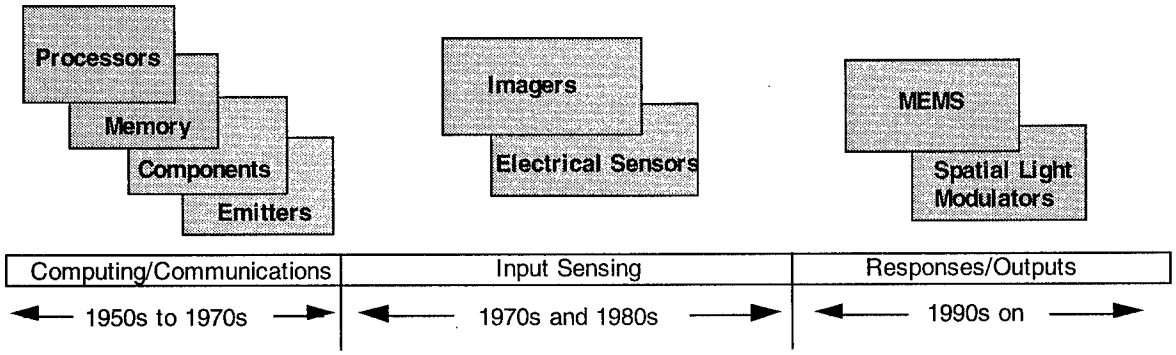


Figure 1. Evolution of Semiconductor Functionality Into MEMS

In effect, the advent of MEMS enables the third function, and the opportunity exists for inexpensive, monolithic, integrated systems that can sense, react, and respond. These systems seem to transcend conventional machines. A term that captures this essence is "autotelic." In its simplest application, one can envision a system that improves with use, because of this functionality. But the functionality has to be enabled at low cost, with flexibility and ease of implementation, suggesting an integrated, semiconductor-like strategy.

DLP for Color Printing

The DMD has been adapted for printing applications and used to successfully demonstrate a fast color printer. Figure 2 illustrates the concept of writing a latent image on photosensitive media, the OPC drum in this case, which, through subsequent process steps, results in a high-quality color print.

This paper covers the system design decisions that led to the manufacture of a monolithic DMD containing 451,584 individually addressable mirrors, each only 17 micrometers by 17 micrometers in extent [4]. The resulting silicon chip is 125 millimeters long and represents one of the larger silicon integrated circuits (ICs) in existence. The choice to introduce a seemingly immense complexity into the DMD SLM chip and related ICs improves the performance and overall system design of the printing process.

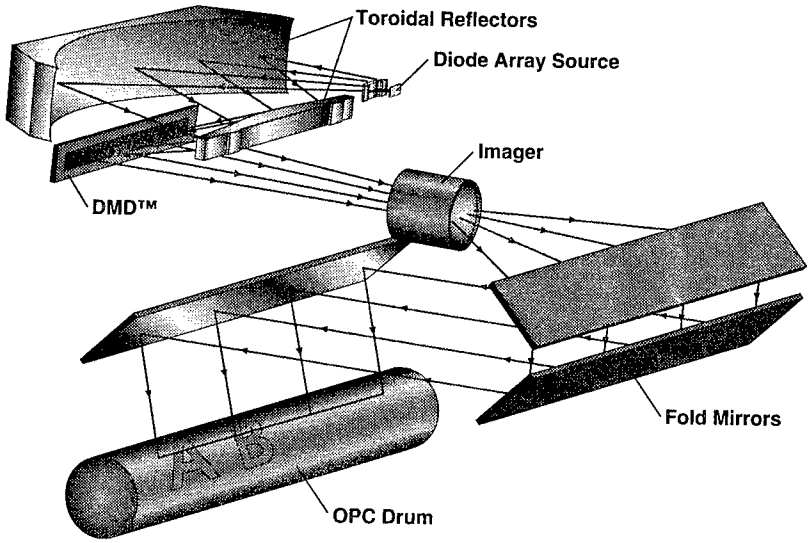


Figure 2. Optical Schematic of DMD Printing System

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A MEMS-Based Tunable Infrared Filter for Spectroscopy

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A strong need exists for compact, low cost real time chemical analyzers for application to process control and environmental monitoring. Advances in MEMS and micromachining technology may provide means to meet these needs. The infrared region of the electromagnetic spectrum is rich in information about chemical composition and temperatures in the local environment. The ability to cost-effectively analyze the IR spectrum would provide the user with significant information about the environment being sampled.

We report here on the development of a tunable high-pass infrared transmission filter for application to chemical detection and IR spectral analysis. The tunability of the filter allows one to vary the long-wavelength cutoff over the useful wavelength range of the detector material. Figure 1 shows a drawing of the concept. The tunable filter uses an electromagnetic actuator to mechanically drive the filter structure, which consists of an array of vertical parallel metal plates connected at the side edges by springs or flexures. When driven by the actuator, the flexures allow the plate spacing and the transmission properties of the filter to be changed while keeping the filter plates parallel and equally spaced. The cutoff behavior of the filter is expressed in terms of a characteristic wavelength:

$$\lambda_c = 2d$$

where d is the plate spacing. Because of the wealth of spectroscopic information in the 2-to-30 μm wavelength region, we want to be able to control the plate spacing from approximately 1 to 15 μm.

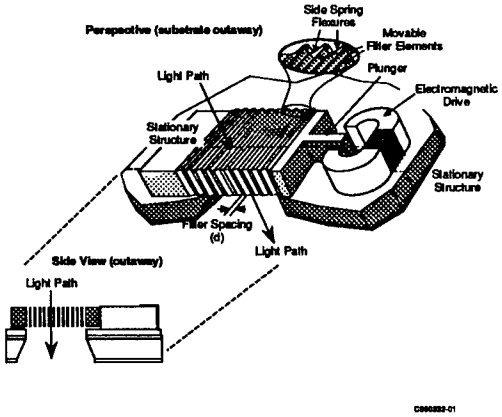


Figure 1. Tunable IR filter concept showing vertical parallel structure and linear magnetic drive actuator.

Figure 2 shows the measured IR transmittance characteristics for a set of LIGA-fabricated (1) fixed filters with d-spacing varying from 4 μm to 13 μm. As predicted, the wavelength cutoff occurs at twice the filter plate spacing. The filters were made of electroplated Ni; the LIGA process was used because of its ability to yield extremely precise metal microstuctures with very high aspect ratios.

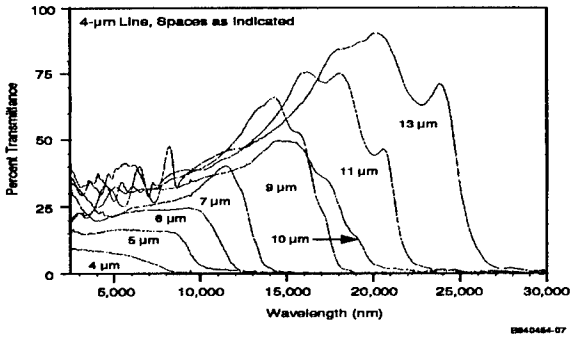


Figure 2. Measured transmittance for a set of fixed space filters with 4 μm lines and spacings from 4 to 13 μm.

Tunability of the filters is achieved by incorporating a spring flexure system to allow expansion or contraction of the filter plate spacing. Figure 3 shows a SEM of a tunable filter structure. The design is such that as the structure is compressed or extended, the flexure elements will bend while keeping the filter plates in the center of the structure parallel and equally spaced. Consequently, the one filter in Figure 3 can achieve the filtering action shown by the several fixed filters of Figure 2. If the grating spacings can be controlled to sufficient tolerances, an infrared spectrometer can be realized.

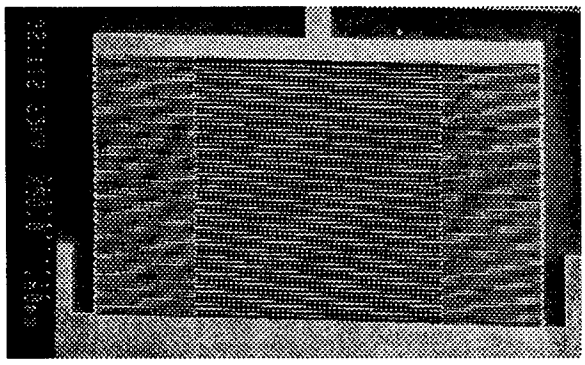


Figure 3. SEM photograph of a LIGA filter structure which incorporates a spring flexure system for filter tunability.

A LIGA-based actuator is used to drive and control the tunable IR filter structure. The design objective for the actuator is to have a force output greater than ~ 1mN with large travel (>>100 μm) to sufficiently tune the filter structures, which are initially 1 mm^2 in area. A second design objective is that the force vary linearly with current and be relatively independent of actuator position to smoothly vary the displacement of the actuator with the mechanical spring load. The large forces and travel are more compatible with magnetic actuation than electrostatic actuation.

Figure 4 shows a SEM photograph of a LIGA fabricated actuator-filter assembly. The parts are made of electroplated permalloy (78% Ni, 22% Fe). At resonance, displacements of 250 μm have been measured with a power dissipation of only several milliwatts. More advanced linear actuator designs have shown displacements exceeding 1mm.

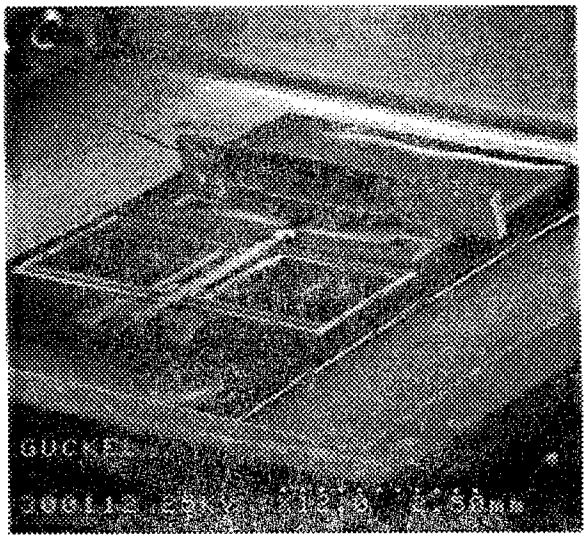


Figure 4. Assembled LIGA filter-actuator structure.

At the time of this writing, mechanical tunability of several filter designs have been demonstrated. Presently, evaluation of the mechanical and optical properties of the tunable filters is underway. The latest results will be reported and prospects for a compact low cost MEMS-based infrared analyzer will be discussed.

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4:00pm - 4:15pm
WD2

Silicon Etalon Arrays For IR Transform Spectroscopy

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A model, simulations, and fabrication concepts are presented for a spectrometer-on-a-chip : an array of micromachined stepped-thickness, low-finesse, silicon etalon plates, optically coupled to an IR detector array.

Fourier-transform infrared (FTIR) spectroscopy provides the well-known optical advantages of high throughput and multiplexing. Typically however, FTIR is implemented with a Michelson interferometer having a beam splitter and an opto-mechanical, moving mirror. MEMS provides design opportunities to avoid the beam splitter and all moving components, as well as to greatly reduce the size and complexity of FTIR spectrometers. Our design is based on the Fabry-Perot (FP) interferometer, or more accurately, an array of these, that each receives the same IR beam, i.e., optically in parallel [1,2]. The array of FP interferometers is an array of solid etalons, micromachined from a single silicon wafer, but each with a unique thickness and hence etalon fringe pattern. The fringe-modulated IR is passed to an array of broad-band IR detectors (such as bolometers) [3,4], in one-to-one correspondence with the etalon array. The detectors integrate the spectral bandwidth, and the array of output signals can be made to correspond to an interferogram of the incident IR spectrum [1-4]. This interferogram passes into a digital computing device, which calculates the inverse transform based on a knowledge of the detailed fringe patterns of the etalon array. Low-doped or cryogenic silicon wafers are suitably transparent over much of the IR spectrum, and the high index-of refraction assists in some aspects of the design of our device. Further, we have constructed a detailed model of the optical and electrical processes in our design and run many simulations, which have allowed us to determine design opportunities and critical parameters. For example, the spectral fidelity of the entire spectrometer is improved by *not* using high-finesse etalons, which will improve fabrication reliably and lower the cost. Methods to fabricate the etalon array by micromachining are reviewed, including processes that require only one timed wet-etch in KOH solution. The total array area need not be more than a few square centimeters [1].

The optical function of the etalon array is similar to that of a single etalon in step-scan mode, but now the array performs all interferometry at each step position simultaneous in time and parallel in space [5,6]. Simulations of models with 256 etalon elements indicate that excellent calculated spectra (inverse transform) can be obtained for realistic fabrication design choices. The choice of the series of etalon-plate thicknesses across the array is critical. Essentially, the thinnest plate must have fringes wide enough that one will span the IR-spectral bandwidth of

interest, i.e., the series fundamental in the transformed representation. The thickest plate must have several fringes within the bandwidth, but not so many as to exceed the Nyquist criterion. High finesse may result in fringes that are so narrow that some spectral portions of the bandwidth are not well sampled by any of the etalons in a finite number of array elements. Low finesse results in over sampling. The finesse of the fabricated array can be adjusted by thin-film gold.

The transmission $T(\nu)$ through an etalon is given by Airy's formula. Consider an array of M etalons, with thicknesses d_j, for j =0,1,2,...M. The fringe mode spacings are $\Delta\nu_j(d_j)$, the transmission spectral functions $T_j(\nu)$, and, in discrete form, the frequency is ν_i, for i =1,2,...N (N>>M). Then, the incident irradiation $I(\nu)$ becomes I_i, and the transmissions $T_j(\nu)$ a rectangular matrix Ω_{ij}. We define an instrument function $Z_{mn} = \Omega_{mi}^{T}\,\Omega_{in}$. The $Z_{mn} = 0$ for $m \neq n$, if the $T_j(\nu)$ are orthogonal. The interferogram, or transform of $I(\nu)$, is then $V_j = \Omega_{ji}^{T}\, I_i$ (i.e., the detector-array voltages). For Z_{mn} not fully diagonal, define $U_k = Z_{kj}^{-1}\, V_j$, then the inverse transform is $P_i = 2\,\Omega_{ik}\, U_k$, where ideally the $limit(P_i) \rightarrow I_i$, for sufficiently large M.

To gain insight into the effect of design choices, such as the series d_j and the finesse, we have coded the model are run simulations. As an example, for the IR band of 2000 to 4000 cm^{-1}, a 128-element array will have $P_i = I_i$ within ~1% for an incident Lorentzian line with FWHM of 50 cm^{-1}. We find that techniques such as apodization and Fourier filtering of the interferogram can improve on the overall transform quality.

Tedious fabrication of large arrays by a timed, anisotropic, wet etch of one element at a time may be avoided if the following scheme is used. Silicon wafers with one surface a few degrees off-axis (i.e., vicinal) could be fitted with a stencil mask and etched in one step, to result in a sequence of etalons spread across the wafer, each a thickness increment from its neighbors. We have run Monte-Carlo etch simulations of various types of vicinal surfaces, and find that a particular choice of (111) surface may be most suitable. Essentially, anisotropic etch rates allow the vicinal Si(111) to reorient, within the etch-mask opening, until an on-axis (111) surface forms. This on-axis facet, in the bottom of each etch pit, will then be accurately aligned with the backside face, which is also (111), and hence form the etalon optical cavity. Roughness of the etched etalon faces must be controlled, but since low finesse is desired, this should not be a difficult criterion to meet. The optical fill factor will not be particularly high, but the planar layout of the companion array of detectors is simplified by more modest fill factors, and the system sensitivity of this on-chip-spectrometer will not suffer unduly due to the high throughput of transform spectrometers.

Supported by U.S. Dept. of Energy, SBIR program (DE-FG05-93ER81507).

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4:15pm - 4:45pm (Invited)
WD3

Integrated Micro-Optical Interferometer Arrays

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Surface micromachining is an emerging technology that has rapidly found its applications in optoelectronics and micro-optics. Micromachining technology will become even more attractive to optical applications if micromechanical devices can be treated as readily available add-on structures to photonic devices such as lasers, detectors, and modulators for new functionalities. Recently, we have developed a low temperature, low stress surface micromachining process that has such features. Using this technology, we fabricated micromachined Fabry-Perot tunable filters and integrated them with various optical devices operating at 1.3/1.55 micron wavelength regimes.

Figure 1 shows a micromachined Fabry-Perot tunable interferometer. The front mirror of the device was made of three and a half periods of quarter wavelength Si/SiO_2 layers and was located at the center of the membrane released from the substrate. The back mirror had a similar structure as the front mirror and was deposited directly on a double-polished silicon substrate. Underneath the back mirror was an evaporated aluminum layer that defined the aperture of the tunable Fabry-Perot interferometer and was used as the bottom electrode. To facilitate optical coupling, the mirror aperture had a diameter of 50 microns or greater, matching the size of a multimode optical fiber. The corrugated structures at the peripheral region of the membrane enhance the stiffness of the membrane to maintain an optically flat surface, critical to the performance of the optical filter. The holes were etched to facilitate the release etching of the sacrificial layer between the substrate and the membrane and to relieve the material stress. The membrane was made of a 1.3 micron thick sputtered TiW layer sandwiched between a 1.1 μm CVD oxide layer and a 1.36 μm Si/SiO_2 Bragg mirror. The supporting beams are typically 10 μm wide and about 100 μm long. The length of the vertical F-P optical cavity is about 3 μm. We used polyimide as the sacrificial layer, which was cured at 240 °C and then removed by isotropic O_2 plasma to release the membrane. For membranes of a size of 140 microns, the release etching takes about 60 minutes.

The transmission properties of the devices were measured using two multimode fibers for input and output light coupling. A broadband light emitting diode covering a spectral range of 0.9 μm to 1.6 μm was used to provide the input light. The light that passed through the micromachined F-P tunable filter was coupled into the output fiber and detected by an optical spectrum analyzer. To compare the changes of optical properties before and after membrane release, we measured the transmission spectrum of a device with a 50 micron diameter aperture in both cases, as shown in Fig. 2. Before membrane release, the full-width-half-maximum (FWHM) of the transmitted light is about 3.7 nm. After release etching, the transmission spectrum was broadened to about 5 nm. These values agree qualitatively with the theoretical values: 2 nm FWHM for the unreleased device and 3.2 nm FWHM for the released device. Comparing the transmitted power of the F-P interferometer before and after release, we derived the loss of the released interferometer to be about 5 dB. Other evidences showed that this loss was predominantly due to the curvature of the released front mirror. The tuning of the transmission spectrum was

achieved by applying a voltage to the released membrane. Figure 3 shows the tuning characteristics for two different devices with different mechanical designs (different spring constants). The x-axis shows the square of the applied voltage, proportional to the displacement. A tuning range of 40 nm and 60 nm was achieved for these devices at a maximum applied voltage of 65 Volts. With an improved design of the mechanical structure, a substantial reduction of the applied voltage is achievable. In addition, the motion of the top mirror is only a very small fraction of the cavity length (< 10%), so there is no concern about the stiction of the top mirror to the bottom mirror during device operation. Such micromachined tunable interferometers can be fabricated on nearly any substrates including Si, quartz, GaAs, and InP and can be integrated with surface emitting lasers, LEDs, and detectors.

This work is partly supported by NSF, ARPA, and JSEP/AFOSR. The devices were fabricated at the Cornell Nanofabrication Facility (CNF) sponsored by the National Science Foundation and the industrial affiliates.

1. A. T. T. D. Tran, Y.-H. Lo, Z.H. Zhu, D. Haronian, E. Mozdy, IEEE Photon. Technol. Lett., vol. 8, pp. 393-395, 1996.

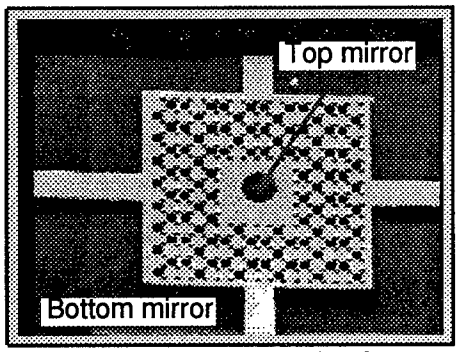


Fig. 1 SEM photograph of a micro-machined Fabry-Perot interferometer.

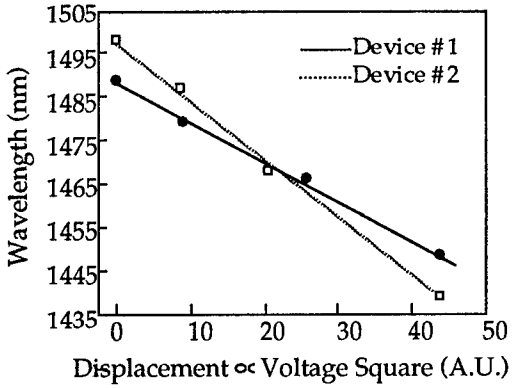


Fig. 3 Wavelength tuning characteristics for two tunable F-P interferometers.

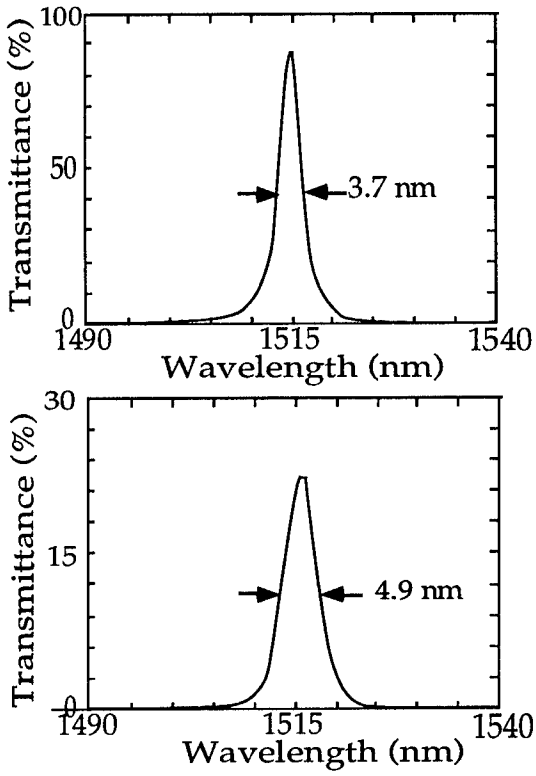


Fig. 2 Transmission spectrum of an unreleased (upper) and a released (lower) F-P interferometer.

4:45pm - 5:00pm
WD4

Micromechanical Slit System in HPLC Diode-Array Detection

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Introduction

Most conventional spectrophotometers allow the widths of the entrance slit and of the exit slit to be varied. The slit widths are adjusted to improve the sensitivity or the spectral resolution of the spectrophotometer. Spectrophotometers with diode-array detection have one fixed entrance slit only. The 'exit slit' function is realized by electronically combining the output signal of adjacent photodiodes [1]. However, a complete optimization of sensitivity versus resolution cannot be achieved with only one fixed entrance slit. With the availability of modern photodiode arrays, which exhibit a higher dynamic range, the need for a cost effective and reliable variable entrance slit is increasing. The most critical issue is the reproducibility of the slit center position in the submicron range. The solution to meet this requirement and to increase the flexibility in HPLC diode-array detection is presented in this paper.

Technical Solution

The slit device developed combines both silicon bulk-micromachining elements with precision mechanical parts (Fig.1). The slit plate, machined out of a monolithic piece of silicon, comprises a set of discrete slit widths (including a shutter position) and their guiding structure for positioning the slits under a fixed aperture plate. The rectangular center hole of the aperture plate defines the slit height for each slit positioned beneath it. The flexible beam structure was designed to allow millimeter-long linear translations with a reproducibility of the slit center position of better than ±0.01 µm. Translations of the slits take place by means of transmission gears connected to a standard miniature stepping motor. The mechanical stops, which limit the slit displacements, are utilized for referencing the count of steps required for positioning each slit under the aperture hole. The slit pitch is oversized with respect to the slit height and takes any positioning inaccuracy associated with the use of a stepping motor into account. The displacement force can easily be produced by the stepping motor, and the currentless holding torque of this actuator is strong enough to maintain the slits in any position when a gear reduction ratio of approximately 3:1 is implemented. An aluminum cover unit (not shown in Fig.1) protects the slit displacement mechanism.

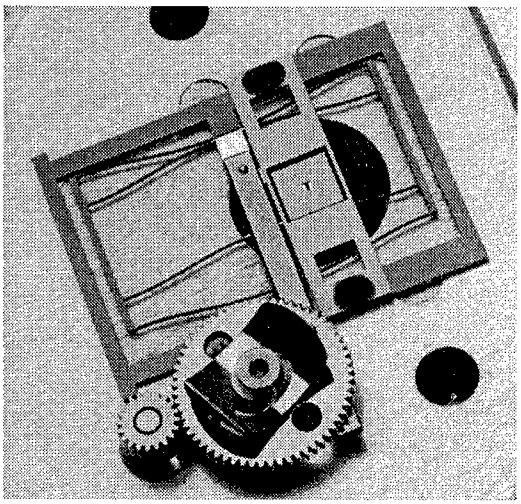


Fig 1: Close-up view of the developed slit device showing the slit displacement mechanism.

The slit and the aperture plates are anisotropically etched silicon plates using standard bulk-micromachining techniques [2]. Optical slits and flexible beams are produced simultaneously with high accuracy in batch processes.

Application

The optical slit width plays an important role in a HPLC diode-array detector as it determines sensitivity and spectral resolution. The programmable slit device can change optical slit widths to either 1, 2, 4, 8 or 16 nm in less than a second. To demonstrate the flexibility, benzene was used because of its fine spectral structure. As shown in Fig.2 an optical slit width of 2 nm already provides an excellent spectral resolution, the fine structure of benzene is well separated. If higher sensitivity is required the optical slit width is opend, for example to 8 nm, to improve the chromatographic signal-to-noise ratio at the expense of resolution (see again Fig.2). The fast switching speed and the remarkable resettability of the slit may allow for other interesting possibilities. For example, the slit width could be time-programmable in a chromatographic run.

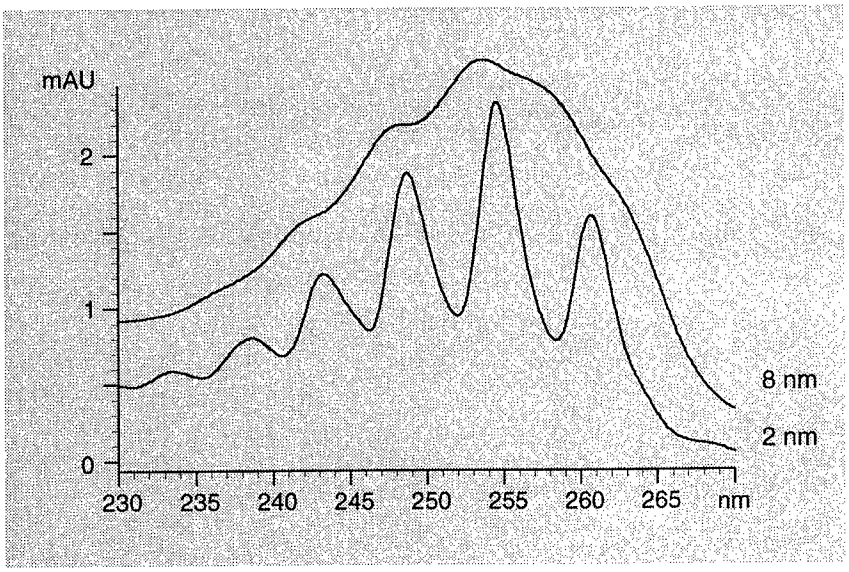


Fig.2: Spectral resolution of benzene using different optical slit widths.

Conclusions

The remarkable performance of the micromechanical slit device makes it possible to equip diode-array detectors with adjustable entrance slits. The device combines the required optical functions, i.e., slit and shutter, in a simple, reliable and compact component. The slit width is directly controlled by the microprocessor of the instrument and can be set as method parameter. It is used in the HP1100 Series HPLC Diode-Array Detector.

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Thursday, August 8, 1996

SESSIONS:

ThA: Micromachining on Compound-V Semiconductors I

ThB: Free-Space Optics

ThC: Micromachining on Compound-V Semiconductors II

ThD: CAD/Metrology

8:30am - 9:00am (Invited)
ThA1

Broad-Range Continuous Wavelength Tuning in Microelectromechanical Vertical-Cavity Surface-Emitting Lasers

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Abstract: A single-mode continuous wavelength tuning range as large as 18 nm is achieved in a vertical-cavity surface-emitting laser employing a suspended micro-electro-mechanically-movable deformable membrane mirror.

Wavelength-tunable semiconductor diode lasers have potential applications ranging from wavelength division multiplexed optical communications and interconnects to spectroscopic remote sensing. A wide and continuous tuning range is desirable in many of these applications. However, monolithically-fabricated devices are typically tuned by modulation of the refractive index through thermal or carrier injection effects, and have been limited to a fractional tuning range of 1% at most [1,2]. Besides imposing tuning range limits that are much smaller than the gain bandwidth of the active layer, these effects can also impose excess loss or have undesirable consequences for the gain medium. Tuning based on micromechanical modulation of the physical cavity length does not face these limitations, and is especially suitable for the short cavity lengths in vertical-cavity surface-emitting lasers (VCSELs). We have developed a number of devices based on the micromechanical motion of a suspended gold/silicon nitride/GaAs top mirror. We demonstrated a tunable resonant-cavity light emitter (RCLED) with a 40 nm wavelength range operating near 970 nm [3], and achieved pulsed laser oscillation in a similar device, yielding a 15 nm range [4]. Unfortunately, these proton implant-isolated structure suffer from poor efficiency because of excessive leakage current. However, by employing AlAs-oxide confinement, we have achieved continuous-wave operation of a VCSEL operating in a single longitudinal and transverse mode and continuously tunable over 18 nm, for a relative tuning of over 1.8% [5].

The general device structure, depicted schematically in Fig. 1, consists of a bottom mirror, semiconductor cavity, air gap, and a deformable-membrane top mirror. The bottom mirror is formed by a 22.5 period GaAs/AlAs distributed Bragg reflector (DBR) with a center wavelength λ_0 near 975 nm, and the $2\lambda_0$ GaAs cavity contains three 5 nm $In_{0.2}Ga_{0.8}As$ / 5 nm GaAs quantum wells (QWs) placed within the intrinsic region of a *p-i-n* diode. The membrane is a three layer structure made of a 120 nm thick Au reflector/electrode on top of a 380 nm thick SiN_XH_Y phase-matching layer and GaAs quarter wave layer. The central reflector of the membrane is attached by four flexible legs to rigid contact pads, and the air gap thickness is modulated around $3\lambda_0/4$ as a result of electrostatic force from applied voltage bias between the suspended membrane and the underlying semiconductor p-layer. The membrane, air gap, and air/semiconductor-cavity interface effectively form a distributed top mirror with a tunable phase shift and a total reflectance predicted to be above 99%. Diode drive current is injected from four intracavity p-type contact fingers and from the n-substrate contact, and lateral injection is confined by means of an AlAs-oxide current blocking layer [6].

VCSELs with 16 μm to 30 μm square top reflectors and current apertures less than 10 μm demonstrated CW threshold currents as low as 5.5 mA, threshold voltage of 3-4 V and slope efficiencies of around 0.01 W/A, as shown in Fig. 2. Pulsed output in excess of 300 μW was obtained. The low efficiency is likely due to a combination of loss in the top mirror, quantum well design, and low output coupling in the bottom DBR. Spectra reveal mode suppression ratios in excess of 20 dB. In Fig. 3(a), superimposed spectra for various membrane-p bias voltages are shown, and the wavelength vs. voltage curve is plotted in Fig. 3(b). A continuous single-mode tuning range of up to 18 nm was obtained for a membrane voltage ranging from 0 to 20.5 V and constant drive current. This corresponds to a vertical membrane motion of approximately 200 nm. Tuning ranges larger than 20 nm are seen in multiple-transverse-mode devices. The blue shift of lasing wavelength with increasing membrane bias is characteristic of electrostatic force, which is attractive in nature and parabolic with respect to voltage. Since the output power does not roll off

at the long wavelength edge of the tuning range, we believe even wider tuning can be achieved in devices with a longer zero-biased lasing wavelength and therefore better alignment of the cavity wavelength range to the gain spectrum. Ultimately, the wavelength range is limited by the large threshold gain required for the excessive loss in the membrane; improved top mirror designs should extend this range. The transient wavelength-switching response was also characterized in these devices. A switching risetime of 1 μs was observed with a settling time of 3-5 μs due to the underdamped motion of the membrane. By comparison, RCLED membranes with thinner metal and nitride layers exhibited risetimes of under 350 ns and settling times of 1-2 μs.

In summary, we have demonstrated continuous wavelength tuning as wide as 18 nm near 975 nm in a microelectromechanically-tuned deformable-membrane VCSEL, with wavelength switching times suitable for many applications.

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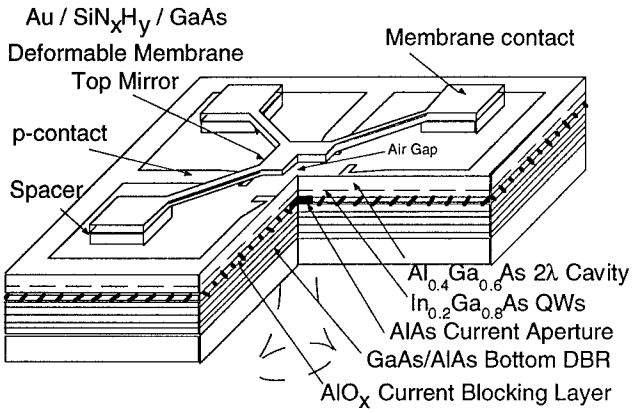


Fig. 1 Schematic diagram of the microelectromechanical tunable vertical-cavity surface-emitting laser.

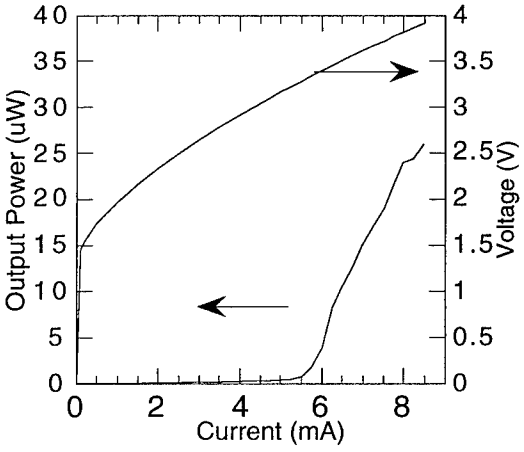


Fig. 2 Light-voltage-current characteristics for the laser diode with zero-biased membrane tuning voltage.

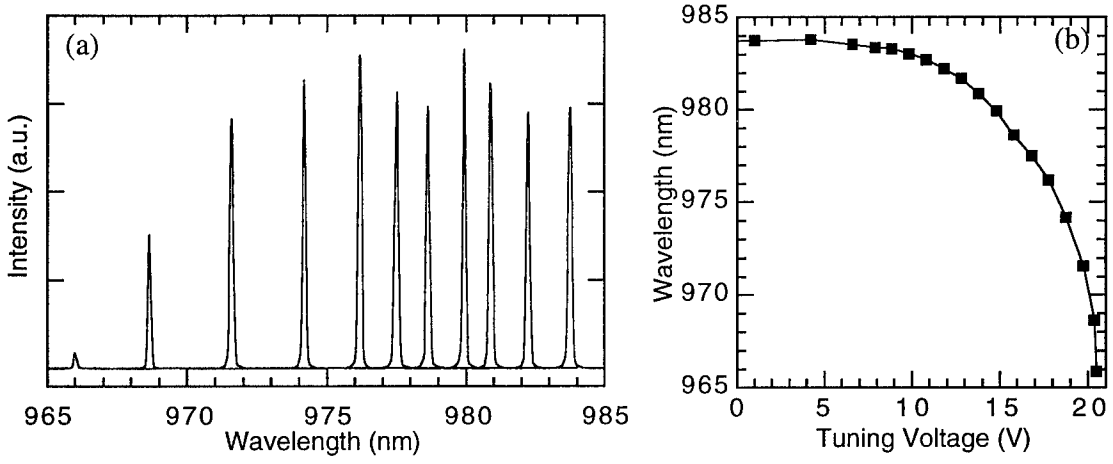


Fig. 3 (a) Spectra taken at various membrane tuning voltages spanning the range from 0 V - 20.5 V and a constant diode current. (b) Lasing wavelength as a function of tuning voltage.

Invited paper

Coupled-Cavity Laser Diode with Micromachined External Mirror

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Introduction

Micromachining technology presents a great opportunity for developing on-chip mechanical components that can be integrated with a laser diode (LD). We have developed micromachined external mirrors to composite a compact coupled-cavity LD for both optical-communication and optical-sensing systems.

Tunable laser diode with silicon micromachined external mirror

Vertical silicon plate with a high aspect ratio such as more than 100-μm high and a few-μm thick can be fabricated by anisotropic etching of (110) silicon. This enables a micro-deflection mirror to be made with large area for free-space micro-optics[1]. We have fabricated a tunable LD (TLD) with silicon micromachined external mirror by using this technology[2]. An SEM photograph of this device is shown in Fig. 1 (a). The (111) sidewall of the actuated cantilever beam functions as an external mirror for the LD bonded near the beam. Figure 1 (b) shows the wavelength variation as a function of the excitation voltage of the actuation mirror. The wavelength varies discretely within a period of about 3 nm. The discrete variation interval was 0.3 nm, which coincides with the Fabry-Perot mode of the LD cavity length, because there was no anti-reflection coating on the LD facet facing the mirror.

Tunable laser diode with nickel micromachined external mirror

Mold and plating technology is one of the simplest and most practical ways to fabricate a metallic microstructure for MEMS. Metallic materials, such as nickel, which have better optical reflectance than silicon, are suitable not only for mechanical components, but also for optical mirrors. We developed an electrostatically actuated micromirror fabricated by nickel surface micromachining. The SEM photograph of the nickel micromirror and the schematic drawing of TLD with nickel micromirror are shown in Fig. 2 (a) and (b). The LD is closely bonded to the mirror on the actuator chip. The mirror is actuated by a comb-drive actuator to change the length of the external cavity of the LD precisely.

GaAs micromachined coupled cavity laser diode

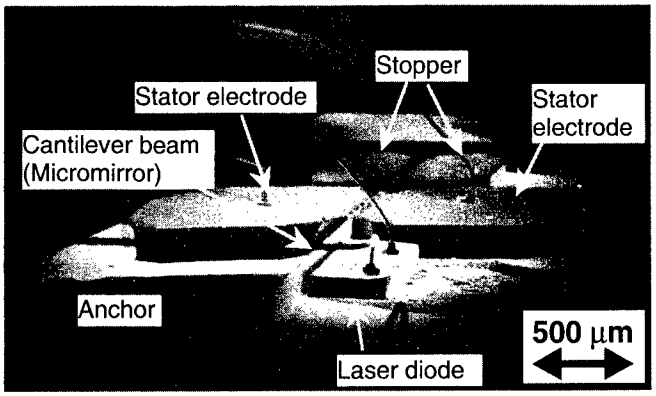
We have monolithically integrated a microbeam resonator with two LDs and a photo-diode by using an AlGaAs/GaAs micromachining[3,4]. As shown in Fig. 3, the microbeam sidewall and the detection LD facets compose the short-coupled cavity LD. An intensity-modulated light beam from the excitation LD induces thermal stress in the cantilever beam, causing it to vibrate. This vibration is detected by the LD-PD sensor on the other side of the beam. Good compatibility with the LD process makes it possible to integrate a micromechanical structure with a LD without degrading the LD characteristics. Because the microbeam is very small (110 μm), its natural frequency is 0.2 MHz, which can thus detect a mass of molecules of about 7×10^{-11} g.

Conclusion

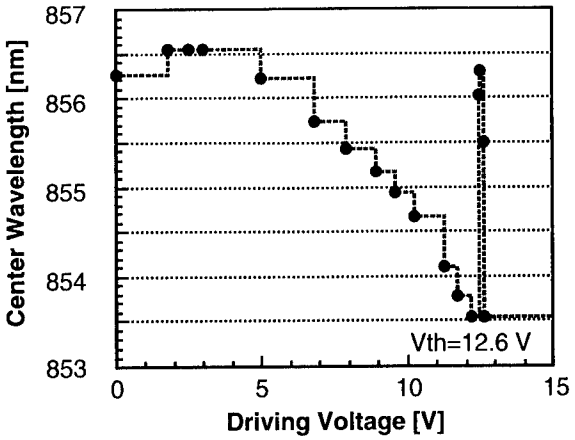
Incorporating MEMS into optical devices will open up the new field for optical devices system that integrate micromechanics and micro-optics.

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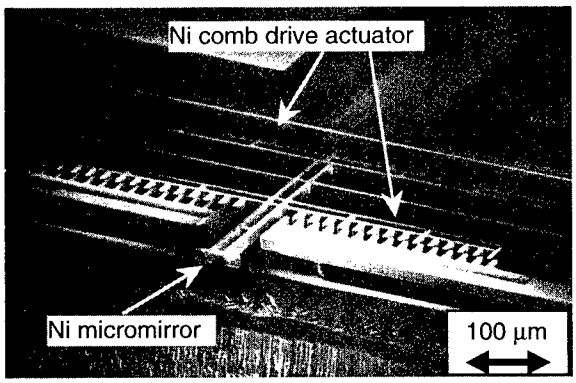


(a) SEM photo of the device

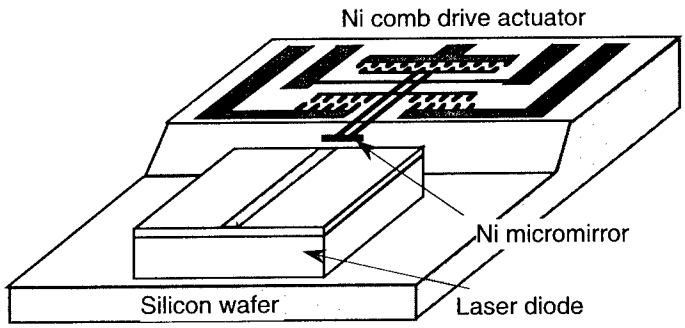


(b) Wavelength tunability

Fig. 1 Tunable laser diode with silicon micromirror.

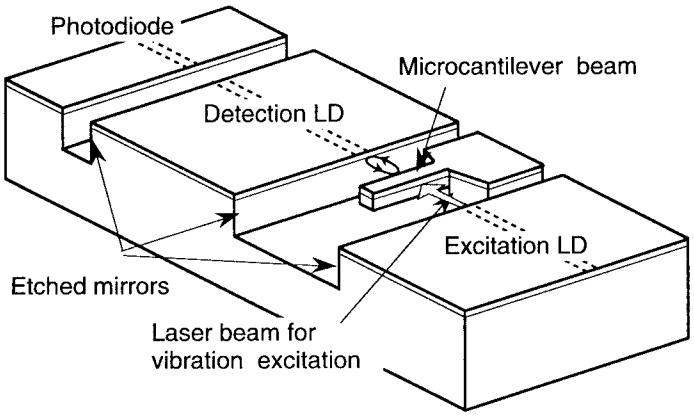


(a) SEM photo of the nickel micromirror

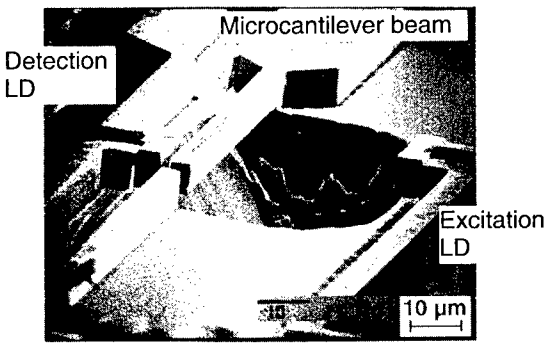


(b) Schematic of tunable laser diode with nickel micromirror

Fig. 2 Nickel micromirror for an external cavity of a laser diode.



(a) Schematic drawing



(b) SEM photo of the main part

Fig. 3 Microbeam resonator sensor.

9:30am - 9:45am
ThA3

Monolithic Optical Interferometers for MEMS Applications

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Switzerland

For high-resolution optical measurements, interferometry is often the technique of choice. The ability to perform optical interferometry inside a microsystem may prove to be lucrative for many MEMS systems, where small size, high physical robustness and reduced needs for optical alignment are of primary relevance. For these reasons, the combination of photonic integrated circuits (PICs) with MEMS may lead to microsystems of considerable physical ruggedness, high functionality and small size.

PICs are monolithically integrated semiconductor optical circuits, typically including lasers, waveguide circuits and photodetectors, and often modulators and grating structures. As with most ICs, volume semiconductor batch fabrication is an attractive feature. Due to their suitability for light emission and their efficient electro-optic behavior, the III-V materials are almost exclusively employed; considerable interesting and challenging work then revolves about the hybrid assembly of such PICs with Si-based MEMS structures.

We discuss here two monolithically integrated interferometric sensor systems of interest for MEMS applications. The first is an optical displacement measurement microsystem on a chip; this system consists of a Michelson interferometer with an integrated DBR laser, waveguide photodetector and phase modulators. The second is configured as a Mach-Zehnder interferometer and is used for high-resolution refractometry with applications in biological and chemical sensing. Both of these sensor PICs employ the same optical and optoelectronic devices and share closely related fabrication technologies.

The integrated interferometers were based on a GaAs/AlGaAs double heterostructure laser substrate, with one or more quantum wells in the active region; a selective vacancy-enhanced disordering process was used to define transparent and absorbing regions on the single substrate such that only one epitaxy step was required. A distributed Bragg reflector (DBR) laser was used as a light source, employing a 3rd order (Λ = 385 nm), holographically defined grating etched into a recess above the waveguide core and emitting at 820 nm. Monomode operation, essential for a clean interference characteristic, was achieved; the discrete device had a linewidth of 500 kHz, implying a coherence length of 600 m. Typical output powers were 5 mW with threshold current densities on the order of 1.3 kA/cm^2. The waveguide photodetectors had responsivities of 0.6 A/W and dark currents of 500 pA for device areas of 3x500 μm. Phase modulation relied on the quantum-confined Stark effect (QCSE).

The displacement measurement chip, shown in Figure 1, employs an optical measurement beam, emitted from the upper arm of the interferometer, which is reflected from an external object and returned to the interferometer by the same waveguide; this reflection interferes with a reference beam, returned from the cleaved facet at the edge of the chip, and the interference signal is measured by the detector. Examination of a typical interference characteristic shows that one interference fringe is seen for each 408 nm of displacement, as measured by the photodetector current. Length resolution is thus better than

100 nm, dependent on system noise; maximum measurement distance is at present 45 cm. The addition of a second, phase-shifted reference beam allows the generation of two signals in phase quadrature thus permitting a determination of movement direction as well as displacement; the lower interferometer in the figure has the QCSE modulators for this purpose. Current work is studying the expected improvement in resolution to below 10 nm using this structure.

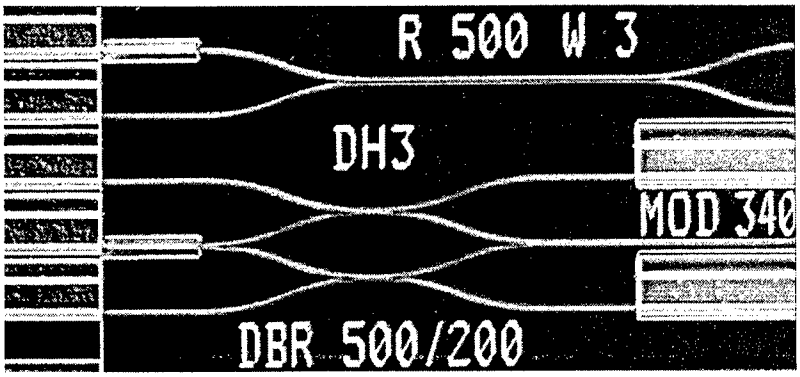


Figure 1: Michelson interferometers for displacement measurement. DBR lasers and photodetectors are on the left. The lower device also has two phase modulators on the right. Total chip length is 2 mm.

An integrated optical transducer for the translation of environmental refractive index shifts into optical intensity changes, using the same optoelectronic components, is also under development. This PIC is based on a Mach-Zehnder interferometer and is used for refractometric biological/chemical sensing. One arm of the interferometer, shown in the SEM photograph of Figure 2, contains a dielectric waveguide sandwich of which the core is exposed. A change in the refractive index of either a chemically selective film deposited on this waveguide or a fluid in contact with the core, leads to a relative phase shift in the one interferometer arm and thus an interference signal. Measurements using this configuration have demonstrated a refractive index resolution of 3×10^{-5} for a 2 mm long sensor region, a value currently limited by system drift.

Both of these monolithically integrated sensor PICs may be of interest for systems applications involving MEMS structures. Numerous hybridization techniques suitable for assembly and mounting of a PIC onto a Si substrate have been developed: the use of passive, physical alignment features, etched into both parts, is probably of particular relevance due to their simplicity and low additional cost. The displacement sensor, because of its reduced size and eliminated need for critical optical alignment, may be used for precision measurement in more complex opto-mechanical microsystems including movable electrostatic actuators, diaphragms and resonant beams; the sub-100 nm resolution currently attained is likely to be sufficient. Improvements in resolution, currently underway, may make the determination of AFM-tip movement appealing, suggesting means for the fabrication of more compact and robust hybrid AFM heads.

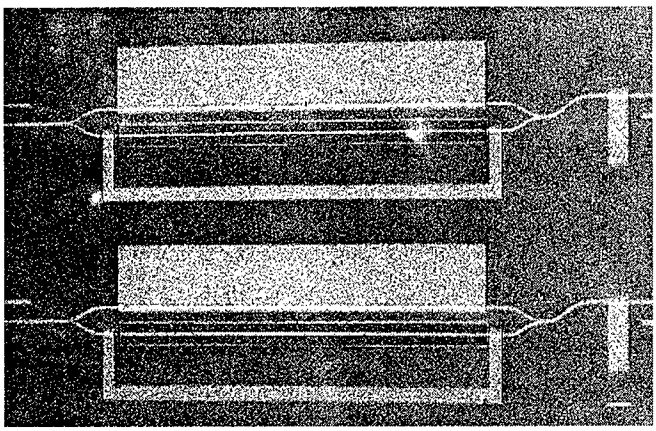


Figure 2: Mach-Zehnder interferometers for refractometric measurements. The length of the sensor region, in the lower arm, is 2 mm. The photodetector is visible at the right.

The integrated optical refractometer may be employed individually as a chemical sensor or in arrays as portion of an optical sensor microsystem. The use of Si MEMS-based flow cells, micropumps or fluid-handling systems may ease the development of compact and rugged chemical diagnostic units. The ability to easily fabricate multi-sensor arrays is a particularly attractive feature of such a PIC/MEMS hybrid.

11:00am - 11:15am
ThB2

Surface-Micromachined Micro-XYZ Stages for Free-Space Micro-Optical Bench

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UCLA, Electrical Engineering Department, Los Angeles, CA 90095-1594

The surface-micromachined free-space micro-optical bench (FS-MOB) has demonstrated its potential for monolithically integrating the entire micro-optical systems on a single chip [1]. Various three-dimensional micro-optical elements such as microlenses, mirrors, and gratings have been successfully demonstrated [2,3]. The surface micromachining fabrication process further enables on-chip optical alignment by integrating the free-space micro-optical elements with micropositioners such as translation or rotation stages. Vertically scanning micromirrors have been demonstrated for bar-code scanners [3]. In this paper, we propose a novel integrated XYZ stage with three degrees of freedom for precise on-chip optical alignment as well as input/output coupling for FS-MOB.

One application of the integrated XYZ stage is on-chip alignment of hybrid-integrated active optoelectronic components (e.g., semiconductor lasers or photodetectors) in micro-optical systems. Previously, we have demonstrated a self-aligned hybrid integration scheme which utilizes side-mounting approach to match the optical axis of the semiconductor laser with that of the micro-optical elements [2]. On the other hand, vertical adjustment of the optical axis is required in many other applications. Though vertical comb drive has been demonstrated, large travel distance in vertical direction is difficult. Recently, we demonstrated a monolithic optical beam steering structure to convert vertical movement into in-plane translation, which can be readily implemented by the standard surface-micromachining techniques. The beam-steering device, as shown in Fig. 1, consists of a pair of parallel, 45° mirrors. The upper mirror is integrated with a linear translation stage. Translation of the upper mirror achieves vertical adjustment *without angular squinting* of optical beams. This beam-steering device has been used to change the height of the optical axis of an upright-mounted semiconductor laser [4].

By combining the beam-steering device (Z-adjustment) with an XY stage, an integrated XYZ stage with three degrees of freedom can be realized. Figure 2 shows the schematic drawing of a micro-Fresnel lens integrated with the micro-XYZ stage. The incoming beam (a horizontal beam from an upright-mounted semiconductor laser in this example) is bent upward by the lower 45° mirror which is integrated with a linear translation stage. The X-adjustment (see Fig. 2 for definition of X, Y, and Z) is achieved by the translation of the lower mirror. The upper 45° mirror is orthogonal to the lower mirror and is responsible for the Z-adjustment. The Y-adjustment is achieved by the translation of the micro-Fresnel lens. Both the micro-XYZ stage and the free-space micro-optical elements are fabricated using the micro-hinge technique [5]. The translation stages can be integrated with comb drive actuators for fine-adjustment of beam position or combined with actuators with long travel distance to achieve optical scanning. The advantage of this unique design is that the X, Y, and Z position can be adjusted independently without any angular beam squinting. The micro-XYZ stage can be readily integrated with other surface-micromachined micro-optical elements, and is very useful for high performance single-chip micro-optical systems.

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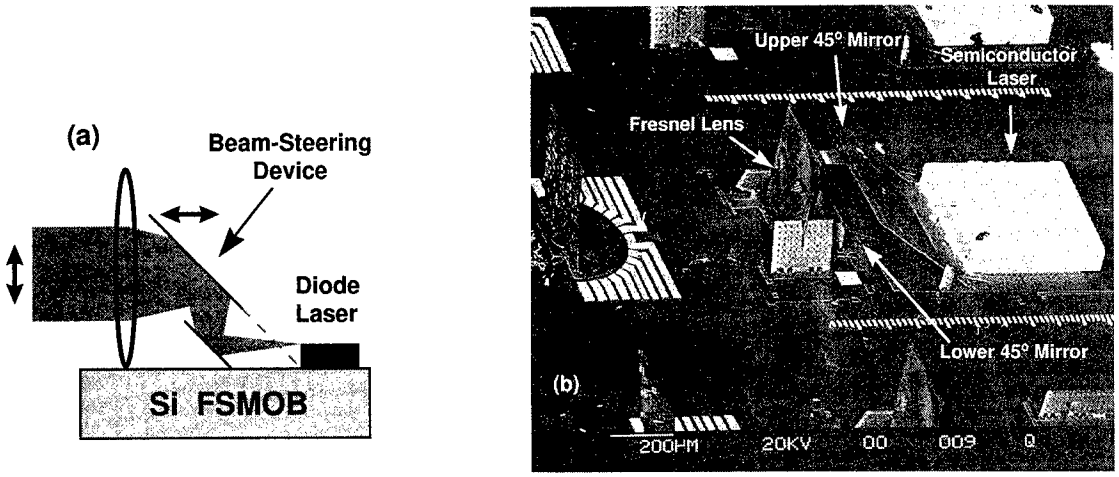


Fig. 1. (a) The schematic drawing and (b) the SEM of the vertical beam-steering device integrated with a micro-Fresnel lens

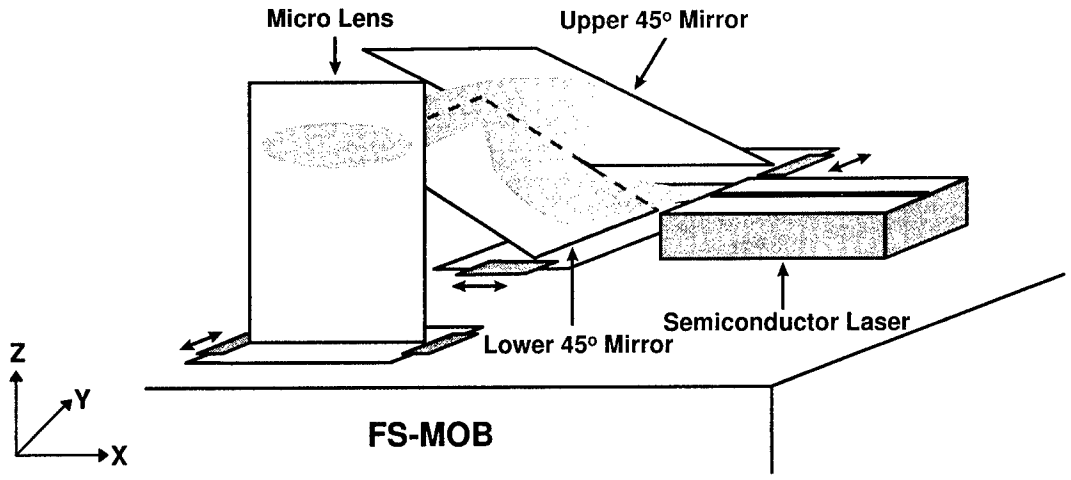


Fig. 2 The schematic drawing of a micro-lens monolithically integrated with the micro-XYZ stage.

A Surface Micromachined Rotating Micro-Mirror Normal to the Substrate

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Introduction

An optical mirror for directing a laser parallel to the substrate surface has been designed and fabricated. The mirror consists of a 214 μm x 210 μm, 3.5 μm thick polysilicon plate, coated with a 0.5 μm thick layer of gold. The mirror is connected to the substrate by 3 floating substrate hinges [1]. Using microprobes, the mirror is lifted off of the substrate and up into a latch mechanism as shown in Figure 1. The latch holds the mirror normal to the substrate. The floating substrate hinges are connected to a 200 μm diameter circular 2.0 μm thick polysilicon plate. This plate is mounted to the substrate via a rotating sliding anchor. The entire device after being lifted into position is illustrated in Figure 2. The mirror is designed to be driven by an array of thermal actuators, visible on the left of Figure 2. The actuators have been used in a micro-motor similar to the design presented here [2].

Fabrication

The mirror design was fabricated through the ARPA sponsored Multi-User MEMS Process (MUMPS) [3]. The MUMPS process is a surface micromachining process utilizing three structural polysilicon layers, separated with two sacrificial oxide layers. The first polysilicon layer is 0.5 μm thick and cannot be released from the substrate. The second and third polysilicon layers are both releasable and are 2.0 μm, and 1.5 μm thick, respectively. A 0.5 μm thick layer of gold can be deposited on the third polysilicon layer.

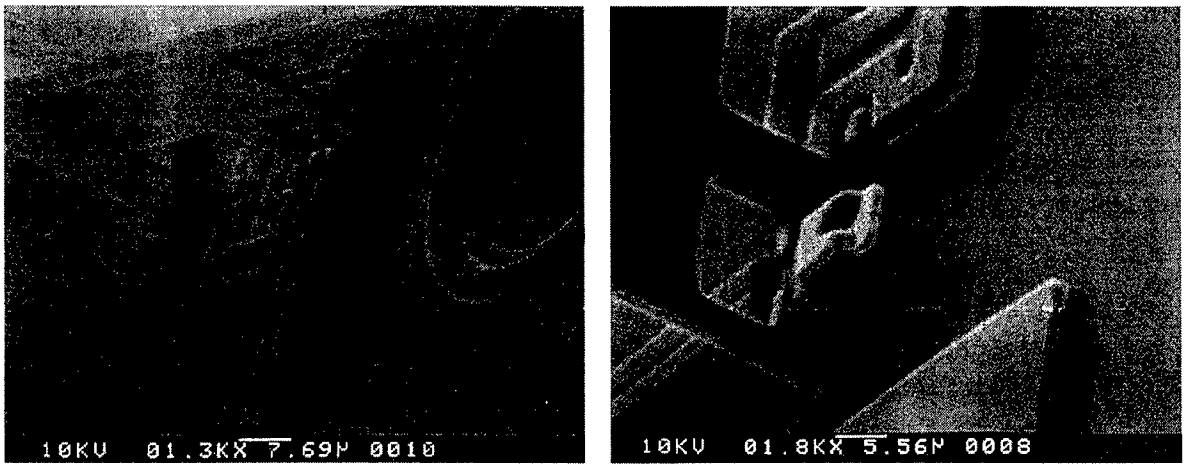
The polysilicon structures are released by etching away the sacrificial oxide layers in hydrofluoric acid. Using microprobes, the mirrors are flipped up off of the substrate and pushed into the latching mechanism. The mirrors are capable of rotating through a full 360 degrees, however, the drive system is only designed to rotate through a range of 90 degrees.

Discussion

The device design consists of three separate parts; the mirror, the rotating circular plate, and the thermal actuator drive system. The mirror is composed of both releasable layers of polysilcion combined together to form a 3.5 μm thick layer. At the base of the mirror 3 floating substrate hinges are used to hold the mirror. The floating substrate hinges are formed using both releasable polysilicon layers. The lower layer forms a thin 2.0 μm square pin connected to the mirror. This layer is also used for a surrounding support that encloses the pin in the lateral directions. The top polysilicon layer is used to form a cap for the hinge. The pin is thus trapped laterally by the support, and vertically between the top polysilicon layer and the substrate as seen in Figure 1.

The polysilicon hinge supports are connected to a 200 μm diameter polysilicon plate composed of the lower 2.0 μm thick polysilicon layer. To secure the mirror in the normal position, two supports are used. Each support is 179 μm long and 8 μm wide. A small notch is cut into the base of the mirror 14 μm above the pin to correspond with notches in the support. When the mirror is lifted off the substrate, the supports lock into the notch fixing the mirror in place. To mount the circular support, while still allowing rotation, a circular sliding anchor is used. The anchor consists of a circular structure formed from the top polysilicon layer covering the inside rim of the circular plate. The anchor is directly mounted to the substrate, but is not connected with the circular plate. This is visible in Figure 1 (a). The outside edge of the plate is composed of both releasable polysilicon layers to form a 3.5 μm thick rim. This rim has a serrated edge for interfacing with the driving actuator.

The thermal actuator drive system is based on that used by Comtois [2]. First, a single actuator is used to provide a locking mechanism. When engaged, the lock prevents the device from moving. The lock can disengaged by running current through the thermal actuator. Second, an array of actuators is connected to a 3.5 μm thick paw. The paw has triangular teeth to interface with the serrated rim of the circular mirror. Finally, the third set of actuators is used to push the paw towards the plate allowing the teeth to engage. Comtois has demonstrated that this type of actuator can provide bi-directional rotation [2].



(a) (b)

Figure 1. SEM images of a floating hinge, and the latch mechanism. (a) Front side. (b) Back side.

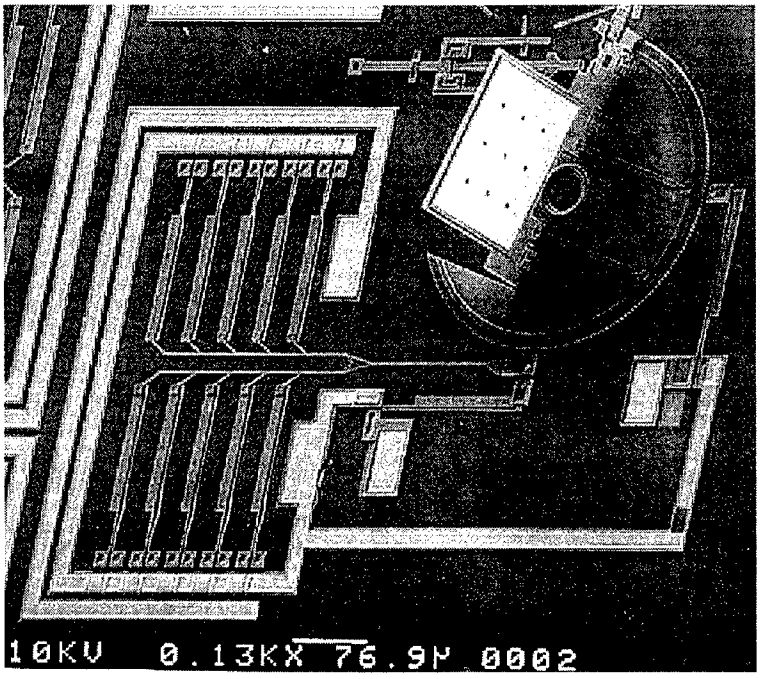


Figure 2. An SEM image of the rotating mirror flipped up normal to the substrate.

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11:30am - 11:45am
ThB4

An Electrostatically-tunable Switching Micromirror using (110) Silicon Wafers

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ABSTRACT A bulk-micromachined electrostatic micromirror has been designed, fabricated and tested for applications to tunable optomechanical switching microdevices. Static deflections of the micromirror have been measured up to 26.5μm with a DC threshold voltage of 330V. Resonant switching frequencies have been tuned in the ranges of 580-450Hz by varying the DC bias voltage within 50-300V for a AC drive voltage of 10V.

Recently, micromachined mirrors [1-4] have received an increasing attention due to their potential for optomechanical switching microdevices. In this paper, we present a *bulk-micromachined translational* micromirror (Fig.1), suspended *perpendicular* to the the substrates; while the previous work [1-4] has presented the *surface-micromachined torsional* micromirrors, suspended *parallel* to the substrates. The micromirror (Fig.1a), fabricated by an anisotropic etching of (110) silicon, has been suspended by two pairs of boron-diffused microflexures (Fig.1c); thereby generating an electrostatic motion *parallel* to the substrate. For the mirror deflection, the microflexures (Fig.1c) act not only as a mechanical flexural suspensin, but also as an electrical interconnection to the micromirror. The resonant frequency of the micromirror can be adjusted through the control of an electrostatic bias voltage between the micromirror (Fig.1a) and the counter-electrode (Fig.1b).

Figure 3 illustrates the microfabrication process for the microswitching mirror device (Fig.1). The process starts with the growth of 7000Å-thick thermal oxide layers (Fig.3a) on the both sides of a 400μm-thick (110) silicon wafer [5]. A boron diffusion process (Fig.3b) defines the microbeams (Fig.1c,d), while an oxide etch process (Fig.3c) defines both the micromirror (Fig.1a) and the counter-electrode (Fig.1b). An anisotropic EDP etching process(Fig.3d), based on the special corner compensation technique of Fig.4, defines the micromirror (Fig.1a), the counter-electrode (Fig.1b), and the boron-diffused microbeams (Fig.1c,d), simultaneously. The boron-diffused dummy supporting beams (Fig.1d) are destroyed after the bonding (Fig.3e) of the fabricated devices with the silicon base. (Fig.1f) Figure 5 shows the fabricated silicon microswitching device, where the high-aspect-ratio micromirror (1000μm-long, 400μm-high, 90μm-thick) is suspended by two pairs of the microflexure (1000μm-long, 90μm-wide, 4μm-thick).

In an electrostatic drive test, stable deflections (Fig.6) of the micromirror have been observed up to the threshold deflection (Fig.7) of 26.5μm at a DC voltage of 330V. In a dynamic test, resonant frequency of the suspended micromirror has been measured as 590Hz. For a 10V-amplitude AC drive, resonant switching-frequency of the suspended micromirror has been tuned in the ranges of 580-450Hz (Fig.8) through the control of the DC bias voltage within 50-300V.

The present micromirror is applicable to tunable microswitching devices, including microinterferometers, optical microswitches, optical microshutters, laser-beam choppers, optical filters and couplers.

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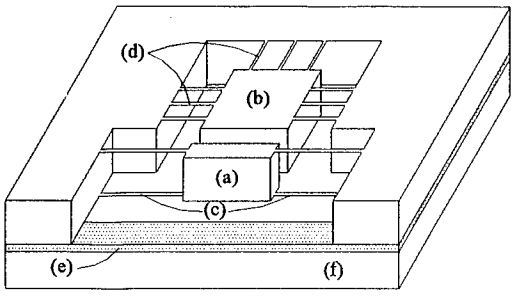


Fig.1 Perspective view of the silicon micromirror: (a) micromirror; (b) counter electrode; (c) microflexures; (d) dummy supporting beams; (e) bonding/insulating layer; (f) silicon base.

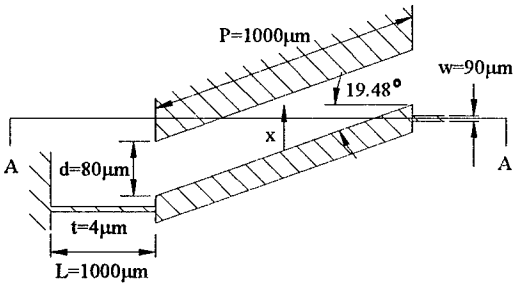


Fig.2 Top view of the silicon micromirror.

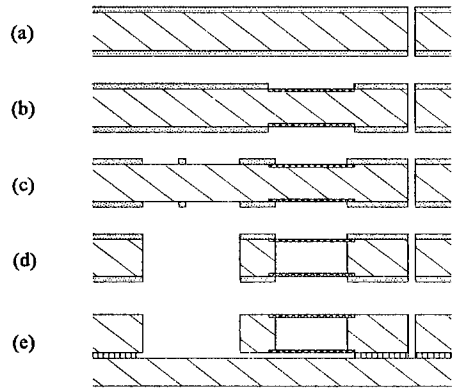


Fig.3 Microfabricated process of the silicon micromirror: A cross-sectional view along A-A of Fig.2.

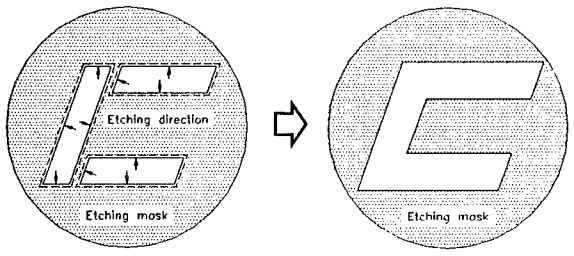


Fig.4 Corner compensation technique based on anisotropic silicon etch-rates.

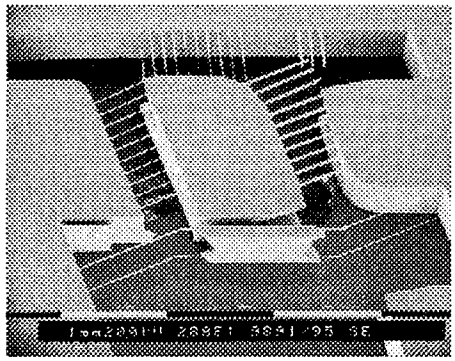


Fig.5 SEM of the fabricated silicon micromirror.

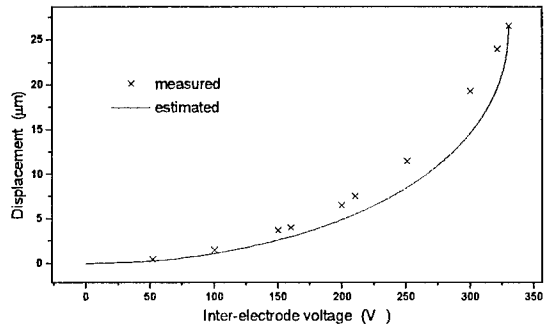


Fig.6 Measured and estimated displacement of the micromirror due to DC inter-electrode voltage.

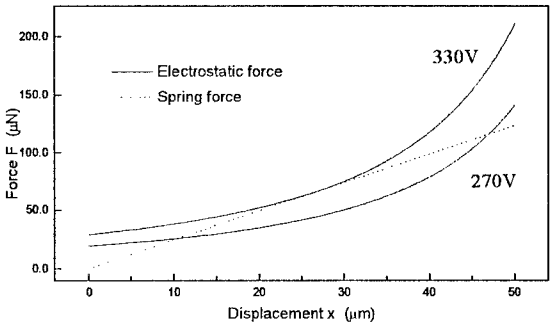


Fig.7 Electrostatic force and spring force.

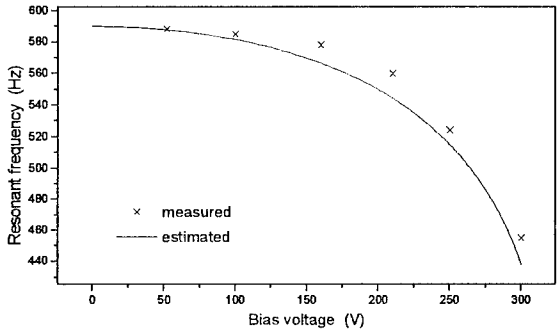


Fig.8 Resonant switching frequencies of the micromirror tuned by DC bias voltages for a 10V-amplitude AC drive-voltage.

1:30pm - 2:00pm (Invited)
ThC1

Widely-Tunable Micro-Mechanical Vertical Cavity Lasers and Detectors

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Abstract: Recent progress on micromechanically tuned vertical cavity lasers surface emitting lasers (VCSEL) and resonant cavity detectors will be reviewed. Results of large continuous tuning range, low threshold and high power VCSEL and novel self-tracking tunable detectors will be discussed.

Continuously tunable lasers and detectors are desirable for a variety of applications in wavelength division multiplexing (WDM) communications, remote sensing and scientific instrumentation. We have recently demonstrated a new family of widely-tunable VCSELs and detectors with high performance using micromechanically tunable vertical cavity structures. These devices take advantage of the vertical cavity structure having an ultrashort cavity, which results in a very large Fabry-Perot (FP) mode spacing, which thus help to determine the lasing or detector wavelength. By varying the cavity length, the laser or detector wavelength can thus be easily varied

The principle of our tunable VCSEL and resonant cavity detector (RCD) is based on making one of the mirrors movable. This can be done by making a large part of the top distributed Bragg reflector (DBR) on a cantilever freely suspended over the rest of the structure, which includes a small remainder of the top DBR, the active region and the bottom DBR (Fig. 1). The FP wavelength can thus be continuously varied by applying a voltage across the cantilever, between the top and middle contacts, to move the top DBR towards the substrate with electrostatic attractive force. The VCSEL drive current is applied separately between the middle and bottom contact, and similarly, the detector current is collected.

Using oxide confined structure to provide both current and optical confinements, we recently demonstrated tunable VCSELs with tuning range as high as 19.1 nm under room temperature CW operation [1]. To the best of our knowledge, this represents the widest tuning range for any monolithic tunable semiconductor laser. Fig. 2 (a) and (b) show the tuning spectra and LI curves for a device oxidized to have an aperture of 10 μm. The device continuously tunes over 19.1 nm as the tuning voltage is changed from 0 to 14.4 V with < 0.5 μA tuning current. At 14.4 V, the wavelength of the emitted light has completely wrapped around to the original wavelength at 0 V. A single step wavelength discontinuity is seen ~955 nm due to our design not being optimized in layer thickness, resulting a FP wavelength at 0V being near the center of the free-spectra range. However, the tuning is truly continuous as can be seen from the complete coverage of the free spectra range. The threshold current is less than 5.4 mA over 18 nm of tuning

The spectra and LI curves for a device oxidized to an aperture of 5 μm diameter are shown in Figure 3. This device has a threshold of 460 μA and a tuning range of 9 nm. The device lases in a single transverse mode and the side mode suppression ratio for this device is greater than 20 dB over the entire tuning range. Peak output power is 0.9 mW. Both the threshold and the output power are the best for a micromechanically tunable VCSEL.

Wavelength tunable detectors are highly desirable for allowing reconfigurability in a WDM system. Further, it eliminates the need of a cumbersome wavelength demultiplexer. Recently we reported the first tunable detector that can track incoming signal and has a wavelength registration capability [2]. We achieved a 30 nm continuous tuning for this resonant cavity detector with 7 V tuning voltage. By simply connecting a feedback load to the tuning electrode, it can track the incoming wavelength over 25 nm.

The tracking mechanism works in the following way. As the incoming wavelength red shifts, the detector current reduces, the voltage drop across the feedback load is reduced, causing the voltage across the cantilever to increase, which shifts the FP resonance to a longer wavelength, tracking the red shift. On the other hand, as the incoming wavelength blue shifts, the detector current increases, the voltage across the feedback increases, causing the cantilever voltage to

reduce, which shifts the FP to a shorter wavelength, tracking the blue shift. The detector remains narrow band during tracking.

To summarize, the advantages of micromechanical vertical cavity devices are numerous including a wide continuous tuning range, 2D array fabrication, wavelength tracking capability, and compatibility with multimode fibers. Furthermore, the entire structure is epitaxially grown so that all the essential parameters can be designed, e.g. tuning range, detectivity, passband shape and width, extinction ratio.

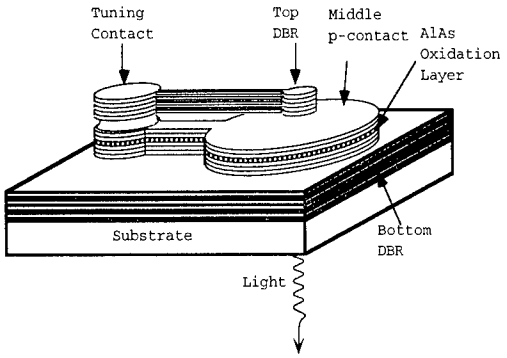


Fig. 1 Schematic of tunable VCSEL

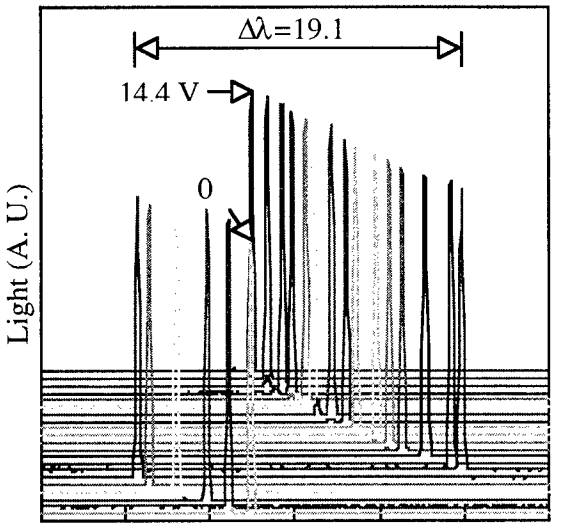


Fig. 2a Spectra of a micromechanical tunable VCSEL with 12 μm aperture and 19 nm continuous tuning.

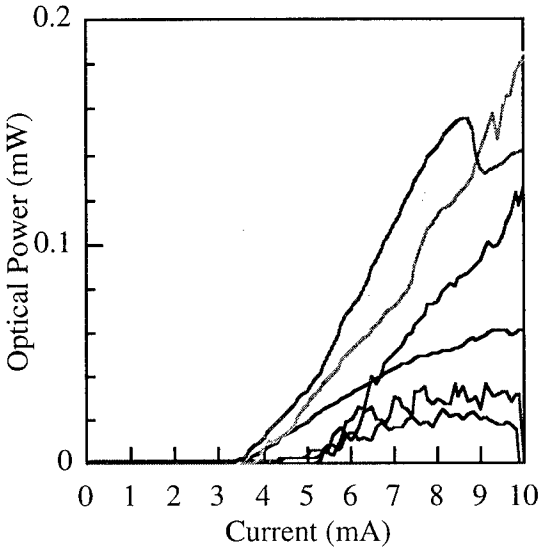


Fig. 2b LI curves for the tunable VCSEL.

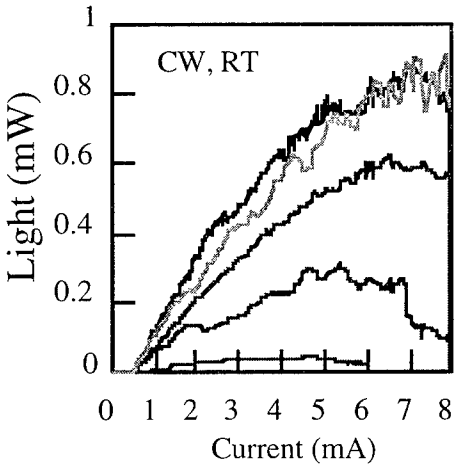


Fig. 3 LI for a 5 μm aperture tunable VCSEL

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2:00pm - 2:30pm (Invited)
ThC2

Indium Phosphide Based Micro Optoelectro Mechanics

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In micro optoelectronical applications like lasers, photodiodes or phototransistors, III-V direct band-gap compounds are predominant. This should also be the case if micromechanics are integrated with active optoelectronic structures. Alredy much encourageing work has been made in GaAs based micro optoelectro mechanical systems (MOEMS)[1-3]. We propose that indium phosphide (InP) based surface micromachined micromechanics could also provide cost effective MOEMS, and for longer wavelengths. Application could be gas sensors, and in Fibre-to-the-House wavelength division multiplexing (WDM) 1.55 μm telecommunication systems.

A compairison is made with the state of the art concepts in optical MEMS, today provided by silicon and GaAs based technologies. Most of these are Fabry-Perot or Mach-Zender configurated structures, which are perfectly suitable also to InP based MOEMS. Among the III-V based structures many metal-dielectric surface micromachined mechanical structures have been proposed[4]. In low cost butt coupled fibre applications, these structures should have a lower sensitivity and higher cross-talk than in semiconductor based optical MEMS, due to the longer coupling distance to the fibre, or a high absoption in the structure when front side coupled.

With the technology already developed for InP based lasers, most the surface micromachined concepts above are also possible to be made in InP based semiconductor structures. In our collaborating groups we have experience in III-V micromechanics, mechanical modelling and characterisation of microstructures, VCSEL technology (including epitaxial regrowth, III-V wafer fusion bonding, Bragg mirror fabriction in both Si-SiO_2, and semiconductor heterostructures, and deep vertical reactive ion etching (RIE)), as well as III-V sacrificial layer surface micromachining[5-10]. Some micrographs of III-V micromachined structures are shown in Figs. 1 to 3. Surface micromachining issues like sacrificial etching of single crystalline material, and anti-sticking treatments will also be presented together with InP based surface micromachined demonstrator structures. From our results, we are confident that InP based MOEMS are able to provide low cost alternatives in long wavelength optical applications.

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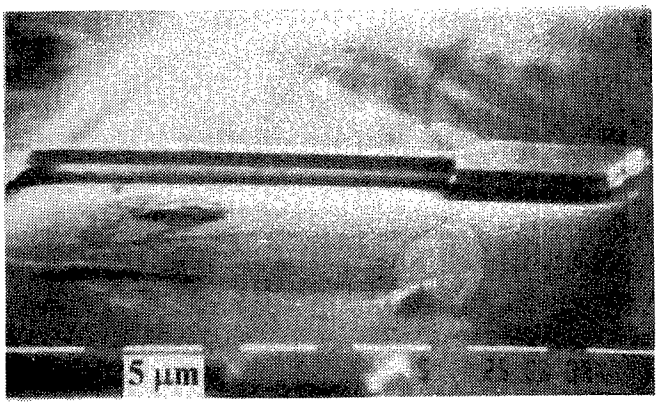


Figure 1. A paddle shaped structure of $In_{0.53}Ga_{0.47}As$ where $In_{0.53}Al_{0.47}As$ has been used as a sacrificial layer, stripped by $HCl:H_2O$ (3:1).

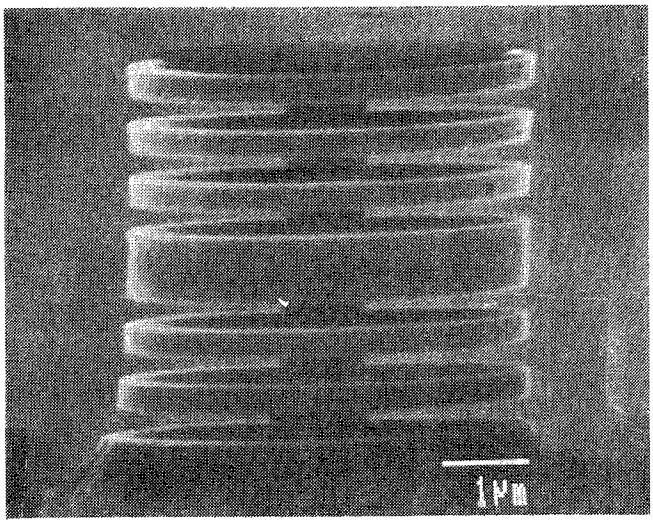


Figure 2. A multilayer demonstrator with InP layers alternated by $In_{0.53}Ga_{0.47}As$ sacrificial layers.

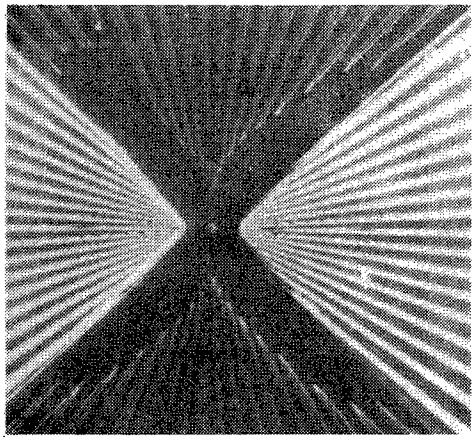


Figure 3. The anisotropy of the HCl underetching in InP. A wagon-weel structure is etched, having nitride masking sections of 2.5° and 2.5° openings inbetween. The closer to the center, the thinner is each section, and the quicker it is etched away. The etched away length of each section gives a figure of the underetching perpendicular to it.

Microoptical applications of porous silicon superlattices

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Porous silicon (PS) layers can easily be formed by an electrochemical etch process using a mixture of hydrofluoric acid (HF) and ethanol [1,2]. The properties of the microstructure and the porosity of the layers depend on the HF concentration, the doping level of the substrate and the current density applied during the etch process [3]. Changing the current density during the etch process can be used to form a well defined layer structure consisting of layers with different porosities. Each single layer can be treated as an effective medium [4] with a refractive index depending mainly on the porosity of the layer. Using reflectance measurements we have investigated the dependence of the refractive index of PS layers on the formation current density for different substrates. Based on these results various kinds of optical interference filters were fabricated. We have formed samples consisting of discrete single layers with different porosities as well as samples with continuous variations of the refractive index (rugate filters [5]). Using this technique the fabrication of anti-reflectance coatings with low reflectance over a wide range of wavenumbers becomes possible.

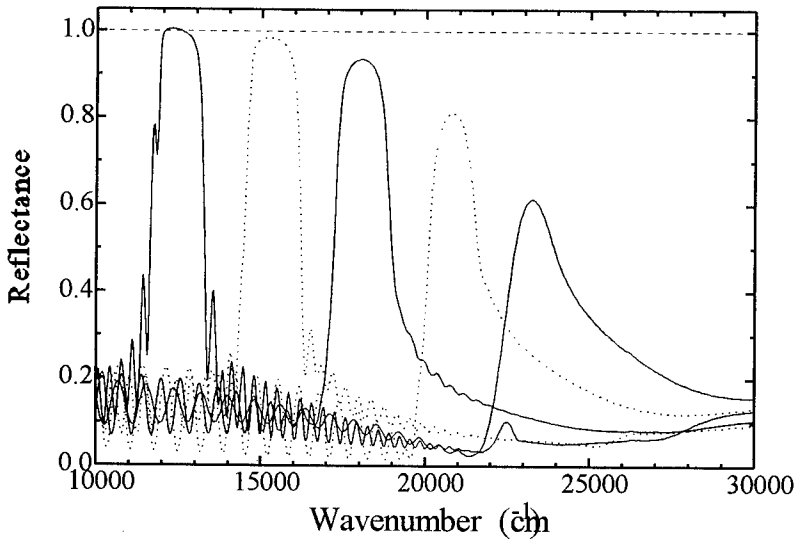


Fig. 1: *Reflectance spectra of Bragg reflectors in the visible made of PS. By changing the optical thicknesses of the quarter wave layers the reflectance maximum can be shifted over a wide spectral range of wavenumbers.*

In Fig. 1 the reflectance spectra of Bragg reflectors for different wavelengths in the visible spectral range is shown. These filters consist of alternating layers with high and low porosities corresponding to low and high refractive index layers respectively. Each

of the single layers in the multilayer structure has an optical thickness of a quarter of the design wavelength.

The formation process for porous silicon superlattices is compatible with standard silicon microelectronics and can therefore be integrated in a silicon process line. In addition the lateral size of the silicon superlattice can easily be scaled down to areas of only a few micrometers using standard photolithography steps. This allows the fabrication of conventional silicon photodiodes which gain a color sensitivity due to a porous silicon superlattice placed above the p/n junction. In Fig. 2 we present the spectral response of photodetectors with different Bragg filters on top. These detectors can be integrated in an array of detectors sensitive to different wavelengths.

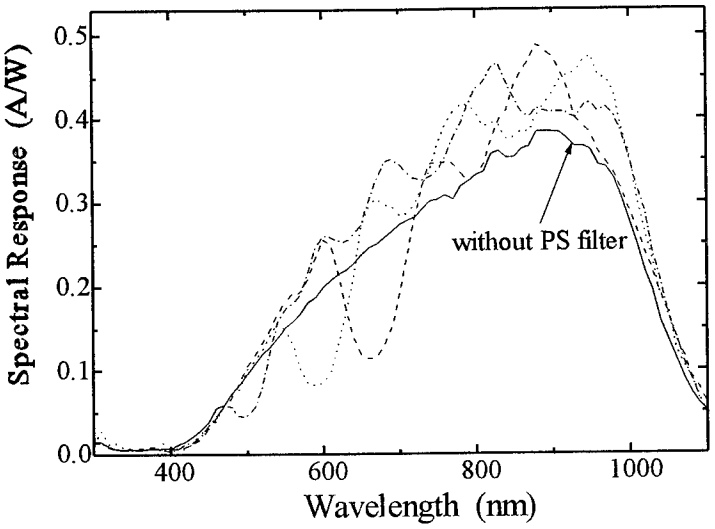


***Fig.2**: Spectral response of a photodetector with a porous silicon filter on top. For comparison a photodetctor with bulk silicon is given.*

Furthermore we have fabricated waveguides out of porous silicon. Waveguiding was shown for several different structures.

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3:30pm - 3:45pm
ThD1

Ultra Sensitive Displacement Detection of Micromechanical Structures

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School of Electrical Engineering
Cornell University
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Recent advances in Micro-Electro-Mechanics have led to the development of many types of microsensors and microactuators. These devices have a typical range of motion from submicrometers to a few micrometers. Compare with macroscopic sensors and actuators, these micromachined devices are light weight, compact and can possess a higher frequency response. Until now, the most common method of visually observing the motion of these micromechanical devices have been using a Scanning Electron Microscope (SEM). There is an increasing need for a simple yet sensitive technique for detecting very fine motions of these devices. In this paper, we propose an optical detection scheme based on Moiré effect to achieve high resolution. Using a simple image processing technique, a resolution of 50 nm has been achieved.

The moiré effect is a well known phenomenon, first investigated by Lord Rayleigh in 1874. When two gratings are superimposed, a series of dark and bright fringes are produced. These fringes, called Moiré fringes, are produced due to the intensity variation of transmitted light. For two identical gratings of pitch p, at an angle θ with respect to each other, the Moiré fringe pitch G is given by

$$G=\frac{p}{2\sin\frac{\theta}{2}} \qquad (1)$$

When one grating is displaced by δp in the direction normal to the grating, the Moiré fringe is shifted by $\delta G=\delta p/2\sin(\theta/2)$. For a small θ, the displacement is magnified by a factor of $1/\theta$. This enables us to detect motion which otherwise is too small to observe with conventional microscope. Moiré effect can also be used to detect rotation or deformation of one grating with respect to the other. From Eq. (1), any change in rotation angle θ, or grating pitch p will produce a change in Moiré fringe pitch G. This decoupling of signals into a phase and frequency components make Moiré pattern a very useful tool in motion detection. Figure 1 shows a typical Moiré pattern produced when two gratings of equal pitch are oriented with an angle θ.

Figure 2 shows a micromechanical sensor designed for x motion detection. The device has a grating of 4 μm pitch supported by cantilever beams which are connected to a pair of comb drive actuators. The grating is magnified 200 times and detected by a CCD camera with a second grating superimposed. Figure 3(a) and (b) shows the Moiré patterns of a micromechanical device that have been moved by 2 μm or half a grating period. Correspondingly, the Moiré fringes have shifted by half a Moiré period.

In conclusion, we have proposed and demonstrated a fine motion detection scheme using Moiré effect. This technique is simple, very sensitive and should have a large signal to noise ratio.

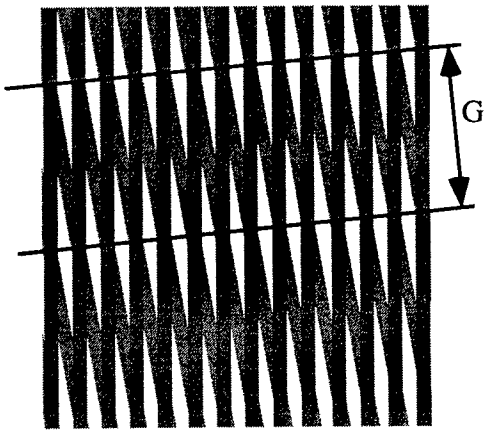


Figure 1: Moiré fringes are formed by two gratings with an angle θ.

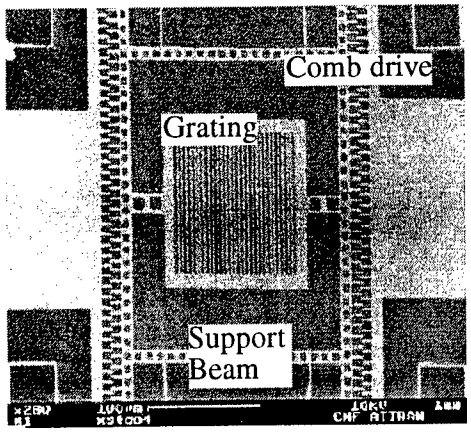


Figure 2: Scanning Electron Micrograph (SEM) of grating with linear actuator for fine motion detection.

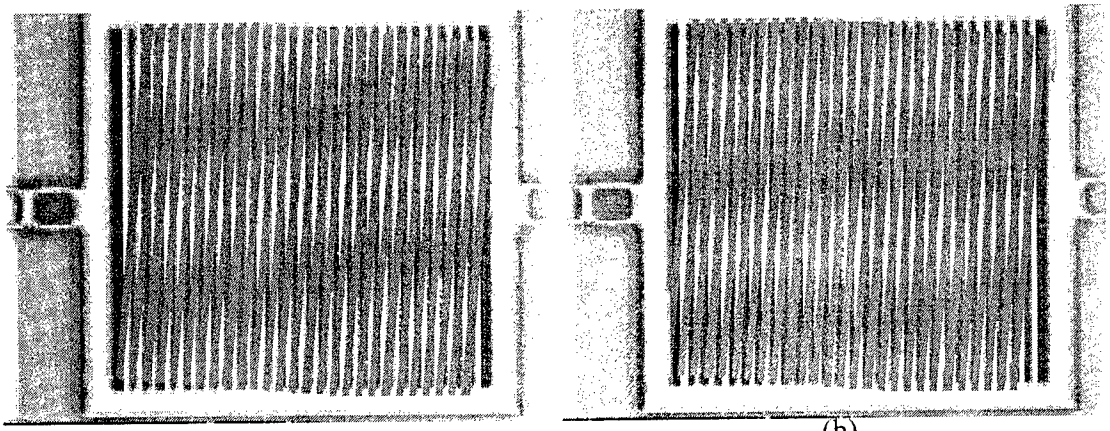


Figure 3: The Moiré patterns of (a) and (b) are 180 degrees out of phase, corresponding to a displacement of half a grating pitch.

Compound-Cavity Micro-Interferometer using VCSEL and Piezoelectric Actuator

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Hiroshi MIYAJIMA, Shinobu SHINOHARA and Kazuhisa YANAGISAWA

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A novel compound-cavity interferometer which measures displacement without ambiguity is studied. A vertical-cavity surface-emitting laser (VCSEL) has several advantages in comparison with a conventional edge-emitting laser for sensing use.[1] Authors have proposed an optical sensor using a VCSEL and it has realized very small size without optical parts such as a collimator lens.[2] The new sensor we proposed in this paper is based on a combination of a micro optical interferometer using a VCSEL and a piezoelectric actuator. In this study, two signal waves which have $\pi/2$ radian phase difference are obtained in order to enable detection of the displacement direction.

Figure 1 is a conceptual scheme of a micro displacement sensor. As a VCSEL and an external mirror consist an optical compound-cavity, the output power of the VCSEL is strongly modulated with a $\lambda/2$ period (λ; optical wavelength) in the displacement of the mirror. A photodetector (PD) detects a back side emission of the VCSEL. The VCSEL/PD unit is arranged on a piezoelectric actuator which is fabricated on a substrate. The actuator is driven by a pulsed voltage and changes its thickness T from T_o to $T_o+\lambda/8$ periodically. Therefore, the VCSEL/PD module is moved vertically and an external cavity length L is modulated from L_o to $L_o-\lambda/8$.

Figure 2 shows a timing chart of displacement sensing. A principle to obtain two phase shifted signals will be explained with this chart. The actuator is driven with a constant frequency in order to modulate the external cavity length. Accordingly, the VCSEL output which is detected by the PD is changed from initial waves phase A to $\pi/2$ radian shifted waves phase B alternatively with the constant period. Finally, the PD output is sampled synchronously for the phase A and the phase B signals.

Figure 3 is an experimental setup for displacement sensing. A VCSEL (λ=980nm) and a PD is integrated in one chip with hybrid technology as shown in Fig. 4. The size of the VCSEL/PD module is 1.8mm x 1.4mm x t0.6mm. The module is mounted on a piezoelectric bimorph actuator which size is 6mm x 18mm x t0.5mm. The actuator is driven with a pulse signal of a peak voltage V_p=3.8V and a frequency f_p=1kHz. The VCSEL is operated with a constant current of I_f=12mA and a VCSEL output is measured by the PD and recorded into a memory. An external cavity length L is about 0.4mm and the external mirror is moved vertically with a velocity v=40μm/sec.

The PD output signal waves are shown in Fig. 5 and Fig. 6. In Fig. 5, the piezoelectric actuator is not driven and simple sinusoidal waves is obtained. On the other hand, Fig. 6 shows higher frequency waves which is induced by the modulation of the external cavity length. Figure 7 represents a pair of phase shifted signals processed from the signal shown in Fig. 6. Two sinusoidal signals having a phase difference of approximately $\pi/2$ radian are obtained. Figure 8 is an example of a Lissajous' figure for the phase A and the phase B signals with a parameter of time transient.

In conclusion, we have demonstrated a novel micro optical interferometer which can measure displacement without ambiguity. The experimental results show good performance to detect a displacement direction. Further integration of a VCSEL, a PD and an actuator will be possible with a combination of improved III-V technology and MEMS technology.

References

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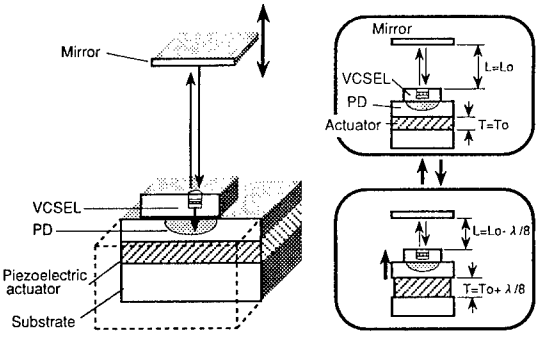


Figure 1. Conceptual scheme of micro-displacement sensor (cross section)

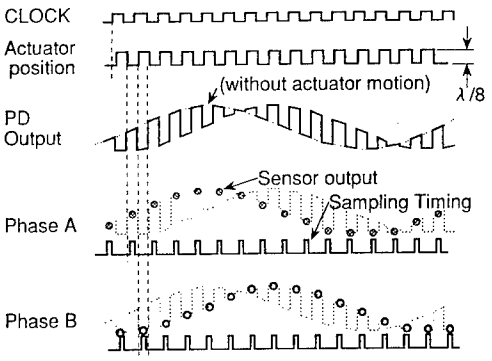


Figure 2. Timing chart

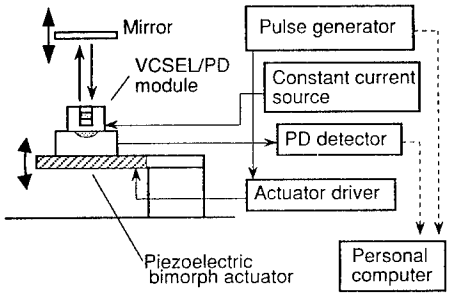


Figure 3. Experimental setup

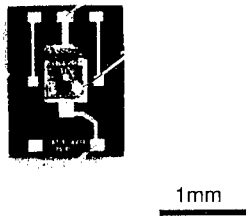


Figure 4. VCSEL/PD module (top view)

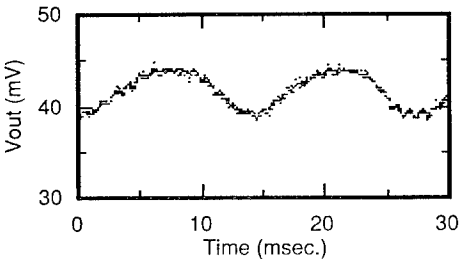


Figure 5. PD output (without actuating)

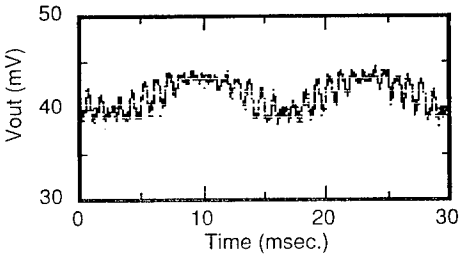


Figure 6. PD output (with actuating)

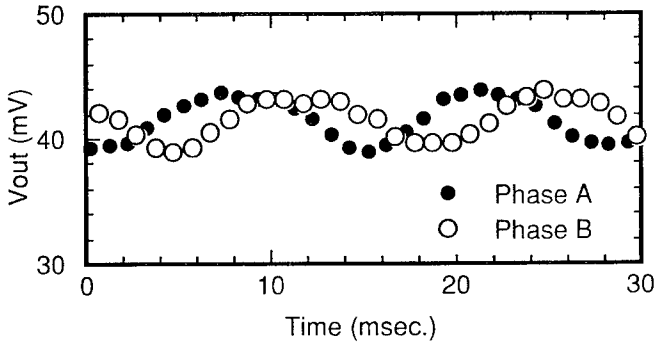


Figure 7. Output of the micro-displacement sensor

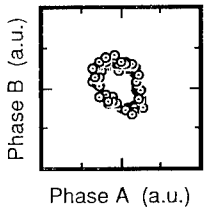


Figure 8. Lissajous' figure

4:00pm - 4:30pm (Invited)
ThD3

A virtual prototype manufacturing software system for MEMS

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IntelliSense reports on a new computer-aided design software system for rapid prototype development of microelectromechanical systems. This system, called IntelliCAD™, is self-contained, easy-to-use and has an open architecture. IntelliCAD's integration is accomplished by an architecture different from a previously reported academic system [1]. The new architecture integrates mask layout, a material database, a fabrication database, process simulation, forward and backward search at each fabrication step, process debugging, solid modeling, and parametric electrostatic, thermomechanical and electromechanical analysis into one efficient and user friendly system. The novelty of our approach is in linking the performance modeling to the manufacturing (machine) parameters and allowing modifications for user applications.

IntelliCAD uses a process sequence builder developed to capture at a high level the process steps that go into building a device. Detailed process parameter information is transferred automatically from IntelliCAD's fabrication database to the process builder. An expert system process checker has been developed and integrated into IntelliCAD. The process checker debugs processes to ensure completeness and continuity. IntelliCAD has a new solid modeling engine tailored for MEMS. IntelliCAD's solid modeler is capable of conformal deposition, etching and three-dimensional animation and display of the geometry built at any given fabrication step (from the detailed process information and layout). The solid modeler supports a layout editor developed for IntelliCAD. The new layout editor converts and reads files in GDS-II and CIF formats. For discretization purposes, an automatic meshing algorithm has been developed and integrated into the solid modeler. The discretized geometries are transferred automatically to IntelliCAD's performance simulator for mechanical, electrostatic and electromechanical analysis.

At any process step, users can investigate the process parameter variation on the film thicknesses or the impact of such variations on the thin-film material behavior through the material deposition module (MEMaterial®) developed by IntelliSense. Process simulation is accomplished by user-defined models and other simulators for the microfabrication processes (such as SUPREM®III and empirical models). Performance simulation is performed by an electrostatic analysis module, a non-linear finite element module and a coupling module for combined electromechanical analysis. Improved methodologies have been implemented in the electrostatic analysis module. Due to space limits, the detailed features of IntelliCAD will be presented in the paper.

The use of IntelliCAD will be shown by an example. We will use the process builder to input the surface micromachining process sequence of a polysilicon-based comb drive developed at BSAC. A commonly used folded tether comb drive mask layout similar to that of Tang was selected as the geometry to be investigated. The structure was simplified to reduce computational redundancies without loss of generalities. The process sequence is input in the process builder, geometries are captured in the solid modeler, material parameters are determined automatically from the material database and coupled electromechanical analysis is performed. We will show: (1) the results of charge density distribution (which specifies pressure loads for mechanical deformation) will be shown, (2) the deformed comb drive structure under electrostatic loads, (3) the deformation of the comb drive tip versus polysilicon deposition time, and (4) the tip displacement of a comb finger as a function of applied voltage.

4:30pm - 5:00pm (Invited)
ThD4

Exploring Design Spaces for Optical MEMS Devices

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ABSTRACT

The MEMCAD system enables the designer of Optical Micro-Electro-Mechanical Systems to explore interesting design spaces in simulation. In this paper we investigate the space of torsional micromirrors and explore three specific micromirror designs.

INTRODUCTION

In any area of MEMS an engineer will have a target device to develop, and will want to explore all its possible designs, we refer to this as the "design space" of the device. The MEMCAD system allows a MEMS designer to explore much of their chosen design space in simulation. This paper uses as an example the design space of torsional micromirrors, a device of particular interest to Optical Micro-Electro-Mechanical Systems (OMEMS) designers. We consider three variants of the torsional micro-mirror, to illustrate the exploration of that space by simulation.

MEMCAD

MEMCAD has four logical components: Device Design, Model Construction, Domain Solvers, and Simulation Management. Device Design consists of editing or retrieving layout, process and material property information. Model Construction automatically constructs 3D solid models from the information specified in device design, and gives the user a suite of tools for meshing and assembling detailed 3D models of their devices. Domain Solvers is a full suite of simulation tools for different physical domains, including elastic mechanics, electrostatics, and coupled electromechanics[1]. Simulation Management gives the MEMS engineer the ability to ask questions about the dependence of device behavior on any of a large set of variables, including process variables, material parameters, and design variables such as critical dimensions of the device. MEMCAD Integrates these tools together so the designer can easily and rapidly develop models and simulate them to understand their behavior, and the behavior of near variants of each design.

TORSION MIRROR I

The first torsion mirror is shown in Figure 1. The mirror plate and its supports is formed in a single material layer, and is fixed at the ends of either arm, and able to twist about them. There are two electrodes below the mirror, and a ground plane below everything. A voltage is placed on one electrode (the forward one) and all other conductors are held at 0V. The mirror plate is 20μm x 20μm.

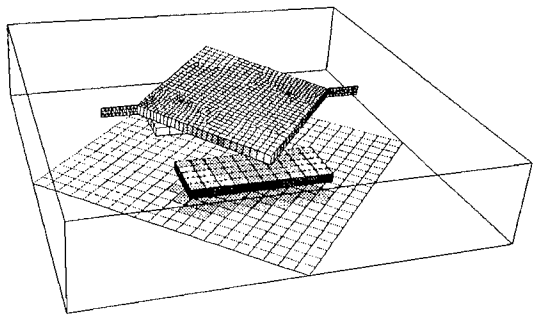


Figure 1 Torsion Mirror I, at 4.0 V. Mirror tip displacement is 0.65 μm, corresponding to a tilt angle of 1.3°. The figure is scaled by 5x in Z for visualization.

TORSION MIRROR II

The second torsion mirror is shown in Figure 2, again it is fabricated from a single layer for mirror and support. The mirror plate is fixed at the ends of either arm, and able to twist about them. The reflecting surface of the mirror is in two lobes on either side of the supports. There are two electrodes below the mirror, and a ground plane below everything. A voltage is placed on one electrode (the forward one) and all other conductors are held at 0V.

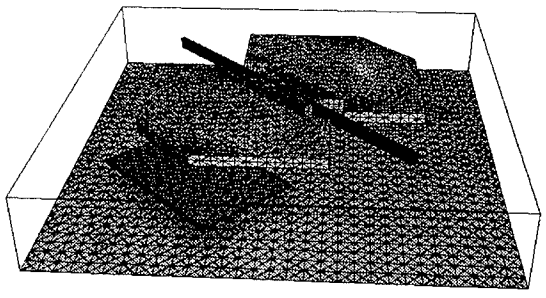


Figure 2 Torsion Mirror II. The mirror is suspended at the ends of its narrow tethers. The figure is scaled by 2x in Z for visualization

TORSION MIRROR III

The third torsion mirror is shown in Figure 3. This micromirror is an example of a two-phase zipping actuator [2]. The mirror plate is fixed at the ends of either arm, and able to twist about them. In this case the mirror is formed of two different layers of aluminum, a mirror plate of 3 μm thick having tethers and a neck region that are 0.5μm thick. There are two electrodes below the mirror. A voltage is placed on one electrode (the starter) to initiate contact. Then the driving voltage is placed on the driver electrode, causing the neck of the mirror plate to zip in and tilt the mirror. This mirror has stable control of its tilt angle over its operating range of 1.5-10 degrees.

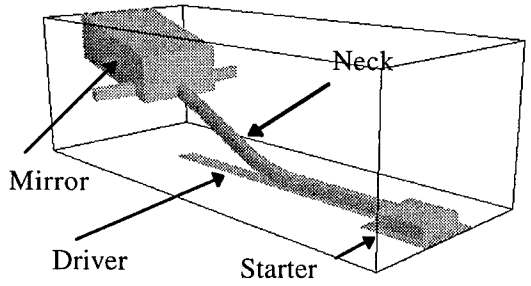


Figure 3 Torsion Mirror III at drive voltage V_D=20V. The drive is zipping in the neck of the mirror plate, causing the mirror to tilt. At 20V the mirror has tilted to angle 3.5 degrees.

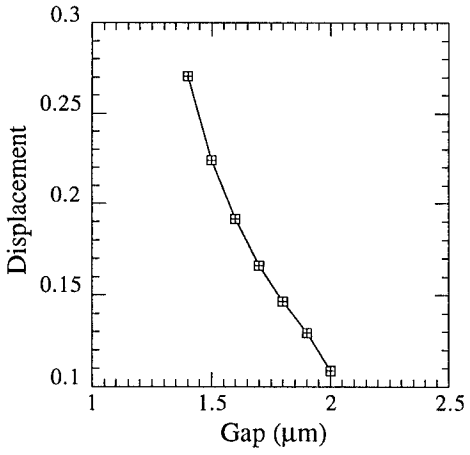


Figure 4 Graph of displacement vs. gap for Torsion Mirror I, at 2.0V. The gap between the mirror and its driving electrodes is varied from 1.4 to 2.0 μm. This curve is used to understand the relationship between a process parameter (gap thickness) and a device behavior (deflection at 2.0V).

MIRROR BEHAVIOR ANALYSIS

Having constructed these device models in MEMCAD, we would like to analyze their behaviors. Examples of such analyses are presented in Figure 4 and Figure 5. Figure 4 shows the relationship between the gap thickness and the deflection of the mirror tip at 2.0V for Torsion Mirror I. Figure 5 shows the angular deflection vs. applied voltage for Torsion Mirror III.

CONCLUSION

MEMCAD can be used to explore design spaces for MEMS and Optical MEMS devices. Such design spaces include alternative structures (I vs. II. vs. III), variations in process or design parameters (see Figure 4) and variations in operational parameters (see Figure 5). The MEMS engineer can now make considerable progress in design by using simulation before fabrication.

Microcosm Technologies' MEMCAD 3.0 became available in the 2nd quarter of 1996, and has been installed at several industrial sites.

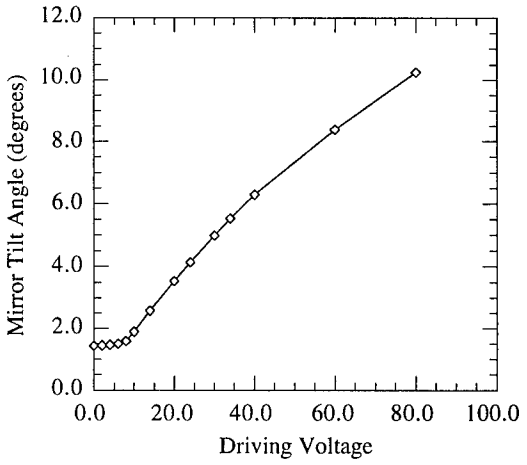


Figure 5 The mirror tilt angle vs. the driving voltage V_D. We obtain near linear control of tilt angle over most of the Torsion Mirror III's operating range of 1.4-10.3 degrees.

ACKNOWLEDGMENTS

We would like to acknowledge the contributions of Steve Senturia and the MEMCAD group at MIT for years of research and inspiration before the construction of Microcosm MEMCAD.

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Friday, August 9, 1996

SESSIONS:

FA: Communications/Switching

FB: Waveguide Devices and Processing

Mechanical Anti-Reflection Switch (MARS) Device for Fiber-in-the-Loop Applications

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Wavelength Division Multiplexed Passive Optical Network Systems (WDM-PONS) are being explored as a means to cost-effectively implement fiber-to-the-home in order to increase the bandwidth of the telecommunications network. One type of WDM-PONS being explored utilizes an optical modulator rather than an active source (laser or LED) at the subscriber node to provide upstream data transmission [1]. In such a system, the same light which is transmitted downstream from the central office (CO) to the Optical Network Unit (ONU) at the home, is then overmodulated and "looped-back" upstream to the central office. These systems have the cost advantage of sharing the high-performance CO components over many users. Since the receivers and modulators located at the ONU are not shared among users however, the cost of these components becomes an extremely significant issue. For initial deployment, lower cost, moderate performance ONU components can be installed with potential upgrades later at any user's request. These low cost components must still provide moderate data rates (>1 Mbit/sec.), have wide spectral width in order to allow many wavelength channels, thermal stability, and good optical contrast (>10 dB). Achieving these performance levels at low cost is a difficult problem, however the device we are describing here has been shown to satisfy these requirements.

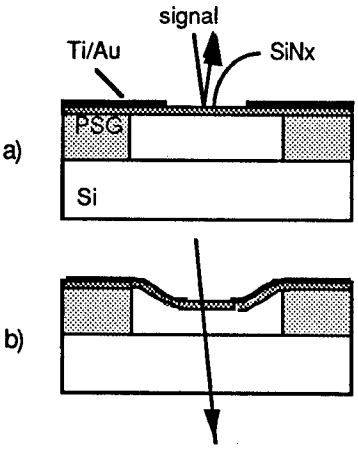


Figure 1: MARS modulation.

The Mechanical Anti-Reflection Switch (MARS) device is an optical modulator based on the principle of a vertically moving anti-reflection film suspended above a silicon substrate [2]. The operating principle and device structure are shown in Fig. 1. A $\lambda_o/4$-thick film of silicon nitride is suspended above a silicon substrate with a $3\lambda_o/4$-thick air gap (λ_o being the center wavelength of the desired operating spectrum). In this configuration, the nitride/air/substrate film structure provides a high reflection (>70%) condition for the desired wavelength λ_o. When a voltage is applied between a gold electrode on top of the nitride and the silicon substrate, the film is electrostatically attracted toward the substrate, reducing the air gap thickness. When the air gap becomes $\lambda_o/2$, a low reflection condition (< 1%) is achieved. Contrast ratios of up to 24 dB have been measured on these devices. The operating principles of the MARS device are discussed more thoroughly in Reference 2, and the fabrication is discussed in Reference 3.

A typical device geometry is shown in Fig. 2. The MARS consists of a central plate suspended above the substrate via support beams, comprising the mechanically active area of the device. An optical window is defined by the absence of electrode material in the center of the plate area. Modulators with central plates ranging from 10 μm x 10 μm to 100 μm x 100 μm, support beams ranging from 4 μm wide to 21 μm wide, and 5 μm long to 100 μm long have been fabricated and tested.

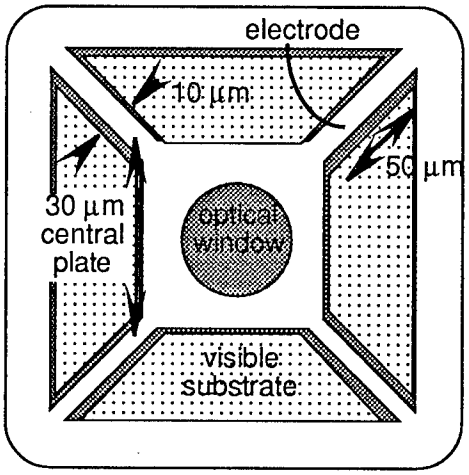


Figure 2: Top view of a MARS design.

Figure 3 shows the optical response of a typical MARS device to a square wave drive signal. This particular modulator exhibited rise and fall times of 132 and 125 ns respectively. As seen in Fig. 3, the response includes mechanical ringing at a characteristic resonant frequency of roughly 3.5 MHz. With proper device design, this ringing can be reduced and modeling predicts that usable data rates can be achieved at three times the resonant frequency of a device, or for this particular modulator,

roughly 10.5 Mbit/sec. In practice however, we have yet to demonstrate system operation at such high data rates. System experiments have been run to determine bit-error-rates for fully packaged devices under normal operating conditions. Figure 4 shows the response of such a modulator to a pseudo random bit stream of 2^{15}-1 word length at 3.5 Mbit/sec. As shown in Fig. 4, the modulator can achieve this data rate with error rates of less than 10^{-8} with less than 2 dB power penalty from the system base band. This penalty arises mainly from pattern dependent inter-symbol interference.

The final cost of a packaged MARS modulator will be dominated by the expense incurred in packaging the device. It is in this area that the MARS modulator has some distinct advantages. Due to the large size of the optical window region (20-30 μm), inherent polarization insensitivity, and uncomplicated fabrication, multi-mode packaging techniques can be exploited to obtain single-mode fiber devices. Measurements show a wide alignment tolerance exists when coupling to a single mode optical fiber. This tolerance is large enough to enable passive packaging techniques, thereby eliminating the expensive active alignment process used for most photonic packages today.

CONCLUSION

We have demonstrated a micromechanical modulator with the capability of providing upstream data rates of 3.5 Mbit/sec with 10^{-8} BER in a fiber-to-the-home communications system. Due to several advantageous aspects of the MARS, packaging costs for the device should be quite low, resulting in an extremely inexpensive moderate data rate optical modulator.

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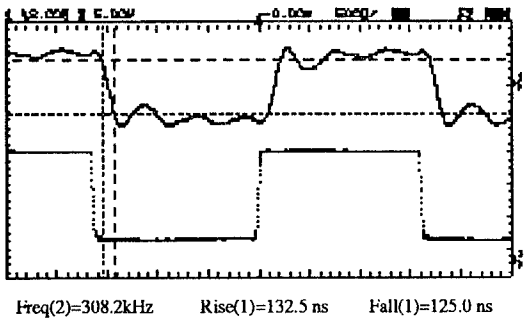


Figure 3: Typical optical response to a square wave drive signal. Drive voltage is roughly 50 V.

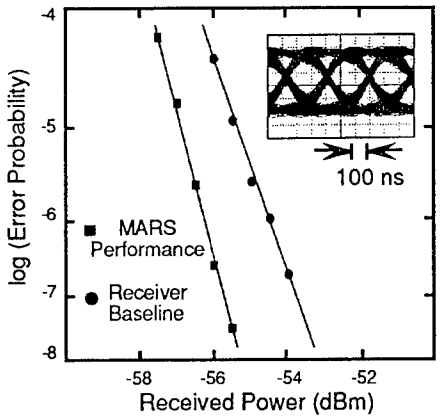


Figure 4: BER result and eye pattern for a fully packaged modulator.

Packaging of a reflective optical duplexer based on silicon micromechanics

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The deployment of optical fiber in communication access networks is under way, not only for business customers but also for residential. Unmatched transmission quality, demand adaptation capability, ease of protection, and access to the future information super highway are the main driving forces to introduce the fiber in the loop (FITL). Crucial for a rapid and large scale expansion of FITL is the price of the optical line termination. An alternative to the active transceiver comprising a light emitting device is the reflective duplexer [1,2]. Such a device modulates and reflects back a part of the light provided by the network. Cost attractive solutions based on the optical MEMS technology are promising for the realisation of a reflective modulator for moderate bitrates of a few Mbit/s [3,4].

Fig.1 illustrates the device architecture. The heart of the device is a surface micromachined reflective modulator based on the Fabry-Perot effect. Both semi-transparent mirrors of the Fabry-Perot resonator are made of polysilicon. The bottom mirror is directly deposited on the oxide-nitride substrate passivation. The top mirror is a free standing membrane obtained by selective etching of a sacrificial layer [4]. The geometry, the stress of the membrane, and the air gap define the frequency response of the modulator [5]. With a special design, a resonance frequency of 1.6 MHz with close to critical damping has been achieved. The cavity length of the resonator, which determines its reflectivity, is tuned electrostatically by applying a voltage between the polysilicon mirrors. Reflectivities above 90% with extinction ratios of up to 23 dB have been obtained [5]. Since silicon is transparent at 1300 nm, the reflective modulator can be illuminated by the fiber through the substrate. To minimise optical loss due to beam divergence, a hole is etched on the back of the substrate in order to bring the fiber closer to the modulator. In silicon, the divergence of a gaussian beam coming out of a single mode fiber is round 23.5 mrad. With a distance of 90 µm between the fiber end and the modulator, the calculated fiber to fiber loss due to the beam divergence is kept below 1 dB. In addition, an appropriate design of the hole allows a passive alignment of the fiber. The accuracy of the fiber positioning depends on the membrane geometry, and also on the modulator bandwidth: for MHz modulators typical tolerances of ±5 µm must be met, which is 2-3 times more

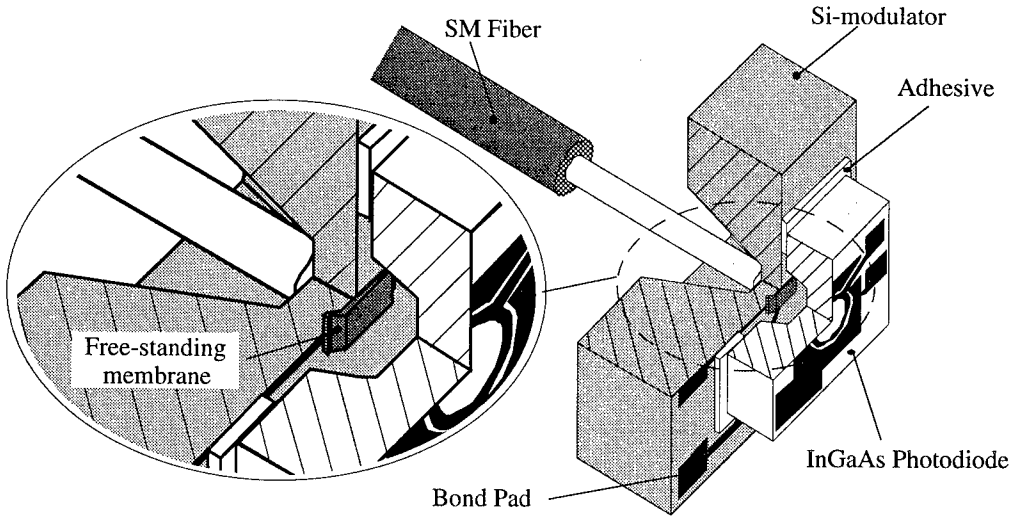


Fig.1: Schematic half cross-section of a reflective duplexer.

tolerant than with conventional optical waveguide components. Special care must be taken at the fiber-silicon interface. To prevent interferences on the back reflected optical signal, a high grade anti-reflection coating is necessary. Only 1% back reflection of the AR-coating can generate variations of the ON-state of more than 20% depending on the optical path length in the silicon substrate. In the same way, the extinction ratio can vary by up to 15 dB.

On the top side of the surface micromachined modulator, a back illuminated InGaAs photodiode with an etched access hole is attached, serving two functions: detection of the transmitted part of the light coming from the fiber, and protection of the free standing polysilicon membrane of the modulator. The active area of the photodiode has a diameter of 175 µm, and a capacitance of less than 2.5 pF including the electrodes, corresponding to a bandwidth of 1.2 GHz. Its responsivity is close to 1 A/W. The beam waist on the active area is less than 20 µm, resulting in a photodiode position tolerance of ±60 µm.

Fig.2 shows the characteristics of a fully packaged module. The minimum reflection occurs at 90 V with more than 70% of the incident light reaching the active area of the photodiode. The fiber to fiber loss is less than 2.5 dB, and the extinction ration reaches 13.8 dB. The eye diagram shows the good performance of the module up to 2.8 Mbit/s. The modulator has been directly driven, without equalisation, by a pseudo random pattern generator with a DC bias of 87.5 V and an AC amplitude of 4 $V_{peak\text{-}peak}$.

In conclusion, we have presented a fully packaged duplexer implementing a reflective Fabry-Perot modulator realised by silicon surface micromachining. The device demonstrates excellent performances for bitrates up to 2.8 Mbit/s. Relaxed positioning tolerances, a fiber to fiber loss below 3 dB, an extinction ratio better than 12 dB, and a potential for low cost fabrication make this device very attractive for use in economical optical links.

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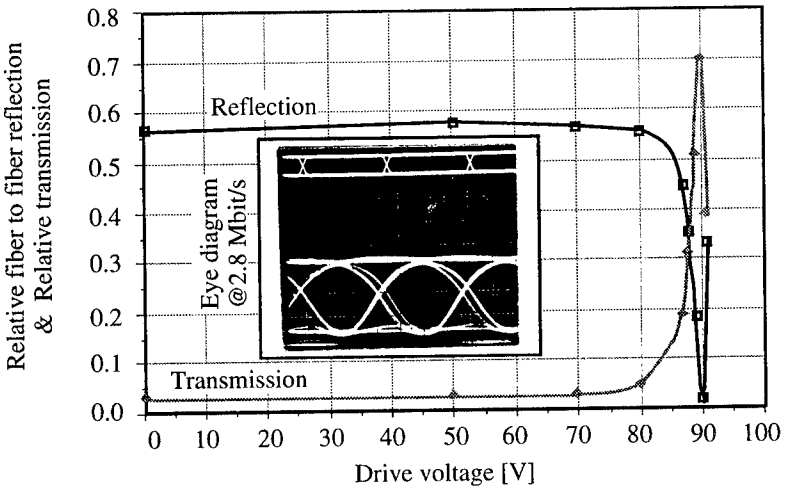


Fig 2: Relative back reflection coupled into the fiber and relative transmission detected by the photodiode versus voltage between both polysilicon layers. Eye diagram for a pseudo random pattern at 2.8 MBit/s with a bias of 87.5 V and a modulated signal of 4 $V_{peak\text{-}peak}$.

Optical Crossconnection by Silicon Micromachined Torsion Mirrors

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1. Introduction

Optical switches by means of mechanical movements have favorable characteristics such as wavelength independence, polarization independence, a large attenuation ratio, and small crosstalk. However, the conventional mechanical switches composed of fiber-connectors are not suitable for miniaturization, integration, or mass-production because of the fabrication process based on machining and assembling of workpieces. Micromachining is, therefore, expected to overcome the problems, and several micromachined optical switches have been proposed[1,2,3,4,5,6].

We developed a new type of free-space 2x2 optical switching matrix composed of micro torsion mirrors which were operated electrostatically. To suppress the loss of the light-beam traveling in a free-space, we used collimated-beam optical fibers for coupling. The present paper reports the operation and performance of the produced optical switching matrix.

2. Torsion Mirrors for Optical Switching

Figure 1 shows an SEM (Scanning Electron Microscope) view of the torsion mirror by silicon micromachining. The mirror (300 micron by 600 micron) is composed of poly-Si and Cr/Au for metalization, and sustained by thin torsion beams of 16 microns wide, 320 micron long, and only 0.4 micron thick over the through-hole in the silicon substrate. The flat surface of the mirror is obtained by supporting the it with a "boss structure" on the backside. Figure 2 shows the mirrors arranged in a 2x2 matrix (3mm x 5mm x 0.3mm *t*) for optical crossconnection. There are deep grooves on the backside of the substrate so that a light beam can transmit through; the mirrors are located at the crossings. By applying voltage, electrostatic force attracts the mirrors inwards by 90 degrees to reflect the incident light. Torsion mirrors presented here is compatible to high-density integration of free-space micro-mechanical optical switches.

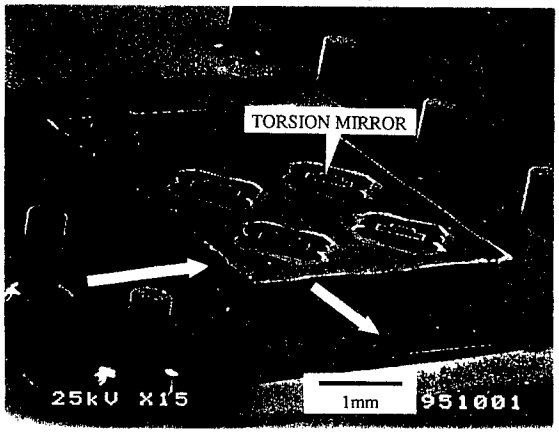


Figure 1: SEM view of a 2x2 switching matrix composed of torsion-mirrors

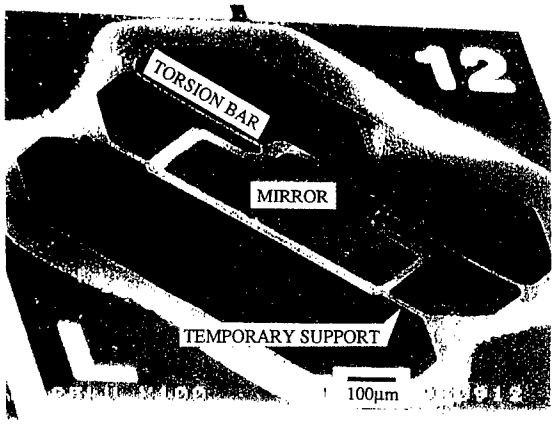


Figure 2 Close SEM view of the torsion-mirror.

The torsion beam was designed thinner than 5000 angstrom to suppress the driving voltage lower than 100V. To avoid the breakage of the fragile structures, we have developed a successful releasing process using a silicon oxide diaphragm, as shown in Fig.3. The first two steps are composed of deposition of silicon oxide and poly-silicon by CVD and metal layers by vacuum evaporation. In step (3) the mirror and the suspension are patterned on the top surface. The backside Cr is also patterned to use as an etching mask. In step (4) backside is slightly etched (30~40microns deep) by RIE (Reactive Ion Etching) to form the boss structure on the backside of the mirror. After striping the etching mask of the boss, the backside is etched again to complete the holes and grooves) to the silicon oxide as an etch-stop layer. The chance of breakage of the mirrors is negligible because they are supported by the diaphragm of silicon oxide and photoresist. In the next step (6) silicon oxide is etched away in buffered HF. Finally the photoresist is removed by O_2 ashing. In the structure-releasing sequence we have no sticking problem because the final step is a dry process.

3. Result of Optical Switching

The switching matrix was designed to combine with optical fibers for coupling. However, diameter of the light beam emitted from a typical optical fiber generally expands to eventually increase the coupling loss.

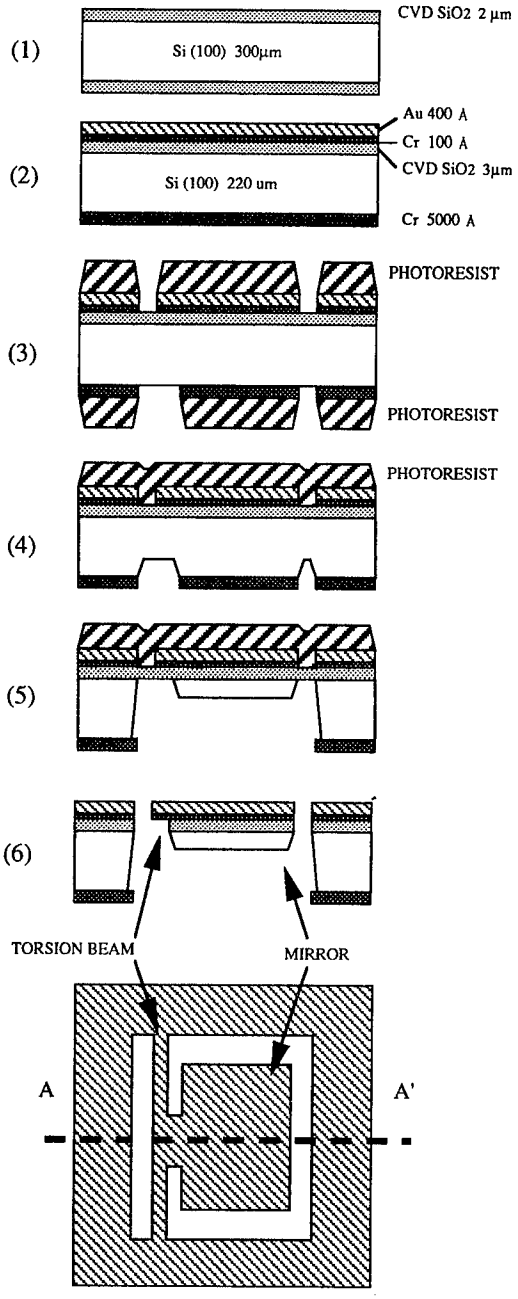


Figure 3: Fabrication sequence of torsion-mirror

Therefore, we used collimated-beam optical fiber (CBF) which has a spherical glass lens (ϕ1mm) fused at the end of a single mode fiber. Optimized coupling loss between two CBSs of 13mm gap is less than 0.5dB and 1.0 for the wavelengths of 1.55μm and 680nm, respectively. The torsion-mirror chip and CBFs were set on an optical bench using *XYZ*-stage and fiber-holders to demonstrate optical crossconnection. Both transmission and reflection are coupled by arranging the CBFs as illustrated in Fig.4. Semiconductor laser of 653nm wavelength was used.

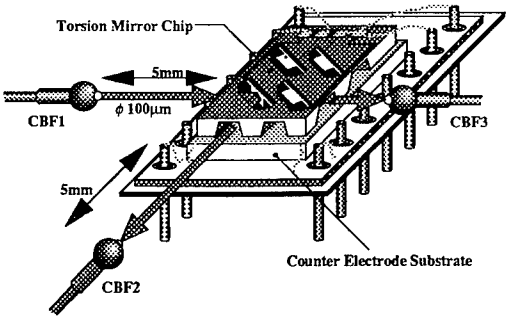


Figure 4: Configuration of the torsion-mirror chip and optical fibers

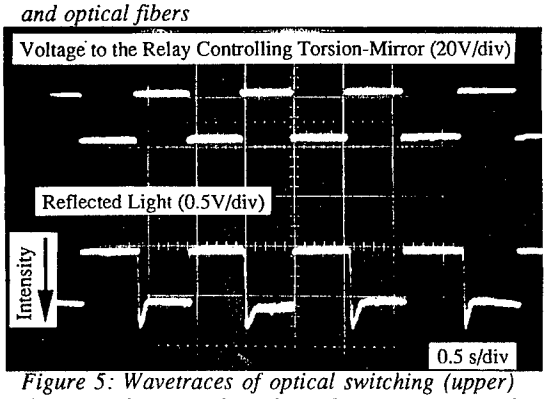


Figure 5: Wavetraces of optical switching (upper) driving voltage to the relay (lower) intensity of reflected light.

Figure 5 shows the wavetraces of the reflected light. Large attenuation ratio (> 60dB) and small crosstalk (<-60dB) were obtained. Since coupling of the CBS is sensitive to the optical axis of the light, i.e. the angle of the mirror, it took relatively large delay (0.2s); the switching speed can be reduced by reducing the mass of the mirror. The average insertion loss of 10dB was obtained.

4. Conclusion

Micromachined torsion-mirrors are suitable to integrate monolithic optical-crossconnectors of large attenuation ratio and small crosstalk. The configuration of the switches presented here is expandable for nxn (n>2). We are also planning to utilize the grooves on the substrate for the self-alignment of the fibers.

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FA4

Fabrication and Analysis of Si/SiO_2 Micro-Mechanical Modulators

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Micro-mechanical electrostatically tunable modulators have widespread applications in sensing, display and optical communication systems. Several methods for the formation of suspended membrane/cantilever modulators have been reported in the literature using GaAs or silicon substrates[1]

We report on a new and inexpensive fabrication technique for micro-mechanical electrically tunable modulators. The modulators consist of thermally grown silicon dioxide (SiO_2) cantilever structures fabricated on a (111) Si substrate. Thermally grown SiO_2 was chosen because of its excellent mechanical and optical properties. A combination of dry and wet etching is used to undercut the SiO_2 cantilevers and to provide electrical isolation. An SEM was used to analyze the electro-mechanical behavior of the cantilevers.

A cross-sectional schematic of the cantilever modulator is shown in Fig.1. The structure was fabricated by growing a 0.5 μm thick thermal oxide on a (111) oriented silicon wafer. The cantilever pattern was etched into the oxide as well as 7.5 micron deep into the silicon wafer by RIE using CF_4. A 200 nm thick Chrome layer was used as a mask during the RIE. The structure was subsequently etched in a 10 % KOH solution to laterally undercut the SiO_2. The structures where completed by sputtering a 20 nm thick gold layer over the whole wafer to form the top mirror as well as the electrical contact. The pattern was designed so that the KOH etching stopped on the desired (111) planes yielding the correct undercut of the structures while also providing electrical isolation between adjacent structures. Processing was done using 2 inch substrates containing more than 5,000 devices.

Theoretical analysis predicted a hysteric behavior of the membranes (shown in Fig. 2) which was also observed in the SEM as illustrated with Fig. 3. Experimental switching voltage are 45 V and 10 V. Strobing was used to find the resonant frequency of the cantilever. By applying a small AC signal the resonance could be clearly identified because of the large deflection of the cantilever. For our structure this occurs at 40 KHz. No degradation of the structure was observed after several hours of operation.

The optical micrographs (Fig.4 a) and b)) illustrate the optical properties of the structure, showing well-resolved interference fringes when the cantilever touches the silicon substrate. Preliminary spectrally resolved measurements showed the expected quadratic change of the wavelength with applied voltage.

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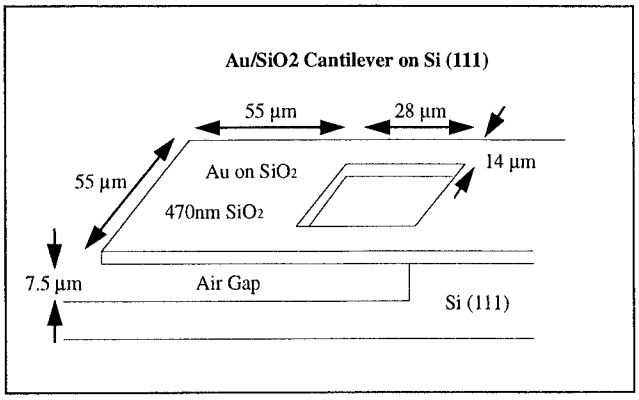


Fig.1 Crosssectional view of the cantilever structure

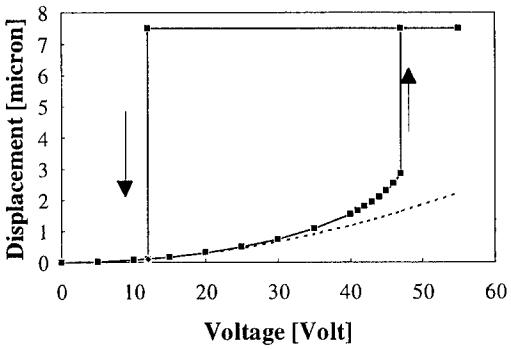


Fig.2 Predicted displacement-Voltage characteristic

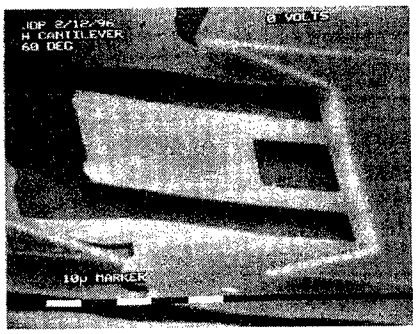


Fig. 3a SEM micrograph at 0 Volt bias

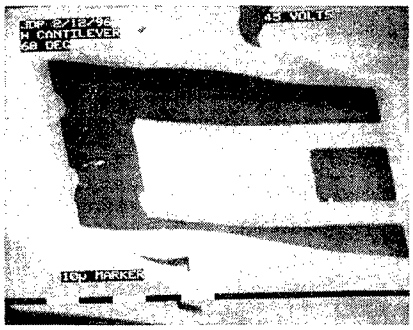


Fig. 3b SEM micrograph at 45 Volt bias

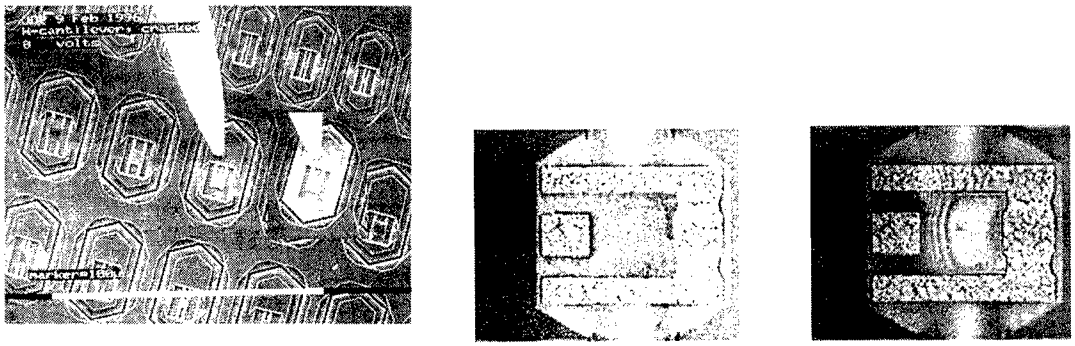


Fig.4 Top view of the cantilever a) SEM micrograph with (inset) and without applied voltage showing voltage contrast b) Optical micrograph without bias and c) Optical micrograph with 40 V bias for which the membrane touches the Si Surface

Q-switched fiber laser using a torsional micro-mirror

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1 Introduction

Micro-optical and micro-electro-mechanical technology has been highlighted during the past 5 years. Thanks to their potential of batch processing and cheap replication these technologies are merging to create a new and broader class of micro-opto-electro-mechanical (MOEM) devices.
The goal of this paper is to study the functionality of a micro-mirror in a switchable opto-mechanical system. For that purpose, we have built a compact pulsed fiber laser with a torsional micro-mirror as switching element.

2 Fibre laser

Figure 1 shows the setup of the Q-switched fiber laser. The fibre laser is based on a $120mm$ long Nd^{3+} doped fiber. The cavity consists of a micro-mirror and a Bragg grating. The fiber laser is spliced on a wavelength division multiplexing (WDM) coupler, allowing to use the Bragg grating as output reflector, while pumping through it. With this configuration, we measured the laser threshold (3 mW) and the slope efficiency (19 %). Figure 2 shows the output power versus the absorbed pump power. The measured value for the threshold is in good agreement with results commonly reported in the literature [1].

3 Torsional micro-mirror

The torsional micro-mirrors ($50\mu m \times 70\mu m$) are fabricated by polysilicon surface micro-machining. They are covered with $2\mu m$ of aluminum [2]. The SEM picture of Fig. 3 shows the address electrode and the landing electrode below the mirror. When a voltage of $35V$ is applied to the address electrode, the electrically grounded mirror rotates by an angle of 2.6^o and hits the landing electrode (Fig. 4).

4 Results

In order to get a pulsed fiber laser, the micro-mirror was actuated at frequencies between $1kHz$ and $30kHz$ to produce a modulation of the resonator loss. In such a configuration, we were able to get pulses which are about 100 times higher than the continuous emission. Figure 5 shows a typical output train at $20kHz$ mirror frequency. The pulse width at half maximum is typically $2\mu s$. If the mirror is operated at lower frequencies, the switching is too slow to get Q-switched pulses; the laser produces multiple pulses, corresponding to relaxation oscillations. Figure 6 shows such relaxation peaks for $7kHz$ mirror frequency.

5 Outlook

We have demonstrated a Q-switched fiber laser using a torsional micro-mirror. The technology for the fabrication of these mirrors is compatible with the fabrication of other micro-optial elements, such as microlenses, fan-out and fan-in elements [3]. Furthermore, arrays of pulsed lasers can be combined with arrays of micro-optical elements in order to form highly parallel optical networks.
The authors are thankful to Dr. H. Limberger at the Swiss Federal Institute of Technology - Lausanne for manufacturing the Bragg grating and to J. P. Dan, G. Kotrotsios, V. Neuman and H. Berthou at CSEM for fabricating the doped fiber.
The project was supported by the SWISS priority program OPTIQUE II and MINAST.

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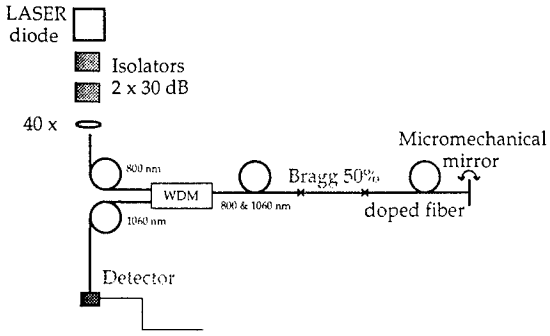


Figure 1: Schematic diagram of the Q-switched fiber laser system.

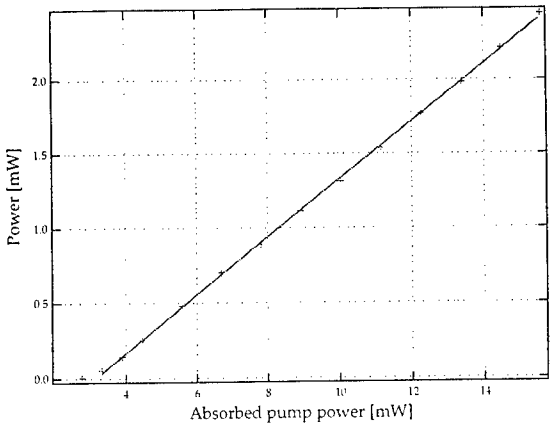


Figure 2: Characterisation of the cavity: output power vs absorbed pump power.

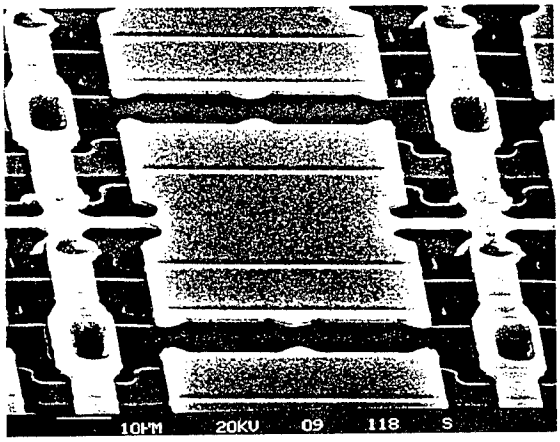


Figure 3: Top view (SEM) of a torsional micro-mirror without metallisation.

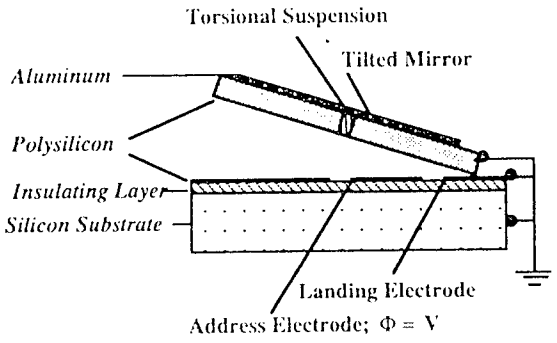


Figure 4: Crosssection of tilted position (schematic drawing).

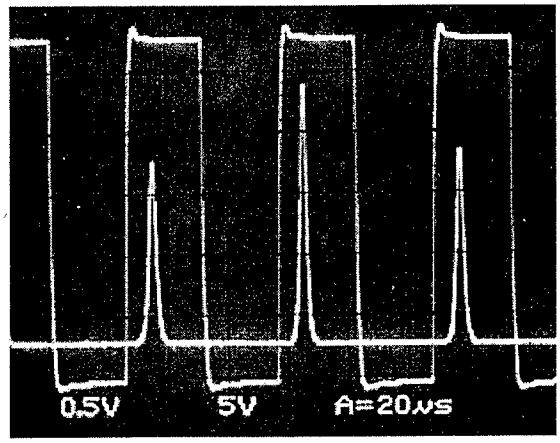


Figure 5: Q-switched output train with repetition rate $f = 20kHz$ and pump power $P = 15.8mW$.

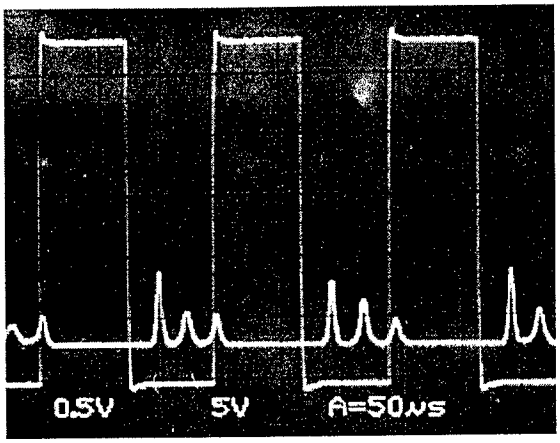


Figure 6: Output train with repetition rate $f = 7kHz$ and pump power $P = 15.8mW$.

10:30am - 11:00am (Invited)

FB1 Optical Waveguides on Silicon Combined with Micromechanical Structures

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Introduction

The integration of planar optical waveguides on silicon substrates offers a wide variety of applications in sensor as well as in communication systems. Additionally, silicon allows the monolithic integration of microelectronic circuits and micromechanical structures.

A large number of fabrication technologies were developed for optical waveguides on silicon. The most important technologies are flame hydrolysis deposition (FHD, [1]) and chemical vapor deposition (CVD), especially plasma-enhanced-CVD (PECVD). They all are based on depositing silica layers for the cladding and doped silica for the core layer. The most common dopants are germanium [2], phosphorus [3], nitrogen (see fig. 1) [4,5], arsenic [6], silicon [7] or titanium [8], which all increase the refractive index, or fluorine [9] causing an index reduction. The core layer is commonly structured by using reactive ion etching (RIE).

The FHD technology requires high (1200°C) sintering temperatures. Low-loss PECVD waveguides are usually annealed at 900-1100°C for densification and reduced hydrogen content.

For silica-on-silicon waveguides, well known and high-yield microelectronic technologies can be used like CVD-processes, sub-µm lithography or reactive ion etching. Also micromechanical structures can easily be produced on silicon substrates using e.g. anisotropic wet (e.g. KOH, NH_4OH) or dry etching of silicon.

Photonic integrated circuits

The silica-on-silicon-technology allows the integration of waveguide structures like 1xN-power dividers, multiplexers, add-drop-multiplexers or switches in planar lightwave circuits (PLC), which are coupled to standard fibers [10]. The thermo-optical effect is utilized for switches, modulators and phase shifters. Their power consumption can drastically be reduced by a micromechanical structuring of the silica and silicon layers (see fig. 2) [11]. On silicon substrates, a passive alignment of the fibers is achieved by V-grooves[12]. Well-known etching properties of single crystal silicon wafers combined with the sub-µm tolerances in UV-lithography lead to accurate passive alignment grooves [13]. This technique allows the hybrid integration of active components like lasers or photodiodes [14], which is know as the "silicon motherboard" technique. A silicon motherboard can contain PLCs, fiber alignment grooves and hybrid components on one silicon substrate [15].

Moreover, silicon microstructures can elegantly be employed to fabricate preforms for the replication of polymeric photonic waveguide devices [16].

Integrated optical sensors and actuators

The combination of integrated optics and micromechanics on silicon offers new integration potentials for sensor applications. It overcomes the difficult adjustment of fibers relative to mechanical sensor heads. A vibration sensor with integrated optical read-out is shown in fig. 3 [17]. Here, also V-grooves can be used for a passive fiber alignment. This cantilever resonator can be used for mechanical oscillation detection or it can work as a modulator using a proper drive mechanism like the bimetallic effect [18]. The cantilever design with an incorporated waveguide can be extended to a micromechanical switch using the electrostatic effect[19] or to optically interrogated electric field sensors.

The technologies for silica on silicon waveguides with emphasis on PECVD fabrication techniques will be described including waveguide design and characterization. Applications of combined optical and micromechanical technologies refer to the fields of planar lightwave circuits and silicon motherboards for photonic devices, and to integrated sensor microsystems. Silicon-based preform technologies for replicated polymeric waveguide devices are included.

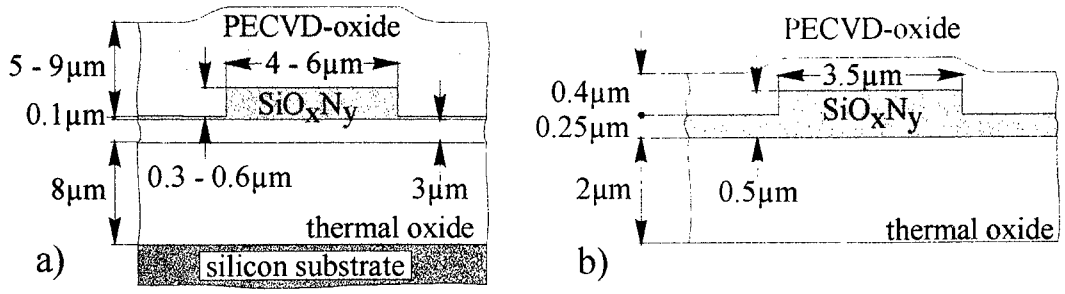


Figure 1: Plasma-deposited waveguides:
a) fiber-matched waveguide, λ = 1300-1560 nm;
b) waveguide for sensor applications, λ = 633-850 nm

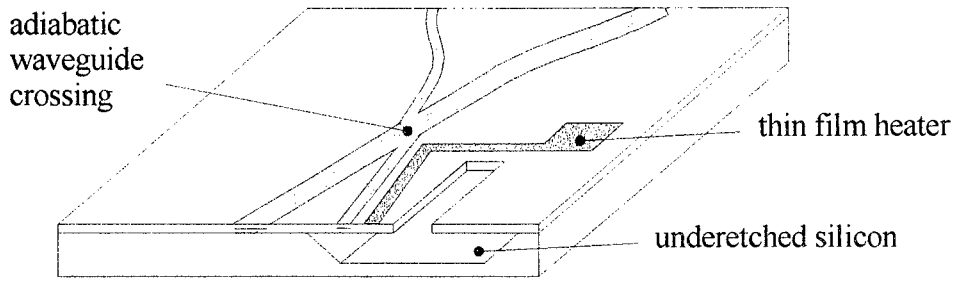


Figure 2: Thermo-optical digital switch with silicon microstructuring for reduced drive power

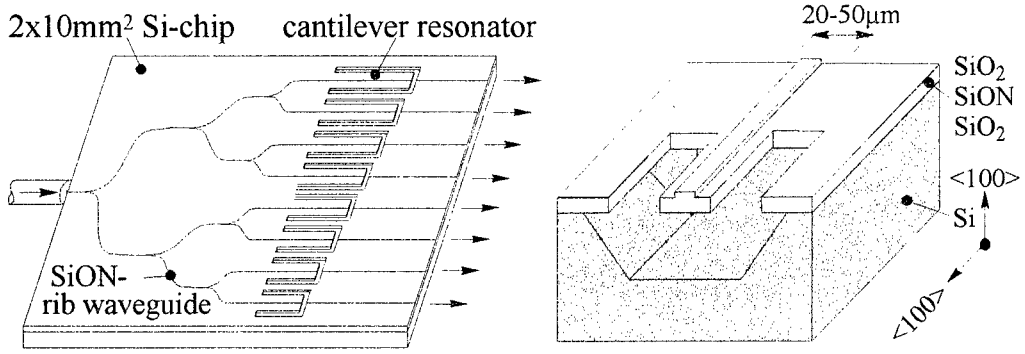


Figure 3: Array of cantilever resonators (resonance frequencies 130-210 kHz)
with integrated optical read-out

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19: E. Ollier, P. Labeye, F. Revol: Proceedings: 7th Europ..Conf. on Integr. Opt., ECIO 1995, Delft, p. 149-152

11:00am - 11:30am (Invited)
FB2

A micro-opto-mechanical switch integrated on silicon for optical fiber network

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Due to the increasing complexity of optical networks, low speed, polarisation and wavelength insensitive fiber compatible optical switches become more and more interesting, especially for network safety and network reconfiguration. We propose an integrated opto-mechanical switch by combining two mass-production technologies : Integrated Optics on Silicon [1] and Silicon Micromachining [2].

1 - Device description and modelling.

The device structure is depicted on figure 1. A voltage (U1,U2) applied between two adjacent electrodes produces an electrostatic force. This force does the cantilever beam bearing the input waveguide deflect from a distance d1 or d2. Consequently, the input waveguide faces the selected output waveguide and can switch from one to the other .
The waveguide structure is made of a sandwich of 3 PECVD silica layers with different phosphorus doping levels. The main advantage of this device is its insensivity to wavelength (1,3 µm or 1,55 µm) and polarisation.

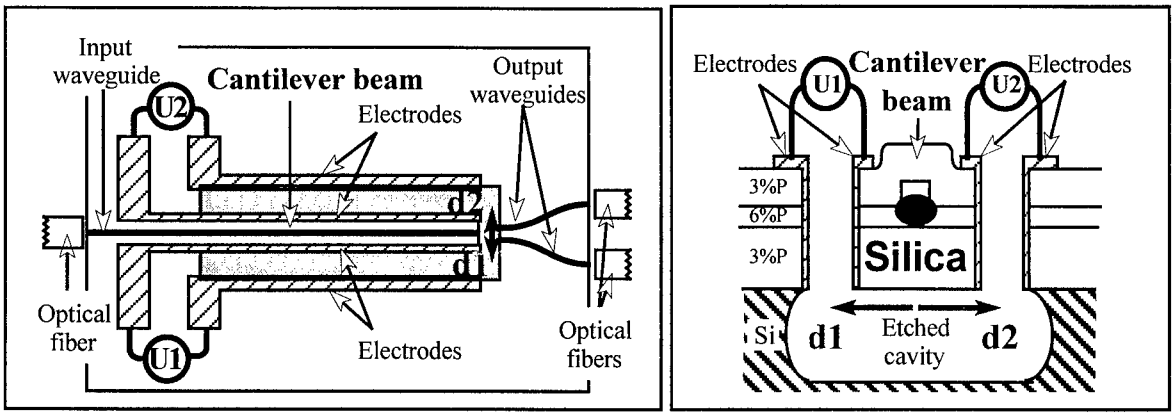


Figure 1 : Schematic views of the device

The design of the device implies a trade off between low loss, good optical isolation, and the lowest possible driving voltage. The separation between the two output waveguides has been set to 20 µm in order to get an isolation of at least 30 dB. The width of the cantilever beam has been set to 25 µm so as to ensure a low driving voltage and to avoid optical losses due to plasmons wave propagating along lateral electrodes.The inter-electrodes gap and the beam length have been set to 30 µm and 2 mm respectively. This configuration allows a deflection of 10 µm with a theoritical voltage of 360 V. In that configuration, the total predicted optical losses (fiber coupling, gap between input and output waveguides, propagation) were 1.7 dB.

2 - Device fabrication.

Three main steps are required for the fabrication. The first one is the waveguide fabrication. It is performed using LETI's usual PECVD and reactive ion etching technology [1]. The second is the mechanical structure fabrication. This step uses RIE anisotropic etching of the three silica layers (about 25 µm thick) and isotropic etching of silicon using an isotropic microwave reactive ion etching. This step makes the mechanical structure to be free standing. The last step is the driving electrode fabrication using a lateral evaporation of metal to the beam sidewalls.
Fabrication of the first silica beams pointed out an undesirable deformation problem due to residual stress in the silica layers. This residual stress made the beam tip deflect vertically. Consequently, the waveguides were misaligned. The undesirable bending of the structure was due to an intrinsic stress gradient in silica.
The problem has been solved with a dual solution : most of the undesirable deflection was suppressed by a thermal treatment and the remaining deflection was canceled by a compensating mechanical structure. This structure is made of two narrow beams (500 µm long, 5 µm large) between the beam tip and the static part of device (Figure 2).

3 - Experimental results.

The efficiency of the solution (thermal treatment+compensation mechanical system) for cancelling the vertical deviation of the beam tip has been tested. The results on the residual deviations and on the optical losses reported on figure 3 have shown that both solutions must be used to cancel the average vertical misalignment and to limit the dispersion below 1 µm. Then the devices were tested under complete operation. Results are summerized in table 1.

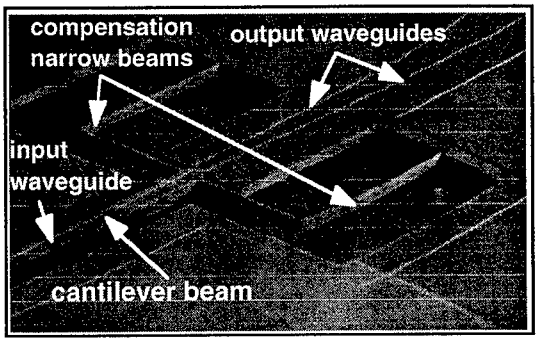


Figure 2 : SEM photograph of a micro-opto-mechanical switch with compensating mechanical system (generation1)

	I	II	theory
Residual deflection (µm)	0 +/- 5	**0 +/- 1**	0
Driving voltage (V)	270	**346**	360
Insertion loss 1,3µm (dB)	6,1	**3,6**	1,9
Insertion loss 1,55µm (dB)	6,3	**4,7**	1,8
Isolation 1,3µm (dB)	34	**33,6**	36,3
Isolation 1,55µm (dB)	24,2	**25,7**	31,9
Switching time (ms)	-	**0,6**	-

Table 1 : Results of micro-opto-mechanical switches
I : thermal treatment, no compensation structure
II : thermal treatment, compensation structure 500 µm

4 - Device improvement : reduction of the driving voltage

In order to reduce the high driving voltage of the first devices, a second generation of micro switches with a new electrostatic driving structure has been achieved (Figure 4). The way to obtain low optical losses (thermal treatment + compensating mechanical system) is the same as for the first generation devices. The reduction of the driving voltage has been obtained by the combination of two means : an electrostatic comb (gap : 15 µm) and the using of the phenomenon of electrostatic instability [3]. This configuration decreases the sensitivities to polarisation and temperature that were due to the metallisation of the beam. Results of this last version are summerised in table 2.

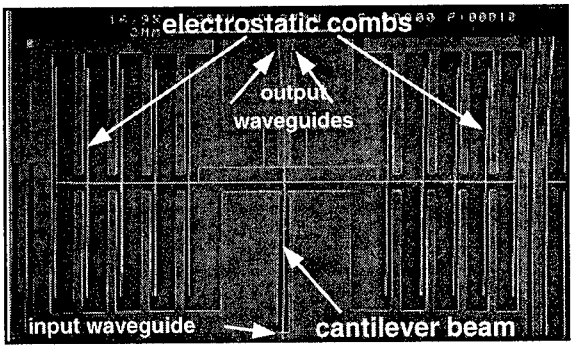


Figure 4 : SEM photograph of a "generation 2 "switch

Driving voltage (V)	**28**
Insertion loss 1,3µm (dB)	**3,3**
Insertion loss 1,55µm (dB)	**4,3**
Isolation 1,3µm (dB)	**37**
Isolation 1,55µm (dB)	**27,2**
Switching time (ms)	**0,8**

Table 2 : Results of "generation 2" switches

Conclusion.

The feasibility of a micro-opto-mechanical switch combining "integrated optics" and "micromechanics" on silicon technologies has been demonstrated and the performances are not far from the telecommunication specifications.This work shows that "Micro-Opto-Mechanics" is of a great interest to achieve active components for telecommunication systems. Moreover "Micro-Opto-Mechanics" is also very attractive for sensors with integrated optical read out. For instance, a vibration opto-mechanical sensor for hydroelectric generating sets has been achieved in our laboratory.

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11:30am - 11:45am
FB3

PACE, A Dry Etch, Ultra-High Speed, Precision Machining and Polishing Process for Micro/Macroscopic Features w/o Subsurface Damage

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Hughes Research Laboratories
Malibu, CA 90265

Summary

A non-incremental improvement in the fabrication of integrated Micro-Electro-Mechanical (MEMS) devices can be expected from Plasma Assisted Chemical Etching(1) (PACE) because it is an extremely fast (0.1 mm/min or ~10^3 faster than RIE) and precise (~1% or ~ 10 times more repeatable) dry etch process with the ability to shape and polish both microscopic and macroscopic features (~ 0.1 micron to > 1 cm) without subsurface damage. For example, PACE offers precision machining of large area arbitrarily aspheric surfaces, and in the same process, microstructures with the small feature sizes required for sensors, microelectronic devices, monolithic packages for microwave circuits and antennas, optical gratings and detector arrays over these areas.

PACE was first developed for macroscopic applications such as optical figuring, thinning and flattening of Si & SiO_2 and is now being extended to microscopic applications such as lithographic pattern transfer and to a wider range of materials. It has already found commercial use to uniformly thin &/or flatten 200 mm diameter silicon wafers. It will machine Si, SiO_2, Si_3N_4, SiC, Si-Ge, GaN, GaAs, InP, Ge, Al, W, Cr, among other materials; furthermore it permits reliable control of etch directionality from anisotropic to isotropic.

PACE is based on a well developed theory, in excellent agreement with experiment and is shown(2)(3)(4)(5) to be a parameter extension of the well known plasma or reactive ion etch (RIE) processes, but with important differences:

1- PACE's unusually high etch rate is more striking in terms of its volume removal rate because it is comparable to a mechanical grinding rate, e.g., the volume removal rate may be 10 mm^3/min. for a 10 mm diameter plasma etch tool. The plasma tool can be as large as the wafer and as small as a few mm.Its ultra-high rates permit practical computer controlled scanning with small tools with over the surface average rates of 100 microns/min* $10^2/100^2$ = 1 micron/min (10 mm tool scanned over a 100 mm wafer).

2- PACE is primarily a chemical process, without loss of etch directionality and without perceptible sputtering and subsurface damage(5)(6), because its plasma ion energies are under 10 eV. In contrast, conventional RIE processes generate greater than 50 eV ion energies, necessarily producing subsurface damage because they are well above the sputter energy threshold. Also, its etch selectivities (etch rate ratio between different materials) can approach those of wet etch processes (>300:1)(3) due to the low ion energies.

3- PACE intrinsically polishes homogeneous (crystalline or amorphous) materials, for both the anisotropic(unidirectional) and isotropic(omnidirectional) etching, from considerable roughness (> than 10's of microns rms) down to atomic dimensions(4)(7).

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2:00pm - 2:30pm (Invited)
WC2

MEMS Applications in Optical Systems

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Introduction

We describe progress in the development of basic micro-opto-mechanical; components which are compatible with MEMS and integrated circuit processing processing. Devices which have been developed include polygon and diffraction grating scanners, tunable laser diodes, tunable IR filters, and optical waveguides.

Polygon Microscanners

A planar view of a polysilicon microscanner consisting of a hollow, nickel plated polygon reflector on the rotor of an electrostatic drive micromotor is shown in Figure 1. The nickel plated polygon reflector is approximately 175μm in diameter, 20μm tall, and 10μm thick. The diameter of the micromotor rotor is 500μm. These dimensions are typical of microscanners produced by surface micromachining. The 20μm vertical height of the nickel reflector is typical of elements that can be produced by our electroless nickel plating process. We have produced micromotor scanners similar to Figure 1 with diameters from 250 to 1000μm although the larger micromotors do not operate reliably after release.

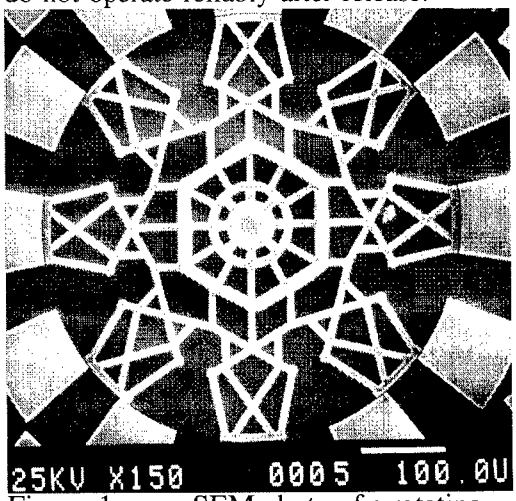


Figure 1. SEM photo of a rotating polygon optical microscanner on a 500μm diameter salient-pole micromotor.

Diffraction Grating Microscanners

An optical microscanner which consists of a diffraction gratings on the rotor of an electrostatic polysilicon micromotor is shown in Figure 2. The diffraction gratings are produced by chemical etching, then chemical-mechanically polished (CMP) to reduce the average surface roughness, improving the optical efficiency of the gratings. This process has been used to produce diffraction grating microscanners. These devices require thick (e.g., 5.5 μm) polysilicon rotors to provide sufficient mechanical stiffness and to prevent out-of-plane warping of large area rotors.

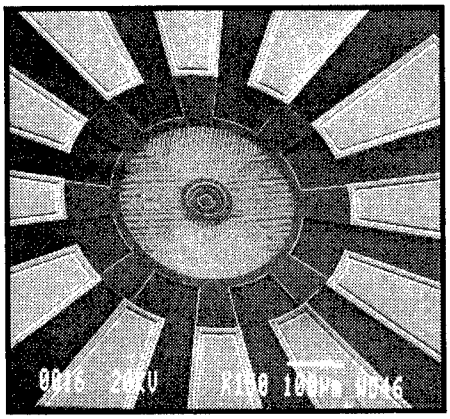


Figure 2. SEM photo of a rotating diffraction grating microscanner. The motor is a 500-μm diameter salient-pole side-drive micromotor with polished rotor/stator polysilicon and pyramidal grating element of 1.8 μm period.

Laser Diode Tuner

A (111) sidewall of a silicon cantilever beam has been developed as a tunable micromirror for a tunable laser diode. The micromirror beam was fabricated by anisotropic etching of (110) silicon in conjunction with silicon-to-glass bonding. Electrodes located on either side of the beam provide the electrostatic force that deflects the beam; the (111) sidewall of the cantilever beam functions as the external mirror of an optical cavity. Mechanical stops limit the lateral deflection of the beam, preventing electrical shorting to the

electrodes. Figure 3 is an SEM image of the final device. The beam is about 1.7 mm long, 8 μm wide, and 130 μm high. The external cavity length, (the gap between the beam sidewall and the laser diode facet) is about 10 μm. The laser diode is a gain guide type with planar stripe; the active layer is an AlGaAs multiquantum well structure. The cavity length of the laser diode is about 340 μm.

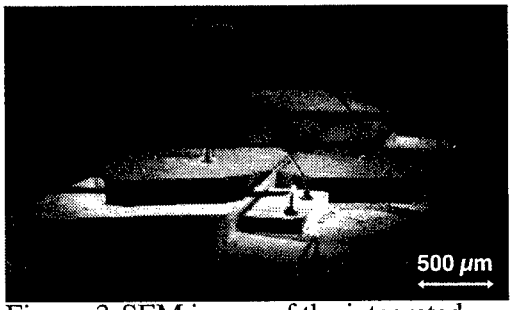
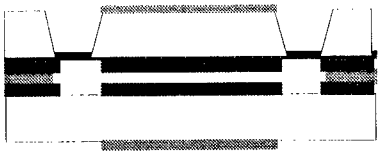


Figure 3. SEM image of the integrated laser diode and micromirror.

Tunable Optical Filters

Many optical devices require specialized optical coatings, for high reflectivity dielectric reflectors and for multi-layer anti-reflection coatings. Our approach to process integration is to do all microlithographic processing prior to any dielectric coating keeping the processes separate. We use shadow masking to pattern the optical reflective coatings on a micromachined device DSP (double sided polished) silicon wafer. We are constructing a tunable IR filter by bonding two DSP wafers with multilayer dielectric reflective optical coatings (of ZnSe and ThF_4) together to form an optical etalon. We use a KOH etched shadow mask to pattern precise thicknesses of the dielectric films used to produce the reflective coatings to maintain strict tolerances on the spacing between the reflective coatings and the parallelism of the optical surfaces. Additional depositions of the dielectric materials can be used to achieve the required spacing between the optical reflective coatings. We are currently investigating how to bond the micromachined, optically coated surfaces together. The most attractive approach appears to be a patterned evaporative coating of a low melting point metal to act as a bonding layer. Figure 4 schematically shows a $ZnSe/ThF_4$ tunable infrared filter.


Figure 4. Tunable IR filter using evaporative coated spacers.

Both wafers are coated with reflective coating, note the reflective coating is also deposited in the spacer region. A subsequent evaporative deposition places material in the spacer region. A antireflective coating may be deposited on the backsides. All deposition is via shadow masks. The wafers may then be brought into contact as shown. Not shown are additional alignment and electrode contact patterning processing steps on both wafers.

Silicon Waveguides

We have fabricated all-silicon rib optical waveguides and U-groove alignment structures on (110) silicon substrates. Such all-silicon waveguides are compatible with our micromachining processing and are necessary components for MEMS based optical fiber devices. Rib waveguides consisting of 6.7 μm tall by 5-15 μm wide ribs have been RIE etched in lightly-doped epitaxial silicon layers deposited on heavily doped silicon substrates. Ultrasonic etching was used to decrease the roughness of etched structures. Experimental measurements of these devices at 1550 nm indicates that the waveguides are single mode. The optical loss was measured to be as low as 1.68 dB/cm.

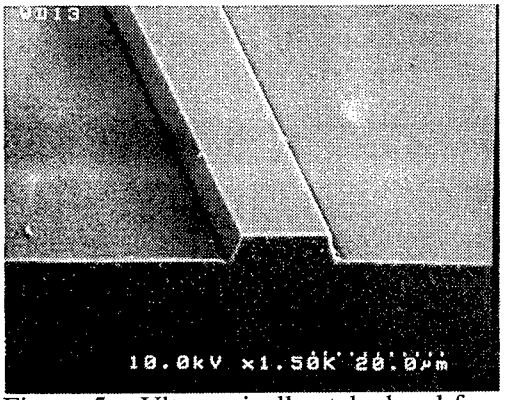


Figure 5. Ultrasonically etched end-face of a rib waveguide with a rib height of 6.7μm, a base width of 15.5μm and an etch angle of 83.6°.

OPTICAL MEMS AND THEIR APPLICATION

PAPERS NOT AVAILABLE FOR THE FOLLOWING

10:30am - 11:00am (Invited)

ThB1: Microphotonics Based on Actuated Silicon Surface-Micromachined Structures,
K. Lau, *UC Berkeley*

A batch- assembled opto-electronic packaging technology based on silicon surface micromachined, movable alignment mirrors will be described which have the functionality, stability, and accuracy required for active copuling in high- precision optoelectronic packages and miniatururized subsystems.

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