SMD-R-113

A Fast-Framing, High Resolution Digital Camera

SBIR Phase I Final Report

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13. ABSTRACT (*Maximum 200 words*)

White Sands Missile Range has identified the need for a solid state camera which can be used to replace older film technology in capturing various high-speed airborne projectiles. Older, film based cameras do not allow for real time focus or light level adjustment and impose significant delays in the processing of image data. In addition, the use of Silver Halide films is an environmental hazard which is under increasing pressure to be eliminated. This report involves the design of a solid-state imaging system based on a 2048x2048 CCD. The new camera will be capable of operating at speeds up to 200 frames per second with 10 bit gray scale and electronic shuttering. The camera is accompanied with up to 250 frames of on-board memory and is capable of porting data through high-speed parallel interface to a variety of expanded memory interfaces.

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1.0 BACKGROUND

White Sands Missile Range has identified the need for a solid state camera which can be used to replace older film technology in capturing various high-speed airborne projectiles. Older, film based cameras do not allow for real time focus or light level adjustment and impose significant delays in the processing of image data. In addition, the user of Silver Halide films is an environmental hazard which is under increasing pressure to be eliminated. A summary of the target specifications for the desired solid-state camera is given below:

Application:	Replacement of 16mm film for imaging airborne intercepts
Requirements:	Solid state camera for digital, high resolution cinematography, with permanent data storage, for immediate data feedback after test, and subsequent playback availability on demand. It is important that there be no data loss upon compression and reconstruction of images.
Array Size:	2K x 2K pixels
Frame Rate:	200 FPS
Shuttering:	Electronic
Dynamic Range:	10 bits
Wavelength:	Visible
Record Duration:	One minute

There are several technical challenges in meeting this need including:

1) What type of imager is best suited for the large area, high-speed array?
2) The imager chip will necessarily be a multiport architecture. What issues must be addressed in matching gains and offsets of the multiple amplifiers over the entire range of anticipated operating conditions?
3) How will shuttering (exposure control) be accomplished to minimize image blur of dynamic objects?
4) How will parasitic currents in the imager substrate be controlled so that imager tile balancing can be maintained?
5) How will 10 bits of gray scale be achieved at this frame rate?
6) What, if any, data compression techniques will be used?
7) What type of memory system should be used?

During the Phase I investigation, SMD evaluated a range of imager and memory architectures, and performed a tradeoff analysis between the possible solutions to find the lowest risk/best fit to the technical needs of White Sands Missile Range. The following paragraphs summarize the various alternatives and conclude with a summary of the proposed approach:

2.0 CMOS ACTIVE PIXEL SENSORS

At first glance, CMOS Active Pixel Sensors (APS) seem quite attractive in this application because:

a) large format wafers used in CMOS fabrication makes very large arrays feasible,

b) small features in CMOS result in high gain and therefore wide band on-chip amplifiers capable of high pixel rates per channel, and

c) small geometries allow for the creation of many pixels in a relatively small area. Unfortunately, the very features which, at first seem attractive, are some of the real weaknesses of APS devices.

First, the fact that small geometries will be needed means that the 1/f noise will extend over a very large bandwidth. In theory, correlated double sampling can be used to remove this noise however current implementation of CDS in CMOS imagers does not function on the entire image at one time. CDS is actually performed on a line by line basis. One line of the imager is addressed and the reset level is sampled for every pixel on that line. Signal charge is then injected and the two values are subtracted on chip. Next, line number two is addressed, the reset level is measured, and finally the signal charge is injected and measured. This process continues until the last line is read. The weakness in this approach is that each line in the image is actually exposed and read at a different instant in time. For static or slow moving targets, this approach works fine. However, extending the APS architecture to fast framing applications is not straightforward. In highly dynamic events, this line-by-line imaging process will introduce missing data and unacceptable blur in the image. One solution to this problem is to sample the reset value across the entire image and store the results in off-chip memory. The signal charge is then injected across the entire array at one time and then the array is read out a second time. Finally, the two images are subtracted and true CDS is achieved. This has been implemented by NASA in some of their APS research and it works quite well (at low frame rates). The problem is that a) it takes off chip memory and b) it requires that the imager be read out twice per frame - thus reducing the effective frame rate by a factor of 2. Now, a 100 Mpixel bandwidth is needed to achieve 50 Mpixel data rates.

An alternative design approach which could be utilized to provide "real" correlated double sampling is to incorporate a memory cell within each pixel site. By incorporating a local memory site, the photo charge in each pixel can be stored while the reset level is measured. After storing the reset level, the signal level at each pixel can be sensed and the two values may then be subtracted. The obvious disadvantage to this approach is that additional silicon real estate is needed and many of the benefits of the small geometry CMOS are effectively lost.

An additional limitation found in all of the architectures described results from the fact that each pixel in the CMOS array must pass through several multiplexers and amplifiers before reaching the final video output. Each of these amplifiers is necessarily wide band and will introduce its own 1/f and thermal (white) noise. In summary, while literature exists suggesting 10-12 bit

performance in CMOS imagers, careful evaluation of the measurement conditions creates significant doubt as to whether low noise and high speed characteristics are simultaneously achieved.

3.0 FRAME TRANSFER CCD

A 2048 x 2048 imager is feasible using a frame transfer CCD. The disadvantage of frame transfer is primarily that the minimum exposure time (shuttering) is not very effective for exposures less than about 2ms. In contrast, interline architectures or intensified architectures can give exposures down to microseconds. The advantage of the frame transfer or full frame architecture is that pixel sizes are typically smaller leading to a simpler design and higher yield.

An example of the problem encountered when trying to shutter frame transfer CCD's is shown in Figure 1. This figure shows a spinning top along with a (stationary) pair of scissors. By shuttering the camera at 1ms, the camera successfully stops the motion of the spinning top. Unfortunately, the time required to transfer the image from image zone to memory zone in this particular imager is about 4 ms. During readout the initial crisp image is shifted through the image plane, and significant vertical smear contaminates the resultant image. There are algorithmic methods of suppressing the smearing effect, however, this post processing results in significantly reduced dynamic range.

Figure 1. Image smear resulting from short exposure in a frame transfer CCD.

4.0 ELECTRON BOMBARDED CCD'S (EBCCD'S)

One solution to the minimum exposure time limitation found in conventional full frame or frame transfer devices is to operate in an Electron Bombarded (EBCCD) mode. EBCCD's are essentially intensified CCD imagers. Rather than imaging light, a photocathode is placed in very close proximity to a backside thinned CCD imager. Photoelectrons liberated from the photocathodes surface are accelerated through a potential of hundreds to thousands of volts and shot into the thinned CCD. Since the accelerated electrons have very high energies upon entering the silicon, multiple electron-hole pairs are generated, and electron bombarding gain occurs. This gain can vary from 100's to 1,000's and is achieved at substantially lower noise levels than traditional image intensifier tubes. In addition to providing the possibility for gain in the system, the EBCCD, like an intensifier, can provide gating speeds on the order of 5-10ns which allows for shuttering of the event. This shuttering would result in sharper pictures of fast moving objects.

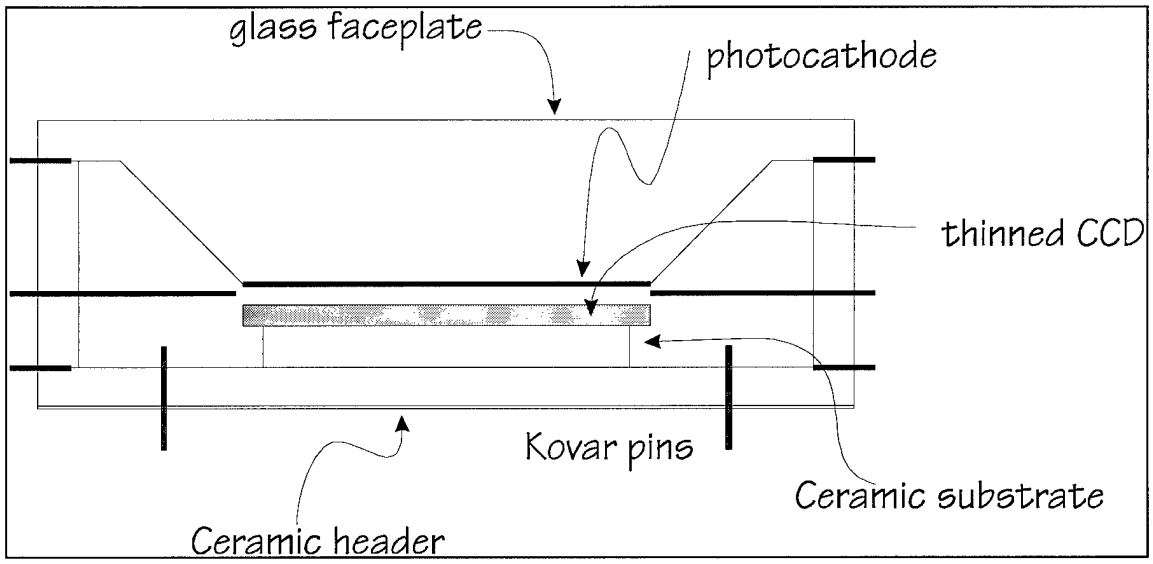

Figure 2. EBCCD intensifier.

Theory of EBCCD based image tubes

EBCCD tubes operate on the principle that electrons generated at the surface of the photocathode are accelerated toward the surface of a backside illuminated, thinned CCD which acts as an almost noise free gain stage through the mechanism known as Electron Bombarded Semiconductor (EBS) gain. When a high energy electron is injected into silicon, the primary electron interacts with the crystalline lattice and loses energy through a variety of loss mechanisms. Fortunately, most of this energy is channeled into the creation of secondary electrons via Rutherford scattering. The mean number of secondary electrons created from each primary electron is given by:

$$N_{secondary} = \frac{energy_{primary}(eV)}{3.65}$$

It is important to note that the energy of the primary electron inside the silicon lattice is often different from the energy in the space between the photocathode and the CCD. This is a result of an energy barrier at the surface of the CCD, usually a thin oxide layer. Thus, the energy in the lattice is the barrier energy subtracted from the incident energy. The values of the energy barrier are very dependent on both the design of the CCD and the process by which it was thinned. Typical values range from a few hundred volts to a few thousand volts, with an average barrier of about one thousand volts. Thus, using an accelerating potential of 1.8 kV, only 800 volts of energy is used to create the secondary electrons: in which case the EBS gain would be 225. Once again, it is important to stress that while this gain is lower than current generation image intensifiers, it is not detrimental, and in fact very beneficial. What is important is not the gain, but the increase in the amount of information. Since a gain of 225 is more than sufficient to overcome the noise floor, it is possible to detect light not only on an analog basis (how much light), but on a digital or binary basis (did a photon strike the photocathode or not?). Once the ability to make a statistically significant statement of detection of an event is achieved, excess gain does not yield further advantages.

Continuing with the description of operation, each incident electron follows a random path inside the silicon, and may indeed scatter out of the silicon. Such electrons are said to be backscattered[1] and the fraction of backscattered electrons generally decreases with increasing energy of the primary electron. Electrons with energy higher than 1.78 keV can also generate K series X-rays, which are not desired in electron imaging applications These X-rays can be absorbed by the silicon dioxide layer between the substrate and the gate structure which causes increased dark current and a flat band voltage shift, slowly decreasing the full well capacity of the CCD. It is possible to reverse some of the damage by heating the CCD to allow the trapped charge to recombine, but this may cause trapped gasses to evaporate off of the silicon, harming the photocathode.

What makes semiconductors, and silicon in particular, so desirable to use as high energy particle detectors is the associated variance of the number of secondaries created. Consider a scintillator (or phosphor) that requires a 100 eV particle to create one 2 eV photon. Since the energy lost is 98 eV, there are many loss mechanisms occurring, and the resulting statistical distribution of photon creation must be Poisson. Next, consider a scintillator that has no energy loss mechanism except for photon generation (a 2 eV particle creates a 2 eV photon). Such a device would have no variance associated, and the statistical distribution would be a delta function. Now, consider a semiconductor that requires only 3.65 eV to create a 1.1 eV secondary electron. The statistical distribution of secondary electrons must then lie between a Poisson and a delta function distribution. The ratio of the variance to the mean is unity for Poisson, and for the semiconductor detector as mentioned above, the ratio must be less than one. This ratio is termed

[1] Ravel, M. and Reinheimer, A. "Backside-thinned CCDs for keV electron Detection". CCDs and Solid State Optical Sensors II, pp. 10. Proc. SPIE vol. 1447.

the Fano factor[2], and for silicon, typically is around 0.1. It is this phenomena which marks out CCDs as excellent electron detectors.

4.1 Figures of Merit for Design

Factors relating to figures of merit

One of the primary benefits of EBCCD tubes is their simplicity of operation. In fact, once the tube is built, the only parameters that can be changed are the bias voltages of the photocathode and CCD. With this simplicity comes a "disadvantage" of several figures of merit being coupled. The accelerating voltage (bias voltage between the photocathode and the CCD) determines not only the EBS gain, but also:

- affects the resolution (radial spread of electrons in a proximity focused tube is inversely proportional to the square root of the accelerating voltage)
- affects the size (the higher the voltage, the further apart the photocathode and CCD must be to prevent arcing)
- affects the noise (higher electric fields cause higher rates of field emission of ions, which propagate toward the photocathode and, upon impact, release a flood of non-signal electrons-thus higher noise)
- affects the dynamic range (since the electron creation is a discrete and quantized process, a high gain will place a limit the number of electrons needed to create a full well)

The dynamic range of the device can be defined as the ratio of the largest detectable signal to the smallest detectable signal. In the case of the Gen II tube, it is limited on the high end by the buffer layer and the amount of standing wall current[3], while the EBCCD is limited on the high end by the full well capacity of the CCD. The full well capacity of a CCD is determined by several factors including: gate voltage, pixel size, and surface versus buried channel operation. Obviously, increasing the pixel size will increase the full well capacity, thus increasing the dynamic range. However, spatial resolution suffers due to a larger sampling period. In addition, the gate voltage cannot be increased indiscriminately because there is a point at which the electric field in the silicon and oxide layers will break down, resulting in a shorted pixel. On the low end, both the Gen II tube and the EBCCD tube are limited by the amount of system noise present. Since both tubes have photocathodes, the thermal noise of the photocathodes is the same in both types, but the EBCCD tube will have lower noise limited primarily by the read noise of the CCD. The Gen II tube has a higher noise associated with the multiple conversions, and the associated variances of conversion efficiency.

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[2] Van Roosbeck, W. "Theory of the Yield and Fano Factor of Electron-Hole Pairs Generated in Semiconductors by High-Energy Particles". Physical Review, v. 139, 5A pp. 1702. 1965.

[3] Laprade, Bruce N. "The high output technology microchannel plate". SPIE Milestone v. 20 p52.

SMD is currently developing two different EBCCD architectures - a 512x512 and a 1Kx1K - 12 bit (video rate) camera. Our experience with EBCCD and other high frame cameras has shown that one of the keys to high-quality, high frame rate imaging (particularly in the case of multiport architectures) is the existence of a good, low impedance substrate connection. The CCD substrate acts as the ground plane for the CCD circuit, and must provide a low impedance path for displacement current generated within the bulk of the device. Clocking of the vertical polysilicon gates in a large area imager results in a displacement current which must be efficiently sinked by the substrate connection. At low frame rates, the vertical clock edges are not very fast, and even relatively resistive substrate connections will typically suffice. However, at higher frame rates, the vertical edge rates can easily be 50 to 100ns. This edge rate combined with the capacitive load of a large area imager (e.g. 50,000pF) and 10 volt clock swings can generate instantaneous displacement current on the order of 10 amps.

A highly resistive substrate connection means that these large displacement currents will generate a voltage drop across the substrate volume. The displacement current is not uniform across the device because the amount of capacitance varies spatially across the array. For example in a multiple output imager, some output amplifiers are near the center of the array where there is a high level of displacement current, while others are near the edge of the device where current levels are lower. Thus, the substrate becomes biased to a different level at different physical locations across the chip. To further complicate things, the difference in substrate bias is affected by both the frame rate of the chip and device temperature since current levels increase at higher frame rates, and substrate resistivity changes with temperature. From a system level, the primary effect of this differing substrate bias is that the gain and offset of each output node will vary with both frame rate and temperature.

The EBCCD starts with a backside thinned CCD, which, in a sense, provides the worst possible substrate connection. Thinning of the CCD removes the highly doped substrate (leaving the lightly doped epitaxial layer, and inherently results in a very poor substrate connection). Thus, left alone, the EBCCD is a fairly poor candidate for high frame rate operation. However, the EBCCD has so many other useful attributes in the proposed imaging scenario, that it warrants some effort to find a solution to the substrate problem.

SMD has been working with researchers at NASA's Jet Propulsion Labs on a proprietary solution which provides the necessary low impedance connection while simultaneously being compatible with standard CCD processing techniques. The proposed solution is to deposit a thin layer of metal on the surface of the backside thinned CCD. The metal would be deposited at a low temperature to avoid doping the silicon backside, and holes (or "apertures") would be opened in the metal layer to act as "photosites" for the proximity focused electron beam. Some loss of fill factor will result from this technique because of the aperture pattern. However, the gain offered by the EBCCD approach should more than compensate for this small loss. *[An alternative means of biasing the back surface through the use of implants (delta doping) was also investigated. Since the doping is transparent, it was hoped to eliminate the problem of reduced fill factor. However, the delta doped back side treatment is designed only to pre-bias the silicon surface, and does not provide an adequate low impedance connection for high speed operation.*]

5.0 INTERLINE TRANSFER CCD

Interline transfer CCD's have several clear advantages in high speed imaging applications. Since the interline architecture has a shielded memory zone adjacent to each active photosite, transfer of charge from the imaging to storage areas can be completed in 10's of nanoseconds rather than the millisecond time frame more typical of frame transfer architectures. This fast transfer in combination with ether lateral or vertical antibloom diffusions gives the interline architecture the ability to provide on-chip electronic shuttering to as fast as 10 microseconds. Moreover, since the "snapped" image is shielded from additional exposure during the image readout phase, the image smearing problem found in frame transfer devices is nearly non-existent. After reviewing several alternative architectures and the requirements of the White Sands applications, it was concluded that the lowest risk path to the problem at hand is to use a conventional interline transfer CCD. SMD is currently building a 1024 x 1024, 1,000 FPS interline transfer CCD capable of 10 to 12 bit dynamic range. Preliminary testing of the new imager has been completed by NASA's Jet Propulsion Labs, and excellent results have been

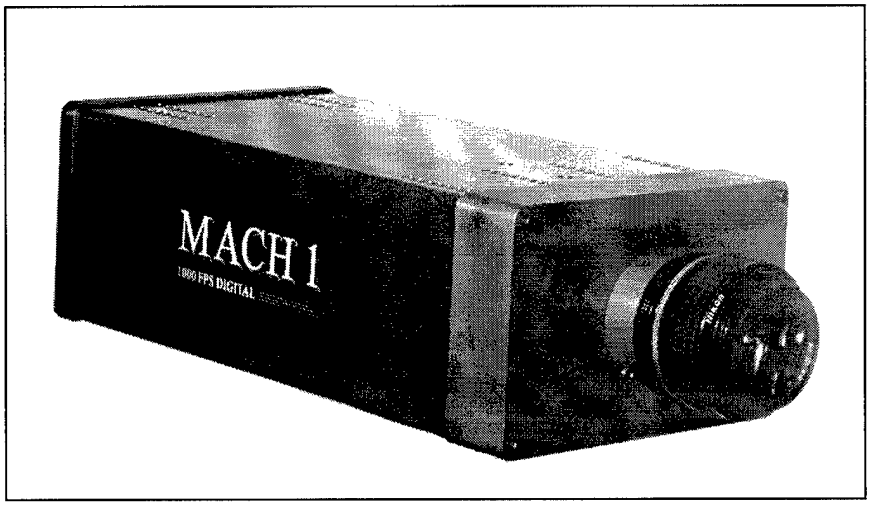


Figure 3. 512 x 512 camera.

achieved. Testing by JPL at reduced frame rates have resulted in an rms noise floor of less than 7 electrons (cooled) and around 60 electrons at room temperature. The device is a modification of a commercially available 512 x 512 design which is currently yielding 10 bits at 1,000 FPS without cooling. The images shown in Figure 4 are of a static bomb drop at Eglin Air Force Base using the 512 x 512 camera.

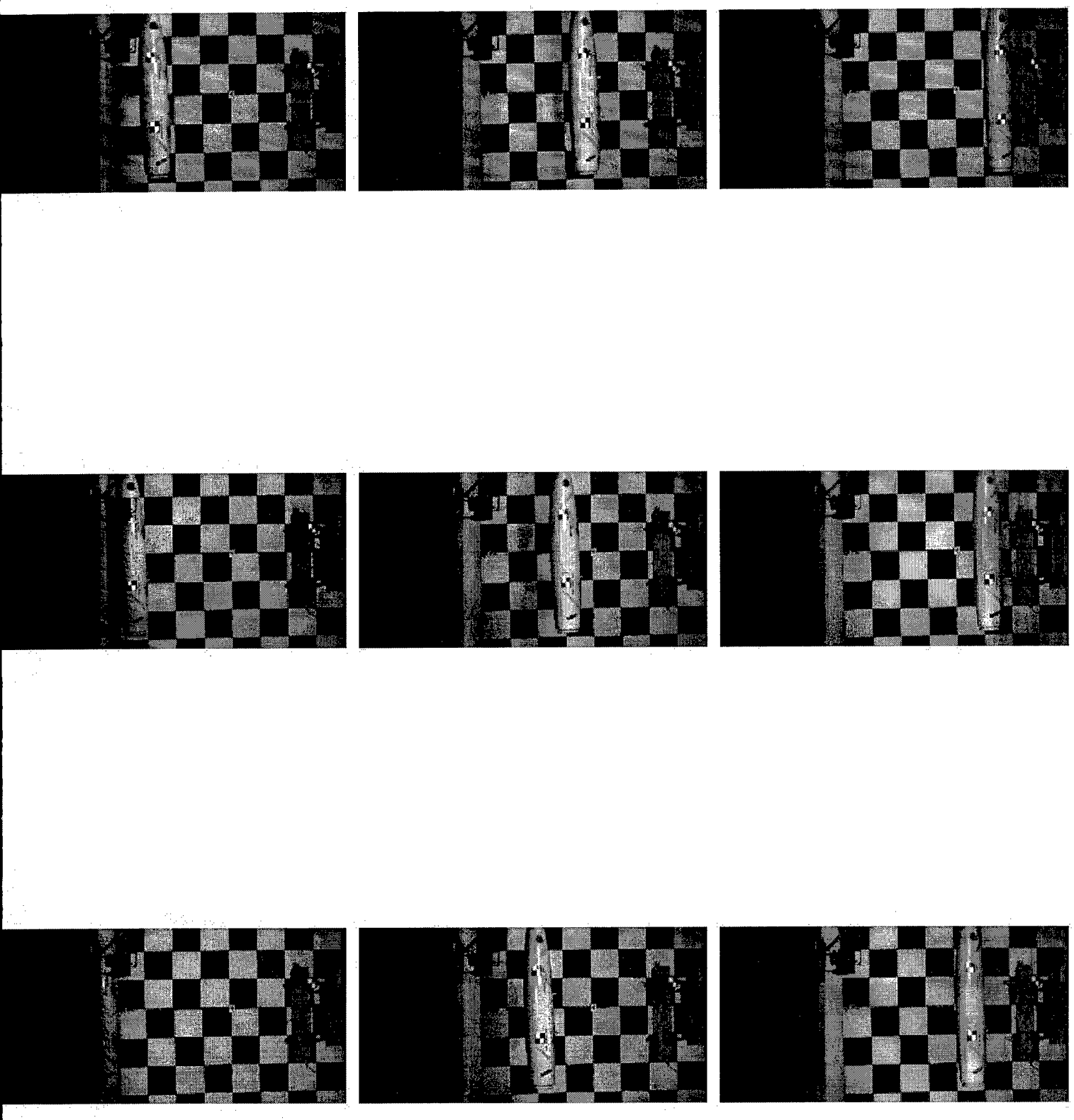


Figure 4. Static bomb drop.

Modifying the 1024 x 1024 design to yield a 2048 x 2048 or larger device is primarily a matter of device yield. With current operational parameters, a 2048 x 2048 camera based upon this architecture would provide 250FPS at 10 bits. Additional output amplifiers could be added to increase this rate to around 500FPS. SMD's current camera based upon an interline transfer CCD offers 10 microsecond shuttering capability, 10 bit gray scale and on-board memory to capture up to 1000 frames of data.

Since SMD has already demonstrated the ability to design and build high speed interline CCD cameras, the extension to a larger format is the lowest risk path to delivery of a functional 2Kx2K camera at 200 FPS. The paragraphs below summarize some of the key operating parameters of the proposed interline transfer approach.

6.0 GENERAL ARCHITECTURE

The proposed interline CCD architecture is shown schematically below. 32 channels are shown in total with one half of the imager tiles reading out to the left and the other 16 tiles reading out to the right. Each tile is essentially a 128x1024 imager which is running synchronously with the other 31 imager sections. Each of the output structures consist of a floating diffusion sense node buffered by a two-stage source follower.

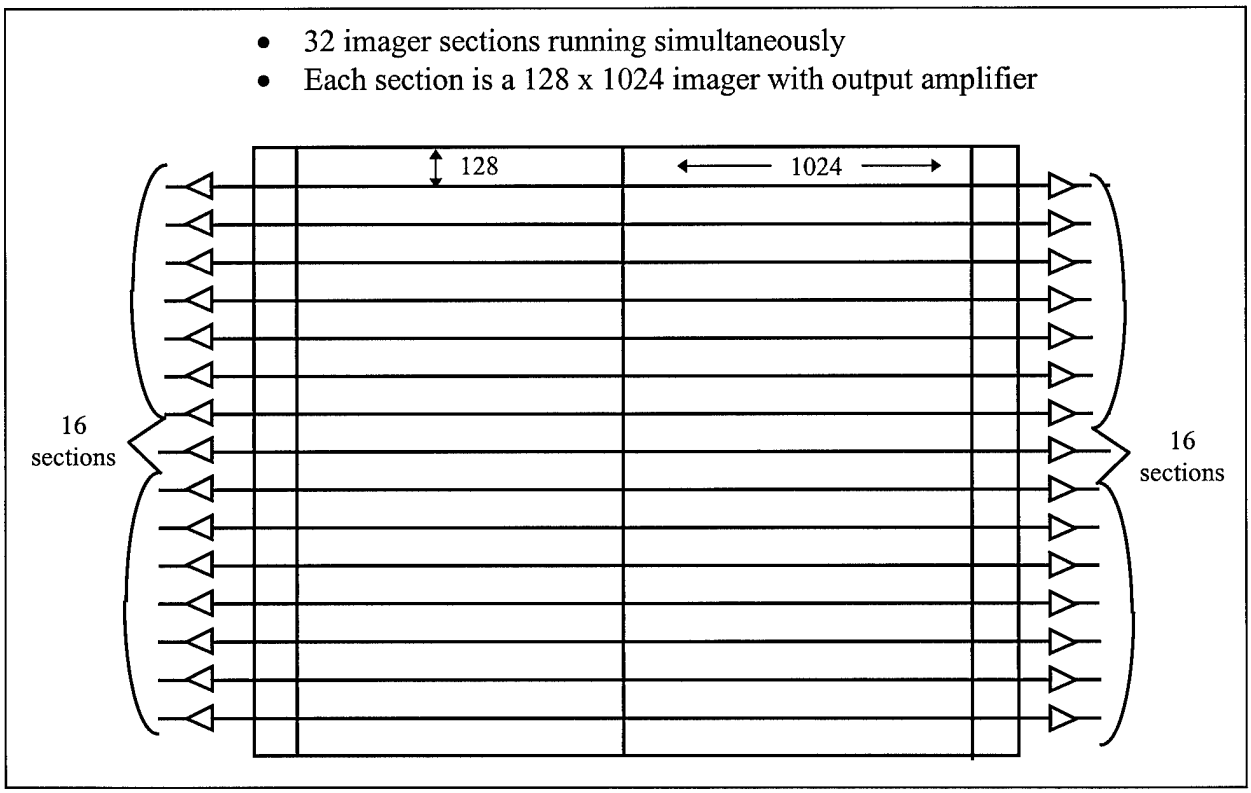


Figure 5. General imager architecture.

6.1 Composite Data Rate

At 2K x 2K, 200 FPS, the composite data rate from the imager is 840 MP/sec. The imager is designed as a split frame interline transfer architecture to minimize blur, and has a minimum vertical clock frequency of about 250 KHz. The interline architecture will allow for 100% integration time with on-chip electronics shutter speeds of down to 10 microseconds.

6.2 Number of Output Ports Required and Channel Data Rate

The data rate per channel is limited first by availability of mass memory systems. A large, high speed memory system developed by SPEC Corporation is capable of handling up to 32 Mpixels/sec on 32 independent channels. With timing overhead for vertical and horizontal syncs, this means that the effective data rate on each of the 32 data channels will be 27MP/sec. At this rate, the imager will provide up to 205 frames per second of 10 bit data. A typical problem in multiport imagers is the existence of a shaded line between each of the imager tiles. This line is due to limited bandwidth in the imager's output amplifier and is most apparent when the imager illuminated with a relatively bright background. The dark line typically seen stems from the fact that the imager's video output must transition from black (prescan data) to full white (full scale) in less than one pixel time. The same problem exists in single port imagers, however, the dark line is present only at one edge of the imager and is not typically noticed. The solution to he problem is to design the output amplifier so that the analog bandwidth is at least five times the required pixel rate. This additional bandwidth allows the amplifier to reach its final value and settle before the video is sampled. A schematic diagram of the proposed amplifier and its spectral bandwidth is shown in Figures 6, 7, and 8.

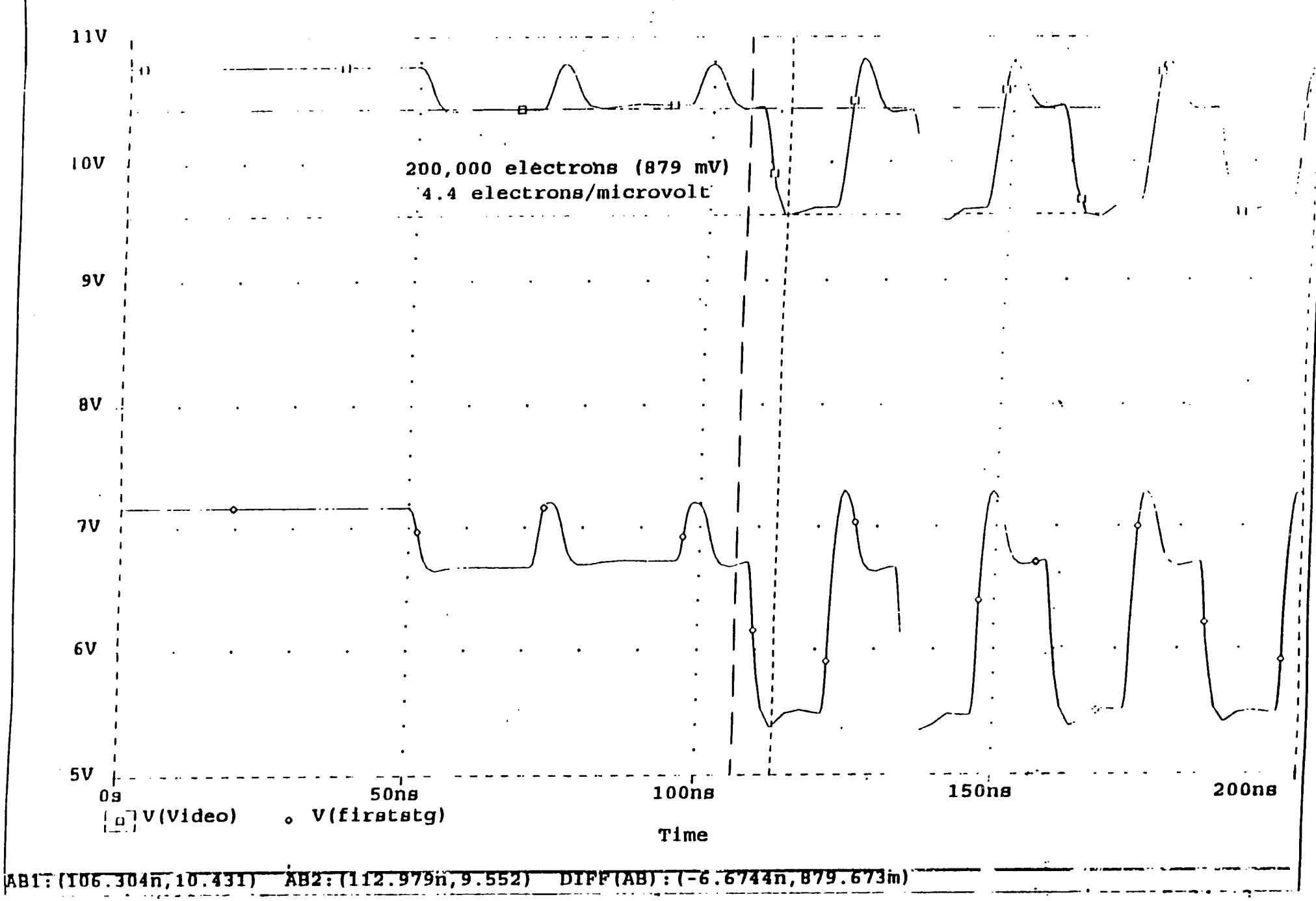


Figure 6. Simulated video output from wideband amplifier

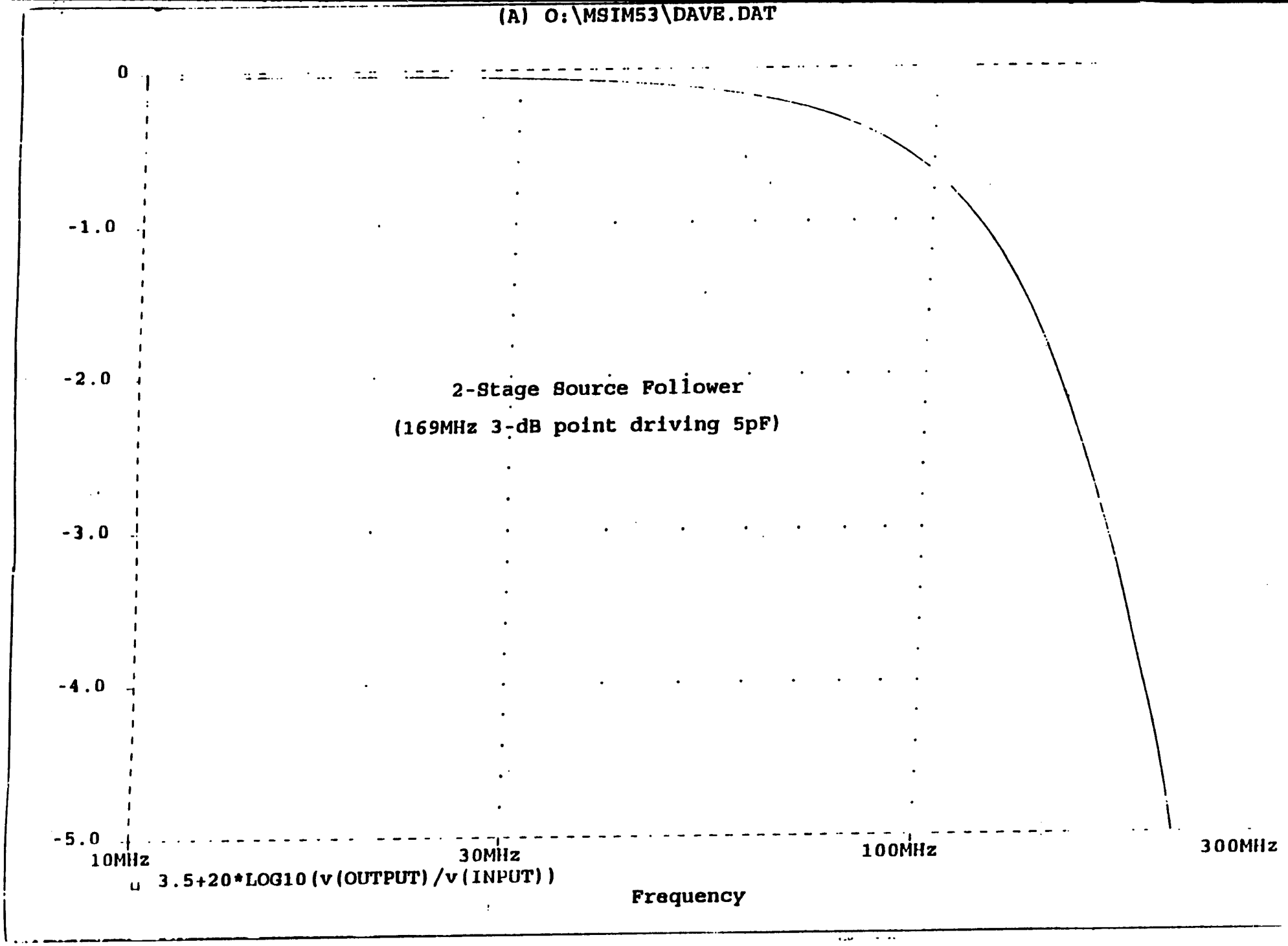


Figure 7. 2-Stage source follower

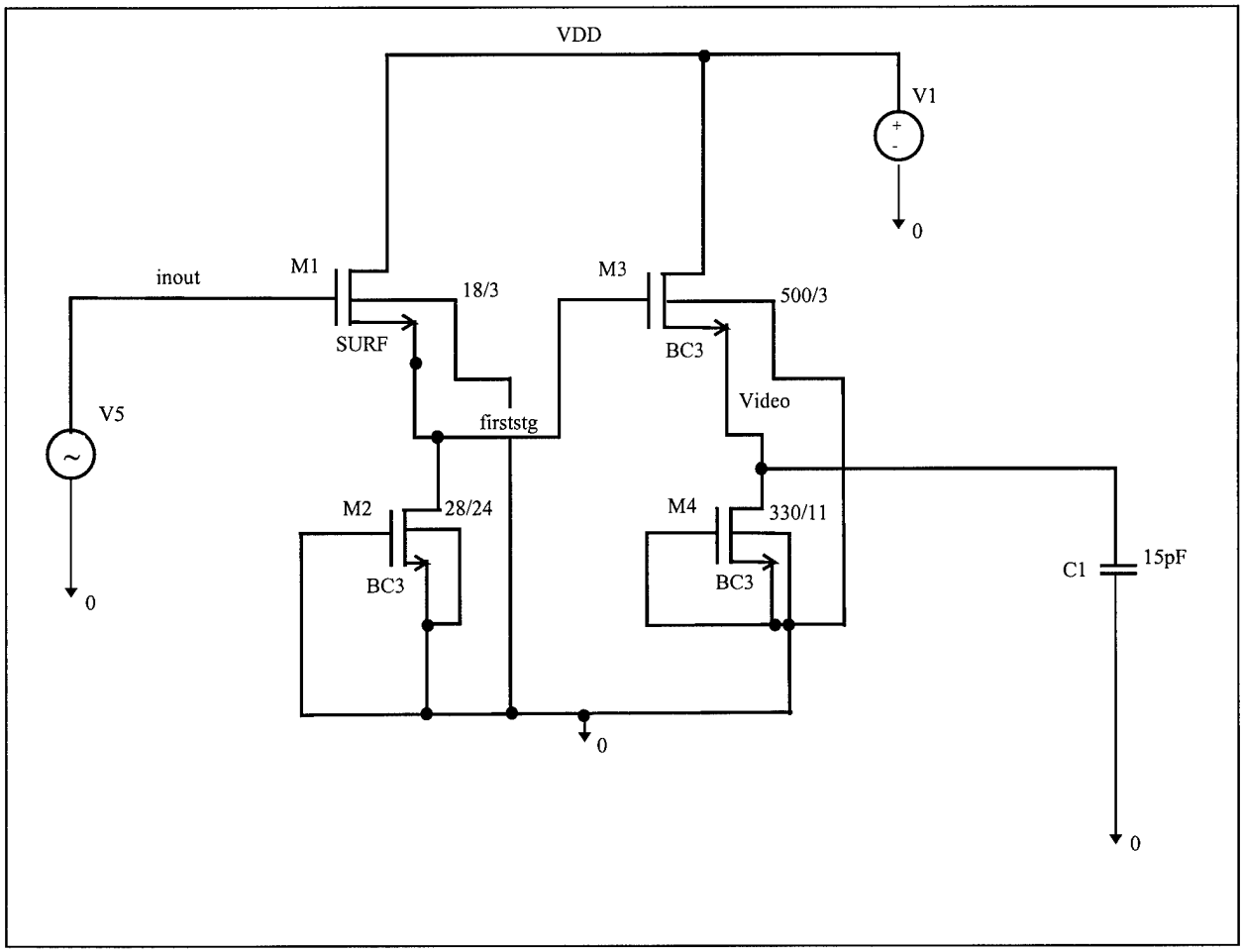


Figure 8. Double source follower AMP.

6.3 Approximate Chip Power

Assuming 200 FPS operation the total chip power will be given approximately by the sum of the vertical gate (CV2f) dissipation and the output amplifier quiescent dissipation. Assuming 8 Volt drive, and a total vertical gate capacitance of 180,000pf, the gate drive power will be 2.88 watts. It is reasonable to assume a power dissipation of at least 100mW per amplifier for a total amplifier dissipation of 3.2 watts. This brings the total power dissipation up to about 6 watts.

6.4 Shuttering

On chip electronics shuttering on the interline transfer architecture is anticipated to be on the order of 10 microseconds.

6.5 Cabling

The imager output must be digitized within the imager head. This means that for 10 bits, a total of 320 signals will be transmitted at high speed to the host memory.

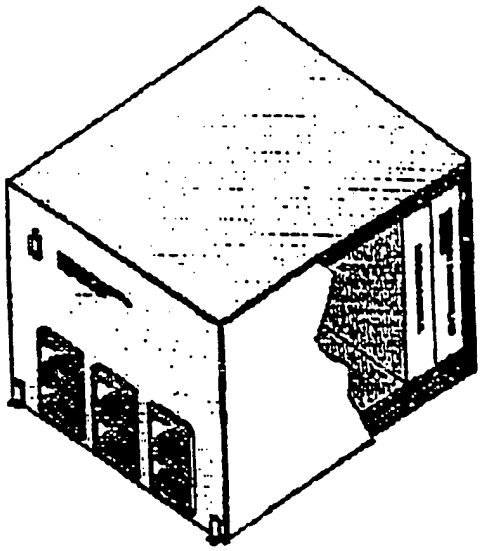
6.6 Data Compression

Because of the nature of the imaging at White Sands, it was decided that only lossless compression was acceptable. Several lossless algorithms exist ranging widely in their complexity. Frame to frame temporal compression was considered because it offers a high level of compression, and can be accomplished in a lossless manner. However, the use of temporal redundancy to compress data is extremely sensitive to noise and may result in significant artifact. The most practical compression scheme for this application appear to be simple intraframe compression which offers a lossless compression of about 3:1.

6.7 Memory

The new high speed camera will be designed to operate in either of two modes. For camera demonstration purposes, 250 frames of solid state memory will be integrated into the camera itself. The proposed Phase II camera will be delivered to White Sands with 250 frames of on-board memory for concept verification, and will be designed so that it can be interfaced to larger memory systems such as the SPEC "Python" (see attached memory specification). During Phase I, SMD contacted various vendors in the area of large, high-speed memory including Storage Tec and Walt Disney Imaging. While several vendors seem to have a viable solution, the least expensive and most directly compatible is the SPEC Python. The Python is equipped with n board lossless data compression providing 2:1 compression.

The SPEC memory system may be integrated to the camera via cable connection to provide up to 48 Gbytes of total storage. SMD will work with SPEC and other vendors of high-speed, high-capacity memory systems during the Phase II effort to provide a simple path for future memory upgrades.



FEATURES:

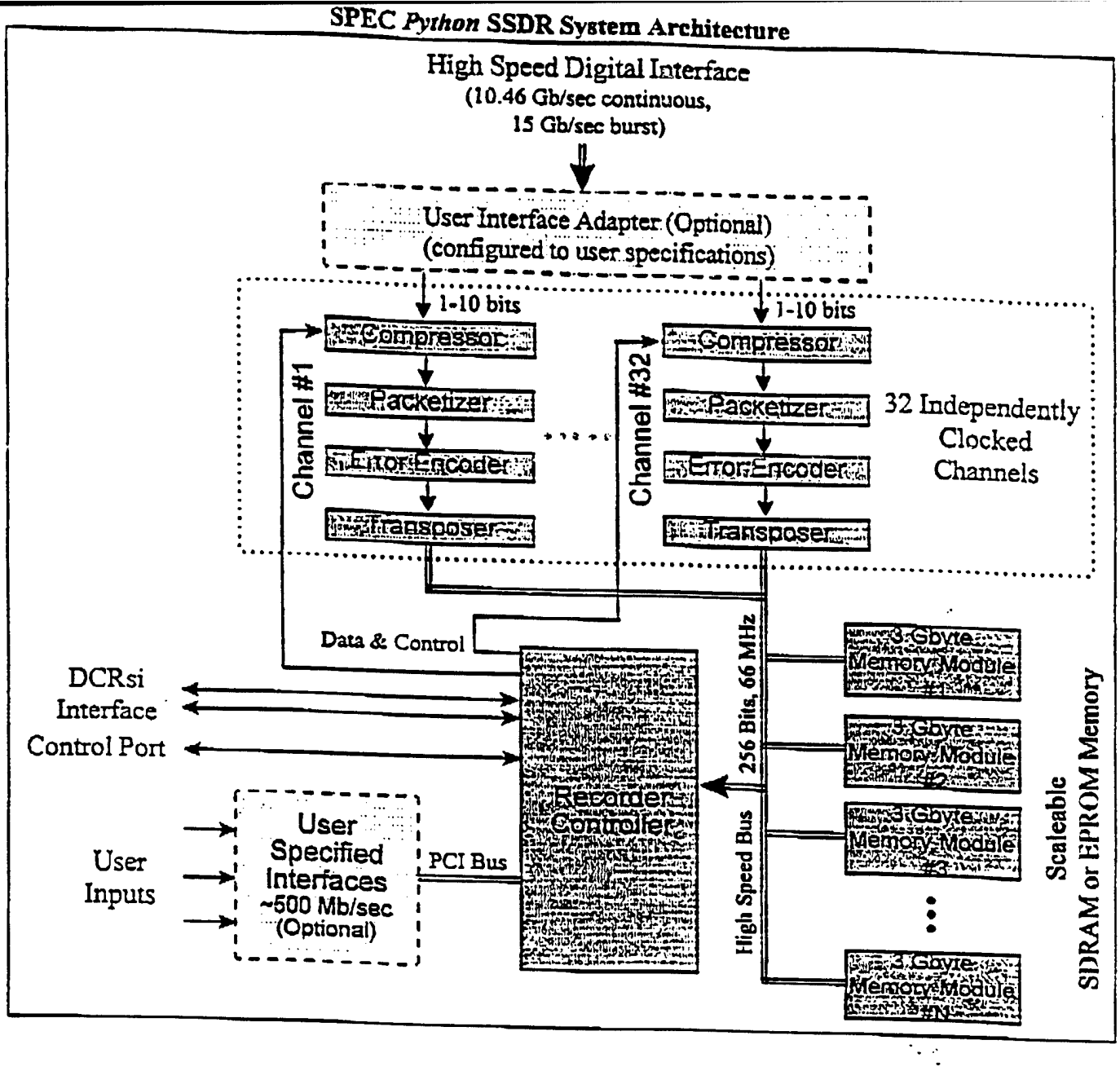
- High speed video or digital data inputs
- 15 Gbit/sec input burst data rate
- 10.46 Gbit/sec continuous data rate
- Over 48 Gbytes or data storage
- 3 Bbyte memory upgrade modules
- Lossless data compression to reduce memory cost over 2:1
- 32 independent input channels
- Optional user definable interfaces
- Data packetization and time stamps
- Proprietary error encoding architecture for robust fault tolerance
- Solid state reliability
- Reduced size, weight and power

DESCRIPTION:

Systems & Processes Engineering Corporation's (SPEC's) *Python* series Solid State Data Recorder (SSDR) offers significant performance improvements over conventional data recorders for both digital video and data storage. SPEC's SSDR provides for capture of data rates up to 15 giga bits per second with storage capacities in excess of 48 giga bytes. Additionally, the use of high density solid state memory offers improved reliability over mechanical tape based recorders while simultaneously reducing size, weight and power consumption.

Tape based data recorders designed for ruddedized use are limited by tape recording rates in the 30 to 400 mega bit per second range. These rates do not come close to accomodating today's requirements for high speed instrumentation data or high resolution, high frame rate digital video data recording. Digital video cameras can provide data rates in excess of 10 giga bits per second. As new high speed video cameras proliferate the instrumentation market, high data rate recorders are required to meet the new recording demands. Additionally, mechanical tape based recorders have limited temperature and vibration performance as well as excessive size and weight. SPEC is addressing these user demands and current product shortfalls by leading the way in high speed ruggedized recorder products.

SPEC's *Python* SSDR design employs state-of-the-art solid state memory devices combined with a proprietary high speed internal bus structure. To greatly reduce the product price, SPEC has designed and developed its own proprietary data compression Application Specific Integrated Circuit (ASIC) that reduces physical memory storage requirements by over a factor of two without loss of data. Data reliability has been a key focus and Reed Solomon error encoding and a proprietary internal data distribution technique allows for multiple memory component failures without the loss of a single bit of data. SPEC's *Python* SSDR is fully compatible with existing recorder support equipment by implementing the defacto "industry standard" DCRsi input/output interface for moderate data rates (~300 mega bits per second) in addition to the high speed interface. The modular design allows for customization of data inputs, outputs and memor configurations at minimal cost to the user.



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fax: 512-327-5487

TOTAL P.04

7.0 PROPOSED PHASE II DEVELOPMENT PLAN

The following technical objectives will be pursued during the Phase II development. A detailed development plan will be presented in the Phase II proposal.

1. Design and fabricate 2048x2048 CCD sensor. This objective represents the modeling, design, layout, mask generation and foundry fabrication of the 2048 x 2048 sensor.

2. Design and fabricate sensor support electronics. This will entail integration of the optics, control circuitry, memory and mechanical packaging of the imaging system. Following integration, the imaging system will be evaluated according to the prescribed specification. SMD has a fully equipped optics and electronics lab to facilitate the testing process.

3. Integrate and test camera system. Independent test of the camera and sensor array will be followed by integration and final test. Camera testing will include processing functionality, frame rate, dynamic range, modulation transfer functions and quantum efficiency.

4. Refine design. It is anticipated that two design and fabrication cycles will be required to optimize sensor and camera performance. Risk in each design cycle will be minimized through the use of multiple experimental camera test circuits and on-chip process verification structures.

5. Deliver and demonstrate system. Following thorough testing, SMD will have as a target to deliver and demonstrate the completed camera systems to the Army along with appropriate documentation and operation manuals. Three complete cameras are targeted to be developed and delivered under this contract.

6. Maintain open communications with the Army. It is important to maintain an open communications path between the Army and SMD in order to keep Army technical personnel informed on technical progress and to insure a final implementation which is of maximum utility. This will be accomplished through written reports, presentations and routine telephone conversations.

8.0 COMMERCIALIZATION STRATEGY

SMD was formed to commercialize and is very proud of its record in commercializing the technologies evolving out of SBIR projects. SMD has obtained almost one million of follow-on funding and other support from commercial companies including Teledyne, Roche and Thomson. SMD has developed world-wide marketing and distribution relationships, and is now marketing a line of high performance cameras including:

- The ***SMD-MACH I***, a 1,000 frame per second 512x512 pixel camera with 8-bit gray scale

- The **SMD-1M60**, a 1Kx1K pixel camera with 12-bit gray scale which is particularly useful for medical radiography.
- The **SMD-4M15**, a 2Kx2K, 15 frame per second, 12 bit camera geared towards industrial inspection
- The **SMD-64K1M**, a 1 million frame per second camera capable of capturing up to 16 images with 12 bit gray scale

SMD has attended various trade shows and is presently negotiating with companies including ADI, Inc., InfiMed, Thomson, Siemens Medical Systems and Hewlett-Packard in connection with commercial and Government manufacturing and supply.

SMD's successful record of commercializing SBIR technologies was recently recognized by the Federal Government. SMD was awarded the "Industrial/Manufacturing SBIR Technology of the Year Award" at the 1995 Technology-2005 Conference in Chicago. SMD was also awarded the Grand Prize SBIR technology of the Year Award in 1996 for the development of a 1 million frame per second camera under an Air Force Phase I SBIR. Selection for these awards are based upon a combination of technical merit and successful commercialization of the technology.

SMD will apply these aggressive commercialization strategies to the ultrafast CCD imagers developed under this contract. Concurrently with demonstrating feasibility and filing one or more patent applications (to facilitate working with third parties), SMD will aggressively seek to develop markets in the areas of particle physics, high speed chemical physics, high resolution long range reconnaissance, optical diagnostics in combustion flow fields in the automotive and aerospace industries, and high speed optical pattern/target recognition. SMD will also plan to manufacture and market its own products in the commercial and military markets.