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FINAL TECHNICAL REPORT

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1. Phase I Program Goals

The main goals of our program can be summarized as follows:

- To design and build a helmet-mounted display with commercially available components in order to demonstrate the proposed dual-insertion-display concept which will provide a very large field of view (FOV image).

- To design and layout silicon-on-sapphire circuits which will be used in the Phase II work.

- To examine the issues associated with the wireless communication of images.

The goal of the Phase II program is to replace the commercially available low-resolution displays of the Phase I HMD prototype with ultrathin-silicon-on-sapphire based active matrix addressed liquid crystal displays (AMLCDs). As explained in the following sections of the proposal, the use of ultrathin silicon-on-sapphire (UTSOS) technology provides some fundamental advantages which gives us the technological edge when competing with other display companies such as Kopin. The final HMD will receive image data via wireless transmission channels. Color will be generated using Textronix color shutters.

2. The Phase I HMD prototype

Figure 1 illustrates the Phase I prototype. In our approach, two displays per eye have been utilized. The reason for the dual display approach is very simple: The human eye is most sensitive to the resolution of an image when the image is right in front of the eye (foveal vision). On the other hand, displays will not furnish high-resolution image information to the fovea when the user "peers" at the edge of the display (using the rotation of the eye in its socket). Therefore, use of high resolution images for peripheral vision can be regarded as an "inefficient use of display resolution" as the human eye is insensitive to large number of pixel counts in that area. This is where our dual-display approach plays an important role by optimizing the resolution vs. viewing angle.

As can be seen from Figure 1, LCD2 is used to create a high-resolution image right in front of the users eye where it is most needed. In contrast to the first display, the second display LCD1 is projected over a larger viewing angle which results in a fewer number of pixels per viewing angle. However, most of the LCD1 image is projected to the areas where peripheral vision dominates, and therefore loss of resolution in that area does not seriously effect the image quality. The end result is an optimized blending of the two images where the best of the two worlds is combined: high resolution for foveal vision, and large viewing angle for peripheral vision. This "insertion-display" approach will create a more friendly environment compared to the other approaches where multiple displays are tiled up in front of the user eye.

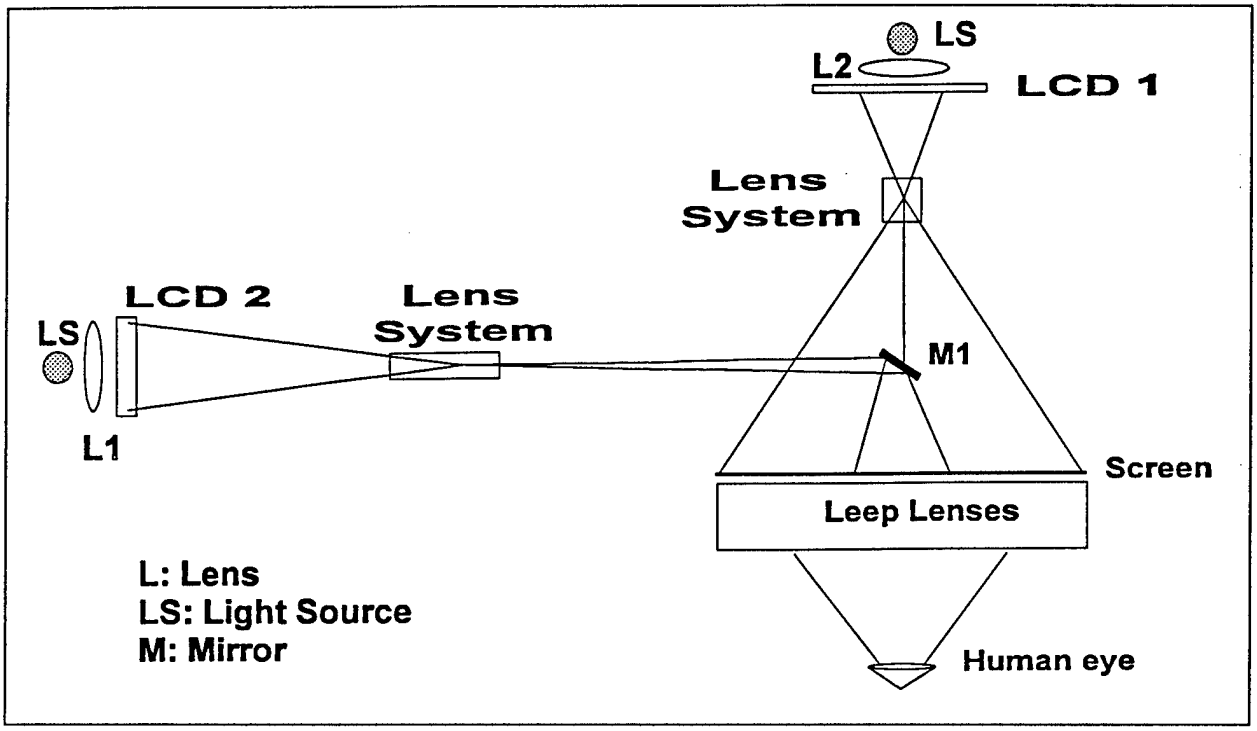


Figure 1. Illustration of the dual display approach.

2.1. The Dual Resolution Demonstration Platform (DRDP)

The Dual Resolution Demonstration Platform (DRDP) comprises a hand held viewer for the right eye, and a two-camera signal source, both connected by cable to a separate power unit. The photograph of the dual display system for the right eye is shown Figure 2.a. The unit is 4"x2"x15" and weighs less than quarter of a pound. The signal source, which can be seen in Figure 2.b, can be physically attached to the viewer, so the effect during scanning of accurate coupling of the image source and the viewer image can be evaluated, or the two may be separated, giving a more realistic sense of the weight and bulk of the viewer by itself. The signal source consists of four miniature cameras (two per eye). Each camera provides the signals for the insertion as well as the wide angle display for the right and left eyes of the HMD.

The DRDP viewer uses a LEEP wide angle lens system giving a 70 degree field from center to right. The field to the left is somewhat less (depending on elevation, because part of the lens is cut away to make room for the nose of the person viewing). Two rear projection systems place the real images from two small LCDs in the object plane of the LEEP optics. One fills the object plane (except for a small part at the top and the bottom) with the image from a wide-angle LCD, which gets a video signal from a video camera with matching wide angle lens on the signal source. The other projection system projects the image of an LCD having an image from a camera with a telephoto lens. The image is projected via a small 45 degree mirror to the center of the large image, where, because of its much narrower field (approximately 25 degrees) it provides a sharp central image for detailed viewing.

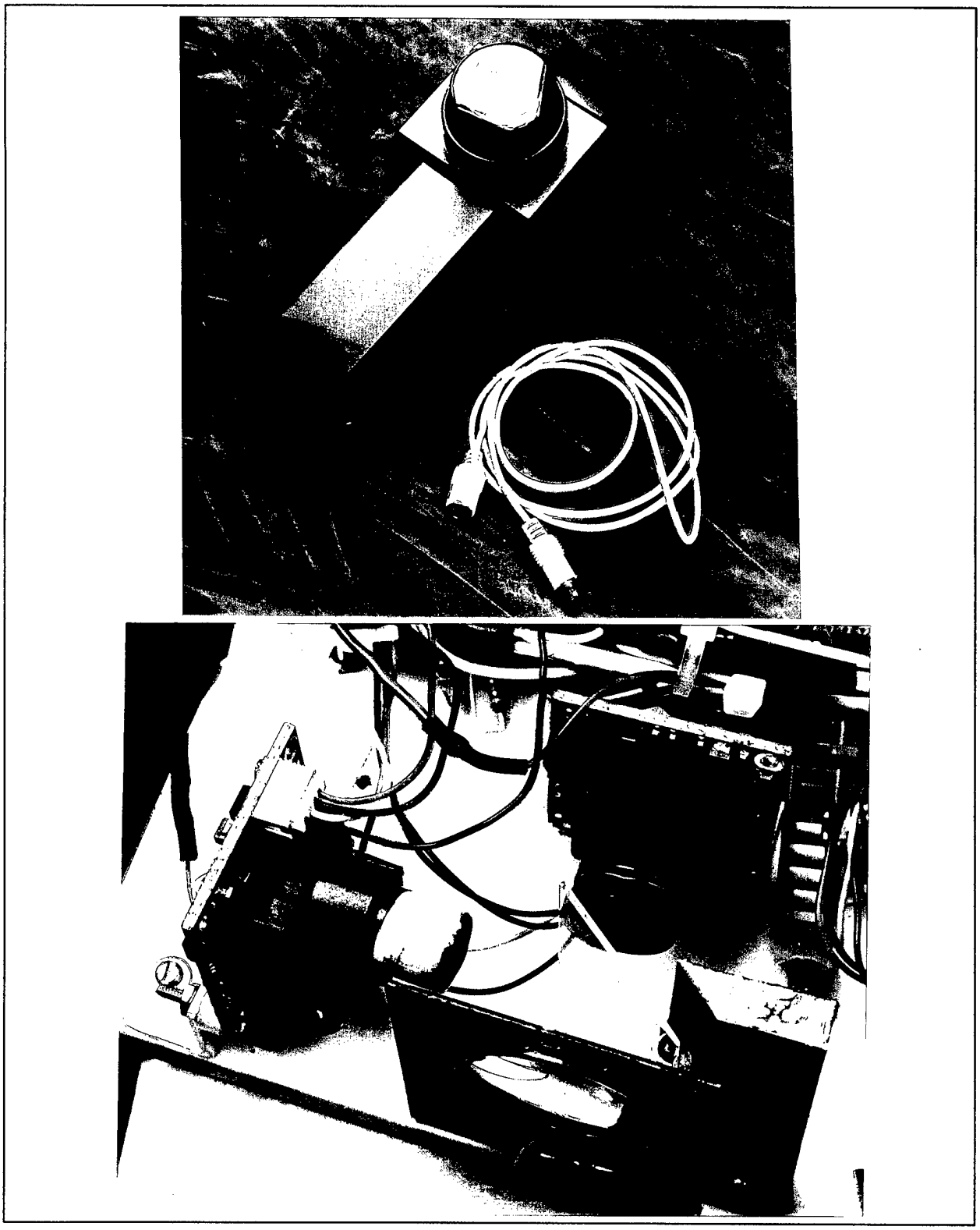


Figure 2. The photograph of the Phase I prototype (a) the right-eye channel of the HMD utilizing two displays, (b) the signal source for the HMD; the miniature cameras are less than 1" in length.

The DRDP is constructed of vacuum-formed ABS and 50 percent PVC foam, with a few critical pieces from solid PVC. This construction makes the assembly rugged and reasonably light. Assembly is mostly by solvent welding except where screws are required for assembly and cleaning.

The LCDs used in the DRDP are readily available units from SONY. They are used as monitors for video cameras and have rather low resolution (315 by 109 pixels) and bulky drive circuitry. These drawbacks will be largely eliminated by the higher resolution SOS units with integral drivers that OPTRON plans to demonstrate using the DRDP.

Significant DRDP Components (omitting materials, cables, connectors, assembly hardware, etc.) are listed below by Vendor.

LEEP SYSTEMS, INC.

ARV-1 three element Virtual Reality optical system (one eye only - modified for this application)

NAS-1 Dual Camera Experimental Video Platform

NAS-1 Utility Power Source

EDMUND SCIENTIFIC CO.

Cat # 40874 8mm zoom projection lens (in new barrel),

Cat # 32944 round front surface mirror (ground to shape),

Cat # 43023 aspheric Fresnel condenser lens 15mm f.l. 2 each,

Cat # 44684 Fresnel field lens 5" f.l,

Cat # 32317 achromatic lens 50 mm f.l., Cat #37756 heat shield

MILLES GRIOT: Condenser lens Cat B-1059 12 mm f.l.

NASHUA CORPORATION: Experimental Depixillation Film

SONY: Model XC-M07 Color Video Monitor (modified) 2 each

WELSH ALLYN: Miniature lamp type 01213, 2 each

2.2. Evaluation of the DRDP

We have built the right eye channel of the HMD to evaluate the human related factors of the insertion display concept. The initial results are very encouraging. The blending of the two display images has been successfully accomplished. Actually, it was very difficult for the viewer to see the line separating the two images. In some cases, when the viewer was not warned, he could not tell there were two separate images projected into the eye. However, we severely suffered from the low resolution of the Sony displays. Especially, in the case of the peripheral image, where the display is projected over a larger area, individual pixels are easily visible to the viewer. This "pixelation" of the image is really bothering, and it is the biggest obstacle preventing us from creating a 3-D VR environment. We believe that this problem will

be eliminated with the availability of high-resolution UTSOS based displays. Also, our UTSOS displays will be 36 mm by 30 mm, almost four times the area of the current Sony displays we use. The larger size will not only simplify the optics of the HMD, it will also help to create a more realistic VR environment.

3. Silicon-on-Sapphire Circuits

During the course of the Phase I program, we have been in touch with NRAD, San Diego, CA. NRAD is the Navy Research and Development Laboratories from which the ultrathin-silicon-on-sapphire technology originated. As a first step in the Phase I program, they provided us with the SPICE simulation parameters of their UTSOS transistors for digital operation. These parameters will be extensively used for the design of the digital display driver circuits at the Phase II level.

As a result of the extensive discussions with NRAD, we decided to lower the pixel count of the display from 1600x1280 down to 1280x1024 in the Phase II program. There are various reasons for this change:

- The yield of a very large display chip is the most critical issue. Even the 1280x1024 chip is larger than Intel's Pentium (36 mm by 30 mm). Considering the limited budget of a Phase II program, we decided to lower the pixel count in order to demonstrate a successful prototype. Also, even the reduced resolution of 1280x1024 can be considered as a very high resolution for many applications.
- The lower resolution also reduces the requirements on the wireless communication equipment and channels. As will be explained in Section C.3, the lack of commercially available wireless communication equipment for very high resolution images will force us to design custom-made hardware. The lower pixel count will also help us in the design of such hardware.
- We have found a very significant commercial interest from a projection display company, Proxima, San Diego, CA, for a 1280x1024 monochromatic display (please see Attachment I). Such a demand by a large company will speed up the transition of our Phase II results into the commercial markets.

3.1. The Architecture of the Digital Display Chip

The architecture of the proposed 1280x1024 display chip can be seen in Figure 3. The digital data can have as many as 8 bits per color. We have shown 4 bits only in the figure for the sake of simplicity. Each bit is the input to a shift register array. At any given time, only one of the input bits can have a value of logic 1. Once all the shift registers are scanned, the stored information in the shift registers is evaluated, and one of the four voltage levels is written into the corresponding pixel of each row. Each frame is written by scanning the entire set of rows of the display.

The heart of any self-scanning display circuits is the shift register array. Several issues are important in the design of a shift register array:

- Each shift register should draw a minimum current.

- Ground and supply lines to the array should be refreshed regularly to minimize the voltage drops in these lines.
- If possible, the array should be laid out without using second level of metal. This ensures later that more voltage is applied to the LC cell.
- A two-phase shift register is preferred as it is less susceptible to unwanted signal propagation.

Other critical circuits of the display chip are a two-phase non-overlapping clock generator, and a driver circuit which can drive the clock signal across the highly capacitive lines of the shift register array. Maybe, the most important component is the unit cell of the display chip. The unit cell is very similar in nature to a DRAM memory element. It consists of a pass transistor and a storage capacitor. The value of the storage capacitor is dictated by the leakage current of the pass transistors. In the case of UTSOS, p-channel transistors have less leakage currents than their n-channel counterparts (1 pA/μm for a two-micron channel length).

The unit pixel is illustrated in Figure 4. This unit-pixel is simply repeated in the x and y directions as many times as the array size (1280x1024 times in our case). The data lines are run in metal 1, whereas the select lines are run in poly. As these metal lines run across the entire chip which can be as large as 36x30 mm, it is important to know the exact capacitance of these lines. One can then tailor the size of the drivers which will charge and discharge these largely capacitive lines. For example, the capacitance of the data lines can be estimated as follows:

$$C_{line} = N_{hor} (C_{line} + C_{junction} + C_{LC})$$

where N_{hor} is the number of horizontal scan lines, $C_{junction}$ is the source/drain capacitance of the pixel transistor, C_{LC} is the capacitance of the LC layer within a pixel, C_{line} is the capacitance of the metal line in a unit pixel. It has several components:

$$C_{line} = C_{line\text{-}to\text{-}substrate} + C_{line\text{-}to\text{-}line} + C_{line\text{-}to\text{-}poly}$$

$C_{line\text{-}to\text{-}line}$ is the fringing field capacitance between the neighboring metal lines in an active array which is negligible for the geometries in a typical AMLCD display chip. Also, $C_{line\text{-}to\text{-}substrate}$ is zero due to the insulating nature of sapphire. Finally, $C_{line\text{-}to\text{-}poly}$ is the overlap capacitance of the data and poly select lines. If the corresponding values are put in the above equation, the line capacitance for a 1280x1024 driver is close to 7.5 pF. When the line drivers are designed, they should be able to charge and discharge this capacitance within the time frame allocated for the writing of a horizontal line (less than 13.5 μs).

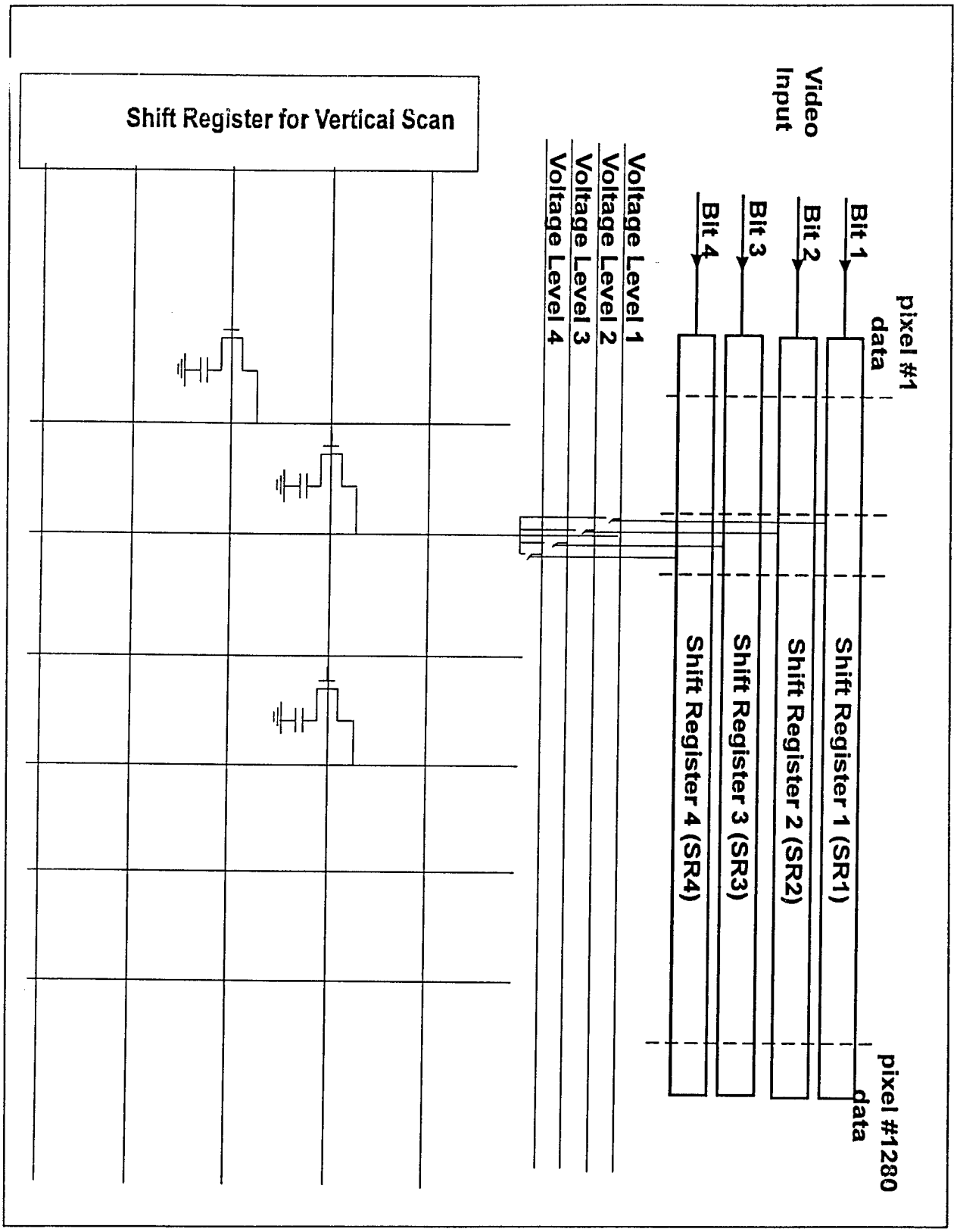


Figure 3. The architecture of the proposed 1280x1024 display chip.

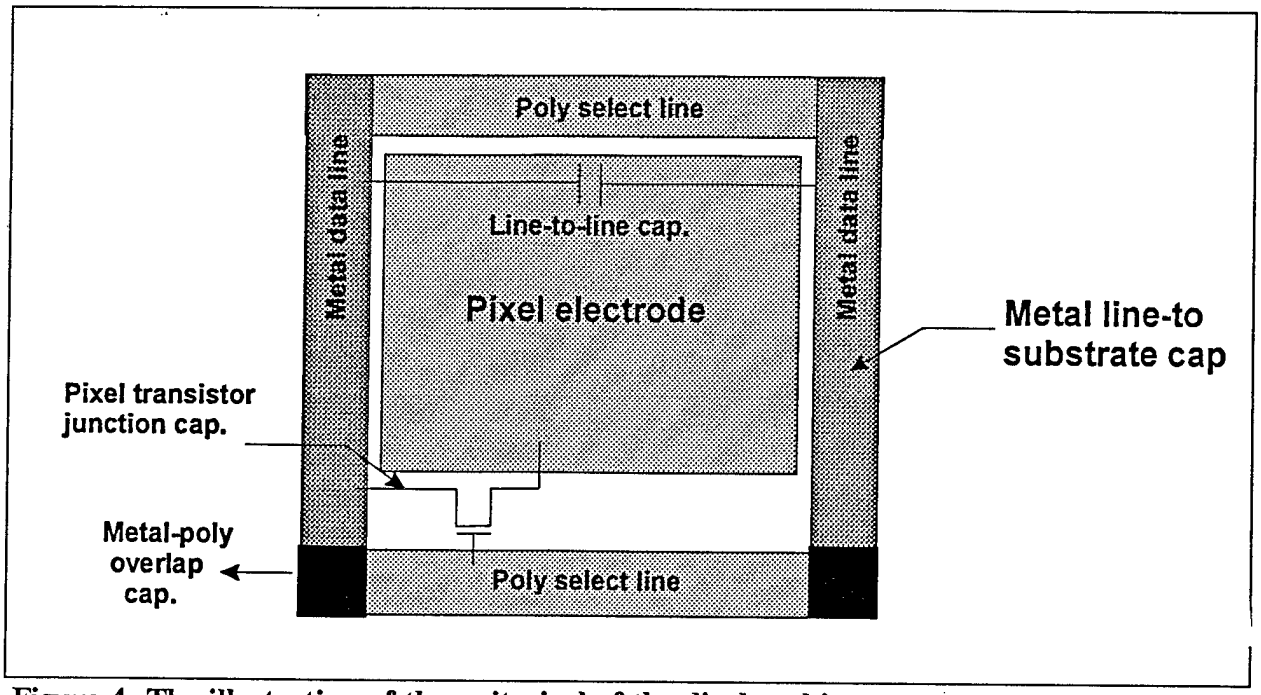
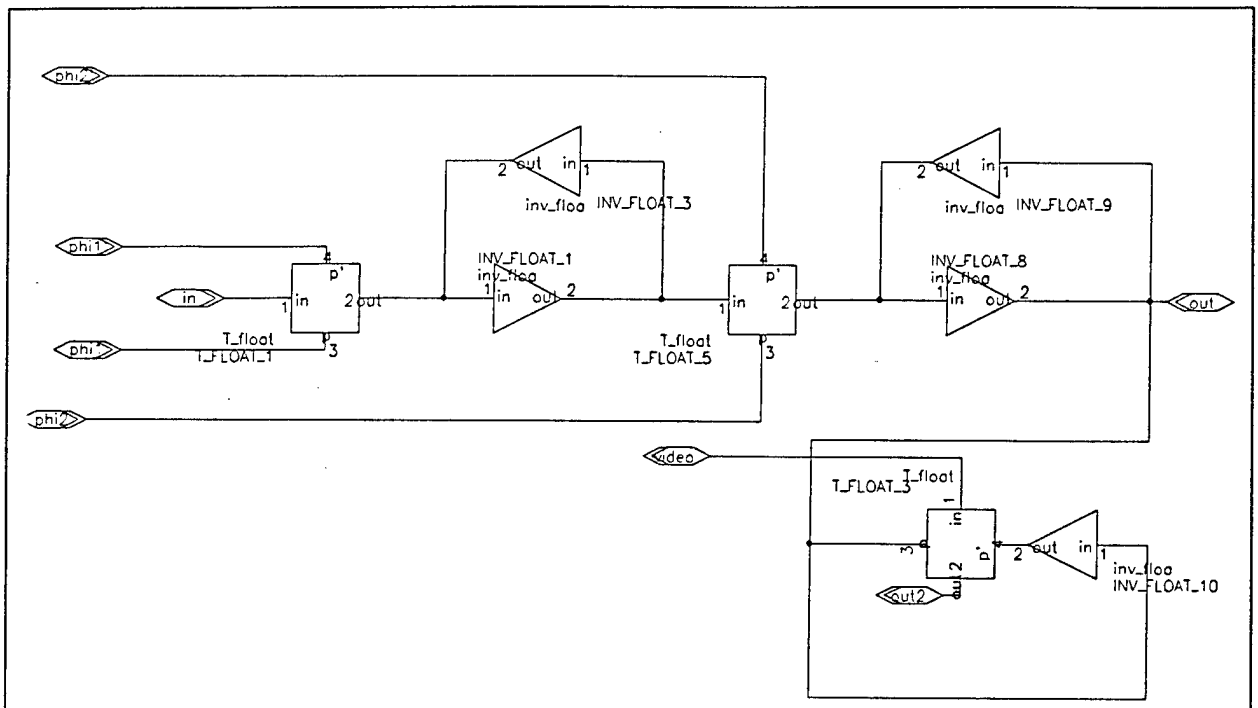


Figure 4. The illustration of the unit-pixel of the display chip.

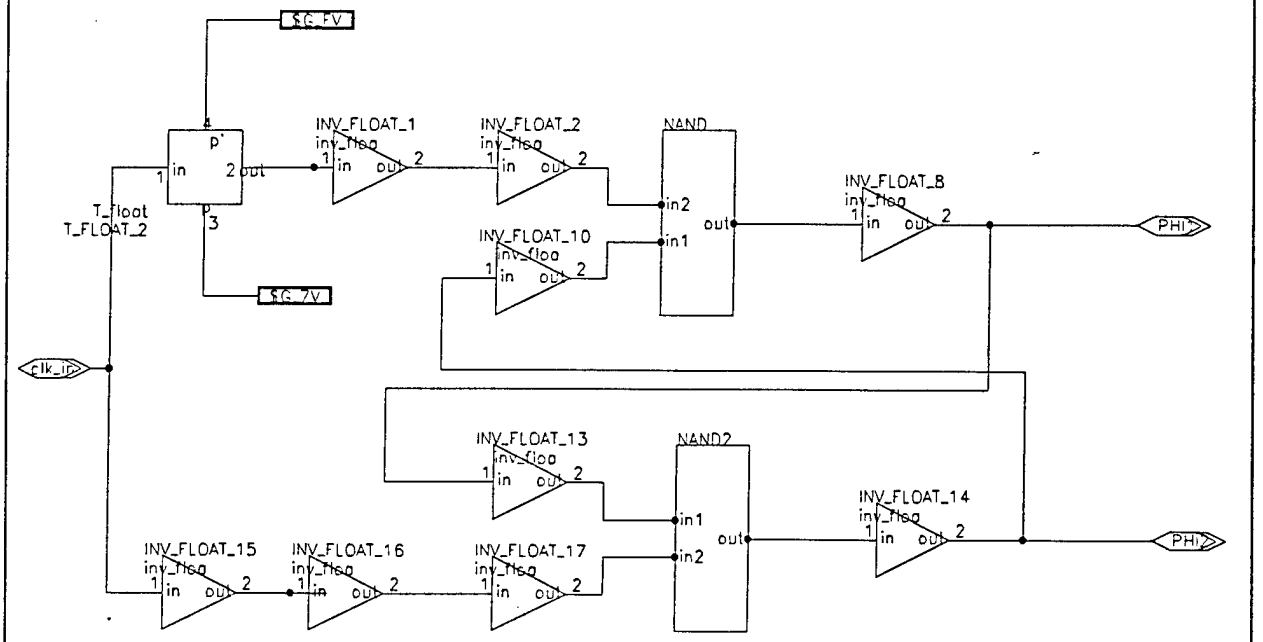
In the Phase I work, we simulated and laid out the following circuits of the display drivers:

- A two phase clock generator: This circuits takes an off-chip clock signal and creates two non-overlapping signals. These signals are used to drive the two-phase shift register array.
- Line drivers: As the shift register clock lines have large capacitance values, a buffer circuit needs to be used as the output of the clock generator. This buffer circuit should introduce the exact same amount of delay to the non-overlapping phases of the clock signal.
- Shift registers: These circuits are used to scan the display chip in the horizontal as well as vertical directions.
- Unit cell: A pitch size of 12 microns was used in the layout of the unit cell.

Figure 5.a. illustrates the schematics of the shift register for the horizontal scan circuits. Figure 5.b is the schematics of the two phase non-overlapping clock generator.



5 a.



5 b.

Figure 5 The schematics of the (a) shift register for the horizontal scanners, (b) two phase non-overlapping clock generator.

3.2. Negotiations with David Sarnoff Research Center

During the course of the Phase I program, we had intensive negotiations with David Sarnoff Research Center. They are one of the leading companies in the design of AMLCD displays. In the past, they designed several high resolution displays for other government funded R&D programs. Although we designed and laid out all the circuits which are necessary for a digital display, we decided to subcontract the design of the display to David Sarnoff in our Phase II program. The reason for this major decision is for the sake of immediate transition of UTSOS technology to commercial display markets. If we were to proceed with our own design at the Phase II level, it would have certain limitations which might prevent us from aggressively entering the display market. On the other hand, David Sarnoff's past designs are already commercially available. If they modify their existing designs to accommodate our UTSOS process, we would significantly increase our chances of having a commercial product at the end of the Phase II program, and we would also be spending the government research funds in the most efficient way.

4. Wireless Communications

A 1280x1024 image is typically represented with 24 color bits (8 bits per red, green and blue colors, respectively). If one wants to send 30 images per second, the total number of bits, N_{total} corresponds to:

$$N_{total} = 1280 \times 1024 \times 24 \times 30 = 944 \text{ Mbit}$$

A good compression algorithm is needed in order to minimize the number of bits one needs to send high resolution pictures over the transmission channel. In 1990's digital video and image compression standards were developed. These standards provide efficient use of the communication channel's capacity. A 1280x1024 image can be compressed to 1 bit/pixel without introducing any visual degradation by the JPEG standard. This is equivalent to a Compression Ratio (CR) of 24. Recently developed wavelet transform based image coding techniques can achieve higher compression ratios such as 40 to 1. In digital video even higher CR's can be obtained by exploiting the similarity of consecutive video frames.

JPEG Standard: JPEG stands for ``Joint Photographic Experts' Group''. This is a transform domain image compression technique. In this algorithm, the image is divided into small pixel blocks of size 8 by 8 or 16 by 16 and each block is transformed into another domain by Discrete Cosine Transform (DCT) which is a transform similar to the Discrete Fourier Transform (DFT). In a small block the pixel values are highly correlated with each other. The DCT takes advantage of this fact and decorrelates the pixel values. In this way the redundant information within a block is removed by the DCT. The transform domain coefficients are quantized and encoded into a bit stream by Hufmann coding or arithmetic coding. In the receiver inverse DCT of the quantized coefficients are computed to reconstruct the pixel block. The JPEG algorithm has a poor performance in the blocks containing edges (less correlation among the pixel values) and continuity among the pixel blocks cannot be achieved at low CR values. VLSI implementation of DCT is possible, and DCT chips have been available since late 1980's. Several US companies offer JPEG compression hardware as well Wavelet based Image Compression: Wavelets are probably be the basis of the next generation image

compression standards. Currently AWARE, Inc., MA offers wavelet based image and video compression hardware which produces higher compression ratios in most images and video.

CELP-based Image Coding: Code Excited Linear Prediction (CELP) is a speech compression algorithm. DoD standard 4016 operating at 4.8 kbits/sec is a CELP based technique. The CELP algorithm has recently been used to compress images as well. The two-dimensional image matrix is first scanned to a one-dimensional stream of numbers and then fed to the CELP algorithm. In this way a CR of 20 to 30 can be achieved for color images. A 1K by 1K color image can be transmitted to a soldier in the field in about two minutes (120 sec= 1000*1000*24/(4800*(CR=30))) with a 4.8 kbit/sec channel [1]. The transmission time can be further reduced with higher rate channels. An advantage of this technique is that it almost requires no extra hardware (except the scanning system and a larger codebook for the CELP), if the soldier has a DoD-4016 based hand held radio receiver.

MPEG Video Coding Standard: MPEG stands for Motion Picture Expert Group. MPEG-I and MPEG-II video coding standards are based on DCT and motion compensation. A video signal is basically a sequence of images. In the MPEG algorithms first a reference image frame from the sequence is compressed similar to the JPEG algorithm and sent to the receiver. Since the next image frame is quite similar to the current frame in a typical video sequence there is no need to transmit the whole frame. Only differences which correspond to the moving objects are encoded and transmitted to the receiver. After four frames another reference frame is compressed and transmitted and the above procedure is cyclically repeated. MPEG-II standard will be used in the forthcoming HDTV standard as well. A high resolution video signal can be compressed to 5 to 10 Mbits/sec (1000*1000*24*30/100 = 7.2 Mbit/sec) using the MPEG-II algorithm and the CR ranges from 50 to 150 for a typical video sequence.

At this point, MPEG seems to be the most suitable algorithm for the successful completion of our program. Also, the wide range of commercially available hardware is another important advantage for MPEG. However, we will also use CELP in our Phase II program as it allows the transfer of images through the use of existing audio channels. With a very minor modification to the soldier's existing wireless audio communication equipment, it is possible to send an image every two minutes which might be a desired feature for the Army as it does not necessitate any additional equipment to the soldier's existing electronic gear.

4.1. Wireless Digital Data Transmission

During the Phase I program, we also reviewed the commercially available equipment for wireless image transmission. We have found various vendors which provide wireless video transmission equipment. Optaphone, Spystuff, HDS Inc., Precision Solution, Prism Video, Southern California Microwave are some of the companies we have been in touch with to find out more on the commercially available wireless equipment. At the present time, to the best of our knowledge, there is no commercially available equipment for wireless transmission of a

[1] For a given perceptual quality, different images may yield different compression ratios. The higher the high frequency content of the image, the lower the CR

1280x1024 image. This is mostly due to the fact that the TV broadcasting is still done following the NTSC and PAL/SECAM standards and there is simply not any motivation from industry's point of view to manufacture and sell equipment which can handle higher resolutions. Although there are some equipment developed by the Grand Alliance companies under the high definition TV program, we do not believe that they will soon be available at a reasonable cost to the Army. During the Phase II program, we have several options to reach our program goals:

- We can convert a high resolution image to NTSC format and then broadcast it to the users. This is not a desirable solution as it would result in the loss of resolution when the image reaches the user.
- In the case of digital transmission, an image can be transmitted as a bit stream and stored in a memory on the user's end. Once the transmission of the entire image is complete, the image can be displayed on the high resolution screen. The disadvantage of this technique, is that it is limited to 5-20 frames per second.
- Finally, a custom-designed system can be built. Five MPEG cards can be combined to create a high resolution image. In this case, a digital-signal-processing (DSP) board should be used to synchronize all the MPEG cards with respect to each other. Initially, a personal or a lap-top computer needs to be used to control the entire system will make the system bulky. In the future, custom designed electronics can be tailored to make the system lighter in weight and more rugged for battlefield conditions. This system will be capable of handling 30 frames/second.

We will be following the second and third options in our Phase II work. The second option is very straightforward to implement whereas the combination of 5 MPEG cards is a more engineering-intensive task.

4.2. Image Sources and Driver Circuits

Another important issue is the lack of high resolution image sources. The most practical way of achieving such an image source is to use a personal computer which is equipped with a video generator card. Team Systems, Santa Clara, CA is one of the companies which provide such a PC compatible video card. Their model ASTRO VG-823 provides digital images with up to 1600x1280 pixels.

Honeywell is one of the leading companies in the design of image generators and drivers. In the past, they did manufacture the video drivers for the displays made by Kopin under other government funded research programs. Their drivers also provide all the timing signals which are necessary to scan the active matrix display array. As a result of our negotiations with Honeywell, they agreed to design and submit the video drivers we need in the Phase II program.

5. Summary and Conclusions

During the Phase I work, we not only accomplished important technical goals, we also developed very good relationships with some of the leading companies in the display community. We strongly believe that the team we put together for the Phase II work will enable us to make a rapid transition into the commercial markets.

The Phase I work demonstrated a first prototype of the insertion display concept for an HMD application. An image source platform with four miniature cameras was built in order to provide images to the displays of the HMD. One channel of the HMD was built and tested to see the effects of the insertion display concept. Our initial results are very encouraging. The blending of two display images in front of the user's eye has successfully been demonstrated. The dual display approach created a very large FOV (120 by 140 degrees) which is essential to create a 3-D environment. The prototype suffered from the low resolution of commercially available Sony display (320 by 240 pixels only). This problem will be eliminated when the proposed high resolution SOS displays become available.

With regard to silicon-on-sapphire circuit design, we have determined most of the critical circuit elements which are required in a digital display. SPICE simulations for these circuits were carried out, and most of the circuits were laid out. We also determined the architecture of the chip.

During the Phase I work, we had the opportunity to get in touch with David Sarnoff Research Center. Sarnoff has designed most of the display circuits in the past under different government funded programs. They developed active matrix array circuits for liquid crystal as well as electroluminescent films. Their latest design include a 1280x1024 and a 2560x 2096 display. As a result of negotiations with Sarnoff, we decided to use their 1280x1024 design in our Phase II work by modifying the design for ultrathin silicon on sapphire. This will not only provide us with a proven commercial design at the end of the Phase II work, it also makes the best use of government research funds. Please see Attachment II for the agreement we made with David Sarnoff.

Another important development of the Phase I work was the development of very promising relationship with a potential customer. Proxima Corporation, a San Diego based projection display company, showed great interest in the proposed UTSOS based LC display. They gave us a letter of support stating that they will be dedicating internal research funds (up to $1M) to develop a projection display system based on our proposed 1280x1024 display. Once the projection system is ready for commercial sales, they expect a volume of 3000-5000 displays per month from us (See Attachment 1).

For the purpose of wireless image transmission, various image compression algorithms have been examined. We will be utilizing CELP and MPEG in our Phase II work. CELP will enable us to use the existing audio equipment of the soldier's electronic gear. This is a simple and quick demonstration of wireless video images, and we should be able to transmit 1-30 frames per second to the soldier on the field using the existing audio transmission equipment. The frame count is a function of image complexity. Black and white images with no gray scale take far less bandwidth than color images with up to 8-bit gray scale for red, green and blue. Finally, we could not find any commercially available system which can be used for the transmission of color pictures at 30 frames/second. We will use a custom-made system consisting of four MPEG cards, a digital signal processor board, and a lap-top (or PC) computer in the Phase II work for this purpose.

Image sources for high resolution displays still seem to be a problem. For this purpose, we got in touch with Honeywell during the course of the Phase I work. Their expertise will be utilized in the Phase II work to create the image sources we need. They have been the major provider of image sources in other government funded display programs. Honeywell also expressed great interest in our program, as they see it vital to their own internal research program (Please see Attachment III). This is why they agreed to be a team member in the Phase II program although the subcontract we will issue to Honeywell is not a substantial amount.

Finally, silicon-on-sapphire display chips will be fabricated by Peregrine Semiconductor Corp., San Diego. They are the only source for UTSOS chip manufacturing in the USA. They showed great interest in our program as they think the successful results of this program can increase the volume of UTSOS chip fabrication. For this purpose, they agreed to lower their standard initial lot price of $125K down to $85K in order to see the program successful (Attachment IV).

In summary, we laid the groundwork for a successful Phase II program in this Phase I work. The team we put together consists of David Sarnoff, Peregrine Semiconductor, Honeywell and LEEP Systems, and Optron Systems, Inc. Every member of this team has demonstrated successful prototypes in the area of displays. The joint effort between these team members will lead to a very successful Phase II program after which we will have commercially available products for Proxima Corporation, San Diego.