Solution of 1-D Schrödinger and Poisson Equations in Single and Double Gate SOI MOS

Claudio Fiegna
Dept. of Engineering, Via Saragat 1, 44100 University of Ferrara, Italy, cfiegna@ing.unife.it

Antonio Abramo
INFM, Dept. of Physics Dept., University of Modena, Italy

1995

Abstract— In this paper the self-consistent solution of Schrödinger and Poisson equations is applied to single- and double-gate SOI MOS structures. The reasons for possible advantages related to the presence of the two symmetric gates in the latter case are investigated.

I. Introduction

The double-gate MOS structure (DGM) has been proposed for fabrication of future MOSFETs due to superior control of short channel effects, lower sub-threshold leakage and higher currents compared to a single gate SOI MOS (SGM) of same area [1]–[3]. The increase of DGM's current is due, above all, to the formation of a double conducting channel close to the two Si-SiO_2 interfaces. Additional gain in terms of transconductance and current drive was claimed in [1], [2] (total gain of the DGM over the SGM up to a factor 2.5-3) and attributed to the inversion of the silicon region away from the two interfaces. Previous theoretical studies devoted to such effects were based on a classical approach [4]. Since the detailed spatial distribution of mobile charge in silicon is crucial for the evaluation of volume inversion, a study based on the self-consistent solution of Schrödinger and Poisson equations is mandatory.

In this paper, such a study is performed for a one-dimensional DGM structure and for the corresponding SGM one, in order to clarify the role played by volume inversion, gate capacitance improvements due to the interaction between the two gates, and finally the effect of different transverse electric field profiles.

II. Simulated structures and simulation approach

In Fig. 1 a schematic picture of the simulated structures is sketched. In the DGM case, a thin silicon layer is included between two symmetric gates while in the SGM case a much thicker back oxide is present.

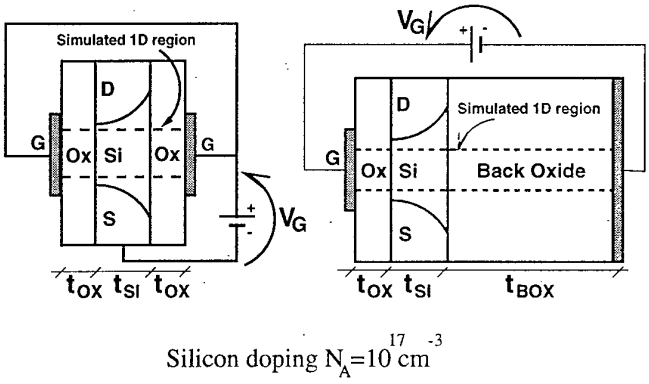

Fig. 1. Schematic section of the simulated structures; left: double gate MOS, right: single gate MOS.

Since we are investigating a possible structure for MOS devices with gate length $L_G \leq 0.1\,\mu$m, we assumed very thin gate oxide (t_{OX}) and silicon layer (t_{SI}). In our simulations, we considered t_{SI} down to 5 nm, t_{OX}=3 nm and the thickness of the back oxide of the SGM devices t_{BOX}=50 nm. For the silicon layers, p-type doping with $N_A=10^{17}\,cm^{-3}$ was assumed for both structures. The two gate electrodes of the DGM and the front gate of the SGM are assumed of n-polysilicon type, while in the SGM device a grounded p-polysilicon gate mimics the effect of the silicon bulk. As for the silicon thickness, its reduction weakens short channel effects both in SGM [5] and DGM [3]. Furthermore, reducing t_{SI} enhances the effects of volume inversion in the DGM case [1], [6]. In this work, as we were particularly interested in volume inversion, we considered very small t_{SI} in order to enhance such an effect in the DGM structure.

The issues of volume inversion, electron effective field and gate-to-channel capacitance have been investigated by a one-dimensional approach. Therefore, the results obtained are valid for low applied drain-to-source voltages, i.e. in the linear MOSFET regime, or, more in general, when two-dimensional effects can be assumed to be small. Despite to this limitation, the results of this paper are anyway valid as a comparison between the different

One of the authors (A.A.) thanks A.R.O., O.N.R, and E.R.O. for partially funding the work.

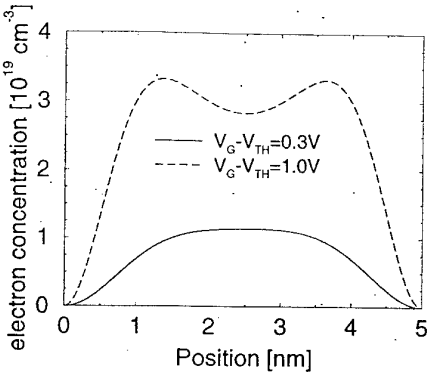

Fig. 2. Inversion charge density profile within the silicon layer of a double gate MOS with t_{SI}=5 nm, t_{OX}=3 nm, for two different bias points above threshold.

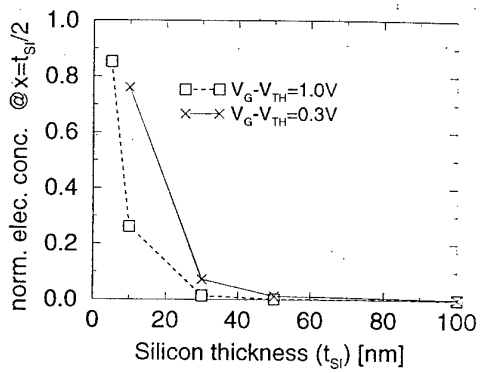

Fig. 3. Electron concentration at the middle of the silicon film of a DGM, normalized to the peak value close to the interfaces, as a function of silicon layer thickness.

structures analyzed. In fact, since the concept of "short MOSFET" (i.e. suffering of relevant 2D short channel effects) is relative to the adopted technology, even a 0.1 micron MOSFET fabricated with a 50 nm technology and operating at low voltages [7], can be considered as a "long channel" device. Therefore, for such a device 1D results are relevant.

The simulations were carried out by self-consistently solving the Poisson and Schrödinger equations in a Gummel-like scheme. The quasi-Fermi levels for electrons and holes are set within the whole simulation domain, to reflect a bias condition with grounded source and drain. The envelope function equation (i.e. Schrödinger equation in the effective mass approximation) is solved to determine the eigenvalues and eigenvectors of the system, neglecting wavefunction penetration into the gate oxide.

III. Simulation results

Fig. 2 reports the electron concentration in a DGM with very thin t_{SI} biased above threshold. A maximum at the center of the silicon film is obtained for biases close to the threshold, while at higher V_G two inversion maxima are formed with non-negligible concentration in the silicon volume. The effect of volume inversion vanishes rapidly as t_{SI} is increased, leading to a reduction of the minority carrier concentration in the middle of the silicon film. This is shown in Fig. 3 reporting the electron concentration of that middle point normalized to the peak concentration close to the interfaces, as a function of t_{SI} and for two given gate drive voltages (well above threshold). The presence of a maximum of the electron concentration at the middle point, due to the interaction of the two gate fields, may be the sign of a larger inversion sheet density for the DGM compared to the SGM biased at the same gate drive. Therefore, in presence of substantial volume

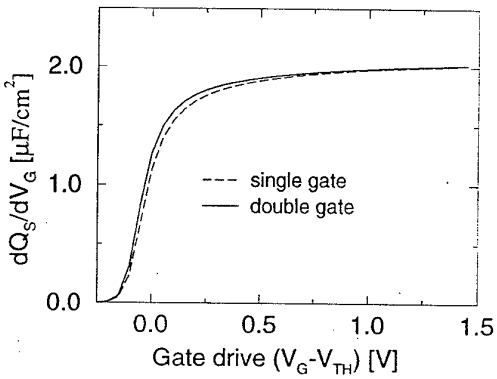

Fig. 4. Gate control capacitance (dQ_S/dV_G) in single and double gate MOS structures with t_{SI}=5 nm, t_{OX}= 3 nm (in order to compensate the for DGM's double channel, the inversion charge per unit area of the SGM is multiplied by a factor of two).

inversion, a larger inversion charge and a larger derivative with respect to the gate voltage (dQ_S/dV_G, Q_S=q·N_S being the inversion sheet density) could be expected in the DGM case compared to the SGM one. Simulation results show that even when t_{SI} is comparable to the displacement of the charge peak from the interface, the increase of inversion charge and capacitance of the DGM case with respect to the SGM one occurs only for bias points close to the threshold voltage, and it is almost negligible. In addition, the two cases become coincident above threshold (Fig. 4).

From this result we may not expect a large improvement in the currents and transconductance as a direct consequence of the increase of the inversion charge due to the interaction between the two gates of the DGM structure.

Another possible explanation for the larger current and transconductance in the DGM can relate to the different distributions of the inversion charge in the two structures, leading to a different influence of the surface roughness scattering. In Fig. 5 the charge density profile of a DGM

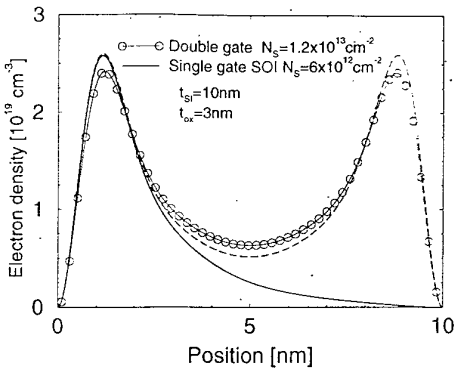

Fig. 5. Electron density profile in the silicon film of a DGM structure (symbols) and a SGM one (solid line). V_G-V_{TH}≃1.0 V, t_{SI}=10 nm, t_{OX}=3 nm for both structures. Dashed line: sum of two specular SGM charge profiles.

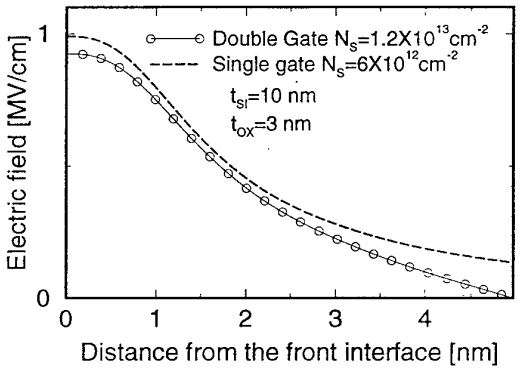

Fig. 6. Transverse electric field within the upper half of the silicon film of a DGM structure and a SGM one with t_{SI}=10 nm, t_{OX}=3 nm.

structure is compared to that of a SGM with same silicon thickness biased with the same gate drive. The DGM charge density profile is more displaced from the interface than the SGM one, and its value at the middle of the silicon layer is larger than what obtained summing the charge profiles of two specular SGMs (dashed line). However, such differences appear to be only marginal and do not evidence a relevant volume inversion effect.

Finally, we can compare the two structures on the basis of the transverse effective electric field (i.e. the transverse field averaged over the channel carriers' spatial distribution) that, at least for the case of bulk MOSFETs and SOI SGM with $t_{SI} \geq$10 nm, is related to low-field mobility through the universal mobility curves [8], [9]. Here, we extend the concept of effective field to the DGM case for the purpose of comparison.

Fig. 6 compares the transverse electric field (TEF) within one half of the silicon layer of a DGM and a SGM biased at the same V_G-V_{TH} . The TEF is lower in the DGM case and vanishes at the middle of the silicon layer due to the symmetry of the structure. As a consequence,

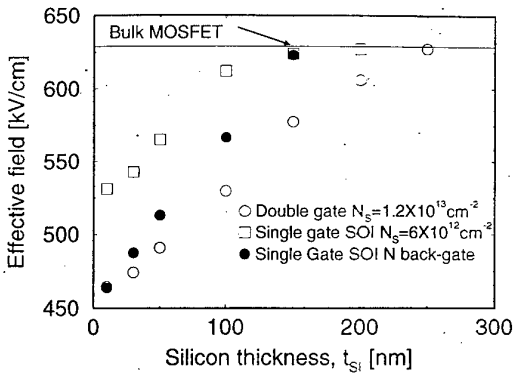

Fig. 7. Effective electric field vs. silicon layer thickness for the DGM (N_S=1.2 × 10^{13} cm^{-3}) and the SGM (N_S=6 × 10^{12} cm^{-3}) structures. Dashed line: effective electric field for a uniform bulk MOS of same doping, gate oxide thickness and N_S=6 × 10^{12} cm^{-3}.

the effective field (EEF) is lower in the DGM case, possibly leading to improved mobility. Fig. 7 reports the EEF, computed starting from the self-consistent charge and TEF, as a function of t_{SI}.

$$E_{EFF} = \frac{\int_0^{x1} E(x)n(x)dx}{\int_0^{\infty} n(x)dx}$$

where x, $n(x)$ and $E(x)$ are the distance from the device surface, the electron density, and the TEF, respectively; x1 represents the upper integration bound corresponding to the back interface in the SGM and to the middle of the silicon thickness in the DGM case (we compute the effective field associated to one of the gates only, thus, due to the symmetry of the DGM, to each of the two inversion layers). In this comparison, to account for the double channel in the DGM, the gate bias is set to obtain a DGM inversion charge twice that of the SGM. As t_{SI} is increased, the EEF increases towards the bulk value, that is reached both by SGM and DGM when they become non-fully depleted. Due to the two depletion layers, the DGM reaches the non-fully-depleted regime with a double t_{SI} compared to the SGM. At relatively large t_{SI} ($\geq$ 100 nm), the larger EEF of the SGM is due to the different amount of fixed charge contributing to the transverse field. In fact, the EEF of each specular half of the DGM is affected only by the depletion charge located in the same half of silicon film. By reducing t_{SI}, the role of the depletion charge decreases (N_S kept constant in these simulations). In spite of that, the EEF of the SGM is larger than the DGM one even for t_{SI} as thin as 10 nm ($N_{DEPL} \approx 10^{11}$ cm$^{-2} \ll N_S$), due to the coupling between the silicon layer and the back-gate (grounded p-silicon in this case) that, for very thin t_{SI}, enhances the EEF. This is confirmed by the filled circles obtained for the SGM

with a grounded n-type back-gate: the EEF of the SGM is strongly reduced for very small t_{SI}, while for large t_{SI} the DGM recovers its advantages over the SGM.

IV. Conclusions

In this paper the self-consistent solution of Shrödinger and Poisson equations was applied to compare single and double-gate SOI MOS structures. Based on the simulation results, and extending the concept of effective field to the DGM case, we may conclude that the DGM features a lower effective field compared to the SGM.

The largest reduction of the DGM's effective field can be obtained, at given substrate doping, for silicon thicknesses close to the depletion layer width associated to the non-fully depleted SGM and, for the doping concentration considered here, it is slightly larger than 100 nm.

Definitive conclusions about the superiority of DGM require additional studies, (either experimental and theoretical) devoted to establish the relationship between effective field and low-field mobility for DGMs.

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