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THESIS

A DIRECT SEQUENCE - CODE DIVISION MULTIPLE ACCESS/DIFFERENTIAL PHASE-SHIFT KEYING (DS-CDMA/DPSK) MODEM DESIGN

by

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March 1997

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The development of a differential phase-shift keying (DPSK), direct sequence, spread spectrum modem is conducted for the purpose of creating a prototype design to be implemented in a multi-user environment. In this design, a maximal length sequence of 31 chips is used to spread the information data. The multi-user performance analysis is performed by using Bit Error Rate (BER) test equipment (1645 Hewlett Packard data error analyzer). A multi-user interference cancellation circuit for two users is introduced, and measurements are performed to show its effectiveness.

The design itself encompasses the selection of components and demonstrates that the preliminary operational characteristics of a spread spectrum DPSK modem scheme for CDMA application can be achieved.

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A DIRECT SEQUENCE - CODE DIVISION MULTIPLE ACCESS/DIFFERENTIAL PHASE-SHIFT KEYING (DS-CDMA/DPSK) MODEM DESIGN

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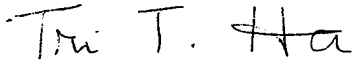
Approved by: 
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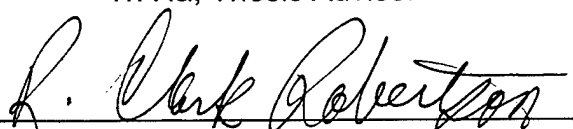
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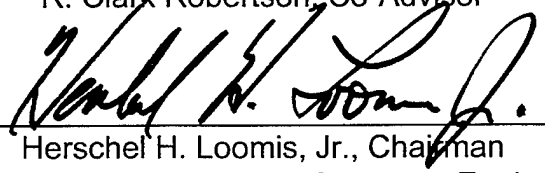
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ABSTRACT

The development of a differential phase-shift keying (DPSK), direct sequence, spread spectrum modem is conducted for the purpose of creating a prototype design to be implemented in a multi-user environment. In this design, a maximal length sequence of 31 chips is used to spread the information data. The multi-user performance analysis is performed by using Bit Error Rate (BER) test equipment (1645 Hewlett Packard data error analyzer). A multi-user interference cancellation circuit for two users is introduced, and measurements are performed to show its effectiveness.

The design itself encompasses the selection of components and demonstrates that the preliminary operational characteristics of a spread spectrum DPSK modem scheme for CDMA application can be achieved.

TABLE OF CONTENTS

I. INTRODUCTION

Coordination and control of spread spectrum networks consist of the usual issues such as architecture, protocols, throughput, system delay, routing and relay control, gateways, data quality, acknowledgment, and cryptographic key distribution. In addition, networking of spread spectrum radios involves monitoring signaling activity, controlling the number of users, taking advantage of the increase in throughput of code division multiple access (CDMA), and maintaining gateway interoperability.

Code division multiple access [Ref.1] is a very attractive area for research and development in satellite and cellular network systems because of the increasing demand on capacity and privacy.

Entering a CDMA network poses difficulties for both receivers and transmitters. As a receiver, network entry requires code acquisition and synchronization. As a transmitter, uncontrolled network entry may cause interference at other receiving nodes in the network. CDMA systems utilize a high chip rate coding sequence to spread and despread the information data to overcome these difficulties. By using a pseudo-noise (PN) sequence, the baseband information spectrum is spread over a wideband spectrum. The CDMA signal usually has a maximum power spectral density below the channel

noise level. When two CDMA signals share the same frequency band, a certain amount of crosstalk, or mutual interference, occurs.

The interference can be minimized since it is possible to design spreading sequences, such as Gold sequences, with low cross-correlation values so that the different code sequences are nearly orthogonal. The number of users in the same frequency band has an upper limit since system performance degrades as the number of users increases [Ref.1].

The objective of this thesis is to design and build a direct sequence code division multiple access, differential phase-shift keying (DS-CDMA/DPSK) spread spectrum modem that can be used in satellite network systems and to test its multi-user performance. An interference cancellation circuit is introduced to test the elimination of multi-user interference for two users. The following initial parameters are provided as guidance in formulating the design:

1. DPSK modulation with coherent detection [Ref.2].
2. Direct sequence spread spectrum using Gold Sequences of 31 chips generated from a preferred-pair of m-sequences [Ref.1].
3. Each data bit to be spread by one complete Gold sequence [Ref.1].
4. Data bit rate equal to 1200 bits per second.
5. Four users in the frequency band.

The basic concept of the PN sequence synchronization circuit is taken from [Ref.1,3,4,5]. The basic characteristics of code division multiple access (CDMA) are taken from [Ref. 1,6].

II. THE DESIGN OF DS-CDMA/DPSK MODEM

A. GENERAL

The modulator section of the DS-CDMA/DPSK modem design has six main functional blocks:

1. Pseudo-random noise sequence generator [Ref. 2,3,4,5].
2. Data source and clock generator [Ref.7].
3. Differential encoder [Ref.8,9].
4. Level shifter [Ref.8].
5. Low pass filter and mixer [Ref.8,9,10,11].
6. Signal Generator (carrier).

The DPSK modulator functional block diagram is shown in Figure 1.

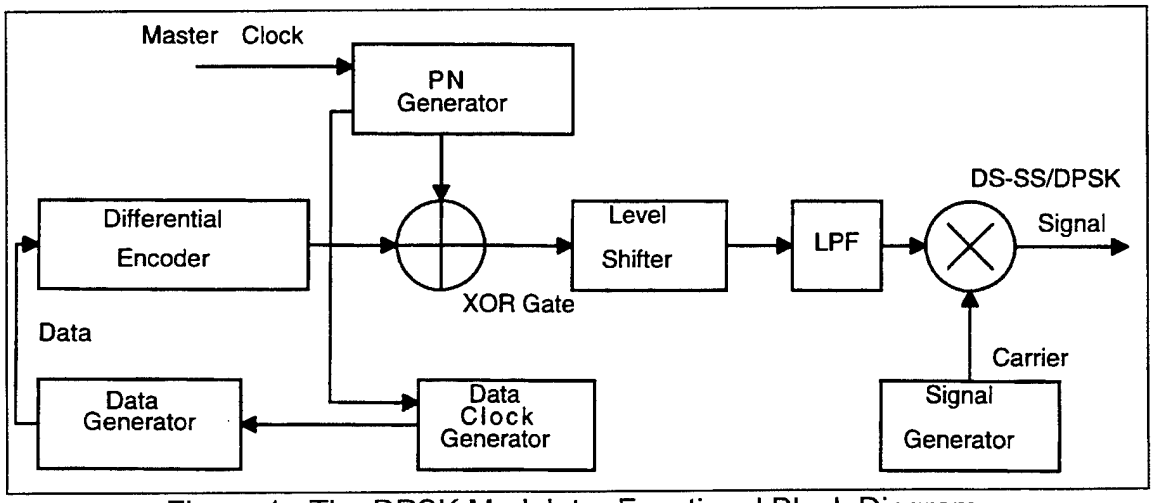

Figure 1. The DPSK Modulator Functional Block Diagram.

A 37.2 kHz master clock is generated by a WAVETEK Model 142 function generator. This master clock provides clock pulses for the PN generator and the pattern generator (Model 1645A).

Two 5-bit shift registers are used as a pseudo-random Gold sequence generator in this spread spectrum modulator. By design, each data bit will contain an entire PN sequence of 31 chips. The PN sequence is also used to generate a 1.2 kHz clock which in turn is used to trigger a 1.2 kbps data signal from the pattern generator.

The data is spread digitally by using a modulo-2 adder as detailed later. After spreading the data, the signal levels are shifted from TTL levels to ± 5 volts. A low pass filter with a cut-off frequency of 37.2 kHz was designed and built to suppress the side lobes of the baseband spread spectrum signal. The resultant signal at the output of low pass filter is mixed with the 76.2 kHz carrier signal. This DS-CDMA/DPSK signal is connected to the demodulator directly via hardwire.

The demodulator functional block diagram is obviously more complicated than that of the modulator. There are several functions performed by the demodulator:

1. Signal demodulation [Ref.6,14,17,21].
2. Spectrum despreading [Ref.12].
3. PN sequence generation [Ref.3,23].
4. Acquisition and tracking [Ref.4,6].

The demodulator functional block diagram is shown in Figure 2.

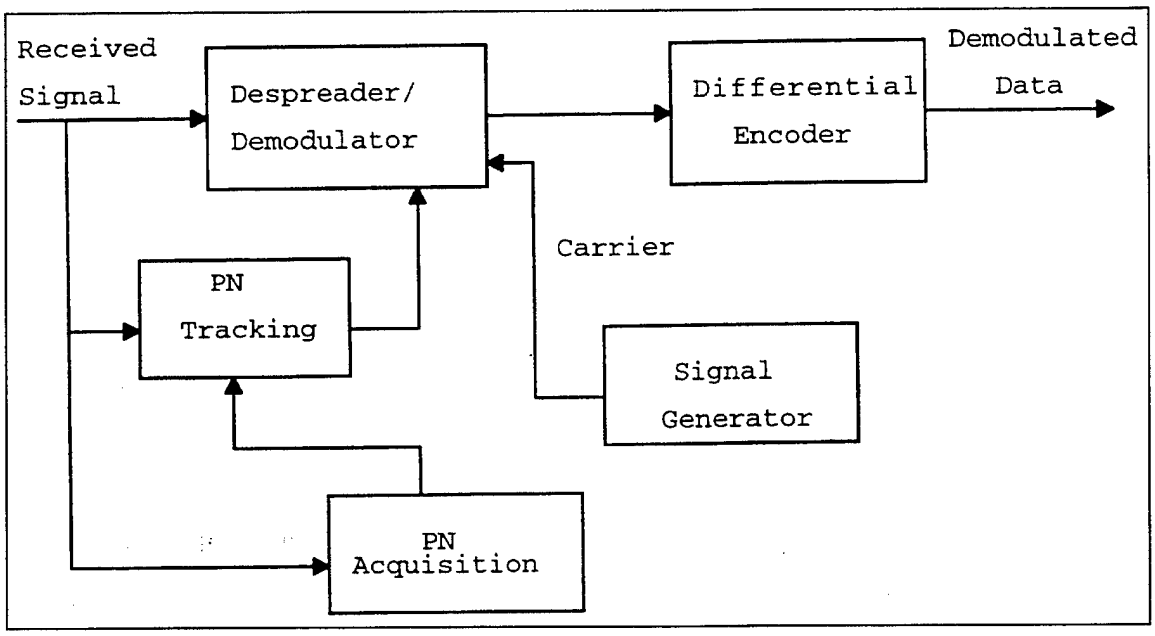

Figure 2. Demodulator Functional Block Diagram.

The function of the PN acquisition subsystem is to bring the PN signal generated in the demodulator to within $\pm T_c/2$ of the received PN signal where T_c is the chip duration. To obtain the phase difference in the range of $\pm T_c/2$, the acquisition subsystem searches through a set of 31 different discrete phases and selects the one which yields the highest correlation with the incoming PN signal.

Once the phase of the local PN signal is within $\pm T_c/2$ of the incoming PN signal, the tracking circuit attempts to bring the phase difference to zero.

The PN signal from the tracking circuit and a coherent carrier are used for despreading and demodulation to obtain an estimate of the transmitted data.

A detailed block diagram of demodulator is shown in Figure 3.

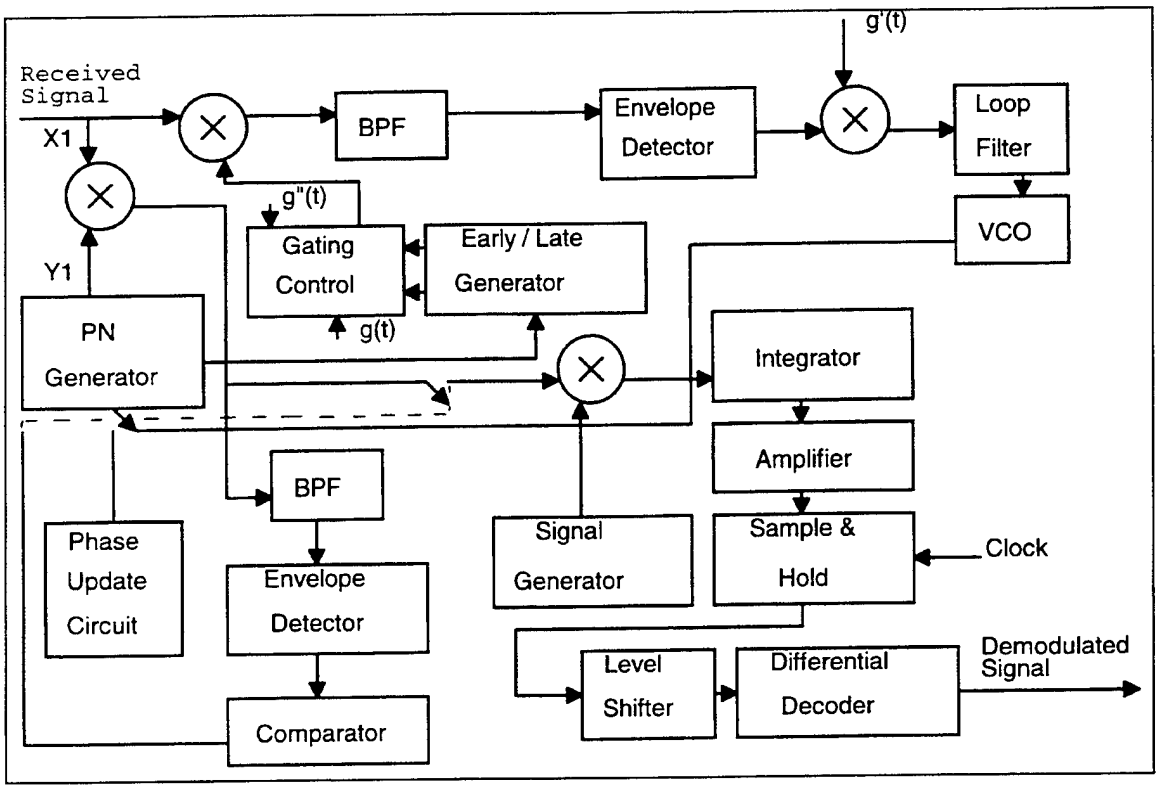

Figure 3. The Functional Block Diagram of the Demodulator.

PN acquisition is performed before tracking. Since the carrier frequency and phase are available, coherent carrier demodulation is used with the acquisition circuit. Once the PN code phase has been acquired, the PN tracking circuit is initiated.

B. PN GENERATOR

The generation of PN sequences for spread spectrum applications is a topic that has received considerable attention in the technical literature [Ref.1,3]. The baseband frequency spectrum of the PN sequence which is used in this design is shown in Figure 4.

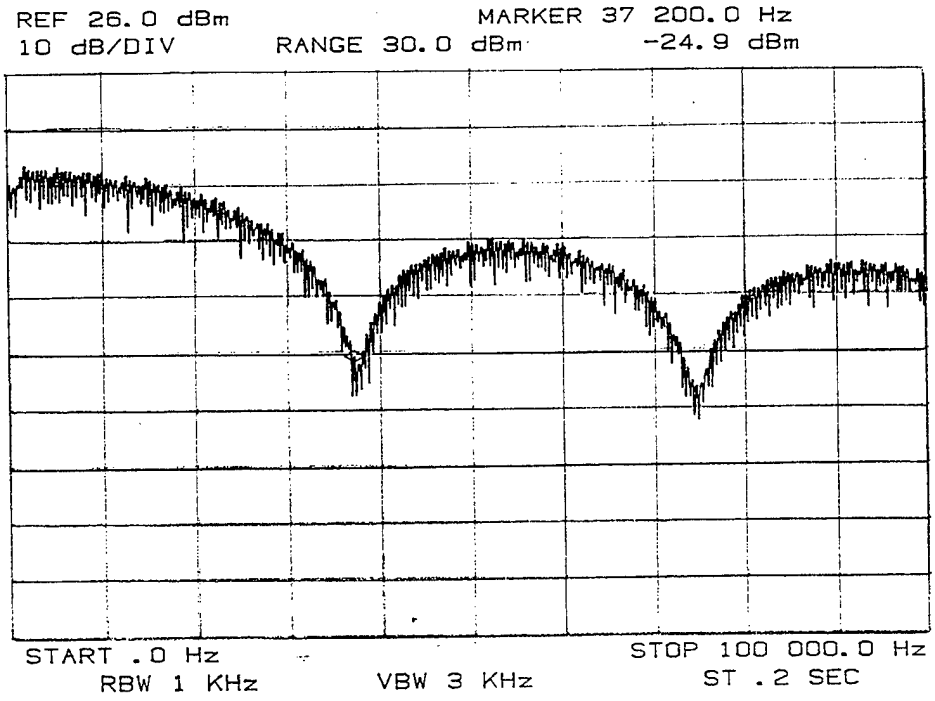

Figure 4. Power Spectral Density of the PN Sequence.

The cross-correlation properties of PN sequences are as important as the auto-correlation properties for CDMA applications. For example, in CDMA each user is assigned a particular PN sequence. Ideally, the PN sequences among users should be mutually orthogonal. However, the PN sequences used in practice exhibit some cross-correlation [Ref.1,6].

High peak values for the cross-correlations are undesirable in CDMA. Although it is possible to select a small subset of *m*-sequences that have relatively small cross-correlation peak values, the number of sequences in the set is usually too small for CDMA applications. PN sequences with better periodic cross-correlation than *m*-sequences are given by Gold. Two *m*-

sequences of length *n* with a periodic cross-correlation function that takes on the possible values {-1, -t(m), t(m) -2} where $t(m)=1+2^{\lfloor (m+2)/2 \rfloor}$, with $\lfloor c \rfloor$ denoting the integer part of the real number c, are called preferred sequences. From a pair of preferred sequences, a set of sequences of length *n* are constructed by taking the modulo-2 sum of the first sequence with *n* cyclic shifted versions of the second sequence or vice versa. Thus, *n* new periodic sequences with period

$$n=2^m-1 \qquad (2.1)$$

are obtained. The sequences constructed in this manner are called Gold sequences [Ref.2].

A generalized Gold sequence generator configuration is taken from Dixon [Ref.3] and shown in Figure 5.

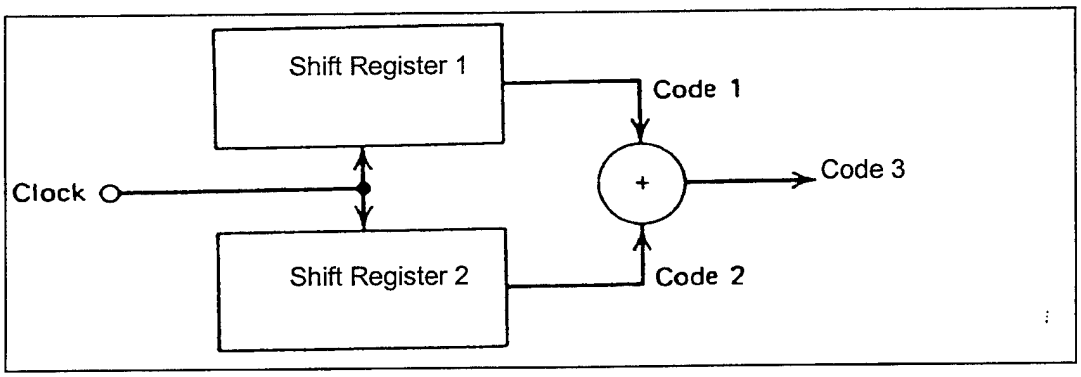

Figure 5. The Configuration of the Gold Code Sequence Generator. [Ref.3]

Each *m*-sequence generator itself consists of two 4-bit, serially connected feedback shift registers. The main structure of the PN generator design is taken from Pickholtz [Ref. 4]. The illustration of the Gold sequence generation is shown in Figure 6.

In the design of the first of the two *m*-sequence generators, the second and fifth stages of the shift register are modulo-2 added by an exclusive OR gate [Fig.6]. The resultant logic level is fed back to the input of the third stage of the shift register. For the second of the two *m*-sequence generators, the fourth and fifth stages of the shift register are modulo-2 added, and the resultant signal is fed back to the input of the fifth stage of the shift register. Similarly, the second and fifth stages are also modulo-2 added, and the resultant signal is fed back to the input of the third stage of the shift register. The resultant PN sequences, which are the outputs of the fifth stage of each shift register, are maximal length sequences with outputs consisting of a series of TTL levels in pseudo random order. This binary sequence is repeated every 31 clock cycles and each sequential pattern is identical.

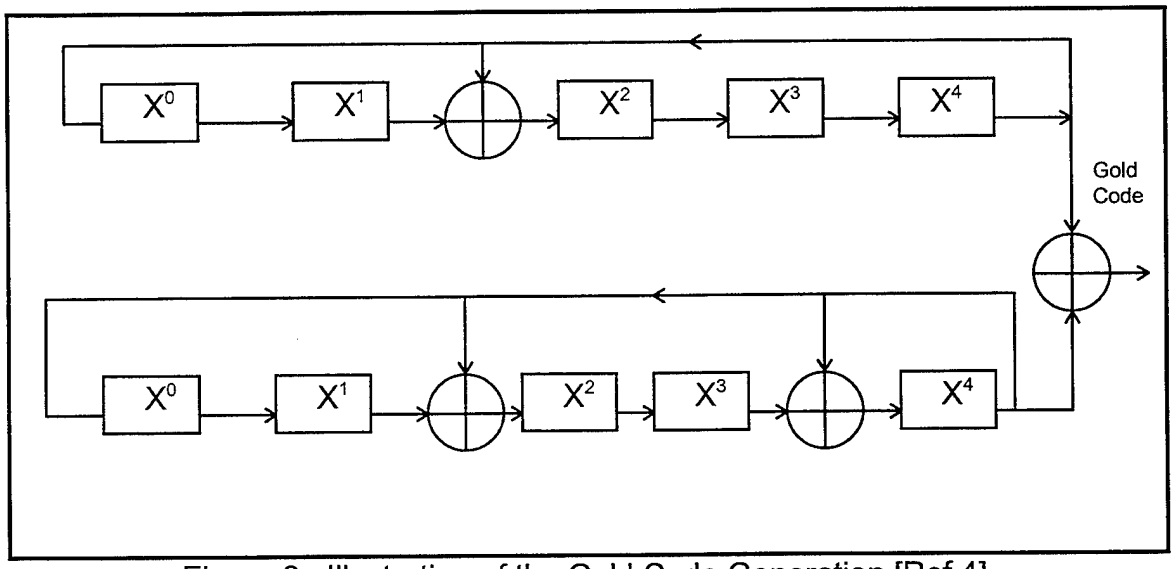

Figure 6. Illustration of the Gold Code Generation [Ref.4].

A representative sample of the first Gold sequence employed in the spreading and despreading sections is shown in Figure 7. A 31-bit period of the Gold sequence in Figure 7 is marked by the vertical dotted lines.

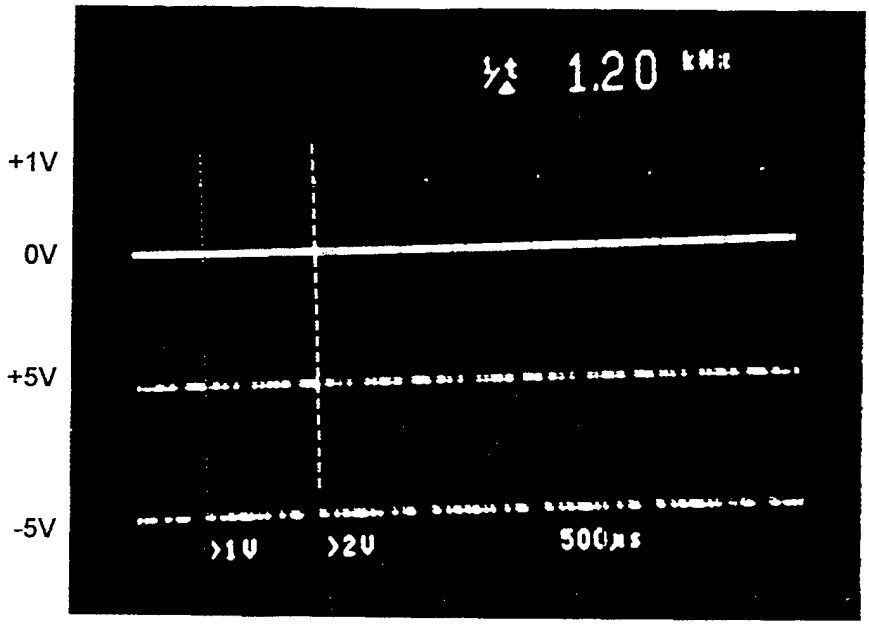

Figure 7. Top: Clock (37.2 kHz).
Bottom: PN Sequence (Gold Sequence).

The Gold sequence which consists of two preferred *m*-sequences having the generator polynomials $f_1(x)=(1+x^2+x^5)$ and $f_2(x)=(1+x^2+x^4+x^5)$ is shown in Figure 8 with the resultant Gold sequence $f(x)=f_1(x).f_2(x)=(1+x+x^3+x^9+x^{10})$ [Ref.4].

The generation of the 1.2 kbps data clock is accomplished internally by using the master clock used in the PN generator. To accomplish this, all five outputs of the shift register stages are fed to an AND gate to generate a 1.2 kHz square wave clock which is used to trigger the 1.2 kbps data.

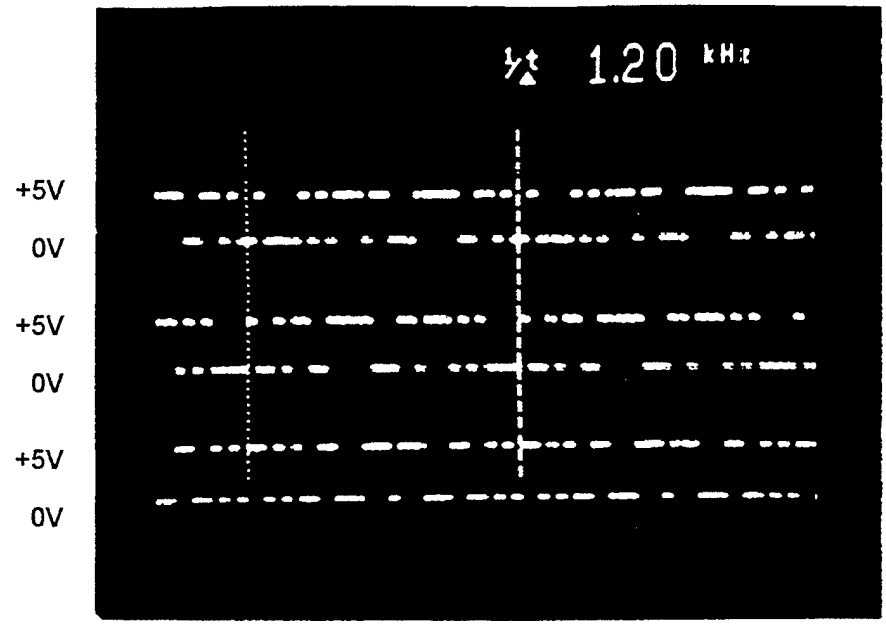

Figure 8. Top: First Preferred m Sequence. $f_1(x)=(1+x^2+x^5)$.
Middle: Second Preferred m Sequence. $f_2(x)=(1+x^2+x^4+x^5)$.
Bottom: Gold Sequence. $f(x)=(1+x+x^3+x^9+x^{10})$.
(The vertical lines show a 31-bit period of the Gold sequence).

C. MODULATOR

For a DPSK signal, data bits are differentially encoded, and the information is contained in the change in phases between successive bits. The differential encoding operation is described mathematically by [Ref.14]:

$$c_k = b_k \oplus c_{k-1} \tag{2.2}$$

where b_k is the k th information bit into the encoder, c_k is the k th output bit of the encoder, c_{k-1} is the (k-1) th encoded bit, and $\oplus$ denotes modulo-2 addition. The output bit c_k represents a logic one by a change in polarity and a logic zero by no change in polarity. A practical implementation of Equation 2.2 is shown in Figure 9.

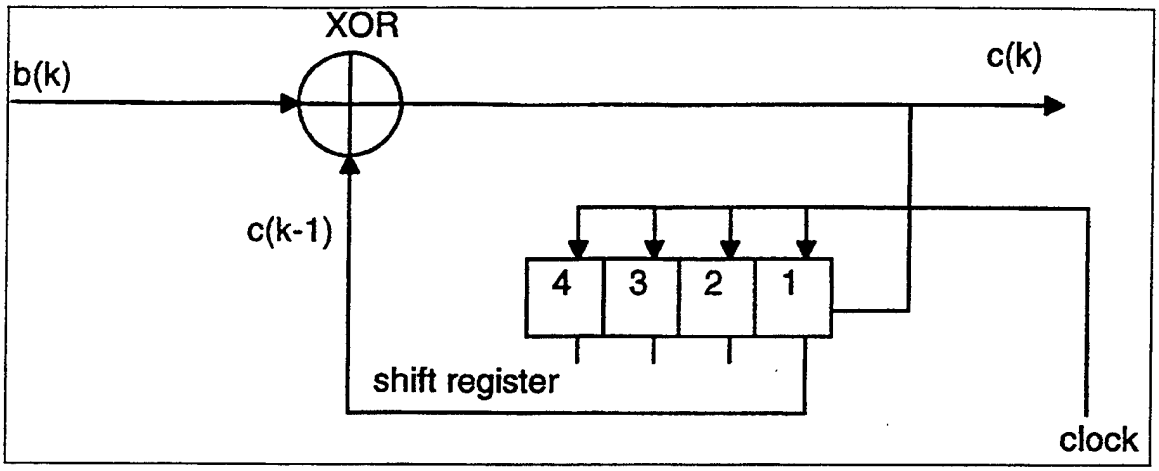

Figure 9. The Configuration of Differential Encoder.

The differential encoder is constructed by employing an exclusive OR (XOR) gate and a four-bit shift register. The differentially encoded data is presented in Figure 10.

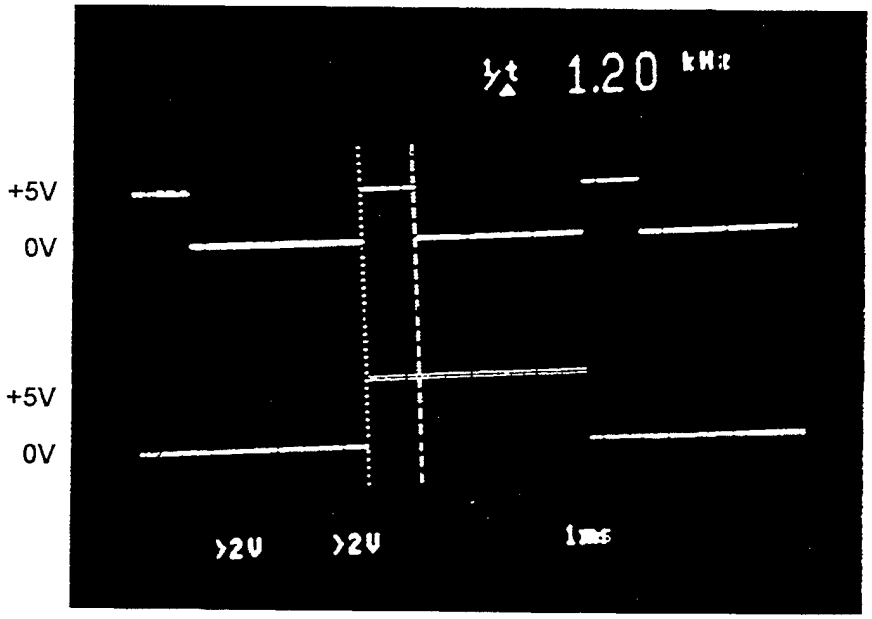

Figure 10. Top: Information Data (b_k).
Bottom: Differentially Encoded Data (c_k).

The generation of the DPSK modulated signal is achieved by two sequential mixing operations. The 1.2 kbps data sequence is mixed with the PN sequence in the modulator section to create the PN encoded data stream. An XOR gate is used for this process. The TTL voltages are converted to their analog equivalents for interfacing with the analog components in this design.

The mixers employed for modulation consist of an XOR gate (7486) and an analog voltage multiplier (AD 534). The spreading section consists of two elements: the spreading gate and the level shifter. The spreading gate is an XOR gate that modulo-2 adds the 1.2 kbps data signal and the PN sequence with a chip rate of 37.2 kchip per second.

The inputs to the XOR gate are the data stream (at 1.2 kbps) and the PN sequence generated by the PN generator section of the modulator. The output of the XOR gate can be thought of essentially as a bi-phase shifted PN sequence. Considering the length of the sequence (31 chips) as one period, each data transition, which contains 31 chips, causes the PN sequence to invert. The PN sequence phase relationship is thus similar to that of a bi-phase shifted sinusoid since the PN sequence is also a periodic wave form. The maximum periodicity is the reciprocal of the data rate, 833.33 μs.

The PN output of the XOR is fed to a level shifter. The level shifting is accomplished by connecting the output of the spreading gate to a LM311 comparator (with an amplification of 2:1) whose reference voltage is set at 2.5V, the mid-point between 0 and 5V. The resultant output is a balanced PN encoded

sequence with bipolar voltages of +5 and -5 volts as the digital logic PN sequence changes the logic levels between 0 and 5 volts, respectively. The resulting PN data stream from the comparator is interfaced with the (AD534) mixer. The AD 534 is a monolitic, laser trimmed, four-quadrant multiplier/divider having a maximum multiplication error of 0.25% [Ref.13]. This signal is connected directly to the Y1 input of the mixer (AD534). The sinusoidal carrier from the signal generator is connected to X1 input of the mixer where X2, Y2, and Z2 are connected to ground. The mixer accomplishes multiplication according to [Ref. 13]:

$$V_{output} = \frac{(X1 - X2)(Y1 - Y2)}{10} + Z2 \qquad (2.3)$$

The phase reversals at the output of the modulator due to the PN code employed can be observed in Figure 11. The output is the carrier frequency changing its phase with the change of phase of the PN sequence.

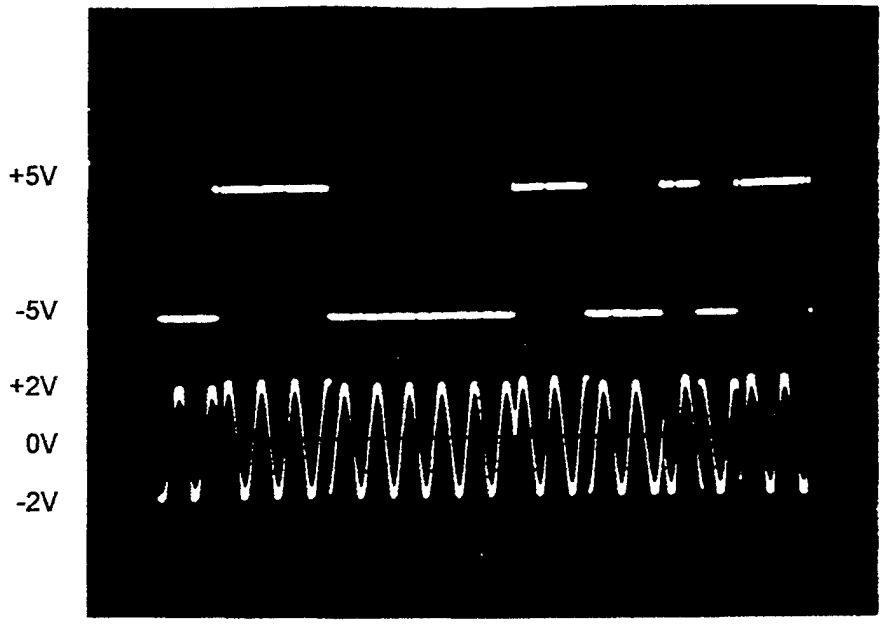

Figure 11. Top: PN Code.
Bottom: Modulator Output

D. DEMODULATOR

The coherent detection of DPSK signals assumes the availability of local carriers (reference signals) that are in perfect synchronism with the carriers in the transmitter.

As shown in Figure 3, after the despreading process, the resultant band pass signal is translated to baseband by mixing it with the carrier signal (76.2kHz) having the same frequency and phase as the carrier in the modulator. The frequency translation is achieved by an AD534 multiplier. A fourth order low-pass filter with a cut-off frequency of 1.2 kHz suppresses the image frequencies after the mixing process. The frequency response of the low-pass filter is shown in Figure 12.

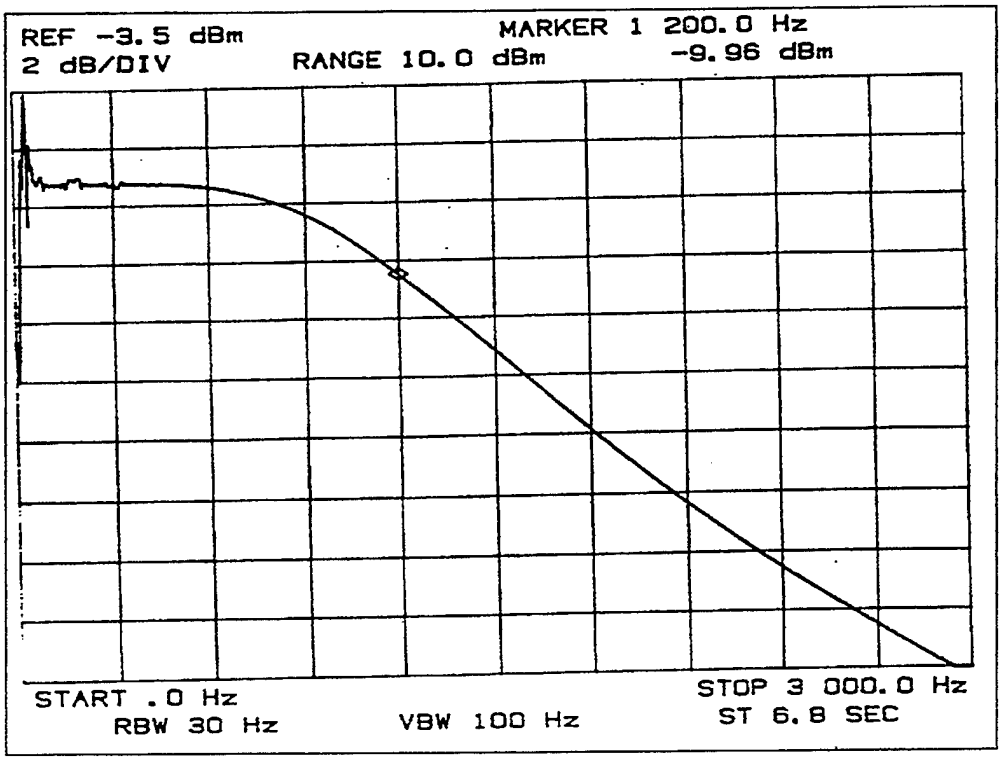

Figure 12. Frequency Response of the Fourth Order Low-Pass Filter.

The amplification factor of 0.1 of all the mixers employed in the demodulation process is compensated for by a non-inverting voltage amplifier (LM318) [Ref.8]. The integrator output in the demodulator is shown in Figure 13.

The resultant signal is sampled with the rising edge of the 1.2 kHz clock by a sample-and-hold circuit (LF398) and is then applied to a level shifter circuit (LM311).

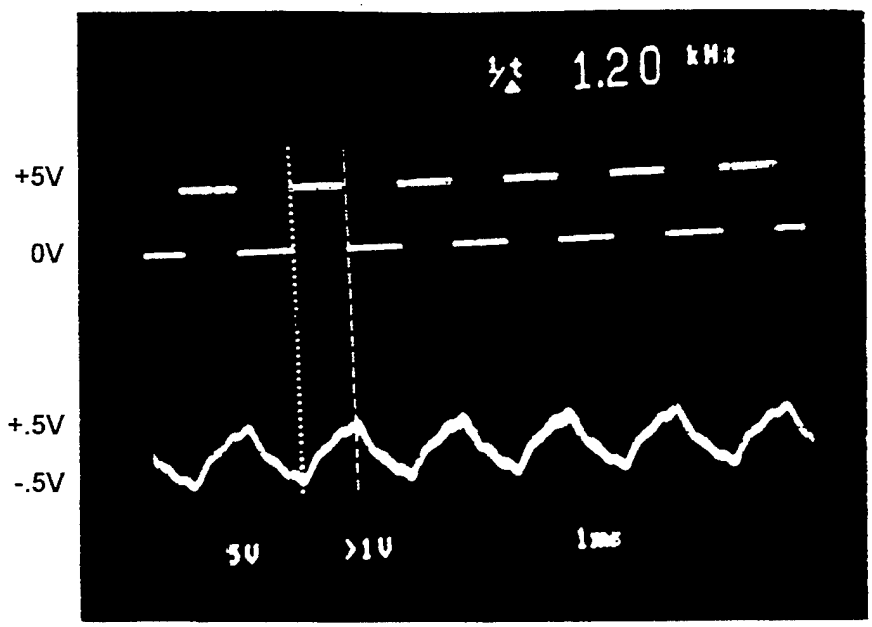

Figure 13. Top: Transmitted Data.
Bottom: Integrator Output in the Demodulator.

The last task in the DPSK demodulator is to decode the received data differentially. The differentially decoded data (b_k) is related to the received data (c_k) by [Ref.14]

$$b_k = c_k \oplus c_{k-1} \tag{2.4}$$

The decoder is implemented by using a configuration similar to the encoder but with a slight difference. The decoder is shown in Figure 14. The decoding operation in the demodulator can easily be verified by substituting Equation (2.2) into Equation (2.4); i.e.,

$$b_k = (b_k \oplus c_{k-1}) \oplus c_{k-1} = b_k \tag{2.5}$$

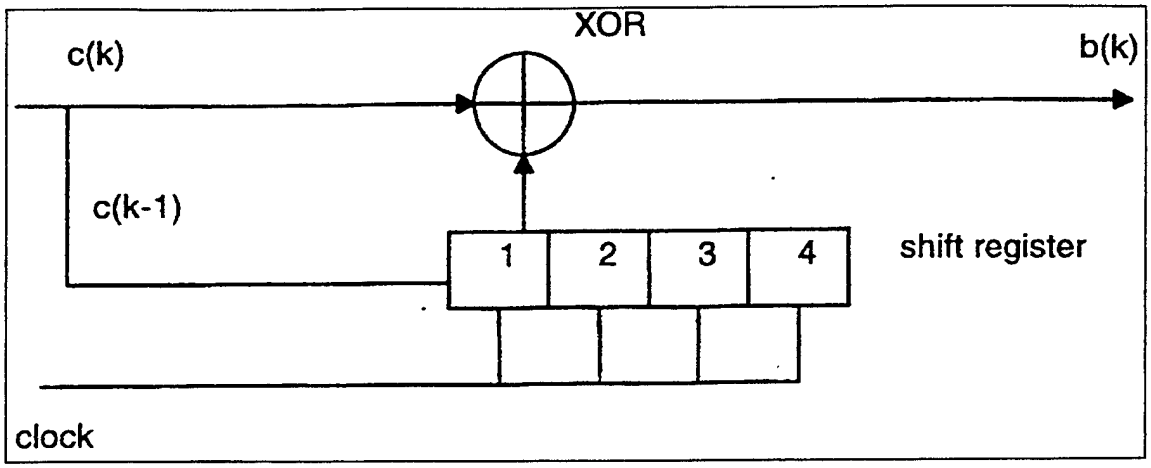

Figure 14. The Configuration of the Decoder.

The transmitted information signal and the received signal are shown in Figure 15.

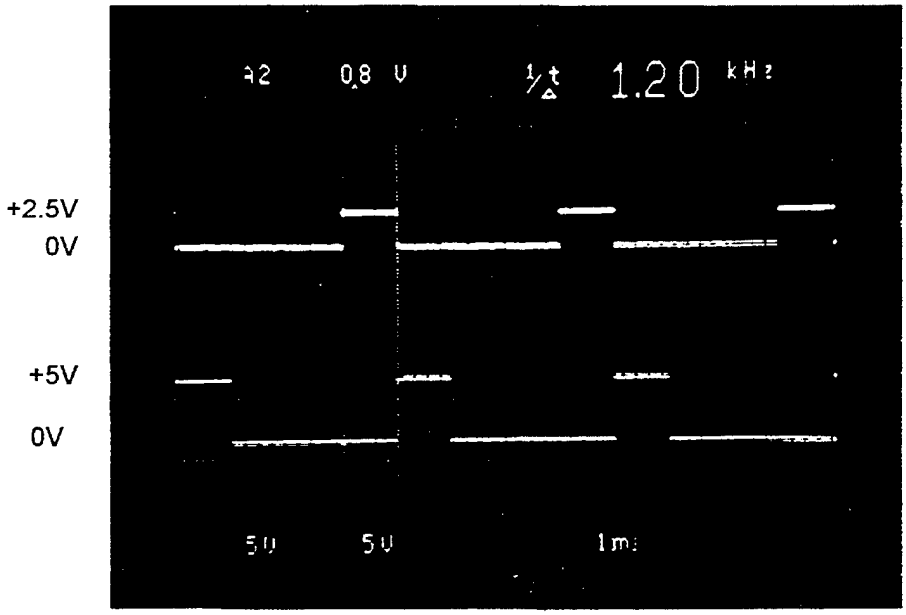

Figure 15. Top: Transmitted Information Signal.
Bottom: Received Information Signal

The other two functions performed by the receiver are acquisition and tracking, which are explained in the following sections in detail.

E. ACQUISITION

PN acquisition is usually the first task that the receiver has to perform. The acquisition process brings the phases of the local and the incoming PN signals to within a certain range. This range must also be within the pull-in range of the tracking circuit. Acquisition was the most difficult and the most time consuming task in this receiver design. The block diagram of the acquisition circuit is shown in Figure 16.

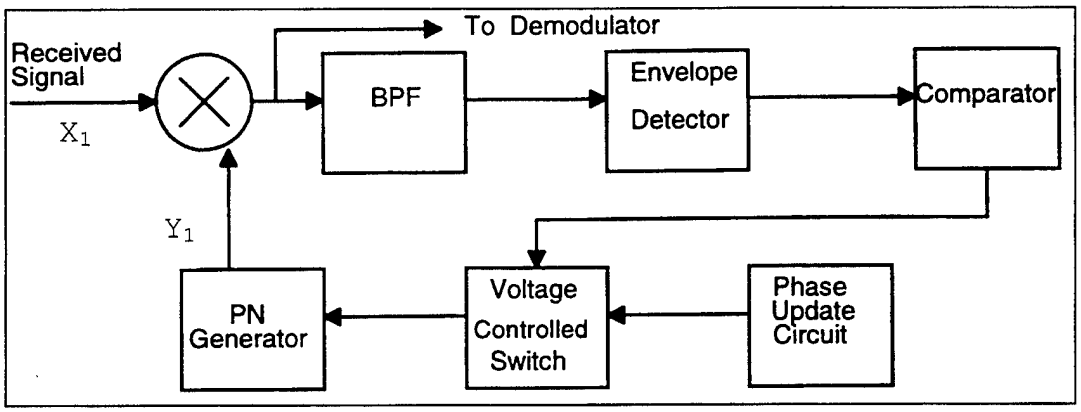

Figure 16. The Functional Block Diagram of the Acquisition Circuit

As shown in Figure 16, the receiver generated PN sequence is applied to the Y_1 input of an AD534 multiplier and the incoming signal is applied to its X_1 input. The instantaneous output of the AD534 is characterized by one of two possibilities when the spread spectrum signal is present at the input of the demodulator. In the first case, the receiver generated PN sequence lines up chip for chip with the received PN sequence. In the second case, further spreading of the already widened frequency spectrum is caused by misalignment of the PN sequences. The multiplier output is connected through a band-pass

filter to an envelope detector. The voltage level at the envelope detector output is used to determine alignment or misalignment.

In the uncorrelated case as shown in Figure 17, where the misalignment is one (greater than half) chip, the resulting signal at the output of the band pass filter is presented. The envelope detector output is rather low, approximately 0.1V, when the incoming PN sequence is not aligned with the local PN sequence. When the two PN sequences are correlated, the output from the envelope detector is notably greater and ranges between 1.9V and 2.2V. Thus, a band of correlation exists within one half chip either early or late relative to the received PN sequence. In this region, alignment of the PN sequences used in the modulator and the demodulator is possible.

The change from the acquisition to the synchronization mode is triggered by this higher output which is also used as an indication of acquisition of the incoming signal. In the analysis of the spectral outputs of the band-pass filter for each case, a difference in the correlated versus uncorrelated signals at the output of the envelope detector can be seen. The uncorrelated and correlated spectra as they appear on a spectrum analyzer from the output of the band-pass filter of the punctual channel are presented in Figures 19 and 20 where for this thesis the punctual sequence is defined as the PN sequence which despreads the received signal. Note that the output spectrum of the band-pass filter changes significantly when correlation occurs.

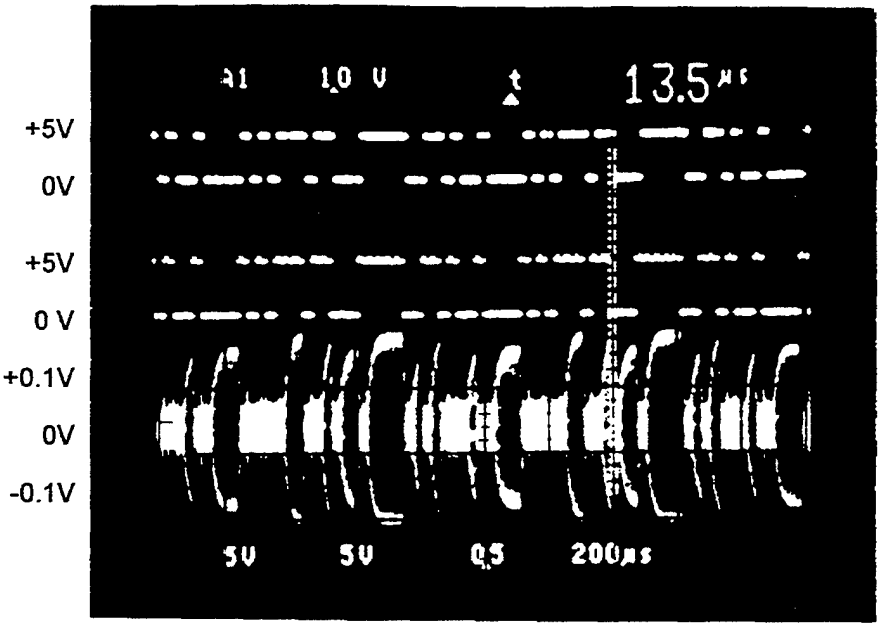

Figure 17. Top: PN Sequence Used in Modulation.
Middle: Punctual PN Sequence from Demodulator.
Bottom: Band-Pass Filter Output (Uncorrelated).

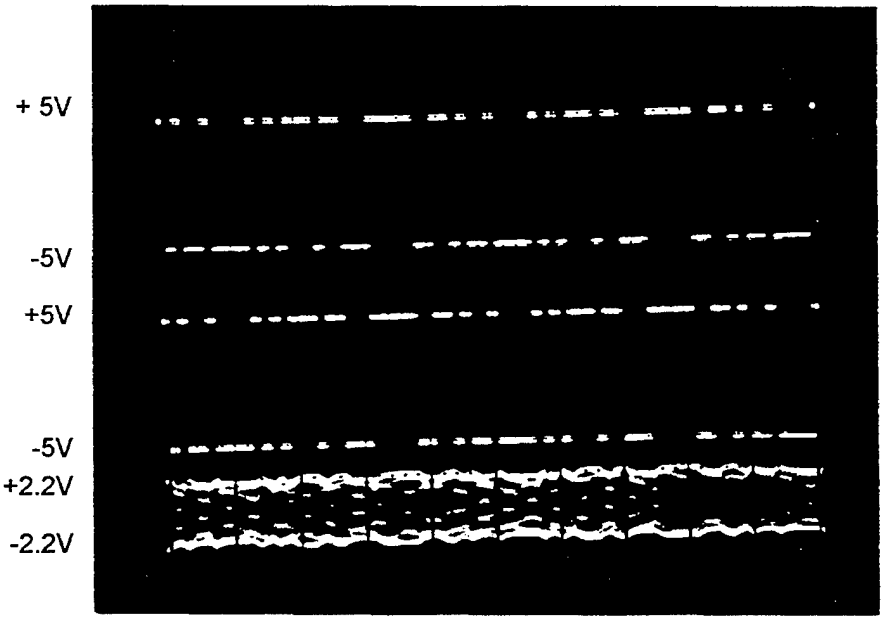

Figure 18. Top: PN Sequence Used in Modulation.
Middle: Punctual PN Sequence from Demodulator.
Bottom: Band-Pass Filter Output (Correlated).

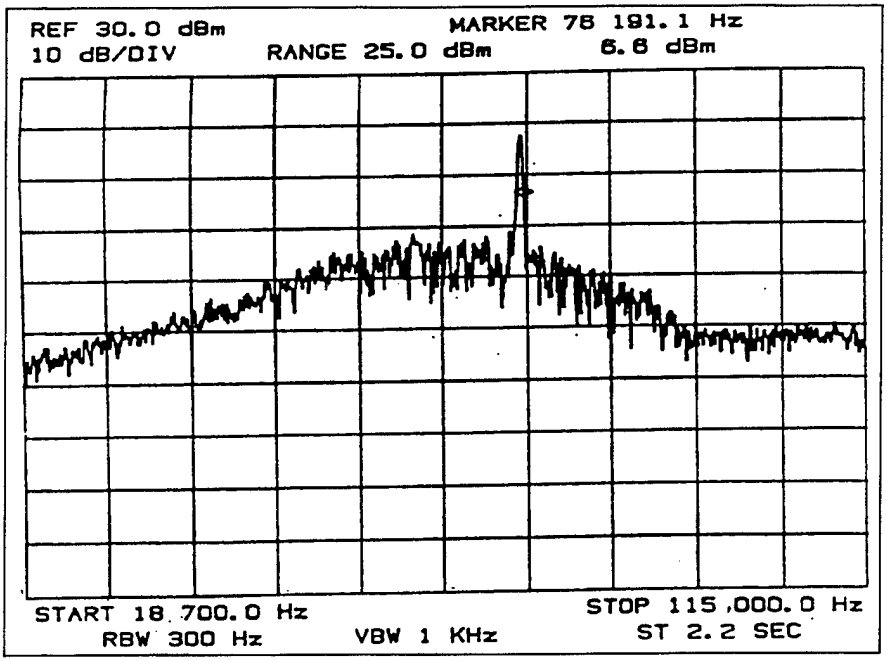

Figure 19. Uncorrelated Spectrum Output of the Punctual Channel Band-Pass Filter

The side lobes appearing at the output of the band-pass filter during correlation are representative of the despread DPSK modulated carrier. Moreover, in the correlated case, the spectral distance that occurs between the center frequency of the main lobe and the side lobes is just about 1.5 times the data rate (R_b).

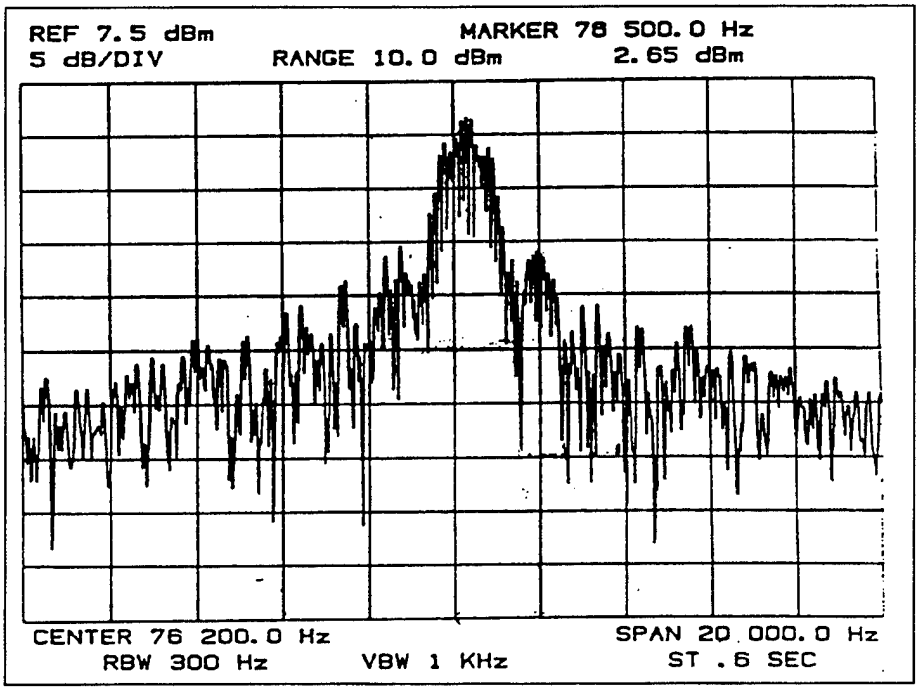

Figure 20. Correlated Spectrum Output of the Punctual Channel Band-Pass Filter

F. SYNCHRONIZATION

All direct sequence spread spectrum receivers must be synchronized to the incoming PN sequence in order to achieve despreading. The synchronization circuit consists of a loop that monitors the error and adjusts the desired signal in such a way so that the error goes to zero. Tracking is initiated after the acquisition circuit has brought the phase difference between the incoming and the local PN signals to within $\pm \frac{T_c}{2}$ seconds. The primary concern in an operational spread spectrum system is to ensure that the demodulator can despread the incoming spread spectrum signal to a narrow-band modulated signal from which the original transmitted data may be demodulated.

To achieve this, a demodulator design must possess two critical features. First, the same local PN sequence must be used in the despreading process as was used to originally spread the data. Second, the phase of the local PN sequence must be controlled and compensated for differences between it and the PN sequence imbedded within the incoming signal. This design uses a means of tracking referred to as a tau-dither loop [Ref.1,3,4]. This tracking loop is a delay-locked loop with only a single branch as shown in Figure 21. A tau-dither loop is similar to the delay-lock loop, but it uses only one correlator branch as opposed to two branches for the delay-lock loop. The correlation with early and late versions of the PN signal is achieved by dithering back and forth between these early and late signals. An advantage of tau-dither loop is that it eliminates the problem of matching the characteristics of the two correlator branches.

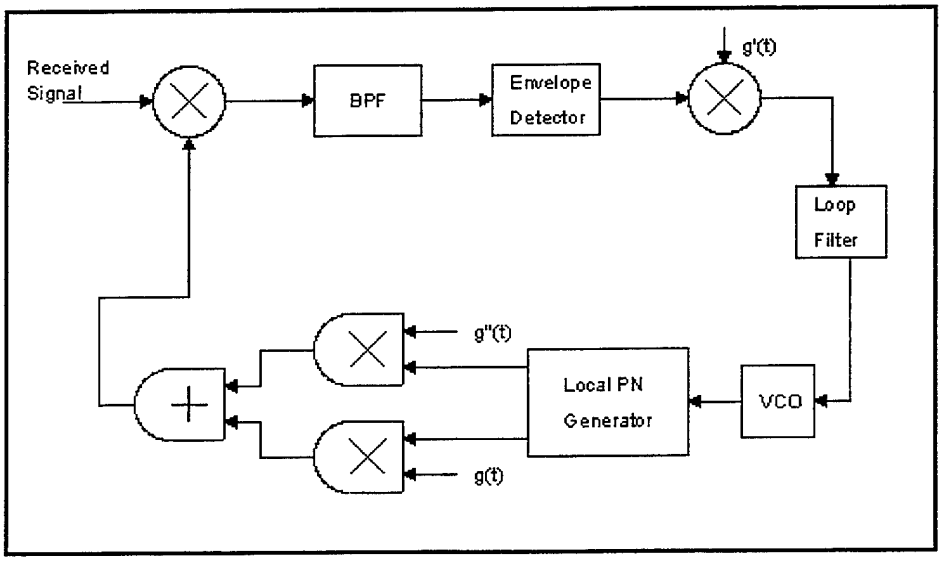

Figure 21. The Tau-Dither Loop [Ref. 1,3,4].

Unmatched branches can degrade performance. However, the signal power in the tau-dither loop is 3 dB smaller than that in the delay-lock loop and, accordingly, the tracking jitter is larger. The control or gating waveforms (g(t), g'(t) and g"(t) which are shown in Figure 22) are used to generate both arms of the delay-lock loop (DLL) through one branch [Ref.4]. Due to its simplicity, the tau-dither loop is often used instead of the DLL. It has a signal channel which is switched between early and late correlation by switching signal g'(t). The signal g'(t) is a square wave voltage which takes on values $\pm$1V. If g'(t)= -1V, then g(t)= 1V and g"(t)=0V. In this first case, the half bit early PN sequence is selected by the controlling gates and the half bit late PN sequence is blocked. On the other hand, if g'(t)=1V, then g(t)=0V and g"(t)=1V. In the second case, conversely, the resultant signal is the late PN sequence. The signal g'(t) is also used to multiply the envelope detector output. This multiplication provides the sign inversion necessary to generate the correlation curve from early and late signals. A representation of an ideal correlation signal at the input of the loop filter is shown in Figure 23.

When a frequency difference exists, the punctual PN sequence will attempt to drift (early or late) out of correlation if a correcting voltage is not applied to the voltage controlled oscillator (VCO). Upon drifting from the maximum correlation value, the early or late correlation signal, depending upon the direction of drift, will correspondingly add to or subtract from the control voltage sensed by the VCO.

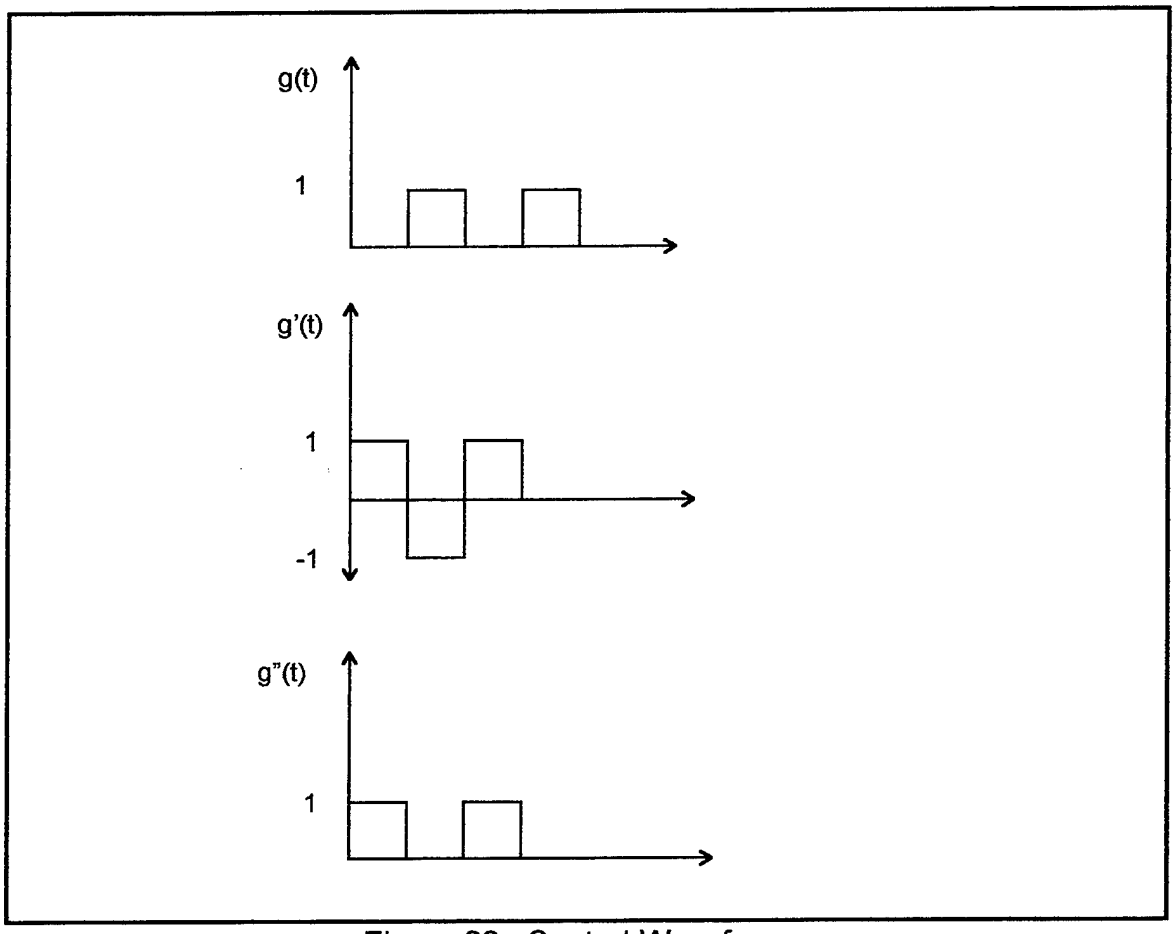

Figure 22. Control Waveforms.

The VCO will then adjust the frequency of oscillation until the frequency that matches the maximum point of punctual correlation is reached. This feedback continues throughout the receipt of the incoming signal, and the demodulator is thus maintained in a tracking mode.

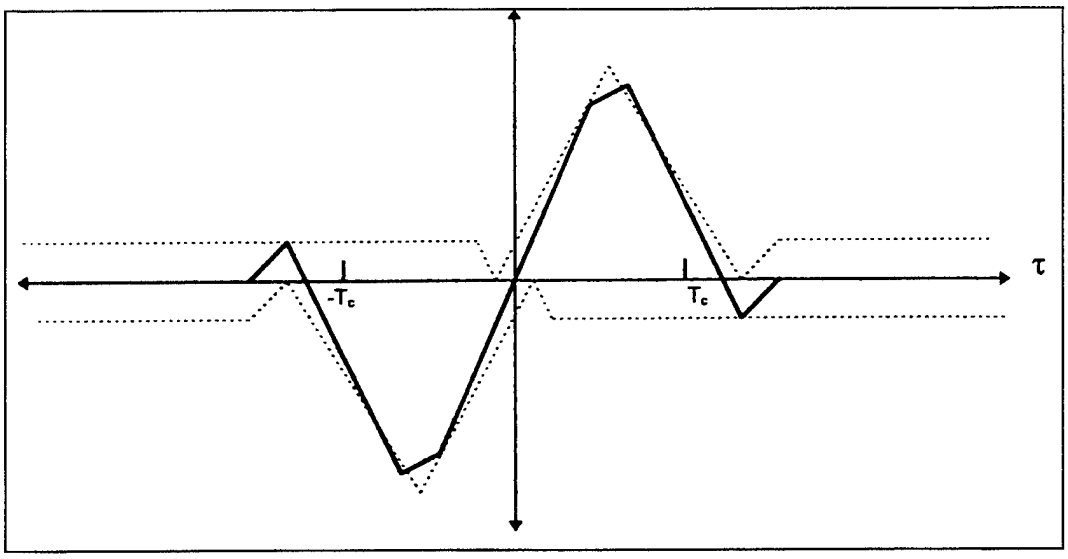

Figure 23. Ideal Correlation Signal [Ref. 4]
(Dotted lines: Early/late correlation signals,
Solid lines: Early minus late correlation signal).

G. FILTERS

The filters which are used in this design need to provide sufficient filtering to help eliminate noise that may interfere with the proper demodulation of the incoming signal.

The design of the filters here dictates an active filter realization using operational amplifiers. Although a majority of the power consumed in this design is attributed to the operational amplifiers that make up the band-pass filters, aspects of this solution may be viable for ground station applications where the power consumption of the modem is not a concern. Passive elements such as crystal filters can be used in a final design if the power is limited. The characteristics of the design remain the same and, as a matter of practicality, the use of operational amplifiers here allows for proof of concept in this design.

The operational amplifiers employed to construct the filters are LM318 operational amplifiers. The second order band-pass filters can be changed to fourth order by cascading a second stage. Appendix C contains the filter response curve for the filters in this design. The basis for the design of the band pass filters is taken from [Ref. 9, 10 and 11].

H. CODE DIVISION MULTIPLE ACCESS

Code division multiple access is an application of spread spectrum techniques. In CDMA, specified members of a set of orthogonal or nearly orthogonal spread spectrum codes, each using the full channel bandwidth, are allocated. Spread spectrum communications provide a degree of privacy. When the code for a particular user group is only distributed among authorized users, the CDMA process provides communications privacy since the transmissions cannot easily be intercepted by unauthorized users without the code. CDMA is also more efficient than other techniques for fading channels and jam resistance. The most important advantage of CDMA schemes is that precise time coordination need not be achieved among the various simultaneous transmitters. The orthogonality between user transmissions on different codes is not affected by transmission-time variations.

The spread spectrum signals shares the same frequency band, and there is a certain amount of crosstalk, or mutual interference. This interference does not make communications impossible, but it effects the performance of the system.

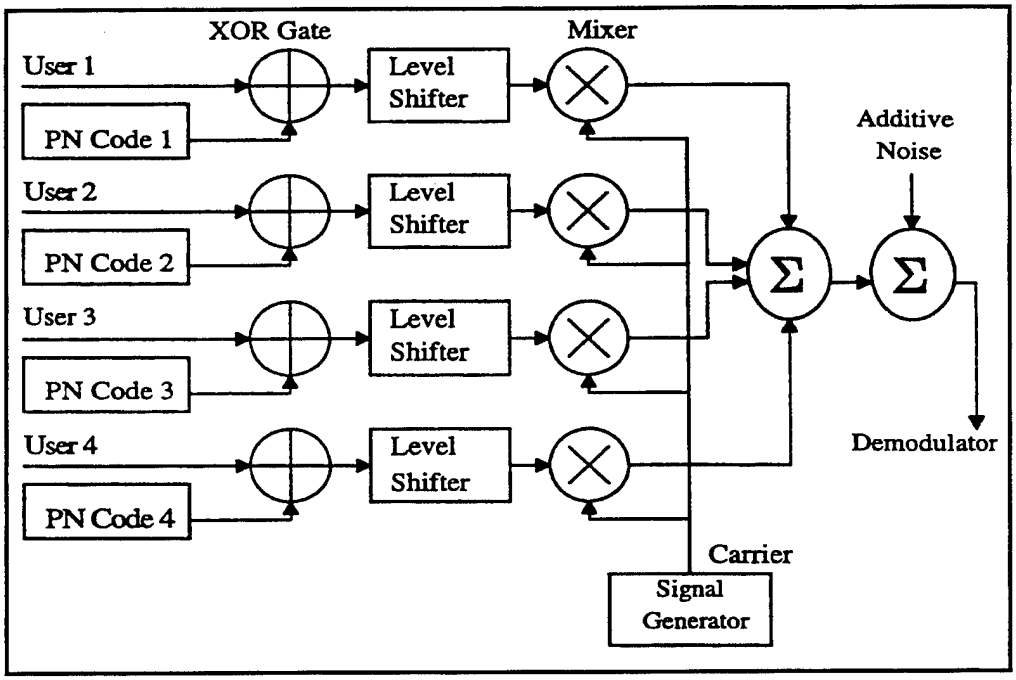

Figure 24. DS/CDMA-DPSK System with Four Users.

In this design, a synchronous DS/CDMA-DPSK system was built for four users. The system block diagram is given in Figure 24.

For multiple-user applications, the information bits are spread by Gold sequences which are the most convenient sequences since they have the smallest cross-correlation values. The set of Gold sequences includes the two preferred-pair of *m*-sequences and modulo 2 sums of the first *m*-sequence and cyclic shifts of the second *m*-sequence. In particular, the set of four Gold sequences is

$$S(\text{Gold})=\{x \oplus y,\ x \oplus T^{-1}y,\ x \oplus T^{-2}y,\ x \oplus T^{-3}y\} \qquad (2.6)$$

where x and y are the preferred pair, $\oplus$ is the modulo-2 sum operator, and T^{-1} is a one bit shift left operator [Ref.6]. The Gold sequences assigned for each user are derived from the different combinations of the preferred pair. The generation of the four PN codes are shown in Figure 25.

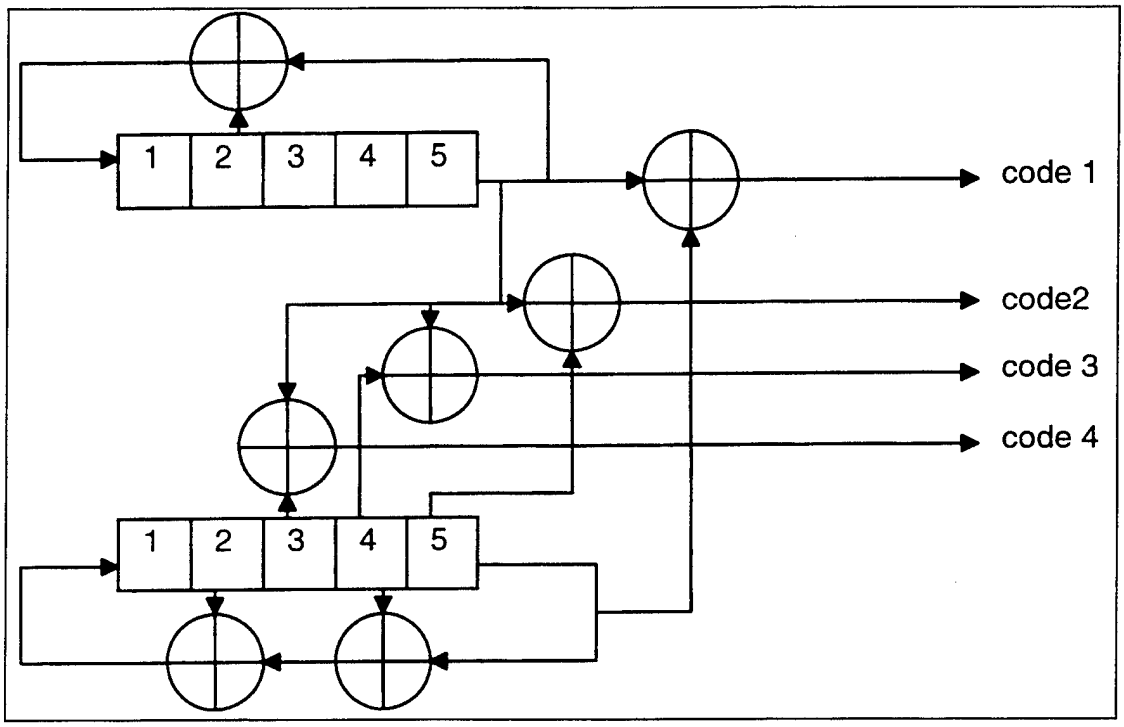

Figure 25. Gold Sequence Generator for the Preferred Pair $f_1(x)=(1+x^2+x^5)$ and $f_2(x)=(1+x^2+x^4+x^5)$.

The performance of a direct sequence CDMA system has been extensively analyzed in both Lam and Ziemer [Ref. 1, 6, 24]. For system design purposes, the Gaussian approximation is extensively used [Ref. 6]. In this design, the multi-user interference is treated as Gaussian noise with zero mean and variance determined by K and N where K is the number of CDMA users and N is the PN code length. This simplifies the analysis greatly because a Gaussian

random variable is completely characterized by its mean and variance. The standard Gaussian approximation for bit error probability for CDMA/DPSK is given by [Ref. 6]:

$$P_b \cong 2 \cdot Q\left(\left[\frac{K-1}{3N} + \frac{N_0}{2E_b}\right]^{-1/2}\right) \tag{2.7}$$

where E_b is the bit energy, $\frac{N_0}{2}$ is the AWGN power spectral density, K is the number of CDMA users, N is the PN code length, and $Q(\cdot)$ is the Q-function.

A more accurate formula, the improved Gaussian approximation, is given by [Ref. 6]:

$$P_b \cong \frac{4}{3}Q\left(\left[\frac{K-1}{3N} + \frac{N_0}{2E_b}\right]^{-1/2}\right) + \frac{1}{3}Q\left(\left[\frac{K-1}{3N} + \frac{\sqrt{3}c}{N^2} + \frac{N_0}{2E_b}\right]^{-1/2}\right) + \frac{1}{3}Q\left(\left[\frac{K-1}{3N} - \frac{\sqrt{3}c}{N^2} + \frac{N_0}{2E_b}\right]^{-1/2}\right) \tag{2.8}$$

where

$$c^2 = (K-1)\left[N^2\frac{23}{360} + N\left(\frac{1}{20} + \frac{K-2}{36}\right) - \frac{1}{20} - \frac{K-2}{36}\right] \tag{2.9}$$

In the next chapter, the P_b obtained with the improved Gaussian approximation (Equation 2.8) is compared with experimental measurements.

III. EXPERIMENTAL RESULTS

First, the performance of the DPSK system without the PN code is tested using BER equipment. When the amplitude A is adjusted to a value of 0.4V, the energy per bit is calculated from

$$E_b = \frac{A^2 T}{2} \tag{3.1}$$

and found to be -41.6 dB where T is the bit duration.

The information data and the received data were connected to the BER equipment (1645A Data Error Analyzer) so that errors could be counted digitally [Ref.7].

To calculate the bit energy-to-noise density ratio (E_b/N_o), the noise power spectral density N_o is estimated at high BER where noise dominates receiver performance. Bit error rate is measured via BER equipment (HP1645A). Since the exact signal power is known, the noise power spectral density (N_o) can be approximated by using the BER of DPSK with coherent detection at a high BER (Ref.26):

$$\text{BER}=2Q\left(\sqrt{\frac{2E_b}{N_o}}\right)\left[1-Q\left(\sqrt{\frac{2E_b}{N_o}}\right)\right] \tag{3.2}$$

The measurement of N_o was carried out at BER$\cong 10^{-3}$. The one-sided noise power spectral density N_o is found to be 1.39×10^{-5} W/Hz, and this result is used to find E_b/N_o for subsequent BER measurements. When comparing the experimental error performance of the DPSK modem with the theoretical results, for the same P_b the experimental values are approximately 0.5 dB more than theoretical values as shown in Figure 26.

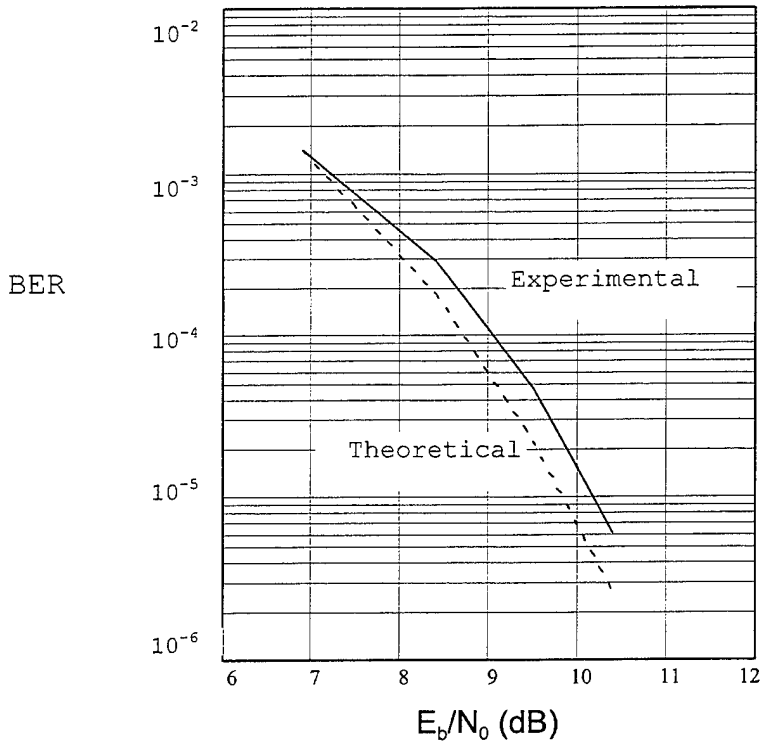

Figure 26. The Experimental and Theoretical DPSK Bit Error Rate (BER) Curves.

The multi-user performance for K=1,2,3, and 4 is shown in Table 3.1 and plotted in Figure 27. For the first performance test, only one user is employed (K=1) and multi-user interference is not present. The second set of

measurements is performed with 2, 3, and 4 users. All channels corresponding to the each user are summed by a non-inverting adder (LM 741), and the same carrier power is applied to the each mixer before the adder (Figure 24).

	E_b/N_0 (dB)			
	6.9(dB)	8.4(dB)	9.5(dB)	10.4(dB)
DPSK (Experimental)	1.4×10^{-3}	2.9×10^{-4}	4.7×10^{-5}	6.1×10^{-6}
K=1	2×10^{-3}	3.7×10^{-4}	6.3×10^{-5}	8.4×10^{-6}
K=2	3×10^{-3}	8.8×10^{-4}	2×10^{-4}	4.1×10^{-5}
K=3	6.3×10^{-3}	1.9×10^{-3}	5×10^{-4}	1.3×10^{-4}
K=4	1×10^{-2}	4.2×10^{-3}	1.5×10^{-3}	6.5×10^{-4}

Table 3.1. Experimental Bit Error Rates of DS-CDMA/DPSK System.

Results obtained with the improved Gaussian approximation (Equation 2.8) are also shown in Figure 27. It is noted that at BER$\approx 10^{-3}$ there is a degradation in E_b/N_o of about 0.5dB for the experimental DS-CDMA/DPSK system. At BER=10^{-4} the degradation is about 0.3 dB for K=2 and 3. The experimental results agree well with the improved Gaussian approximation taking into account receiver imperfections such as filtering in the demodulator.

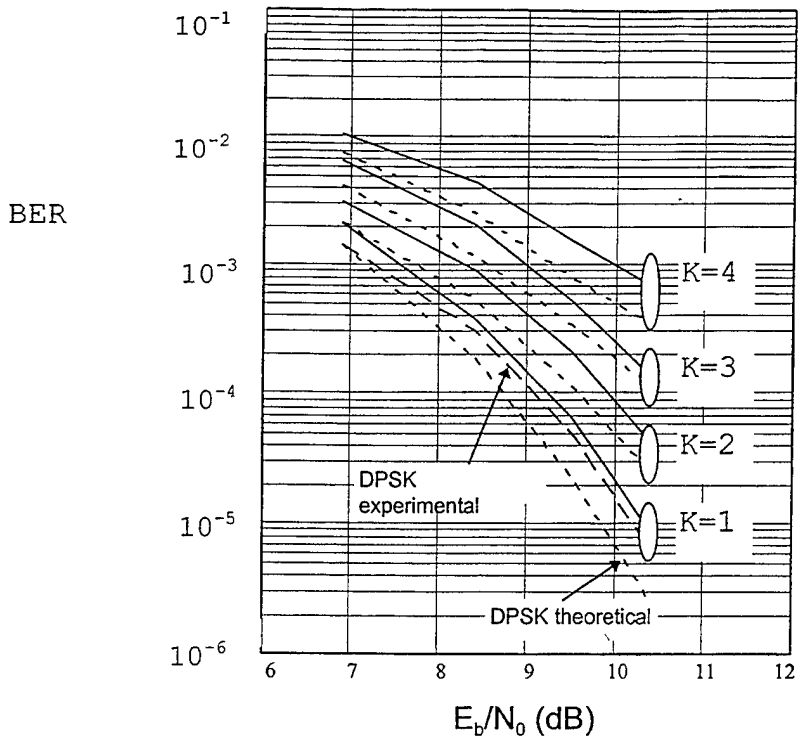

Figure 27. Theoretical and Experimental Bit Error Rate Curves for DS-CDMA/DPSK System. (Dotted curves show the theoretical results and solid curves show the experimental results for CDMA/DPSK). (The long-dashed curve shows the experimental DPSK Bit Error Rate curve without any PN code).

IV. MULTI-USER INTERFERENCE CANCELLATION

Although CDMA offers the convenience of no frequency and/or time coordination as required by frequency-division multiple access (FDMA) or time-division multiple access (TDMA), its bandwidth efficiency is rather low. The low bandwidth efficiency results from the multi-user interference. As seen from the standard Gaussian approximation (Equation 2.7) or the improved Gaussian approximation (Equation 2.8), the number of users K is limited for a specified bit error probability even as E_b/N_o approaches infinity. At $P_b=10^{-4}$ the limiting number of users K is given in Table 4.1. The bandwidth efficiency is defined as K/N [Ref.6].

N	K	BANDWIDTH EFFICIENCY
31	8	0.26
63	15	0.24
127	29	0.23
255	57	0.22

Table 4.1. Number of users K versus PN code length N for $E_b/N_o \rightarrow \infty$ and $P_b= 10^{-4}$.

From Table (4.1), we see that CDMA bandwidth efficiency is rather low compared to that of TDMA which is between 0.80-0.95 or that of FDMA which is between 0.60-0.70 [Ref.19].

CDMA bandwidth efficiency can be improved if the multi-user interference can somehow be reduced. In the following section, a multi-user interference cancellation circuit is proposed, shown in Figure 28, that can nullify the interference for K=2 users. The purpose is to use the knowledge of the other user's PN sequence to cancel out its effect. This is applicable to a network where PN sequences are not used to provide privacy. Applications such as wireless communications for warehouses or retailers may fit this description.

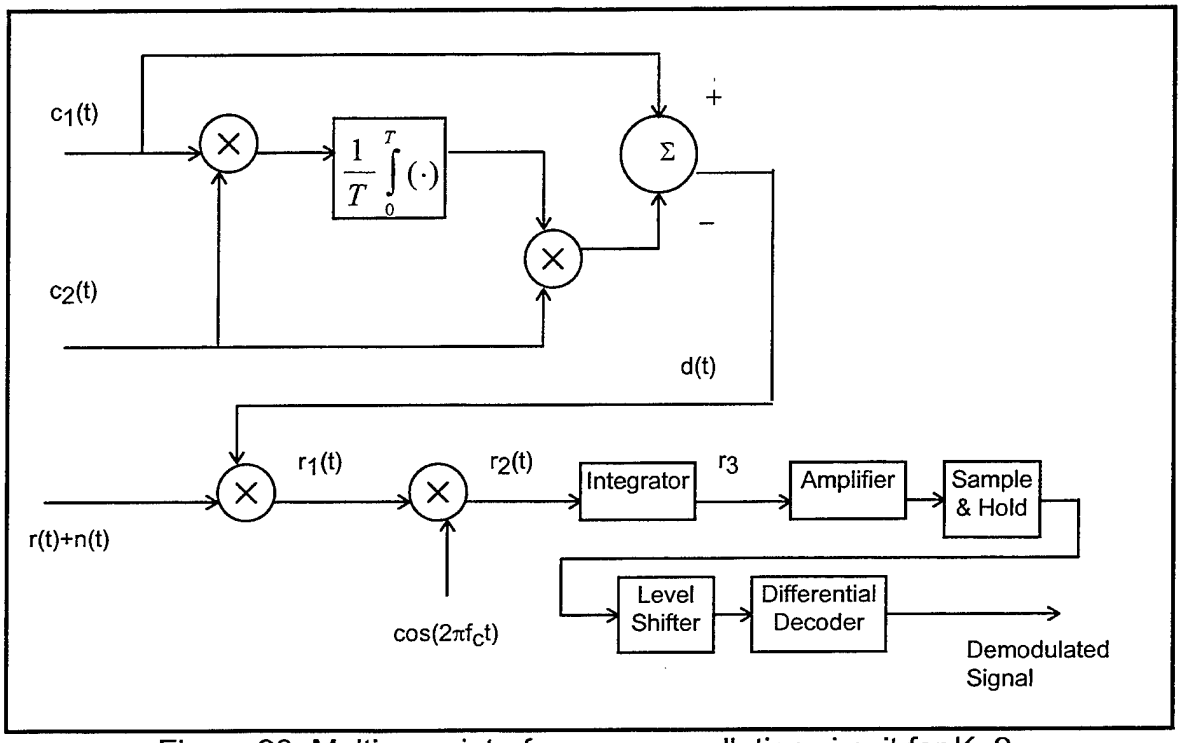

Figure 28. Multi-user interference cancellation circuit for K=2.

The circuit in Figure 28 is analyzed in the subsequent discussion. Let r(t) be the received synchronous DS-CDMA/DPSK signal plus AWGN n(t) with power spectral density $N_o/2$ (W/Hz):

$$r(t) = A_1 b_1 p_T(t) c_1(t) \cos(2\pi f_c t) + A_2 b_2 p_T(t) c_2(t) \cos(2\pi f_c t) + n(t) \qquad (4.1)$$

where A_1 and A_2 are the amplitudes of the synchronous DS-CDMA/DPSK signals of user 1 and 2, respectively, b_1 and $b_2 \in \{\pm 1V\}$, $p_T(t)$ is the unit pulse of duration T, and $c_1(t)$ and $c_2(t)$ are the PN codes of users 1 and 2, respectively, with amplitudes $\pm 1V$ and period T.

The received signal r(t) is despread by the signal d(t) given by

$$d(t) = c_1(t) - \alpha_{12}c_2(t) \tag{4.2}$$

where α_{12} is the cross-correlation between the PN code $c_1(t)$ of the intended user 1 and the PN code $c_2(t)$ of the interfering user 2:

$$\alpha_{12} = \frac{1}{T}\int_0^T c_1(t)c_2(t)dt \tag{4.3}$$

The output of the multiplier in Figure 28 is given by

$$\begin{aligned} r_1(t) &= r(t)d(t) \\ &= [A_1b_1p_T(t)c_1(t)\cos 2\pi f_c t + A_2b_2p_T(t)c_2(t)\cos 2\pi f_c t + n(t)]\,[c_1(t) - \alpha_{12}c_2(t)] \\ &= [A_1b_1p_T(t)c_1^2(t) - \alpha_{12}A_1b_1p_T(t)c_1(t)c_2(t) + A_2b_2p_T(t)c_1(t)c_2(t) \\ &\quad - \alpha_{12}A_2b_2p_T(t)c_2^2(t)]\cos 2\pi f_c t + c_1(t)n(t) - \alpha_{12}c_2(t)n(t) \end{aligned} \tag{4.4}$$

The signal $r_1(t)$ is then coherently demodulated to give $r_2(t)$ as

$$r_2(t) = [A_1b_1p_T(t)c_1^2(t) - \alpha_{12}A_1b_1p_T(t)c_1(t)c_2(t) + A_2b_2p_T(t)c_1(t)c_2(t) - \alpha_{12}A_2b_2p_T(t)c_2^2(t)]$$

$$\left[\frac{1}{2} + \frac{1}{2}\cos 4\pi f_c t\right] + c_1(t)n(t)\cos 2\pi f_c t - \alpha_{12}c_2(t)n(t)\cos 2\pi f_c t \quad (4.5)$$

The decision variable r_3 is obtained by integrating $r_3(t)$ over one bit period T. Since the integrator rejects the second harmonic at $2f_c$, we get

$$r_3 = \frac{1}{2}A_1b_1\int_0^T c_1^2(t)dt - \frac{1}{2}\alpha_{12}A_1b_1\int_0^T c_1(t)c_2(t)dt + \frac{1}{2}A_2b_2\int_0^T c_1(t)c_2(t)dt$$

$$- \frac{1}{2}\alpha_{12}A_2b_2\int_0^T c_2^2(t)dt + N \quad (4.6)$$

where

$$N = \int_0^T \left[c_1(t) - \alpha_{12}c_2(t)\right]n(t)\cos 2\pi f_c t \cdot dt \quad (4.7)$$

Since $\int_0^T c_1^2(t)dt = \int_0^T c_2^2(t)dt = T$, from Equation (4.6) we get

$$r_3 = \frac{1}{2}A_1Tb_1 - \frac{1}{2}\alpha_{12}^2A_1Tb_1 + \frac{1}{2}\alpha_{12}A_2Tb_2 - \frac{1}{2}\alpha_{12}A_2Tb_2 + N = \frac{1}{2}A_1Tb_1(1-\alpha_{12}^2) + N \quad (4.8)$$

The decision variable r_3 is a Gaussian random variable with mean $E\{r_3\}=\frac{1}{2}A_1Tb_1(1-\alpha_{12}^2)$ and variance σ^2 which can be calculated as follows:

$$\sigma^2=E\{N^2\}=\int_0^T\int_0^T\left[c_1(t)-\alpha_{12}c_2(t)\right]\left[c_1(\tau)-\alpha_{12}c_2(\tau)\right]E\{n(t)n(\tau)\}\cos 2\pi f_c t\cos 2\pi f_c\tau\cdot d\tau dt$$

$$=\int_0^T\int_0^T\frac{N_0}{2}\delta(t-\tau)\left[c_1(t)-\alpha_{12}c_1(t)\right]\left[c_1(\tau)-\alpha_{12}c_2(\tau)\right]\cos 2\pi f_c t\cos 2\pi f_c\tau\cdot d\tau dt$$

$$=\frac{N_0}{2}\int_0^T\left[c_1(t)-\alpha_{12}c_2(t)\right]^2\cos^2 2\pi f_c t dt$$

$$=\frac{N_o}{2}\int_0^T\left[c_1^2(t)-2\alpha_{12}c_1(t)c_2(t)+\alpha_{12}^2c_2^2(t)\right]\cdot\left[\frac{1}{2}+\frac{1}{2}\cos 2\pi f_c t\right]dt$$

$$=\frac{N_o}{4}\left(T-2\alpha_{12}^2T+\alpha_{12}^2T\right)=\frac{N_oT}{4}\left(1-\alpha_{12}^2\right) \qquad (4.9)$$

Note that the high frequency terms are very small and can be ignored. The bit error probability based upon the Gaussian random variable r_3 can be shown to be [Ref. 2]:

$$P_b=2Q\left(\sqrt{\frac{E\{r_3\}^2}{\sigma^2}}\right)=2Q\left(\sqrt{\left(\frac{A_1^2T}{N_0}\left(1-\alpha_{12}^2\right)\right)}\right)=2Q\left(\sqrt{\frac{2E_1}{N_o}(1-\alpha_{12}^2)}\right) \qquad (4.10)$$

where $E_1=\frac{A_1T}{2}$ is the bit energy of user 1.

For Gold codes with $n=2^m-1$, the normalized cross-correlation α_{12} is bounded by [Ref.6]:

$$|\alpha_{12}| \le \frac{1+2^{\left\lfloor \frac{m+2}{2} \right\rfloor}}{2^m-1} \tag{4.11}$$

where $\lfloor x \rfloor$ is the integer part of x. For n=31, $|\alpha_{12}| \le \left(\frac{1+2^{\left\lfloor \frac{(5+2)}{2} \right\rfloor}}{31} \right) = \left(\frac{9}{31} \right)$. Using this value of $|\alpha_{12}|$ in Equation (4.11), we see that the interference cancellation circuit reduces $\frac{E_b}{N_o}$ by a factor of $(1-\alpha_{12}^2)=1-\left(\frac{9}{31}\right)^2$ = 0.916 or -0.38 dB. This small reduction in signal-to-noise ratio is fixed no matter how large the amplitude A_2 of the DS-CDMA/DPSK signal of user 2 compared to A_1 of the DS-CDMA/DPSK signal of user 1. This is certainly interesting for situations where one user is closer to the base station than the other. No power control is necessary to avoid the near-far effect. In conclusion, the multi-user interference cancellation circuit can significantly improve performance for two users even when they have different received powers.

The performance improvement of the CDMA system with the interference cancellation circuit is tested with K=2 where the signal power of the interfering user 2 is equal to three times the signal power of the intended user 1 ($P_2=3P_1$).

The despreading code d(t) is generated by the interference cancellation circuit is shown in Figure 28. The experimental BER measurements are plotted in Figure 29. Also shown in Figure 29 for comparison are the BER curve for K=2 with $P_2=3P_1$ without the interference cancellation circuit and the theoretical BER curve from (Equation 4.10).

From Figure 29, we observe that the performance of DS-CDMA/DPSK with the interference cancellation circuit for K=2 users and $P_2=3P_1$ is within 0.5dB of the theoretical curve obtained with (Equation 4.10). The improvement over the case of 2 users without the interference cancellation circuit and $P_2=3P_1$ is about 2 dB at BER $\cong 10^{-3}$.

The idea of multi-user interference cancellation can be extended to more than two users, although the required circuitry is much more complex. For example, for K=3 users we need the cancellations between users 1 and 2, 1 and 3, and 2 and 3. Thus, the despreading signal d(t) (Equation 4.2) must be chosen accordingly. The order of complexity increases as K grows. One possible solution is to despread all K signals simultaneously and process the K samples which include multi-user interference with a Digital Signal Processing (DSP) chip that uses a priori knowledge of the K codes to cancel out the interference. This question is for future research.

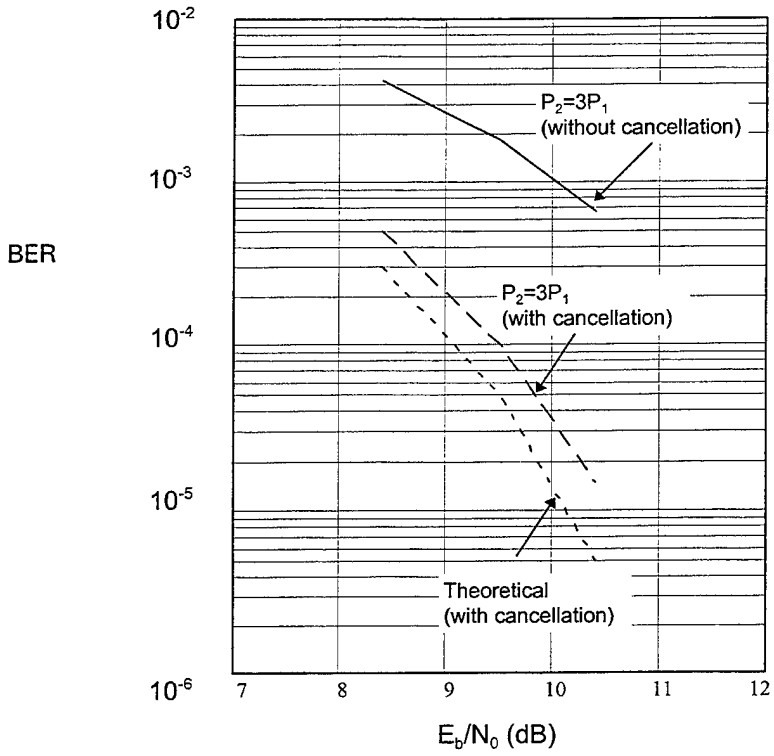

Figure 29. The DPSK Bit Error Rate (BER) Curves for K=2 with $P_2=3P_1$.

V. CONCLUSIONS

The best known and commonly used spread spectrum systems for CDMA applications are direct sequence systems. This thesis presents the design and testing of a DS-CDMA/DPSK system. Its multi-user performance is tested for up to four users. The multi-user performance of the modem approximates the theoretical results closely. The multi-user interference cancellation circuit is designed to nullify the interference for two users and its performance improvement is proven theoretically and experimentally. In order to obtain results that are more precise and practical, the following points are suggested:

1. A more accurate bit error analyzer should be used for the laboratory tests.
2. Higher data rates and processing gains can be used. However, high speed components with lower tolerances are required for this modification.
3. A module producing the required wave forms through a crystal oscillator and division chains can replace the signal generators.
4. By today's standards, this preliminary hardware design is power inefficient. The least power efficient variety of TTL components were utilized and were selected solely because of availability. Conversion of all 7400 series components to their 74LS00 equivalents would result in some power savings.

5. The tau-dither loop eliminates the problem of matching the characteristics of the two correlator branches. Unmatched branches can degrade performance. However, the signal power in the tau-dither loop is 3 dB smaller than that in the delay lock loop and accordingly the jitter is larger. If an efficient solution can be implemented to this problem, better performance can be obtained from the experimental results. Also, for better performance, special boards and crystal filters can be used in the modem design.

APPENDIX A. BLOCK DIAGRAMS

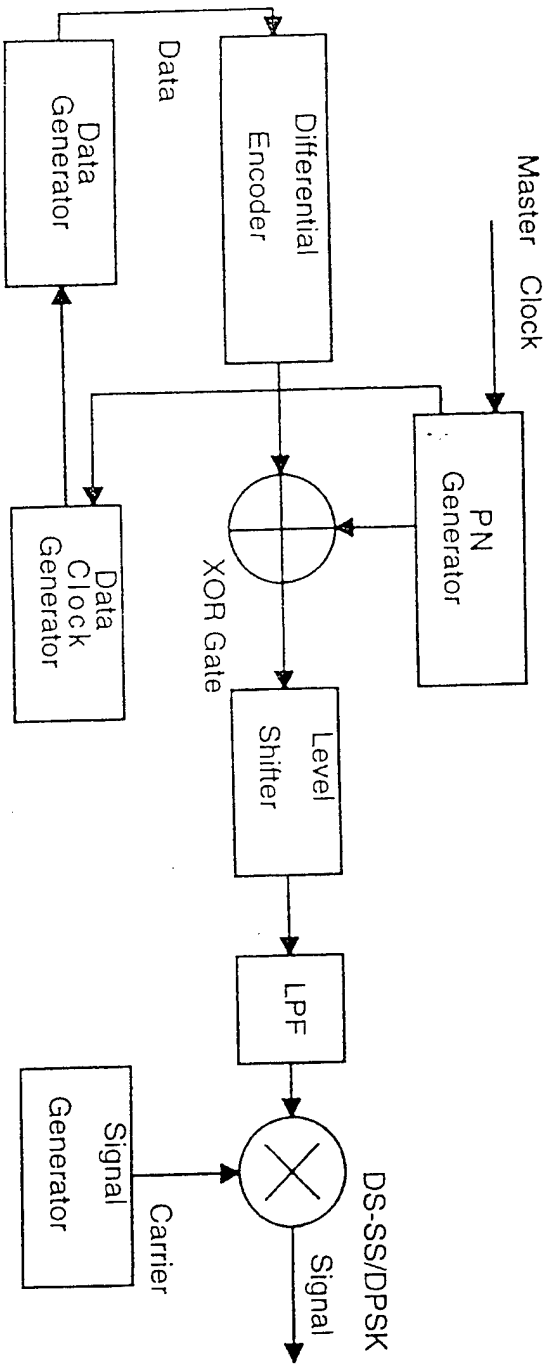

Figure A.1. The Functional Block Diagram of the DPSK Modulator

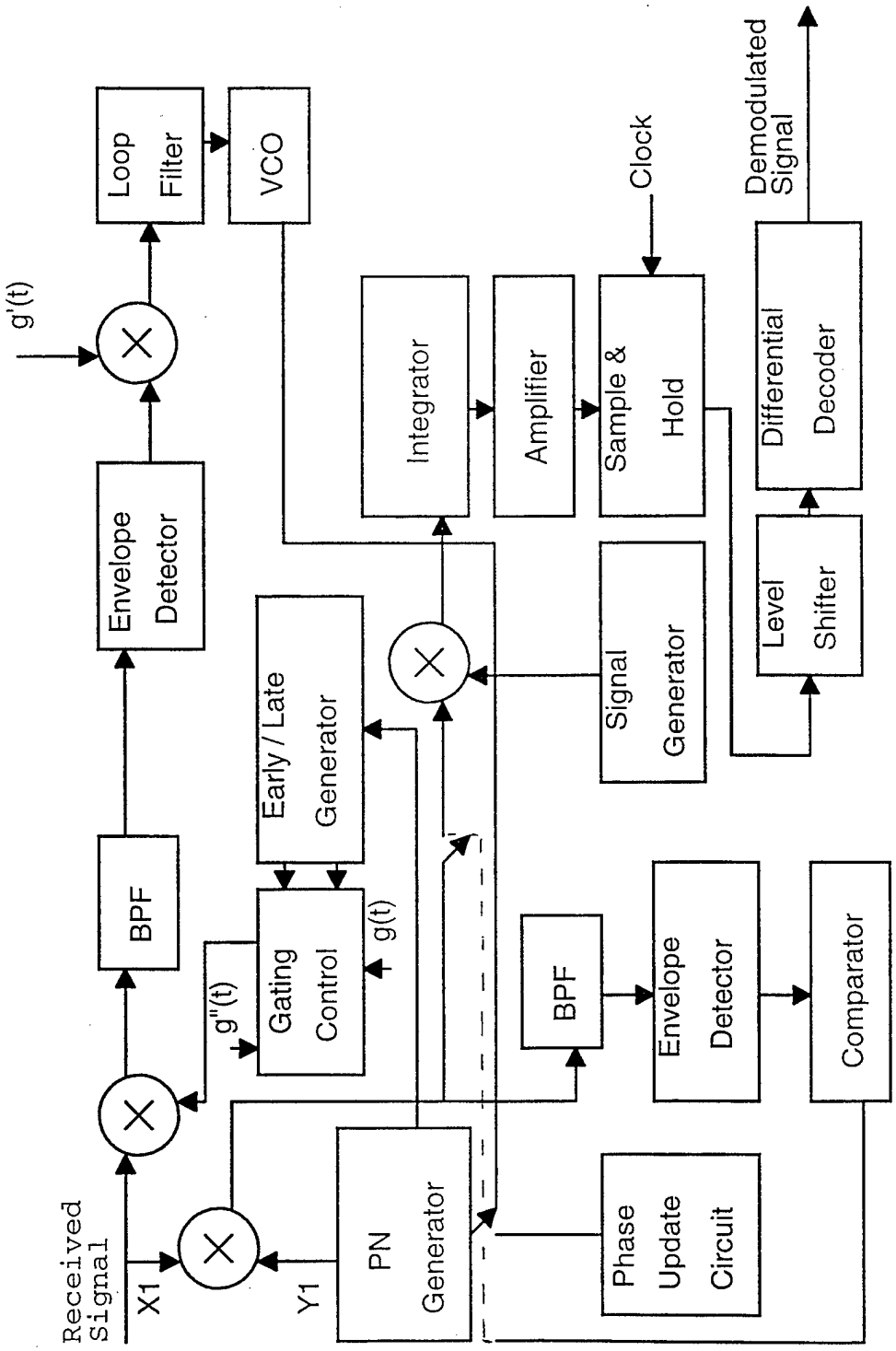

Figure A.2. The Functional Block Diagram of the DPSK Demodulator

APPENDIX B. CIRCUITS

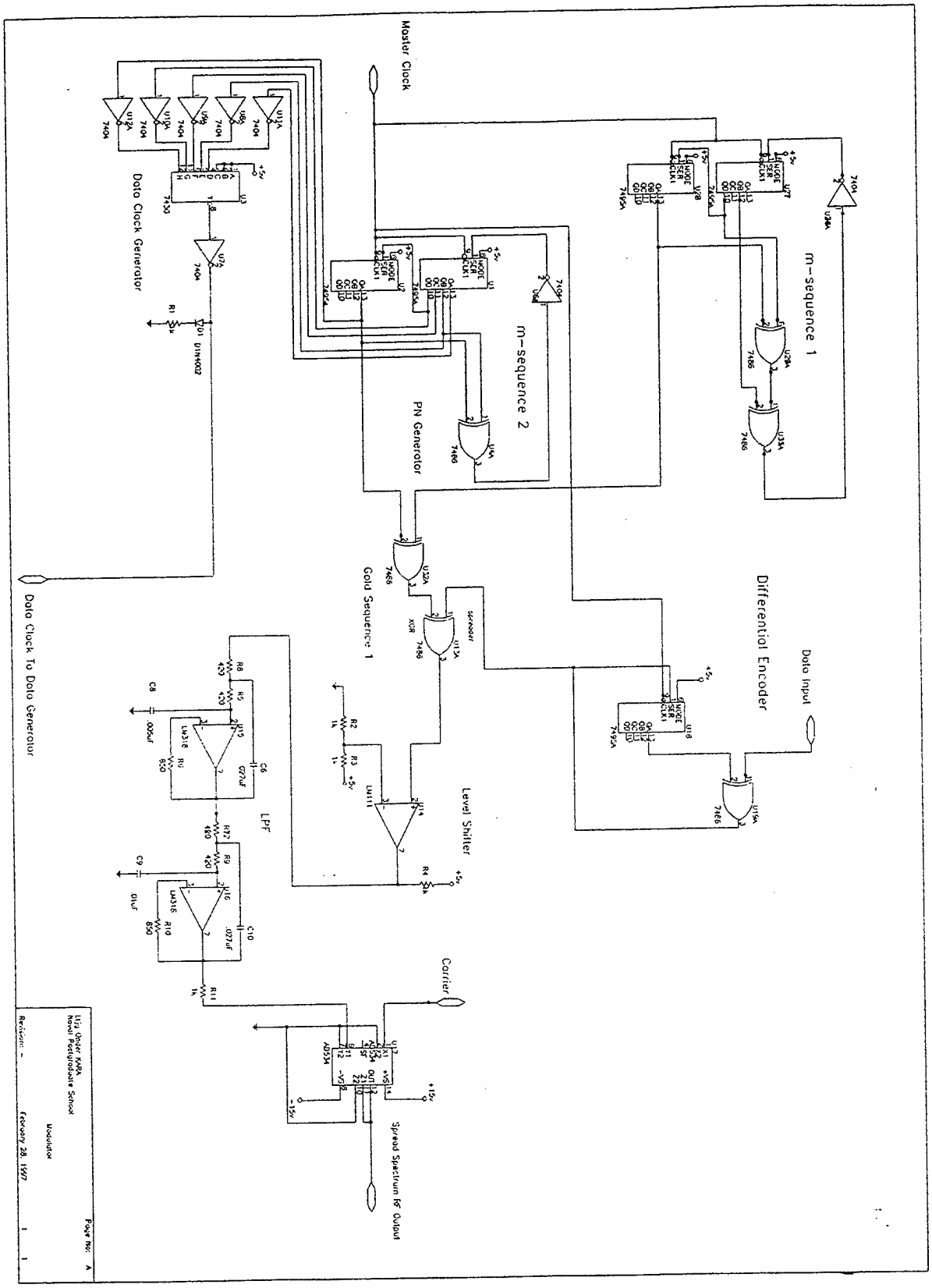

Figure B.1. Modulator Schematic

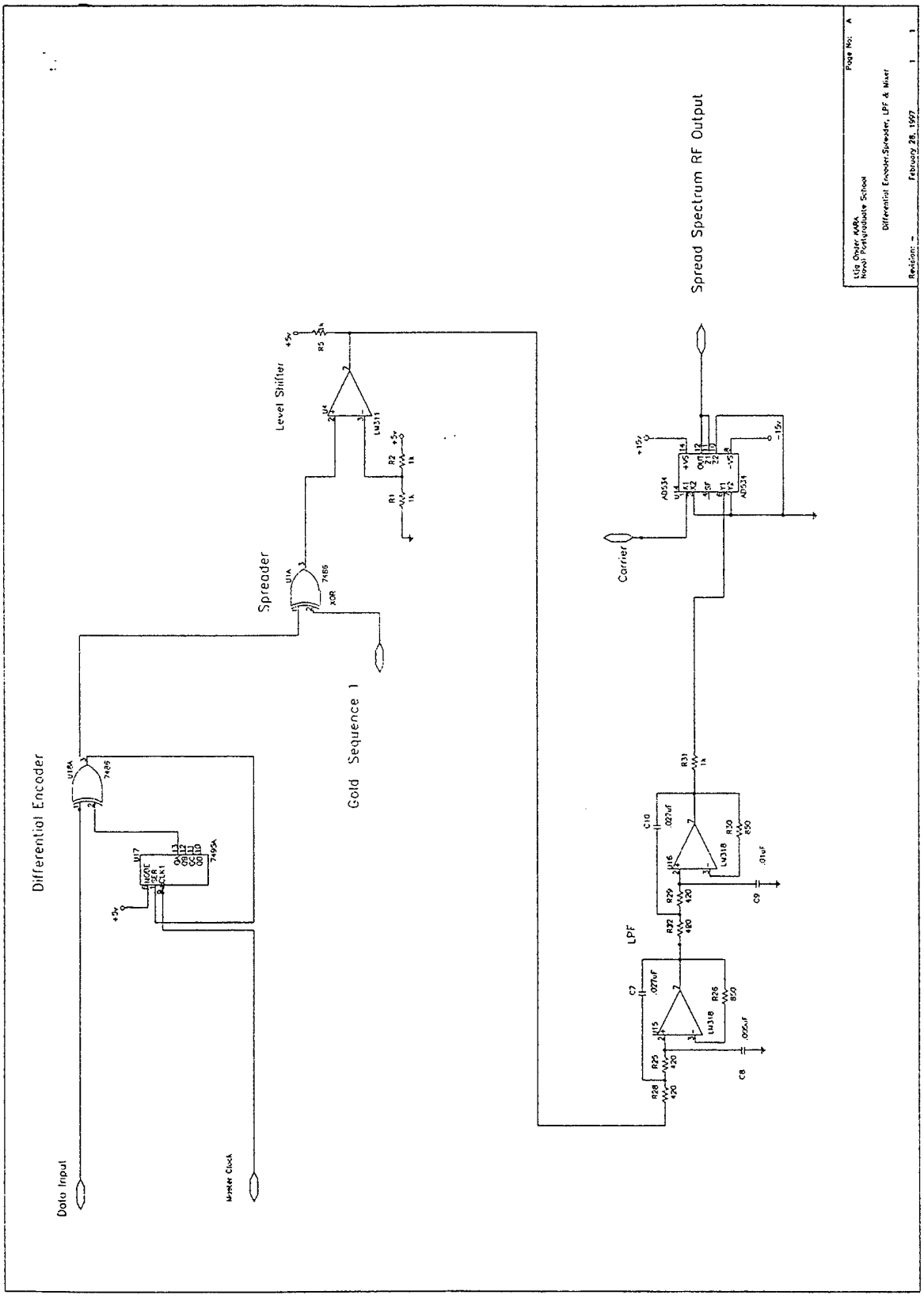

Figure B.2. Differential Encoder, Spreader, LPF and Mixer

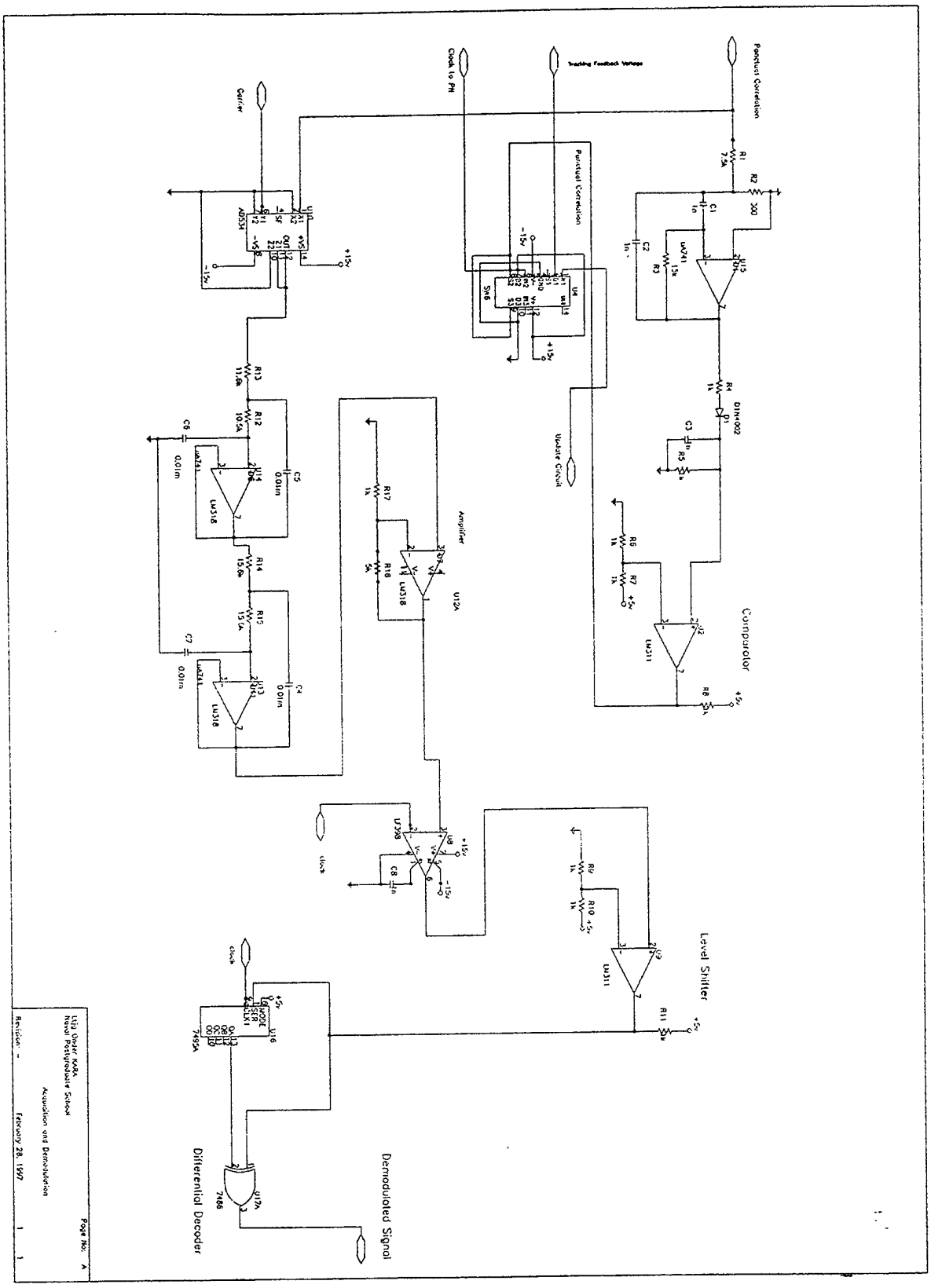

Figure B.3. Acquisition and Demodulation

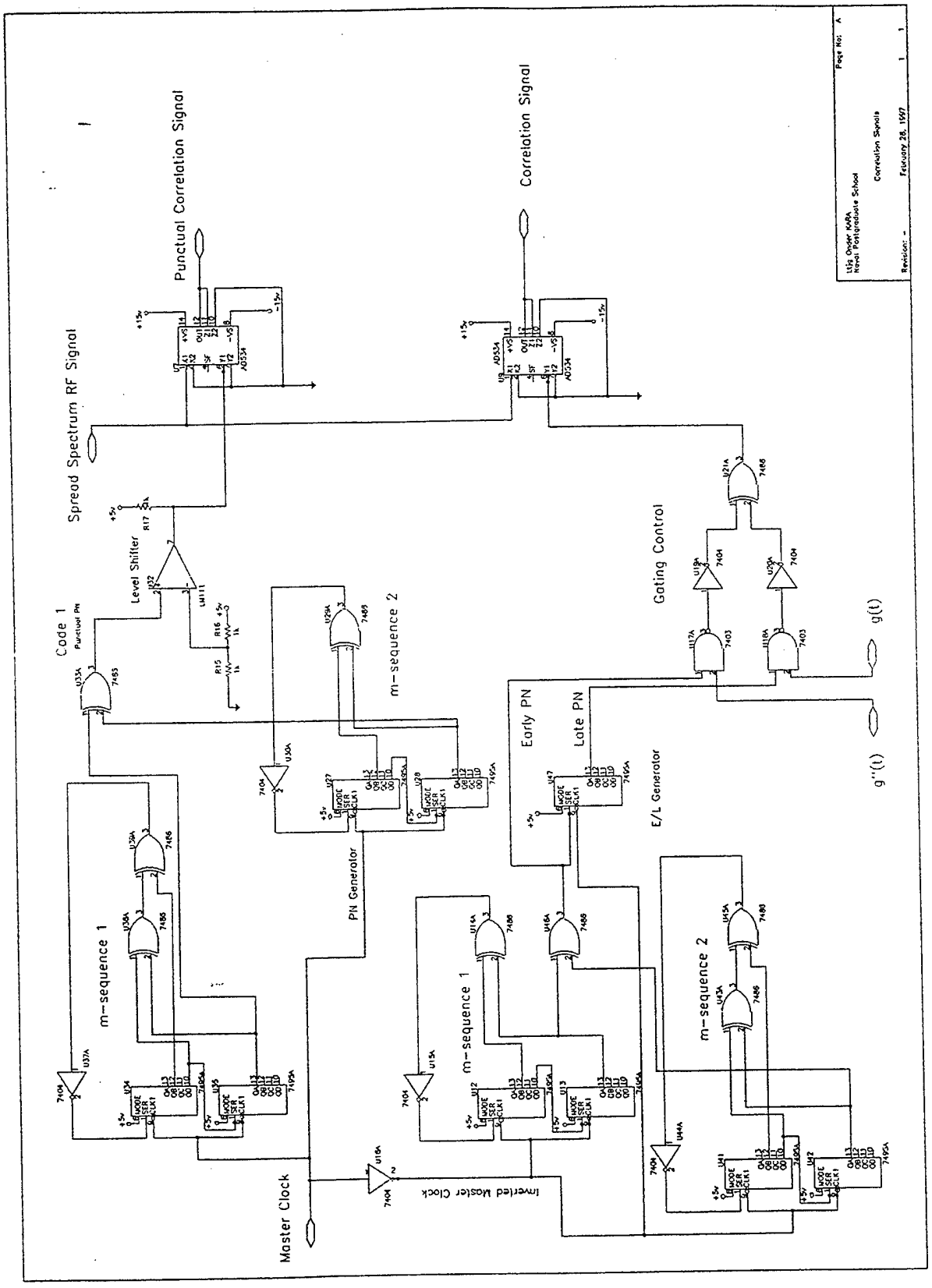

Figure B.4. Correlation Signals

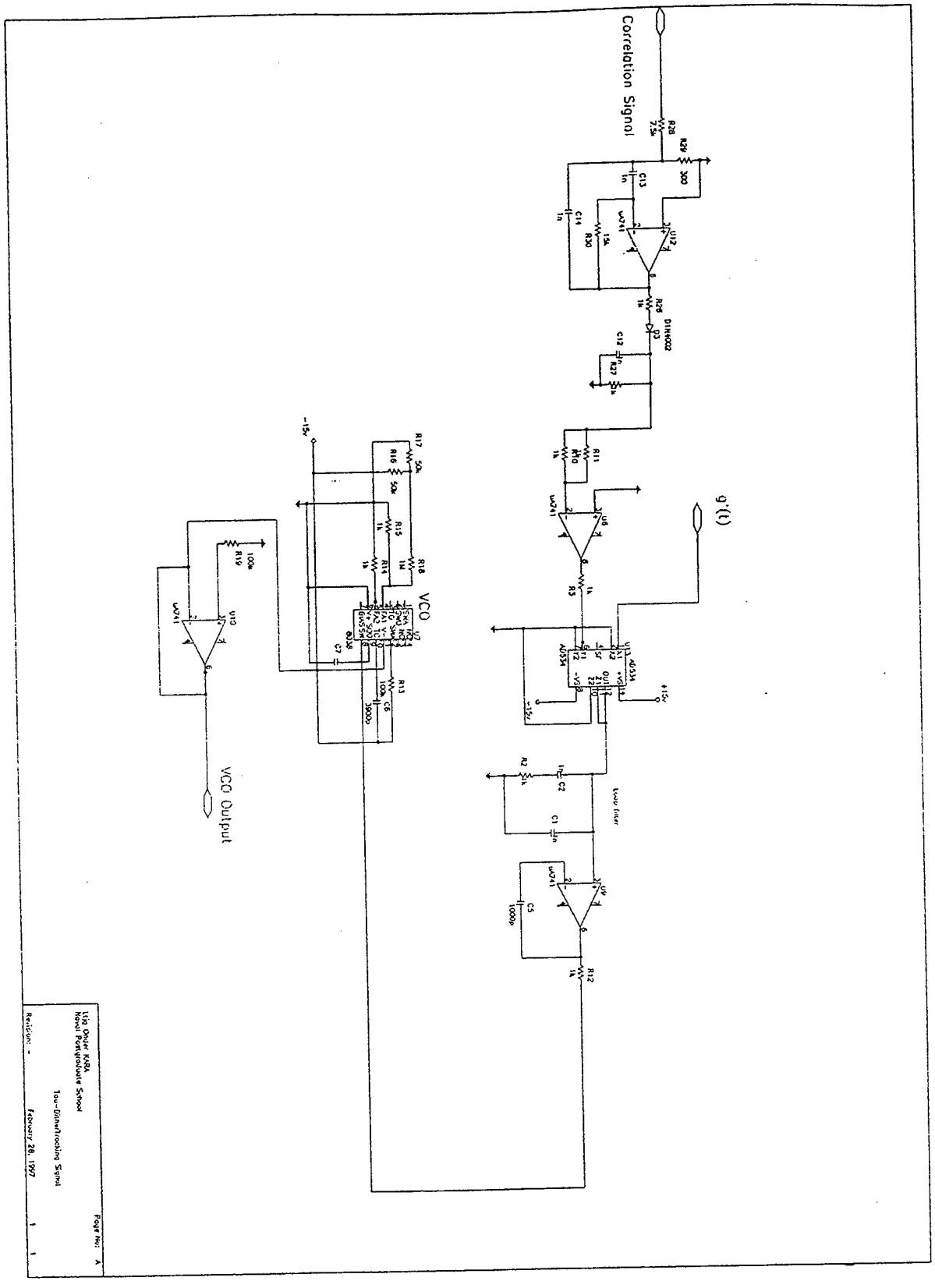

Figure B.5. Tau-Dither Tracking Signal

APPENDIX C. THE DESIGN OF THE BAND PASS FILTER

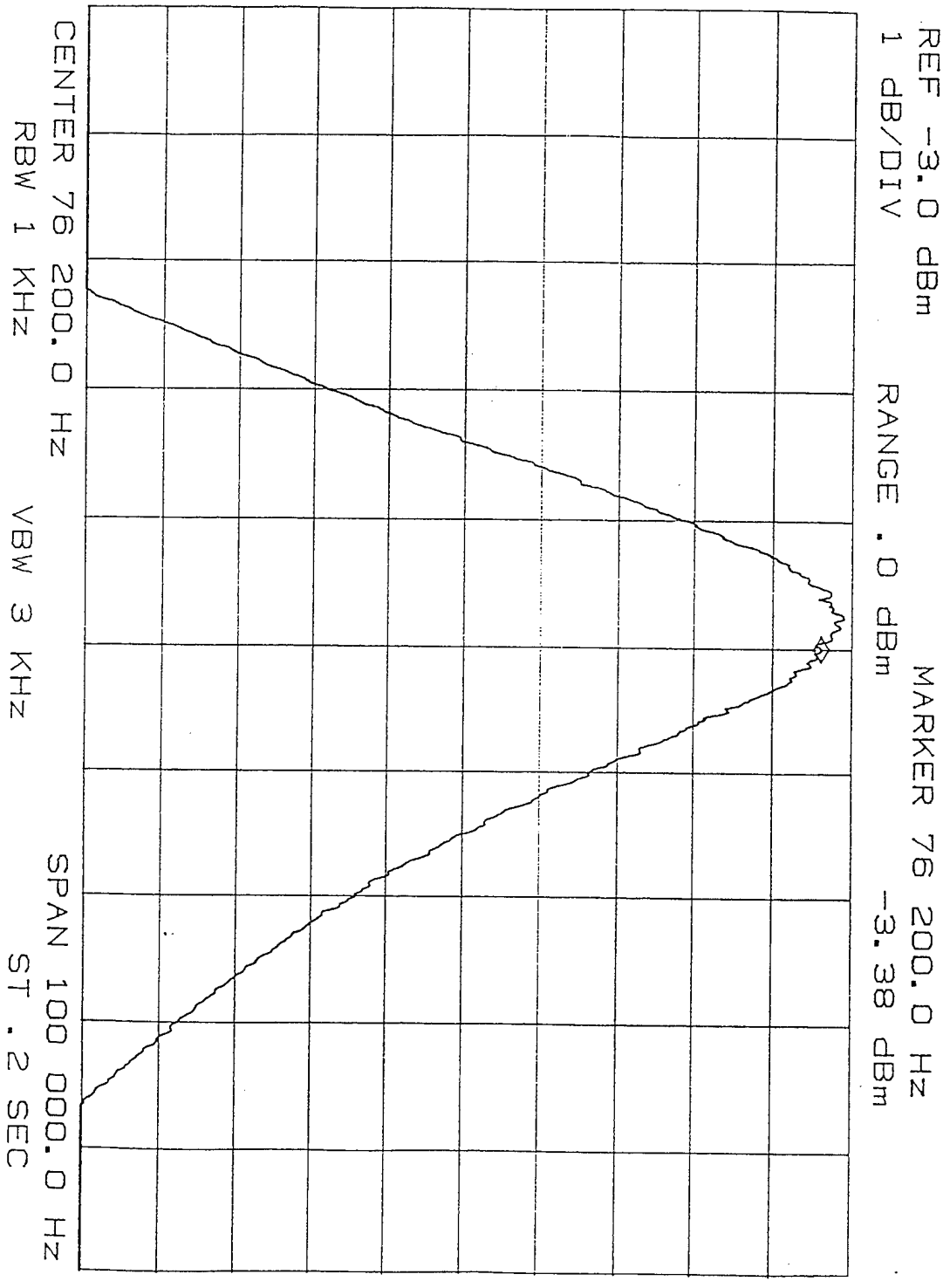

Figure C.1. The Frequency Response of the Band Pass Filter

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