TRW

Monthly Report for

12-Bit High Dynamic Range ADC

Reporting Period: 15 December 1997 to 15 January 1998

NRL Contract No. N00014-97-C-2033

TRW Sales No. 67219

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1.0 Technical Progress

During this reporting period, detailed layout of the ADC chip continued, and final circuit simulations with major interconnect parasitics are in progress. A program review was held on December 18, 1998. A detailed technical summary of of the ADC chip and subsystem design was presented. No major action items were recorded at the program review. Figures 1 through 5 are selected charts from the review presentation material (ADC overview chart, ADC development schedule, ADC chip preliminary floorplan, ADC calibration subsystem block diagram, and ADC requirements versus capabilities table).

2. Plans for Next Reporting Period

During the next reporting period, the detailed chip layout and circuit simulations will continue.

3. Financial Status

The attached table shows the forecasted versus actual expenditures for the Phase 1 program. At month-end December, 1997 we are showing a deviation from forecast of $37.2K (out of a cumulative actual of $356K, or about 10%). This was due to the addition of a senior digital designer to assist in the conceptual design of the ADC subsystem, as well as preparation time for the December review.

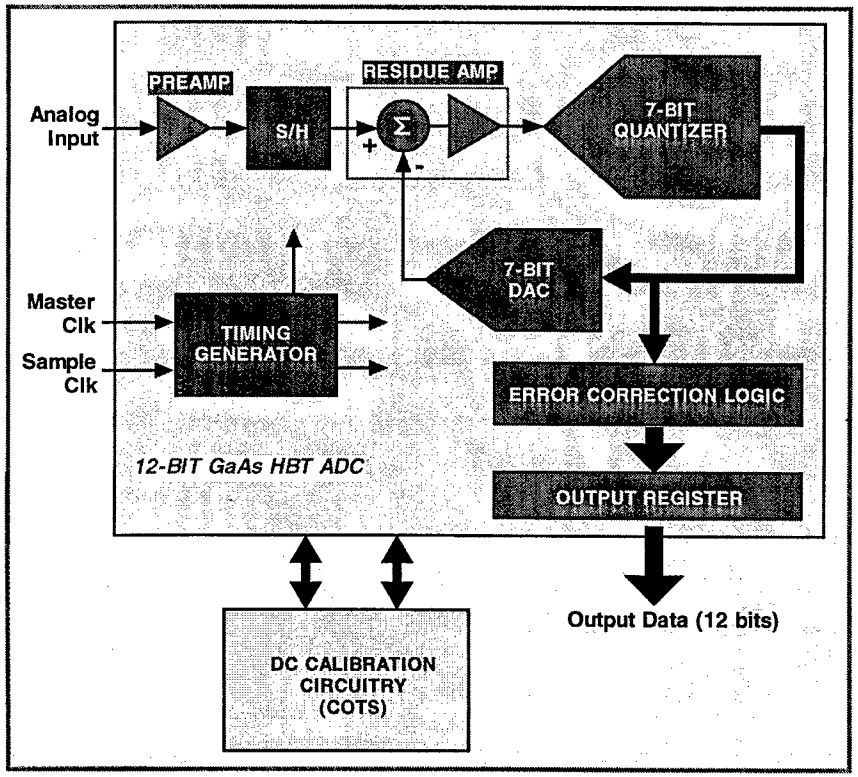
Table 1. Program Expenditures Forecast

Month	Monthly Total ($K)	Cumulative Total ($K)	Cumulative Actuals ($K)	Delta (Forecast - Actuals)
Jun-97	5.3	5.3	2.3	3.0
Jul-97	35.7	41.0	26.4	14.6
Aug-97	42.4	83.4	65.6	17.8
Sep-97	40.7	124.1	127.8	-3.7
Oct-97	81.1	205.2	203.6	1.6
Nov-97	58.4	263.6	268.1	-4.5
Dec-97	55.2	318.8	356.0	-37.2
Jan-98	89.1	407.9		
Feb-98	73.0	480.9		
Mar-98	75.7	556.6		
Apr-98	121.8	678.4		
May-98	64.6	743.0		
Jun-98	73.7	816.7		
Jul-98	103.4	920.1		
Aug-98	77.8	997.9		
Sep-98	64.9	1062.8		
Oct-98	72.2	1135.0		
Nov-98	54.0	1189.0		

NRL Contract N00014-97-C-2033

12-Bit, 213 Msps Analog-to-Digital Converter

ADC Block Diagram:



Features:

- Monolithic ADC implemented in TRW advanced GaAs HBT technology
- Error-Corrected Subranging Feedback architecture
- Static calibration circuitry implemented using low cost COTS parts
- Resolution: 12 bits
- Max. Sample Rate: 213 Msps
- SNR:50 dB (Pclip - 12 dB)
  (130 MHz < fin < 190 MHz)
- SFDR: 62 dB (Pclip - 12 dB)
- Power: 5 watts
- Size:6" x 6" (prototype pcb (1Q99)
  2" x 2" MCM (1Q00)

Figure 1. 12-Bit ADC Overview.

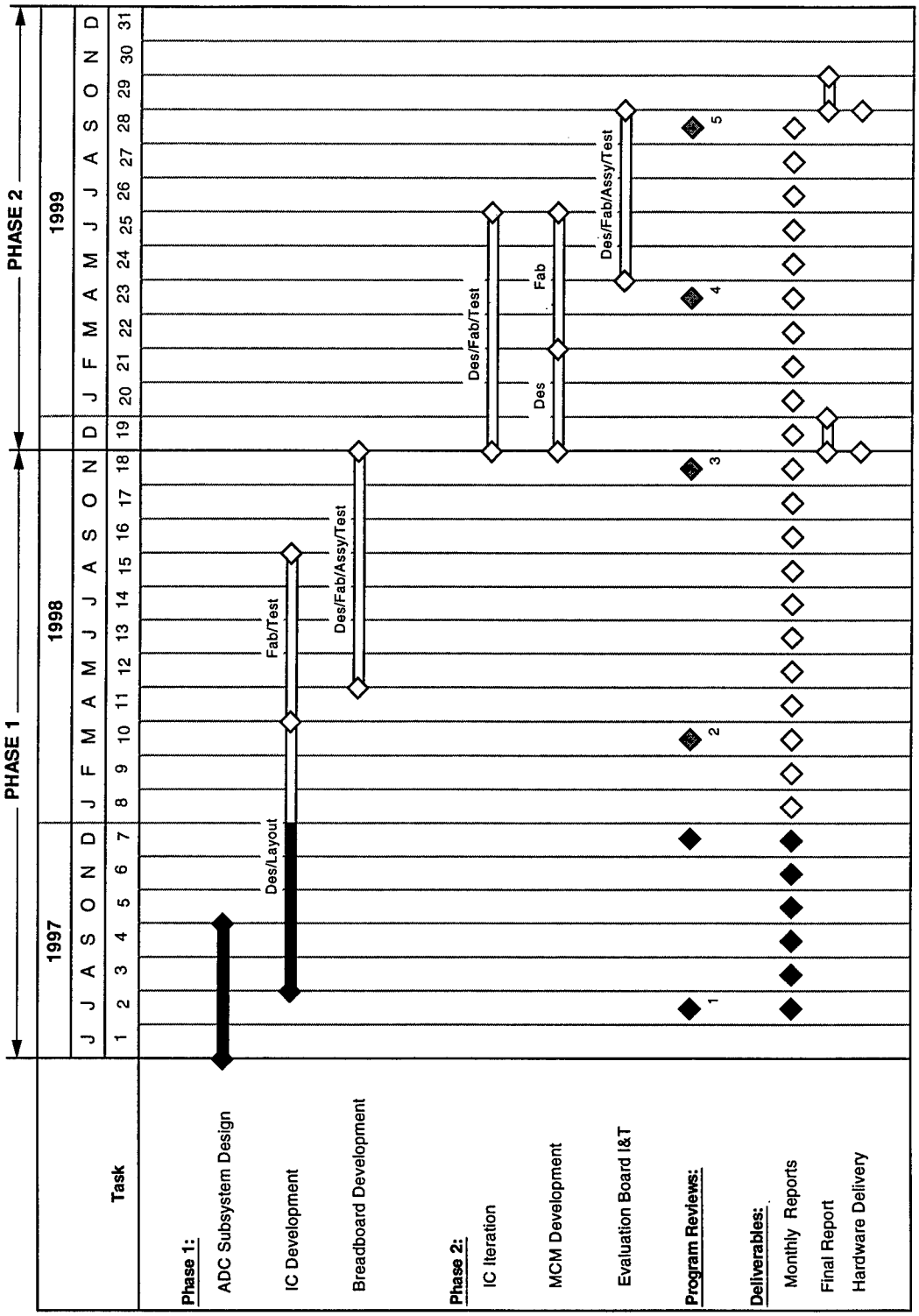
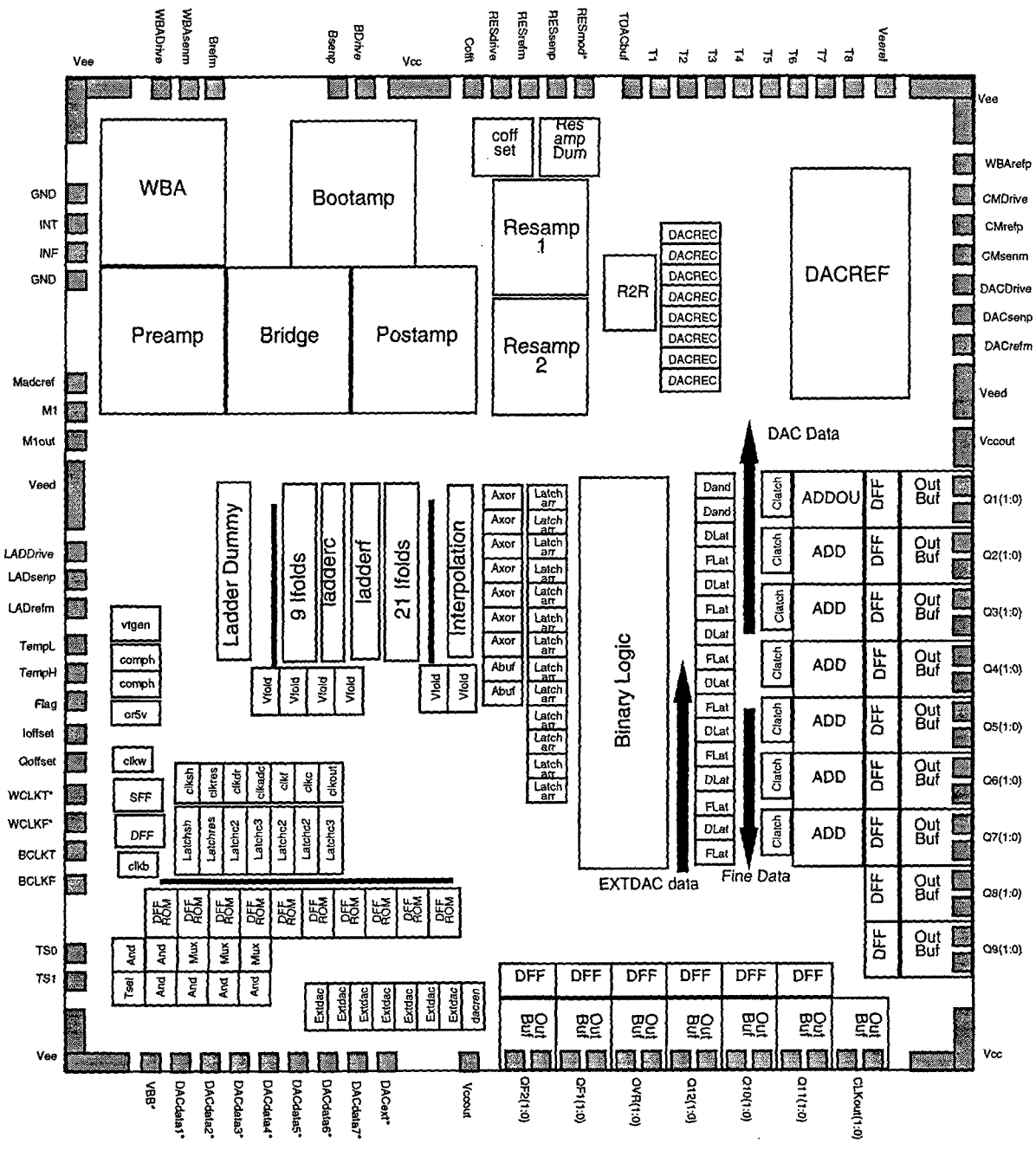


Figure 2. 12-Bit ADC Development Schedule.



Chip Size X=4.9mm, Y=5.28mm

Figure 3. 12-Bit ADC Chip Preliminary Layout Floorplan.

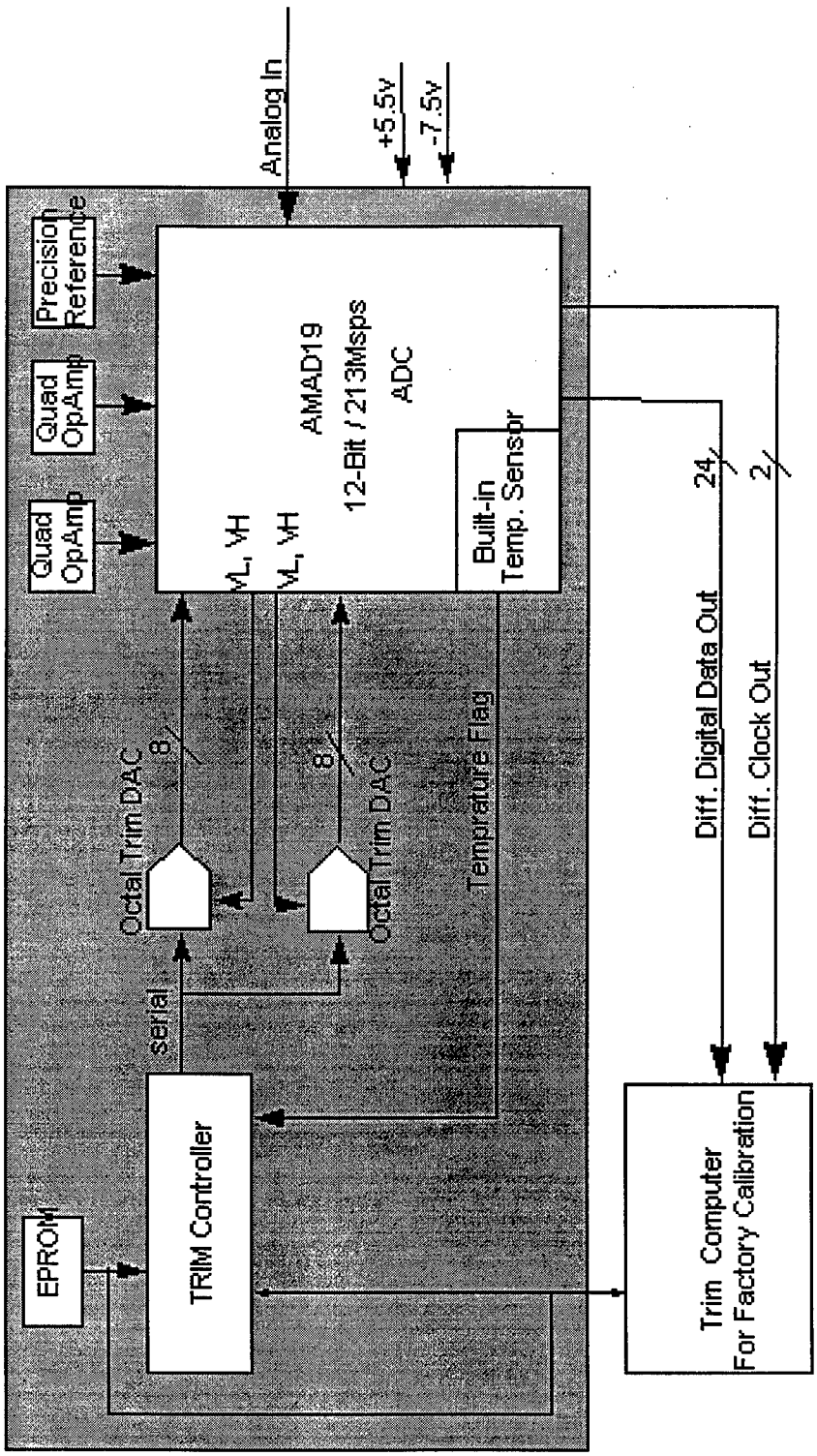


Figure 4. 12-Bit Calibration Subsystem Block Diagram.

Parameter	Requirement	Capability	Units	Comment
General				
Sample Rate	213	250	Msps	
Resolution	12	12	Bits	
Coding	Offset Binary	Offset Binary	Offset Binary	
Clock	1704	2000	MHz	8X (TBD)
Calibration				Factory Cal
Cal Update Duration	1.0	0.1	msec	Performance is degraded temporarily when cal logic senses temp change
Analog Input				
Clip Level		4	dBm	(= Pclip)
Gain		244	µV/Q	Input referred Q-step
Initial Gain Tolerance		TBD	dB	
Gain Variation		TBD	dB	
Signal Frequency				
min	130	5	MHz	BW=60 MHz IFc=160 MHz
max	190	250	MHz	
Input Offset		20	+/- LSBs	
Input Resistance		50	Ohms	Internal Termination
Input Capacitance		<5	pF	
Overload Voltage	TBD	20	dBm	
Recovery Time	100	20	nsec	
AC Performance				
SNR				
P clip - 0.5dB	50	57	dB	
P clip - 12dB	50	50	dB	SNR rolls off classically at 1dB/dB of input power
SFDR				
P clip - 0.5dB	50	60	dB	
P clip - 12dB	50	62	dB	
Gain Flatness	1.0	0.5	dB pp	fin=130 to 190 MHz

Figure 5. 12-Bit ADC Requirements versus Capabilities.

Parameter	Requirement	Capability	Units	Comment
Inputs				
Conversion Clock	Single Ended sine wave	Single End sine wave		AC-coupled
Frequency	1704	2000	MHz	8X (TBD)
Duty cycle				
min		40	%	
max		60	%	
Input Power		0 +/- 2	dBm	
Termination		50	Ohm	
Data				
Data Interface	LVDS -compatible	LVDS -compatible		(Diff. CMOS)
Data Rate	213	250	Msps	
Output Clock	same	same		
Overrange Bit	same	same		Electrically identical to data and clock. Indicates input has exceeded range
Data to Clock skew				
min	TBD	-100	psec	Variation in clock-to-data delay
max	TBD	100	psec	
V swing				
min	250	250	mV	Into 100 Ohm load
max	400	400	mV	
V common mode				
min	0	1000	mV	Nominal Vcm = 1.2V
max	2400	1400	mV	
Power				
Vee		-7.5	V	
Iee		557	mA	(TBD)
Vcc		5.5	V	
Icc		243	mA	(TBD)
Supply Tolerance		+/- 5	%	
Power	6	5.5	W	
Max Ripple		5	mVrms	
Temperature (ambient)				Performance Range
min	0	-15	C	
max	+70	+85	C	

Figure 5. 12-Bit ADC Requirements versus Capabilities (continued).